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TREBALL FINAL DE GRAU

TÍTOL DEL TFG: Telecommunications system of a CubeSat satellite.

TITULACIÓ: Grau en Enginyeria d'Aeronavegació

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Resum

Aquest Treball Final de Grau es dóna sota el programa UPC-Canadà, el qual l'autor realitza el seu últim any de grau a Mont-real, Canadà, a l'escola Polytechnique de Mont-real, sota la tutela del Dr. Giovanni formant part del seu laboratori Mistlab i alhora formant part del grup d'estudiants Polyorbite.

Polyorbite consta d'una organització que participa en l'esdeveniment bianual CSDC (Canadian Satellite Design Challenge) que consta de la realització partint de zero d'un CubeSat de mida 3U per part d'estudiants de grau i de postgrau.

En l'inici d'aquest treball al Setembre del 2015, el concurs es trobava just enmig de la iteració 2014-2016 sense tenir absolutament res realitzat per part del subgrup de telecomunicacions, tenint així tan sols 2 semestres per a dissenyar, construir i provar un sistema de telecomunicacions sencer, adient pel propòsit satèl·lit, fins al Juny del 2016 en el que es realitzaven les presentacions finals del concurs a Ottawa.

El propòsit d'aquest treball és doncs, el de dissenyar un sistema de telecomunicacions per a un satèl·lit CubeSat.

Title: Telecommunications system of a CubeSat satellite

Author: Roger Cano Marí

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Date: April 29th 2016

Overview

This Final degree's thesis is done under the UPC-Canadà program in which the author realizes his last degree year in Montréal, Canada, to the Polytechnique de Montréal university under the supervision of Dr. Giovanni Beltrame being part of his laboratory Mistlab and also on the Polyorbite group of students.

Polyorbite is an organization that participates in the biannual contest CSDC (Canadian Satellite Design Challenge) that consists on the realization from 0 of a 3U CubeSat by undergraduate and master students.

By the start of this thesis on September 2016, the contest was in the middle of the 2014-2016 iteration without having almost nothing on the telecommunication part, having just 2 semesters for design, build and test an entirely telecommunications system, suitable for the satellite purpose, until June 2016 in which the final presentations of the contest took place on Ottawa.

The purpose of this thesis is then an early design of a telecommunications system for a CubeSat satellite

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1. SYSTEM REQUIREMENTS

1.1. Missions

The CubeSat named Hathor is intended to realize two main missions. The first one consists on the study of a growing plant into space “space bean”, and the other involves an ionic engine capable of modify the orbit of the satellite “IonDrop”.

In order to obtain the data of the missions and to give orders to the satellite a communication system is mandatory between the satellite and the earth. The first question there has to be made before design it is “How much data it is required to exchange with the satellite?” And consecutively compute “how much time there are for send this data?”. From those parameters the type of modulation and speed is decided.

We need to know the quantity of bits to send and the bitrate (bits/s or bauds) that will allow to send the data in one pass.

1.2. Satellite orbit and time per pass

The satellite is expected to be placed into a LEO orbit. That means that his altitude can be from 200 to 2000 Km over the earth sea level. For Hathor an altitude between 600 and 800 Km is expected.

Any relatively little satellite or object orbiting a huge mass like the earth will have a linear speed determined by his altitude and type of orbit. Since we are expected to maintain always a constant altitude, the orbital speed will be also constant and given by the expression 2.1.

$$v_0 \approx \sqrt{\frac{GM}{r}}$$

Where $G = 6.674 \cdot 10^{-11} Nm^2/kg^2$ is the gravitational constant, $M = 5.97219 \cdot 10^{24} Kg$ is the mass of Earth and r the radius orbit taking into account that it is the altitude plus the radius of Earth.
Taking into account the fastest case of our CubeSat will occur at the lowest altitude of 600Km, the orbit velocity and its period is:

$$v_0 \approx 7557\ m/s = 7.557\ km/s$$

$$v_0 \approx \frac{2\pi r}{T} \rightarrow T \approx 5801.18\ s = 1h\ 36\,\text{min}\ 46s$$

In order to obtain the time per pass over a determined point on the earth situated just under the orbit we can take use of the sinus theorem and Pythagoras theorem used on Fig. 1.1.

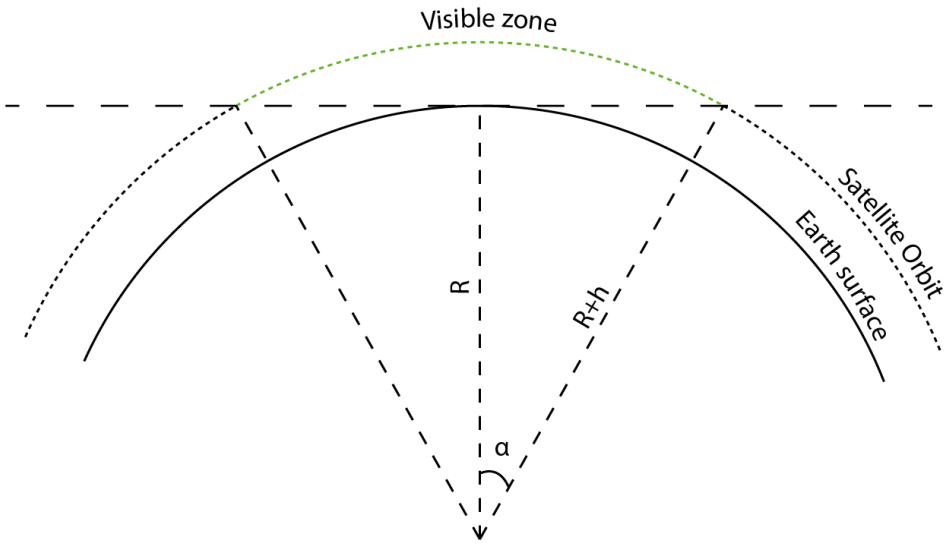

Fig. 1.1 Time per pass scheme computation

$$(R+h)\cos \propto = R$$

$$\propto = \cos^{-1}\left(\frac{R}{R+h}\right) = 23.947º$$

$$5801.18\frac{s}{\cancel{orbit}} \cdot \frac{1\ \cancel{orbit}}{360º} \cdot \frac{2 \cdot 23.947º}{1\ \cancel{pass}} = 771.803\frac{s}{pass} = 12\ \text{min}\ 51s\ per\ pass$$

This let us almost 13 minutes with the satellite visible. In reality is almost impossible to be at an exact point under the orbit. Also the earth surface is not flat while the most probably is that there will be mountains or buildings that hide us part of the horizon.
Re-computing the time per pass of a theoretically scenario which the physical horizon is 5º over the normal horizon we obtain from the figure 1.1 $\propto = 19.43º$ and then

$$t = 626.27\ \text{s/pass} = \ 10\ \text{min}\ 26\ \text{s per pass}$$

So we will assume this time per pass in order to assure the radio link in this restricted condition. The distance between the satellite and the ground station at 5º will be the maximum one being 2370 Km.

1.3. Doppler effect

Known the velocity of the satellite and the apparent velocity at an elevation of 5º (that will be the maximum of the whole pass) we can easily compute the electromagnetic Doppler Effect of the signals. This is needed for computations later.

The apparent speed of the satellite at 5º elevation is given by

$$v_a = v \cdot \cos(\alpha' + 5º) = 6880.4\ m/s$$

Given the Electromagnetic Doppler Effect formula:

$$f' = \gamma \frac{c+v}{c} f \qquad \gamma = \frac{1}{\sqrt{1-\frac{v^2}{c^2}}}$$

At the frequency that the satellite will work, 437 MHz, we have:

$$\nabla f_{DL} = f' - f = \pm 10{,}022\ kHz$$

1.4. Data Budget

The amount of data to be send is obtained from the other members that works on the missions. This data budget is resumed on the next excel tables:

During plant mission					
Telemetry		Bits per measurement	Freq.	Bits per orbit	Bits per day
Euler angle	ACDS	32	2	1440	23040
CO2 sensor	Payloads	8	10	72	1152
02 sensor		8	10	72	1152
Barometer		32	10	288	4608
Hygrometer		8	10	78	1152
Temperature		16	10	144	2304
Volt sensor trust		32	60	48	768
I sensor		32	60	48	768
V sensor radiators		16	2	720	11520
Volt sensor	Power	32	1	2880	46080
Voltsensor		32	2	1440	23040
sub total					**115584**
Bytes conversion					14448

During ionic thruster mission					
Telemetry		Bits per measurement	frequency	Bits per orbit	Bits per day
Euler angle	ACDS	32	2	1440	23040
CO2 sensor	Payloads	0	inf	72	0
02 sensor		0	inf	72	0
Barometer		0	inf	288	0
Hygrometer		0	inf	78	0
Temperature		16	inf	144	0
Volt sensor trust		32	0,2	14400	230400
I sensor		32	0,2	14400	230400
V sensor radiators		16	2	720	11520
Volt sensor	Power	32	1	2880	46080
Volt sensor		32	2	1440	23040
sub total					**564480**
Bytes conversion					70560

Two different amounts of data are expected depending on the mission that is

taking place into the satellite. We can consider that both missions will not take place at time, so the biggest one is during the ionic thruster mission, where every day about 565 Kbits has to be send to earth.

1.5. Speed transmission

Although there is assumed 2-3 passes per day from the previous report made on Polyorbite, we assume that we will recollect the data just once a day. So in order to send 565 kbits in 10 minutes it is need a link of minimum 941 bauds (bits/s).

The data but will not be send directly. A protocol must be implemented into the transceivers in order to success with the transference. This protocol will divide the data into packets and add to each one a header that contains information about it, methods of determining if the packet is corrupt, etc. This protocol will make increase the total amount of data about a % depending on the configuration.

This % is chose to be around 7%. So the real amount of data per day will be 604 Kb. That means a minimum speed of 1006 bauds.[1]

Taking into account but that:

- It is wanted the interaction with the satellite sending orders.
- Make the first contact with the satellite while rising the horizon will need some time.
- The antennas have to be oriented actively to the satellite

It is evident that the useful link cannot be considered with such amount of minutes.

It needs to be faster enough to try almost 2 or 3 times the data downloading taking into account the possible errors that can occur. This speed or bitrate in a communication system is given mostly by the type of digital modulation employed. Some are explained on the Annex A chapter 2. Giving examples: code Morse, CW can have a speed of about 20WPM (words per minute) in order to be possible to decode by human ear. This is insufficient for our data budget.

AFSK or Audio Frequency Shift Keying is widely used by radio amateurs for its simplicity to use with just a computer and an audio transceiver. It can reach up to 1200 bauds, marginally enough for download the daily data.

Other types like PSK, FSK, ASK and their extensions BPSK, 4FSK, GFSK, GMSK… can reach speeds from 1200 bauds to 154 kbauds and more. And we will be focused on one of those.

[1] Selected aleatory to not cause much load as it can be designed with any specifications.

2. Link study

In order to achieve a bitrate with the choose modulation successfully it is necessary to accomplish a certain BER value at the input of each transceiver from the satellite and the base station. BER stands for Bit error rate and is computed in terms of the ratio of power of received data over power of noise and speed transmission.

For compute that we firstly need to define the frequencies that we are going to work for the uplink and downlink the power of each transceiver and loses.

2.1. Frequencies

As the CSDC-0080 constraint imposed by the CSDC express, the satellite has to comply with the ITU regulations. Used frequencies have to be those authorized by ITU for an amateur service.

Regarding the most used in CubeSat satellites it is widely used the VHF and UHF bands due to the need of small and low cost transmitter and receiver.

ITU regulations allows amateur satellite service into those two bands between the frequencies: 144.000 MHz - 146.000 MHz for the VHF 2m band, and 435.000 MHz - 438.000 MHz for the UHF 70cm band.[2]

This project started assuming the use of both bands as it is usually on other CubeSats for a full duplex link, being possible transmitting and receiving data at the same time. But lately, due to hardware restrictions and complexity of the system, it is designed a half-duplex transceiver that works in just one frequency band.

For the study we will employ the middle frequency of the 70cm band: 437MHz.

Theoretically it is better used the one band less power demanding for the satellite. This can be seen into the basic next radio link formula which f_o is the working frequency and the result P_r is the received power that depends also on the transmitted power, the range and the antenna gains.

$$P_r = \frac{P_t G_t G_r c^2}{(4\pi)^2 R^2 f_0^2}$$

If we maintain the Range, gains and transmitted power constant we can see that the link one which higher frequency will receive much less power as the frequency is dividing elevated to square. So for the system the use of 145MHz would assure a better received power signal against the 437MHz. But again, due to limitations on the hardware part, 145MHz it is too low or at the boundary to implement it.

$$f_{uplink} = f_{UL} = f_{downlink} = f_{DL} = 436.5MHz$$

[2] https://en.wikipedia.org/wiki/Amateur_radio_frequency_allocations#10_Metres

3. System design introduction

3.1. Main view

The main purpose of the communication subsystem is to have an exchange of data between the GS and the Satellite. In a hardware point of view what it is needed here is a connection between two users. This is achieved with a link between those two and can be wired or wireless. What the users sees is represented on Fig. 3.1, which is equivalent to the wireless format in Fig. 3.2 that has exactly the same behavior from the point of view of the users.

Fig. 3.1 User point of view

Fig. 3.2 Electrical engineer point of view

The objective of this project is to design the red square marked on the figure, in other words make an interface between two hardware components such as a PC at the ground station and the OBC (On board Computer) of the CubeSat.

The digital binary data coming from the users to the communications system has to be adapted into a properly format in order to be send through the air and then once received by the other side it has to be reconverted to the original format. This adaptation or conversion is called modulation and there exists lots of different modulations depending on the final purpose.

These modulated signals cannot be send at baseband frequencies. Those has to be raised to the operative band such as 145 MHz or 437 MHz for our case using an upconverter and a downconverter when receiving.

Is important also to determine a way that ensures detect possible errors occurred on transmissions. Corrupt input messages to the satellite can cause fatal errors and cannot be allowed.

3.2. Main link system - General conception

After research previous CubeSat's COMM systems employed and related Master's projects it can be made a general conception of the system. We can divide it into some parts such as:

- **Antennas**: Receives or transmits the RF signal.

- **Amplifiers and filters**: That amplifies and processes the RF signal.
- **Radio**: Converts analog high frequency RF signals to analog low frequency signals and vice versa.
- **Digital Modem**: Modulates the binary digital data coming from the microprocessor to a low frequency signal and vice versa.
- **Microprocessor / µC**: Intercommunicates between the modem and the OBC of the satellite or the PC at GS.

Those are expressed into an example shown by the Fig. 3.3.

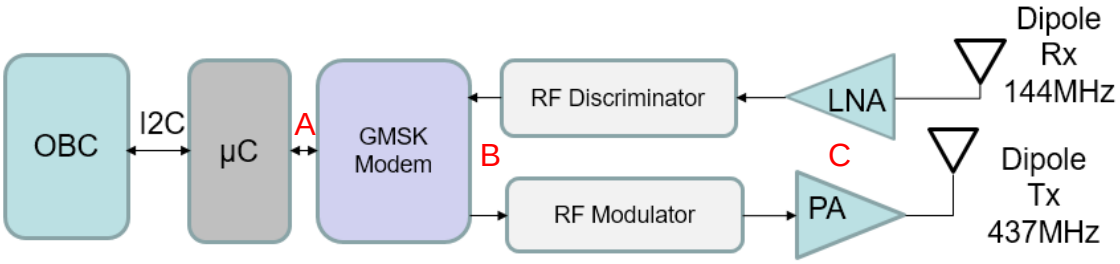

Fig. 3.3 General conception: Parts of a typical RF system.

Where the represented red letters on each link expresses the next data type:

A- Binary digital data to transmit and Control Bus.
B- Low frequency digital modulated (GMSK) data into frames.
C- High frequency digital modulated RF signal.

In this case I2C is the interface protocol used for the commands between the OBC and the microprocessor.

This scheme can vary depending on the type of hardware components. There are three different designs for the system:

- The first is a unique chip that manages the roles of modem and radio. Chips like CC1100 from Texas instruments, ADF7020 from Analog Devices, nRF903 from Nordic Semiconductors or SI446x from SiLabs are examples of fully integrated solution. The last one mentioned is the final one employed in this thesis.
- The second one is to use discrete components for the signal processing. Which is mainly used for explain in theory a transceiver, but not practical or too complex.
- The third one is a semi-integrated design consisting on using a modem and radio chips separately.

3.2.1. First version designed

The first version of the designed system during this thesis was a Third type, based on the Master Thesis “Study of a 145 MHz Transceiver” made by Roger Birkeland of the Norwegian University of Science and Technology the 2007 that contains a

wide study of the implementation of the GMSK modem chip CMX909B from CML circuits with some other analogical Radio components like SA606 receiver suitable for a CubeSat.

CMX909B was expected to reach 38.4kbits/sec on Rx and Tx. Also includes FEC and CRC encoding besides on interleaving and MOBITEX encapsulation.

Once analyzed this thesis there was found lot of misunderstanding and not really precise information and errors that would make the system not working as computations on the noise levels received for the satellite case at 9600 baud speed. Some modifications and further analysis were made for adapt it to our desired product, but failed in front of some practical limitations like the precision of oscillators or real radio sensibility.

In the same thesis, it is concluded that the system is not working properly nor there exists any amplifier capable of provide the sufficient amount of power, which is false, misunderstanding the efficiency of an amplifier as the relation between the real output power and the output power expressed on datasheets.

The redacted report part concerning the V1 design is allocated on the chapter 3 of the Annexes.

3.2.2. Second version designed

After the failure of the first version, analyzing products of the same CML circuits website, it was found more integrated solutions standing for a Third/First type where:

- CMX7164 digital chip modem modulates the binary data to GMSK.
- CMX994 and CMX998 chips acts as a Transceiver and Receiver up and down-converting the GMSK signal to the required frequency.

Although they provide an evaluation board named DE9941 that combines all those chips in a really similar integrated system that complies with our requirements, including the designs, components list and gerbers of the same board, CML circuits refused to provide me the extended datasheet of each chip which was necessary for their programming due to “too much complexity for an undergraduate student”. Also the chips are only available for big commands, oriented to big companies.

3.2.3. Third version designed

After the failure of the second version, and having just 6 months ahead, it was decided to design a system based on just components available in stock in the Digikey distributor website. With this, some different First type systems where studied, like the Texas Instruments CC1100 chips or the SiLabs Si446x.

Both acts as a unique chip that includes different digital modulations, speeds, and integrated up and down-conversion from 140MHz to 1GHz, being able to transmit and receive but in a half-duplex way (not at the same time).

The CC1100 and variants are widely used in previous CubeSats but knowing that is a bit deaf, failing in half of the missions. That's why it was selected the SiLabs Si446x. In this way a new telecommunications system not really explored for space solutions would be studied.

This version is accurately studied on chapter 4.

As a note regarding the figure 3.3, this final version has no Microcontroller included for the main link. The Si4460 chip is controlled directly via SPI by the main Onboard Computer with the possibility of simple operation in which RAW data is transmitted and received by the GPIOs input and output pins. Also more complex operation with data headers and scrambling can be used via SPI.

3.3. Beacon system – General conception

Apart of the Main link, it is highly recommended to include an auxiliary telecommunication system that provides basic telemetry and Satellite status via Morse code.

This is useful for multiple reasons. One of them is to know in the case in which the main link is not responding, the status of the main computer of the satellite ("Dead", "Alive"). Another is to rapidly knowing the voltages for example of different sections of the satellite that would be useful for troubleshooting in the case of failure once deployed in space.

Another reason is to have an audible indication useful in the moment when the Ground Station operator is waiting for its contact. Having a simple audio receiver at the beacon frequency connected to the main antenna at ground will provide an easy audible reference in which then it can be started the main link operation.

This auxiliary system unlike the main link system, has to be redundant form the main computer of the satellite. In order to accomplish that, a microcontroller (MCU) has to be used.

For simplicity the same MCU employed on Arduino boards (Atmega328P) is used to create the Morse signal with ordinary data messages from the main computer using I2C. This Morse signal consists just in a digital signal (high-low) that indicates when tone or silence has to be sent. Then a simple ASK modulator chip converts it to a tone at a frequency given by a provided oscillator. Finally, is amplified and sent to the Beacon monopole antenna of the satellite.

More accurate information about the matching circuits and chips is explained on chapter 5.

4. System design – Main Link

4.1. Introduction – Si4460

The employed chip for the third and final version of the system is based on one model of the Si446x Low Current Transceivers, a Silicon Labs product.

Si4460 consists on a single chip capable of receive and transmit digital data into a frequency range between 142 MHz to 1050 MHz, using (G)FSK, 4(G)FSK and OOK modulations within a maximum output power of +13 dBm and a sensibility of -124 dBm. It includes a fully programmable Local Oscillator capable of have 28.6 Hz of maximum accuracy step on the working frequency.

It can be seen that Si4460 is the less powerful transceiver, being Si4463 the most with about +20 dBm output. The reason of choose the less one is due to the added Power Amplifier on the transmission line and will be discussed in detail later.

The chip consists on a 20-pin QFN package, a really little one with dimensions 4 x 4 x 0.85 mm.

It is linked with the main board computer with SPI protocol and it has 4 GPIOs lines that can be used for multiple purposes including input or output of RAW data.

Silicon Labs provide on its web plenty of application notes and datasheets of this product including the designs of their different evaluation boards.

The main job concerning the hardware part of the transceiver leads to the design of the matching circuits between chips and antenna. That is fully explained on their application notes and resumed in next section 4.2.

4.2. Matching circuits

Si4460 is capable of being used with two different match topologies, Class-E and switched-current for the transmission.

The type of amplifier that is included on the chip is called a switching amplifier, which consist basically on a switch (or multiple switches named legs) that creates an amplified squared signal from an original analogic signal, that then is passed through a low pass filter to have the sine signal.

Switching amplifiers are really efficient since in reality they do not amplify but creates a new similar signal. The implementation of this kind of amplifier is using a type of matching circuit that is fully explained on the SiLabs application note AN627.

Into it can be seen different methods of connecting the receiver and transmission. It can be employed using just one antenna for both uplink and downlink plus a Switch, one antenna but in direct Tie or in split-mode using two antennas.

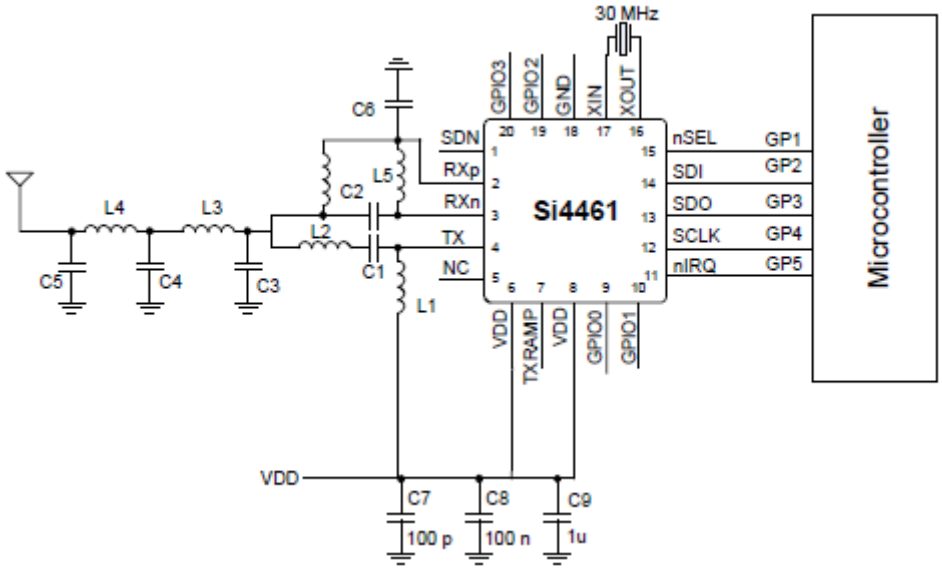

Fig. 4.1 Si4461 Direct-Tie Application example[3]

Due to the losses that a Switch would provide to the system, a split type is chosen. That means, using two antennas, one for transmitting and other for receiving with two different circuits not being connected between them.

The external circuitry of the transceiver can be resumed in 4 parts. The transmitter (TX) and receiver (RX) circuits that has to match the different impedances of the antennas and transceiver and filters; the alimentation circuit which includes coupling filters and the crystal which provides the required resonance to make the internal oscillator of the transceiver work.

Both RX and TX matching circuits and components values are computed in sections 4.2.1 and 4.2.2.

4.2.1. RX Matching

From the Application Note AN643 for Split topology it is used a Four-Element Match Network as showed on Fig. 4.2Fig. 4.3.

[3] Scheme obtained from Silabs Si4463-61-60-C datasheet, page 15, available on Annex C.

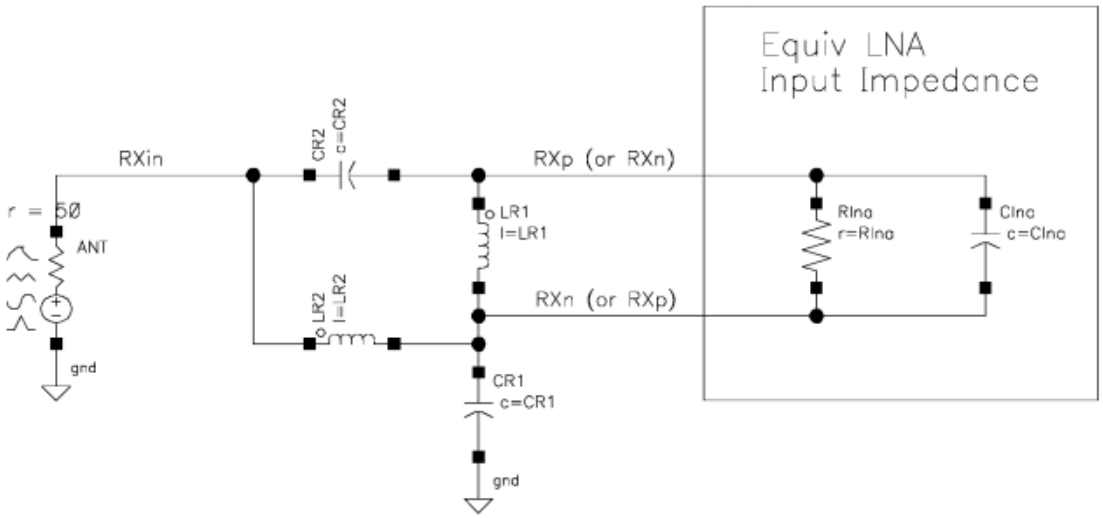

Fig. 4.2 Four-Element Match Network.[4]

R_{lna} and C_{lna} is given by tables in the application note AN643 that depends on the frequency. We can interpolate for 436.5 MHz those are R_{lna} = 478 Ω and C_{lna} = 0.976 pF.

The rest of components are computed with the given formulas from AN643:

$LR2 = \frac{\sqrt{Re(Z_{ANT}) \times R_{LNA}}}{\omega_{RF}} = \frac{\sqrt{50\Omega \times R_{LNA}}}{\omega_{RF}}$	$CR2 = \frac{1}{(\omega_{RF})^2 LR2}$	$CR1 = 2 \times CR2$
$L_{LNA} = \frac{1}{(\omega_{RF})^2 C_{LNA}}$	$L_M = 2 \times LR2$	$LR1 = \frac{L_{LNA} L_M}{L_{LNA} + L_M}$

For 436.5 MHz it is obtained the values from table on Fig. 4.3.

Component	Obtained value	Real component value
LR1	61.68 nH	62 nH
LR2	56.368 nH	56 nH
CR1	4.717 pF	4.7 pF
CR2	2.358 pF	2.2 pF

Fig. 4.3 RX Matching component values

4.2.2. TX Matching

Application Note AN627 states for a Split TX/RX the topology showed on figure Fig. 4.4. Its purpose is to match the impedance of the TX_Pin of the transceiver to the antenna and to operate the in-build Switching Amplifier.

[4] Scheme obtained from the same Silabs Application note AN643, available on Annex C.

Due to the operation of a Switching Amplifier, it is needed alimentation directly to the line, as we can see VDD trough R_{dc} resistance and L_{choke}.

Due to the type of operation as stated on the application note, R_{dc} is not used. Its function is to limit the output power of the transmitter. Instead of use this resistor, it will be used the parameter PA_PWR_LVL of the transceiver, that defines the number of legs (switches) of the amplifier. This parameter is computed later on section 4.2.3.

The other components are computed by the next resumed steps:

1. L_{choke}, which consists on a pull-up inductor will just act as a high pass filter between the VDD and the TX_Pin. For 470MHz is stated approximately **Lchoke = 220nH**.

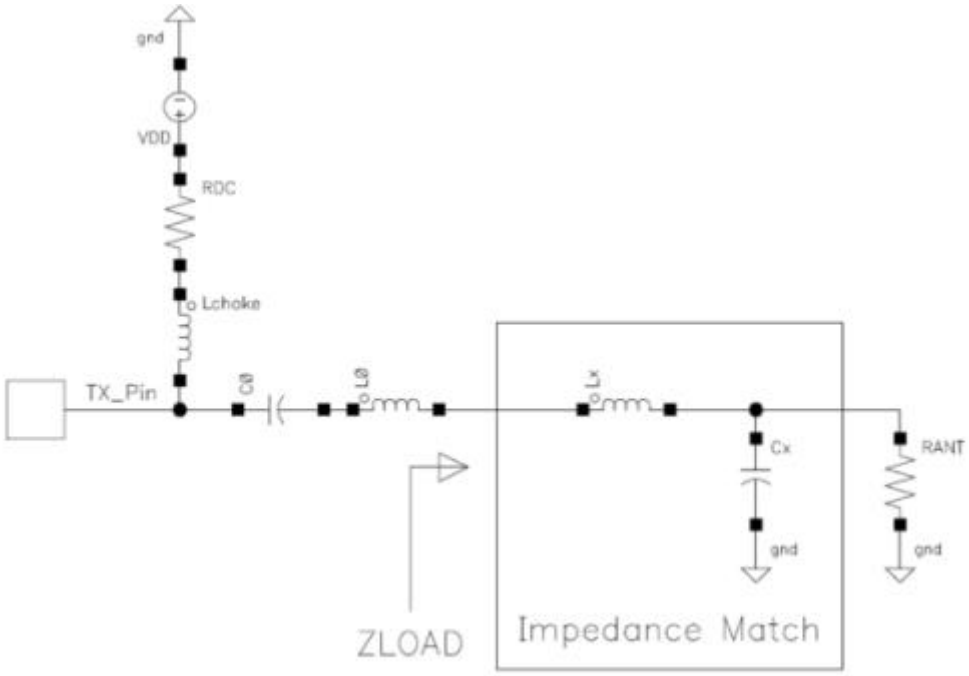

Fig. 4.4 Impedance Match to transform Rant to Z_{load}.[5]

2. C0-L0 Series-Resonant Tank, are two components that with the properly values, will resonate at the wanted operation frequency. It is other requirement of the Switching Amplifier and there exists infinite possibilities of values for one frequency. In practice, it is decided **C=8.3pF** and **L=16nH** which will provide resonance at 436.5MHz.

[5] Scheme obtained from the same Silabs Application note AN627, available on Annex C.

3. Z_{load}, is the output impedance of the TX_pin. As the external Power Amplifier to be used will operate at 50Ω, we will need an impedance matching circuit. The value of Z_{load} is computed with the provided formula:

$$Z_{LOAD(fund)} = \left(\frac{0.2815}{\omega_0 C_{SHUNT}}\right) e^{j \times 49.0524°}$$

Where C_{shunt} for Si4460 is 1.25 pF and $\omega_0 = 2\pi f$, where f = 436.5 MHz.
Z_{load} = 53.813 + j62.019 Ω

4. Matching Lx-Cx, will adapt the Zin = 50 Ω of the external Power Amplifier to Zload of our transceiver. The values are **Lx=22.6nH** and **Cx=0.2 pF**, being the capacitor in parallel first nearer to the TX_Pin and then Lx in series.

The next step in the Application Note is to design the Low Pass filter, in our case but, it will be done after study the external Power Amplifier employed.

4.2.3. Sky65116 Power Amplifier

Given the fact that it is needed about 32 - 33 dBm (1.5W – 2W) of emitted power as showed on the data budget of section 1.6 of the annex, an additional Power Amplifier has to be selected as the more powerful transceiver Si4463 just gives 20 dBm of maximum power.

RF Amplifiers has two basic parameters: Gain and Output Power. A properly Amplifier has to be selected that provides the required output power, and then it has to be adjusted its input power (that is the output power of the transceiver) depending of its Gain.

Using a component searcher like everythingRF.com it was found two suitable amplifiers. The first, RF5110G designed for operate from 800 MHz to 950 MHz but it is shown that provides successful results also on 437 MHz, it is a typical solution used on several CubeSats and similar designs. It has 32dBm of output power, which given the fact that its matching will be not perfect, is at the limit of our requirements.

The other solution used in this thesis is the SKY65116 Power Amplifier from Skyworks. This amplifier consists on a single chip that already includes matching to 50Ω (RF5110G has not) and an output of 34.5 dBm which is more than enough.

It has a Gain of 35 dB, and a pretty high consumption needing 1.5A at 3.6V while transmitting.

It was designed an evaluation board for this Amplifier that would convert the needed 3.6V from 5V with a regulator for testing purposes, as there are limited tests available online of the chip. The design is showed on figure Fig. 4.5.

Even the Gerbers of a PCB of about 10 x 10 cm were designed with ADS software with coplanar waveguides, and the components were bought on Digikey.

Due to the high cost of printing such a PCB it was not possible to make it.

Polygrammes, a group on Polythechinque de Montréal, was the only group capable of reaching the required precision PCBs oriented to RF. They quoted about $320 (CAD) being not possible for the Polyorbite budget in just testing.

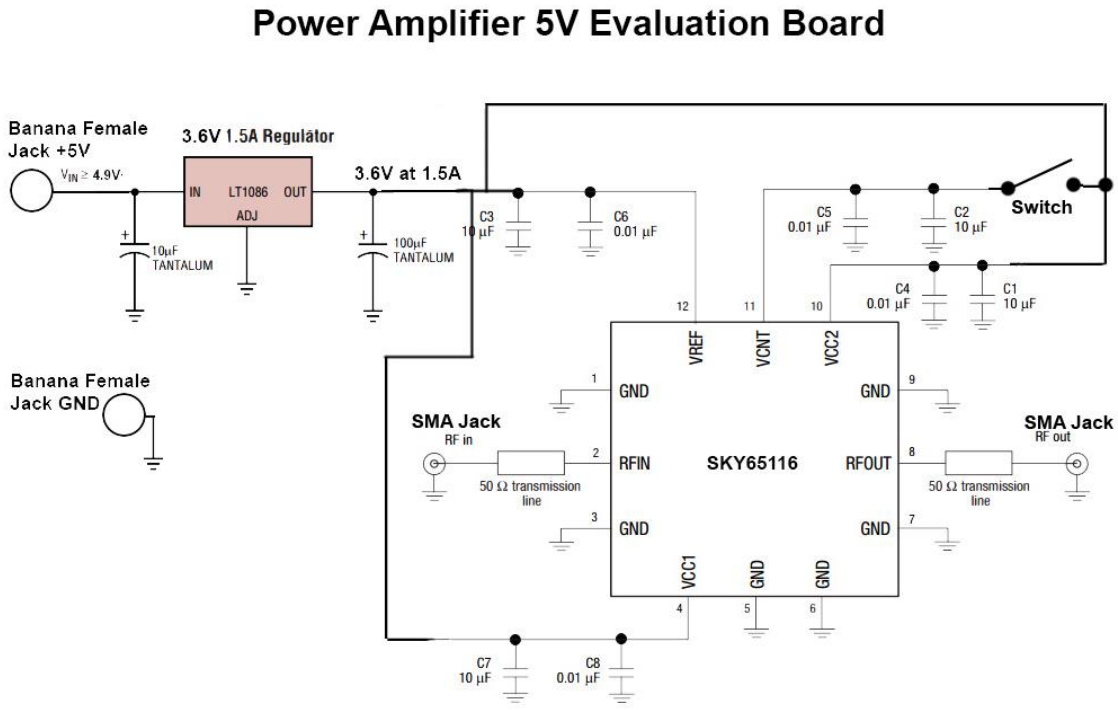

Fig. 4.5 Evaluation board designed for SKY65116 at 5V.

Given its gain of 35 dB and its P1dB of 34.5 dBm a properly input power has to be selected. As it can be seen, the input power must not exceed -0.5 dBm. For an operation at 32 dBm it has to be -3 dBm and this is controlled by the number of legs (switches) used on the on-chip switching amplifier of the transceiver. This number is controlled by the PA_PWR_LVL command, and given the graph from page 35 of its datasheet for si4463 it is obtained about less than 10. Our transceiver but is the Si4460 which has a maximum output power of +13 dBm and such as it can be deduced that the required output power of -3 dBm is achieved with less than active 30 legs.

4.2.4. LPF and final matching

The Low Pass Filter for the TX part is recommended in order to comply with standards attenuating harmonics in non-desired frequencies which falls out of the allowed Radio Amateur band.

Into the AN627 it is recommended a fifth-order low pass filter using the PI-topology. Given a Chebyshev filter with peak frequency on 436.5 MHz (that leads

a cut frequency of 442MHz) gives the values **LM = 18.5 nH**, **CM = 7.5 pF** and **CM2 = 15 pF.**

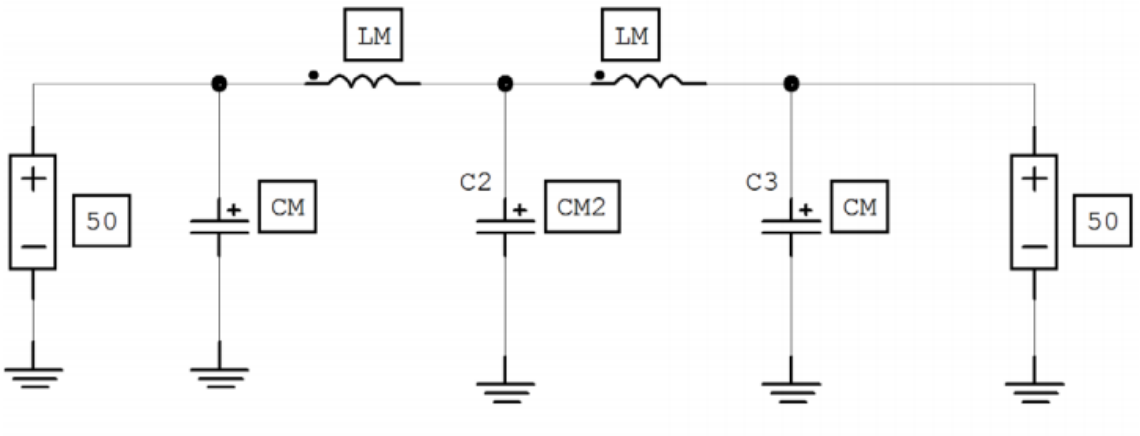

Fig. 4.6 5th-Orded Pi-Topology Low-Pass Filter

Simulation using RFSim99 software shows that for about 430 MHz gives the minimum losses (S21) to the signal. We can see on figure Fig. 4.8 that at 430 MHz it has almost S21 = 0 dB (no losses) and S11 = -87 dB (almost no reflections). That means, the LPF is optimized for working near our desired frequency of 436.5 MHz.

The simulation also shows that this LPF is useful for other frequencies up to 500 MHz, which will assure no bandwidth problems for its use in the 70cm band.

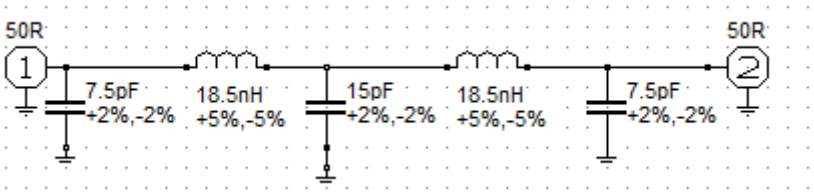

Fig. 4.7 LPF Scheme with the values in RFSim99

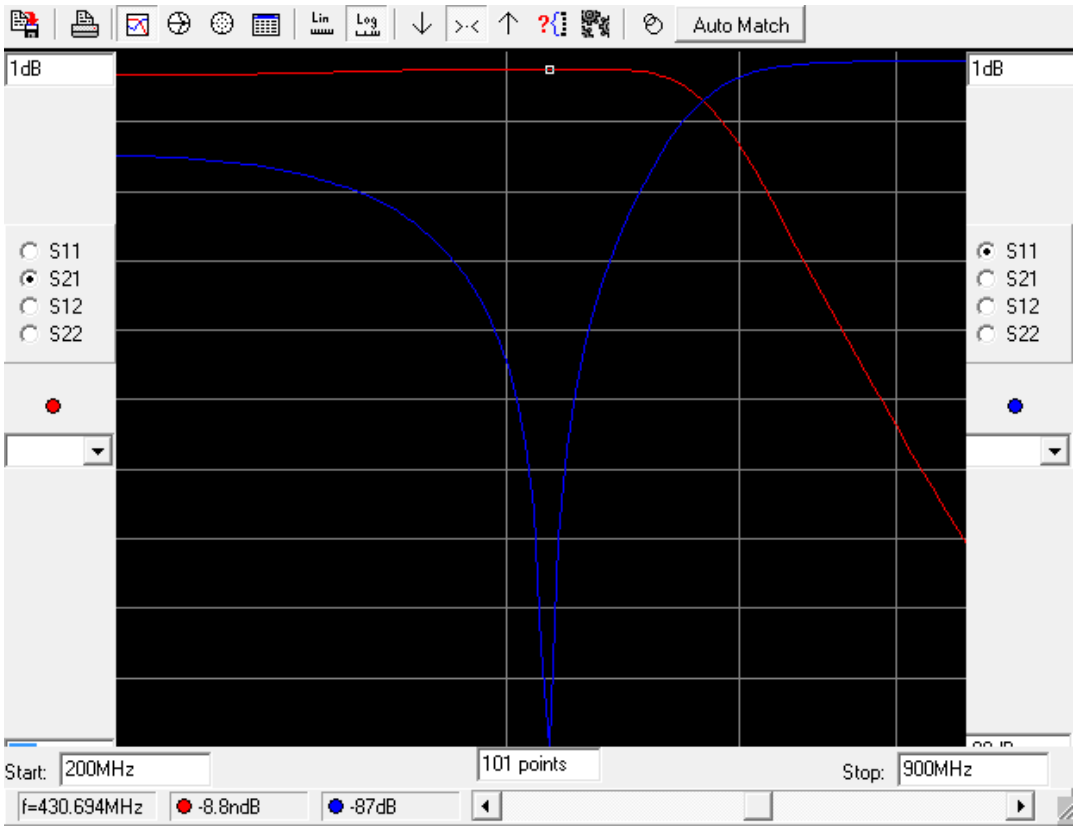

Fig. 4.8 LPF S21 and S11 results on RFSim99

The whole link including TX matching, SKY65116 Amplifier and LPF is done placing the Amplifier on the middle of the LPF.

In figure Fig. 4.9 it is expressed the whole TX circuit, from the Transceiver to the Antenna connector without simplifying.

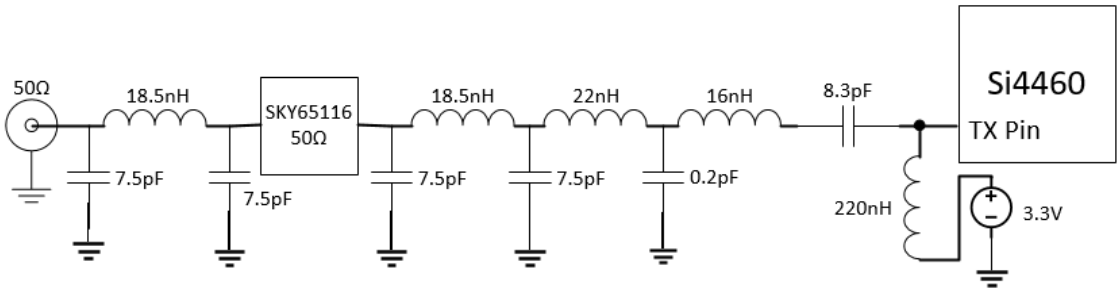

Fig. 4.9 TX circuit not optimized

Then as it can be seen some components can be summed placing the equivalent one. For example, when removing the 0.2pF capacitor. The final result is expressed in figure Fig. 4.10.

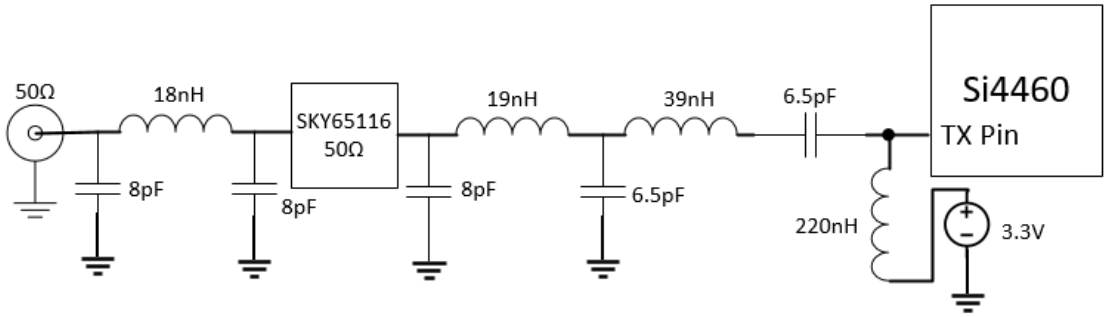

Fig. 4.10 TX circuit simplified

The modifications in the components of Fig. 4.10 are deduced when employed a Smith Chart. In figure Fig. 4.11 it is shown the impedance results of the simplified TX circuit using the Smith Chart utility of ADS software.

a. Being normalized for 50Ω and using the component values for 436.5MHz, starting from the center (Antenna connector - 50 Ω) the first pi-part of the LPF creates a “half-moon” path on the Smith Chart that finishes at the same middle point. That assures that the output and input of the amplifier which is matched at 50 Ω will work properly.

b. Then, the other pi-part of the LPF creates another loop, in which now finishes a bit separately from the middle (due to the 19nH inductance instead of the computed 18nH; and the 6.5pF capacitor instead of the 8pF) in order to pass over the wanted TX-Pin impedance (marked pink square).

c. Immediately, the 39nH capacitor will pass over this TX-Pin impedance and surpass it which thanks to the last 6.5pF capacitor conforms the Tank Circuit necessary to resonate at 436.5 MHz.

The network response of the same circuit is also expressed on Fig. 4.12. As it can be seen, it resonates over 436 MHz thanks to the tank circuit, and filtrates the rest. Note that the x axis of the figure expresses the response from 200 MHz to 600 MHz.

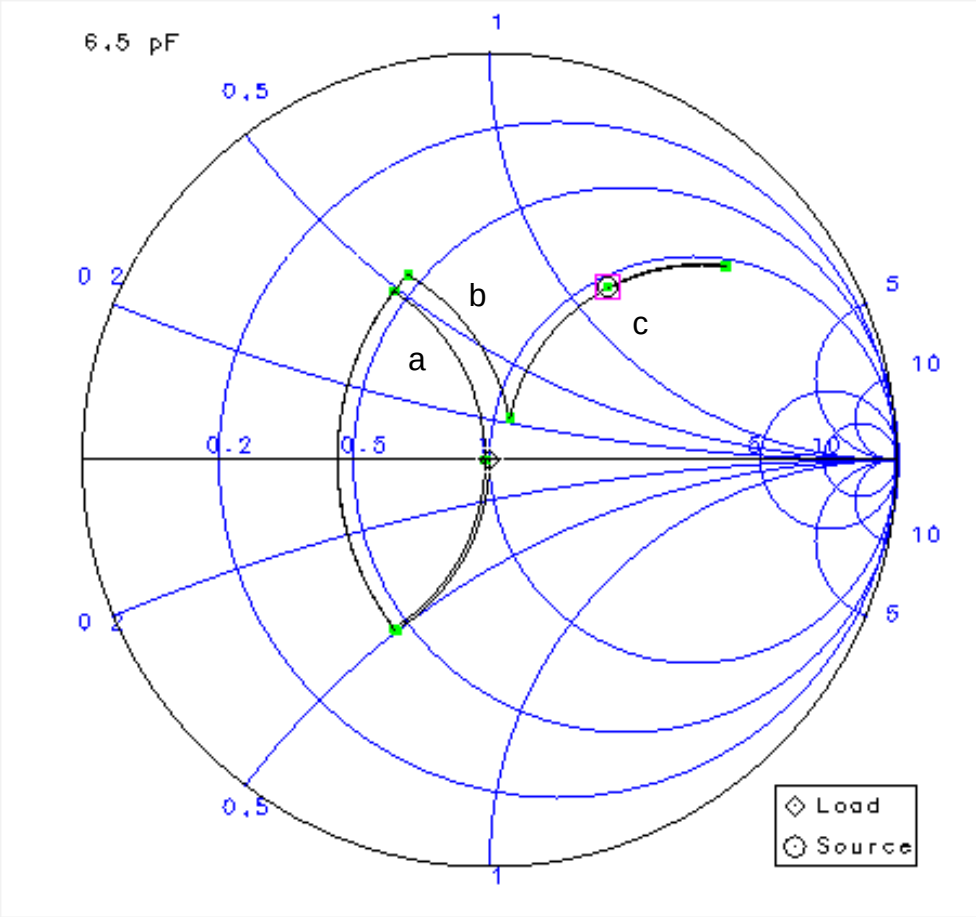

Fig. 4.11 Smith Chart of the TX circuit. Being the pink square the TX_Pin impedance. Previous mentioned steps are marked as a, b and c. Note that there are two half-moon patterns that conforms a and b. Center as starting point, initiating downsides.

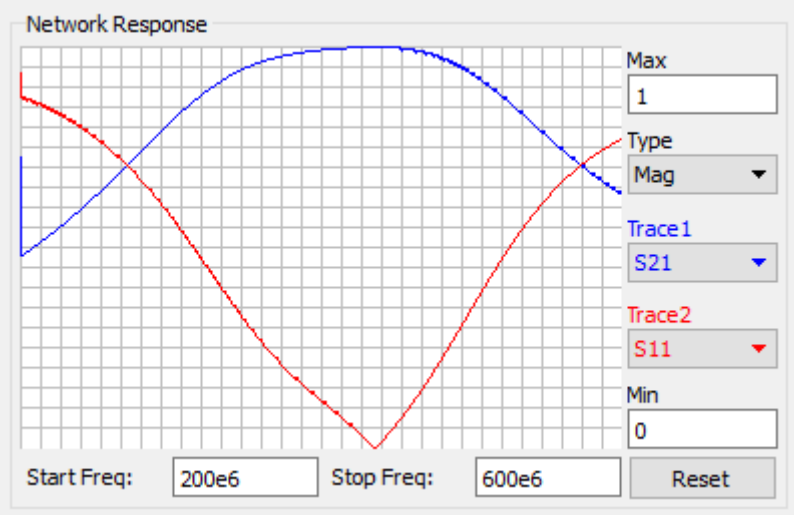

Fig. 4.12 Network response of TX circuit, optimized for 436.5MHz.

4.3. Power – V_{DD} filter

4.3.1. Transceiver power and V_{DD} filter

The transceiver Si4460 operates with 3.3V that has to be filtered properly as it shares the same PCB board as the High Frequency section. Due to filtrations, V_{DD} filter capacitors has to be added.

A Capacitor acts as a filter erasing the high frequency components due to its high pass filter type of frequency response. The -3dB cutoff frequency is given by the next expression from which it can be seen that as higher is the Capacitance lower is the cutoff frequency.

$$fc = \frac{1}{2\pi C}$$

Placing that capacitor between the direct current signal and ground will short-circuit all HF components over its cutoff frequency and act as a Low pass filter for the power signal.

Normally and as stated on the SiLabs layout design guides AN629, the lowest capacitance is placed nearer to the transceiver and following an ascendant order.

On figure Fig. 4.13 it can be seen the Vdd filtering section. Note that 3.3pF is the nearest to VBATA pin.

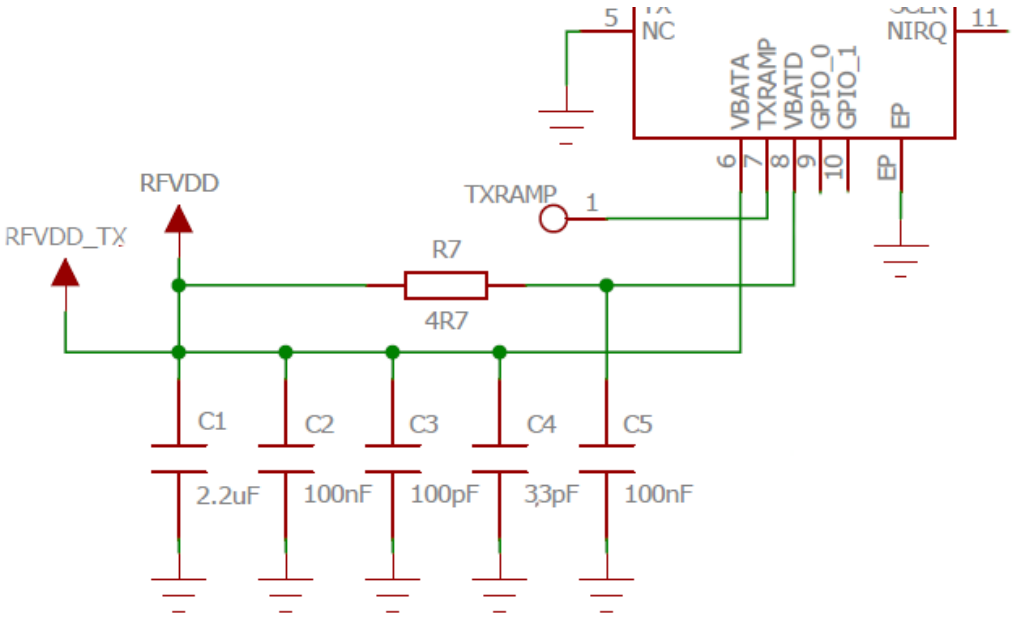

Fig. 4.13 V_{DD} filter and power section[6]

[6] Figure obtained from the Silabs 4463-PCE20B915 evaluation board scheme. Available on Silabs website.

4.3.2. SKY65116 power section

The Amplifier employed needs 3.6V in DC.[7] Being the available voltages provided from the PC104 bus 5V and 3.3V, the LT1086 regulator is used in order to obtain 3.6V from the 5V signal capable to drive currents up to 1.5 A, being 1300 mA the maximum stated for the amplifier.

In previous figure Fig. 4.5 it can be seen the design of the not made evaluation board which includes the regulator and the needed capacitors for AC coupling filtering.

At the input and output of the LT1086 there are two Tantalum Capacitors of 10 µF and 100 µF respectively as it is expressed on its datasheet for stability purposes.

A part, two capacitors of 0.01 pF and 10 pF are placed in each of the 3 power pins that the SKY65116 has as a V_{DD} filters as expressed on the SKY65116 datasheet.

4.4. Crystal

Si4460 needs an external crystal to drive the internal oscillator needed to create the operating frequency of the transceiver and operate its internal components.

As stated on its datasheet, a crystal from 25 MHz to 32 MHz.

A XC1562CT-ND 30 MHz crystal is selected from Digikey which provides ±10 ppm of stability, that corresponds to ±4.3 kHz at 436 MHz operation, more than enough for our purposes.

5. Beacon Design

5.1. Introduction

As expressed on section 3.3 Beacon system – General conception, the use of a constant Morse transponder adds a critical redundancy on the satellite in case of failure of the main transceiver.

The basis of this beacon is based on the use of a microcontroller that supervises the satellite status and creates the Morse tone messages, and a secondary transmitter that emits the Morse signal at the required frequency with the required power.

The microcontroller employed is based on the same chip used on the Arduino UNO board. A MCU easy to program with already existing libraries for Morse

[7] See Sky65116 datasheet, on Annex B.

messaging which are basically a digital 0 and 1 signal from one of its digital out pins which will go to the enable/disable pin of the transmitter.

5.2. TH72012 ASK Transmitter

The employed transmitter is the basic TH72012 ASK modulator. It is an 8 pins chip in which a $f_c/32$ crystal has to be connected in order to obtain an output signal at frequency f_c.

Being not available crystals for working on 436.5 MHz or similar inside the amateur band suitable for this chip, it was decided to use a 13.560 MHz crystal, which are more popular. The model is 7A-13.560MAAE-T, from TXC CORPORATION. That gives an output at 433.92 MHz with a Load Capacitance of 12 pF. That corresponds to an ISM band for the Region 1 in which license is not required.

Being just an ISM band for Region 1, it will be needed to check properly its allowance to work for satellite purposes. This an early design or concept, in which further investigation is needed in the case if the satellite is going to be launched. Even though a crystal which provides a resonant frequency which leads inside the amateur band was found, with 13.605 MHz model ABLS-13.6050MHZ-20-R50-D-T from Abracon LLC, which would provide a signal of 435.36 MHz (within the 70cm amateur band) its Load Capacitance of 20 pF falls off the maximum that the ASK modulator can handle (15 pF).

As stated on the TH72012 datasheet, the crystal pulling caused by the Load capacitance and the added CX1 capacitance in series with the crystal (see figure Fig. 5.3 and Fig. 5.4) causes an equivalent Load Capacitance CL seen by the ASK modulator expressed by the expression in Fig. 5.1. The frequency of operation varies in function of CL and given the values on the test circuit of its datasheet (Fig. 5.4), for 433.92 MHz operation using a crystal with C_L = 12pF (same employed), then CX1 = 27 pF. Further information about crystal operation can be seen in the datasheet of the more complex ASK/FSK modulator TH72015 from the same brand.

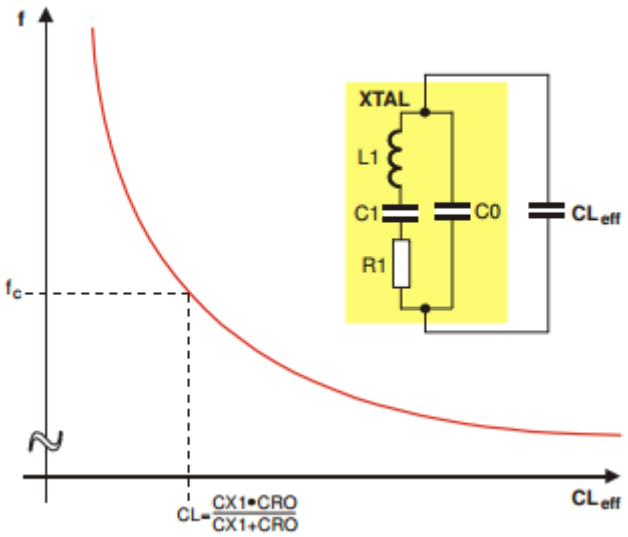

Fig. 5.1 Crystal pulling characteristic.

The chip creates a carrier at f_c when its ASKDATA pin is driven high and silence when is in low as it is expressed on figure 5.1 extracted from the TH72012 datasheet. Also the ENTX pin (enable pin) needs to be in high. This kind of modulation is also known as OOK modulation, which corresponds to Morse code when audible Morse messages are modulated instead of digital bits.

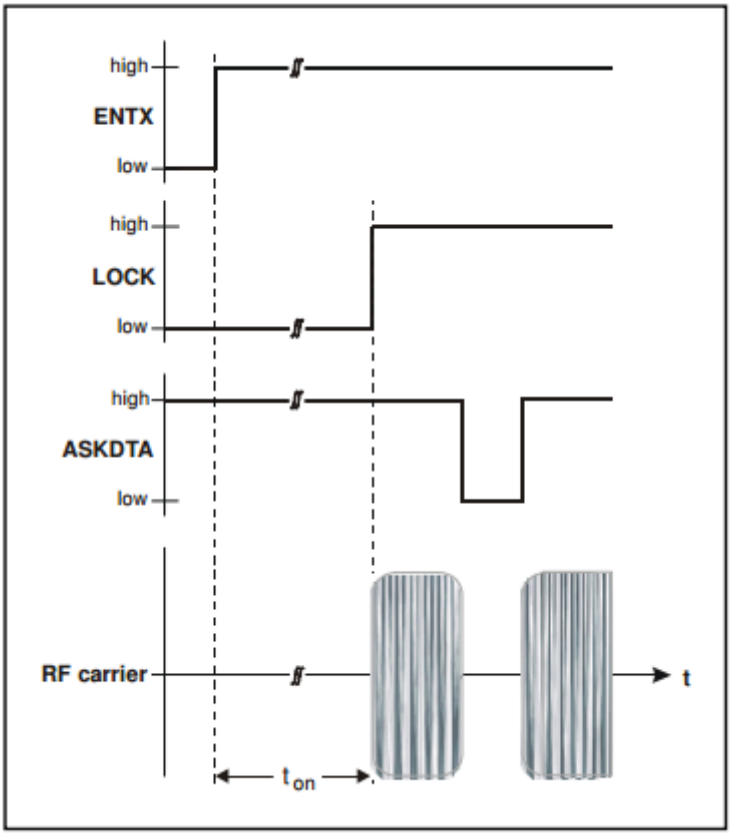

Fig. 5.2 ASK diagram

TH72012 has an output power regulated by a resistor which selects over 4 possible power levels depending of the chosen value. The power level chosen is 2 with a resistor of 56 kΩ having an output of -3 dBm. That is chosen depending on the maximum input of the selected Amplifier for the Morse beacon.

The matching circuitry of TH72012 is explained on its own datasheet with already defined components values as it is shown for the same operation at 433.92 MHz.

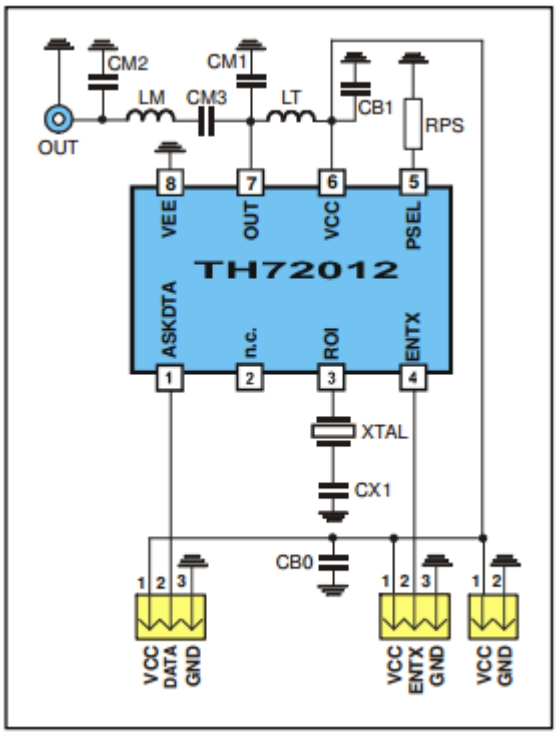

Fig. 5.3 50Ω Test circuit extracted from its own datasheet.

Part	Value @433.92 MHz	Description
CM1	5.6 pF	impedance matching capacitor
CM2	10 pF	impedance matching capacitor
CM3	82 pF	impedance matching capacitor
LM	33 nH	impedance matching capacitor
LT	33 nH	output tank inductor
CX1	27 pF	XOSC capacitor
RPS	56 kΩ	power-select resistor
CB0	220 nF	blocking capacitor
CB1	330 pF	blocking capacitor
XTAL	13.560 MHz	fundamental wave crystal, C_L=12pF

Fig. 5.4 Component values table

5.3. MAAL-010704 Power Amplifier

The TH72012 ASK modulator has a maximum output of 10 dBm which is too low for our beacon purpose. That is why it is added a power amplifier.
Different possibilities of ASK modulation + Amplifier was available on Digikey stock. Due to its rapidly sold out ratio of those components the beacon system had to be redesigned 2 times, being this the V3.

In order to have a transponder with enough output power the 22 dB of Gain MAAL-010704 amplifier is chosen which provides 18.5 dBm of signal output being 21 dBm its P1dB at 400 MHz.

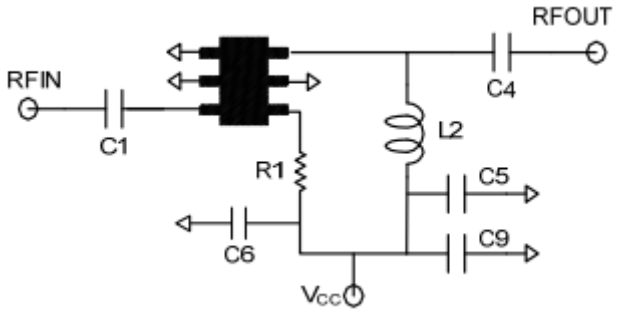

Fig. 5.5 Evaluation board example circuit.

The application circuit of this amplifier is expressed on Fig. 5.5 in which C1 and C4 acts as a DC blocking capacitors (High Pass Filters); C5, C6 and C9 as a AC blocking capacitors for the power line (Low Pass Filters); and R1 is chosen for the wanted total current I_{DQ} value, which will define the signal output value.

The relation between I_{DQ} and R1 is given by Fig. 5.6 at 5V operation.

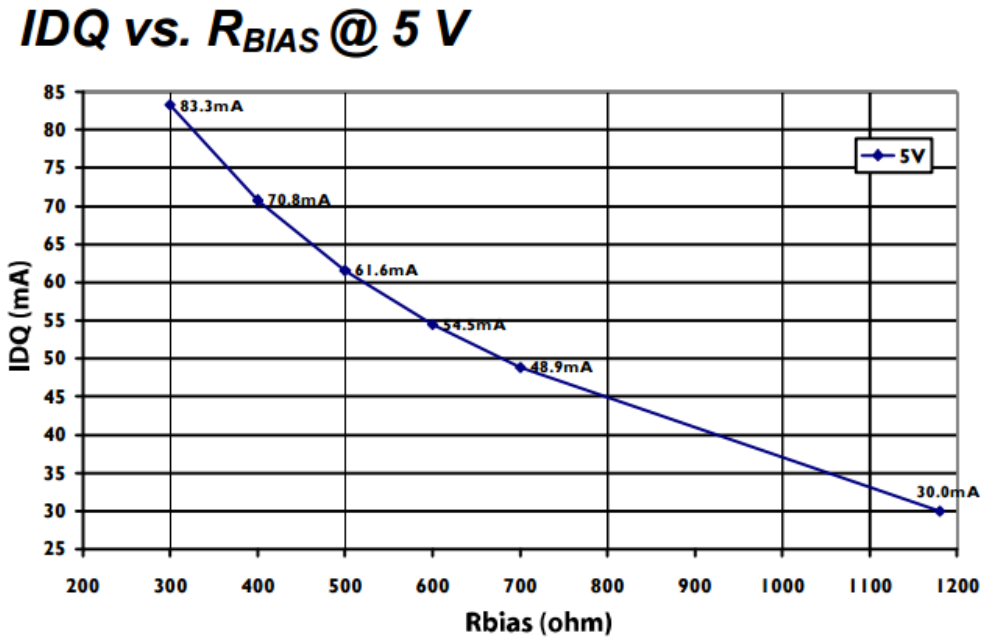

Fig. 5.6 I_{DQ} vs. R1 graph from MAAL-010704 datasheet.

Graphs for operation at 5V with IDQ 30mA and 60mA are provided on the datasheet. It can be seen that for approx. 500 MHz the amplifier provides:

- Gain G = 22 dB and P1dB = 20 dBm for 60 mA.
- Gain G =20.5 dB and P1dB = 21 dBm at 30mA.

Having an input coming from the ASK modulator of -3 dBm would provide an output power of 19dBm@60mA and 17.5 dBm@30mA. It is chosen an intermediate option, with R1=750 Ω it provides about IDQ = 50mA which provides a gain G = 21.5 dB and P1dB = 21.5 dBm that stands for an output power of 18.5 dBm.

Operation at 3V it was not taken into account initially because of its lower output power and gain, but given the significant lower consumption that gives at 3V, a properly redesign should be made for this voltage. The complexity on the PCB design of having 3V (or 3.3V) at the Amplifier with just a 2-layer PCB was the reason to consider using the 5V source, same used on the ASK modulator.

The components values are taken from averaging the different testing circuits included on the datasheet and are expressed on table Fig. 5.7.

Part	Value
C1, C4	1 nF
C6	10 nF
C9	100 µF
L2	100 nH
R1	750 Ω

Fig. 5.7 MAAL-010704 component values for 433.92 MHz operation.

5.4. Atmega328P MCU

The microcontroller chosen to create the short Morse messages is the one employed on the Arduino UNO boards. It is really easy to program with the properly bootloader installed from Arduino and the free software provided. Also lots of examples and libraries are available for Morse code and I2C interface operation, the one which is used to obtain information from the main computer of the satellite.

The chip consists on a 43 pin TQFP package showed on Fig. 5.8.

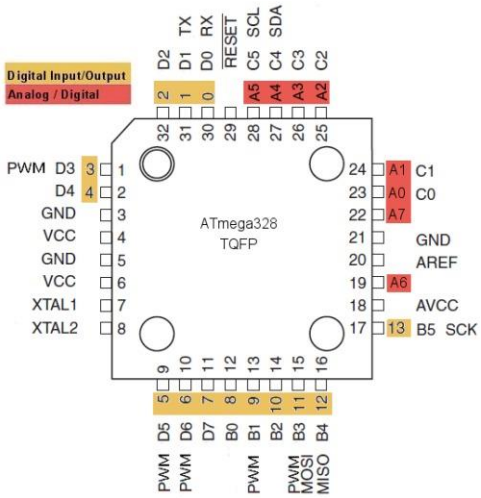

Fig. 5.8 TQFP Atmega328p pin configuration.

There are different ways to program it. The one selected is using an external Arduino UNO board as an ISP programmer. The method to connect both boards for bootloader purposes is using a PCI interface which consists of 4 digital lines (SS, MISO, MOSI and SCK) interconnected between both as it is seen on Fig. 5.9 for an ATmega328 with different package. To program normally once burned the bootloader it is used just the TX and RX pins interconnected between both boards or using a special Serial-USB converter.

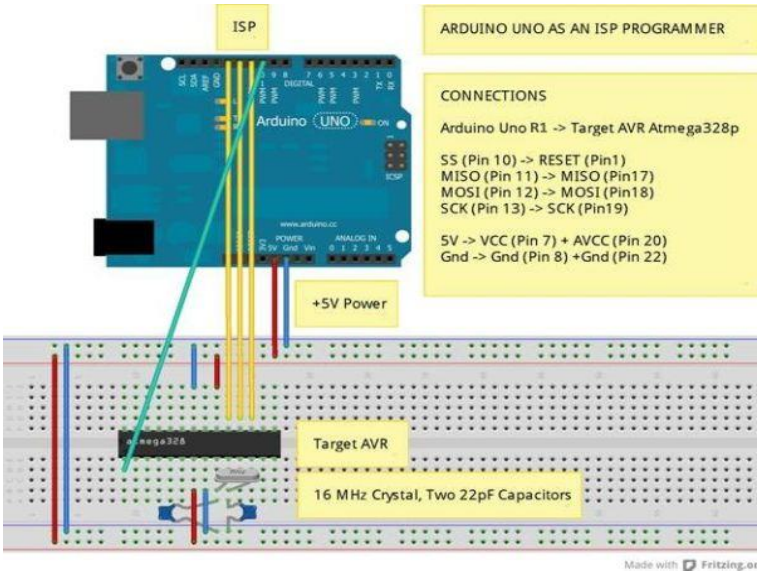

Fig. 5.9 Example of using an Arduino UNO board as an ISP programmer.

ATmega328p needs also an external 16 MHz crystal with two 22 pF capacitors as shown in multiple websites and forums about projects about modelling homemade Arduino boards (DIY-Duino) using ATmega328 chips. Also a resistor is needed on the RESET pin of the chip, with chosen value of 10 kΩ based on the different examples on internet.

To interconnect the ATmega328p integrated chip with the other Arduino Board programmer it is employed a 10 pin 0.1-inch pitch connector (same kind used on Arduino boards). On it, it is possible to connect directly GND, +5V, the PCI bus

(4 pins), RX and TX for normal programming and 2 Analog-Digital I/O for testing purposes.

5.5. Beacon layout

All the previous detailed modules are assembled with the same components values as showed in Fig. 5.10 for the HF section and Fig. 5.11 for the MCU section.

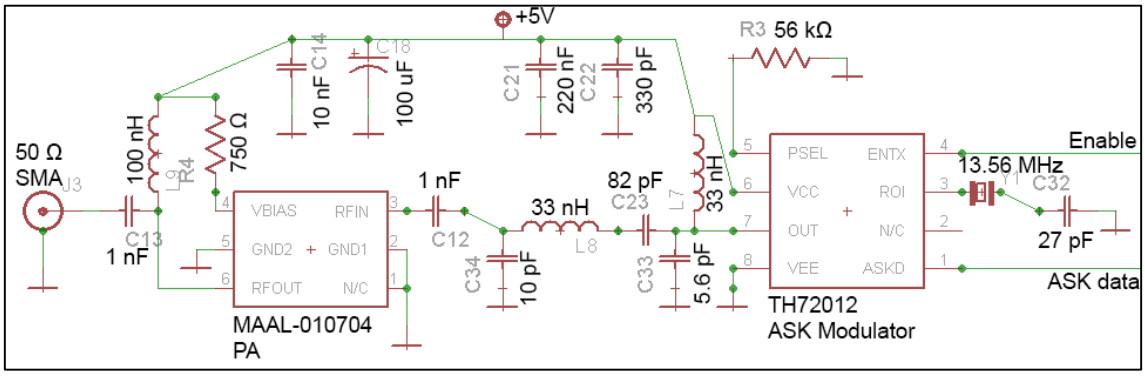

Fig. 5.10 HF Beacon layout section.

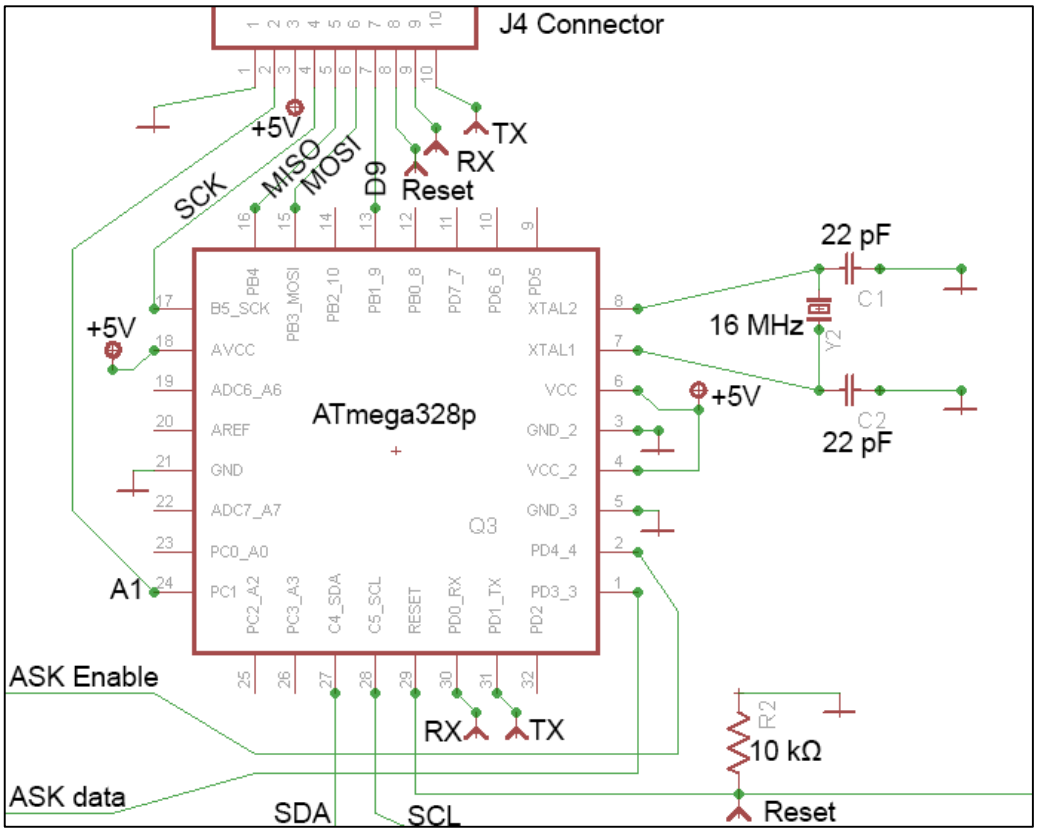

Fig. 5.11 MCU Beacon layout section.

6. Antennas

6.1. Main link antennas

Being restricted the use of directional antennas onboard the satellite as a general recommendation when designing CubeSats due to the need of a complex system of orientation that needs to know the real position of the satellite respect the Base station in ground, it is needed to use omnidirectional antenna type.

One of the simplest and widely used is the dipole antenna. It consists of 2 straight active elements in opposite ways with approx. λ/2 of total length. This type of antenna is named λ/2 dipole or half wave dipole and is shown in Fig. 6.1.

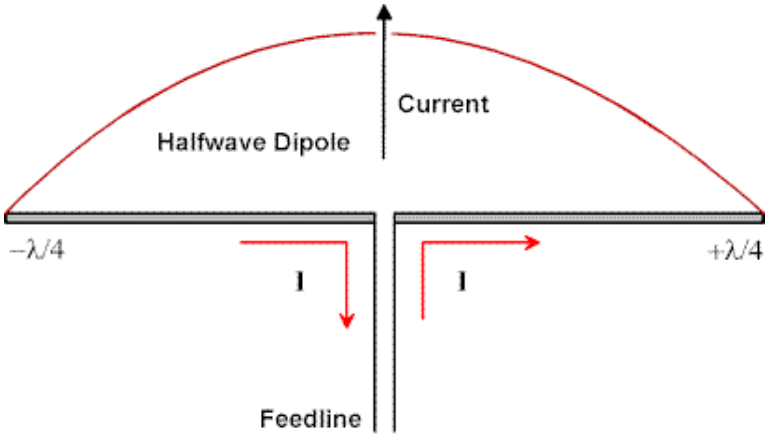

Fig. 6.1 Half wave dipole with its current distribution.

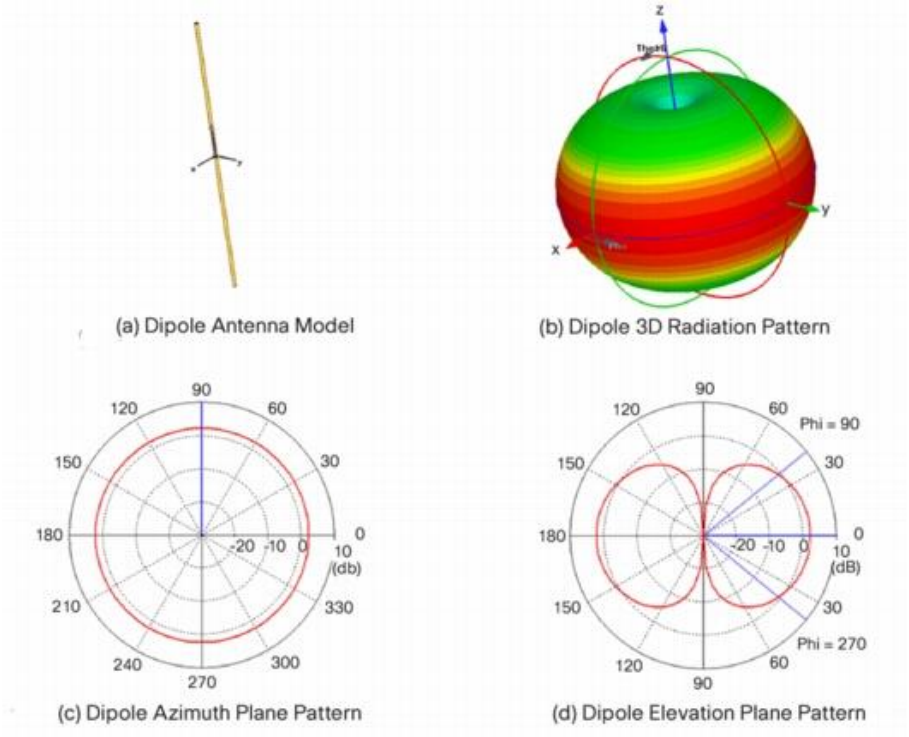

Fig. 6.2 Diagram pattern of a half wave dipole antenna.

The radiation diagram of a half wave dipole is near omnidirectional shown on Fig. 6.2 with a directivity of 2.16 dB.

The idea is to use two antennas for the main link. One for uplink and the other for downlink. As it is going to work in half-duplex mode, there is no interaction between them while working.

Dipole antennas have linear polarization. That means that in order to use it properly it is needed to orient the antennas in the same plane vertical or horizontal (apart of the orientation in elevation and azimuth if they are directive). As stated on the link design, the ionosphere induces a rotation effect to the polarization that can vary as much as 360º being not possible a linear polarized link. In order to fix that, it is used circular polarized antennas in ground which will introduce a 3 dB loss but fixes the ionosphere problem.

Another property of a dipole antenna is that both elements needs a balanced signal. That means that it is needed a conversion between the unbalanced signal given by the coaxial cable (Signal-Ground) to balanced (Signal-Signal'). That is done by a component named Balun which apart of provide balanced-unbalanced conversion usually also acts as a matching circuit.

The theoretically thin wire half wave dipole antenna (L=0.5λ) working at (λ) has Z = 73 + j42.5 Ω impedance. This imaginary reactance part means a loss of power if just real matching is done. A solution is made shorting the antenna to L=0.48λ which became resonant with Z = 70 Ω or similar, without reactive part. In experience antennas are not thin wires, having thickness that reduces the resonant length of the antenna, which often is close to 0.47λ. Further information is obtained in the testing section 9.3.1.

A Balun that creates balanced signal and matches between 2 different impedances can be easily made with just 2 inductors and 2 capacitors in the same way expressed on Fig. 6.3.

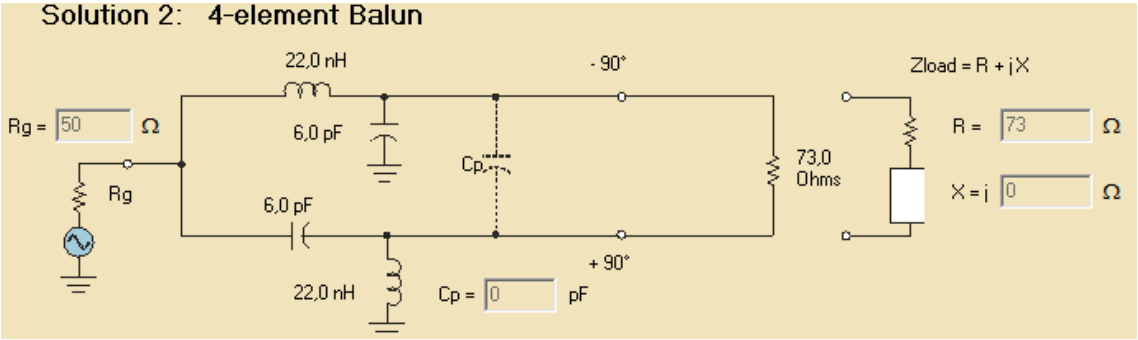

Fig. 6.3 4 Element Balun with 73 Ω to 50 Ω matching.

6.2. Beacon antenna

For the beacon transponder it is chosen a typical quarter wave monopole for its simplicity. Basically it consists on half of a dipole antenna, in which there is a

ground plane on the bottom that acts as another virtual λ/4 performing a whole dipole.

A λ/4 monopole is simpler than a dipole as does not need a Balun as it works with unbalanced signals. Usually this ground plane is made by wires or by the place where the antenna is placed like the roof of a metallic car for example. In our case it is assumed that the satellite structure will provide enough grounding to the antenna.

The diagram pattern is half of the dipole antenna and it is shown by Fig. 6.4.

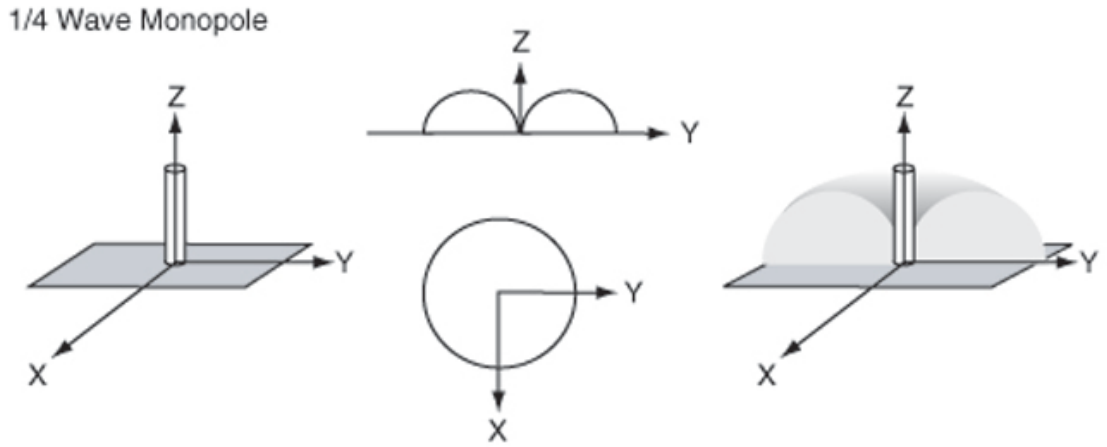

Fig. 6.4 Monopole antenna diagram pattern.

The impedance is also half of the dipole, being theoretically Z = 36.5 Ω for its resonant frequency. Its matching can be performed with 2 LC components from 50 Ω to 36.5 Ω.

6.3. Deployment system

During launch the satellite has to comply with its dimensions of 30 x 10 x 10 cm. It cannot have any device or antenna that surpasses those dimensions. It is needed then a system that deploys the antennas once it is launched.

The idea is taken by several previous CubeSats. It consists on using measuring tape for the active components of the antennas, and fold those around the satellite to comply with the restricted spacing. The measuring tapes are tied to the satellite body by a special Nickel Chromium wire hat when a current flow on it, it melts and liberates the measuring tapes that due to its shape became straight in their corresponding positions. The design of this wire and the system that melts those is not designed as there was no time and is placed apart, on the outside of the satellite. Further research should be done.

The antennas are soldered into an internal 10 x 10 cm PCB in which contains the Baluns, the matching circuit of the monopole antenna, 3 SMA connectors and the feed points of the antennas.

7. PCB design

7.1. PC104

PC104 stands for a family of embosses computer standards which defines both form factor and computer buses. It is a type of boards that are optimum for CubeSats purposes as its dimensions are 9.01 x 9.58 cm which fits the interior pretty well.

The bus employed in Hathor is the a non-standard one used for the Pumpkin Computer that consists of two 52 pin 0.1 pitch double row connectors. Those two are named H1 and H2 being H1 the one on the inside part of the board. The connectors employed are the model ESQ-126-39-G-D from Samtec. Further dimensions can be found on the "CubeSat Kit PCB Specification" datasheet provided by Pumpkin[8].

Based on that, a PC104 library in PCB making Eagle Software is modified to our purposes. The power pins and I/O of the computer are detailed on the "CubeSat Kit Motherboard (MB)" Hardware Revision: D datasheet from Pumpkin, in which pins like the 3.3V, 5V and PCI bus are defined.

The pins that are used by the telecommunication system are showed in table on Fig. 7.1.

Pin number by Pumpkin	Physical pin number	Description
IO.13	H1.11	SPI Slave Selector
IO.12	H1.12	Beacon Reset
IO.11	H1.13	Transceiver Shutdown
IO.10	H1.14	GPIO1
IO.9	H1.15	GPIO0
IO.8	H1.16	NIRQ Interrupt event
IO.3	H1.21	SPI SCK clock
IO.2	H1.22	SPI SDI Master data in
IO.1	H1.23	SPI SDO Master data out
SDA	H1.41	I2C SDA
SCL	H1.43	I2C SCL
5V_SYS	H2.25	+5 V
5V_SYS	H2.26	+5 V
VCC_SYS	H2.27	+3.3 V
VCC_SYS	H2.28	+3.3 V
GND	H2.29	Ground
GND	H2.30	Ground
A_GND	H2.31	GND at FM430 MCU
GND	H2.32	Ground

Fig. 7.1 Used pins by the telecommunication system.

[8] http://www.cubesatkit.com/docs/datasheet/DS_CSK_MB_710-00484-D.pdf, included on Annex C.

7.2. PCB Layout

A little bit of research in PCB designing was done learning basic concepts. Due to the limitations found on ADS software while designing the evaluation board for the amplifier, it was decided to use another software more focused on designing, like CadSoft EAGLE PCB design.

The SiLabs application note AN629 provides a useful guide with design recommendations and steps for high frequency products like the si4460.

The high frequency signal needs to be routed using a waveguide, as the equivalent impedance varies depending on the substrate and thickness of the PCB.

The type of waveguide employed is named coplanar waveguide with ground, which is depicted by Fig. 7.2.

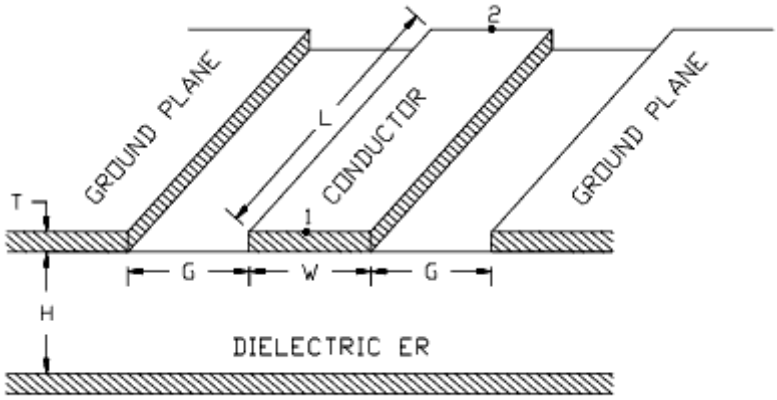

Fig. 7.2 Coplanar with ground waveguide[9].

Using a coplanar waveguide calculator[10], for the standard FR4 PCB substrate with H = 52 mils thickness, a suitable configuration is with W = 60 mils and G = 15 mils that provides an impedance Z = 52 Ω at ε = 4.8. FR4 material is not optimum for High frequency purposes as the permittivity ε can vary very much between 4.0 and 4.9 which produces variations in the equivalent impedance between 56 Ω and 51 Ω. Optimal materials for HF would include ROGERS substrate which has considerable higher price.

The final design of the Satellite PCB is shown on Fig. 7.3 while the PCB board used for the ground station is shown on Fig. 7.4.

---

[9] Coplanar Waveguide – Microwaves101.com,
Link: https://www.microwaves101.com/encyclopedias/327-coplanar-waveguide-microwave-encyclopedia-microwaves101-com

[10] Coplanar Waveguide Analysis/Synthesis Calculator http://wcalc.sourceforge.net/cgi-bin/coplanar.cgi

Additionally the PCB that is used to attach the two diploes antennas and the monopole, is shown on Fig. 7.5, in which contains the SMA connectors on the bottom, and the balun components next to it. Then waveguides connects to each active element of each dipole antennas.

Most of the RLC components where chosen from Digikey respecting the recommendations that SiLabs states like wire-bounds inductors for the TX section. Almost all are Murata components of sizes 0402 and 0603 respecting the maximum Voltages and currents that the circuit is going to have.

For example, for the LPF section between the SKY65116 Amplifier and the TX antenna connector, with almost 3W of power it was simulated in ADS software that the wave has a voltage up to 17V-rms and 355 mA-rms for the 50 Ω impedance of the line at 35 dBm of transmitted power. Those values were taken into account when selected the affected components.

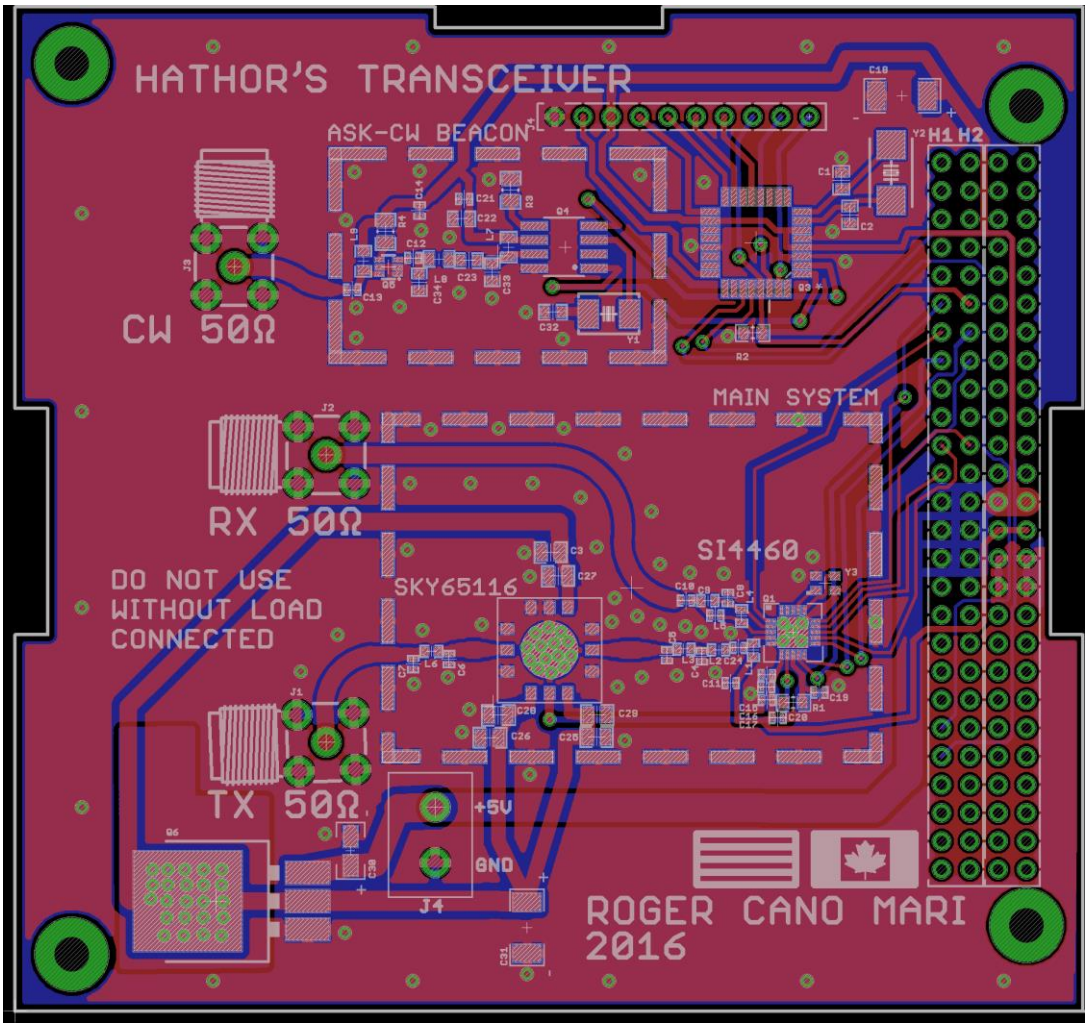

Fig. 7.3 PC104 Hathor's PCB Transceiver.

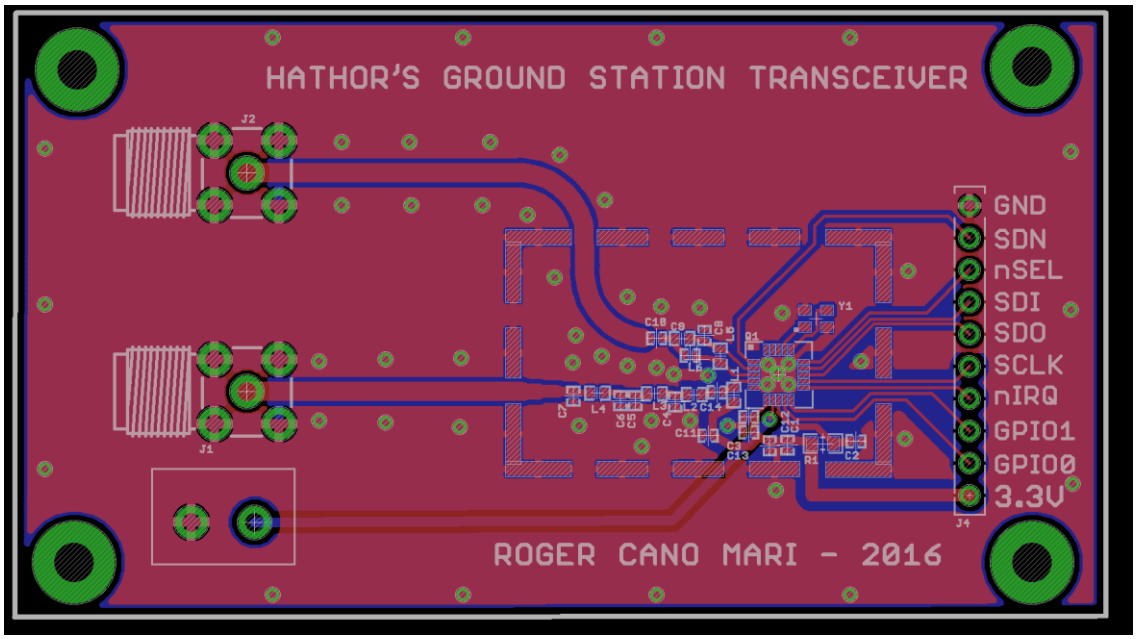

Fig. 7.4 Ground Station transceiver PCB.

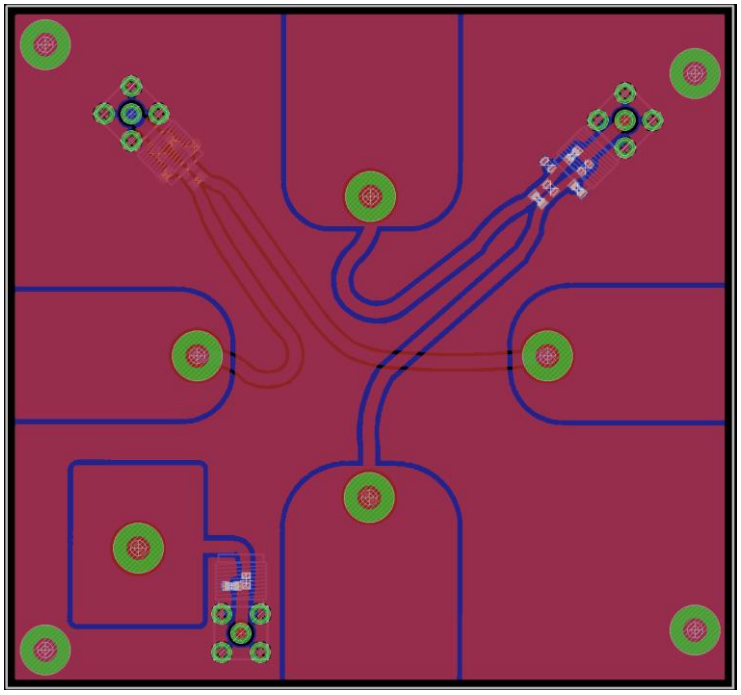

Fig. 7.5 Antenna base PCB.

All the designs are respecting the specifications of the PCB manufacturer chosen: Canadian Circuits. About 10 Quotes were made to multiple PCB manufacturing.

Due to the high cost of PCB manufacturing, Polyorbite decided to include the 5 PC104 boards and 4 solar panel PCB it is needed to print from all the Polyorbite sub-teams into one big board. The joining of PCBs was done by the author of this thesis using the same EAGLE software. With that Polyorbite obtained all the PCB by a student quote of 325$ CAD.

As it can be seen on Fig. 7.4 and Fig. 7.3, the ground station PCB is considerably simpler than the satellite one. That is due to the lack of a more code transponder and that because the transmitted power in ground has to be much greater than the transmitted in satellite, external Power Amplifiers has to be used.

There are Amplifiers up to 100 W available on internet that consists on boxes with input and output connectors.

The control of the ground station is thought to be made with a bought Arduino UNO board, although it should work with any PCI device.

The Digikey chart of used components is shown on Annex A chapter 3.

7.3. Assembly

The assembly was made by Optimont Inc. in which due to the lack of time and cost some of the important components of the main system such as the Amplified were not soldered, as they quoted 400$ for the Radio SAT (Hathor's transceiver) due to the need of stencils. The quote is available on Annex A chapter 4.

In that way just the antennas and the beacon system of the Hathor's transceiver could be tested.

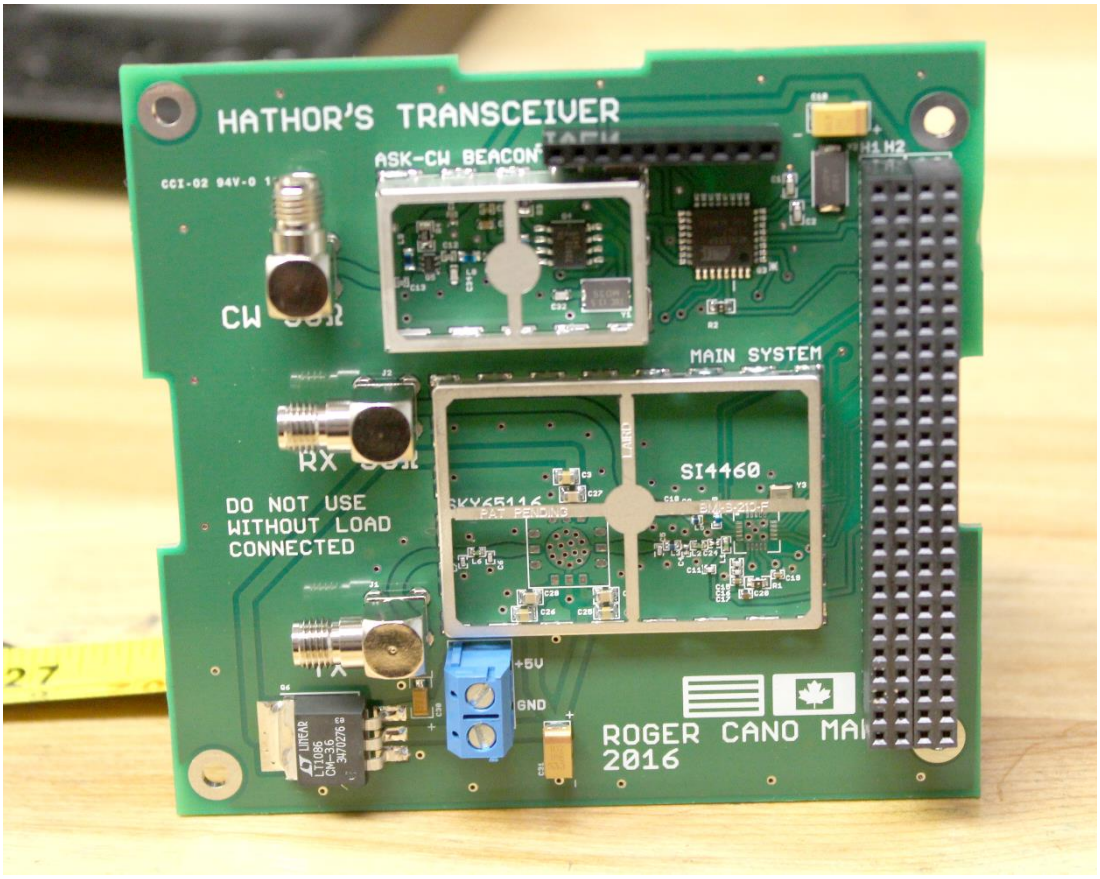

Fig. 7.6 Hathor's transceiver, without the SKY65116 nor the Si4460 chips soldered. RF shields showed without covers.

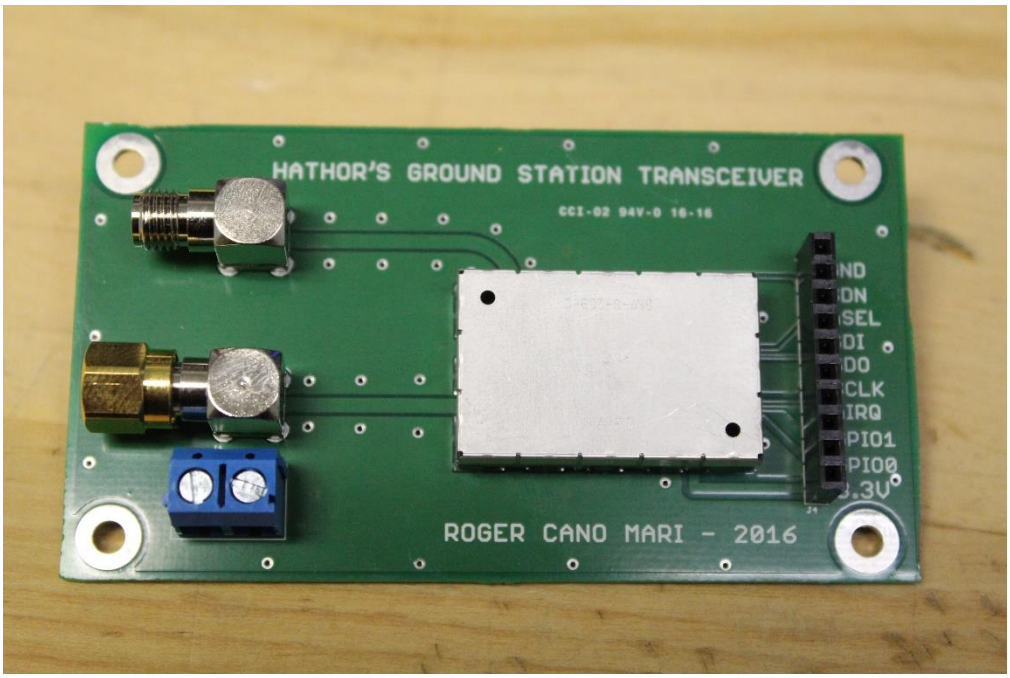

Fig. 7.7 Hathor's ground station PCB.

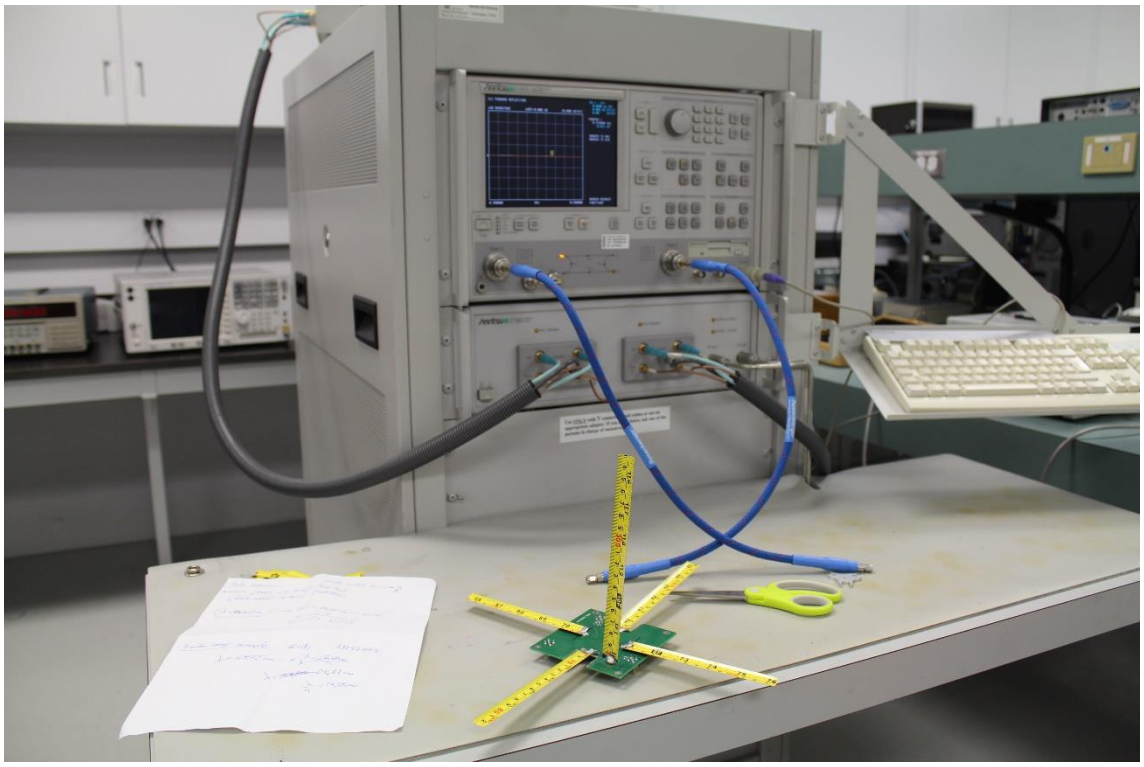

Fig. 7.8 Antenna's PCB after tests with the Vector Network Analyzer.

8. Programming

It was found few places that provided libraries to control the Si4460 transceiver.

Commercially this transceiver can be found with different names like the RH_RF24 that Works with Silicon Labs Si4460/4461/4463/4464 family of transceivers chip. There is a section of the website airspayce called RadioHead[11] which provides libraries for controlling that model of transceivers for Arduino boards.

Also, the transceiver needs a configuration file that can be done using a free emulator official from SiLabs named Wireless Development Suite[12], in which the type of modulation, packet type, speed, crystal, etc. is introduced and then it provides a dat file necessary while programming.

The Morse beacon program is simpler and part extracted from online forums. It is expressed on Annex A chapter 5.

9. Testing

9.1. Transceiver

The transceiver can be tested in two main ways. From one part, the real output power can be measured to assure that it complies with the theoretical computations. From the other, digital tests can be done by simulating a link between the Satellite PCB and the Ground station by wire placing an attenuator.

The kind of attenuator necessary to simulate digital messaging for our case was found to be more expensive than all the system, being about 900$ USD. Using antennas instead of wire would violate the broadcasting laws as it is needed an amateur license. That is why this kind of testing should be made by decreasing a lot the output power of the transmitter.

As a precaution it has to be known that the use of the transceiver with no load connected will severe damage the system, as the input relative impedance is infinite and all the power is reflected backwards burning the amplifier.

In order to avoid that, a type of component called terminator is plugged on the output connectors of the transceiver. The bought terminators but are designed to work at a maximum of 2W which is below what the amplifier can provide. That is why long use of the transceiver with that terminators should be also avoid without the properly programming.

[11] http://www.airspayce.com/mikem/arduino/RadioHead/
[12] http://www.silabs.com/Support%20Documents/Software/WDS3-Setup.exe

9.2. Morse beacon

To test the Morse beacon is easier with just an oscilloscope in which it can be seen the sent messages and transmitted power on screen.

The code shown on Annex A chapter 5 is employed for testing in which a predetermined text message is coded by a user function to a digital signal with Morse signal behavior. Using an oscilloscope with 10s of time scale is tested the digital signal as shown on

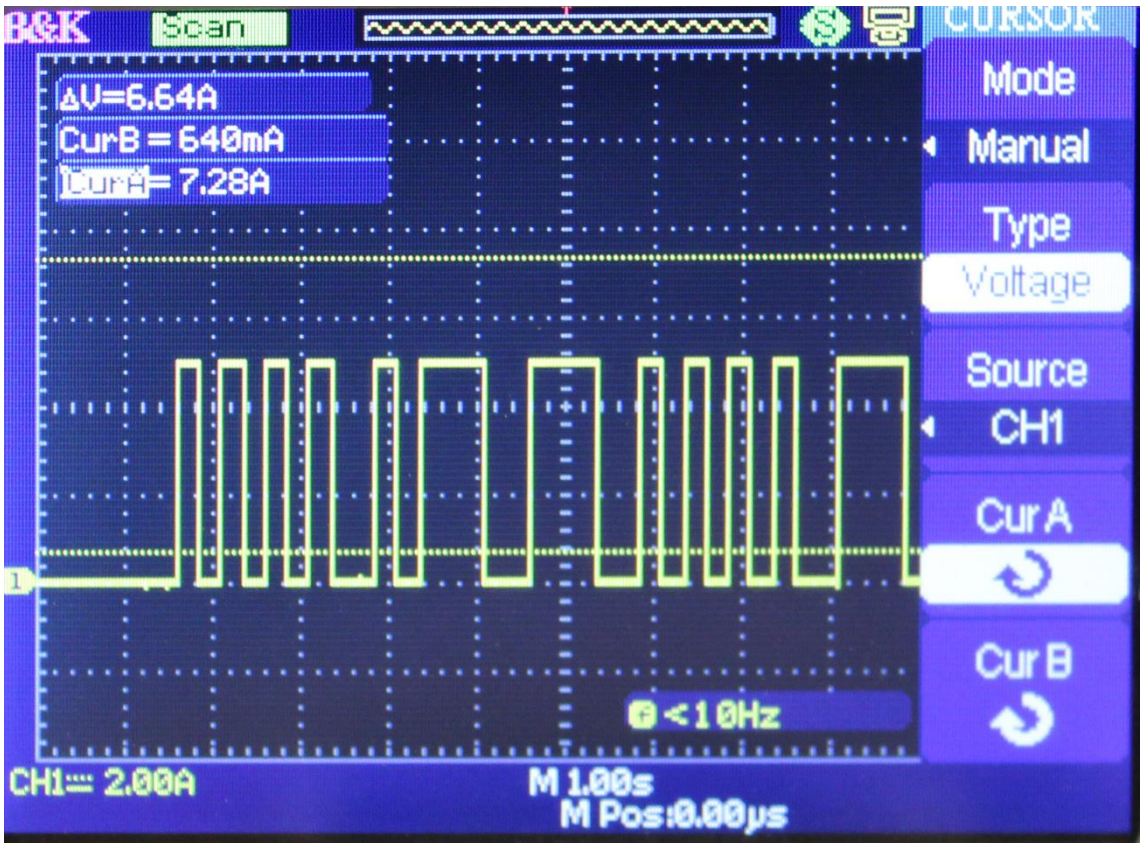

Fig. 9.1 Digital signal with Morse shape, output from an Arduino. HATH… can be deduced, from the heading of the message which includes the name of the satellite: Hathor.

The bootloader was successfully uploaded to the ATmega328P microcontroller included on the PCB and the code uploaded on it. Using the same method with the oscilloscope and a probe it was tested that Morse code is sent between the microcontroller to the ASK modulator, but the output didn't correspond to the wanted signal. No captures could be done about its behavior but it can be deduced that the amplifier worked well.

After a while, given a short-circuit caused by the probe on the amplifier, this one burned down and no more tests could be done to the end signal.

Anyway, the problem seems to be related with the ASK modulator which seems to not create the carrier signal properly on its output. Further investigation should

be done on the ASK modulator, probably with the crystal parameters and its capacitor, which has not really clearly application notes on the datasheet.

9.3. Antennas

Testing the antennas is very important as it should be measured its real impedance for its properly matching to 50Ω. Not matching properly will produce reflections of the signals which would greatly damage the amplifier in the transmitter case or receive nothing in the receiver case.

The optimum way is to measure the input impedance of the measurement tapes soldered on the antennas PCB and inside the structure.

The impedance computation can be made by a Vector Network Analyzer or VNC, in which provides S11 values or reflecting coefficients that can be translated to its impedance in function of the frequency.

Once analyzed its parameters, corrections on the wire lengths of the dipoles can be done. Although it was found that in the degree thesis “UHF-VHF CubeSat Antennas Design” by Teresa Lucía Aparicio Jiménez, measurement tape antennas produce too unexpected results that are partially solved by doubling the dipole length (which has no sense) or pouring with copper the measurement tape.

The tests done but gives very good results.

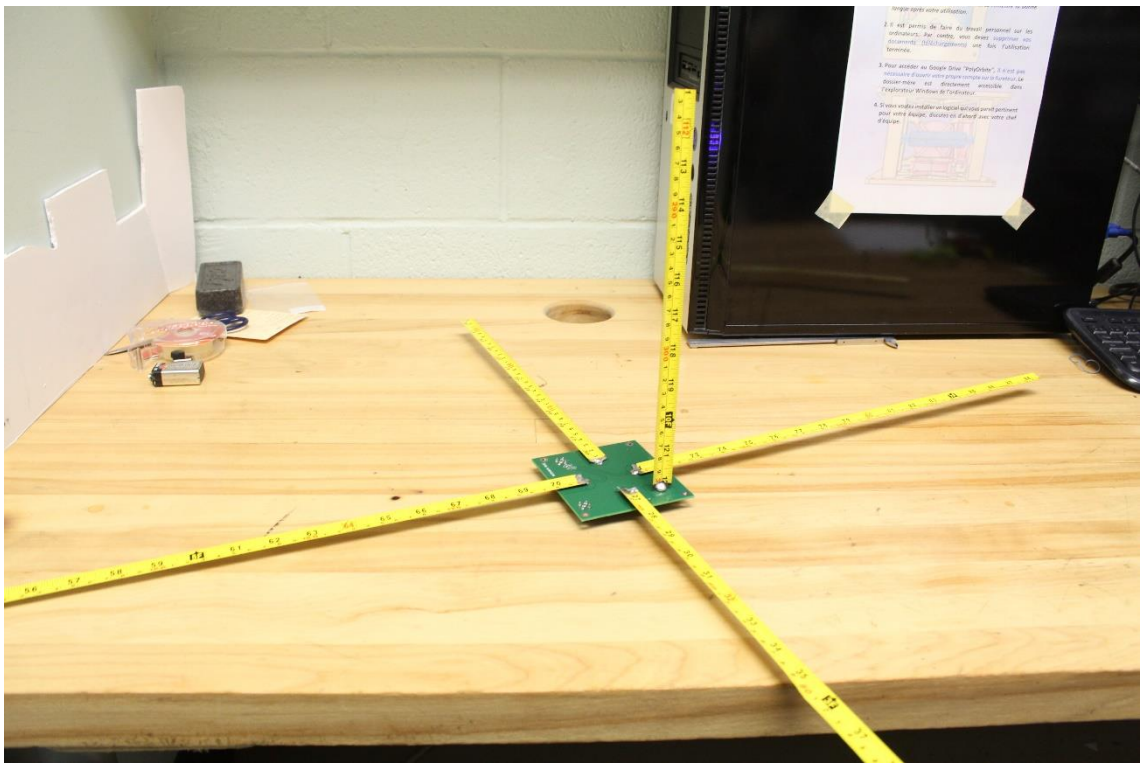

Fig. 9.2 Antennas used before testing (larger than needed). Two horizontal dipole antennas (half-duplex) and a vertical monopole antenna.

9.3.1. Test results - Dipoles

The two dipole antennas have same baluns and circuits employed. The firsts tests are employed with lengths of 41.23 cm (0.6λ), 40cm, 37cm and 35cm. As it can be seen on the captures of the S11 obtained from the VNA, the resonance frequency shifts to the right (higher frequency) as the dipole length is reduced.

Although the theoretical dipole length should be 0.47λ (34.36 cm) the best result is obtained at L=37 cm with a S11 = -5.45 dB, that stands for a VSWR[13] = 1.79 which is not really fine.

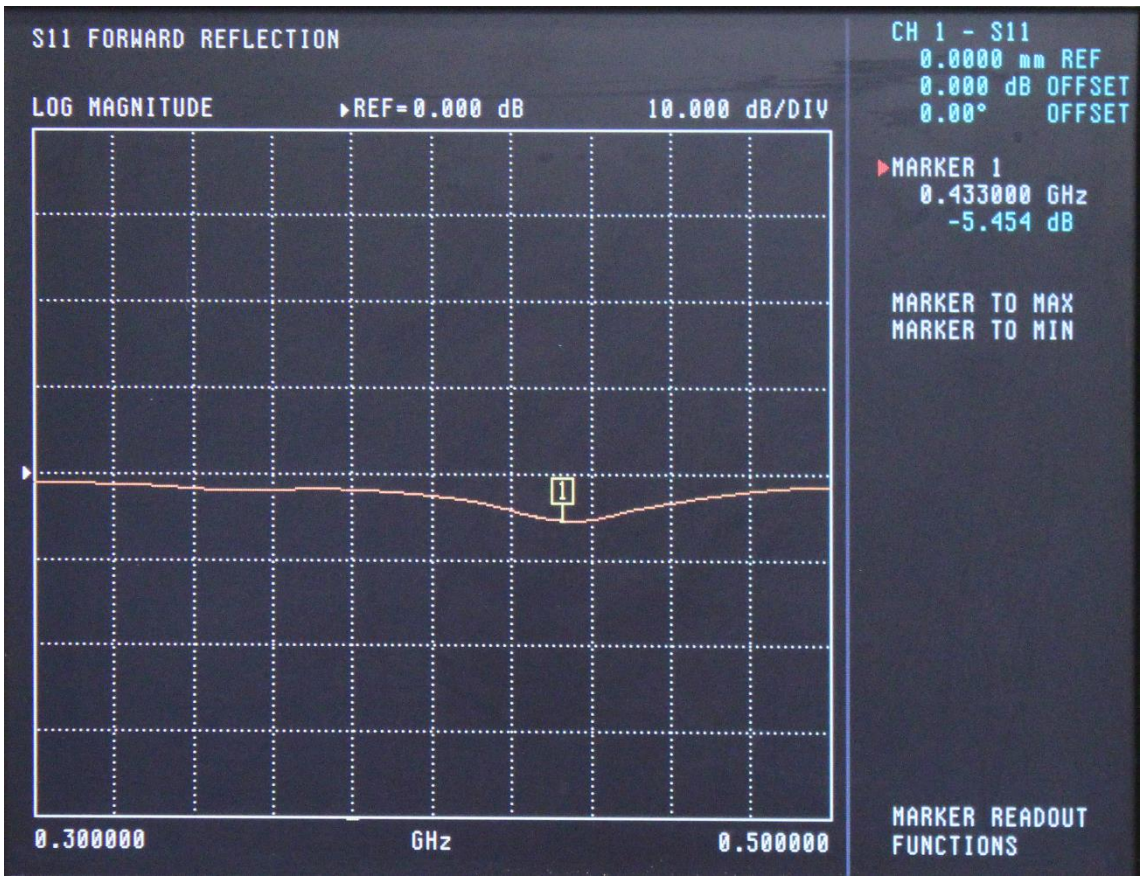

Fig. 9.3 First round of dipole tests, best value shown, at L = 37 cm. S11 = -5.454 dB (VSWR = 1.79) (-10.9 dB of reflected power).

After thinking about the PCB design, it was seen that the zone in which each active element of the antenna is soldered on, corresponds to a coplanar waveguide but with much different impedance as it changes drastically its width. After cutting the affected zone another round of tests were done with much better results. That affected zone can be appreciated on Fig. 9.4, in which a comparison between the previous original PCB and the machined PCB.

[13] Further information about VSWR: http://www.antenna-theory.com/definitions/vswr.php

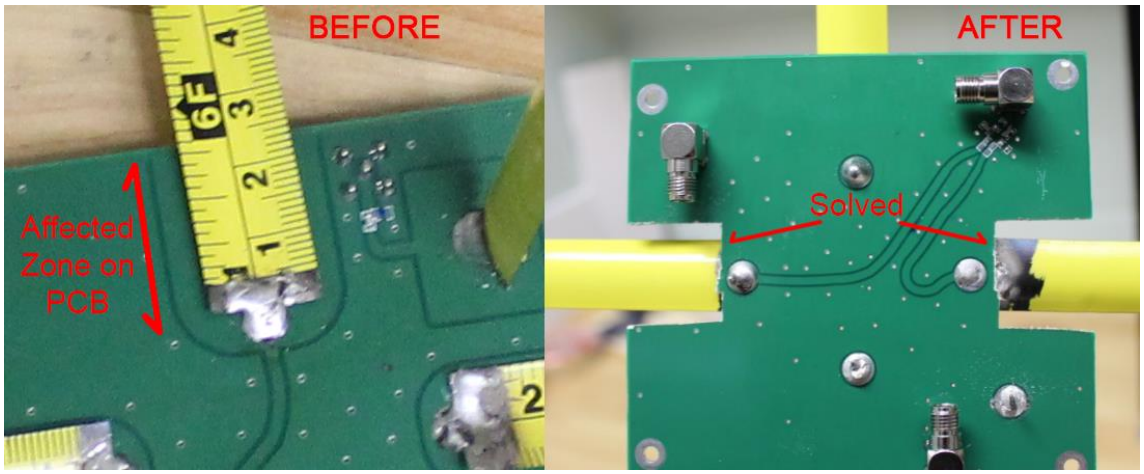

Fig. 9.4 After and before the machining of the unwanted section marked as "Affected zone on PCB". Machining should be done on both dipoles.

The second round of tests with that modification previously expressed was done for lengths 35 cm, 37 cm and 38 cm. The best result was also L = 37 cm but now with S11 = -24.9 dB, that stands for a VSWR = 1.006 with a reflected power of almost -50 dB which is a great result. The measurement graph is shown in Fig. 9.5, where it can be seen that it has even better results at 420 MHz with S11 = -30 dB. Fine tuning can be done in future iterations of the contest.

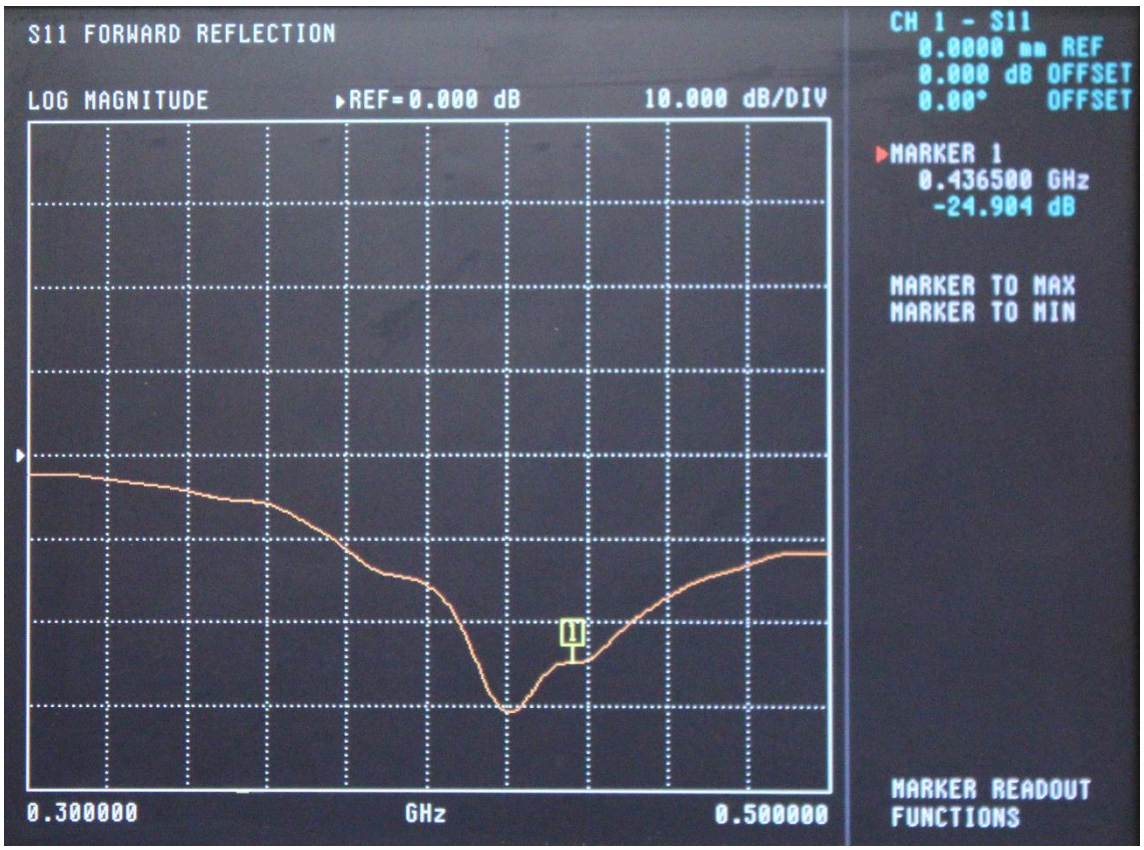

Fig. 9.5 Second round of dipole tests, best value shown, at L = 37 cm. S11 = -24.904 dB (VSWR = 1.006) (-49.81 dB of reflected power).

9.3.2. Test results – Monopole

The same measurements were done to the monopole antenna for lengths of 25cm, 23cm, 22cm, 21cm, 20cm, 19cm, 18cm, 17.5cm, 17.2cm (0.25λ). The best value is at 17.2 cm with S11 = -7.94 dB. VSWR = 1.433 which stands for a reflected power of about -15 dB. The obtained values are acceptable in the monopole case. From all the round of tests (all the results expressed on the Annex B) it can be seen that the firsts measurements at large length the S11 value improves down to -12.4 dB for 378 MHz. That suggests that the matching employed (from 50Ω to 36.5Ω) can be improved as the real impedance of the antenna differs from the theory.

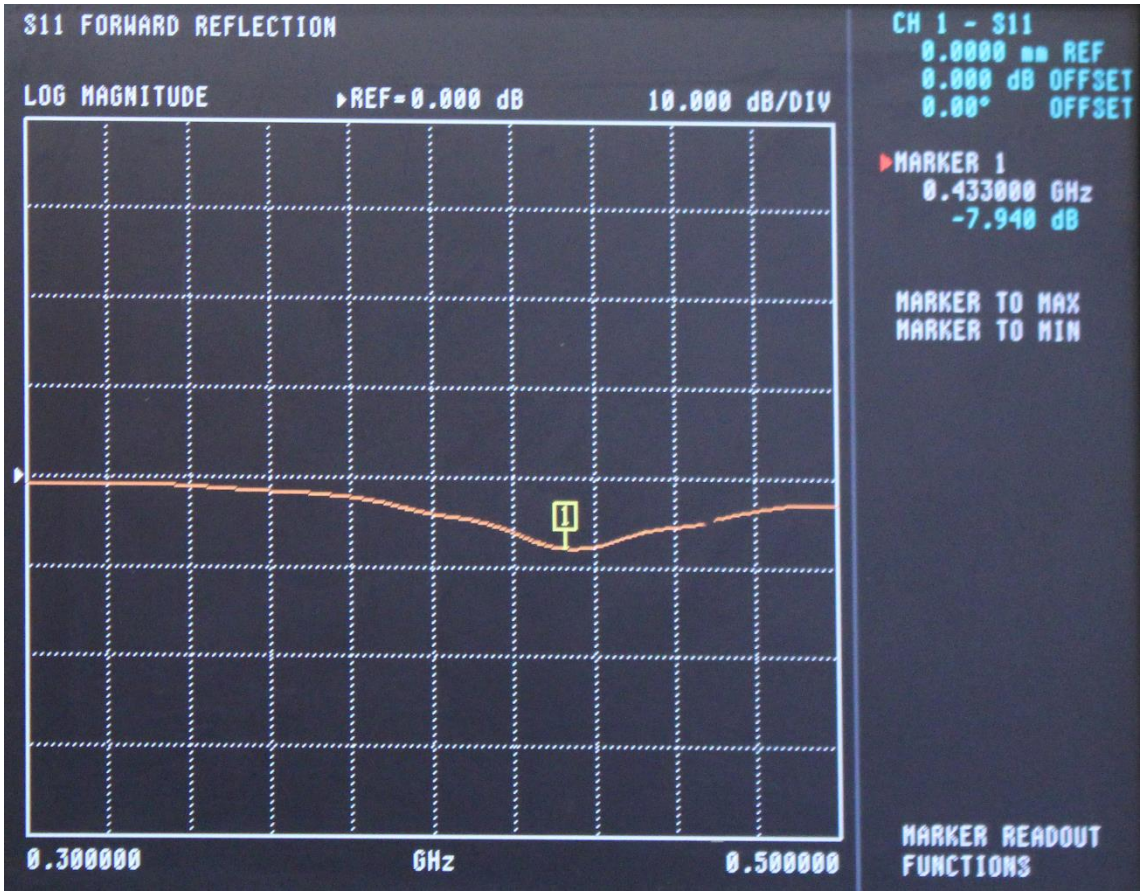

Fig. 9.6 Monopole round of test, best value shown, at L = 17.2 cm. S11 = -7.94 dB (VSWR = 1.433) (-15 dB of reflected power).

All the tests done to the antenna are done without the satellite structure. Properly tests and final tune should be done employing the satellite cage if the PCB is going to stay in the inside.

10. Conclusions

The fact that undergraduate students usually don't have enough formation about this ambit is why in this kind of challenges in which CubeSats have to be designed, telecommunications members chose to buy an already made transceiver which some brands provide by a really high cost up to 10.000$ per unit as it is seen on other Canadian CubeSat teams from the same contest. Even in Polyorbite, the same fact was recommended by the last telecommunication head member.

It is shown that within the two-year period that each iteration of the contest has it is more than enough to have a homemade system suitable to work for the satellite purposes with a relative low cost being under 1000$.

Nowadays there are plenty of solutions as extremely little transceivers that performs lots of complex functions as it is seen on this report, which simplifies the workload of the engineer a lot.

Even though there was not enough time to make properly tests and properly assemble it, with better communication with the other Polyorbite members and better engineering cost prediction, tests would be properly done. Being Polyorbite a non-profit organization but, things became difficult as important members appears and disappears and also people cannot spend much time on it specially while people have courses and exams to study.

Even though tests could be done on the beacon system and the antennas, further testing and study about the programming of the main system should be done.

The test results for the antennas showed very successful with really good and unexpected values for the dipole antennas, as few documentation is available online being the only available test of measurement tape antenna failed. It is shown that no deployment systems are needed to buy such as the "ISIS deployable antenna system" which costs the exaggerated sum of 4500€.

I hope this thesis to be useful as a basis for those interested on continue the study and design of the telecommunications system, especially for Polyorbite, to reach one day the space.

Escola d'Enginyeria de Telecomunicació i Aeroespacial de Castelldefels
UNIVERSITAT POLITÈCNICA DE CATALUNYA

ANNEXOS

TÍTOL DEL TFG: Telecommunications system of a CubeSat satellite

TITULACIÓ: Grau en Enginyeria d'Aeronavegació

AUTOR: Roger Cano Marí

DIRECTOR: Giovanni Beltrame

DATA: 29 d'Abril del 2016

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ANNEX A

ADDITIONAL DETAILS

1. Theoretical link study

A link study is done for our system taking into account the typical losses occurred on the atmosphere. This study but, is done into an early stage of this thesis, and corresponds mainly to the first version of the system. A version in which individual components like the SA606 is used as a RF demodulator and external filters are employed on it.

A well-made theoretical link study needs the properly specifications of each of the components like its noise figure and gain. Those were pretty expressed on the first version, in which the link budget is showed on section 1.5 of this annex.

Although it corresponds to a completely different system than the final one, the same values are taken into account as an approximate value when searching the transceiver, like the received noise power or the SNR ratio.

In the final design, this kind of theoretical link study does not apply, as not enough information is provided. Having available for the Si4460 transceiver just sensibility at a given data rate and transmitted power, and with the theoretical Eb/N0 to BER for a given modulation, an approximate “required transmitted power” is computed.

1.1. Transmission Losses[1]

The link study has to assure the required amount of power level at the receiver in order to understand the message send by the transmitter given an amount of power on it.

This transmitted power will be highly attenuated during the link due to losses which are given by different sources.

We can divide them into various sections: Propagation losses and Local losses.

1.1.1. Propagation Losses

Propagation losses can be expressed with 3 other types such as free space losses, atmosphere losses and pointing losses.

[1] All transmission losses formulas and pictures extracted from the publication PROTOCOL OF COMMUNICATIONS FOR VORSAT SATELLITE - Link Budget – by *Carlos Jorge Rodrigues Capela,* April 2012. Link: http://paginas.fe.up.pt/~ee97054/Link%20Budget.pdf

1.1.1.1. Free space losses

The free space loss depends on the distance between the ground station and the satellite. It is not the attenuation of the signal but the spreading of power emitted by an omnidirectional antenna.

The amount of Maximum power flux density at a certain distain r depends on the Power emitted and the gain of its antenna:

$$\psi_M = \frac{G_T.P_S}{4\pi r^2}$$

The EIRP that stand for Equivalent Isotropic Radiated Power is defined by the Gain of the Tx antenna and its power.

$$EIRP = G_T.P_S$$

Then the effective aperture of the receiver antenna is given by the Rx antenna gain, and the wave length landa.

$$A_{eff} = \frac{\lambda^2 G_R}{4\pi}$$

The received Rx power is then the product of the power flux density which contain the EIRP, the Rx gain and the Effective aperture of the Rx antenna:

$$P_R = \frac{EIRP}{4\pi r^2}\frac{\lambda^2 G_R}{4\pi}$$

$$P_R = EIRP.G_R.\left(\frac{\lambda}{4\pi r}\right)^2$$

Into the logarithm form with dB the formula can be written as:

$$P_R = EIRP + G_R - 10\log\left(\left(\frac{4\pi r}{\lambda}\right)^2\right)$$

From which $\lambda = c/f$, the last expression is the Free Space Loss (FSL) value:

$$FSL = 10\log\left(\left(\frac{4\pi rf}{c}\right)^2\right)$$

Where f is the frequency used, r the distance and c the speed of light.
As this study has to assure the link within the moment of sightseeing of the satellite at an elevation of 5º as we assumed on the chapter 2.1 the distance at this point between the satellite and ground station will be 2370 Km.

The frequency used is 436.5MHz. With this we can compute the FSL of each case. Given the frequency in MHz and the distance in Km the FSL expression becomes:

$$FSL = 32{,}4 + 20\log(r) + 20\log(f)$$

And it is obtained:

$$FSL_{DL} = 152.55\ dB$$

1.1.1.2. Atmospheric losses

This loss is due to the gases in atmosphere as they absorb energy of the link. Those can be due to ionosphere, troposphere and other local effects.

Ionosphere effects

Ionosphere layer contains ionized particles due to the sun radiation that causes signal fluctuations. Those that affects more into a CubeSat are the Polarization rotation and the Scintillation effects.

The polarization rotation causes a shift into the polarization within a Faraday rotation angle θ_F. This effect is reduced when the frequency is high. For a link at 500MHz the Faraday rotation angle can be as high as 360º[2]. Due to this effect for our frequencies forces us to use circular polarizations in order to assure the radio link.

But due to the complexity of a circular polarized antenna in front of a simple dipole linear antenna what it can be used is both polarizations at same link. Being a simple dipole at the satellite and a circular polarization antenna on ground will assure no Faraday rotation effect and a simple antenna mounted on the satellite. However, this will cause a polarization loss of 3dB as shown into the table Fig 2.1.

Transmit Antenna Polarization	Receive Antenna Polarization	Ratio of Power Received to Maximum Power		
		Theoretical	Practical Horn	Practical Spiral
		Ratio in dB	Ratio in dB	Ratio in dB
Vertical	Vertical	0	*	N/A
Vertical	Slant (45º or 135º)	-3	*	N/A
Vertical	Horizontal	-∞	-20	N/A
Vertical	Circ (RHCP/LHCP)	-3	*	*
Horizontal	Horizontal	0	*	N/A
Horizontal	Slant (45º or 135º)	-3	*	N/A
Horizontal	Circ (RHCP/LHCP)	-3	*	*
Circ (RHCP)	Circ (RHCP)	0	*	*
Circ (RHCP)	Circ (LHCP)	-∞	-20	-10
Circ (RHCP/LHCP)	Slant (45º or 135º)	-3	*	*

Fig. 1.1 Polarization losses for different polarizations in antennas[3]

[2] Faraday effect https://en.wikipedia.org/wiki/Faraday_effect [13/10/2015]
[3] http://paginas.fe.up.pt/~ee97054/Link%20Budget.pdf [13/10/2015]

$$L_{pol} = 3dB$$

This will not be a loss caused by the atmosphere but caused due to apply the solution that fixes the problem of the Faraday angle induced by the atmosphere at the polarization that makes the linear polarization impossible to be used in both satellite and base station antennas.

The scintillation effects are due to differences in the atmospheric refractive index that provokes scattering and multipath effects. Those are often taken into account into the link study as a Fade margin. As they are infrequent over EEUU, south of Canada and Europe we can depreciate this type of loss[4].

Tropospheric effects

Troposphere is composed by miscellany of molecules of different compounds such as rain, hail and other gases. The scatter suffered into various directions of the signal due to troposphere is a problem with frequencies higher than 10GHz, so it does not represent a problem for our CubeSat.

The rain attenuation can cause severe attenuations in heavy rain situations. Those are punctual cases for the typical weather of Canada so are not taken into account. Also there is more than one opportunity every day for contact with the satellite.

The gas absorption due to oxygen and water vapor vary with frequency and is given by the graph on Fig. 2.2.

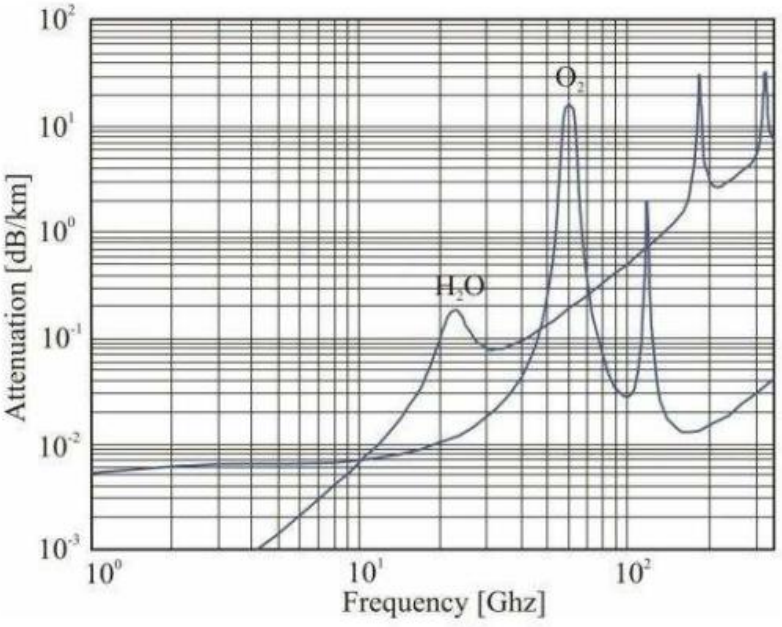


Fig. 1.2 Attenuation due to gas absorption vs Frequency of Oxygen and Water.

[4] Scintillation map showing that the effect is least frequent at mid-latitudes and maximum at the equator zone. http://www.insidegnss.com/auto/popupimage/Sun_Figure_1.jpg [13/10/2015]

At our frequencies the water vapor absorption effect will be null and the oxygen effect very low at a value of approximately 0.004 dB/Km. Taken into account the troposphere thickness of 20km at maximum elevation angle of 90º the loss is minimum and its value is 0.08 dB. For lower angles, the atmospheric absorption is given by:

$$L_{abs}\,(dB) = L_{abs|90^o}\,(dB/km)\ \mathrm{cosec}\ \theta\ .\ T_{trop}\,(km)$$

Where $L_{abs|90º} = 0.004\ dB/Km$ and $\theta = 5º$ for the most restrictive case when satellite arises the horizon. Then it is obtained a maximum of:

$$L_{abs,max} = 0.91\ dB$$

So we will assume a loss of 1dB due to the oxygen absorption.

The Elliptical Polarization effect will affect the desired circular polarization. Depolarization occur when an orthogonal component is created due to the passing of the signal through the ionosphere. It can be measured by two ways: cross polarization discrimination (XPD) and polarization isolation (I).

The rain and ice depolarization will just cause an addition of rotation to the circular polarization, so this one will not affect our link.

1.1.1.3. Pointing losses

This term refers to the misalignment of the antennas at ground station and satellite. The perfect alignment will cause 0dB of loss. But due to the high speed of the satellite this is nearly impossible. This can be computed by the off-axis loss at the satellite or at the Ground Station.

Because of the satellite will cannot be aligned specifically for the transmission of data due to its ionic propulsion mission the antenna onboard the satellite has to be near omnidirectional as possible.

Then the misalignment effect will be computed over the directional antenna on GS (Ground station). It is usually quite small, not reaching ever 1dB being it a good approximation based on real data in several GS.

$$L_{aml} = 0.91\ dB \rightarrow 1dB$$

1.1.1.4. 3.2.2 Local losses

Referred to loss in quality in ground station. The equipment losses are due to the equipment used. For the link study we are using directly EIRP values so those are already taken into account within the transmitter and receiver features.

1.1.1.5. 3.2.3 Other impairments

Sun outage is caused when the satellite is obscured by the sun. This causes about 100 minutes per year of negative consequences for geostationary satellites but not for LEO satellites.

The total propagation losses then are given by the sum of the previously named losses.

$$L_{prop} = FSL + L_{abs} + L_{pol} + L_{aml}$$

For downlink and uplink cases we obtain:

$$L_{prop} = 157.55\ dB$$

1.2. System noise

The system noise T_S is the sum of the antenna noise temperature T_A and the noise temperature of the other components.

$$T_S = T_A + T_{comp}$$

1.2.1. Antenna noise temperature

T_A may be known if the total attenuation due to rain and gas absorption (A), the temperature of the rain medium (T_m) and the temperature of the cold sky (T_C) are also known. Then, the following expression may be applied:

$$T_A = T_m\,(1 - 10^{-A/10}) + T_C \cdot 10^{-A/10}$$

Where usually, for clouds it is considered $\boldsymbol{T_m = 280\ K}$ and for rain $T_m = 260\ K$. Then the clouds case is taken for the most restrictive case.

T_C is given by the sky noise and for the downlink case when its noise enters to the GS antenna is for 437MHz about $\boldsymbol{T_C}$ **= 120 K** according to this graph:

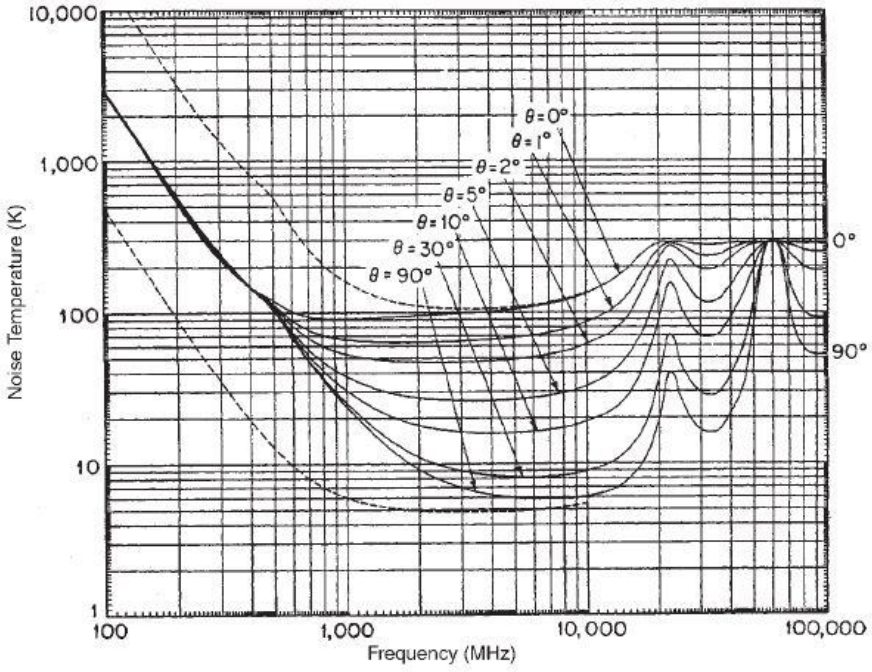


Fig. 1.3 Antenna sky temperature.[5]

With those values the antenna temperatures for uplink and downlink are:

$$T_A = 280\left(1 - 10^{-\frac{1}{10}}\right) + 210 \cdot 10^{-\frac{1}{10}}$$

$$T_A = 224\ K$$

1.2.2. Components noise temperature

In order to compute T_{comp} it is necessary to determine the effective noise temperature and the gain of each stage of the system.

Noise Figure that measures the degradation of Signal-to-Noise ratio between the entry and exit of a component or group of components is used for compute the equivalent noise temperature of the system. The value of Noise Figure is given on datasheets for each components, where also Gain or Insertion Losses for the case of filters is found.

---

[5] Antenna sky temperature http://www.antetec.com/news/2010/02/01-377.html [13/10/2015]: Noise T of an idealized antenna located at earth surface as a function of frequency. Solid curves are for geometric-mean galactic temperature, sun noise 10 times quiet level, sun in unity-gain side lobe, cool temperate-zone troposphere, 2.7K cosmic blackbody radiation, zero ground noise. The upper dashed curve is for maximum galactic noise (center of galaxy, narrow-beam antenna). Sun noise 100 times quiet level, zero elevation, other factors the same as solid curves.

The Friis formula allows us to compute the total equivalent noise figure:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}$$

And then the effective noise temperature depends on the total noise figure (F) and the reference temperature (T0) which is 290K, according to this relation:

$$T_N = (F - 1)\, T_0$$

Those values are computed taking into account each component selected for the version 1 system. The computations are made on the chapter 2.2 of this annex. The temperature noise values are:

$$T_{comp} = 136K$$

Then the total system temperature is computed:

$$T_S = 224K + 136K = 360K$$

1.2.3. Noise Bandwidth Calculations

The noise bandwidth of a receiver usually is taken as the bandwidth of the narrower filter. In order to achieve the best Signal-to-Noise ratio then it is important to have filters with the minimum possible bandwidth according to the type of signal we are going to transmit and in the case of high speed scenarios like satellites, the Doppler shift effect, as it has not an Automatic Frequency Control implemented.

In our case (last V1 system) this determining filter are the IF filters contained between the two IF sections of the Superheterodyne receiver SA606 employed which are analyzed on the next section 2.2.1.4.

GMSK signals like MSK its power spectral density have a main lobe width of 1.5 times the bitrate employed.

For 4800 bps we have a signal with a bandwidth of 7200 Hz.

The required system bandwidths taking into account the Doppler shift computed before on chapter will be:

$$BW \quad = 7200Hz + 2 \cdot 10kHz = 27200\ Hz \approx 30\ kHz$$

We will need into every link almost one filter as narrower as those values in order to achieve the minimum noise power into the discriminator.

1.3. Antenna Gain

The gain of the antenna at the satellite is given by its type of antenna. As it is used two dipole antennas, one for each link, with a gain of 2.14 dB we will have:

$$G_{R,UL} = G_{T,DL} = 2.14\ dB$$

For the ground station high gain circular polarization antennas are required.
The most suitable are Yagi antennas, named Cross Yagi antenna for the circular case. Those are really easy to achieve inclusive homemade ones with just a plastic tube, wires, a connector and the dimensions of it.

At the market we can obtain a 14 / 18 elements Cross Yagi antennas for 2m and 70cm bands that achieves gains of 15 and 14 dBi respectively[6].

1.4. BER

Eb/N0 represents the amount of energy bit over noise power and it is essential for compute the BER or Bit Error Rate.

BER is the amount of errors per bit occurred in a digital transmission. And in order to have a good link BER has to be a small value. The relation between BER and Eb/N0 is given by the modem specifications. From the datasheet of the CMX909B we can obtain for this graph:

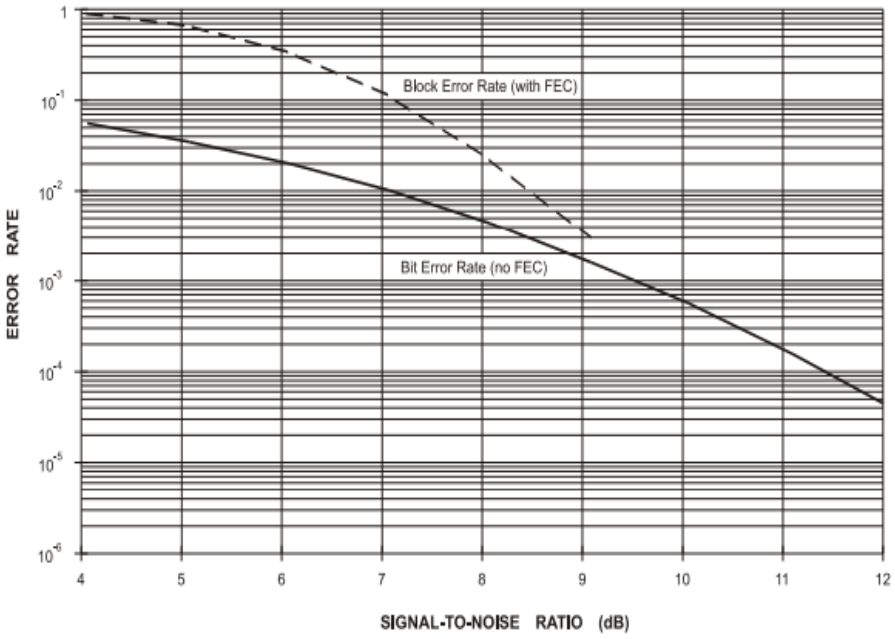


Fig. 1.4 BER vs. SNR from the CMX909B datasheet.

[6] Yagis WiMo pour 2m and 70cm http://www.wimo.de/yagi-antennes-wimo_f.html [13/10/2015]

And an approximately BER = 10^-5 we can expect an Eb/N0 = 13dB. If we use the FEC mode on the modem we can obtain better values at lower Eb/N0. For example, with Eb/N0 = 9 we have 3*10^-3 of Block Error Rate where each block is composed by 32 bytes and then this value of Block Error Rate is approximately equivalent to BER = 10^-5.

Known the amount of Noise Power received computed before, the received power and the Data rate we can obtain the downlink margin:

$$BER \rightarrow Required\,\frac{\boldsymbol{E_b}}{\boldsymbol{N_0}} = Req\,\frac{S}{N}\cdot\frac{B}{R_b}$$

$$M_D = \frac{E_b}{N_0} - Req\,\frac{E_b}{N_0} = \frac{S}{N} - Req\,\frac{S}{N}$$

Power Noise is obtained from the Noise chapter from which is:

$$N = KT_SG_RB$$

Where K is the Boltzmann constant, Ts the Noise temperature system, Gr the gain of the receiver antenna, S the received power and B the bandwidth of the narrower filter on the receiver.

$$N = -156.1\ dBW = -126.1\ dBm$$

Combining the two previous formulas and the relation between emitted and received power we can eliminate the Bandwidth and compute the required transmitted power that it's needed in order to comply with the introduced values:

$$P_{TX-req}[dBW] = \frac{E_b}{N_0} - G_{TX} + L_{prop} + 10\log(K\cdot T_S\cdot R_b)$$

Thanks to this formula some changes are made from the initially sketched link of 9600 bauds. As the satellite antenna has a gain of 2.16 dB, the required Eb/N0 is 9dB and the propagation losses, Boltzmann constant and Temperature noise are computed invariant constants it is seen that in order to achieve 9600 bauds on the downlink it's needed a transmission power on the satellite of 1.31W which is really high taking into account that is without any fading margin.

For the 13dB of Eb/N0 in order to obtain 10^-5 BER without using the FEC mode it is needed 3.28W on the satellite which it is even more impossible.
Some change has to be done for assure the downlink. One of the possible solutions is incrementing the Gain antenna of the satellite but due to the necessity of any attitude for the ionic propulsion mission no antenna pointing can be done so we need the omnidirectional 2.16 dB antenna.

The other possibility is to reduce the bitrate R_b down to 4800 bps. Which this and 1W of power at the satellite transmitter we achieve an Eb/N0 value of 10.8 dB at ground station, sufficient for the FEC mode.

Another possibility would be decrease the receiver IF filter's bandwidth down to the bandwidth of the GMSK signal without taking into account the Doppler shift. For that it is required an AFC function that constantly modifies the value of the Local Oscillator on the Superheterodyne receptor correcting the Doppler shift.

This requires but a controllable oscillator (not enough precise as a XTAL one) and an external program managed by a computer software. It would decrease the complexity of the system too much.

1.5. Link Budget

Once computed the losses and equivalent noise temperatures we can compute which power is required for transmission in order to achieve a good link.
The received power of each case will be given by:

$$P_r = EIRP - L_{prop}$$

The emitted power is mainly given by the Power amplifier installed on both satellite and GS. For the downlink taken into account that a SKY65116 3W 35dBm PA is used at the satellite then we have:

$$P_{r-DL} = 30dBm + 2.16dBi - 157.55dB = -111.39dBm$$
$$P_{r-UL} = 40dBm + 14dBi - 147.97dB = -90.8dBm$$

The required transmitted power for both cases in order to achieve an Eb/N0 of 9dB is then:

$$P_{TX-DL} = -1.833\ dBW = 28.16\text{dBm} = 0.65\text{W}$$
$$P_{TX-UL} = -23.52\ dBW = 6.477dBm = 0.0044W$$

The huge difference between both that seems contradictory (as Ground Station needs less power) is due to the Gain of the transmitter antenna. As what is critical here is the Signal-to-Noise ratio at the receivers rather than the level of strength of each signal. Though this last has to be taken into account in order to comply with the Sensibility of each demodulator SA606.

Nothing on the receivers can be done in order to improve the SNR received as any amplifier or gain on the receiver antenna will increase the level of power of both signal and noise power at the same value. Transmitter is who determines the received SNR.

UPLINK BUDGET		
Parameter	Value	Unit
Frequency	145	MHz
Boltzmann constant	1.380658E-23	J/K
Bitrate Rb	4800	Bauds
Bandwidth BW	15	kHz
Relation BW/Rb	4.95	dB
Gain receiver antenna	2.16	dBi
Gain transmitter antenna	15	dBi
Noise power		
Antenna Temperature	290	K
Components Temperature	136	K
Total system Temperature	426	K
Noise power	-115.5	dBm
Transmitted power	10	W
	40	dBm
Propagation losses	147.97	dB
Received Power	-90.8	dBm
Minimum receiver Eb/N0	9	dB
Received SNR	**24.7**	**dB**
Received Eb/N0	**29.7**	**dB**
Fading Margin	**20.64**	**dB**

DOWNLINK BUDGET		
Parameter	Value	Unit
Frequency	437	MHz
Boltzmann constant	1.380658E-23	J/K
Bitrate Rb	4800	Bauds
Bandwidth BW	30	kHz
Relation BW/Rb	7.95	dB
Gain receiver antenna	14	dBi
Gain transmitter antenna	2.16	dBi
Noise power		
Antenna Temperature	244	K
Components Temperature	136	K
Total system Temperature	360	K
Noise power	-114.26	dBm
Transmitted power	1	W

	30	dBm
Propagation losses	157.55	dB
Received Power	-111.39	dBm
Minimum receiver Eb/N0	9	dB
Received SNR	**2.87**	**dB**
Received Eb/N0	**10.82**	**dB**
Fading Margin	**1.82**	**dB**

Although the fading margin is really low on the downlink case it has to take into account that those computations are made over the worst case in which the satellite is over 5º of the horizon with pointing errors, polarization errors and the maximum height orbit.

An advantage is the high fading margin of the uplink where it is important due to the criticality of the command operations on the CubeSat computer.

1.6. Final link budget

Given the available information about the Si4460 transceiver it can be concluded just that its sensibility for a BER (Bit error rate) less than 0,1% at a speed and modulation that fits our purposes is:

Sensibility	**Bitrate**	**Modulation**
-127 dBm	500 bps	GFSK
-109/-107 dBm	40 kbps	GFSK

Given the path loss computed in previous sections, at 437 MHz and given the distances that the satellite has with the ground station (which varies depending on its elevation) it is computed the total losses for each elevation:

Loss	**Elevation**
157.55 dB	10º
155.21 dB	20º
151.5 dB	40º
150.3 dB	50º
148.31 dB	90º (800 Km)

Analyzing the Output power of the satellite:

$$Pt_{SAT} = 33 \text{ dBm } (2W)$$

The received power at the ground station is then:

Pr_{GS} = 33 dBm + 2.14 dBi – 157.55 dB + 14 dBi = **-108.41 dBm** @ EL=10º

Doing the same for each elevation it is found the received power for all the pass:

Power received @ 2W	**Elevation**
-108.41 dBm	10º
-106.07 dBm	20º
-102.36 dBm	40º
-101.06 dBm	50º
-98.97 dBm	90º

As it can be seen, the link assures almost -108 dBm of transmitted power between 10º and 10º of elevation, which is almost during all the pass. Given the stated sensibility of the transceiver of about -107 / -109 dBm working at 40 kbps, it can be assured that transmission at this bitrate is possible. Maybe not just at 10º, but more than enough near the zenith.

At 40 kbps the total amount of data collected in one day is sent with just a burst of 14,1 seconds which is interesting as with the high consumption of 5W leads to just 19.6 mWh of energy consumed per message.

Using a higher bitrate has high benefit, as the consumption of the Power amplifier does not depend of the bitrate, and given the first stated speed of 9600 bps would last 1 minute per message with about 8 times more consumed power.

2. Previous system designs

2.1. Modulation

Modulation of the binary digital data is needed in order to be send into a RF high frequency format. What is mainly done in modulation is conveying a message signal (lowpass signal), for example a digital bit stream, inside another signal that can be physically transmitted called carrier signal. The result is the RF signal called modulated signal.
As already mentioned the modulation used will be GMSK. In order to explain that it's needed to mention its origin, FSK.

2.1.1. FSK - Frequency Shift Keying

Which is the digital variant of FM modulation, consists on different changes on frequency for distinguish between the digital symbols. The simplest FSK is BFSK or Binary Frequency Shift Keying has two different frequencies that expresses the digital binary 1 or 0.
This is represented on Fig. 2.1.

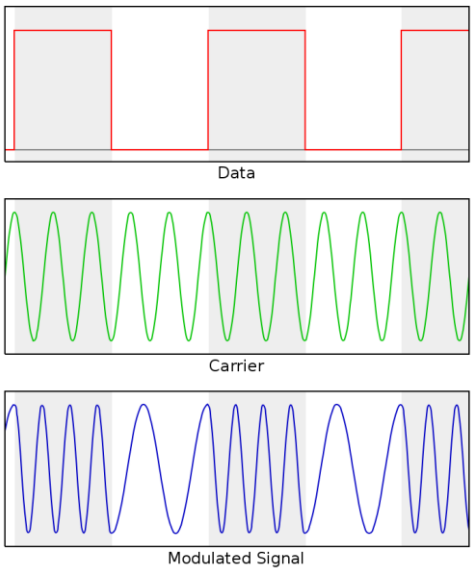


Fig. 2.1 FSK modulation scheme[7].

2.1.2. MSK - Minimum Shift Keying

Being a spectrally efficient form of FSK, de main difference between FSK is that where the frequency change of FSK is instant in time, the MSK scheme changes its frequency linearly during the entire bit period. In MSK the signal is not represented by two static frequencies, but by a continuous phase change on center carrier. This fact reduces the occupied bandwidth by ½ compared with FSK. In a more visual way, the input binary square pulses are transformed to each bit as a half sinusoid.

[7] Image: https://en.wikipedia.org/wiki/Frequency-shift_keying

2.1.3. GMSK - Gaussian Minimum Shift Keying

It consists on a variant of MSK where the digital data stream is first shaped with a Gaussian filter. This has the advantage of reducing sideband power. It is widely used in GSM communications and AIS.

This is the primary thought modulation to use in the V1 and V2 systems. In the final but, the Si4460 transceiver the available modulations are (G)FSK, 4(G)FSK, (G)MSK and OOK, where (G) means the possibility of using the Gaussian version of the modulation.

As the best receiver performance and channel modulation spectrum is the GFSK[8], that will be used for our purposes. GMSK can be used also by just changing the modulation index to h=0.5 while using GFSK.

The Gaussian filter improves the spectral efficiency given that it juxtaposes multiple radio channels over the frequency channel minimizing it. The drawback is the interference between symbols as expressed on the Fig. 2.2 right in which one bit of Tb time is expanded depending the BT value. BT is related to the filter's 3dB bandwidth and the data rate used by:

$$BT = \frac{f_{-3dB}}{BIT\ RATE}$$

Usual BT values are 0.5 and 0.3 as it's used on GSM data and AIS marine services.

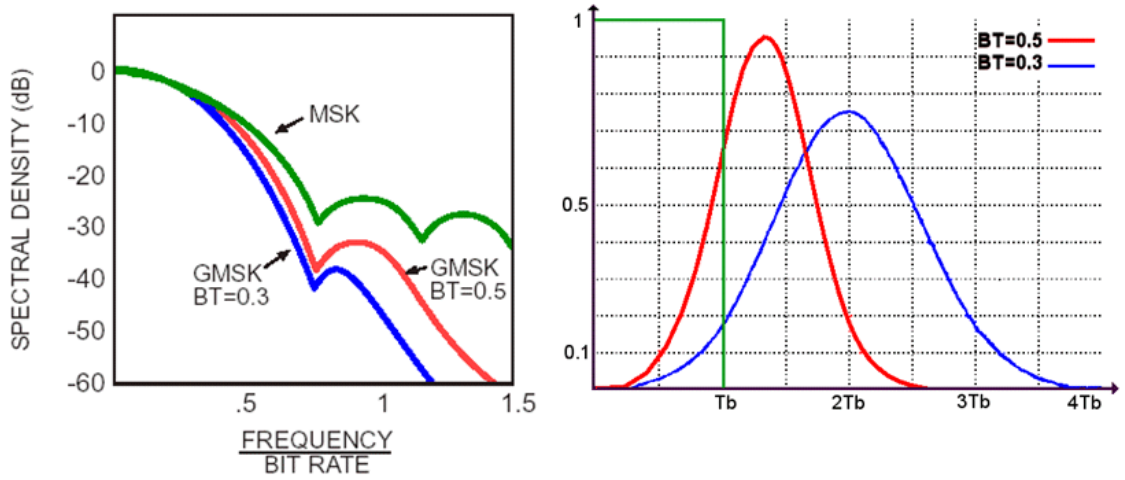


Fig. 2.2 Comparison of spectral density by using Gaussian filter in left and bit form in right.

Further information about GMSK can be found on the Application note "Practical GMSK Data Transmission by MX-COM inc.[9]

[8] Si4463/61/60-C datasheet page 24.
[9] Practical GMSK Data Transmission http://sss-mag.com/pdf/gmsk_tut.pdf

2.2. V1 System design study (outdated)

Although anything of the first version of the system is not used in the final design, the made study is included here on the annexes in order to make sense for the theoretical link study.

It is 100% based on the master thesis “Study of a 145 MHz Transceiver” made by Roger Birkeland of the Norwegian University of Science and Technology at 2007.

Parallel with the theoretical link the design of the system is done as it is needed to know the specifications of each component in order to compute the link budget.

After a meeting with the Data Handling group of the Hathor project the telecommunication system is simplified as the microcontroller is no longer needed to control the GMSK CMX909B. Instead, the 12 lines that contains data and control signals to the modem are headed into 12 pins on the shared CubeSat bus P/C 104. The modem is managed directly with the Hathor’s On Board Computer so the programming part of the modem is no longer telecommunication’s group task.

The analysis has to be done for both hardware implemented on Satellite and Ground Station. As it is used the same system conception, both will be implemented by similar components. The analysis can be divided by input and output sections of each system.

2.2.1. Input Section

The input section is composed by the receiving antenna, an amplifier, some filters a mixer and the demodulator that converts RF signals to Baseband. This can be seen on figure Fig. 2.3.

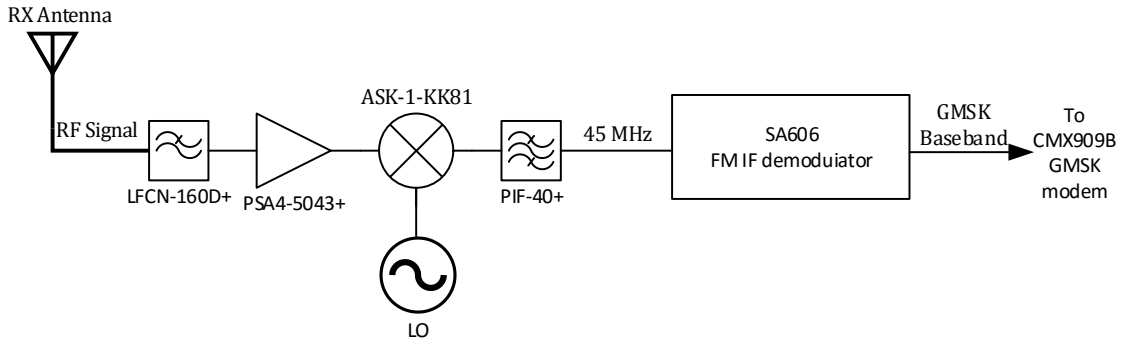


Fig. 2.3 V1 receiver diagram.

2.2.1.1. Amplifier

The Low Noise Amplifier selected from Minicircuits PSA4-5043+ gives a Gain of approximately 25.4dB and 23dB on the input over the RF signal for the respectively frequencies 145MHz and 437 MHz. Its Noise Figure is 1.161 suitable for Low Noise processes.

2.2.1.2. SA606 Demodulator

SA606 from NXP consists on a Low-voltage high performance mixer FM IF system. It is a Superheterodyne FM demodulator that combines all the mixers, IF amplifiers and a quadrature detector inside a same chip.

The total Gain of the chip is around 90dB being its IF input sensitivity of -109 dBm. IF filters, an oscillator, matching circuits and other components has to be added around the SA606 in order to make it functional. Those are given into the datasheet and a diagram can be seen on figure Fig. 2.4.

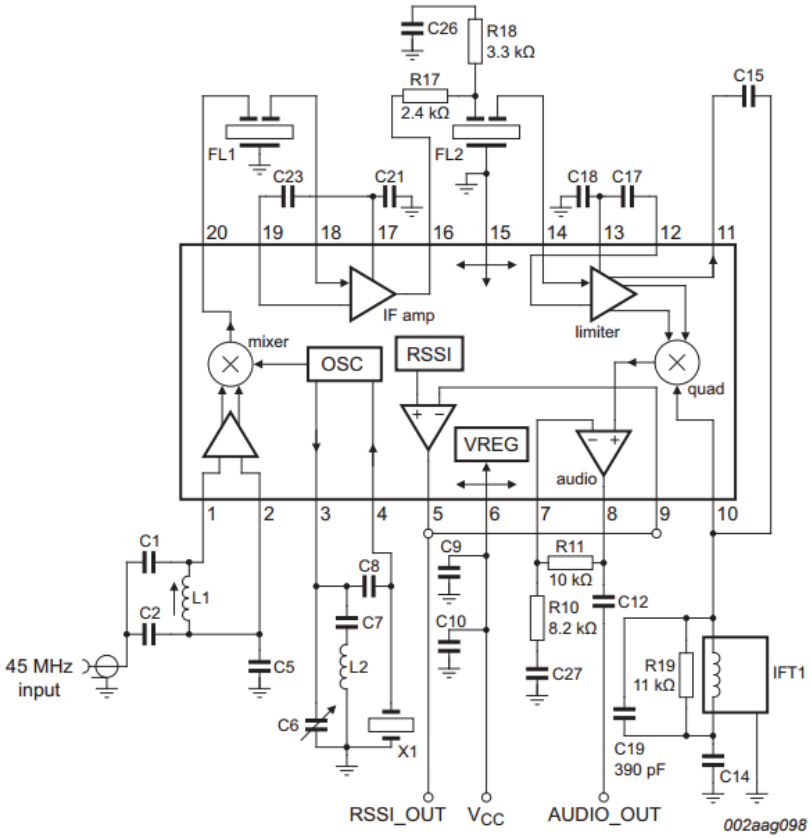


Fig. 2.4 SA606 receiver configuration as expressed on its datasheet

It consists on a demo board layout for an input RF signal of 45MHz and it is recommended to use the same circuit as the performance of the receiver is very critical. Apart of the resistors, capacitors and inductors there is two IF filters (Band Pass Filters) marked as FL1 and FL2 that will determine the total Bandwidth of our receiver for the Noise Power computation. An IF oscillator marked as X1 is used for down convert the 45 MHz signal to the standard IF frequency of 455 kHz using its internal mixer with an oscillator of 44.545 MHz.

Two IF stages amplifies the 455 kHz signal with the IF amp and the limiter with a total of 102dB but due to the IF filters between those it will decrease its total gain down to 86dB for the uplink case and 90dB for the downlink case due to the insertion losses of both filters and the matching at 1500 Ω for the 1000 Ω 30kHz filter at uplink. Matching needed as shown at the SA606 datasheet. The 15 kHz filter is already adapted with 1500 Ω.

Then a quadrature detector will convert the 455 kHz FM signal to the GMSK baseband signal named as “Audio signal” on the scheme.

A conceptual scheme of the SA606 demodulator is given by figure Fig. 2.5 where the previous stages are showed in a linear way.

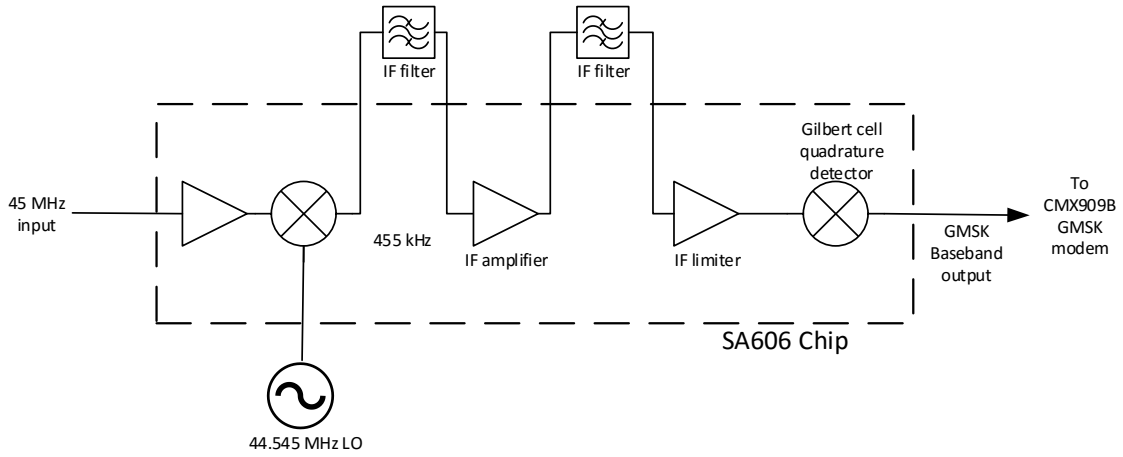


Fig. 2.5 SA606 Conceptual scheme

2.2.1.3. Mixers and oscillators

Two mixers and two oscillators are used for down convert the signal during the process. The first one pair of mixer-oscillator down converts the RF signal from its frequency to 45MHz and the other down converts the 45MHz to the IF frequency of 455 kHz.

The first one is composed by the ASK-1-KK81 Frequency Mixer from Minicircuits. It has a conversion loss of 5.14 dB at 166.24 MHz and it requires a 7 dBm Local Oscillator signal. For the downlink case it has a conversion loss of 5.57 dB at 455.51 MHz, so it will be useful for both cases.

The second one mixer is included into the SA606 chip in which just a 44.545 MHz oscillator has to be added for the down-conversion to the IF frequency of 455 kHz. The mixer includes an amplifier with a gain of 2.14 dB and a total Noise Figure of the both mixer-amplifier of 6 dB. The oscillator shown on the datasheet is a 44.545 MHz crystal ICM4712701 model (which is no longer available).

One of the conclusions of the Master Thesis 145MHz Transceiver from which the concept is taken is the needing of enough precise oscillators. The ideal ones are XTAL oscillators which consists on mechanical resonators that has to be made specifically for the exact frequency that one needs to work without the possibility of vary it. In the thesis it is not included any test with oscillators due to that the official link frequencies of the satellite are not given until it is nominated to be launched. So dynamic resonators are taken on this project in order to just be able of test it.

2.2.1.4. Filters

The input system has several filters designed for erase all the other undesired signals of the band as much as possible including the noise.

2.2.1.4.1. Uplink BPF LFCN-160D

The first one filter consists on a Low Pass Filter. Ideally a Band Pass Filter is used but due to the high performance vs size of the component respect to a BPF a LPF is used.

For the uplink case a LFCN-160D+ from Minicircuits is used which has a 160 MHz bandwidth and an attenuation of 0.77 dB at 150 MHz known as Insertion Loss. As it is a passive element the Noise Figure is equivalent to its loss.

2.2.1.4.2. BPF PIF-40+

After downconverting the incoming RF signal from 145MHz to 45MHz with the first mixer, it is used a band pass filter that will enhance the input signal to the demodulator.
Its bandwidth is 14MHz working from 35 to 49 MHz being suitable for our 45MHz pre-IF signal. IT has an Insertion Loss (and so Noise Figure) of 0.31dB at 45MHz.
This component is used on both uplink and downlink cases.

2.2.1.4.3. BPF IF filters

After each IF amplifier of the SA606 an IF filter is added being the ones who determines the Power Noise level. So the most possible narrower has to be implemented.

On the previous section it is computed the total bandwidth needed in order to have the signal into the band taking into account that it will shift due to the Doppler Effect during the satellite's pass. This bandwidth results 30 kHz and 15 kHz for the downlink and uplink respectively.

The filters shown on the same SA606 datasheet are CFUKF455KB4X-R0 from Murata. Those are 30 kHz BW 455 kHz filters with 5dB of insertion losses ideal for the downlink case.

For the uplink case the model CFUKF455KE1X-R0 of same brand with 15 kHz BW and 8dB of Insertion Loss is chosen.

2.2.1.5. Specifications

UPLINK – INPUT SAT			
Part	**Name**	**F`[linear][dB]**	**G [linear][dB]**
LPF	LFCN-160D+	1.193	0.838
LNA	PSA4-5043+	1.161 / 0.65 dB	346.73 / 25.4 dB
MIXER	ASK-1-KK81	3.981 / 5.14 dB	/ -5.14 dB
BPF	PIF-40+	1.073	0.931 / -0.31 dB
SA606 – MIX/OSC		4.168 / 6dB	1.778 / 2.5 dB
SA606 – IF amp		+0.2dB	44 dB
SA606 – IF limiter			58 dB
BPF x2	CFUKF455KE1X-R0	/ 8dB	-8 dB
	TOTAL	1.4697	108.806 dB
	EQ. TEMP	136.21 K	

DOWNLINK – INPUT GS			
Part	**Name**	**F`[linear][dB]**	**G [linear][dB]**
LPF			
LNA	PSA4-5043+	1.161 / 0.65 dB	199.52 / 23 dB
MIXER	ASK-1-KK81	/ 5.57dB	/ -5.57dB
BPF	PIF-40+	1.073	0.931 / -0.31 dB
SA606 – MIX/OSC		4.168 / 6dB	1.778 / 2.5 dB
SA606 – IF amp		+0.2dB	44 dB
SA606 – IF limiter			58 dB
BPF x2	CFUKF455KB4X-R0	/ 5dB → 6dB	-5 dB → -6dB
	TOTAL	-	-
	EQ. TEMP	-	-

With those values it is computed then the link budged of previous chapter 1.5 of this annex.

2.2.2. Output Section and amplifiers

The output section of each system is simpler than the input and consists basically on a mixer and oscillator that modulates the baseband GMSK signal up to the desired RF frequency, some amplifiers, filters and the transmitter antenna.

Two amplifiers are employed. The first one called buffer amplifier grows up the already modulated signal to a suitable one for the second one Power Amplifier that will deploy the wanted power level of the transmitter.

2.2.3. End of the V1 study

Up until this point of the partial study, it was decided to stop and focus the system to another type of system as this one had too much unknown parameters.

Such as the real bandwidth use. This system, is composed by SA606 which consists on a FM demodulator. The input should be an FM audio signal, which in our case the audio consists on digital data, modulated by the CMX909B modem.

The real bandwidth of the transmitted is not the stated by the CMX909B GMSK signal, but the final one once FM modulated in high frequency, which depends on the modulation index, and walls out of the computed noise bandwidth. In this case, the link computations are of no use.

That is why an alternative to the FM is searched and leads to the V2 system.

2.3. V2 system main view (outdated)

As expressed before, in order to avoid this kind of audio – FM modems, another solution is searched for the up and down conversion in frequency, of the GMSK signal created by the CMX909B modem.

A type of transceivers called I/Q modulators where found on the same website than CML circuits.

For example, it was found the next suitable components:

- CMX7164 digital chip modem modulates the binary data to GMSK (with more functionalities than CMX909B modem, and suitable to use with the CML transceivers.
- CMX994 and CMX998 chips acts as a I/Q Transceiver and Receiver up and down-converting the GMSK signal to the required frequency.

Both chips where not available for small quantity purchases and CML refused to provide the extended versions of the datasheets, necesary to programme those.

Up to this point, with just 6 month ahead, a completely new type of system, easier to made and based on inmediattely available components was the main objective of the thesis, starting with the final V3 of the system.

3. Components chart

The bought components from digikey are selected from the system study and showed on this section, with the link and digikey part number when it was bought. SAT and GS stands for the Satellite and the Ground Station PCBs which shares most of the components, especially on the main link.

Name	**#**	**SAT Part**	**Digikey Link**	**Digikey part num**	**#**	**GS Part**
Osc 30mhz	1	Y3	http://www.digikey.com/product-detail/en/ECS-300-8-36CKM-TR/XC1562CT-ND/1693731	XC1562CT-ND	1	Y1
Osc 16mhz	1	Y2	http://www.digikey.com/product-detail/en/ABM7-16.000MHZ-D2Y-T/535-9840-1-ND/2001463	535-9840-1-ND		
Atmega328p	1	Q3	http://www.digikey.com/product-detail/en/ATMEGA328P-15AZ/ATMEGA328P-15AZCT-ND/2477177	ATMEGA328P-15AZCT-ND		
Si4460	1	Q1	http://www.digikey.com/product-detail/en/SI4460-B1B-FM/336-2470-5-ND/3681118	336-2470-5-ND	1	Q1
Osc 13.56mhz	1	Y1	http://www.digikey.com/product-detail/en/7A-13.560MAAE-T/887-1744-1-ND/3518794	887-1744-1-ND		
ASK TX	1	Q4	http://www.digikey.com/product-detail/en/TH72012KDC-BAA-000-TU/TH72012KDC-BAA-000-TU-ND/3641028	TH72012KDC-BAA-000-TU-ND		
PA ASK	1	Q5	http://www.digikey.com/product-detail/en/MAAL-010704-TR3000/1465-1261-1-ND/4429958	1465-1261-1-ND		
22pF arduin	2	C1, C2	http://www.digikey.com/product-detail/en/C0603C220F1GACTU/399-11145-1-ND/4357839	C0603C220F1GACTU		
Others						
SMA con pcb	3	J1, J2, J3	http://www.digikey.ca/scripts/DkSearch/dksus.dll?Detail&itemSeq=190423098&uq=635917055040909211	CONSMA002-ND	2	J1, J2

Arduino uno	1	ALT	http://www.digikey.com/product-detail/en/A000066/1050-1024-ND/2784006	1050-1024-ND		
Ard usb to serial conv	1	ALT	http://www.digikey.com/product-detail/en/A000059/1050-1021-ND/2784002	1050-1021-ND		
10 pin .100”	1	J4	http://www.digikey.ca/scripts/DkSearch/dksus.dll?Detail&itemSeq=190357167&uq=635914990457589616	S7043-ND	1	J4
Pc104 cubes altre	2	H1, H2	http://www.digikey.com/product-detail/en/7-534998-6/A123261-ND/2278581	A123261-ND		
Terminal con 5V wires	1	J5	http://www.digikey.com/product-detail/en/691102710002/732-2028-ND/2060524	732-2028-ND	1	J3
Shield Fram Main	1	S1F	http://www.digikey.com/product-detail/en/BMI-S-210-F/903-1057-1-ND/2182411	903-1057-1-ND		
Shield Covr Main	1	S1C	http://www.digikey.com/product-detail/en/BMI-S-210-C/903-1020-ND/2175921	903-1020-ND		
Shield Fram Beacon	1	S2F	http://www.digikey.com/product-detail/en/BMI-S-209-F/903-1212-1-ND/3505696	903-1212-1-ND	1	-
Shield Covr Beacon	1	S2C	http://www.digikey.com/product-detail/en/BMI-S-209-C/903-1185-ND/3505683	903-1185-ND	1	-
Terminator 50ohm	2	ALT	http://www.digikey.com/product-detail/en/132360/ACX1251-ND/1011928	ACX1251-ND	1	-
SMA con RA	3-6	ALT	http://www.digikey.com/product-detail/en/CONSMA012/CONSMA012-ND/1577224	CONSMA012-ND	2-4	-
RG174/U coax 15m	1	ALT	http://www.digikey.com/product-detail/en/C1156.21.01/C1156-50-ND/5039672	C1156-50-ND	-	-
RESISTORS						
4.7ohm	1	R1	http://www.digikey.com/product-detail/en/ESR03EZPJ4R7/RHM4.7DCT-ND/4053796	RHM4.7DCT-ND	1	R1
10kOhm	1	R2	http://www.digikey.com/product-detail/en/ESR03EZPJ103/RHM10KDCT-ND/1762925	RHM10KDCT-ND		
56kOhm	1	R3	http://www.digikey.com/product-detail/en/MCR10ERTF5602/RHM56KCHCT-ND/4084908	RHM56KCHCT-ND		
750Ohm	1	R4	http://www.digikey.com/product-detail/en/MCR10ERTF7500/RHM750CHCT-ND/4084981	RHM750CHCT-ND		
CAPACITORS						

8pF	3	C5, C6, C7	http://www.digikey.com/product-detail/en/GRM1555C1H8R0BA01D/490-8230-1-ND/4380524	490-8230-1-ND	3	C5, C6, C7
6.5pF	2	C24, C4	http://www.digikey.com/product-detail/en/GRM0225C1E6R5CDAEL/490-10229-1-ND/5026096	490-10229-1-ND	2	C4, C14
4.7pF	1	C8	http://www.digikey.com/product-detail/en/GRM1555C1H4R7BA01D/490-6244-1-ND/3845441	490-6244-1-ND	1	C8
2.2pF	1	C9	http://www.digikey.com/product-detail/en/GRM1555C1H2R2BA01D/490-6227-1-ND/3845424	490-6227-1-ND	1	C9
27pF	1	C32	http://www.digikey.com/product-detail/en/GRM1885C1H270GA01D/490-11455-1-ND/5333295	490-11455-1-ND		
5.6pF	1	C33	http://www.digikey.com/product-detail/en/GRM1885C1H5R6CA01D/490-12723-1-ND/5797692	490-12723-1-ND		
82pF	1	C23	http://www.digikey.com/product-detail/en/GRM1885C1H820GA01D/490-11480-1-ND/5333320	490-11480-1-ND		
10pF	1	C34	http://www.digikey.com/product-detail/en/GRM1885C1H100FA01J/490-9682-1-ND/4934803	490-9682-1-ND		
270pF	1	C10	http://www.digikey.com/product-detail/en/GRM1555C1H271JA01J/490-6225-1-ND/3845422	490-6225-1-ND	1	C10
220pF	1	C11	http://www.digikey.com/product-detail/en/GRM1555C1H221GA01J/490-11383-1-ND/5333223	490-11383-1-ND	1	C11
3.3pF	1	C15	http://www.digikey.com/product-detail/en/GRM1555C1H3R3BA01D/490-6238-1-ND/3845435	490-6238-1-ND	1	C3
100pF	1	C16	http://www.digikey.com/product-detail/en/GRM1555C1H101FA01J/490-7753-1-ND/4358004	490-7753-1-ND	1	C13
100nF	2	C19, C17	http://www.digikey.com/product-detail/en/GRM155R62A104KE14D/490-10458-1-ND/5026370	490-10458-1-ND	2	C12, C2
1nF	2	C12, C13	http://www.digikey.com/product-detail/en/GRM1555C1H102JA01D/490-3244-1-ND/702785	490-3244-1-ND		
10nF	1	C14	http://www.digikey.com/product-detail/en/GRM155R71E103JA01J/490-6340-1-ND/3845537	490-6340-1-ND		
220nF	1	C21	http://www.digikey.com/product-detail/en/GRM155R61A224KE19J/490-6303-1-ND/3845500	490-6303-1-ND		
330pF	1	C22	http://www.digikey.com/product-detail/en/GRM188R71H331KA01D/490-1486-1-ND/587820	490-1486-1-ND		
2.2uF	1	C20	http://www.digikey.com/product-detail/en/GRM155C71A225KE11D/490-12697-1-ND/5797666	490-12697-1-ND	1	C1

100uF TANT	1	C18	http://www.digikey.com/product-detail/en/T491C107M006AT/399-8339-1-ND/3472062	399-8339-1-ND		
INDUCTORS RX						
56nH	1	L5	http://www.digikey.com/product-detail/en/LQW15AN56NG00D/490-6830-1-ND/3846027	490-6830-1-ND	1	L6
62nH	1	L4	http://www.digikey.com/product-detail/en/LQW15AN62NG00D/490-6836-1-ND/3846033	490-6836-1-ND	1	L5
INDUCTORS TX						
18nH high P	1	L6	http://www.digikey.ca/product-detail/en/LQW15AN18NG00D/490-6776-1-ND/3845973	490-6776-1-ND	1	L4
19nH	1	L3	http://www.digikey.com/product-detail/en/LQW15AN19NG00D/490-6778-1-ND/3845975	490-6778-1-ND	1	L3
33nH	2	L7, L8	http://www.digikey.com/product-detail/en/LQW18AN33NJ00D/490-1175-1-ND/584620	490-1175-1-ND		
39nH	1	L2	http://www.digikey.com/product-detail/en/LQG15HS39NJ02D/490-2630-1-ND/662910	490-2630-1-ND	1	L2
100nH	1	L9	http://www.digikey.com/product-detail/en/LQW18ANR10G00D/490-6918-1-ND/3846115	490-6918-1-ND		
220nH	1	L1	http://www.digikey.com/product-detail/en/LQG15HSR22J02D/490-2639-1-ND/662919	490-2639-1-ND	1	L1

The components bought for the Baluns and antennas where based on the computations from section 6.1 of the main report.

Name	#		Link	Ref
DIPOLES				
22nH highP	4	TX,RX	http://www.digikey.ca/product-detail/en/LQW18AN22NG00D/490-6874-1-ND/3846071	490-6874-1-ND
6pF highP	4	TX,RX	http://www.digikey.ca/product-detail/en/GRM1885C1H6R0DA01D/490-10722-1-ND/5251378	490-10722-1-ND
SMA con pcb	3	TX,RX,CW	http://www.digikey.ca/scripts/DkSearch/dksus.dll?Detail&itemSeq=190423098&uq=635917055040909211	CONSMA002-ND
MONOPOLE				
30nH CW	1	CW	http://www.digikey.ca/product-detail/en/LQW18AN30NJ00D/490-6883-1-ND/3846080	490-6883-1-ND

16pF CW	1	CW	http://www.digikey.ca/product-detail/en/GRM1885C1H160JA01D/490-1408-1-ND/587641	490-1408-1-ND

Also some of the components were already bought when designed the SKY65116 evaluation board, and used then in the main system:

Name	**#**	**SAT**
Sky65116	1	Q2
3.6v regultr	1	Q6
0.01uF	3	C27, C28, C29
10uF	3	C3, C25, C26
10uF TANT	1	C30
100uF	1	C31

4. COSTS AND PCB MANUFACTURING

The final cost of the system is resumed in this section. Basically it consists on the components cost and the PCB manufacturing.

Item	**Manufacturer**	**Cost**
Components 1st buy	Digikey	43.36$
Components 2nd buy	Digikey	298.42$
PCB	Canadian Circuits	325$
Assembly	Optimont	Free
TOTAL		**666.79$**

The PCB has a student discount applied by Canadian Circuits in which Tooling and Testing are free, having a really affordable final price given the other quotes obtained by other companies.

The PCB making consisted on a jointed board that included other systems of Polyorbite in which Alimentation and ADCS coexisted with the 3 PCBs of telecommunications.

The procedure to join all the Eagle designs in one was made also by the author of this thesis and is showed on Fig. 4.1.

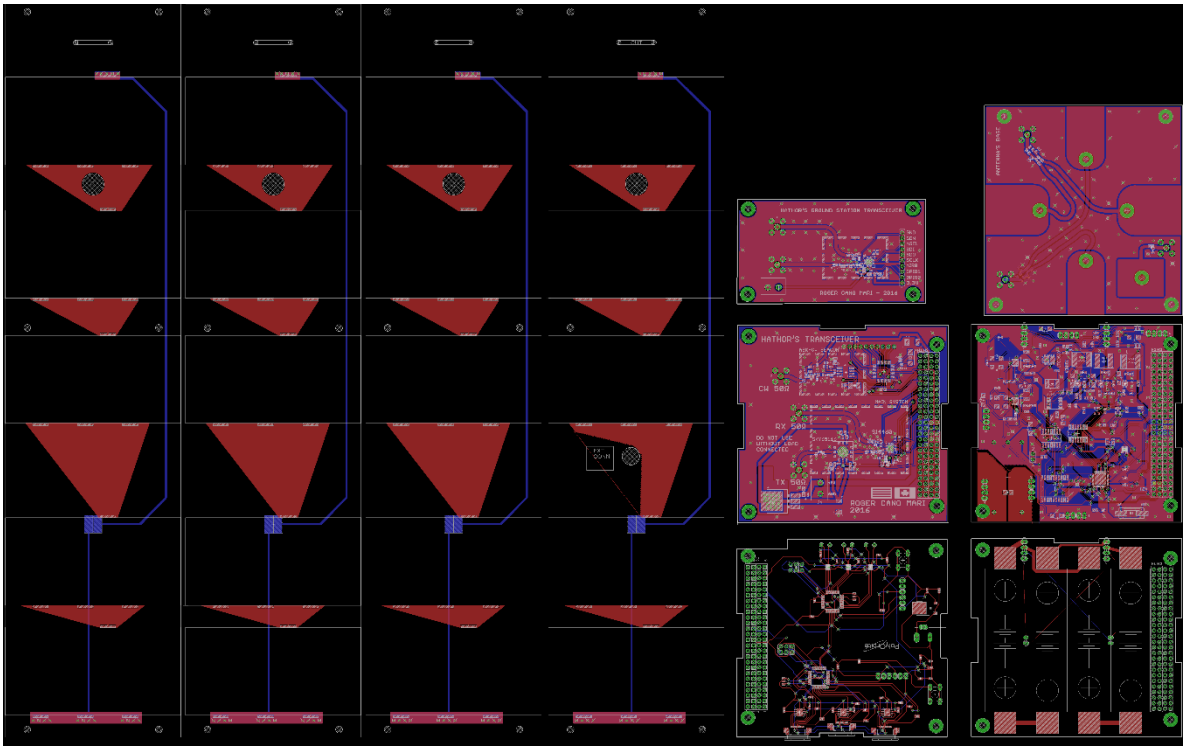


Fig. 4.1 Big PCB design sent to Canadian Circuits.

It can be seen at left of the picture the 4 large PCBs that goes at each side of the satellite which contains soldered the solar panels. A part of the 3 PCBs for telecommunications (Radio satellite, Ground satellite and antennas) two more boards were included from Alimentation team (Main alimentation and Batteries) and another board from ACDS.

In Fig. 4.2 it is shown one of the two copies that Canadian Circuits manufactured.

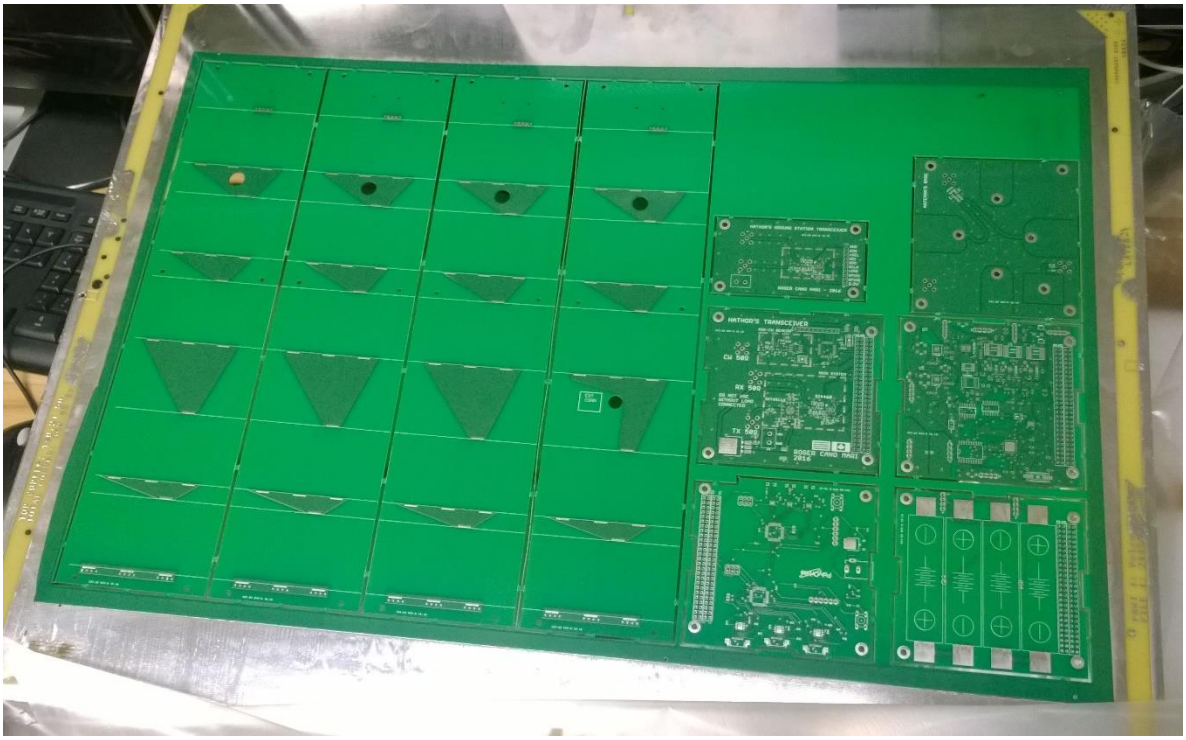


Fig. 4.2 Big PCB board once arrived in middle April 2016.

The assembly was made by Optimont, a Canadian company situated on Montreal, which its founder was a teacher also on Polytecnique and provided us free services for the simpler PCBs.

The SKY65116 amplifier needed a stencil (metal machined sheet used to deposit a special solder flux to the pins of the PCB in order to sold it properly) and that increased the cost of assembly by 400$ each PCB (Radio SAT PCB and also others from ACDS and Alimentation).

Given that fact and that the assembly time increases from 2 to 10 days if stencils are required, it was just produced the 3 telecommunications PCB but the “Radio SAT” without assemble the Main Radio components.

Received the PCBs by April 26th and leaving the country the author by the 1st of May, no tests could be done to the main system.

The next email extraction is the Optimont quote for assembly:

The Poly Orbite Antennas PCB

- has no silk screen layer – an assembly drawing is required to do the job (it could eventually be generated from the P&P file provided)
- can be manually assembled in two working days
- at no cost to Poly Orbite

- The Poly Orbite PCB Batteries
  - Has what it appears to be a design flaw, with a trace to pad clearance of only 0.0015''
  - can be manually assembled in two working days
  - at no cost to Poly Orbite

- The Poly Orbite PCB SystAlim
  - Has a very limited silk screen layer – an assembly drawing is required to do the job (it could eventually be generated from the P&P file provided)
  - Can be manually assembled in 5 working days
  - For a price of $350.

- The Poly Orbite Radio Gnd
  - Is professionally designed
  - Can be manually assembled in two working days
  - At no cost to Poly Orbite

- The Poly Orbite Radio Sat
    - Is professionally designed
    - Requires a paste stencil for the Skyworks PA (the Silicon Labs Xceiver would benefit from it too)
    - Can be manually assembled on paste and completed at the latter of 5 working days after order (to get the stencil made), and 2 days after receipt of the parts kit
    - For a price of $400.

We assume a unit quantity for each PCB.

5. Programming

5.1. Morse messaging code

The next Arduino code was used for morse testing purposes, in which the Arduino outputs the introduced text via serial data into a morse signal:

```
// Test code for Hathor's Cubesat Morse beacon. It sends a message in
// code morse.
// Final system should obtain main relevant data via I2C from the
// CubeSat's I2C
// bus instead of the test message now included.
// This code contains Serial data for testing purposes. No serial needed
// for CubeSat.

//Define the LED Pin
#define PIN_OUT       3
#define ENABLE        4

//Define unit length in ms
#define UNIT_LENGTH    200

//Build a struct with the morse code mapping
static const struct {const char letter, *code;} MorseMap[] =
{
      { 'A', ".-" },
      { 'B', "-..." },
      { 'C', "-.-." },
      { 'D', "-.." },
      { 'E', "." },
      { 'F', "..-." },
      { 'G', "--." },
      { 'H', "...." },
      { 'I', ".." },
      { 'J', ".---" },
      { 'K', ".-.-" },
      { 'L', ".-.." },
      { 'M', "--" },
      { 'N', "-." },
      { 'O', "---" },
      { 'P', ".--." },
      { 'Q', "--.-" },
      { 'R', ".-." },
      { 'S', "..." },
      { 'T', "-" },
      { 'U', "..-" },
      { 'V', "...-" },
      { 'W', ".--" },
      { 'X', "-..-" },
      { 'Y', "-.--" },
      { 'Z', "--.." },
      { ' ', "     " }, //Gap between word, seven units
```

```
      { '1', ".----" },
      { '2', "..---" },
      { '3', "...--" },
      { '4', "....-" },
      { '5', "....." },
      { '6', "-...." },
      { '7', "--..." },
      { '8', "---.." },
      { '9', "----." },
      { '0', "-----" },

      { '.', "·–·–·–" },
      { ',', "--..--" },
      { '?', "..--.." },
      { '!', "-.-.--" },
      { ':', "---..." },
      { ';', "-.-.-." },
      { '(', "-.--." },
      { ')', "-.--.-" },
      { '"', ".-..-." },
      { '@', ".--.-." },
      { '&', ".-..." },
};

void setup()
{
  pinMode( PIN_OUT, OUTPUT );
  pinMode( ENABLE, OUTPUT );
  digitalWrite( PIN_OUT, LOW );
  digitalWrite( ENABLE, LOW );
  Serial.begin(9600);
  Serial.print("init");
// Using the serial command I program the Arduino to communicate at a
// baud rate of 9600 bits per second.
}

void loop()
{

  String morseWord = encode( "SOS " );
  delay(5000);
  digitalWrite( ENABLE, HIGH );
  Serial.write("Enable ON");
Serial.print(morseWord.length());
  for(int i=0; i<=morseWord.length(); i++)
  {
    switch( morseWord[i] )
    {
      case '.': //dit
        digitalWrite( PIN_OUT, HIGH );
        delay( UNIT_LENGTH );
        digitalWrite( PIN_OUT, LOW );
        delay( UNIT_LENGTH );
         Serial.print(".");
```

```
        break;

      case '-': //dah
        digitalWrite( PIN_OUT, HIGH );
        delay( UNIT_LENGTH*3 );
        digitalWrite( PIN_OUT, LOW );
        delay( UNIT_LENGTH );
         Serial.print("-");
        break;

      case ' ': //gap
        delay( UNIT_LENGTH );
        Serial.print(" ");
    }
  }
    digitalWrite( ENABLE, LOW );
      Serial.write("Enable OFF");
    Serial.print("");

}
String encode(const char *string)
{
  size_t i, j;
  String morseWord = "";

  for( i = 0; string[i]; ++i )
  {
    for( j = 0; j < sizeof MorseMap / sizeof *MorseMap; ++j )
    {
      if( toupper(string[i]) == MorseMap[j].letter )
      {
        morseWord += MorseMap[j].code;
        break;
      }
    }
    morseWord += " "; //Add tailing space to seperate the chars


  }
    return morseWord;

}
```

ANNEX B

TESTS

6. DIPOLE ANTENNAS – 1st ROUND

The next captures shows the S11 measurements for the different dipole lengths during the first rounf (without machining).

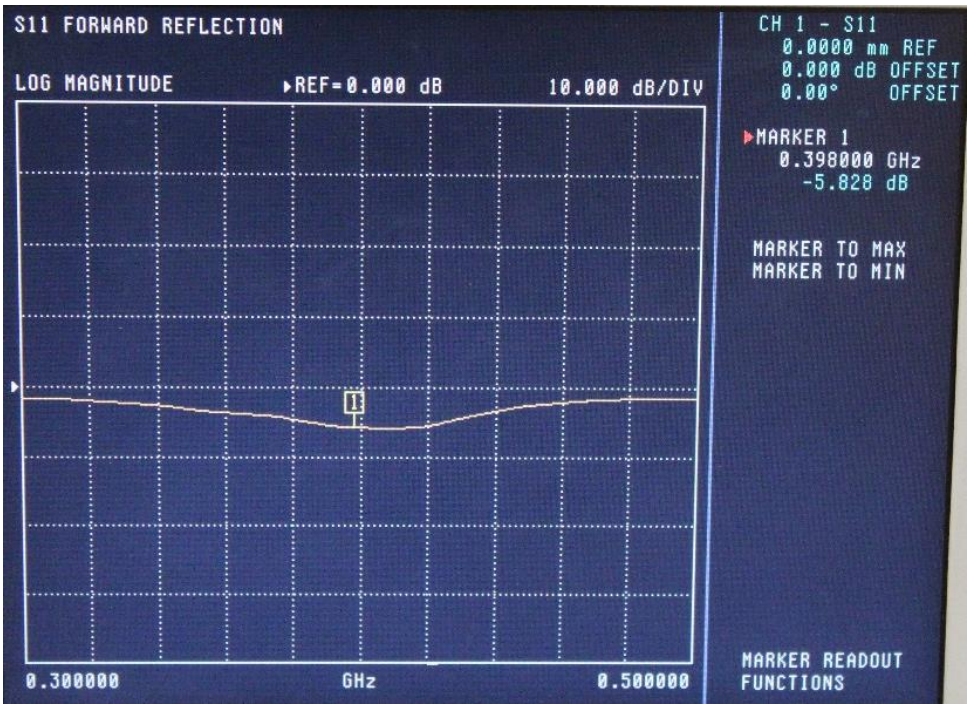


Fig. 6.1 L = 41.23 cm.

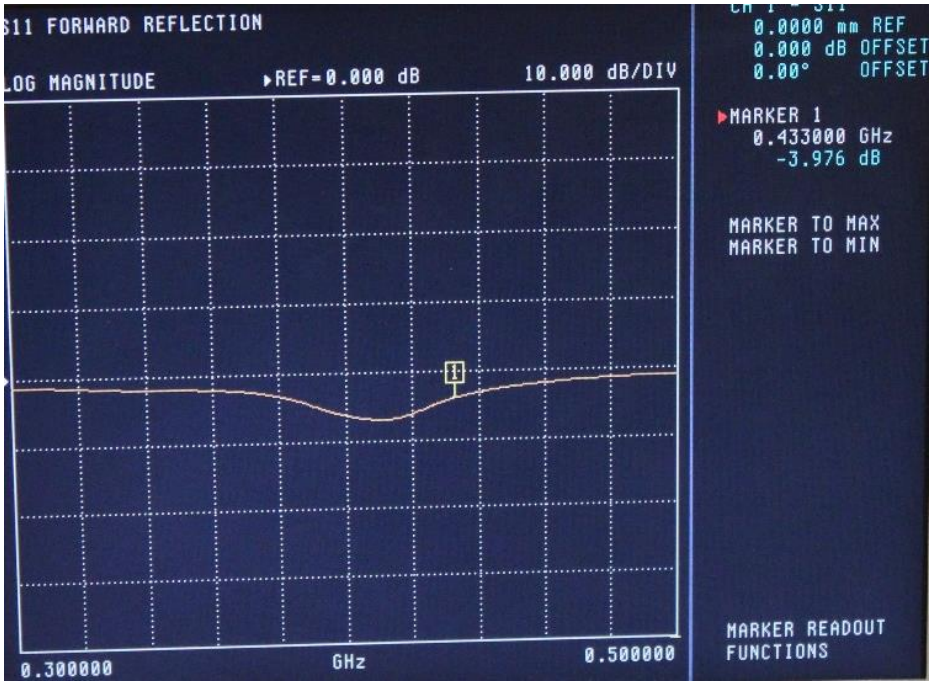


Fig. 6.2 L = 40 cm.

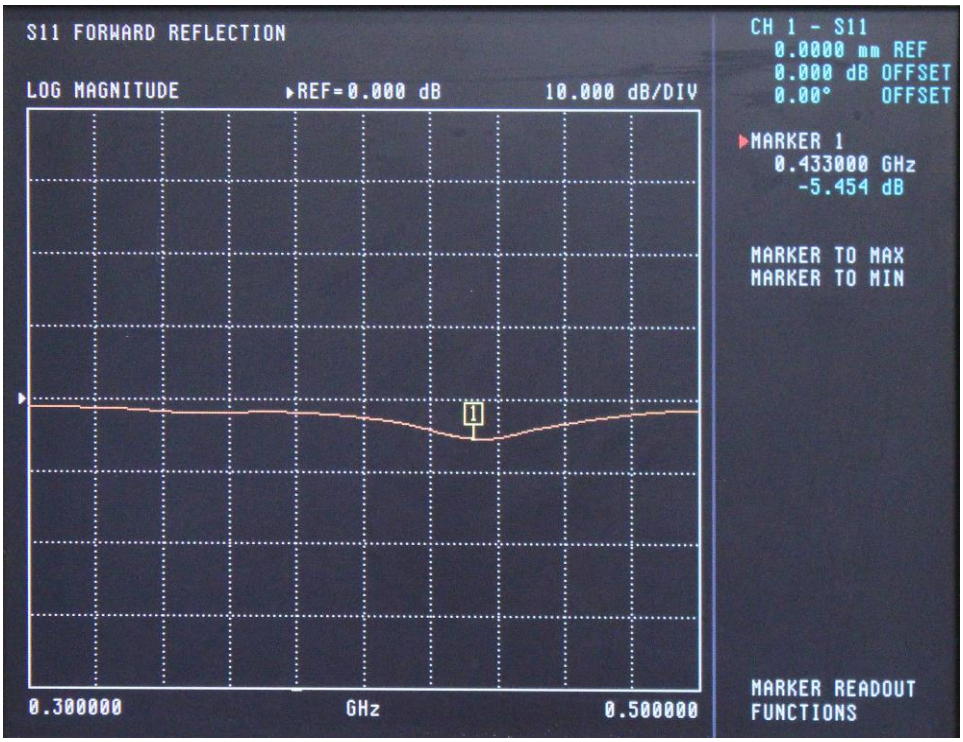


Fig. 6.3 L = 37 cm.

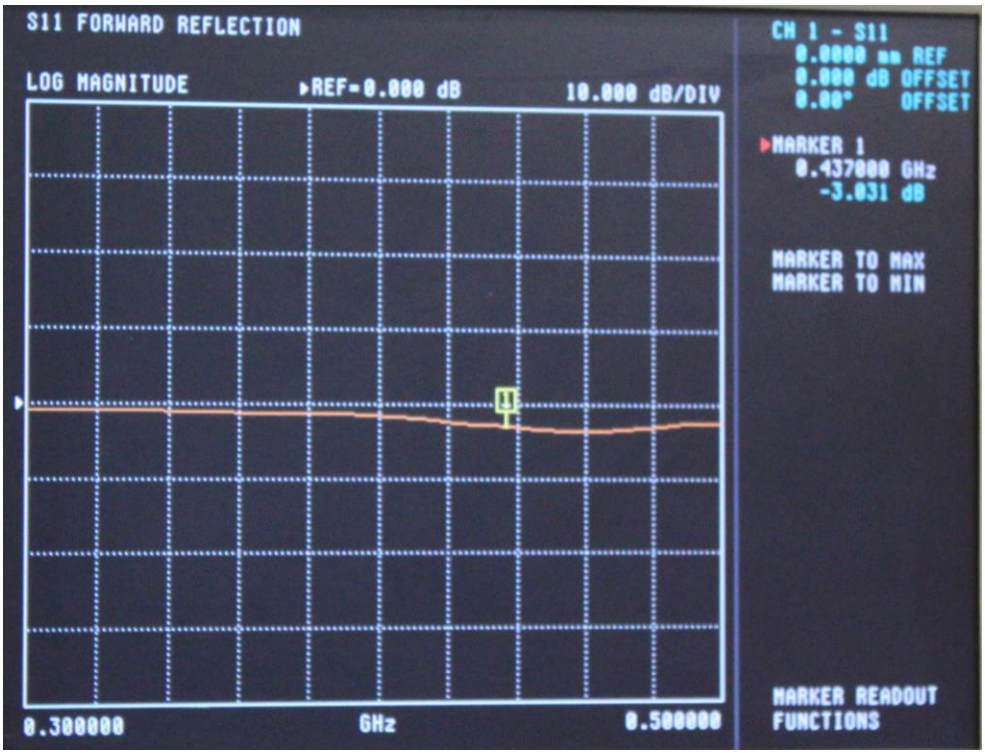


Fig. 6.4 L = 35 cm.

7. DIPOLE ANTENNAS – 2nd ROUND

After machining results were much better:

Fig. 7.1 L = 35 cm.

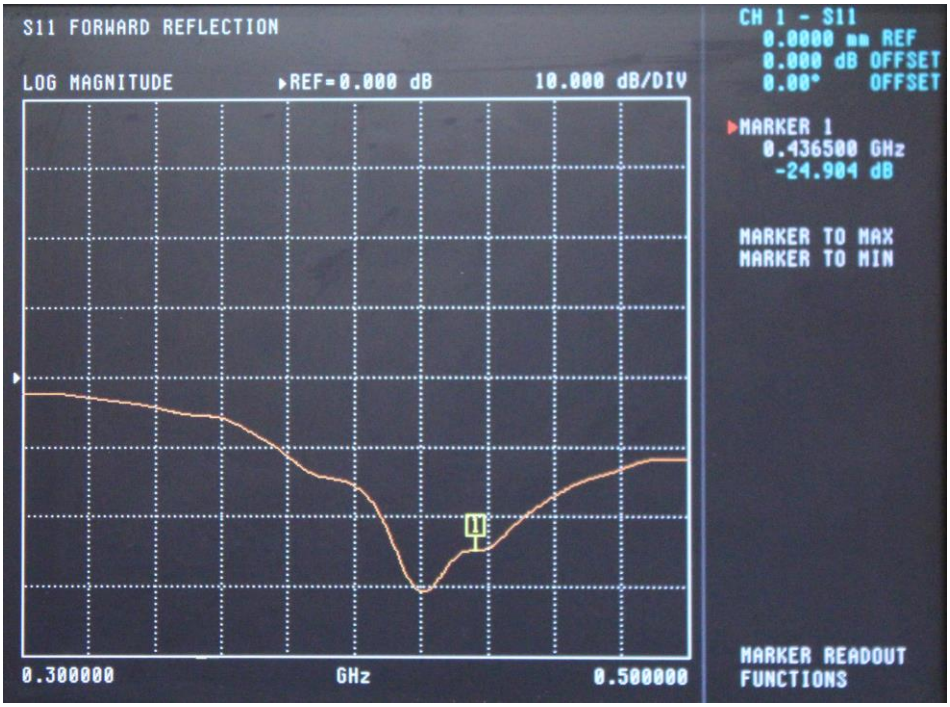


Fig. 7.2 L = 37 cm.

Fig. 7.3 L = 38 cm.

8. MONOPOLE ANTENNA

Fig. 8.1 L = 25 cm.

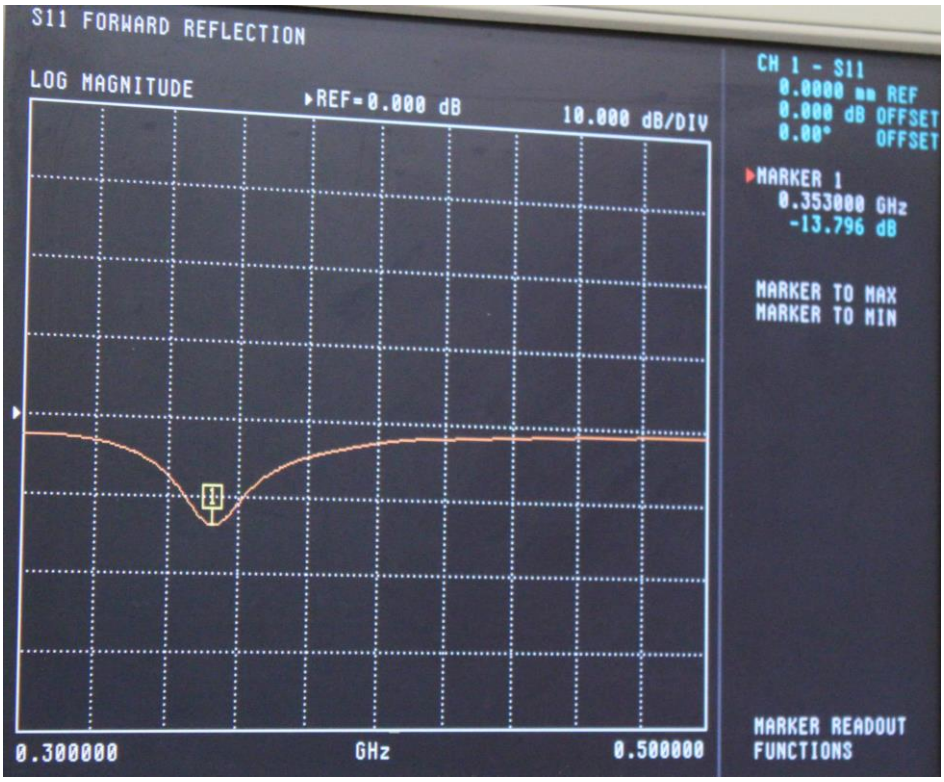


Fig. 8.2 L = 23 cm.

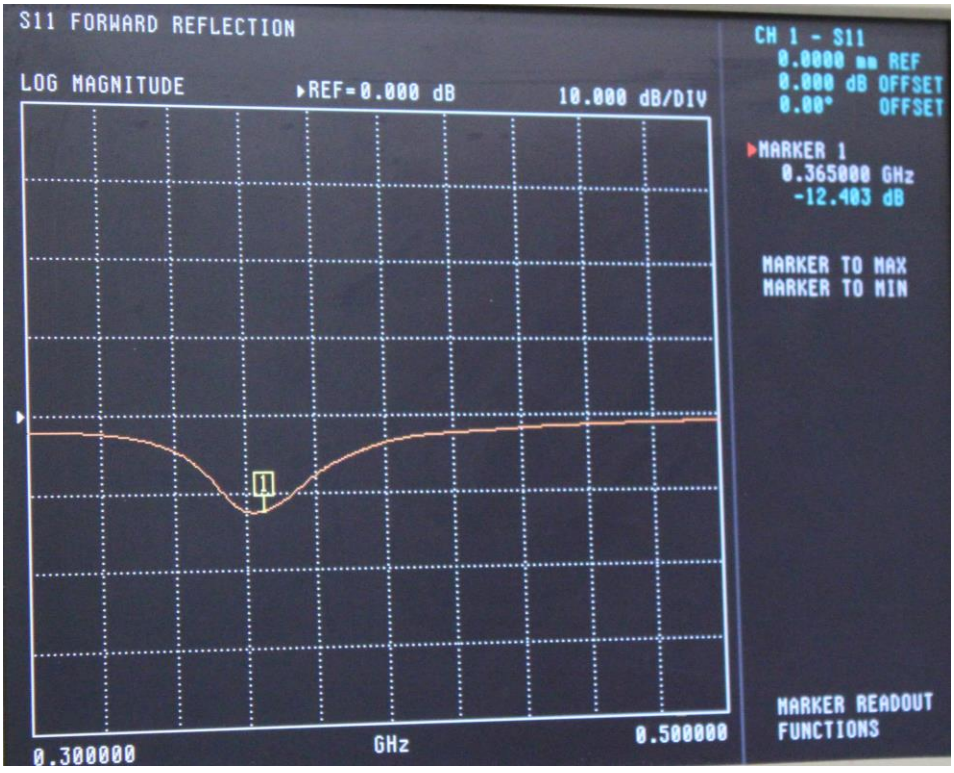


Fig. 8.3 L = 22 cm.

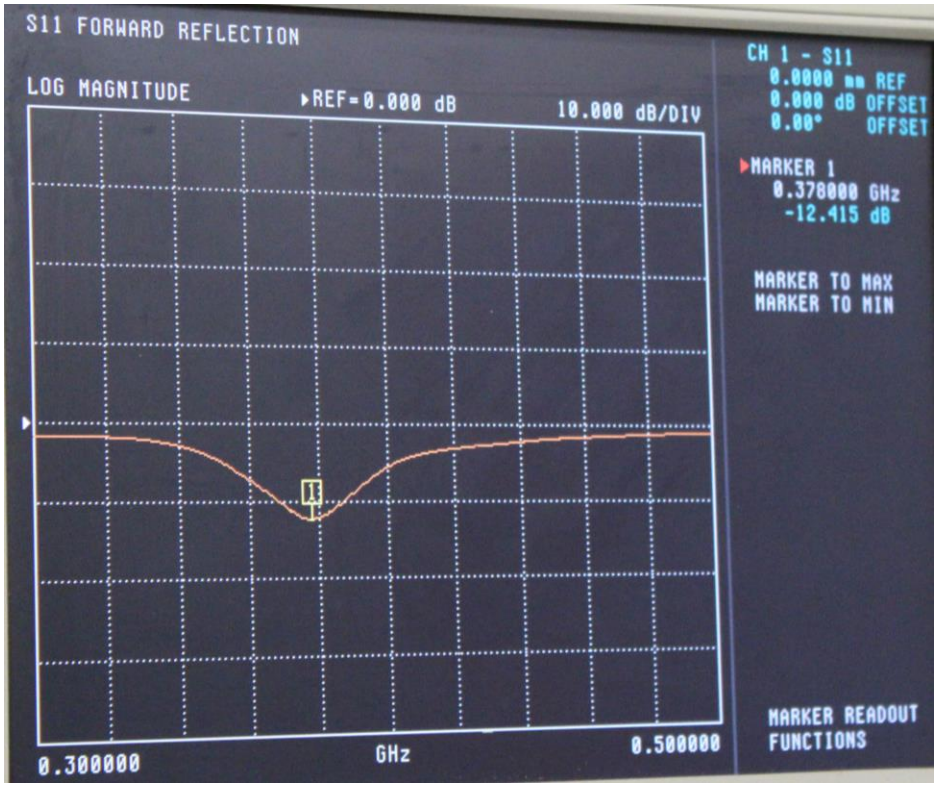


Fig. 8.4 L = 21 cm.

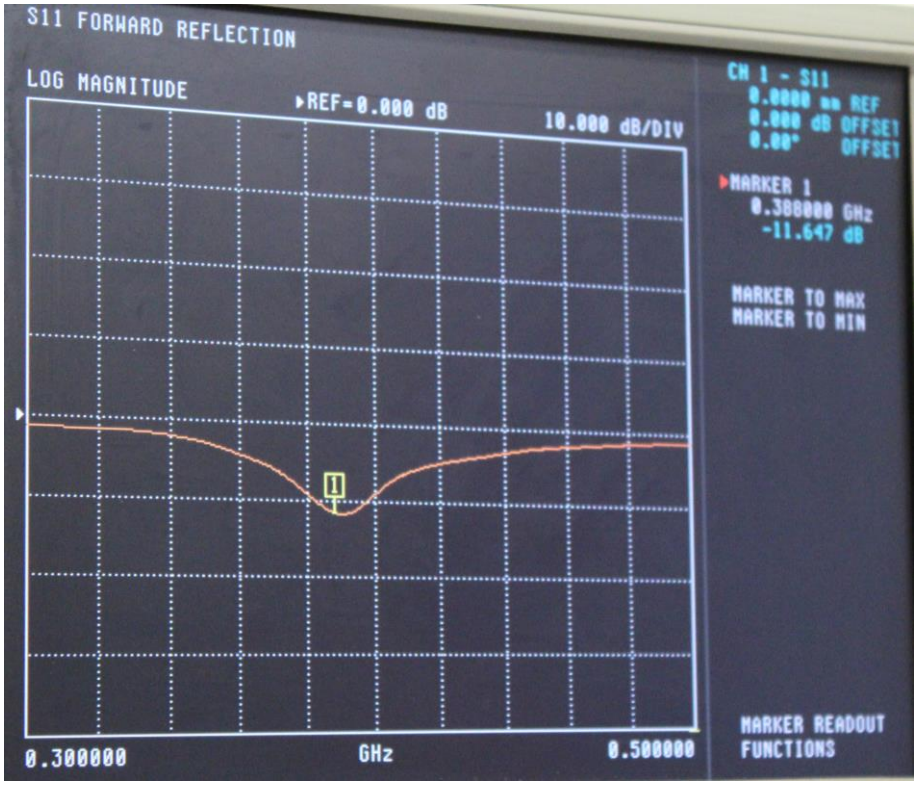


Fig. 8.5 L = 20 cm.

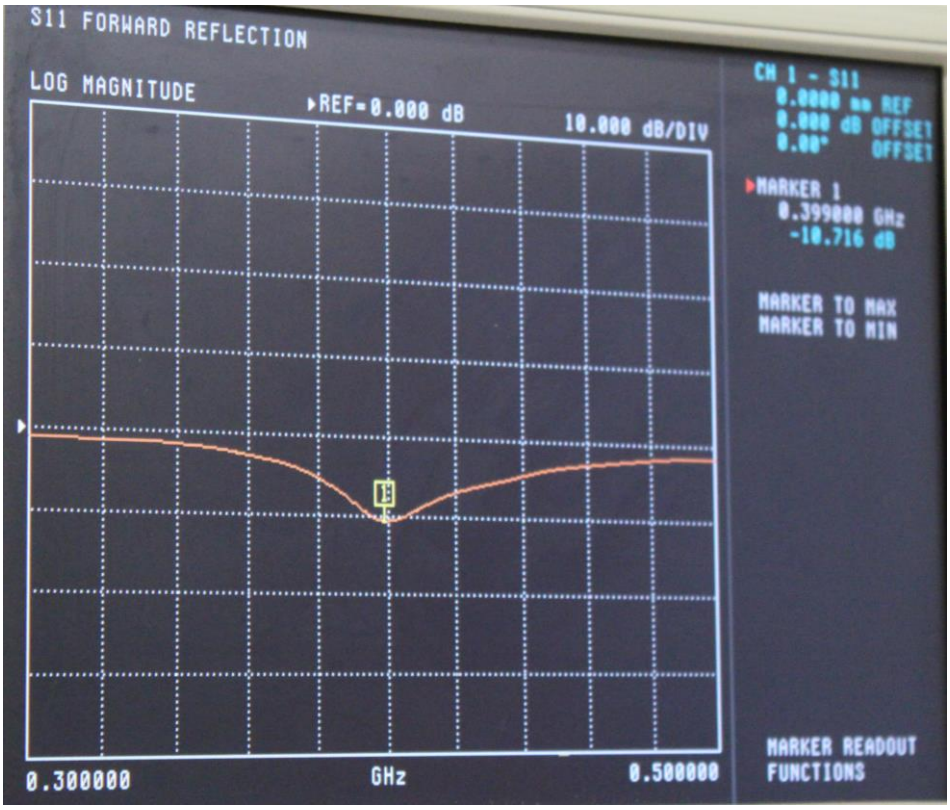


Fig. 8.6 L = 19 cm.

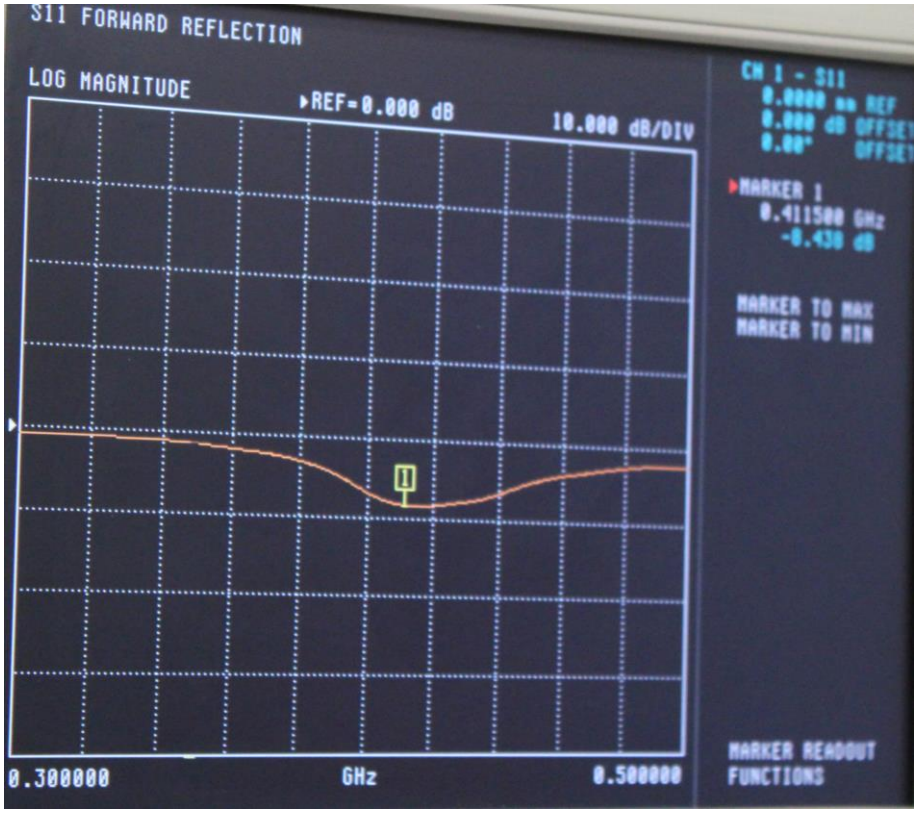


Fig. 8.7 L = 18 cm.

Fig. 8.8 L = 17.5 cm.

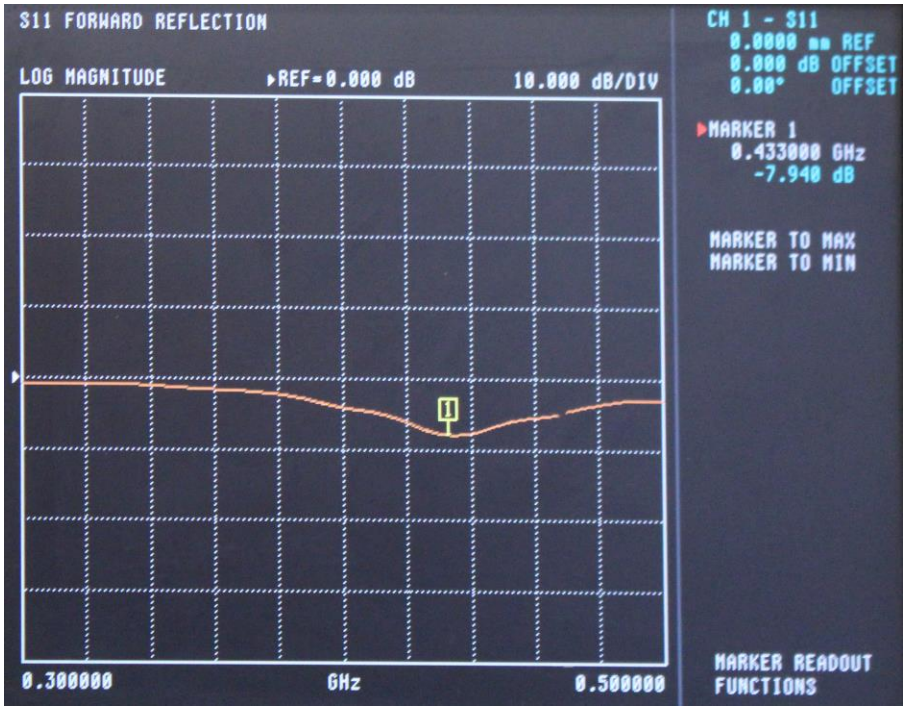


Fig. 8.9 L = 17.2 cm.

ANNEX C

IMPORTANT DATASHEETS

Escola d'Enginyeria de Telecomunicació i Aeroespacial de Castelldefels
UNIVERSITAT POLITÈCNICA DE CATALUNYA

ANNEX C

TÍTOL DEL TFG: Telecommunications system of a CubeSat satellite

TITULACIÓ: Grau en Enginyeria d'Aeronavegació

AUTOR: Roger Cano Marí

DIRECTOR: Giovanni Beltrame

DATA: 29 d'Abril del 2016

ANNEX C

IMPORTANT DATASHEETS

CCI CANADIAN CIRCUITS INC.
#10 - 13140 88th Avenue
Surrey, BC, Canada V3W 3K3
www.canadiancircuits.com
Contacts: Pam Arya

Tel: (604) 599-8600
Fax: (604) 599-8181
Toll Free: 1-888-590-6464
Email:sales@canadiancircuits.com

Date: 23-Feb-16

Quotation

Quotation No: Q16025269

Board P/N: Polyorbite

To:

Polytechnique de Montreal

Montreal, QC, Canada

Contact: Roger Cano
Tel:
Fax:

PCB SPECIFICATION

Board Size	.	**" X** .	**"**	**Pane**	19.48 **"**	**X** 15.77 **"** 1	**Up**
Material	FR4						
# Of Layers	2						
Thickness:	0.062						
Finish Copper	1 oz	**Inner Copper**					
Board Finish	HASL						

SOLDERMASK

Component	☑	LPI	GREEN	MATTE
Solder	☑	LPI	GREEN	MATTE

SILKSCREEN

Component	☑	**Color**	White
Solder	☐	**Color**	White

OTHERS

Routing Type	TAB	**E-Test**	☑

Quantity	Turn Around	Price	Tooling	E Test	Finish	Lot	Note
1	5 days	$0.00	$0.00	$0.00		$325.00	1 panel

Comments: Student discount applied

PLEASE DOUBLE CHECK ALL SPECIFICATIONS ON THIS RFQ. YOUR APPROVAL SIGNATURE IS REQUIRED BEFORE PRODUCTION. PLEASE FAX TO 604-599-8181, OR EMAIL TO sales@canadiancircuits.com, WITH YOUR PO#.

APPROVED BY: _____

All applicable taxes are extra.

All quotes are valid 30 days subject to credit terms. UL ISO certified printed circuits board manufacturer serving the Pacific Northwest since 1993. CCI Canadian Circuits Inc. liability shall not exceed the cost of above supplied circuit boards.

http://www.cubesatkit.com/

CubeSat Kit™ Motherboard (MB)

Hardware Revision: D

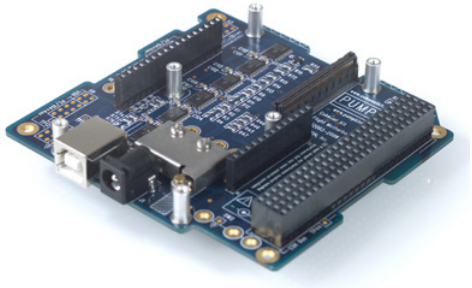
Single Board Computer Motherboard for Harsh Environments

Applications

- CubeSat nanosatellite C&DH, TT&C, mass storage and battery / power switching
- General-purpose low-power computing in a PC/104-size form factor
- Remote sensing for harsh environments

Features

- Open architecture – accepts Pluggable Processor Modules (PPMs)
- Compatible with a wide range of supply and I/O voltages
- Extremely low (<10µA) quiescent current
- Integrated peripherals:
  - I2C real-time clock
  - 3V Lithium backup battery
  - USB 2.0 device interface for pre-launch communications, battery charging and power
  - MMC/SD card socket for mass storage (32MB to 2GB and beyond)
- Support for a wide range of transceivers
- Stackable 104-pin CubeSat Kit Bus connectors includes processor's complete I/O space, user-assignable signals and more
- Extensible to multiprocessor architectures, with processor reset / NMI pin on bus
- Direct wiring for heavy-duty Remove-Before-Flight and Deployment switches
- Comprehensive overcurrent, overvoltage & undervoltage (reset) protection
- Independent latchup (device overcurrent) protection on critical subsystems
- Bus override for critical power and data/control paths
- Power consumption can be monitored externally
- Wiring-free module interconnect scheme
- PC/104-size footprint, with +5V and GND on PC/104 J1/J2 connectors
- 6-layer gold-plated blue-soldermask PCB with dual ground planes for enhanced signal integrity
- Compatible with Pumpkin's Salvo™ RTOS and HCC-Embedded's EFFS-THIN SD Card file FAT file system for ease of programming
- Backwards-compatible with CubeSat Kit Rev. A through Rev. C FM430



ORDERING INFORMATION

Pumpkin P/N 710-00484

Option Code	PPM Connector Height	CubeSat Kit Bus Connector[1]
/00 (standard)	+6mm	non-stackthrough
/10	+6mm	stackthrough

Contact factory for availability of optional configurations. Option code /00 shown.

CAUTION

Electrostatic Sensitive Devices

Handle with Care

[1] Stackthrough connectors are used in CubeSat Kit configurations where the MB is not in Slot 0.

CHANGELOG

Rev.	Date	Author	Comments
I	20090808	AEK	Updated to match Development Board datasheet.
J	20090911	AEK	Corrected **H1** & **H2** pin numbers for **IO.[47..40, 7..0]**, **SCL_SYS** and **SDA_SYS**.

OPERATIONAL DESCRIPTION

The CubeSat Kit Motherboard (MB) is the fourth generation of Pumpkin's line of single-board computers (SBCs) designed for use in the CubeSat Kit and elsewhere.

Unlike earlier Pumpkin SBCs like the FM430[2], the MB does not have a permanently soldered processor.[3] Instead, it has a socket to accommodate a Pluggable Processor Module (PPM). PPMs can be sourced from Pumpkin, third parties or can be created by the end-user of a CubeSat Kit. Thus, a wide range of potential processors (e.g. MSP430, 8051, AVR®, PICmicro®, ARM®, x86, FPGA, ASIC, etc.) can be used with the MB via a suitable PPM.

The MB has a flexible power scheme that permits the use of PPMs with different power and I/O requirements. All of the MB's on-board peripheral I/O (RTC, MHX interface, USB & SD Card) is level-shifted and zero-power-isolated to interface with PPMs at any I/O voltage from +1.65V to +5.5V.

The MB provides the PPM socket with all of the CubeSat Kit Bus Connector I/O and power signals, as well as some dedicated and special-purpose MB signals.[4]

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Operating temperature [5]	T_A	-40 to +85	ºC
Voltage on **+5V_USB** bus		-0.3 to +6	V
Voltage on **+5V_SYS** bus			
Voltage on **PWR_MHX** bus			
Voltage on **VCC_SYS** bus			
Voltage on **–FAULT** open-collector output			
Voltage on local **VCC** bus		-0.3 to +5.5	V
Voltage on any I/O pin		-0.3 to (**VCC** + 0.3)	V
Voltage on local **VCC_SD** bus		-0.3 to +3.6	V
Voltage on **VBACKUP** bus		-0.3 to +3.6	V
Voltage at external +5V power connector [6]		-20 to +20	V
DC current through any pin of PPM Connector	I_{PIN1_MAX}	1.2	A
DC current through any pin of CubeSat Kit Bus Connector	I_{PIN2_MAX}	3	A
DC current through external +5V power connector [7]	I_{EXT_MAX}	4	A
DC current through Remove-Before-Flight or Deployment Switches [8]	I_{SW_MAX}	10	A

[2] The FM430 utilized TI's MSP430 16-bit RISC microcontroller.

[3] The processor was previously referred to in Pumpkin literature as the Flight MCU.

[4] The only signals from the CubeSat Kit Bus Connector that are not presented at the PPM connector are the **S0**-**S5** signals (Remove-Before-Flight and Deployment Switches) and direct MHX interface signals (e.g., **-RTS_MHX**, etc.).

[5] Does not include any SD card fitted to the MB. Typical commercial SD card operating temperatures are 0ºC to + 55ºC. Typical industrial extended temperature range SD cards operate over -25ºC to + 85ºC.

[6] Voltages between 0V and +5.5V are passed through to +5V_SYS on the CubeSat Kit Bus.

[7] Limited by a fast-blo 4A fuse.

[8] Make only. Not rated for repetitive make and break cycles of dc current. AC rating for switches alone. Switches are typically wired by the user directly to the MB to simplify S[5..0] bus connections. User should analyze temperature rise on inner layers as a function of currents passed through RBF and Deployment Switches. For high-current applications, wiring directly to the switch (instead of indirectly through the CubeSat Kit Bus connector's S[5..0] pins and the MB PCB) may be preferred.

PHYSICAL CHARACTERISTICS

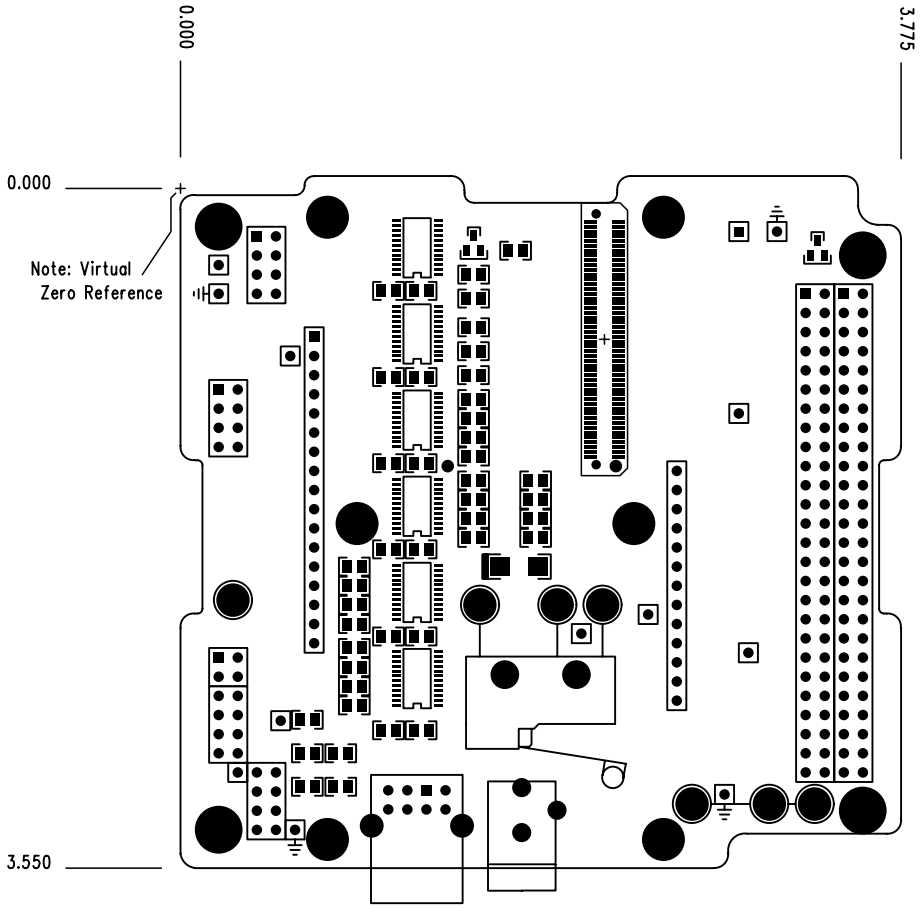
Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Mass [9]	With standoff and fastener hardware to accept a short PPM (e.g., PPM A1) mounted 9mm above the MB			77		g
	With PPM A1 mounted using abovementioned hardware [10]			88		
	With PPM A1 mounted using abovementioned hardware, 10mm CubeSat Kit Bus Connector extenders and 15.5mm standoffs for MHX transceiver			103		
Height of components above PCB	Without PPM, MHX transceiver or 10mm CubeSat Kit Bus Connector extenders fitted				11.4	mm
	With PPM fitted, and without MHX transceiver or 10mm CubeSat Kit Bus Connector extenders fitted				12.5	
	With MHX transceiver and 10mm CubeSat Kit Bus Connector extender fitted				24.5	
Height of components below PCB					3.5	mm
PCB width	Corner hole pattern matches PC/104			96		mm
PCB length				90		mm
PCB thickness				1.6		mm
Mating external power jack dimensions	Outer diameter				5.5	mm
	Internal diameter		2.1			
CubeSat Kit Bus Connector terminal pitch	Horizontal or vertical distance to nearest terminal			2.54		mm
Switch terminal hole diameter	For C, NO & NC switch terminals [11]			2.54		mm
Compatible coin cell battery dimensions	Diameter			12		mm
	Height		2.0	2.5	2.5	mm

[9] With Remove-Before-Flight Switch and cover fitted. No SD Card in socket.

[10] PPMs are not included with each MB, and must be purchased separately. Data supplied as an example only.

[11] Common, Normally Open and Normally Closed.

SIMPLIFIED MECHANICAL LAYOUT [12]



[12] Dimensions in inches.

ELECTRICAL CHARACTERISTICS

(T = 25ºC, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Operating Voltage	I/O voltage for all on-board peripherals except RTC and SD Card interface	V_{CC}	1.65		5.5	V
	RTC [13]		2.7		5.5	V
	SD Card interface [14]	V_{CC_SD}		3.3		V
Maximum external dc voltage	External dc voltage increased until protection circuitry forces disconnect	V_{EXT_TRIP}			5.5	V
Backup battery voltage	Feeds **VBACKUP** through **R20** (4.7kΩ).	V_{BT1}		3.0	3.5	V
Voltage drop from external dc power connector to **+5V_SYS** [15]	I_{IN} = 5mA	V_{EXT_DROP}			10	mV
	I_{IN} = 4A			400		
Operating current	Typical operation	I_{OP}		500		µA
	All control outputs inactive, PPM asleep	I_{SLEEP}		5	10	µA
RTC crystal frequency	No external capacitors	f_{CLK_RTC}	32.768 ± 0.001			kHz
USB bus current [16]	Powered over USB	I_{USB_MAX}			500	mA
Overcurrent trip point for SD Card socket	Set by **R61**	I_{TRIP_SD}		170		mA
Overcurrent trip point for MHX transceiver socket	Set by **R23**	I_{TRIP_MHX}		2400		mA
Time to switch between **+5V_SYS** and **+5V_USB** power sources	Automatic				1	µs
Data rate through any on-board isolator (**U1**-**U3**, **U16**-**U18**)	May be reduced (due to parasitic capacitance) by inline resistors (e.g., **R9**-**R12**, **R59**) where fitted with non-zero values		50			MHz

USB DEVICE CHARACTERISTICS

Parameter	Conditions / Notes	Value
Speed [17]	USB 2.0 compatible	Low Speed (1.5Mbps) Full Speed (12Mbps)
Vendor ID (VID)		0403
Product ID (PID)		F020
Reported options	Unique serial number	/03F0
Reported serial number	Format: PUdddddd	unique to each unit
Required driver	See CubeSat Kit website	provided by Pumpkin

[13] MB is fitted with M41T81S RTC. **Vcc** of +2.7V or higher is required for proper operation. Operation at lower values of **Vcc** requires the removal of the RTC and/or its substitution with one capable of running at voltages lower than +2.7V.

[14] SD Card standard requires operation at +3.3V. Lower-voltage SD cards can be accommodated by PPM supplying **VCC_SD** with an appropriate voltage, and by using SD cards specified for lower operating voltages.

[15] Measured at +5V system test point **TP9**. External +5V passes through a fuse and an active overvoltage protection circuit before reaching system +5V. MB PCB is implemented with 2oz copper to minimize resistance of power traces.

[16] The MB's USB interface is configured at the factory to report a maximum current of 500mA for a bus-powered device to any attached USB host.

[17] Actual throughput is dependent on coding in and configuration of processor, and is often much lower.

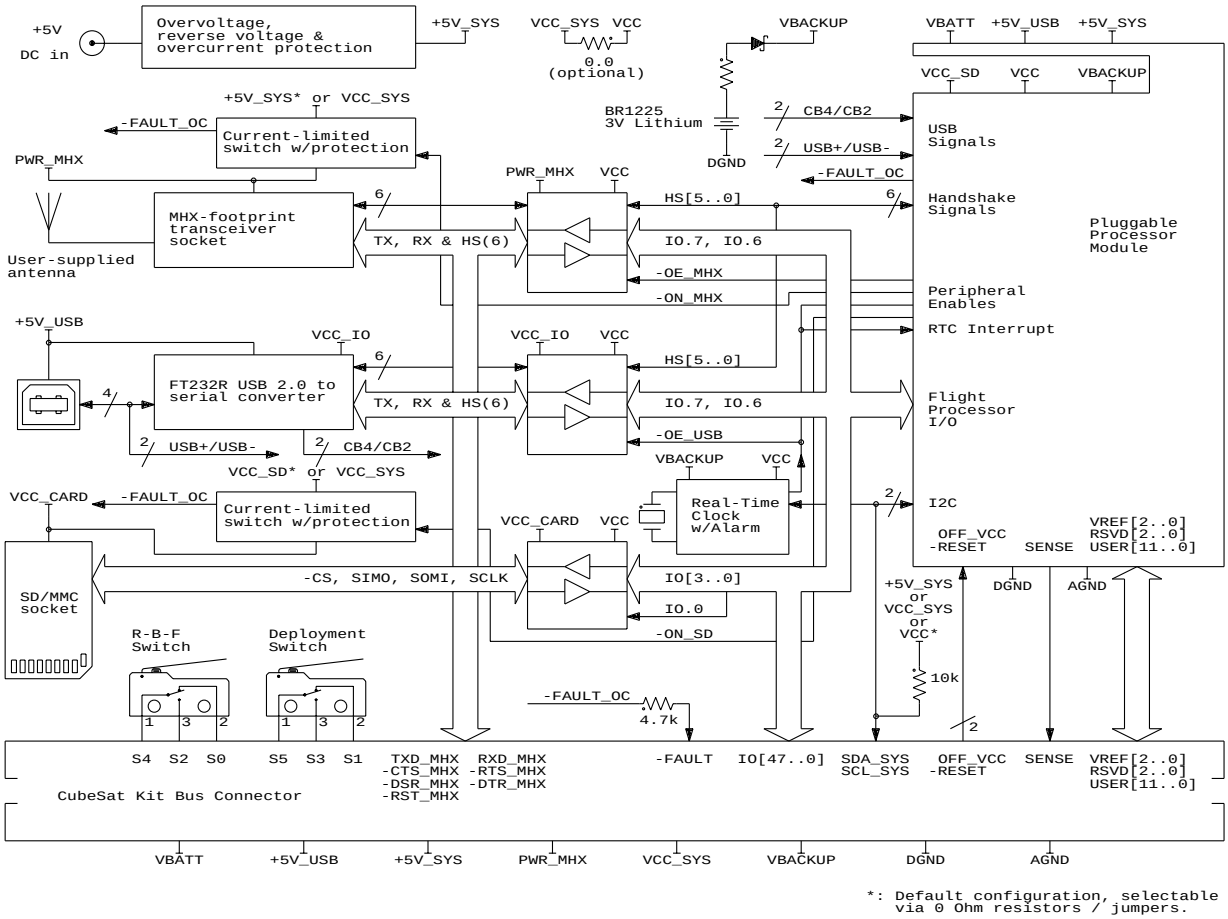
Backup Battery

The MB has a replaceable BR1225 3V Lithium coin cell to serve as a backup battery for real-time clocks and other components requiring battery backup of volatile information.

Battery BT1 is held in place by a coin cell battery holder in one corner of the underside of the MB. The all-metal battery holder is oriented in such a way that once installed onto a CubeSat Kit Base Plate, the battery cannot slide out of its battery holder and is thereby physically restrained along five of six axes. However, since the battery has a conductive outer shell, excessive movement of the battery along its insertion / removal axis could result in a short if it were to contact the Base Plate. Therefore insulating Kapton tape and/or an epoxy or silicone adhesive should be applied to the battery and battery holder.

Alternately, the customer can feed **VBACKUP** on the CubeSat Kit bus via their own backup battery located elsewhere in the system.

BLOCK DIAGRAM



*: Default configuration, selectable via 0 Ohm resistors / jumpers.

PPM PIN DESCRIPTIONS

The PPM connector **H10** connects resources on the MB and accessible via the CubeSat Kit Bus connector to a PPM.[18]

Those signals that are connected directly to the PPM connector and to the CubeSat Kit Bus connectors are tagged under the CSKB label below.[19] Signals marked with an '*' are associated with dedicated peripherals on the MB. They may also be used with off-board peripherals through the proper use of MB peripheral enables and MB power control.

The *potential* for a pin's function is described by the I/O field. The *recommended usage* (as a digital or analog input or output, or as a power pin) is listed in the Description field. I/O pins can generally be configured as general-purpose I/O if the recommended usage is not desired.

Inputs are signals *from* the MB *to* the PPM's processor **U1** or other circuitry. *Outputs* are signals *from* the PPM's processor **U1** or other circuitry *to* the MB.

H10
LSS-150-02-L-DV

<->	IO.23	1	2	IO.47	<->
<->	IO.22	3	4	IO.46	<->
<->	IO.21	5	6	IO.45	<->
<->	IO.20	7	8	IO.44	<->
<->	IO.19	9	10	IO.43	<->
<->	IO.18	11	12	IO.42	<->
<->	IO.17	13	14	IO.41	<->
<->	IO.16	15	16	IO.40	<->
<->	IO.15	17	18	IO.39	<->
<->	IO.14	19	20	IO.38	<->
<->	IO.13	21	22	IO.37	<->
<->	IO.12	23	24	IO.36	<->
<->	IO.11	25	26	IO.35	<->
<->	IO.10	27	28	IO.34	<->
<->	IO.9	29	30	IO.33	<->
<->	IO.8	31	32	IO.32	<->
-->	IO.7 *	33	34	IO.31	<->
<--	IO.6 *	35	36	IO.30	<->
-->	IO.5	37	38	IO.29	<->
<--	IO.4	39	40	IO.28	<->
<--	IO.3 *	41	42	IO.27	<->
-->	IO.2 *	43	44	IO.26	<->
<--	IO.1 *	45	46	IO.25	<->
<--	IO.0 *	47	48	IO.24	<->
	+5V_USB	49	50	+5V_USB	
	+5V_SYS	51	52	+5V_SYS	
	VCC_SD	53	54	VCC_SD	
	VCC	55	56	VCC	
	DGND	57	58	DGND	
	AGND	59	60	AGND	
	VBATT	61	62	VBATT	
	VBACKUP	63	64	VBACKUP	
	VREF0	65	66	-FAULT_OC	-->
	VREF1	67	68	SENSE	-->
	VREF2	69	70	-RESET	<--
	RSVD0	71	72	OFF_VCC	<--
	RSVD1	73	74	SDA_SYS	<->
	RSVD2	75	76	SCL_SYS	-->
-->	USBDP/CB4	77	78	USER0	
-->	USBDM/CB2	79	80	USER1	
<--	-ON_SD	81	82	USER2	
<--	-ON_MHX	83	84	USER3	
<--	-OE_MHX	85	86	USER4	
<->	-OE_USB/-INT	87	88	USER5	
-->	HS0	89	90	USER6	
-->	HS1	91	92	USER7	
-->	HS2	93	94	USER8	
<--	HS3	95	96	USER9	
<--	HS4	97	98	USER10	
<--	HS5	99	100	USER11	

[18] Not included. PPMs are purchased separately from MBs.
[19] The CubeSat Kit's system peripherals are numbered from 0 onwards (e.g., UART0, SPI0, etc.), and this nomenclature is used when referring to a PPM or CSK bus signal.

PPM PIN DESCRIPTIONS – I/O

Name	Pin	I/O	CSKB	Description
IO.0	H10.47	I/O	•	**-CS_SD**. Controls SD Card interface. *Part of the MB's SD card interface. Normally configured as an output from the PPM processor.*
IO.1	H10.45	I/O	•	**SDO0**. SPI master data out. *Part of the MB's SD card interface. Normally configured as an output from the PPM processor.*
IO.2	H10.43	I/O	•	**SDI0**. SPI master data in. *Part of the MB's SD card interface. Normally configured as an input to the PPM processor.*
IO.3	H10.41	I/O	•	**SCK0**. SPI clock. *Part of the MB's SD card interface. Normally configured as an output from the PPM processor.*
IO.4	H10.39	I/O	•	**UTX0**. Tx0 data out. *Often configured as an output from the PPM processor.*
IO.5	H10.37	I/O	•	**URX0**. Rx0 data in. *Often configured as an input to the PPM processor.*
IO.6	H10.35	I/O	•	**UTX1**. Tx1 data out to MHX transceiver or USB. *Part of the MB's MHX/USB interface. Normally configured as an output from the PPM processor.*
IO.7	H10.33	I/O	•	**URX1**. Rx1 data in from MHX transceiver or USB. *Part of the MB's MHX/USB interface. Normally configured as an input to the PPM processor.*
IO.8	H10.31	I/O	•	General-purpose I/O.
IO.9	H10.29	I/O	•	General-purpose I/O.
IO.10	H10.27	I/O	•	General-purpose I/O.
IO.11	H10.25	I/O	•	General-purpose I/O.
IO.12	H10.23	I/O	•	General-purpose I/O.
IO.13	H10.21	I/O	•	General-purpose I/O.
IO.14	H10.19	I/O	•	General-purpose I/O.
IO.15	H10.17	I/O	•	General-purpose I/O.
IO.16	H10.15	I/O	•	General-purpose I/O.
IO.17	H10.13	I/O	•	General-purpose I/O.
IO.18	H10.11	I/O	•	General-purpose I/O.
IO.19	H10.9	I/O	•	General-purpose I/O.
IO.20	H10.7	I/O	•	General-purpose I/O.
IO.21	H10.5	I/O	•	General-purpose I/O.
IO.22	H10.3	I/O	•	General-purpose I/O.
IO.23	H10.1	I/O	•	General-purpose I/O.
IO.24	H10.48	I/O	•	General-purpose I/O.
IO.25	H10.46	I/O	•	General-purpose I/O.
IO.26	H10.44	I/O	•	General-purpose I/O.
IO.27	H10.42	I/O	•	General-purpose I/O.
IO.28	H10.40	I/O	•	General-purpose I/O.
IO.29	H10.38	I/O	•	General-purpose I/O.
IO.30	H10.36	I/O	•	General-purpose I/O.
IO.31	H10.34	I/O	•	General-purpose I/O.
IO.32	H10.32	I/O	•	General-purpose I/O.
IO.33	H10.30	I/O	•	General-purpose I/O.
IO.34	H10.28	I/O	•	General-purpose I/O.
IO.35	H10.26	I/O	•	General-purpose I/O.
IO.36	H10.24	I/O	•	General-purpose I/O.
IO.37	H10.22	I/O	•	General-purpose I/O.
IO.38	H10.20	I/O	•	General-purpose I/O.
IO.39	H10.18	I/O	•	General-purpose I/O.
IO.40	H10.16	I/O	•	General-purpose I/O. *Normally configured as analog input **AN0** to the PPM processor.*

IO.41	H10.14	I/O	•	General-purpose I/O. *Normally configured as analog input **AN1** to the PPM processor.*
IO.42	H10.12	I/O	•	General-purpose I/O. *Normally configured as analog input **AN2** to the PPM processor.*
IO.43	H10.10	I/O	•	General-purpose I/O. *Normally configured as analog input **AN3** to the PPM processor.*
IO.44	H10.8	I/O	•	General-purpose I/O. *Normally configured as analog input **AN4** to the PPM processor.*
IO.45	H10.6	I/O	•	General-purpose I/O. *Normally configured as analog input **AN5** to the PPM processor.*
IO.46	H10.4	I/O	•	General-purpose I/O. *Normally configured as analog input **AN6** to the PPM processor.*
IO.47	H10.2	I/O	•	General-purpose I/O. *Normally configured as analog input **AN7** to the PPM processor.*

PPM PIN DESCRIPTIONS – Power

Name	Pin	I/O	CSKB	Description
+5V_USB	H10.49 H10.50	–	•	+5V USB power. From USB host. Powers on-board USB-to-serial converter and PPM.
+5V_SYS	H10.51 H10.52	–	•	+5V system power. From EPS or external +5V connector. Powers some on-board peripherals and PPM.
VCC_SD	H10.53 H10.54	–		SD Card power. Nominally +3.3V. Sourced from PPM or from **VCC_SYS** via **R58**.
VCC	H10.55 H10.56	–		MB power and I/O level. From +1.65V to +5.5V. Sourced from PPM or from **VCC_SYS** via **R68**.
DGND	H10.57 H10.58	–	•	Digital ground.
AGND	H10.59 H10.60	–	•	Analog ground.
VBATT	H10.61 H10.62	–	•	Battery voltage. EPS-dependent. Typically +7V to +10V.
VBACKUP	H10.63 H10.64	–	•	Battery backup voltage (e.g. for RTC). From MB's 3V Lithium battery **BT1**.

PPM PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	CSKB	Description
VREF0	H10.65	-	•	Intended for analog voltage references.
VREF1	H10.67	-	•	Intended for analog voltage references.
VREF2	H10.69	-	•	Intended for analog voltage references.

PPM PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	CSKB	Description
RSVD0	H10.71	–	•	Not connected. Reserved for future use.
RSVD1	H10.73	–	•	Not connected. Reserved for future use.
RSVD2	H10.75	–	•	Not connected. Reserved for future use.

PPM PIN DESCRIPTIONS – MB-Specific

Name	Pin	I/O	CSKB	Description
CB4	H10.77	I		Configurable CBUS4 signal from FT232R USB chip **U7**.
USBDP				When **U7** is not fitted and **R56** is fitted, provides the '+' half of the USB differential signal pair from **J3** to the PPM processor.

CB2	H10.79	I		Configurable CBUS2 signal from FT232R USB chip **U7**.
USBDM				When **U7** is not fitted and **R57** is fitted, provides the '-' half of the USB differential signal pair from **J3** to the PPM processor.
-ON_SD	H10.81	O		Control signal for SD Card power. Active LOW, pulled high on MB. When active, enables **VCC_CARD** on MB, thereby powering SC Card socket and SD Card level translators / isolators **U17** & **U18**. *Normally configured as a digital output from the PPM processor.*
-ON_MHX	H10.83	O		Control signal for MHX socket power. Active LOW, pulled high on MB. When active, enables **PWR_MHX** on MB, thereby powering MHX socket and MHX level translators / isolators **U2** & **U3**. *Normally configured as a digital output from the PPM processor.*
-OE_MHX	H10.85	O		Control signal for MHX interface. Active LOW, pulled high on MB. When active, enables signals to pass through MHX level translators / isolators **U2** & **U3**. *Normally configured as a digital output from the PPM processor.*
-OE_USB	H10.87	O		Control signal for USB interface. Active LOW, pulled high on MB. When active, enables signals to pass through USB level translators / isolators **U1** & **U16**. *Normally configured as a digital output from the PPM processor.*
-INT		I		Output from RTC's –IRQ open-collector output. When properly configured, can be used to interrupt Processor via RTC. *Normally configured as a digital input to the PPM processor.*
HS0	H10.89	I		Handshake signal. –RTS (USB) or –CTS (MHX). *Normally an input to the PPM processor. Requires that **R10** be fitted on the MB.*
HS1	H10.91	I		Handshake signal. –DTR (USB) or –DSR (MHX). *Normally an input to the PPM processor. Requires that **R11** be fitted on the MB.*
HS2	H10.93	I		Handshake signal. –PWE (USB) or –DCD (MHX). *Normally an input to the PPM processor. Requires that **R12** be fitted on the MB.*
HS3	H10.95	O		Handshake signal. –CTS (USB) or –RTS (MHX). *Normally an output from the PPM processor. Requires that **R75** be fitted on the MB.*
HS4	H10.97	O		Handshake signal. –RI (USB) or –DTR (MHX). *Normally an output from the PPM processor. Requires that **R76** be fitted on the MB.*
HS5	H10.99	O		Handshake (reset) signal. –RST (USB) or –RST (MHX). *Normally an output from the PPM processor. Requires that **R77** be fitted on the MB.*

PPM PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	CSKB	Description
-FAULT_OC	H10.66	O		Open-collector output from PPM's latchup prevention overcurrent switch. Active LOW. Wire-ORed to –FAULT_OC on MB.
SENSE	H10.68	O	•	Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – **SENSE**) / 75mΩ. Depends on PPM implementation.
-RESET	H10.70	I	•	Reset signal to PPM's reset supervisor. Active LOW.
OFF_VCC	H10.72	I	•	Control signal to PPM's power circuit(s). Active HIGH.

PPM PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	CSKB	Description
SDA_SYS	H10.74	I/O	•	I2C data. *Normally configured as an I2C data input/output to/from the processor.*
SCL_SYS	H10.76	O	•	I2C clock. *Normally configured as an I2C clock output from the PPM processor.*

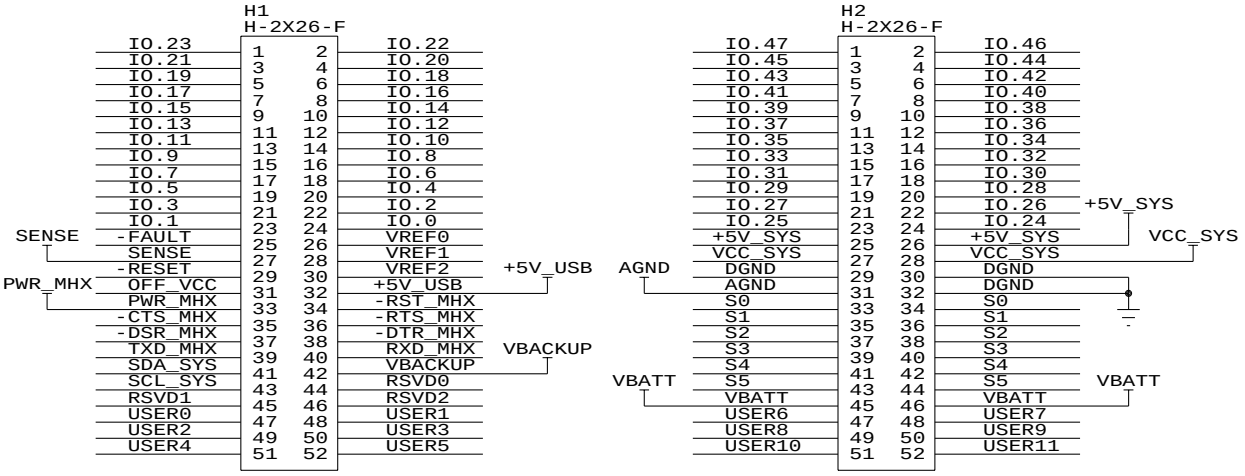
PPM PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	CSKB	Description
USER0	H10.78	I/O	•	User-defined.
USER1	H10.80	I/O	•	User-defined.
USER2	H10.82	I/O	•	User-defined.
USER3	H10.84	I/O	•	User-defined.
USER4	H10.86	I/O	•	User-defined.
USER5	H10.88	I/O	•	User-defined.
USER6	H10.90	I/O	•	User-defined.
USER7	H10.92	I/O	•	User-defined.
USER8	H10.94	I/O	•	User-defined.
USER9	H10.96	I/O	•	User-defined.
USER10	H10.98	I/O	•	User-defined.
USER11	H10.100	I/O	•	User-defined.

CubeSat Kit Bus PIN DESCRIPTIONS [20]

Those signals that are connected directly between the CubeSat Kit Bus connectors and the PPM connector are tagged under the PPM label below.

CubeSat Kit Bus Connectors



CubeSat Kit Bus PIN DESCRIPTIONS – I/O

Name	Pin	I/O	PPM	Description
IO.0	H1.24	I/O	•	**-CS_SD**. Controls SD Card interface. *Part of the MB's SD card interface. Normally configured as an output from the PPM processor.*
IO.1	H1.23	I/O	•	**SDO0**. SPI master data out. *Part of the MB's SD card interface. Normally configured as an output from the PPM processor.*
IO.2	H1.22	I/O	•	**SDI0**. SPI master data in. *Part of the MB's SD card interface. Normally configured as an input to the PPM processor.*
IO.3	H1.21	I/O	•	**SCK0**. SPI clock. *Part of the MB's SD card interface. Normally configured as an output from the PPM processor.*
IO.4	H1.20	I/O	•	**UTX0**. Tx0 data out. *Often configured as an output from the PPM processor.*
IO.5	H1.19	I/O	•	**URX0**. Rx0 data in. *Often configured as an input to the PPM processor.*
IO.6	H1.18	I/O	•	**UTX1**. Tx1 data out to MHX transceiver or USB. *Part of the MB's MHX/USB interface. Normally configured as an output from the PPM processor.*
IO.7	H1.17	I/O	•	**URX1**. Rx1 data in from MHX transceiver or USB. *Part of the MB's MHX/USB interface. Normally configured as an input to the PPM processor.*
IO.8	H1.16	I/O	•	General-purpose I/O.
IO.9	H1.15	I/O	•	General-purpose I/O.
IO.10	H1.14	I/O	•	General-purpose I/O.
IO.11	H1.13	I/O	•	General-purpose I/O.
IO.12	H1.12	I/O	•	General-purpose I/O.
IO.13	H1.11	I/O	•	General-purpose I/O.
IO.14	H1.10	I/O	•	General-purpose I/O.
IO.15	H1.9	I/O	•	General-purpose I/O.
IO.16	H1.8	I/O	•	General-purpose I/O.

[20] The fact that the CubeSat Kit Bus has 104 pins (like PC/104) is purely coincidental – the original CubeSat Kit Bus used in the Rev A and Rev B FM430 had only 80 pins, and was expanded in Rev C to 104 pins.

IO.17	H1.7	I/O	•	General-purpose I/O.
IO.18	H1.6	I/O	•	General-purpose I/O.
IO.19	H1.5	I/O	•	General-purpose I/O.
IO.20	H1.4	I/O	•	General-purpose I/O.
IO.21	H1.3	I/O	•	General-purpose I/O.
IO.22	H1.2	I/O	•	General-purpose I/O.
IO.23	H1.1	I/O	•	General-purpose I/O.
IO.24	H2.24	I/O	•	General-purpose I/O.
IO.25	H2.23	I/O	•	General-purpose I/O.
IO.26	H2.22	I/O	•	General-purpose I/O.
IO.27	H2.21	I/O	•	General-purpose I/O.
IO.28	H2.20	I/O	•	General-purpose I/O.
IO.29	H2.19	I/O	•	General-purpose I/O.
IO.30	H2.18	I/O	•	General-purpose I/O.
IO.31	H2.17	I/O	•	General-purpose I/O.
IO.32	H2.16	I/O	•	General-purpose I/O.
IO.33	H2.15	I/O	•	General-purpose I/O.
IO.34	H2.14	I/O	•	General-purpose I/O.
IO.35	H2.13	I/O	•	General-purpose I/O.
IO.36	H2.12	I/O	•	General-purpose I/O.
IO.37	H2.11	I/O	•	General-purpose I/O.
IO.38	H2.10	I/O	•	General-purpose I/O.
IO.39	H2.9	I/O	•	General-purpose I/O.
IO.40	H2.8	I/O	•	General-purpose I/O. *Normally configured as analog input **AN0** to the PPM processor.*
IO.41	H2.7	I/O	•	General-purpose I/O. *Normally configured as analog input **AN1** to the PPM processor.*
IO.42	H2.6	I/O	•	General-purpose I/O. *Normally configured as analog input **AN2** to the PPM processor.*
IO.43	H2.5	I/O	•	General-purpose I/O. *Normally configured as analog input **AN3** to the PPM processor.*
IO.44	H2.4	I/O	•	General-purpose I/O. *Normally configured as analog input **AN4** to the PPM processor.*
IO.45	H2.3	I/O	•	General-purpose I/O. *Normally configured as analog input **AN5** to the PPM processor.*
IO.46	H2.2	I/O	•	General-purpose I/O. *Normally configured as analog input **AN6** to the PPM processor.*
IO.47	H2.1	I/O	•	General-purpose I/O. *Normally configured as analog input **AN7** to the PPM processor.*

CubeSat Kit Bus PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	PPM	Description
VREF0	H1.26	-	•	Intended for analog voltage references.
VREF1	H1.30	-	•	Intended for analog voltage references.
VREF2	H1.28	-	•	Intended for analog voltage references.

CubeSat Kit Bus PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	PPM	Description
RSVD0	H1.44	–	•	Not connected. Reserved for future use.
RSVD1	H1.45	–	•	Not connected. Reserved for future use.
RSVD2	H1.46	–	•	Not connected. Reserved for future use.

CubeSat Kit Bus PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	PPM	Description
SDA_SYS	H1.41	I/O	•	I2C data. *Normally configured as an I2C data input/output to/from the processor.*
SCL_SYS	H1.43	O	•	I2C clock. *Normally configured as an I2C clock output from the PPM processor.*

CubeSat Kit Bus PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	PPM	Description
-FAULT	H1.25	O	•	Open-collector output. Active LOW. Active when an overcurrent fault condition is detected by any of the MB's or PPM's latchup prevention overcurrent switches. With series 4.7kΩ resistor. Normally pulled up externally to **VCC_SYS** or **+5V_SYS**.
SENSE	H1.27	O	•	Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – **SENSE**) / 75mΩ. Depends on PPM implementation.
-RESET	H1.29	I	•	Reset signal to PPM's reset supervisor. Active LOW.
OFF_VCC	H1.31	I	•	Control signal to PPM's power circuit(s). Active HIGH.

CubeSat Kit Bus PIN DESCRIPTIONS – RBF and Launch Switches

Name	Pin	I/O	PPM	Description
S0	H2.33 H2.34	–		Switch terminal. Normally connected to RBF Switch normally closed (NC) terminal.
S1	H2.35 H2.36	–		Switch terminal. Normally connected to Deployment Switch normally closed (NC) terminal.
S2	H2.37 H2.38	–		Switch terminal. Normally connected to RBF Switch normally open (NO) terminal.
S3	H2.39 H2.40	–		Switch terminal. Normally connected to Deployment Switch normally open (NO) terminal.
S4	H2.41 H2.42	–		Switch terminal. Normally connected to RBF Switch common (C) terminal.
S5	H2.43 H2.44	–		Switch terminal. Normally connected to Deployment Switch common (C) terminal.

CubeSat Kit Bus PIN DESCRIPTIONS – Power

Name	Pin	I/O	PPM	Description
VBATT	H2.45 H2.46	–	•	Battery voltage. EPS-dependent. Typically +7V to +10V.
+5V_USB	H1.32	–	•	+5V USB power. From USB host.
+5V_SYS	H2.25 H2.26	–	•	+5V system power. From EPS or external +5V connector.
PWR_MHX	H1.33	–	•	MHX transceiver power. Derived from **+5V_SYS** or **VCC_SYS** system power. Under PPM control. The current used by the MHX transceiver is (**+5V_SYS** – **PWR_MHX**) / 75mΩ or (**VCC_SYS** – **PWR_MHX**) / 75mΩ, depending on the source of MHX power. Can be overridden by feeding **+5V_SYS** or **VCC_SYS** directly into **PWR_MHX**.
VBACKUP	H1.42	–	•	Battery backup voltage (e.g. for RTC). From MB's 3V Lithium battery **BT1**.
VCC_SYS	H2.27 H2.28	–	•	VCC system power. Normally generated by EPS. Not normally connected to MB's local **VCC**.
AGND	H2.31	–	•	Analog ground.

DGND	H2.29 H2.30 H2.32	–	•	Digital ground.

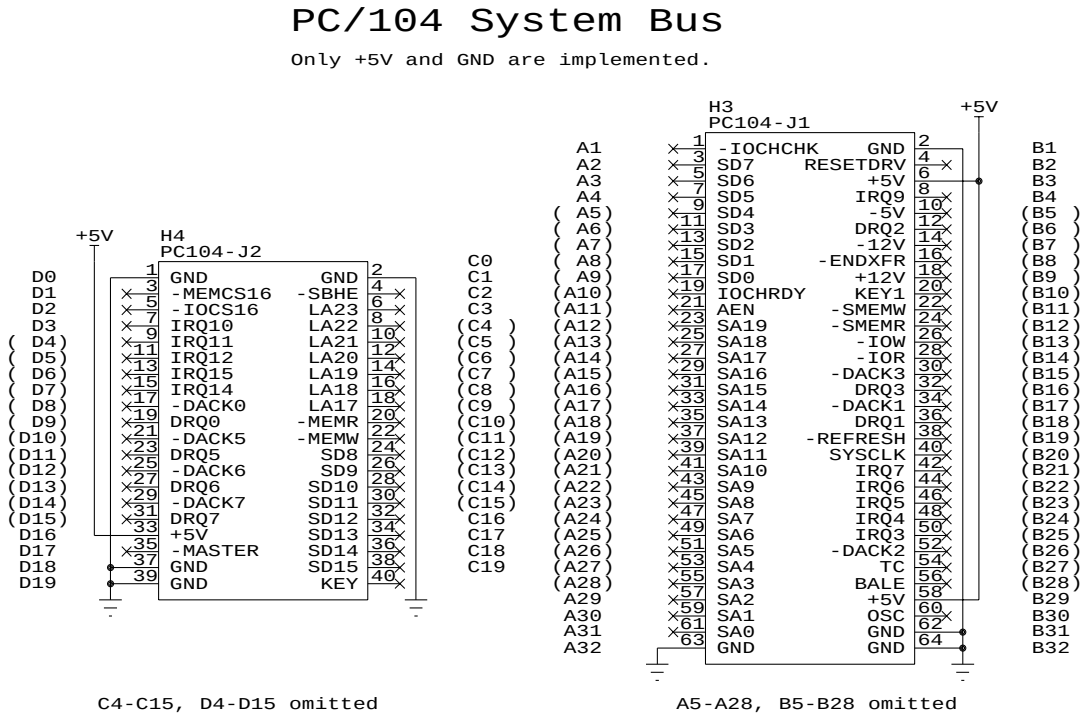
CubeSat Kit Bus PIN DESCRIPTIONS – Transceiver Interface

Name	Pin	I/O	PPM	Description
-RST_MHX	H1.34	I		Reset input to transceiver. Active LOW.
-CTS_MHX	H1.35	O		Clear-to-send output from transceiver. Active LOW.
-RTS_MHX	H1.36	I		Request-To-Send input to transceiver. Active LOW.
-DSR_MHX	H1.37	O		Data Set Ready output from transceiver. Active LOW.
-DTR_MHX	H1.38	I		Data Transmit Ready input to transceiver. Active LOW.
TXD_MHX	H1.39	I		Transmit data input to transceiver. Idles HIGH.
RXD_MHX	H1.40	O		Receive data output from transceiver. Idles HIGH.

CubeSat Kit Bus PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	PPM	Description
USER0	H1.47	I/O	•	User-defined.
USER1	H1.48	I/O	•	User-defined.
USER2	H1.49	I/O	•	User-defined.
USER3	H1.50	I/O	•	User-defined.
USER4	H1.51	I/O	•	User-defined.
USER5	H1.52	I/O	•	User-defined.
USER6	H2.47	I/O	•	User-defined.
USER7	H2.48	I/O	•	User-defined.
USER8	H2.49	I/O	•	User-defined.
USER9	H2.50	I/O	•	User-defined.
USER10	H2.51	I/O	•	User-defined.
USER11	H2.52	I/O	•	User-defined.

PC/104 System Bus PIN DESCRIPTIONS



The MB implements a subset of the PC/104 specification in the form of two connectors that provide only +5V and GND for PC/104 modules. Only a total of 32 pins are implemented, 16 on **J1** and 16 on **J2**. By adding up to four 8-pin connectors to the MB, PC/104 modules can be plugged directly into the MB to obtain +5V power and GND. No other connections between the PC/104 bus and the CubeSat Kit Bus are provided.

CONNECTORS

Item	Description	Source	Part Number	Application
1	52-pin non-stackthrough	Samtec[21]	ESQ-126-37-G-D	CubeSat Kit Bus connector for non-stackthrough applications (e.g., MB option /00).
2	52-pin stackthrough	Samtec	ESQ-126-39-G-D	CubeSat Kit Bus connector for stackthrough applications (e.g., MB option /10).
3	52-pin	Samtec	SSQ-126-22-G-D	CubeSat Kit Bus connector 10mm extension.
4	8-pin non-stackthrough	Samtec	ESQ-104-37-G-D	CubeSat Kit PC/104 power connector for non-stackthrough applications.
5	8-pin stackthrough	Samtec	ESQ-104-39-G-D	CubeSat Kit PC/104 power connector for stackthrough applications.
6	8-pin	Samtec	SSQ-104-22-G-D	CubeSat Kit PC/104 power connector 10mm extension.
7	100-pin, hermaphroditic	Samtec	LSS-150-02-L-DV	PPM connector (standard, +6mm)

Items 1-6: Non-stackthrough connectors are normally fitted only to an MB and form an endpoint to the CubeSat Kit Bus connector stack. Stackthrough connectors are normally fitted to all other modules (e.g. EPS modules). The normal stacking height is 15mm between modules. The 10mm extension can be used to increase this distance, e.g. to 25mm. 8-pin connectors are used to provide +5V and GND (only) to PC/104 modules. A 15mm extension can be accomplished via a stackthrough connector.

[21] http://www.samtec.com/, 1-800-SAMTEC9.

This connector information is provided for reference only.

REPLACEMENT FUSES

The overcurrent fuse **F1** protects only against overcurrent conditions drawing too much current from the external +5V dc supply. It is soldered in place. The replacement fuse is LittleFuse 0451004.MRL, 4A, 125V, fast-acting Nano SMF Fuse, and is available e.g. through Digi-Key®. Should replacement be required, it should be replaced by the factory or by a qualified electronics technician.

BACKWARDS COMPATIBILITY

Please note the following when replacing a Rev C FM430 with a Rev D MB:

- **H8**: The RSSI breakout connector for the MHX transceiver is no longer supported and is not present on the MB.

Users with older (i.e., Rev A or Rev B) FM430s should consult the FM430 Rev C datasheet for issues concerning backwards compatibility.

MHX WIRELESS TRANSCEIVER COMPATIBILITY

The MB is designed to interface directly to Microhard Corporation's[22] line of MHX OEM wireless transceiver modules, and any other footprint-compatible transceivers. The mechanical interface is through four M2.5 F/F threaded standoffs at a prescribed height of 15.5mm above the MB PCB. The electrical interface is through the MB's **H5** connectors, which connect the MHX module to the MB via the MHX pins 1-17 and 21-33 only.[23] Because of minor physical differences between the earlier (e.g., MHX-2400) and later (e.g., MHX-2420) Microhard transceivers, the MB as supplied from the factory supports only later transceivers. The MB uses a high-side switch capable of supplying currents to the transceiver greatly in excess of the 1.2A supplied by the FM430 Revs A through C.

[22] http://www.microhardcorp.com/.

[23] These pins were originally No Connect (NC) on the MHX-2400 and similar modules. Later versions use these pins. The functionality of most of these additional pins is not required to operate these newer MHX modules (e.g,. MHX-2420), and hence they are backwards-compatible with the earlier MHX modules.

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DATA SHEET

SKY65116: 390 to 500 MHz Linear Power Amplifier

Applications

- TETRA radio
- GSM450 and GSM480
- NMT450
- Wireless local loop

Features

- Wideband frequency operation: 390 to 500 MHz
- High linearity: OIP3 +43 dBm
- High efficiency: 40% PAE
- High gain: 35 dB
- P1dB = +32.5 dBm
- Single DC supply: 3.6 V
- Internal RF match and bias circuits
- PA on/off voltage control
- Operating temperature: –40 °C to +85 °C
- Low cost, MCM (12-pin, 8 x 8 mm) Pb-free (MSL3, 250 °C per JEDEC J-STD-020) package

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

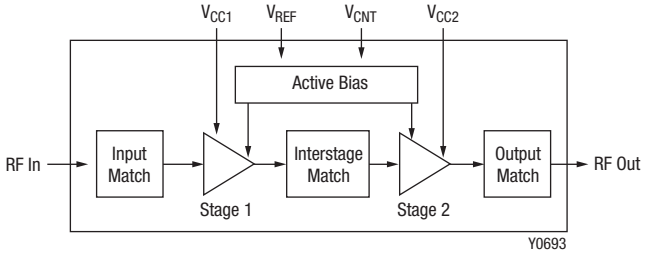


Figure 1. SKY65116 Functional Block Diagram

Description

The SKY65116 is a fully matched, linear Power Amplifier (PA), high linearity and high efficiency surface mount module designed for use in the 390 to 500 MHz band.

The device is fabricated using Skyworks high reliability Gallium Arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) process, which allows for single supply operation while maintaining high efficiency and good linearity. Microwave Monolithic Integrated Circuits (MMICs), comprised of GaAs and Silicon CMOS, contain all the active circuitry in the module. This includes the in-module bias circuitry, as well as the RF interstage matching circuit. The input and output match is realized off-chip within the module package to optimize efficiency and high power performance ($P_{1\,dB}$ = +32.5 dBm) into a 50 Ω load.

Primary bias to the SKY65116 can be supplied directly from a single cell lithium-ion or other suitable battery with a nominal output of 3.6 V. No external supply side switch is needed as typical “off” leakage is a few microamperes with full primary voltage supplied from the battery.

The module can operate over the temperature range of –40 °C to +85 °C.

The SKY65116 is provided in a low-cost, Surface Mount Technology (SMT) 8 x 8 mm Multi-Chip Module (MCM) package. Figure 1 shows a functional block diagram for the SKY65116. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

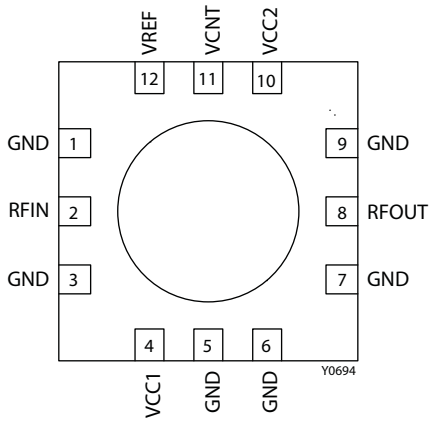


Figure 2. SKY65116 Pinout– 12-Pin MCM Package

Table 1. SKY65116 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	7	GND	Ground
2	RFIN	RF input	8	RFOUT	RF output
3	GND	Ground	9	GND	Ground
4	VCC1	Stage 1 collector voltage	10	VCC2	Stage 2 collector voltage
5	GND	Ground	11	VCNT	PA on/off coltrol voltage
6	GND	Ground	12	VREF	Bias reference voltage

Technical Description

The SKY65116 is comprised of two amplifier stages. The matching circuits for the input stage, inter-stage, and output stage are contained within the device. The bias circuits for both input and output stages are included within the device for optimum temperature tracking performance.

The SKY65116 is internally matched for optimum linearity and efficiency. The input and output stages are independently supplied using the VCC1 and VCC2 supply lines, pins 4 and 10, respectively. The bias reference voltage is supplied using a common VREF (pin 12) line. The device can be switched on and off using the VCNT signal (pin 11).

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY65116 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics over temperature of the SKY65116 are illustrated in Figures 3 through 29.

Figure 34 shows the package dimensions for the 12-pin SKY65116 MCM and Figure 35 provides the tape and reel dimensions.

Table 2. SKY65116 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Min	Typical	Max	Units
RF output power	P_{OUT}			+34.5	dBm
Supply voltage	V_{CC1}, V_{CC2}, V_{REF}, V_{CNT}			4.5	V
Supply current	I_{CC}			1300	mA
Power dissipation	P_{DISS}			3.7	W
Case operating temperature	T_C	–40		+85	°C
Storage temperature	T_{ST}	–55		+125	°C
Junction temperature	T_J			+150	°C

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY65116 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	V_{CC}	3.2	3.6	4.0	V
Reference voltage	V_{REF}	3.2	3.6	4.0	V
Control voltage (power-up)	V_{CNT}	2.7	3.6		V
Control voltage (power down)	V_{CNT}		0	0.5	V
Operating frequency	f	390		500	MHz
Operating case temperature	T_C	–40	+25	+85	°C

Table 4. SKY65116 Electrical Characteristics
(VCC1 = VCC2 = VCNT = VREF = 3.6 V, T_C = +25 °C, Z0 = 50 Ω, Unless Otherwise Specified)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency	F		390		500	MHz
Quiescent current	I_{CQ}	No RF	0.1	0.33	0.375	A
Small signal gain	G	P_{IN} = -15 dBm	33.5	35		dB
Input return loss	$\|S_{11}\|$	P_{IN} = -15 dBm	10	22		dB
Output return loss	$\|S_{22}\|$	P_{IN} = -15 dBm	4.5	6		dB
Output power	P_{OUT}	@ $P_{1\ dB}$	31.5	32.5		dBm
Power added efficiency	PAE	P_{OUT} @ $P_{1\ dB}$	35	42		%
Output IP3	OIP3	P_{OUT} = 25 dBm/tone	38	43		dBm
Noise figure	NF	P_{IN} = -15 dBm		6	7.5	dB
Thermal resistance	Θ_{JC}	Junction to case		17.6		°C/W

Typical Performance Characteristics
(VCC1 = VCC2 = VCNT = VREF = 3.6 V, T_C = +25 °C, Z0 = 50 Ω, Unless Otherwise Specified)

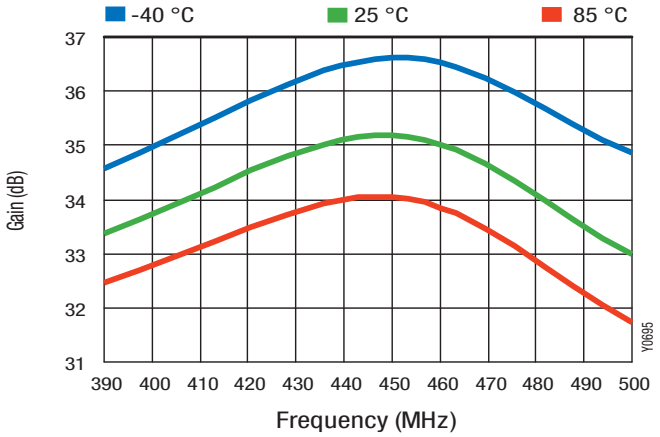


Figure 3. Gain vs Frequency Across Temperature

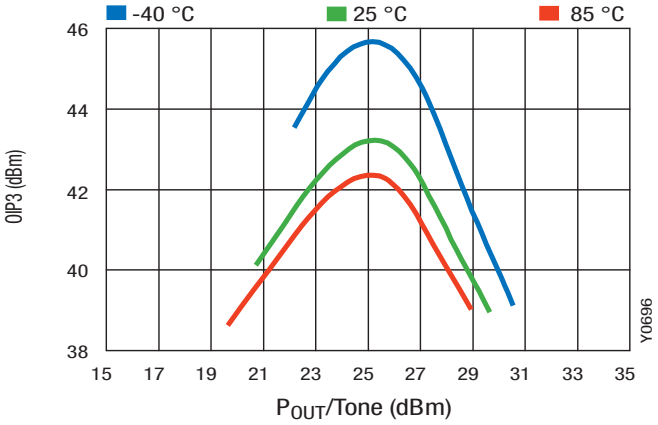


Figure 4. OIP3 vs Output Power /Tone Across Temperature

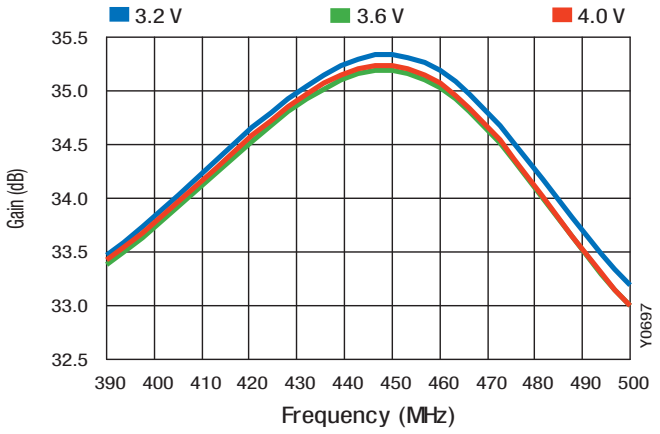


Figure 5. Gain vs Frequency Across Voltage

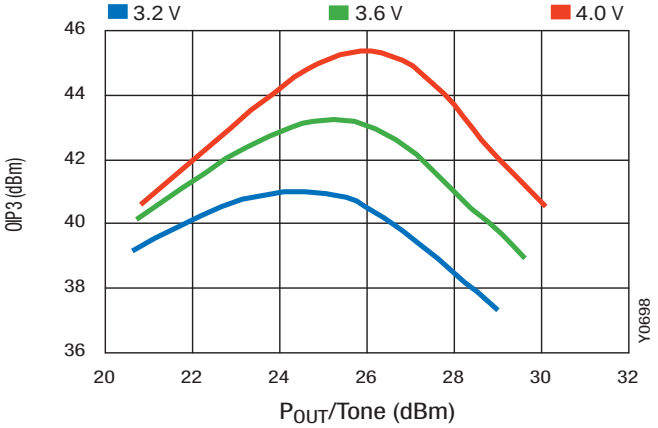


Figure 6. OIP3 vs Output Power /Tone Across Voltage

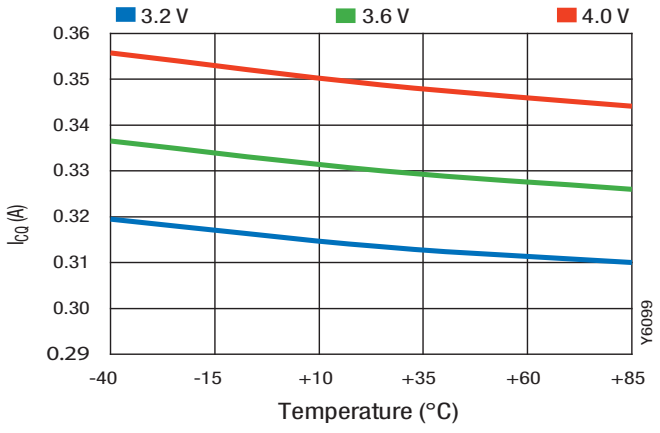


Figure 7. I_{CQ} vs Temperature Across Voltage

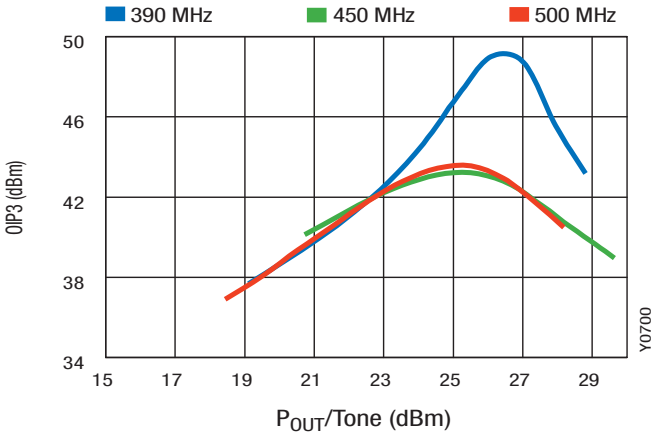


Figure 8. OIP3 vs Output Power/Tone Across Frequency

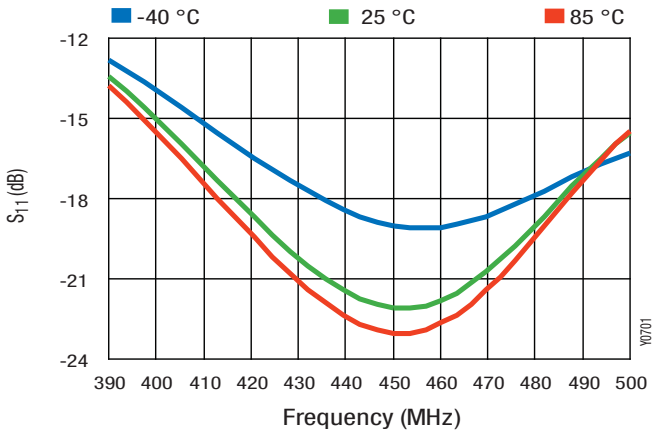


Figure 9. S11 vs Frequency Across Temperature

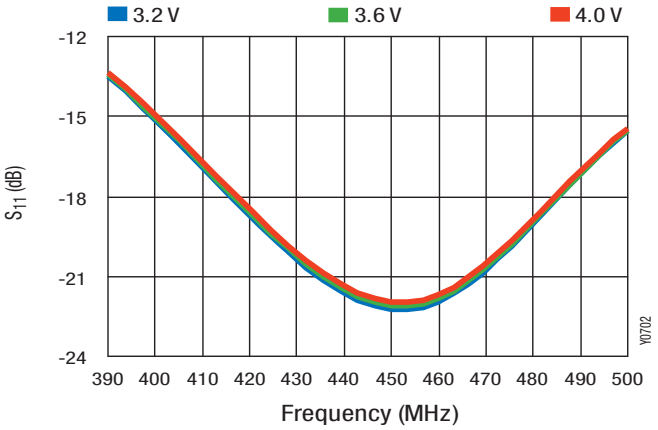


Figure 10. S11 vs Frequency Across Vcc

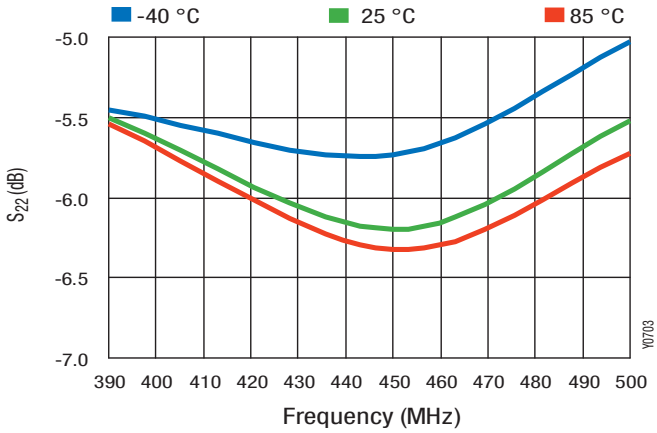


Figure 11. S22 vs Frequency Across Temperature

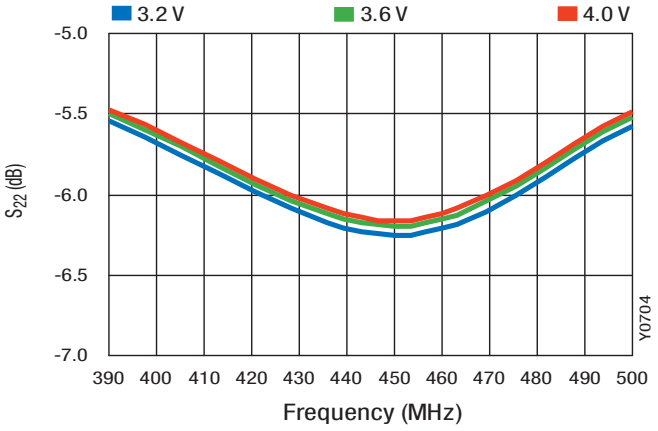


Figure 12. S22 vs Frequency Across Vcc

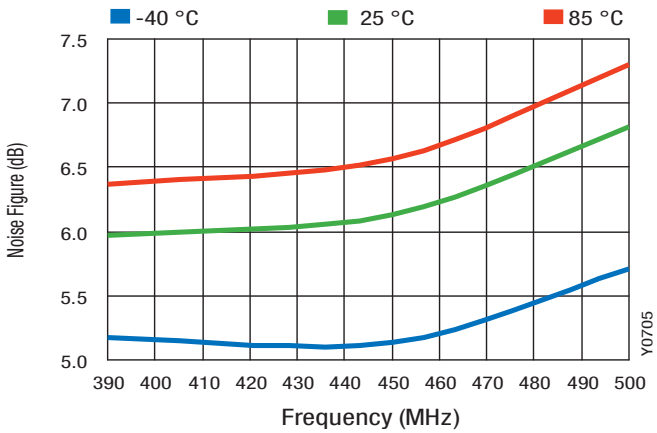


Figure 13. Noise Figure vs Frequency Across Temperature

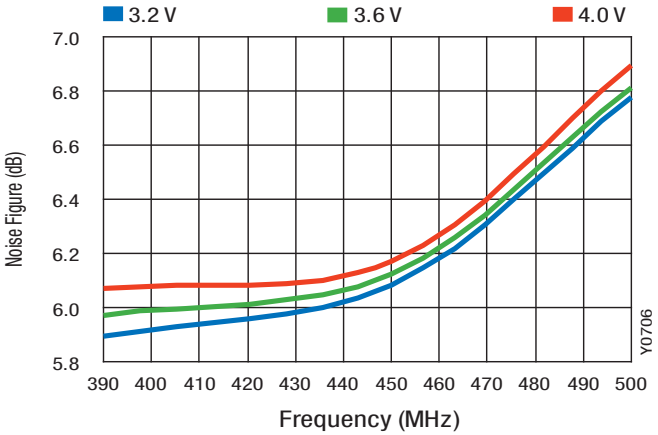


Figure 14. Noise Figure vs Frequency Across VCC

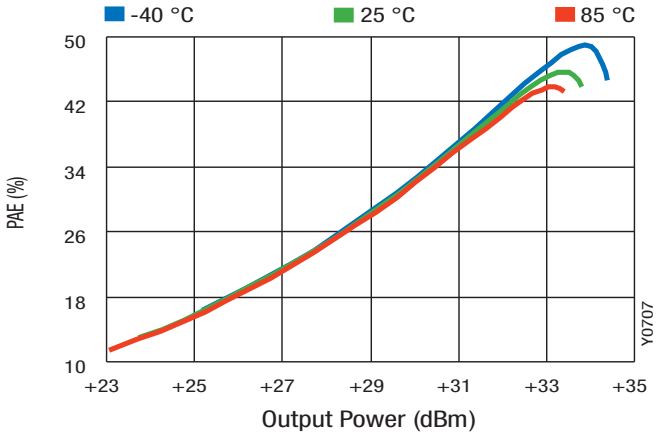


Figure 15. PAE vs Output Power Across Temperature

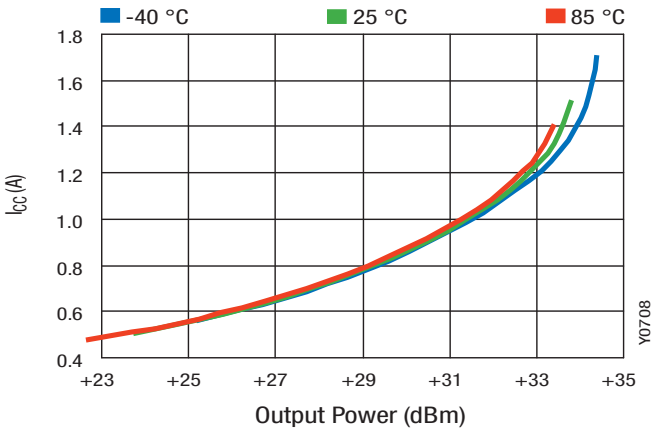


Figure 16. ICC vs Output Power Across Temperature

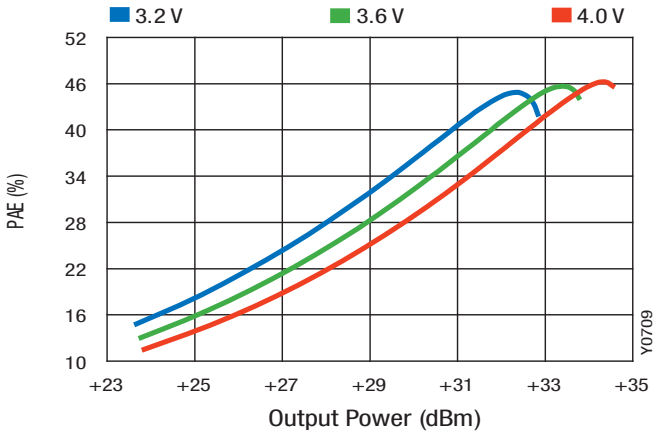


Figure 17. PAE vs Output Power Across VCC

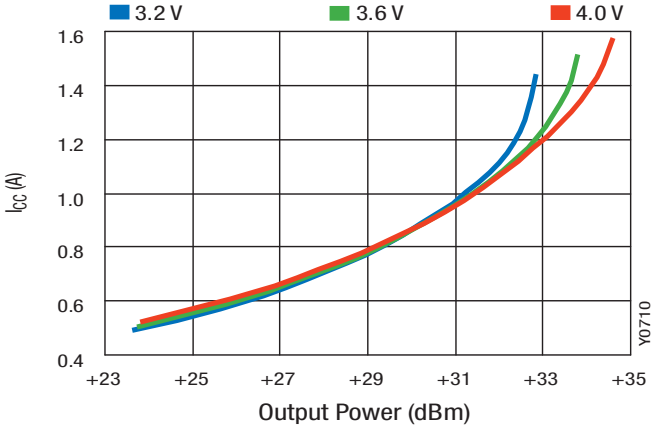


Figure 18. ICC vs Output Power Across VCC

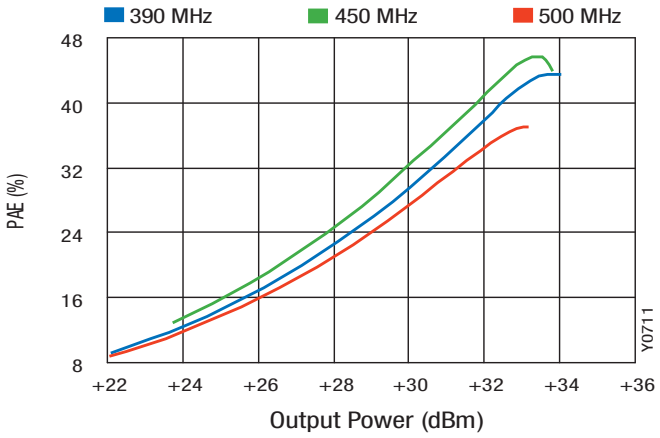


Figure 19. PAE vs Output Power Across Frequency

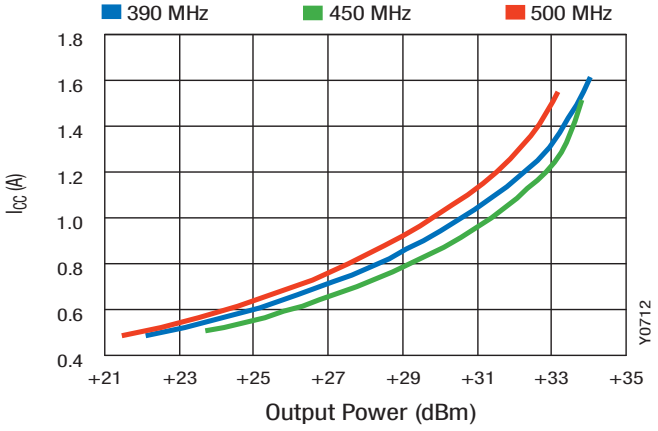


Figure 20. ICC vs Output Power Across Frequency

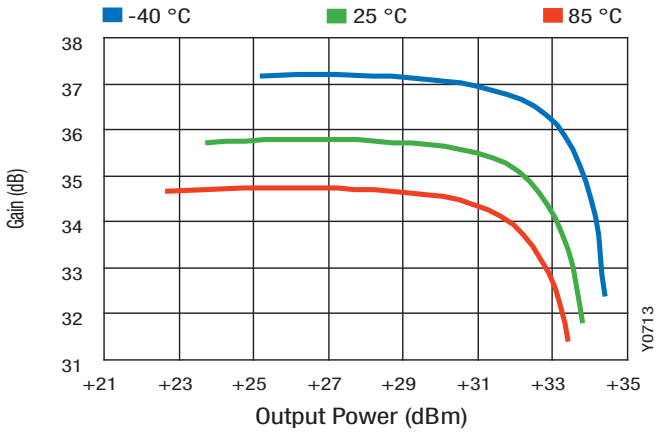


Figure 21. Gain vs Output Power Across Temperature

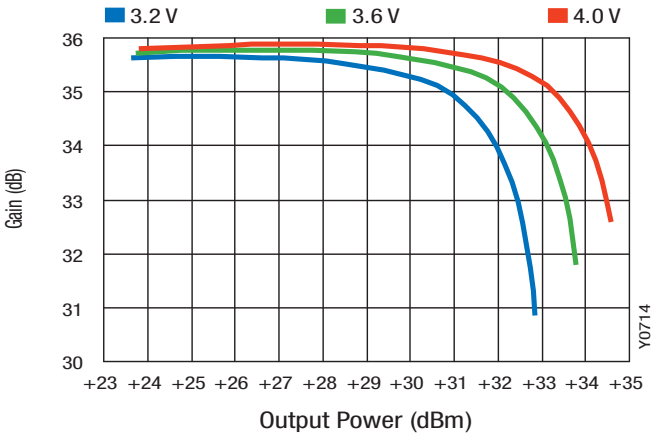


Figure 22. Gain vs Output Power Across VCC

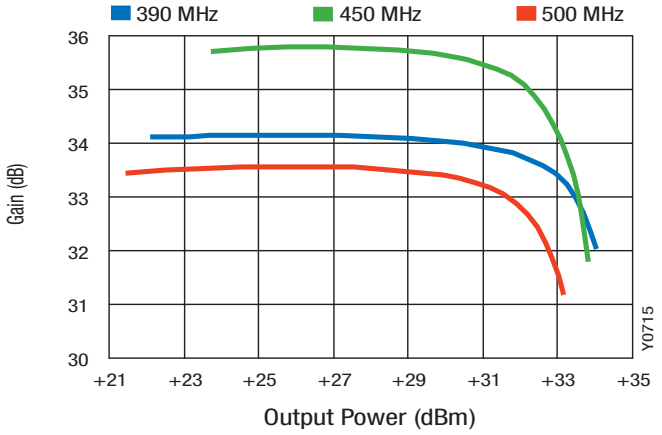


Figure 23. Gain vs Output Power Across Frequency

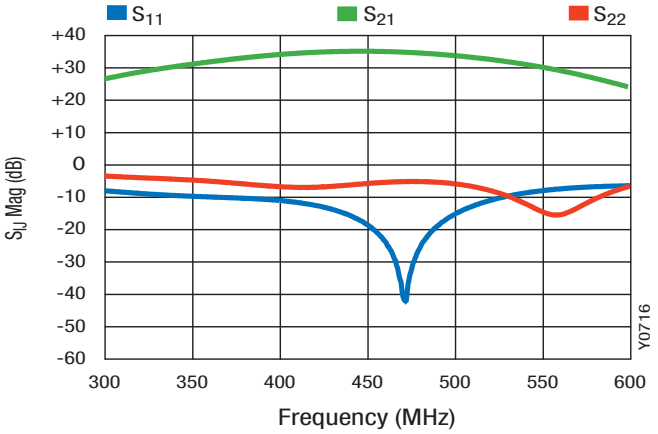


Figure 24. S-Parameters vs Frequency

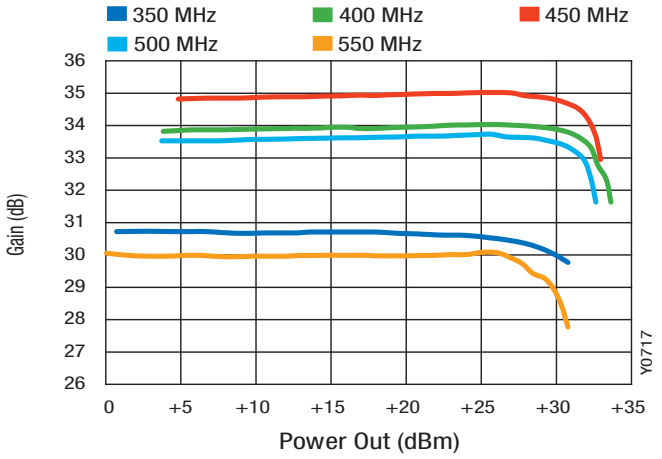


Figure 25. Gain vs CW Power Out

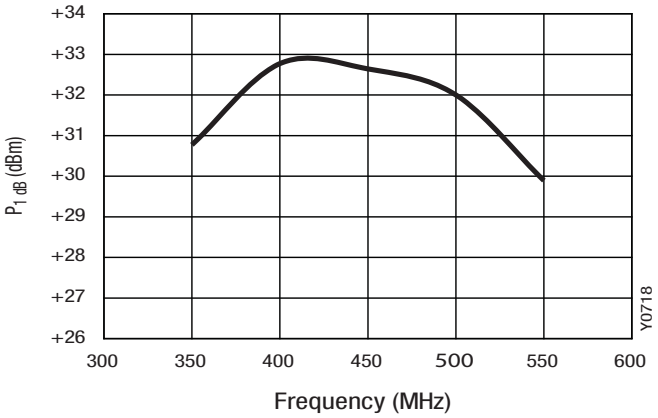


Figure 26. P1dB vs Frequency

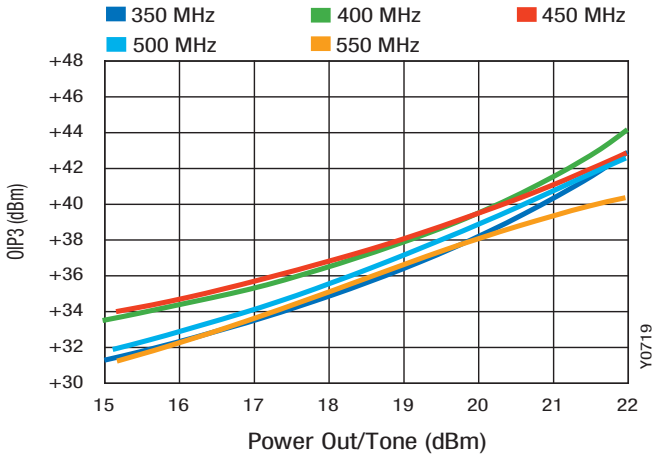


Figure 27. OIP3 vs Output Power/Tone Across Frequency (Tone Spacing = 1 MHz)

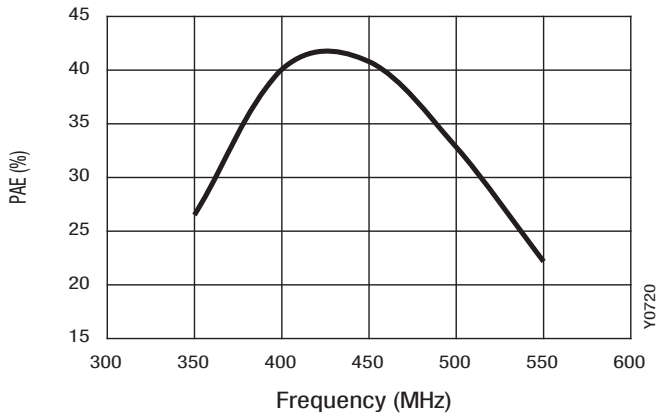


Figure 28. PAE at P1dB vs Frequency

DC/RF Response Time

(V_{CC1}, V_{CC2}, V_{REF} = 3.6 V, V_{CNT} = 0/3.6 V, T_A = 25 °C unless otherwise specified)

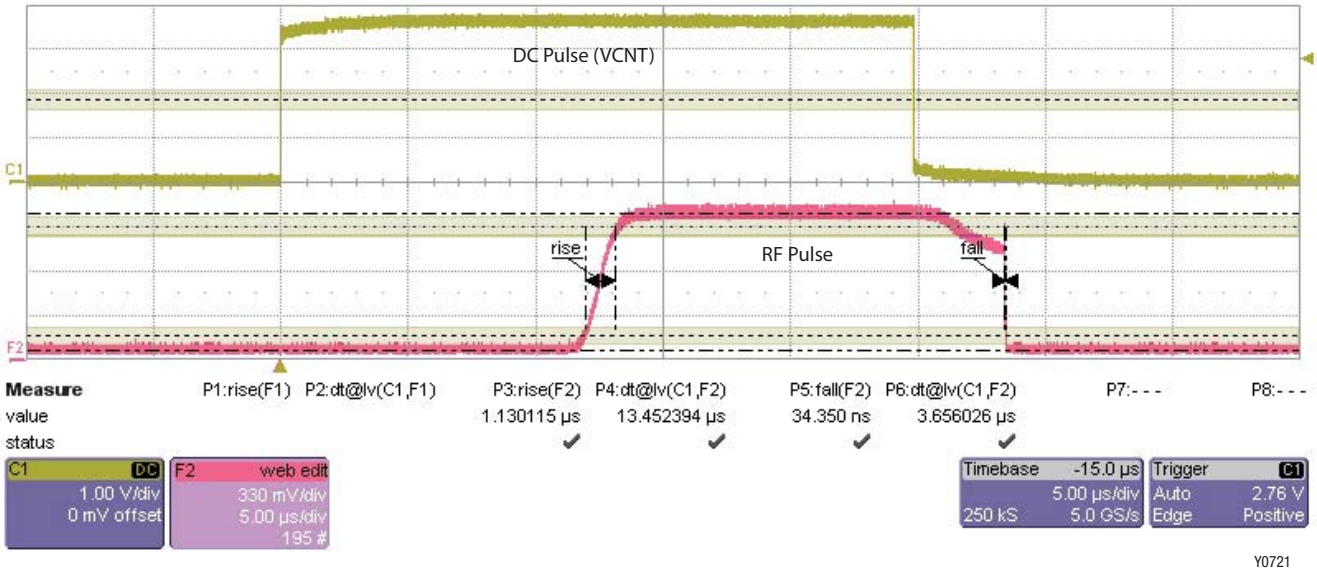


Figure 29. SKY65116 Rise/Fall Times

Table 5. SKY65116 Rise/Fall Times (Note 1)

Pulse	Percent	Label	Rise/Fall	Time
RF-RF	10-90	P3	Rise	1.13 µs
DC-RF	50-90	P4	Rise	13.45 µs
RF-RF	90-10	P5	Fall	0.034 µs
DC-RF	50-10	P6	Fall	3.66 µs

Note 1: 10 µF capacitor, C2 and 0.01 µF capacitor, C5 removed for rise-fall time measurements. Their purpose is to filter DC noise < 200 MHz due to long bias leads to power supply. No noise observed with the removal of C2 and C5.

Theory of Operation

The SKY65116 is comprised of two amplifier stages, and is internally matched for optimum linearity and efficiency. The matching circuits for the input stage, inter-stage, and output stage are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages providing for excellent gain tracking over temperature and voltage variations. The module operates with all positive DC voltages while maintaining high efficiency and good linearity. The nominal operating voltage is 3.6 V for maximum power, but can be operated at slightly lower voltages for other mobile applications.

The input and output stages are independently supplied using the V_{CC1} and V_{CC2} supply lines, pins 4 and 10, respectively. The bias reference voltage is supplied using a common V_{REF} (pin 12) line.

The module includes a silicon CMOS controller circuit to provide an amplifier On/Off operation. V_{CNT} (pin 11) is the PA on/off control voltage to the CMOS controller for stages 1 and 2. 0 V = Off, 3.6 V = On. Nominal "On" operating range is between 2.7 to 3.6 V_{DC}. V_{CNT} set to 0 V_{DC} will force the amplifier into off mode, drawing only microamperes of current.

Application Circuit Notes

Center Ground. It is extremely important that the device paddle be sufficiently grounded for both thermal and stability reasons. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

Ground (Pins 1, 3, 5, 6, 7, 9). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout will allow. Multiple small vias are also acceptable and will work well under the device if solder migration is an issue.

RF_IN (Pin 2). Amplifier RF Input Pin. Z_O = 50 W. The module includes an onboard internal DC blocking capacitor. All impedance matching is provided internal to the module.

V_{CC1} (Pin 4). Supply voltage for the first stage collector bias (typically 3.6 V). Bypassing of V_{CC1} is accomplished with C7 and C8 and should be placed in the approximate location shown on the evaluation board, but placement is not critical.

RF_OUT(Pin 8). Amplifier RF Output Pin. Z_O = 50 W. The module includes an onboard internal DC blocking capacitor. All impedance matching is provided internal to the module.

V_{CC2} (Pin 10). Supply voltage for the output (final) stage collector bias (typically 3.6 V). Bypassing of V_{CC2} is accomplished with C1 and C4 and should be placed in the approximate location shown on the evaluation board, but placement is not critical.

V_{CNT}(Pin 11). V_{CNT} is the PA on/off control voltage to the silicon CMOS controller for stages 1 and 2. 0 V = Off, 3.6 V = On. Nominal "On" operating range is between 2.7 to 3.6 V_{DC}. V_{CNT} set to 0 V_{DC} will force the amplifier into standby mode.

V_{REF} (Pin 12). Bias reference voltage for amplifier stages 1 and 2. V_{REF} should be operated over the same voltage range as V_{CC}, with a nominal voltage of 3.6 V.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY65116 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, Solder Reflow Information, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Evaluation Board Description

Skyworks SKY65116 Evaluation Board is used to test the performance of the SKY65116 PA. The Evaluation Board schematic diagram is shown in Figure 30. The schematic shows the basic design of the board for the 390 to 500 MHz range. An assembly drawing for the Evaluation Board is shown in Figure 31 and the layer detail is provided in Figures 32 and 33.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration.

1. Paths to ground should be made as short as possible.
2. The ground pad of the SKY65116 PA has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the amplifier. As such, design the connection to the ground pad to dissipate the maximum wattage produced to the circuit board. Multiple vias to the grounding layer are required.
3. Two external output bypass capacitors (0.01 μF and 10 μF) are required on the VCC1 (pin 4) supply input. The same two capacitors are also required on the VCC2 (pin 10) supply input and on the VREF input (pin 12). Each of these capacitors should be placed in parallel between the supply line and ground. See Figure 30 for a detailed diagram.
4. VCC1 (pin 4) and VCC2 (pin 10) may be connected together at the supply.

NOTE: *Junction temperature (T_J) of the device increases with a poor connection to the ground pad and ground. This reduces the life of the device.*

Evaluation Board Test Procedure

Use the following procedure to set up the SKY65116 Evaluation Board for testing:

1. Connect a +3.6 V supply to VCC1 and VCC2, and +3.6 V supply to VREF and VCNT. If available, enable the current limiting function of the VCC power supply to 1.5 A.
2. Connect a signal generator to the RF signal input port. Set it to the desired RF frequency at a power level of 2 dBm or less to the Evaluation Board but do NOT enable the RF signal.
3. Connect a spectrum analyzer to the RF signal output port.
4. Enable the power supply.
5. Enable the RF signal.
6. Take measurements.

NOTE: *It is important that the V_{CC1} and V_{CC2} voltage source be adjusted such that 3.6 V is measured at the board. The high collector currents will drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.*

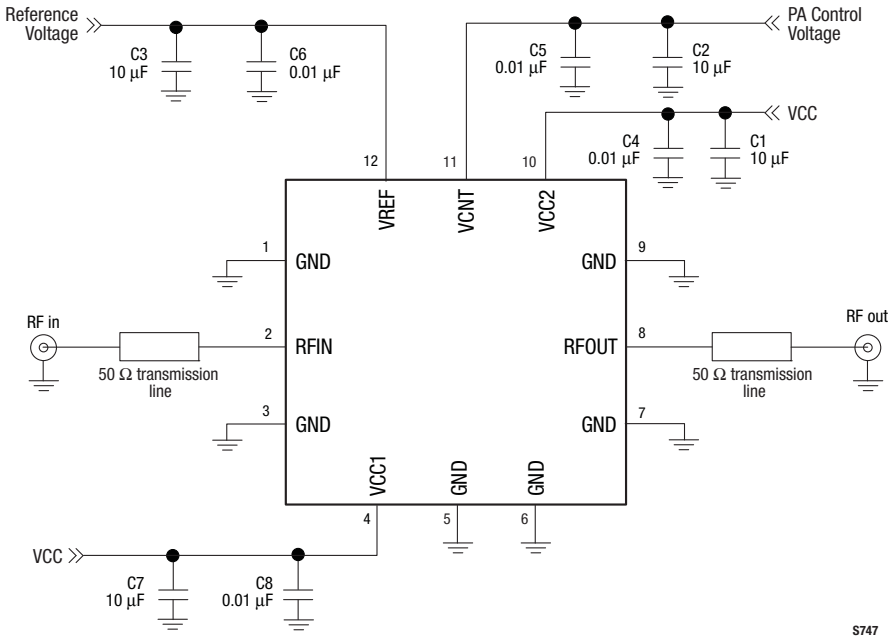


Figure 30. SKY65116 Evaluation Board Schematic

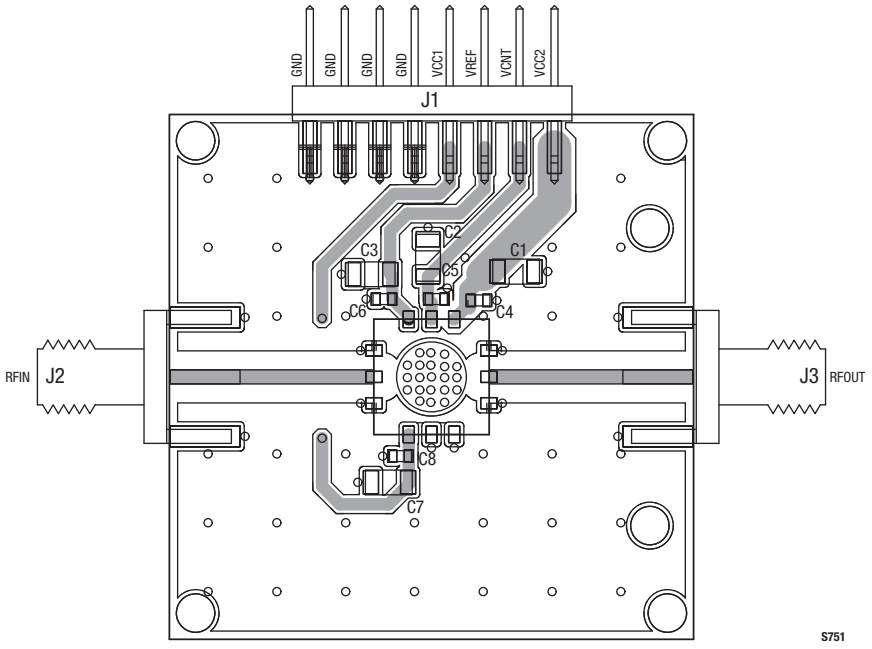
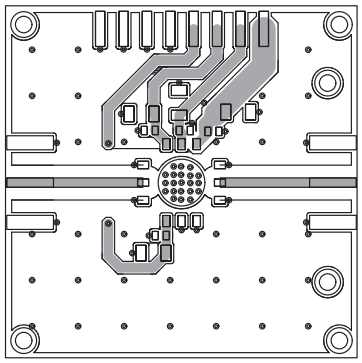
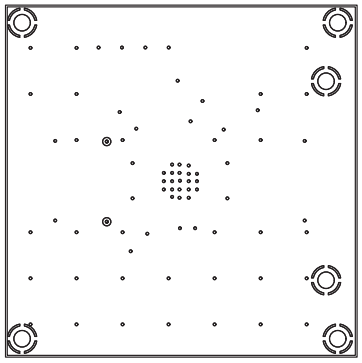


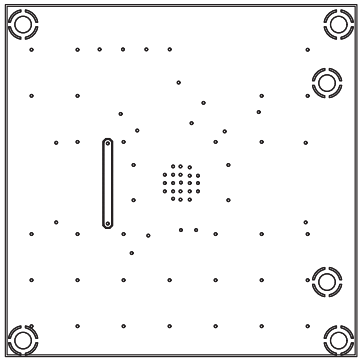
Figure 31. Evaluation Board Assembly Diagram



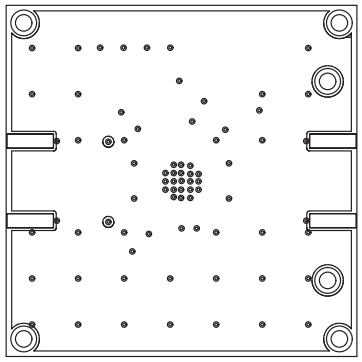
Layer 1: Top -- Metal



Layer 2: Ground



Layer 3: Ground



Layer 4: Solid Ground Plane

S752

Figure 32. Evaluation Board Layer Detail

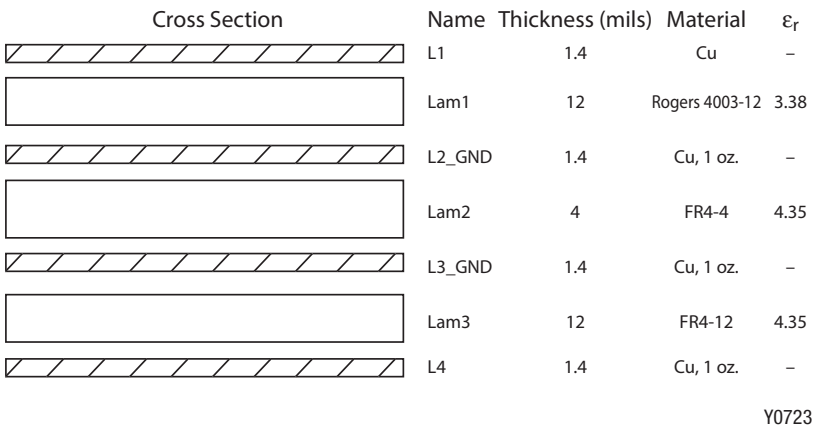
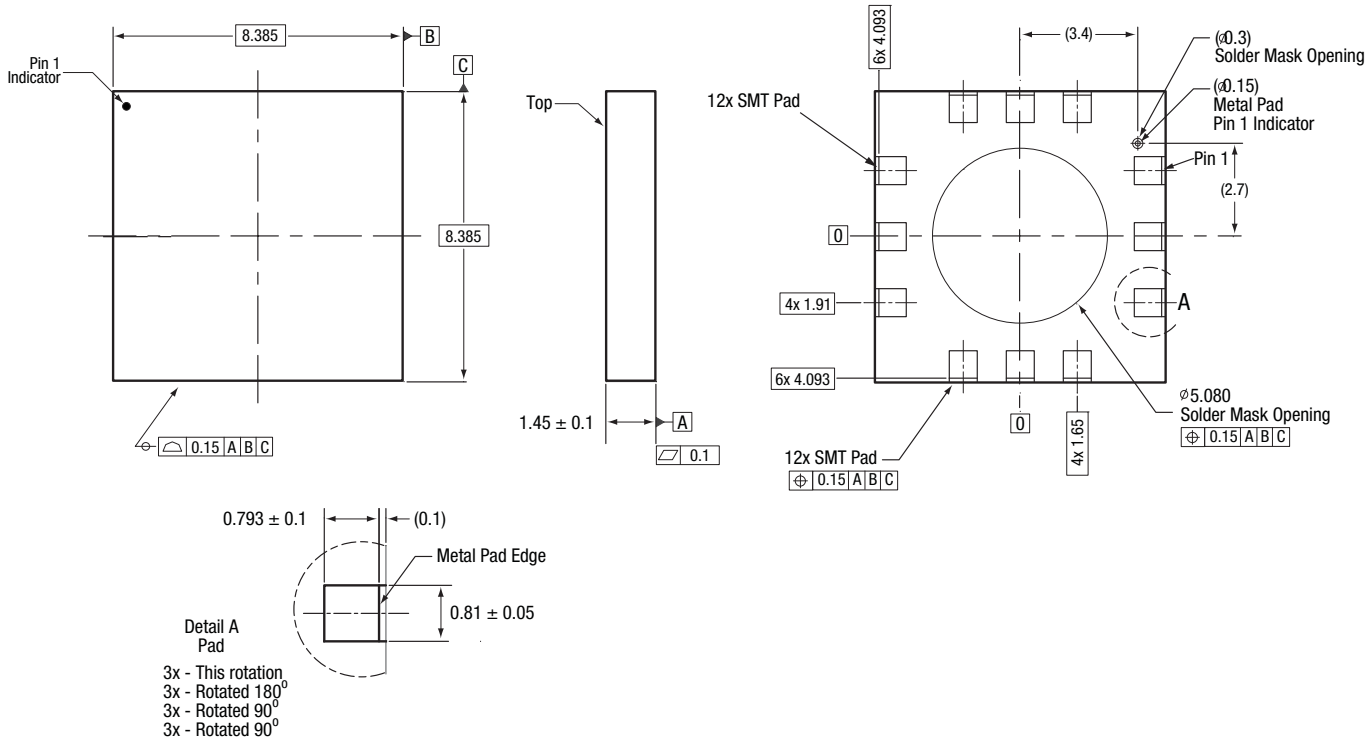


Figure 33. Evaluation Board Layer Detail – Physical Characteristics

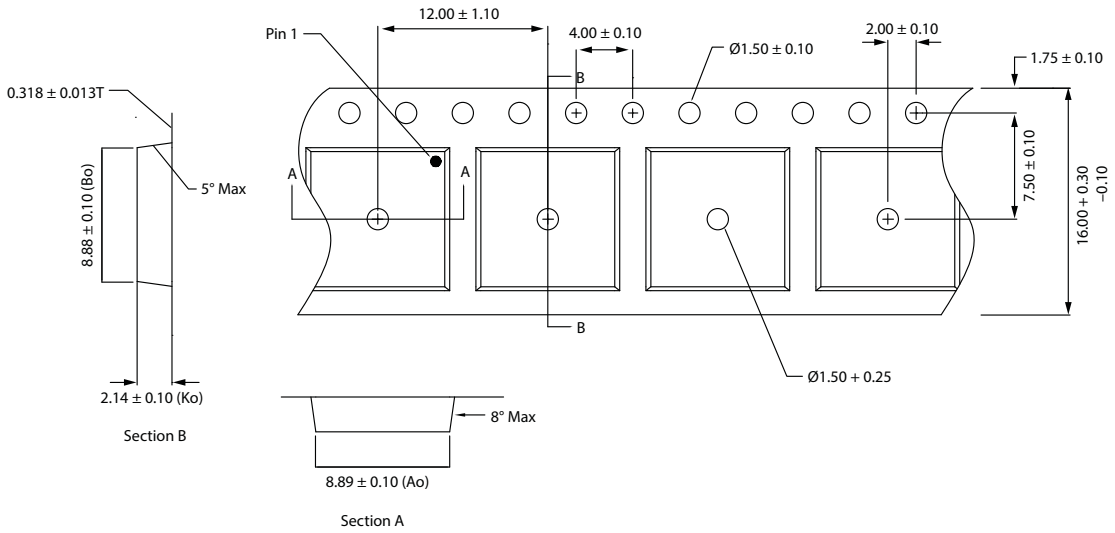


Notes:

Y0724

1. Dimensions and tolerances in accordance with ASME Y14.5M–1994.
2. All measurements are in millimeters.
3. Pad definitions per details on drawing.

Figure 34. SKY65116 12-Pin MCM Package Dimensions



Notes:

1. Carrier tape material: black conductive polycarbonate or polystyrene.
2. Cover tape: transparent conductive pressure sensitive adhesive (PSA) material, 13.3 mm width.
3. ESD-surface resistivity shall be < / =1 X 10⁸ ohms/square per EIA, JEDEC TNR specification.
4. All dimensions are in millimeters

Y0725

Figure 35. SKY65116 12-Pin MCM Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
SKY65116 390-500 MHz Linear Power Amplifier	SKY65116-21	TW14-D621

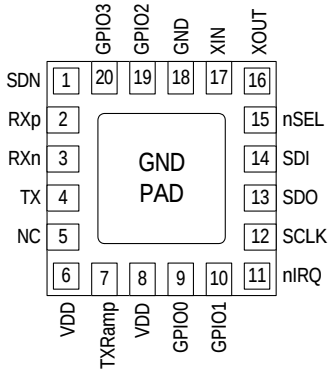
Si4463/61/60-C

HIGH-PERFORMANCE, LOW-CURRENT TRANSCEIVER

Features

- Frequency range = 142–1050 MHz
- Receive sensitivity = –129 dBm
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK
  - OOK
- Max output power
  - +20 dBm (Si4463)
  - +16 dBm (Si4461)
  - +13 dBm (Si4460)
- PA support for +27 or +30 dBm
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm (Si4460)
- Ultra low current powerdown modes
  - 30 nA shutdown, 40 nA standby
- Preamble sense mode
  - 6 mA average RX current at 1.2 kbps
  - 10 µA average RX current at 50 kbps and 1 sec sleep interval
- Fast preamble detection
  - 1 byte preamble detection
- Data rate = 100 bps to 1 Mbps
- Fast wake and hop times
- Power supply = 1.8 to 3.8 V
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
  - 129 bytes dedicated Tx or Rx
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- Low BOM
- Low battery detector
- Temperature sensor
- 20-Pin QFN package
- IEEE 802.15.4g and WMBus compliant
- Suitable for FCC Part 90 Mask D, FCC part 15.247, 15,231, 15,249, ARIB T-108, T-96, T-67, RCR STD-30, China regulatory
- ETSI Category I Operation EN300 220

Pin Assignments



Patents pending

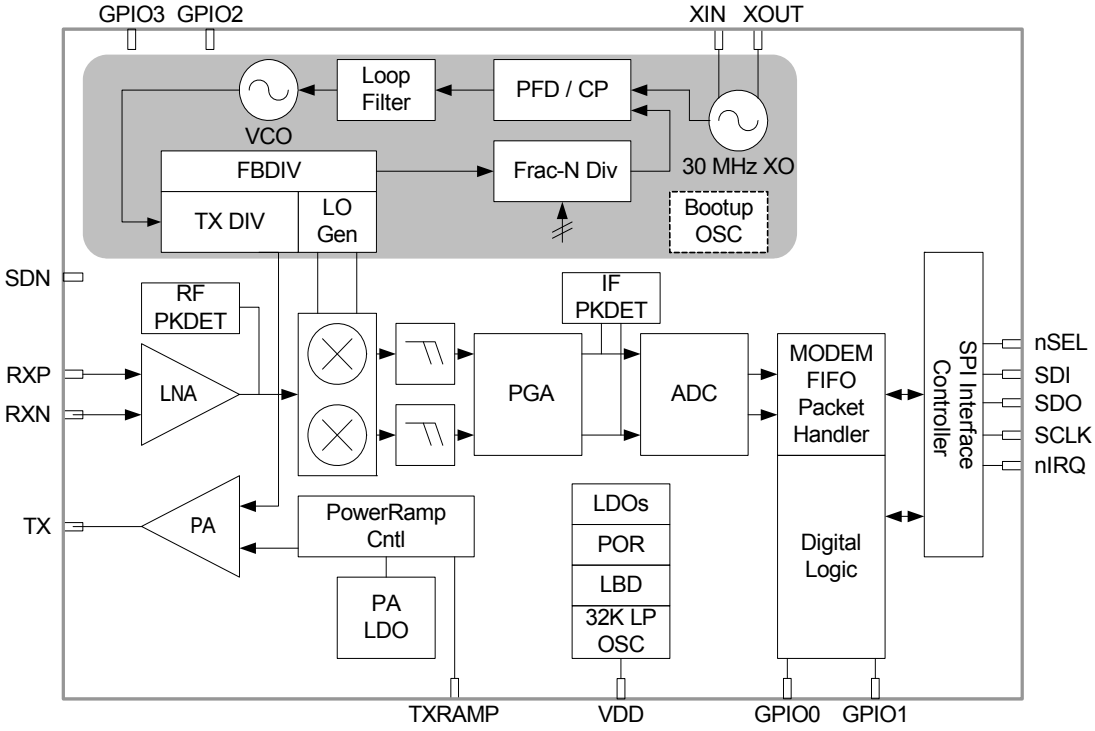
Applications

- Smart metering (802.15.4g and WMBus)
- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Electronic shelf labels

Description

Silicon Laboratories' Si446x devices are high-performance, low-current transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. The radios are part of the EZRadioPRO® family, which includes a complete line of transmitters, receivers, and transceivers covering a wide range of applications. All parts offer outstanding sensitivity of –129 dBm while achieving extremely low active and standby current consumption. The Si4463/61/60 offers frequency coverage in all major bands. The Si446x includes optimal phase noise, blocking, and selectivity performance for narrow band and wireless MBus licensed band applications, such as FCC Part90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The Si4463 offers exceptional output power of up to +20 dBm with outstanding TX efficiency. The high output power and sensitivity results in an industry-leading link budget of 146 dB allowing extended ranges and highly robust communication links. The Si4460 active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times ensure extended battery life in the most demanding applications. The Si4463 can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, wireless MBus, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be configured via the Wireless Development Suite (WDS) available on the Silicon Labs website.

Functional Block Diagram



Product	Freq. Range	Max Output Power	TX Current at Max Power and 868 MHz	Narrow Band Support	IEEE 802.15.4g PHY
Si4463	Major bands 142-1050 MHz	+20 dBm	85 mA	✓	✓
Si4461	Major bands 142-1050 MHz	+16 dBm	43 mA	✓	✓
Si4460	Major bands 142-1050 MHz	+13 dBm	24 mA	✓	✓

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.8	3.3	3.8	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	1300	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF	—	40	2900	nA
	$I_{SleepRC}$	RC Oscillator/WUT ON and all register values maintained, and all other blocks OFF	—	740	3800	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal	—	1.7	—	µA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
Preamble Sense Mode Current	I_{psm}	Duty cycling during preamble search, 1.2 kbps, 4 byte preamble	—	6	—	mA
	I_{psm}	Fixed 1 s wakeup interval, 50 kbps, 5 byte preamble	—	10	—	µA
TUNE Mode Current	I_{Tune_RX}	RX Tune, High Performance Mode	—	7.6	—	mA
	I_{Tune_TX}	TX Tune, High Performance Mode	—	7.8	—	mA
RX Mode Current	I_{RXH}	High Performance Mode (measured at 915 MHz and 40 kbps data rate)	—	13.7	22	mA
	I_{RXL}	Low Power Mode (measured at 315 MHz and 40 kbps data rate)	—	10.9	—	mA
TX Mode Current (Si4463)	I_{TX_+20}	+20 dBm output power, Class-E match, 915 MHz, 3.3 V	—	88	108	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	68.5	80	mA
		+13 dBm output power, Class-E match, 915 MHz, 3.3 V	—	44.5	60	mA
TX Mode Current (Si4460)	I_{TX_+10}	+10 dBm output power, Class-E match, 915/868 MHz, 3.3 V[2]	—	19.7	—	mA
	I_{TX_+10}	+10 dBm output power, Class-E match, 169 MHz, 3.3 V[2]	—	18	—	mA
	I_{TX_+13}	+13 dBm output power, Class-E match, 915/868 MHz, 3.3 V	—	24	—	mA
TX Mode Current (Si4461)	I_{TX_+16}	+16 dBm output power, class-E match, 868 MHz, 3.3 V	—	43	55	mA
	I_{TX_+13}	+13 dBm output power, switched-current match, 868 MHz, 3.3 V	—	33.5	40	mA

Notes:
1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. Measured on direct-tie RF evaluation board.

Table 2. Synthesizer AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Resolution	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	µs
Phase Noise	$L\phi(f_M)$	ΔF = 10 kHz, 169 MHz, High Perf Mode	—	–117	–108	dBc/Hz
		ΔF = 100 kHz, 169 MHz, High Perf Mode	—	–120	–115	dBc/Hz
		ΔF = 1 MHz, 169 MHz, High Perf Mode	—	–138	–135	dBc/Hz
		ΔF = 10 MHz, 169 MHz, High Perf Mode	—	–148	–143	dBc/Hz
		ΔF = 10 kHz, 915 MHz, High Perf Mode	—	–102	–94	dBc/Hz
		ΔF = 100 kHz, 915 MHz, High Perf Mode	—	–105	–97	dBc/Hz
		ΔF = 1 MHz, 915 MHz, High Perf Mode	—	–125	–122	dBc/Hz
		ΔF = 10 MHz, 915 MHz, High Perf Mode	—	–138	–135	dBc/Hz

Note: All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.

Table 3. Receiver AC Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
RX Sensitivity 169 MHz[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)	—	–129	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–110	–108	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–106	–104	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–98	–96	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–89	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–110	–107	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–103	–100	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–97	–93	dBm

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 3. Receiver AC Electrical Characteristics[1,2] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity 915/868 MHz[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)	—	–127	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109	–107	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–104	–102	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–97	–92	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–109	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–88	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–108	–104	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–101	–97	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–96	–91	dBm
RX Channel Bandwidth	BW		1.1	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from –110 dBm to –90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity, 169 MHz[3]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz, channel spacing = 12.5 kHz	—	–69	–59	dB
±1-Ch Offset Selectivity, 450 MHz[3]	$C/I_{1\text{-}CH}$		—	–60	–50	dB
±1-Ch Offset Selectivity, 868 / 915 MHz[3]	$C/I_{1\text{-}CH}$		—	–55	–45	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER = 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps, ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz	—	–79	–68	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	–86	–75	dB

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 3. Receiver AC Electrical Characteristics[1,2] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image Rejection (IF = 468.75 kHz)	Im_{REJ}	No image rejection calibration. Rejection at the image frequency. RF = 460 MHz	30	40	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. RF = 460 MHz	40	55	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 915 MHz	30	45	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. RF = 915 MHz	40	52	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 169 MHz	35	45	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. RF = 169 MHz	45	60	—	dB

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 4. Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
(G)FSK Data Rate	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{420}	350–420 MHz	—	600	—	kHz
	Δf_{350}	283–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Resolution	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Output Power Range (Si4463)	P_{TX63}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency	–20	—	+20	dBm
Output Power Range (Si4461)	P_{TX61}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency	–40	—	+16	dBm
Output Power Range (Si4460)	P_{TX60}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency. Efficiency can be traded off for higher Tx output power up to +13 dBm	–20	—	+12.5	dBm

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 4. Transmitter AC Electrical Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Power Variation (Si4463)		At 20 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	19	20	21	dBm
Output Power Variation (Si4460)		At 10 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	9	10	11	dBm
Output Power Variation (Si4463)		At 20 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	18.5	20	21	dBm
Output Power Variation (Si4460)		At 10 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	9.5	10	10.5	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power using CLE match within 6 dB of max power	—	0.25	0.4	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2.3	3	dB
TX RF Output Level Variation vs. Frequency	ΔP_{RF_FREQ}	Measured across 902–928 MHz	—	0.6	1.7	dB
Transmit Modulation Filtering	BT	Gaussian Filtering Bandwith Time Product	—	0.5	—	

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 5. Auxiliary Block Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Sensor Sensitivity	TS_S		—	4.5	—	ADC Codes/ °C
Low Battery Detector Resolution	LBD_{RES}		—	50	—	mV
Microcontroller Clock Output Frequency Range[2]	F_{MC}	Configurable to Fxtal or Fxtal divided by 2, 3, 7.5, 10, 15, or 30 where Fxtal is the reference XTAL frequency. In addition, 32.768 kHz is also supported.	32.768K	—	Fxtal	Hz
Temperature Sensor Conversion	$TEMP_{CT}$	Programmable setting	—	3	—	ms
XTAL Range[3]	$XTAL_{Range}$		25	—	32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Start-up time will vary with XTAL type and board layout.	—	300	—	µs
30 MHz XTAL Cap Resolution	$30M_{RES}$		—	70	—	fF
32 kHz XTAL Start-Up Time	t_{32k}		—	2	—	sec
32 kHz Accuracy using Internal RC Oscillator	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	—	6	ms

Notes:
1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –45 to +85 °C unless otherwise stated. All typical values apply at Vdd=3.3V and 25C unless otherwise stated.
2. Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested by bench characterization.
3. XTAL Range tested in production using an external clock source (similar to using a TCXO).

Table 6. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ, SDN)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time[2,3]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2.3	—	ns
Fall Time[3,4]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–1	—	1	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	4	µA
Drive Strength for Output Low Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	1.13	—	mA
Drive Strength for Output High Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.96	—	mA
Drive Strength for Output High Level for GPIO0	I_{OmaxLL}	DRV[1:0] = LL[3]	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	1.70	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD} x 0.2	V

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. 6.7 ns is typical for GPIO0 rise time.
3. Assuming VDD = 3.3 V, drive strength is specified at Voh (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.
4. 2.4 ns is typical for GPIO0 fall time.

Table 7. Thermal Characteristics

Parameter	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Thermal Impedance Junction to Ambient*	θ_{JA}	25	°C/w
Junction Temperature Maximum Value*	T_j	+105	°C
Storage Temperature Range	T_{STG}	–55 to +150	°C
***Note:** θ_{JA} and T_j are based on RF evaluation board measurements.			

Table 8. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.8	V
Instantaneous $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +8.0	V
Sustained $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +6.5	V
Voltage on Analog Inputs	–0.7, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.		

2. Functional Description

The Si446x devices are high-performance, low-current, wireless ISM transceivers that cover the sub-GHz bands. The wide operating voltage range of 1.8–3.8 V and low current consumption make the Si446x an ideal solution for battery powered applications. The Si446x operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2/4-level FSK/GFSK or OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 100 bps to 1 Mbps. The Si4463/61/60 operate in the frequency bands of 142–175, 283–350, 350–525, and 850–1050 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The Si4463 contains a power amplifier (PA) that supports output power up to +20 dBm with very high efficiency, consuming only 70 mA at 169 MHz and 85 mA at 915 MHz. The integrated +20 dBm power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. Competing solutions require large and expensive external PAs to achieve comparable performance. The Si4461 supplies output power up to +16 dBm. The Si4460 is designed to support single coin cell operation with current consumption below 18 mA for +10 dBm output power. Two match topologies are available for the Si4461 and Si4460, class-E and switched-current. Class-E matching provides optimal current consumption, while switched-current matching demonstrates the best performance over varying battery voltage and temperature with slightly higher current consumption. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The Si446x family supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. Antenna diversity is completely integrated into the Si446x and can improve the system link budget by 8–10 dB, resulting in substantial range increases under adverse environmental conditions. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure. Additional system features, such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, and preamble detection, reduce overall current consumption and allows for the use of lower-cost system MCUs. An integrated temperature sensor, power-on-reset (POR), and GPIOs further reduce overall system cost and size. The Si446x is designed to work with an MCU, crystal, and a few passive components to create a very low-cost system.

The application shown in Figure 1 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most applications with output power less than 17 dBm will use this configuration. Figure 2 demonstrates an application for +20 dBm using an external T/R-switch.

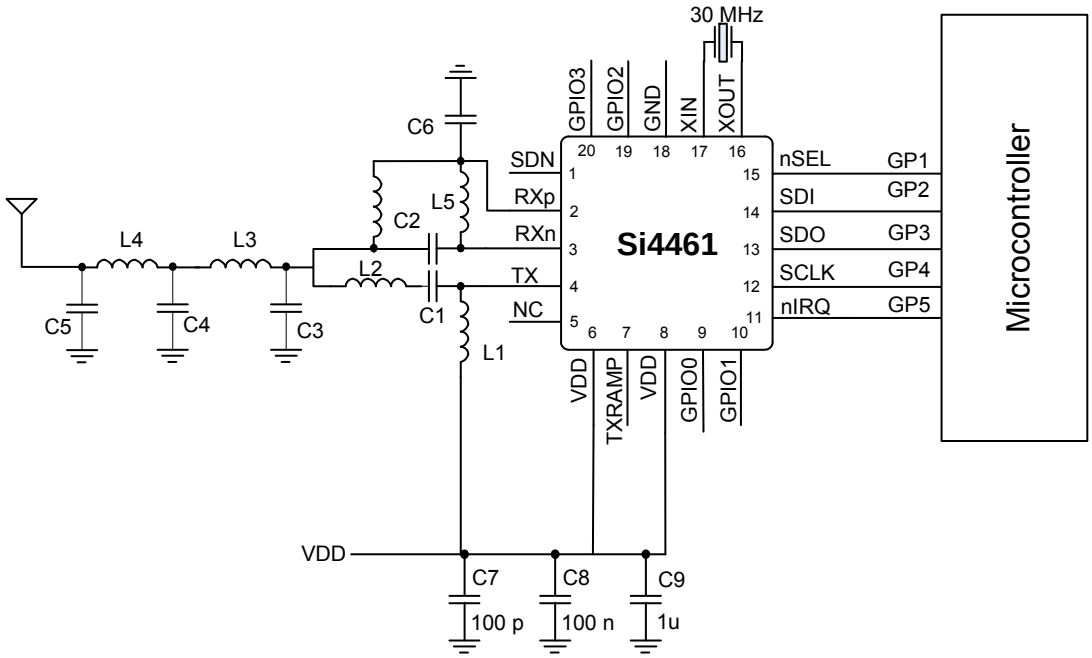


Figure 1. Si4461 Direct-Tie Application Example

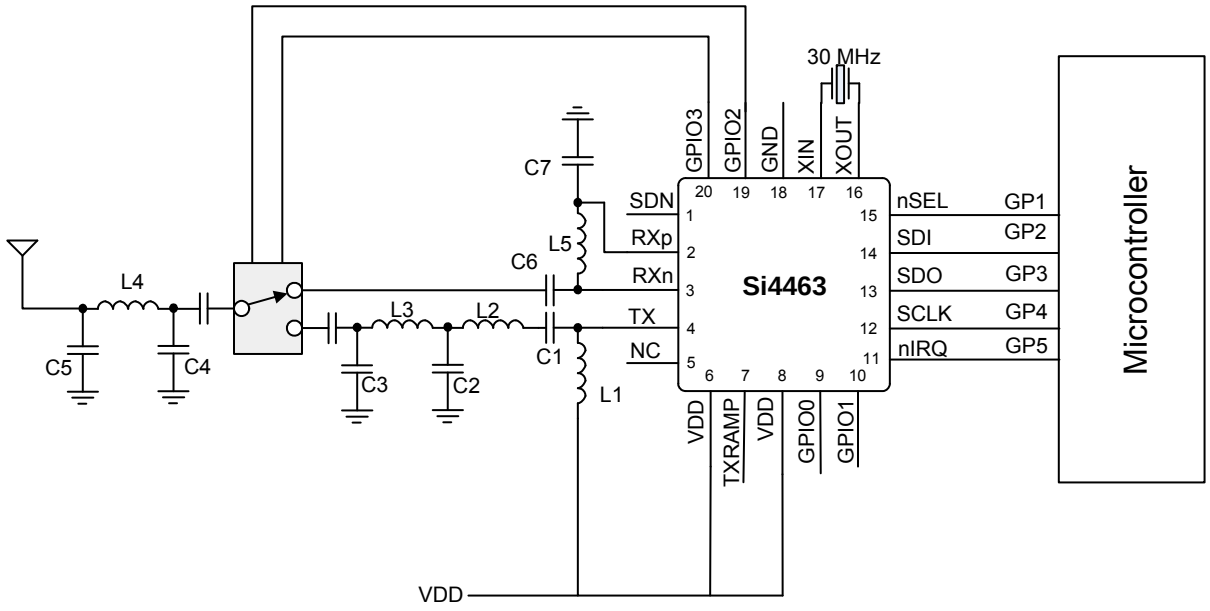


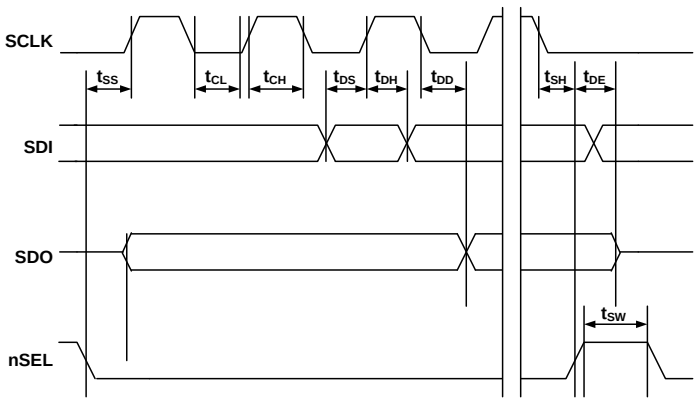
Figure 2. Si4463 Single Antenna with RF Switch Example

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si446x communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are demonstrated in Table 9. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 3 demonstrates an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the firmware commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Max (ns)	Diagram
t_{CH}	Clock high time	40		
t_{CL}	Clock low time	40		
t_{DS}	Data setup time	20		
t_{DH}	Data hold time	20		
t_{DD}	Output data delay time		43	
t_{DE}	Output disable time		45	
t_{SS}	Select setup time	20		
t_{SH}	Select hold time	50		
t_{SW}	Select high period	80		

***Note:** CL = 10 pF; VDD = 1.8 V; SDO Drive strength setting = 10.

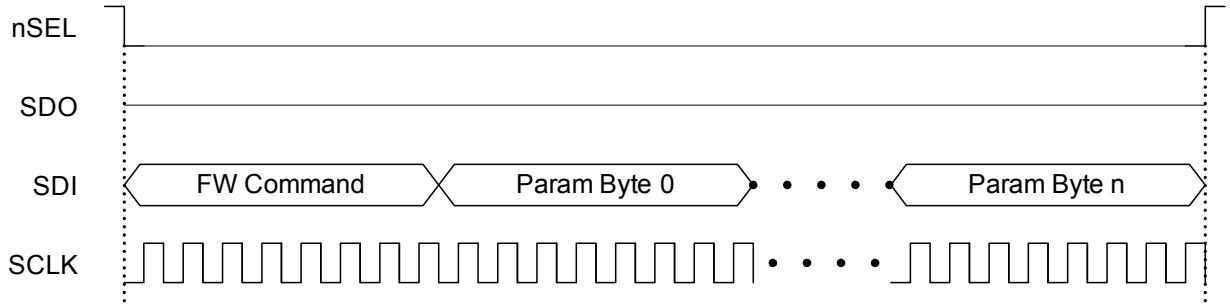
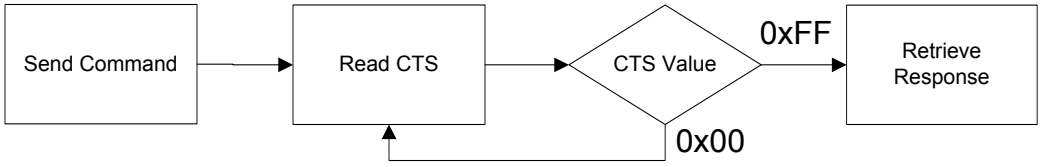


Figure 3. SPI Write Command

The Si446x contains an internal MCU which controls all the internal functions of the radio. For SPI read commands a typical MCU flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 4 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 5 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

Firmware Flow



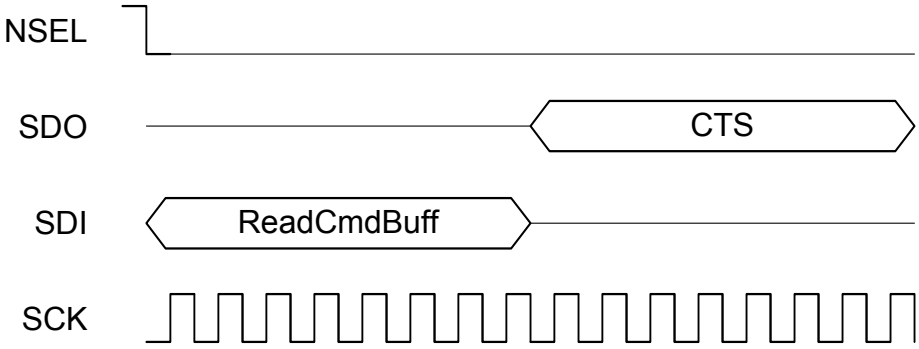


Figure 4. SPI Read Command—Check CTS Value

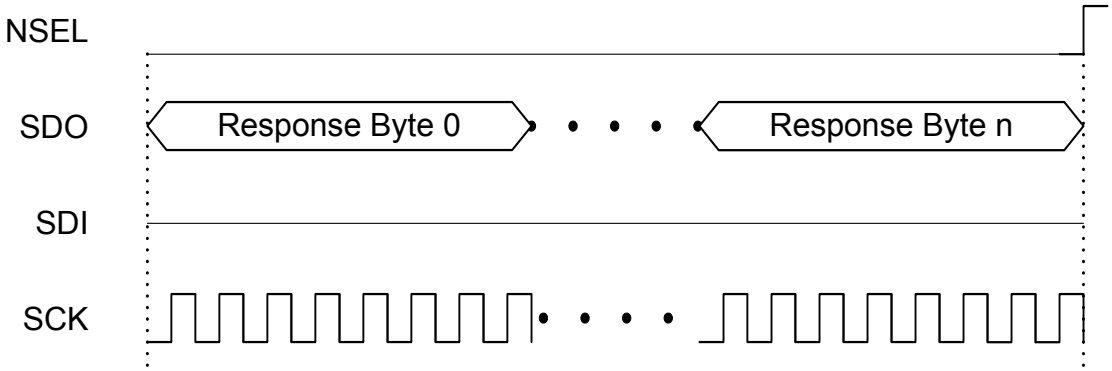


Figure 5. SPI Read Command—Clock Out Read Data

3.2. Fast Response Registers

The fast response registers are registers that can be read immediately without the requirement to monitor and check CTS. There are four fast response registers that can be programmed for a specific function. The fast response registers can be read through API commands, 0x50 for Fast Response A, 0x51 for Fast Response B, 0x53 for Fast Response C, and 0x57 for Fast Response D. The fast response registers can be configured by the “FRR_CTL_X_MODE” properties.

The fast response registers may be read in a burst fashion. After the initial 16 clock cycles, each additional eight clock cycles will clock out the contents of the next fast response register in a circular fashion. The value of the FRRs will not be updated unless NSEL is toggled.

3.3. Operating Modes and Timing

The primary states of the Si446x are shown in Figure 6. The shutdown state completely shuts down the radio to minimize current consumption. Standby/Sleep, SPI Active, Ready, TX Tune, and RX tune are available to optimize the current consumption and response time to RX/TX for a given application. API commands START_RX, START_TX, and CHANGE_STATE control the operating state with the exception of shutdown which is controlled by SDN, pin 1. Table 10 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode. The times in Table 9 are measured from the rising edge of nSEL until the chip is in the desired state. Note that these times are indicative of state transition timing but are not guaranteed and should only be used as a reference data point. An automatic sequencer will put the chip into RX or TX from any state. It is not necessary to manually step through the states. To simplify the diagram it is not shown but any of the lower power states can be returned to automatically after RX or TX.

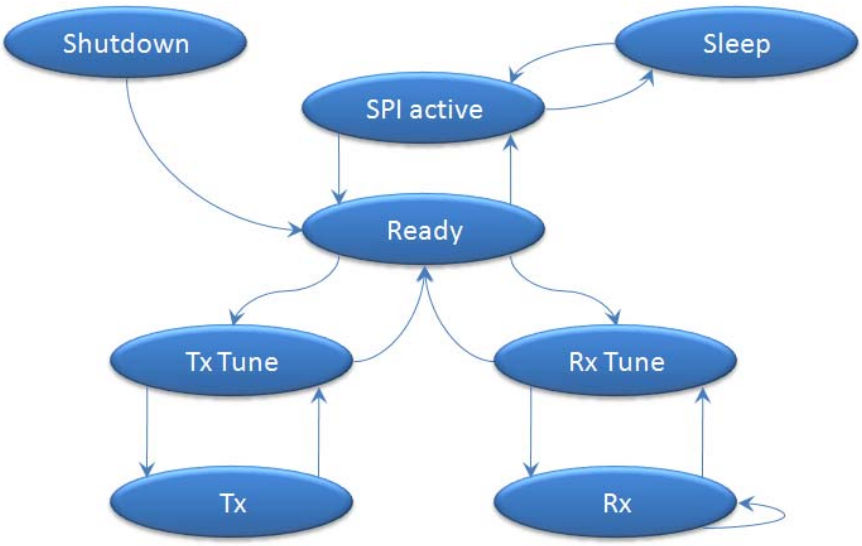


Figure 6. State Machine Diagram

Table 10. Operating State Response Time and Current Consumption

State/Mode	Response Time to		Current in State /Mode
	TX	RX	
Shutdown State	15 ms	15 ms	30 nA
Standby State	440 µs	440 µs	40 nA
Sleep State	440 µs	440 µs	740 nA
SPI Active State	340 µs	340 µs	1.35 mA
Ready State	100 µs	100 µs	1.8 mA
TX Tune State	58 µs	—	7.8 mA
RX Tune State	—	60 µs	7.6 mA
TX State	—	100 µs	18 mA @ +10 dBm
RX State	100 µs	75 µs	10.9 or 13.7 mA
Note: TX→RX and RX→TX state transition timing can be reduced to 70 µs if using Zero-IF mode.			

Figure 7 shows the POR timing and voltage requirements. The power consumption (battery life) depends on the duty cycle of the application or how often the part is in either Rx or Tx state. In most applications the utilization of the standby state will be most advantageous for battery life but for very low duty cycle applications shutdown will have an advantage. For the fastest timing the next state can be selected in the START_RX or START_TX API commands to minimize SPI transactions and internal MCU processing.

3.3.1. Power on Reset (POR)

A Power On Reset (POR) sequence is used to boot the device up from a fully off or shutdown state. To execute this process, VDD must ramp within 1ms and must remain applied to the device for at least 10 ms. If VDD is removed, then it must stay below 0.15 V for at least 10 ms before being applied again. See Figure 7 and Table 11 for details.

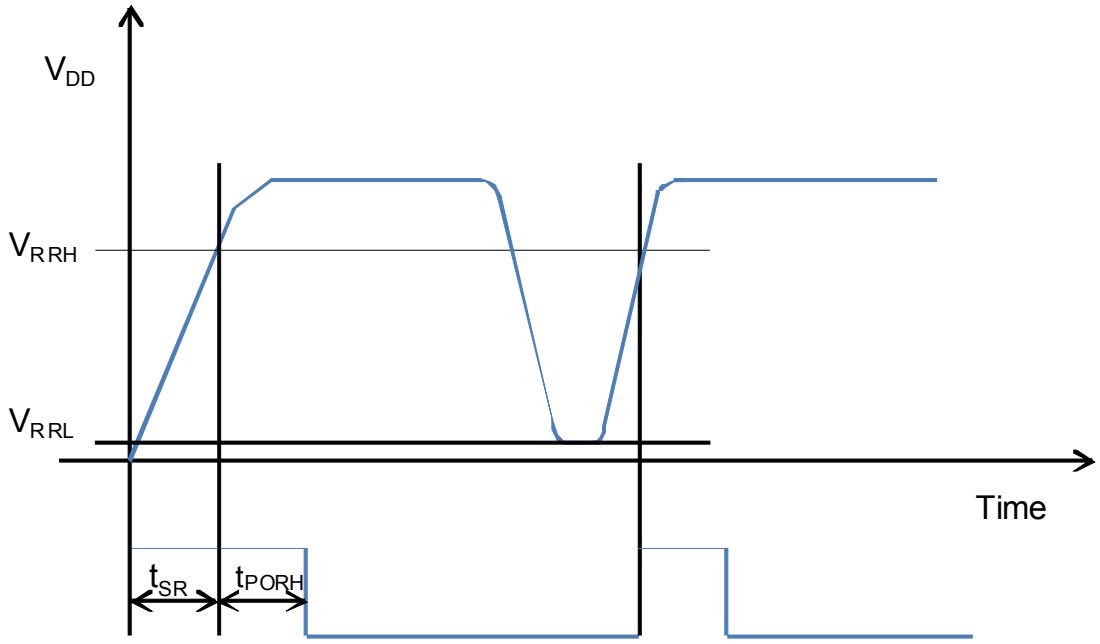


Figure 7. POR Timing Diagram

Table 11. POR Timing

Variable	Description	Min	Typ	Max	Units
t_{PORH}	High time for VDD to fully settle POR circuit	10			ms
t_{PORL}	Low time for VDD to enable POR	10			ms
V_{RRH}	Voltage for successful POR	90% x Vdd			V
V_{RRL}	Starting Voltage for successful POR	0		150	mV
t_{SR}	Slew rate of VDD for successful POR			1	ms

3.3.2. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 30 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 1) high. The SDN pin should be held low in all states except the shutdown state. In the shutdown state, the contents of the registers are lost and there is no SPI access. When coming out of the shutdown state a power on reset (POR) will be initiated along with the internal calibrations. After the POR the POWER_UP command is required to initialize the radio. The SDN pin needs to be held high for at least 10us before driving low again so that internal capacitors can discharge. Not holding the SDN high for this period of time may cause the POR to be missed and the device to boot up incorrectly. If POR timing and voltage requirements cannot be met, it is highly recommended that SDN be controlled using the host processor rather than tying it to GND on the board.

3.3.3. Standby State

Standby state has the lowest current consumption with the exception of shutdown but has much faster response time to RX or TX mode. In most cases standby should be used as the low power state. In this state the register values are maintained with all other blocks disabled. The SPI is accessible during this mode but any SPI event, including FIFO R/W, will enable an internal boot oscillator and automatically move the part to SPI active state. After an SPI event the host will need to re-command the device back to standby through the “Change State” API command to achieve the 40 nA current consumption. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.4. Sleep State

Sleep state is the same as standby state but the wake-up-timer and a 32 kHz clock source are enabled. The source of the 32 kHz clock can either be an internal 32 kHz RC oscillator which is periodically calibrated or a 32 kHz oscillator using an external XTAL.The SPI is accessible during this mode but an SPI event will enable an internal boot oscillator and automatically move the part to SPI active mode. After an SPI event the host will need to re-command the device back to sleep. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.5. SPI Active State

In SPI active state the SPI and a boot up oscillator are enabled. After SPI transactions during either standby or sleep the device will not automatically return to these states. A “Change State” API command will be required to return to either the standby or sleep modes.

3.3.6. Ready State

Ready state is designed to give a fast transition time to TX or RX state with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time.

3.3.7. TX State

The TX state may be entered from any of the state with the “Start TX” or “Change State” API commands. A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The following sequence of events will occur automatically when going from standby to TX state.

1. Enable internal LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).

3. Enable PLL.
4. Calibrate VCO/PLL.
5. Wait until PLL settles to required transmit frequency (controlled by an internal timer).
6. Activate power amplifier and wait until power ramping is completed (controlled by an internal timer).
7. Transmit packet.

Steps in this sequence may be eliminated depending on which state the chip is configured to prior to commanding to TX. By default, the VCO and PLL are calibrated every time the PLL is enabled. When the START_TX API command is utilized the next state may be defined to ensure optimal timing and turnaround.

Figure 8 shows an example of the commands and timing for the START_TX command. CTS will go high as soon as the sequencer puts the part into TX state. As the sequencer is stepping through the events listed above, CTS will be low and no new commands or property changes are allowed. If the Fast Response (FRR) or nIRQ is used to monitor the current state there will be slight delay caused by the internal hardware from when the event actually occurs to when the transition occurs on the FRR or nIRQ. The time from entering TX state to when the FRR will update is 5 µs and the time to when the nIRQ will transition is 13 µs. If a GPIO is programmed for TX state or used as control for a transmit/receive switch (TR switch) there is no delay.

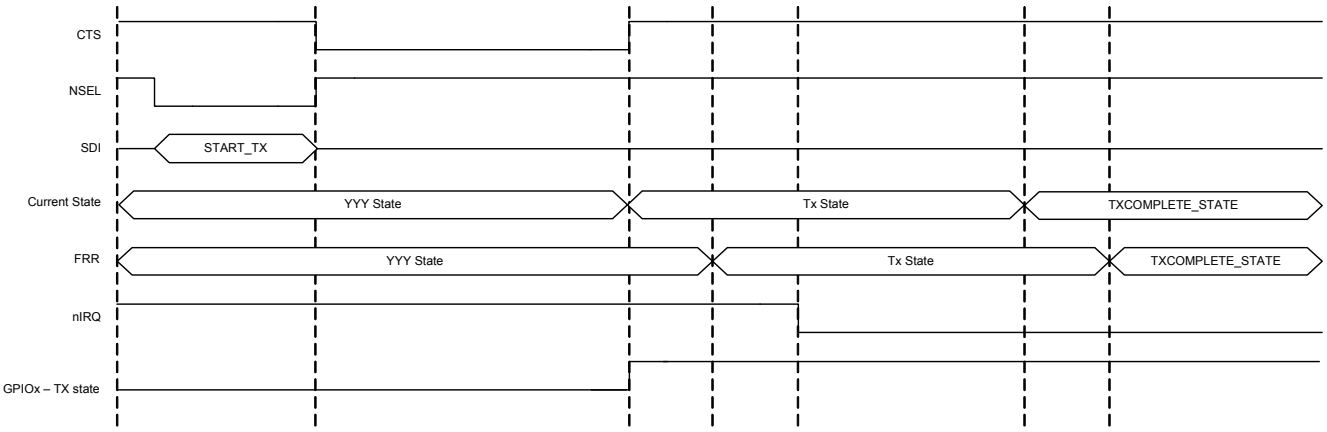


Figure 8. Start_TX Commands and Timing

3.3.8. RX State

The RX state may be entered from any of the other states by using the “Start RX” or “Change State” API command. A built-in sequencer takes care of all the actions required to transition between states. The following sequence of events will occur automatically to get the chip into RX mode when going from standby to RX state:

1. Enable the digital LDO and the analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO
5. Wait until PLL settles to required receive frequency (controlled by an internal timer).
6. Enable receiver circuits: LNA, mixers, and ADC.
7. Enable receive mode in the digital modem.

Depending on the configuration of the radio, all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC. Similar to the TX state, the next state after RX may be defined in the “Start RX” API command. The START_RX commands and timing will be equivalent to the timing shown in Figure 8.

3.4. Application Programming Interface (API)

An application programming interface (API), which the host MCU will communicate with, is embedded inside the device. The API is divided into two sections, commands and properties. The commands are used to control the chip and retrieve its status. The properties are general configurations which will change infrequently. The API descriptions can be found on the Silicon Labs website.

3.5. Interrupts

The Si446x is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Registers. The nIRQ output signal will then be reset until the next change in status is detected.

The interrupts sources are grouped into three groups: packet handler, chip status, and modem. The individual interrupts in these groups can be enabled/disabled in the interrupt property registers. An interrupt must be enabled for it to trigger an event on the nIRQ pin. The interrupt group must be enabled as well as the individual interrupts in API properties described in the API documentation.

Once an interrupt event occurs and the nIRQ pin is low there are two ways to read and clear the interrupts. All of the interrupts may be read and cleared in the “GET_INT_STATUS” API command. By default all interrupts will be cleared once read. If only specific interrupts want to be read in the fastest possible method the individual interrupt groups (Packet Handler, Chip Status, Modem) may be read and cleared by the “GET_MODEM_STATUS”, “GET_PH_STATUS” (packet handler), and “GET_CHIP_STATUS” API commands.

The instantaneous status of a specific function maybe read if the specific interrupt is enabled or disabled. The status results are provided after the interrupts and can be read with the same commands as the interrupts. The status bits will give the current state of the function whether the interrupt is enabled or not.

The fast response registers can also give information about the interrupt groups but reading the fast response registers will not clear the interrupt and reset the nIRQ pin.

3.6. GPIO

Four general purpose IO pins are available to utilize in the application. The GPIO are configured by the GPIO_PIN_CFG command in address 13h. For a complete list of the GPIO options please see the API guide. GPIO pins 0 and 1 should be used for active signals such as data or clock. GPIO pins 2 and 3 have more susceptibility to generating spurious in the synthesizer than pins 0 and 1. The drive strength of the GPIOs can be adjusted with the GEN_CONFIG parameter in the GPIO_PIN_CFG command. By default the drive strength is set to minimum. The default configuration for the GPIOs and the state during SDN is shown below in Table 12.The state of the IO during shutdown is also shown inTable 12. As indicated previously in Table 6, GPIO 0 has lower drive strength than the other GPIOs.

Table 12. GPIOs

Pin	SDN State	POR Default
GPIO0	0	POR
GPIO1	0	CTS
GPIO2	0	POR
GPIO3	0	POR
nIRQ	resistive VDD pull-up	nIRQ
SDO	resistive VDD pull-up	SDO
SDI	High Z	SDI
SCLK	High Z	SCLK
NSEL	High Z	NSEL

4. Modulation and Hardware Configuration Options

The Si446x supports different modulation options and can be used in various configurations to tailor the device to any specific application or legacy system for drop in replacement. The modulation and configuration options are set in API property, MODEM_MOD_TYPE. Refer to the API documentation for details on modem related properties.

4.1. Modulation Types

The Si446x supports five different modulation options: Gaussian frequency shift keying (GFSK), frequency-shift keying (FSK), four-level GFSK (4GFSK), four-level FSK (4FSK), and on-off keying (OOK). Minimum shift keying (MSK) can also be created by using GFSK with the appropriate modulation index (h = 0.5). GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. The modulation type is set by the “MOD_TYPE[2:0]” field in the “MODEM_MOD_TYPE” API property. A continuous-wave (CW) carrier may also be selected for RF evaluation purposes. The modulation source may also be selected to be a pseudo-random source for evaluation purposes.

4.2. Hardware Configuration Options

There are different receive demodulator options to optimize the performance and mutually-exclusive options for how the RX/TX data is transferred from the host MCU to the RF device.

4.2.1. Receive Demodulator Options

There are multiple demodulators integrated into the device to optimize the performance for different applications, modulation formats, and packet structures. The calculator built into WDS will choose the optimal demodulator based on the input criteria.

4.2.1.1. Synchronous Demodulator

The synchronous demodulator's internal frequency error estimator acquires the frequency error based on a 101010 preamble structure. The bit clock recovery circuit locks to the incoming data stream within four transactions of a “10” or “01” bit stream. The synchronous demodulator gives optimal performance for 2- or 4-level (G)FSK modulation that has a modulation index less than 2.

4.2.1.2. Asynchronous Demodulator

The asynchronous demodulator should be used for OOK modulation and for (G)FSK modulation under one or more of the following conditions:

- Modulation index $\geq$ 2
- Non-standard preamble (not 1010101... pattern)

When the modulation index exceeds 2, the asynchronous demodulator has better sensitivity compared to the synchronous demodulator. An internal deglitch circuit provides a glitch-free data output and a data clock signal to simplify the interface to the host. There is no requirement to perform deglitching in the host MCU. The asynchronous demodulator will typically be utilized for legacy systems and will have many performance benefits over devices used in legacy designs. Unlike the Si4432/31 solution for non-standard packet structures, there is no requirement to perform deglitching on the data in the host MCU. Glitch-free data is output from Si446x devices, and a sample clock for the asynchronous data can also be supplied to the host MCU; so, oversampling or bit clock recovery is not required by the host MCU. There are multiple detector options in the asynchronous demodulator block, which will be selected based upon the options entered into the WDS calculator. The asynchronous demodulator's internal frequency error estimator is able to acquire the frequency error based on any preamble structure.

4.2.2. RX/TX Data Interface With MCU

There are two different options for transferring the data from the RF device to the host MCU. FIFO mode uses the SPI interface to transfer the data, while direct mode transfers the data in real time over a GPIO pin.

4.2.2.1. FIFO Mode

In FIFO mode, the transmit and receive data is stored in integrated FIFO register memory. The TX FIFO is accessed by writing command 66h followed directly by the data/clk that the host wants to write into the TX FIFO. The RX FIFO is accessed by writing command 77h followed by the number of clock cycles of data the host would like to read out of the RX FIFO. The RX data will be clocked out onto the SDO pin.

In TX FIFO mode, the data bytes stored in FIFO memory are “packaged” together with other fields and bytes of information to construct the final transmit packet structure. These other potential fields include the Preamble, Sync word, and CRC checksum. In TX mode, the packet structure may be highly customized by enabling or disabling individual fields; for example, it is possible to disable both the Preamble and Sync Word fields and to load the entire packet structure into FIFO memory. For further information on the configuration of the FIFOs for a specific application or packet size, see "6. Data Handling and Packet Handler" on page 38. In RX mode, the Packet Handler must be enabled to allow storage of received data bytes into RX FIFO memory. The Packet Handler is required to detect the Sync Word, and proper detection of the Sync Word is required to determine the start of the Payload. All bytes after the Sync Word are stored in RX FIFO memory except the CRC checksum and (optionally) the variable packet length byte(s). When the FIFO is being used in RX mode, all of the received data may still be observed directly (in realtime) by properly programming a GPIO pin as the RXDATA output pin; this can be quite useful during application development. When in FIFO mode, the chip will automatically exit the TX or RX State when either the PACKET_SENT or PACKET_RX interrupt occurs. The chip will return to the state programmed in the argument of the “START TX” or “START RX” API command, TXCOMPLETE_STATE[3:0] or RXVALID_STATE[3:0]. For example, the chip may be placed into READY mode after a TX packet by sending the “START TX” command and by writing 30h to the TXCOMPLETE_STATE[3:0] argument. The chip will transmit all of the contents of the FIFO, and the PACKET_SENT interrupt will occur. When this event occurs, the chip will return to the READY state as defined by TXCOMPLETE_STATE[3:0] = 30h.

4.2.2.2. FIFO Direct Mode (Infinite Receive)

In some applications, there is a need to receive extremely long packets (greater than 40 kB) while relying on preamble and sync word detection from the on-chip packet handler. In these cases, the packet length is unknown, and the device will load the bits after the sync word into the RX FIFO forever. Other features, such as Data Whitening, CRC, Manchester, etc., are supported in this mode, but CRC calculation is not because the end of packet is unknown to the device. The RX data and clock are also available on GPIO pins. The host MCU will need to reset the packet handler by issuing a START_RX to begin searching for a new packet.

4.2.2.3. Automatic TX Packet Repeat

In TX mode, there is an option to send the FIFO contents repeatedly with a user-defined number of times to repeat. This is limited to the FIFO size, and the entire contents of the packet including preamble and sync word need to be loaded into the TX FIFO. This is selectable via the START_TX API, and packets will be sent without any gaps between them.

4.2.2.4. Direct Mode

For legacy systems that perform packet handling within the host MCU or other baseband chip, it may not be desirable to use the FIFO. For this scenario, a Direct mode is provided, which bypasses the FIFOs entirely. In TX Direct mode, the TX modulation data is applied to an input pin of the chip and processed in “real time” (i.e., not stored in a register for transmission at a later time). Any of the GPIOs may be configured for use as the TX Data input function. Furthermore, an additional pin may be required for a TX Clock output function if GFSK modulation is desired (only the TX Data input pin is required for FSK or OOK). To achieve direct mode, the desired GPIO pin must be configured as a digital input by setting the GPIO_PIN_CFG API command = enumeration 0x04 in addition to setting the MODEM_MOD_TYPE API property to source the TXDATA stream from that same GPIO pin. For GFSK, “TX_DIRECT_MODE_TYPE” must be set to synchronous. For 2FSK or OOK, the type can be set to asynchronous or synchronous. The MOD_SOURCE[1:0] field within the MODEM_MOD_TYPE property should be set = 0x01h for all Direct mode configurations. In RX Direct mode, the RX Data and RX Clock can be programmed for direct (real-time) output to GPIO pins. The microcontroller may then process the RX data without using the FIFO or packet handler functions of the RFIC.

4.3. Preamble Length

4.3.1. Digital Signal Arrival Detector (DSA)

Traditional preamble detection requires 20 bits to detect preamble. This device introduces a new approach to signal detection that can detect a preamble pattern in as little as one byte. If AFC is enabled, a preamble length of two bytes is sufficient to reliably detect signal arrival and settle a one-shot AFC. The impact of this is significant for low-power solutions as it reduces the amount of time the receiver has to stay active to detect the preamble. This feature is used with Preamble Sense Mode (see "8.6. Preamble Sense Mode" on page 42) and the latest WMBus N modes as well as with features, such as frequency hopping, which may use signal arrival as a condition to hop. The traditional preamble detector is also available to maintain backward compatibility. Note that the DSA is using the RSSI jump detector. When used for collision detection, the RSSI jump detector may need to be reconfigured after preamble detection. Refer to the API documentation for details on how to configure the device to use the signal arrival detector.

4.3.2. Traditional Preamble Detection

Optimal performance of the chip is obtained by qualifying reception of a valid Preamble pattern prior to continuing with reception of the remainder of the packet (e.g., Sync Word and Payload). Reception of the Preamble is considered valid when a minimum number of consecutive bits of 101010... pattern have been received; the required threshold for preamble detection is specified by the RX_THRESH[6:0] field in the PREAMBLE_CONFIG_STD_1 property. The appropriate value of the detection threshold depends upon the system application and typically trades off speed of acquisition against the probability of false detection. If the detection threshold is set too low, the chip may readily detect the short pattern within noise; the chip then proceeds to attempt to detect the remainder of the non-existent packet, with the result that the arrival of an actual valid packet may be missed. If the detection threshold is set too high, the required number of transmitted Preamble bits must be increased accordingly, leading to longer packet lengths and shorter battery life. A preamble detection threshold value of 20 bits is suitable for most applications. The total length of the transmitted Preamble field must be at least equal to the receive preamble detection threshold, plus an additional number of bits to allow for acquisition of bit timing and settling of the AFC algorithm. The recommended preamble detection thresholds and preamble lengths for a variety of operational modes are listed in Table 13.

Configuration of the preamble detection threshold in the RX_THRESH[6:0] field is only required for reception of a standard Preamble pattern (i.e., 101010... pattern). Reception of a repetitive but non-standard Preamble pattern is also supported in the chip but is configured through the PREAMBLE_CONFIG_NSTD and PREAMBLE_PATTERN properties.

Table 13. Recommended Preamble Length

Mode	AFC	Antenna Diversity	Preamble Type	Recommended Preamble Length	Recommended Preamble Detection Threshold
(G)FSK	Disabled	Disabled	Standard	4 Bytes	20 bits
(G)FSK	Enabled	Disabled	Standard	5 Bytes	20 bits
(G)FSK	Disabled	Disabled	Non-standard	2 Bytes	0 bits
(G)FSK	Enabled		Non-standard	Not Supported	
(G)FSK	Disabled	Enabled	Standard	7 Bytes	24 bits
(G)FSK	Enabled	Enabled	Standard	8 Bytes	24 bits
4(G)FSK	Disabled	Disabled	Standard	40 symbols	16 symbols
4(G)FSK	Enabled	Disabled	Standard	48 symbols	16 symbols
4(G)FSK			Non-standard	Not Supported	
OOK	Disabled	Disabled	Standard	4 Bytes	20 bits
OOK	Disabled	Disabled	Non-standard	2 Bytes	0 bits
OOK	Enabled			Not Supported	

Notes:

1. The recommended preamble length and preamble detection thresholds listed above are to achieve 0% PER. They may be shortened when occasional packet errors are tolerable.
2. All recommended preamble lengths and detection thresholds include AGC and BCR settling times.
3. “Standard” preamble type should be set for an alternating data sequence at the max data rate (…10101010…)
4. “Non-standard” preamble type can be set for any preamble type including …10101010...
5. When preamble detection threshold = 0, sync word needs to be 3 Bytes to avoid false syncs. When only a 2 Byte sync word is available the sync word detection can be extended by including the last preamble Byte into the RX sync word setting.

5. Internal Functional Blocks

The following sections provide an overview to the key internal blocks and features.

5.1. RX Chain

The internal low-noise amplifier (LNA) is designed to be a wide-band LNA that can be matched with three or four external discrete components to cover any common range of frequencies in the sub-GHz band. The LNA has extremely low noise to suppress the noise of the following stages and achieve optimal sensitivity; so, no external gain or front-end modules are necessary. The LNA has gain control, which is controlled by the internal automatic gain control (AGC) algorithm. The LNA is followed by an I-Q mixer, filter, programmable gain amplifier (PGA), and ADC. The I-Q mixers downconvert the signal to an intermediate frequency. The PGA then boosts the gain to be within dynamic range of the ADC. The ADC rejects out-of-band blockers and converts the signal to the digital domain where filtering, demodulation, and processing is performed. Peak detectors are integrated at the output of the LNA and PGA for use in the AGC algorithm.

The RX and TX pins may be directly tied externally for output powers less than +17 dBm in the higher-frequency bands and can support +20 dBm in the lower bands, such as 169MHz. This reduces BOM cost by saving the expense of a switch for single antenna solutions. See the direct-tie reference designs on the Silicon Labs web site for more details.

5.1.1. RX Chain Architecture

It is possible to operate the RX chain in different architecture configurations: fixed-IF, zero-IF, and scaled-IF. There are trade-offs between the architectures in terms of sensitivity, selectivity, and image rejection. Fixed-IF is the default configuration and is recommended for most applications. With 35 dB native image rejection and autonomous image calibration to achieve 55 dB, the fixed-IF solution gives the best performance for most applications. Fixed-IF obtains the best sensitivity, but it has the effect of degraded selectivity at the image frequency. An autonomous image rejection calibration is included in Si446x devices and described in more detail in "5.2.3. Image Rejection and Calibration" on page 30. For scaled-IF and zero-IF, the sensitivity is degraded for data rates less than 100 kbps or bandwidths less than 200 kHz. The reduction in sensitivity is caused by increased flicker noise as dc is approached. The benefit of zero-IF is that there is no image frequency; so, there is no degradation in the selectivity curve, but it has the worst sensitivity. Scaled-IF is a trade-off between fixed-IF and zero-IF. In the scaled-IF architecture, the image frequency is placed or hidden in the adjacent channel where it only slightly degrades the typical adjacent channel selectivity. The scaled-IF approach has better sensitivity than zero-IF but still some degradation in selectivity due to the image. In scaled-IF mode, the image frequency is directly proportional to the channel bandwidth selected. Figure 9 demonstrates the trade-off in sensitivity between the different architecture options.

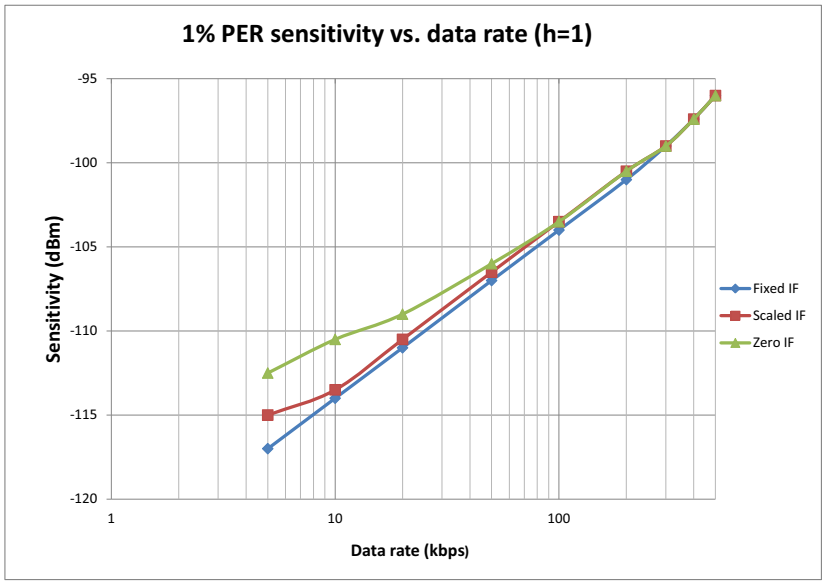


Figure 9. RX Architecture vs. Data Rate

5.2. RX Modem

Using high-performance ADCs allows channel filtering, image rejection, and demodulation to be performed in the digital domain, which allows for flexibility in optimizing the device for particular applications. The digital modem performs the following functions:

- Channel selection filter
- TX modulation
- RX demodulation
- Automatic Gain Control (AGC)
- Preamble detection
- Invalid preamble detection
- Radio signal strength indicator (RSSI)
- Automatic frequency compensation (AFC)
- Image Rejection Calibration
- Packet handling
- Cyclic redundancy check (CRC)

The digital channel filter and demodulator are optimized for ultra-low-power consumption and are highly configurable. Supported modulation types are GFSK, FSK, 4GFSK, 4FSK, GMSK, and OOK. The channel filter can be configured to support bandwidths ranging from 850 kHz down to 1.1 kHz. A large variety of data rates are supported ranging from 100 bps up to 1 Mbps. The configurable preamble detector is used with the synchronous demodulator to improve the reliability of the sync-word detection. Preamble detection can be skipped using only sync detection, which is a valuable feature in some applications. The received signal strength indicator (RSSI) provides a measure of the signal strength received on the tuned channel. The resolution of the RSSI is 0.5 dB. This high-resolution RSSI enables accurate channel power measurements for clear channel assessment (CCA), carrier sense (CS), and listen before talk (LBT) functionality. A comprehensive programmable packet handler is integrated to create a variety of communication topologies ranging from peer-to-peer networks to mesh networks. The extensive programmability of the packet header allows for advanced packet filtering, which, in turn enables a mix of broadcast, group, and point-to-point communication. A wireless communication channel can be corrupted by noise and interference, so it is important to know if the received data is free of errors. A cyclic redundancy check (CRC) is used to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the end of each transmitted packet and verified by the receiver to confirm that no errors have occurred. The packet handler and CRC can significantly reduce the load on the system microcontroller allowing for a simpler and cheaper microcontroller. The digital modem includes the TX modulator, which converts the TX data bits into the corresponding stream of digital modulation values to be summed with the fractional input to the sigma-delta modulator. This modulation approach results in highly accurate resolution of the frequency deviation. A Gaussian filter is implemented to support GFSK and 4GFSK, considerably reducing the energy in adjacent channels. The default bandwidth-time product (BT) is 0.5 for all programmed data rates, but it may be adjusted to other values.

5.2.1. Automatic Gain Control (AGC)

The AGC algorithm is implemented digitally using an advanced control loop optimized for fast response time. The AGC occurs within a single bit or in less than 2 µs. Peak detectors at the output of the LNA and PGA allow for optimal adjustment of the LNA gain and PGA gain to optimize IM3, selectivity, and sensitivity performance.

5.2.2. Auto Frequency Correction (AFC)

Frequency mistuning caused by crystal inaccuracies can be compensated for by enabling the digital automatic frequency control (AFC) in receive mode. There are two types of integrated frequency compensation: modem frequency compensation and AFC by adjusting the PLL frequency. With AFC disabled, the modem compensation can correct for frequency offsets up to ±0.25 times the IF bandwidth. When the AFC is enabled, the received signal is centered in the passband of the IF filter, providing optimal sensitivity and selectivity over a wider range of frequency offsets up to ±0.35 times the IF bandwidth. When AFC is enabled, the preamble length needs to be long enough to settle the AFC. As shown in Table 13 on page 27, an additional byte of preamble is typically required to settle the AFC.

5.2.3. Image Rejection and Calibration

Since the receiver utilizes a low-IF architecture, the selectivity will be affected by the image frequency. The IF frequency is 468.75 kHz (Fxtal/64), and the image frequency will be at 937.5 kHz (2 x Fxtal/64) below the RF frequency. The native image rejection of the Si446x family is 40 dB. Image rejection calibration is available in the Si446x to improve the image rejection to more than 55 dB. The calibration is initiated with the IRCAL API command. The calibration uses an internal signal source, so no external signal generator is required. The initial calibration takes 250 ms, and periodic re-calibration takes 100 ms. Recalibration should be initiated when the temperature has changed more than 30 °C.

5.2.4. Received Signal Strength Indicator

The received signal strength indicator (RSSI) is an estimate of the signal strength in the channel to which the receiver is tuned. The RSSI measurement is done after the channel filter, so it is only a measurement of the in-band signal power (desired or undesired). There are two methods for reading the RSSI value and several different options for configuring the returned RSSI value. The fastest method for reading the RSSI is to configure one of the four fast response registers (FRR) to return a latched RSSI value. The latched RSSI value is measured once per packet and is latched at a configurable amount of time after RX mode is entered. The fast response registers can be read in 16 SPI clock cycles with no requirement to wait for CTS. The RSSI value may also be read out of the GET_MODEM_STATUS command. In this command, both the current RSSI and the latched RSSI are available. The current RSSI value represents the signal strength at the instant in time the GET_MODEM_STATUS command is processed and may be read multiple times per packet. Reading the RSSI in the GET_MODEM_STATUS command takes longer than reading the RSSI out of the fast response register. After the initial command, it takes 33 µs for CTS to be set and then the four or five bytes of SPI clock cycles to read out the respective current or latched RSSI values.

The RSSI configuration options are set in the MODEM_RSSI_CONTROL API property. The latched RSSI value may be latched and stored based on the following events: preamble detection, sync detection, or a configurable number of bit times measured after the start of RX mode (minimum of 4 bit times). The requirement for a minimum of four bit times is determined by the processing delay and settling through the modem and digital channel filter. In MODEM_RSSI_CONTROL, the RSSI may be defined to update every bit period or to be averaged and updated every four bit periods. If RSSI averaging over four bits is enabled, the latched RSSI value will be delayed to a minimum of seven bits after the start of RX mode to allow for the averaging. The latched RSSI values are cleared when entering RX mode so they may be read after the packet is received or after dropping back to standby mode. If the RSSI value has been cleared by the start of RX but not yet latched, a value of 0 will be returned if it is attempted to be read.

The RSSI value read by the API may be translated into dBm by the following linear equation:

RF_Input_Level_dBm = (RSSI_value / 2) – MODEM_RSSI_COMP – 70

The MODEM_RSSI_COMP property provides for fine adjustment of the relationship between the actual RF input level (in dBm) and the returned RSSI value. That is, adjustment of this property allows the user to shift the RSSI vs RF Input Power curve up and down. This may be desirable to compensate for differences in front-end insertion loss between multiple designs (e.g., due to the presence of a SAW preselection filter, or an RF switch). A value of MODEM_RSSI_COMP = 0x40 = 64d is appropriate for most applications.

Clear channel assessment (CCA) or RSSI threshold detection is also available. An RSSI threshold may be set in the MODEM_RSSI_THRESH API property. If the Current RSSI value is above this threshold, an interrupt or GPIO may notify the host. Both the latched version and asynchronous version of this threshold are available on any of the GPIOs. Automatic fast hopping based on RSSI is available. See “5.3.1.2. Automatic RX Hopping and Hop Table”.

5.2.5. RSSI Jump Indicator (Collision Detection)

The chip is capable of detecting a jump in RSSI in either direction (i.e., either a signal increase or a signal decrease). Both polarities of jump detection may be enabled simultaneously, resulting in detection of a Jump-Up or Jump-Down event. This may be used to detect whether a secondary interfering signal (desired or undesired) has "collided" with reception of the current packet. An interrupt flag or GPIO pin may be configured to notify the host MCU of the Jump event. The change in RSSI level required to trigger the Jump event is programmable through the MODEM_RSSI_JUMP_THRESH API property.

The chip may be configured to reset the RX state machine upon detection of an RSSI Jump, and thus to automatically begin reacquisition of the packet. The chip may also be configured to generate an interrupt.

This functionality is intended to detect an abrupt change in RSSI level and to not respond to a slow, gradual change in RSSI level. This is accomplished by comparing the difference in RSSI level over a programmable time period. In this fashion, the chip effectively evaluates the slope of the change in RSSI level.

The arrival of a desired packet (i.e., the transition from receiving noise to receiving a valid signal) will likely be detected as an RSSI Jump event. For this reason, it is recommended to enable this feature in mid-packet (i.e., after signal qualification, such as PREAMBLE_VALID.) Refer to the API documentation for configuration options.

5.3. Synthesizer

An integrated Sigma Delta (ΣΔ) Fractional-N PLL synthesizer capable of operating over the bands from 142–175, 283–350, 350–525, and 850–1050 MHz. Using a ΣΔ synthesizer has many advantages; it provides flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider, which results in very precise accuracy and control over the transmit deviation. The frequency resolution in the 850–1050 MHz band is 28.6 Hz with finer resolution in the other bands. The nominal reference frequency to the PLL is 30 MHz, but any XTAL frequency from 25 to 32 MHz may be used. The modem configuration calculator in WDS will automatically account for the XTAL frequency being used. The PLL utilizes a differential LC VCO with integrated on-chip inductors. The output of the VCO is followed by a configurable divider, which will divide the signal down to the desired output frequency band.

5.3.1. Synthesizer Frequency Control

The frequency is set by changing the integer and fractional settings to the synthesizer. The WDS calculator will automatically provide these settings, but the synthesizer equation is shown below for convenience. The APIs for setting the frequency are FREQ_CONTROL_INTE, FREQ_CONTROL_FRAC2, FREQ_CONTROL_FRAC1, and FREQ_CONTROL_FRAC0.

$$\text{RF\_channel} = \left(\text{fc\_inte} + \frac{\text{fc\_frac}}{2^{19}}\right) \times \frac{2 \times \text{freq\_xo}}{\text{outdiv}} (\text{Hz})$$

Note: The fc_frac/2^{19} value in the above formula has to be a number between 1 and 2.

Table 14. Output Divider (Outdiv) Values for the Si4463/61/60

Outdiv	Lower (MHz)	Upper (MHz)
24	142	175
12	284	350
10	350	420
8	420	525
4	850	1050

5.3.1.1. EZ Frequency Programming

In applications that utilize multiple frequencies or channels, it may not be desirable to write four API registers each time a frequency change is required. EZ frequency programming is provided so that only a single register write (channel number) is required to change frequency. A base frequency is first set by first programming the integer and fractional components of the synthesizer. This base frequency will correspond to channel 0. Next, a channel step size is programmed into the FREQ_CONTROL_CHANNEL_STEP_SIZE_1 and FREQ_CONTROL_CHANNEL_STEP_SIZE_0 API registers. The resulting frequency will be:

$$\text{RF Frequency} = \text{Base Frequency} + \text{Channel} \times \text{Stepsize}$$

The second argument of the START_RX or START_TX is CHANNEL, which sets the channel number for EZ frequency programming. For example, if the channel step size is set to 1 MHz, the base frequency is set to 900 MHz with the FREQ_CONTROL_INTE and FREQ_CONTROL_FRAC API properties, and a CHANNEL number of 5 is programmed during the START_TX command, the resulting frequency will be 905 MHz. If no CHANNEL argument is written as part of the START_RX/TX command, it will default to the previously-programmed value. The initial value of CHANNEL is 0; so, if no CHANNEL value is written, it will result in the programmed base frequency.

5.3.1.2. Automatic RX Hopping and Hop Table

The transceiver supports an automatic RX hopping feature that can be fully configured through the API. This functionality is useful in applications where it is desired to look for packets but to hop to the next channel if a packet is not found. The sequence of channel numbers that are visited are specified by entries in a hop table. If this feature is enabled, the device will automatically start hopping through the channels listed in the hop table as soon as the chip enters RX mode.

The hop table can hold up to 64 entries and is maintained in firmware inside the RFIC. Each entry is a channel number, allowing construction of a frequency plan of up to 64 channels. The number of entries in the table is set by RX HOP TABLE_SIZE API. The specified channels correspond to the EZ frequency programming method for programming the frequency. The receiver starts at the base channel and hops in sequence from the top of the hop table to the bottom. The table will wrap around to the base channel once it reaches the end of the table. An entry of 0xFF in the table indicates that the entry should be skipped. The device will hop to the next entry in the table that contains a non-0xFF value.

There are three conditions that can be used to determine whether to continue hopping or to stay on a particular channel. These conditions are as follows:

- RSSI threshold
- Preamble timeout (invalid preamble pattern)
- Sync word timeout (invalid or no sync word detected after preamble)

These conditions can be used individually, or they can be enabled all together by configuring the RX_HOP_CONTROL API. However, the firmware will make a decision on whether or not to hop based on the first condition that is met.

The RSSI that is monitored is the current RSSI value. This is compared to the threshold value set in the MODEM_RSSI_THRESH API property, and, if it is above the threshold value, it will stay on the channel. If the RSSI is below the threshold, it will continue hopping. There is no averaging of RSSI done during the automatic hopping from channel to channel. Since the preamble timeout and the sync word timeout are features that require packet handling, the RSSI threshold is the only condition that can be used if the user is in “direct” or “RAW” mode where packet handling features are not used.

The RSSI threshold value may be converted to an approximate equivalent RF input power level through the equation shown in "5.2.4. Received Signal Strength Indicator" on page 30. However, performance should be verified on the bench to optimize the threshold setting for a given application.

The time spent in receive mode will be determined by the configuration of the hop conditions. Manual RX hopping will have the fastest turn-around time but will require more overhead and management by the host MCU.

The following are example steps for using Auto Hop:

1. Set the base frequency (inte + frac) and channel step size.
2. Define the number of entries in the hop table (RX_HOP_TABLE_SIZE).
3. Write the channels to the hop table (RX_HOP_TABLE_ENTRY_n)
4. Configure the hop condition and enable auto hopping- RSSI, preamble, or sync (RX_HOP_CONTROL).
5. Set preamble and sync parameters if enabled.
6. Program the RSSI threshold property in the modem using “MODEM_RSSI_THRESH”.
7. Set the preamble threshold using “PREAMBLE_CONFIG_STD_1”.
8. Program the preamble timeout property using “PREAMBLE_CONFIG_STD_2”.
9. Set the sync detection parameters if enabled.
10. If needed, use “GPIO_PIN_CFG” to configure a GPIO to toggle on hop and hop table wrap.
11. Use the “START_RX” API with channel number set to the first valid entry in the hop table (i.e., the first non 0xFF entry).
12. Device should now be in auto hop mode.

5.3.1.3. Manual RX Hopping

The RX_HOP command provides the fastest method for hopping from RX to RX but it requires more overhead and management by the host MCU. The timing is faster with this method than Start_RX or RX hopping because one of the calculations required for the synthesizer calibrations is offloaded to the host and must be calculated/stored by the host, VCO_CNT0. For VCO_CNT values, download the Si446x RX_HOP PLL calculator spreadsheet from the Si446x product website.

5.4. Transmitter (TX)

The Si4463 contains an integrated +20 dBm transmitter or power amplifier that is capable of transmitting from –20 to +20 dBm. The resolution of the programmable steps in output power is less than 0.25 dB when operated within 6 dB of the maximum power setting; the resolution of the steps in output power becomes coarser and more non-linear as the output power is reduced towards the minimum end of its control range. The Si4463 PA is designed to provide the highest efficiency and lowest current consumption possible. The Si4460 is designed to supply +10 dBm output power for less than 20 mA for applications that require operation from a single coin cell battery. The Si4460 can operate with Class-E matching and output up to +13 dBm Tx power at a supply voltage of VDD = 3.3 V. All PA options are single-ended to allow for easy antenna matching and low BOM cost. Automatic ramp-up and ramp-down is automatically performed to reduce unwanted spectral spreading. Refer to “AN627: Si4460/61 Low-Power PA Matching” and “AN648: PA Matching” for details on TX matching options.

The chip’s TXRAMP pin is disabled by default to save current in cases where the on-chip PA provides sufficient output power to drive the antenna. In cases where on-chip PA will drive the external PA, and the external PA needs a ramping signal, TXRAMP is the signal to use. To enable TXRAMP, set the API Property PA_MODE[7] = 1. TXRAMP will start to ramp up, and ramp down at the SAME time as the internal on-chip PA ramps up/down.

However, the time constant of the TXRAMP signal for the external PA is programmed independently of the ramp time constant for the on-chip PA. The ramp time constant for TXRAMP is programmed by the TC[3:0] field in the PA_RAMP_EX API property and provides the following approximate ramp times as a function of TC[3:0] value.

Table 15. Ramp Times as a Function of TC[3:0] Value

TC	Ramp Time (µs)
0	1.25
1	1.33
2	1.43
3	1.54
4	1.67
5	1.82
6	2.00
7	2.22
8	2.50
9	2.86
10	3.33
11	4.00
12	5.00
13	6.67
14	10.00
15	20.00

The ramping profile is close to a linear ramping profile with smoothed out corner when approaching Vhi and Vlo. The TXRAMP pin can source up to 1 mA without voltage drooping. The TXRAMP pin's sinking capability is equivalent to a 10 kΩ pull-down resistor.

Vhi = 3 V when Vdd > 3.3 V. When Vdd < 3.3 V, the Vhi will be closely following the Vdd, and ramping time will be smaller also.

Vlo = 0 V when NO current needed to be sunk into TXRAMP pin. If 10uA need to be sunk into the chip, Vlo will be 10 µA x 10k = 100 mV.

Number	Command	Summary
0x2200	PA_MODE	Sets PA type.
0x2201	PA_PWR_LVL	Adjust TX power in fine steps.
0x2202	PA_BIAS_CLKDUTY	Adjust TX power in coarse steps and optimizes for different match configurations.
0x2203	PA_TC	Changes the ramp up/down time of the PA.

5.4.1. Si4463: +20 dBm PA

The +20 dBm configuration utilizes a class-E matching configuration for all frequency bands except 169 MHz where it uses a Square Wave match. Typical performance for the 915 MHz band for output power steps, voltage, and temperature are shown in Figures 10–12. The output power is changed in 128 steps through PA_PWR_LVL API. For detailed matching values, BOM, and performance at other frequencies, refer to “AN648: PA Matching”.

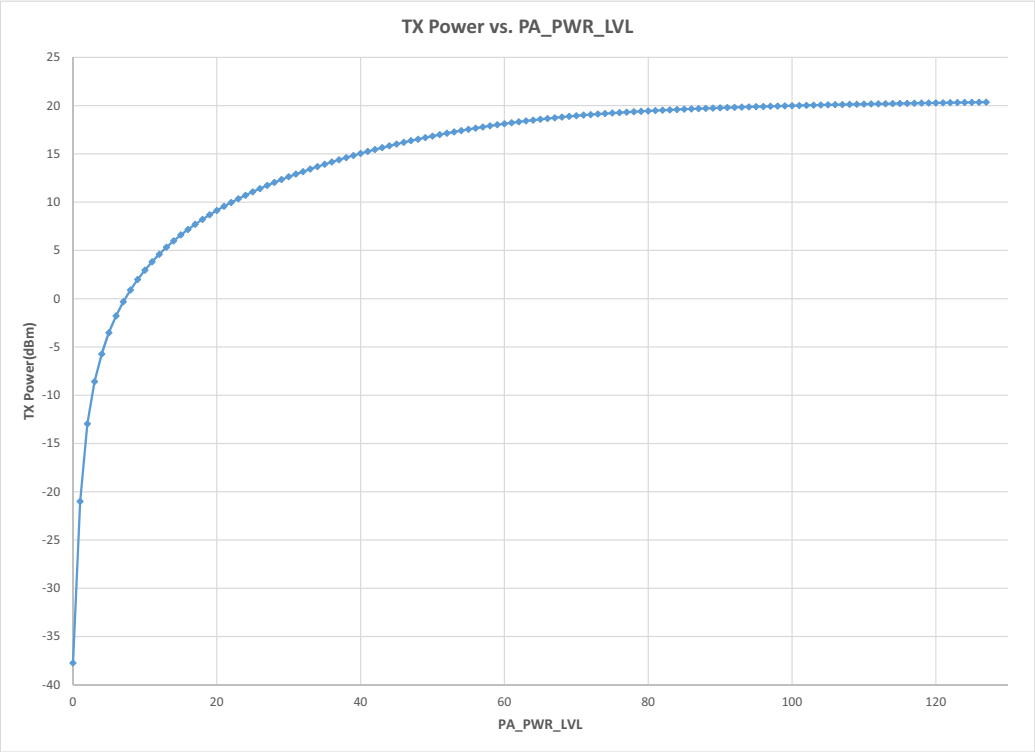


Figure 10. +20 dBm TX Power vs. PA_PWR_LVL

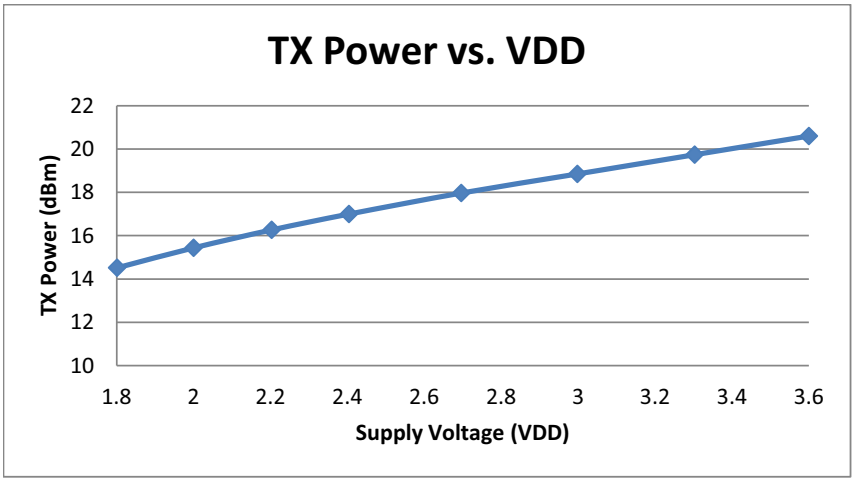


Figure 11. +20 dBm TX Power vs. VDD

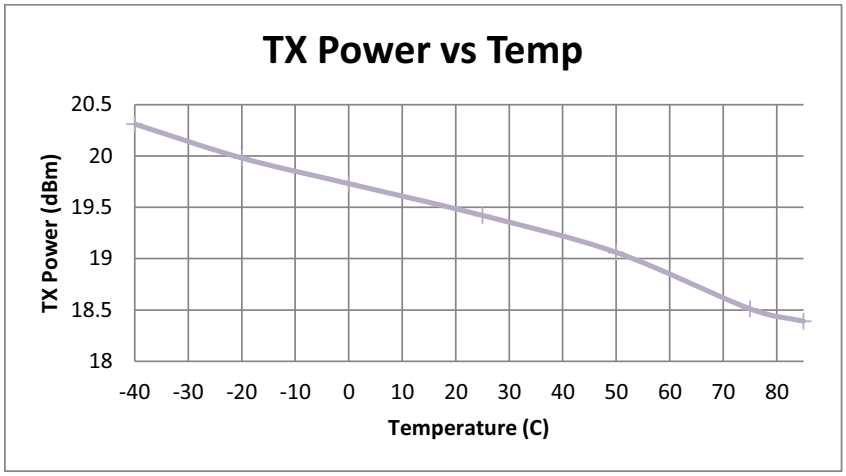


Figure 12. +20 dBm TX Power vs. Temp

5.5. Crystal Oscillator

The Si446x includes an integrated crystal oscillator with a fast start-up time of less than 250 µs. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the crystal. The default crystal is 30 MHz, but the circuit is designed to handle any XTAL from 25 to 32 MHz. If a crystal different than 30 MHz is used, the POWER_UP API boot command must be modified. The WDS calculator crystal frequency field must also be changed to reflect the frequency being used. The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the GLOBAL_XO_TUNE API property. The total internal capacitance is 11 pF and is adjustable in 127 steps (70 fF/step). The crystal frequency adjustment can be used to compensate for crystal production tolerances. The frequency offset characteristics of the capacitor bank are demonstrated in Figure 13.

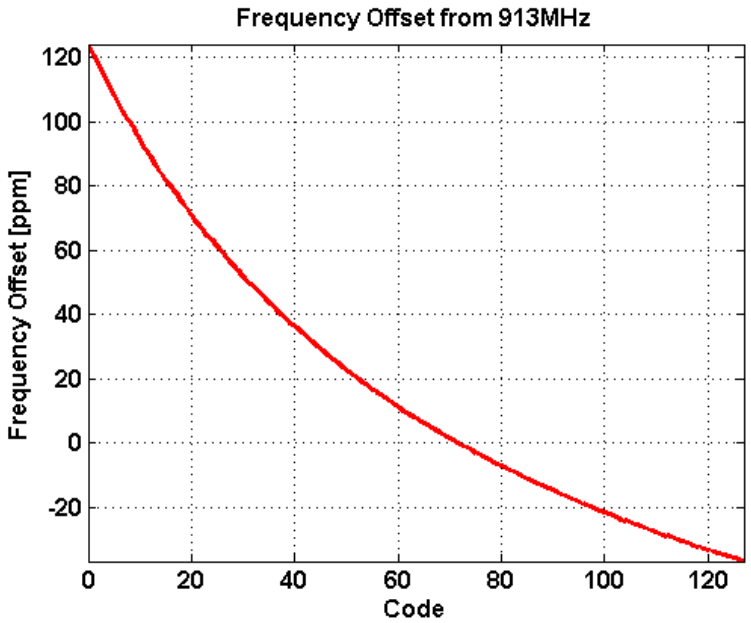


Figure 13. Capacitor Bank Frequency Offset Characteristics

Utilizing the on-chip temperature sensor and suitable control software, the temperature dependency of the crystal can be canceled.

A TCXO or external signal source can easily be used in place of a conventional XTAL and should be connected to the XIN pin. The incoming clock signal is recommended to have a peak-to-peak swing in the range of 600 mV to 1.4 V and ac-coupled to the XIN pin. If the peak-to-peak swing of the TCXO exceeds 1.4 V peak-to-peak, then dc coupling to the XIN pin should be used. The maximum allowed swing on XIN is 1.8 V peak-to-peak.

The XO capacitor bank should be set to 0 whenever an external drive is used on the XIN pin. In addition, the POWER_UP command should be invoked with the TCXO option whenever external drive is used.

6. Data Handling and Packet Handler

6.1. RX and TX FIFOs

Two 64-byte FIFOs are integrated into the chip, one for RX and one for TX, as shown in Figure 14. For dedicated TX or RX, the FIFO size is up to 129 bytes. Writing to command Register 66h loads data into the TX FIFO, and reading from command Register 77h reads data from the RX FIFO. The TX FIFO has a threshold for when the FIFO is almost empty, which is set by the “TX_FIFO_EMPTY” property. An interrupt event occurs when the data in the TX FIFO reaches the almost empty threshold. If more data is not loaded into the FIFO, the chip automatically exits the TX state after the PACKET_SENT interrupt occurs. The RX FIFO has one programmable threshold, which is programmed by setting the “RX_FIFO_FULL” property. When the incoming RX data crosses the Almost Full Threshold, an interrupt will be generated to the microcontroller via the nIRQ pin. The microcontroller will then need to read the data from the RX FIFO. The RX Almost Full Threshold indication implies that the host can read at least the threshold number of bytes from the RX FIFO at that time. Both the TX and RX FIFOs may be cleared or reset with the “FIFO_RESET” command.

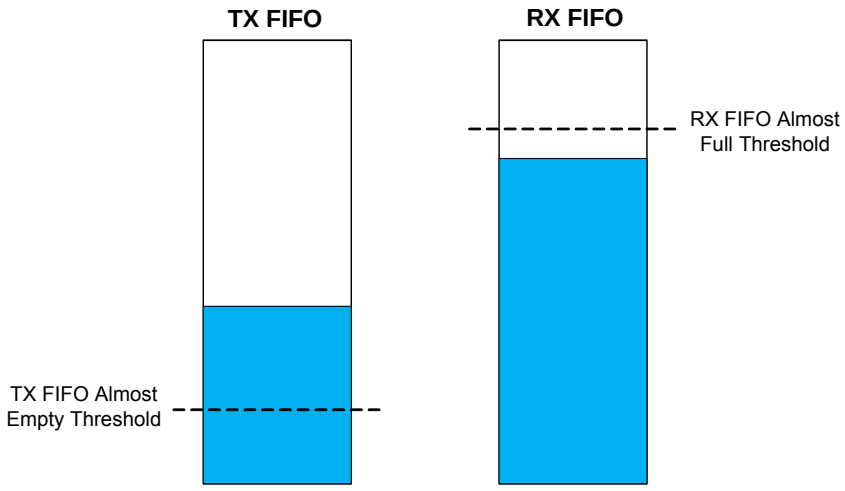


Figure 14. TX and RX FIFOs

6.2. Packet Handler

When using the FIFOs, automatic packet handling may be enabled for TX mode, RX mode, or both. The usual fields for network communication, such as preamble, synchronization word, headers, packet length, and CRC, can be configured to be automatically added to the data payload. The fields needed for packet generation normally change infrequently and can therefore be stored in registers. Automatically adding these fields to the data payload in TX mode and automatically checking them in RX mode greatly reduces the amount of communication between the microcontroller and Si446x. It also greatly reduces the required computational power of the microcontroller. The general packet structure is shown in Figure 15. Any or all of the fields can be enabled and checked by the internal packet handler.

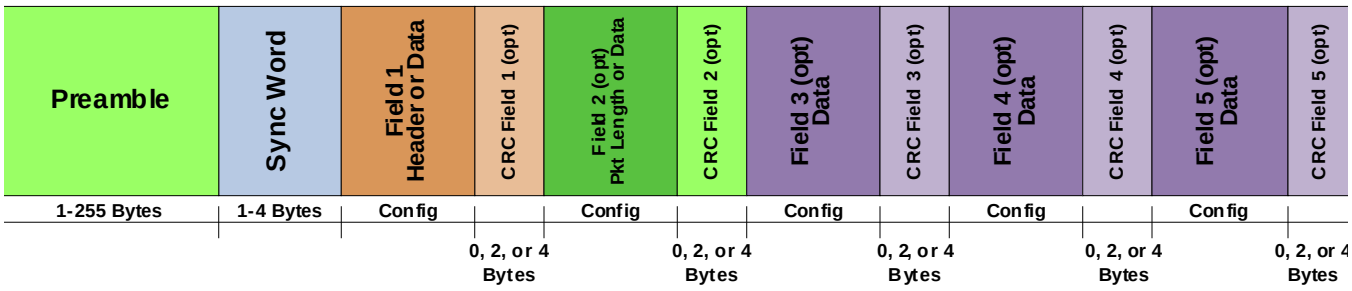


Figure 15. Packet Handler Structure

The fields are highly programmable and can be used to check any kind of pattern in a packet structure. The general functions of the packet handler include the following:

- Detection/validation of Preamble quality in RX mode (PREAMBLE_VALID signal)
- Detection of Sync word in RX mode (SYNC_OK signal)
- Detection of valid packets in RX mode (PKT_VALID signal)
- Detection of CRC errors in RX mode (CRC_ERR signal)
- Data de-whitening and/or Manchester decoding (if enabled) in RX mode
- Match/Header checking in RX mode
- Storage of Data Field bytes into FIFO memory in RX mode
- Construction of Preamble field in TX mode
- Construction of Sync field in TX mode
- Construction of Data Field from FIFO memory in TX mode
- Construction of CRC field (if enabled) in TX mode
- Data whitening and/or Manchester encoding (if enabled) in TX mode

For details on how to configure the packet handler, see “AN626: Packet Handler Operation for Si446x RFICs”.

7. RX Modem Configuration

The Si446x can easily be configured for different data rate, deviation, frequency, etc. by using the Radio Configuration Application (RCA) GUI which is part of the Wireless Development Suite (WDS) program.

8. Auxiliary Blocks

8.1. Wake-up Timer and 32 kHz Clock Source

The chip contains an integrated wake-up timer that can be used to periodically wake the chip from sleep mode. The wake-up timer runs from either the internal 32 kHz RC Oscillator, or from an external 32 kHz XTAL.

The wake-up timer can be configured to run when in sleep mode. If WUT_EN = 1 in the GLOBAL_WUT_CONFIG property, prior to entering sleep mode, the wake-up timer will count for a time specified defined by the GLOBAL_WUT_R and GLOBAL_WUT_M properties. At the expiration of this period, an interrupt will be generated on the nIRQ pin if this interrupt is enabled in the INT_CTL_CHIP_ENABLE property. The microcontroller will then need to verify the interrupt by reading the chip interrupt status either via GET_INT_STATUS or a fast response register. The formula for calculating the Wake-Up Period is as follows:

$$WUT = WUT\_M \times \frac{4 \times 2^{WUT\_R}}{32.768}[ms]$$

The RC oscillator frequency will change with temperature; so, a periodic recalibration is required. The RC oscillator is automatically calibrated during the POWER_UP command and exits from the Shutdown state. To enable the recalibration feature, CAL_EN must be set in the GLOBAL_WUT_CONFIG property, and the desired calibration period should be selected via WUT_CAL_PERIOD[2:0] in the same API property. During the calibration, the 32 kHz RC oscillator frequency is compared to the 30 MHz XTAL and then adjusted accordingly. The calibration needs to start the 30 MHz XTAL, which increases the average current consumption; so, a longer CAL_PERIOD results in a lower average current consumption. The 32 kHz XTAL accuracy is comprised of both the XTAL parameters and the internal circuit. The XTAL accuracy can be defined as the XTAL initial error + XTAL aging + XTAL temperature drift + detuning from the internal oscillator circuit. The error caused by the internal circuit is typically less than 10 ppm. Refer to API documentation for details on WUT related commands and properties.

8.2. Low Duty Cycle Mode (Auto RX Wake-Up)

The low duty cycle (LDC) mode is implemented to automatically wake-up the receiver to check if a valid signal is available or to enable the transmitter to send a packet. It allows low average current polling operation by the Si446x for which the wake-up timer (WUT) is used. RX and TX LDC operation must be set via the GLOBAL_WUT_CONFIG property when setting up the WUT. The LDC wake-up period is determined by the following formula:

$$LDC = WUT\_LDC \times \frac{4 \times 2^{WUT\_R}}{32.768}[ms]$$

where the WUT_LDC parameter can be set by the GLOBAL_WUT_LDC property. The WUT period must be set in conjunction with the LDC mode duration; for the relevant API properties, see the wake-up timer (WUT) section.

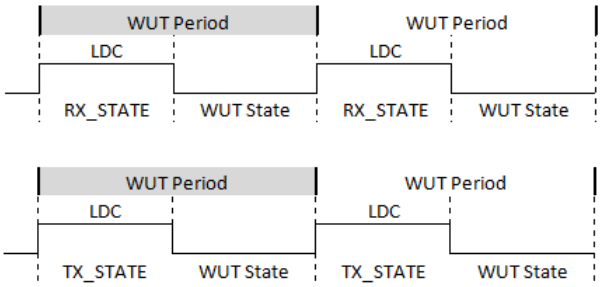


Figure 16. RX and TX LDC Sequences

The basic operation of RX LDC mode is shown in Figure 17. The receiver periodically wakes itself up to work on RX_STATE during LDC mode duration. If a valid preamble is not detected, a receive error is detected, or an entire packet is not received, the receiver returns to the WUT state (i.e., ready or sleep) at the end of LDC mode duration and remains in that mode until the beginning of the next wake-up period. If a valid preamble or sync word is detected, the receiver delays the LDC mode duration to receive the entire packet. If a packet is not received during two LDC mode durations, the receiver returns to the WUT state at the last LDC mode duration until the beginning of the next wake-up period.

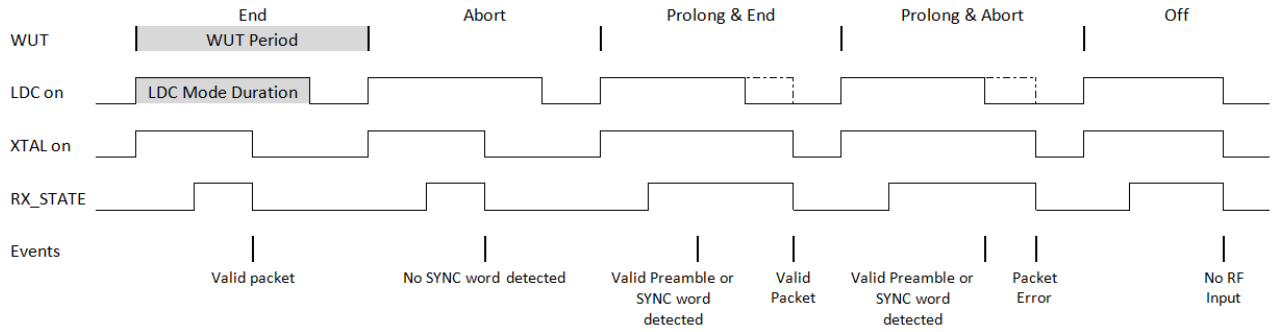


Figure 17. Low Duty Cycle Mode for RX

In TX LDC mode, the transmitter periodically wakes itself up to transmit a packet that is in the data buffer. If a packet has been transmitted, nIRQ goes low if the option is set in the INT_CTL_ENABLE property. After transmitting, the transmitter immediately returns to the WUT state and stays there until the next wake-up time expires.

8.3. Temperature, Battery Voltage, and Auxiliary ADC

The Si446x family contains an integrated auxiliary ADC for measuring internal battery voltage, an internal temperature sensor, or an external component over a GPIO. The ADC utilizes a SAR architecture and achieves 11-bit resolution. The Effective Number of Bits (ENOB) is 9 bits. When measuring external components, the input voltage range is 1 V, and the conversion rate is between 300 Hz to 2.44 kHz. The ADC value is read by first sending the GET_ADC_READING command and enabling the inputs that are desired to be read: GPIO, battery, or temp. The temperature sensor accuracy at 25 °C is typically ±2 °C. Refer to API documentation for details on the command and reply stream.

8.4. Low Battery Detector

The low battery detector (LBD) is enabled and utilized as part of the wake-up-timer (WUT). The LBD function is not available unless the WUT is enabled, but the host MCU can manually check the battery voltage anytime with the auxiliary ADC. The LBD function is enabled in the GLOBAL_WUT_CONFIG API property. The battery voltage will be compared against the threshold each time the WUT expires. The threshold for the LBD function is set in GLOBAL_LOW_BATT_THRESH. The threshold steps are in increments of 50 mV, ranging from a minimum of 1.5 V up to 3.05 V. The accuracy of the LBD is ±3%. The LBD notification can be configured as an interrupt on the nIRQ pin or enabled as a direct function on one of the GPIOs.

8.5. Antenna Diversity

To mitigate the problem of frequency-selective fading due to multipath propagation, some transceiver systems use a scheme known as antenna diversity. In this scheme, two antennas are used. Each time the transceiver enters RX mode the receive signal strength from each antenna is evaluated. This evaluation process takes place during the preamble portion of the packet. The antenna with the strongest received signal is then used for the remainder of that RX packet. The same antenna will also be used for the next corresponding TX packet. This chip fully supports antenna diversity with an integrated antenna diversity control algorithm. The required signals needed to control an external SPDT RF switch (such as a PIN diode or GaAs switch) are available on the GPIOx pins. The operation of these GPIO signals is programmable to allow for different antenna diversity architectures and configurations. The antdiv[2:0] bits are found in the MODEM_ANT_DIV_CONTROL API property descriptions and enable the antenna diversity mode. The GPIO pins are capable of sourcing up to 5 mA of current; so, it may be used directly to forward-bias a PIN diode if desired. The antenna diversity algorithm will automatically toggle back and forth between the antennas until the packet starts to arrive. The recommended preamble length for optimal antenna selection is 8 bytes.

8.6. Preamble Sense Mode

This mode of operation is suitable for extremely low power applications where power consumption is important. The preamble sense mode (PSM) takes advantage of the Digital Signal Arrival detector (DSA), which can detect a preamble within eight bit times with no sensitivity degradation. This fast detection of an incoming signal can be combined with duty cycling of the receiver during the time the device is searching or sniffing for packets over the air. The average receive current is lowered significantly when using this mode. In applications where the timing of the incoming signal is unknown, the amount of power savings is primarily dependent on the data rate and preamble length as the Rx inactive time is determined by these factors. In applications where the sleep time is fixed and the timing of the incoming signal is known, the average current also depends on the sleep time. The PSM mode is similar to the low duty cycle mode but has the benefit of faster signal detection and autonomous duty cycling of the receiver to achieve even lower average receive currents. This mode can be used with the low power mode (LP) which has an active RX current of 10 mA or with the high-performance (HP) mode which has an active RX current of 13 mA.

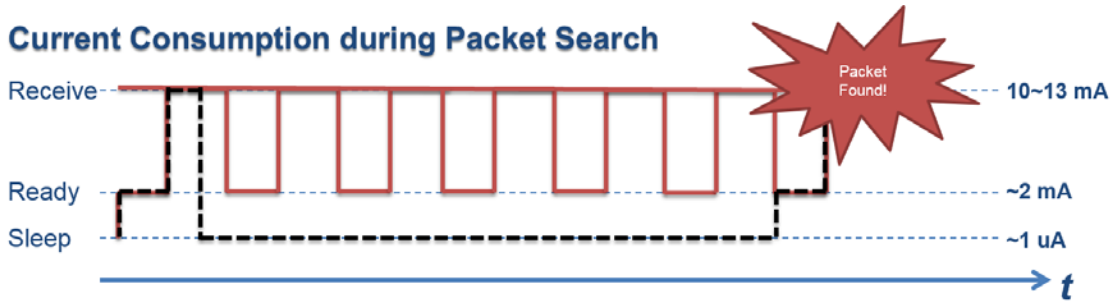


Figure 18. Preamble Sense Mode

Table 16. Data Rates

	Data Rate				
	1.2 kbps	**9.6 kbps**	**50 kbps**	**100 kbps**	
PM length = 4 bytes	6.48	6.84	8.44	10.43	mA
PM length = 8 bytes	3.83	3.96	4.57	5.33	mA
Note: Typical values. Active RX current is 13 mA.					

9. Wireless MBUS support

Wireless MBus is a widely accepted standard for smart meter communication in Europe. The radio supports all WMBus modes per the latest draft specification of the EN13757-4 standard. This includes a much wider deviation error tolerance of ±30% and frequency error tolerance of ±4 kHz, short preamble support (16-bit preamble for 2 and 4 level FSK modes), 3-of-6 encoding and decoding and 169 MHz N modes including N2g.

In addition, Silicon Labs has a production ready WMBus stack available at no additional cost which supports all modes and runs on the EFM32 (32-bit ARM) family of energy friendly microcontrollers. This stack and complete documentation including PHY configuration and test results are available for download from the EZRadioPRO page on the Silicon Labs website.

10. ETSI EN300 220 Category 1

The radio is capable of supporting ETSI Category 1 applications (social alarms, healthcare applications, etc.) in the 169 MHz and 868 MHz bands. Blocking performance is improved at the 2 MHz and 10 MHz offsets allowing for additional margin from the regulatory limits. The radio complies with ACS limits at the 25 kHz offset in both, 169 MHz and 868 MHz bands. In the 169 MHz band, there is no need for an external SAW filter for 2 MHz and 10 MHz blocking resulting in a lower system cost. In the 868 MHz band, an external SAW filter is still required to meet the Cat 1 blocking limits. An RF Pico board is available for evaluation specifically for ETSI Cat 1 applications.

Test conditions for ETSI Cat 1 specifications are different from the typical conditions and are stated below.

Data Rate: 3 kbps

Deviation: 2 kHz

Modulation: 2 GFSK

IF mode: Fixed and/or Scaled IF

RX bandwidth: 13 kHz

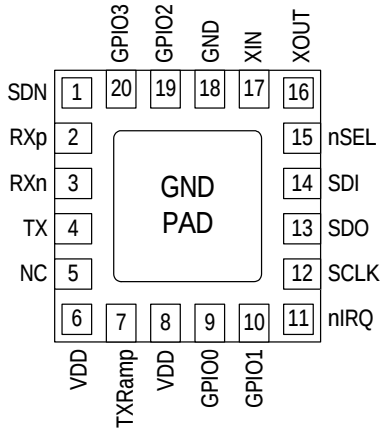
BER target: 0.1%

Blocker signal: CW

	ETSI Cat 1 limits	169 MHz band (no SAW)	868 MHz band (no SAW)
±25 kHz ACS	54 dB	62 dB	58 dB
±2 MHz blocking	84 dB	88 dB	76 dB
±10 MHz blocking	84 dB	90 dB	82 dB
RX sensitivity	–107 dB	–108 dB	–108 dB
Spurious response	35 dB	40 dB	40 dB

For further details on configuring the radio for ETSI Cat 1 applications, refer to the application notes available on the Silicon Labs website.

11. Pin Descriptions: Si4463/61/60



Pin	Pin Name	I/0	Description
1	SDN	I	**Shutdown Input Pin**. 0–VDD V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN = 1, the chip will be completely shut down, and the contents of the registers will be lost.
2	RXp	I	**Differential RF Input Pins of the LNA.** See application schematic for example matching network.
3	RXn	I	
4	TX	O	**Transmit Output Pin.** The PA output is an open-drain connection, so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.
5	NC		It is recommended to connect this pin to GND per the reference design schematic. Not connected internally to any circuitry.
6	VDD	VDD	**+1.8 to +3.8 V Supply Voltage Input to Internal Regulators.** The recommended VDD supply voltage is +3.3 V.
7	TXRAMP	O	**Programmable Bias Output with Ramp Capability for External FET PA.** See "5.4. Transmitter (TX)" on page 33.
8	VDD	VDD	**+1.8 to +3.8 V Supply Voltage Input to Internal Regulators.** The recommended VDD supply voltage is +3.3 V.
9	GPIO0	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
10	GPIO1	I/O	
11	nIRQ	O	**General Microcontroller Interrupt Status Output.** When the Si4463/61 exhibits any one of the interrupt events, the nIRQ pin will be set low = 0. The Microcontroller can then determine the state of the interrupt by reading the interrupt status. No external resistor pull-up is required, but it may be desirable if multiple interrupt lines are connected.

Pin	Pin Name	I/0	Description
12	SCLK	I	**Serial Clock Input.** 0–VDD V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the Si4463/61 on positive edge transitions.
13	SDO	O	**0–VDD V Digital Output.** Provides a serial readback function of the internal control registers.
14	SDI	I	**Serial Data Input.** 0–VDD V digital input. This pin provides the serial data stream for the 4-line serial data bus.
15	nSEL	I	**Serial Interface Select Input.** 0–VDD V digital input. This pin provides the Select/Enable function for the 4-line serial data bus.
16	XOUT	O	**Crystal Oscillator Output.** Connect to an external 25 to 32 MHz crystal, or leave floating when driving with an external source on XIN.
17	XIN	I	**Crystal Oscillator Input.** Connect to an external 25 to 32 MHz crystal, or connect to an external source.
18	GND	GND	When using an XTAL, leave floating per the reference design schematic. When using a TCXO, connect to TCXO GND, which should be separate from the board's reference ground plane.
19	GPIO2	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions, including Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
20	GPIO3	I/O	
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the Si446x supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the Si446x.

12. Ordering Information

Part Number	Description	Package Type	Operating Temperature
Si4463-C2A-GM	ISM EZRadioPRO Transceiver	QFN- Pb-free	–40 to +85 °C
Si4461-C2A-GM	ISM EZRadioPRO Transceiver	QFN- Pb-free	–40 to +85 °C
Si4460-C2A-GM	ISM EZRadioPRO Transceiver	QFN- Pb-free	–40 to +85 °C
Note: Add an “(R)” at the end of the device part number to denote tape and reel option.			

13. Package Outline: Si4463/61/60

Figure 19 illustrates the package details for the Si446x. Table 17 lists the values for the dimensions shown in the illustration.

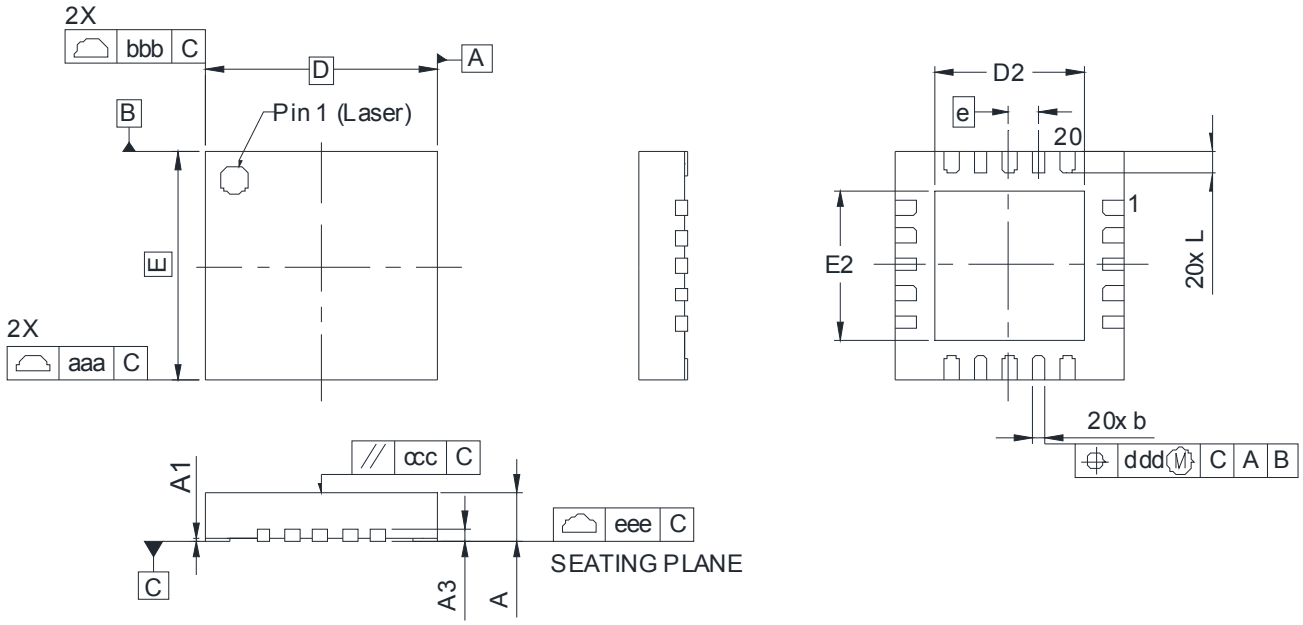


Figure 19. 20-Pin Quad Flat No-Lead (QFN)

Table 17. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.45	2.60	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.45	2.60	2.75
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.08	

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

14. PCB Land Pattern: Si4463/61/60

Figure 20 illustrates the PCB land pattern details for the Si446x. Table 18 lists the values for the dimensions shown in the illustration.

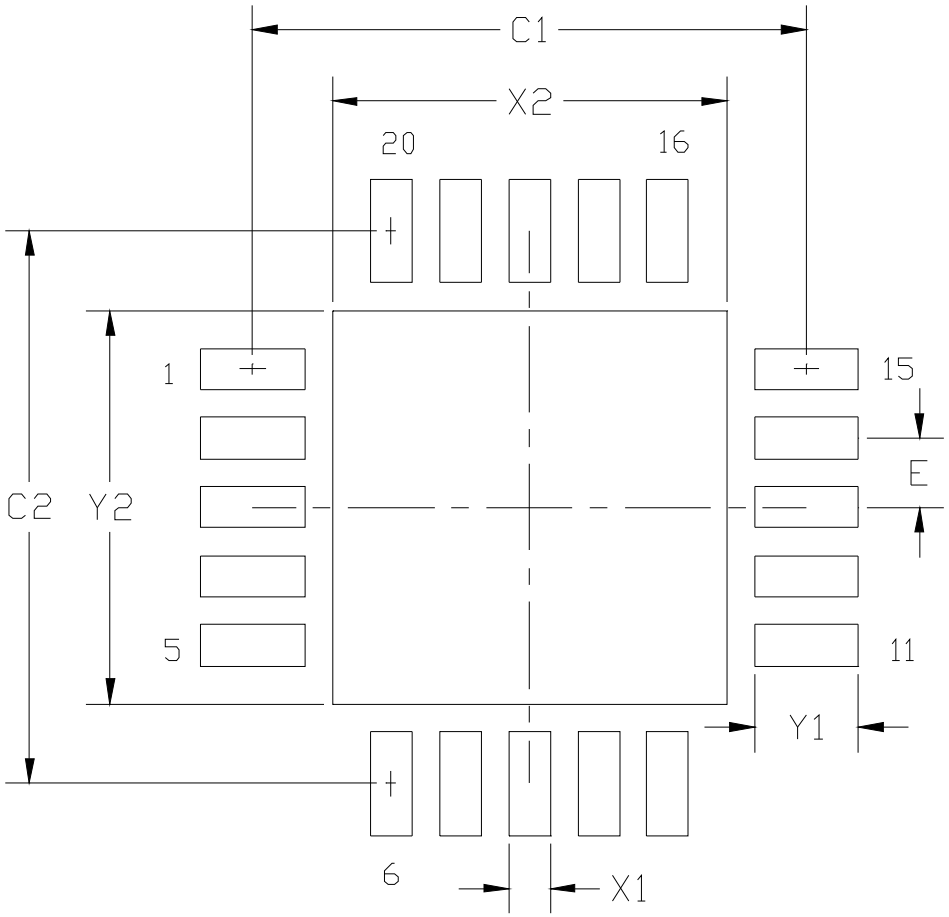


Figure 20. PCB Land Pattern

Table 18. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 REF	
X1	0.20	0.30
X2	2.55	2.65
Y1	0.65	0.75
Y2	2.55	2.65

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

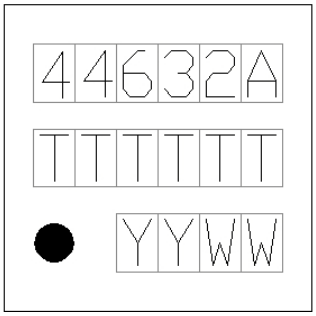
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

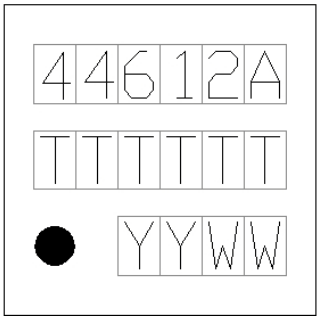
Card Assembly

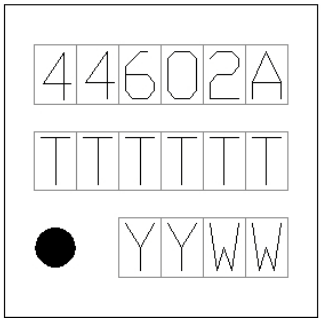
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

15. Top Marking

15.1. Si4463/61/60 Top Marking







15.2. Top Marking Explanation

Mark Method	YAG Laser	
Line 1 Marking	Part Number	44632A = Si4463 Rev 2A[1] 44612A = Si4461 Rev 2A[1] 44602A = Si4460 Rev 2A[1]
Line 2 Marking	TTTTTT = Internal Code	Internal tracking code.[2]
Line 3 Marking	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

Notes:

1. The first letter after the part number is part of the ROM revision. The last letter indicates the firmware revision.
2. The first letter of this line is part of the ROM revision.

Document Change List

Revision 0.1 to Revision 0.2

- Corrected minor typos in text descriptions.
- Updated several parameters in the Electrical Spec Tables.
- Updated sections 4, 5 and 8.6 for better description of Modem and Hardware configuration options, Internal Functional Blocks and Preamble Sense Mode.
- Updated Table 9, “Serial Interface Timing Parameters,” on page 16.
- Updated "12. Ordering Information" on page 46.
- Updated "15. Top Marking" on page 51.

Revision 0.2 to Revision 1.0

- Updated parameters in “1. Electrical Specifications”.
- Minor updates to text descriptions.
- Updated Table 15.
- Updated “11. Pin Descriptions: Si4463/61/60”.

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Si446x/Si4362 RX LNA Matching

1. Introduction

The purpose of this application note is to provide a description of the impedance matching of the RX differential low noise amplifier (LNA) on the Si446x/Si4362 family of RFICs.

It is desired to simultaneously achieve two goals with the matching network:

- Match the LNA input to the antenna source impedance (e.g., 50 Ω)
- Provide a single-ended-to-differential conversion function (i.e., a balun)

The matching procedure outlined in this document provides for achieving the goals listed above.

For those users who are not interested in the theoretical derivation of the match network, but are just concerned with quickly obtaining matching component values, refer to the Summary Tables shown in "4.1.7. Summary Tables of 3-Element Match Network Component Values vs. Frequency" on page 12 and "4.2.7. Summary Tables of 4-Element Match Network Component Values vs. Frequency" on page 19.

Measurements were performed on the Si4461-B0 chip but are applicable to other members of the Si446x family of chips (e.g. Si446x-B1, C0, C1, C2 and the Si4362 chip).

2. Match Network Topology

The LNA on the Si446x/Si4362 family of chips is designed as a differential amplifier and thus has two input pins (RXp and RXn) on the RFIC. It is necessary to design a network that not only provides a conjugate match to the input impedance of the LNA but also provides a balanced-to-unbalanced conversion function (i.e., a balun).

The LNA design is differential and thus the RXp and the RXn input pins may be considered interchangeable. Although the figures in this document may show the matching components connected to the RXp/RXn pins in a certain fashion, the pin connections may be reversed without change in functionality.

Use of two basic matching network topologies will be considered within this application note.

2.1. Three-Element Match Network

The simplest match network that may be fabricated from discrete components is comprised of three discrete elements. Two forms of the 3-element match network may be constructed: one with a highpass filter (HPF) response, and one with a lowpass filter (LPF) response. However, the form with a lowpass filter response is not realizable at all frequencies and input impedances. As a result, only the form with a highpass filter response is discussed within this document.

A 3-element (CR1-LR1-CR2) HPF matching network is shown in Figure 1. This matching network has the virtue of requiring a minimum number of components but results in slightly sub-optimal performance. It is not theoretically possible to achieve a perfectly balanced single-ended-to-differential conversion function with this matching network for input impedances with finite values of R_{LNA}. As will be demonstrated, the waveforms obtained at the RXp and RXn inputs to the RFIC will not be exactly 180° out of phase; the result is a very slight loss in conversion gain in the LNA and a small drop in overall sensitivity of the RFIC. The reduction in performance is typically less than 0.5 dB; many customers may view this as an acceptable trade-off for the reduction in the bill of materials (BOM).

The RXp and RXn inputs of the Si446x/Si4362 RX LNA internally contain high value (~15 kΩ) pull-down resistors to GND. As a result, supplying a DC voltage to these pins is not recommended; use of external AC-coupling to these pins is suggested. This is inherently supplied by capacitor CR2 of Figure 1.

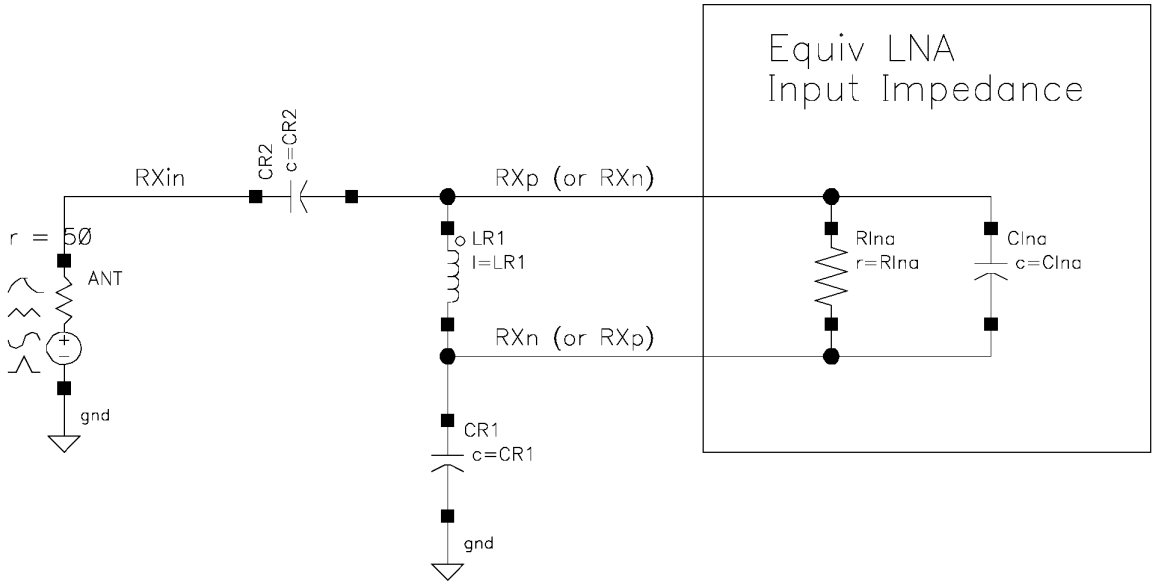

Figure 1. HPF Three-Element Match Network

2.2. Four-Element Match Network

For those customers concerned with obtaining optimal performance, the 4-element match network of Figure 2 is recommended. This match network can provide theoretically perfect phase balance between the RXp and RXn inputs (exactly 180° out-of-phase), thus optimizing LNA conversion gain and receiver sensitivity. The only drawback is the addition of one more component (an inductor) to the BOM. Use of this matching topology is also mandatory for circuit configurations in which the TX and RX paths are tied directly together without use of an RF switch. This is discussed in greater detail in "4.2.8. Use of 4-Element Match Network in Direct Tie Board Configurations" on page 22.

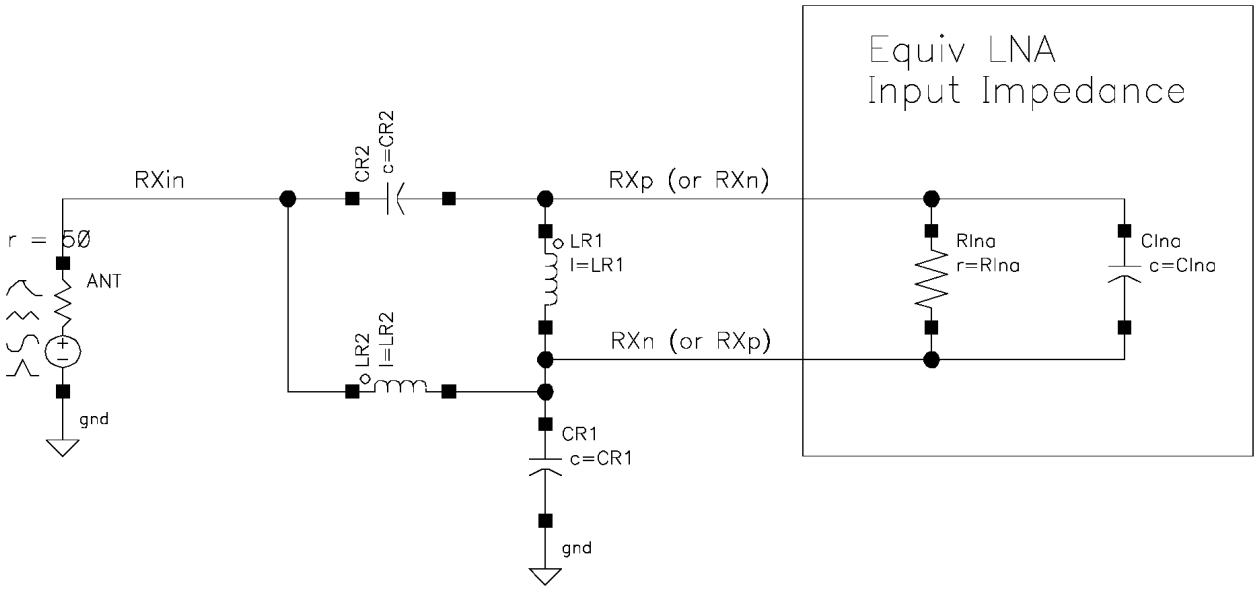

Figure 2. Four-Element Match Network

3. Si446x/Si4362 Differential LNA Input Impedance

Silicon Laboratories has measured the differential input impedance of the Si4461 RX LNA directly at the RXp/RXn input pins of the RFIC, with no matching network. Although this measurement was taken on a Si4461 chip, the data is applicable to other members of the Si446x family of chips and also on the Si4362, as the LNA is similar in all devices.

The plot shown in Figure 3 shows the measured differential input impedance in the RX mode of operation over the 140 to 960 MHz frequency band, with markers placed at various points throughout the frequency range.

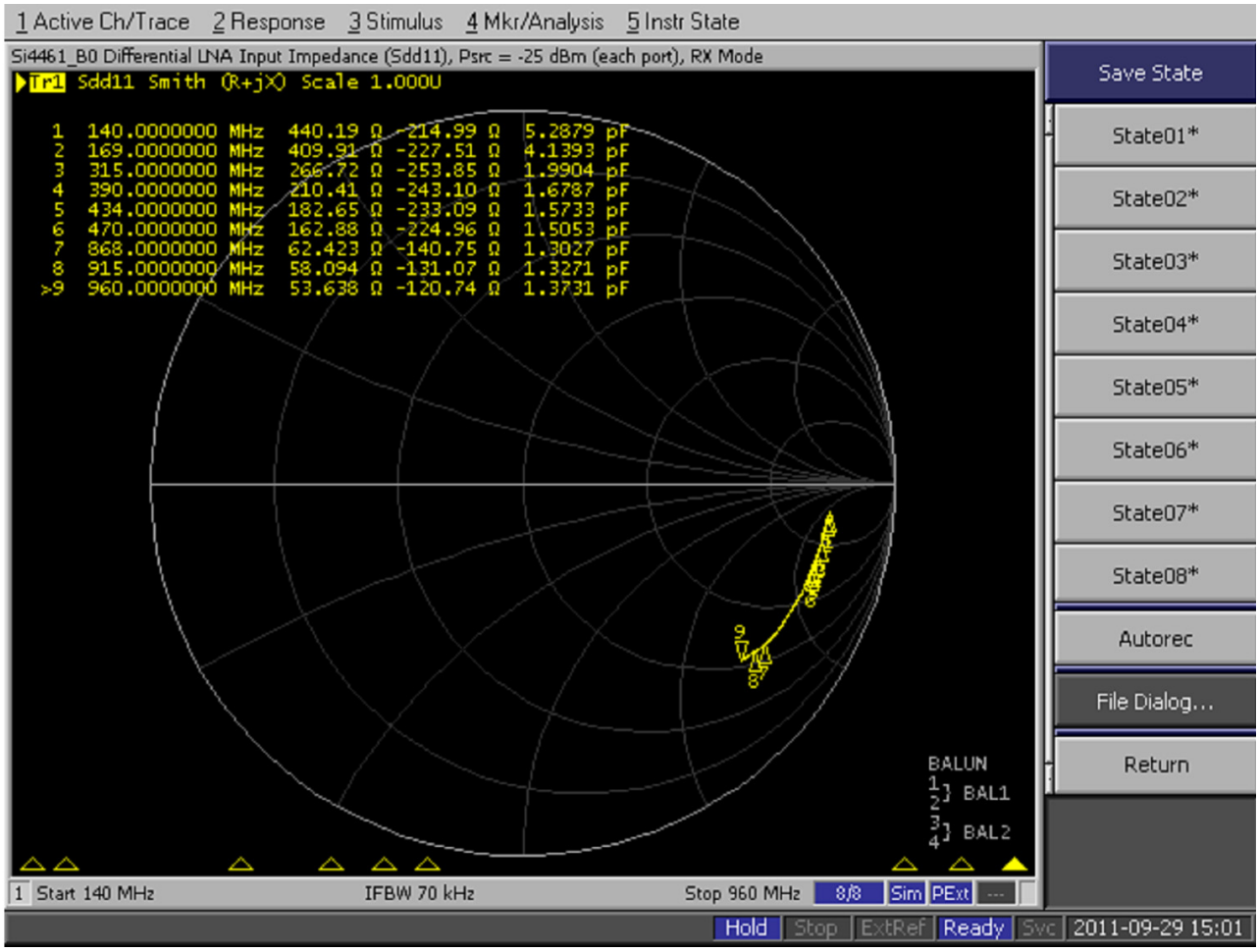

Figure 3. Si446x/Si4362 Differential RX LNA Input Impedance 140-960 MHz (RX Mode)

As can be seen from this curve, at any given single frequency the input impedance of the LNA may be considered as a resistance in parallel with a small amount of capacitance. That is to say, the input impedance of the LNA falls in the capacitive half of the Smith Chart across its entire operating frequency range.

The impedance curve shown in Figure 3 cannot be described by a single fixed value of resistance, placed in parallel with a single fixed value of capacitance. The equivalent values of parallel resistance and capacitance (R_{LNA} and C_{LNA} in Figure 1 and Figure 2) vary as a function of frequency. However, the variation with frequency is not rapid; it is possible to construct a moderately wideband (~100 MHz) matching network by simply designing for the value of R_{LNA} and C_{LNA} in the center of the desired frequency range.

From the differential input impedance values (Z = R + jX) shown in Figure 3, it is necessary to first calculate the equivalent input admittance, where Y = 1/Z = G + jB. It is then a simple matter to calculate the values of the equivalent input resistor and capacitor (i.e., R_{LNA} and C_{LNA} in Table 1) as $R_{LNA} = 1/G$ and $C_{LNA} = B/(2\pi F_{RF})$.

Silicon Laboratories has performed these computational steps on the measured S_{dd11} data of Figure 3, and the resulting equivalent values of R_{LNA} and C_{LNA} are shown in Table 1 as a function of frequency.

Table 1. Equivalent R_{LNA}-C_{LNA} from 140-960 MHz

Freq	R_{LNA}	C_{LNA}
140 MHz	545 Ω	1.02 pF
169 MHz	536 Ω	0.98 pF
200 MHz	530 Ω	0.96 pF
250 MHz	520 Ω	0.94 pF
300 MHz	512 Ω	0.95 pF
315 MHz	509 Ω	0.95 pF
350 MHz	499 Ω	0.95 pF
390 MHz	491 Ω	0.96 pF
400 MHz	488 Ω	0.96 pF
434 MHz	480 Ω	0.97 pF
470 MHz	474 Ω	0.99 pF
500 MHz	467 Ω	1.00 pF
550 MHz	460 Ω	1.01 pF
600 MHz	451 Ω	1.02 pF
650 MHz	437 Ω	1.04 pF
700 MHz	424 Ω	1.05 pF
750 MHz	414 Ω	1.07 pF
800 MHz	402 Ω	1.08 pF
850 MHz	387 Ω	1.09 pF
868 MHz	380 Ω	1.09 pF
900 MHz	362 Ω	1.10 pF
915 MHz	354 Ω	1.11 pF
955 MHz	327 Ω	1.14 pF
960 MHz	325 Ω	1.15 pF

4. LNA Matching Procedure for the Si446x/Si4362 RFIC

Armed with the measured values of unmatched differential input impedance of the Si446x/Si4362 LNA, it is now possible to proceed with constructing a matching network. For demonstration purposes, a frequency of 470 MHz is chosen to illustrate the examples.

4.1. Three-Element Matching Procedure

The matching procedure for the 3-element (CR1-LR1-CR2) HPF match is outlined below.

4.1.1. Step #1: Plot the LNA Input Impedance

The matching procedure begins with the equivalent parallel R_{LNA}-C_{LNA} circuit values obtained from Table 1. At 470 MHz, the equivalent circuit values are found to be R_{LNA} = 474 Ω and C_{LNA} = 0.99 pF. It is useful to plot this value on a Smith Chart, as shown in Figure 4.

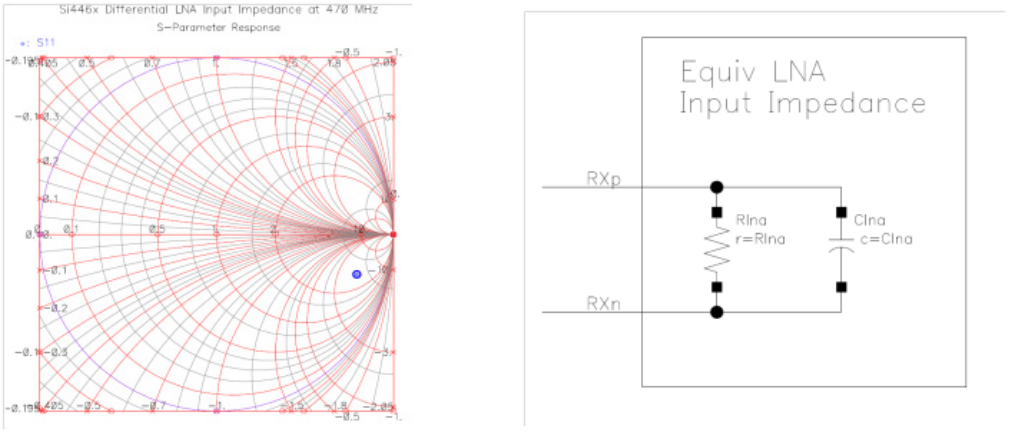

Figure 4. Step #1: Plot LNA Input Impedance

4.1.2. Step #2: Add Parallel Inductance L_{LNA} to Resonate with LNA Capacitance

Although Step #2 may technically be combined with the subsequent Step #3, the design equations are somewhat easier to manipulate if the equivalent LNA input capacitance C_{LNA} is first effectively cancelled (at the frequency of interest) by resonating it with a parallel inductance L_{LNA}.

$$L_{LNA} = \left(\frac{1}{(\omega_{RF})^2 C_{LNA}} \right)$$

Equation 1.

In the design example at 470 MHz, this value of inductance is calculated to be equal to L_{LNA} = 115.83 nH. After this amount of parallel inductance is added across the LNA inputs, the input impedance can be considered to be purely real and of a value equivalent to R_{LNA}. This is shown in Figure 5.

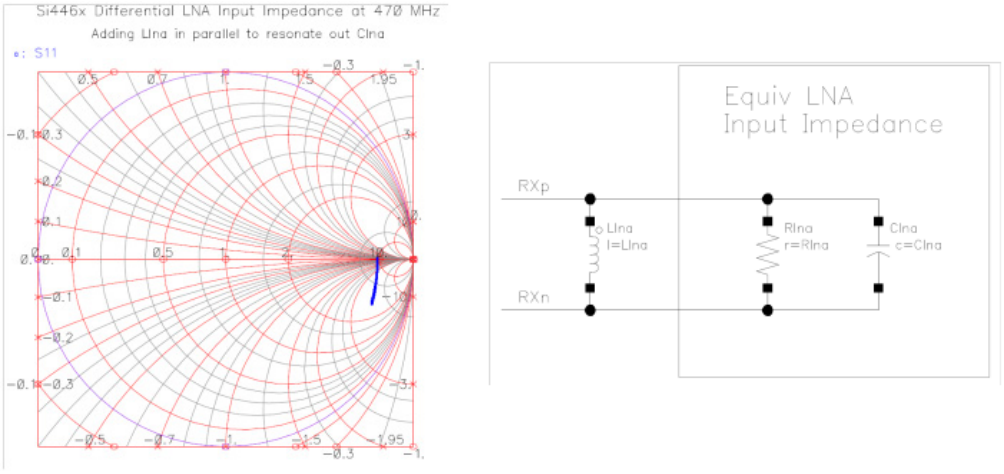

Figure 5. Step #2: Add Parallel Inductance to Resonate C_{LNA}

4.1.3. Step #3: Place Additional Matching Inductance in Parallel with LNA Input

Next an additional matching inductor L_M is placed in parallel with the LNA input network. The value of the inductance should be chosen to further rotate the susceptance on the Smith Chart along a line of constant conductance (in the -jBP direction) until the 50 Ω circle is reached (assuming the antenna source impedance is 50 Ω). The required value of matching inductance L_M is given by the following:

$$L_M = \frac{1}{\omega_{RF}\sqrt{\left(\frac{1}{50\Omega \times R_{LNA}}\right) - \left(\frac{1}{R_{LNA}}\right)^2}}$$

Equation 2.

Note: The mathematical derivations for all equations within this document are not shown. The full derivations are contained within a Mathcad worksheet developed by the Silicon Laboratories Application Team; this worksheet is available from Silicon Laboratories upon request.

Using this equation, or by employing graphical methods on the Smith Chart, the additional parallel matching inductance required to reach the 50 Ω circle is found to be L_M = 55.12 nH.

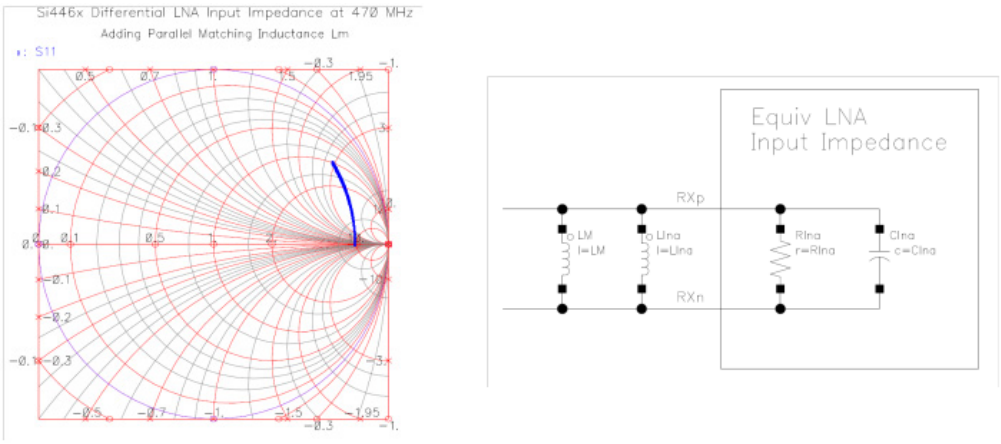

Figure 6. Step #3: Add Parallel Matching Inductance L_M

As L_{LNA} and L_M are in parallel with each other, they may be combined into one equivalent inductance LR1.

$$L_{R1} = \frac{L_{LNA}L_M}{L_{LNA} + L_M}$$

Equation 3.

Using this equation, it is quickly determined that a single inductor of value LR1 = 37.35 nH may be used in place of L_{LNA} and L_M.

4.1.4. Step #4: Determine Total Amount of Series Capacitive Reactance

It is next necessary to determine the total amount of series capacitive reactance ($-jX_{CTOTAL}$) required to match this point to 50 Ω. That is to say, it is desired to rotate the reactance along a line of constant resistance until arriving at the center of the Smith Chart. The required value of total capacitance is given by the following:

$$C_{TOTAL} = \frac{1}{\omega_{RF} \times 50\Omega \sqrt{\left(\frac{R_{LNA}}{50\Omega}\right) - 1}}$$

Equation 4.

Using this equation, or by employing graphical methods on the Smith Chart, the total series capacitance required to reach the 50 Ω origin of the Smith Chart is found to be C_{TOTAL} = 2.33 pF.

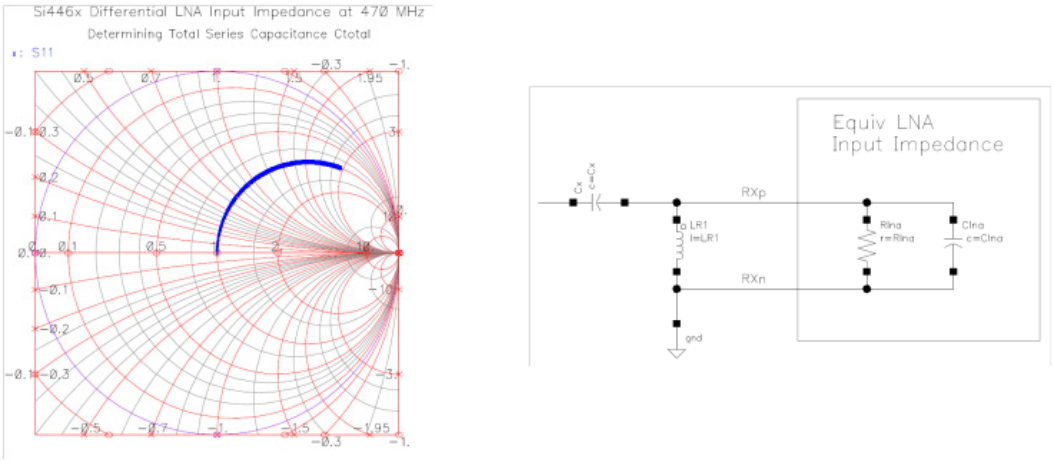

Figure 7. Step #4: Determine TOTAL Series Capacitive Reactance

4.1.5. Step #5: Allocate Total Series Capacitance Between CR1 and CR2

The final step is to properly allocate this total required series capacitive reactance between CR1 and CR2.

There are an infinite number of possible matching networks which achieve a perfect match to 50 Ω. However, only one of these solutions also achieves the best possible equal-amplitude-with-180°-phase relationship between the waveforms at the RXp / RXn inputs.

For example, it would be possible to set the value of CR1 so large that it provides essentially 0 Ω of capacitive reactance and essentially ac-shorts the RXn pin to GND. Under this condition, it would be possible to set the value of CR2 to provide all of the required series capacitive reactance (determined in Step #4 above) and still achieve a perfect match to 50 Ω. However, it is clear that the waveforms at the RXp and RXn nodes would not be balanced. The voltage at the RXn pin in this scenario would be zero (ac-shorted to GND by CR1). From an AC standpoint, this is equivalent to the schematic shown in Figure 7.

To properly allocate the total series capacitive reactance between CR1 and CR2, the required relationship between LR1 and CR1 must first be recognized. It is desirable for the voltages at the RXp and RXn pins to be equal in amplitude but opposite in phase, and thus the voltage developed "across" the parallel network of LR1-R_{LNA}-C_{LNA} must be twice the amplitude (and of opposite polarity) as the voltage that exists at the RXn node.

A portion of the parallel inductance LR1 is simply used to resonate out the capacitance C_{LNA}. As shown in Steps #2 and #3, it was useful to consider the inductance LR1 as consisting of two inductors in parallel: L_{LNA} and L_M, as re-drawn in Figure 8.

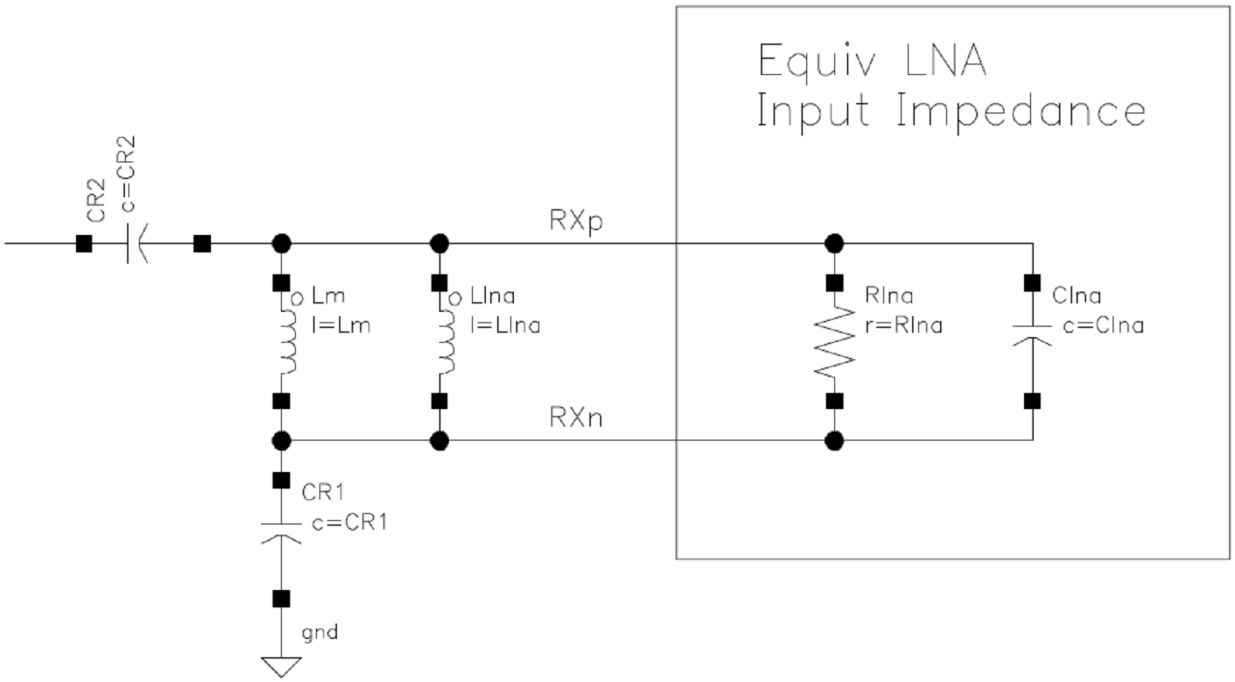

Figure 8. Resolving LR1 into Two Parts

The values of these two inductances have previously been determined to be L_{LNA} = 115.83 nH and L_M = 55.12 nH. As the inductance L_{LNA} is simply used to resonate with C_{LNA} at the desired frequency of operation, the match network may thus be re-drawn as shown in Figure 9.

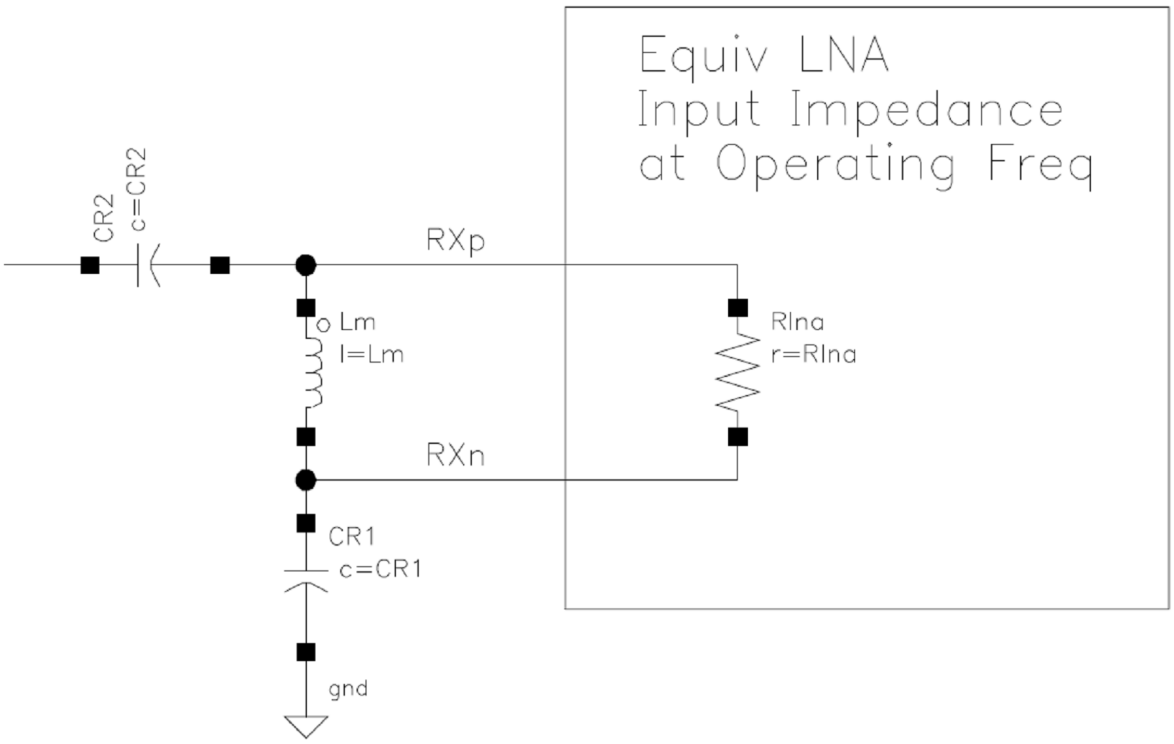

Figure 9. Equivalent Match Network at Operating Frequency

The voltage across L_M is desired to be twice the amplitude (and opposite in phase) to the voltage across CR1. Temporarily ignoring the effects of R_{LNA}, the following relationship is obtained:

$$X_{LM} = 2 \times X_{CR1}$$

Equation 5.

As the required value of inductance L_M has already been determined, the required value for CR1 follows immediately from the previously-derived equation for L_M.

$$CR1 = 2 \times \frac{\sqrt{\left(\frac{R_{LNA}}{50\Omega}\right) - 1}}{\omega_{RF} R_{LNA}}$$

Equation 6.

Using this equation, the value for this capacitor is determined to be CR1 = 4.16 pF. It is then a simple matter to allocate the remaining portion of total required series capacitive reactance to CR2.

$$CR2 = \frac{1}{\left(\frac{1}{C_{TOTAL}}\right) - \left(\frac{1}{CR1}\right)}$$

Equation 7.

From this equation, the value for the remaining capacitor is quickly found to be CR2 = 5.27 pF. Thus all of the components in the 3-element match network have been determined:

- CR2 = 5.27 pF
- LR1 = 37.35 nH
- CR1 = 4.16 pF

4.1.6. Phase Imbalance of RXp/RXn Signals

If the input impedance of the LNA were infinite (R_{LNA} =), this procedure would result in equal-amplitude perfectly-balanced (180° out-of-phase) waveforms at the RXp and RXn nodes. However, a finite value for R_{LNA} has the effect of shifting the phase of the signal developed across the parallel combination of LR1- R_{LNA} -C_{LNA}; thus the voltage developed at the RXp node can never be exactly 180° out-of-phase with respect to the voltage at the RXn node. This effect may be clearly seen in the simulated results of Figure 10; the differential voltages are equal in amplitude but not quite opposite in phase.

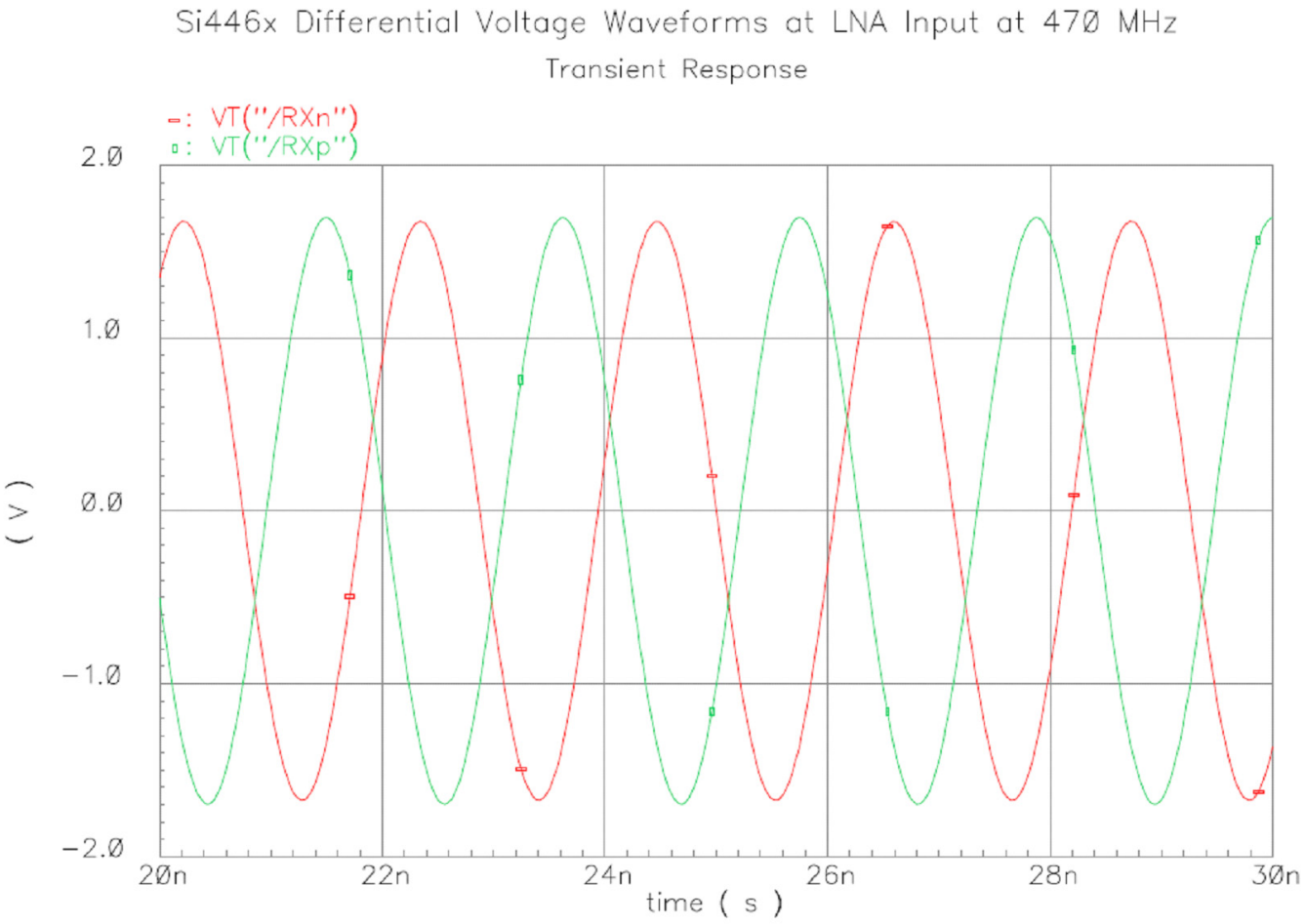

Figure 10. Differential Voltage Waveforms at LNA Input (3-Element Match)

As stated earlier, the 3-element match network provides slightly less-than-optimal performance when compared to a perfect balun. However, the difference is usually quite small (< 0.5 dB degradation) and is often acceptable.

4.1.7. Summary Tables of 3-Element Match Network Component Values vs. Frequency

Some users may not be greatly interested in the theoretical development of the matching network, but are concerned only with quickly obtaining a set of component values for a given desired frequency of operation. For those users, the resulting calculated component values for the 3-element match network for multiple frequencies across the operating range of the Si446x/Si4362 RFIC are summarized below. The calculations in this table assume the antenna source impedance is Z_{ANT} = 50 + j0 Ω.

Table 2. 3-Element Match Network Component Values (Calculated)

Freq	R_{LNA}	C_{LNA}	CR1	LR1	CR2
140 MHz	545 Ω	1.02 pF	13.12 pF	170. 48 nH	16.07 pF
169 MHz	536 Ω	0.98 pF	10.96 pF	137.41 nH	13.47 pF
200 MHz	530 Ω	0.96 pF	9.30 pF	112.90 nH	11.47 pF
250 MHz	520 Ω	0.94 pF	7.51 pF	86.25 nH	9.30 pF
300 MHz	512 Ω	0.95 pF	6.30 pF	68.71 nH	7.83 pF
315 MHz	509 Ω	0.95 pF	6.02 pF	64.56 nH	7.49 pF
350 MHz	499 Ω	0.95 pF	5.46 pF	56.20 nH	6.83 pF
390 MHz	491 Ω	0.96 pF	4.94 pF	48.59 nH	6.20 pF
400 MHz	488 Ω	0.96 pF	4.83 pF	46.88 nH	6.07 pF
434 MHz	480 Ω	0.97 pF	4.48 pF	41.83 nH	5.66 pF
470 MHz	474 Ω	0.99 pF	4.16 pF	37.37 nH	5.28 pF
500 MHz	467 Ω	1.00 pF	3.94 pF	34.18 nH	5.01 pF
550 MHz	460 Ω	1.01 pF	3.60 pF	29.75 nH	4.61 pF
600 MHz	451 Ω	1.02 pF	3.33 pF	26.18 nH	4.28 pF
650 MHz	437 Ω	1.04 pF	3.12 pF	23.10 nH	4.05 pF
700 MHz	424 Ω	1.05 pF	2.93 pF	20.54 nH	3.84 pF
750 MHz	414 Ω	1.07 pF	2.77 pF	18.39 nH	3.65 pF
800 MHz	402 Ω	1.08 pF	2.63 pF	16.57 nH	3.49 pF
850 MHz	387 Ω	1.09 pF	2.51 pF	14.97 nH	3.39 pF
868 MHz	380 Ω	1.09 pF	2.48 pF	14.44 nH	3.37 pF
900 MHz	362 Ω	1.10 pF	2.44 pF	13.47 nH	3.37 pF
915 MHz	354 Ω	1.11 pF	2.42 pF	13.04 nH	3.38 pF
955 MHz	327 Ω	1.14 pF	2.40 pF	11.85 nH	3.45 pF
960 MHz	325 Ω	1.15 pF	2.39 pF	11.73 nH	3.45 pF

The above analysis assumes use of ideal discrete components in the matching network. However, surface-mount 0603- or 0402-size components themselves contain parasitic elements that modify their effective values at the frequency of interest. Additionally, the analysis presented above does not make allowance for any PCB parasitics, such as trace inductance, component pad capacitance, etc. Furthermore, it is convenient to use the nearest-available 5% or 10% component value; the component values shown above represent results of exact mathematical calculations.

As a result, it will almost certainly be necessary to “tweak” the final matching values for a specific application and board layout. The above component values should be used as starting points, and the values modified slightly to zero-in on the best match to the antenna source impedance (e.g., 50 Ω), and the best RX sensitivity.

Silicon Laboratories has empirically determined the optimum matching network values at a variety of frequencies, using RF Test Boards designed by (and available from) Silicon Laboratories. Wire-wound inductors (Murata LQW15A 0402-series and LQW18A 0603-series) were used in all of these matching examples. Multi-layer inductors (such as Murata LQG15HS 0402-series) may also be used; however, the insertion loss of the match may be increased slightly due to the higher loss of these inductors. By comparing the empirical values of Table 3 with the calculated values of Table 2, the reader may observe that the component values are in close agreement at frequencies below 500 MHz. However, somewhat larger deviations in value occur at higher frequencies, primarily due to the unmodeled parasitic effects of the PCB traces and discrete components. As mentioned previously, the calculated matching component values of Table 2 should be used as a starting point and adjusted for best performance.

Table 3. 3-Element Match Network Component Values (Optimized)

Freq	R_{LNA}	C_{LNA}	CR1	LR1	CR2
169 MHz	536 Ω	0.98 pF	10.0 pF	150 nH	13.0 pF
315 MHz	509 Ω	0.95 pF	5.6 pF	68 nH	7.5 pF
390 MHz	491 Ω	0.96 pF	4.7 pF	51 nH	6.2 pF
434 MHz	480 Ω	0.97 pF	4.3 pF	43 nH	5.6 pF
470 MHz	474 Ω	0.99 pF	3.9 pF	39 nH	5.1 pF
868 MHz	380 Ω	1.09 pF	2.0 pF	18 nH	3.0 pF
915 MHz	354 Ω	1.11 pF	1.8 pF	16 nH	3.0 pF
955 MHz	327 Ω	1.14 pF	1.8 pF	15 nH	2.7 pF

A 3-element RX match at 470 MHz was built and tested, using CR1=3.9 pF, LR1=39 nH, and CR2=5.1 pF. The measured input impedance (S11) is shown in Figure 11.

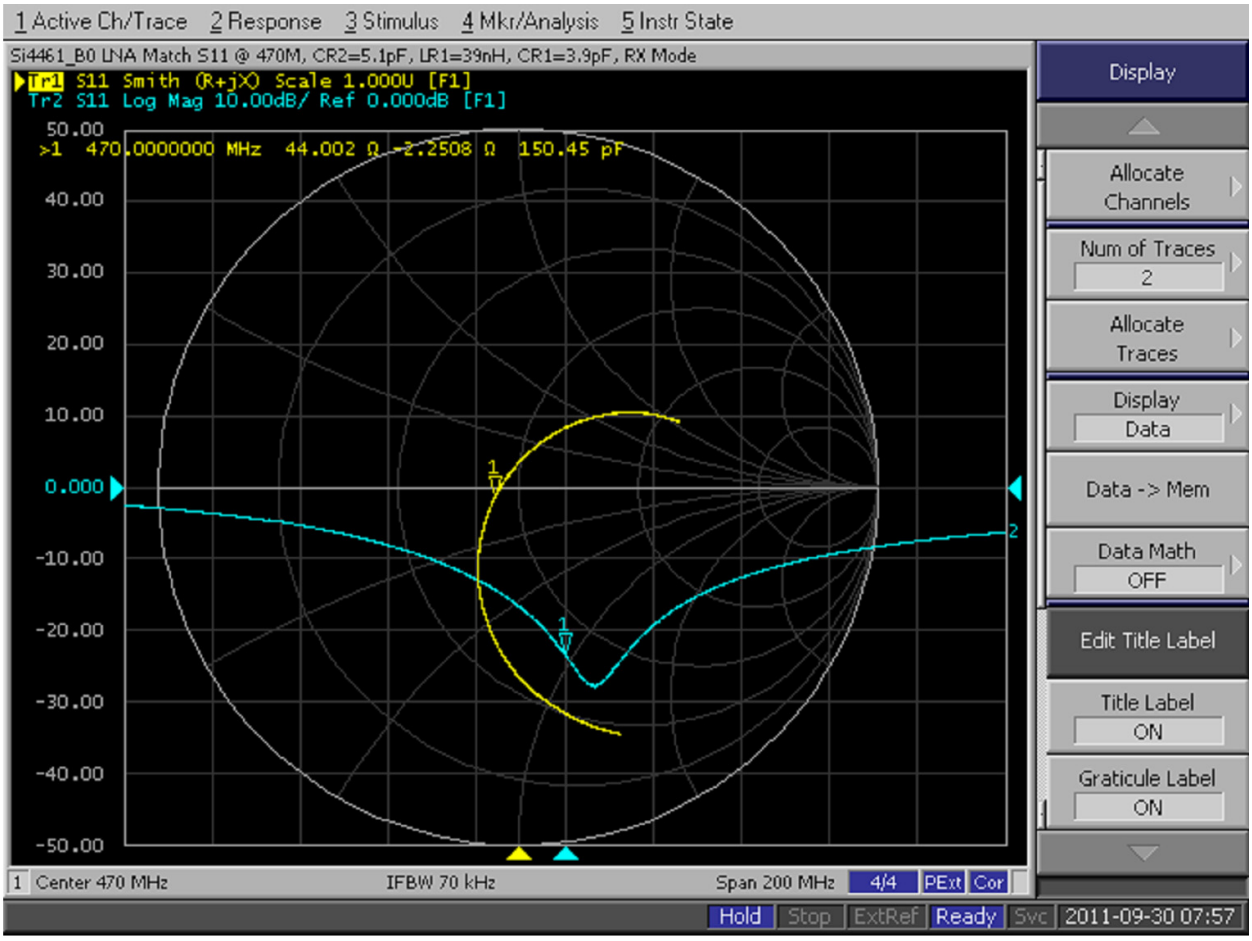

Figure 11. Input Impedance of 3-Element Match at 470 MHz

4.2. Four-Element Matching Procedure

As discussed previously, it is possible to achieve a theoretically-perfect match with the 4-element match network shown in Figure 2. The complete mathematical derivation of the equations for the required component values is beyond the scope of this application note; a Mathcad worksheet containing the complete derivation is available from Silicon Laboratories upon request.

The matching procedure for the 3-element network was readily understood and explained by plotting each step on a Smith Chart. This graphical approach is somewhat less intuitive for the 4-element matching procedure. Therefore, a combination of graphical and textual descriptions of the main steps in the mathematical derivation is presented, along with the important equations resulting from following these steps.

4.2.1. Step #1: Voltage at the RXn Node (V_{RXn})

If a network is created to successfully match to a purely-real input impedance of Z_{IN} = 50 Ω, the input current I_{IN} will also be purely real (arbitrarily assuming an input voltage from the source generator V_{IN} of unity magnitude and zero phase). This input current passes through capacitor CR1 to develop the voltage at the RXn node (V_{RXn}). It is apparent that this voltage V_{RXn} exhibits a –90° phase shift with respect to the input current I_{IN}, due to the capacitive reactance of CR1.

4.2.2. Step #2: Voltage at the RXp Node (V_{RXp})

The voltage at the RXp node (V_{RXp}) is desired to be equal in amplitude to V_{RXn} but opposite in phase. For this condition to be satisfied, the voltage *across* the LNA input pins must be *twice* the amplitude of V_{RXn}, as well as exactly opposite in phase. That is to say, if the phase of V_{RXn} is –90°, the phase of V_{RXp} must be +90°.

4.2.3. Step #3: Splitting the Input Current

Although the phase of the voltage across the LNA input pins must be +90°, the input impedance of the LNA network is not purely inductive (unless $R_{LNA} = \infty$). Thus, for the voltage across the LNA network to be purely reactive, the phase of the current through the LNA network must compensate for the phase shift introduced by R_{LNA}. As a result, it is necessary that the current through the LNA network be different from the current through CR1.

Thus the purpose of inductor LR2 is to split the input current I_{IN} into two different components, with the current passing through the LNA network being of the appropriate phase to produce a voltage of opposite phase to V_{RXn}.

4.2.4. Equations for Component Values

Following these derivational steps, it is possible to obtain the following set of design equations for the necessary component values.

$$LR2 = \frac{\sqrt{Re(Z_{ANT}) \times R_{LNA}}}{\omega_{RF}} = \frac{\sqrt{50\Omega \times R_{LNA}}}{\omega_{RF}}$$

Equation 8.

$$CR2 = \frac{1}{(\omega_{RF})^2 LR2}$$

Equation 9.

$$CR1 = 2 \times CR2$$

Equation 10.

$$L_{LNA} = \frac{1}{(\omega_{RF})^2 C_{LNA}}$$

Equation 11.

$$L_M = 2 \times LR2$$

Equation 12.

$$LR1 = \frac{L_{LNA} L_M}{L_{LNA} + L_M}$$

Equation 13.

Continuing the design example at 470 MHz, the component values for a 4-element match network are calculated as follows:

- CR1 = 4.40 pF
- LR1 = 54.87 nH
- CR2 = 2.20 pF
- LR2 = 52.13 nH

4.2.5. Phase Balance of RXp/RXn Signals

It was previously stated that an advantage of the 4-element match network was the ability to achieve perfect phase balance (180 degrees) between the RXp and RXn input nodes. This effect may be clearly seen in Figure 12; the differential voltages are now both equal in amplitude *and* perfectly opposite in phase.

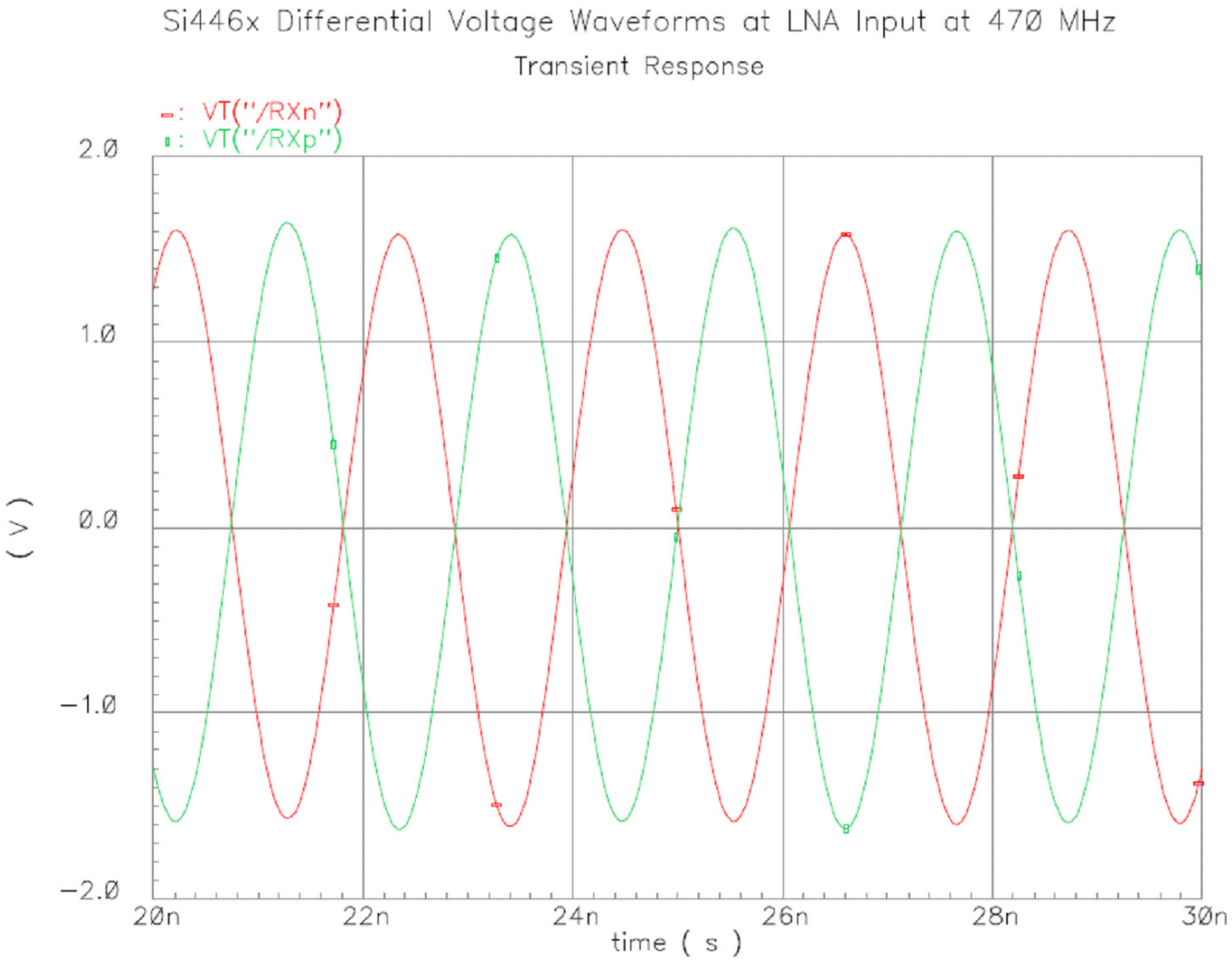

Figure 12. Differential Voltage Waveforms at LNA Input (4-Element Match)

4.2.6. Graphical Interpretation of 4-Element Match

It is informative to consider a graphical interpretation of the 4-element match using a Smith Chart. In practicality, it is simpler to use the design equations to obtain the required component values. However, the reader may gain insight into the behavior and functionality of the match by tracing its impedance progression on a Smith Chart.

The investigation is simplified if the LNA input impedance is temporarily considered to be purely real (i.e., C_{LNA} = 0 pF). Although this situation does not exist in practice, the input capacitance of the LNA may be easily canceled at the desired frequency of operation by placing a parallel inductance L_{LNA} across the RXp/RXn input pins, as discussed in "4.1.2. Step #2: Add Parallel Inductance L_{LNA} to Resonate with LNA Capacitance" on page 6. After cancellation of the input capacitance C_{LNA}, the “starting” point on the Smith Chart for the matching procedure then becomes $Z_{LNA} = R_{LNA} + j0 = R_{LNA}$.

If considering ***only*** the input impedance (while ignoring differential signal balance), the entire match circuitry may be redrawn as shown in Figure 13. While this schematic does not represent the ***physical*** arrangement of

components of the match, its input impedance is identical to that of the actual circuit. Furthermore, representation of the match network in this “ladder” form simplifies plotting the progression of the impedance match on a Smith Chart.

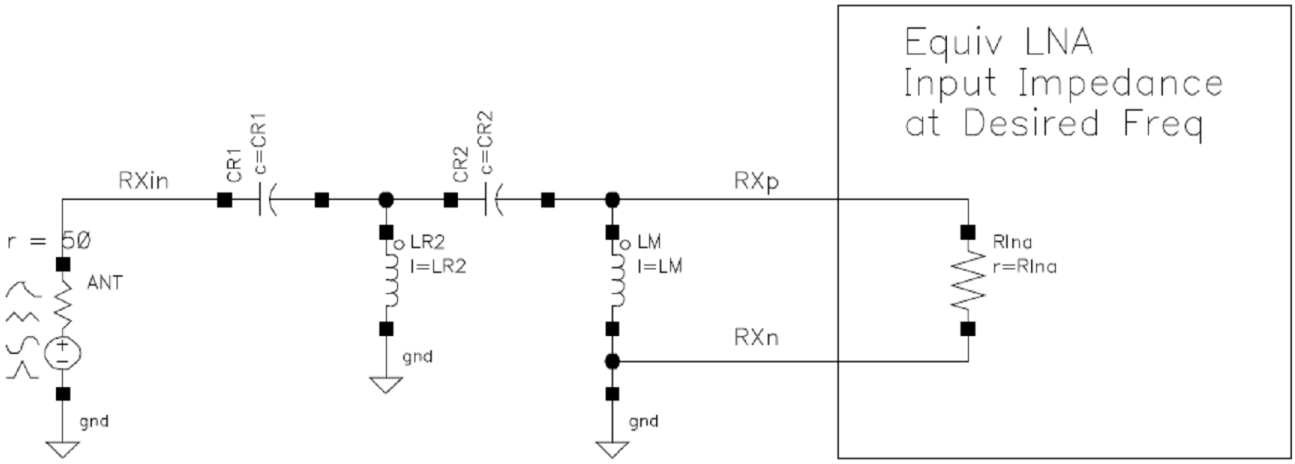

Figure 13. 4-Element Match (re-drawn in ladder form)

Equation 8 may be manipulated as follows:

$$X_{LR2} = \omega_{RF} LR2 = \sqrt{Re(Z_{ANT}) \times R_{LNA}} = \sqrt{50\Omega \times R_{LNA}}$$

Equation 14.

This equation states that the inductive reactance of LR2 is equal to the geometric mean of the antenna source impedance (e.g., 50 Ω) and the real part of the LNA input impedance R_{LNA}. Equation 9 states that the reactance of CR2 is equal to the reactance of LR2 (i.e., together they resonate at the desired frequency of operation). Equation 12 then further indicates that the matching inductor L_M is equal to 2 x LR2, while indicates that CR1 is equal to 2 x CR2.

It is informative to consider the Q-factors formed by R_{LNA} in parallel with L_M, and by CR1 in series with R_{ANT}.

$$Q_{LNA} = \frac{R_{LNA}}{X_{LM}} = \frac{R_{LNA}}{\omega_{RF} L_M} = \frac{R_{LNA}}{2\omega_{RF} L_{R2}} = \frac{R_{LNA}}{2 \times \sqrt{50\Omega \times R_{LNA}}} = \left(\frac{1}{2}\right)\sqrt{\frac{R_{LNA}}{50\Omega}}$$

Equation 15.

$$Q_{ANT} = \frac{X_{CR1}}{R_{ANT}} = \frac{X_{CR2}}{2 \times R_{ANT}} = \frac{X_{LR2}}{2 \times R_{ANT}} = \frac{\sqrt{50\Omega \times R_{LNA}}}{2 \times 50\Omega} = \left(\frac{1}{2}\right)\sqrt{\frac{R_{LNA}}{50\Omega}}$$

Equation 16.

It is well known that the locus of all impedance points with the same Q-factor describes an ellipse on a Smith Chart. These last two equations indicate that the impedance at two of the internal nodes within the 4-element match share the same Q-factor and thus fall upon the same ellipse (constant-Q curve) on a Smith Chart. This is illustrated in the impedance progression plot of Figure 14.

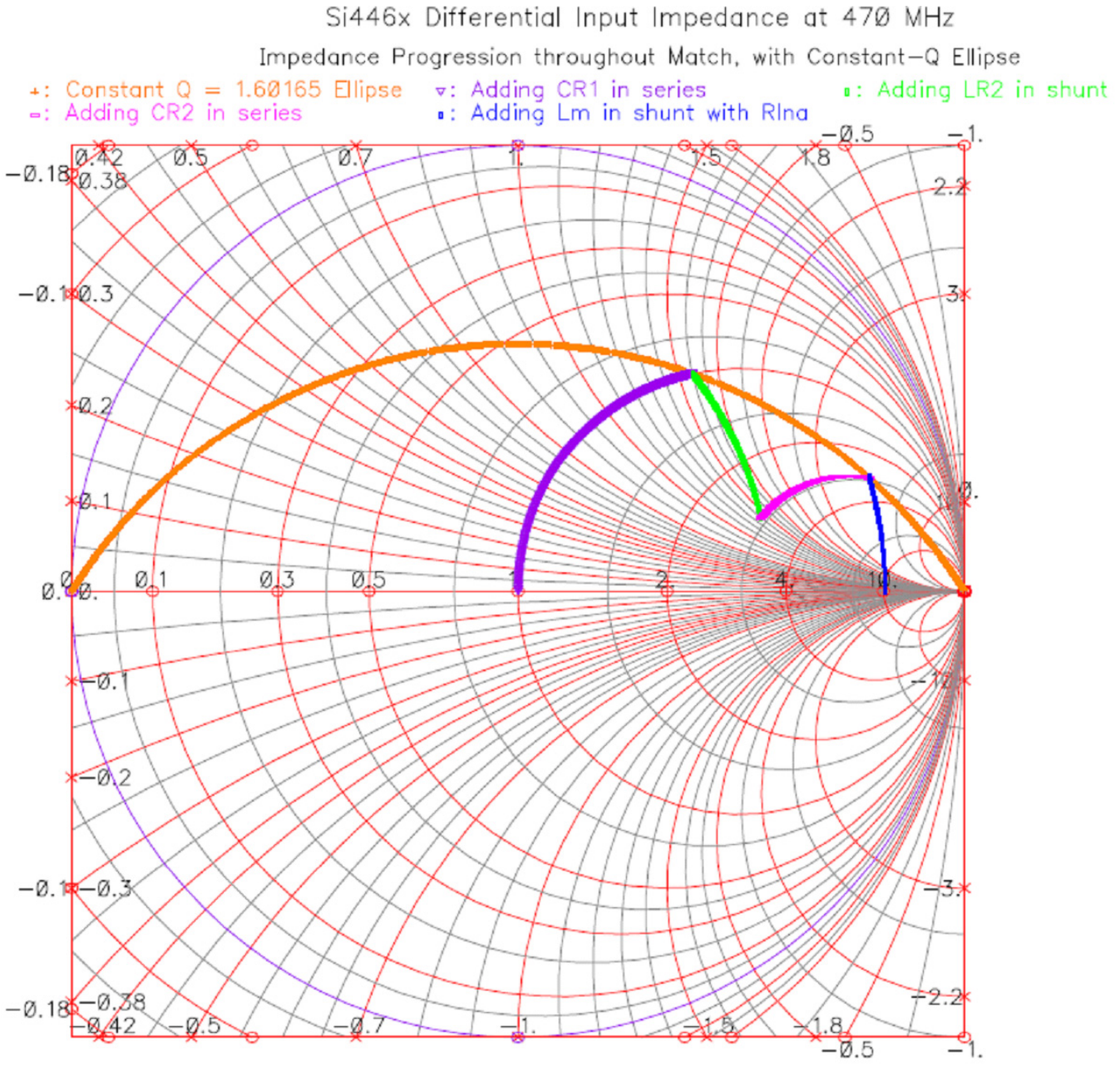

Figure 14. Impedance Match Progression Plot (with constant-Q Ellipse)

In this plot, the impedance path on the Smith Chart is traced as each successive component in the match is added. The plot begins on the purely-real axis at $Z = R_{LNA} + j0$. The dark blue curve describes the change in impedance as the matching inductor L_M is added in parallel with R_{LNA}, the pink curve describes subsequently adding on series capacitor CR2, and so on. Using the component values in the design example at 470 MHz, the calculated LNA Q value is ~1.6 as shown in Equation 17.

$$Q_{LNA} = \left(\frac{1}{2}\right)\sqrt{\frac{R_{LNA}}{50\Omega}} = \left(\frac{1}{2}\right)\sqrt{\frac{513\Omega}{50\Omega}} = 1.60165$$

Equation 17.

As predicted in the earlier discussion, it is found that the endpoints of two of the segments in this impedance progression plot fall directly upon the Q = 1.60165 elliptical curve.

This then suggests a graphical solution to the problem of constructing a 4-element match network:

- Plot both R_{LNA} and R_{ANT} on the Smith Chart
- Calculate Q = (1/2) * SQRT(R_{LNA} / R_{ANT})
- Construct a constant-Q ellipse on the Smith Chart with this value of Q
- Plot the intersection of the constant-R_{ANT} impedance circle (e.g., 50 circle) with this ellipse
- Plot the intersection of the constant-G_{LNA} admittance circle with this ellipse
- These four points (R_{ANT}, R_{LNA}, two Q-intersection points) describe four of the five segment endpoints of the impedance progression plot
- The fifth endpoint is graphically obtained from the segments (series CR2, shunt LR2) that must be traversed to connect the two constant-Q points.

The corresponding component values are readily obtained by denormalizing each shunt or series path traversed on the Smith Chart.

Note: Using the equations is easier.

4.2.7. Summary Tables of 4-Element Match Network Component Values vs. Frequency

Some users may not be greatly interested in the theoretical development of the matching network, but are concerned only with quickly obtaining a set of component values for a given desired frequency of operation. For those users, the resulting calculated component values for the 4-element match network for multiple frequencies across the operating range of the Si446x/Si4362 RFIC are summarized in Table 4. The calculations in Table 4 assume the antenna source impedance is Z_{ANT} = 50 + j0 Ω.

Table 4. 4-Element Match Network Component Values (Calculated)

Freq	RLNA	CLNA	CR1	LR1	CR2	LR2
140 MHz	545 Ω	1.02 pF	13.77 pF	289.69 nH	6.89 pF	187.69 nH
169 MHz	536 Ω	0.98 pF	11.51 pF	230.20 nH	5.75 pF	154.15 nH
200 MHz	530 Ω	0.96 pF	9.78 pF	186.19 nH	4.89 pF	129.55 nH
250 MHz	520 Ω	0.94 pF	7.90 pF	138.84 nH	3.95 pF	102.63 nH
300 MHz	512 Ω	0.95 pF	6.63 pF	108.07 nH	3.32 pF	84.88 nH
315 MHz	509 Ω	0.95 pF	6.34 pF	100.91 nH	3.17 pF	80.58 nH
350 MHz	499 Ω	0.95 pF	5.76 pF	86.58 nH	2.88 pF	71.85 nH
390 MHz	491 Ω	0.96 pF	5.21 pF	73.63 nH	2.60 pF	63.96 nH
400 MHz	488 Ω	0.96 pF	5.09 pF	70.77 nH	2.55 pF	62.15 nH
434 MHz	480 Ω	0.97 pF	4.73 pF	62.31 nH	2.37 pF	56.82 nH
470 MHz	474 Ω	0.99 pF	4.40 pF	54.87 nH	2.20 pF	52.13 nH

Table 4. 4-Element Match Network Component Values (Calculated) (Continued)

Freq	RLNA	CLNA	CR1	LR1	CR2	LR2
500 MHz	467 Ω	1.00 pF	4.16 pF	49.72 nH	2.08 pF	48.66 nH
550 MHz	460 Ω	1.01 pF	3.82 pF	42.57 nH	1.91 pF	43.87 nH
600 MHz	451 Ω	1.02 pF	3.53 pF	36.93 nH	1.77 pF	39.85 nH
650 MHz	437 Ω	1.04 pF	3.31 pF	32.16 nH	1.66 pF	36.18 nH
700 MHz	424 Ω	1.05 pF	3.12 pF	28.23 nH	1.56 pF	33.09 nH
750 MHz	414 Ω	1.07 pF	2.95 pF	24.97 nH	1.48 pF	30.52 nH
800 MHz	402 Ω	1.08 pF	2.81 pF	22.27 nH	1.40 pF	28.22 nH
850 MHz	387 Ω	1.09 pF	2.69 pF	19.93 nH	1.35 pF	26.03 nH
868 MHz	380 Ω	1.09 pF	2.66 pF	19.17 nH	1.33 pF	25.27 nH
900 MHz	362 Ω	1.10 pF	2.63 pF	17.78 nH	1.31 pF	23.80 nH
915 MHz	354 Ω	1.11 pF	2.62 pF	17.16 nH	1.31 pF	23.14 nH
955 MHz	327 Ω	1.14 pF	2.61 pF	15.47 nH	1.30 pF	21.32 nH
960 MHz	325 Ω	1.15 pF	2.60 pF	15.30 nH	1.30 pF	21.15 nH

Similar to the 3-element match network, it will almost certainly be necessary to “tweak” the final matching values for a specific application and board layout due to parasitic effects of PCB traces and non-ideal discrete components. The above component values should be used as starting points, and the values modified slightly to zero-in on the best match to the antenna source impedance (e.g., 50 Ω), and the best RX sensitivity.

Silicon Laboratories has empirically determined the optimum matching network values at a variety of frequencies, using RF Test Boards designed by (and available from) Silicon Laboratories. Wire-wound inductors (Murata LQW15A 0402-series and LQW18A 0603-series) were used in all of these matching examples. Multi-layer inductors (such as Murata LQG15HS 0402-series) may also be used; however, the insertion loss of the match may be increased slightly due to the higher loss of these inductors. By comparing the empirical values of Table 5 with the calculated values of Table 4, the reader may observe that the component values are in close agreement at frequencies below 500 MHz. However, somewhat larger deviations in value occur at higher frequencies, primarily due to the unmodeled parasitic effects of the PCB traces and discrete components. As mentioned previously, the calculated matching component values of Table 4 should be used as a starting point and adjusted for best performance.

Table 5. 4-Element Match Network Component Values (Optimized)

Freq	R_{LNA}	C_{LNA}	CR1	LR1	CR2	LR2
169 MHz	536 Ω	0.98 pF	12.0 pF	220 nH	6.2 pF	150 nH
315 MHz	509 Ω	0.95 pF	6.2 pF	100 nH	3.0 pF	82 nH
390 MHz	491 Ω	0.96 pF	5.1 pF	75 nH	2.4 pF	62 nH
434 MHz	480 Ω	0.97 pF	4.7 pF	62 nH	2.2 pF	56 nH
470 MHz	474 Ω	0.99 pF	3.9 pF	56 nH	2.2 pF	51 nH
868 MHz	380 Ω	1.09 pF	3.0 pF	20 nH	1.0 pF	24 nH
915 MHz	354 Ω	1.11 pF	3.0 pF	18 nH	1.0 pF	22 nH
955 MHz	325 Ω	1.15 pF	2.4 pF	18 nH	0.9 pF	22 nH

A 4-element RX match at 470 MHz was built and tested, using CR1=3.9pF, LR1=56nH, CR2=2.2pF, and LR2=51nH. The measured input impedance (S11) is shown in Figure 15.

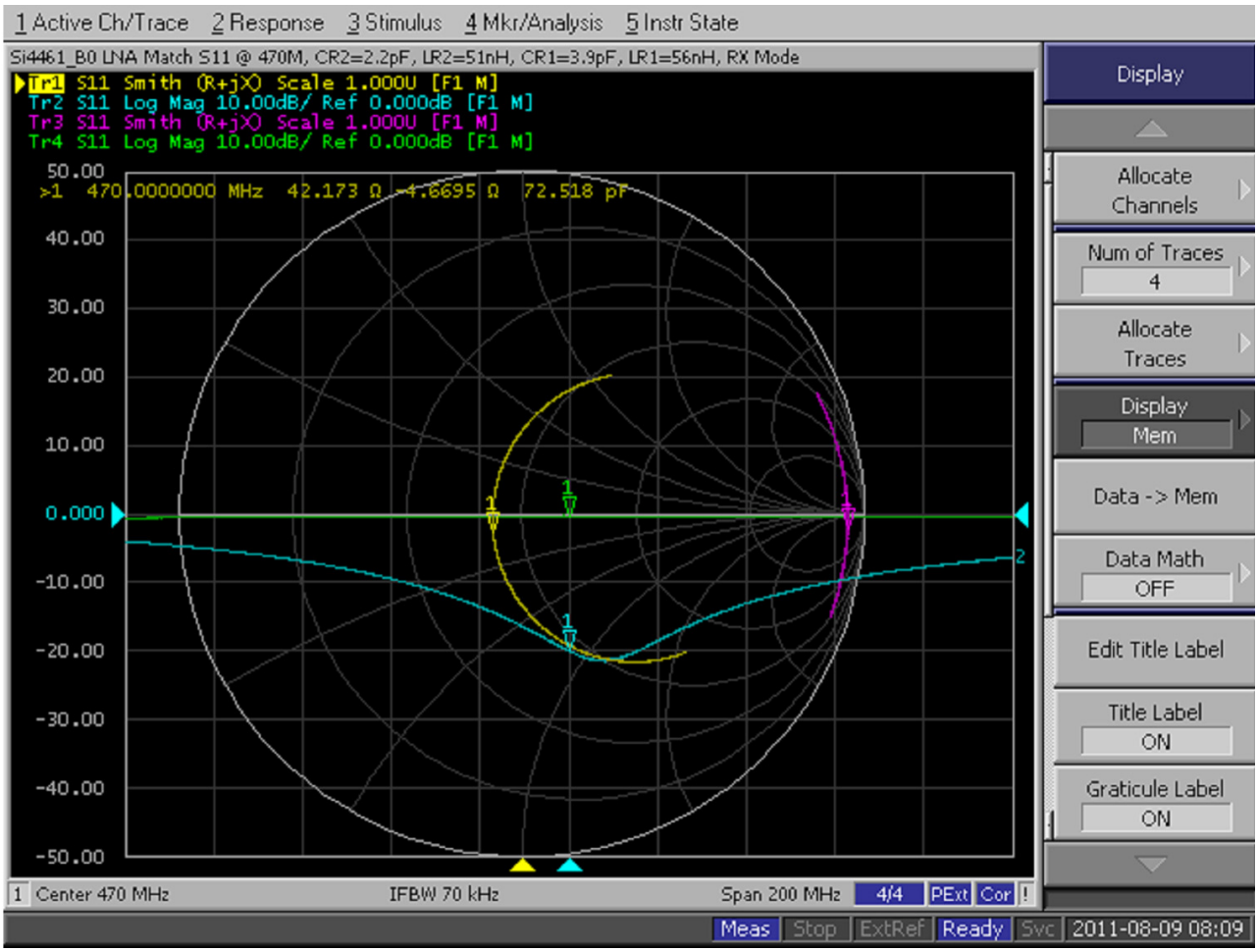

Figure 15. Input Impedance of 4-Element Match at 470 MHz

4.2.8. Use of 4-Element Match Network in Direct Tie Board Configurations

Silicon Laboratories has developed a referenced design board configuration in which the TX and RX paths are tied directly together at a common point without the use of an RF switch. This board configuration is referred to as a Direct Tie board configuration. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode, and that the TX output circuitry does not degrade receive performance while in RX mode. This design procedure requires the ***mandatory*** use of the 4-element RX match topology; it is not possible to construct a Direct Tie match with use of the 3-element RX match topology.

The RX input circuitry of the Si446x/Si4362 chip contains a set of switches that aids in isolation of the TX and RX functions. This set of switches is implemented internally as shown in Figure 16.

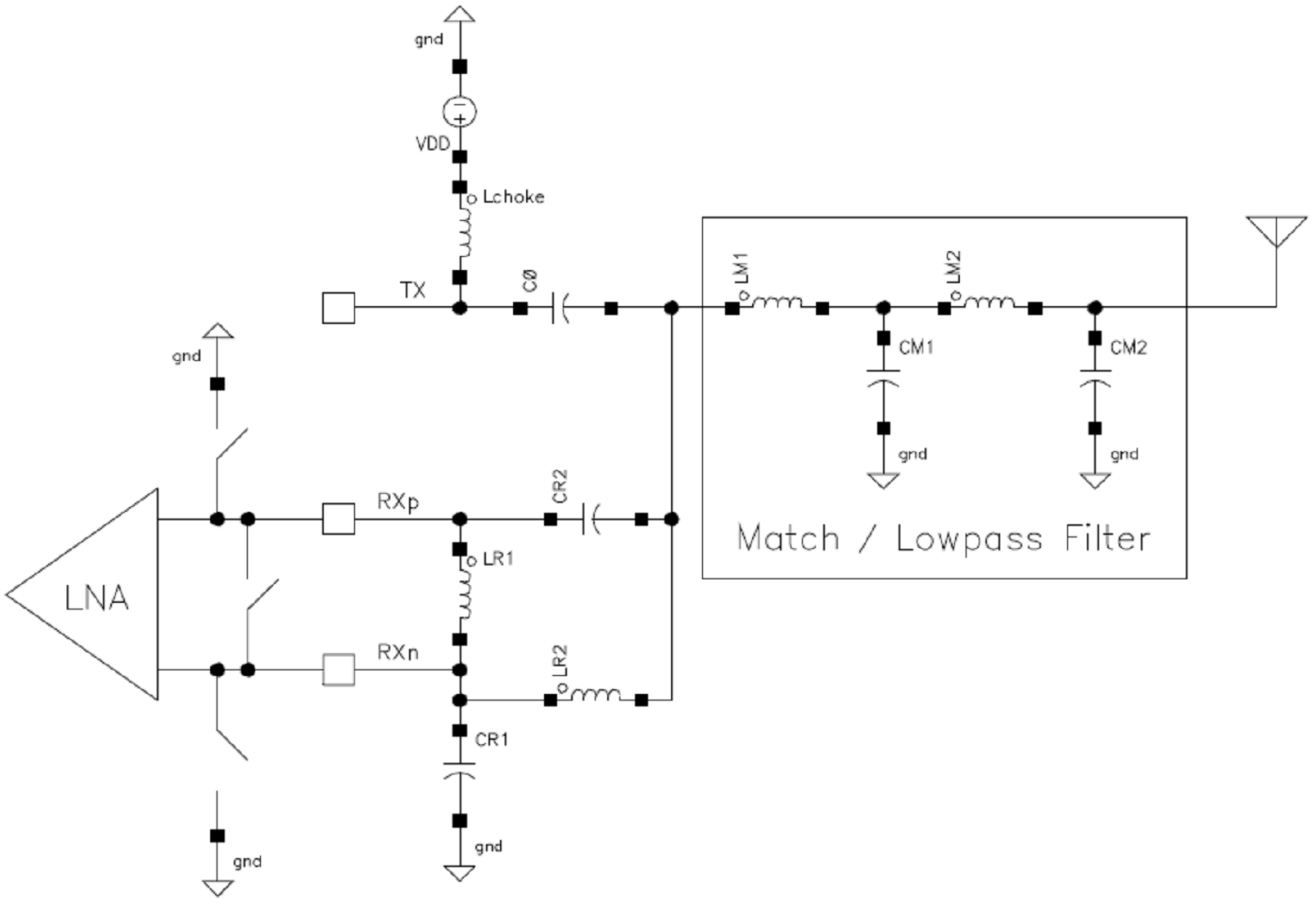

Figure 16. RX Input Switches for Direct Tie Operation

These three switches are activated and closed simultaneously upon entering TX mode; the switches remain open in all other modes, including RX mode. Closing these switches during TX mode effectively shorts the RXp and RXn input pins together and also shorts them to GND. The effective circuit may be re-drawn as shown in Figure 17. Inductor LR2 and capacitor CR2 have effectively been placed in parallel by the closure of the switches, and are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.

Further information regarding the design of a Direct Tie match may be found in application note “AN627: Si4460/61/67 Low-Power PA Matching”.

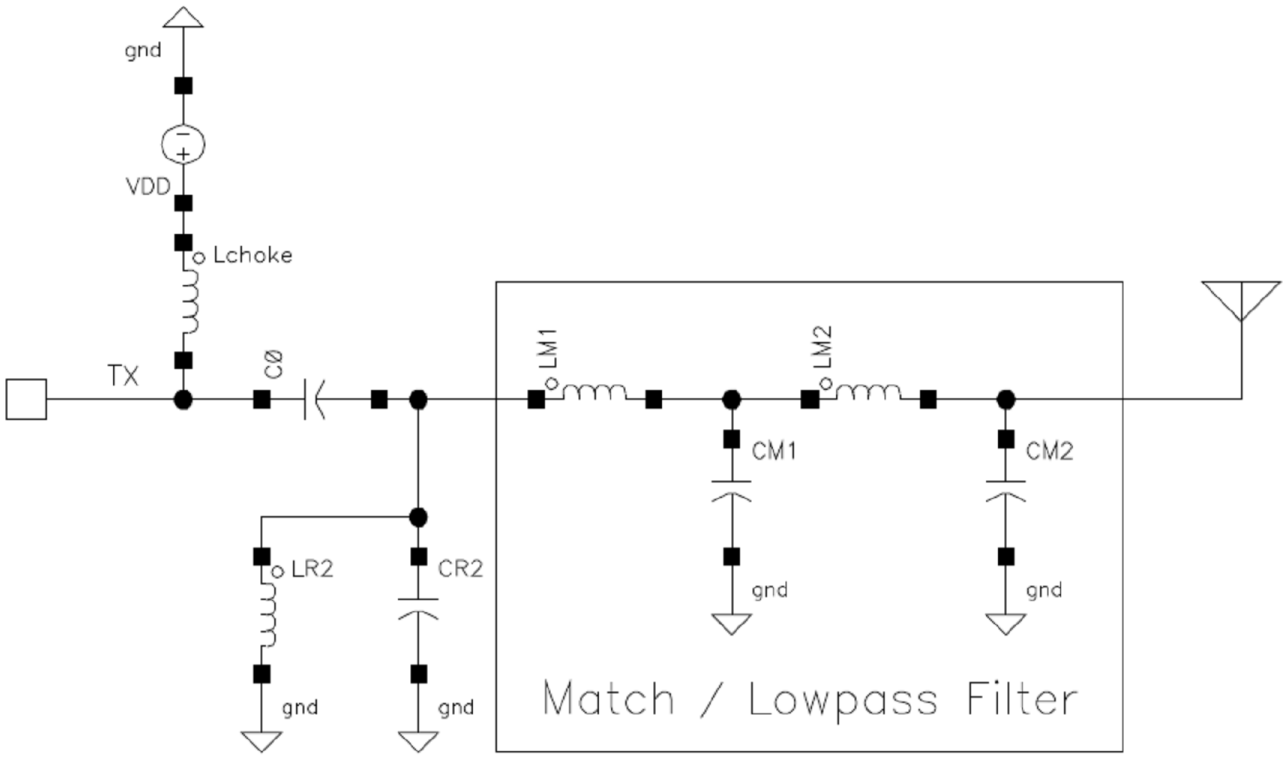

Figure 17. Effective Direct Tie Circuit in TX Mode

Document Change List

Revision 0.1 to Revision 0.2

- Replaced Si446x with Si446x/Si4362 throughout.
- Updated "1. Introduction" on page 1.

Revision 0.2 to Revision 0.3

- Clarified that RXp and RXn pins are interchangeable.

Revision 0.3 to Revision 0.4

- C0, C1, C2 added to B0 and B1 on page 1.
- Si4467 was added to Si4460/61.
- B0 was removed from Si4461_B0 on page 4.

NOTES:

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Si4060/Si4460/61/67 Low-Power PA Matching

1. Introduction

This application note provides a description of the matching techniques applied to the low-power Si4060 TX and Si4460/61/67 TRX RFIC family. The typical power regime of the Si4461 is in the +13 to +16 dBm range, while the Si4060/Si4460/67 is primarily devoted to the +10–13 dBm applications.

Specifically, this document does *not* address the matching procedure for the PA on the Si4063/4463/64/68 family of RFICs. Because the output power level on the Si4063/4463/64/68 family of RFICs is considerably higher than the Si4060/Si4460/61/67 RFIC, the matching procedure is somewhat different.

The matching network achieves a number of goals simultaneously:

- Targets a nominal output power level of +10 to +16 dBm
- Minimizes current consumption (i.e., maximize efficiency)
- Constrains the peak voltage at the drain of the output devices
- Complies with ETSI and FCC specifications for spurious emissions
- Is immune against termination impedance variations as much as possible
- Has low variation over temperature and supply voltage
- Has low bill of materials and cost

Unfortunately, not all of these goals can be satisfied in the most optimal way simultaneously. Silicon Labs investigates different matching types and methods to meet as much as possible with the above requirements. In this document, the best three TX matching types (the switched PA mode Class E (CLE) type, the switched PA mode square wave (SQW) type, and the Switched Current (SWC) type) are presented in detail.

The main advantage of the switched mode (especially CLE) matching types is their very high efficiency. They are proposed for applications where the current consumption is most critical, e.g., the typical total chip current with CLE match (assuming 3.3 V Vdd) is ~17–19 mA at ~10 dBm, ~25 mA at ~13 dBm and ~40 mA at 16 dBm power levels.

The SQW type match is proposed for use only at low frequencies (below 260 MHz, e.g. at 169 MHz), where the Class E operation is not efficient with the Pro IC family due to its low capacitance.

The main disadvantage of the switching type PA matches is the high Vdd dependency (the power variation is proportional to the square of the Vdd change: i.e. dp = ~6 dB in the 1.8–3.8 V range) and the inaccurate nonlinear power steps.

Also their current consumption and the peak voltage on the TX pin are sensitive to the termination impedance variation, and they usually require slightly higher order filtering and thus higher bill of materials cost.

Some of these drawbacks can be cured to varying degrees with special methods that are described detailed later in this document.

The main advantages of the SWC matches are the flat power vs. Vdd characteristic, better stability over temperature, accurate and linear power steps, simpler design process, and lower BOM costs due to the required weaker filtering. Therefore, the SWC match is proposed for applications in which the flat power characteristic and accurate power steps are the primarily concern and where the 10–20% higher current consumption is tolerated.

However, the biggest disadvantage is the significantly worse efficiency compared to class E. Basically, the design can be tuned between better efficiency and better power flatness, i.e., by sacrificing efficiency, better power stability can be achieved.

Typical current consumption of SWC matches tuned for high efficiency (and having worse flatness i.e. dp=~3 dB in the 1.8–3.8 V Vdd range) is 22–23 mA at 10 dBm and 30–32 mA at 13 dBm power levels.

Typical current of flat power designs (dP=~1 dB in the 1.8–3.3 V Vdd range) is 24–25 mA at 10 dBm and 38 mA at 13 dBm power levels.

Some of the switching type (CLE and SQW) disadvantages mentioned above can be cured to some extent by special methods.

For example, the high V_{DD} variation can be cured efficiently at low power levels (e.g., 10 dBm with Si4060/Si4460/67 or 14 dBm with Si4461), by the so-called adaptive power setting method. Since the low-power matches are usually designed in such a way that the specified power at the specified supply voltage is achieved at a relatively low power level setting, at decreasing supply voltage (e.g., due to a discharging battery), the power drop can be compensated by the proper increase of the power level setting i.e., with the decrease of the switcher loss. Unfortunately, this method works well only at lower power regimes (+10 dBm with Si4060/Si4460/67 and +14 dBm with Si4461) where a low power level setting is enough to get the targeted power, and, thus, there is room for compensation. In these cases, the Class E stability over V_{DD} can be even better than 1 dB in the 3.6–.2.1 V Vdd range.

A low power setting (at low power regimes) with higher switcher loss is also good to have immunity against termination antenna impedance variations. It especially reduces the variation of the dc current consumption with variable environmental conditions suffered by the antenna, which is favorable for long-life battery-operated applications, such as meters or sensors, because the excess current drain is limited.

The operation type (CLE, SQW or SWC) can be set by the PA_MODE (0x2200) register. The 0x18 (Si4060/Si4460/67) and 0x20 (Si4461) values result in switching mode (CLE or SQW) operation, while the 0x19 (Si4060/Si4460/67) and 0x21 (Si4461) values result in SWC operation.

In case of the switched PA mode (SQW and CLE) matches, the power can be set by the DDAC field in the PA_PWR_LVL (0x2201) register. The DDAC determines the number of used switching MOS fingers and thus the on-state resistance of the switcher.

In the case of SWC operation, the PA behaves like a high-impedance switched current generator; so, besides the number of fingers (DDAC), the delivered current per finger also determines the power. The current delivered by a finger can be set by the OB field of the PA_BIAS_CLKDUTY register in 10 µA steps.

Here, it is important to note that the critical output parasitic cap value of the PA does not depend on the number of active fingers (DDAC) as determined by the uppermost cascode MOS device connected to the TX pin.

It is theoretically possible to increase the efficiency of low-power CLE matches by reducing the current of the internal PA drivers. For that, they can work in 25% duty cycle mode, by setting all bits of the CLK_DUTY field in the PA_BIAS_CLKDUTY register (0x2202) to 1, resulting in a PA_BIAS_CLKDUTY register value of 0xC0.

The 10 dBm and 13 dBm CLE matches with Si4060/Si4460 use this 25% duty cycler mode to save current. The drawback of this mode is the increased harmonic content and the consequently greater number of filtering components.

With 50% duty cycle mode (PA_BIAS_CLKDUTY register is left in its default value of 0x00), the Si4060/Si4460/67 high power (HP) CLE matches can achieve the 13–14 dBm power with sufficient margin, even with multilayer inductors. However, in this case, the current consumption will be nearly the same as it is with the Si4461 matches. Since the Si4461 has more robust PA, which is designed primarily to the 13–14 dBm power range, there is no reason to use the Si4060/4460/67 ICs instead in 50% duty cycle CLE mode.

The matching procedure outlined in this document for CLE/SQW and SWC allows the user to achieve the above mentioned properties and is applicable for two different types of board configurations: one with separate antennas for the TX and RX paths (Split TX/RX board configuration: in the case of TX only chips (Si4060) the TX path can be used by simply omitting the RX path) and one with a single antenna where the TX and RX paths are tied directly together without the use of an RF switch (Direct Tie board configuration: again, in case of TX only chips (Si4060), the TX path can be used and the Rx path can be omitted).

The differences in the matching procedure required for the two board configurations are discussed in detail.

The next chapter is provided for users more interested in quickly obtaining matching component values than in the methodology used to develop the matching network. The methodology is described in detail in Sections 3, 4, and 5.

Table 1. Silicon Labs EZRadio Pro Sub-GHz Wireless IC Family RF Match Cross References

Match Type	Advantages	Disadvantages	RF IC Types						
			Si4463/64/68 (TRX)	Si4461 (TRX)	Si4460/67 (TRX)	Si4438 (TRX)	Si4063 (TX)	Si4060 (TX)	Si4362 (RX)
Class E Split	High Efficiency, High Power	power varies with VDD, nonlinear power steps	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868M 13–16 dBm & 26–43 mA	**AN627**, 434/868/ 915M 10…13 dBm & 16–24 mA	**AN732**, 490 MHz, 20 dBm & 85 mA	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868/915M 10–13 dBm & 16–24 mA	—
Class E DT	High Efficiency, High power, One antenna	power varies with VDD, nonlinear power steps	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868M 13–16 dBm & 26.5–43 mA	**AN627**, 434/868/ 915M 10–13 dBm & 17–25 mA	**AN732**, 490 MHz, 20 dBm & 85 mA	—	—	—
Class E TX/RX Switch	High Efficiency, One antenna	power varies with VDD, nonlinear power steps, extra RF switch adds cost	**AN648**, 868/915M 20 dBm & 85 mA	—	—	—	—	—	—
SQW DT	High Efficiency, High power, one antenna	power varies with VDD, nonlinear power steps	**AN648**, 169M 20 dBm & 70 mA	—	**AN627**, 169M, 10 dBm & 18 mA	—	—	—	—
SWC SPLIT	Flat VDD characteristic, lower BOM (than class E), linear power steps	less efficient, medium power	—	**AN627**, 868/915M 13–14 dBm & 31–36 mA	**AN627**, 315/ 434/868/ 915M 10 dBm & 24 mA	—	—	**AN627**, 315/434/868/ 915M 10 dBm & 24 mA	—
SWC DT	Flat VDD characteristic, lower BOM (than class E), linear power steps, one antenna	less efficient, medium power	—	**AN627**, 868/915M 13–14 dBm & 31–36 mA	**AN627**, 315/434/868/ 915M 10 dBm & 24 mA	—	—	—	—
4 Element RX Match	Balun with minimum phase and magnitude error, fully matched		—	—	—	—	—	—	**AN643**, 10/13 mA

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2. Summary of Matching Network Component Values

Some users are not greatly interested in the theoretical development of the matching network; rather, they are concerned with quickly obtaining a set of component values for a given desired frequency of operation. For those users, the resulting component values for the CLE, SQW and SWC PA matching network for multiple frequencies and power levels across the operating range of the Si4060/Si4460/67 and Si4461 RFIC are summarized in this section.

The matching networks may be realized with either wire-wound SMD inductors or multi-layer SMD inductors. The cost of a multi-layer inductor is significantly lower than that of a wire-wound inductor, and, thus, in cost sensitive applications, the multi-layer solution is preferred. However, the performance of a circuit realization using only wire-wound inductors is generally better due to the higher Qs and lower ohmic losses than multi-layer inductors of equivalent value. Due to the increased loss, a realization using multi-layer inductors typically requires a higher power level setting and thus exhibits a slight increase in current consumption for the same amount of output power.

Also, multi-layer SMD inductors are often available only in coarser-spaced inductance values. It may cause a higher deviation from the ideal class E values, especially in Direct Tie solutions where significant adjustments of the value of L0 are usually necessary in order to avoid degradation to RX sensitivity; this may be more difficult with only the set of values available for a multi-layer series of inductors.

The component values shown in these tables are appropriate for a supply voltage of V_{DD} = 3.3 V.

For other V_{DD} voltages the 10 dBm Si4060/Si4460/67 and 14 dBm Si4461 CLE design needs adjustment of the PA power level (e.g., the previously-mentioned adaptive power control), which, to some extent, can compensate the power variations. However, in case of 13–14 dBm Si4060/Si4460/67 and 16 dBm Si4461 CLE designs, the power setting is close to maximum, and, thus, the margin for power degradation compensation at low supply voltage levels is very limited.

The output power of a properly-matched SwC PA is relatively insensitive to the supply voltage changes; so, the component values and the power level settings (DDAC and OB register fields) can be used for other values of V_{DD} as well.

The matching networks are separated based on RFIC (Si4060/Si4460/67 and Si4461) types due to the different PA properties.

The Si4461 PA has 127 MOS switching fingers so the DDAC register can go up to 0x7F. Its typical output capacitance is 2.0 pF independently of the DDAC setting due to its cascade architecture.

The Si4060/Si4460/67 PA has 79 MOS switching fingers; so, the DDAC register can go up to 0x4F. Its typical output capacitance is 1.25 pF independently of the DDAC setting due to its cascade architecture.

The component values shown in the following sections are appropriate when using 0402-size SMD components, such as the 0402HP-series of wire-wound inductors from CoilCraft, the LQG15HS-series of multi-layer inductors from Murata, and the GRM15-series of ceramic capacitors from Murata. These values are appropriate for use on the official Split TX/RX and Direct Tie reference board designs available on the Silicon Labs web site. The presented solutions are likely to operate satisfactorily with 0603-size SMD elements as well.

Surface-mount 0603-size or 0402-size components contain parasitic elements that modify their effective values at the frequency of interest. Furthermore, it is convenient to use the nearest-available 5% or 10% component values rather than the exact component values predicted by, for example, filter design CAD software or filter prototype tables. Additionally, any printed circuit board layout has parasitics, such as trace inductance, component pad capacitance, etc.

This means that it will almost certainly be necessary to adjust the final matching values for the reader's specific application and board layout. The above component values should be used as starting points and the values modified slightly to zero-in on the best filter response and impedance match to 50 Ω.

2.1. Component Values for Si4461 Matching

The Si4461 High Efficient SWC and CLE matches fit most for the 13–14 dBm power regime. At this power level, the CLE has enough margin to be stable over V_{DD} with adaptive power control. The basic 13–14 dBm Si4461 SWC match is optimized for efficiency around 3.3 V. Despite, the power drop in the 1.8–3.6 V Vdd range is only 2–3 dB, much better than that of the CLE match. It has also linear power steps.

A second 868M SWC match optimized for flat power characteristic (dP=~1 dB) is also given in the tables below, but with higher current consumption.

The efficiency of the CLE solution is still significantly better than that of any SWC solution.

The 16 dBm regime can be achieved only with CLE matching. Unfortunately, as mentioned previously, it has high variation over supply voltage because adaptive power control is no longer efficient due to the power setting here, which is close to the maximum.

2.1.1. Si4461 with Split TX\RX SWC Board Configuration: Component Values and Performance

Table 2 provides the component values required for output power levels of both +13 and +14 dBm, using the Split SWC TX/RX board configuration of Figure 1 and a supply voltage of V_{DD} = 3.3 V. The matches described in Table 2 are optimized for the best efficiency and use wire-wound type inductors. At the time of this writing, no Si4461 SWC split match with multilayer inductors are fully tested, but the matches given in Table 2 give satisfactory results with multilayer inductors as well (if an inductor value does not exist, use the closest one). Some tuning (slight increase on OB and/or DDAC value) of the power setting and/or the element values may required here. For other frequencies not given here, consult with a Silicon Labs representative.

If a flat Si4461 SWC TX only/split solution is required, use the TX part of the flat DT SWC match given in Table 4 on page 9.

Table 2. TX Matching Network Component Values vs. Frequency (Split Si4461 High-Efficiency SWC TX/RX Board, V_{DD}=3.3 V, Tested with Wire-Wound Inductors)

Freq Band	Lchoke	C0	LM1	CM1	LM2	CM2	LM3
Pout = +13 dBm							
868 MHz	120 nH	47 pF	18 nH	5.1 pF	13.0 nH	3.9 pF	0 Ω
915 MHz	100 nH	39 pF	16 nH	5.1 pF	12.0 nH	3.9 pF	0 Ω
Pout = +14 dBm							
868 MHz	120 nH	47 pF	16 nH	5.1 pF	13.0 nH	3.9 pF	0 Ω
915 MHz	100 nH	39 pF	15 nH	5.1 pF	12.0 nH	3.9 pF	0 Ω

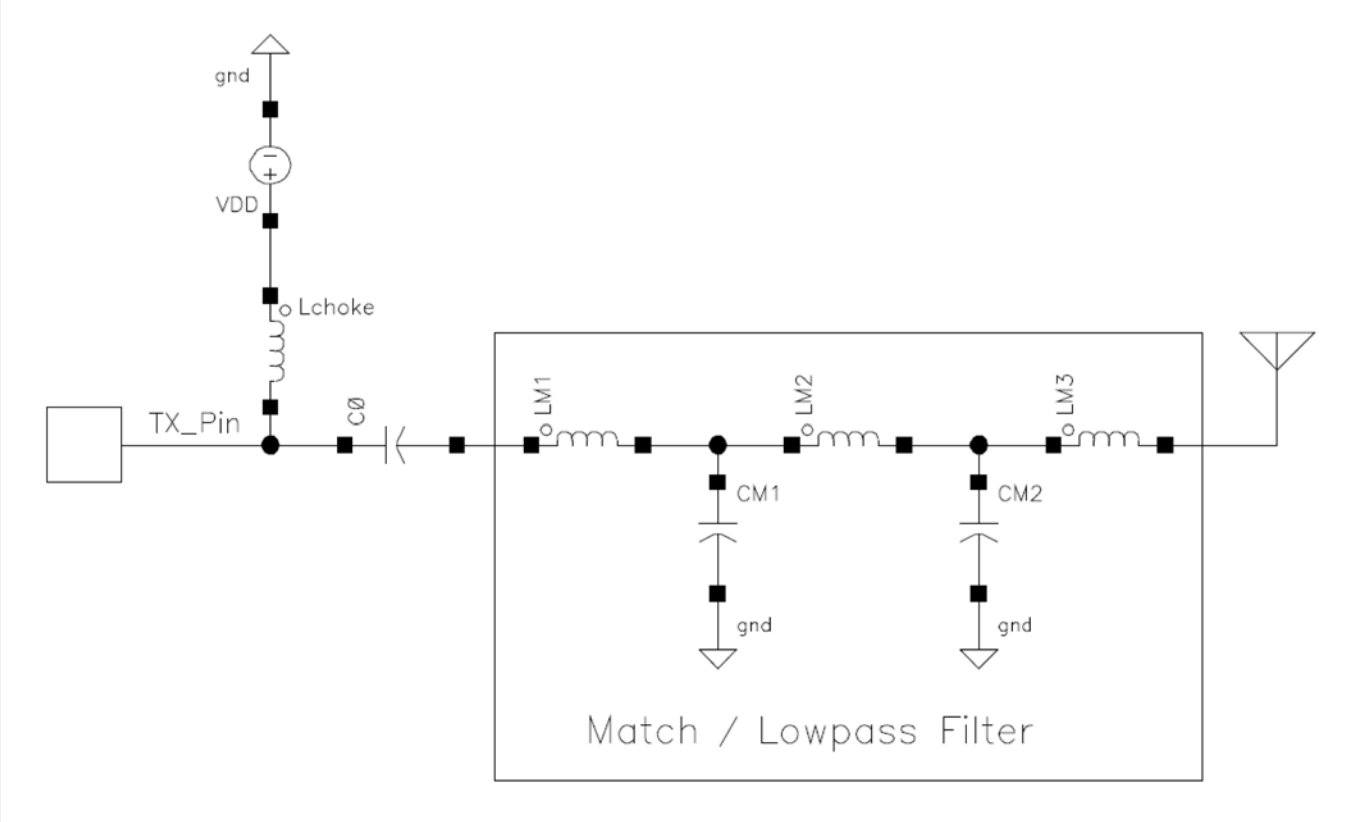

Figure 1. TX Matching Topology for Split SWC TX/RX Board Configuration

Table 3 lists summary of typical measured output power and current consumption for split board configurations given in Figure 1 and in Table 3. These results are obtained with a supply voltage of VDD = 3.3 V and with wire-wound inductors.

Table 3. Output Power and Current Consumption vs. Frequency (Split Si4461 High-Efficiency SWC TX/RX Board, V_{DD} = 3.3 V, Tested with Wire-Wound Inductors)

Freq Band	OB[5:0]	DDAC[6:0]	Pout (dBm)	IDC (mA)
Pout = +13 dBm				
868 MHz	0x21	0x64	12.96 dBm	30.56 mA
915 MHz	0x22	0x64	12.85 dBm	30.15 mA
Pout = +14 dBm				
868 MHz	0x2C	0x64	14.10 dBm	35.61 mA
915 MHz	0x2E	0x64	14.01 dBm	36.10 mA

2.1.2. Si4461 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance

Table 4 provides the component values required for output power levels of both +13 and +14 dBm using the Single Antenna with Direct Tie SWC board configuration of Figure 2 and a supply voltage of V_{DD} = 3.3 V. One part of these matches is optimized for the best efficiency (denoted by HE in Table 4) and thus has 2–3 dB power variation in the 1.8–3.8 V Vdd range. It is still significantly better than the flatness of any CLE match.

At 868M there is also a second, flat Vdd characteristic SWC DT proposal (denoted by FC). This has 1.5 dB power variation in the 1.8–3.8 V Vdd range (see Table 7). At the time of this writing, these 4461 SWC DT matches were not tested with multilayer inductor yet. Consult with a Silicon Labs representative for other frequency SWC matches.

Table 4. Matching Network Component Values vs. Frequency (Direct Tie Si4461 SWC Board, V_{DD} = 3.3 V, Tested with Wire-Wound Inductors)

Pout = +13 dBm												
Freq Band	RX Side				TX Side							
	LR1	LR2	CR1	CR2	Lchoke	C0	LM1	CM1	LM2	CM2	LM3	CM3
HE868M	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	47 pF	18 nH	5.1 pF	13 nH	3.9 pF	0 Ω	N.F
HE915M	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	39 pF	16 nH	5.1 pF	12 nH	3.9 pF	0 Ω	N.F.
FC868M	16 nH	16 nH	3.6 pF	1.5 pF	120 nH	47 pF	8 nH	8.2 pF	8 nH	8.2 pF	7.5 nH	3.9 pF
Pout = +14 dBm												
Freq Band	RX Side				TX Side							
	LR1	LR2	CR1	CR2	Lchoke	C0	LM1	CM1	LM2	CM2	LM3	CM3
HE868M	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	47 pF	16 nH	5.1 pF	13 nH	3.9 pF	0 Ω	N.F.
HE915M	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	39 pF	15 nH	5.1 pF	12 nH	3.9 pF	0 Ω	N.F.

A summary of typical measured output power, current consumption, and sensitivity (40 kbps, dev = 50 kHz (H = 1), 0.1% BER) for high efficiency (denoted by HE) and a 868M flat (FC) SWC direct tie board configurations of Table 4 are shown in Table 5. These results are obtained with a supply voltage of V_{DD} = 3.3 V.

Table 5. Output Power, Current Consumption and Sensitivity vs. Frequency (Direct Tie Si4461 SWC Board, V_{DD} = 3.3 V, Tested with Wire-Wound Inductors)

Pout = +13 dBm					
Freq Band	OB[5:0]	DDAC[6:0]	Pout (dBm)	IDC (mA)	Sens. (dBm)
HE868M	0x20	0x64	12.77 dBm	30.62 mA	–109.0 dBm
HE915M	0x20	0x64	12.79 dBm	30.23 mA	–108.8 dBm
FC868M	0x27	0x7F	13.00 dBm	38.00 mA	–108.3 dBm

Table 5. Output Power, Current Consumption and Sensitivity vs. Frequency (Direct Tie Si4461 SWC Board, V_{DD} = 3.3 V, Tested with Wire-Wound Inductors) (Continued)

Pout = +14 dBm					
HE868M	0x2D	0x64	13.86 dBm	35.97 mA	–109.0 dBm
HE915M	0x2C	0x64	13.99 dBm	35.60 mA	–108.8 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 1.5 dB of those obtained with the Split TX/RX board configuration. The power vs. Vdd characteristic is given for the 868M flat (FC868M) DT design in Table 6.

Table 6. Output Power, Current Consumption vs. Vdd (Direct Tie Si4461 flat SWC Board, Wire Wound Inductors)

Vdd [V]	FC868M PA_BIAS = 0x27, PA_PWR_LVL = 0x7F	
	Pout [dBm]	Idc [mA]
1.8	11.7	34
2.1	12.5	35.6
2.4	12.8	37
2.7	12.9	37.5
3	13.1	38
3.3	13	38
3.6	13	38
3.8	13	38
delta (2.1–3.3 V)	0.5	2.4
delta (1.8–3.8 V)	1.4	4

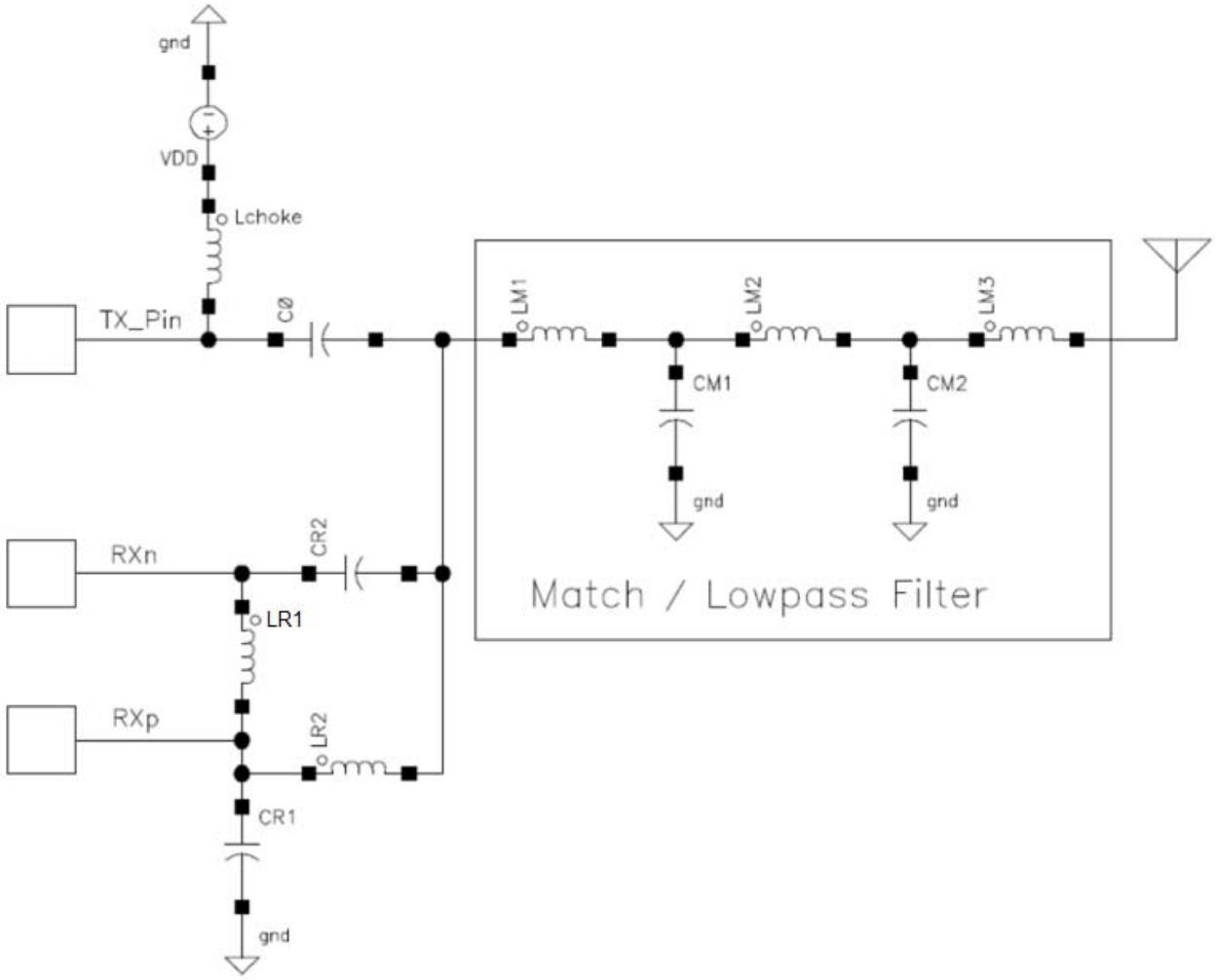

Figure 2. Matching Topology for Single Antenna with Direct Tie SWC Board Configuration

2.1.3. Si4461 CLE Split TX/RX Board Configuration: Component Values and Performance

Table 7 lists the component values required for output power levels for +14 and +16 dBm using the Split CLE TX/RX board configuration of Figure 3 and a supply voltage of V_{DD} = 3.3 V. Table 7 matching is proper for both wire-wound and multilayer type inductors. For other frequencies, consult with a Silicon Labs representative.

Table 7. TX Matching Network Component Values vs. Frequency (Split Si4461 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound and Multilayer Inductor Versions)

Freq Band	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	LM3	R_{DC}
Pout = +14 dBm										
434 MHz	220 nH	15 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω	0 Ω
868 MHz	120 nH	22.0 pF	12.0 nH	4.7 pF	8.2 nH	3.9 pF	0 Ω	N.F.	0 Ω	0 Ω
Pout = +16 dBm										
434 MHz	220 nH	8.2 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω	0 Ω
868 MHz	120 nH	22.0 pF	10.0 nH	4.7 pF	8.2 nH	3.9 pF	0 Ω	N.F.	0 Ω	0 Ω

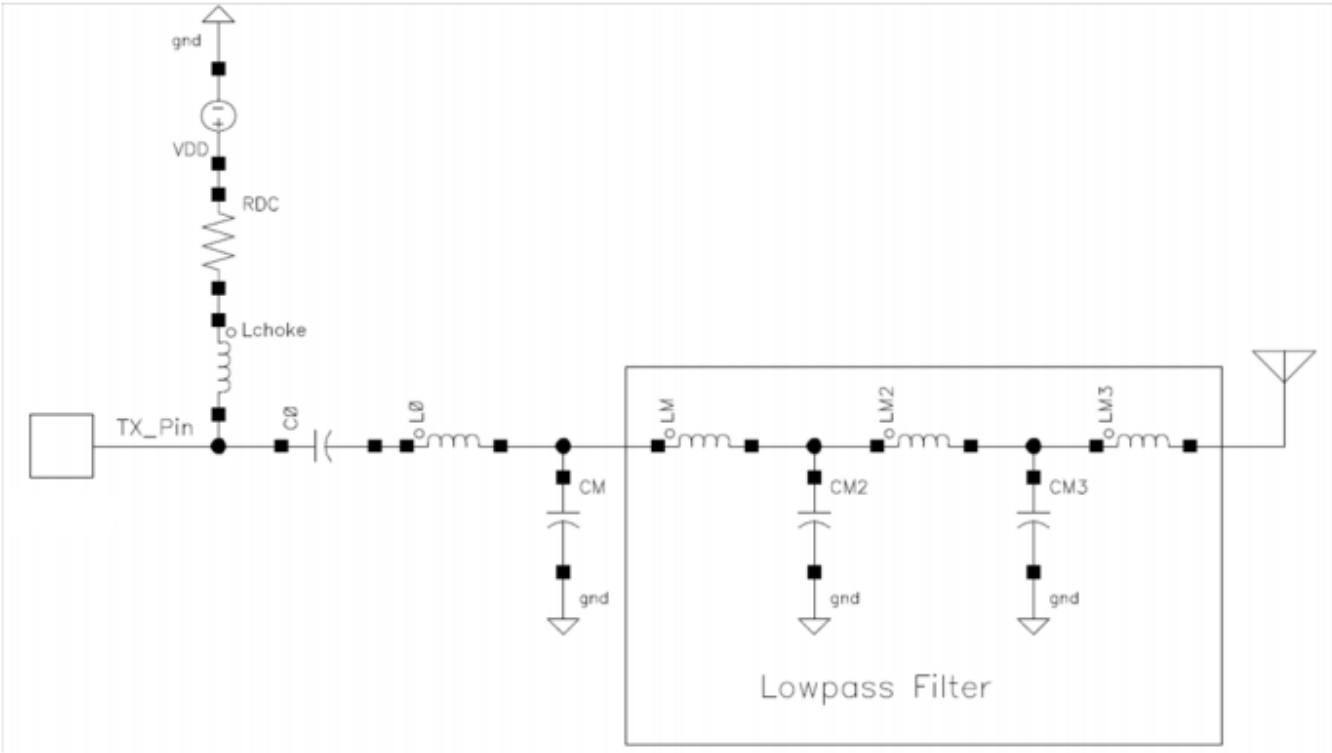

Figure 3. TX Matching Topology for Si4461 Split TX/RX Board CLE Configuration

A summary of typical measured output power and current consumption for split board configurations (both with wire-wound and multilayer inductors) is given in Table 8. These results are obtained with a supply voltage of V_{DD} = 3.3 V.

In the case of WW inductors, a lower power state setting is enough for the same output power due to the lower loss. Due to the lower power setting, the WW solution is more robust against supply voltage variations with adaptive power control. In addition, it is more robust against-load impedance variations. The efficiency is also better compared to the Multilayer matches. Moreover, with some slight component value adjustments (basically, of C0 and CM), the WW solutions can be tuned for slightly better efficiency (~2…5%) with a simultaneous sacrifice of robustness.

Table 8. Output Power and Current Consumption vs. Frequency (Split Si4461 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductor)

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)
Pout = +14 dBm						
434 MHz	20h	14.3 dBm	28.1 mA	2Dh	14.3 dBm	29.7 mA
868 MHz	2Bh	14.4 dBm	31.6 mA	34h	14.3 dBm	34.4 mA
Pout = +16 dBm						
434 MHz	32h	16.3 dBm	35.8 mA	7Fh	16.3 dBm	38.9 mA
868 MHz	40h	16.3 dBm	38.9 mA	4Fh	16.2 dBm	42.7 mA

2.1.4. Si4461 CLE for Direct Tie Board Configuration: Component Values and Performance

Table 9 (wire-wound inductor) and Table 10 (multilayer inductor) provide the component values required for output power levels of both +14 and +16 dBm using the Single Antenna with Direct Tie board configuration of Figure 4 and a supply voltage of V_{DD} = 3.3 V. For other frequencies, consult with a Silicon Labs representative.

Table 9. Matching Network Component Values vs. Frequency (Direct Tie Si4461 CLE Board, V_{DD} = 3.3 V, Wire-Wound Inductor)

Pout = +14 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	51 nH	3.9 pF	2.2 pF	220 nH	15 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω
Pout = +16 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	51 nH	3.9 pF	2.2 pF	220 nH	15.0 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω

Table 10. Matching Network Component Values vs. Frequency (Direct Tie Si4461 CLE Board, V_{DD} = 3.3 V, Multilayer Inductor)

Pout = +14 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	15 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	18 nH	22 nH	3.0 pF	1.2 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω
Pout = +16 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	8.2 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	18 nH	22 nH	3.0 pF	1.2 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω
915 MHz	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	22 pF	6.8 nH	3.9 pF	6.8 nH	3.9 pF	0 Ω	N.F.	0 Ω

A summary of typical measured output power, current consumption, and sensitivity in RX mode (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 11. These results are obtained with a supply voltage of V_{DD} = 3.3 V. The multilayer inductor version has worse efficiency.

Table 11. Output Power, Current Consumption and RX Sensitivity vs. Frequency (Direct Tie Si4461 CLE Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
Pout = +14 dBm								
434 MHz	21h	14.4 dBm	28.7 mA	–104.7 dBm	2Fh	14.3 dBm	30.1 mA	–103.7 dBm
868 MHz	2Eh	14.3 dBm	33.2 mA	–103.5 dBm	34h	14.3 dBm	34.4 mA	–101.3 dBm
Pout = +16 dBm								
434 MHz	3Fh	16.3 dBm	33.0 mA	–104.7 dBm	7Fh	16.4 dBm	40.1 mA	–104.0 dBm
868 MHz	41h	16.3 dBm	39.6 mA	–103.5 dBm	5Eh	16.3 dBm	42.9 mA	–101.3 dBm
915 MHz					4Fh	16.3 dBm	43.3 mA	–102.5 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 2 dB of those obtained with the Split TX/RX board configuration.

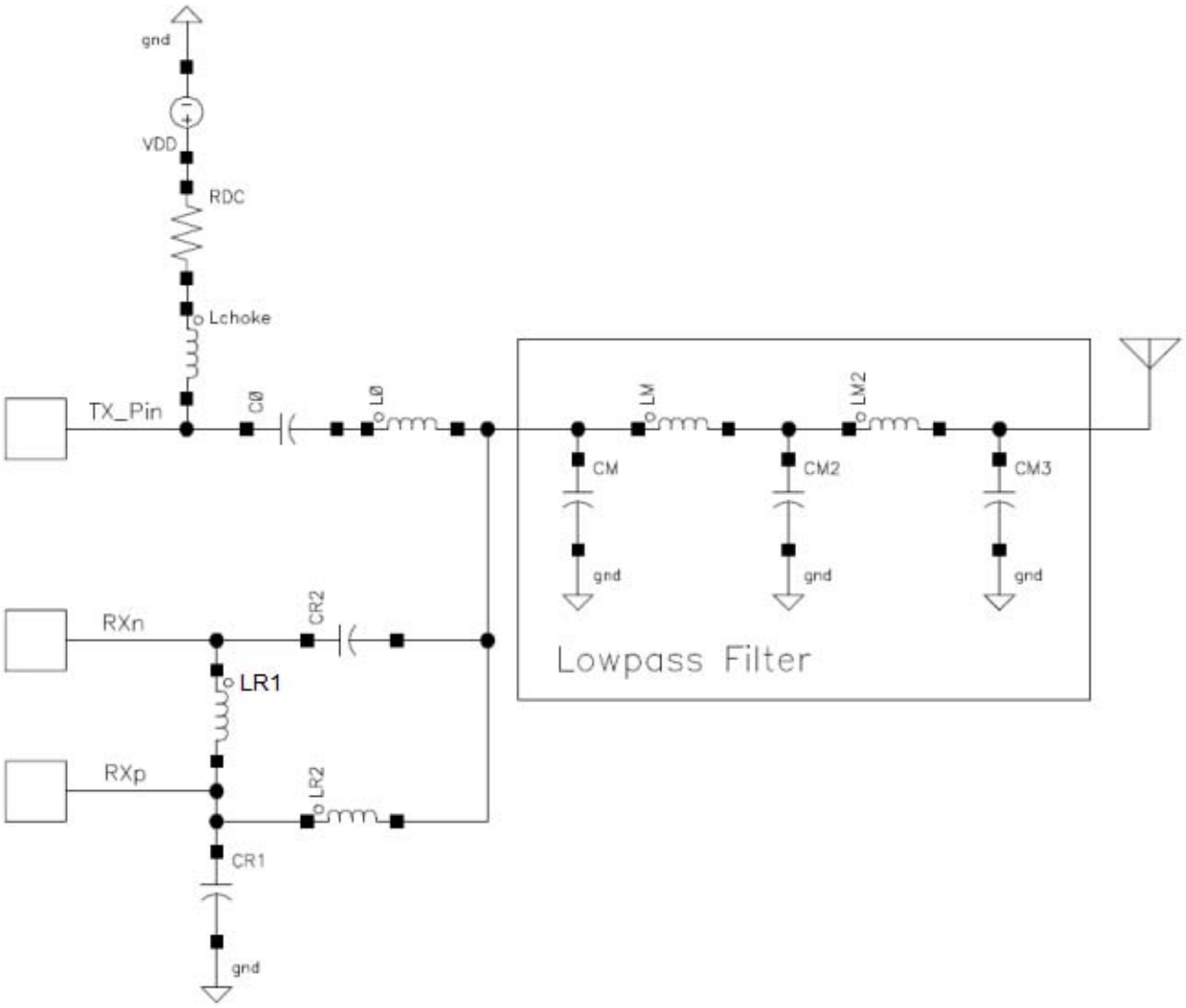

Figure 4. Matching Topology for Single Antenna with Si4461 Direct Tie CLE Board Configuration

2.2. Component Values for Si4060/Si4460/67 Matchings

The Si4060/Si4460/67 CLE, SQW, and SWC types are typically proper for 10 dBm applications, where they have either good efficiency (CLE match with 17–19 mA total current) or stable operation (a SWC match designed for flat power characteristic has a power variation ~1 dB in the 1.8–3.8 V Vdd range). For flat Vdd characteristic (1–2 dB power variation), the CLE needs adaptive power control.

The 13 to 14 dBm regime can only be achieved with CLE matching. It has high variation over Vdd, even with adaptive power control, because it is no longer efficient due to the power setting here, which is close to the maximum. Also, with this high power, the CLE matching is sensitive to the termination impedance variations. The only advantage of these high-power Si4460/67 CLE matchings is the good efficiency.

It must be noted that all Si4060/Si4460/67 CLE matches are working in 25% duty cycle mode to achieve the best efficiency (PA_BIAS_CLKDUTY register is set to 0xC0).

The 13 dBm power CLE Si4060/4460/67 matches could work better with a 50% duty cycle, with a lower power state, i.e., with more margin. But, in this case, the current consumption would be also higher, and it would be close to that of the 13–14 dBm Si4461 CLE matches; so, with 50% duty cycle the 13 dBm Si4060/Si4460 solutions have no efficiency advantage compared to the Si4461 solutions.

2.2.1. Si4060/Si4460/67 CLE Split TX/RX Board Configuration: Component Values and Performance

Table 12 provides the component values required for output power levels for +10 and +13 dBm using the Split CLE TX/RX board configuration of Figure 5 and a supply voltage of V_{DD} = 3.3 V. The matchings of Table 12 are proper for wire-wound type inductors. For other frequencies, consult with a Silicon Labs representative. Split TX Matches using multilayer type inductors are not developed yet. For that, use the TX part of the DT matches with multilayer inductors (see Table 15). If the last inductor is only 0 Ω, a proper bypass cap can be used instead (220 pF at 434M and 56 pF at 868M) if dc blocking required. The L0 and C0 can be replaced with negligible effect.

Table 12. TX Matching Network Component Values vs. Frequency (Split Si4060/Si4460/67 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound Inductor Versions)

Pout = +10 dBm										
Freq Band	**Lchoke**	**C0**	**L0**	**CM**	**LM**	**CM2**	**LM2**	**CM3**	**LM3**	**R_{DC}**
434 MHz	220 nH	15 pF	56 nH	8.2 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0 Ω	0 Ω
868 MHz	120 nH	15 pF	19 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0 Ω	0 Ω
Pout = +13–14 dBm										
Freq Band	**Lchoke**	**C0**	**L0**	**CM**	**LM**	**CM2**	**LM2**	**CM3**	**LM3**	**R_{DC}**
434 MHz	220 nH	10 pF	56 nH	10.0 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0 Ω	0 Ω
868 MHz	120 nH	3.6 pF	19 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0 Ω	0 Ω

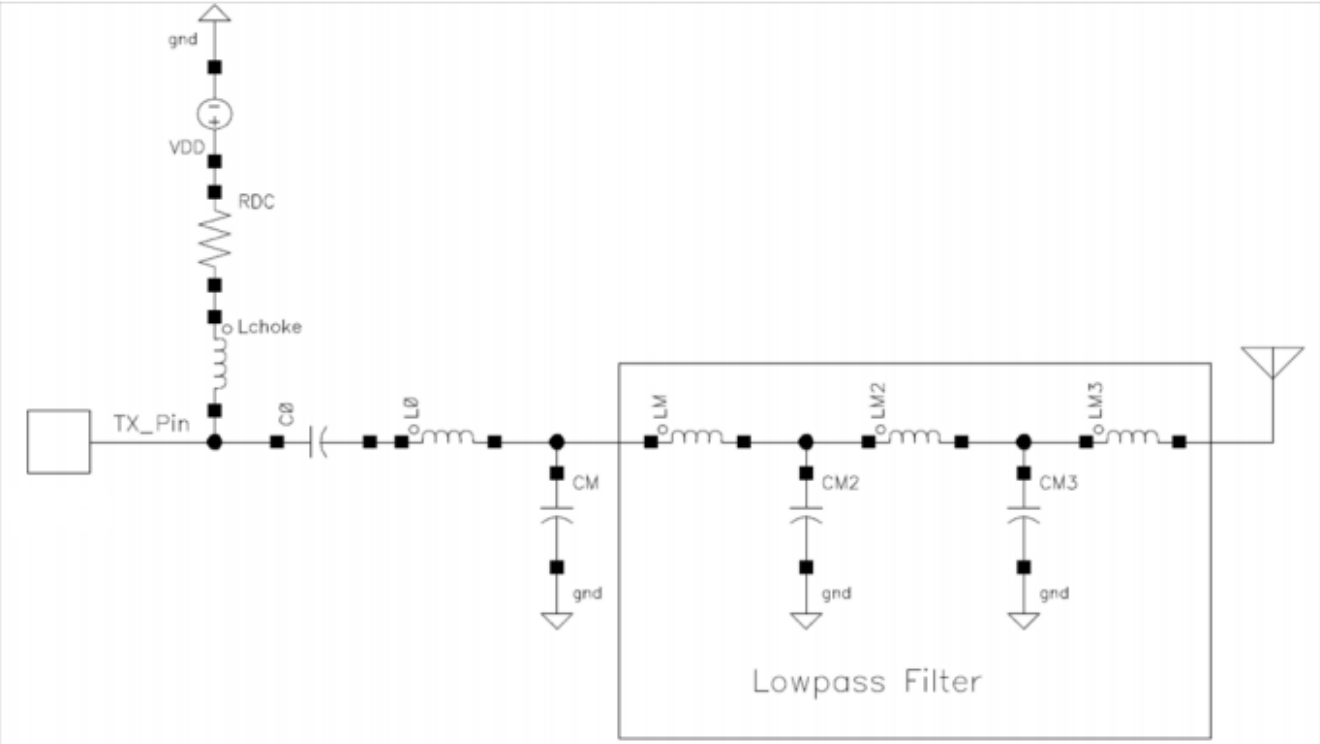

Figure 5. TX Matching Topology for Si4060/Si4460/67 Split TX/RX Board CLE Configuration

A summary of typical measured output power and current consumption for split board configurations with wire-wound inductors given in Table 13. These results are obtained with a supply voltage of V_{DD} = 3.3 V.

Table 13. Output Power and Current Consumption vs. Frequency (Split Si4060/Si4460/67 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound Inductors)

Pout = +10 dBm			
Freq Band	**DDAC[6:0] WW**	**Pout WW (dBm)**	**IDC WW (mA)**
434 MHz	19h	10.4 dBm	16.9 mA
868 MHz	19h	10.3 dBm	16.4 mA
Pout = +13–14 dBm			
Freq Band	**DDAC[6:0] WW**	**Pout WW (dBm)**	**IDC WW (mA)**
434 MHz	3Fh	13.4 dBm	22.7 mA
868 MHz	3Dh	14.3 dBm	24.8 mA

2.2.2. Si4460/67 CLE for Direct Tie Board Configuration: Component Values and Performance

Table 14 provides the component values required for output power levels of both +10 and +12–13 dBm using the Single Antenna with Direct Tie board configuration of Figure 6 and a supply voltage of V_{DD} = 3.3 V. The matchings of Table 14 are proper for wire-wound type of inductors. The same is given for multilayer inductors in Table 15. For other frequencies, consult with a Silicon Labs representative. If the last inductor is only 0 Ω, a proper bypass cap can be used instead (220 pF at 434M and 56 pF at 868/915M) if dc blocking is required. The L0 and C0 can be replaced with negligible effect.

Table 14. Matching Network Component Values vs. Frequency (Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Wire-Wound Inductor)

Pout = +10 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	15.0 pF	56.0 nH	8.2 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
868–915 MHz	18.0 nH	22.0 nH	3.0 pF	1.2 pF	120.0 nH	36.0 pF	6.8 nH	3.9 pF	6.8 nH	10.0 pF	6.8 nH	4.7 pF	0.0 Ω
Pout = +13 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
HP 434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	10.0 pF	56.0 nH	10.0 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
HP 868 MHz	20.0 nH	24.0 nH	3.0 pF	1.0 pF	120.0 nH	3.6 pF	19.0 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0.0 Ω

Table 15. Matching Network Component Values vs. Frequency (Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Multilayer Inductor)

Pout = +10 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	RDC
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	18.0 pF	56.0 nH	8.2 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
868-915 MHz	18.0 nH	22.0 nH	3.0 pF	1.2 pF	120.0 nH	36.0 pF	6.8 nH	3.3 pF	6.8 nH	10.0 pF	6.8 nH	4.7 pF	0.0 Ω
Pout = +13 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	RDC
HP 434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	6.2 pF	56.0 nH	10.0 pF	18.0 nH	15.0 pF	18.0 n H	8.2 pF	0.0 Ω
HP 868 MHz	18.0 nH	22.0 nH	3.0 pF	1.2 pF	120.0 nH	3.6 pF	18.0 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0.0 Ω

The 169 MHz Class E multilayer DT match has a significantly different structure as shown in Figure 7. The element values are given in Table 16. The value of CC2 is 470 pF. Also, here, the 470 nH Lchoke inductor is a 0603 sized one because this value does not exist in the 0402 size. Currently, the 169 MHz DT match exists with multilayer inductors only.

Table 16. Matching Network Component Values at 169 MHz (Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Multilayer Inductor)

Pout=+10 dBm																	
RX Side				TX Side													
LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	LM2	CM2	LM3	CM3	LM4	CP1	CP2	Lchoke	R_{DC}
220 nH	150 nH	12.0 pF	6.2 pF	470 nH	39 pF	22 nH	6.8 pF	56 nH	47 nH	18 pF	68 nH	18 pF	47 nH	3 pF	2 pF	470 nH	0 Ω

A summary of typical measured output power, current consumption and sensitivity in RX mode (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 17. These results are obtained with a supply voltage of V_{DD} = 3.3 V. The multilayer inductor versions usually has worse efficiency and sensitivity. The 13 dBm power range can be achieved at 868 and 915M with the dual band (868–915M) 10 dBm matches as well. However, for that the maximum (0x4F) power state must be used. Also, with multilayer inductors, the dual band match cannot achieve the 13 dBm at 915M.

But, there is a possibility for tuning: by increasing the CM value (to 4.7pF), the power at maximum power state increases, and even the multilayer 10 dBm match achieves 13.1 dBm (with 26.5 mA) at 915M. However, with 4.7 pF CM, the efficiency becomes worse, and, thus, the 10 dBm power (10.2 dBm) is achieved only at power state 0x22 with 20.6 mA.

The high power (HP) 868 match can achieve the 13 dBm with large margin (i.e. in a power state significantly lower than maximum) even with multilayer inductors. Unfortunately, at 434M, even the high power match cannot achieve the 13 dBm with multilayer inductors.

Table 17. Output Power, Current Consumption and RX Sensitivity vs. Frequency (Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)

Pout = +10 dBm								
Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
169 MHz	TBD	TBD	TBD	TBD	23h	10.3 dBm	18.4 mA	–102.8 dBm
434 MHz	1Ah	10.2 dBm	16.9 mA	–106.1 dBm	2Ah	10.3 dBm	17.1 mA	–103.1 dBm
868-915M, 868M op.	20h	10.5 dBm	19.7 mA	–104.2 dBm	20h	10.7 dBm	19.7 mA	–103.2 dBm
868-915M, 915M op.	20h	10.5 dBm	19.6 mA	–104.1 dBm	20h	10.3 dBm	19.3 mA	–102.9 dBm

Table 17. Output Power, Current Consumption and RX Sensitivity vs. Frequency (Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)

Pout = +12...13 dBm								
HP 434 MHz	3Fh	13.3 dBm	23.0 mA	–105.2 dBm	4Fh	12.3 dBm	23.3 mA	–104.2 dBm
HP 868 MHz	44h	14.3 dBm	25.6 mA	–104.2 dBm	3Ch	13.3 dBm	24.1 mA	–102.0 dBm
868-915M, 868M op.	4Fh	13.7 dBm	25.5 mA	–104.2 dBm	4Fh	13.4 dBm	24.7 mA	–103.3 dBm
868-915M, 915M op.	4Fh	13.3 dBm	24.7 mA	–104.1 dBm	4Fh	12.4 dBm	23.7 mA	–103.3 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 2 dB of those obtained with the Split TX/RX board configuration.

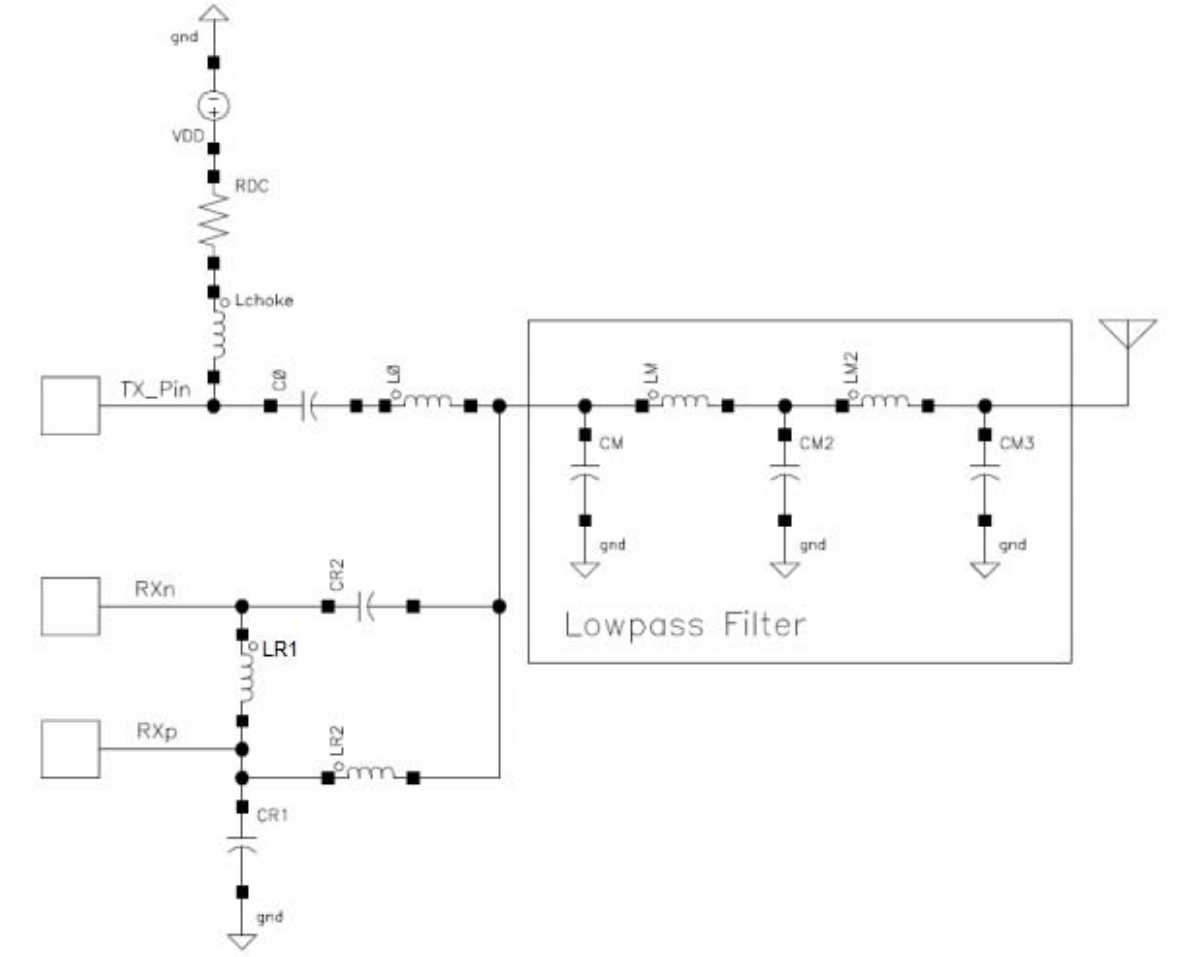

Figure 6. Matching Topology for Single Antenna with Si4460/67 Direct Tie CLE Board Configuration

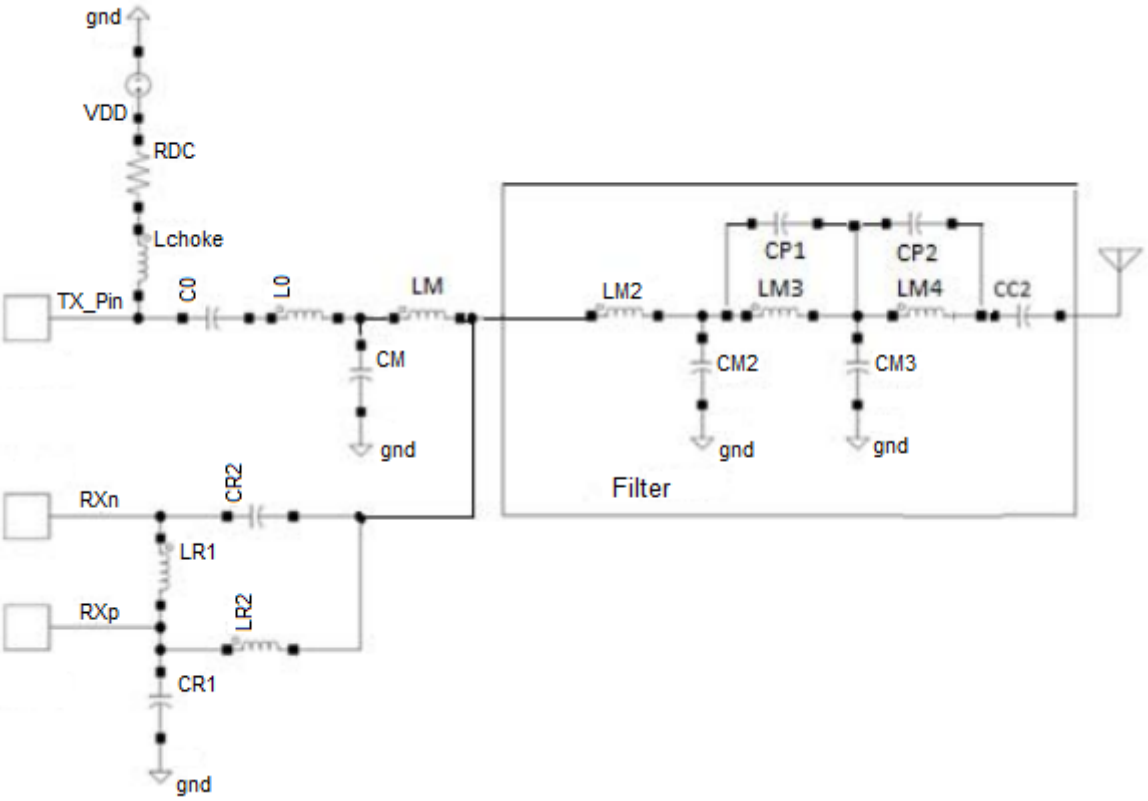

Figure 7. Matching Topology for Single Antenna with Si4460/67 Direct Tie CLE Board Configuration at 169 MHz

The vdd dependency of the power of the 434M 10 dBm CLE DT is shown in Table 18. As mentioned earlier, the power of the CLE match varies with the square of the Vdd change.

Table 18. Output Power, Current Consumption vs. Vdd (Direct Tie Si4460/67 434M CLE Board, WW Inductors)

Vdd	Fix Power Level 1A			Adaptive Power Level		
	power[dBm]	current[mA]	power st	power[dBm]	current[mA]	power st
3.5	10.2	17.2	1A	10.2	17.2	1A
3.3	10.2	17.1	1A	10.2	17.1	1A
3	10.1	16.6	1A	10.2	16.8	1B
2.7	9.6	16.1	1A	10.2	16.7	23
2.4	8.6	14.9	1A	9.9	16.3	4f
2.1	7.6	14.3	1A	8.8	15.5	4f
1.8	6.3	13.6	1A	7.6	14.7	4f
delta	**3.9 dB**			**2.6 dB**		
delta 2.4…3.3V	**1.6 dB**			**0.3 dB**		

Since the match works in a strongly reduced power level setting (DDAC), there is room for compensation at low Vdds. During this compensation, the power setting can be increased to reduce the internal switching loss and thus maintain the power as much as possible. For this, monitoring of the Vdd level is required. This so called “adaptive power control” method gives significant improvement of the Vdd flatness, especially in the most critical 2.4–3.3 V Vdd range. The result with the “adaptive power control” are also given in the table.

The flatness characteristics can be seen here to be typical for 10 dBm Si4060/4460/67 CLE and SQW matches operating on other bands as well.

At 13 dBm power levels, the Si4060/4460/67 CLE matches are working close to the maximum power state; so, the adaptive power control is not efficient there.

2.2.3. Si4060/4460/67 with Split TX\RX SWC Board Configuration: Component Values and Performance

The Si4460/67 SWC match were realized only in Direct Tie configuration. It will be detailed in section 2.2.4. If one would like to make a split TX/RX configuration or TX only match for Si4060, please use the TX path of the DT solution (Table 18). For the RX path, in split configuration, the Rx part of the CLE DT matches is recommended to use (LR1, LR2, CR1 and CR2 in Table 13 and 14) as the SWC DT matches may use other than 50 Ω RX match input impedances.

The power and current consumption of the split solution in TX mode is very close to the DT results (Table 19).

Important to note that these SWC matches are designed for flat (dP<~1.2 dB in the 1.8…3.8 V Vdd range) power and not for the highest efficiency. Due to this the impedance level of the match is lower and thus requires higher current for the same power.

2.2.4. Si4460/67 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance

Table 19 provides the component values required for output power levels of +10 dBm, using the Single Antenna with Direct Tie SWC board configuration of Figure 8 and a supply voltage of VDD = 3.3 V. The matches are working with low cost multilayer inductors. For other frequencies pls. consult with a Silicon Labs representative.

Table 19. Match Network Component Values vs. Frequency (Direct Tie Si4460/67 SWC Board, VDD = 3.3 V, Multilayer Inductors)

Pout = +10 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	CM	LM	CM2	LM2	CM3	LM3	CM4
315 MHz	82 nH	68 nH	7.5 pF	3.6 pF	270 nH	470 pF	3.9 pF	27 nH	8.2 pF	22 nH	8.2 pF	0 Ω	N.F.
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	270 pF	1.8 pF	22 nH	8.2 pF	18 nH	15.0 pF	18.0 nH	8.2 pF
868 MHz	18 nH	27 nH	3.0 pF	1.2 pF	120 nH	68 pF	N.F.	8.2 nH	5.1 pF	6.2 nH	5.1 pF	0 Ω	N.F.
915 MHz	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	56 pF	N.F.	6.8 nH	3.9 pF	6.8 nH	3.9 pF	0 Ω	N.F.

The value of CC1 capacitor is equal to the value of C0 in Table 19.

A summary of typical measured output power, current consumption and sensitivity (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 20. These results are obtained with a supply voltage of VDD = 3.3 V.

Table 20. Output Power, Current Consumption and Sensitivity vs. Frequency (Direct Tie Si4460/67 SWC Board, VDD = 3.3 V, Multilayer Inductors)

Pout = +10 dBm					
Freq Band	**OB[5:0]**	**DDAC[6:0]**	**Pout (dBm)**	**IDC (mA)**	**Sens. (dBm)**
315 MHz	0x21	0x44	10.28 dBm	23.50 mA	–103.9 dBm
434 MHz	0x2B	0x44	10.40 dBm	26.60 mA	–103.5 dBm
868 MHz	0x1E	0x44	10.50 dBm	23.70 mA	–102.0 dBm
915 MHz	0x22	0x44	10.40 dBm	24.20 mA	–102.7 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 1.5 dB of those obtained with the Split TX/RX board configuration.

The Vdd dependency of the flat SWC 4460/67 designs are given in Table 21. The flatness is 0.5…0.8 dB and 1–1.2 dB in the 2.1…3.3 V and 1.8…3.8 V Vdd range, respectively.

Table 21. Output Power, Current Consumption vs. Vdd (Direct Tie Si4460/67 SWC Board, Multilayer Inductors)

Vdd [V]	**315M 4460TSC10D315, PA_BIAS = 0x21, PA_PWR_LVL = 0x44**		**434M 4460TSC10D434, PA_BIAS = 0x2B, PA_PWR_LVL = 0x44**		**868M 4460TSC10D868, PA_BIAS = 0x1E, PA_PWR_LVL = 0x44**		**915M 4460TSC10D915, PA_BIAS = 0x22, PA_PWR_LVL = 0x44**	
	Pout [dBm]	**Idc [mA]**	**Pout [dBm]**	**Idc [mA]**	**Pout [dBm]**	**Idc [mA]**	**Pout [dBm]**	**Idc [mA]**
1,8	9.34	22.2	9.34	24.83	9.28	22.7	9.27	23.76
2.1	9.85	22.53	9.95	25.3	9.66	22.72	9.68	23.52
2.4	10.15	22.89	10.26	25.76	10.15	23.07	9.97	23.67
2.7	10.27	23.31	10.39	26	10.28	23.2	10.23	24.04
3	10.28	23.39	10.39	26.46	10.48	23.59	10.39	24.15
3.3	10.28	23.45	10.4	26.6	10.5	23.66	10.44	24.2
3.6	10.28	23.54	10.4	26.7	10.5	23.73	10.49	24.33
3.8	10.29	23.62	10.4	26.83	10.51	23.8	10.5	24.4
delta (2.1–3.3 V)	0.43 dB	0.92	0.45 dB	1.3	0.84 dB	0.94	0.76 dB	0.68
delta (1.8–3.8 V)	0.95 dB	1.42	1.06 dB	2	1.23 dB	1.1	1.23 dB	0.64

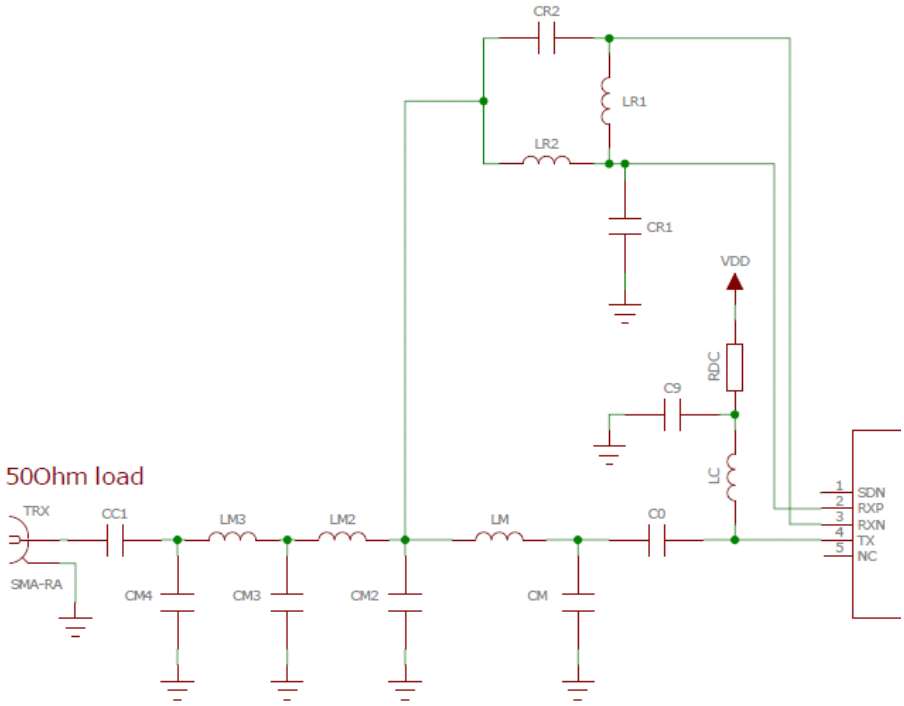

Figure 8. Matching Topology for Single Antenna with Direct Tie SWC Board Configuration

3. Switched Current (SWC) Matching Procedure Overview

3.1. SCW Matching Design for Split TX/RX Boards

In this section, the procedure for matching the Si4461 RFIC on a Split TX/RX board with SWC matching type is discussed in detail. The Si4060/Si4460/67 SWC matching use the same procedure only the target external load impedance is different due to the lower power level and lower IC shunt output capacitance. The main steps in the matching procedure are summarized below:

1. Measure the typical PA shunt output capacitance (C_{PA}) and resistance (R_{PA}) of the chip.
2. Choose L_{CHOKE} (pull-up inductor) for high impedance at the desired frequency of operation.
3. Select/calculate internal load resistance R_{LOAD_INT} for the desired output power level.
4. Calculate PA bias current setting.
5. Calculate required external load impedance Z_{LOAD} to present to the TX pin.
6. Construct a simple 2-element L-C matching network to transform the antenna load impedance (typically R_{ANT} = 50 Ω) to the calculated PA load impedance Z_{LOAD}.
7. Add sections of lowpass filtering (while maintaining the desired impedance transformation ratio), necessary to attenuate the harmonic levels below the applicable regulatory standard.

3.1.1. Measurement of PA Shunt Output Capacitance/Resistance (C_{PA}/R_{PA})

The output of the PA may be modeled as a shunt resistor R_{PA} in parallel with a shunt capacitor C_{PA} as illustrated in Figure 9. The values of R_{PA} and C_{PA} are not constant but instead vary over the frequency range of the Si4461 chip. It is necessary to determine the values of both R_{PA} and C_{PA} prior to constructing a matching network. The shunt output capacitance and resistance of the PA may be measured using a network analyzer.

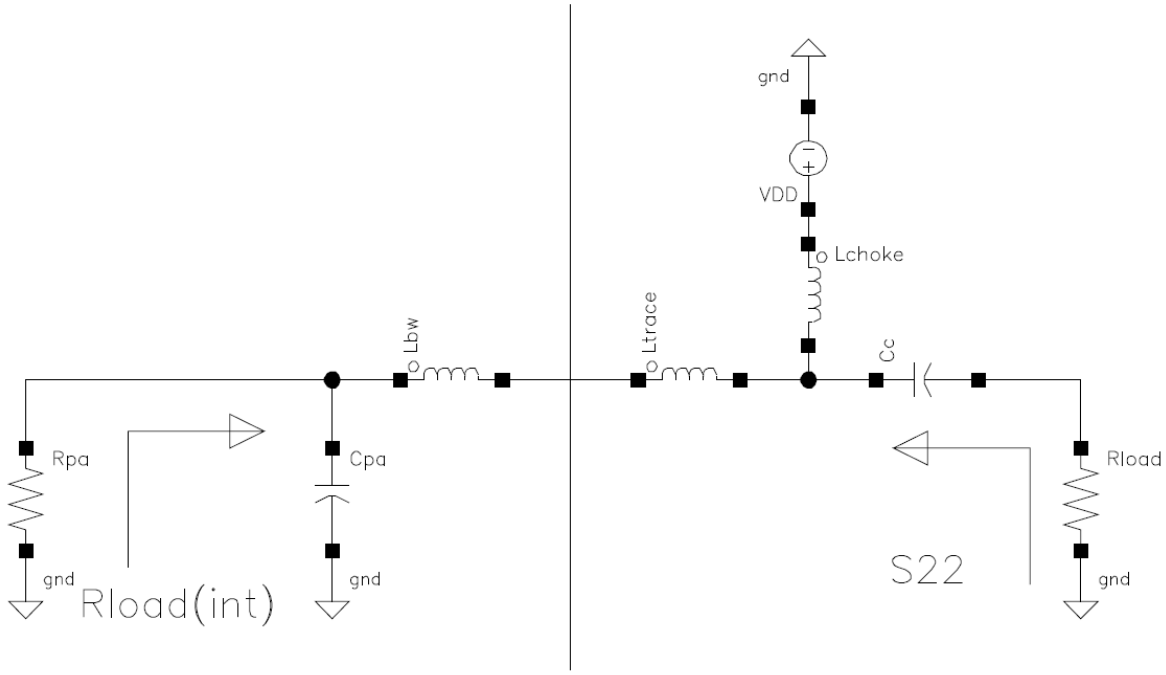

Figure 9. Model of PA Output Circuit and Impedance Measurement Network

DC bias to the PA output circuit is provided through a pull-up inductor, L_{CHOKE}. The value of this pull-up inductor should be chosen to present a very high impedance at the desired frequency of operation, such that it has no effect upon the impedance measurement. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 270 to 390 nH
- 470 MHz: approximately 220 nH
- 868 MHz: approximately 120 nH
- 915 MHz: approximately 100 nH

The network analyzer is connected to the TX output pin and pull-up inductor through a dc blocking capacitor to ensure that the VDD supply voltage does not damage the port of the network analyzer. The Si4461 chip is configured for CW TX operation at a frequency close to (but not directly at) the desired frequency of operation. The reason for this is that the chip is transmitting a signal (although at lower power) that is not correlated with the swept signal from the network analyzer. The network analyzer displays this anomalous signal as a “spike” in the S-parameter curve with the amplitude of the spike growing as the output power is increased. Thus, it is convenient to move this spike slightly to one side of the frequency at which we desire to place the measurement marker. Also, it is advisable to configure the chip for a relatively low value of output power in order to prevent damage to the input of the network analyzer. By trial-and-error, one can observe that the value of shunt output capacitance and resistance does not appear to be significantly influenced by the number of PA device fingers selected (i.e., PA_DDAC property setting).

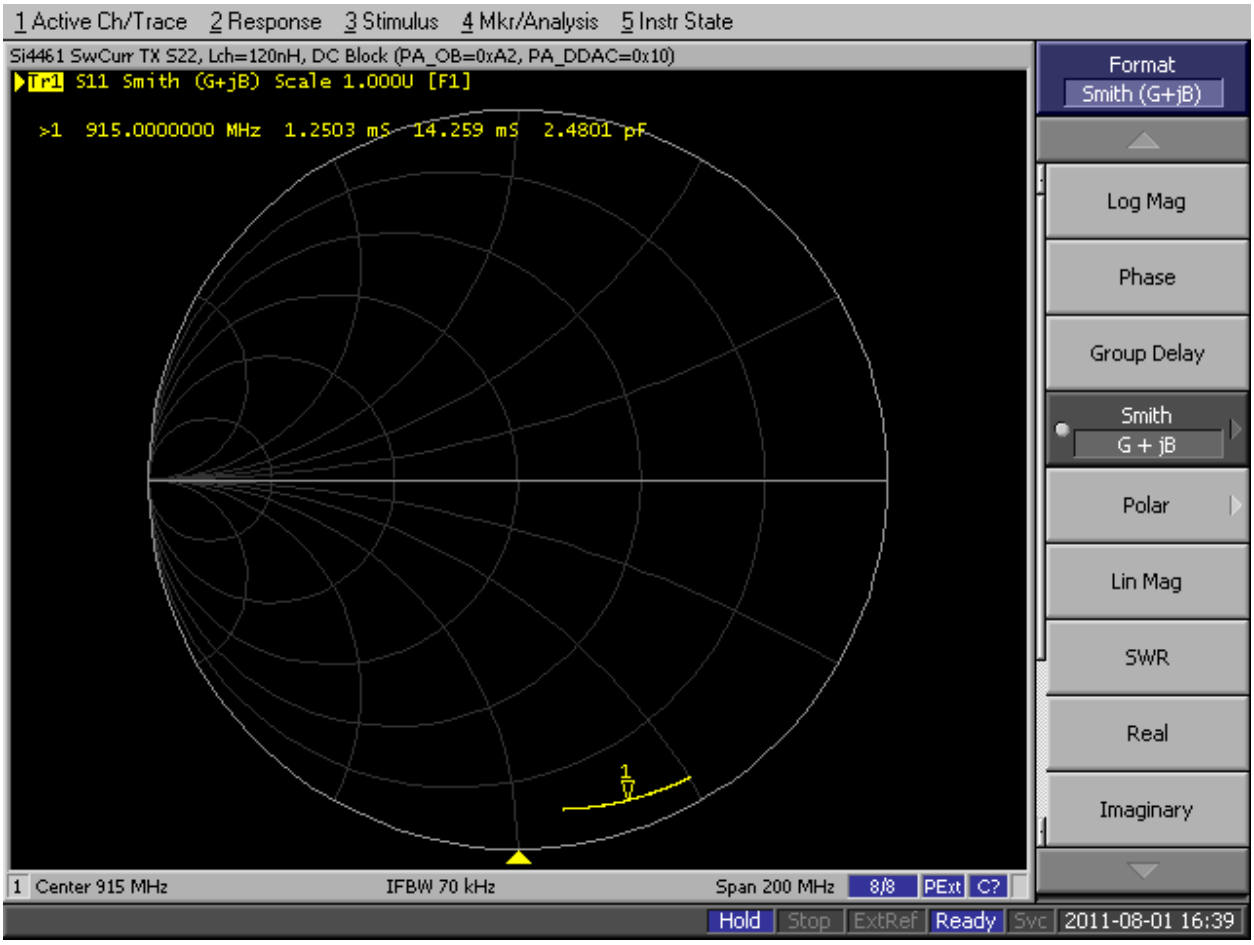

Figure 10. Si4461 PA Shunt Output Capacitance at 915M (TX Mode)

The plot of Figure 10 illustrates the measured value of output admittance (with L_{CHOKE} = 100 nH) at 915 MHz to be $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 1.25 + j14.26 ms. The output admittance may be measured at each desired frequency (with an appropriate selection of pull-up inductor L_{CHOKE}) and is found to be the following:

- 169 MHz (L_{CHOKE} = 470 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.010 + j1.79 ms
- 315 MHz (L_{CHOKE} = 390 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.207 + j2.87 ms
- 470 MHz (L_{CHOKE} = 220 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.291 + j4.96 ms
- 868 MHz (L_{CHOKE} = 120 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 1.07 + j12.93 ms
- 915 MHz (L_{CHOKE} = 100 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 1.25 + j14.26 ms

These admittance values are quite repeatable from chip to chip; so, these published values may be used by the designer without the need to remeasure each application.

However, it is apparent that this measured value of output admittance does *not* represent the equivalent internal shunt PA capacitance and resistance. This is due to the impedance-transforming effect of the series bond wire and trace inductance as illustrated in Figure 9. As seen from outside the chip, the apparent value of shunt PA resistance will appear to be lower than the actual internal value. Additionally, the apparent value of shunt PA capacitance will appear to be higher than the actual internal value.

The actual internal values may be calculated if the total value of series inductance ($L_{SERIES} = L_{BW} + L_{TRACE}$) is known. Although this value of inductance is not known precisely, it is reasonably estimated to be L_{SERIES} = 2.9 nH (L_{BW} = 1 nH, L_{TRACE} = 1.9 nH). With a bit of mathematical manipulation, the formulas for the equivalent internal PA resistance and capacitance values may be derived as follows:

$$Z_{OUT} = R_{OUT} + jX_{OUT} = \left(\frac{1}{Y_{OUT}}\right) = \left(\frac{1}{G_{OUT} + jB_{OUT}}\right)$$

Equation 1.

$$R_{OUT} = \left(\frac{G_{OUT}}{G_{OUT}^{\ 2} + B_{OUT}^{\ 2}}\right)$$

Equation 2.

$$X_{OUT} = \left(\frac{-B_{OUT}}{G_{OUT}^{\ 2} + B_{OUT}^{\ 2}}\right)$$

Equation 3.

$$Z_{OUT} = R_{OUT} + jX_{OUT} = \left(\frac{1}{G_{PA} + jB_{PA}}\right) + jX_{L_{SERIES}}$$

Equation 4.

$$G_{PA} + jB_{PA} = \left(\frac{1}{R_{OUT} + jX_{OUT} - jX_{L_{SERIES}}}\right)$$

Equation 5.

$$G_{PA} = \frac{1}{R_{PA}} = \frac{R_{OUT}}{R_{OUT}^{\ 2} + (X_{OUT} - X_{L_{SERIES}})^2}$$

Equation 6.

$$B_{PA} = 2\pi f C_{PA} = \frac{X_{L_{SERIES}} - X_{OUT}}{R_{OUT}^2 + (X_{OUT} - X_{L_{SERIES}})^2}$$

Equation 7.

From these equations, the following values of internal PA shunt resistance and capacitance are obtained:

- 169 MHz: R_{PA} = 101 kΩ, C_{PA} = 1.68 pF
- 315 MHz: R_{PA} = 4991 Ω, C_{PA} = 1.427 pF
- 470 MHz: R_{PA} = 3735 Ω, C_{PA} = 1.611 pF
- 868 MHz: R_{PA} = 1356 Ω, C_{PA} = 1.970 pF
- 915 MHz: R_{PA} = 1226 Ω, C_{PA} = 2.006 pF

3.1.1.1. Impedance Values for Si4060/Si4460/67 SWC Configurations

As mentioned earlier, the SWC match design process flow is the same for the Si4060/Si4460/67, but the chip output impedance, power level, current magnitude (and thus the R_{LOAD_INT}) are different. In this step, the measured Si4060/Si4460/67 output admittances and internal RC equivalents are given:

The Si4060/Si4460/67 output admittance is measured at each desired frequency (with an appropriate selection of pull-up inductor L_{CHOKE}) and is found to be as follows:

- 169 MHz (L_{CHOKE} = 470 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.75 + j1.01 ms
- 315 MHz (L_{CHOKE} = 390 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.18 + j1.74 ms
- 434 MHz (L_{CHOKE} = 220 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.25 + j2.36 ms
- 470 MHz (L_{CHOKE} = 220 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.25 + j2.88 ms
- 868 MHz (L_{CHOKE} = 120 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.79 + j7.57 ms
- 915 MHz (L_{CHOKE} = 100 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.84 + j7.85 ms

The Si4060/Si4460 internal PA shunt resistance and capacitance values are obtained via Equations 1 to 7:

- 169 MHz: R_{PA} = 1330 Ω, C_{PA} = 0.95 pF
- 315 MHz: R_{PA} = 5670 Ω, C_{PA} = 0.87 pF
- 434 MHz: R_{PA} = 4100 Ω, C_{PA} = 0.85 pF
- 470 MHz: R_{PA} = 4150 Ω, C_{PA} = 0.95 pF
- 868 MHz: R_{PA} = 1590 Ω, C_{PA} = 1.24 pF
- 915 MHz: R_{PA} = 1530 Ω, C_{PA} = 1.21 pF

3.1.2. Selection/Calculation of R_{LOAD_INT}

Successfully obtaining the desired level of output power while minimizing current consumption or achieving Vdd flatness depends strongly upon the load resistance presented to the PA. However, it is important to distinguish between the load impedance presented to the TX pin (R_{LOAD}) and the impedance present at the drain of the output devices internal to the chip (R_{LOAD_INT}). These values are different due to the impedance-transforming effect of the series bond wire inductance and trace inductance (discussed in the previous section). It is apparent that, due to the series inductance (L_{BW}-L_{TRACE}) and internal shunt PA capacitance (C_{PA}), the effective internal load resistance R_{LOAD_INT} is larger than R_{LOAD}. The total internal load resistance (R_{TOTAL}) seen by the PA output device is the parallel combination of R_{PA} and R_{LOAD_INT}.

The power extracted from the PA output devices may be readily calculated as $P_{PA} = I_{PA}^2 \times R_{TOTAL}$. Note that the power sourced from the PA output devices (P_{PA}) is not the same as the power delivered (P_{OUT}) to the load impedance, R_{LOAD}, because some power is dissipated in the internal PA resistance, R_{PA}. For a given value of PA output current I_{PA}, the output power may be increased by presenting a larger total load impedance. Obviously, this statement only holds true for sufficiently small values of R_{TOTAL}, such that clipping of the peaks of the drain voltage waveform does not occur. That is to say, the voltage swing at the drain of the output device must be held to a reasonably low value. A reasonable design constraint is to keep the peak drain voltage swing at $V_{PK} \leq V_{DD} - 0.7$ V. This provides some voltage headroom on the output devices to ensure they remain in a linear region and continue to operate as switched current sources. It also allows for some tolerance against variations in supply voltage; if the output devices remain in a linear operating region, the output power is not significantly a function of supply voltage. The voltage peak at the internal drain node is *not* the same value as may be measured at the TX output pin of the device (again due to the impedance transforming effects of the series inductance).

It is also clear that, if the desired output power level is low enough, drain voltage clipping is not a concern. There are many combinations of I_{PA} and R_{TOTAL} that will theoretically provide the target value of P_{PA} and thus also P_{OUT}. Optimal current efficiency is obtained by selecting the lowest possible value of I_{PA} (i.e., highest value of R_{TOTAL}) that will result in a drain voltage waveform that remains just below clipping amplitude at the operation supply voltage. However, if the design target is the flat power vs. Vdd characteristic, the load impedance has to be decreased to avoid clipping even at the lowest possible supply level. In this case, the current efficiency will not be optimal at higher Vdd levels because the target power is achieved with lower voltage swing (and higher current magnitude) optimized for the low Vdd level. In other words, efficiency has to be sacrificed to achieve flatness.

On the other side, If the design target is the highest efficiency at a given supply voltage, the value of R_{TOTAL} cannot be made arbitrarily large; it is self-evident that it cannot be larger than the internal equivalent parallel resistance of the PA itself (R_{PA}). The limiting case would occur if the transformed value of load impedance (R_{LOAD_INT}) was infinite, such that $R_{TOTAL} = R_{PA} // R_{LOAD\_INT} \approx R_{PA}$. In such a case, all of the output power would be dissipated in the output devices themselves rather than being delivered to the load impedance. Thus, the incremental benefit to PA efficiency diminishes as R_{LOAD} (and thus R_{LOAD_INT}) is raised to higher and higher values.

The output impedance measurements of the previous section indicate that the internal parallel output resistance of the PA output device is R_{PA} = 1226 Ω (using the Si4461 at 915 MHz as an example. For the Si4060/4460/67, the Rpa is 1530 Ω). It is desirable to present an effective internal load impedance, R_{LOAD_INT}, that is significantly lower than the PA output resistance itself so that most of the power is delivered to the load and not dissipated in the PA output devices. However, this constraint is weakly defined; so, there are many possible values of R_{LOAD_INT} that could be considered as satisfactory. It is necessary to provide further design constraints or “rules of thumb” in order to select an appropriate value of R_{LOAD_INT}.

One factor to consider is the impedance transformation factor required from the external matching network. The antenna load impedance (into which the output power must eventually be delivered) is typically a low value, such as 50 Ω. The external matching network must transform this antenna impedance (R_{ANT}) into the load impedance (R_{LOAD}) seen at the TX pin, which is then further transformed by the series bond wire/trace inductance into the internal load resistance (R_{LOAD_INT}). The Q-factor of the external matching network is approximately proportional to the square root of the ratio R_{LOAD}:R_{ANT}, and thus, as R_{LOAD} is made larger, the required Q-factor of the external network also increases. If the required impedance transformation ratio is too large, the loss of the external matching network may increase, and tuning of the circuit may become sensitive to component tolerances.

An additional factor to consider is the amount of power dissipated in the internal PA devices that is considered

acceptable. This is a loss term that decreases current efficiency; so, it is desirable to make it as small as possible. As the internal PA resistance R_{PA} is not infinite, this loss term cannot be made zero. However, it can be minimized by making the value of R_{LOAD_INT} small in comparison to R_{PA}, such that most of the power is delivered to the output load and not dissipated in the PA devices.

Thus the selection criteria for R_{LOAD_INT} may be summarized as follows:

- A large value of R_{LOAD_INT} increases R_{TOTAL}, thereby improving the current efficiency (by requiring a lower value of I_{PA} for a given target value of P_{PA}).
- A small value of R_{LOAD_INT} decreases the percentage of power dissipated in the internal PA resistance.
- A small value of R_{LOAD_INT} decreases the impedance transformation ratio required from the external matching network, thus decreasing losses due to finite Q of discrete components and improving sensitivity to component tolerances.
- A small value of R_{LOAD_INT} ensures that the peak drain voltage does not exceed levels where clipping may occur. This is the most important condition for flat power vs. Vdd characteristic, even at the lowest Vdd limit.

Given these somewhat conflicting design goals, the selection of R_{LOAD_INT} is made as a compromise to partially satisfy all four criteria and is stated as the following rule-of-thumb:

R_{LOAD_INT} shall be chosen as large as possible while not exceeding $R_{PA}/5$ or 5 x R_{ANT}, while remaining low enough to ensure $V_{PK} < V_{DD} – 0.7$ V (with flat VDD design, the VPK can be fine-tuned during bench evaluation to satisfy the specification).

In the Si4461 high-efficiency match design example at 915 MHz with R_{PA} = 1226 Ω, R_{ANT} = 50 Ω, and a target output power level of +14 dBm, this rule of thumb leads to choosing $R_{LOAD\_INT} \approx 90$ Ω (limited by the V_{PK} design constraint at 3.3 V Vdd, as will be shown shortly). A larger value of R_{LOAD_INT} may be selected if the target output power level is reduced (e.g., $R_{LOAD\_INT} \approx 120$ Ω for P_{OUT} = +13 dBm). Similarly, for +10 dBm high-efficiency Si4060/Si4460/67 SWC solutions, $R_{LOAD\_INT} \approx 240$ Ω is the optimum. For flat power design, the optimum impedance is around 50 Ω for 13 dBm and 120–140 Ω for 10 dBm.

3.1.3. Calculation of PA Bias Current I_{PA}

The total load resistance is readily calculated as the parallel combination of R_{LOAD_INT} and R_{PA}. In our Si4461 14 dBm example:

$$R_{TOTAL} = \frac{1}{\left(\frac{1}{R_{PA}}\right) + \left(\frac{1}{R_{LOAD\_INT}}\right)} = \frac{1}{\left(\frac{1}{1226}\right) + \left(\frac{1}{90}\right)} = 83.84\ \Omega$$

Equation 8.

The finite value of R_{PA} implies that some output power will be internally dissipated in the output device itself, and thus the power delivered to the load will be less than that obtained from straightforward calculations of $P = I^2 \times R$. This loss factor may be calculated as:

$$P_{LOSS\_INT} = 10 \log\left(\frac{R_{PA}}{R_{PA} + R_{LOAD\_INT}}\right) = 10 \log\left(\frac{1226}{1226 + 90}\right) = –0.31\ \text{dB}$$

Equation 9.

This internal loss is unavoidable; it is simply necessary to adjust the PA bias current for a higher level in order to compensate for this power loss.

If the external matching network is assumed to be lossless (i.e., discrete matching components with infinite Q), the only loss in the circuit is due to P_{LOSS_INT}. For a target output power P_{OUT} delivered to the load, the PA current may be calculated as the following:

$$I_{PA} = \sqrt{\frac{P_{PA}}{R_{TOTAL}}} = \sqrt{\frac{P_{OUT} - P_{LOSS}}{R_{TOTAL}}}$$

Equation 10.

If the desired output power level is chosen as P_{OUT} = +14 dBm = 25 mW, P_{PA} = 14.0 + 0.31 = 14.31 dBm = 27.0 mW and the PA current may be calculated as follows:

$$I_{PA} = \sqrt{\frac{0.0270}{83.84}} = 17.95 \text{ mA}$$

Equation 11.

Thus, I_{PA} = 17.95 mA (RMS) or 25.38 mA peak current (50.76 mA pk-pk) at the fundamental frequency. This current amplitude would theoretically result in peak *internal* drain voltage swing of $V_{PEAK} = I_{PA\_PEAK}$ x R_{TOTAL} = 25.38 mA x 83.84 Ω = 2.13 Vpk. This peak drain voltage swing appears acceptably small to ensure linearity (non-clipping), assuming a supply voltage of VDD ≥ V_{PEAK} + 0.7 V = 2.83 V. However, this voltage calculation takes into account only the peak voltage at the *fundamental* frequency. The square-wave current pulse delivered by the switched output devices is presented with a considerably different load impedance at harmonic frequencies; the resulting harmonic voltage components may add to the fundamental to result in a somewhat larger peak drain voltage than that calculated above. Therefore, it may be prudent to allow for a slightly greater voltage headroom, if flatness of power vs. VDD is a design goal.

As the output power is theoretically a function of only I_{PA} and R_{LOAD_INT}, the output power should not vary with changes in supply voltage as long as I_{PA} remains at its programmed value. If greater tolerance against a reduction in supply voltage is desired, it would be necessary to select a lower target value for R_{LOAD_INT}; this would result in a lower peak voltage swing (at the expense of an increase in the required value of I_{PA} and thus overall current consumption of the chip).

The PA output devices operate as programmable switched current sources and, ideally, deliver square wave pulses of current to the load. The amplitude of these square wave current pulses is programmable through the properties PA_PWR_LVL at 0x2201 and PA_BIAS_CLKDUTY at 0x2202. The value of PA bias current per transistor unit finger (in increments of 10 µA) is configured by the OB[5:0] field in the PA_BIAS_CLKDUTY property, while the total number of enabled transistor fingers is configured by the DDAC[6:0] field in the PA_PWR_LVL property. The total amplitude of the square wave current pulse is the product of these two values. As an example, if the OB[5:0] field is set to 0x22 = 34d and the DDAC[6:0] field is set to 0x64 = 100d, the programmed amplitude of the current pulse is I_{BIAS} = 34.0 mA (34 x 10 µA per finger x 100 fingers). Since the amplitude of the current pulse is a product of two values, it is often possible to obtain the same bias current amplitude with different combinations of settings. Silicon Labs recommends using a nominal value of DDAC[6:0] = 0x64 = 100 fingers and then selecting OB[5:0] as required; this allows for both upwards and downwards adjustment range if fine tuning of the output power is required.

The previously-calculated value for I_{PA_PK} of 25.38 mA represented the required current amplitude at the fundamental frequency. This is not the same as the amplitude of the square wave current pulse configured through the OB[5:0] and DDAC[6:0] fields. The relationship between the amplitude of a 50% duty cycle square wave pulse train and the amplitude of its fundamental component may be found through Fourier analysis to be:

$$I_{BIAS} = 2 \times I_{PA\_PK} \times \left(\frac{\pi}{4}\right) = 2 \times 25.38 \text{ mA} \times \left(\frac{\pi}{4}\right) = 39.9 \text{ mA}$$

Equation 12.

This value of bias current could be obtained by setting OB[5:0] = 0x28 = 400 µA per finger and DDAC[6:0] = 0x64 = 100 fingers, for a total square wave current pulse amplitude of 40.0 mA. The average (dc component) of this 50% duty cycle current pulse is half of the amplitude: $I_{BIASDC} = I_{BIAS}/2$ = 19.95 mA.

This analysis assumes a square waveform with 50% duty cycle. The duty cycle of the current pulse may be adjusted to other selected values through the CLK_DUTY[1:0] field in the PA_BIAS_CLKDUTY property. The analysis for other values of duty cycle is not discussed here.

3.1.4. Calculation of Required Z_{LOAD} at the TX Pin

It is desired that the PA output devices be presented with a purely-real load at the fundamental frequency (i.e., $Z_{TOTAL} = R_{TOTAL} + j0$). It is thus necessary to present a load impedance Z_{LOAD} at the TX pin that appears inductive, such that the inductive reactance cancels the internal shunt capacitance of the PA devices (C_{PA}). It is necessary to calculate the external load impedance that when placed in series with $L_{SERIES} = L_{BW} + L_{TRACE} \approx 2.9$ nH and then in shunt with $C_{PA} = 2.006$ pF results in $Z_{LOAD\_INT} = 90 + j0\ \Omega = R_{LOAD\_INT}$ (continuing our Si4461 design example at 915 MHz).

The required impedance value Z_{LOAD} to present to the TX pin may easily be determined through graphical means (e.g., Smith Chart) or through the use of the impedance transformation equation shown below.

$$Z_{LOAD} = Z_R + jZ_I = \left(\frac{G_{LOAD\_INT}}{G_{LOAD\_INT}^2 + B_{CPA}^2}\right) - j\left(X_{Lseries} - \frac{B_{CPA}}{G_{LOAD\_INT}^2 + B_{CPA}^2}\right)$$

Equation 13.

For our 14 dBm design example at 915 MHz, this may be calculated to be $Z_{LOAD} = 43.3 + j28.3\ \Omega$.

3.1.5. Transforming R_{ANT} into Z_{LOAD}

A simple two-element L-C match is thus required to transform the (assumed) 50 Ω antenna impedance to the calculated value of $Z_{LOAD} = 43.3 + j28.3\ \Omega$. The required component values are again found easily through use of a Smith Chart and are determined to be a shunt capacitor CM1 = 1.37 pF and series inductor LM1 = 7.9 nH. Standard 5% component tolerance values of CM1 = 1.2 pF and LM1 = 8.2 nH are considered sufficiently close, as shown in Figure 11.

If lower impedance required (for a flat Vdd characteristic) the LM1 can be reduced. To keep the ZLOAD_INT pure real at the internal TX pin slight increase of the CM1 is required: E.g. with LM1 = 5.6 nH and CM1 = 1.5 pF the resulted a ZLOAD_INT = ~64 Ω instead of the original ~90 Ω.

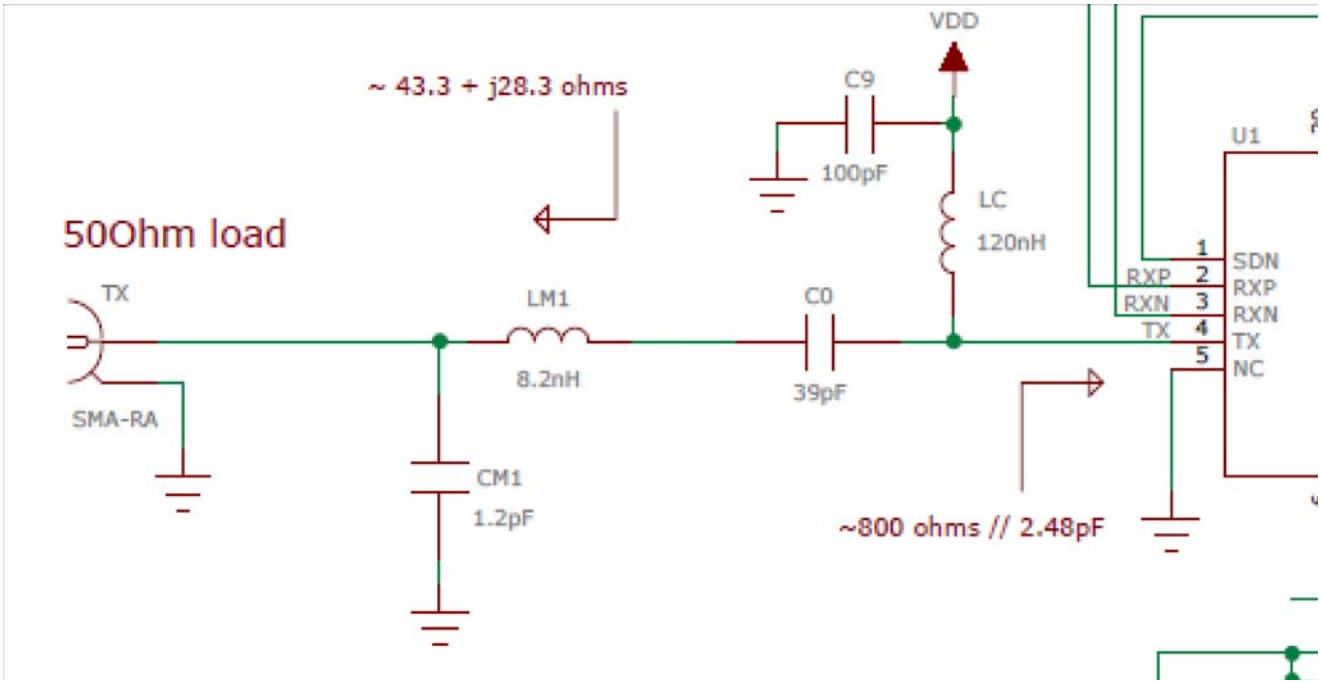

Figure 11. Simplified SwCurr Match for +14 dBm at 915 MHz

3.1.6. Verifying Initial TX Performance

The next step is to verify the performance of this simple SwCurr match. The match of Figure 11 was constructed on an RF test card and characterized. The measured performance for OB[5:0] = 0x28 (400 µA per finger), and DDAC[6:0] = 0x64 (100 fingers) was:

2-Element Match						
LM1	**CM1**	**DDAC**	**OB**	**V_{DD}**	**P_{OUT}**	**I_{DD}**
8.2 nH	1.2 pF	0x64	0x28	1.80 VDC	11.02 dBm	28.93 mA
				2.10 VDC	11.72 dBm	30.51 mA
				2.40 VDC	12.08 dBm	31.71 mA
				2.70 VDC	12.23 dBm	32.62 mA
				3.00 VDC	13.02 dBm	33.48 mA
				3.30 VDC	13.27 dBm	33.65 mA
				3.60 VDC	13.44 dBm	33.81 mA

The measured output power of +13.27 dBm for VDD = 3.3 VDC was about 0.73 dB below the target output power of +14.0 dBm. After some bench investigation, the following reasons were discovered for the discrepancy:

- The PA output resistance (R_{PA}) in large-signal conditions is somewhat lower than the small-signal value measured in "3.1.1. Measurement of PA Shunt Output Capacitance/Resistance (CPA/RPA)" on page 26. This results in a greater value of P_{LOSS} and thus a lower output power.
- The measured PA bias current (through L_{CHOKE}) was slightly lower than the programmed value, due to some compression in large-signal conditions. This also resulted in lower-than-calculated output power.

The value of PA bias current was increased to OB[5:0] = 0x2D (450 µA per finger) to compensate for the additional loss.

2-Element Match						
LM1	**CM1**	**DDAC**	**OB**	**V_{DD}**	**P_{OUT}**	**I_{DD}**
8.2 nH	1.2 pF	0x64	0x2D	1.80 VDC	11.22 dBm	29.78 mA
				2.10 VDC	12.14 dBm	32.00 mA
				2.40 VDC	12.71 dBm	33.57 mA
				2.70 VDC	12.93 dBm	34.59 mA
				3.00 VDC	13.71 dBm	35.45 mA
				3.30 VDC	14.05 dBm	35.67 mA
				3.60 VDC	14.26 dBm	35.85 mA

There is some reduction in output power as the VDD supply voltage is reduced; this is in agreement with our expectation of voltage clipping at supply voltages less than VDD ≈ 2.8 to 3.0 V. As stated in "2. Summary of Matching Network Component Values" on page 6, the Si4461 SWC 13 dBm 868M board designed for flat Vdd characteristic has only 1.5dB drop in the 1.8–3.8 V supply voltage range. This is due to the fact that the impedance (ZLOAD_INT) is lower (~60 Ω).

The measured conducted harmonics for the 915M simplified SwCurr match example are shown in Figure 12.

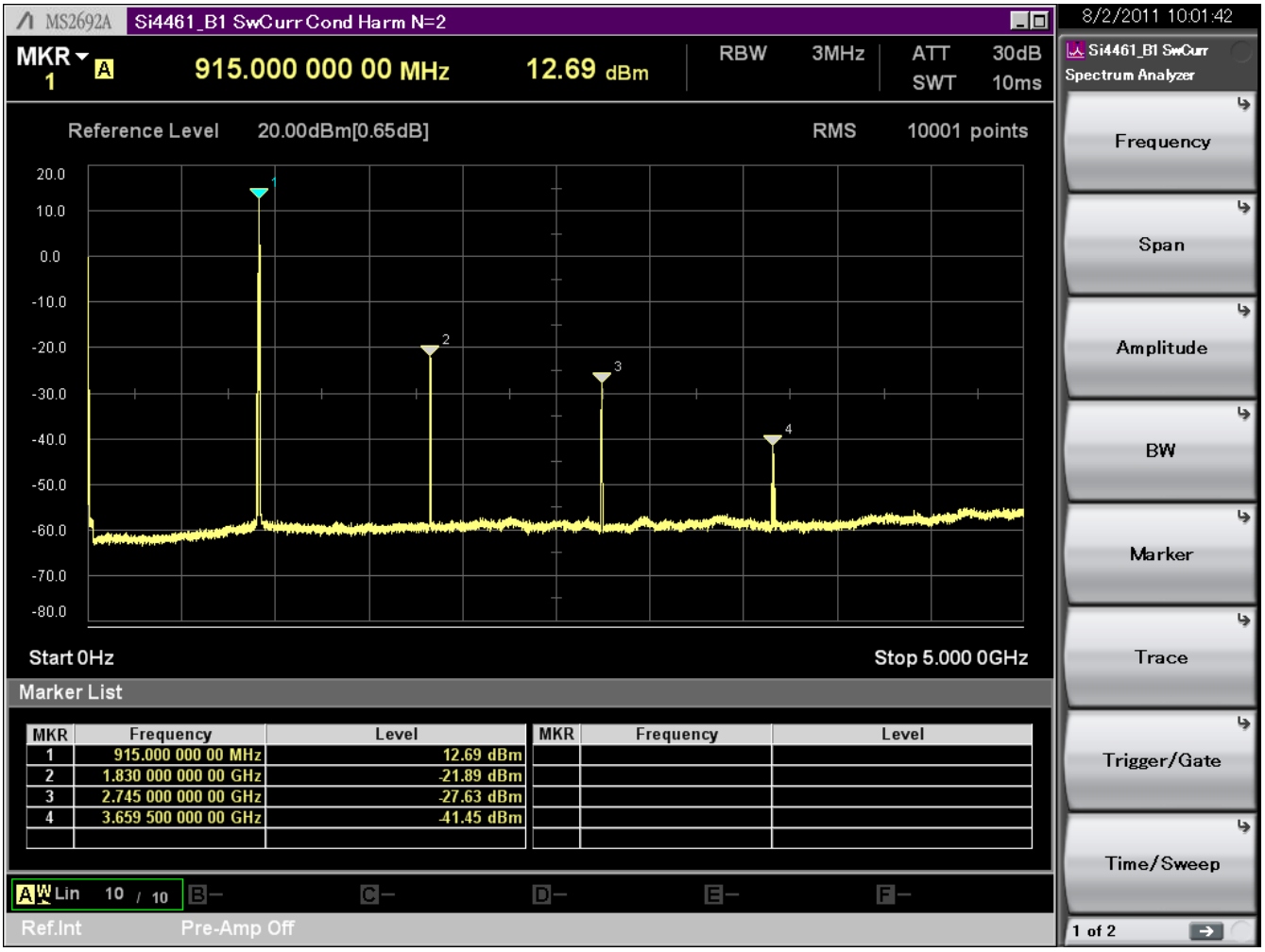

Figure 12. Conducted Harmonics for SwCurr Match at 915 MHz (N = 2)

3.1.7. Adding a Low-Pass Filter

Although this initial measured performance is reasonable, the level of harmonics is unacceptably high. It is necessary to increase the order of the lowpass filter to reduce these harmonic signals to a level that is compliant with applicable regulatory standards (e.g., ETSI, FCC).

Theoretically, it should be possible to add more stages of lowpass filtering without modifying the impedance presented to the TX pin. If this is accomplished, then the only degradation in performance should be due to the insertion loss of the additional filter components.

The SwCurr match configuration that was built and verified in the previous section was only a 2nd order lowpass filter structure (CM1 and LM1). From experience on past designs (e.g., Si443x chips), it is expected that the required order of lowpass filtering to be N=3 to 4 (for ETSI) or N=4 to 5 (FCC). Continuing our design example at 915 MHz, a higher-order lowpass filter is now designed that also attempts to maintain the target load impedance of Z_{LOAD} = 43.3 + j28.3 ohms.

Using a graphical Smith Chart program (WinSmith™), a 4th order low-pass filter was designed. It should provide improved harmonic attenuation while theoretically transforming R_{ANT} = 50 Ω to Z_{LOAD} = 43.3 + j28.3 Ω. This low-pass filter was installed on our test board, and the performance was remeasured.

4-Element Match						
LM1	**CM1**	**DDAC**	**OB**	**V_{DD}**	**P_{OUT}**	**I_{DD}**
15.0 nH	5.1 pF	0x64	0x2E	1.80 VDC	11.03 dBm	28.92 mA
				2.10 VDC	12.11 dBm	31.65 mA
LM2	**CM2**			2.40 VDC	12.78 dBm	33.72 mA
12.0 nH	3.9 pF			2.70 VDC	13.13 dBm	35.06 mA
				3.00 VDC	13.93 dBm	35.99 mA
				3.30 VDC	14.24 dBm	36.29 mA
				3.60 VDC	14.39 dBm	36.51 mA

A reduction in output power level may again be obtained with this same match by simply reducing the PA output bias current field OB[5:0]. Output power levels of +13 dBm, +10 dBm, or 0 dBm may be obtained with a bias current of 390 µA per finger (OB = 0x27), 260 µA per finger (OB = 0x1A), or 70 µA per finger (OB = 0x07), respectively. Note that, as the voltage swing is reduced (as a result of lowering the unit bias current), the variation of output power as a function of supply voltage is also reduced. This is in agreement with theory. If it is desired to obtain less variation of output power vs. VDD at higher output powers (e.g. +14 dBm), it is necessary to redesign the match to target a lower value of R_{LOAD_INT} and increase the PA bias current accordingly.

4-Element Match						
LM1	**CM1**	**DDAC**	**OB**	**V_{DD}**	**P_{OUT}**	**I_{DD}**
15.0 nH	5.1 pF	0x64	0x27	1.80 VDC	10.79 dBm	28.08 mA
				2.10 VDC	11.60 dBm	30.02 mA
LM2	**CM2**			2.40 VDC	12.05 dBm	31.48 mA
12.0 nH	3.9 pF			2.70 VDC	12.24 dBm	32.44 mA
				3.00 VDC	12.98 dBm	33.30 mA
				3.30 VDC	13.16 dBm	33.47 mA
				3.60 VDC	13.25 dBm	33.64 mA
		0x64	0x1A	1.80 VDC	9.34 dBm	24.50 mA
				2.10 VDC	9.59 dBm	25.22 mA
				2.40 VDC	9.69 dBm	26.08 mA
				2.70 VDC	9.75 dBm	26.86 mA
				3.00 VDC	10.14 dBm	27.59 mA
				3.30 VDC	10.20 dBm	27.70 mA
				3.60 VDC	10.25 dBm	27.82 mA
		0x64	0x07	1.80 VDC	0.27 dBm	15.12 mA
				2.10 VDC	0.13 dBm	15.80 mA
				2.40 VDC	0.10 dBm	16.68 mA
				2.70 VDC	0.08 dBm	17.46 mA
				3.00 VDC	0.27 dBm	18.12 mA
				3.30 VDC	0.31 dBm	18.22 mA
				3.60 VDC	0.34 dBm	18.33 mA

In practice, the value of PA output bias current is selected to nominally center the desired output power level. Further fine adjustment of the output power (upwards or downwards) may be accomplished by selecting a larger or smaller number of output device fingers (DDAC[6:0] field). The default value of DDAC used in the above measurements is 100 fingers (0x64). As the allowed range for this field is from 0 to 127 fingers, there remains room for upwards or downwards adjustment of the output power.

The measured conducted harmonics for VDD = 3.3 V, OB = 0x2E (460 µA per finger), and DDAC = 0x64 (100 fingers) for the schematic of Figure 14 are shown in Figure 13 below. These conducted levels of harmonics now comply with the Radiated Spurious Emission requirements of FCC Part 15.205/209.

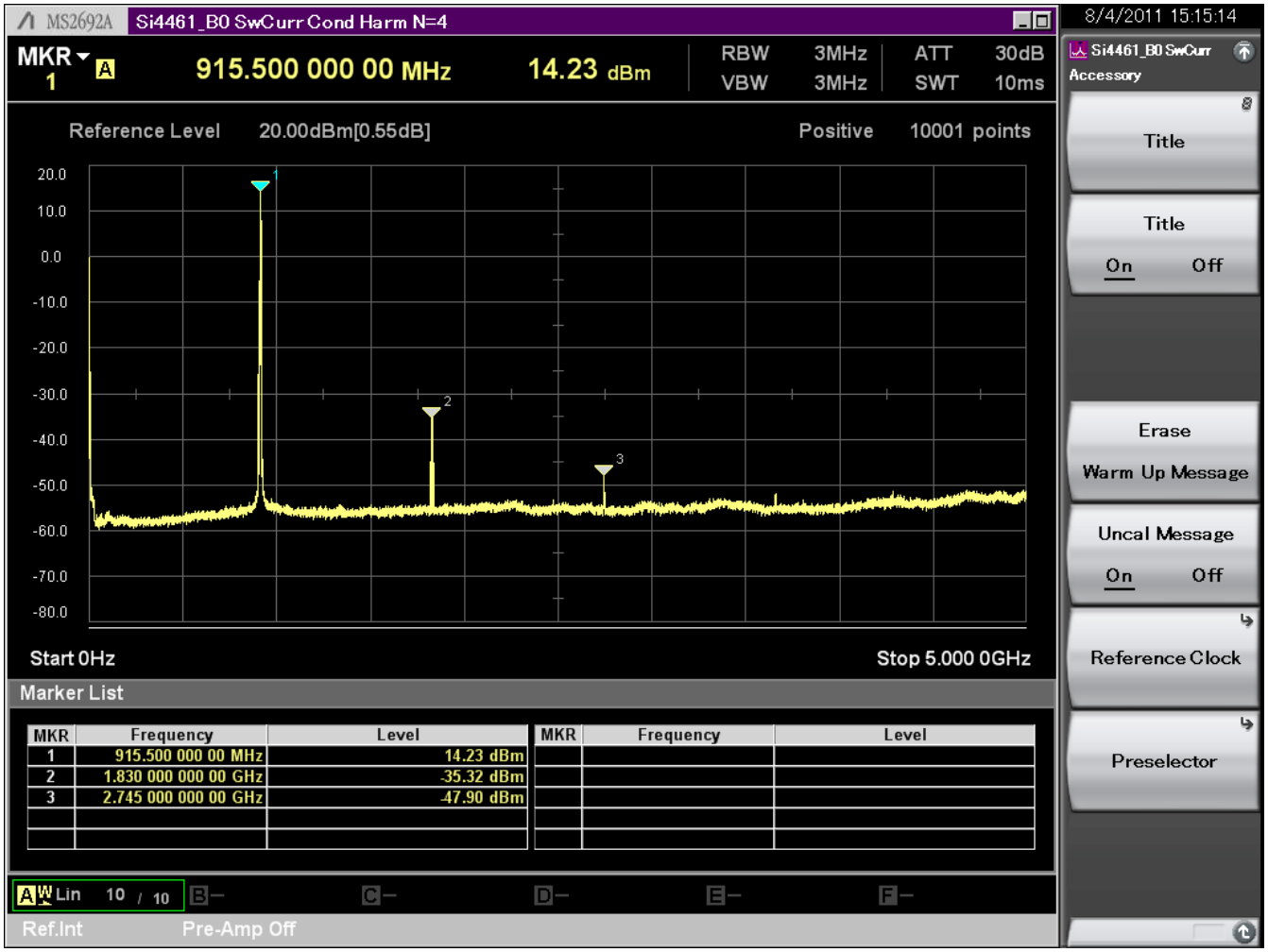

Figure 13. Conducted Harmonics for SwCurr Match at 915 MHz (N = 4)

3.1.8. Final Split TX/RX Schematic

The final schematic for a Split Si4461 TX/RX board Switched Current Match at 915 MHz for +14 dBm output power is shown in Figure 14 below.

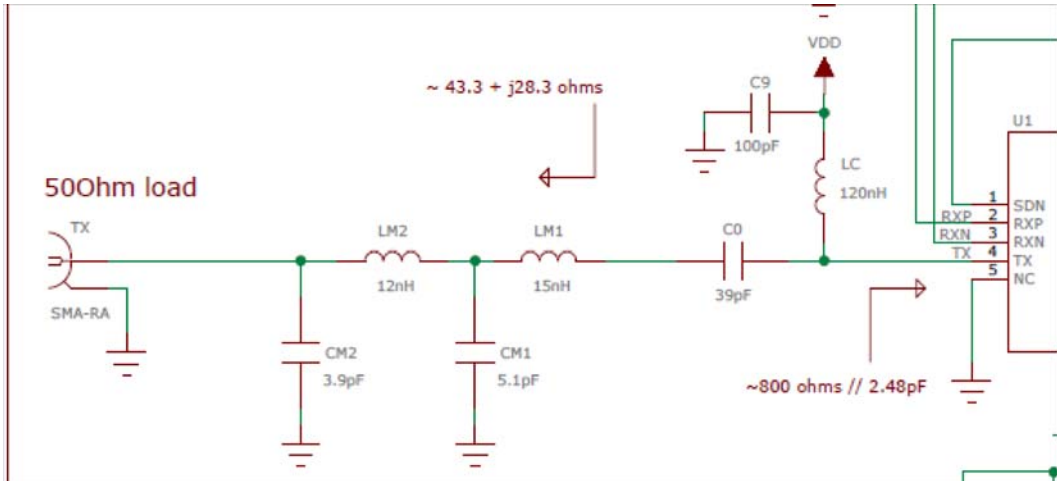

Figure 14. Final Schematic for Split SwCurr Match for +14 dBm at 915 MHz

3.1.9. Improved Efficiency at Lower Output Power Levels

As discussed in "3.1.2. Selection/Calculation of RLOAD_INT" on page 30, the selection of R_{LOAD_INT} is driven largely by the desired target output power level and the available VDD supply voltage. It is necessary to select a value of R_{LOAD_INT} such that drain voltage compression/clipping does not occur for the commanded output power level. If a lower output power level is desired, the value of R_{LOAD_INT} may be increased, thus requiring a lower value of PA bias current but providing improved current efficiency.

The design calculations and resulting component values shown in the previous sections assumed a target output power level of +14 dBm. If the desired output power level is reduced to (e.g.) +13 dBm, a higher value of $R_{LOAD\_INT} \approx 120\ \Omega$ may be selected. In such a case, the design equations will result in the following parameters and component values:

- $R_{TOTAL} = 109.3\ \Omega$
- $P_{LOSS\_INT} = -0.41$ dB
- $I_{PA} = 14.2$ mA (RMS fundamental), 20.0 mA (peak fundamental)
- $I_{BIAS} = 31.4$ mA → OB[5:0] = 0x20
- $Z_{LOAD} = 41.15 + j40.29\ \Omega$
- CM1 = 1.8 pF, LM1 = 11 nH

For the reasons discussed earlier, the initial measured output power for this design was again about 0.6 dB below the target output power of +13.0 dBm. The value of PA bias current was increased to OB[5:0] = 0x22 (340 µA per finger) to compensate for the additional loss, and the performance was remeasured.

2-Element Match						
LM1	**CM1**	**DDAC**	**OB**	**V_{DD}**	**P_{OUT}**	**I_{DD}**
11.0 nH	1.8 pF	0x64	0x22	1.80 VDC	10.46 dBm	25.91 mA
				2.10 VDC	11.08 dBm	27.15 mA
				2.40 VDC	11.46 dBm	28.29 mA
				2.70 VDC	12.03 dBm	29.50 mA
				3.00 VDC	12.51 dBm	29.99 mA
				3.30 VDC	12.85 dBm	30.15 mA
				3.60 VDC	13.05 dBm	30.30 mA

A significant improvement in current efficiency may be observed. For Si4060/4460/67 10 dBm SWC designs, the impedance should be even higher (~240 Ω for high efficiency target or lower if flatness is a concern).

3.2. Overview of Matching Procedure for SWC Direct Tie Board

In this section, the procedure for matching the Si4461 RFIC on an SWC Direct Tie (DT) board is discussed in detail. The procedure for the Si4460/67 chip is the same with different impedance and thus element values. The main steps in the matching procedure are summarized below:

1. Measure the typical PA shunt output capacitance (C_{PA}) and resistance (R_{PA}) of the chip.
2. Choose L_{CHOKE} (pull-up inductor) for high impedance at the desired frequency of operation.
3. Select/calculate internal load resistance R_{LOAD_INT} for the desired output power level.
4. Calculate PA bias current setting.
5. Calculate required external load impedance Z_{LOAD} to present to the TX pin.
6. Construct a simple 2-element L-C matching network to transform the antenna load impedance (typically R_{ANT} = 50 Ω) to the calculated PA load impedance Z_{LOAD}.
7. Add sections of low-pass filtering (while maintaining the desired impedance transformation ratio) necessary to attenuate the harmonic levels below the applicable regulatory standard.
8. Calculate the impedance at the common Direct Tie point in the TX=OFF state (i.e., RX mode).
9. Construct a standard four-element RX balun/matching network, assuming this value of impedance as the source impedance for the match.
10. Tie the TX and RX paths together at the common-impedance point, and verify that the performance of each path has not been significantly degraded.

A comparison of the above procedure with that shown in "3.1. SCW Matching Design for Split TX/RX Boards" on page 26 reveals that the first seven steps are identical. For either type of board configuration (Split TX/RX or Direct Tie), it is necessary to first construct a TX match. In the case of a DT board configuration, the RX match is added after the TX match has been designed.

3.2.1. Concept of Direct Tie Matching

In the Direct Tie board configuration, the TX and RX paths are tied directly together at a common point without the use of an RF switch. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the Si4461 and Si4460/67 chip contains a set of switches that aids in isolation of the TX and RX functions. This set of switches is implemented internally as shown in Figure 15.

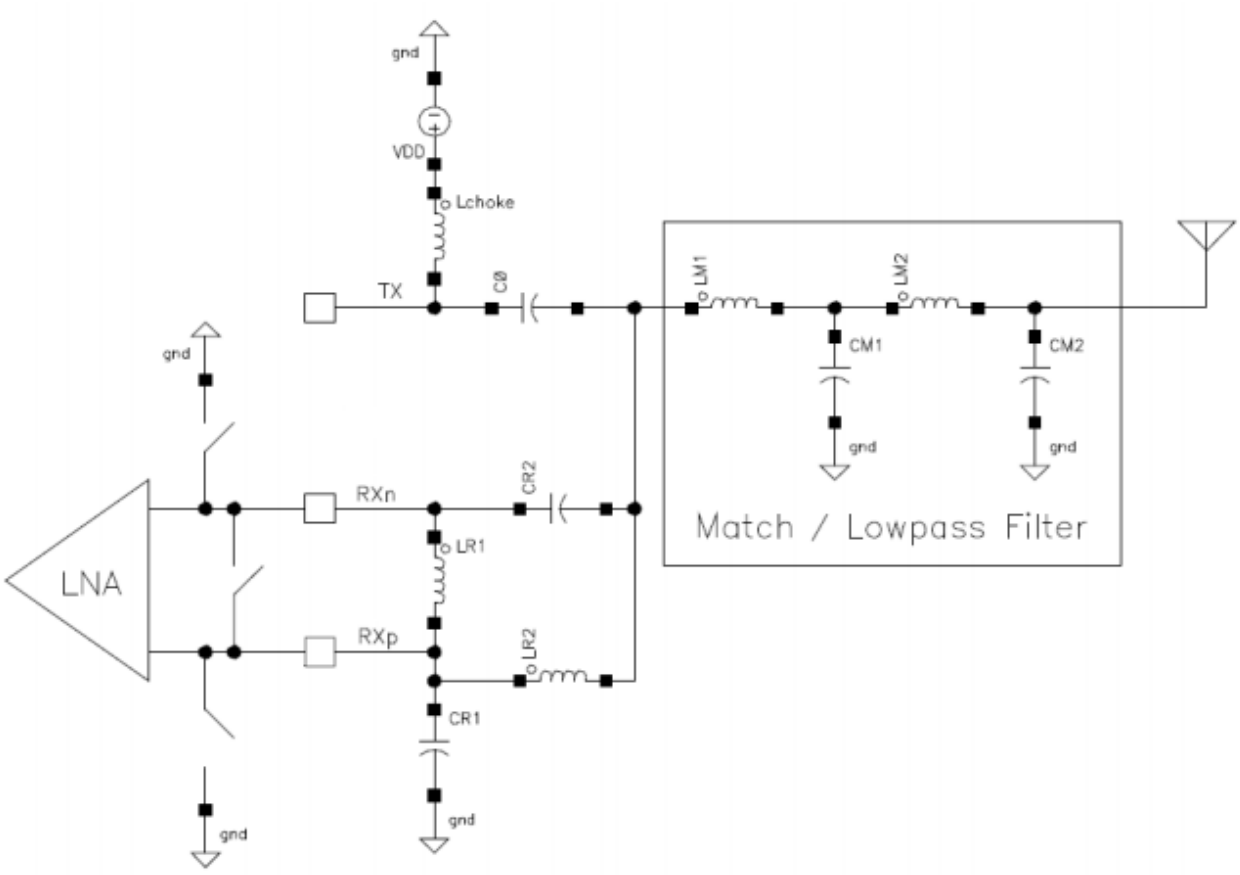

Figure 15. RX Input Switches for Direct Tie Operation

These three switches are activated and closed simultaneously upon entering TX mode; the switches remain open in all other modes, including RX mode. Closing these switches during TX mode effectively shorts the RXp and RXn input pins together and also shorts them to GND. The effective circuit may be redrawn as shown in Figure 16. Inductor LR2 and capacitor CR2 have effectively been placed in parallel by the closure of the switches and are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.

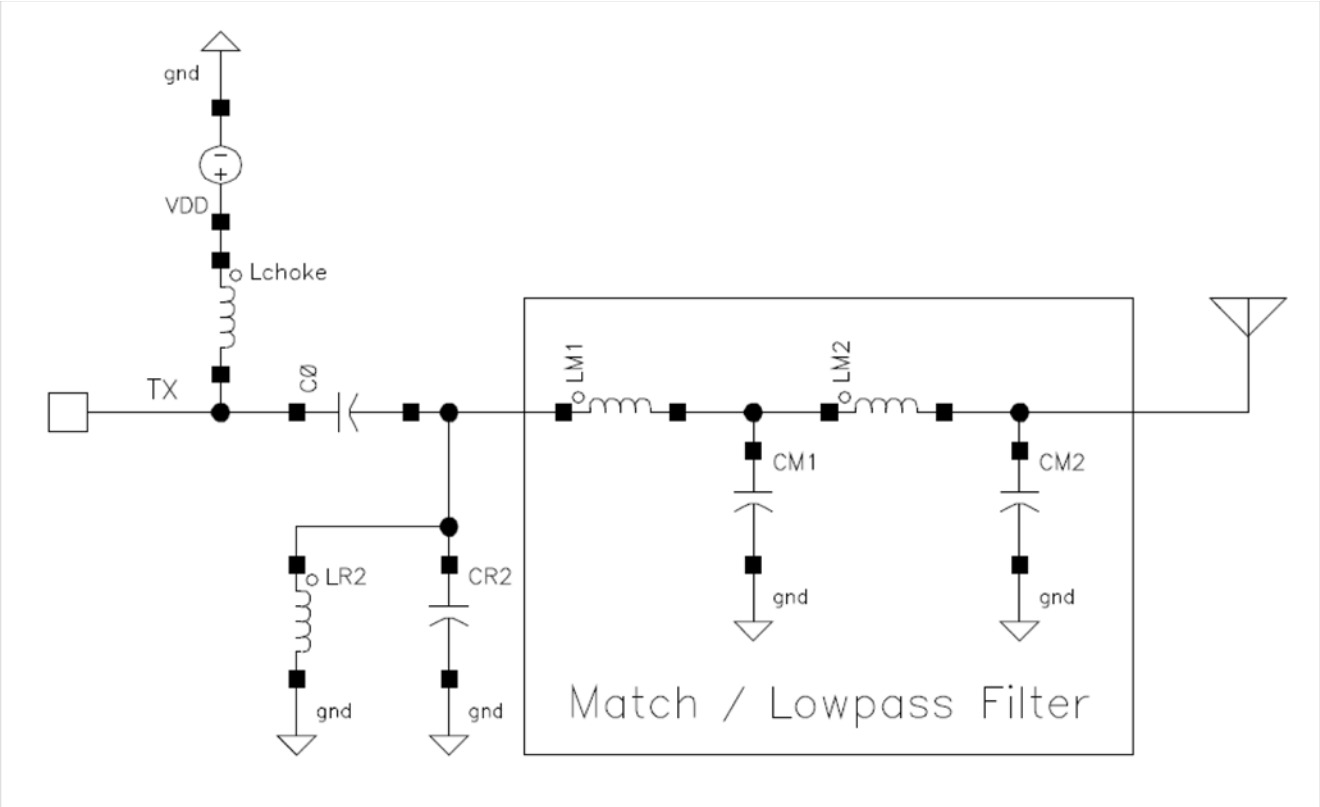

Figure 16. Effective Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state. However, the output impedance parameters of the PA (R_{PA} and C_{PA}) do not vary greatly between TX and RX modes. (The shunt output capacitance does decrease slightly in RX mode as compared to TX mode, but the decrease is only about 10%.) As a result, the output impedance parameters determined in "3.1.1. Measurement of PA Shunt Output Capacitance/Resistance (CPA/RPA)" on page 26 may be reasonably used in both TX and RX modes. The impedance of the pull-up inductor, L_{CHOKE}, is quite high and the impedance of the coupling cap, C0, is quite low, and both may be ignored for this discussion.

A key step in the DT matching procedure is to design/measure the impedance at the common direct tie point and to then construct the four-element RX match, assuming that impedance value as the source impedance. This common-point impedance is typically not exactly 50 Ω; however, there is nothing that prevents construction of an RX matching network for an arbitrary value of source impedance.

As discussed in "3.1.5. Transforming RANT into ZLOAD" on page 33, the impedance seen looking back into the match/low-pass filter network (i.e., looking back into LM1 with the chip disconnected) is equal to Z_{LOAD}. Additionally, connecting the TX pin of the chip results in placing the L_{SER}-R_{PA}-C_{PA} network in shunt to GND at this point, as shown in Figure 17. This modifies the source impedance presented to the input of the RX matching network away from the Z_{LOAD} value. While it is possible to express the resulting impedance mathematically in terms of Z_{LOAD} and the PA output impedance parameters, the resulting equation is rather unwieldy; it is much simpler to graphically determine the impedance on a Smith Chart.

The resulting impedance is reasonably close to being purely real and is close to (but slightly lower than) R_{LOAD_INT}. This is not unexpected; if the series bond wire/trace inductance (L_{SERIES}) was equal to zero, the resulting impedance would be *exactly* equal to R_{LOAD_INT}. A non-zero value of L_{SERIES} has an impedance-transforming effect that tends to lower the impedance observed at this point.

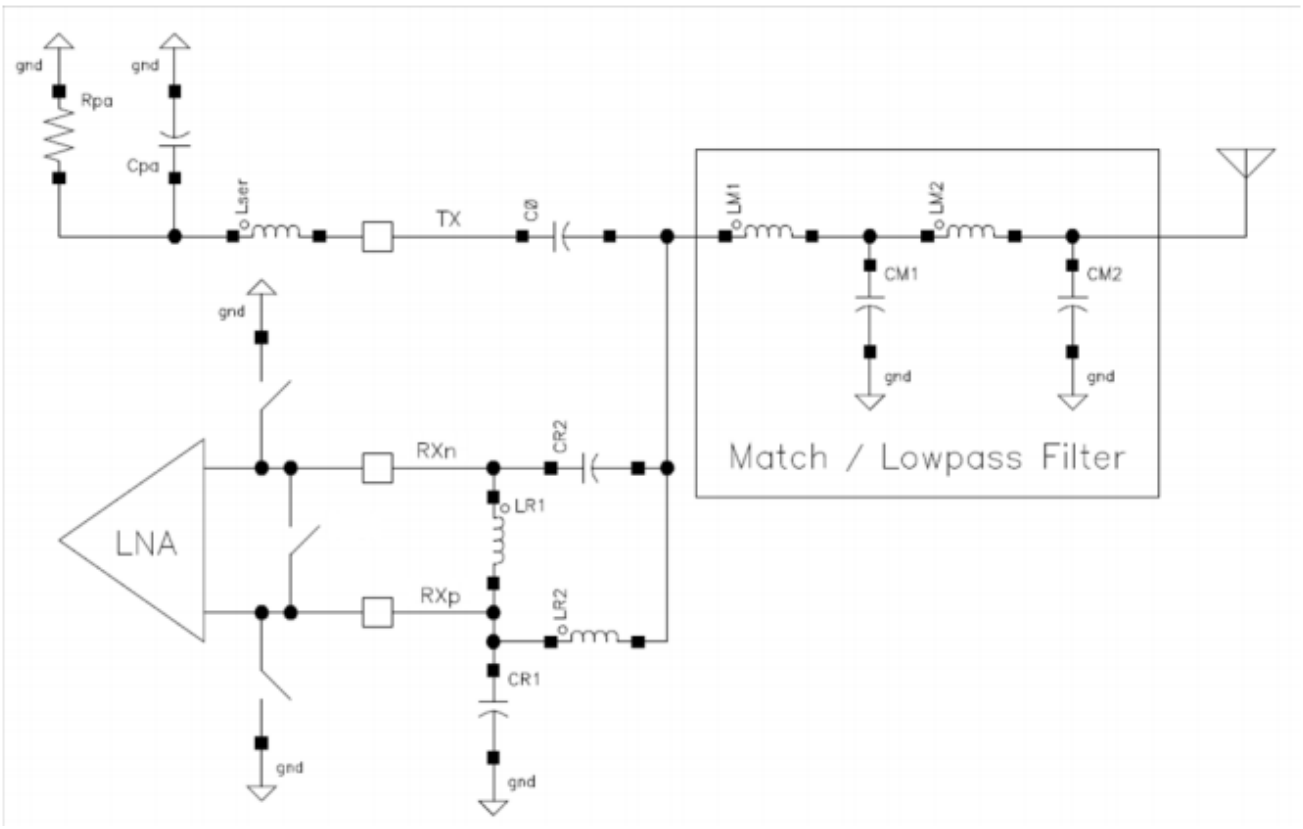

Figure 17. Effective Direct Tie Circuit in RX Mode

This (nearly) purely-real common impedance value now allows for a convenient tie-point that simultaneously satisfies the matching requirements for both signal paths. In TX mode, the RX matching network presents a high impedance and thus does not load down the TX signal. In RX mode, the R_{PA}-C_{PA}-L_{SERIES} network placed in parallel with Z_{LOAD} results in an approximately-real impedance that may be used as the source impedance for construction of the RX match. In this fashion, the performance of both signal paths may be maintained near their optimum levels (i.e., performance levels similar to those obtainable with a Split TX/RX board configuration).

3.2.2. Construction of TX Match

The construction of the TX match (see Steps 1 through 7) is performed exactly the same as in "3. Switched Current (SWC) Matching Procedure Overview" on page 26 and is not discussed again here.

3.2.3. Calculate the Common Tie-Point Impedance

The circuit of Figure 18 may be analyzed to determine the source impedance presented to the input of the RX match in RX mode. This may done using graphical methods (e.g., Smith Chart) or with a basic circuit analysis program, such as SPICE. Continuing the Si4461 design example of 915 MHz, the impedance at this point is found to be ZSRC = 55 – j13 Ω. This impedance is sufficiently close to purely real to consider the common tie-point impedance to simply be RSRC = 55 Ω.

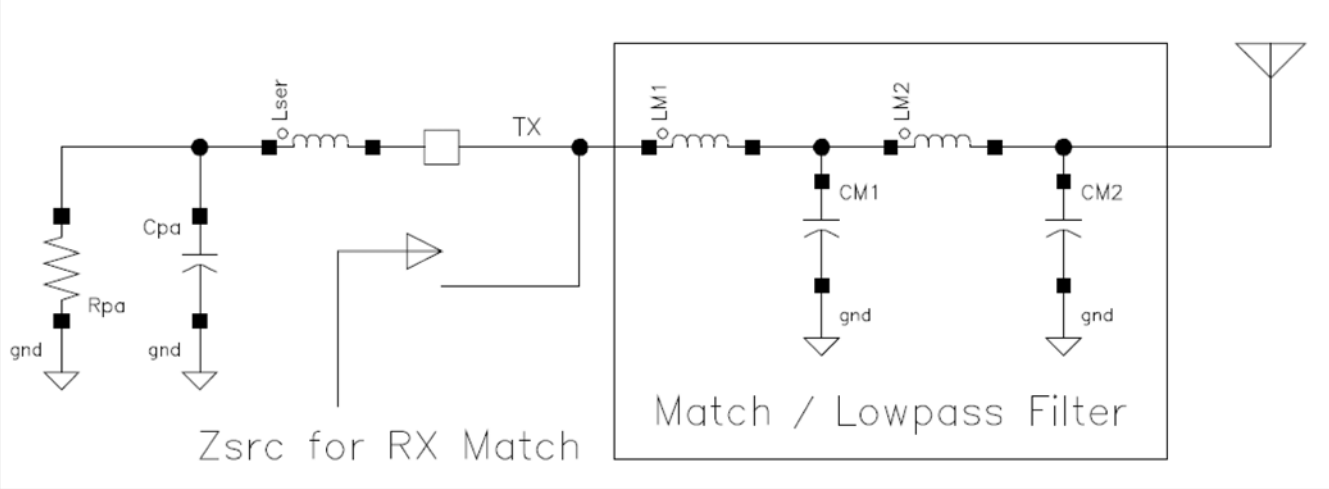

Figure 18. Equivalent Circuit of Source Impedance for RX Match

3.2.4. Construction of RX Match

It is next necessary to construct a four-element RX matching network to simultaneously provide an impedance match as well as a single-ended-to-differential conversion function (i.e., balun). The mathematical derivation for the required component values has been thoroughly described in “AN643: Si446x/Si4362 RX LNA Matching”; the relevant equations from that document are shown here.

$$L_{LNA} = \frac{1}{\omega_{RF}^2 C_{LNA}}$$

Equation 14. .

$$L_{R2} = \frac{\sqrt{Re(Z_{ANT})R_{LNA}}}{\omega_{RF}}$$

Equation 15. .

$$L_M = \frac{2L_{R2}}{\left(\frac{2 \times Im(Z_{ANT})}{\omega_{RF} L_{R2}}\right) + 1}$$

Equation 16. .

$$L_{R1} = \frac{L_{LNA} L_M}{L_{LNA} + L_M}$$

Equation 17. .

$$C_{R1} = \frac{1}{\omega_{RF} L_{R2}}$$

Equation 18. .

$$C_{R2} = 2C_{R1}$$

Equation 19. .

In order to make use of the above equations, it is first necessary to know the LNA differential input impedance at the desired frequency of interest. This has been measured by Silicon Labs and is shown in Figure 19. The value of the RX input impedance is the same for both the Si4461 and Si4460/67. At 915 MHz, the input impedance is Z_{RX_LNA} = 48.8 – j109.4 Ω; the equivalent parallel input resistance and capacitance may be calculated to be R_{LNA} = 296 Ω and C_{LNA} = 1.33 pF.

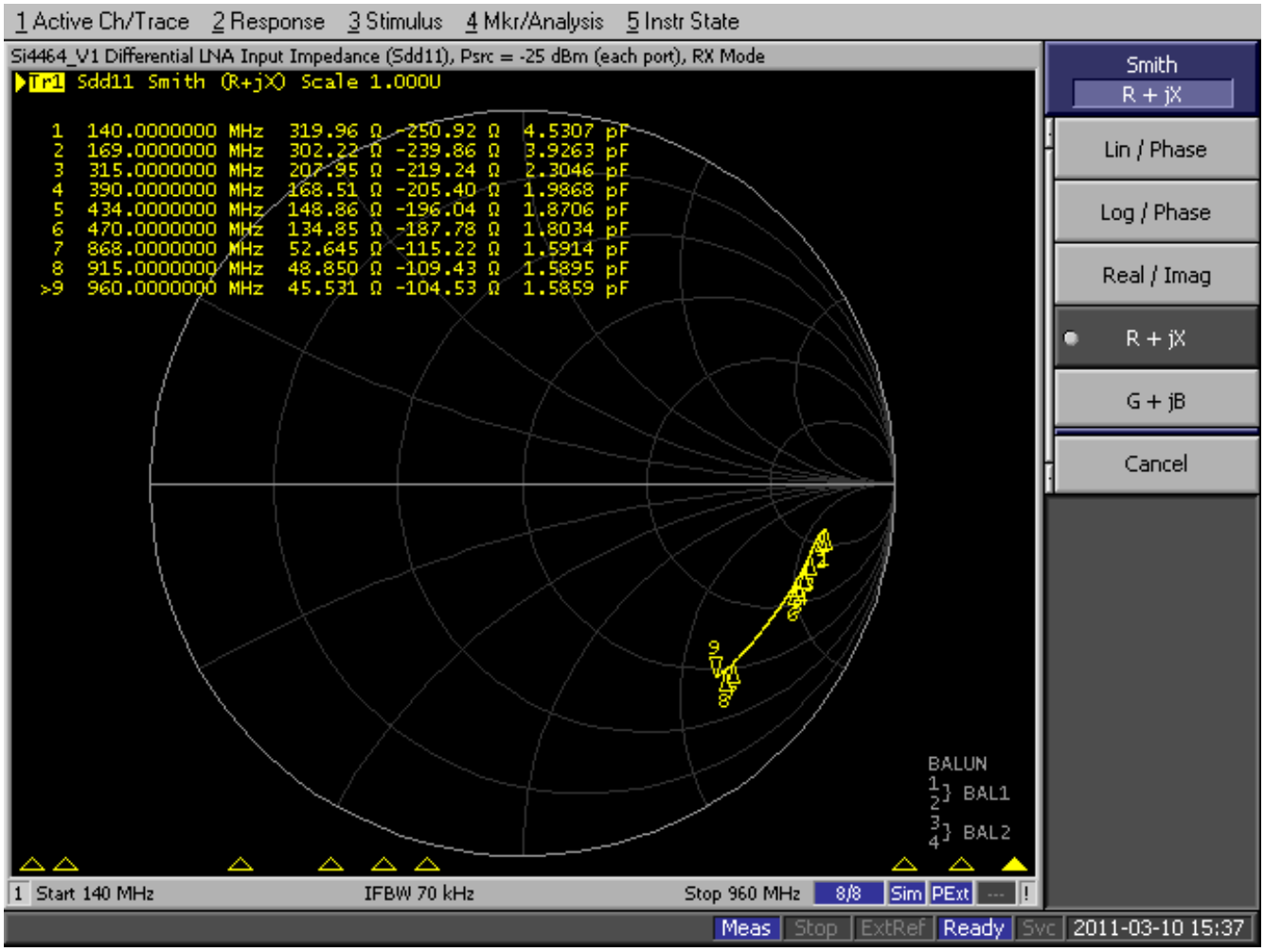

Figure 19. Si4461/Si4460/67 RX Differential LNA Input Impedance

The source impedance to which the RX input must be matched is the common tie-point impedance of Z_{SRC} = 55 Ω (in the 915 MHz Si4461 design example). Plugging the values of Z_{ANT}, R_{LNA}, and C_{LNA} into the above equations, the following calculated RX match component values are obtained:

- L_{R1} = 15.04 nH
- L_{R2} = 22.19 nH
- C_{R1} = 1.36 pF
- C_{R2} = 2.72 pF

These exact values may be rounded to the nearest-available 5% component tolerance values to arrive at L_{R1} = 15 nH, L_{R2} = 22 nH, C_{R1} = 1.3 pF, and C_{R2} = 2.7 pF. If desired, as an additional step of confirmation, this match may be constructed in a “stand-alone” configuration (i.e., not connected to the TX path) and its impedance measured. It was found that the input impedance and resonance were slightly off-target, likely due to parasitic trace and pad effects. The component values were adjusted slightly to optimize the impedance at the desired frequency.

- L_{R1} = 18 nH
- L_{R2} = 22 nH
- C_{R1} = 1.0 pF
- C_{R2} = 3.0 pF

The measured input impedance in RX mode for these component values is shown in Figure 20. The input impedance at the desired frequency of 915 MHz is 44 Ω; this is sufficiently close to the design target of 55 Ω.

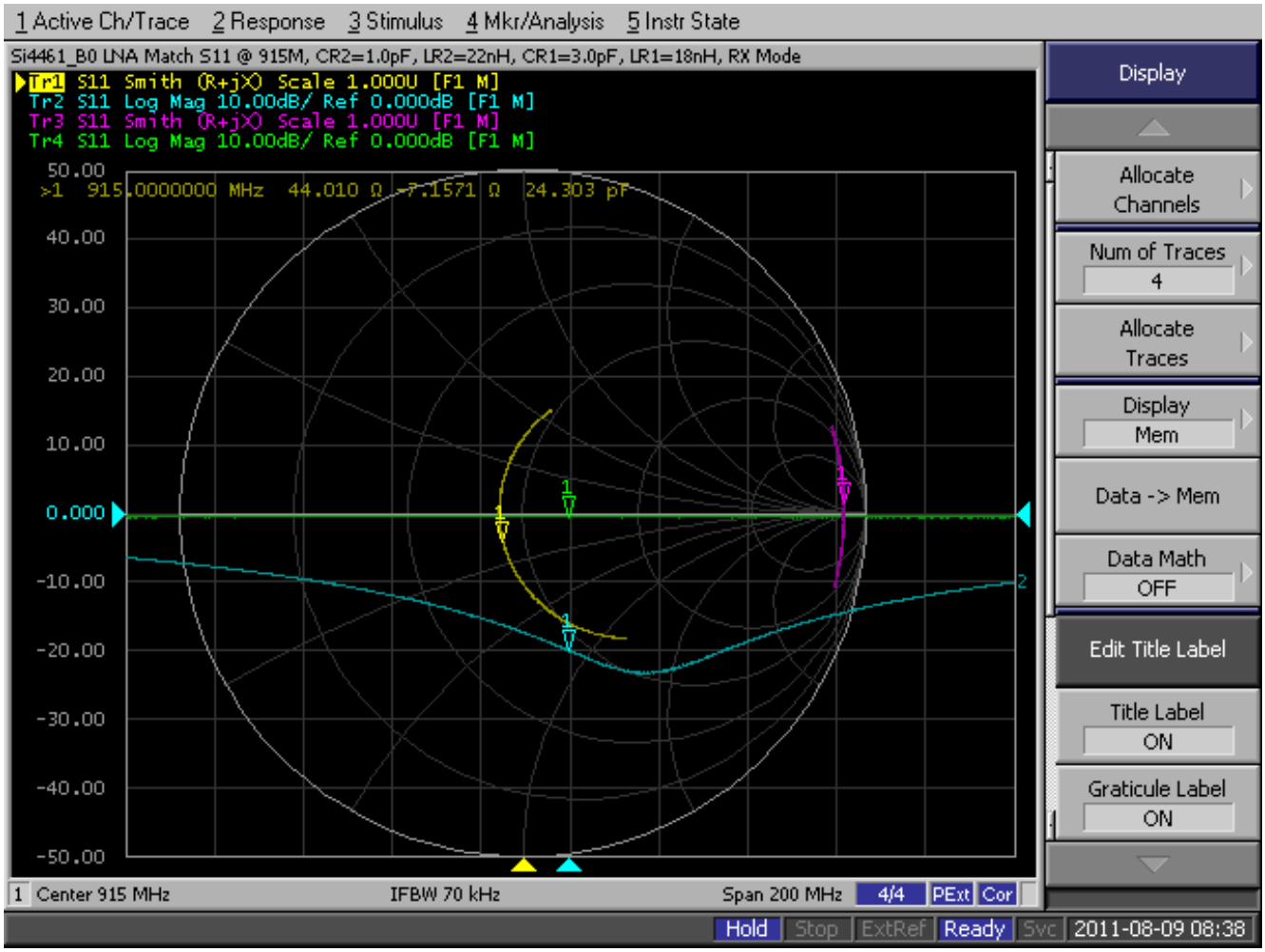

Figure 20. Si4461 SWC RX Match Input Impedance (RX and TX Modes)

It is also useful to verify the input impedance of this network in TX mode, when the LNA input pins are shorted together and also to GND. The input impedance of the match in TX mode is also shown in Figure 20 (magenta trace). It is seen that the circuit is nicely tuned to parallel-resonate at 915 MHz, thus presenting a very high impedance (~1.4 kΩ). This should allow the RX path to be connected to the TX path with very little degradation in TX mode.

3.2.5. Direct Tie Connection of TX and RX Paths

The next step is to actually connect the TX and RX paths at the common tie point (just after the series dc blocking capacitor). The TX and RX performance in the Direct Tie configuration is then remeasured.

The TX performance in Direct Tie configuration was measured as shown below.

2-Element TX Match						
LM1	**CM1**	**DDAC**	**OB**	**V_{DD}**	**P_{OUT}**	**I_{DD}**
8.2 nH	1.5 pF	0x64	0x2E	1.80 VDC	11.24 dBm	29.74 mA
				2.10 VDC	12.15 dBm	31.89 mA
				2.40 VDC	12.65 dBm	33.48 mA
				2.70 VDC	12.83 dBm	34.38 mA
				3.00 VDC	13.57 dBm	35.31 mA
				3.30 VDC	13.83 dBm	35.52 mA
				3.60 VDC	13.97 dBm	35.69 mA

Comparing with the previously-measured performance in Split configuration, the loss of output power is only ~0.2 dB! This is considered quite acceptable DT performance.

The RX sensitivity is also measured. The typical RX sensitivity performance in a Split configuration is known (from measurements on a large number of other boards) for 2GFSK DR = 40 kbps Dev = 20 kHz (h = 1) condition to be approximately –109.6 dBm for BER = 1E-3 (0.1%). The measured performance on this board in Direct Tie configuration is found to degrade by less than 1 dB. Again, this is considered quite acceptable performance.

4-Element RX Match				RX Sens (DR=40K Dev=20K)		
LR1	**CR1**	**LR2**	**CR2**			
18.0 nH	3.0 pF	22.0 nH	1.0 pF	Split =	-109.6 dBm	
				DT =	-108.8 dBm	

3.2.6. Final Direct Tie Schematic

It is again necessary to add further stages of lowpass filtering in order to comply with the harmonic radiated spurious emission requirements of various regulatory standards, such as FCC or ETSI. The resulting final schematic for a Direct Tie board Si4461 Switched Current Match at 915 MHz for +14 dBm output power is shown in Figure 21.

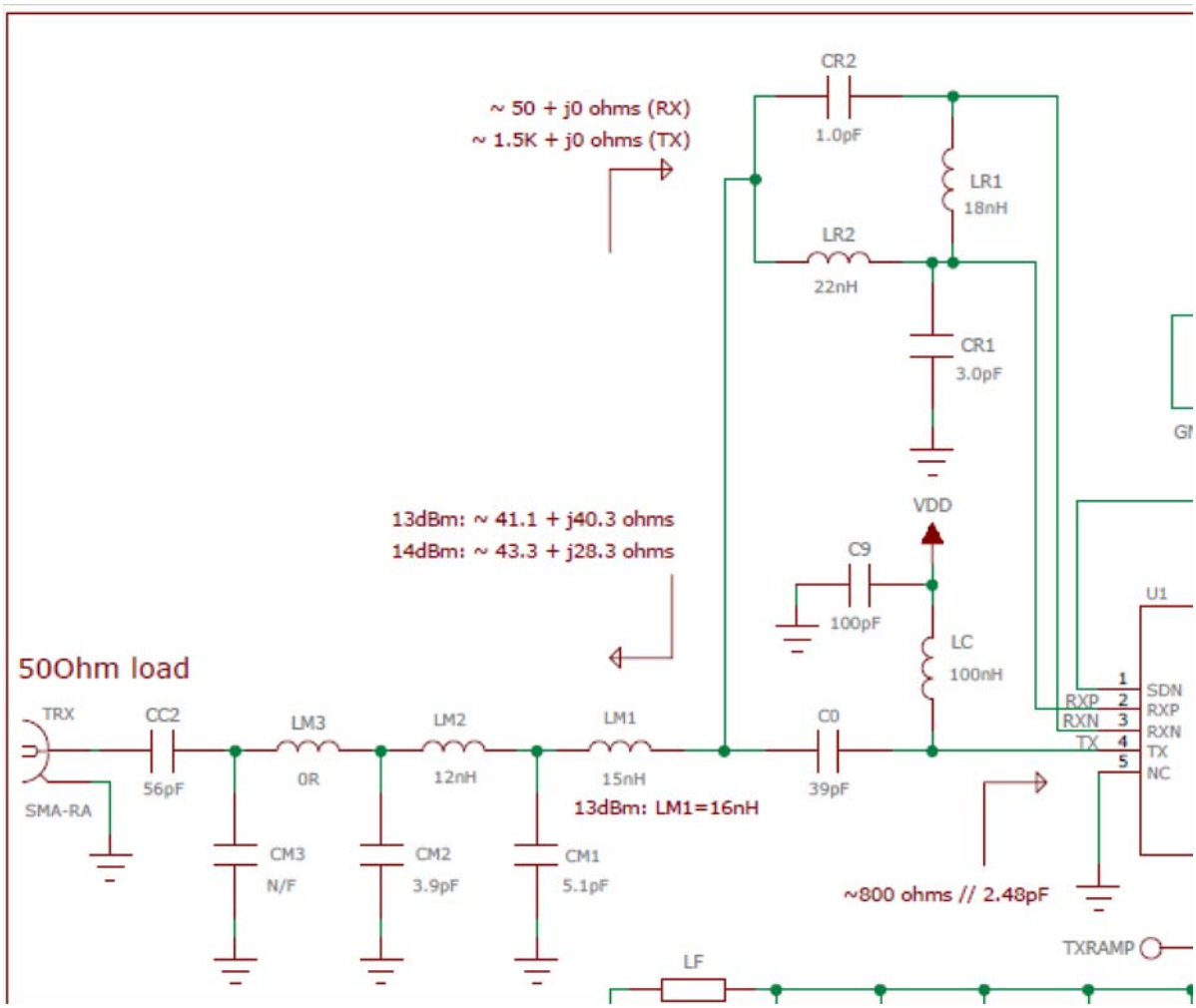

Figure 21. Final Schematic for Direct Tie Si4461 SwCurr Match for +14 dBm at 915 MHz

4. Class E (CLE) Matching Procedure Overview

Published matching procedures for well-defined classes of operation of switching amplifiers (such as Class-D or Class-E) may lead to operating conditions that exceed the maximum ratings (voltage or current) for the semiconductor process. As a result, we turn to a “customized” matching methodology that satisfies our desire for output power and efficiency while maintaining operation below the maximum voltage and current ratings for the RFIC. Note that this matching methodology is based upon Class-E theory but adds additional steps to aid in constraining the peak drain voltage. The drain voltage peak limit for long term reliable PA operation is 8 V in the case of the EZRadioPRO® family.

4.1. Brief Overview of CLE Matching Procedure

This application note discusses the CLE matching philosophy and procedure for the Si4060/Si4460/61/67 RFIC in great detail. However, some users may be interested in quickly gaining a high-level overview of the procedure before getting into the fine details. For those readers, the main points of the matching procedure are summarized below:

- Choose L_{CHOKE} (pull-up inductor) for high impedance at the operating frequency, Fo.
- Calculate the required value of Z_{LOAD} at the given Fo.
- Calculate the required PA switcher loss for a given V_{DD} and desired output power. In the matchings applied here, instead of an external R_{DC}, the necessary loss is introduced by tuning the PA switcher FET loss (i.e with the PA power level setting).
- Choose a value for C_0 (series capacitor).
- Calculate L_0 (series inductor) and the required matching component values L_X and C_X.
- Design a Chebyshev LPF (for attenuation of harmonics).

4.2. Power Amplifier Circuit Description

RF design engineers are familiar with matching conventional (Class A/B/C) power amplifiers. In such cases, the matching procedure is relatively simple: provide a load impedance that is the complex conjugate of the output impedance of the PA. The reader may also employ Load Pull techniques in which a match is found that optimizes the output power but differs from the complex conjugate of the PA output impedance. In these conventional classes of power amplifiers, the output waveform ranges from a full 360 degree copy or reproduction of the driving waveform (e.g., Class A) to a partial (less than 360 degree) reproduction of the driving waveform (e.g., Class B or Class C).

However, the Class E type PA circuitry in the Pro family RFIC differs considerably from such a conventional power amplifier. Specifically, the PA circuitry in the Pro family is capable of working as a “switching power amplifier” or “switching power converter”. The matching procedure for such a class of PA is entirely different and may not be immediately intuitive.

4.3. Basic Switching PA Circuit Topology

At the very heart of a switching PA is a switch. In the Si4060/Si4460/61/67, the switch is provided by group of NMOS transistors. Above the switcher FETs, a cascode stage with open collector output is used to increase the Vpeak allowed at the output. The number of bottom transistors can be tuned and sized to handle the current required for the specified output power.

- The higher-power Si4461 PA has 127 MOS switching fingers; so, the DDAC[6:0] field in the PA_PWR_LVL property register can go up to 7Fh. Its typical output capacitance is 1.9–2.2 pF, independent of the DDAC setting due to its cascode architecture.
- The lower-power Si4060/Si4460/67 PA has 79 MOS switching fingers; so, the DDAC[6:0] field in the PA_PWR_LVL property register can go up to 4Fh. Its typical output capacitance is 1.2–1.25 pF, independent of the DDAC setting due to its cascode architecture.

Figure 22 shows the basic class E matching circuitry necessary to extract RF power from a switching amplifier. In very general terms, the value of the pull-up inductor “L_{CHOKE}” is chosen to be a very large impedance at the frequency of operation (and its nearest harmonics), while the series-resonant output tank (L_0-C_0) is chosen to resonate at the frequency of operation. The shunt capacitance, C_{SHUNT}, is required to store energy during the switching cycle. This shunt capacitance, along with the extra series inductance, L_X, also works to tailor the time-domain shape of the output waveform. It is important to understand that, in order to optimize the efficiency of a switching-type amplifier, it is necessary to control the time-domain shape of the output waveform.

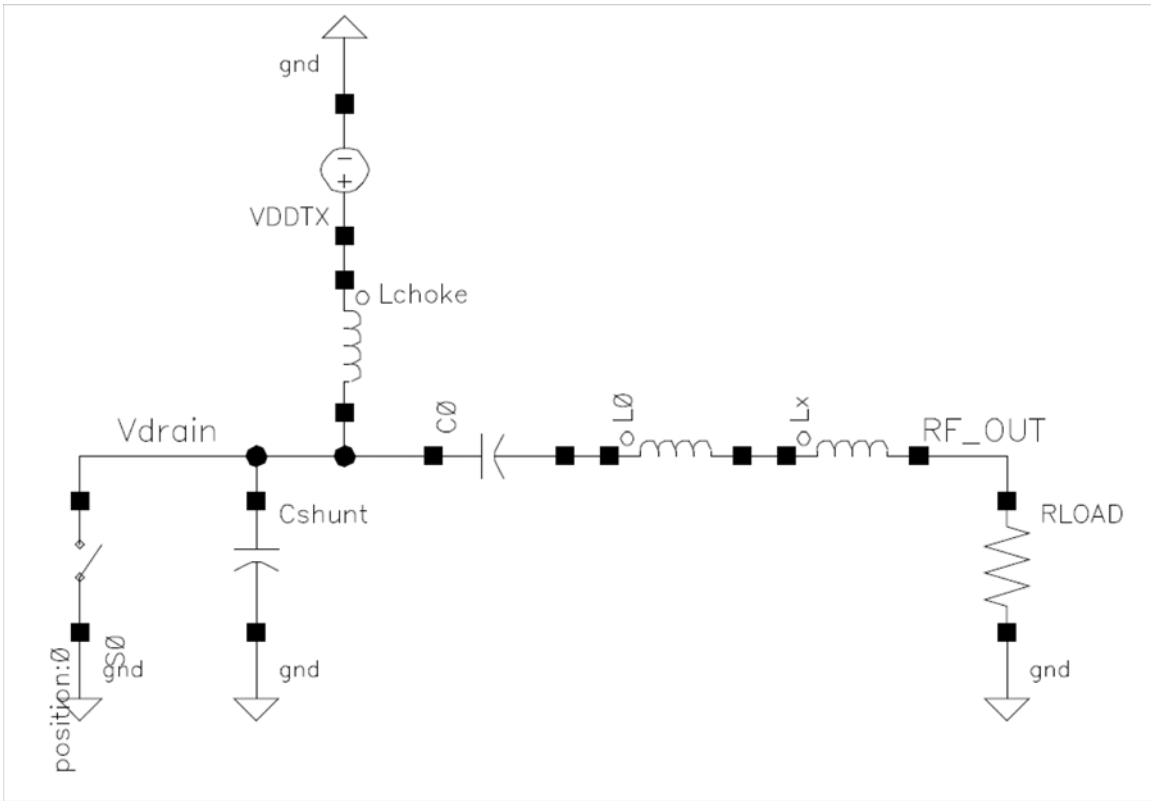

Figure 22. Basic Switching PA Circuit Topology

4.4. Theory of Operation of an Ideal Switching PA

How does a switch “amplify” an RF signal? The simple answer is that it does not. As long as the input control signal to the switch is sufficient to toggle the switch between its ON and OFF states, the output waveform remains the same. Thus, the amount of output power delivered to the load resistance is independent of the amplitude of the input control signal (i.e., amplitude of the RF signal at the gate of the output MOS device); that is, a switching PA is a strongly nonlinear device. In such a case, defining the “gain” or amplification factor of the PA no longer has much meaning. Technically speaking, it is more correct to refer to this circuit as a “power converter” rather than a “power amplifier”.

If the circuit does not amplify the internal RF input signal, what determines the level of the output power?

In an ideal class E switching PA, the level of output power is primarily dependent upon two parameters: the dc supply voltage and the shunt capacitance. This statement is interesting because, theoretically, there is no limit to the amount of power we can extract from a switching PA. Higher levels of output power can be obtained by either increasing the supply voltage or by increasing the shunt capacitance at the switching output device.

Furthermore, in an ideal switching PA, it is theoretically possible to achieve 100% efficiency. This is significantly different than conventional PAs. It is easily shown that the theoretical maximum efficiency of a Class-A PA is 50%, 78.5% for Class-B, and so on. However, in a switching PA, it is possible to tailor the output waveform such that the voltage across the switch is always zero during any period of time that the switch is conducting current, and the current conducted by the switch is always zero during any period of time that the voltage across the switch is non-zero. Thus, the power dissipated by the switching device itself is zero, and, in the absence of any other losses in the circuit, the efficiency approaches 100%. The theoretical voltage waveform at the drain of a switching amplifier operated in Class-E is shown in Figure 23.

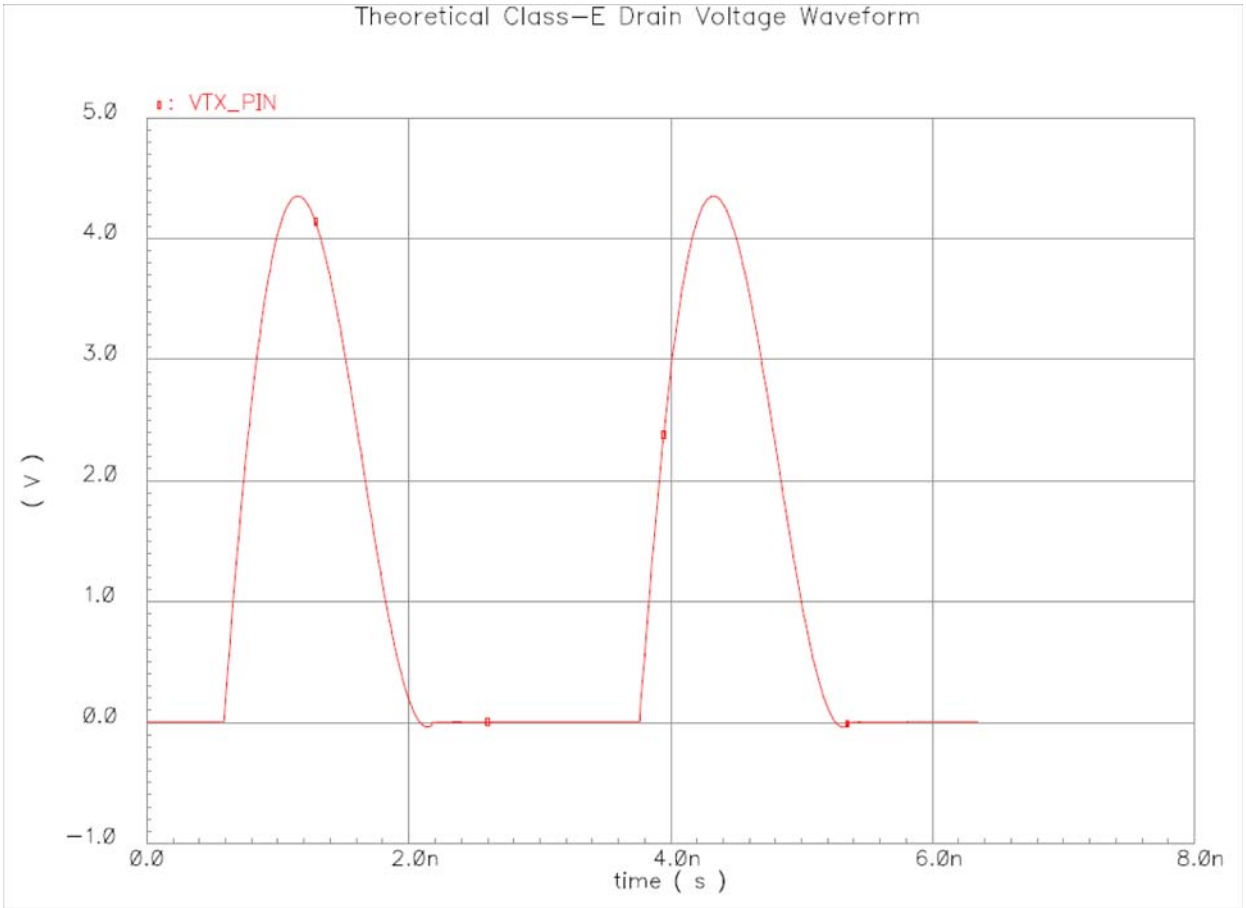

Figure 23. Theoretical Class-E Drain Voltage Waveform

For those interested in learning more about the theoretical operation of switching amplifiers (especially Class-E amplifiers), the following papers are recommended:

- *Class E – A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers*, N. Sokal and A. Sokal, IEEE Journal of Solid State Circuits, Vol. SC-10, No. 3, June 1975.
- *Idealized Operation of the Class-E Tuned Power Amplifier*, F. Raab, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, December 1977.

4.5. Limitations of a Practical MOS Switching PA

In practice, several factors prevent the “ideal” operation of a switching PA. These factors include the maximum operating voltage of the switch (i.e., MOS output device), the maximum current (limited by the size of the MOS output device), ON and OFF state resistances of the MOS output device, non-zero switching times of the MOS output device, and losses in the output matching components due to finite Qs. All of these factors combine to limit the achievable output power and efficiency.

The limitation on the maximum drain voltage of the MOS output device turns out to be a considerable constraint. RF design engineers may be quite familiar with the waveforms obtained with inductively-loaded conventional PAs, where the peak output voltage reaches a value equal to twice the dc supply voltage. However, the peak of the output voltage waveform in a switching PA may far exceed this “$2xV_{DD}$” rule-of-thumb. As is shown in the papers listed above, the peak drain voltage for a Class-E switching amplifier can reach 3.56 x V_{DD}.

The operational range of supply voltage for the Si4460/61/67 RFICs are specified as V_{DD} = 1.8 V to 3.6 V. It is apparent that, if the switching PA circuit was matched for Class-E operation at V_{DD} = 3.6 V, the resulting peak drain voltage would reach 12.8 V peak. This exceeds the maximum voltage at which the MOS devices (even in cascade configuration) can operate reliably without damage. As a result, at a higher VDD regime, the drain voltage must be constrained when matching the Si4060/Si4460/61/67 for Class-E operation. This is accomplished by introducing loss. It can be either a suitable choice of a limiting resistor R_{DC} in series with Lchoke, as shown in Figure 3, or it can be a properly tuned switcher loss. The matching procedure discussed in this application note takes care to constrain the peak drain voltage to a specified maximum value by proper tuning of the switcher loss.

Unfortunately, the introduction of any kind of loss causes a reduction in efficiency. One way to avoid this is to apply a dc-dc converter instead, which reduces the dc supply voltage properly at the Lchoke inductor. However, this method is usually too expensive for low-cost, short-range radio applications. Moreover, the switching noise generated by the dc-dc converter can cause several close-in mixing products in the TX spectrum. For these reasons, the introduction of loss remains the only low-cost way to limit the peak voltage at the PA's switching device drain.

The switching loss here can be modeled as a series resistance, which causes a dc voltage drop on the switcher; that is, with this loss, the PA supply voltage on the switcher output is decreasing. If the class E waveform is maintained, the allowed maximum of this PA supply voltage is Vpeakmax / 3.56 V = 8 V/3.56 V = 2.24 V since, for the cascode configuration to have reliable long-term operation, the maximum voltage rating of the semiconductor process is 8 V.

As mentioned earlier, in Class E operation, the output power at a given operating frequency is determined by the PA supply voltage and by the shunt capacitance at the drain of the switching output device. In the case of a real amplifier, where the PA supply voltage is decreased by the loss to limit the peak voltage, the shunt capacitance has to be increased to keep the targeted power. The increased capacitance results in a higher current peak and, thus, a higher dc current as well (since the peak current/dc current ratio is fixed ~2.56 in class E operation). That is, a real class E PA with tuned loss sacrifices efficiency to keep the 8 V peak voltage restriction at higher supply voltage levels.

Moreover, this is an optimized situation where the PA shunt capacitor value is adjusted to be close to the 8 V maximum peak limit at the operating frequency with the targeted power.

In real life, the PA capacitance is usually fixed. Especially at higher frequencies and lower power applications, it may happen that the capacitance value is larger than the optimum for 8 V peak voltage. In this case, the peak voltage (and thus the effective supply voltage on the switcher) is lower than the 8 V optimum; that is, a higher voltage drop, higher switcher loss, and higher power level back off must be introduced. Besides, due to the higher-value capacitor, the current peak (and thus the dc current) is also higher, which degrades the efficiency even more

significantly. This is why a device with a higher PA capacitance value is not efficient in high-frequency, low-power applications (e.g. the Si4461 is not efficient at 868 MHz with +10 dBm power).

On the other hand, a device with an excessively low shunt capacitance value cannot achieve the targeted power with the 8 V voltage peak limit. To achieve the target power, a voltage peak higher than 8 V is necessary. Since it cannot be allowed again, switcher loss must be introduced. This is the reason why the lower capacitance device (e.g Si4060/Si4460/67) cannot achieve the +13 dBm level at low (169/315/434 MHz) frequencies even with wire-wound inductors (although, at 434 MHz, it is very close to that).

The calculation in "5.3.4. Step #4: Estimate the Required PA_PWR_LVL Register Value from the Calculated Value of a Voltage-Limiting Resistor" on page 60 helps to describe the situation even better.

The output capacitances and number of fingers of the Si4460/61/67 devices are sized in such a way that they can achieve the targeted normal operating power (i.e. 10 dBm in case of Si4060/Si4460/67 and 14 dBm in case of Si4461) at a wide frequency range with a strongly reduced power state at the typical 3.3 V external supply voltage level. Although, in this way, the RFICs sacrifices efficiency, it is still one of the best on the market at the time of this writing.

On the other hand, the reduced power state has many advantages, an important one being the improved robustness of the PA:

- The PA is less sensitive to load impedance variations. This is especially advantageous in battery-powered applications where any excess current increase of the RFIC (even a short one) caused by antenna impedance changes due to environmental condition variations significantly reduces the battery lifetime.
- There is room for power compensation with decreasing external supply voltage level (e.g. battery discharge) by simply increasing the number of switching fingers of the output device (i.e. by decreasing the switcher loss). Since the device has a built-in supply voltage detector, in theory, with a proper external MCU code, it can be adjusted automatically. Silicon Labs calls it “adaptive power control”. Unfortunately, it is usually efficient only in the supply voltage range of 2.2 to 3.6 V.

The PA capacitance of the Si4060/Si4460/67 is 1.2–1.25 pF. With that, the IC can achieve 14 dBm at a maximum power state of 3.3 V V_{DD} at 868 MHz.

At lower frequencies (434/315 MHz), the capacitance value is too low, and, thus, the typical power the Si4060/Si4460/67 can deliver is only 12 to 13 dBm at 3.3 V V_{DD}.

The PA capacitance of the Si4461 is 1.9–2.2 pF. With that value, the maximum achievable power at 868 MHz is ~+18 dBm, while it is ~+17 dBm at ~434 MHz; so, here, there is a slight margin to use some back-off at the targeted 16 dBm power.

It must be emphasized that the given power values can be measured after the harmonic filter at the output SMA connector. The power at the class E tank output (before the filter) is approx 0.5 to 0.8 dB higher than that indicated with wire-wound inductors. With multilayer inductors, the power on the SMA is ~0.5 dB lower due to the higher losses (especially filter losses).

A good solution to have flat power and efficiency characteristics over a wide frequency range would be to use a tunable internal PA capacitance feature. However, since the achieved power and efficiency still meet the target (both at low and high frequencies), the simpler fixed PA capacitance method is used in the Si4060/Si4460/61/67.

5. CLE Matching Procedure for the Si4060/Si4460/61/67

This section provides a description of the Class E type switching mode matching process of the power amplifier (PA) on the Si4060/Si4460/61/67 family of RFICs. Specifically, this document does not address the matching procedure for the PA on the Si4063/Si4463/64/68 RFIC. Since the output power level on the Si4063/Si4463/64 RFIC is considerably higher than the Si4060/Si4460/61/67 RFIC, the matching procedure is somewhat different.

Also, due to the different power targets, the CLE matching network elements are quite different for the Si4060/Si4460/67 and Si4461. PA properties (basically the PA capacitance and the on-state FET loss), which primarily influence the achievable power, are different. In both chip versions, the maximum peak voltage should be lower than 8 V for long-term reliability.

The Class E matching design flow here is shown on the TX path of a split configuration. The special steps required for DT design (incl. RX path design) are summarized in "5.4. Detailed Matching Procedure for Direct Tie Board Configuration" on page 77.

5.1. Goals for the Matching Procedure

The matching methodology for the Si4060/Si4460/61/67 RFIC is aimed at achieving the following simultaneous goals:

- Basically, obtain +10 dBm (Si4060/Si4460/67) or 14 dBm (Si4461) of conducted RF output power even in DT configuration with multilayer inductors. In some bands, the Si4060/Si4460/67 can achieve 13 dBm, and the Si4461 can achieve 16 dBm.
- Constrain the peak drain voltage so that it does not exceed +8 V.
- Maximize efficiency on the PA output stage.
- Comply with ETSI and FCC specifications for spurious emissions.

These goals will be met under the following conditions:

- Operation at any frequency in the 169 – 960 MHz range.
- Antenna load impedance = 50 Ω.
- The chip is commanded to reduced power level mode (PA_PWR_LVL register is typically between 18h and 2Fh).
- Output power is measured at the matching output after the low-pass filter.
- Limitation on peak drain voltage are met for any V_{DD_RF} = 1.8 V to 3.6 V
- Si4060/Si4460/67 Output power of +10 dBm is met for V_{DD_RF} = 3.3 V (minimum) with less than 20 mA current or, in some bands, the power of +13 dBm with less than 25 mA current, even with multilayer inductors.
- Si4461 Output power of +14 dBm is met for V_{DD_RF} = 3.3 V (minimum) with less than 34 mA current or, in some bands, the power of +16 dBm with less than 45 mA current, even with multilayer inductors.

5.1.1. Comments on Peak Drain Voltage Limit

It should be noted that the +8 V peak drain voltage limit referred to above is not the same as the absolute maximum voltage rating at which the device may experience permanent damage. This absolute maximum voltage rating is higher than +12 V on the TX output pin.

Instead, this peak drain voltage limit of +8 V has been calculated as a limit, which, if not exceeded for continuous periods of time, should allow for multiple years of operation without noticeable degradation in output power. That is to say, if the peak drain voltage were to momentarily slightly exceed +8 V, the device would likely not be instantaneously damaged but might suffer a small decrease in long-term reliability.

In all cases, the voltage limit specified by the absolute maximum voltage rating should not intentionally be exceeded (however briefly) because instantaneous damage may occur.

5.1.2. Comments on Achieving the Targeted Output Power

This section is largely targeted at applications that require +10 dBm (Si4060/Si4460/67) or +14 dBm (Si4461) output power. While this level of output power is readily achievable, meeting other design constraints, such as harmonics, requires careful attention to matching component selection and good board layout techniques. That is

to say, it is possible to fail through poor design and poor board layout practices.

5.2. Matching Procedure Overview

5.2.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for the Split TX/RX board configuration. Further details of each step will be provided later. The required design equations are discussed in “5.3. Detailed Matching Procedure for Split TX/RX Board Configuration”.

1. First, select a value for the pull-up inductor, L_{CHOKE}, that provides a very large impedance at the frequency of operation (and its nearest harmonics).
2. Choose/calculate values for series-resonant tank, L_0-C_0, such that L_0-C_0 resonates at Fo.
3. Calculate the required value of Z_{LOAD} given the desired frequency of operation (Fo) and the known shunt drain capacitance of the Si4060/Si4460/61/67 chip ($C_{SHUNT60/61}$ = ~1.25/2.0 pF).
4. Estimate the necessary back-off of the power level setting. For this, calculate the required value for a hypothetical voltage-limiting resistor given the desired output power and main chip supply voltage, V_{DD_RF}. However, the calculated value does not used as an R_{DC} in series with Lchoke; instead, it is used to estimate the tuned switcher loss.
5. Calculate the values for the matching components, L_X and C_X, given the antenna load resistance (e.g., R_{ANT} = 50 Ω) and the calculated value for Z_{LOAD}.
6. Design a low-pass filter to provide sufficient attenuation of harmonic signals.
   a. The unfiltered waveform at the TX output pin will inherently contain high levels of harmonics.
   b. Depending upon the output power level and the desired level of harmonic attenuation, a third- to fifth-order low-pass filter will likely be required.

5.2.2. Single Antenna with Direct Tie Board Configuration

The following steps provide a broad overview of the matching methodology for the Single Antenna with Direct Tie board configuration. Further details of each step will be provided later. The required design equations are discussed in "5.4. Detailed Matching Procedure for Direct Tie Board Configuration" on page 77.

1. The same as the first step in the split match design (see “5.2.1. Split TX/RX Board Configuration”)
2. The same as the second step in the split match design (see “5.2.1. Split TX/RX Board Configuration”)
3. The same as the third step in the split match design (see “5.2.1. Split TX/RX Board Configuration”)
4. The same as the fourth step in the split match design (see “5.2.1. Split TX/RX Board Configuration”)
5. The same as the fifth step in the split match design (see “5.2.1. Split TX/RX Board Configuration”)
6. The same as the sixth step in the split match design (see “5.2.1. Split TX/RX Board Configuration”).
7. Construct a four-element match to the differential RXp/RXn input pins using the methodology outlined in “AN643: Si446x/Si4362 RX LNA Matching”.
8. At 868/915 MHz, deliberately mis-tune the calculated value of L_0 downwards by approximately 20-30%. At 315/434 MHz, the split L_0 values usually work well.

5.3. Detailed Matching Procedure for Split TX/RX Board Configuration

In this section, we provide further detail about each step of the matching procedure for the Split TX/RX board configuration outlined above. We assume a general chip supply voltage of V_{DD_RF} = 3.3 V.

5.3.1. Step #1: Select a Value for L_{CHOKE}

In Step #1, we select an appropriate value for the pull-up inductor, L_{CHOKE}.

In the theoretical derivation for Class-E switching amplifiers, it is desired that the impedance of the pull-up inductor, L_{CHOKE}, be zero at dc and infinite at all other frequencies. This is not achievable in practice; however, a large value of inductance provides a reasonable approximation of this performance. The value of L_{CHOKE} should be chosen such that it provides a high impedance at not only the fundamental operating frequency but also at the first few harmonic frequencies. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 270 nH to 390 nH
- 470 MHz: approximately 220 nH
- 915 MHz: approximately 100 nH

With these inductance values, the self-resonant frequency is at least three times higher than the operating frequency.

5.3.2. Step #2: Choose/Calculate Values for the L_0-C_0 Series-Resonant Tank

In Step #2, we design the L_0-C_0 tank to be series-resonant at the desired operating frequency, Fo.

It is self-evident that there is an infinite number of combinations of L_0-C_0 values that can achieve resonance at a desired frequency. However, certain broad guidelines may be used to select one particular solution of component values.

First, it is desirable that the inductive and capacitive values be neither very large nor very small. Discrete inductors and capacitors with very large values are subject to degrading effects due to self-resonance. Discrete components with very small values are subject to greater degradation due to component tolerance. In either case, the actual resonant frequency of the tank may be significantly different than the frequency predicted by mathematical calculations.

Second, in the theoretical derivation for Class-E switching amplifiers, it is desirable for the impedance of the L_0-C_0 series-resonant tank to be zero at Fo and infinite at all other frequencies. This is not achievable in practice; however, a reasonable approximation of this performance may be obtained by using values with a high L-to-C ratio.

Third, it is desirable to minimize the insertion loss of the resonant tank. Since the quality factor (Q) of discrete inductors is generally much lower than that of discrete capacitors, it is important to select an L_0-C_0 ratio that maximizes the inductor Q. The Q of discrete inductors generally increases as the inductance value is increased until the inductance approaches the value where self-resonance becomes a concern.

Finally, it is desirable to select component values that are near standard 5% tolerance values. Unfortunately, this is rare in the case of multilayer inductors.

These considerations lead to the following guidelines for selecting the values for L_0-C_0:

- The L_0-C_0 tank must resonate at Fo.
- The value of L_0 should be chosen as large as possible (while remaining low enough for the effects of self-resonance to not be an issue and are close to standard 5% tolerance values).

In the present 868M design, we choose 3.6 pF as C0 and 9.3 nH as an L0 value.

5.3.3. Step #3: Calculate the Required Value for Z_{LOAD}

In Step #3, we calculate the required value of load impedance to be presented to the output of the L_0-C_0 resonant tank at the fundamental operating frequency, Fo.

In the theoretical derivation for Class-E switching amplifiers, it may be shown that the equations for output power (P_{OUT}) and load impedance (Z_{LOAD}) as a function of shunt drain capacitance (C_{SHUNT}) and supply voltage (V_{DD}) are as follows:

$$P_{OUT} = \pi\omega_0 C_{SHUNT} V_{DD}^2$$

Equation 20.

$$Z_{LOAD(fund)} = \left(\frac{0.2815}{\omega_0 C_{SHUNT}}\right) e^{j \times 49.0524°}$$

Equation 21.

These two equations are quite interesting. Equation 20 states that the theoretical output power is not a function of load impedance, but instead depends only upon the shunt drain capacitance (C_{SHUNT}), the desired operating frequency ($\omega_o = 2\pi Fo$), and the PA supply voltage (V_{DD}). Equation 21 states that the required load impedance (Z_{LOAD}) does not vary with the desired level of output power but depends only on the desired operating frequency and the value of shunt drain capacitance.

The value of shunt drain capacitance, C_{SHUNT}, is a design parameter of the Si4060/Si4460/61/67 RFICs and is not adjustable by the user. This shunt capacitance is composed primarily of the drain-source capacitance, C_{ds}, of the output MOS cascade devices in parallel with a small amount of explicit integrated capacitance. Silicon Labs states that the value of this shunt drain capacitance is approximately:

$$C_{SHUNT} = 2.0 \text{ pF for Si4461 and } C_{SHUNT} = 1.25 \text{ pF for Si4060/Si4460/67}$$

These values may be substituted in the equations above and used to calculate other matching parameters. Assuming a desired operating frequency of Fo = 868 MHz as an example, the following value for Z_{LOAD} may be calculated, e.g., for the Si4060/Si4460/67:

$$Z_{LOAD(868M)} = \left(\frac{0.2815}{2\pi \times 868M \times 1.25\text{ pF}}\right) e^{j \times 49.0524°} = 27.06 + j31.18\Omega$$

Equation 22.

This is the value of load impedance (at the fundamental operating frequency) that must be presented to the output of the L_0-C_0 resonant circuit.

It should be clearly understood that this value of load impedance (Z_{LOAD}) discussed above and the antenna impedance (Z_{ANT}) are not the same parameter nor do they necessarily have the same ohmic value. Given the arbitrary impedance of the antenna, one of the next tasks is to construct a matching network that transforms Z_{ANT} into Z_{LOAD}, as seen at the output of the L_0-C_0 resonant circuit.

5.3.4. Step #4: Estimate the Required PA_PWR_LVL Register Value from the Calculated Value of a Voltage-Limiting Resistor

In Step #4, we estimate the necessary power back-off, i.e. the DDAC field value of the PA_PWR_LVL register required for the desired output power. For this, the calculation of a hypothetical voltage-limiting resistor (not used directly in the circuit as R_{DC}) is required for a given specified value of PA supply voltage (V_{DD}).

Equation 20 clearly shows that, for a given desired operating frequency, the only "knob" remaining to the user to select the output power is the PA supply voltage, V_{DD}, since the value of C_{SHUNT} is an internal chip design parameter and is not adjustable by the user. Equation 20 is easily solved for V_{DD}, which is found to be:

$$V_{DD} = \sqrt{\frac{P_{OUT}}{\pi \omega_0 C_{SHUNT}}}$$

Equation 23.

Continuing our design example at 868 MHz and assuming a desired output power of +13.7 dBm (~23.4 mW) to compensate the losses and get ~13 dBm after filtering, the required value of V_{DD} may be calculated as:

$$V_{DD} = \sqrt{\frac{0.0234}{2\pi^2 \times 868\text{M} \times 1.25\text{ pF}}} = 1.045\text{ V}$$

Equation 24.

This equation states that, if the voltage supplied to the top of pull-up inductor L_{CHOKE} is equal to 1.045 V and the previously-calculated value of load impedance, Z_{LOAD}, is presented to the chip, the resulting output power will be P_{OUT} = 23.4 mW = +13.7 dBm at the class E tank output in an ideal, loss-free case.

This required PA supply voltage (V_{DD}) is significantly different than the general supply voltage (V_{DD_RF}) for the rest of the RFIC (e.g., for the VBATA and VBATD input pins). It is obviously not desirable to maintain two separate, independent sources of supply voltage for the RFIC; therefore, it is convenient to create the PA output supply voltage from the main supply voltage by means of an I-R voltage drop across a resistor.

This resistor can be either a series external one with Lchoke, as shown in Figure 3 on page 12 (R_{DC}), or an internal switcher loss. Although introducing the switcher loss instead of R_{DC} resistor results in a somewhat different operation, the final aim is achieved, i.e., the current flowing through on the switcher is limited, and, thus, the peak of the off-state voltage transient on Lchoke is reduced. The use of the internal loss instead of an external R_{DC} yields higher efficiency because, at significantly reduced power states, the previous internal PA drivers consume less current. Since the *theoretical* efficiency of an ideal Class-E switching amplifier tank is 100%, the average drain current, I_{DD}, may be calculated as:

$$P_{OUT} = \pi \omega_0 C_{SHUNT} V_{DD}^{\ 2} = I_{DD} V_{DD}$$

Equation 25.

This equation may be solved for I_{DD} to obtain:

$$I_{DD} = \pi \omega_0 C_{SHUNT} V_{DD}$$

Equation 26.

Given the main supply voltage for the remainder of the chip (V_{DD_RF}) and having previously calculated the required value of PA supply voltage (V_{DD}) and average drain current (I_{DD}), it is a simple matter to calculate the required value for R_{DC}:

$$R_{DC} = \frac{V_{DD\_RF} - V_{DD}}{I_{DD}}$$

Equation 27.

Continuing our design example at 868 MHz for +13.7 dBm class E tank output power, we calculate:

$$I_{DD} = 2\pi^2 \times 868\text{M} \times 1.25\ \text{pF} \times 1.045\ \text{V} = 22.4\ \text{mA}$$

Equation 28.

Assuming a general chip supply voltage of V_{DD_RF} = 3.3 V, we calculate:

$$R_{DC} = \frac{3.3 - 1.045}{0.0224} = 100.7\ \Omega$$

Equation 29.

Theoretically, this value of resistance must be placed in series with L_{CHOKE} (if it is loss-free) in order to drop the general chip supply voltage down to the value required to obtain the desired output power. In actuality, due to losses at the operation frequency (e.g., Lchoke has significant losses on the order of 10 to 15 Ω, and there are other component losses as well), the required resistance value is lower.

This power is achieved at a Si4060/Si4460/67 DDAC field (of the PA_PWR_LVL register) value of ~34h with wire-wound inductors at 3.3 V. At this power setting, the switcher loss is approx ~88 Ω; so, together with the other losses, it is a realistic value.

5.3.5. Step #5: Calculate the Values for Matching Components L_X and C_X

In Step #5, we calculate the values of the matching components required to transform the given antenna impedance, Z_{ANT}, into the required load impedance, Z_{LOAD}.

This matching effort may accomplished by simple and normal design methods, such as the Smith Chart or impedance matching CAD software (e.g., WinSmith™). Continuing our design example at 868 MHz and assuming an antenna impedance of $Z_{ANT} = R_{ANT} = 50\ \Omega$, we find that 50 Ω may be transformed to the required value of $Z_{LOAD} = 27.1 + j\ 31.2\ \Omega$ by shunt matching capacitance $C_X = 3.39$ pF and series matching inductance $L_X = 10.26$ nH. The resulting circuit topology is shown in Figure 23.

It should be noted that this is only one possible solution for the required impedance transformation; other matching topologies could have been used as well. The reader should also note that the required L_X-C_X match topology depends upon the real part of the load impedance, $Re(Z_{LOAD})$. In this example, the real part of the load impedance was less than 50 Ω and thus an appropriate matching topology consisted of a shunt capacitor (C_X) and a series inductor (L_X). In the event that $Re(Z_{LOAD})$ had been greater than 50 Ω, an appropriate matching topology would have consisted of first a series inductor (L_X) followed by a shunt capacitor (C_X).

It is apparent that series inductors L_0 and L_X in Figure 24 may be combined into one equivalent inductor with a value equal to the sum of their individual inductances in order to reduce parts count. This is a normal and usual practice.

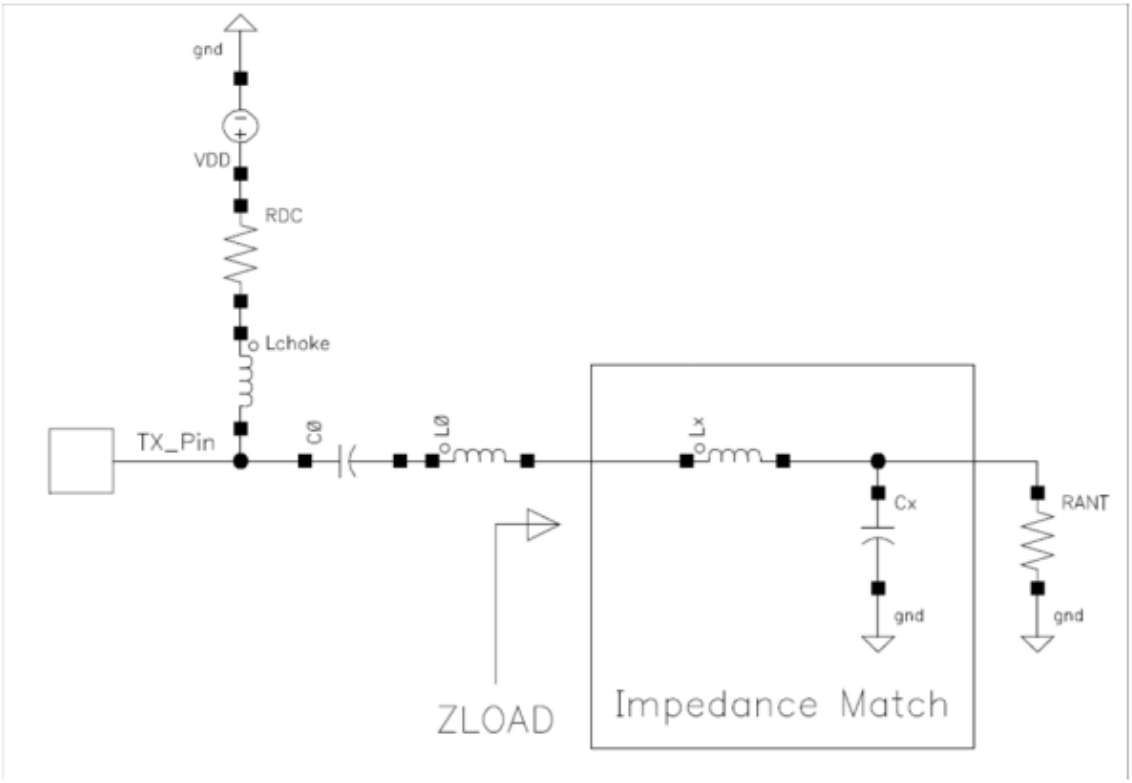

Figure 24. Impedance Match to Transform R_{ANT} to Z_{LOAD}

5.3.5.1. Voltage Waveforms at TX Output Pin

At this point, the *basic* PA output match is complete. Although we have not yet designed a low-pass filter to sufficiently attenuate the harmonic signals, it is possible to measure the output power by substituting a power meter or spectrum analyzer in place of the antenna impedance, R_{ANT}.

It was previously mentioned that the peak of the drain voltage waveform in a Class-E switching amplifier may reach levels of $V_{PEAK} = 3.56 \times V_{DD}$. (This statement was offered without proof; for those readers interested in the derivation, refer to the papers listed in "4.4. Theory of Operation of an Ideal Switching PA" on page 53.) It is desirable to measure the actual drain voltage waveform in order to ensure compliance with our stated design goal of constraining the peak drain voltage to less than 8 Vpk.

It is not difficult to verify the resulting voltage waveform at the TX output pin (at least for the lower frequency bands of operation). A high-speed oscilloscope with an input bandwidth of at least 4 GHz (preferably higher) is required. A low-capacitance, high-bandwidth scope probe is also required, or, alternatively, the “resistive-sniffing” network of Figure 25 may be used. In this schematic, it may be seen that the inductors, L_0 and L_X, have been combined into one equivalent series inductance.

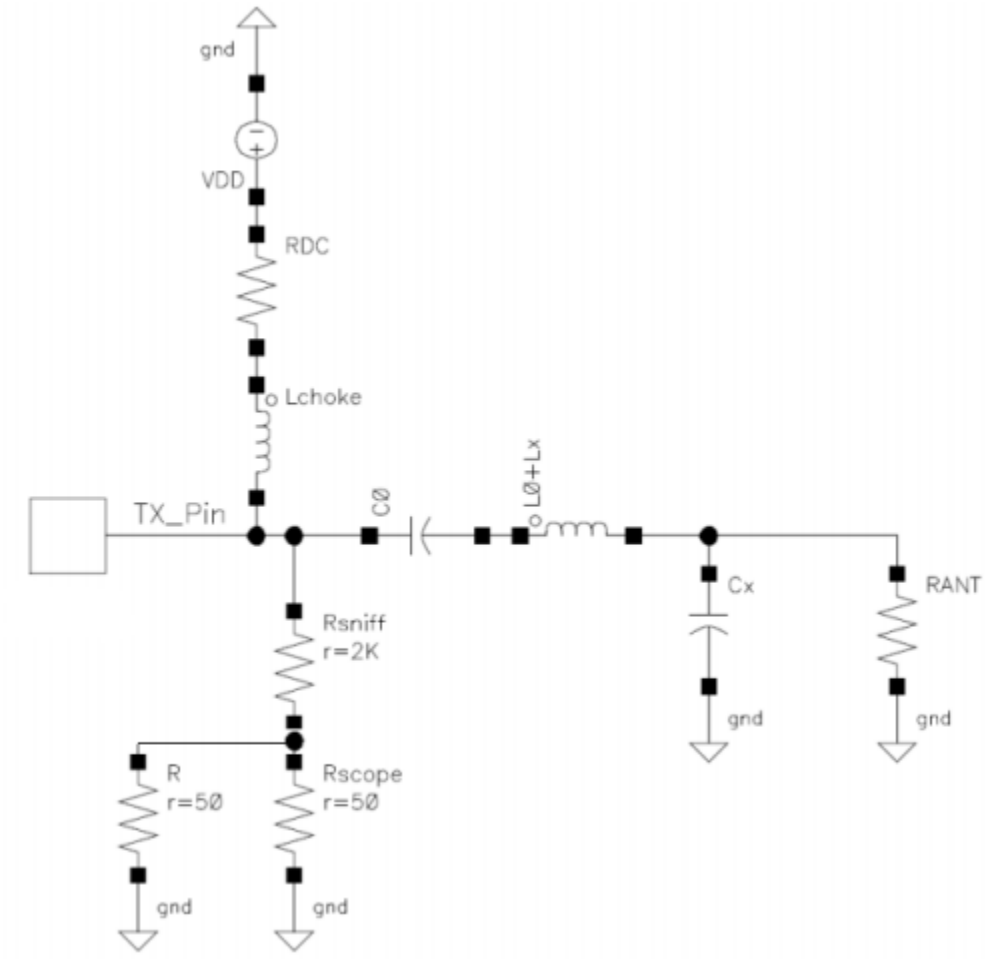

Figure 25. Resistive Sniffing Network

Using the “resistor sniffing” technique of Figure 25, the drain voltage waveform of Figure 26 was observed for an operating frequency of Fo = 868 MHz. In the example shown here, the following component values (obtained through use of the design equations above) were used:

- $P_{OUT(TARGET)}$ = +13.7 dBm
- VDD_RF = 3.2 V
- C_{SHUNT} = 1.25 pF (Si4460/67)
- L_{CHOKE} = 100 nH
- R_{DC} = 0 Ω
- DDAC value is 0x35
- C_0 = 3.6 pF
- L_0+L_X = ~19 nH
- C_X = 3.3 pF

The measured output power was +13.7 dBm at power state 0x35 at 3.2 V. The power state 0x35 required for the targeted power corresponds to approximately 86 Ω switcher on state loss. Together with the dc resistance of the Lchoke, it is approximately 88 Ω; so, the introduced loss is slightly lower than what is calculated by Equation 29. This is because the design equations above assume ideal switching operation of the output devices (i.e., zero ON-state resistance, infinite OFF-state resistance, zero switching time, etc.) as well as lossless discrete matching components. A practical switching amplifier and output match will inherently fall short of such ideal operation; some small degradation in output power is to be expected, which has to be compensated for by a slight increase of the PA power level setting (i.e further decrease of switcher on-state impedance). In any case, the difference is not significant.

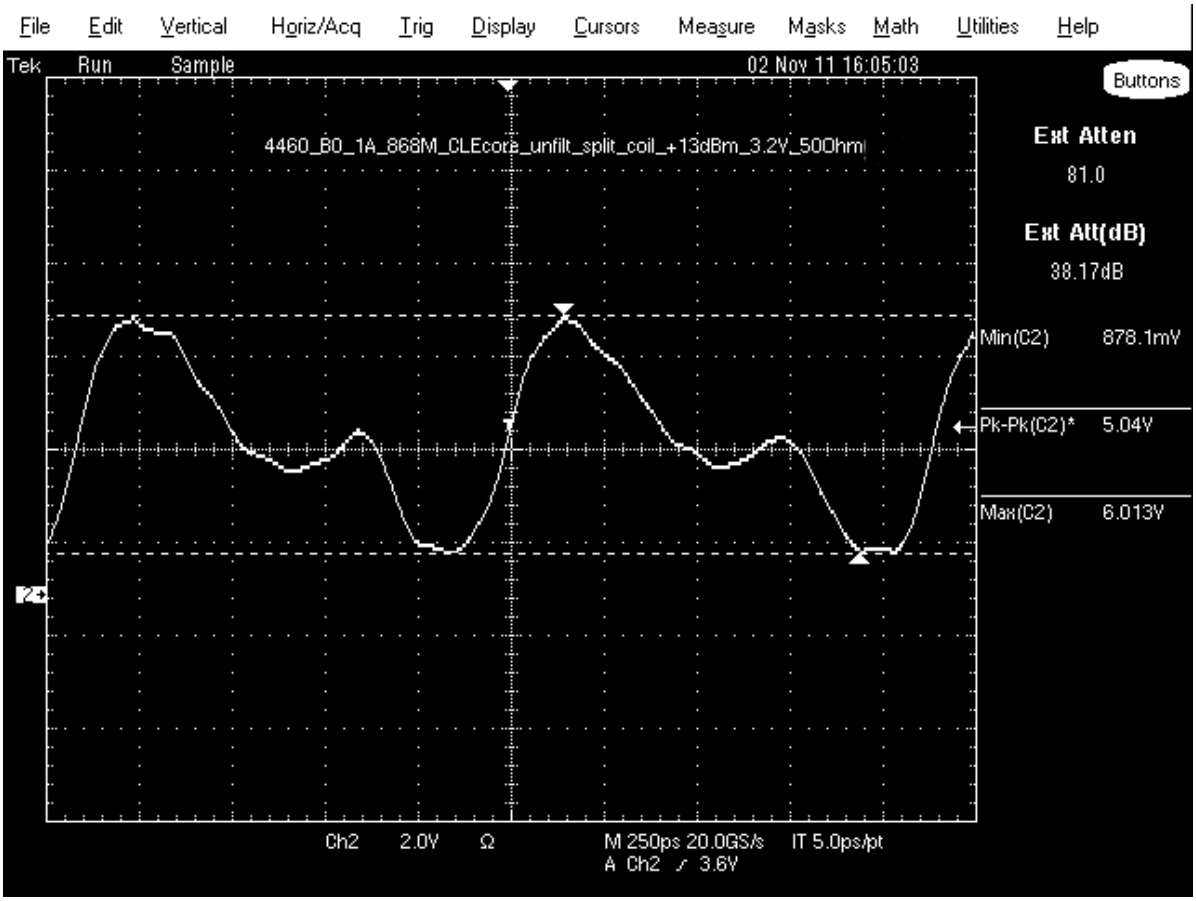

Figure 26. Drain Voltage Waveform (Fo = 868 MHz)

As can be observed in Figure 26, the measured waveform deviates to some extent from the theoretical “Class-E like” waveform at higher (868 MHz) frequencies. However, the maximum drain voltage is 6 V, much less than the critical 8 V.

It should be noted that the waveform would be closer to the theoretical Class E waveform at lower (315/868M) frequencies, as shown in Figure 27. As the operating frequency increases, it also becomes more difficult to faithfully observe the waveform. The input bandwidth of the oscilloscope used to display the waveform must increase in accordance with the operating frequency. Additionally, parasitic capacitances of the sniffing system and/or in the PCB layout as well as in the output device(s) of the RFIC tend to limit the high-frequency response of the amplifier.

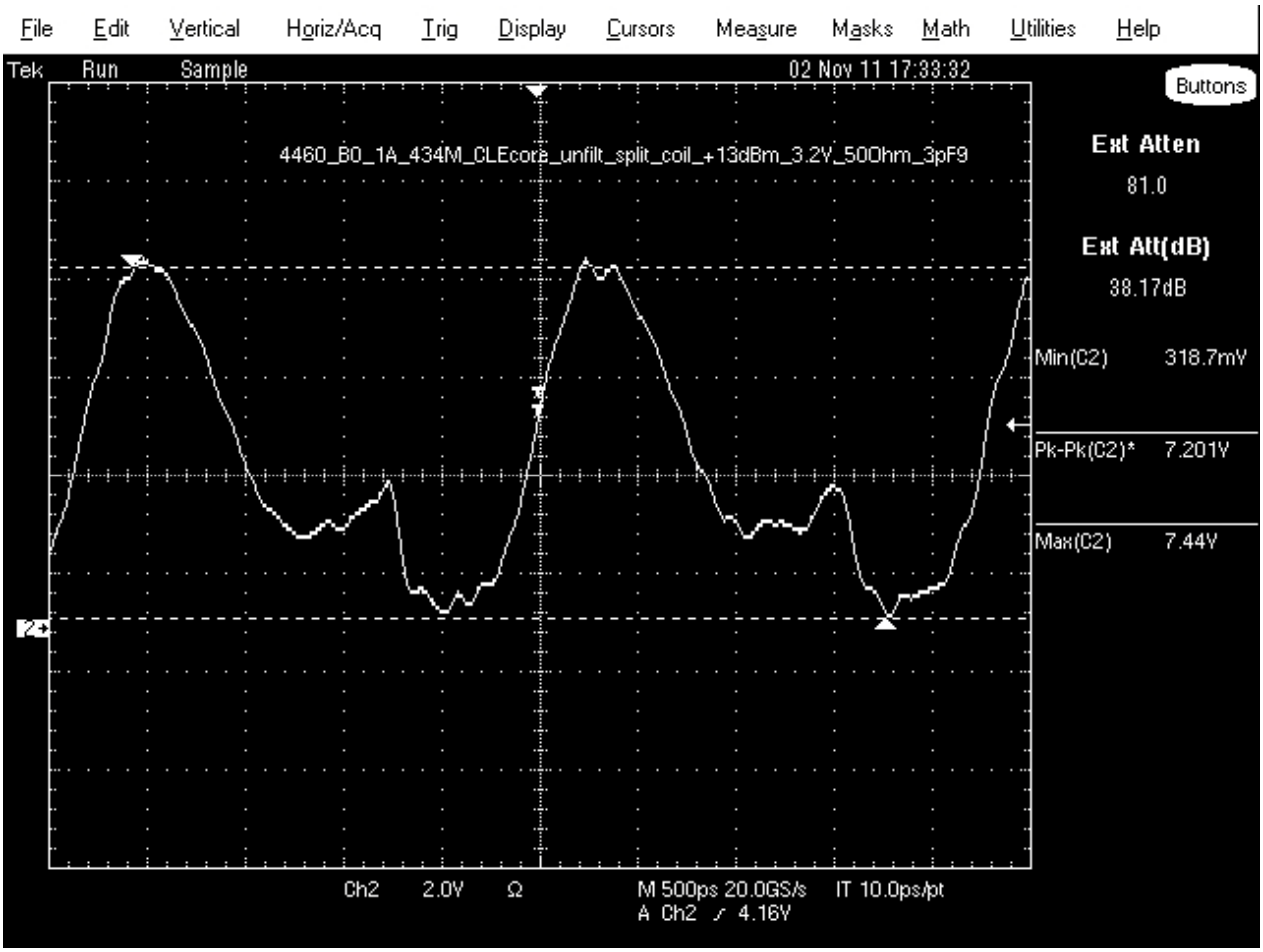

Figure 27. Drain Voltage Waveform of a 434 MHz Class E Tank

5.3.6. Step #6: Design a Low-Pass Filter

In Step #6, we design a low-pass filter network to attenuate the harmonics below the level required to meet applicable regulatory standards (e.g., FCC or ETSI).

5.3.6.1. Unfiltered Harmonic Spectrum

It should be understood that the waveform at the output of the match shown in Figure 24 will still contain relatively high levels of harmonics. Although the bandpass response of the series-resonant L_0-C_0 tank provides some attenuation of harmonic signals, it is generally not sufficient to meet applicable regulatory standards. This is normal for such a switching-amplifier and matching topology.

By way of example, the harmonic spectrum at the antenna load, R_{ANT}, for the matching network and component values of Figure 25 is shown in Figure 28 at power state 35h with 25.4 mA total current consumption at 3.2 V.

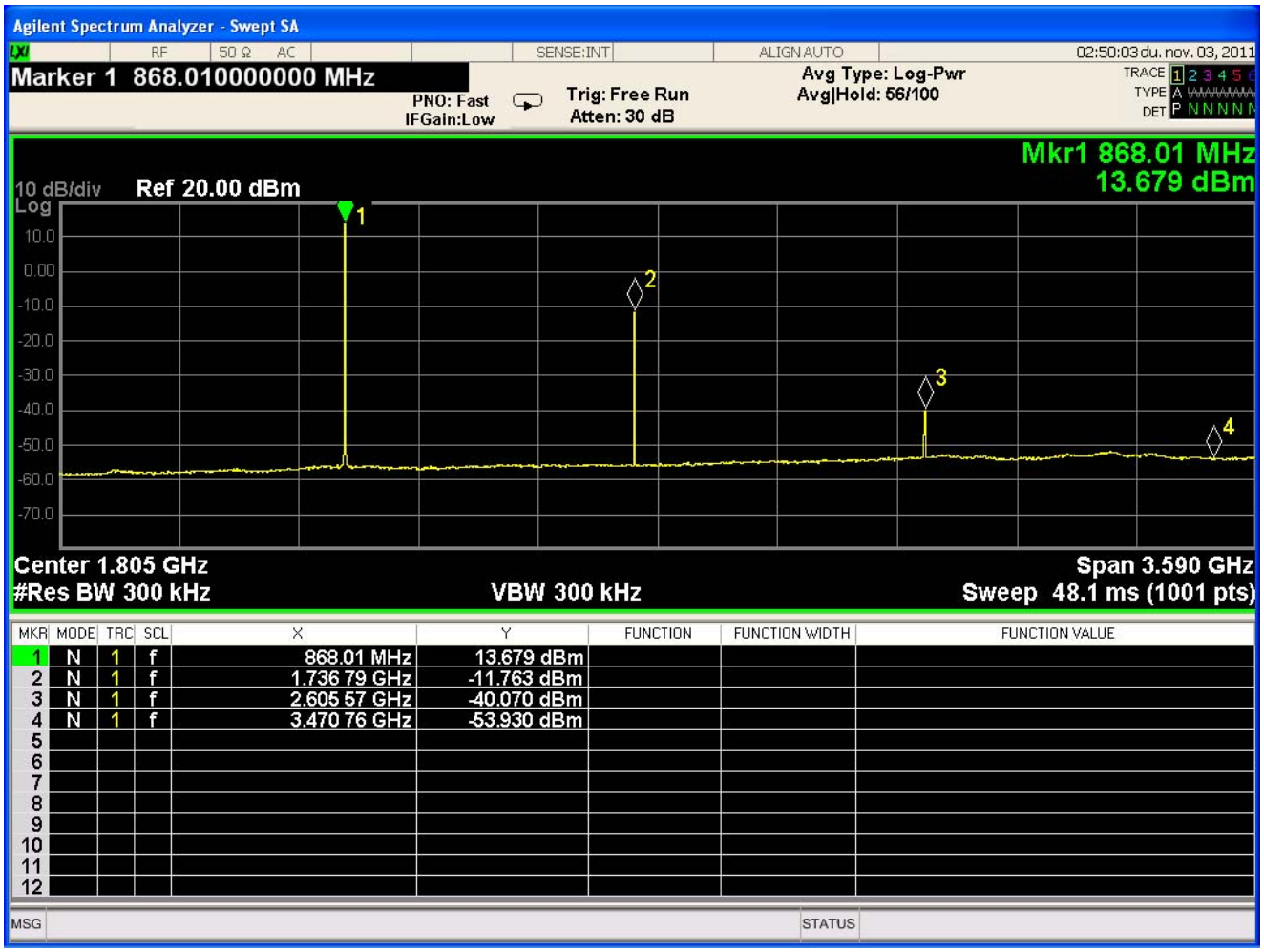

Figure 28. Unfiltered Harmonic Spectrum at Power State 35h at 3.2 V (Fo = 868 MHz, 25.4 mA Total Current)

It must be noted that this Class E tank mainly uses the calculated values, assuming ideal loss and a parasitic-free case. As described earlier, in a real realization, there are losses, non-ideal switching characteristics, and several other parasitics, which degrades the operation with the calculated ideal values. Due to this, some bench tuning is usually useful to improve the performance. Although its mechanism is not fully clarified yet, a typical way to improve efficiency is to decrease the value of Cx (i.e., CM as it is denoted in "2. Summary of Matching Network Component Values" on page 6). In cases of strongly-reduced power (10 dBm Si4060/Si4460/67 design), the slight increase in C0 may also improve the efficiency. In any case, bench tuning/tweaking is always useful in the case of such a strongly nonlinear circuit.The following sections describe the final design with filtering.

5.3.6.2. Filtering Requirements

Since customers may operate under widely-differing regulatory standards, each with differing harmonic requirements, it is difficult for Silicon Labs to recommend one single low-pass filter design that is appropriate for all customers. However, a common regulatory standard that may be applicable to our design example at 868 MHz is ETSI Part EN300 220. This standard specifies the permitted levels of fundamental and harmonic frequencies in terms of Effective Radiated Power (ERP). The 868 MHz ETSI frequency band comprises several sub-bands with different properties. For example, the allowed power varies between +7 and +27 dBm with the most cases of 14 dBm ERP. At our desired operating frequency of 868.3 MHz (G1 sub-band), these maximum permitted ERP levels are:

- Fundamental = +14 dBm ERP
- Harmonics = –30 dBm ERP

Since the limits are specified in terms of ERP, compliance must be verified by measuring in an anechoic chamber with the unit operated into its intended antenna. The ERP is the power required to the input of an ideal dipole antenna with a gain of 2.14 dB to generate the same electric field at the far field. However, if an ideal isotropic antenna is assumed with 0 dB gain, higher conducted power is required at the antenna input by 2.14 dB. This equivalent level of conducted power is known as Equivalent Isotropic Radiated Power or EIRP.

Using EIRP limits, the equivalent conducted power ETSI limits are slightly higher:

- Fundamental = +16.14 dBm EIRP
- Harmonics = –28.86 dBm EIRP

It can be seen that the targeted +13 dBm power level with the Si4060/Si4460/67 is approx 3 dB lower than the fundamental EIRP limit of the ETSI; so, in theory, the gain of the applied antenna can go up to 3 dB. Unfortunately, in real applications, the typical monopole antenna gain is –5 to +2 dB, depending on many variables, such as available space, circuit dimensions (working as an electrical mirror ground plane), case, etc.; so, the ETSI fundamental limit is not approached in most cases. If operation close to the ETSI fundamental limit is required, Silicon Labs recommends the stronger Si4461.

On the other hand, the same antenna can became a good radiator at the harmonic frequencies where the antenna's relative size is longer and the same circuit (ground plane) dimensions give better electrical mirror properties, i.e. better radiation. It is especially true if the antenna impedance, varying strongly with frequency, causes acceptable reflection levels at these harmonic frequencies.

In any case, most of the antenna properties strongly depend on the actual antenna design and are difficult to predict in advance. Therefore, to have margin for a possible worst-case scenario, Silicon Labs usually defines the conducted harmonic levels to be 5 to 6 dB lower than the ERP limit; that is, in the case of 868 MHz operation, the harmonic levels should be below. ~–36 dBm.

5.3.6.3. Selecting a LPF Order and Type

Given the unknown radiation efficiency of every possible antenna selectable by the user, it is difficult for Silicon Labs to conclusively state the required filter attenuation characteristics. As a reasonable design compromise, the following design goals for the low-pass filter were settled upon:

- Minimal insertion loss at the desired operating frequency.
- A minimum conducted level of –36 dBm at all harmonic frequencies. Since the most critical second harmonic level is approx –8 to –10 dBm, the necessary minimum harmonic attenuation is approx 28 dB.
- The lowest filter order possible to still achieve this required harmonic attenuation.
- A 1:1 impedance transformation (i.e. 50 Ω input and 50 Ω output impedance).

Note that the amplitude characteristics in the lower portion of the passband of the LPF are relatively unimportant because the output signal contains no frequency components below the fundamental frequency. We are free to choose the filter type (e.g., Butterworth, Chebyshev, Elliptic) based primarily upon the filter's attenuation characteristics rather than its passband response.

A Butterworth filter design is not optimal because it provides relatively poor high-frequency attenuation characteristics; there is no need to sacrifice high-frequency attenuation in order to obtain a maximally-flat in-band frequency response.

Similarly, an Elliptic filter design (Cauer-Chebyshev) may provide insufficient attenuation at higher-order harmonic frequencies. While it may be possible (and advantageous) to tune a transmission zero in the stopband to the frequency of a problematic harmonic (e.g. N = 2 or N = 3), it is paid for with a decrease in attenuation at higher harmonic frequencies. As the unfiltered harmonic spectrum of Figure 28 shows, there remain several higher-order harmonics with significant energy that cannot be ignored and must be attenuated.

As a result, we settle on a Chebyshev low-pass filter design as an acceptable type of filter response.

With a Chebyshev filter, it is possible to obtain a greater rate of attenuation roll-off in the stopband by accepting a larger amount of amplitude ripple in the passband. The next issue to be addressed is the amount of passband ripple to be targeted in the filter design.

Greater attenuation at high frequencies can be obtained by employing a filter designed for a relatively large amount of passband ripple, but this trade-off should not be pushed too far. While a reasonable amount of passband ripple is perfectly acceptable, there is a limit to what can be considered reasonable.

Figure 29 shows the passband frequency response of an ideal (lossless) Chebyshev filter with 0.17 dB of amplitude ripple in the passband. It is quickly apparent that, in order to minimize the insertion loss of the filter at the desired operating frequency, it is necessary to design the cutoff frequency of the filter such that the desired operating frequency falls at one of the passband amplitude ripple peaks (Cursor "A" in the plot). If the filter cutoff frequency varies due to component tolerances, the filter response may vary such that the desired operating frequency falls on a minimum of the amplitude ripple response rather than on a maximum. In such a scenario, the filter insertion loss will increase, and the TX output power will decrease.

By designing for a limited amount of passband amplitude ripple, an upper limit is placed on the filter insertion loss due to mistuning of the component values. It is the opinion of Silicon Labs that a Chebyshev passband amplitude ripple of 0.15 dB to 0.5 dB represents a reasonable design trade-off between high-frequency stopband attenuation and potential passband filter insertion loss due to component tolerance.

As mentioned earlier, at 868 MHz, the filter attenuation should be at least 26 dB at the second harmonic frequency. To achieve this, at least a five-order filter is required with the targeted ripple level. Since the cost of an SMD capacitor is usually much lower than that of an SMD inductor (even though they are multilayer ones), it is advantageous to chose a filter structure in which the filter starts with a parallel capacitance (PI topology).

As usual, the SMD inductors, especially the multilayer ones, have much lower Q than the SMD capacitors; the lower number of series inductors is also advantageous since the extra attenuation caused by the losses is lower.

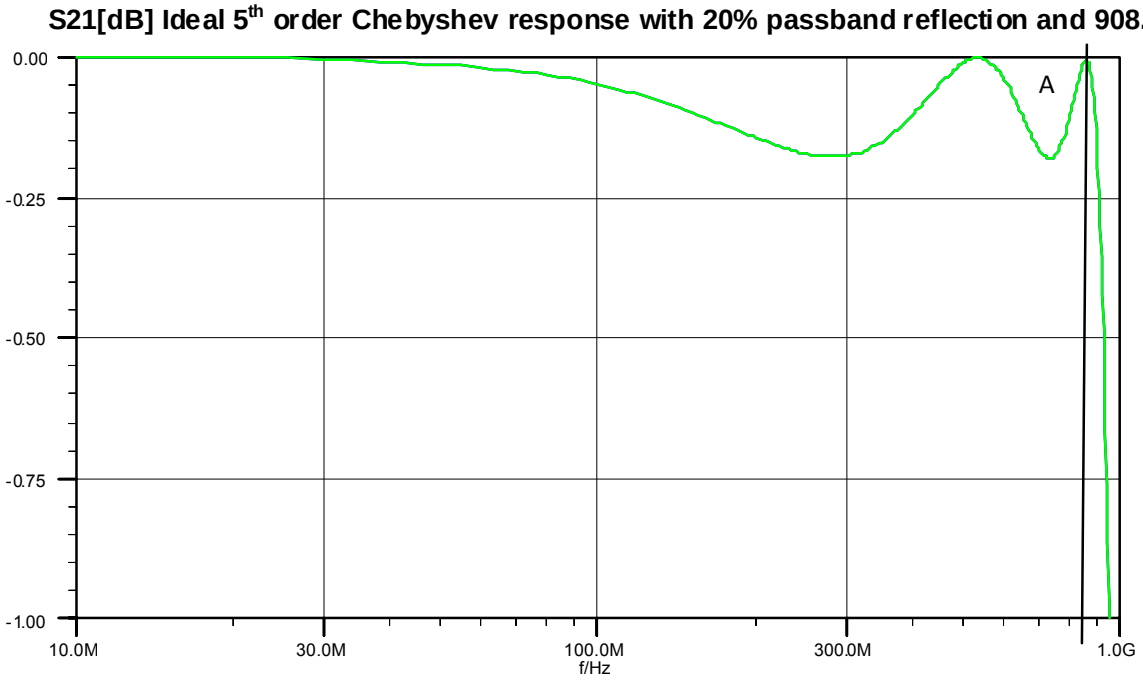

Figure 29. Ideal 5th-Order 0.17 dB Ideal Chebyshev Filter Response at 868 MHz

5.3.6.4. Calculation/Design of Component Filter Values

Actual filter component values may be obtained by the usual design methods, such as Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation.

Due to the attenuation margin of the fifth-order design and the extra loss introduced by the losses, a slightly lower ripple prototype is chosen here: T520, that is, the maximum passband voltage reflection is 20%, which corresponds to approximately 0.17 dB ripple in a loss-free case.

The possibility of a fourth-order filter was also investigated, but, with that, the highest attenuation at the second harmonic is around 28 to 29 dB, that is, at the edge without loss parasitics. In order to have margin and also decrease the insertion loss (i.e. achieve better attenuation with lower passband loss) the fifth-order filter was chosen. Moreover, the fifth-order filter uses only one more capacitor, which is a very low-cost element.

Note that Silicon Labs recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or at the equal amplitude ripple cutoff frequency (F_{ERCUT}). In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized. For a fifth-order 0.17 dB Chebyshev filter, the ratio of FERCUT to FPEAK is approximately 1.0468:1. That is, if the desired operating frequency is 868 MHz, the filter must be designed for an F_{ERCUT} of
868 x 1.0468 = 908.6 MHz.

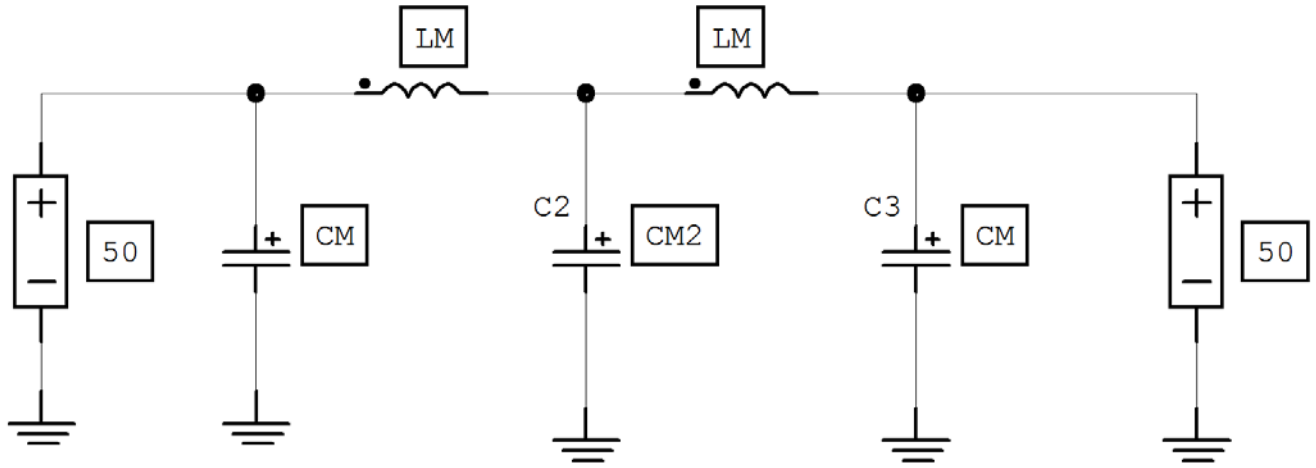

Figure 30. 3rd-Order PI-Topology Low-Pass Filter

Figure 30 shows the general architecture of a fifth-order, low-pass filter using the PI-topology. After design of a 0.17 dB ripple Chebyshev filter with a peak frequency of 868 MHz (F_{ERCUT} = 908.6 MHz), the following component values are obtained between 50 Ω termination impedances:

- CM = 4.561 pF
- LM = 11.79 nH
- CM2 = 7.458 pF

It is generally sufficient to use the nearest available standard 5% component tolerance values. Making these substitutions results in the following set of component values:

- CM = 4.7 pF
- LM = 12 nH
- CM2 = 7.5 pF

5.3.6.5. Simulation of Actual Filter Frequency Response

An ideal frequency response is not possible in practice because it is necessary to use inductors and capacitors that not only possess finite Qs but also internal self-resonances due to parasitic elements. These factors, as well as parasitic effects due to board layout, may cause the actual frequency response to be degraded relative to the ideal response shown in Figure 29.

The effects of using non-ideal components can be predicted by simulation with SPICE models obtained from the manufacturers of discrete components, such as Murata or CoilCraft. Figure 31 shows the simulated frequency response of this low-pass filter design implemented with the real (i.e. lossy) 5% components given above. Although the filter attenuation at the second harmonic frequency (1732 MHz) is very strong (58.8 dB) and far exceeds the design goal of 28 dB minimum, the attenuation at 868 MHz is also very high (~2.59 dB). The introduced losses and parasitics deteriorate the filter response significantly and increase the useful band attenuation to an unacceptable level.

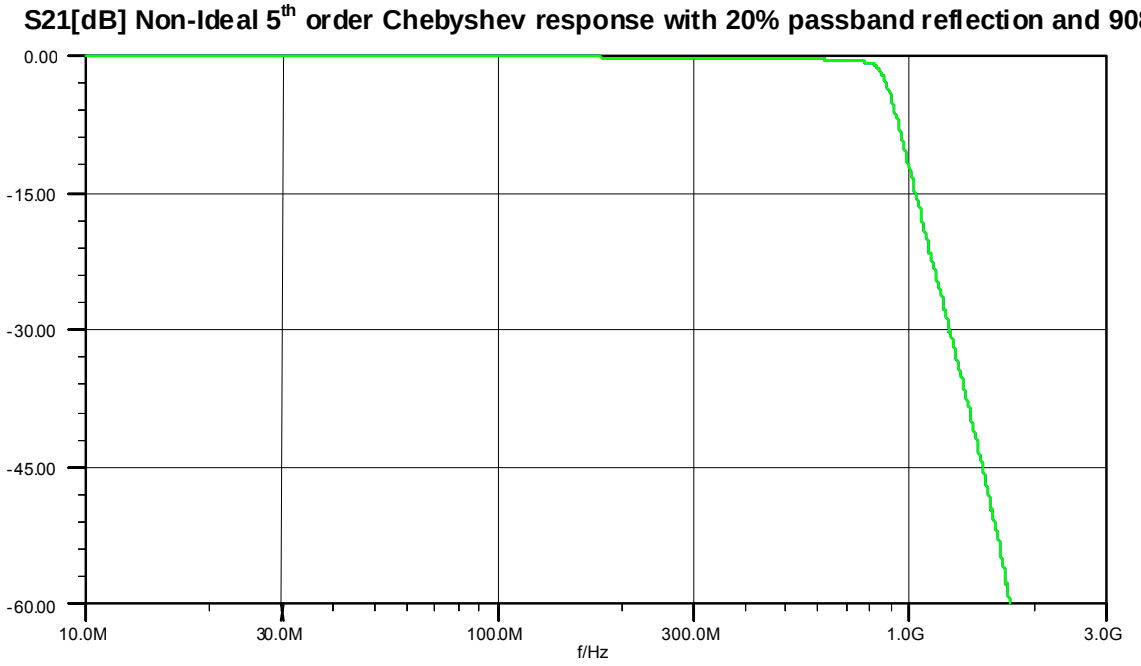

Figure 31. Non-Ideal Simulated Freq Response of 0.17 dB Chebyshev Filter (Fo = 868 MHz) with 5% Elements

A possible solution is to tweak the filter first in the simulator and later on the bench. Basically, some harmonic attenuation can be sacrificed to get lower attenuation at 868 MHz. The new set of element values after tweaking are:

- CM = 2.7 pF
- LM = 9.1 nH
- CM2 = 5.1 pF

The non-ideal filter response after adjustment is given in Figure 32. Here, the cutoff frequency is shifted up; thus, the simulated attenuation at 868 MHz is approximately 0.32 dB. The second harmonic (1732 MHz) attenuation is still ~29 dB (1 dB better than the targeted 28 dB). In addition, due to the parasitics, the attenuation decreases at very high frequencies (10th harmonic and above), but is still around –40 dB, which is far enough for the low-level high harmonics. The filter attenuation at higher harmonics easily exceeds the design target of 28 dB, thus validating the choice of filter type, order, and passband amplitude ripple.

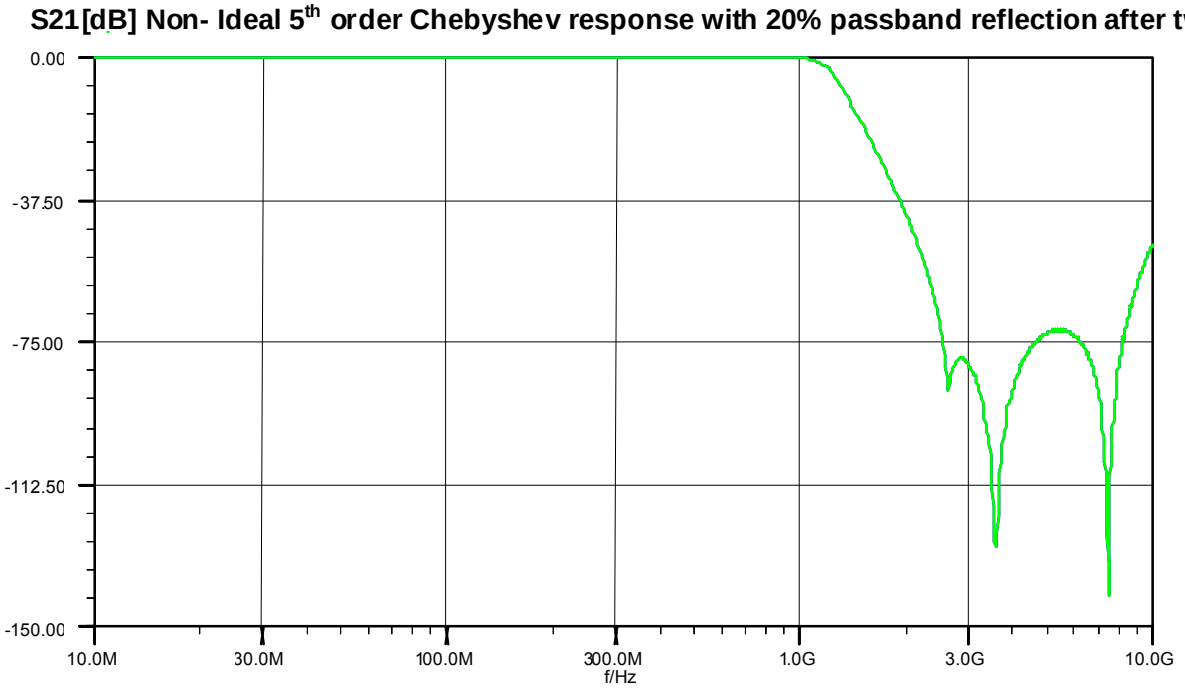

Figure 32. Non-Ideal Simulated Freq Response of 0.17 dB Chebyshev Filter after Adjustment (Fo = 868 MHz)

However, it should be clearly understood that Silicon Labs does not guarantee that a fifth-order low-pass filter design is appropriate for all customer applications. Depending upon the applicable regulatory standard and desired output power level, the filter order may need to be modified to suit a particular customer's needs.

It is apparent that there are transmission zeros in the simulated frequency response. These transmission zeros (e.g. near 3.6 and 7.45 GHz in Figure 32) are due to self-resonances in the discrete components. The shunt capacitors in the filter network (CM and CM2) exhibit a series self-resonance at some frequency, while the series inductors (L0, LM, and LM2) exhibit a parallel self-resonance at some frequency. The presence of such transmission zeros may help to "bend down" the attenuation curve more quickly, resulting in improved attenuation at lower harmonic frequencies, but at the cost of degraded attenuation at higher harmonic frequencies. Despite this, due to spreading issues, it is not advisable to rely too heavily upon "tuning" of these transmission zeros to aid in meeting harmonic performance.

5.3.6.6. Combining the LPF with the Output Match

The methodology used to design the low-pass filter was for a filter with a 1:1 impedance transformation ratio. That is, if the antenna impedance was R_{ANT} = 50 Ω, then the impedance seen looking into the input of the low-pass filter at C_M is also 50 Ω (at the fundamental frequency). Thus, our calculations for impedance matching components L_X and C_X remain unchanged. The resulting schematic for the output match and low-pass filter is shown in Figure 33.

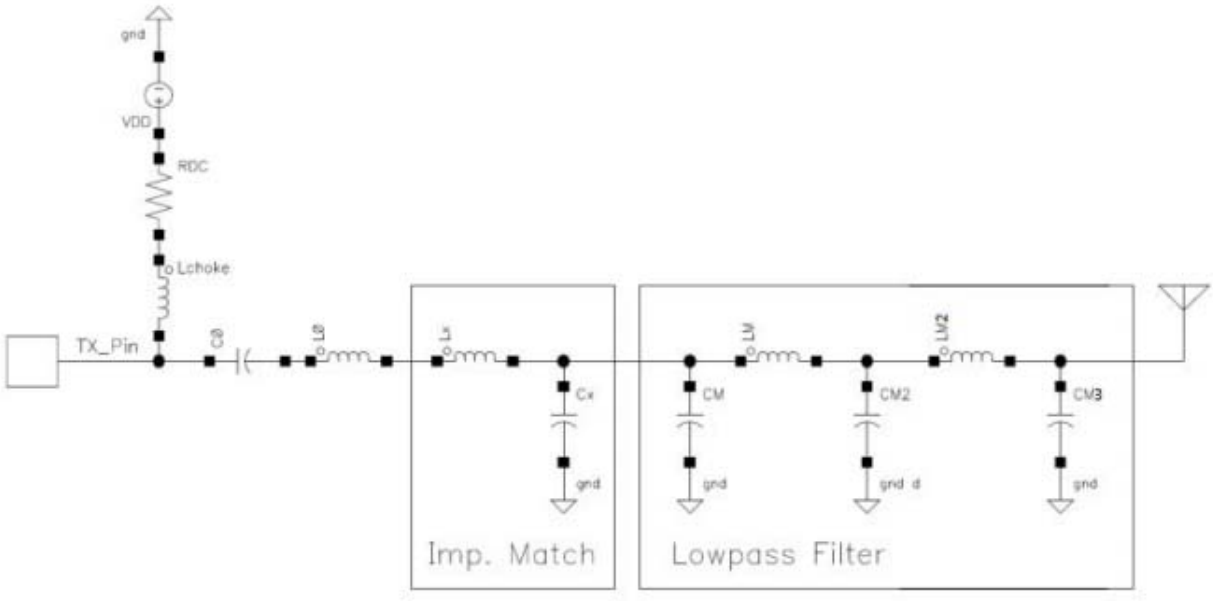

Figure 33. Schematic of Output Match and Lowpass Filter

However, it is quickly apparent that this schematic may be simplified. As discussed previously, series inductors L_0 and L_X may be combined into one equivalent series inductance. Shunt capacitors C_X and C_M may be combined in a similar fashion. After simplification, the schematic appears as shown in Figure 34. The combined value of L0 + Lx = 19 nH, while the combined value of CM + Cx = 6 pF.

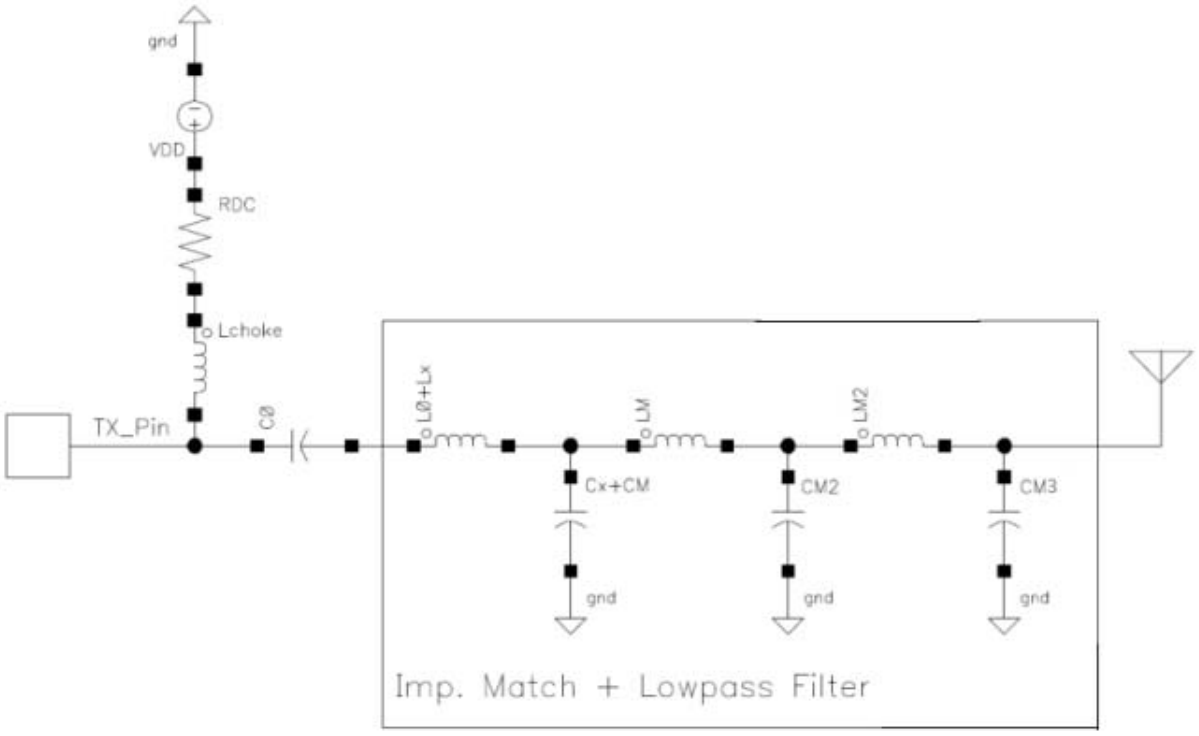

Figure 34. Schematic of Output Match and Lowpass Filter (Simplified)

After the filtered class E Tx match is finalized, some bench tuning is also advisable. As mentioned earlier, during the adjustment process, it was seen that the efficiency can be improved slightly if the shunt (CM + Cx, which, in any case, is denoted simply by CM in the tables in "2. Summary of Matching Network Component Values" on page 6) capacitor is reduced to 2.7 pF. Again, this sacrifices some second harmonic attenuation, but the harmonic spectrum still complies with a large margin (see Figure 35).

The final class E Split TX match component values are given for the Si4461 in Table 8 on page 13 and for the Si4060/Si4460/67 Table 13 on page 18.

5.3.6.7. Final Measurement of Harmonic Spectrum of the 13 dBm Class E High-Efficiency Match

The conducted output power spectrum of the final circuit is shown in Figure 35. These results are measured at the TX output power level setting of 0x31 of the Si4060/Si4460/67 RFIC with 22.8 mA total current consumption at 3.2 V supply voltage. As can be seen, the output power is approximately 0.5 dB lower than that without a filter, i.e the real lossy filter attenuation is approximately 0.5 dB. However, due to the reduced CM, the efficiency improved, and the total IC current is only 22.8 mA.

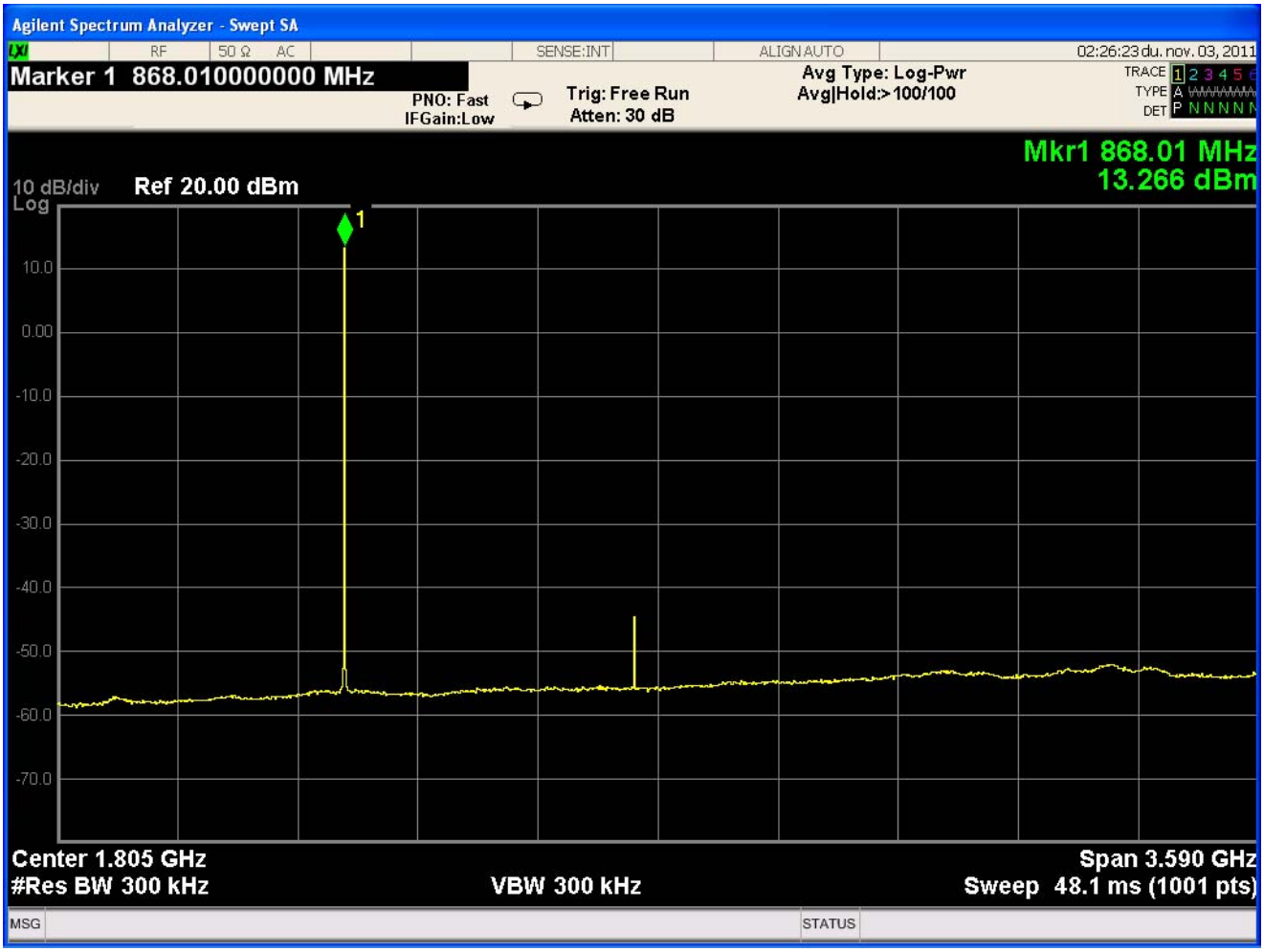

Figure 35. Filtered Harmonic Spectrum at Power State 0x31 (with 22.8 mA Total IC Current) of the 13 dBm Si4060/Si4460/67 High-Efficiency Class E Match (Fo = 868 MHz—See Table 12 on page 17)

5.3.6.8. Final Measurement of Harmonic Spectrum of the 10 dBm Class E Match

In theory, the 10 dBm Class E design should be the same as the 13 dBm one; only the power level is reduced properly by a lower power level setting. However, during bench tweaking, it is seen that the efficiency at low power levels can be improved further if the C0 value is increased slightly. The conducted output power spectrum of the final 10 dBm circuit (given in Table 12 on page 17) is shown in Figure 36. These results are measured at the TX output power level setting of 0x19 of the Si4060/Si4460/67 RFIC with 16.4 mA total current consumption at 3.2 V supply voltage.

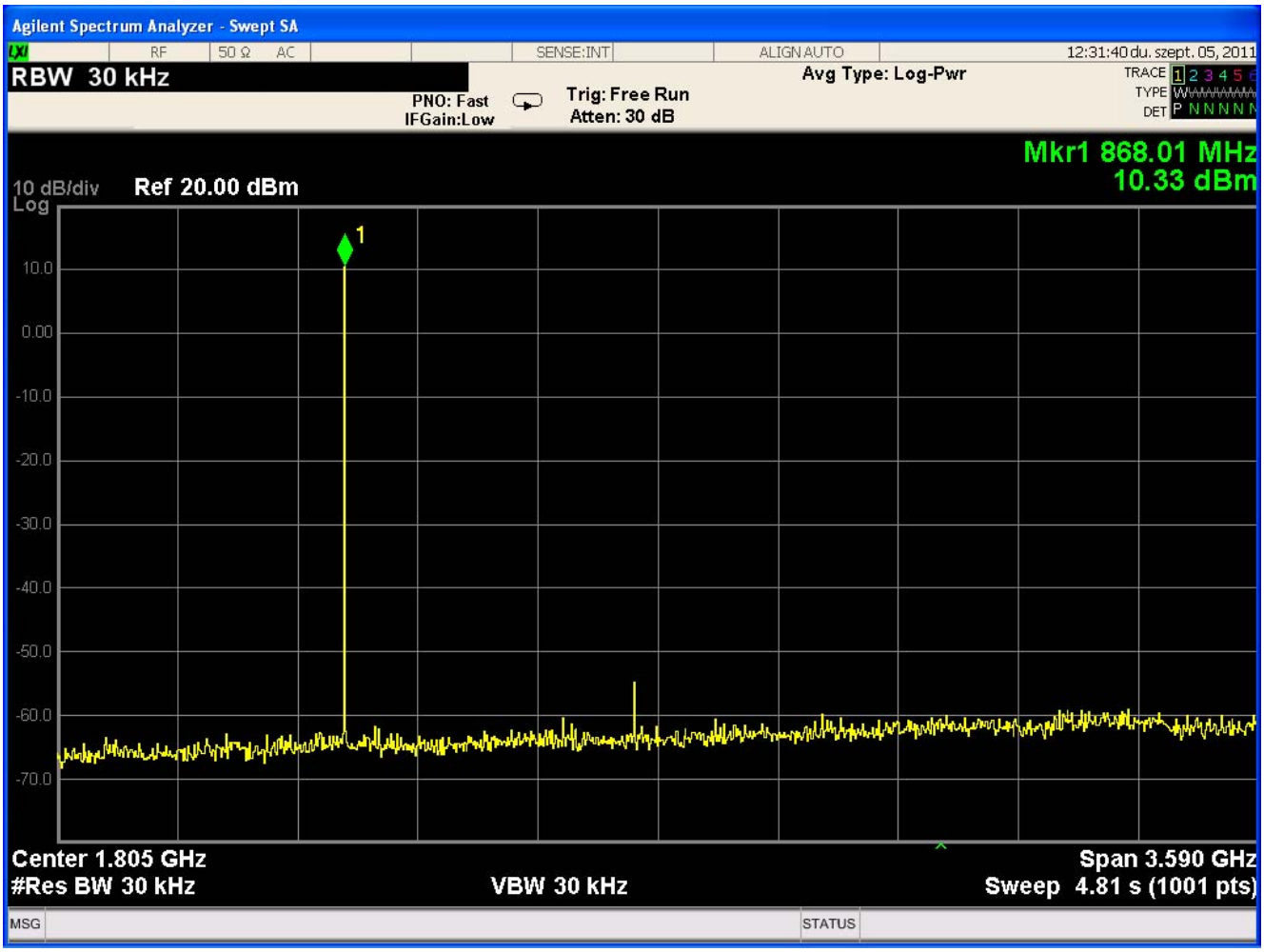

Figure 36. Filtered Harmonic Spectrum at Power State 19h of the Tuned 10 dBm Si4060/Si4460/67 Class E Match (Fo = 868 MHz—See Table 12 on page 17 for Component Values)

5.3.7. Summary of Match

This completes the steps of the match design process for the Split TX/RX board configuration. This match design process may be used to obtain matching component values at any desired operating frequency as well as for the Si4461. A summary table of these matching component values is shown in Tables 7 and 12.

5.4. Detailed Matching Procedure for Direct Tie Board Configuration

In the Direct Tie board configuration, the TX and RX paths are tied directly together without the use of an RF switch, as shown in Figure 37. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the EZRadioPRO 2 family of chips contains a set of switches that aids in isolation of the RX pins in TX mode. This set of switches is implemented internally as shown in Figure 37.

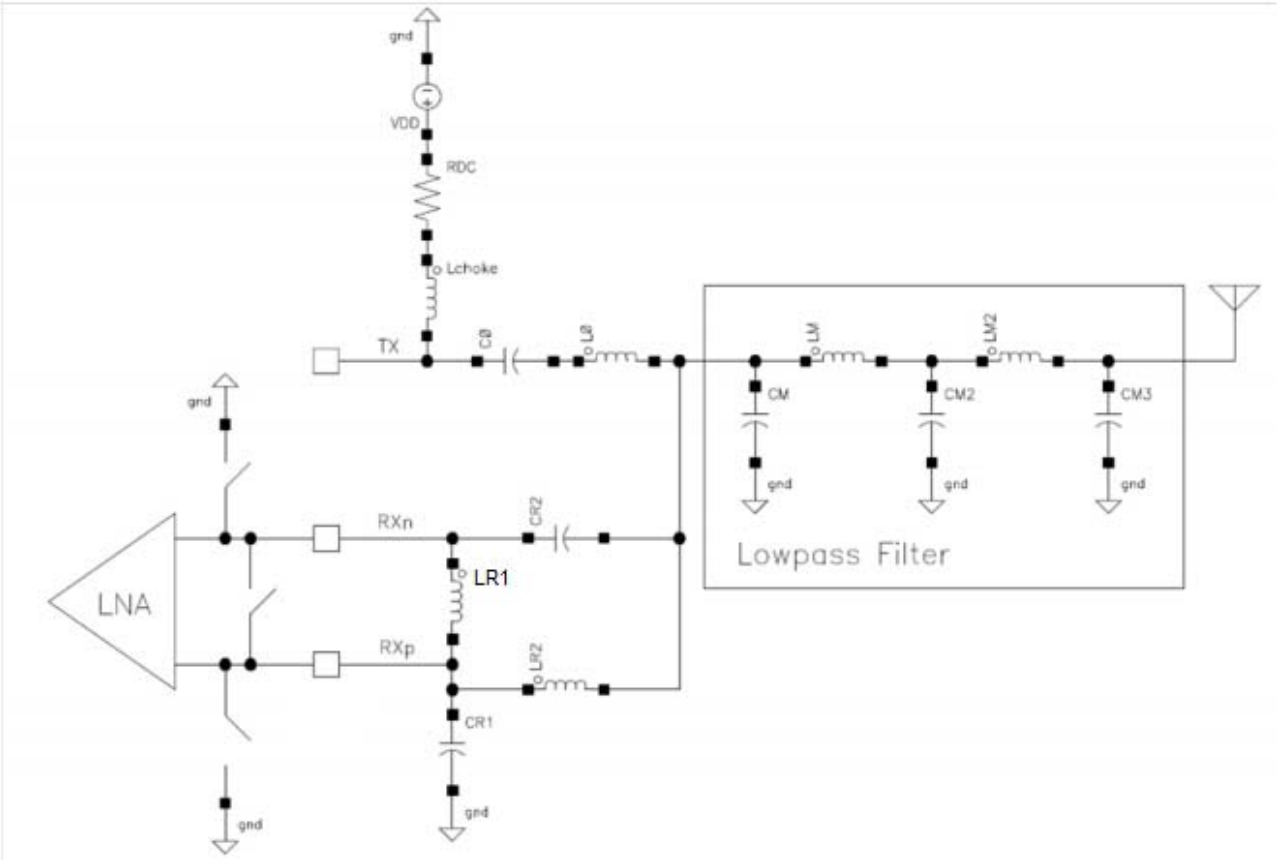

Figure 37. RX Input Switches for Direct Tie Operation

These three switches are activated simultaneously upon entering TX mode. They are opened only in RX mode and closed during all other modes (including TX mode).

Here, the operation in TX mode (when the switchers are closed) is the same as what was described in the case of the SWC DT match (see "3.2.1. Concept of Direct Tie Matching" on page 41); closing these switches during TX mode effectively shorts the RXp and RXn input pins together and shorts them to GND. The effective circuit may be redrawn as shown in Figure 38. Note that inductor LR2 and capacitor CR2 have been placed in parallel by the closure of the switches, and they are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path, resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.

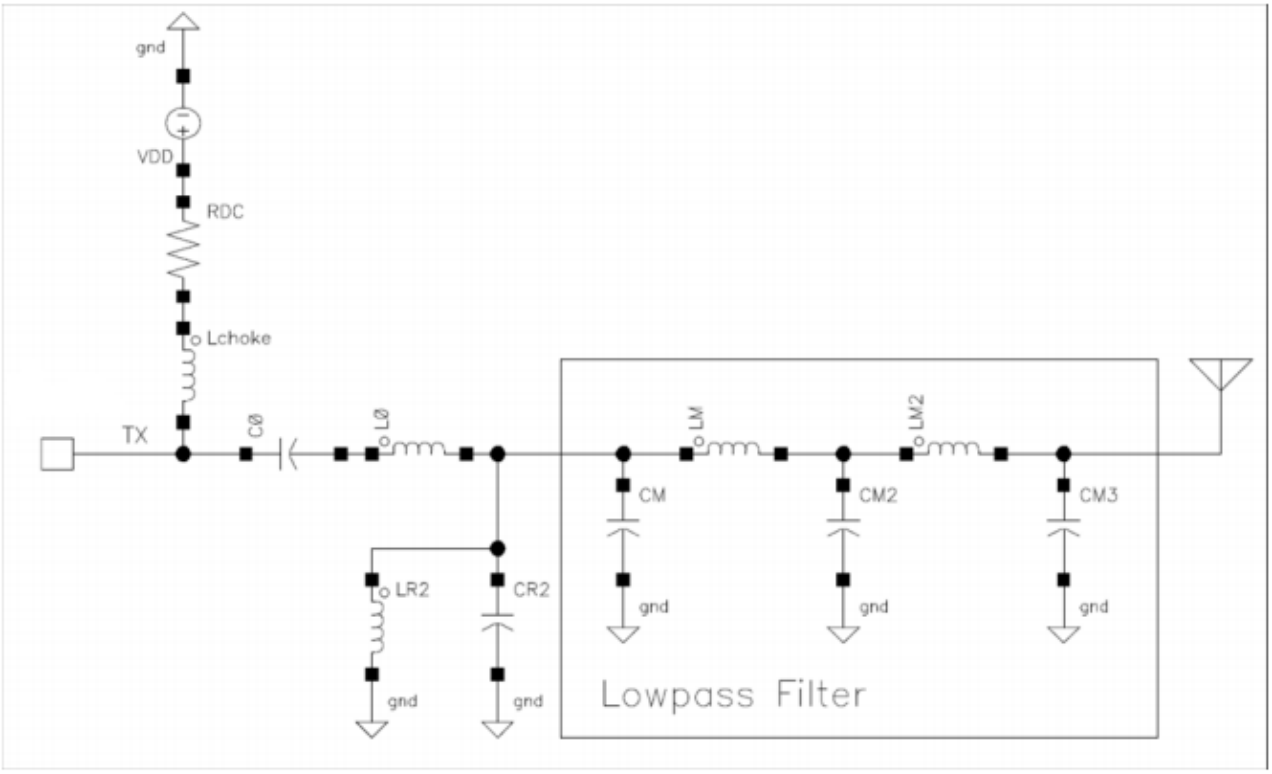

Figure 38. Effective Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state, and the impedance seen looking back into the TX pin is comprised mostly of the output capacitance of the transistors. (The impedance of the pull-up inductor, L_{CHOKE}, is quite high and may be ignored for this discussion.) This OFF stated PA output capacitance value, C_{PAOFF}, is not much different from the ON STATED value. In the case of a Class E match, this PA capacitance is effectively in-series with matching capacitor C0 and results in series-resonance with inductor L0 at some frequency, as shown in Figure 39. At this series-resonant frequency, the input to the LNA matching network (LR2, CR2, LR, CR1) is effectively shorted to GND and thus significantly degrades receive performance. As the PA output capacitance, C_{PAOFF}, is fixed, it is necessary to choose L0 and C0 to ensure that this series-resonance does not excessively degrade RX performance at the desired operating frequency. It may be necessary to alter the values of L0 (variation of C0 is less efficient as it is in-series with the fixed C_{PAOFF}) slightly away from their calculated optimum values in order to accomplish this goal, thus slightly degrading TX performance in an effort to minimize the impact to RX performance.

With the typical C_{PAOFF} values of the Si4460/61/67 RFIC family, this effect is most critical at the upper frequency bands (868 or 915 MHz). At lower frequency bands (169 or 434 MHz) it usually does not cause any problems, and the DT TX match element values are identical to the values of the Split TX/RX configuration.

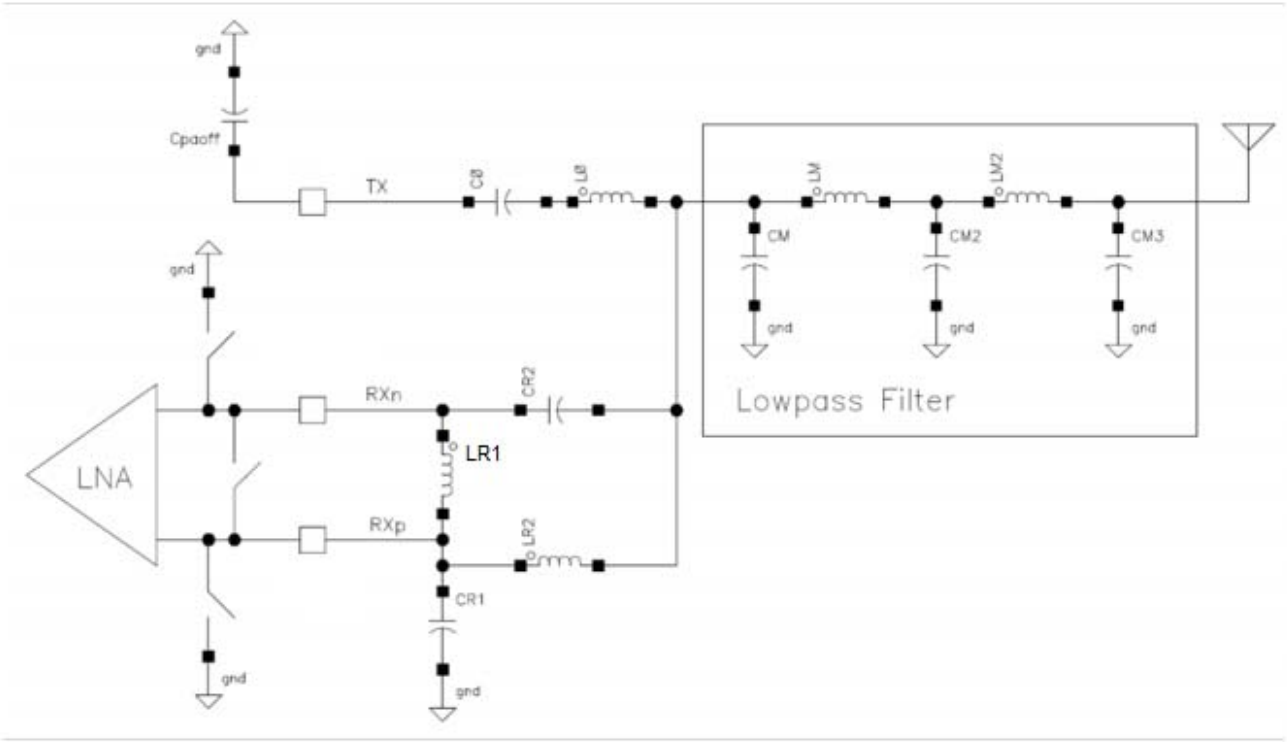

Figure 39. Effective Direct Tie Circuit in RX Mode

We next provide further detail about each step of the matching procedure for the Single Antenna with Direct Tie board configuration. Again, assume a general chip supply voltage of V_{DD_RF} = 3.3 V. Our design example will be constructed for Si4460/67 for the 868 MHz ETSI band, with a targeted output power level of +13 dBm.

5.4.1. Steps #1–6: Same Design Procedure as for Split TX/RX Board Configuration

Steps 1 through 6 are exactly the same as those shown in "5.3. Detailed Matching Procedure for Split TX/RX Board Configuration" on page 58.

5.4.2. Step #7: Design RX Input Match

In Step #7, we design an impedance matching network for the differential RX input. The RX matching network is comprised of a total of four inductors and capacitors (LR2, CR2, LR, CR). The goals for this network are as follows:

- Match the LNA input to a 50 Ω source impedance (i.e., the antenna)
- Provide a single-ended to differential conversion function (i.e., a balun)
- Ensure that LR2,CR2 are parallel-resonant at the desired operating frequency

The design equations (and their mathematical derivation) for selection of the matching component values are discussed in detail in “AN643: Si446x/Si4362 RX LNA Matching”. This procedure is also the same one described in "3.2.4. Construction of RX Match" on page 45. The following equations are introduced here without proof or further discussion; refer to AN643 for further details.

$$L_{R2} = \frac{\sqrt{50\ \Omega \times R_{LNA}}}{\omega_{RF}}$$

Equation 30.

$$C_{R2} = \frac{1}{\omega_{RF}^{2} \times L_{R2}}$$

Equation 31.

$$C_{R1} = 2 \times C_{R2}$$

Equation 32.

$$L_{LNA} = \frac{1}{\omega_{RF}^{2} \times C_{LNA}}$$

Equation 33.

$$L_{M} = 2 \times L_{R2}$$

Equation 34.

$$L_{R1} = \frac{L_{LNA} \times L_{M}}{L_{LNA} + L_{M}}$$

Equation 35.

Note that our goal of parallel-resonance between LR2 and CR2 is inherently satisfied, as evidenced by Equation 31.

At any given frequency, the differential input impedance at the RX pins of the chip may be represented by an equivalent parallel R-C circuit; their values are represented by the parameters R_{LNA} and C_{LNA} in the above equations. It is necessary to know these equivalent circuit values at the desired frequency of operation, prior to constructing the match.

The differential input impedance of the RX port on the Si446x RFIC is provided in AN643. The values of R_{LNA} and C_{LNA} at a desired operating frequency of 868 MHz are found to be R_{LNA} = 380 Ω and C_{LNA} = 1.09 pF. After plugging these values into the above equations, the following ideal matching component values are calculated:

- LR2 = 25.27 nH
- CR2 = 1.33 pF
- LR1 = 19.15 nH
- CR1 = 2.66 pF

In practice, it is often necessary to slightly modify the matching component values suggested by the above equations. Any printed circuit board layout has parasitics, such as trace inductances or component pad capacitances, and these may have an effect upon the circuit. Silicon Labs has empirically determined that if 0402-size wire-wound or multilayer inductors are used on the Direct Tie reference board designs (available at www.silabs.com), the actual component values are as shown in the 868 MHz rows in Table 14 on page 19 for the wire-wound case and reproduced below:

- LR2 = 24 nH
- CR2 = 1 pF
- LR1 = 20 nH
- CR1 = 3 pF

The above inductor element values are not available in multilayer type; so, new bench-optimized multilayer RX match elements are necessary and are given in Table 15 on page 19.

Although not required, it is useful to measure the input impedance seen looking into the RX match in both RX mode as well as TX mode. Obviously, it is desired to verify a good match to 50 Ω while in RX mode in order to obtain optimum sensitivity. However, it is also useful to verify that the network provides a high impedance while in TX mode (when the switches at the input of the LNA (see Figure 38) are in their CLOSED position, and thus LR2 and CR2 form a high-impedance parallel-resonant network, which isolates the RX path from the TX path); otherwise, the RX circuitry may excessively load down the TX path. Specifically, it may be necessary to slightly adjust the values of LR2 and/or CR2 to achieve optimum parallel resonance at the desired frequency of operation.

The isolation in TX mode is more critical with multilayer inductors since this type has lower Q (higher loss), and the values are available in rarer steps. So both to achieve high impedance at LR2-CR2 parallel resonance and also to tune the resonance exactly to the frequency of operation is more difficult.

The actual measured impedance of the 868M multilayer RX match while in TX mode is shown in Figure 40 and confirms the expectations of “good enough” isolation; the measured impedance at 868 MHz is ~452 Ω + j593Ω, which corresponds to a parallel R-C equivalent of 1.2 kΩ – 0.196 pF. This slight parallel capacitance (~196 fF) may be ignored.

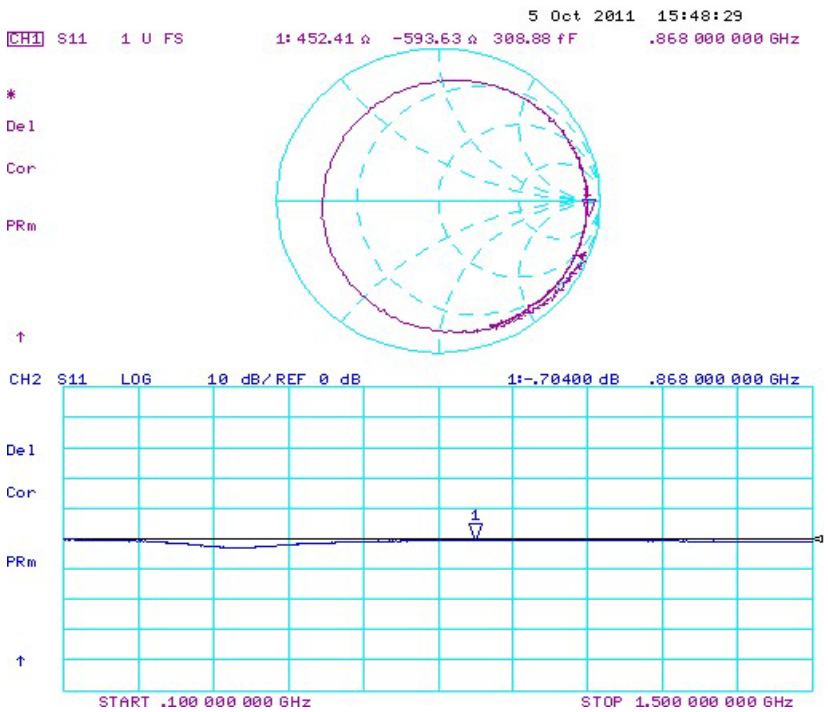

Figure 40. RX Match Input Impedance in TX Mode, Multilayer 868M Type

The measured impedance at the input of the multilayer RX matching network while in RX mode is shown in

Figure 41. It is observed that the input impedance is quite close to 50 Ω, with the network providing S_{11} with better than 15 dB return loss.

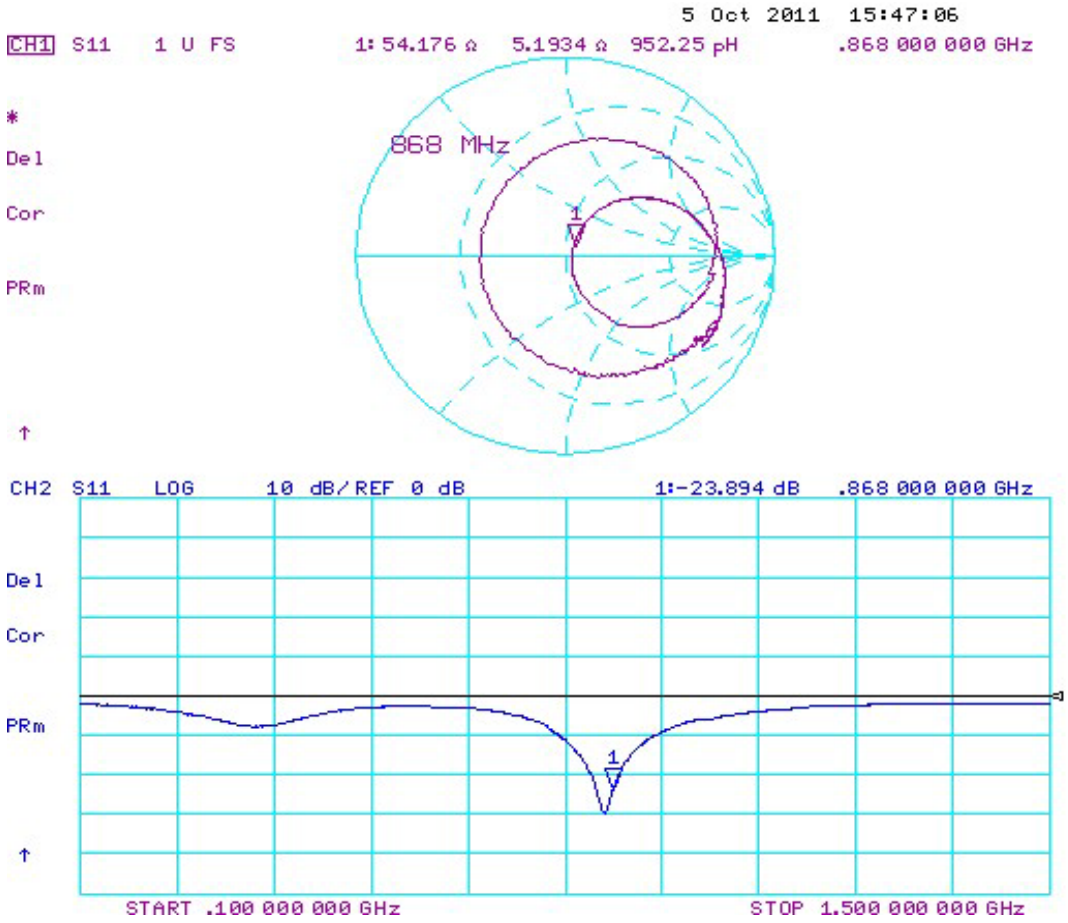

Figure 41. RX Match Input Impedance in RX Mode, Multilayer 868M Type

5.4.3. Step #8: Slightly Modify the Value of L0

In Step #8, we deliberately mistune the value of matching inductor L0 slightly away from its optimum value, as determined in Steps 1 through 6. As illustrated in Figure 39 on page 79, the series-resonance of L0-C0-C_{PAOFF} has the potential to significantly degrade the RX performance by placing a (near) short to GND at the input of the RX matching network. It is important that this series-resonant frequency be adjusted to fall sufficiently far away from the desired operating frequency in order to minimize its effect upon RX sensitivity.

This is accomplished by deliberately increasing or decreasing the value of L0. Here, the variation of C0 is not efficient as it is in series with the fixed C_{PAOFF}; thus, higher deviation from the optimum class-E value would be necessary to achieve the same detuning.

In the 868/915 MHz band and in RX mode, the Si4461 usually needs to have L0 increased (compared to the split TX/RX case) in order to shift away the L0-C0-CPAOFF parasitic resonance while, for the Si4460/67, the L0 usually needs to be decreased in order to shift away the L0-C0-CPAOFF parasitic resonance.

This will push the unwanted resonance lower or higher in frequency and minimize its effect upon RX performance. A typical aim is to suffer less than 2 dB sensitivity degradation at direct tie mode compared to the split TX/RX case.

Some post-tuning of capacitor CM may also be required to improve Class-E operation in TX mode after the change in value of L0.

The value of PA output capacitance in its OFF state may be slightly different than the value of shunt drain capacitance C_{SHUNT} (discussed in "5.3.3. Step #3: Calculate the Required Value for ZLOAD" on page 59). The value of C_{PAOFF} may be measured with a network analyzer connected to the TX output pin with all matching components removed, except for those providing dc bias (i.e., L_{CHOKE} and R_{DC}). Silicon Labs has performed this measurement and determined the value of C_{PAOFF} to be ~1.5 pF in the frequency range of 868 MHz to 950 MHz and 1.4 pF at low bands (315/434M). This is shown by the impedance measurement of Figure 42. The value of L_{CHOKE} must be chosen appropriately to provide a very high impedance at the frequency of interest; otherwise, the measured value of C_{PAOFF} may be affected.

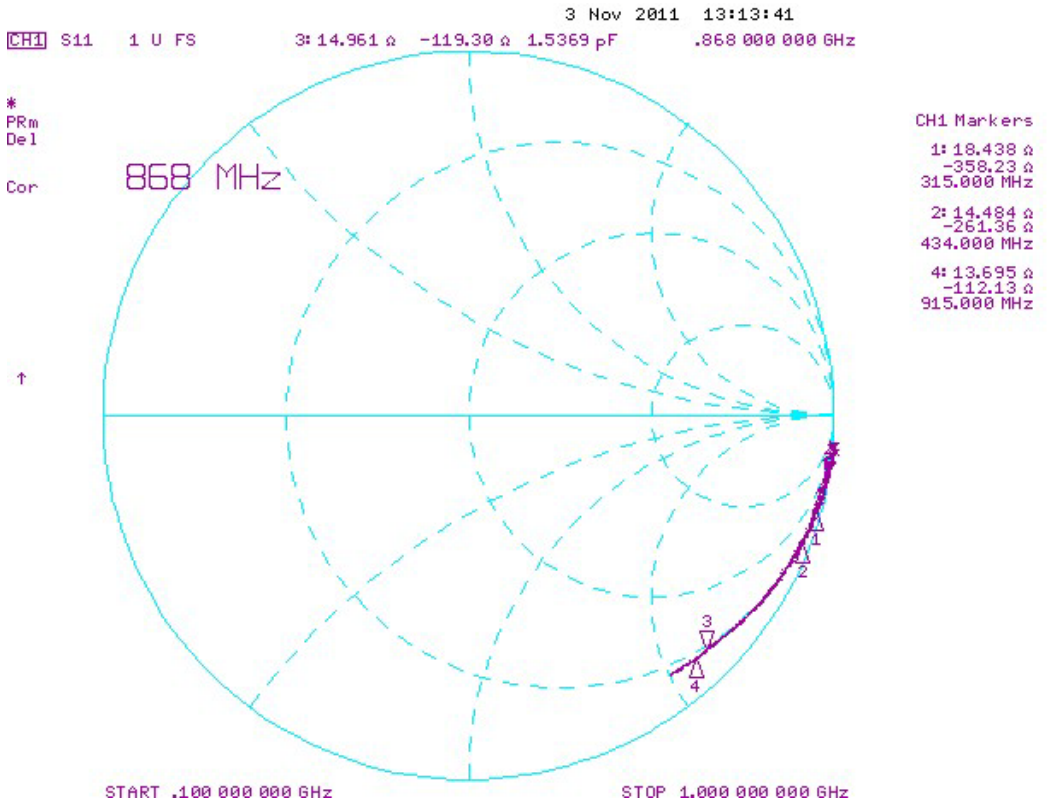

Figure 42. PA Output Capacitance Measurement of Si4460/67 in OFF State

Once the value of C_{PAOFF} has been determined, its effect upon RX performance may be estimated. Continuing with our design example at 868 MHz with the 13 dBm wire-wound split TX/RX board design, we find initial values of L0-C0 to be:

- L0 = 19 nH
- C0 = 3.6 pF

This value of capacitance of C0 is in series with C_{PAOFF} = 1.5 pF, resulting in an equivalent series capacitance of C_{EQUIV} = 1.06 pF. The series-resonant behavior of the resulting L-C circuit may be simulated and is shown in Figure 43; here, the S21 of the TX path is simulated from the filter outputs to the DT point with the L0-C0-C_{PAOFF} part. It can be observed that this L0-C0-C_{PAOFF} circuit introduces only ~0.8 dB of loss at 868 MHz, which is mostly the filter attenuation. Since this circuit is directly connected to the input of the RX match, this will result in approximately 0.8 dB of degradation in RX sensitivity, which is acceptable. It is also clear from the curve that the critical shunt of the RX path occurs far above 1 GHz.

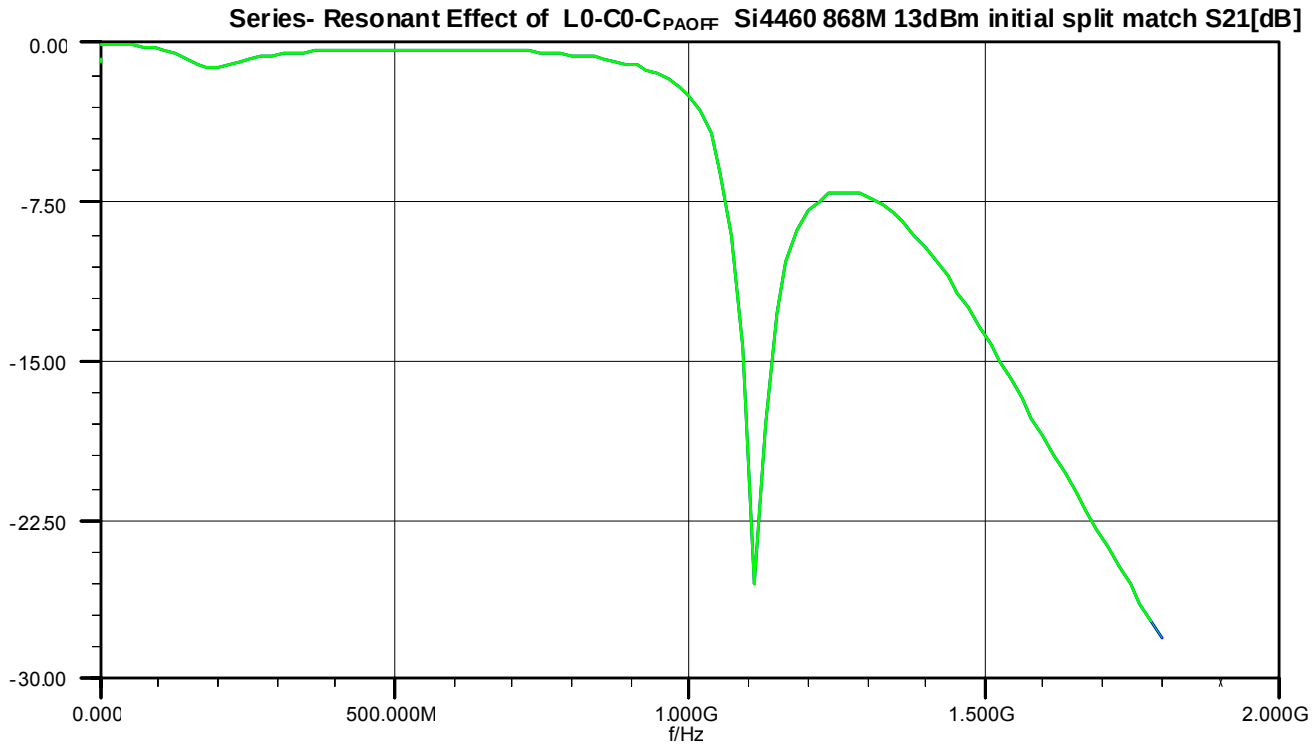

Figure 43. Series-Resonance Behavior of Initial L0-C0 Circuit of Si4460/67 13 dBm Split Class E Match

Unfortunately, the situation is more critical in case of the Si4460/67 10 dBm direct tie. There, the initial split C0 value is much higher (see Table 12 on page 17) in order to achieve better efficiency at reduced power levels. With the initial values of:

- L0 = 19 nH
- C0 = 15 pF

The parasitic L0-C0 – C_{PAOFF} series resonance curve is shown in Figure 44. As can be observed, due to the higher C0, the resultant C_{EQUIV} capacitance is 1.36 pF, and, thus, the resonance is at lower frequencies closer to the useful band. It results in an attenuation of ~2.5 dB according to the simulations. In real bench circumstances, the degradation in RX mode was even higher, approx 3.5 dB, which is unacceptable.

The resonant frequency of these circuit components may be shifted further upwards (away from the desired operating frequency) by decreasing the value of L0. Using our rule-of-thumb of decreasing L0 by ~20%, we arrive

at a modified value of L0 = 15 nH. In theory, with the 20% L0 variation, the class E operation in TX mode is still satisfactory, and, usually, the sensitivity degradation in RX mode will improve to be less than ~2 dB. However, in the case of the +10 dBm 868 MHz Si4460/67 DT match, the bench test of this modified circuit still did not show sufficiently good sensitivity in RX mode.

So, the L0 was decreased further to 12 nH with a parallel increase of C0 to keep the optimum class E TX operation. Simulation of the series-resonant behavior of the modified circuit is shown in Figure 45.

It is seen that the loss at 868 MHz has now been improved significantly to only ~0.9 dB in the simulations. In the bench test, the suffered RX sensitivity degradation is only ~1.1 dB, very close to the simulated value. While this still represents a 1.2 dB reduction in RX sensitivity, this is a good compromise between TX and RX performance.

Although this (12 nH and 27 pF pls. see Table 14 on page 19) set of L0-C0 values is proper for 868M 10 dBm operation, it is not good at 915M. Since dual band CLE TX operation seems to be feasible with minimum compromise, it makes sense to create a dual band DT circuit as well.

To have good Rx sensitivity at 915M the L0-C0-CPAOFF resonance has to be shifted up further. So, the new proposed L0 value is 6.8 nH and the new C0 values is 36 pF (Table 14) to have both moderate Rx sensitivity degradation at 915M and to maintain the acceptable TX class E operation at 868M and 915M.

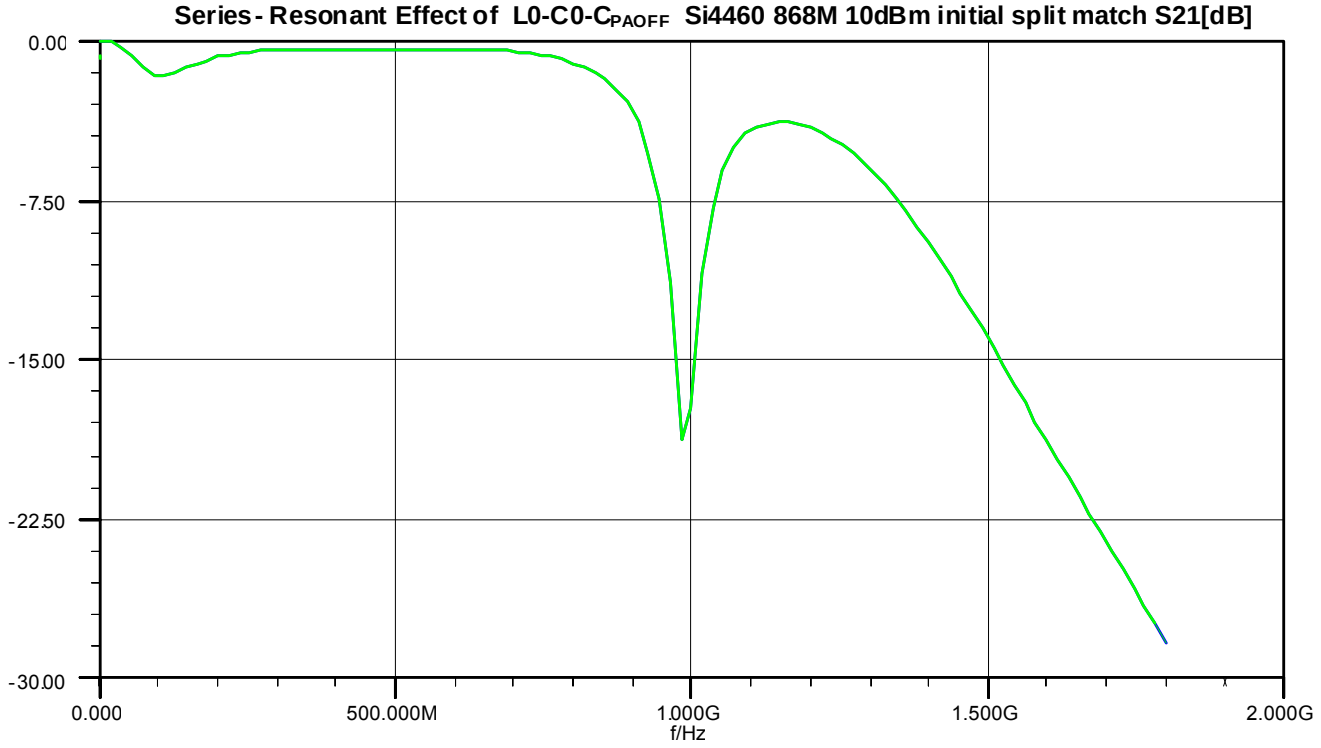

Figure 44. Series-Resonance Behavior of the Off-Stated Si4460/67 PA with the Initial 10 dBm 868M Split Class E L0-C0 Circuit (19 nH–15 pF)

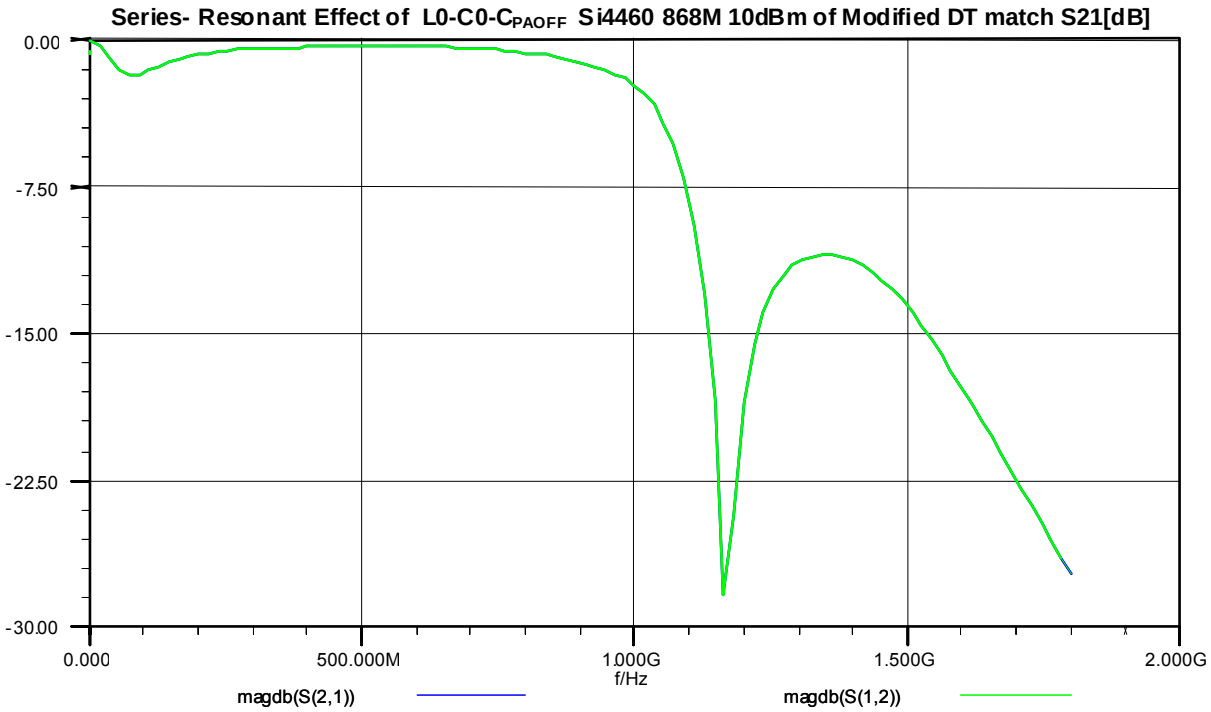

Figure 45. Series-Resonance Behavior of the Off-Stated Si4460/67 PA with the modified 868M 10 dBm Split Class E L0-C0 Circuit (12 nH–27 pF)

It is also possible to increase the resonant frequency of the L0-C0-C_{PAOFF} circuit by decreasing the value of C0 instead of L0. Here, it important to note that the increase of the C0 capacitor will have a reduced effect on the parasitic series-resonant frequency since the value of C_{PAOFF} is significantly lower than that of C0, and, thus, C_{PAOFF} determines primarily the resonance. Hence, a much larger increase of C0 is required to achieve the same resonance shift. This stronger mistuning will result in even greater reduction in performance in TX mode. Therefore, tuning of L0 is preferred and generally results in a better compromise between TX and RX performance.

This increase in the value of L0 is usually required only when working in the upper frequency bands, such as 868/915/950 MHz. In the lower frequency bands (315/390/434 MHz), the values of L0 and C0 obtained for the Split TX/RX board configuration usually continue to work well with the Direct Tie board configuration.

In the final circuit realization on Silicon Labs reference design boards, the value of capacitor CM was reduced to 1.5 pF to provide slightly better TX output power. The final Si4460/67 element values with wire-wound inductors are summarized in Table 14 on page 19. For Multilayer inductors, the same is given in Table 15 on page 19.

For the Si4461, the DT board element values are summarized in Tables 9, 10, and 12, both for wire-wound and multilayer inductor types.

Note that some small degradation in both TX and RX performance is expected for a Direct Tie configuration. That is, it is not possible to directly connect the TX and RX paths and achieve perfect isolation between the two circuit functions; each path will result in some amount of unwanted loading to the other path, and, thus, some there will be slight degradation in performance (relative to a Split TX/RX board configuration in which the TX and RX paths remain entirely separate). The choice of matching inductor L0 heavily impacts the trade-off between optimizing for TX output power at the expense of degraded RX sensitivity, or vice-versa. A value may generally be found that achieves a good compromise between the two, typically resulting in less than 1 dB reduction in TX output power and no more than 2–3 dB reduction in RX sensitivity. Some amount of “tweaking” of the final values of L0 and CM may be necessary to achieve the best compromise.

5.4.4. Summary of Match

This completes the steps of the match design process for the Direct Tie board configuration. This match design process may be used to obtain matching component values at any desired operating frequency.

APPENDIX A—MEASURED SPECTRUM PLOTS

The following section presents some measured spectral data plots on different CLE board configurations in TX mode at a variety of frequencies given in "2. Summary of Matching Network Component Values" on page 6. Measured results for circuit realizations with both wire-wound inductors and multi-layer inductors are presented.

Si4461 Measured Plots

Si4461 Split TX/RX Board CLE Configurations with Wire-Wound Inductors

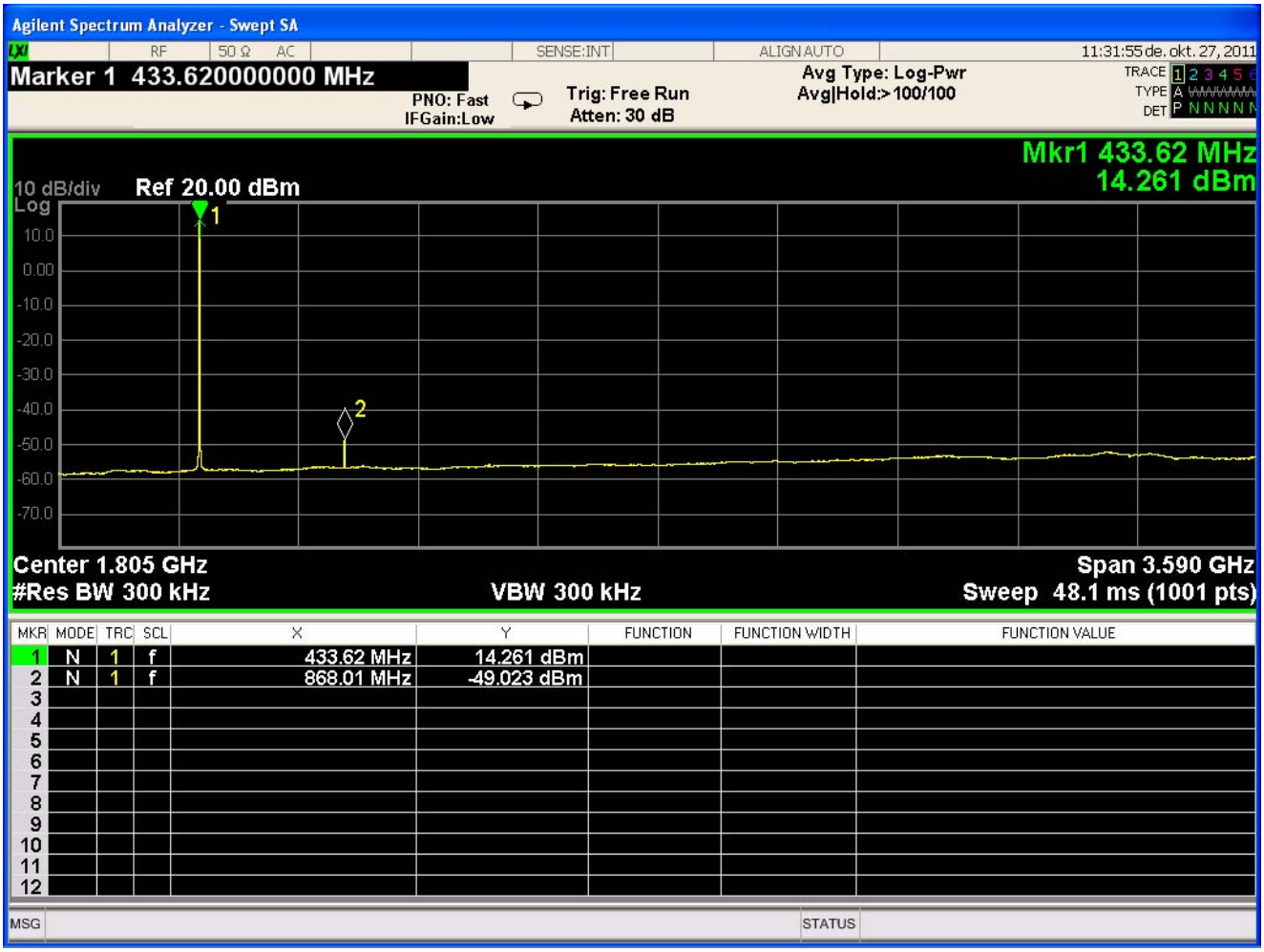

Figure 46. Si4461 14 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 28.1 mA

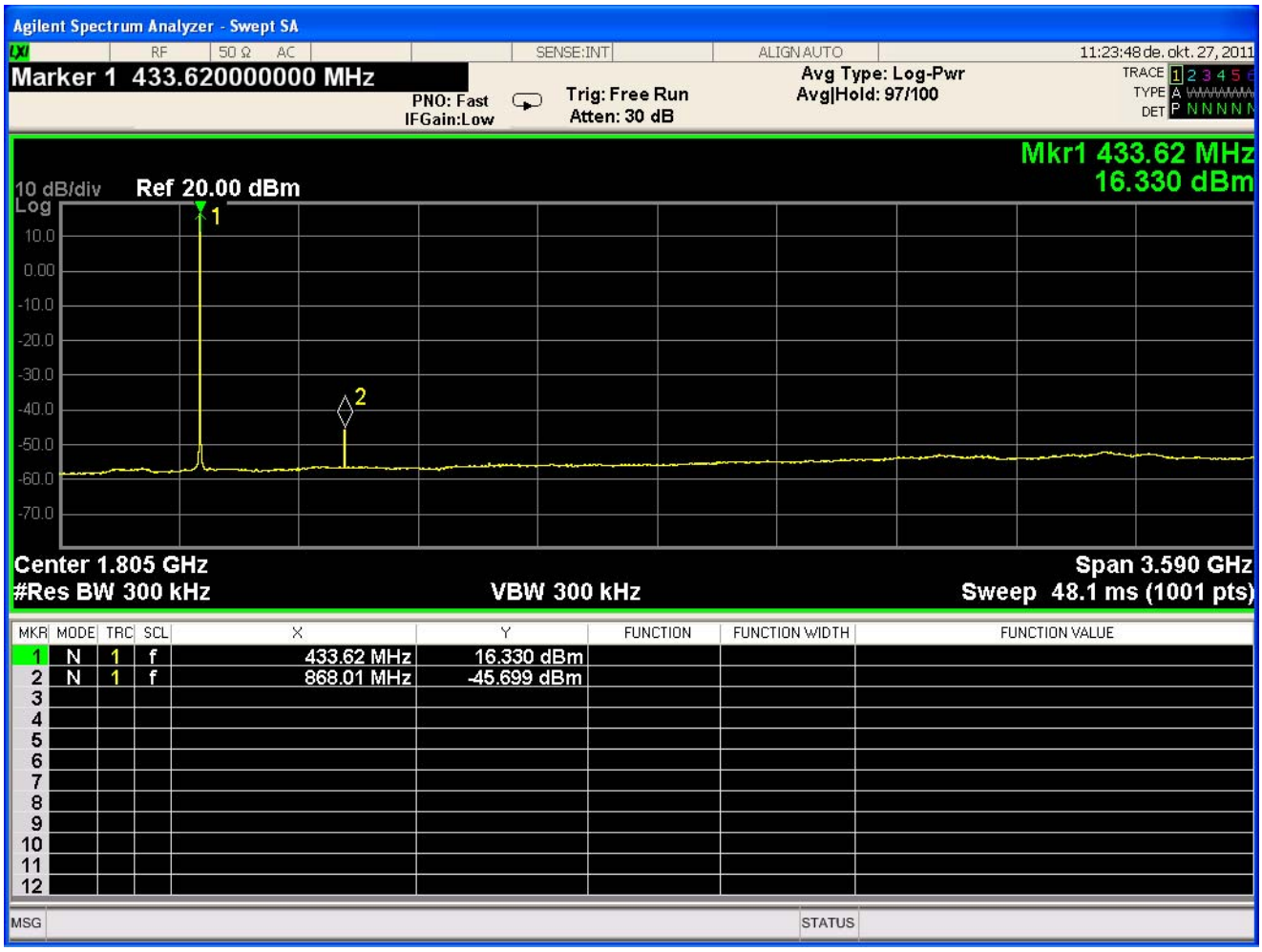

Figure 47. Si4461 16 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x32, 35.8 mA

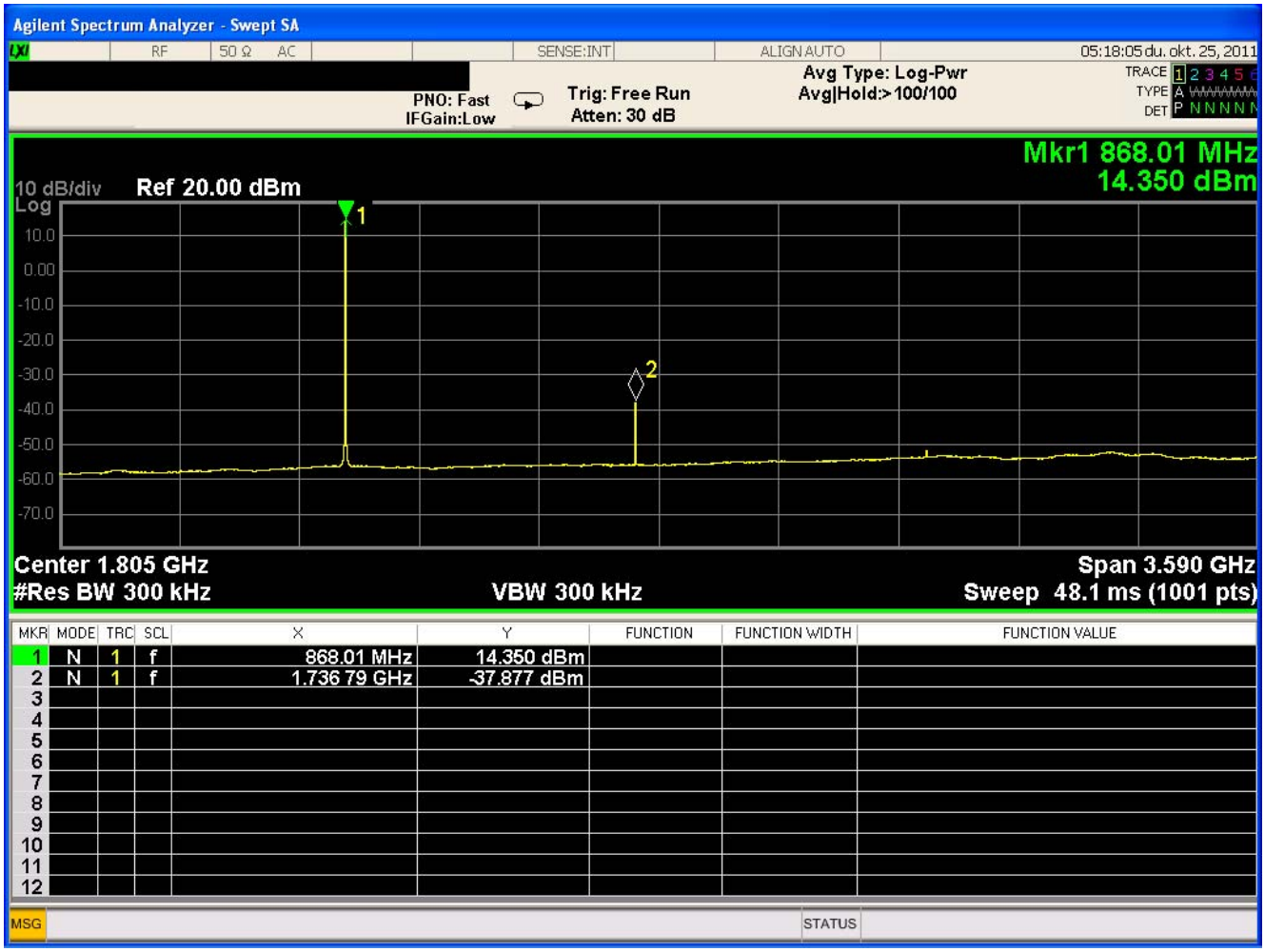

Figure 48. Si4461 14 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x2B, 31.6 mA

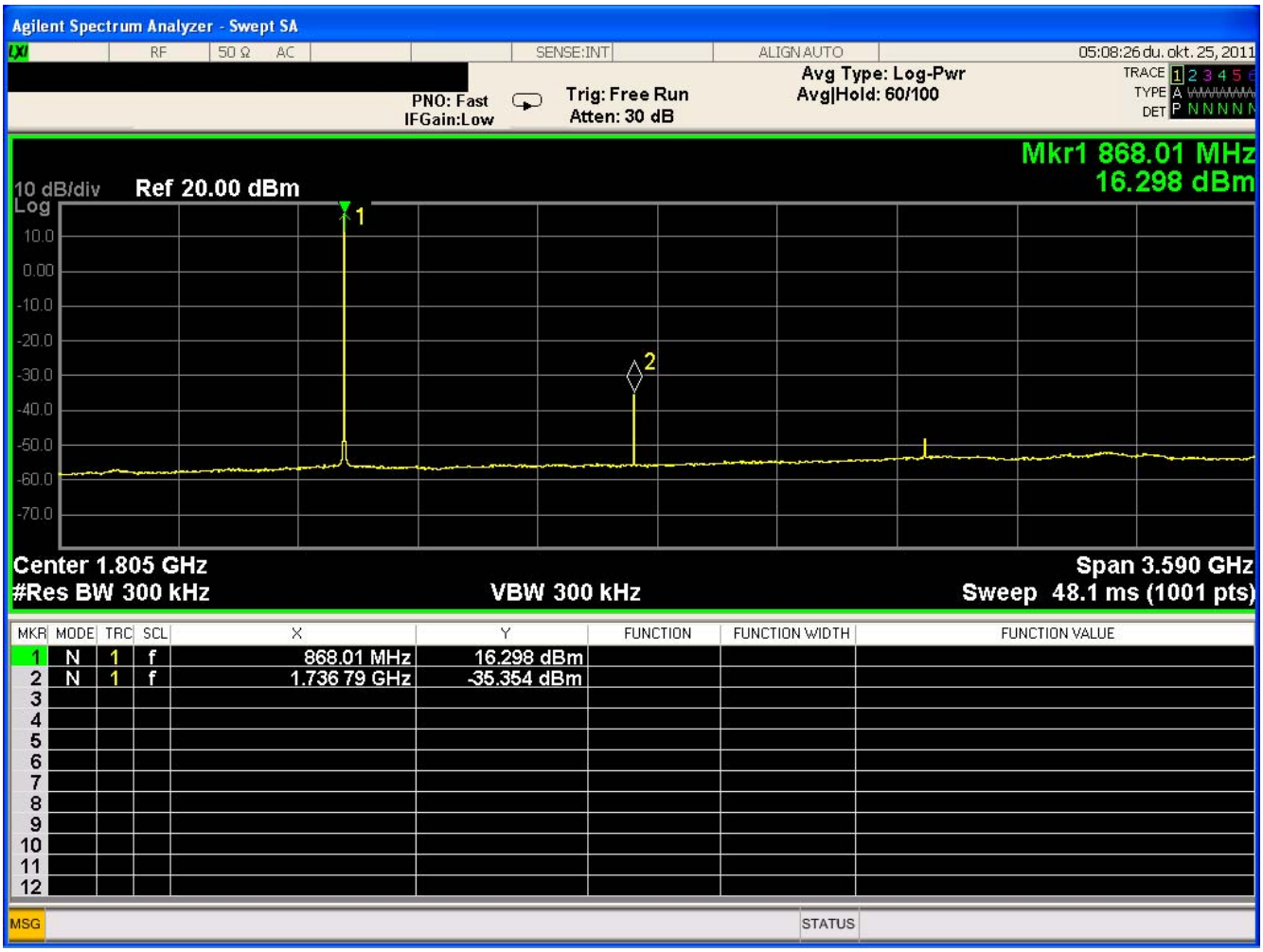

Figure 49. Si4461 16 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x40, 38.9 mA

Si4461 Split TX/RX Board CLE Configurations with Multilayer Inductors

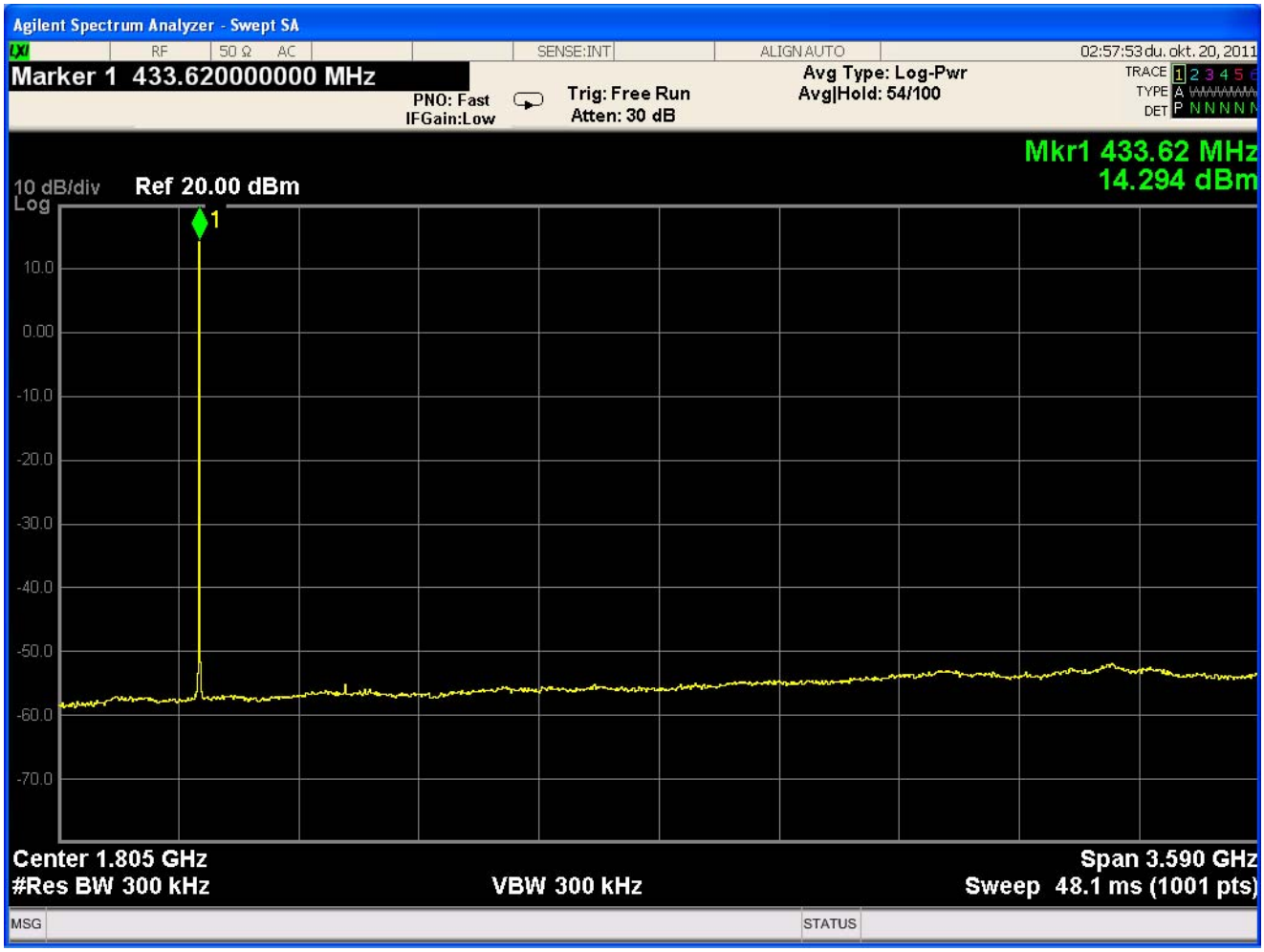

Figure 50. Si4461 14 dBm Split TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x2D, 29.7 mA

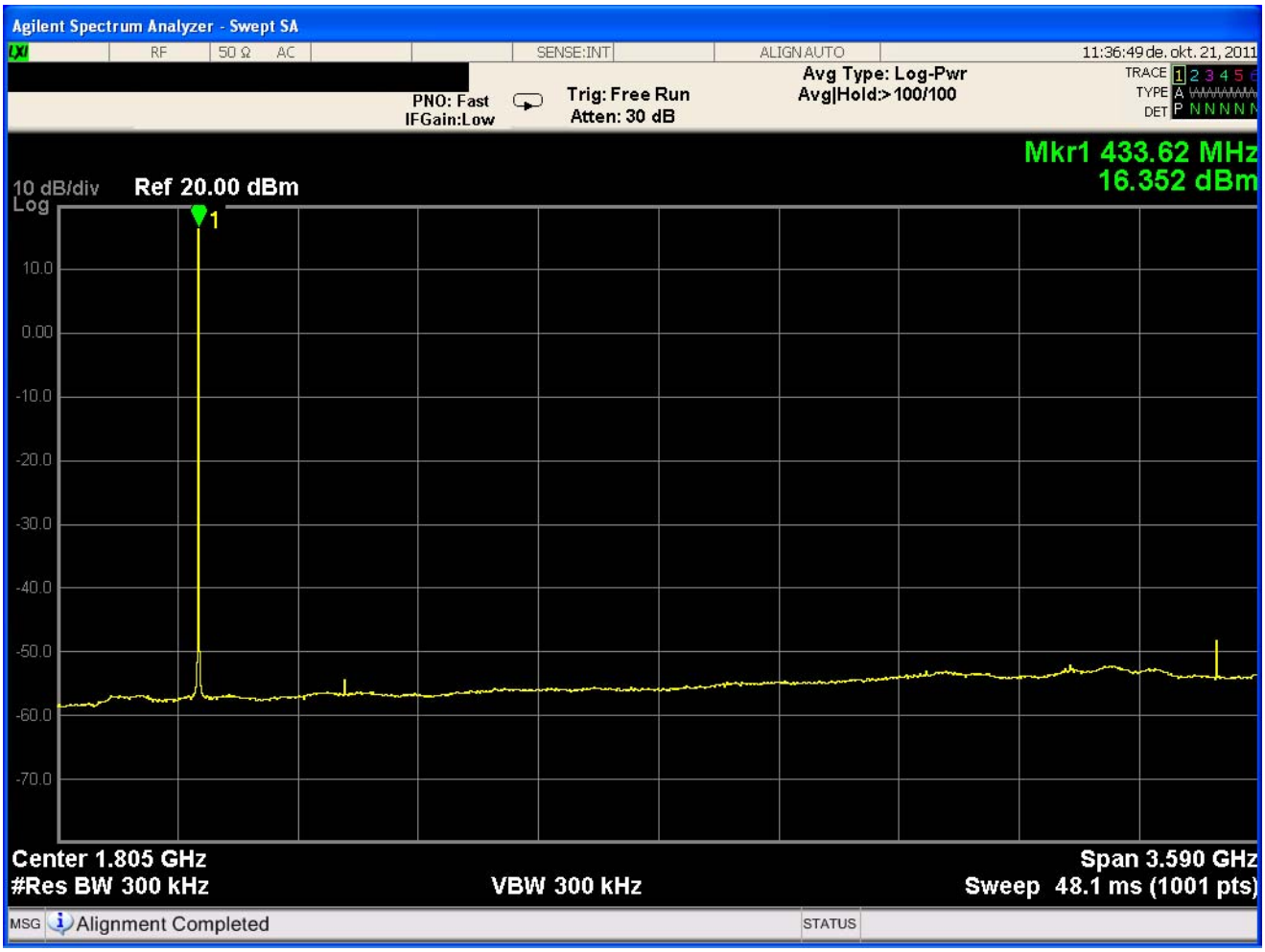

Figure 51. Si4461 16 dBm Split TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x7Fh, 38.9 mA

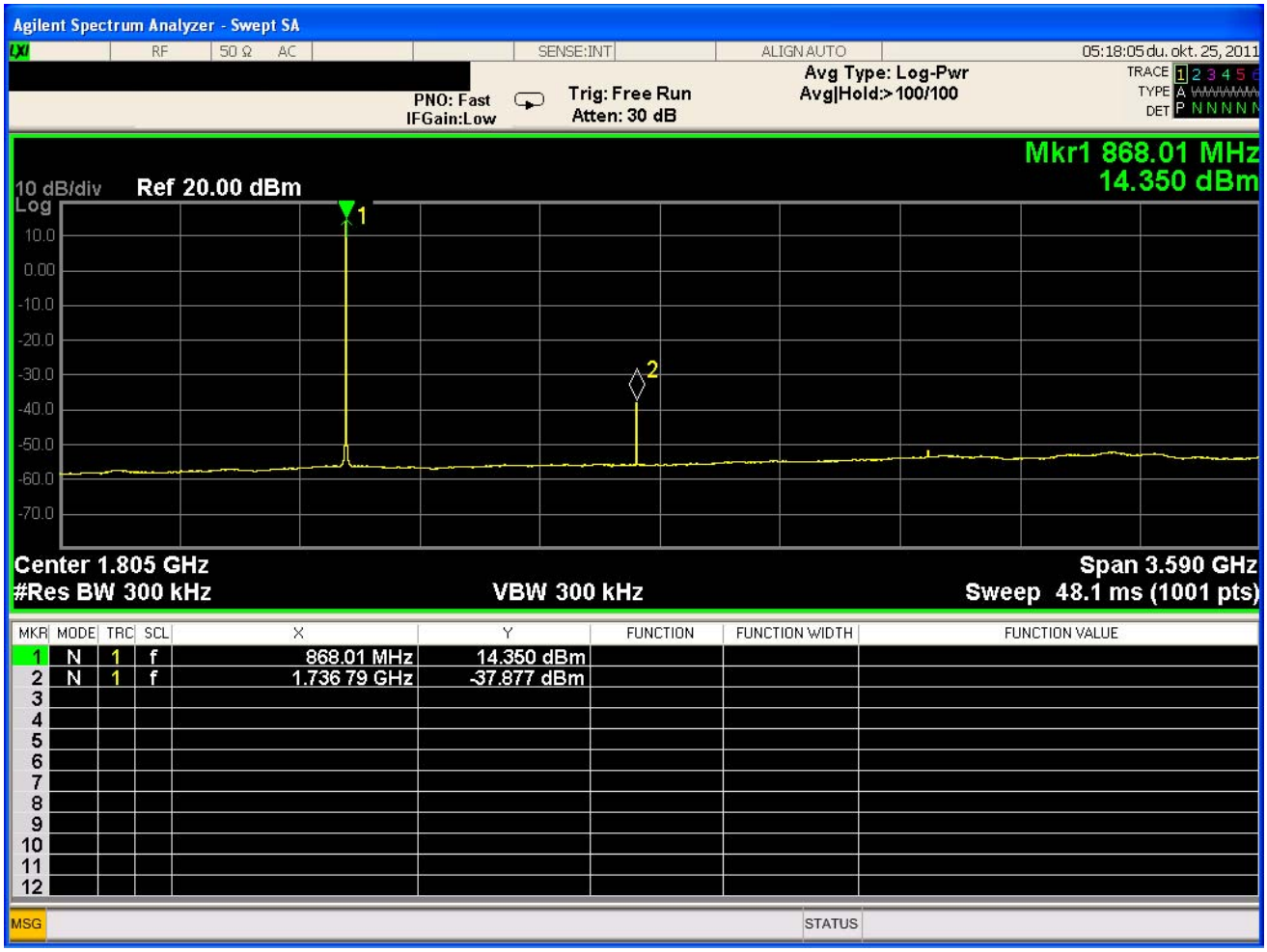

Figure 52. Si4461 14 dBm Split TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL Register is 0x34, 34.4 mA

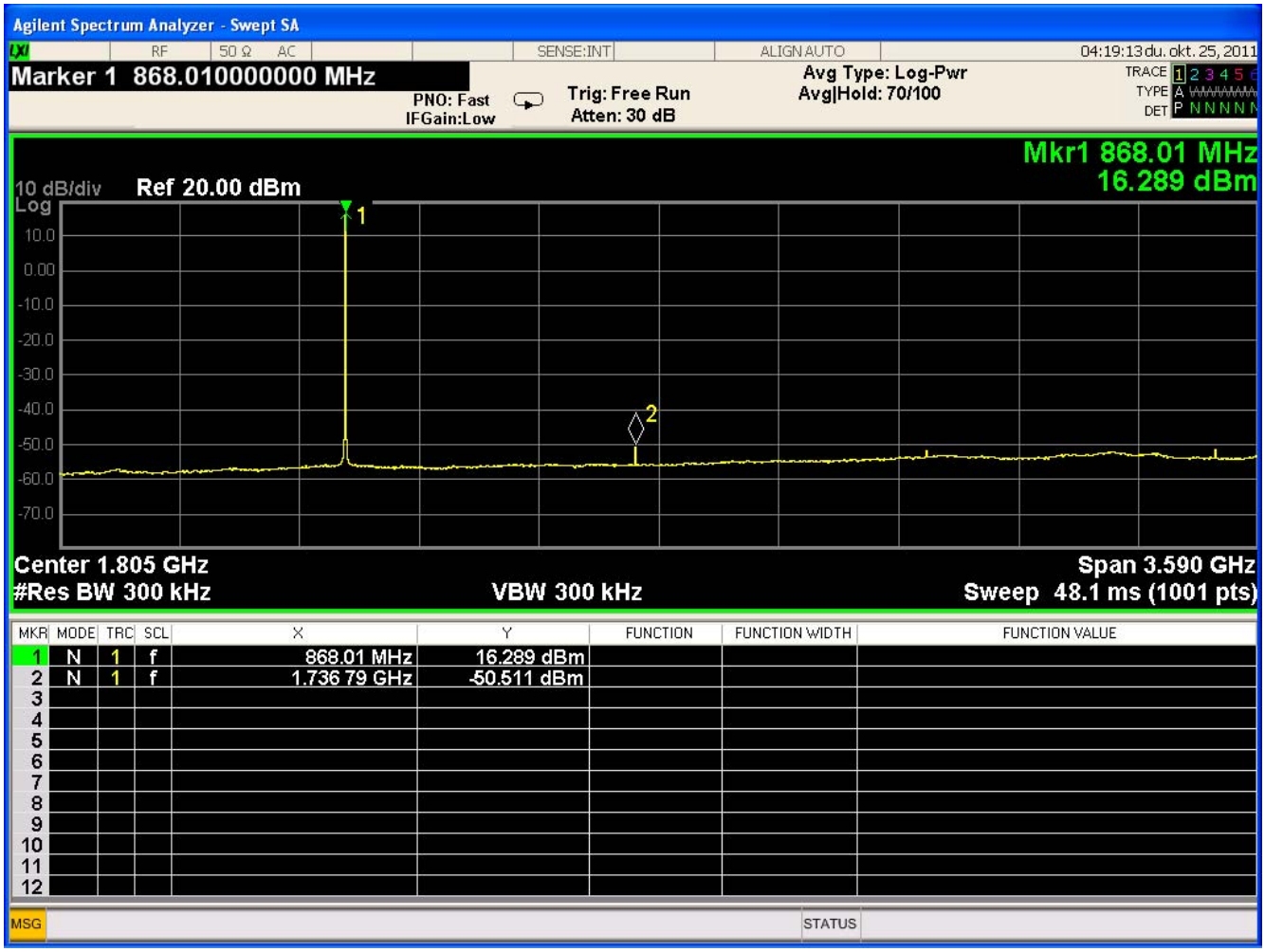

Figure 53. Si4461 16 dBm Split TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 42.7 mA

Si4461 Direct Tie TX/RX Board CLE Configurations with Wire-Wound Inductors

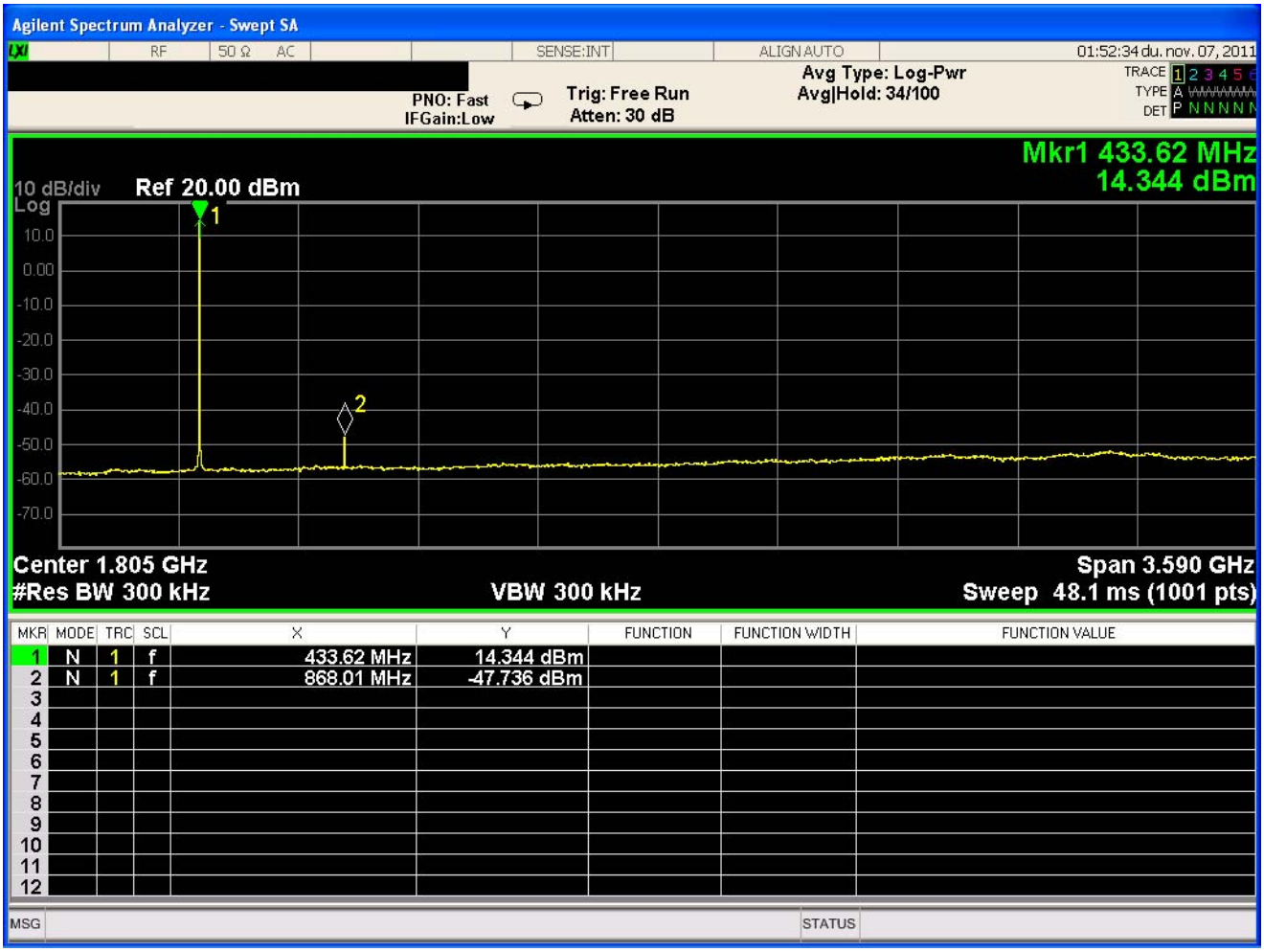

Figure 54. Si4461 14 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x21, 28.7 mA

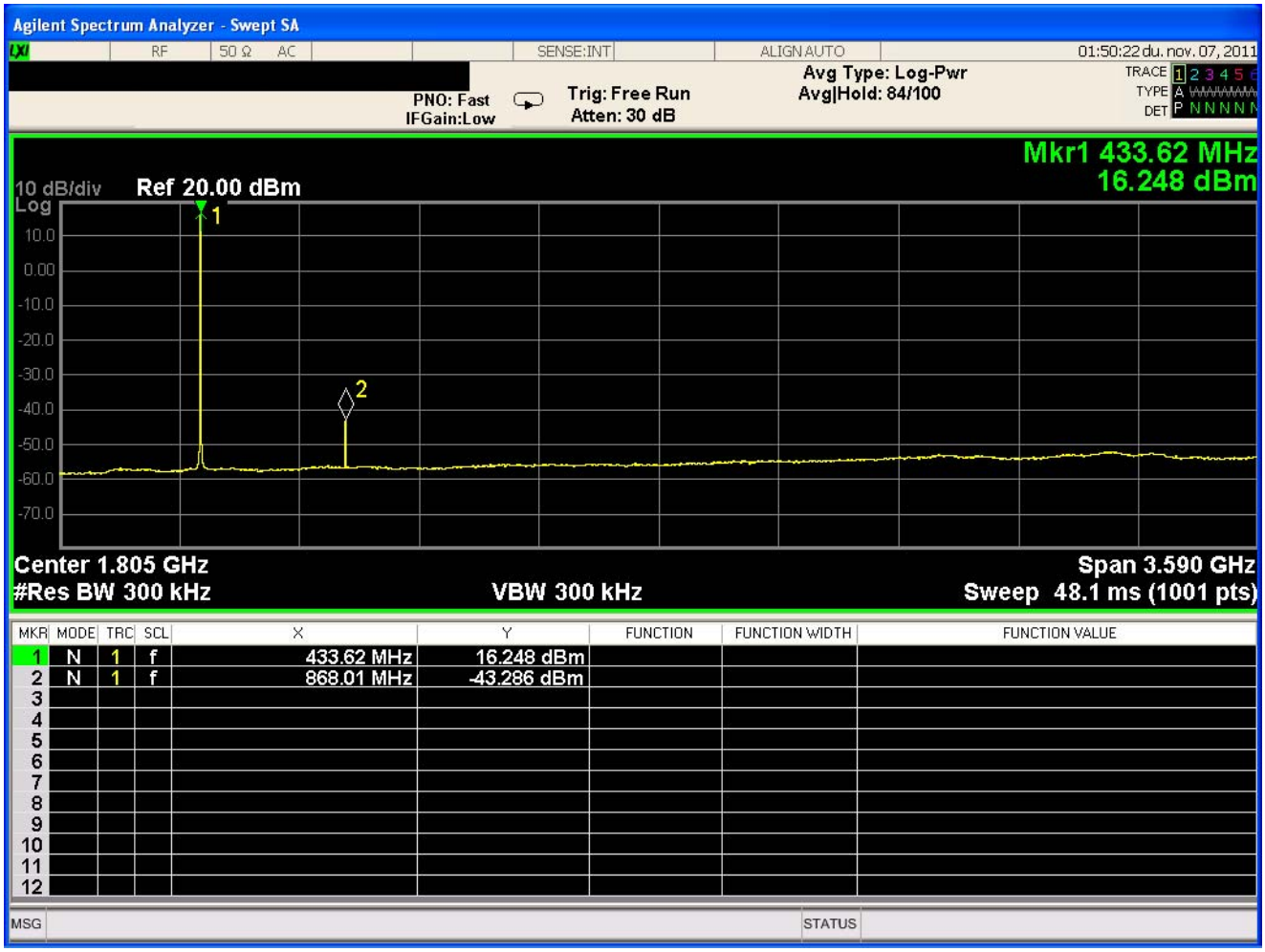

Figure 55. Si4461 16 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x31, 33 mA

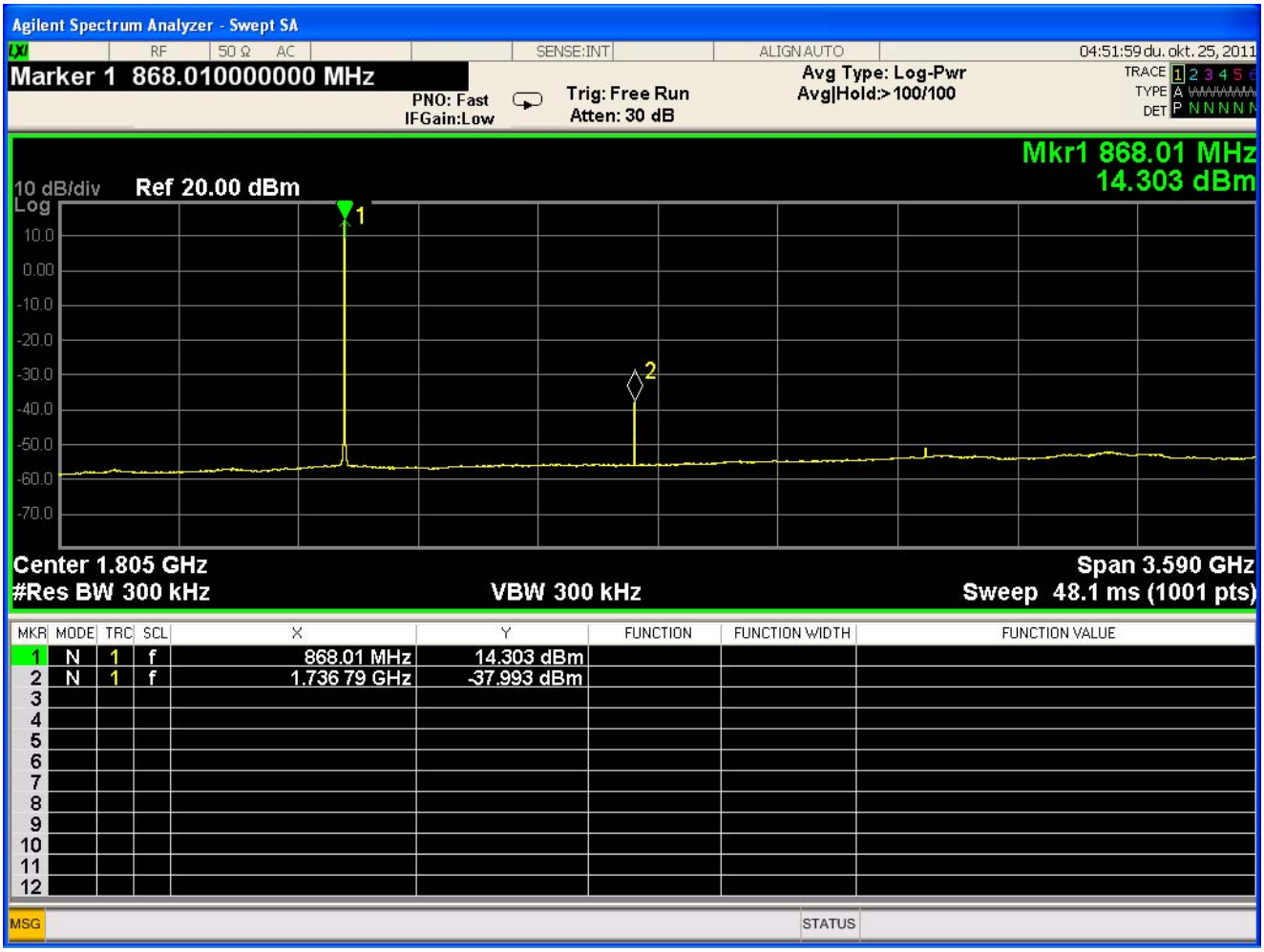

Figure 56. Si4461 14 dBm Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x2E, 33.2 mA

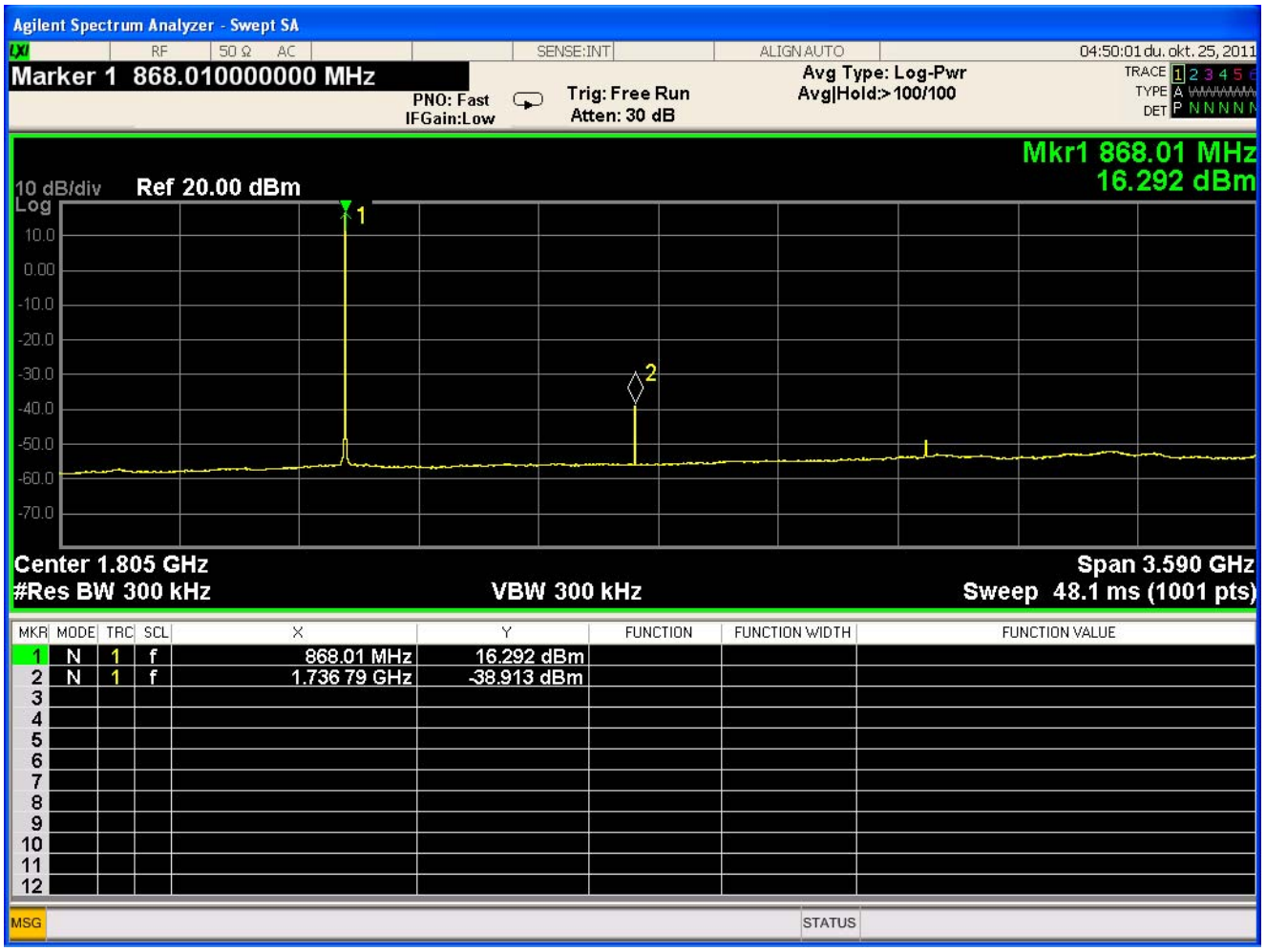

Figure 57. Si4461 16 dBm Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL Register is 0x41, 39.6 mA

Si4461 Direct Tie TX/RX Board CLE Configurations with Multilayer Inductors

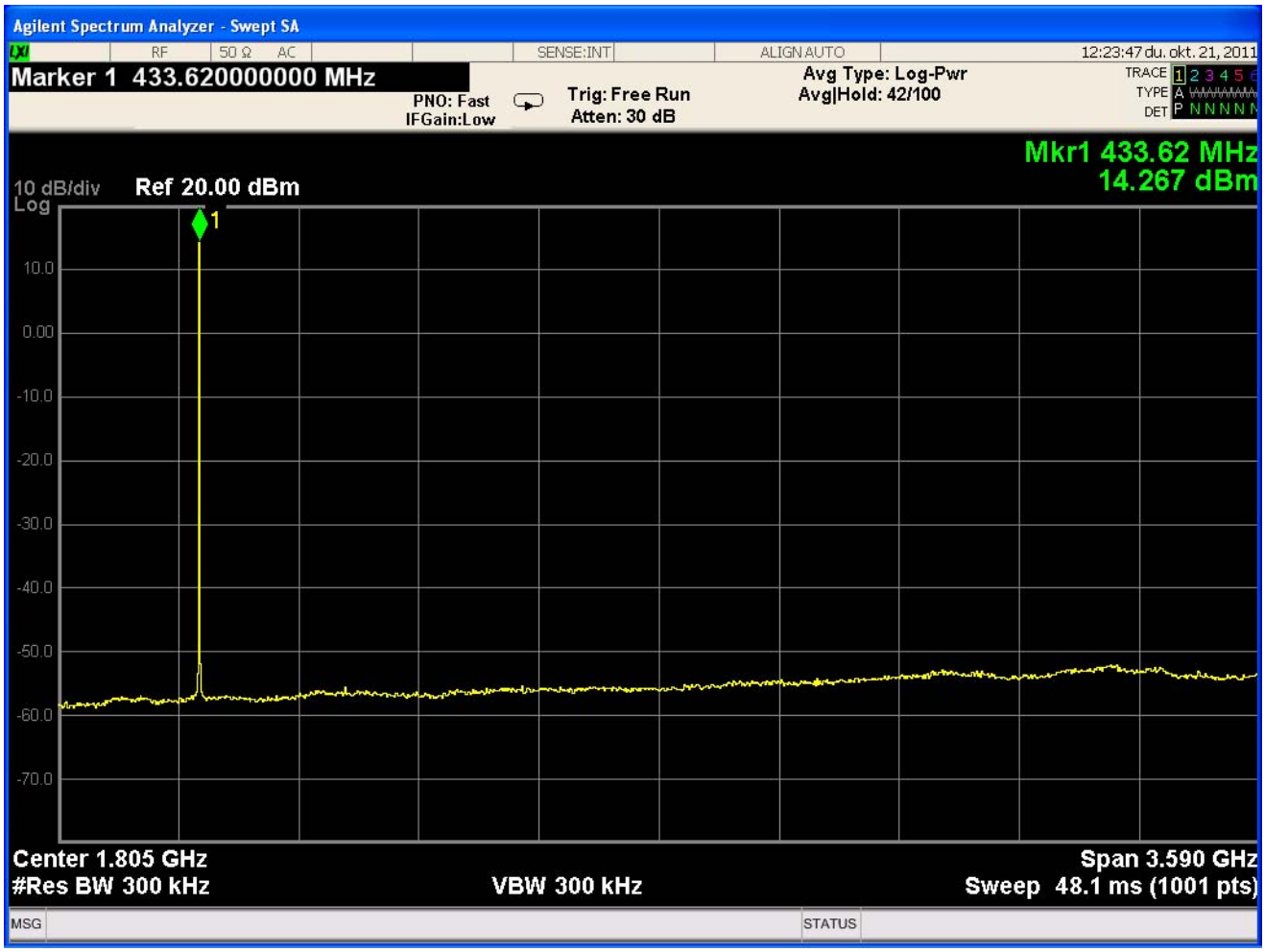

Figure 58. Si4461 14 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x2F, 30.1 mA

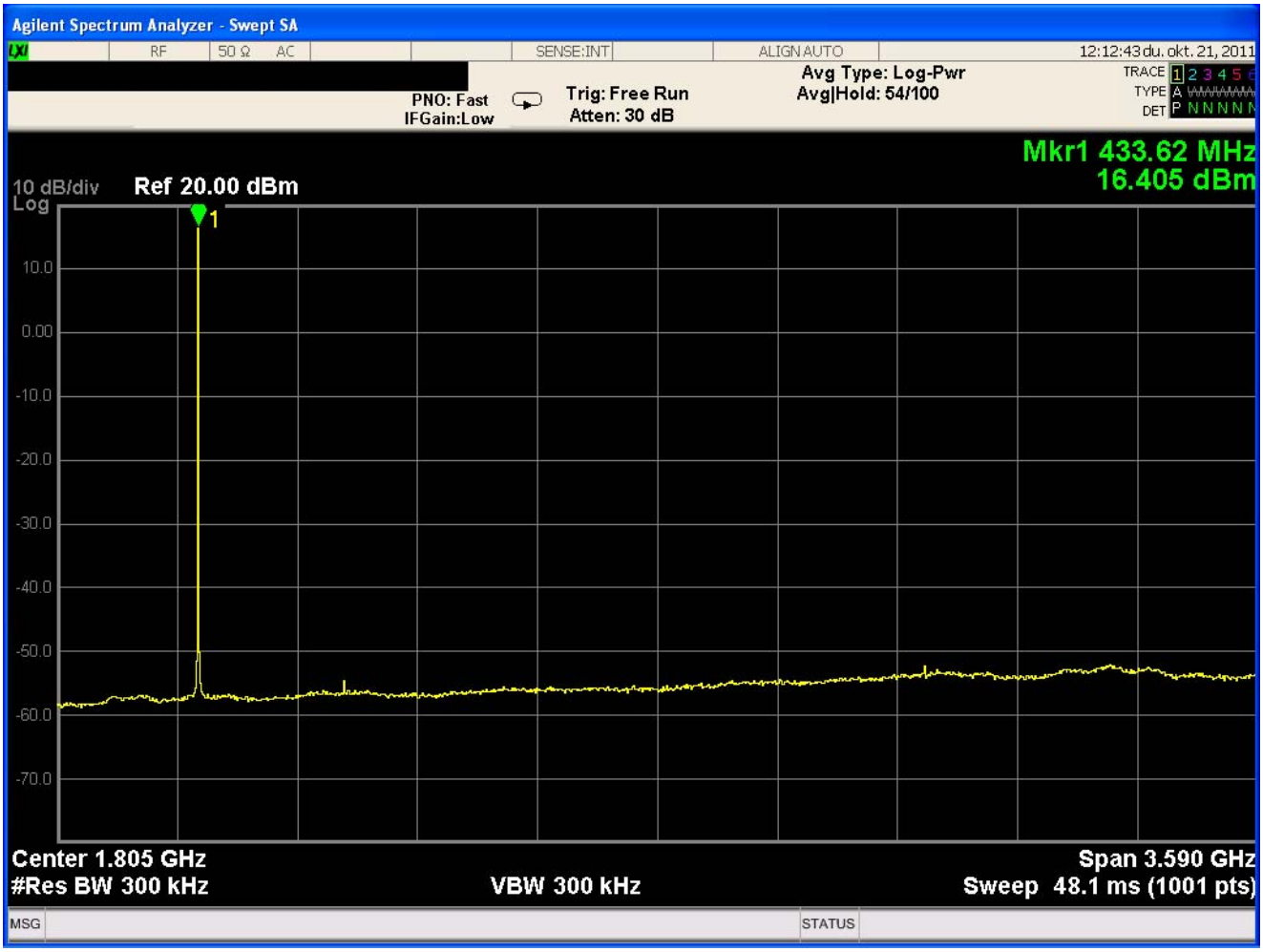

Figure 59. Si4461 16 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x7F, 40.1 mA

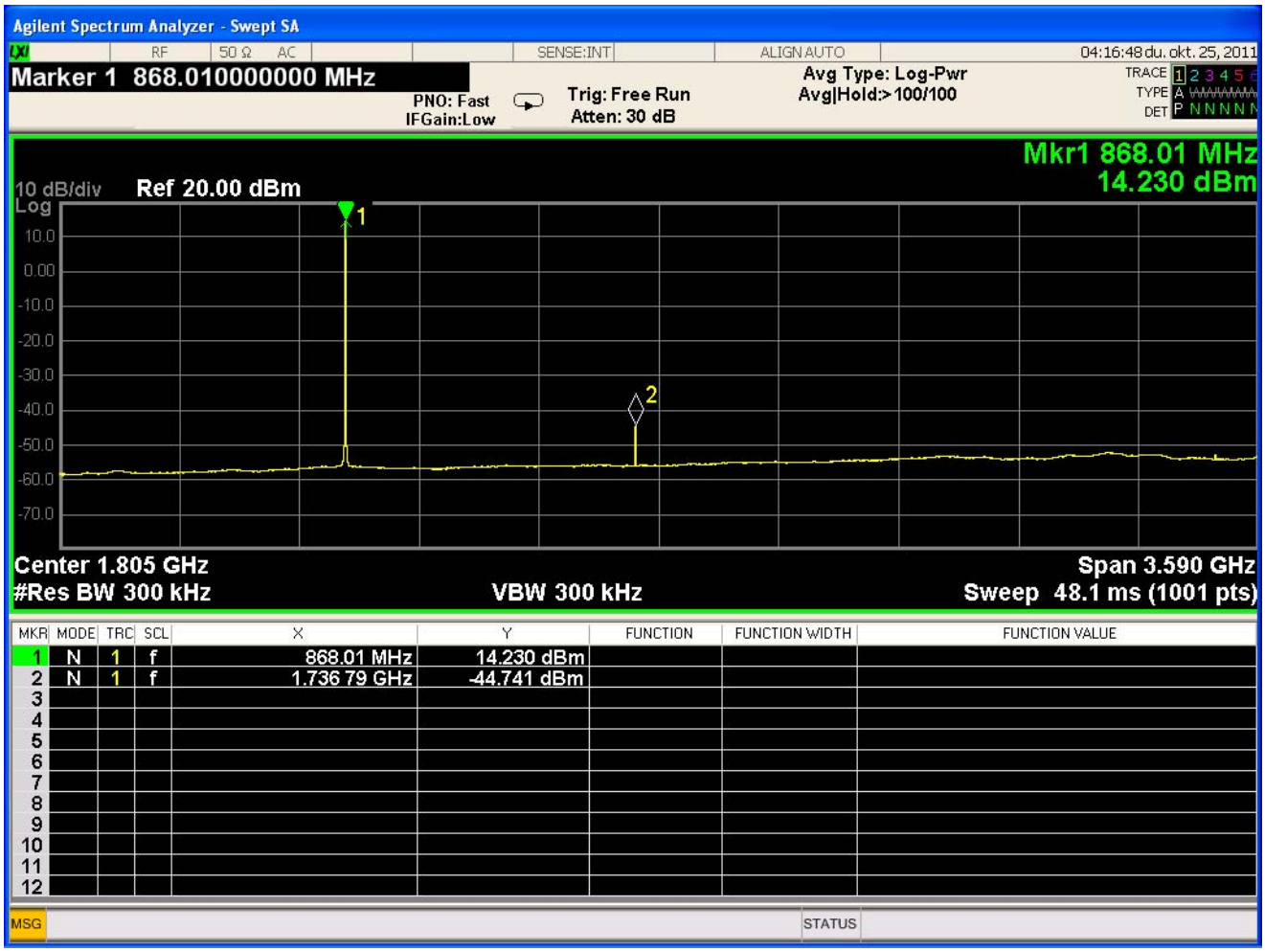

Figure 60. Si4461 14 dBm Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x34, 34.4 mA

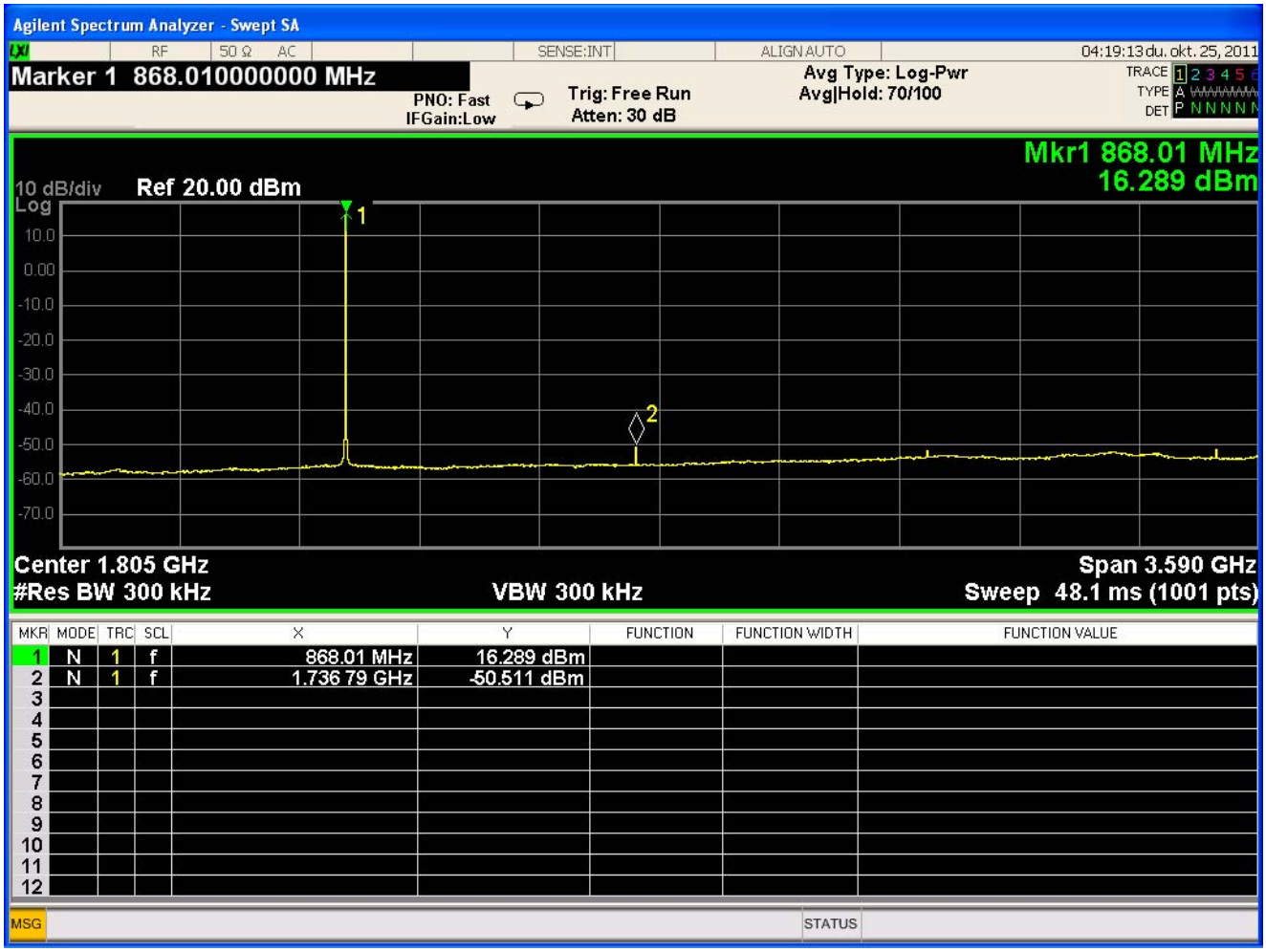

Figure 61. Si4461 16dBm Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x5E, 42.9 mA

Si4060/Si4460/67 Measured Plots

Si4060/Si4460/67 Split TX/RX Board CLE Configurations with Wire-Wound Inductors

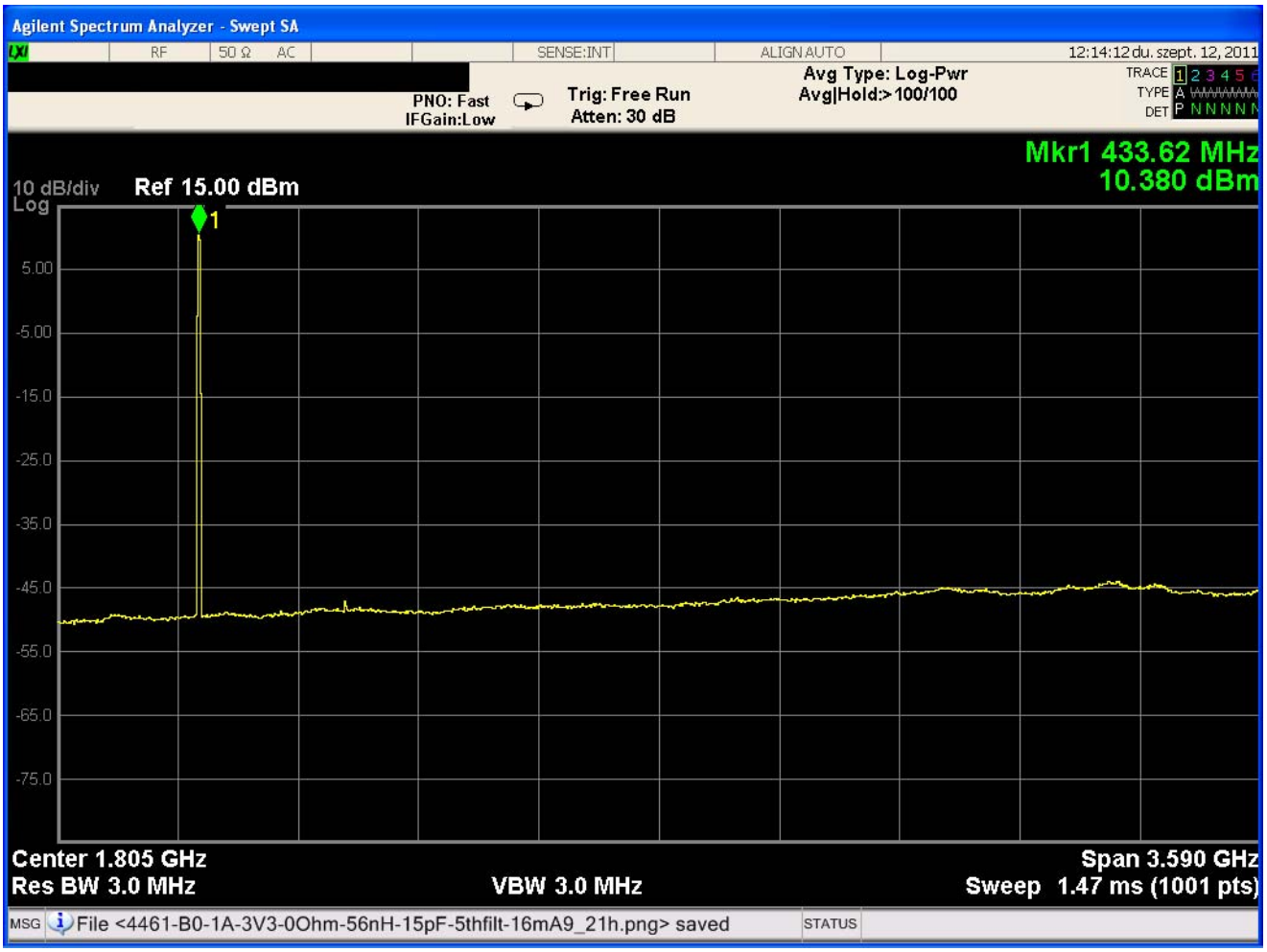

Figure 62. Si4060/Si4460/67 10 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x19, 16.9 mA

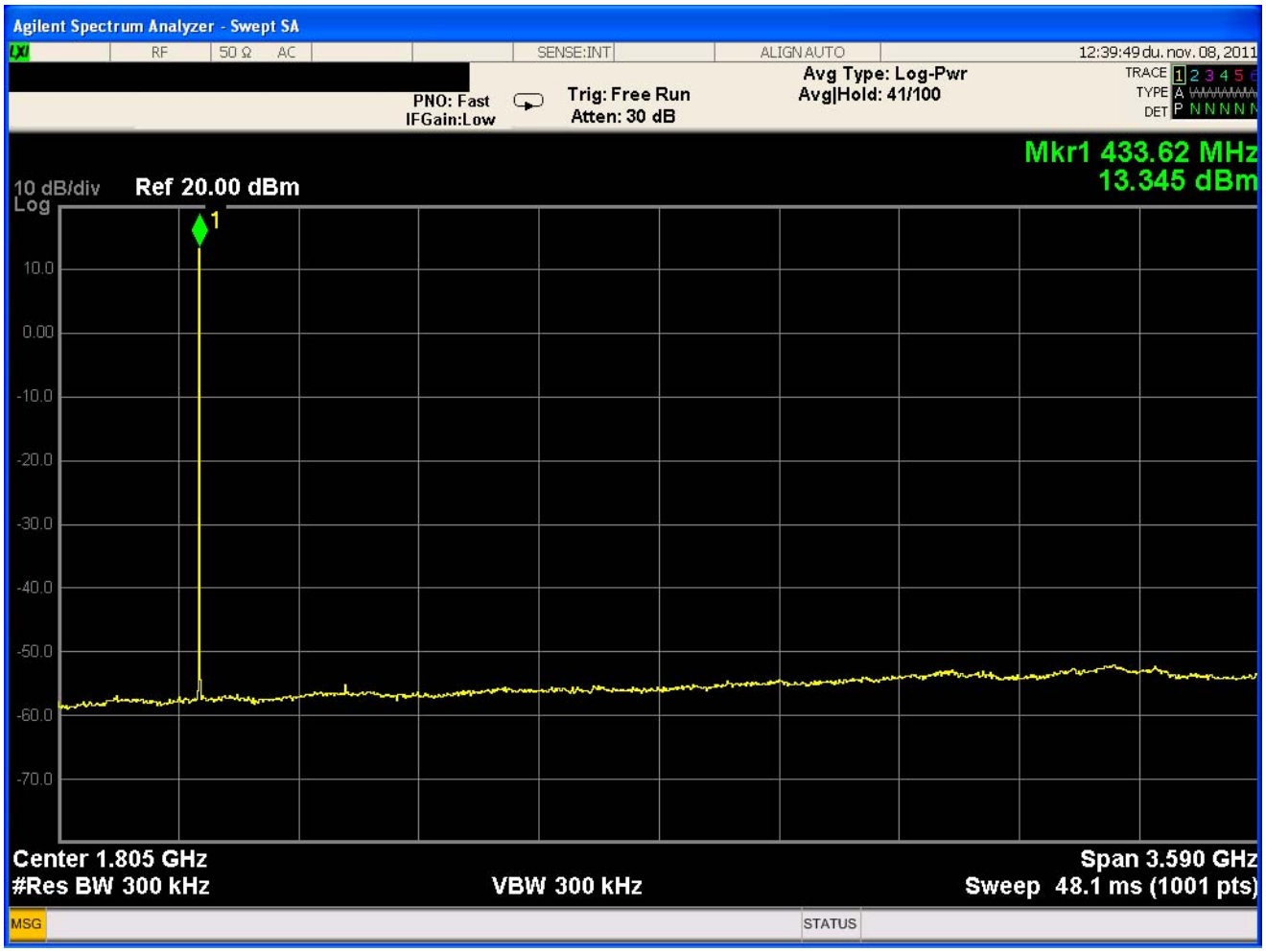

Figure 63. Si4060/Si4460/67 13 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3F, 22.7 mA

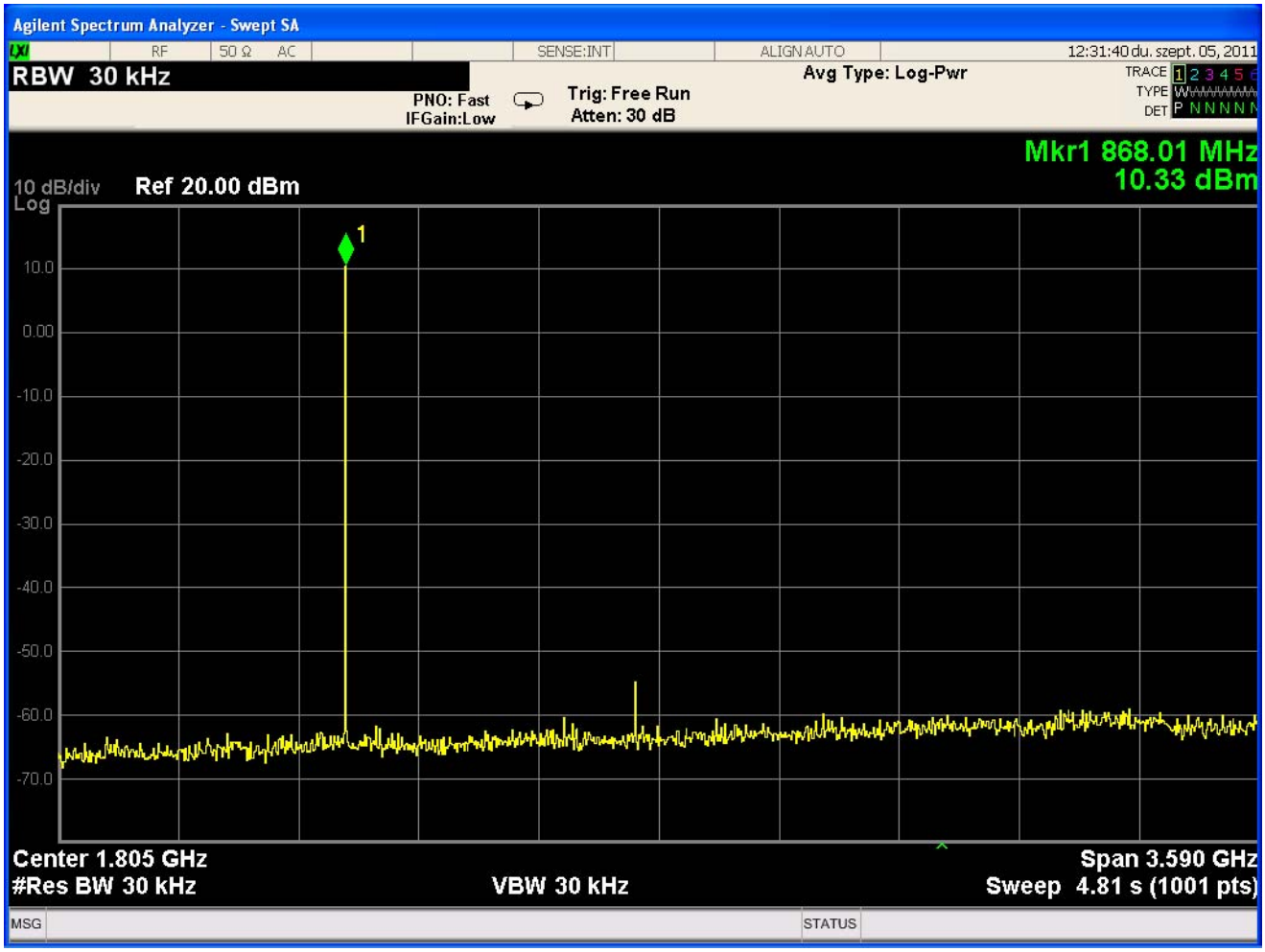

Figure 64. Si4060/Si4460/67 10 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x19h, 16.4 mA

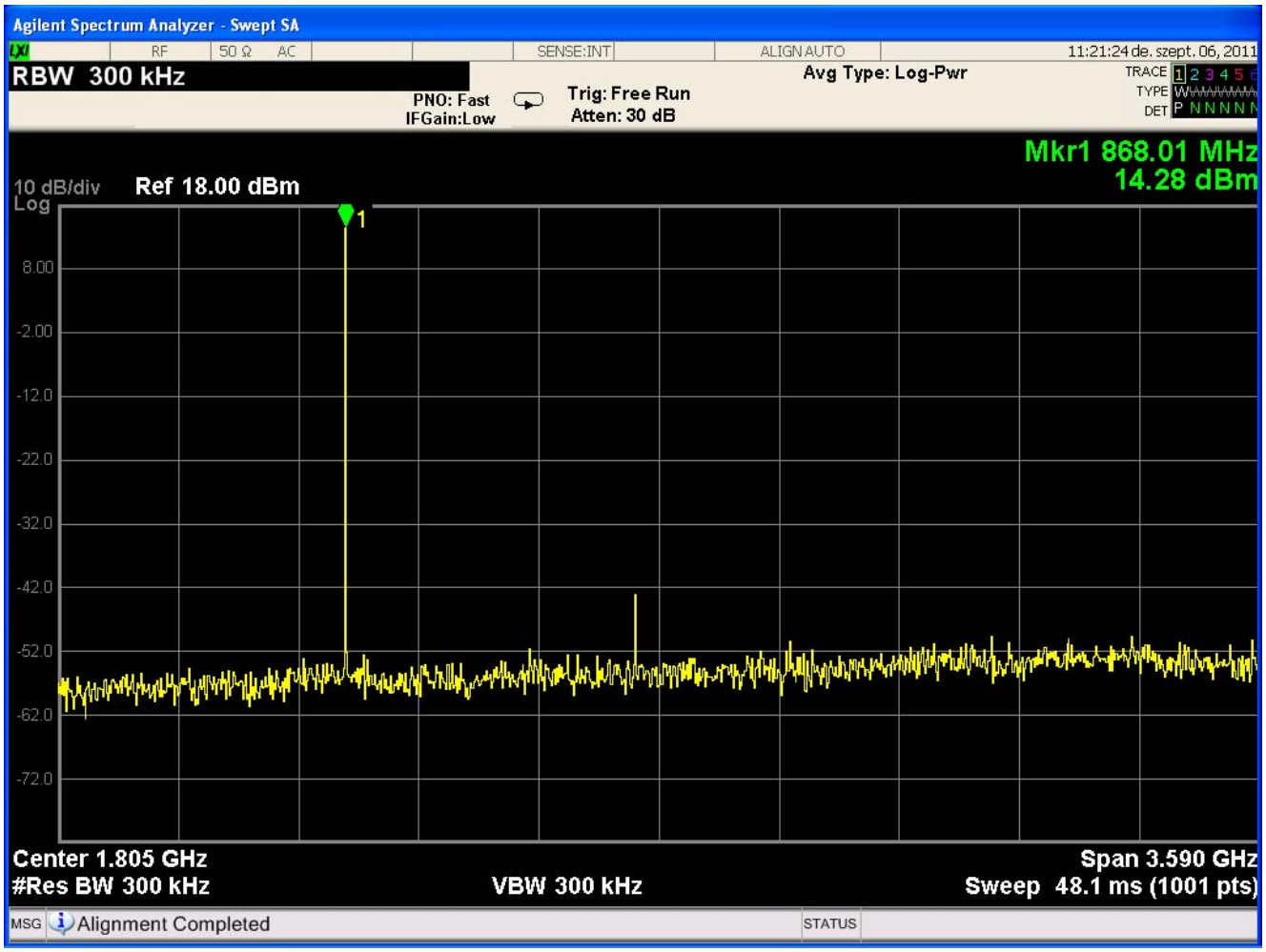

Figure 65. Si4060/Si4460/67 14 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3Dh, 24.8 mA

Si4060/Si4460/67 Split TX/RX Board CLE Configurations with Multilayer Inductors

For Si4060/Si4460/67 Multilayer split TX/RX boards pls. use the TX part of the DT multilayer matches. The resulted spectrum plots are very close to that given for the multilayer DT boards in TX mode (pls. see 6.3.4 chapter).

Si4460/67 Direct Tie TX/RX Board CLE Configurations with Wire-Wound Inductors

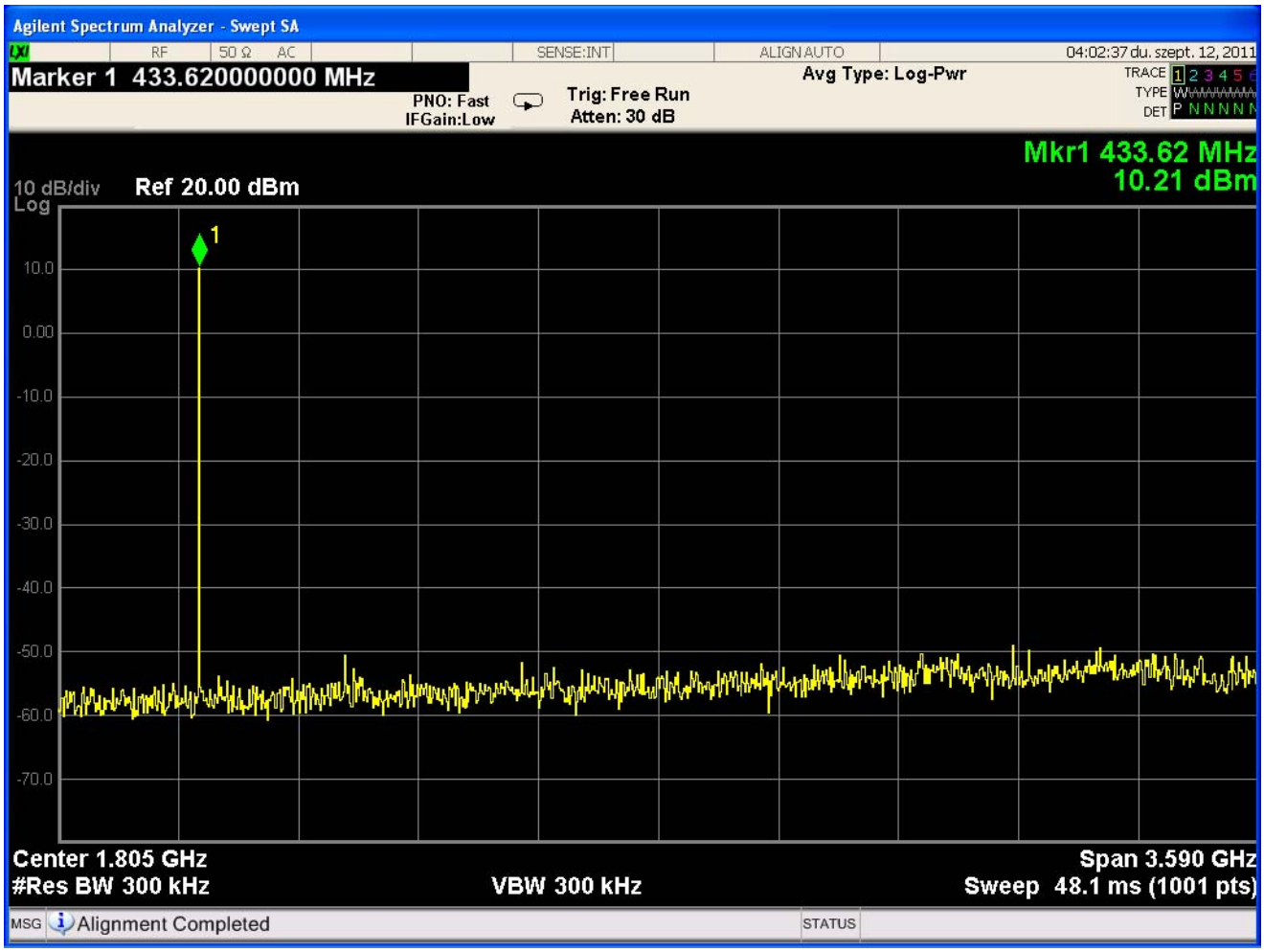

Figure 66. Si4460/67 10 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x1A, 16.9 mA

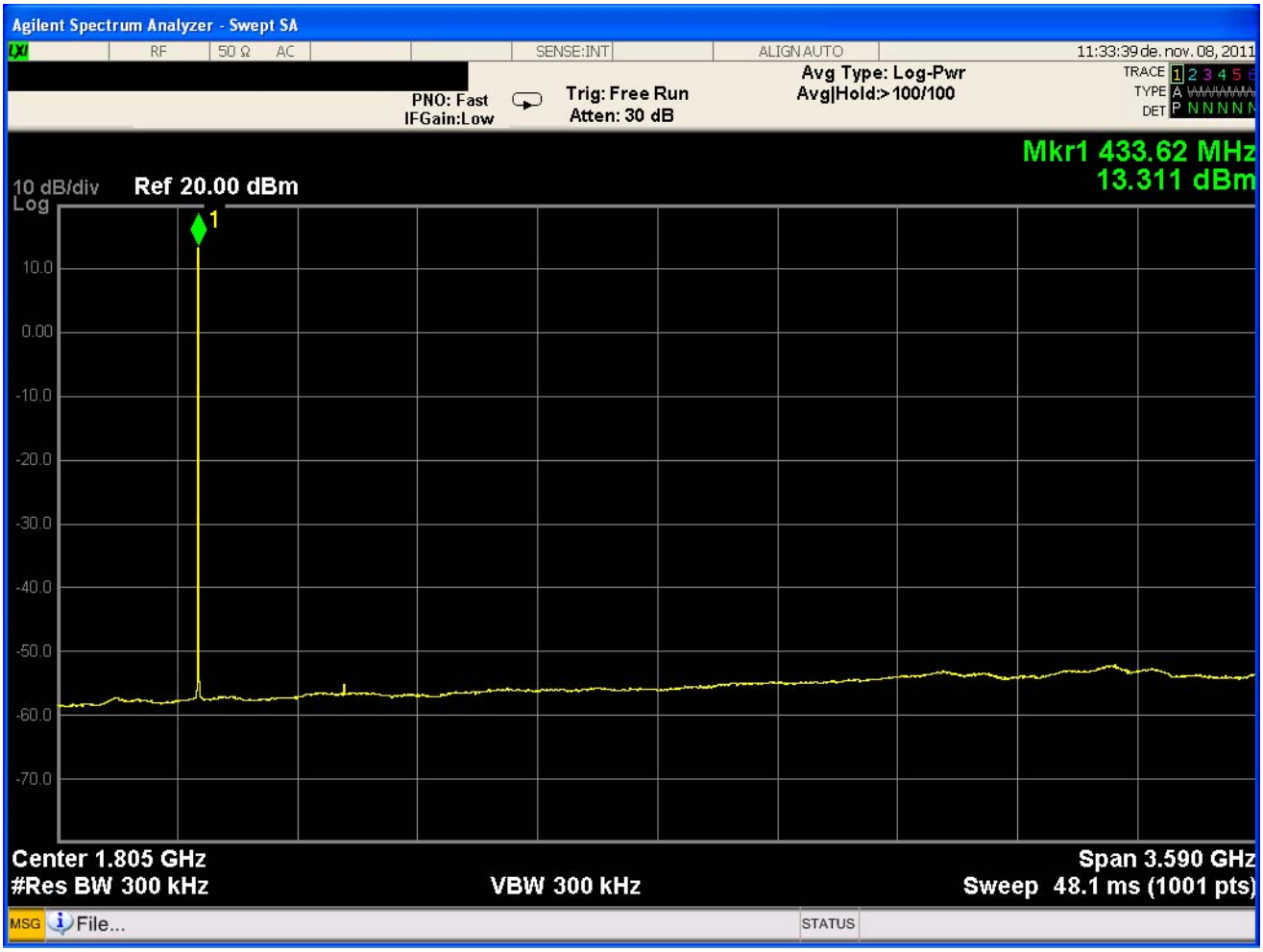

Figure 67. Si4460/67 13 dBm HP Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3F, 23 mA

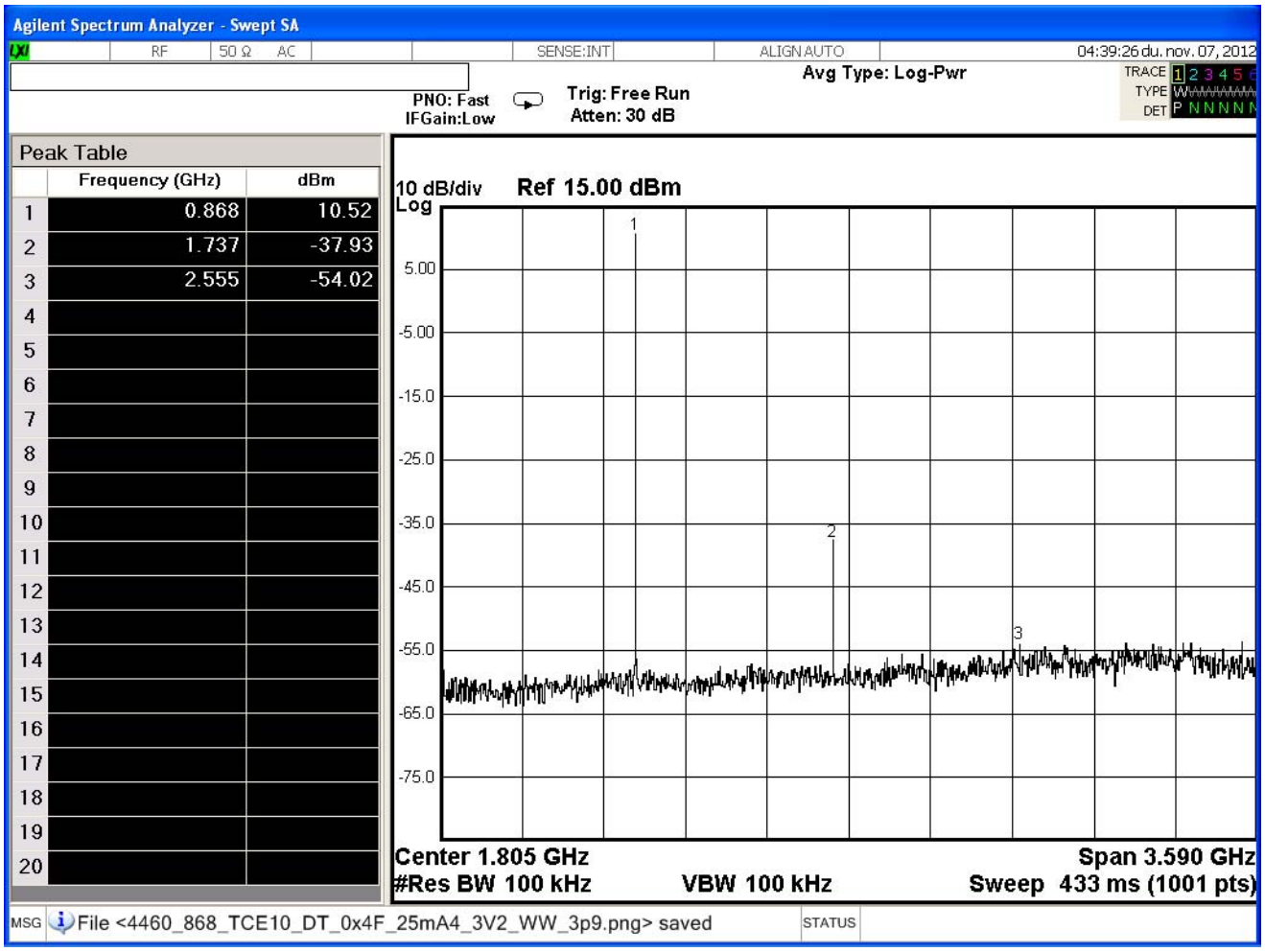

Figure 68. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 19.7 mA

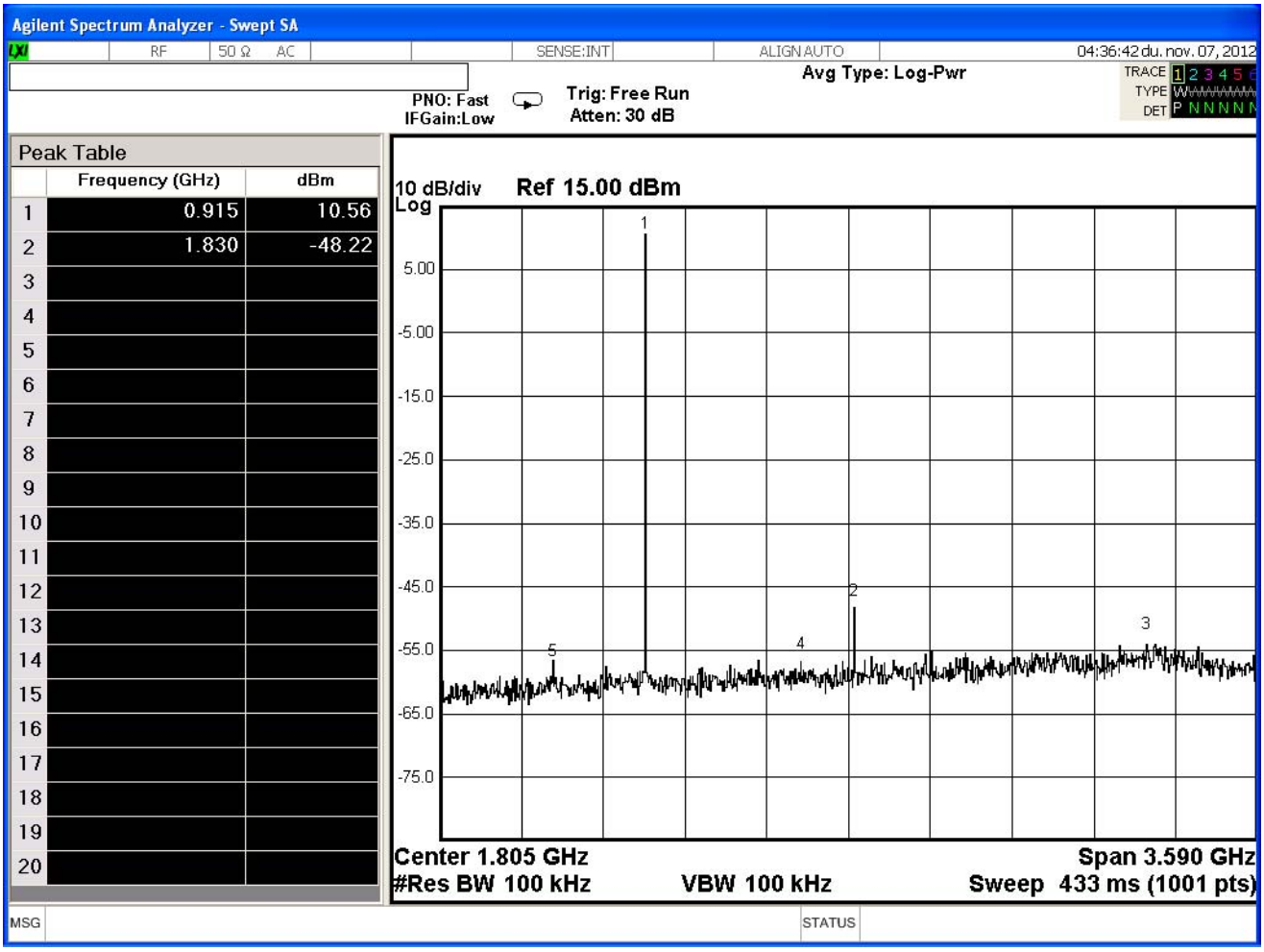

Figure 69. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 915 MHz with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 20 mA

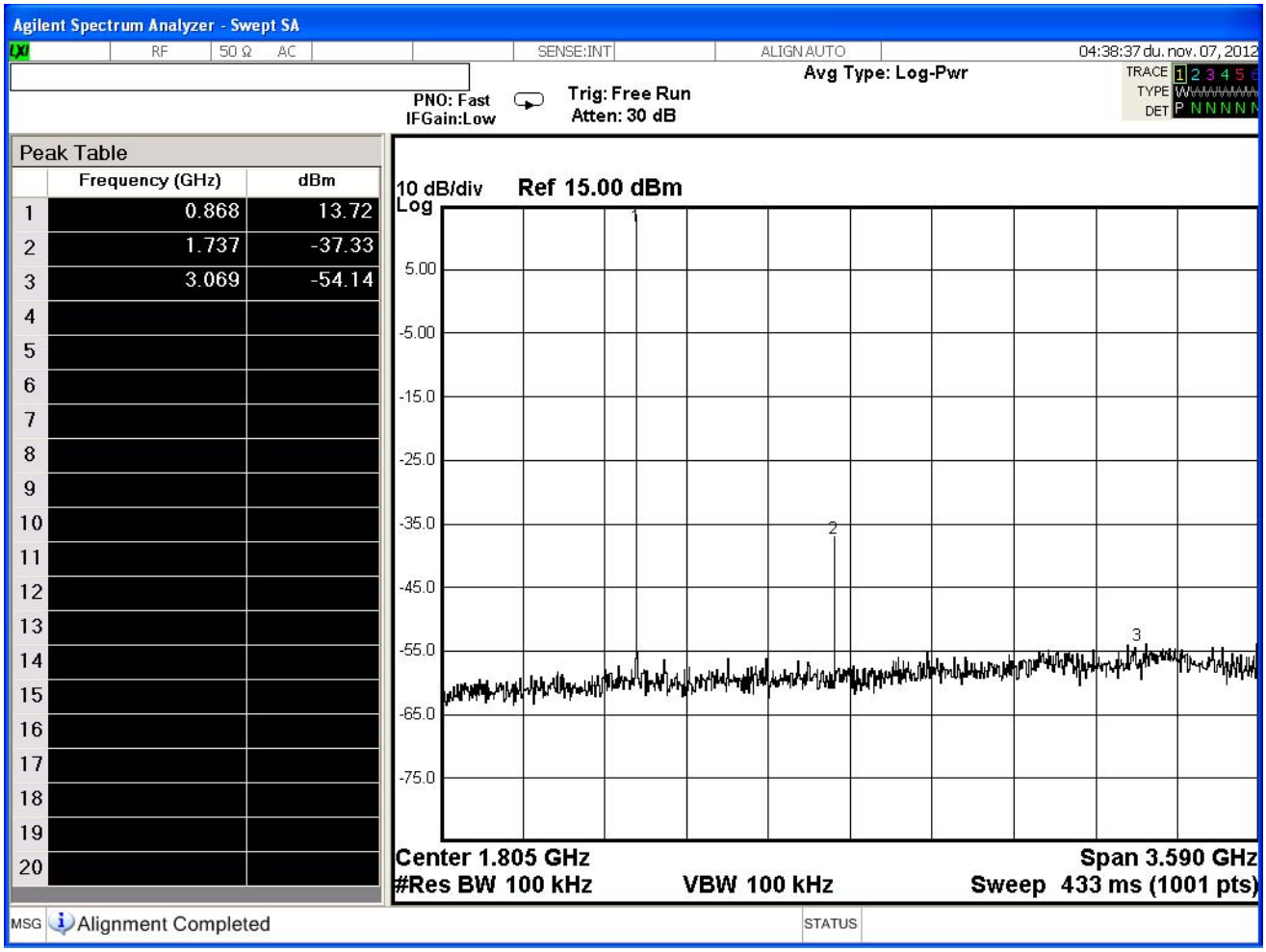

Figure 70. Si4460/67 868-915M Direct Tie TX/RX Board at 868 MHz at Max Power State with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 25.5 mA

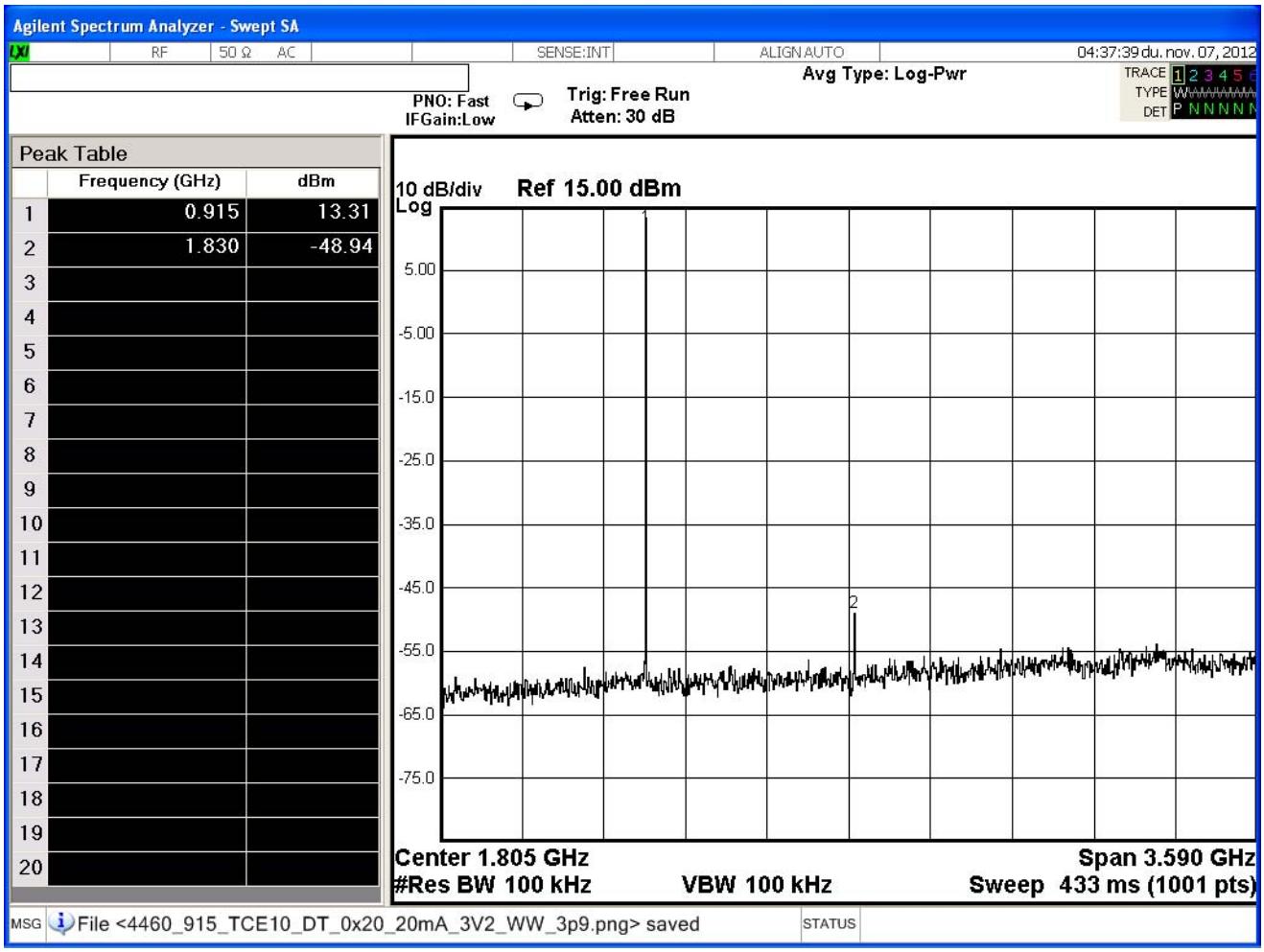

Figure 71. Si4460/67 868–915M Direct Tie TX/RX Board at 915 MHz at Max Power State with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 24.7 mA

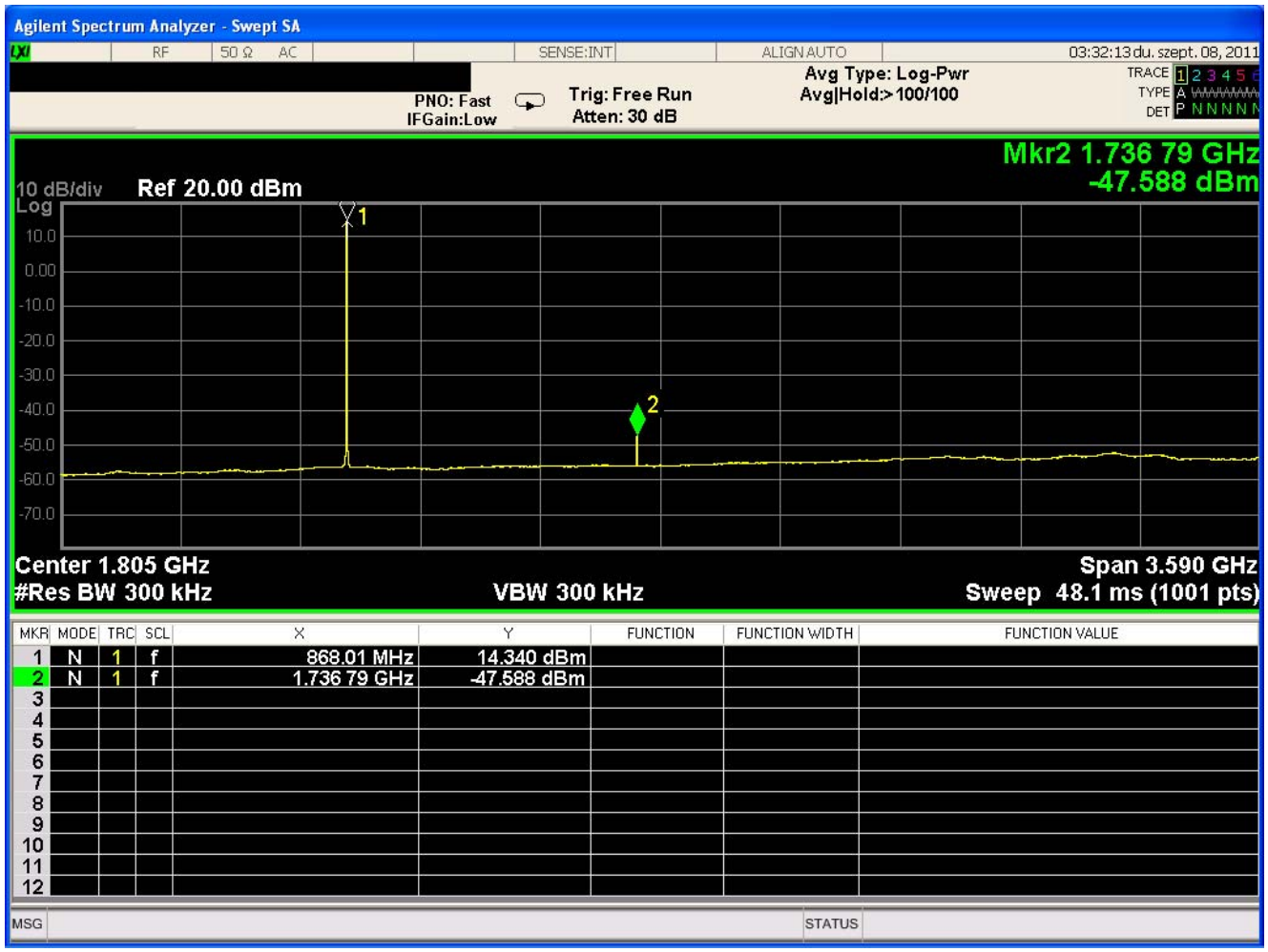

Figure 72. Si4460/67 14 dBm Direct Tie HP TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x44, 25.6 mA

Si4460/67 Direct Tie TX/RX Board CLE Configurations with Multilayer Inductors

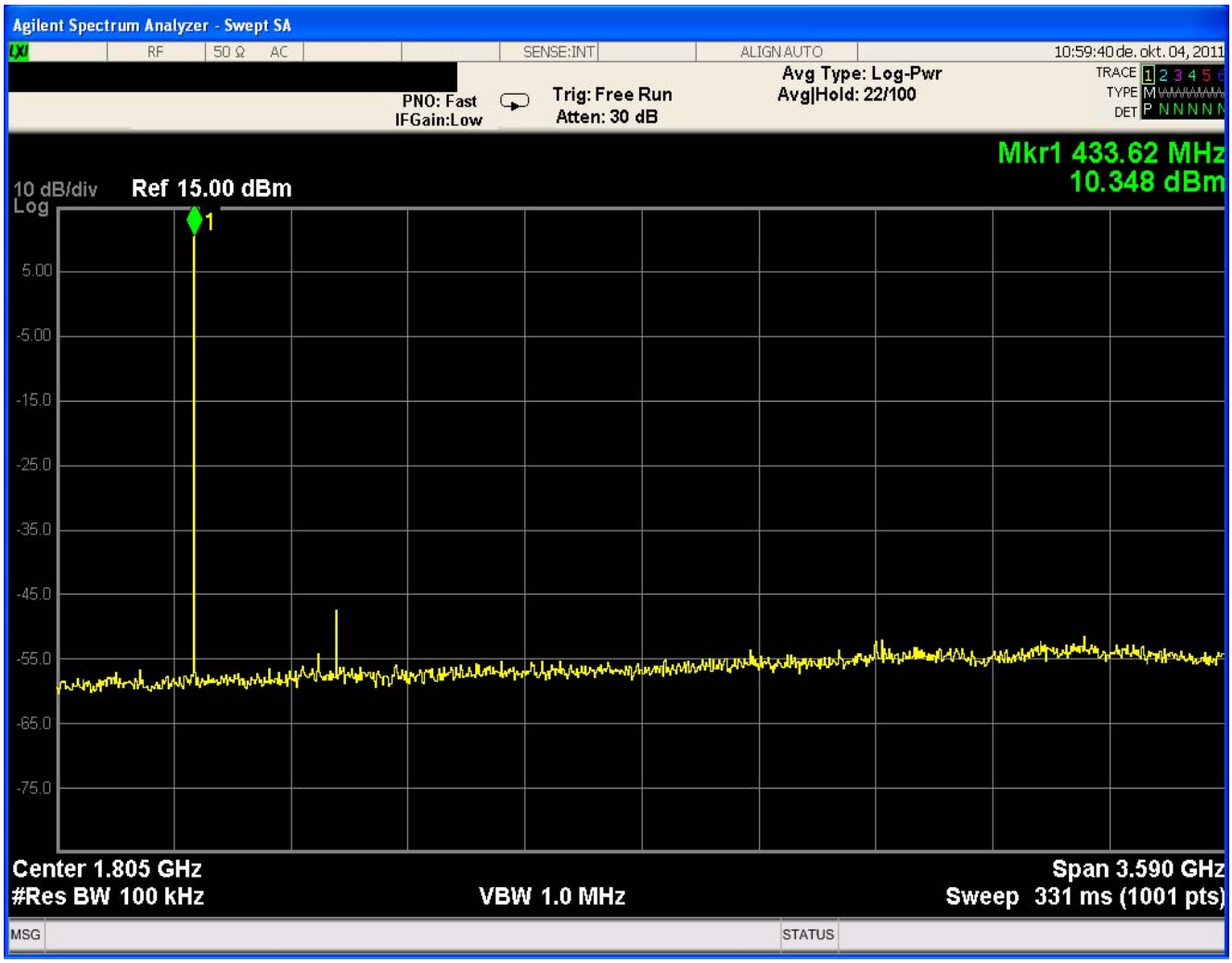

Figure 73. Si4460/67 10 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x2A, 17.1 mA

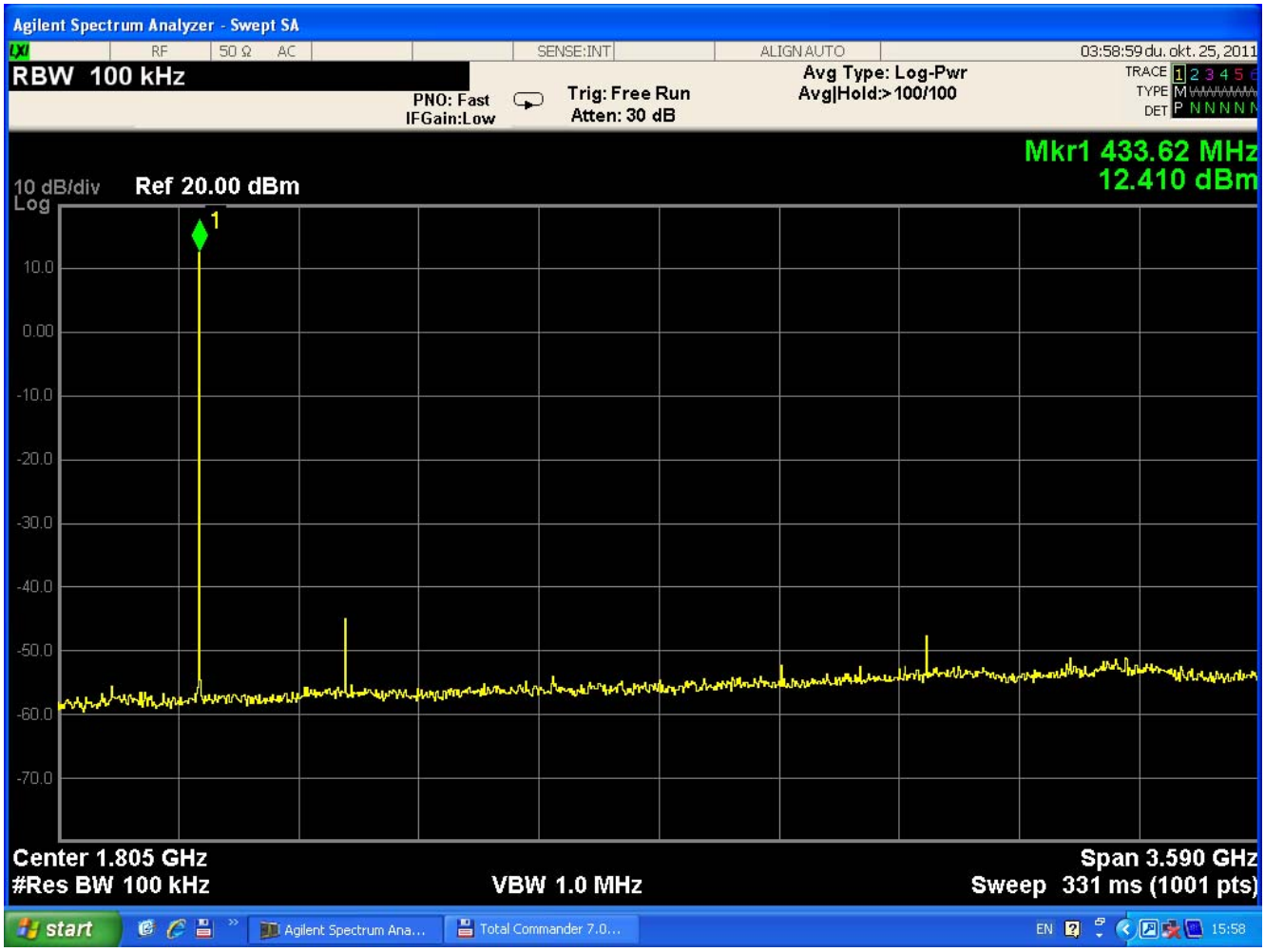

Figure 74. Si4460/67 12.3 dBm Direct Tie HP TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 23.1 mA

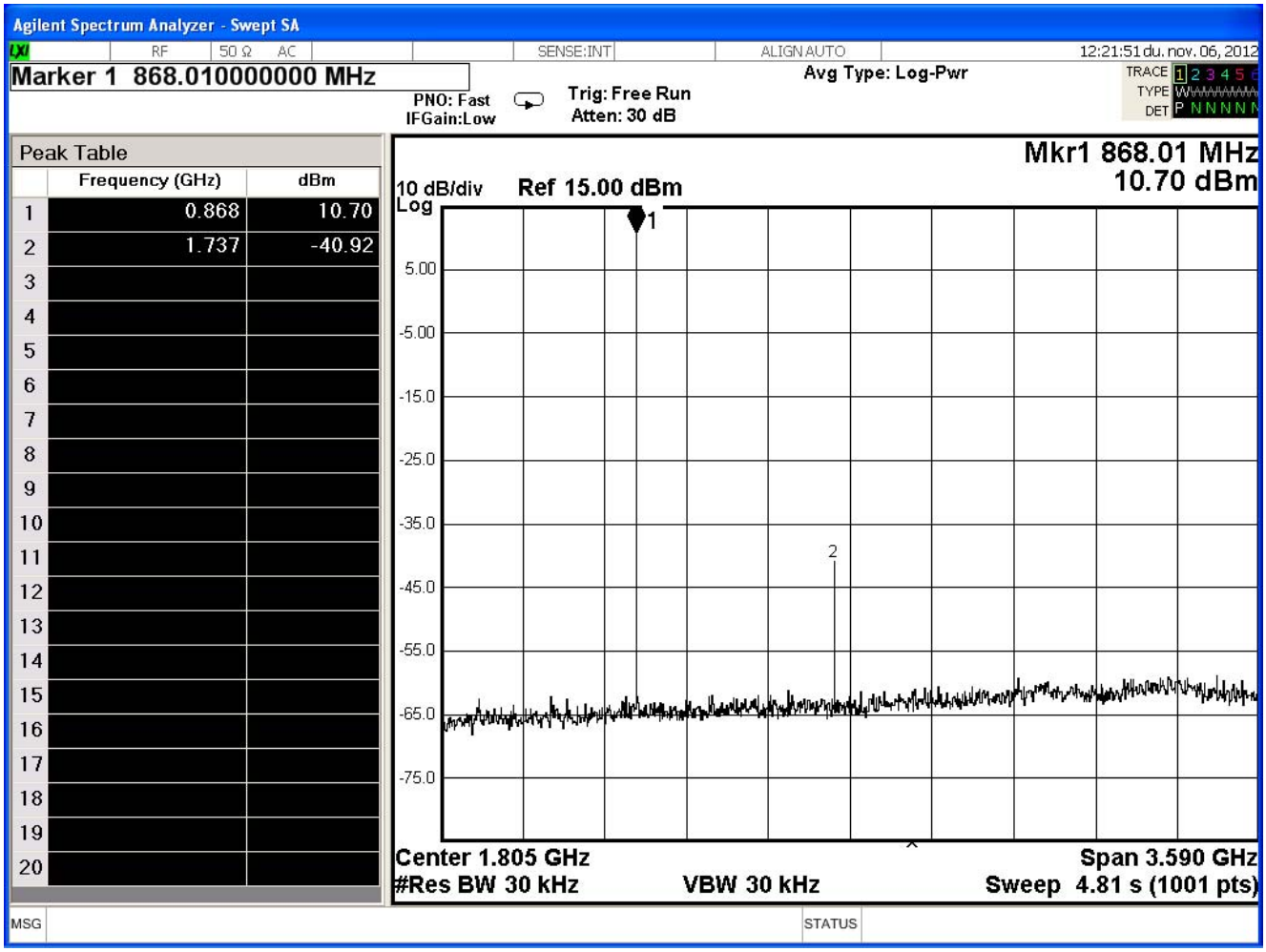

Figure 75. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 19.7 mA

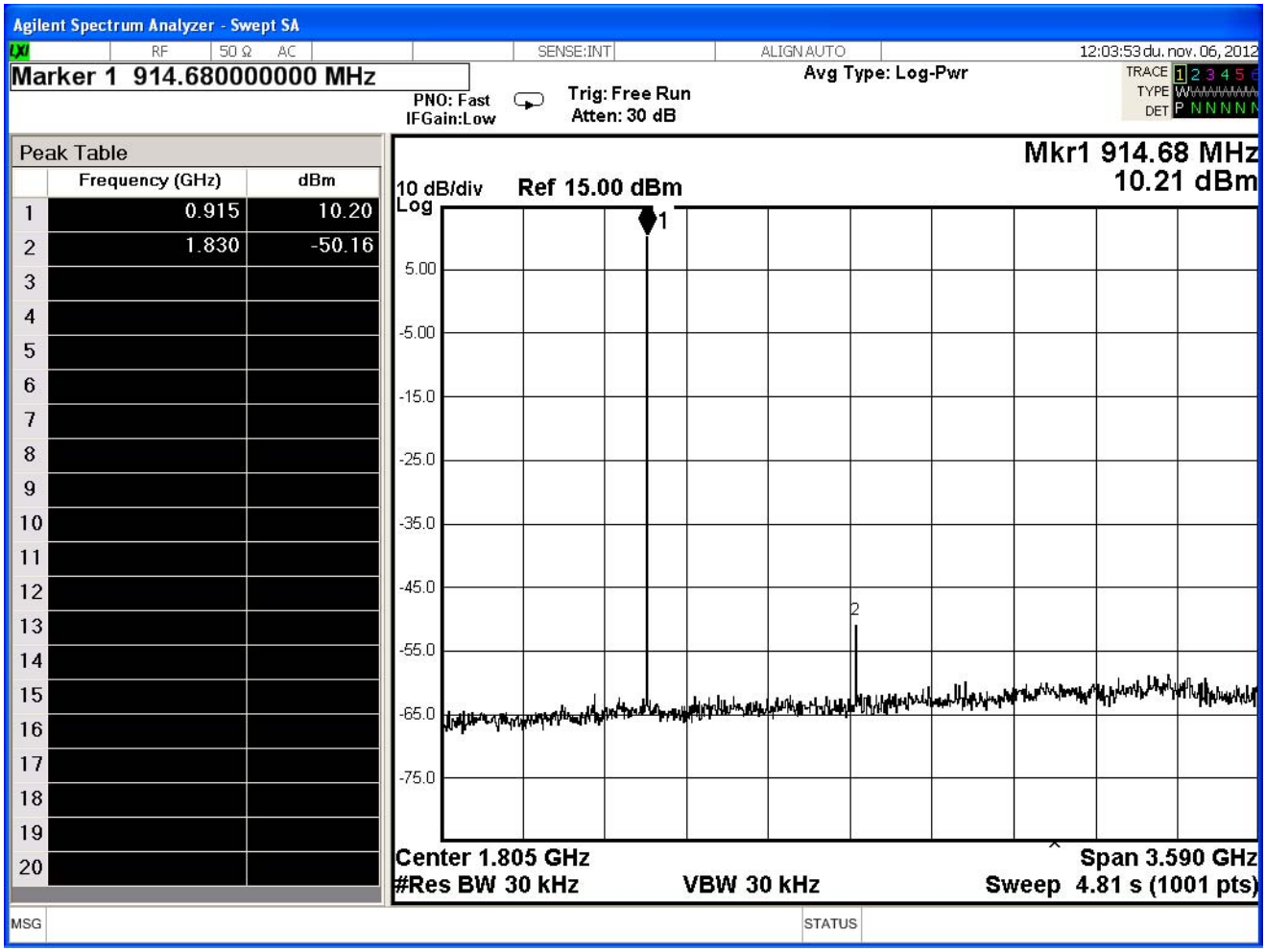

Figure 76. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 915 MHz with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 19.3 mA

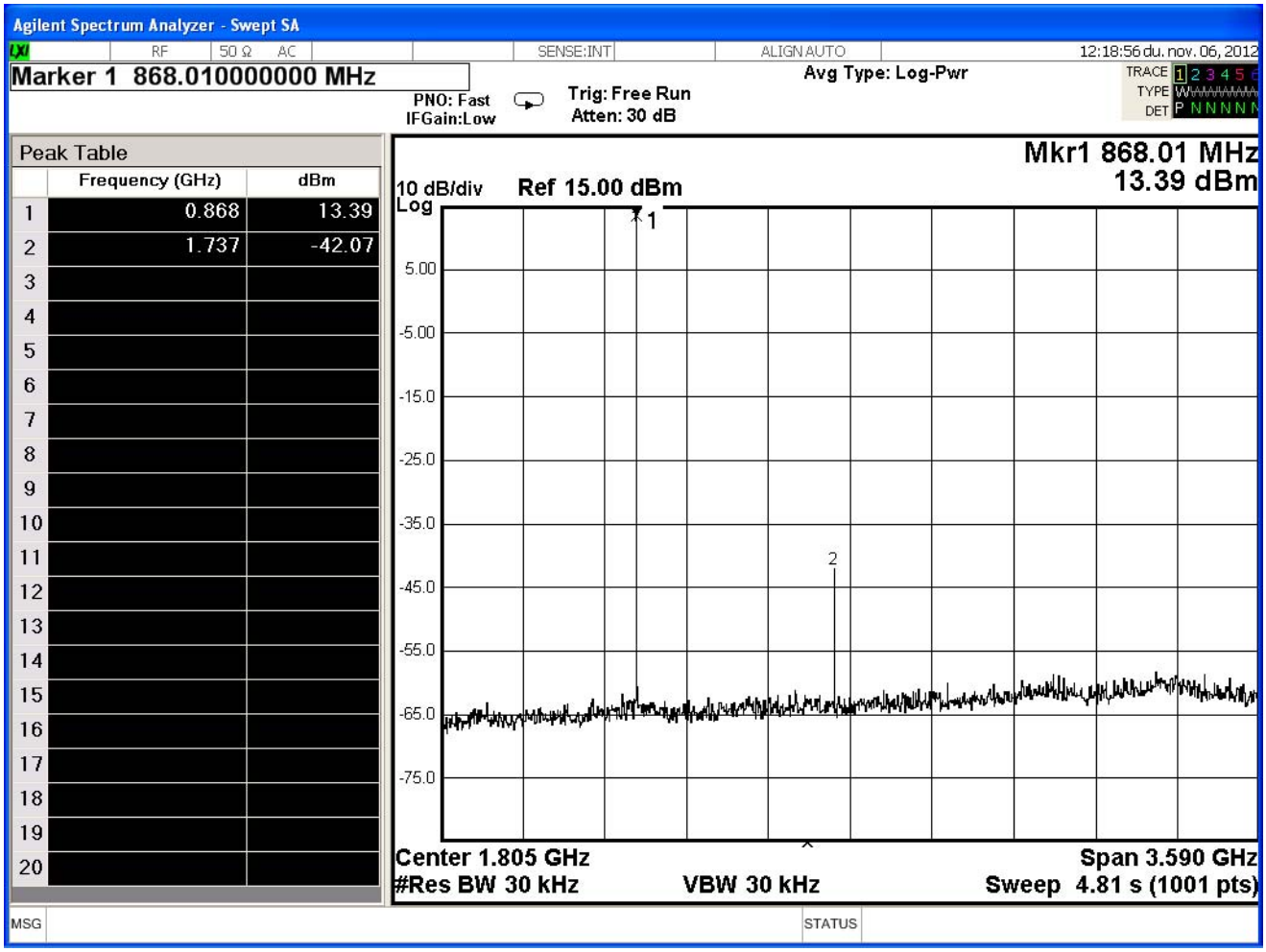

Figure 77. Si4460/67 868–915M Direct Tie TX/RX Board at 868 MHz at Max Power State with Multilayer Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 24.7 mA

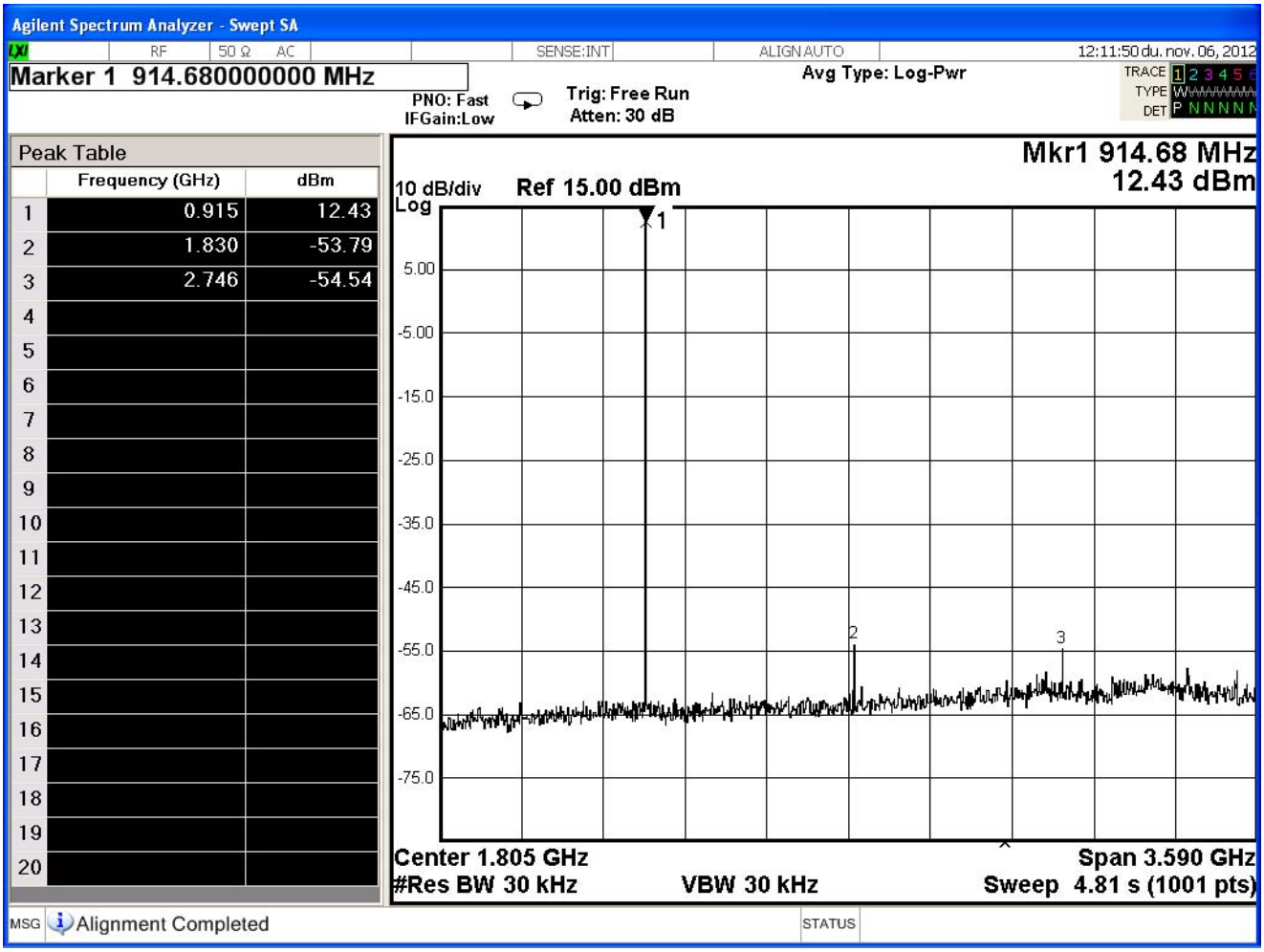

Figure 78. Si4460/67 868–915M Direct Tie TX/RX Board at 915 MHz at Max Power State with Multilayer Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 23.7 mA

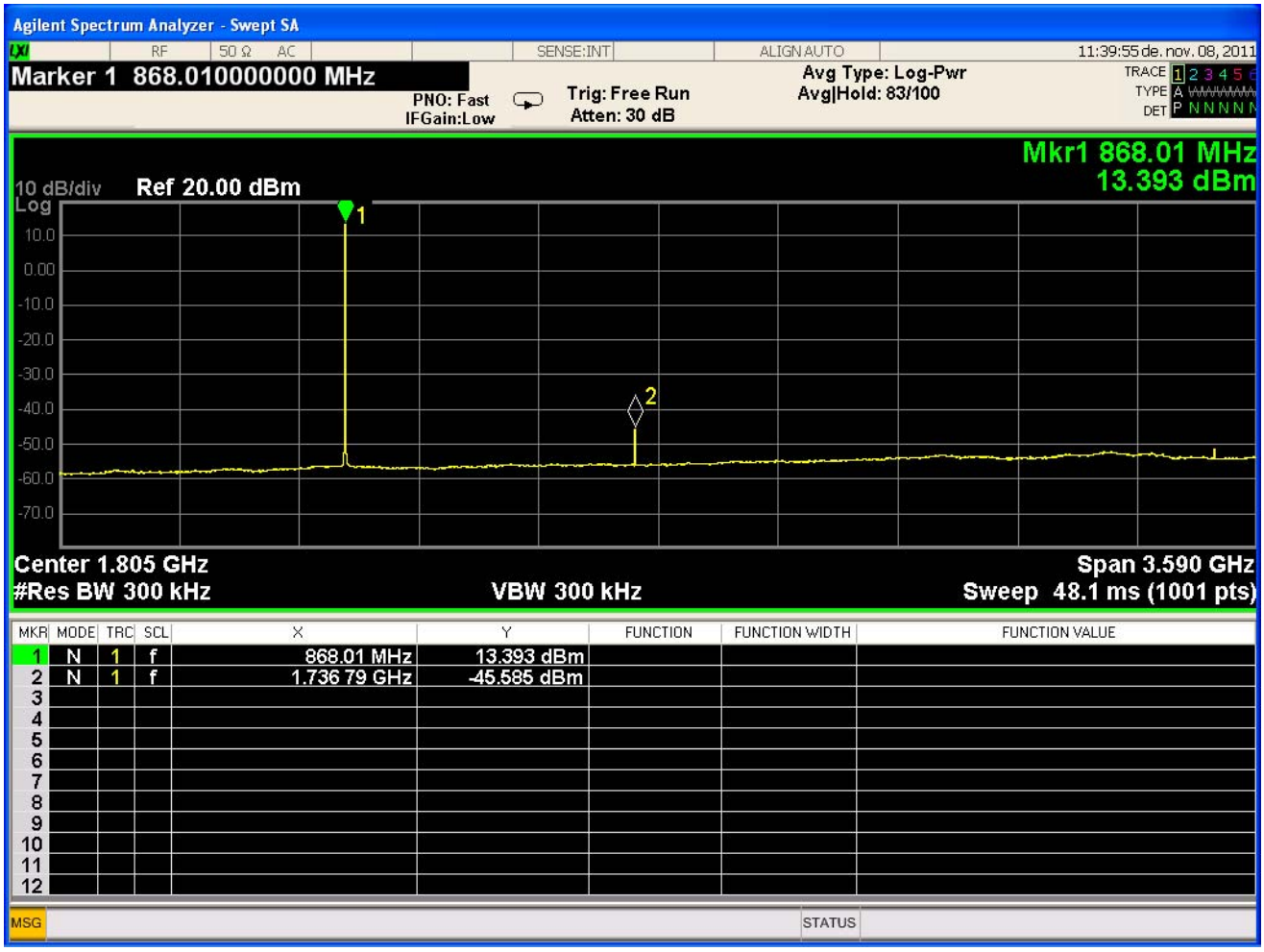

Figure 79. Si4460/67 13 dBm Direct Tie HP TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3C, 24.1 mA

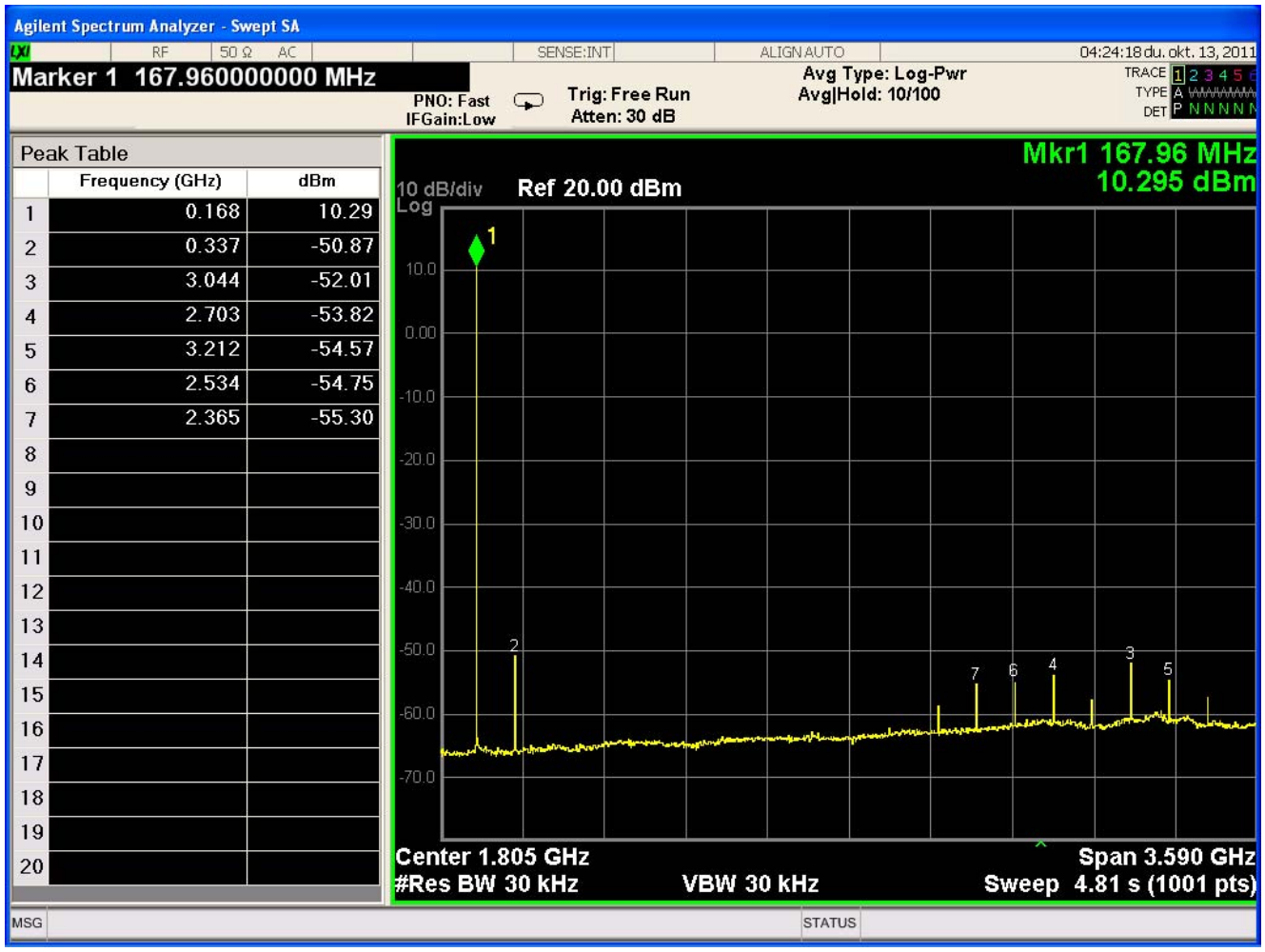

Figure 80. Si4460/67 10 dBm Direct Tie TX/RX Board at 169 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x23, 18.4 mA

Document Change List

Revision 0.1 to Revision 0.2

- Revised "1. Introduction" on page 1.
- Revised "2. Summary of Matching Network Component Values" on page 6.
- Added "4. Class E (CLE) Matching Procedure Overview" on page 50.
- Added "5. CLE Matching Procedure for the Si4060/Si4460/61/67" on page 56.
- Added " Appendix A—Measured Spectrum Plots" on page 88.

Revision 0.2 to Revision 0.3

- Added " Table of Contents" on page 4.
- Extended introduction with more detailed descriptions.
- Updated "2.1.2. Si4461 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance" on page 9.
  - Added a new 868M Si4461 SWC DT Match (FC868M) with flat Pout vs. Vdd characteristic in new Tables 4 and 5 in this section.
  - Added Table 6 in this section.
- Added description of 25% duty cycle PA mode used in Si4460 Class E matches in "2.2. Component Values for Si4060/Si4460/67 Matchings" on page 17.
- New 10 dBm Si4460 Class E 868/915M dual band DT match (old 10 dBm 868M Class E DT eliminated) given in new Tables 14, 15, and 17 (element values and measured results).
- Added Table 18, “Output Power, Current Consumption vs. Vdd (Direct Tie Si4460/67 434M CLE Board, WW Inductors),” on page 22.
- Added "2.2.3. Si4060/4460/67 with Split TX\RX SWC Board Configuration: Component Values and Performance" on page 23.
- Added "2.2.4. Si4460/67 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance" on page 23.
- New Tables 19, 20, and 21.
- Added Figure 8, “Matching Topology for Single Antenna with Direct Tie SWC Board Configuration,” on page 25.
- Updated " Appendix A—Measured Spectrum Plots" on page 88.
  - Added new Figures 68–71 and 75–78.

Revision 0.3 to Revision 0.4

- Added new part (Si4467)
- Added Si4461 DT Class-E 915 MHz +16 dBm multilayer matching.
- Bug fixing.

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