

Operating Principle and Performance Optimization of a Three-Level NPC Dual-Active-Bridge DC-DC Converter

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Abstract—Aiming to improve the performance features of conventional two-level dual-active-bridge (DAB) converters, this paper presents a three-level neutral-point-clamped (NPC) DAB dc-dc converter. A general modulation pattern is initially defined, the dc-link capacitor voltage balancing is analyzed in detail, and a proper balancing control is designed. Then, a set of decoupled optimization problems are formulated as a function of the available modulation degrees of freedom to minimize the predominant converter losses. Finally, a simple and practical specific modulation strategy is provided resembling the optimum solutions. The good performance of the proposed three-level NPC DAB converter operated with the proposed modulation strategy and voltage balancing control is verified through simulation and experiments. The capacitor voltage balancing can be guaranteed for all operating conditions. In addition, it is concluded that the multilevel topology provides benefits compared with the conventional two-level DAB converter.

Index Terms—Active neutral point clamped, bidirectional dc-dc converter, capacitor voltage balancing, dual active bridge, efficiency optimization, multilevel converter.

NOMENCLATURE

| | |
|----------------------------|---|
| V_Z | z -side dc-link voltage. |
| v_{Cz1}, v_{Cz2} | z -side capacitor voltages. |
| v_z | z -side transformer voltage. |
| $\mathbf{V}_{z,h}$ | Phasor of the h -th harmonic of v_z . |
| i_z | z -side transformer current. |
| $\mathbf{I}_{z,h}$ | Phasor of the h -th harmonic of i_z . |
| $i_{z,h}^p$ | Component of the h -th harmonic of i_z in phase with the h -th harmonic of v_z . |
| $i_{z,h}^q$ | Component of the h -th harmonic of i_z in quadrature with the h -th harmonic of v_z . |
| n | Transformer turns ratio. |
| d | Primary-referred dc voltage gain. |
| L | Transformer leakage inductance. |
| f_s | Switching frequency. |
| t_b | Blanking time. |
| α_{z1}, α_{z2} | z -side inner switching angles. |

| | |
|------------------------------|---|
| $\alpha_{z01}, \alpha_{z02}$ | z -side outer switching angles. |
| α_{z1} | Average value of α_{z11} and α_{z01} . |
| α_{z2} | Average value of α_{z12} and α_{z02} . |
| $\Delta\alpha_{z,\min}$ | Minimum value of $\alpha_{z2} - \alpha_{z1}$. |
| φ | Phase shift between v_a and v_b . |
| P | DAB transferred power. |
| X_f | Optimum α_{z1} , α_{z2} , and φ of function F_f . |
| X_{PrS} | α_{z1} , α_{z2} , and φ of the modulation proposed in Section IV-D. |
| X_{PSM} | α_{z1} , α_{z2} , and φ of the conventional phase-shift modulation. |

I. INTRODUCTION

THE two-level (2L) dual active bridge (DAB) was originally presented in [1], and since then, the DAB and its variants (three phase, current fed, half-bridged DAB, etc) have been widely studied in the isolated bidirectional dc-dc conversion area [2], [3]. The original single-phase DAB configuration is composed by a high-frequency single-phase transformer where full-bridge 2L voltage-fed converters are located at the primary and secondary sides. In the conventional phase-shifted modulation (PSM), a square-wave voltage waveform is generated by each full bridge. These two voltages are phase shifted in order to transfer power between both dc links. The phase-shift angle magnitude and sign determine the transferred power magnitude and direction, respectively.

Let us define the dc conversion ratio as the primary-referred dc voltage gain, $d = V_B / (V_A \cdot n)$, where V_A and V_B are the dc-link voltages and n is the transformer turns ratio.

When $d = 1$, PSM achieves zero-voltage switching (ZVS) in all switch turn-on transitions over the whole power range [1]. However, when $d \neq 1$, the transformer rms current increases significantly compared to the case $d = 1$ (for the same transferred power) and ZVS is limited to high powers, hence leading to higher conduction and switching losses, and lower efficiency, especially at low loads [4], [5].

Each DAB full bridge can also generate a zero transformer voltage, which represents two additional degrees of freedom (DoF) to improve the DAB efficiency. Several modulations have been defined taking advantage of these DoF.

References [5]–[7] present modulation strategies using only one of the above additional DoF in order to reduce the conduction losses (within transformer and semiconductor devices) and switching losses for $d \neq 1$. Switching losses are typically

Manuscript received December 9, 2014; revised March 28, 2015 and June 7, 2015; accepted August 11, 2015.

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This work has been supported by the Ministerio de Economía y Competitividad, Spain, under Grant DPI2014-54435-P.

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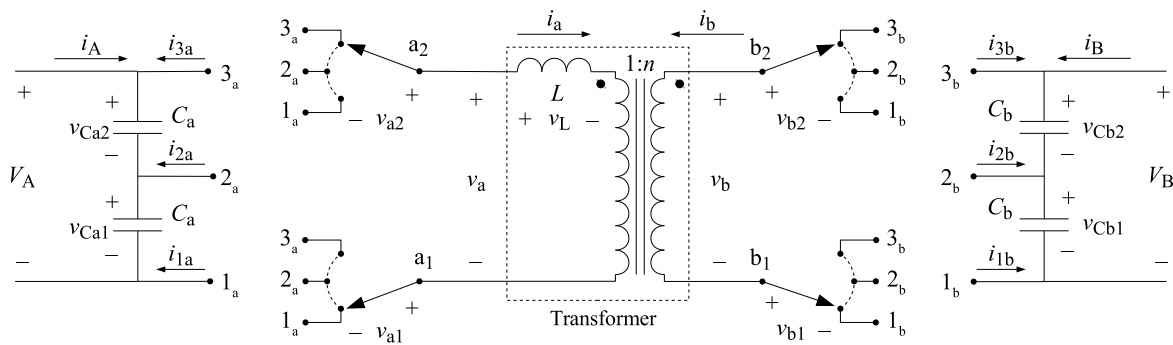


Fig. 1. Topology of the proposed 3L dual-active-bridge dc-dc converter with phase legs a_1 , a_2 , b_1 , and b_2 depicted as single-pole triple-throw switches.

reduced either by minimizing a suitably defined objective function or by extending the ZVS operating range.

References [4], [8], [9] present modulation strategies using both of the above additional DoF. This leads to improved results compared to the previous set of modulation strategies [4], [8]. For instance, [9] proposes a triangular current modulation and a trapezoidal current modulation (TRM-TZM), where the transformer current is actively shaped in order to gain zero-current switching transitions at low loads, which helps reducing the switching losses. On the other hand, [4] studies the minimum transformer rms current solution and the results reveal that the optimum modulation strategy tends to the triangular current modulation for low powers and PSM for high powers. For medium powers, a transitional modulation is defined.

A possible path to increase the available DoF to further improve the DAB performance is to introduce multilevel (ML) topologies in the DAB structure. Moreover, ML topologies [10] offer several additional advantages. On one hand, for a given power rating and semiconductor technology, they allow operating at higher dc voltages, which allows increasing the conversion efficiency. On the other hand, for a given dc-link voltage rating, they allow operating with lower-voltage-rated devices with better performance features, reduce both switching and conduction losses, reduce the total harmonic distortion of voltage and current waveforms, and improve the converter fault-tolerance capacity.

References [11]–[15] introduce three-level (3L) neutral-point-clamped-type legs into the DAB topology, but only [15] addresses the dc-link capacitor voltage balancing, which is a critical issue when the multiple voltage levels are generated through a simple series connection of capacitors. Reference [15] proposes a novel modulation and control scheme to achieve capacitor voltage balancing for the topology shown in Fig. 1, verified via simulation.

This paper is a revision and an extension of [15], including the following new contributions: the analysis of the effect of the transformer current harmonics into the capacitor voltage balancing, the optimization of the modulation strategy parameter values in order to minimize the converter losses, and the experimental verification of both the optimized modulation strategy and the capacitor voltage balancing control.

The paper is organized as follows. Section II presents the fundamentals of the modulation strategy. Section III presents

the capacitor voltage balancing control, where the effect of the transformer current harmonics into the capacitor voltage balancing is discussed. Section IV presents the performance optimization study and proposes a practical solution for the modulation strategy parameters based on the results. Section V presents simulation and experimental results to verify the modulation and control performance, and Section VI outlines the conclusions.

II. MODULATION

Fig. 2 represents the two leg voltages of a full bridge made up of 3L legs in the most general case, assuming a single connection to the top and bottom voltage levels per switching cycle. To force that the average value of v_z equals zero (where $z \in \{a, b\}$), it is necessary that $v_{Cz2} \cdot \delta_{z1} - v_{Cz1} \cdot \delta_{z3} = v_{Cz2} \cdot \delta_{z4} - v_{Cz1} \cdot \delta_{z6}$. This leaves us with 6 DoF (independent variables) in each converter full bridge (e.g., $\delta_{z1}, \delta_{z2}, \delta_{z3}, \delta_{z4}, \delta_{z5}, \phi_z$) leading to a total of 13 DoF in the full converter when considering the phase-shift between v_a and v_b . In this study, to force a symmetrical operation of both legs, it is set $\delta_{z4} = \delta_{z1}$, $\delta_{z5} = 360^\circ - (\delta_{z1} + \delta_{z2} + \delta_{z3})$, and $\delta_{z6} = \delta_{z3}$. Four DoF remain in each converter full bridge ($\delta_{z1}, \delta_{z2}, \delta_{z3}, \phi_z$) leading to a total of 9 DoF in the full converter when considering the phase-shift between v_a and v_b . For convenience, the nine DoF are represented by a new set of independent variables ($\alpha_{ao1}, \alpha_{ao2}, \alpha_{ai1}, \alpha_{ai2}, \alpha_{bo1}, \alpha_{bo2}, \alpha_{bi1}, \alpha_{bi2}, \varphi$), depicted in Fig. 3, where the switching angles boundary values are

$$\begin{aligned} 0^\circ &\leq \alpha_{zi1} \leq \alpha_{zi2} \leq 90^\circ \\ 0^\circ &\leq \alpha_{zo1} \leq \alpha_{zo2} \leq 90^\circ. \end{aligned} \quad (1)$$

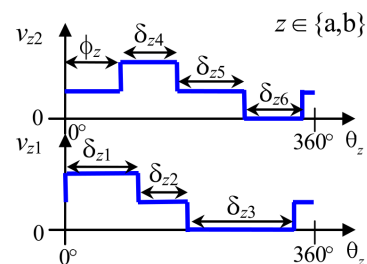


Fig. 2. Analysis of maximum DoF in a 3L DAB.

In Fig. 3, it is shown that with the proposed modulation scheme, a maximum of five-levels are generated in v_z voltage waveform. v_z has a fixed switching-state sequence (v_a switching-state sequence can be seen on top of Fig. 3). The switching states are represented as $(xy)_z$, where $x, y \in \{1, 2, 3\}$ indicate the z -side dc-link point to which nodes z_2 and z_1 are connected, respectively.

Two out of the four DoF in each converter full bridge ($\alpha_{z11} - \alpha_{z01}$ and $\alpha_{z12} - \alpha_{z02}$) affect the capacitor voltage balancing and therefore have to be reserved for the capacitor voltage balancing control. The remaining two DoF ($\alpha_{z1} = (\alpha_{z11} + \alpha_{z01})/2$ and $\alpha_{z2} = (\alpha_{z12} + \alpha_{z02})/2$) can be used to optimize the converter performance. Under capacitor voltage balance, it should be typically verified that

$$\begin{aligned} \alpha_{z01} &= \alpha_{z11} = \alpha_{z1} \\ \alpha_{z02} &= \alpha_{z12} = \alpha_{z2}. \end{aligned} \quad (2)$$

As in the 2L DAB, the fundamental components of voltages v_a and v_b are phase shifted φ degrees, hence building a current i_a in the leakage inductance L of the transformer. Assuming (2), the magnitude of φ determines the amount of power being transferred and the sign of φ determines the direction; i.e., for $\varphi > 0$ power flows from a-side to b-side and for $\varphi < 0$ the power flows in the opposite direction.

It should be noted that, in any case, v_z voltage waveform has odd symmetry ($v_z(\theta_z) = -v_z(-\theta_z)$). Assuming (2), v_z also presents half-wave symmetry and even-order harmonics are eliminated in v_a , v_b , v_L , and i_a waveforms. Then, the transformer voltages and currents can be defined in terms of their different harmonics as

$$\begin{aligned} v_z &= \sum_{h=1,3,5,\dots} [|\mathbf{V}_{z,h}| \cdot \sin(h \cdot \theta_a + \arg(\mathbf{V}_{z,h}))] \\ i_a &= -n \cdot i_b = \sum_{h=1,3,5,\dots} [|\mathbf{I}_{a,h}| \cdot \sin(h \cdot \theta_a + \arg(\mathbf{I}_{a,h}))] \end{aligned} \quad (3)$$

where h is the harmonic number, $\mathbf{V}_{z,h}$ and $\mathbf{I}_{a,h}$ are the voltage and current harmonic h phasors,

$$\begin{aligned} \mathbf{V}_{a,h} &= V_{a,h} + j \cdot 0 \\ \mathbf{V}_{b,h} &= V_{b,h} (\cos(h \cdot \varphi) - j \cdot \sin(h \cdot \varphi)) \\ V_{z,h} &= \frac{2V_Z}{\pi h} \left[\cos(h(90^\circ - \alpha_{z1})) + \cos(h(90^\circ - \alpha_{z2})) \right] \\ \mathbf{I}_{a,h} &= (\mathbf{V}_{a,h} - \mathbf{V}_{b,h}/n) / \mathbf{X}_{L,h} \\ \mathbf{X}_{L,h} &= j(2\pi \cdot h \cdot f_s \cdot L), \end{aligned} \quad (4)$$

$|V_{z,h}|$ is the peak value of the amplitude of harmonic $v_{z,h}$, $Z \in \{A, B\}$, n is the transformer turns-ratio, and f_s is the switching frequency.

The transferred power considering a lossless system is

$$P = \frac{1}{2} \sum_{h=1,3,5,\dots} \|\mathbf{V}_{a,h}\| \cdot \|\mathbf{I}_{a,h}\| \cdot \cos(\arg(\mathbf{V}_{a,h}) - \arg(\mathbf{I}_{a,h})). \quad (5)$$

If $P > 0$, then power is transferred from a-side to b-side, and vice-versa if $P < 0$.

The maximum power that can be transferred for a given V_A and V_B/n , is defined by (5) when $\alpha_{z1} = \alpha_{z2} = 90^\circ$, $\forall z$, and $\varphi = 90^\circ$.

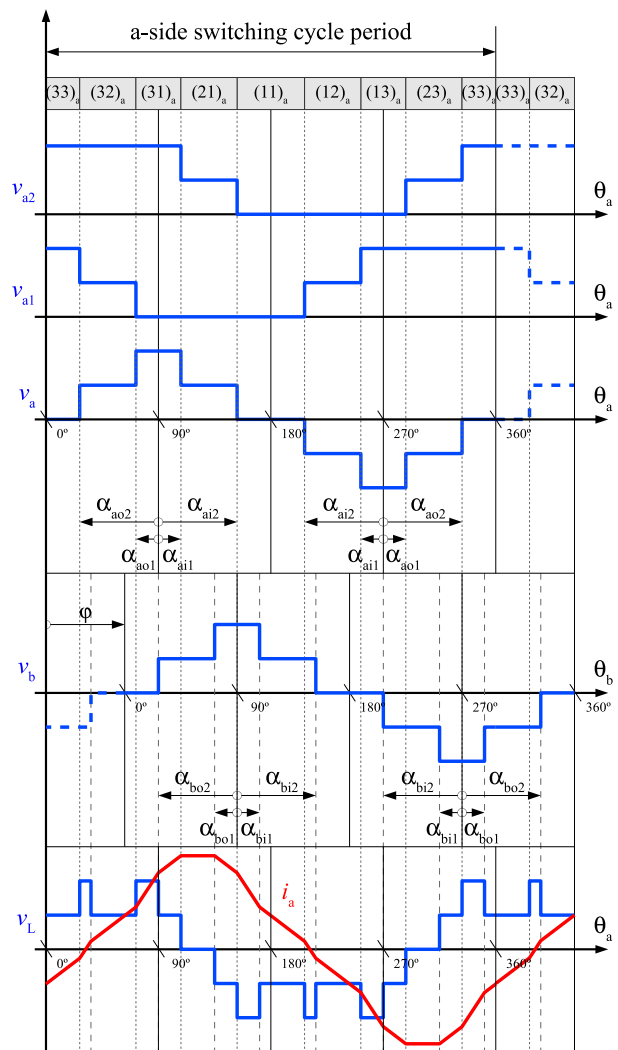


Fig. 3. Voltage waveforms v_{a1} , v_{a2} , v_a , v_b , and v_L , and current waveform i_a for the proposed modulation. Switching states for a-side are shown on top of the figure. All waveforms are plotted assuming $V_A = V_B/n$.

Equations (3) to (5) are used in Section IV, considering all harmonics up to order $h = 63$.

III. CAPACITOR VOLTAGE BALANCING

Fig. 4 shows two examples of the capacitor voltage behavior under the absence of a closed-loop control. In Fig. 4(a) an initial a-side capacitor voltage unbalance is assumed and in Fig. 4(b) a small perturbation in a-side switching angles is introduced to account for switch and gate driver non-idealities (parameter dispersion, etc). Both cases lead to unacceptable capacitor voltage oscillations over long periods of time and even permanent unbalances that could destroy the devices due to an excessive blocking voltage, besides leading to non-optimal operating conditions. Therefore, a closed-loop capacitor voltage balancing control is required.

Capacitor voltage unbalance in voltage-source ML converters is an important issue [10] and many solutions have been proposed for modulations with high switching-to-fundamental frequency ratios. However, the proposed modulation does not

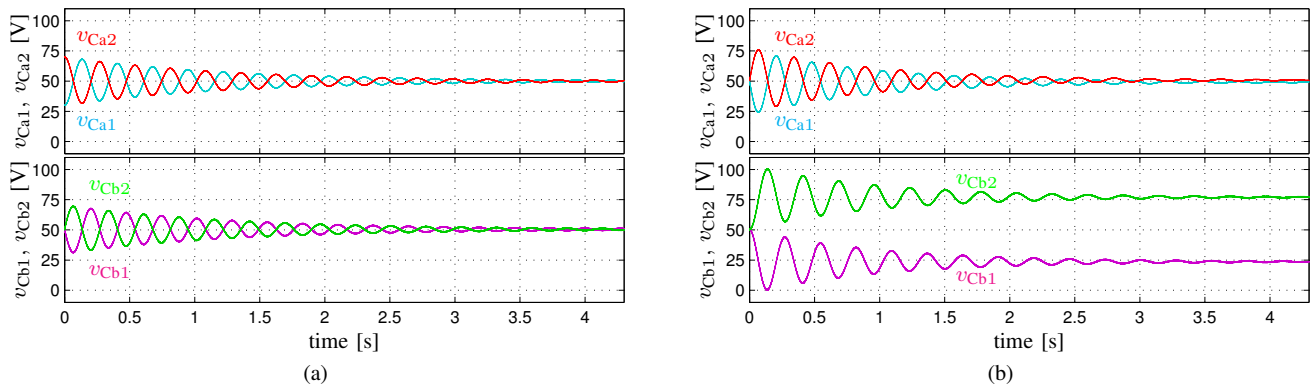


Fig. 4. Simulation results for v_{Ca1} , v_{Ca2} , v_{Cb1} , and v_{Cb2} under the following conditions: $V_A = 100$ V, $C_z = 100$ μ F, b-side load resistance $R_B = 58.1$ Ω , and $\varphi = 60^\circ$. (a) Transient response with an initial a-side unbalance ($v_{Ca1}(0) = 40$ V, $v_{Ca2}(0) = 60$ V) and $\{\alpha_{zi1}, \alpha_{zo1}, \alpha_{zi2}, \alpha_{zo2}\} = \{30^\circ, 30^\circ, 60^\circ, 60^\circ\}, \forall z$. (b) Transient response with a small perturbation in a-side switching angles ($\{\alpha_{ai1}, \alpha_{ao1}, \alpha_{ai2}, \alpha_{ao2}\} = \{28^\circ, 32^\circ, 62^\circ, 58^\circ\}, \{\alpha_{bi1}, \alpha_{bo1}, \alpha_{bi2}, \alpha_{bo2}\} = \{30^\circ, 30^\circ, 60^\circ, 60^\circ\}$).

fall into this category, and hence a new control scheme has to be designed.

A. Control Operating Principle and Control Scheme

The current injected into or drawn from the neutral point of the dc-link alters the ratio between the two dc-link capacitor voltages. This current is

$$i_{2z} = S_{z12} \cdot i_z - S_{z22} \cdot i_z, \quad (6)$$

where S_{zj2} is equal to 1 when leg z_j is connected to dc-link point 2_z , and 0 otherwise.

To preserve the capacitor balance, the total charge injected into the neutral point within a switching cycle has to be equal to zero.

Let us first consider the effect of the fundamental component of i_z ($i_{z,1}$), as its amplitude is greater than each of the harmonic amplitudes. Current $i_{z,1}$ can be decoupled into a $i_{z,1}^p$ component, in phase with $v_{z,1}$ (the fundamental component of v_z), and into a $i_{z,1}^q$ component, in quadrature with $v_{z,1}$. This can be mathematically expressed as

$$\begin{aligned} v_{z,1} &= V_{z,1} \cdot \sin(\theta_z) \\ i_{z,1} &= i_{z,1}^p + i_{z,1}^q = I_{z,1}^p \cdot \sin(\theta_z) + I_{z,1}^q \cdot \cos(\theta_z). \end{aligned} \quad (7)$$

Currents $i_{z,1}^p$ and $i_{z,1}^q$ are depicted in Fig. 5, together with v_z . The shaded areas in Fig. 5 represent the electrical charge injected into (positive sign) or drawn from (negative sign) the z -side dc-link neutral point by these currents. If (2) is verified (i.e., there is quarter-wave symmetry), the total charge injected into the neutral point by both currents is zero for a whole switching cycle. However, if a voltage unbalance exists, the inner ($\alpha_{zi1}, \alpha_{zi2}$) and outer angles ($\alpha_{zo1}, \alpha_{zo2}$) can be modified in order to inject or draw a non-zero charge during a switching cycle. This charge will only be provided by $i_{z,1}^p$ since the total charge injected by $i_{z,1}^q$ is zero thanks to the odd-symmetry of v_z .

Fig. 6 shows the proposed control scheme for the capacitor voltage balancing. This control scheme modifies the initial switching angles (α_{z1}, α_{z2}) on a per-unit basis by means of control variable u_z , resulting from the processing of error

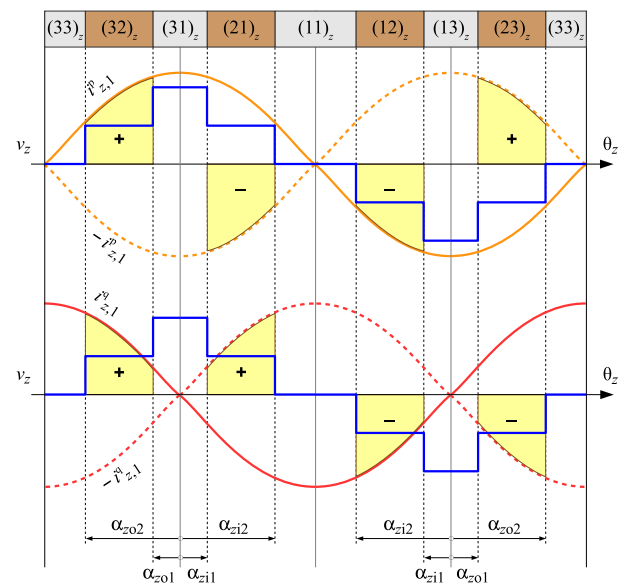


Fig. 5. Voltage v_z and the in-phase and in-quadrature components of i_z fundamental component ($i_{z,1}^p$ and $i_{z,1}^q$). The yellow areas depict the injected (+) or drawn (-) charge from the z -side dc-link neutral point by $i_{z,1}^p$ and $i_{z,1}^q$.

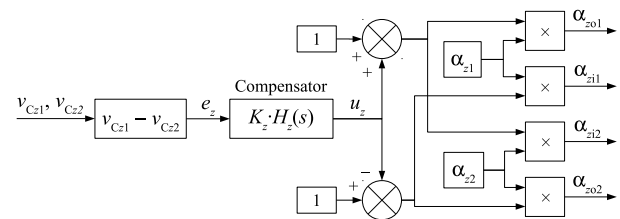


Fig. 6. Control scheme for the capacitor voltage balancing.

variable e_z by the compensator transfer function ($K_z \cdot H_z(s)$). Additional details can be found in [15].

B. Influence of the Transformer Current Harmonics on the Capacitor Voltage Balancing

Current i_z will typically contain non-negligible harmonics. Their effect on the capacitor voltage balancing needs to be

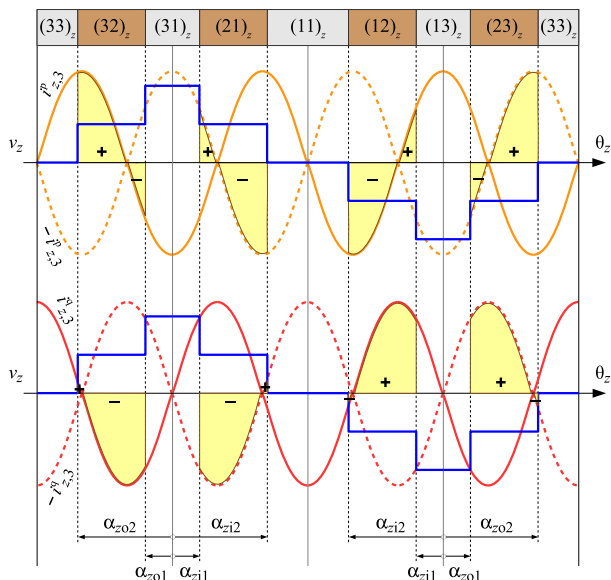


Fig. 7. Voltage v_z and the in-phase and in-quadrature components of i_z 3rd harmonic ($i_{z,3}^p$ and $i_{z,3}^q$). The yellow areas depict the injected (+) or drawn (-) charge from the z -side dc-link neutral point by $i_{z,3}^p$ and $i_{z,3}^q$.

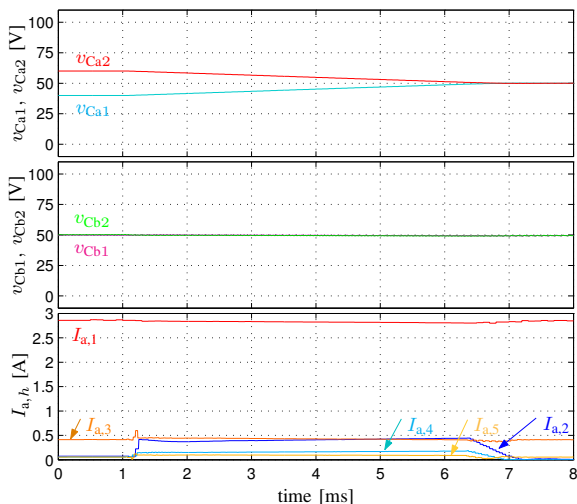


Fig. 8. Simulation results for v_{Ca1} , v_{Ca2} , v_{Cb1} , and v_{Cb2} and the amplitude of the first five harmonics of i_a during a capacitor voltage balance recovery transient starting at $t = 1$ ms. Conditions: $\alpha_{z1} = 60^\circ$, $\alpha_{z2} = 80^\circ$, $\forall z$; $V_A = 100$ V, $R_B = 60 \Omega$, and a steady-state $\varphi = 26.4^\circ$.

assessed.

As an example, Fig. 7 depicts the charge injected into or drawn from the neutral point by the in-phase and in-quadrature components of the third harmonic of i_z ($i_{z,3}^p$ and $i_{z,3}^q$, respectively), when v_z has quarter-wave symmetry.

The odd symmetry of v_z guarantees that for all harmonics, the in-quadrature component of the current ($i_{z,h}^q$), does not affect the capacitor voltage balancing. On the other hand, the half-wave symmetry of v_z guarantees that for all harmonics (in this case, only odd harmonics are present), the in-phase component of the current ($i_{z,h}^p$), does not affect the capacitor voltage balancing.

According to the modulation pattern presented in Fig. 3, voltage v_z will always present odd symmetry. Therefore, $i_{z,h}^q$

will never affect the capacitor voltage balancing. If in addition to odd symmetry, voltage v_z presents half-wave symmetry (i.e., v_z presents quarter-wave symmetry), then neither the i_z fundamental component nor any harmonic will affect the capacitor voltage balancing. This can be verified in the case of the third harmonic presented in Fig. 7. When the capacitor voltage balance is lost, the control action will force that v_z loses its half-wave symmetry, preserving only odd-symmetry. In this case, the in-phase fundamental component of i_z and the in-phase component of all i_z harmonics will introduce a non-zero charge into the neutral point, affecting the capacitor voltage balance. However, since the fundamental component amplitude is typically much larger than the harmonic amplitudes, it can be reasonably assumed that the fundamental component effect will be larger than the joint effect of all other harmonic currents. The presented control is based on this assumption. As an example, Fig. 8 presents the amplitude of the first harmonics of i_a during a capacitor voltage balance recovery transient. All harmonic amplitudes always remain much lower than the fundamental component amplitude, and the proposed voltage balancing control operates well and is able to quickly recover the balance of a-side capacitor voltages without perturbing the balance of b-side capacitor voltages.

IV. PERFORMANCE OPTIMIZATION

Five DoF are available to force the desired power transfer and optimize the converter performance: α_{a1} , α_{a2} , α_{b1} , α_{b2} , and φ . Variable φ is typically determined by the output voltage closed-loop control and controls the power transfer. Therefore, simple closed-form expressions of α_{a1} , α_{a2} , α_{b1} , and α_{b2} as a function of φ that provided good performance in most cases would be highly desirable to define a general-purpose practical modulation that takes advantage of the available DoF. The final goal of this section is to propose such modulation pattern.

The main performance figure of the DAB converter is the efficiency. As shown in [16], [17], transformer copper losses and switch conduction and switching losses on the 2L DAB, represent an 80-90 % of the total losses. It seems reasonable to assume that these losses are also predominant on the presented 3L DAB. Ideally, one would like to find out the values of the modulation parameters (α_{a1} , α_{a2} , α_{b1} , α_{b2} , and φ) that minimize the addition of all these losses on every converter working point, defined by $\{V_A, V_B, P\}$. However, this global optimum is strongly dependent on the constructive and operating parameters of the converter, which define different relative weights on the loss components.

In order to gain insight into the global optimization problem from a general perspective, it is decoupled into three simpler optimization problems. Three different objective functions that only depend on the transformer current values, one associated to conduction losses and the remaining two associated to switching losses, are defined. Each of the three optimization problems leads to a different optimal solution, but from the analysis of their common features, a set of practical closed-form expressions to obtain the modulation parameters for every operating point, providing good performance (in general), is finally proposed.

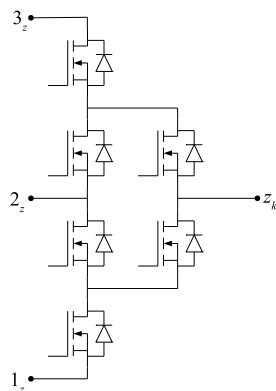


Fig. 9. MOSFET-based 3L active neutral-point-clamped leg used to implement legs a_1 , a_2 , b_1 , and b_2 .

The proposed modulation and capacitor voltage balancing control can be applied with any leg topology functionally equivalent to a single-pole triple-throw switch built upon any suitable set of semiconductor devices, operated at any voltage and current levels, and any switching frequency. However, for the sake of model simplicity and convenience in the experimental implementation, it will be assumed that legs a_1 , a_2 , b_1 , and b_2 are implemented using 3L active neutral-point-clamped legs built upon metal-oxide semiconductor field-effect transistors (MOSFET) (Fig. 9). The legs are operated according to [18], which guarantees a blocking voltage of $V_Z/2$ on each switch.

A. Objective Function Associated to Conduction Losses

The conduction losses in the transformer windings and MOSFETs (mainly conducting through the MOSFET channel) are essentially proportional to the square of the transformer rms current, $I_{a,rms}^2$. Hence, in order to minimize these losses, objective function

$$F_1 = I_{a,rms} = \sqrt{\frac{1}{2} \sum_{h=1,3,5,\dots} \|I_{a,h}\|^2} \quad (8)$$

is defined.

B. Objective Functions Associated to Switching Losses

In the topology of Fig. 9, the leg output terminal is connected to one of the three dc-link terminals or levels. In the transition between adjacent levels, some switches turn off and some others turn on. The switching losses will be concentrated on the first switch turning on or the last switch turning off, depending on the leg output-current direction. Let us designate as Type I the transitions where the losses are concentrated on a switch turning on (and on the associated turning-off diode), and Type II the transitions where the losses are concentrated on a switch turning off.

Regardless of the type of switching transition, in a first approximation, assuming ideal diodes and small parasitic drain-to-source capacitances, the energy lost in a transition between adjacent levels can be modeled as in [19],

$$E_{sw} = \frac{V_Z/2 \cdot I_{sw}^2}{2 \cdot s_i} + \frac{(V_Z/2)^2 \cdot |I_{sw}|}{2 \cdot s_v}, \quad (9)$$

where I_{sw} is the current being switched and s_i , s_v are the current and voltage transition slopes, respectively, which are assumed to be constant during a transition and independent of I_{sw} and V_Z .

With the previous assumptions, E_{sw} is obtained as the addition of $|I_{sw}|$ and I_{sw}^2 with different weighting factors. These weighting factors are unknown because they depend on the specific device selection and other converter implementation details. Therefore, following the optimization problem decoupling approach explained above, two different switching-losses-related objective functions can be proposed: one involving the addition of $|I_{sw}|$ for all leg level transitions within a switching cycle and another one involving the addition of I_{sw}^2 for all leg level transitions within a switching cycle.

However, if real diodes are considered, the losses in Type I transitions increase due to diode reverse recovery. In addition, the losses in Type II transitions can be very small for small currents. Thus, this implies a higher penalty for Type I transitions compared to Type II. This is reflected in the final proposed objective functions

$$\begin{aligned} F_2 &= \sum_{T_s} |I_{sw,I}| + K \cdot \sum_{T_s} |I_{sw,II}| \\ F_3 &= \sum_{T_s} I_{sw,I}^2 + K \cdot \sum_{T_s} I_{sw,II}^2, \end{aligned} \quad (10)$$

where $I_{sw,I}$ and $I_{sw,II}$ are equal to the transition current for Type I and Type II transitions, respectively, in each phase leg and within a switching cycle, and constant $K \in]0, 1[$ is introduced in order to prioritize the minimization of Type I transition losses in front of Type II transition losses. A value of $K = 0.1$ will be considered throughout the paper.

C. Optimization Process

Objective functions F_1 , F_2 , and F_3 are minimized independently using the numerical computation algorithms provided by Matlab's Global Optimization Toolbox. The optimization problems are

$$\min(F_f) = F_f(X_f), \quad (11)$$

where $f \in \{1, 2, 3\}$ and $X_f = \{\alpha_{a1}, \alpha_{a2}, \alpha_{b1}, \alpha_{b2}, \varphi\}_f$ is F_f optimum solution at a given operating point defined by V_A^* , V_B^* , and P^* .

The constraint equations are

$$\begin{cases} 0^\circ \leq \alpha_{z1} \leq \alpha_{z2} \leq 90^\circ \\ 0^\circ \leq \varphi \leq 90^\circ \\ P = P^*. \end{cases} \quad (12)$$

The optimum F_f switching angles $\{\alpha_{a1}, \alpha_{a2}, \alpha_{b1}, \alpha_{b2}\}_f$ for each working point, are presented in Fig. 10 as a function of F_f optimum phase shift ($\{\varphi\}_f$). In all cases, P increases monotonically and non-linearly as $\{\varphi\}_f$ increases.

The optimum switching angles present certain patterns that are similar among all F_f . First, in each F_f , a symmetry can be identified between a- and b-side optimum switching angles, that can be expressed as $\{\alpha_{a1}, \alpha_{a2}\}_f|_d = \{\alpha_{b1}, \alpha_{b2}\}_f|(1/d)$. Second, in all F_f solutions, for $d \neq 1$, α_{z1} begins at nearly 0° and increases, and α_{z2} begins at nearly 90° and decreases.

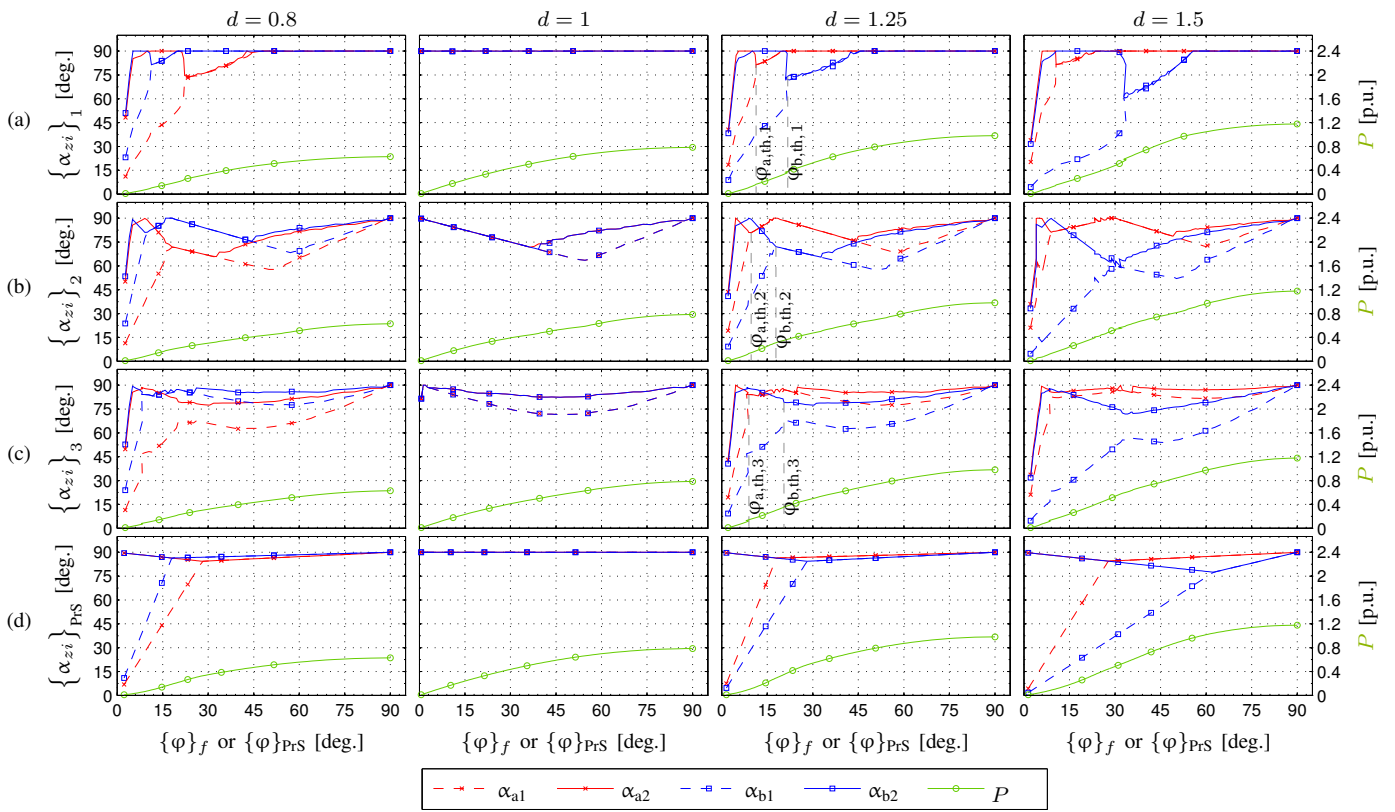


Fig. 10. Switching angle values (left axis on each subfigure) and transferred power (right axis) as a function of phase shift. (a) Solution that minimizes F_1 . (b) Solution that minimizes F_2 . (c) Solution that minimizes F_3 . (d) Proposed practical solution.

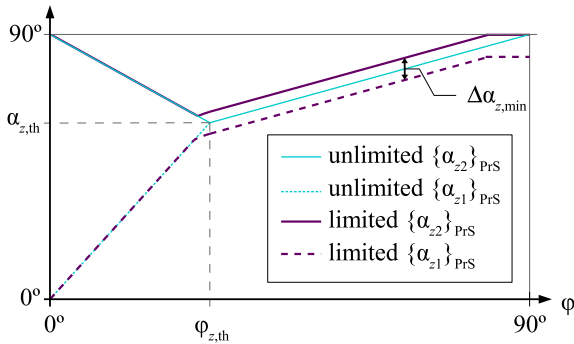


Fig. 11. Practical switching angles as a function of φ .

Both angles present a trend change at approximately the same phase shift value ($\varphi_{z,th,f}$ in Fig. 10). Eventually, they both increase until reaching 90° . $\varphi_{z,th,f}$ is equal to 0° when $d = 1$, and increases as d departs from 1. For $d > 1$, $\varphi_{a,th,f} < \varphi_{b,th,f}$, and for $d < 1$, $\varphi_{a,th,f} > \varphi_{b,th,f}$.

It is interesting to note that for $d = 1$ the optimum solution for F_1 sets all switching angles to 90° , producing pure square voltage waveforms in v_a and v_b as in a conventional 2L DAB operated with PSM. This occurs because in this case, for a given transferred power value, maximizing the amplitude of v_a and v_b fundamental components minimizes the required transformer rms current value, therefore minimizing conduction losses. This is consistent with previous studies on the 2L DAB case [4].

D. Practical Solution

The optimal switching angles as a function of φ of the three formulated optimization problems shown in Fig. 10, present a common pattern, as discussed above. Fig. 11 aims to reproduce this pattern through the plot of the unlimited variables $\{\alpha_{z1}, \alpha_{z2}\}_{PrS}$. These are the switching angles defined by our proposed practical solution, which can be expressed as

$$\{\alpha_{z1}\}_{PrS} = \begin{cases} 0^\circ + \frac{\alpha_{z,th}}{\varphi_{z,th}} \cdot \varphi, & \varphi < \varphi_{z,th} \\ \alpha_{z,th} + \frac{90^\circ - \alpha_{z,th}}{90^\circ - \varphi_{z,th}} (\varphi - \varphi_{z,th}), & \varphi \geq \varphi_{z,th} \end{cases}$$

$$\{\alpha_{z2}\}_{PrS} = \begin{cases} 90^\circ - \frac{90^\circ - \alpha_{z,th}}{\varphi_{z,th}} \cdot \varphi, & \varphi < \varphi_{z,th} \\ \alpha_{z,th} + \frac{90^\circ - \alpha_{z,th}}{90^\circ - \varphi_{z,th}} (\varphi - \varphi_{z,th}), & \varphi \geq \varphi_{z,th}, \end{cases} \quad (13)$$

where

$$\begin{cases} \varphi_{a,th} = K_{\varphi,th} \cdot |1 - 1/d^2| \\ \varphi_{b,th} = K_{\varphi,th} \cdot |1 - d^2| \\ \alpha_{z,th} = 90^\circ - K_{\alpha,th} \cdot \varphi_{z,th} \end{cases} \quad (14)$$

and $K_{\varphi,th}$ is a constant that forces a $\varphi_{z,th}$ value close to $\varphi_{z,th,f}$ in Fig. 10 for all the considered d values in the optimization process. To guarantee the converter capability to transfer maximum power, $\varphi_{z,th}$ has to be limited to $\varphi_{max} < 90^\circ$. From (14), it can be derived that for

$$d \in \left[(1 + \varphi_{max}/K_{\varphi,th})^{-\frac{1}{2}}, (1 + \varphi_{max}/K_{\varphi,th})^{\frac{1}{2}} \right], \quad (15)$$

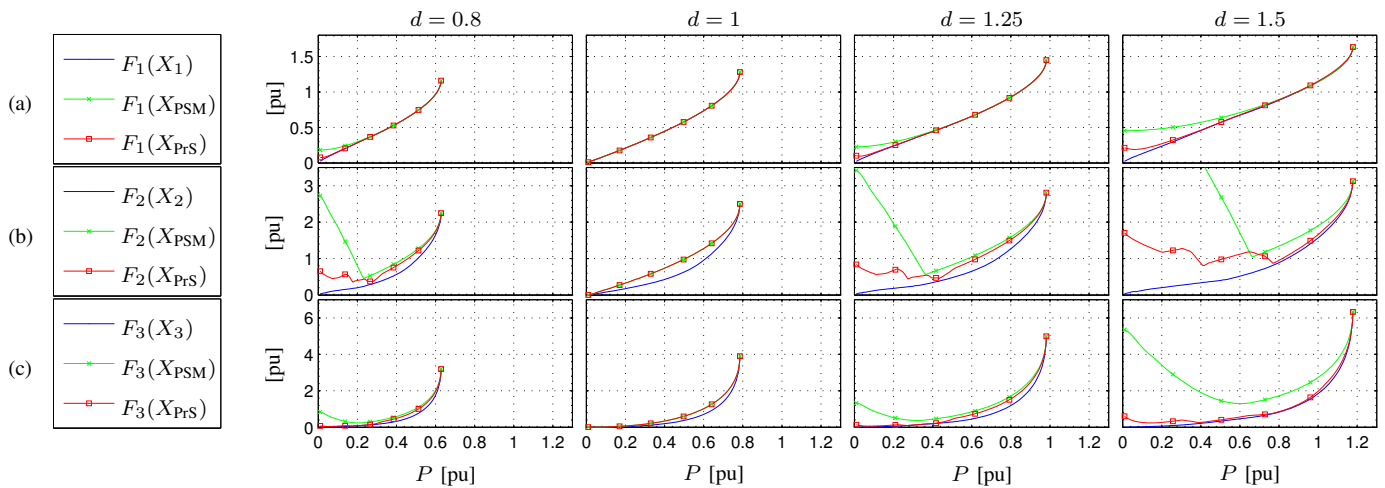


Fig. 12. Objective function values as a function of P for solutions X_f , X_{PrS} , and X_{PSM} . (a) F_1 . (b) F_2 . (c) F_3 .

then $\varphi_{z,th} \leq \varphi_{max}$. Otherwise, for d values outside this range, the maximum value of $\varphi_{z,th} = \varphi_{max}$ will have to be enforced. For instance, if $K_{\varphi,th} = 50^\circ$, $K_{\alpha,th} = 0.2$, and $\varphi_{max} = 80^\circ$, the range defined in (15) is $d \in [0.62, 1.61]$. Fig. 10(d) presents the practical angle values for the previous set of practical solution parameter values, which provide a good approximation of the optimum solutions.

In practice, the required blanking time (t_b) between the turn-off of a switch and the turn-on of another in a switching transition, forces a minimum margin between α_{z1} and α_{z2} , defined as

$$\Delta\alpha_{z,min} = \alpha_{z2} - \alpha_{z1} = t_b \cdot f_s \cdot 360^\circ. \quad (16)$$

This restriction is illustrated in the limited $\{\alpha_{z1}, \alpha_{z2}\}_{PrS}$ in Fig. 11.

The above modulation strategy can be implemented into a single field-programmable gate array (FPGA) together with the capacitor voltage balancing control and the output dc-link voltage control.

E. Comparison of the Practical Solution and F_1 , F_2 , F_3 Optimum Solutions

To evaluate the suitability of the proposed practical solution, the value of the objective functions obtained with the unlimited practical solution, illustrated in Fig. 10(d), ($F_f(X_{PrS})$) are compared with the optimum values of the objective functions ($F_f(X_f)$) and with the values of the objective functions obtained when using the PSM in the present converter ($F_f(X_{PSM})$). These results are presented in Fig. 12 as a function of P . Solution X_{PSM} , $\forall d$, is the same as the practical solution for $d = 1$, shown in Fig. 10(d).

The base voltage, current, and power values are

$$\begin{aligned} V_{base} &= V_A \\ I_{base} &= V_A / (2\pi f_s \cdot L) \\ P_{base} &= V_A^2 / (2\pi f_s \cdot L). \end{aligned} \quad (17)$$

As it can be observed in Fig. 12(a), $F_1(X_{PrS})$ is very close to the minimum possible value ($F_1(X_1)$) and is lower than

$F_1(X_{PSM})$, especially at low-to-medium powers. Only for very low powers, $F_1(X_{PrS})$ is not close to the minimum.

In Fig. 12(b), for low-to-medium powers, $F_2(X_{PrS})$ is greater than the minimum ($F_2(X_2)$) but significantly lower than $F_2(X_{PSM})$. These differences increase for $d \ll 1$ and $d \gg 1$.

In Fig. 12(c), $F_3(X_{PrS})$ is very close to the minimum ($F_3(X_3)$) for the whole d range, and lower than $F_3(X_{PSM})$ for $d \neq 1$ and low-to-medium powers.

In conclusion, the proposed practical solution is expected to achieve lower conduction and switching losses than PSM for low-to-medium powers when $d \neq 1$. Also, if in (9) I_{sw}^2 influence is higher than $|I_{sw}|$ influence due to constructive parameters of the converter, then the switching losses will be very close to the minimum. At high powers and also in all the power range for $d = 1$, both the practical and PSM solutions are close to or equal to the minimum possible conduction and switching losses.

V. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental tests have been carried out to prove the effectiveness of the proposed practical solution. A Matlab-Simulink lossless model of the converter in Fig. 1 is used to perform the simulations. All simulations assume $n = 1$ and $C_z = 100 \mu\text{F}$. Fig. 13 presents the 3L DAB converter prototype used in the experiments, which is implemented using four 3L ANPC legs (Fig. 9) with 100 V - 20 A MOSFETs. The prototype is built with four-level boards where only the six required devices for 3L legs are populated. The control and modulation is implemented using dSpace processor board DS1006 and two synchronized dSpace digital waveform output boards DS5101 (each contains an FPGA). As the selected operating f_s increases, the size of the required passive components (capacitors and transformer) decreases while switching losses increase. For the selected prototype devices, the f_s value that represents a good trade-off solution, maximizing the converter power density, would be relatively high. However, due to control platform limitations, the experimental prototype in Fig. 13 has been designed to operate at $f_s = 10 \text{ kHz}$, which

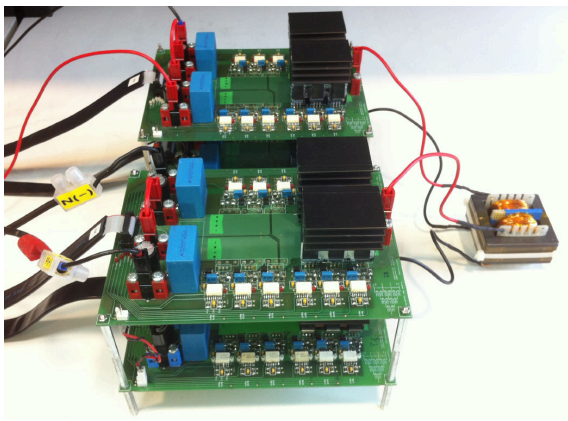


Fig. 13. Three-level DAB prototype. Components: FDPF3860T MOSFETs, $C_z = 103.4 \mu\text{F}$, $n = 1$, $L = 300 \mu\text{H}$, transformer magnetizing inductance $L_m = 12 \text{ mH}$, HCPL-316J gate drivers, and compact and internal gate driver power supply circuits as described in [20].

is the maximum f_s that can be safely reached. The aim of the prototype is to allow an experimental proof of concept, in particular regarding the feasibility of achieving capacitor voltage balancing control.

In all simulations and experiments, a dc voltage source is connected across the a-side dc-link and a resistive load across the b-side dc-link. A simple proportional compensator has been used for the capacitor voltage balancing control presented in Fig. 6. A proportional-integral compensator has been used for the regulation of the load voltage V_B . All compensator parameters have been tuned through simulation and experiments to obtain an acceptable performance and stable behavior.

A. Steady State Results

The converter is controlled at $f_s = 10 \text{ kHz}$ with the proposed limited practical solution presented in Section IV-D and $\Delta\alpha_{z,\min} = 2.52^\circ$, $\forall z$. The balancing control presented in Section III is also enabled. The steady-state behavior at two working points is analyzed: WP1 with $d = 1$ ($V_A = 100 \text{ V}$, $V_B = 100 \text{ V}$) and $\varphi = 60^\circ$; WP2 with $d = 1.5$ ($V_A = 80 \text{ V}$, $V_B = 120 \text{ V}$) and $\varphi = 30^\circ$. Fig. 14 presents the simulation results for the relevant voltage and current waveforms. It can be observed that both dc links have capacitor voltage balance, since v_a and v_b present voltage steps of equal amplitude. The red and green dots indicate when a transition is of Type I or Type II, respectively. Fig. 15 shows the experimental results for the same working points and conditions of Fig. 14. Both the simulation and experimental waveforms are in close agreement. Dc-link capacitor voltage balancing is also achieved.

Table I presents a comparison of the analytical, simulation, and experimental values of the three objective functions for both working points. The results are again fairly similar.

Fig. 16 compares the power loss (P_{loss}) and efficiency (η) of a 3L DAB operated with 100 V MOSFETs (FDPF3860T, on resistance $R_{\text{DS,on}} = 30 \text{ m}\Omega$) and the proposed modulation strategy from Section IV-D and a 2L DAB operated with 200 V MOSFETs (STF20NF20, $R_{\text{DS,on}} = 100 \text{ m}\Omega$) and two possible modulation strategies (PSM and TRM-TZM [9]).

TABLE I
OBJECTIVE FUNCTION VALUES COMPARISON

| | | F_1 | F_2 | F_3 |
|-----|--------------|---------|---------|---------|
| WP1 | Anal. | 0.92 pu | 1.62 pu | 1.64 pu |
| | Sim. | 0.93 pu | 1.62 pu | 1.65 pu |
| | Exp. | 0.95 pu | 1.67 pu | 1.76 pu |
| WP2 | Anal. | 0.56 pu | 0.94 pu | 0.38 pu |
| | Sim. | 0.56 pu | 0.94 pu | 0.38 pu |
| | Exp. | 0.57 pu | 0.81 pu | 0.38 pu |

Only semiconductor device losses (conduction and switching) are considered and a wide operating range at $f_s = 100 \text{ kHz}$ is explored. The comparison has been performed combining simulation and experimental data. The system is simulated in MATLAB-Simulink. Conduction losses are then calculated from the simulated semiconductor current values and the datasheet $R_{\text{DS,on}}$ value. Switching losses are calculated from the simulated current values and the expression in (18). Coefficients a , b , and c depend on the device, the type of switching transition, and the value of the blocking voltage V_{DS} . A suitable set of coefficient values for each different case has been obtained from the switch and diode energy loss during switching transitions experimentally measured using a double pulse board at different blocking voltages V_{DS} , over the full current range up to 16 A, and with a gate resistance $R_g = 6.6 \Omega$. For example, Table II presents the value of these coefficients for the nominal V_{DS} value that together with (18), approximate the experimentally measured losses (in both the switch and diode, at turn-on (E_{on}) and turn-off (E_{off}) transitions, involving one or two diodes ("1d", "2d")) with a coefficient of determination (R^2) higher than 90% for the switch and higher than 70% for the diode. Similar sets of coefficient values have been obtained for $V_{\text{DS}} = \{40, 44.5, 55, 60\} \text{ V}$ for FDPF3860T and $V_{\text{DS}} = \{80, 89, 110, 120\} \text{ V}$ for STF20NF20. For currents below 2 A, a simple linear regression has been applied to compute diode turn-off losses.

$$E_{\text{sw}} = a \cdot I_{\text{sw}}^2 + b \cdot |I_{\text{sw}}| + c \quad [\mu\text{J}]. \quad (18)$$

It can be observed in Fig. 16 that both conduction and switching losses are lower in the 3L DAB case, leading to a higher efficiency.

Table III presents a comparison of the practical solution (PrS) and a global optimum (GO) obtained through the minimization of a function defined by the addition of all converter

TABLE II
SWITCHING LOSS COEFFICIENTS

| | | FDPF3860T @ $V_{\text{DS}} = 50 \text{ V}$ | | | STF20NF20 @ $V_{\text{DS}} = 100 \text{ V}$ | | |
|--------|---------------------|---|--------|-------|--|-------|-------|
| | | a | b | c | a | b | c |
| Switch | $E_{\text{on},1d}$ | 0 | 0.548 | 0 | 0 | 8.059 | 0 |
| | $E_{\text{on},2d}$ | 0 | 0.604 | 0 | - | - | - |
| | $E_{\text{off},1d}$ | 0.046 | -0.192 | 0.398 | 0.088 | 0.053 | 0 |
| | $E_{\text{off},2d}$ | 0.04 | -0.173 | 0.23 | - | - | - |
| Diode | $E_{\text{off},1d}$ | 0 | 0.131 | 2.366 | 0 | 2.466 | 16.55 |
| | $E_{\text{off},2d}$ | 0 | 0.145 | 2.984 | - | - | - |

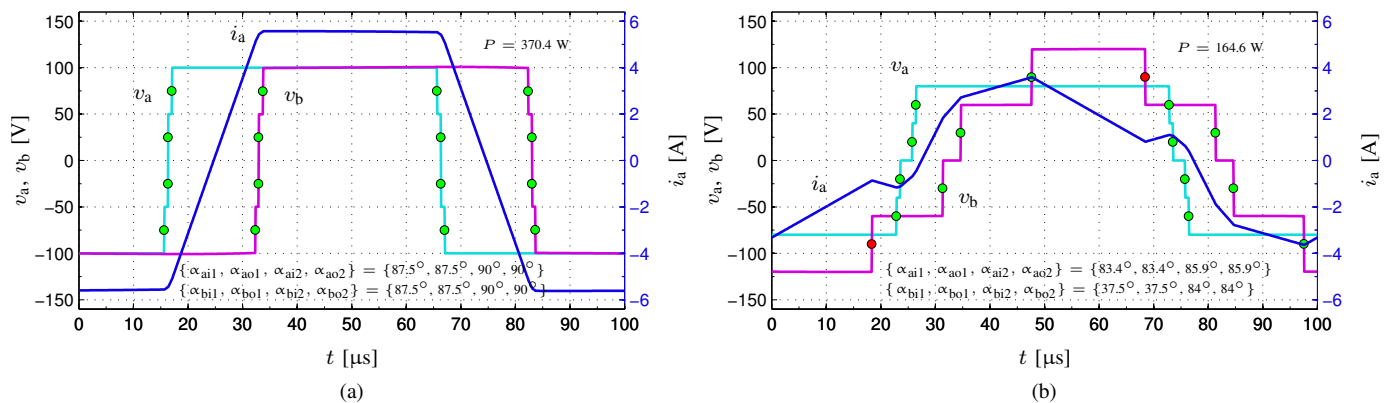


Fig. 14. Simulation results for v_a , v_b , and i_a , using the limited practical solution. (a) WP1. (b) WP2.

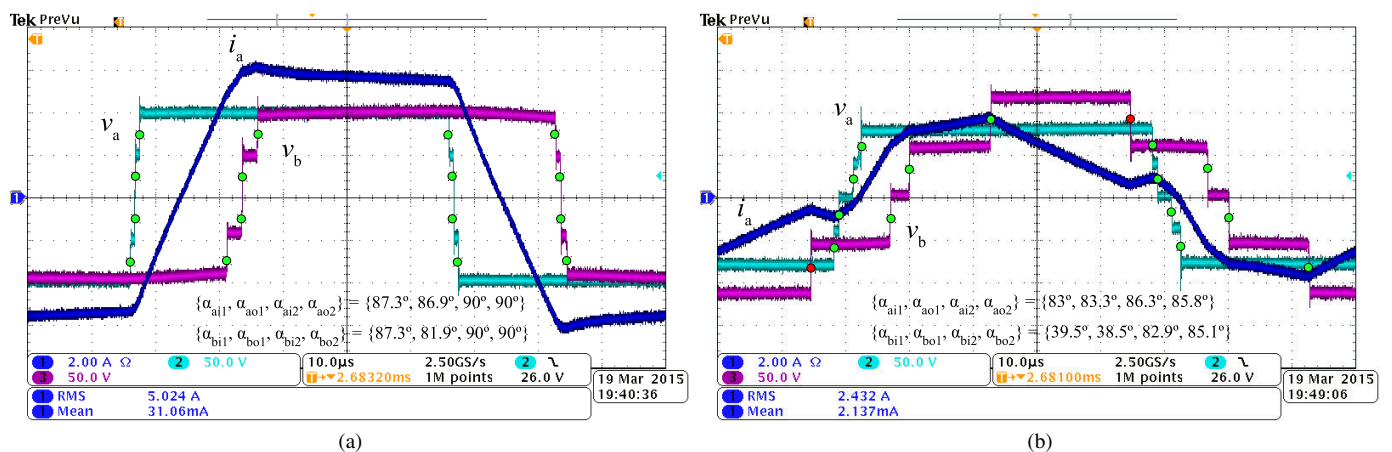


Fig. 15. Experimental results for v_a , v_b , and i_a , using the limited practical solution. (a) WP1. (b) WP2.

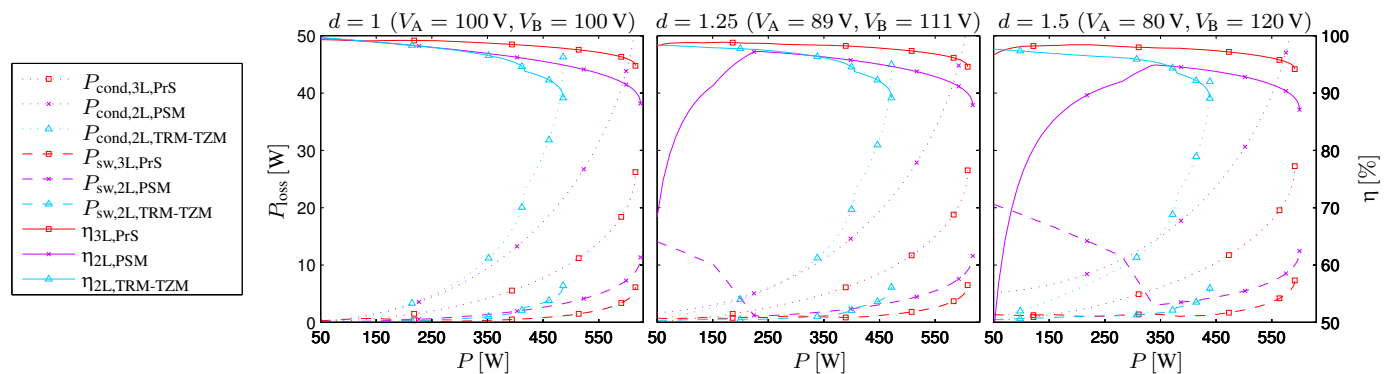


Fig. 16. Comparison of losses and efficiency of a 3L DAB operated with the proposed modulation in Section IV-D and a 2L DAB operated with PSM and TRM-TZM. Conditions: $f_s = 100$ kHz, $L = 20$ μ H, $K_{\varphi,th} = 50$, $K_{\alpha,th} = 0.2$, $\Delta\alpha_{z,min} = 10.8^\circ$, $\forall z$.

semiconductor losses (conduction and switching) in the same conditions as in Fig. 16. The comparison is performed under nine working points. Although differences appear in some switching angles, the efficiency results are in general almost identical except for the cases with $d \neq 1$ and low power levels.

B. Transient Results

Fig. 17 and Fig. 18 present the experimental performance of the system, with the load-voltage V_B control enabled, under different transients: a step in V_B voltage reference (Fig.

17(a)), a step in the load (Fig. 17(b)), and a capacitor voltage balancing transient (Fig. 18). In Fig. 17, all controls perform satisfactorily, keeping the capacitor voltages balanced during the transients. In Fig. 18, an initial unbalance in v_{Cb1} , v_{Cb2} is forced disabling the b-side capacitor voltage balancing control and loading the b-side capacitors with two different resistance values. Once the b-side balancing control is enabled, the capacitor voltage balance is quickly recovered.

Further simulations results proving the effectiveness of the capacitor voltage balancing control can be found in [15].

TABLE III
COMPARISON OF PRACTICAL SOLUTION AND GLOBAL OPTIMUM

| d | P [W] | | α_{a1} | α_{a2} | α_{b1} | α_{b2} | η |
|------|---------|-----|---------------|---------------|---------------|---------------|---------|
| 1 | 100 | PrS | 79.2° | 90° | 79.2° | 90° | 99.17 % |
| | | GO | 79.2° | 90° | 76.6° | 87.4° | 99.2 % |
| | 300 | PrS | 79.2° | 90° | 79.2° | 90° | 98.95 % |
| | | GO | 79.2° | 90° | 79.2° | 90° | 98.95 % |
| | 500 | PrS | 79.2° | 90° | 79.2° | 90° | 97.68 % |
| | | GO | 79.2° | 90° | 79.2° <td 90° | 97.68 % | |
| 1.25 | 100 | PrS | 58.8° | 87.6° | 36.9° | 87.6° | 98.8 % |
| | | GO | 79.2° | 90° | 43.3° | 86.8° | 99.31 % |
| | 300 | PrS | 79.2° | 90° | 77.3° | 88.1° | 98.45 % |
| | | GO | 79.2° | 90° | 66.2° | 90° | 98.58 % |
| | 500 | PrS | 79.2° | 90° | 79.2° | 90° | 97.42 % |
| | | GO | 79.2° | 90° | 73.2° | 90° | 97.44 % |
| 1.5 | 100 | PrS | 48.5° | 86.8° | 19.8° | 86.8° | 98.1 % |
| | | GO | 79.2° | 90° | 26° | 83.1° | 99.19 % |
| | 300 | PrS | 79.2° | 90° | 43.8° | 82.9° | 98.02 % |
| | | GO | 79.2° | 90° | 54.4° | 84.5° | 98.09 % |
| | 500 | PrS | 79.2° | 90° | 69.6° | 80.4° | 96.87 % |
| | | GO | 79.2° | 90° | 66.6° | 90° | 96.9 % |

VI. CONCLUSION

The presented paper constitutes a preliminary study to show the feasibility and potential advantages of replacing the 2L legs of the conventional DAB dc-dc converter by 3L legs, in any application where this converter is of interest. A 3L NPC DAB dc-dc converter has been proposed and studied. An effective modulation scheme with nine independent variables has been first defined. Four variables are employed to design a dc-link capacitor voltage balancing control. The remaining five variables are employed to control the power flow and minimize the predominant converter losses. The pattern of the optimum value of these last variables has been explored through the analysis of three decoupled optimization problems. Finally, simple and practical closed-form expressions of these modulation parameters have been provided, representing this modulation a good trade-off between pattern simplicity and accuracy of approximation to the three individual optimum solutions.

From the analytical, simulation, and experimental results, it is concluded that it is feasible to implement a DAB dc-dc converter from 3L NPC-type legs. The capacitor voltage balancing can be guaranteed for all operating conditions with the proper modulation and control. In addition, the ML topology provides benefits compared with the conventional 2L DAB converter; namely, an increase in the total dc-link voltage for a given semiconductor technology, the possibility of using lower-voltage-rated semiconductor devices with better performance figures for a given dc-link voltage, lower converter losses (especially for $d \neq 1$), and lower transformer-current harmonic distortion which leads to lower magnetic losses. Since the topology only increases the number of semiconductors (not the overall size of the passive components storing energy), highly compact implementations can be envisioned, with a better loss spreading and reduced heat sink requirements, and the overall cost could be competitive if popular devices were used

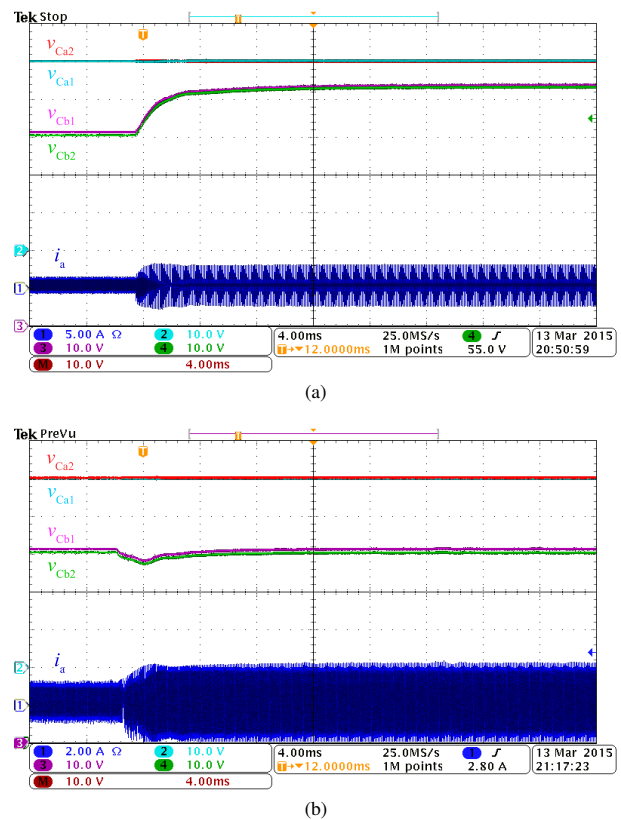


Fig. 17. Experimental results for v_{Ca1} , v_{Ca2} , v_{Cb1} , v_{Cb2} , and i_a with the proposed modulation in the following conditions: $V_A = 100$ V, $f_s = 10$ kHz, $K_{\phi,th} = 50$, $K_{\alpha,th} = 0.2$, $\Delta\alpha_{z,min} = 2.52^\circ$, and capacitor voltage balancing control enabled. (a) Transient response for a step change in V_B reference value from 100 V to 125 V ($R_B = 132 \Omega$). (b) Transient response for a step change in the load R_B from 132 Ω to 66 Ω .

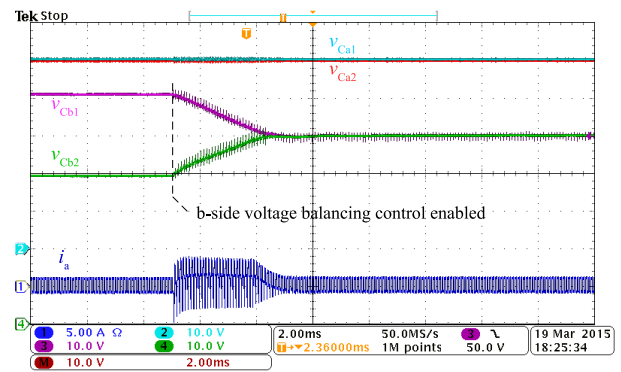


Fig. 18. Experimental results for v_{Ca1} , v_{Ca2} , v_{Cb1} , v_{Cb2} , and i_a under a capacitor voltage balance recovery transient with the proposed modulation in the following conditions: $V_A = 100$ V, $R_B = 132 \Omega$, $f_s = 10$ kHz, $K_{\phi,th} = 50$, $K_{\alpha,th} = 0.2$, $\Delta\alpha_{z,min} = 2.52^\circ$, and a-side capacitor voltage balancing control enabled.

with good performance and low cost due to scale economies. However, the advantages obtained may or may not compensate the drawbacks (increased number of devices, increased control complexity, etc.) depending on the specific application. The optimum number of levels, representing a good trade-off between performance and practicability, will ultimately depend on the particularities of each specific application and the current state of the art in power semiconductor technology.

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