Decoupled Dc-Link Capacitor Voltage Control of Dc-Ac Multilevel Multileg Converters

Sergio Busquets-Monge, *Senior Member, IEEE*, Robert Griñó, *Senior Member, IEEE*, Joan Nicolas-Apruzesse, *Member, IEEE*, and Josep Bordonau, *Member, IEEE*

***Abstract*— This paper studies the coupling between the capacitor voltage control loops of diode-clamped (or functionally equivalent) multilevel multileg (multiphase) dc-ac converters. From a complete model of the plant revealing the coupling, a simple approach consisting on multiplying the vector of control commands by a constant matrix is proposed to decouple the control problem and achieve a better controller performance. Simulation and experimental results are presented to prove the superior performance of the proposed decoupled control.**

***Index Terms*— Active-clamped, capacitor voltage balance, diode-clamped, multilevel, pulsewidth modulation, virtual vector.**

I. Introduction

MULTILEVEL converters [1] have opened a door for advances in the electrical energy conversion technology, bringing advantages in terms of converter power rating, efficiency, harmonic distortion, and electromagnetic noise.

This paper focuses on multilevel multileg dc-ac converters where a single dc-link is formed by the series connection of capacitors. The popular diode-clamped family of multilevel converters belongs to this category. Other arrangements of semiconductors to build the converter legs are also possible, such as in the active-clamped configuration [2]. In all these cases, each converter leg can be modelled as a single-pole *n*-throw switch, as shown in Fig. 1. Each leg has an associated switching-state variable ($s_{ac} \in \{1,2,\ldots, n\}$) storing the dc-link node number to which the ac output terminal is connected. The operation of such multilevel multileg dc-ac converters is challenging due to the well-known and widely reported capacitor voltage balancing issue, which is still an active research topic in the most recent literature [3]-[14].

Recently, a capacitor voltage balancing control based on a suitable modulation strategy (without the need of auxiliary hardware) has been proposed in [14], applicable to dc-ac converters with any number of levels and legs. The basic control structure is reproduced in Fig. 2(a). A set of variables capturing the unbalance between the two normalized partial dc-link voltages associated to each internal dc-link point $y \in \{2,\ldots, n-1\}$ is initially defined as

$$u_y = \frac{\sum_{x=1}^{y-1} v_{Cx}}{y-1} - \frac{\sum_{x=y}^{n-1} v_{Cx}}{n-y}, \quad (1)$$

and grouped into vector $\mathbf{u} = [u_2, u_3, \ldots, u_{n-1}]^T$. Vector $\mathbf{u}^*$ is generated from the command value of the dc-link capacitor voltages. The difference between $\mathbf{u}^*$ and $\mathbf{u}$ defines the error vector $\mathbf{e}$. The vector control signal is then computed as $\mathbf{k} = \mathbf{G}_c(s)\cdot\mathbf{e}$, where matrix $\mathbf{G}_c(s) = \text{diag}\{G_c(s),\ldots, G_c(s)\}$. Thus, each component of the error vector, e_y, is processed by an individual compensator with transfer function $G_c(s)$ to produce the value of the modulator parameter k_y. These $n-2$ modulation parameters are grouped into vector $\mathbf{k}$.

From the value of the modulation index (m), line-cycle angle (θ), parameters $\mathbf{k}$, and the dc-link capacitor voltages ($\mathbf{v}_C$, only necessary in cases where unbalanced dc-link capacitor voltage operation is desired), the modulation strategy in [14] determines each leg switching state, grouped into vector $\mathbf{s}_{ac}$.

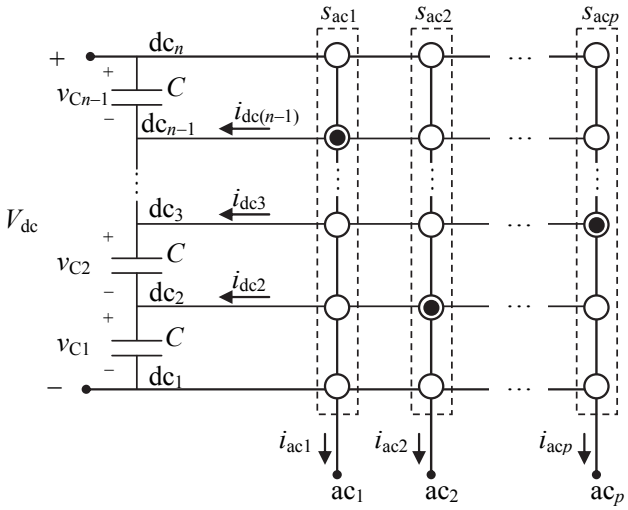

Fig. 1. Functional schematic of a *n*-level *p*-leg converter.

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S. Busquets-Monge, J. Nicolas-Apruzzese, and J. Bordonau are with the Department of Electronic Engineering, Universitat Politècnica de Catalunya, 08028-Barcelona, Spain (e-mail: sergio.busquets@upc.edu; joan.nicolas@upc.edu; josep.bordonau@upc.edu).

R. Griñó is with the Institute of Industrial and Control Engineering (IOC), Universitat Politècnica de Catalunya, 08028-Barcelona, Spain (e-mail: roberto.grino@upc.edu).

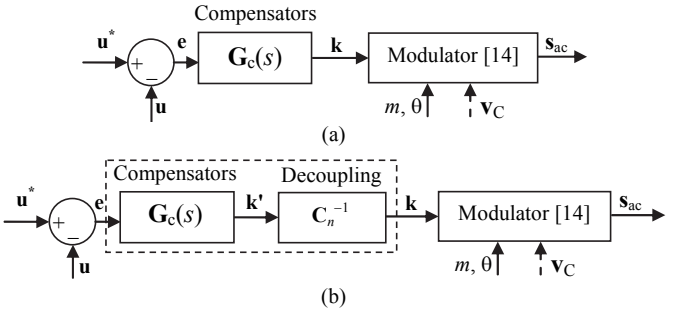

Fig. 2. Capacitor voltage control structure. (a) Without decoupling. (b) With decoupling (the dashed box contains the new proposed controller).

The value of parameter k_y represents the control action applied to mitigate the error e_y through the injection of a switching-cycle-average current at node dc_y equal to

$$i_{dcy} = \frac{2P}{V_{dc}} \cdot k_y, \tag{2}$$

where P is the switching-cycle-average power being transferred from the converter dc side to the ac side. This paper analyzes the coupling between the n–2 control loops (for $n \geq 4$) and proposes a simple method to decouple the control loop.

The paper is organized as follows. Section II presents the relevant plant model revealing the coupling and proposes a simple decoupling approach. Section III presents simulation and experimental results proving the superior performance of the decoupled control, and Section IV outlines the conclusions.

II. Decoupled Capacitor Voltage Balancing Control

In order to illustrate the coupling between control loops, let us first consider the simplest case of a four-level converter. It is assumed that the total dc-link voltage V_{dc} is kept constant through the regulation performed by other systems connected to the dc-link or through other converter control loops. It is also assumed that all capacitors present the same capacitance.

From Fig. 2(a), control action k_2 forces an injection of current i_{dc2} in response to the need to regulate u_2. As shown in Fig. 3, with the above assumptions, two thirds of i_{dc2} flow through the bottom capacitor and one third through the upper two capacitors, leading to a Δv increase of the bottom capacitor voltage and a $\Delta v/2$ decrease of the upper two capacitor voltages. The resulting variation of variables u_2 and u_3 are

$$\begin{aligned} \Delta u_2 &= \Delta v - \left(-\Delta v/2 - \Delta v/2\right)/2 = 3\Delta v/2 \\ \Delta u_3 &= \left(\Delta v - \Delta v/2\right)/2 - \left(-\Delta v/2\right) = 3\Delta v/4 = \Delta u_2/2. \end{aligned} \tag{3}$$

It can be therefore seen that control variable k_2 not only affects u_2, but also affects u_3, although in a smaller proportion. Due to the system symmetry, control variable k_3 also affects both u_3 and u_2 in an analogous manner. This coupling may lead to an inefficient chain of consecutive corrections from all control loops; i.e., conflicting control signals could occur, because the controller is decoupled and the plant is coupled.

The plant transfer function matrix, with control input **k** and output **u**, can be expressed as

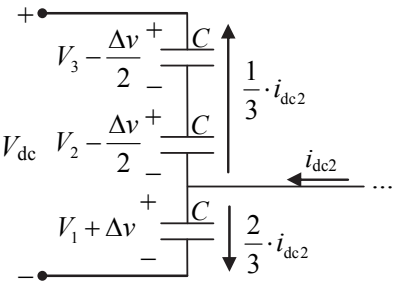

Fig. 3. Effect of current i_{dc2} on the dc-link capacitor voltages of a four-level converter.

$$\mathbf{u} = \frac{2P}{C \cdot V_{dc} \cdot s} \cdot \begin{bmatrix} 1 & 1/2 \\ 1/2 & 1 \end{bmatrix} \cdot \mathbf{k}. \tag{4}$$

In the general n-level case,

$$\mathbf{u} = \frac{2P}{C \cdot V_{dc} \cdot s} \cdot \mathbf{C}_n \cdot \mathbf{k}, \tag{5}$$

where $\mathbf{C}_n$ is the matrix of coupling coefficients, whose general expression is presented in the Appendix.

In order to decouple the plant [15], the vector of control variables fed by the compensators can be multiplied by the inverse of $\mathbf{C}_n$, as shown in Fig. 2(b). Then, the new controller-to-output plant transfer function becomes fully decoupled

$$\mathbf{u} = \frac{2P}{C \cdot V_{dc} \cdot s} \cdot \mathbf{C}_n \cdot \mathbf{C}_n^{-1} \cdot \mathbf{k}' = \frac{2P}{C \cdot V_{dc} \cdot s} \cdot \mathbf{I}_{n-2} \cdot \mathbf{k}', \tag{6}$$

where $\mathbf{I}_{n-2}$ is the (n–2)-order identity matrix. In the case of a four-level converter,

$$\mathbf{C}_4^{-1} = \begin{bmatrix} 4/3 & -2/3 \\ -2/3 & 4/3 \end{bmatrix}. \tag{7}$$

The Appendix also presents the expression of the inverse of the coupling matrix for the general n-level case.

According to (6), a system with the control structure of Fig. 2(b) can be modeled with a set of n–2 single-input single-output decoupled loop gains

$$T_y(s) = \frac{u_y}{e_y} = \frac{2P}{C \cdot V_{dc} \cdot s} \cdot G_c(s) \cdot e^{-T_d \cdot s}, \tag{8}$$

where $y \in \{2,3,..,\ n-1\}$ and T_d is the delay introduced by a digital implementation of the controller. These loops are all independent from each other. With the control structure of Fig. 2(a), the loop gain of each channel is also as in (8), but each loop receives as perturbations the control action from other loops, according to the coupling coefficients of $\mathbf{C}_n$.

The introduction of the decoupling block in the control does not imply any change in the design of the compensator and modulator blocks. The modulator can be the same as in [14] and the compensator can be designed as explained in section III.C of [14]. Assuming $T_d \approx T_s$ (switching period), the compensator can be designed as [14]

$$\begin{aligned} G_c(s) &= \frac{G_{c0}}{\left(s/\omega_p + 1\right)} \\ G_{c0} &= \frac{C \cdot V_{dc} \cdot \omega_s}{20 \cdot P} \\ \omega_p &= \omega_s/10, \end{aligned} \tag{9}$$

where $\omega_s = 2\pi \cdot f_s = 2\pi/T_s$. If T_d is higher than T_s, the maximum value of G_{c0} to guarantee a minimum phase margin will decrease. In applications with a significant unbalanced dc loading/sourcing of the dc-link capacitors, the use of a proportional-integral compensator would be more advisable.

III. Simulation and Experimental Results

Simulations and experiments have been carried out to study the performance of the proposed decoupled dc-link capacitor voltage control.

Simulations have been performed in Matlab-Simulink. The dc-link is fed by a constant voltage source and a wye-connected multiphase series resistive-inductive load is assumed at the converter ac side with per-phase characteristic parameters R and L. Fig. 4 depicts the performance under ramp variations of v^*_{C2} and v^*_{C3} commands in a four-level three-phase system. At t = 20 ms, the first ramp begins with $v^*_{C2} = v^*_{C3} = 50$ V. At t = 25 ms, the first ramp ends with v^*_{C2} = 60 V and v^*_{C3} = 40 V. At t = 50 ms, the second ramp begins with v^*_{C2} = 60 V and v^*_{C3} = 40 V. At t = 55 ms, the second ramp ends with $v^*_{C2} = v^*_{C3} = 50$ V. This translates into a ramp variation of u^*_3 from 0 V to 15 V and then back to 0 V, while u^*_2 remains fixed at 0 V. The compensator gain has been set to a moderate value in order to highlight the difference in behavior with and without the decoupling matrix in the control loop (G_{c0} = 0.02, while the maximum value is G_{c0} = 0.14 for $T_d = T_s$, calculated from (9), and the maximum value is G_{c0} = 0.08 for $T_d = 2T_s$). As it can be observed, under a control without decoupling, undesired variations of u_2 and v_{C1} occur, while these variations are fully suppressed with a decoupled control.

Fig. 5 shows the performance under a five-level five-phase system to prove the applicability of the proposed decoupled control to systems with a higher number of levels and legs. Similar to Fig. 4, two ramps are generated in v^*_{C1} and v^*_{C4} commands, from $v^*_{C1} = v^*_{C4} = 50$ V to v^*_{C1} = 60 V and v^*_{C4} = 40 V and then back to $v^*_{C1} = v^*_{C4} = 50$ V. With the use of the decoupled control, v_{C2} and v_{C3} remain constant over the transients, as desired.

As an additional note, it can be observed that the multiphase currents of Figs. 4 and 5 do not present any low-frequency distortion despite the operation under different capacitor voltages. This is an interesting property of the applied modulation strategy [14].

Experiments have also been carried out with a four-level three-phase active-clamped dc-ac converter prototype [2] built upon 100 V metal-oxide semiconductor field-effect transistors, and controlled with a dSPACE control platform. Experiments have been performed in the same conditions as in Fig. 4. The experimental results depicted in Fig. 6 corroborate the corresponding simulation results from Fig. 4, thus validating the superiority of the decoupled control loop. Fig. 7 presents additional experimental results of a start-up transient under an unbalanced loading of the dc-link capacitors through different resistors connected across the capacitors. With the decoupled control, the capacitor voltage trajectories to reach the commanded value (50 V) are the most effective, significantly reducing the transient time.

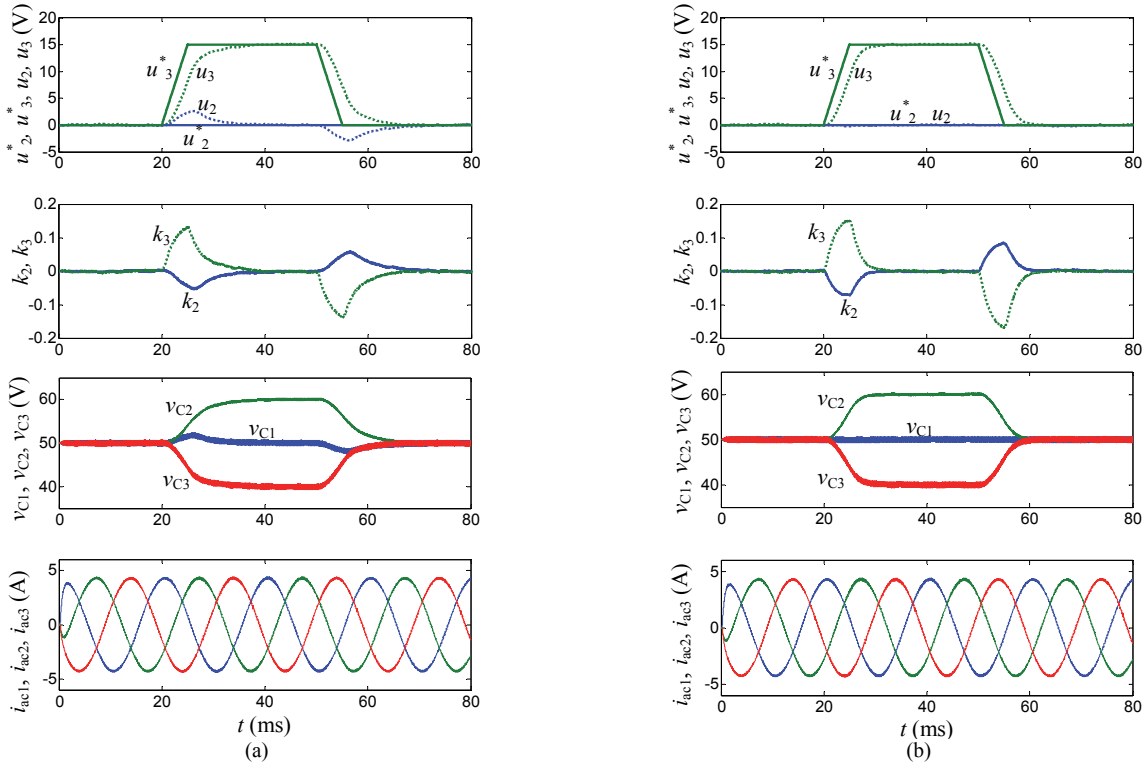

Fig. 4. Simulation results under ramp variations of the v^*_{C2} and v^*_{C3} commands of a four-level three-phase system. Conditions: V_{dc}= 150 V, m = 0.5, C = 155 μF, R = 10 Ω, L = 10 mH, switching frequency f_s = 5 kHz, and $G_c(s) = 0.02/[1+s/(1000\pi)]$. (a) Control without decoupling. (b) Control with decoupling.

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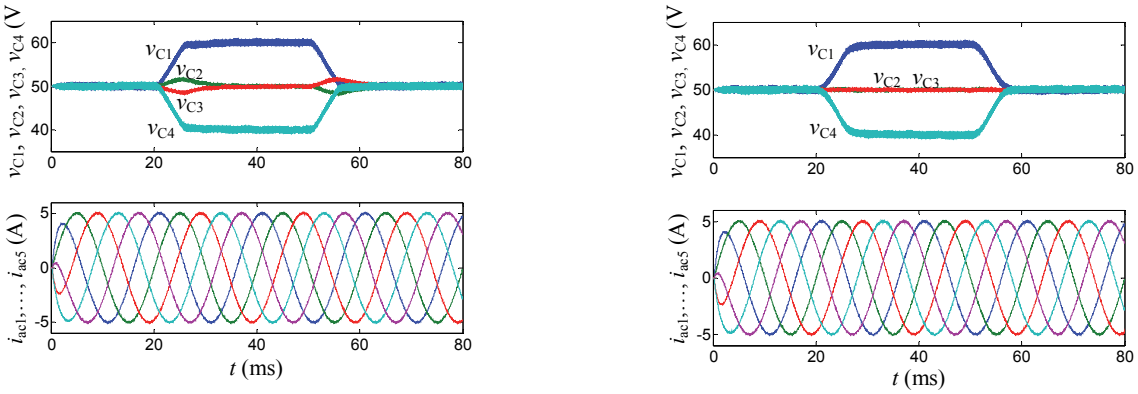
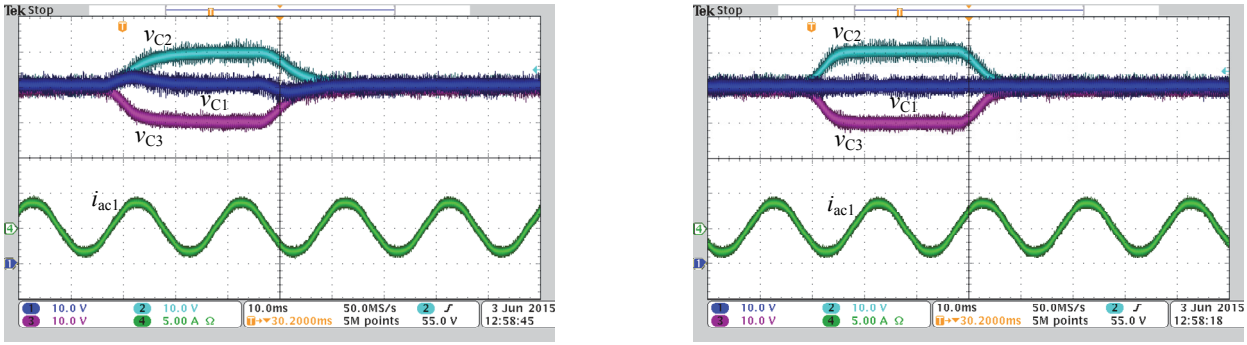


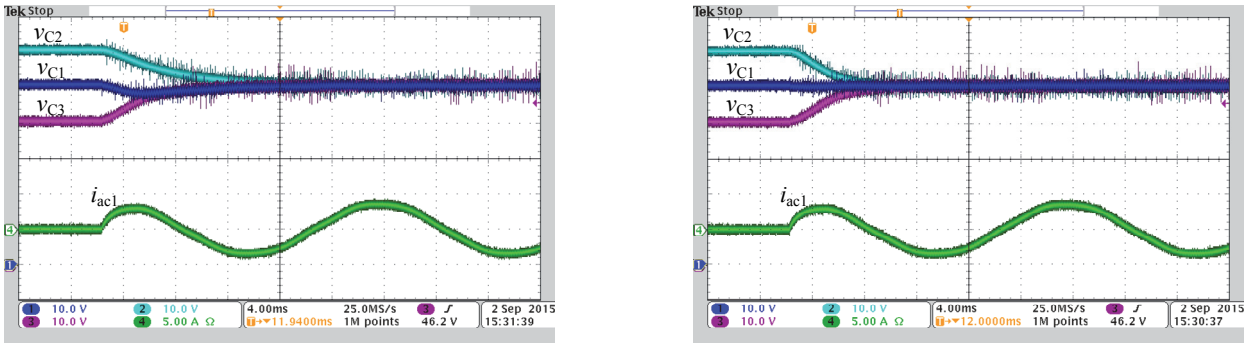
(a) (b)

Fig. 5. Simulation results under ramp variations of the v^*_{C1} and v^*_{C4} commands of a five-level five-phase system. Conditions: V_{dc}= 200 V, m = 0.5, C = 200 μF, R = 10 Ω, L = 10 mH, f_s = 5 kHz, $G_c(s)$ = 0.02/[1+s/(1000π)]. (a) Control without decoupling. (b) Control with decoupling.



(a) (b)

Fig. 6. Experimental results under a ramp variation of the v^*_{C2} and v^*_{C3} commands of a four-level three-phase system. Conditions: the same as in Fig. 4. (a) Control without decoupling. (b) Control with decoupling.



(a) (b)

Fig. 7. Experimental results of a converter start-up transient under an unbalance loading of the dc-link capacitors through three resistors (R_1, R_2, R_3), each connected in parallel with one of the dc-link capacitors (C_1, C_2, C_3, respectively) in a four-level three-phase system. Conditions: the same as in Fig. 4 with v^*_{C1} = v^*_{C2} = v^*_{C3} = 50 V, $R_1 \approx 300$ Ω, $R_2 \approx 360$ Ω, $R_3 \approx 240$ Ω. (a) Control without decoupling. (b) Control with decoupling.

IV. Conclusion

A dc-link model of multilevel multileg diode-clamped-type dc-ac converters has been presented, revealing the coupling among the different capacitor voltage control loops. From this model, a simple approach involving the product by the inverse matrix of coupling coefficients has been proposed to decouple the control problem and improve the controller performance. Although the decoupling is not strictly necessary, it improves the control performance at a low computational cost.

The presented decoupling approach can be easily applied to any multilevel dc-dc and dc-ac conversion system involving a dc-link formed by a series connection of capacitors.

Appendix

The general coupling matrix for an n-level converter is

$$\mathbf{C}_n = \begin{bmatrix} 1 & \cdots & \frac{3}{n-2} & \frac{2}{n-2} & \frac{1}{n-2} \\ \frac{1}{2} & 1 & \vdots & \vdots & \vdots \\ \frac{1}{3} & \frac{2}{3} & \ddots & \frac{2}{3} & \frac{1}{3} \\ \vdots & \vdots & \vdots & 1 & \frac{1}{2} \\ \frac{1}{n-2} & \frac{2}{n-2} & \frac{3}{n-2} & \cdots & 1 \end{bmatrix}, \qquad (10)$$

which is a full-rank $(n–2)\times(n–2)$ matrix. The element from row x and column y is defined as

$$\mathbf{C}_n(x,y)=\frac{y}{x};\quad y\le x$$
$$\mathbf{C}_n(x,y)=\frac{n-1-y}{n-1-x};\quad y>x \tag{11}$$

From the value of the coupling coefficients, it can be seen that the coupling decreases as the distance between the dc-link points increases.

The inverse of the general coupling matrix is

$$\mathbf{C}_n^{-1}=\frac{1}{n-1}\cdot\begin{bmatrix} 2\cdot(n-2) & -(n-3)\cdot 2 & & & & & & & \\ -1\cdot(n-2) & 4\cdot(n-3) & -(n-4)\cdot 3 & & & & \mathbf{0} & & \\ & -2\cdot(n-3) & 6\cdot(n-4) & -(n-5)\cdot 4 & & & & & \\ & & -3\cdot(n-4) & \ddots & \ddots & & & & \\ & & & \ddots & \ddots & -3\cdot(n-4) & & & \\ & & \mathbf{0} & & -(n-5)\cdot 4 & 6\cdot(n-4) & -2\cdot(n-3) & & \\ & & & & & -(n-4)\cdot 3 & 4\cdot(n-3) & -1\cdot(n-2) & \\ & & & & & & -(n-3)\cdot 2 & 2\cdot(n-2) & \end{bmatrix}$$

where only three diagonals contain non-zero elements.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2553-2580, Aug. 2010.

[2] S. Busquets-Monge and J. Nicolas-Apruzzese, "A multilevel active-clamped converter topology - Operating principle," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 3868-3878, Sept. 2011.

[3] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, pp. 242-249, Mar. 2000.

[4] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 3255-3266, Dec. 2007.

[5] S. A. Khajehoddin, A. Bakhshai, and P. K. Jain, "A simple voltage balancing scheme for m-level diode-clamped multilevel converters based on a generalized current flow model," *IEEE Trans. Power Electron.*, vol. 23, pp. 2248-2259, Sept. 2008.

[6] T. Ito, M. Kamaga, Y. Sato, and H. Ohashi, "An investigation of voltage balancing circuit for DC capacitors in diode-clamped multilevel inverters to realize high output power density converters," in *Proc. IEEE Energy Conv. Congr. and Exp.*, 2010, pp. 3675-3682.

[7] K. Hasegawa and H. Akagi, "A new DC-voltage-balancing circuit including a single coupled inductor for a five-level diode-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 47, pp. 841-852, March/Apr. 2011.

[8] J. Shen, S. Schröder, R. Rösner, and S. El-Barbari, "A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped three-level inverters," *IEEE Trans. Power Electron.*, vol. 26, pp. 3084-3095, Nov. 2011.

[9] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, "Voltage balancing approaches for diode-clamped multilevel converters using auxiliary capacitor-based circuits," *IEEE Trans. Power Electron.*, vol. 28, pp. 2111-2124, May 2013.

[10] P. Chaturvedi, S. Jain, and P. Agarwal, "Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 613-624, Feb. 2014.

[11] J.-S. Lee and K.-B. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, pp. 1720-1732, Apr. 2014.

[12] V. Yaramasu, B. Wu, and J. Chen, "Model-predictive control of grid-tied four-level diode-clamped inverters for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, pp. 2861-2873, June 2014.

[13] R. Abdullah, N. A. Rahim, S. R. Sheikh Raihan, A. Z. Ahmad, "Five-level diode-clamped inverter with three-level boost converter," *IEEE Trans. Ind. Electron.*, vol.61, pp.5155-5163, Oct. 2014.

[14] S. Busquets-Monge, R. Maheshwari, J. Nicolas-Apruzzese, E. Lupon, S. Munk-Nielsen, and J. Bordonau, "Enhanced dc-link capacitor voltage balancing control of dc-ac multilevel multileg converters," *IEEE Trans. Ind. Electron.*, vol. 62, pp. 2663-2672, May 2015.

[15] S. Skogestad and I. Postlethwaite, *Multivariable Feedback Control: Analysis and Design*, 2nd ed. Wiley, 2005.

Sergio Busquets-Monge (SM'11) was born in Barcelona, Spain. He received the M.S. degree in electrical engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, in 1999, the M.S. degree in electrical engineering from Virginia Polytechnic Institute and State University, Blacksburg, in 2001, and the Ph.D. degree in electrical engineering from the UPC in 2006.

From 2001 to 2002, he was with Crown Audio, Inc. He is currently an Associate Professor with the Department of Electronic Engineering, UPC. His research interests include multilevel conversion and converter integration.

Robert Griñó (SM'12) received the M.Sc. degree in electrical engineering and the Ph.D. degree in automatic control from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1989 and 1997, respectively.

From 1990 to 1991, he was a Research Assistant with the Instituto de Cibernética, UPC. From 1992 to 1998, he was an Assistant Professor with the Automatic Control Department, Universitat Politècnica de Catalunya, where he has been an Associate Professor since 1998. His research interests include digital control, nonlinear control, stability theory and control of power electronics converters. Dr. Griñó is an affiliate member of International Federation of Automatic Control (IFAC) and a member of the Spanish Society on Automation and Control-IFAC.

Joan Nicolas-Apruzzese (M'15) was born in Maracaibo, Venezuela. He received the M.S. (2008) and Ph.D. (2013) degrees in electrical engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain.

Since 2008, he has been a researcher in the Power Electronics Research Centre of the UPC. His main research interests include power multilevel converters applied to electric vehicles and photovoltaic- and wind-energy systems.

Josep Bordonau (M'89) received the M.Sc. and the Ph.D. degrees in electrical engineering with honors from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain in 1984 and 1990, respectively.

He has been a Lecturer (1984), an Assistant Professor (1990), and an Associate Professor since 1991, in the UPC. Currently, he is Director of the Power Electronics Research Center of the UPC and the Education Director of the Iberia Office in KIC InnoEnergy. He has been active in more than 30 research projects with international institutions and companies, authoring more than 70 international journal and conference papers. His main interest is on ac converters, multilevel technology, renewable energies, energy management systems, distributed generation systems, smart grids, and electric/hybrid vehicles.

Dr. Bordonau is a member of the IEEE Technical Committee in Distributed Generation and Renewable Energy Systems.