Xjenza Online - Journal of The Malta Chamber of Scientists
www.xjenza.org
DOI: 10.7423/XJENZA.2014.2.06

Research Article

Warpage issues in large area mould embedding technologies

Russell Farrugia[1], Ivan Grech[1], Owen Casha[1], Joseph Micallef[1], Edward Gatt[1], Roseanne Duca[2] and Conrad Cachia[2]
[1]Department of Microelectronics and Nanoelectronics, Malta
[2]ST Microelectronics Malta

Abstract. The need for higher communications speed, heterogeneous integration and further miniaturisation have increased demand in developing new 3D integrated packaging technologies which include wafer-level moulding and chip-to-wafer interconnections. Wafer-level moulding refers to the embedding of multiple chips or heterogeneous systems on the wafer scale. This can be achieved through a relatively new technology consisting of thermal compression moulding of granular or liquid epoxy moulding compounds. Experimental measurements from compression moulding on 8" blank wafers have shown an unexpected tendency to warp into a cylindrical-shape following cooling from the moulding temperature to room temperature. Wafer warpage occurs primarily as a result of a mismatch between the coefficient of thermal expansion of the resin compound and the Si wafer. This paper will delve into possible causes of such asymmetric warpage related to mould, dimensional and material characteristics using finite element (FE) software (ANSYS Mechanical). The FE model of the resin on wafer deposition will be validated against the measurement results and will be used to deduce appropriate guidelines for low warpage wafer encapsulation.

Keywords component – 3D packaging – wafe-level moulding – warpage – epoxy moulding compound

1 Introduction

The demands of high functional electronic devices are indicating a trend towards further miniaturisation and increased performance. In the case of devices for consumer electronic applications, 80 % of the components are passives (do not need electrical power to operate) which constitute 70 % of the product assembly cost in today's mobile phones (Souriau et al., 2005). This has driven the packaging industry to develop advanced 3D packaging solutions in order to achieve trade-offs with dimensional requirements, performance maximization, manufacturability, flexibility and cost. A number of technologies (ex: Embedded Wafer Level Ball Grid Array (eWLB) by Infineon (Meyer et al., 2008) and the Chip in Polymer (CiP) by Fraunhofer IZM, TU Berlin and Wuerth (Boettcher et al., 2008)) have been developed on the basis of the two major packaging trends identified as having low cost potential: large area mould embedding of laterally placed dies and 3D integration of vertically stacked dies. Both concepts may also be combined into a stacked wafer-level System-in-Package coupled with the integration of through mould vias (TMVs) to create the smallest form factor package (Takahashi et al., 2012). Other variations to this process have been reported, for instance the assembly of vertical interconnect elements (VIE) instead of laser drilled via interconnections (Braun et al., 2011). However the back-end processes of these technologies commonly involve wafer-level die embedding using several applicable packaging techniques falling under two categories: moulding and liquid encapsulation such as printing. Moulding techniques which include transfer, film lamination and compression have the advantage of precise dimensional control, however they are expensive. Thermosetting polymers, specifically epoxy moulding compounds (EMCs) are the most widely used moulding materials and their reliability is of crucial importance towards system functionality (Sadeghinia et al., 2012).

One important requirement of any embedding technology is the ability to produce a moulded wafer on which subsequent wafer-level processes can be carried out with ease (Kumar et al., 2009). Consequently warpage resulting from the process-induced residual stresses is of great concern in thin-film packaging (below 1 mm). Room temperature warpage of compression moulded EMC on blank Si wafers has been reported to be significant by Tomita et al. (2012), Takahashi et al. (2012) and Kumar et al. (2009). In this paper the warpage issues concerning wafer-level thermal compression moulding will be discussed whereby a finite element technique used to simulate the cooling of the moulded wafer from the moulding temperature to room temperature will be presented.

Correspondence to: Russell Farrugia (russell.farrugia@um.edu.mt)

2 Problem overview

Like in any polymer, EMC consists of an amorphous molecular structure which may exist either in a solid/glassy state or a liquid/rubbery state with the glass temperature, T_G defining the transformation between the two states. Moreover the thermosetting properties of EMC signify that molecular structures readily crosslink when heated above T_G through an exothermic reaction known as the curing process with the aid of a catalyst. In order to reduce processing time (the time required for the epoxy to reach the fully cured state and hence maximize its material properties), external heat is supplied during compression moulding to raise the temperature of the moulding compound.

2.1 Compression Moulding

The basic process flow in compression moulding for packaging applications, schematically displayed in Figure 1 can be described as follows (Matsutani, 2009):

1. wafer substrate is supplied face down to the top mould die;
2. a precise amount of the required EMC is prepared before it is inserted into the bottom mould die chase;
3. the substrate is clamped as the mould begins to close while vacuum is applied to remove gases and moisture emitted by the compound;
4. after the mould is completely closed, it is heated to the moulding temperature T_m and kept constant for a specific amount of time to initiate curing of the compound;
5. after curing at T_m is completed the mould is opened to release the moulded substrate allowing it to be cooled in air to room temperature.

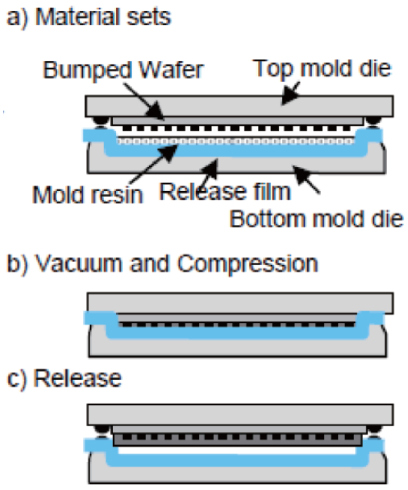

Figure 1: Compression moulding process flow showing (a) the material preparation stage, (b) vacuum, compression and heating stage and (c) final release stage (Tomita et al., 2012).

Compression moulding essentially results in the bonding of two materials having dissimilar thermo-mechanical properties. From the moment that curing is initiated during the mould heating stage, the compound's resistance to deformation starts to increase. Given that the coefficient of thermal expansion of EMC, CTE_{EMC} differs from that of silicon, CTE_{Si}, internal stresses are developed in the moulded wafer during the curing and cooling stages resulting in room temperature warpage. A closed-form mathematical solution of the radius of curvature of the deformation of a bi-material beam under a temperature variation, ΔT, was derived by Timoshenko (Timoshenko, 1925), where the deformation is directly proportional to the beam length, $CTE_{EMC} - CTE_{Si}$, ΔT and inversely proportional to the total moulded wafer thickness. It is additionally dependent on the bending properties and therefore on the characteristic length and Young's modulus.

2.2 Observation of Warpage

Warpage analysis of the moulded Si disc-shaped wafer using analytical calculations is not straight forward. One of the reasons is that the volume change is not constant during the moulding cycle as shown in Figure 2. During the heating stage from room temperature to T_m the compound is largely in the liquid state (above T_G) thus having a linear but relatively high thermal expansion. At the curing stage, the formation of crosslinks results in an isothermal volumetric shrinkage, ϵ_s . During the cooling stage, the thermal shrinkage of the fully cured material is significantly lower than the thermal expansion during heating. However in the case that T_m is higher than T_G, CTE_{EMC} will vary with temperature. A substantial reduction in CTE_{EMC} takes place due to the glassy state transition occurring as the viscoelastic material approaches T_G (see 3).

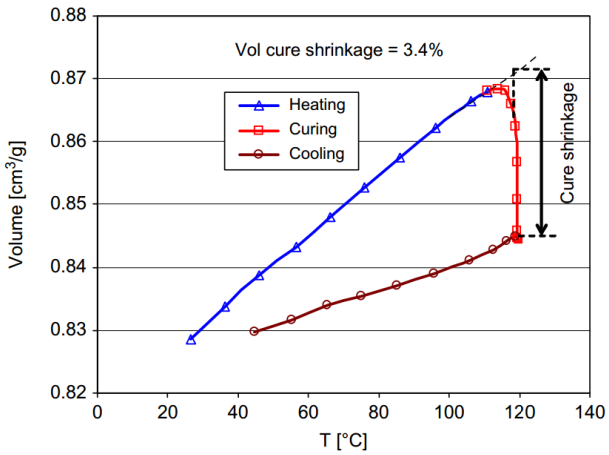

Figure 2: Volume changes during heating (5 °C/min; cooling and shrinkage during isothermal cure of EMC (T_G=120 °C) (Sadeghinia et al., 2012).

The problem of warpage in wafer-level embedding has been recently investigated both experimentally and numerically. Test samples from the back-end process for the stacked TSV- Wafer-level Chip Scale Package (WCSP) platform were presented by Texas Instruments Inc. (Takahashi et al., 2012). Warpage measurements of 8" moulded wafers without stacked chips were found to be as high as 6 mm (EMC thickness: 200 µm, Si thickness: 100 µm). Moreover for all moulded wafers with and without the stacked chips a convex cylindrical-shape deformation

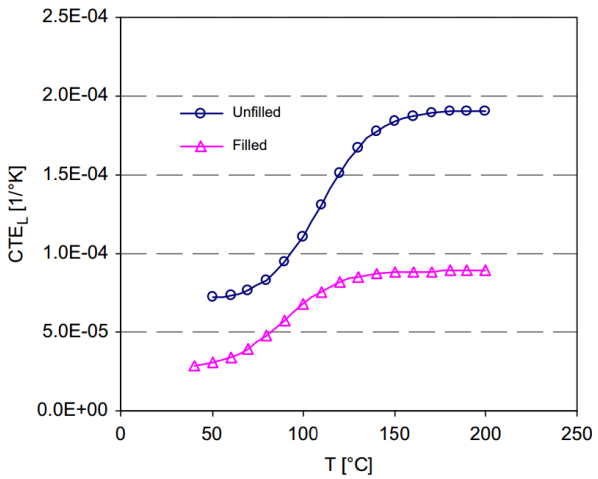

Figure 3: Linear CTE of unfilled and filled EMC vs. temperature (T_G = 120 °C) (Sadeghinia et al., 2012).

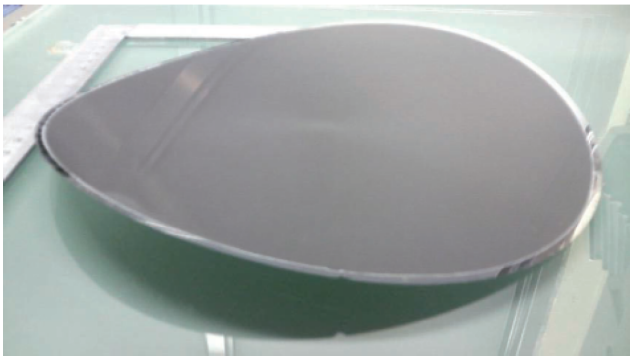

Figure 4: Blank moulded wafer warpage: Si - 100 µm, EMC - 200 µm (Takahashi et al., 2012).

shown in Figure 4 was consistently observed. Warpage was found to increase with an increase in T_G and elastic modulus and a decrease in CTE_{EMC}. Furthermore the effect of post-mould grinding resulted in a deformation increase in accordance with the Timoshenko's analytical formulation.

Similarly Tomita et al. (2012) carried out wafer-level compression moulding whereby the mould thickness uniformity was analysed. This was carried out by measuring the mould deposition thickness at specific radial locations. It was found that a one-directional mould thickness gradient was consistently observed suggesting potential effects due to mould die design and calibration. Other warpage measurements on wafer-level moulding were also carried out by Kumar (Kumar et al., 2009) using infrared interferometry where a warped shape similar to that of Takahashi et al. (2012) was observed. It was also suggested that the thermo-mechanical stresses can be reduced either by adding a low filler content in order to reduce the Young's modulus of the epoxy moulding compound and thus reduce its resistance to deformation or by adding a high filler content to reduce CTE_{EMC} and hence the thermal expansion mismatch within the moulded wafer.

With regards to numerical modelling although the effect of the viscoelastic properties of EMC has been simulated at die level [18], little has been published on the finite element analysis of wafer-level compression moulding. The difficulties in replicating the room temperature deformed shape of the moulded wafer were discussed by Mallik and Stout (2010), Mallik et al. (2014). Due to the fact that the cylindrical-shape is not the only and most likely numerically stable solution, a number of simulation tricks using the ANSYS Mechanical solver were proposed in order to produce a steady and stable cylindrical-shape instead of a bowl-shaped deformation (Mallik and Stout, 2010). Mallik et al. (2014) showed that a good comparison was achieved between the results from FE simulations and measurements for an Al-coated Si wafer.

3 Finite element modelling of Moulded Wafer

Finite element analysis was carried out using the ANSYS mechanical solver within ANSYS Workbench v14 in order to validate measurement results on compression moulded wafers (similar to that depicted in Figure 4) carried out by ST Microelectronics Malta, to test possible causes leading to room temperature warpage and finally to propose improvements which may lead to a reduction in warpage to acceptable production limits.

A static structural simulation was carried out on a model of an 8" (0.2032 m) diameter disc consisting of stacked layers of the epoxy moulding compound and Si. With reference to Figure 4, the EMC layer in the FE model covers the entire wafer while the notch marking the wafer's crystal orientation was assumed to have a negligible effect on the moulded wafer warpage. Both surface and solid modelling approaches were investigated using different element types. In the case of the former a layered shell element (SHELL181) (n.d.) was utilised which enables a layered section to be prescribed to a 2D surface mesh. SHELL181 is typically used for modelling composite shells or sandwich construction and its accuracy is governed by the first-order shear deformation theory (n.d.). Therefore for the layered section function available with ANSYS Mechanical v14, the thicknesses and material type of the respective layers may be inputted in tabular format. The second approach consists of modelling a solid disc using SOLID185 elements whereby the thickness of the EMC and Si layers is prescribed via extrusion.

The following is a description of the properties of the moulding compound and Si wafer prescribed to the previously mentioned models. In the case of EMC the elastic modulus is considered to be isotropic and varies linearly from room temperature to T_m, the rubbery state linear coefficient of thermal expansion ($CTE_{EMC,2}$) is constant above T_G and the glassy state linear coefficient of thermal expansion ($CTE_{EMC,1}$) is constant below T_G. Silicon has anisotropic properties however in the case where thin plates have symmetric boundary conditions, the elastic deformation of such structures can be evaluated using the symmetric biaxial modulus. Therefore the Si properties

for the FE model consist of an isotropic elastic modulus based on the thin film biaxial modulus for a (100) Si wafer: 180 GPa (Hopcroft et al., 2010); together with a constant linear coefficient of thermal expansion. From the experiments, negligible warpage was observed as the moulded wafer is released from the mould die and hence T_m was set as the stress free temperature for both EMC and Si.

The mesh construction is of crucial importance in FE modelling in order to ensure that solution convergence is achieved. A mapped mesh with quadrilateral shaped elements was created for the two previously mentioned modelling approaches. This was carried out by dividing the geometry into 4-edged surfaces/solid bodies to produce an O-mesh displayed in Figure 5. The grid refinement could thus be varied by specifying the number of elements on the body edges. A mesh independence study was also carried out to ensure that the solution does not change with further mesh refinement. For this study only the element dimensions in the x and y-directions were altered, while the element dimension in the z-direction was kept equal to the respective layer thickness.

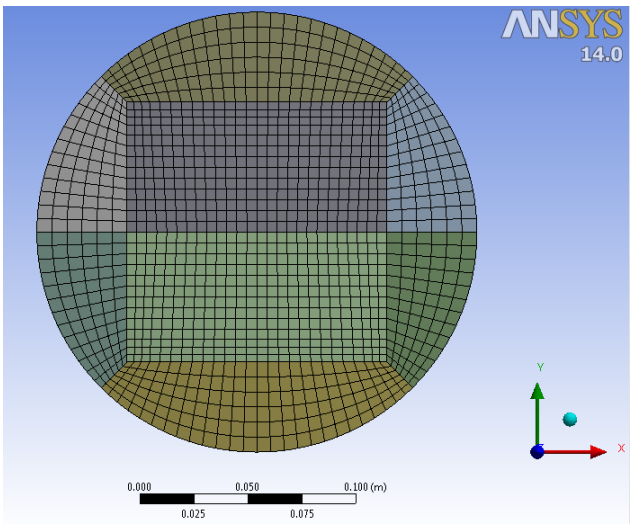

Figure 5: O-mesh with SOLID185 elements

4 Finite element model of moulded wafer: results

The moulded wafer model was initially subjected to a steady state thermal load varying from 175 °C to 25 °C in order to simulate the cooling stage during the mould process. Good agreement was obtained in the resultant out-plane deformation between the surface (using shell elements) and solid models simulated. Preliminary results show that a bowl-shaped warped moulded wafer is obtained when considering isotropic and linear elastic material properties for both EMC and the Si wafer. Additionally simulations carried out by considering silicon's anisotropy in terms of orthotropic material constants resulted in the same warped shape. This implies that in order to generate the cylindrical-shape, anisotropy has to be prescribed either through solver 'tricks' described by Mallik and Stout (2010) whereby 'symmetry-breaking' forces are applied to the moulded wafer during simulated cooling to room temperature which are then removed to obtain the final solution, or by process-related effects observed from the measurements. In fact, the warped shape shown in 6 was obtained by fixing the displacements in all directions of the nodes on the surface of the silicon side along the wafer centre line. It should also be noted that the moulded wafer FE model returns back to the stress-free condition once the displacement constraints are removed at room temperature. Good agreement was obtained between the measurement and numerical results obtained from the 4 moulded wafers listed in Table 1 where the maximum difference between both sets of data was below 5 %.

Compared to the moulded wafer shown in Figure 4, the EMC layer covers the entire wafer in the case of the FE model of Figure 5. A modification to the model whereby the diameter of the EMC layer was reduced by 10 mm showed that the EMC-free wafer edge does not alter the simulation results with and without the displacement constraints applied at the wafer centre-line.

A parametric analysis was carried out in order to evaluate the dependence of warpage on the thickness of the Si wafer and mould cap using the moulding compounds considered in the experimental moulding trials. From these results it can be deduced that the warpage is proportional to the ratio of the mould cap thickness to the wafer thickness as shown in Figure 7. Warpage is also inversely proportional to the total thickness of the moulded wafer (Figure 8) in accordance with the 2D bi-material beam theory by Timoshenko (Timoshenko, 1925). The results also confirm that $(T_m – T_G)$ is significantly important in determining the total thermal contraction during the cooling stage of moulding process. Furthermore a higher elastic modulus for EMC results in increased deformation of the moulded wafer.

The 3D model was also modified in order to simulate the variation in the mould thickness deduced from measurements obtained along the circumference of the moulded wafer. Although initial indications show that the effect of non-planar mould thickness on the warped shape is negligible, further measurements and simulations are required to test this hypothesis.

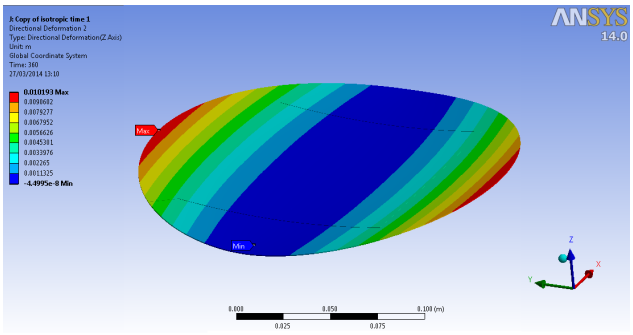

Figure 6: Directional Deformation (Z-Axis) (m) for Moulded Blank Wafer (Si: 375 µm, EMC 200 µm).

Table 1: FE model (using SOLID185 elements) validation against measurement trials.

Wafer thickness	EMC thickness	Mould Temperature	Warpage		% Error
µm	µm	°C	Measurements	FE model	
700	300	175	2	2.091	4.550
375	300	175	9.5	9.847	3.653
375	200	175	6.5	6.803	4.662
280	200	175	11	11.296	2.695

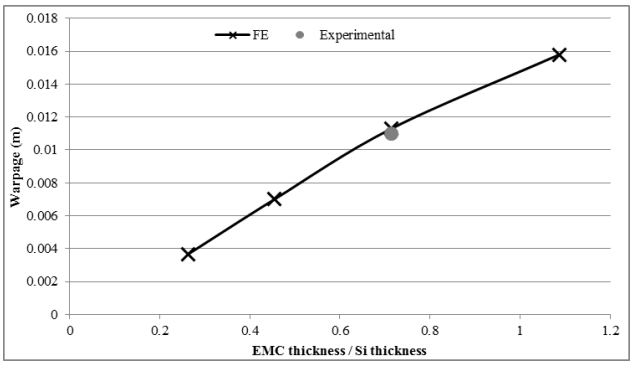

Figure 7: Warpage results against ratio of EMC thickness to Si thickness at $T_m = 175\,°C$ and total mould thickness of 0.48 mm.

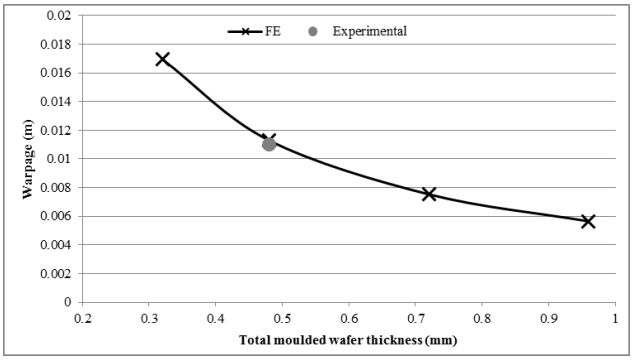

Figure 8: Warpage results against total moulded wafer thickness at $T_m = 175\,°C$ and ratio of EMC to Si thickness of 0.714.

5 Conclusion

Wafer-level embedded moulding is a relatively new technology with great potential towards the development of low cost 3D integration. However the complex properties of the moulding compound compared to those of the Si wafer result in significant warpage at room temperature hampering the subsequent processing of the embedded dies. Therefore the moulding properties of the EMC need to be fully understood in order to optimise the compression moulding technique. Through finite element simulations and experimental observations, it was deduced that the warpage of wafer-level moulded blank wafers can be reduced by:

- increasing the total thickness of the moulded wafer;
- decreasing the ratio of the mould cap thickness to the wafer thickness;
- reducing the total thermal expansion of the moulding compound from the moulding temperature to room temperature. This can be reduced by choosing a moulding compound with the lowest ($T_m - T_G$);
- decreasing the elastic modulus of moulding compound.

Apart from optimisation of the EMC material properties and layer thicknesses, other possible techniques can be adapted to this moulding process which may lead to a reduction in the overall warpage. For instance dicing the wafer prior to moulding would highly alleviate the build-up of stress over the entire wafer (Tomita et al., 2012). Moreover reinforcement of the moulding compound by means of glass or carbon fibres would significantly increase the stiffness and hence the resistance to deformation of the mould layer (Kim, 2012). Further work will be carried out to analyse possible causes leading to the warped shaped at room temperature such as non-planarity in the mould cap thickness. This will entail more detailed measurements of the moulded wafer thickness. Simulations will subsequently be carried out on a moulded wafer with embedded dies.

Acknowledgments

This paper is part of my work in LAB4MEMS, an ENIAC Joint Undertaking financed project

References

(nodate). ANSYS® Academic Research, Release 14.0, Help System, Element Reference, Element Library, SHELL181, ANSYS, Inc., 2011.

(nodate). ANSYS® Academic Research, Release 14.0, Help System, Theory Reference, Structures with Material Nonlinearities: Viscoelasticity ANSYS, Inc., 2011.

Boettcher, L., Manessis, D., Ostmann, A., Karaszkiewicz, S. and Reichl, H. (2008). Embedding of Chips for System in Package realization - Technology and Applications. *2008 3rd Int. Microsystems, Packag. Assem. Circuits Technol. Conf.*

Braun, T., Becker, K.-F., Piefke, K., Voges, S., Thomas, T., et al. (2011). 3D stacking approaches for mold embedded packages. In *Microelectron. packag. conf. (empc), 2011 18th eur.* (pp. 1–8). Brighton: IEEE.

Hopcroft, M. A., Nix, W. D. and Kenny, T. W. (2010). What is the Young's Modulus of Silicon? *J. Microelectromechanical Syst.* 19(2), 229–238.

Kim, T. H. (2012). Method of forming wafer level mold using glass fiber and wafer structure formed by the same. Google Patents.

Kumar, A., Dingwei, X., Sekhar, V., Lim, S., Keng, C., et al. (2009). Wafer level embedding technology for 3D wafer level embedded package. In *Electron. compo-*

nents technol. conf. 2009. ectc 2009. 59th (pp. 1289–1296). San Diego, CA: IEEE.

Mallik, A. and Stout, R. (2010). Simulation of warpage of silicon wafersusing ANSYS finite element analysis. In *Imaps, triangle 43rd int. symp.microelectron.* (pp. 486–493).

Mallik, A., Stout, R. and Ackaert, J. (2014). Finite-Element Simulation of Different Kinds of Wafer Warpages: Spherical, Cylindrical, and Saddle. *IEEE Trans. Components, Packag. Manuf. Technol.* 4(2), 240–247.

Matsutani, H. (2009). Compression molding solutions for various high end package and cost savings for standard package applications. In *Microelectron. packag. conf. 2009. empc 2009. eur.* (pp. 1–4). Rimini: IEEE.

Meyer, T., Ofner, G., Bradl, S., Brunnbauer, M. and Hagen, R. (2008). Embedded Wafer Level Ball Grid Array (eWLB). *2008 10th Electron. Packag. Technol. Conf.*

Sadeghinia, M., Jansen, K. M. B. and Ernst, L. J. (2012). Characterization and modeling the thermo-mechanical cure-dependent properties of epoxy molding compound. *Int. J. Adhes. Adhes.* 32, 82–88.

Souriau, J.-C., Lignier, O., Charrier, M. and Poupon, G. (2005). Wafer level processing of 3D system in package for RF and data application. *Proc. Electron. Components Technol. 2005. ECTC '05.*

Takahashi, Y., Dunne, R., Amagai, M., Koto, Y., Iriguchi, S., et al. (2012). Over Molding Process Development for a Stacked Wafer-level Chip Scale Package with Through Silicon Vias (TSVs). *Trans. Japan Inst. Electron. Packag.* 5(1), 122–131.

Timoshenko, S. (1925). Analysis of bi-metal thermostats. *J. Opt. Soc. Am.* 11(3), 233.

Tomita, Y., Sekihara, Y., Kubota, J., Ichikawa, K. and Sankman, B. (2012). Wafer Level Packaging to Address Future Direct Chip Attach Needs. *Trans. Japan Inst. Electron. Packag.* 5(1), 85–91.