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Enhancement-mode Metal-insulator-semiconductor GaN/AlInN/GaN Heterostructure Field Effect Transistors on Si with a Threshold Voltage of +3.0V and Blocking Voltage Above 1000V

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Enhancement-mode AlInN/GaN metal-insulator-semiconductor heterostructure field effect transistors on silicon substrates are reported. The fabricated devices exhibit a threshold voltage of +3V using a fluorine-based plasma treatment technique and gate dielectric. A drain current density of 295mA/mm at a gate bias of +10V is measured. An excellent off-state blocking voltage capability of 630V at leakage current of 1µA/mm and more than 1000V at 10µA/mm is achieved on a device with 20µm gate-drain separation at gate bias of 0V. The dynamic on-resistance is ~2.2 times the DC on-resistance when pulsing from off-state drain bias of 500V.

GaN-based heterostructure field effect transistors (HFETs), particularly AlGaN/GaN, have attracted much attention due to their potential to replace 600 to 1200V silicon-based power switching devices. Indeed, high-power and high-efficiency AlGaN/GaN power switches that exceed the performance of silicon devices have been demonstrated recently.[1-5] However, AlGaN/GaN devices often suffer from high electric field reliability issues such as the formation of leakage paths through the AlGaN barrier.[6] On the other hand, AlInN has emerged as a promising alternative to AlGaN as a barrier layer, capable of delivering high output current density and low on-resistance owing to its strong spontaneous polarization.[7-10] In addition, the AlInN alloy can be lattice-matched to GaN, which results in a strain-free barrier layer and potentially offers advantages over AlGaN/GaN in term of reliability. Several groups have reported enhancement-mode AlInN/GaN devices, but these devices exhibit a relatively low threshold voltages, V_{TH} (<+2V), and off-state blocking voltage (<350V). [11-13]

In this letter, we demonstrate enhancement mode metal-insulator-semiconductor AlInN/GaN HFETs (MISHFETs) on silicon substrates using a fluorine-plasma treatment technique.[14] V_{TH} as high as +3.0V and output current of 295mA/mm at a gate bias of +10V are measured. A device with 20µm gate-drain separation shows an off-state blocking voltage (BV) of 630V and >1000V with a leakage current at 1µA/mm and 10µA/mm, respectively.

Fig. 1 depicts the device structure of the AlInN/GaN HFETs. The structure was grown by metal-organic vapour phase epitaxy on a 6-inch diameter silicon substrate. After a 250nm AlN nucleation layer, a total of 7µm thick compositionally graded $Al_xGa_{1-x}N$ transition layer and carbon-doped GaN buffer layer were grown. Subsequently, a 250nm unintentionally doped (UID) GaN channel layer and a 2nm AlN spacer layer were grown, prior to the 11nm thick $Al_{0.84}In_{0.16}N$ barrier layer. Finally, the structure was capped with 2nm of GaN. The 6-

inch GaN-on-Si wafer shows a bow of ~30μm (concave). The X-ray diffraction rocking curve full width half maximum for (002) and (102) reflections were 520 and 940arcsec, respectively. A root mean square surface roughness of 0.73nm was measured using atomic force microscopy in a 5x5μm^2 scan area. A 2-dimensional electron gas (2DEG) density of $8.2x10^{12}cm^{-2}$ and an electron mobility of $1240cm^2V^{-1}s^{-1}$ were measured using the Hall technique.

For device fabrication, mesa isolation was performed using inductively coupled plasma etching with a Cl_2-based plasma. A Ti/Al/Ni/Au (20/120/20/45nm) metal stack was thermally evaporated and annealed at 830°C under N_2 ambient to form the source and drain ohmic contacts. A 100nm SiN_x passivation layer was deposited using plasma enhanced chemical vapour deposition (PECVD) and a 1.5μm gate window was opened by etching through the SiN_x layer using reactive ion etching (RIE). A CHF_3 plasma-treatment (RF power of 100W) in an RIE system was performed on the gate window to implant the fluorine and shift V_{TH} from negative to positive. A 20nm PECVD SiN_x layer was then deposited to serve as gate insulator prior to T-shape Ni/Au (20/180nm) gate metal deposition. A further 250nm SiN_x was deposited before the source-connected field plate and probe pad metal deposition. The devices have a 100μm gate width, gate-source separation of 2.5μm and gate-drain separation (L_{GD}) varying between 7 and 20μm.

Fig. 2(a) illustrates the gate transfer characteristics of the AlInN/GaN MISHFETs V_{TH} of ~+3.0V was linear extracted from the gate transfer characteristics. To our knowledge, this is the highest V_{TH} reported in enhancement-mode AlInN/GaN MISHFETs. The high V_{TH} is achieved by the combination of fluorine-based plasma treatment which depletes the 2DEG under the gate[14)] and the 20nm SiN_x gate dielectric. An output current of 295mA/mm was

measured at V_{GS}:+10V and gate current remained below 50nA/mm with the V_{GS} between -6V and +10V. An on-off ratio as high as ~$5x10^7$ was obtained. It is noted that a V_{TH} hysteresis of ~0.68V is observed from the bi-directional gate sweeps between -6 and +10V, which is likely caused by electron trapping in the acceptor-like states at the interface between the gate dielectric and GaN cap.[15,16)] This hysteresis effect may be alleviated by employing surface treatment techniques prior to gate dielectric deposition to reduce the interfacial traps.[16)] Fig. 2(b) shows the DC I-V characteristics of the AlInN/GaN MISHFET. The specific on-resistance ($R_{ON.SP}$) increases linearly with increasing gate-drain separation (L_{GD}). The $R_{ON.SP}$ of the device with L_{GD}:7, 12 and 20 μm is 2.1, 3.4 and 6.1mΩ.cm^2, respectively. ($R_{ON.SP}$ is calculated from the active area between the source and drain contacts and a 2μm contact transfer length extracted from TLM).

Fig. 3(a) shows the three-terminal off-state measurements of AlInN/GaN MISHFETs at V_{GS}: 0V. The sample was immersed in Fluorinert FC-40 to prevent surface flashover and the substrate was grounded during the measurements. The devices show an excellent voltage blocking capability with a BV as high as 606V at I_D:1μA/mm for L_{GD}: 7μm at V_{GS}: 0V. While the 7μm device showed a hard breakdown at 623V due to breakdown of the gate, no hard breakdown was observed up to 1000V for the device with L_{GD}: 20μm.

It is noted that the gate leakage current (I_{GATE}) dominates below 250V and leakage between source and drain terminals (I_{SOURCE}) surpasses I_{GATE} as V_{DS} increases beyond 250V. Fig. 3(b) shows the leakage current measured from the two-terminal lateral buffer leakage structure with ohmic contacts isolated with a mesa etch. The leakage current is more than an order of magnitude higher in the structure with partially etched UID GaN layer (etch depth of 100nm) compared to the structure with completely etched UID GaN layer (etch depth of 500nm).

This suggests that the I_{SOURCE} is primarily due to leakage via the 250nm UID GaN channel in the three terminal off-state measurements. Reducing the UID GaN channel thickness may reduce I_{SOURCE} and provide a better confinement of 2DEG within the channel. Unlike other reported GaN-on-Si transistors,[5,17)] the substrate leakage current ($I_{SUBSTRATE}$) is not the main leakage contribution and stays below 1μA/mm up to 1000 V due to the 7μm thick high resistive GaN buffer and AlGaN transition layers. The $R_{ON.SP}$ versus BV performance of our enhancement mode AlInN/GaN MISHFETs is compared with the reported AlInN and AlGaN MISHFETs in Fig. 4.

Dual-pulse measurements were carried out to characterize the dynamic on-resistance of the AlInN/GaN MISHFETs. The devices were held at V_{GS}:0V during the off-state and switched to V_{GS}: +8V during the on-state. During the off-state, V_{DS} up to 500V was applied and the dynamic on-resistance was measured at V_{DS}:0.5V during on-state. The duration of off-state and on-state were set at 500μs and 100μs, respectively and the substrate was grounded. Fig. 5 shows the ratio of dynamic on-resistance to DC on-resistance as a function of applied V_{DS}. The dynamic on-resistance increases with increasing off-state drain bias and is approximately 2.2 times the DC on-resistance at V_{DS}:500V, attributable to field-assisted charge trapping on the surface and/or in the carbon-doped GaN buffer region between the gate and the drain.[18,19)] Optimization of the field-plate geometry as well as improvement of the GaN buffer design may further reduce the dynamic on-resistance of the devices.

In summary, enhancement-mode AlInN/GaN MISHFETs with a threshold voltage of +3.0V and a blocking voltage of more than 600V at leakage current of 1μA/mm and 1000V at leakage current of 10μA/mm have been demonstrated using a 6-inch silicon substrate. This is, to our knowledge, the highest threshold voltage and blocking voltage reported in the

enhancement-mode AlInN/GaN MISHFETs. Pulsed measurements reveal that the dynamic on-resistance of the AlInN/GaN MISHFETs is nearly 2.2 times the DC value with the incorporation of field plate. These results suggest the excellent potential of AlInN/GaN MISHFETs for power switching applications.

Acknowledgments

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Figure Captions

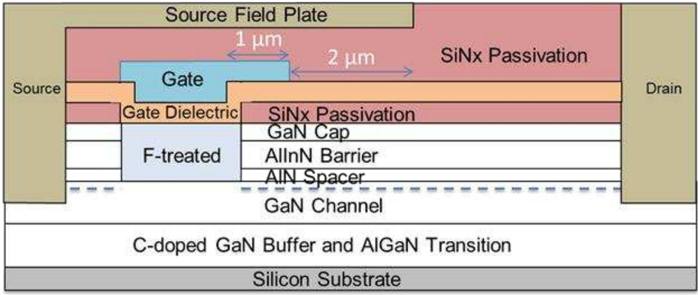
Fig. 1. The device structure of AlInN/GaN MISHFETs.

Fig. 2. (a) Gate transfer characteristic of the enhancement mode AlInN/GaN MISHFET (L_{GD}: 12μm) with a threshold voltage of +3V (V_{GS} sweeps from -6V to +10V). The inset shows the gate (squares) and drain currents (circles) on a semi-logarithm-scale. (b) I-V characteristics of the AlInN/GaN MISHFET with L_{GD}: 12μm.

Fig. 3. (a) Three-terminal off-state measurements of enhancement mode AlInN/GaN MISHFETs at V_{GS}: 0V with varying L_{GD}. The substrate was grounded during the measurements. Inset shows the individual components of off-state leakage current measured at drain, source, gate and substrate terminals of the AlInN/GaN MISHFET with L_{GD}: 20μm. (b) Leakage current measured from two-terminal lateral buffer leakage structure with a mesa isolation etch depth of 100 and 500nm. The gap spacing between the isolated pads is 15μm. The substrate was grounded during the measurements.

Fig. 4. Benchmark of $R_{ON.SP}$ versus BV of AlInN/GaN MISHFETs and enhancement-mode AlGaN/GaN MISHFETs.

Fig. 5. Ratio of dynamic R_{ON} to DC R_{ON} of enhancement-mode AlInN/GaN MISHFETs (L_{GD}: 20 μm) as function of V_{DS}.



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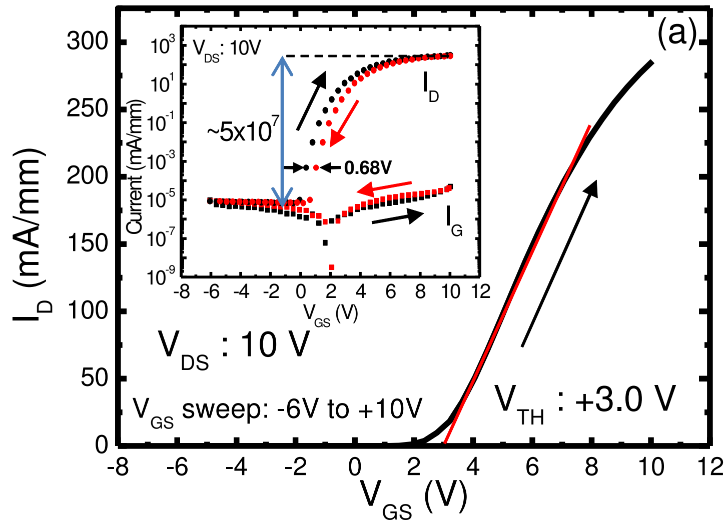


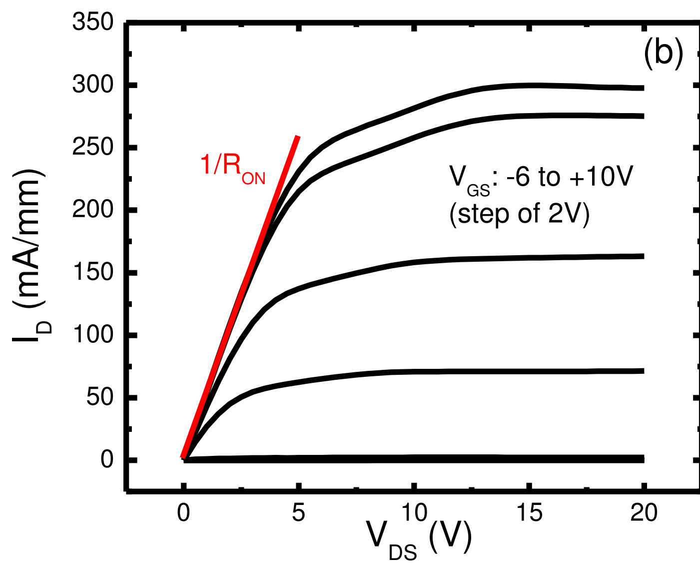
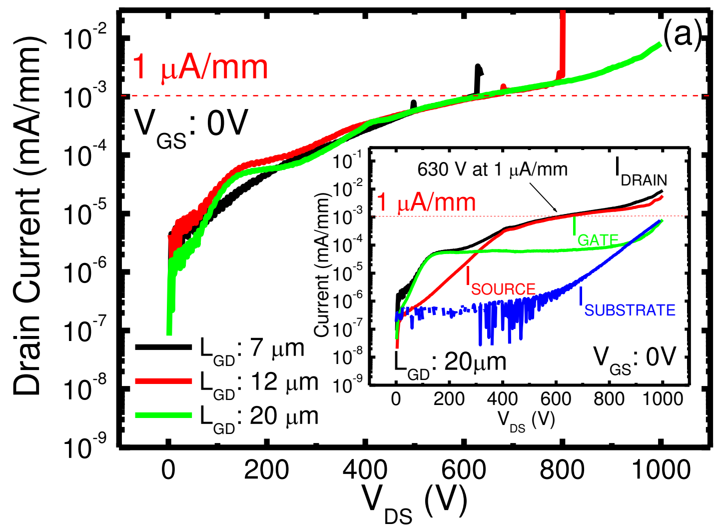


Fig. 2.



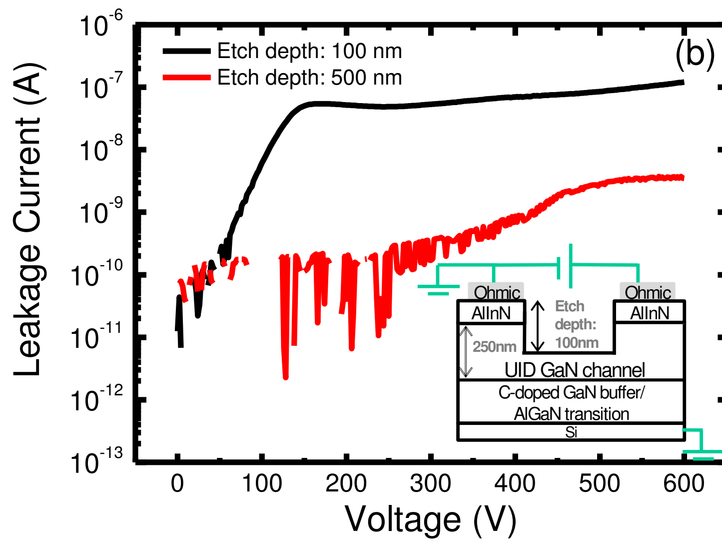


Fig. 3.

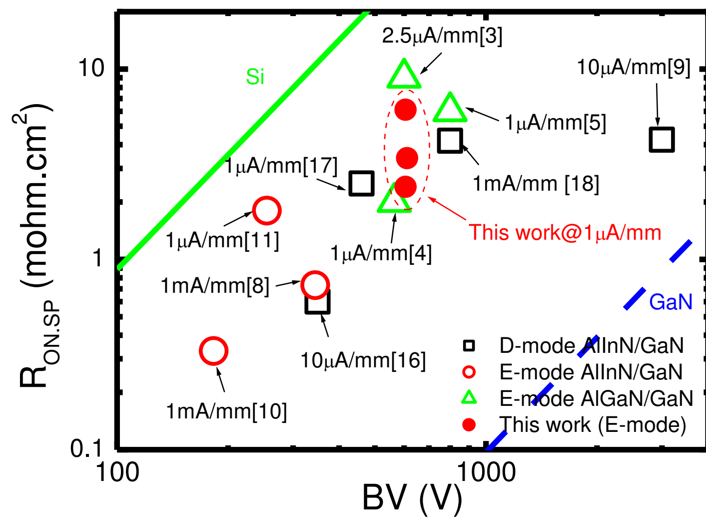


Fig. 4.

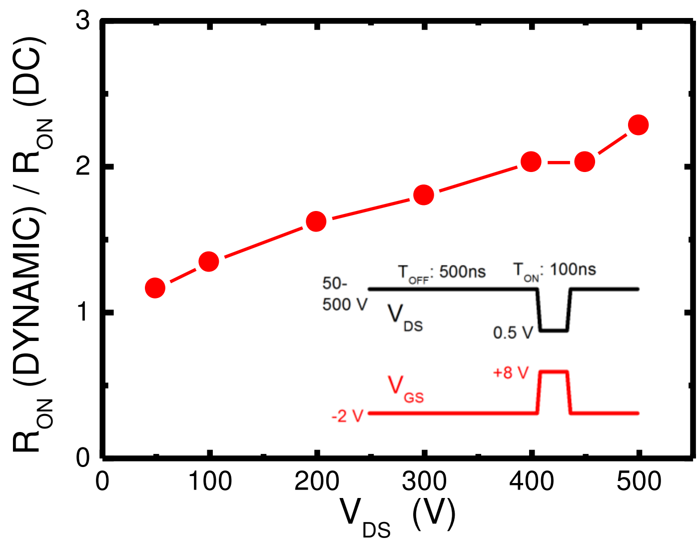


Fig. 5.