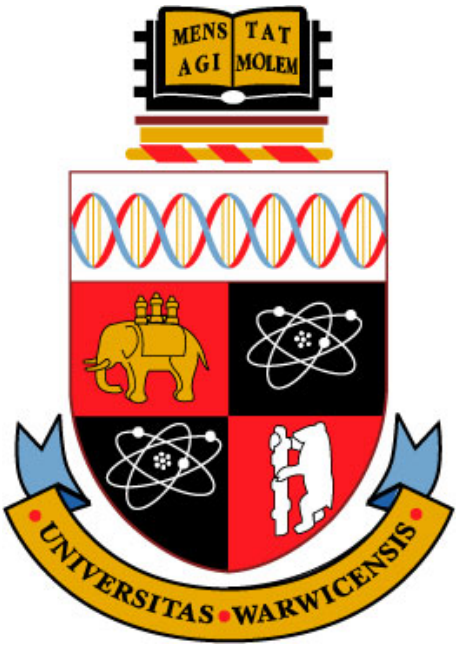
Analysis of Dynamic Performance and Robustness of Silicon and SiC Power Electronics Devices



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Declaration

This thesis is submitted to the University of Warwick in support of the application for the degree of Doctor of Philosophy. It has not been submitted in part, or in whole, for a degree or other qualification at any other University. Parts of this thesis are published by the author in peer-reviewed research papers listed. Apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work described in this thesis is carried out by the author in School of Engineering of University of Warwick.

S. Jahdi
2012 - 2016

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Publications List

Journal Papers:

Chapter 3:

1. **S. Jahdi**, O. Alatise, C. A. Fisher, L. Ran and P. A. Mawby

   'An Evaluation of Silicon Carbide Unipolar Technologies for Electric Vehicle Drivetrains'

   IEEE Journal *of Emerging and Selected Topics in Power Electronics*, volume 2, no. 3, pp. 517, 528, September 2014.

Chapter 4:

2. **S. Jahdi**, O. Alatise, L. Ran and P. A. Mawby

   'Accurate Analytical Modeling for Switching Energy of PiN Diodes Reverse Recovery'

   IEEE Transactions *on Industrial Electronics*, volume 62, no. 3, pp. 1461, 1470, March 2015.

3. **S. Jahdi**, O. Alatise, P. Alexakis, L. Ran and P. A. Mawby

   'The Impact of Temperature and Switching Rate on the Dynamic Characteristics of Silicon Carbide Schottky Barrier Diodes and MOSFETs'

   IEEE Transactions *on Industrial Electronics*, volume 62, no. 1, pp. 163, 171, January 2015.

4. **S. Jahdi**, O. Alatise, L. Ran and P. A. Mawby

   'Analytical Modelling of Switching Energy of Silicon Carbide Schottky Diodes as Functions of dI_{DS}/dt and Temperature'

   IEEE Transactions *on Power Electronics*, volume 30, no. 6, pp. 3345, 3355, June 2015.

Chapter 5:

5. **S. Jahdi**, O. Alatise, R. Bonyadi, P. Alexakis, C. A. Fisher, J. A. Ortiz Gonzalez, L. Ran and P. A. Mawby

   'An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation'

   IEEE Transactions *on Power Electronics*, volume 30, no. 5, pp. 2383, 2394, May 2015.

Chapter 6:

6. **S. Jahdi**, O. Alatise, J. A. Ortiz Gonzalez, R. Bonyadi, L. Ran and P. A. Mawby

   'Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules'

   IEEE Transactions *on Industrial Electronics*, volume 63, no. 2, pp. 849, 863, February 2016.

Other publications also from this thesis:

7. **S. Jahdi**, O. Alatise, J. A. Ortiz Gonzalez, L. Ran and P. A. Mawby

   'Comparative Analysis of False Turn-ON in Si-Bipolar and SiC-Unipolar Devices'

   Presented at the *IEEE Energy Conversion Congress and Exposition (ECCE'15)*, pp. 2239, 2246, Montreal, Canada, 20-24 September 2015.

8. **S. Jahdi**, O. Alatise, J. A. Ortiz Gonzalez, P. Gammon, L. Ran and P. A. Mawby

   'Investigation of Parasitic Turn-ON in Silicon IGBT and SiC MOSFET Devices'

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9. **S. Jahdi**, O. Alatise, P. Alexakis and P. A. Mawby

   'Electrothermal Modeling and Characterization of SiC Schottky and Silicon PiN Diodes Switching Transients'

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10. **S. Jahdi**, O. Alatise and P. A. Mawby

    'Modeling of Turn-off Transient Energy in IGBT Controlled Silicon PiN Diodes'

    Presented at the *IEEE Power Electronics and Applications (EPE'14-ECCE Europe)*, 16$^{\text{th}}$ European Conference, Lappeenranta, Finland, 26-28 August 2014.

11. **S. Jahdi**, O. Alatise and P. A. Mawby

    'Temperature and dI_{DS}/dt Dependence of the Switching Energy of SiC Schottky Diodes in Clamped Inductive Switching Applications'

    Presented at the *International Silicon Carbide and Related Materials Conference (ICSCRM)*, Volume 778, 780, pp. 816, 819, Miyazaki, Japan, 1-4 October 2013.

12. **S. Jahdi**, O. Alatise and P. A. Mawby

    'The Impact of SiC Technology on Grid-connected Distributed Energy Resources'

    Presented at the *IEEE Innovative Smart Grid Technologies Europe Conference, 4th ISGT Europe*, pp. 1, 5, Copenhagen, Denmark, 6-9 October 2013.

13. **S. Jahdi**, O. Alatise and P. A. Mawby

    'On Performance of Voltage Source Converters based on Silicon Carbide Technology'

    Presented at the *IEEE Telecommunications Energy Conference, 35th INTELEC International*, pp. 1, 6, Hamburg, Germany, 13-17 October 2013.

Abstract

The emergence of SiC power devices requires evaluation of benefits and issues of the technology in applications. This is important since SiC power devices are still not as mature as their silicon counterparts. This research, in its own capacity, highlights some of the major challenges and analyzes them through extensive experimental measurements which are performed in many different conditions seeking to emulate various applications scenarios. It is shown that fast SiC unipolar devices, inherently reduce the switching losses while maintain low conduction losses comparable with contemporary bipolar technologies. This translates into lower temperature excursions and an enhanced conversion efficiency. However, such high switching rates may trigger problems in the device utilizations.

The switching rates influenced by the device input capacitance can cause significant ringing in the output, especially in SiC SBDs. Measurements show that switching rate of MOSFETs increases with increasing temperature in turn on and reduces in turn off. Hence, the peak voltage overshoot and oscillation severity of the SiC SBD increases with temperature during diode turn off. This temperature dependence reduces at the higher switching rates. So accurate analytical models are developed for predicting the switching energy in unipolar SiC SBDs and MOSFET pairs and bipolar silicon PiN and IGBT pairs.

A key parameter for power devices is electrothermal robustness. SiC MOSFETs have already demonstrated such merits compared to silicon IGBTs, however not for MOSFET body diodes. This research has quantified this in comparison with the similarly rated contemporary device technologies like CoolMOS. In a power MOSFET, high switching rates coupled with the capacitance of drain and body causes a displacement current in the resistive path of P body, inducing a voltage on base of the parasitic NPN BJT which might forward bias it. This may lead to latch up and destruction if the thermal limits are surpassed. Hence, trade offs between switching energy and electrothermal robustness are explored for the silicon, SiC and superjunction power MOSFETs. Measurements show that performance of body diodes of SiC MOSFETs is the most efficient due to least reverse recovery. The minimum forward current for inducing dynamic latch up decreases with increasing voltage, switching rate and temperature for all technologies. The CoolMOS exhibited the largest latch up current followed by the SiC and silicon power MOSFETs.

Another problem induced by high switching rates is the electrical coupling between complementing devices in the same phase leg which manifests as short circuits across the DC link voltage. This has been understood for silicon IGBTs with known corrective techniques, however it is seen that due to smaller Miller capacitance resulting from a smaller die area, the SiC module exhibits smaller shoot through currents in spite of higher switching rates and a lower threshold voltage. Measurements show that the shoot through current exhibits a positive temperature coefficient for both technologies the magnitude of which is higher for the silicon IGBT. The effectiveness of common techniques of mitigating shoot through is also evaluated, showing that solutions are less effective for SiC MOSFET because of the lower threshold voltages and smaller margins for a negative gate bias.

List of Abbreviations and Symbols

AC	Alternating current
BJT	Bipolar junction transistor
CMF	Channel length modulation factor
CSC	Current source converter
CTE	Coefficient of thermal expansion
DC	Direct current
DIBL	Drain induced barrier lowering
DMOS	Double diffused metal oxide semiconductor
DUT	Device under test
EV	Electric vehicle
FACTS	Flexible AC transmission system
FWD	Free wheeling diode
GTO	Gate turn-off thyristor
HB	Half bridge
HEV	Hybrid electric vehicle
HV	High voltage
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
IGCT	Insulated gate-commutated thyristor
JFET	Junction field effect transistor
JTE	Junction termination extension
KCL	Kirchhoff current law
KVL	Kirchhoff voltage law
LCC	Line commutated conversion
LV	Low voltage
MEA	More electric aircraft
MMC	Modular multilevel converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-channel metal oxide semiconductor

NPC	Neutral point clamped
NPT	Non punch-through
PCB	Printed circuit board
PT	Punch-through
PWM	Pulse width modulation
SBD	Schottky barrier diode
SCC	Self commutated conversion
SCR	Silicon controlled rectifier
SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
THIPWM	Third harmonic pulse width modulation
TRIPWM	Triple harmonic injection pulse width modulation
UMOS	U-Channel (Trench) MOSFET
VDMOS	Vertical diffused metal oxide semiconductor
VSC	Voltage source converter
WBG	Wide bang-gap
ZCS	Zero current switching
ZVS	Zero voltage switching

Al	Aluminium
Au	Gold
B	Boron
C	Carbon
GaN	Gallium nitride
P	Phosphorous
Pt	Platinum
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide

A	Conduction area (cm^2)
A^*	Richardson constant (A/cm^2-K^2)
BV	Breakdown voltage (V)
C_{AK}	Average diode depletion capacitance (F)
C_{DS}	MOSFET drain-source capacitance (F)
C_{GD}	MOSFET Miller capacitance (F)
C_{GS}	MOSFET gate-source capacitance (F)
C_{iss}	MOSFET input capacitance (F)
C_{OX}	MOSFET oxide effective capacitance density ($fF/\mu m^2$)

cp	Cell pitch width (m)
D	Diffusion constant (m^2/s)
$d^2I_{\mathrm{TF}}/dtdT$	Primary dI/dt of recovery current (A/s°C)
D_n	Diffusion constant of electrons (m^2/s)
D_p	Diffusion constant of holes (m^2/s)
dI_{RR}/dt	Primary dI/dt of recovery current (A/s)
dI_{Tail}/dt	Secondary dI/dt of recovery tail current (A/s)
$dI_{\mathrm{TF+}}/dt$	The dI/dt of turn-off current before zero-crossing (A/s)
$dI_{\mathrm{TF\text{-}}}/dt$	The dI/dt of turn-off current after zero-crossing (A/s)
dI_{TF}/dt	Overall dI/dt of turn-off current at high dI/dt (A/s)
dV_{AK}/dt	The dV/dt of diode (V/s)
dV_{DS}/dt	The dV/dt of MOSFET (V/s)
E_{F}	Fermi level energy (eV)
E_{g}	Bandgap energy (eV)
E_C	Bottom edge of conduction band (eV)
E_i	Energy level of intrinsic semiconductor (eV)
E_V	Top edge of valence band (eV)
E_{SW}	Switching energy (J)
g_{fs}	Transconductance (S)
G_{th}	Generation rate ($cm^{-3}s^{-1}$)
I_{AK}	Diode current (A)
I_{DS}	MOSFET current (A)
I_F	Diode forward current (A)
I_G	Gate current (A)
I_{PR}	SBD diode peak reverse current (A)
I_{RR}	PiN diode peak reverse recovery current (A)
I_S	Leakage current (A)
J	Current density (A/cm^2)
J_n	Current density of electrons (A/cm^2)
J_p	Current density of holes (A/cm^2)
J_S	Leakage current density (A/cm^2)
K	Net recombination rate constant (–)
k	Boltzmann constant (J/K)
L	MOSFET channel length (m)
L_{Cr}	Circuit stray inductance (H)
L_E	Circuit energizing inductor (H)
L_G	MOSFET gate stray inductance (H)
L_n	Diffusion length of electrons (m)
L_p	Diffusion length of holes (m)
L_{Stray}	Stray parasitic inductance (H)
L_S	MOSFET source stray inductance (H)

n	Density of n-type carriers (cm^{-3})
N_C	Density of conduction band energy state (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
N_V	Density of valence band energy state (cm^{-3})
n_0	Density of n-type carriers in equilibrium (cm^{-3})
N_A	Density of acceptors (cm^{-3})
N_A^-	Density of ionized acceptors (cm^{-3})
N_D	Density of donors (cm^{-3})
N_D^+	Density of ionized donors (cm^{-3})
n_{p0}	Electron concentration in P-type semiconductor in equilibrium (cm^{-3})
p	Density of p-type carriers (cm^{-3})
p_0	Density of p-type carriers in equilibrium (cm^{-3})
p_{n0}	Hole concentration in N-type semiconductor in equilibrium (cm^{-3})
q	Electrical charge (C)
Q_F	Stored charge in the drift region (C)
Q_{inv}	Channel inversion charge (C)
q_{iss}	Input capacitance charge (C)
Q_{ox}	Fixed oxide charge (C)
Q_{rr}	Reverse recovery charge (C)
R_{AK}	Average diode depletion resistance (Ω)
R_{Cr}	Circuit parasitic resistance (Ω)
R_G	Gate resistance (Ω)
R_{on}	Specific on-resistance (Ω-cm^2)
R_S	Parasitic series resistance (Ω)
R_{th}	Recombination rate ($cm^{-3}s^{-1}$)
S	Ratio of recovery time to turn-off time as a measure of diode snappiness (–)
T	Temperature (°C)
t	Time (s)
T_m	Time of maximum voltage peak (s)
t_{ox}	Oxide thickness (cm)
t_{SW}	Duration of switching (s)
U	Net recombination rate (cm^{-3}/s)
V	Switching voltage (V)
V_0	Built-in potential of PN junction (V)
V_{AKpk}	Peak diode voltage overshoot (V)
V_{AK}	Diode voltage (V)
$V_{bi-N^-N^+}$	Voltage drop across N^-N^+ junction (V)
$V_{bi-P^+N^-}$	Voltage drop across P^+N^- junction (V)
V_{bi}	Junction built-in potential (V)
V_{BR}	Breakdown voltage (V)
V_{CE}	IGBT collector-emitter voltage (V)

V_{CH}	Voltage drop on MOSFET channel (V)
V_{DD}	Supply (input) voltage (V)
V_{Drift}	Voltage drop across drift region (V)
V_{DS}	Drain-Source voltage (V)
V_d	Diode on-state voltage drop (V)
V_{FB}	Flatband voltage (V)
V_{GG}	MOSFET applied gate voltage (V)
V_{GP}	Plateau voltage (V)
V_{GS}	MOSFET gate source voltage (V)
V_m	Maximum voltage peak (V)
V_n	Average speed of electrons (cm/s)
V_p	Average speed of holes (cm/s)
V_R	Reverse voltage (V)
V_{TH}	Threshold voltage of MOSFET gate (V)
W	MOSFET channel width (m)
W_D	Width of drift region (m)

α_I	Current Neper frequency (rad/s)
α_V	Voltage Neper frequency (rad/s)
χ	Electron affinity (ev)
λ_{th}	Thermal conductivity (W/cm-K)
$\mathscr{E}$	Electric field (V-cm)
$\mathscr{E}_C$	Critical electric field (V-cm)
$\mathscr{E}_{BR}$	Breakdown field (V-cm)
μ_n	Electron mobility (cm^2/V-s)
μ_p	Hole mobility (cm^2/V-s)
ω	Oscillations (swing) frequency (rad/s)
Φ_{bi}	Schottky barrier potential (eV)
Φ_{bn}	Schottky barrier height (eV)
Φ_m	Work function of the metal (eV)
Φ_s	Work function of the semiconductor (eV)
τ_n	Carrier lifetime for electrons (s)
τ_p	Carrier lifetime for holes (s)
υ	Velocity (cm/s)
υ_{sat}	Carrier saturation velocity (cm/s)
ε_0	Vacuum permittivity (F/m)
ε_r	Relative dielectric constant (–)
ε_{ox}	Oxide dielectric constant (F/m)
ζ	Damping factor of diode responde (–)

Chapter

1 Introduction

1.1 Background and Motivation

SiC power devices have opened up new avenues in the field of power electronics. The first developed SiC devices were the SiC Schottky barrier diodes (SBD) in the early 2000's and later on, normally-on SiC JFETs were also developed and became available. However the main breakthrough came when CREE®, as today's leader in manufacturing SiC power devices, announced the first commercially available SiC MOSFET in 17 January 2011 [1]. Since then, the implementation of SiC power devices in commercial applications have been hindered by not only the cost of the devices but the lack of confidence in their reliability and controllability. Silicon technology has several decades of reliability analysis and understanding, hence, it will not be easy to displace silicon even if the technical advantages of doing so are overwhelming. Unlike the microelectronics industry where new technologies are implemented rapidly, power electronics applications require a higher threshold of confidence because of the high maintenance costs and the severe consequences of device failure. The industries involved in high levels of electrical power are conservative

and will not adopt new technologies rapidly. For instance, electric vehicle drive-trains currently use 3-phase voltage source converters to convert DC power from the lithium ion battery to 3-phase AC for the traction permanent magnet synchronous motor. In the Toyota® Prius™, for example, the DC bus voltage ranges from 600 V to 800 V, and it uses 600 A silicon IGBTs with a typical switching frequency of 5 kHz [2]. SiC power MOSFETs are thus capable of replacing IGBTs thereby reducing the weight and size of the passive components and increasing the power efficiency of the drive-train. To this end, Mitsubishi® has presented a 300 A single die SiC power MOSFET for the purpose of electric vehicle and rail traction drive-train applications. However, these have not been yet implemented in practice on basis usually not disclosed for commercial reasons.

Therefore, if SiC technology is to penetrate key application spaces like electric drive-trains for hybrid/full electric vehicles, converters for electrically controlled ships, power conversion in the more-electric-aircraft (MEA), on-shore/off-shore wind conversion or distribution level power electronics, high voltage grid connected power converters in the HVDC/FACTS or lower voltage converters for photovoltaic systems, then the control, operation and reliability of SiC devices must be demystified. The failure mechanisms and consequences of increased power density must also be completely understood.

To this end, the research in this thesis is oriented towards testing and characterizing SiC power devices in circuits and understanding the practicalities involved in driving the devices in the presence of parasitic components. The advantages of SiC as a power semiconductor material have been relatively well researched and understood. However, implementing SiC power devices in practical circuits and expediting those advantages requires further investigation. For instance, it is often stated that high switching frequencies enabled by SiC MOSFETs can increase power density of power converters by reducing the size of the passive components; however, the occurrence of electromagnetic oscillations,

ringing, crosstalk induced short circuits and dV/dt induced dynamic latch-up hinders the actualization of such switching frequencies.

1.2 Thesis Outline

This thesis is divided into seven chapters, the first of which is this short introductory chapter. Next, chapter 2 discusses the basic fundamentals of semiconductor devices and the structure of the most common power devices along with material properties of SiC.

Following this, chapter 3 is provided which underpins subsequent chapters by analyzing the switching performance of SiC MOSFETs and diodes as well as simulating an application case where the advantages can be exploited. In this regard, a pair of SiC unipolar devices (SiC MOSFET and SiC Schottky barrier diode) are tested along with contemporary silicon bipolar devices (Si-IGBT and silicon PiN diode). These measurements are performed over a range of temperatures from –75 °C and 175 °C and over a wide range of gate resistances to control the switching rates. The measurements show advantages of SiC devices in terms of switching energy and faster transients. The results of these measurements are used in a model to showcase possible enhancements in conversion efficiency and temperature rise of a given converter using silicon and SiC devices.

Using the measurements obtained in chapter 3, chapter 4 addresses interesting trends visible in the devices transients. These are mainly the reverse recovery in PiN diodes, and more interestingly, the ringing in the output voltage of the SiC SBDs. These oscillations, can be seen as one of the major disadvantages of fast unipolar SiC devices, which must be considered when they are used in a power application. Models have been developed for the accurate estimation of the switching energy of the devices as a function of the switching rate and ambient temperature.

Chapter 5 investigates how the body diode of SiC MOSFETs performs in terms of switching energy, the switching rate and robustness under hard commutation compared with silicon counterparts of different technologies.

Next, chapter 6 addresses another major issue in the application of SiC MOSFETs, which is the false turn-on or crosstalk. This is a point of concern since crosstalk is exacerbated by fast switching which is the key selling point of SiC technology. Hence, the effectiveness of the common mitigation techniques developed for silicon IGBTs is analyzed for SiC MOSFET modules.

Lastly, chapter 7 discusses the conclusions arising from the findings of this thesis, and proposes future work.

Chapter

2 Power Electronics and Silicon Carbide

The traditional electrical grid system is comprised of a network of fossil fuelled powered AC synchronous generators sending power through high voltage transmission lines and low voltage distribution lines. Power flow was unidirectional from centralised producers to passive consumers, hence power electronics was not necessary for power conversion. However, the dual needs of energy independence and de-carbonisation of industrial economies has increased the presence of green energy sources like wind and solar. Furthermore, distributed generators connected in the low voltage distribution systems has accelerated the de-centralisation of the electrical grid. Green energy sources like off-shore/on-shore wind and solar/photo-voltaic systems require power electronics converters for the conditioning of AC power into fixed voltage and fixed frequency necessary for seamless grid interface. HVDC systems are based on power electronics needed for converting power either in the form of line-commuted current-sourced converter or self-commutated voltage-sourced converters. Additionally, FACTS technologies like static VAR compensators (SVC) and static compensators (STATCOM) are increasingly reliant on power electronics.

2.1 Power Electronics in Power Systems

Power electronics (PE) is the appellation used to describe a broad range of technologies aiming the conversion of electrical power into different forms, mainly by the use of power semiconductor devices. Power electronic circuits are used today in various applications, from the low voltage home appliances and medium voltage applications such as electric vehicles to very high voltage applications for transmission systems. As far as power electronic converters are concerned, they can be classified according to the nature of the DC interface and according to how commutation between the switches occur. If the DC current is constant and the direction of power flow depends on the polarity of the DC voltage, then the converter is classified as a current-sourced converter (CSC) and DC is usually interfaced with a large reactor. Likewise, if the DC voltage is constant and the direction of power flow depends on the polarity of the DC current, then the converter is classified as a voltage-sourced converter (VSC) and the DC is interfaced through a capacitor. If phase to phase commutation occurs at the instigation of the field reversal of the power systems AC voltage, then the converter is line commutated (LCC) whereas if it occurs at the instigation of the switching of the devices, then it is a self-commutated converter (SCC).

2.1.1 Line Commutated Current-Sourced Converters

Because current-sourced converters require power semiconductor devices with bi-directional voltage blocking capability, they are implemented using Thyristors. Thyristors are 4 layered devices with 3 PN junctions, 2 of which block both polarities while the last junction modulates conductivity through a gate trigger. Due to the fact that voltage-sourced

transistors (MOSFETs or IGBTs) have 2 PN junctions, they can block voltages in one direction only, hence are not preferred candidates for current-sourced converters (excluding IGBTs with termination on both junctions). Traditional Thyristors lacked self-turn-off capability hence, were deployed in line commutated converters where the AC system voltage forced commutation between the switches. However, modern Thyristors like GTOs and IGCTs have self turn-off capability, hence can be used in self-commutated converters.

Thyristors are usually implemented as whole wafers in pressured packages stacked in series to achieve high blocking voltage capability. These are called Thyristor valve stacks and are used to replace the earlier mercury arc valves in the earliest forms of high power converters. As shown in the Figure 2.1, the vacuum valves (or Mercury arc valves) were among the first switches used for LCC-HVDC transmission. While these valves were relatively robust in terms of their power handling capability, but they were not the most efficient and high losses were common in their usage. Hence, with later developments, the LCC switches became dominated by Thyristor valves. The LCC transmission can be implemented in a 6-pulse configuration with a 60° phase shift as in the traditional Graetz bridge, or in a 12-pulse configuration with a 30° phase shift by cascading 2 Graetz bridges with a star-to-delta transformer for the phase shifting. The former has a simpler structure and does not require a three-phase power transformer, but has a high harmonics output and is therefore not practical. Consequently, the latter is the most widely used structure in LCC-HVDC systems today. Line commutated converters have the advantage of high efficiency however, they operate only at lagging power factor since the system voltage must precede current flow. Furthermore LCCs cannot operate in weak AC systems, hence, are incapable of black-start since synchronous voltages are required for phase commutation. These disadvantages are overcome in self-commutated converters.

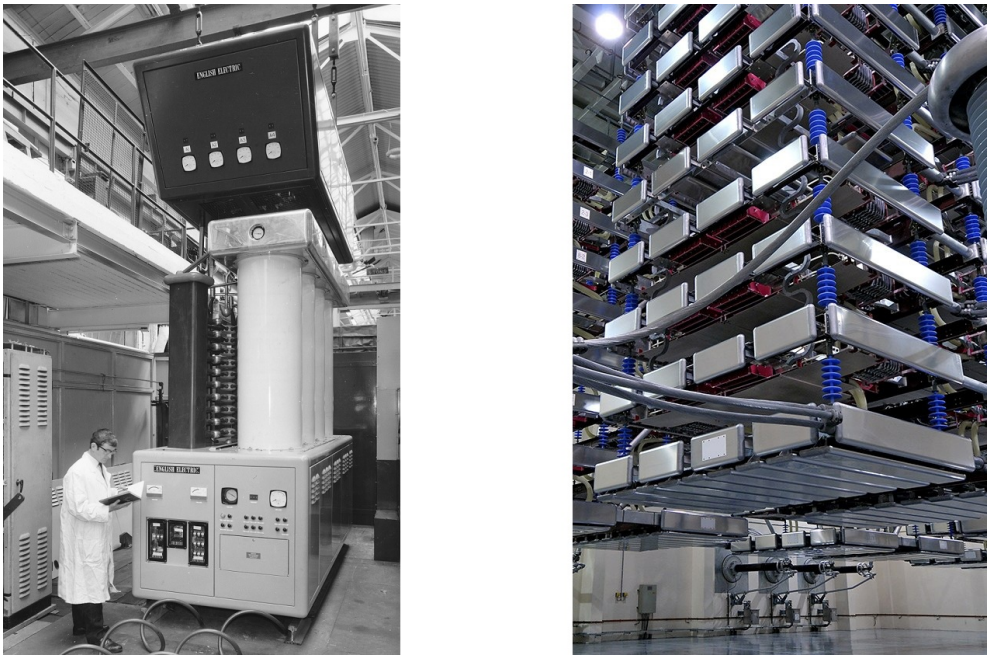


Figure 2.1: Vacuum valves in 1969 and Thyristor valves in 2014 for LCC HVDC (Pictures courtesy of GE Grid Solutions® - Formerly Alstom Grid®).

2.1.2 Self Commutated Voltage-Sourced Converters

Since the DC voltage is constant, voltage-sourced converters require power semiconductor devices capable of bi-directional current conduction, hence, a transistor with an anti-parallel reverse conducting diode is the prime candidate in the VSCs. Unlike traditional Thyristors, transistors have self-turn-off capability and are therefore capable of self-commutation. Phase-to-phase current commutation consequently occurs at the instigation of the power devices switching, hence, VSCs can switch at frequencies significantly higher than the system frequency (50 or 60 Hz). This means self commutated VSCs can invert and rectify at leading and lagging power factor as well as being capable of black-starting since the system voltage is not required for phase commutation.

The VSCs are of different topologies; the simplest one of which is the two-level converter, which compromises of only 6 switches (2 per phase) and as the name implies,

provides two levels of output voltage. The output of this topology, however, has a high degree of harmonics and is not acceptable for applications such as HVDC systems. To reduce the degree of harmonics, a pulse-width-modulation technique can be employed, which produces an output closer to that of a sinusoidal waveform; however this happens at the expense of higher switching frequencies which corresponds to higher switching losses. An alternative solution has been increasing the number of levels in the VSC an example of which is the 3-level neutral-point-clamped converter. This topology will be used in later stages of discussion for evaluation of power devices in applications. Increasing the number of levels significantly reduces the harmonics and by increasing it to very high values, the harmonics are reduced to the extent that no further filtering is required. For instance, a 23-level converter generates less than 1% harmonics on the output, which is ideal. However, increasing the number of levels of a converter proportionally increases the complexity of the system, and control of drivers becomes very difficult. The Modular Multi-level Converter (MMC) has thus been developed as a technique of producing highly sinusoidal waveforms that require minimum filtering with low switching frequencies.

2.1.3 Electric Vehicles and Traction Systems

Power electronics have had a very significant impact on electrifying transportation and reducing carbon emissions from fossil fuel powered internal combustion engines. DC power from lithium ion batteries is converted into AC power for the synchronous machines needed for traction. This can be achieved, for example, by using a 2-level 3-phase voltage-sourced converter comprised of silicon IGBTs and reverse conducting PiN diodes. The switching frequency used is several kHz and the switching losses generated are mainly due to tail currents in the IGBTs, conduction losses in the IGBT and reverse recovery currents in

the PiN diodes. There is currently significant research into improving the conversion efficiency of these converters where wide bandgap semiconductors are expected to play a prominent role in future electric vehicle drive-trains.

2.2 Power Semiconductor Devices

Depending on the application, power electronics converters will require power devices with different characteristics. Usually, applications that require high voltage rating power devices switch at low frequencies while those that require low voltage rated power devices switch at higher frequencies. Examples of the former include LCC converters that switch at system frequency and require Thyristors with voltage blocking capabilities well into several kVs while examples of the latter include switched mode power supplies that require IGBTs and MOSFETs that switch at several kHz. In the past few decades, there have been significant advances in the manufacturing process of power semiconductor devices, which are, as of today, mostly fabricated using silicon as the main substrate. Medium voltage applications like electric vehicle drive-trains are typically implemented in power devices with intermediate switching capabilities. Figure 2.2 shows the voltage/current handling rating of different power devices together with the switching frequency capability [3].

The trend of industrial and academic research is geared towards developing high frequency devices capable of blocking higher voltages and/or getting devices with high voltage blocking capabilities to switch faster. Since self-commutated VSCs are preferable to line commutated CSCs, the preferred device for technology development are fully controllable self turn-off power devices such as IGBTs and MOSFETs instead of semi-controlled devices like Thyristors. High voltage devices are traditionally bipolar technologies like Thyristors and IGBTs that use conductivity modulation to achieve low conduction losses,

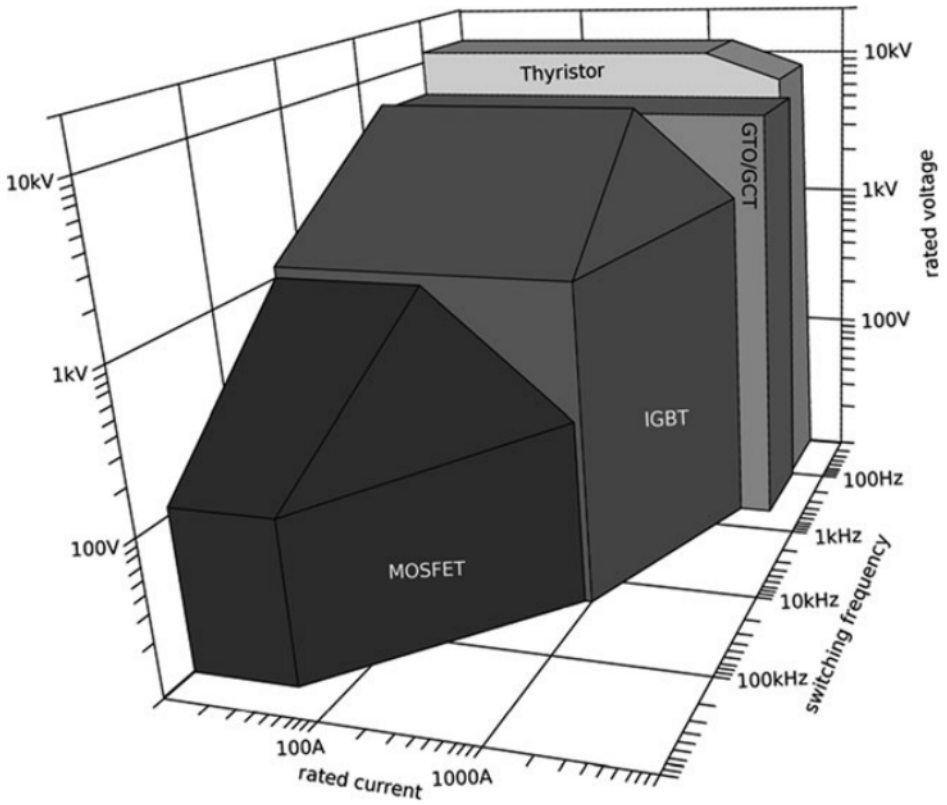


Figure 2.2: Power devices capability in terms of voltage, current and frequency [3].

however at the expense of slow switching rates resulting from minority carrier lifetime. Traditional unipolar devices usually do not fit the requirements for high voltage applications because the thick and highly resistive drift region required for voltage blocking contributes to significant conduction losses. However, low voltage devices are typically unipolar technologies that take advantage of the absence of minority carriers to achieve high frequency operation. Be that as it may, wide bandgap technologies are developed to merge high frequency operation with high voltage blocking. Silicon carbide unipolar power MOSFETs are being developed with voltage ratings as high as 10 kV [4] and with comparable if not lower conduction losses than IGBTs. Hence, the goal of research into wide bandgap technologies is to change Figure 2.2 by pushing MOSFETs more into power levels traditionally reserved for IGBTs and by pushing IGBTs into Thyristor domains.

2.2.1 Fundamentals of Semiconductor Physics

The fundamental operating principle of all semiconductor devices is the P-N junction. A P-N junction, as the name implies, is a junction between a P-type semiconductor and an N-type semiconductor. These two types of semiconductors are developed by adding impurity atoms to an *intrinsic* semiconductor, like silicon. An intrinsic semiconductor is a material with a defined band gap (E_g) with an electrical resistivity between that of metals and insulators. This band gap is a forbidden band between its valance band and the conduction band and is the energy required for an electron to move from the former to the latter. The conductivity of a given material is in direct relation to its band gap. For example, in most metals the bandgap is nearly non-existent as the valence band and the conduction band are very close and even overlap. In insulators the bandgap is very high, therefore it is very difficult for an electron to move to the conduction band, unless a very high voltage (causing a high electric field) is connected to breakdown the material and cause conduction. In semiconductors, as the name implies, the band gaps are relatively close (i.e. 1.12 eV in pure silicon) and in wide bandgap semiconductors, it is even higher (normally above 1.70 eV, i.e. 2.36 eV in case of 3C-SiC and 3.23 eV in case of 4H-SiC), enabling SiC devices to withstand higher voltages (as a result of higher critical electric field capability). These bands are formed due to different chemical structures between atoms. In covalent bonds, by increasing the temperature, it is possible for some energized electrons to free themselves from the nucleus bonds and move to the conduction band. Therefore, most intrinsic semiconductors are slightly conductive in room temperature ($\approx$ 300 K) compared to the zero kelvin. A permanent method to enhance and control the level of conductivity of semiconductors is adding intentional impurities to pure intrinsic semiconductor. The N-type semiconductors are developed by adding an N-type impurity

(or dopant). These are called donors as they donate an excess electron to the structure of the semiconductor (i.e. Phosphorus) while the P-type semiconductors are developed by adding a P-type dopant (i.e. Boron). These are called acceptors, as they lack one electron and hence can accept one. The *carriers* in P-type semiconductors are holes. In an intrinsic semiconductor, by moving of an electron from the valence band to the conduction band, both carriers are *generated* in the two bands. However the movement of the electron in the conduction band is clearly easier than the movement of the hole in the valence band. Hence the *mobility* of the electrons is normally higher than the holes. This makes a crucial impact on the options available for the type of doping used to fabricate the devices, hence why most power devices use an N-type doped semiconductor as the choice for the drift region to enable lower on-state resistance. The number of carriers in the N and P region of a P-N junction (to be described shortly) can be derived from Equation 2.1 as:

$$n = n_i \, exp\left(\frac{E_F - E_i}{kT}\right) \tag{2.1a}$$

$$p = n_i \, exp\left(\frac{E_i - E_F}{kT}\right) \tag{2.1b}$$

which can result in 'Mass Action' law as:

$$\begin{aligned} pn &= N_C N_V \, exp\left(-\frac{E_g}{kT}\right) \\ &= {n_i}^2 \end{aligned} \tag{2.2}$$

Where the requirement of charge neutrality in depletion region imposes 2.3 as:

$$n + N_A^- = p + N_D^+ \tag{2.3}$$

Hence, the minority carriers in each region can then be calculated from:

$$n_{p0} = \frac{n_i^2}{p_{p0}} \approx \frac{n_i^2}{N_D} \tag{2.4a}$$

$$p_{n0} = \frac{n_i^2}{n_{n0}} \approx \frac{n_i^2}{N_A} \tag{2.4b}$$

2.2.1.1 Carriers Mobility

The movement of carriers play an important role in the device structure and switching speed of power devices. There are two major types of movement for carriers; *Drift* and *Diffusion*. The drift of carriers happens as a result of an electric field while the diffusion happens as a result of concentration gradients in the junctions of device. The current as a result of the electron and hole movements due to the applied electric field (drift) is as:

$$I_n = qn\overline{V_n}A \tag{2.5a}$$

$$I_p = qp\overline{V_p}A \tag{2.5b}$$

in which the n and p are concentration of carriers, $\overline{V}$ is the average speed of carriers and A is the area of the conduction. Hence the total current density can be re-written as

$$J = qn\overline{V_n} + qp\overline{V_p} \tag{2.6}$$

The drift speed of carriers against the electric field can be re-written as:

$$\overline{V_n} = \mu_n \mathscr{E} \tag{2.7a}$$

$$\overline{V_p} = \mu_p \mathscr{E} \tag{2.7b}$$

Equation 2.7 is only valid at low enough electric fields (i.e. below 10^5 V/cm in silicon)

since at strong fields electrons velocity saturates at 10^7 cm/s in silicon and 2×10^7 cm/s in SiC. Replacing Equation 2.7 in 2.6 results in:

$$J = qn\mu_n\mathscr{E} + qp\mu_p\mathscr{E} = \sigma\mathscr{E} \tag{2.8}$$

where σ is called the conductivity coefficient of the semiconductor. A basic schematic of a P-N junction is shown in Figure 2.3 of section 2.2.1.3. When the N-type and P-type semiconductors form such junction, a diffusion current is generated due to the difference between the majority carrier concentration of the two types of semiconductors. This diffusion current can be calculated using Fick's flux of carriers law [5] as:

$$\overrightarrow{j} = -D \times \text{grad } N \tag{2.9}$$

resulting in:

$$J_n = qD_n\frac{\mathrm{d}\Delta n}{\mathrm{d}x} \tag{2.10a}$$

$$J_p = -qD_p\frac{\mathrm{d}\Delta p}{\mathrm{d}x} \tag{2.10b}$$

As a result, the electrons from the N-type move towards the P-type and *recombine* while the holes from the P-type also move toward the N-type and recombine. This leaves an area of *immobile* ionized atoms *depleted* of carriers. Hence this area is called *depletion* or *space charge* region. The difference between the ionized atoms polarity causes an electric field from the positive side to the negative side, which in turn will form a *barrier* against further movement of majority carriers. On the other hand, the polarity of the space charge region causes the concentration of minority carriers on intimate distance of each side of the junction to be nil. This will in turn result in a gradient of minority carriers close to

the junction. The electric field will then assist the minority carriers to move across the junction, despite the low concentration, and this drift current forms the reverse leakage current of power devices. Eventually, thermal equilibrium is achieved between the two currents. At this time:

$$qn\mu_n\mathscr{E} = -qD_n\frac{\mathrm{d}n}{\mathrm{d}x} \tag{2.11}$$

From which, the Einstein relation can be obtained as [5]:

$$D_n = \frac{kT}{q}\mu_n \tag{2.12a}$$

$$D_p = \frac{kT}{q}\mu_p \tag{2.12b}$$

2.2.1.2 Carriers Lifetime

Aside mobility of carriers (μ), another determining factor in a semiconductor is the lifetime of carriers. The lifetime is the time it takes for minority carriers to recombine. To understand this, generation and recombination mechanisms of carriers must be considered. A carrier can lose its energy and recombine in different ways, the main two of which are by a photon and by a phonon. The first path is by releasing a radiative photon which holds the excess energy of the carrier thereby assisting to reduce its energy level. The second approach is by transferring the energy to the nearby carriers, as phonon scattering which is called 'Auger recombination'. The same methods can also result in generation of carriers in a semiconductor when the reverse energy transfer occurs. Such process is in direct relation with number of carriers available in both semiconductor bands as [5]:

$$G_{th} = R_{th} = K \times p_0 \times n_0 \tag{2.13}$$

where k is a relative constant. In equilibrium, the generation and recombination are equal. Hence, p_0 and n_0 are constant. However, in a recombination or generation process, i.e. by injection of carriers or external energy, the recombination rate becomes:

$$R = K \times (p_0 + \Delta p) \times (n_0 + \Delta n) \tag{2.14}$$

where the net recombination is then:

$$U = R - G_{th} = K(pn - n_i^2) \tag{2.15}$$

Therefore, the lifetime of carriers can be calculated as:

$$\tau_n = \frac{U}{\Delta n} \tag{2.16a}$$

$$\tau_p = \frac{U}{\Delta p} \tag{2.16b}$$

The carrier lifetime can also be controlled by diffusing recombination centers (such as gold -Au- or platinum -Pt-) in the semiconductor. These intentionally diffused impurities have energy states in between the energy state of the valence and conduction bands and can act as traps for the carriers by assisting them to lose their energy. A further method to generate intentional defects in the lattice is by radiation, which in turn also act as traps for the carriers. It must be noted that the same traps can contribute to generation of carriers, and for example be responsible for increase of leakage current in blocking state. Another important metric in relation to the carrier lifetime is the diffusion length, which is the distance the minority carriers can move before recombination. This is derived as:

$$L_{n,p} = \sqrt{D\,\tau} \tag{2.17}$$

2.2.1.3 The P-N Junction

The barrier field in Figure 2.3 causes a *built-in* voltage which can be calculated from:

$$V_0 = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2} \tag{2.18}$$

where $\frac{kT}{q}$ is the thermal voltage (V_T) in which k is the Boltzmann constant. The E in Figure 2.3 is related to V_0 in Equation 2.18 based on the Poisson's equation as in [5].

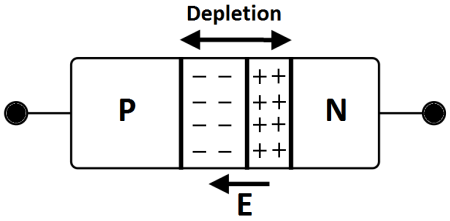


Figure 2.3: The basic formation of depletion region in a P-N junction.

It can also be shown that the width of the depletion region for an *abrupt junction* is:

$$W = \sqrt{\frac{2\varepsilon V_0}{qN_D}} \tag{2.19}$$

where

$$N = \frac{N_A N_D}{N_A + N_D}$$

and

$$\varepsilon = \varepsilon_0 \times \varepsilon_r$$

The width of the depletion region depends on the concentration of carriers on the two sides of the junction, and it extends further in the lower concentrated side of the junction

to maintain the neutral equilibrium between the charges as was described in Equation 2.3.

When a P-N junction is biased, as a result of the applied voltage on the junction, the depletion width changes. In many cases the ohmic resistance of N-type and P-type semiconductors is low enough to assume that the applied voltage only drops on the depletion region. In the *forward bias* mode, the applied potential is in reverse direction of the barrier potential, resulting in narrowing of the depletion region. This causes the potential difference between the two sides to reduce by the degree of the applied voltage. Hence, the diffusion current which was reduced by the barrier potential is increased once again. On the other hand, if a P-N junction is *reversed biased*, the applied voltage is in the same direction of the barrier potential. This results in a further increase in the depletion width of the junction. Hence, the applied voltage is *blocked*, and no diffusion current is allowed through. The drift current can still pass in, however it is still very low and is nearly invariant of the applied voltage, although is very temperature-dependant. The well-known Shockley equation describes the total current in an ideal P-N junction in both forward and reverse bias conditions as [5]:

$$i = I_S(e^{\frac{qv}{nkT}} - 1) \tag{2.21}$$

while I_S can be described as:

$$I_S = qA\left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\right)$$

If expanded, the first term of 2.21 describes the diffusion current by the majority carriers and the second term will describe the drift current by the minority carriers. This is the basic principle of the *pn diode* and forms the foundational characteristics of all semicon-

ductor devices. More details of these diodes will be discussed in subsequent chapters, but here, an important factor should be discussed: the *breakdown*. The breakdown of a diode occurs when the applied reverse bias voltage exceeds a certain magnitude thereby imposing a significant electric field on the junction of the diode and causing an excess rate of carriers to flow. Where this happens depends on parameters such as the critical electric field of the semiconductor material, the doping level, mobility of carriers and temperature amongst other factors. By increasing the electric field in the semiconductor, at a given electric field, a significant number of electrons will leave the valence band instantly and go into the conduction band, leading to a high current flow. This is called *Zener* breakdown. Alternatively, the applied electric field can increase velocity of carriers already present in the conduction and valence bands, resulting in liberation of more carriers by imparting their kinetic energy on other atoms. This can increase carrier density in the semiconductor and eventually result in the so-called *avalanche* breakdown.

Zener breakdown requires a higher electric field compared with avalanche breakdown and mostly happens in PN junctions with high doping levels (so a narrower depletion region). Alternatively the electric field required for avalanche breakdown is lower, and it happens in lower doped junctions with a sufficiently high depletion width so the carriers can speed up and hit each other effectively, causing the so-called avalanche. This process is also called *impact ionization*. Hence, due to the requirement of a lower electric field and presence of low doping in drift region of most power devices, avalanche breakdown happens before the zener breakdown gets an opportunity. Such breakdown of the PN junction is theoretically a reversible phenomenon. However, in the power applications (which are the aim of this study), a breakdown causes a significant current to flow resulting in higher instantaneous energy which in most cases leads to junction temperatures above the tolerance capability of the device or its packaging and results in destruction.

2.2.2 Power PiN Diodes

Power rectifiers are among the most important components of converters in nearly all power electronics applications. They are required to block high voltages in one direction while conduct high currents in the other. During the blocking mode, it is ideal to have minimal reverse leakage current while during the conduction mode it is ideal to have minimal voltage drop and conduction losses. Blocking high voltages in the reverse direction requires a wide depletion width to keep the peak electrical field below the avalanche breakdown limits of the device known as critical electric field.

2.2.2.1 Fundamentals

High breakdown voltages in power rectifiers are primarily achieved by having thick and lowly doped voltage blocking drift layers to minimize the electric field on the junction. This will satisfy the need for a wide depletion region and consequently achieving high blocking voltages. However, the penalty for such breakdown voltages is high conduction losses from the highly resistive voltage blocking drift region. This can partially be overcome by conductivity modulation which is achieved by keeping the P^+ and N^+ regions doping density high, while introducing a low doped N-type middle region in between. This N^- region causes two junctions. One is the P^+N^- junction, and the other is the N^-N^+ junction. Clearly the depletion region formed in the P^+N^- region is much stronger and has the determining role in performance of the diode. It should be noted that although the N^- drift region is not an intrinsic semiconductor, due to its significantly lower doping density compared to the other two regions, these device are called as 'P-i-N' diodes.

In fact, it can be said that within reasonably low doping densities, the lower the doping of drift region the higher will be the blocking voltage capability of devices. The built-in

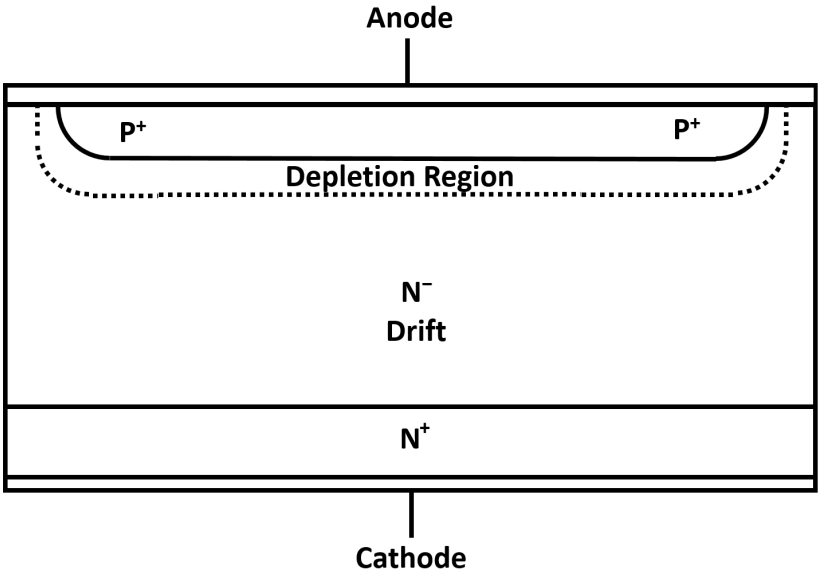


Figure 2.4: The cross-section of a typical power PiN diode.

voltage drop of the PiN diode is the result of three different voltage drops; two of which are on the junctions of the device while the third is on the drift region. Hence:

$$V_{Drop} = V_{bi\ P^+N^-} + V_{Drift} + V_{bi\ N^-N^+} \tag{2.22}$$

The total voltage drop of the two junctions can be calculated as in [6]:

$$V_j = V_{j\ P^+N^-} + V_{j\ N^-N^+} = \frac{kT}{q} ln \frac{p_L n_R}{n_i^2} \tag{2.23}$$

while the voltage drop on the drift region can also be calculated as in [6]:

$$V_{Drift} = \frac{I_F W_B^2}{(\mu_n + \mu_p).Q_F} \tag{2.24}$$

It should be noted that an increase of forward current impacts the concentration and consequently mobility of carriers. It also affects the carrier lifetime since the recombination

of carriers will occur faster. An increase in carrier mobility reduces the forward voltage drop likewise, an increase of the carrier lifetime. The stored charge in the drift region can also be calculated from [5] as:

$$Q_F = \frac{W_D^2 I_F}{V_{Drift}(\mu_N + \mu_P)} \tag{2.25}$$

This means there is a fundamental trade-off between the conduction losses determined by the forward voltage drop and the switching losses determined by the switching transients. The characteristics of PiN diodes under bias will be explained next.

2.2.2.2 Forward Biased Mode

During the forward bias of the PiN diode, it will be in the conduction mode. This is the result of the applied voltage overcoming the junctions built-in potential and reducing the width of depletion region. In this case, the P^+ doped region is connected to the higher potential compared with the N^- doped region. Hence, the depletion region in the P^+N^- region gets weaker and the majority carriers in the P^+ region will diffuse into the drift region as excess minority carriers and recombine. However this is true only at low forward currents where the injection rate of the excess minority carriers is relatively low and there is a high probability of recombination before reaching the end of the drift region. Yet at high forward currents (which are normally aimed by power diodes) the excess minority carriers have significantly higher density and due to the low doping of the drift region, will reach the N^-N^+ junction. The presence of the holes in the immediate vicinity of this junction absorbs the electrons in the highly doped N^+ region toward the drift region. Hence electrons of the N^+ region also experience an increased injection rate into the drift region. This process results in presence of a high density of excess

carriers in the low doped drift region, which is well above its normal carrier density. As a result, the resistivity of this region is significantly reduced and the conduction losses are decreased. This enhanced conductivity of the diode is called 'Conductivity Modulation' and the process of the excess carrier injection into the drift region from both highly doped regions is called 'double injection' of carriers. It should be noted that the carrier density in the vicinity of the P^+N^- junction is higher than that of the N^-N^+ junction due to the significantly higher mobility of the electrons compared with holes. Conductivity modulation is a determining phenomenon in the performance enhancement of all bipolar power devices including PiN diodes and IGBTs and is seen as a significant characteristics compared with unipolar power devices.

2.2.2.3 Reverse Biased Mode

As was explained, when the PiN diodes are biased in the reverse direction, the blocking voltage is determined by the width of the drift region and its doping density. This causes a depletion region on the P^+N^- junction and by increasing the potential difference, the depletion region widens. Due to the significant difference of the doping density on the two sides of this junction, the depletion region almost entirely falls into the drift region and the penetration width at the P^+ side is negligible. The width of the drift region allows a significant voltage blocking capability within the device. However, the depletion region may reach the N^-N^+ junction, causing a punch-through (PT) of this junction. This, if calculated precisely, can actually be beneficial to the blocking capability of the device as increasing the voltage increases the depletion region in the lateral direction in the drift region. Hence, a trapezoidal electric field is formed rather than a triangular one thereby the electric field is more evenly distributed across the drift region. This can be used as an approach to reduce the width of drift region, which further reduces the

forward voltage drop. The devices with punch-through field structure normally have a lower doping density in the drift region compared with non-punch-through devices, to assist the electric field to be more evenly distributed across the drift region. Calculations have shown that the width of the drift region in PT devices is nearly 40% smaller than that of the NPT devices [6] as seen as an example in Figure 2.5. The leakage current of PiN diodes during reverse blocking mode is increased by increase in temperature due to the generation of carriers at higher temperatures.

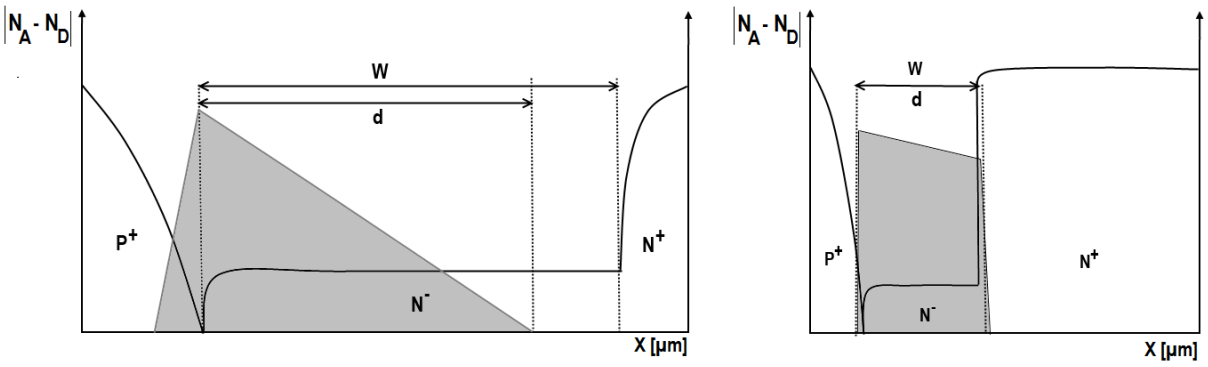


Figure 2.5: The depletion regions in the (left) NPT and (right) PT PiN diode. (Note that the doping of drift region is normally lower in PT compared to NPT)

The breakdown voltage [5] can be approximated by Equation 2.26 as:

$$V_{BR} = \mathscr{E}_{BR}^2 \cdot \frac{\varepsilon_r \varepsilon_0}{2q} \cdot (\frac{1}{N_D} + \frac{1}{N_A}) \tag{2.26}$$

where, for a junction with significant doping difference on the two sides of the junction (as is common in PiN power diodes) is simplified to:

$$V_{BR} = \mathscr{E}_{BR}^2 \cdot \frac{\varepsilon_r \varepsilon_0}{2qN_D} \tag{2.27}$$

2.2.3 Power Schottky Diodes

Another type of power diodes is the Schottky Barrier Diode (SBD). Unlike PiN diodes in which the junctions are formed between two semiconductors, these rectifiers are structured by the connection of a low doped (non-degenerate) semiconductor to a metal interface.

Figure 2.6 shows the schematic of a Schottky diode including the positions of the substrate, the drift region and the contact metal.

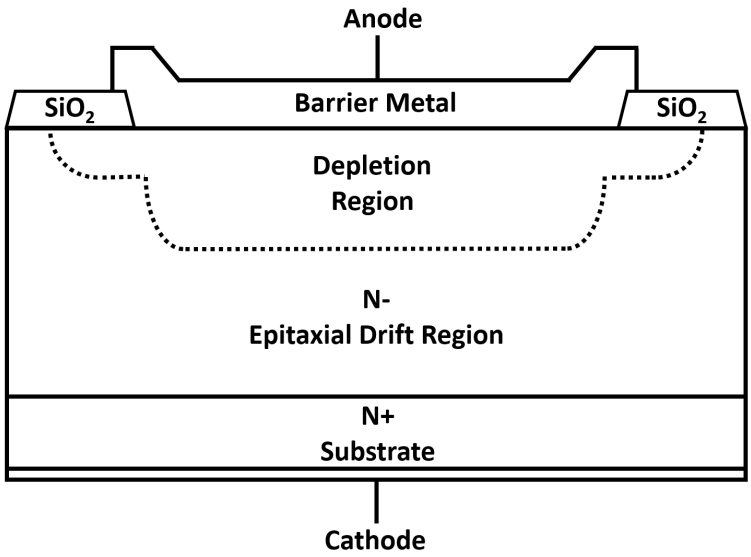


Figure 2.6: The cross-section of a typical power Schottky diode [7].

Depending on the doping level of the semiconductor and the work function of the metal, this junction can be of a contact type, i.e. conduct in both directions or of rectifying type, i.e. conduct only in one direction (the work function is the least energy required to take an electron away from a material and place it in vacuum). The former is called ohmic contact and is used in most devices to connect the semiconductor regions to the metal leads, while the latter is the matter of discussion in this section.

2.2.3.1 Fundamentals

The Schottky barrier structure exhibits interesting characteristics which are useful in certain applications. The semiconductor choice in these junctions is normally selected to be N-type since electrons have an overall higher mobility compared to holes, and can enable faster switching rates. Therefore all the analogies provided in this section are described for N-type devices, although they also hold for a P-type device, with consideration of changes in charge relations. Schottky barrier diodes are unipolar devices, meaning that the current conduction only relies on the majority carriers. In this sense, the carriers (electrons) flow from the semiconductor into the metal and join the 'electron sea' present in the metal; however there is no flow of carriers in the other direction. This is due to the presence of a barrier height which will be discussed shortly. This interesting characteristic of Schottky diodes results in no minority charge storage in the device, causing no reverse recovery although there is still a degree of stored charge in the junction capacitance. The result is lower switching losses and significantly faster switching rates compared to bipolar devices. Schottky diodes have lower junction voltages compared with their PiN counterparts of the same rating, although they present a relatively higher reverse leakage current while in the blocking mode. A Schottky diode fundamentally operates in a manner similar to a P^+-N^- junction where the P-type region is a degenerate semiconductor (very heavily doped). If the N-type region is also degenerate, it appears as a junction of two heavily doped semiconductors, resulting in a very narrow depletion region. This allows the energetic carriers to tunnel through the thin barrier and form the ohmic contact discussed earlier. Looking at the metal region as a heavily doped P^+ semiconductor, it can easily be understood that if the N-type region is relatively low doped, the depletion region nearly entirely falls within the N region. The N-type semiconductor is normally divided into two

regions: a lightly doped epitaxial N region in intimate contact with the metal (acting as a drift region to accommodate the depletion width) and a heavily doped N^+ substrate region to inject the carriers and connect the semiconductor to the metal leads on the cathode end. It should be noted that in unipolar devices, the concept of conductivity modulation is absent; hence Schottky diodes have a significantly higher on-state series resistance across the drift region compared with their PiN counterparts. Additionally to block high voltages, not only should the width of the depletion region be increased but the doping density should also be reduced; hence silicon Schottky diodes are not designed as high power devices due to the very high on-state losses associated with them.

Before the N type semiconductor and the metal are connected to each other to form a junction, the Fermi levels (where the probability of occupance of an energy state by an electron having that energy is exactly 50%) of the two are different as shown in the flatband diagram of Figure 2.7(a) [7]. Here, φ_{m} is the work function of the metal, φ_{s} is the work function of the semiconductor and χ is the electron affinity in the N-type. After the contact, the energy levels at the junction should equalize and reach an equilibrium level (this is called Fermi level pinning), meaning the E_F of the two regions should become equal. This will be done by a process somewhat similar to the formation of the depletion region in a P-N junction. When the contact is formed, electrons with high energy states in the conduction band of the semiconductor flow to the lower energy states in the metal, leaving a region of immobile positively ionized donors behind. As this process continues, an electric field is formed which stops further flow of electrons into the metal. This electric field also causes a potential between the metal surface and the conduction band of the N-type semiconductor. This potential or barrier causes a phenomenon called 'band bending' close to the junction as in Figure 2.7(b). The height of the barrier in front of the electrons is φ_{bn} while the built-in voltage is φ_{bi}.

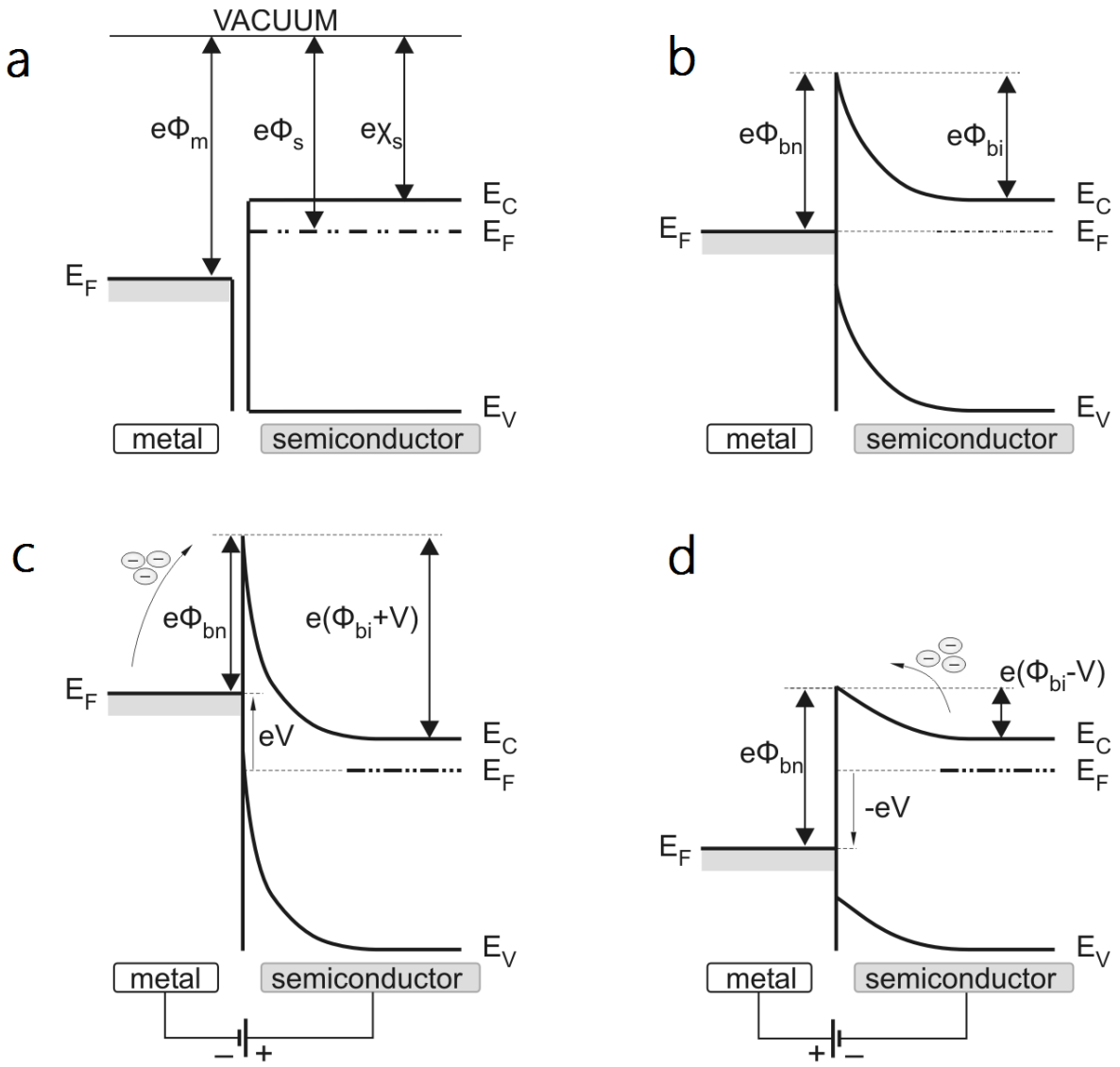


Figure 2.7: The Schottky barrier height formation in equilibrium, forward biased and reverse biased modes [7].

If a voltage is applied to the semiconductor in reverse bias, as shown in Figure 2.7(c), the Fermi level in the semiconductor decreases, causing a higher potential required for the electrons to move from the semiconductor to the metal, while the barrier height (φ_{bn}) is independent of the applied voltage. In this case, only highly energized electrons in the metal can move to the semiconductor, causing a reverse leakage current. On the

other hand, if the voltage is applied in the forward bias mode, as in Figure 2.7(d), the Fermi level in the semiconductor increases, and the potential in front of the electrons in the semiconductor reduces proportionally, assisting an easy flow for the electrons. The electrons in this case have a high level of energy which will be emitted as thermal loss when reached the metal side. This is why Schottky diodes are also named as 'Hot Carrier Diodes'. It should be noted that since the metal has very high concentration of electrons, the additional electrons are seen as negligible and will therefore not impact its energy levels. Adjusting the barrier height is a very important part of the Schottky diode design as it has a determining role in the dynamic performance of the diode. If the barrier height is set to a very high value, this will cause a significant voltage drop across its junction, and if it is set to a very low value, it will cause a significant temperature-dependent reverse leakage current in the blocking mode. Hence the trade-off should be well thought.

2.2.3.2 Properties of Schottky Diodes

As was discussed, it is clear that the trade-offs between the voltage blocking capability of Schottky diodes and the on-state resistance does not allow the silicon Schottky diodes to perform as an efficient power rectifier. Fortunately, emergence of SiC power Schottky diodes have reduced the restrictions on the design and performance trade-offs of these diodes as a high voltage power device. Material characteristics of Silicon Carbide (which will be discussed shortly) enables a thinner drift region and higher doping density for the same blocking voltage thus providing a lower on-state resistance compared with similarly rated silicon counterparts. The series resistance of SiC Schottky diode is higher than that of similarly rated SiC PiN diode, although their junction voltage is lower. SiC PiN diodes have a high junction voltage since the impact of low n_i in them is very pronounced, but use conductivity modulation to keep the on-resistance low. The overall forward voltage

drop of SiC Schottky diodes is relatively acceptable for voltages up to 1.7 kV. Clearly increasing the voltage beyond this level will require an even wider drift region which causes a high conduction loss. Also it should be considered that the overall mobility of carriers in SiC devices is lower than that of silicon and the increase in density of impurities further decreases it. Having said that, it is clear that employing SiC as the semiconductor material in devices reduces the reverse leakage current due to its wider bandgap. This is the consequence of the significant barrier height in the SiC junctions, which has a determining role in the leakage current of the device. The current in a Schottky diode can be explained using an equation similar to that of P-N diodes as in [6]:

$$J = J_S \left(e^{qv/kT} - 1\right) \tag{2.28}$$

Where J_S is:

$$J_S = A^* T^2 e^{-q\varphi_{\mathrm{bn}}/kT} \tag{2.29}$$

J_S is reverse leakage current of the diode and A^* is the so-called 'Richardson constant'. As seen, the reverse leakage current in Schottky diodes is very temperature dependent and increases with temperature with a power of 2. On the other hand, as stated earlier the forward voltage drop of the Schottky diode consists of two major voltages. The first would be the built-in junction voltage between the metal and semiconductor while the second part is the voltage drop on the drift region of device. The factors determining this voltage drop are the forward current flowing through the device and the on-state resistance of the drift region of the device. This resistance which can be calculated [5] as Equation 2.30 also further increases as temperature increases, since the mobility of carriers is reduced

at higher temperatures and will be a determining parameter in subsequent chapters:

$$R_S = \frac{W_D}{q \cdot \mu_n \cdot N_D \cdot A} \tag{2.30}$$

It can be concluded that despite the advantages that Schottky diodes provide, they also have two major drawbacks which makes their application in high power areas limited. The first drawback is the relatively low voltage blocking capability compared to PiN diodes and the second is the lack of conductivity modulation in on-state. To counter both of these issues some techniques can be employed. A common one is to use P-Guard rings on the junction. These P-regions have multiple functions. They assist with distribution of the gradient of electric field across the drift region as a junction termination, hence increasing the voltage blocking capability of the device. Also at high enough forward currents, their P-N junction with the drift region of device is forward biased and injects some minority carriers into the drift region, causing a small degree of conductivity modulation. This will reduce the on-state resistance during the conduction of device, although it has the drawback of presence of some reverse recovery current at turn-off due to the stored charge.

Equations 2.31 and 2.32 provide two important parameters in regard to the properties of Schottky barrier diodes in equilibrium which can be instrumental when the device capabilities are to be determined. These are:

The depletion width as:

$$W_D = \sqrt{\frac{2\varepsilon_{Si}}{qN_D} V_{bi}} \tag{2.31}$$

and the junction charge as:

$$Q_J = \sqrt{2\varepsilon_{Si} q N_D V_{bi}} \tag{2.32}$$

2.2.4 Power MOSFETs

The emergence of power transistors started a new era in the power conversion industry. Starting from low power switch mode power supplies, UPS and battery chargers, power transistors have provided a breakthrough in power electronics circuits. Power MOSFETs (Metal-Oxide-Semiconductor Field-Effect-Transistors), which are the matter of discussion of this section, are among the most popular and practical transistors. However, silicon power MOSFETs typically have a maximum voltage rating of 1.2 kV. Nevertheless, their fast switching has secured them a determining role in low and medium voltage power electronics circuits, aiming for applications where weight and volume of the passives is critical and a fast switching rate is required. Today's power MOSFETs are developed from low voltage MOSFETs which are in use in integrated circuits and share the same principles. MOSFETs are unipolar devices, as their conduction only relies on majority carriers and have faster switching since no minority carrier extraction/recombination occurs. However, MOSFETs switching are still limited by the charging and discharging of the parasitic capacitances present on the gate during transients. MOSFETs are voltage driven devices, and require a gate voltage to turn-on. Figure 2.8 shows the basic cross-section of a lateral and a vertical diffused MOSFET. The latter is the structure that is commonly used as a power MOSFET with presence of a P-body, while the former is a low voltage MOSFET of the same type. The basic principle behind the operation of power MOSFETs is the formation (or removal) of a conduction *channel* through the *field effect* phenomenon. The gate (often polysilicon) of the MOSFETs is isolated from the body through an oxide insulator which is usually thermally oxidised SiO_2. If a conduction channel already exists between the drain and the source and a negative gate voltage is required to remove it, the device is called a depletion mode MOSFET. These are normally-on devices, and hence are not

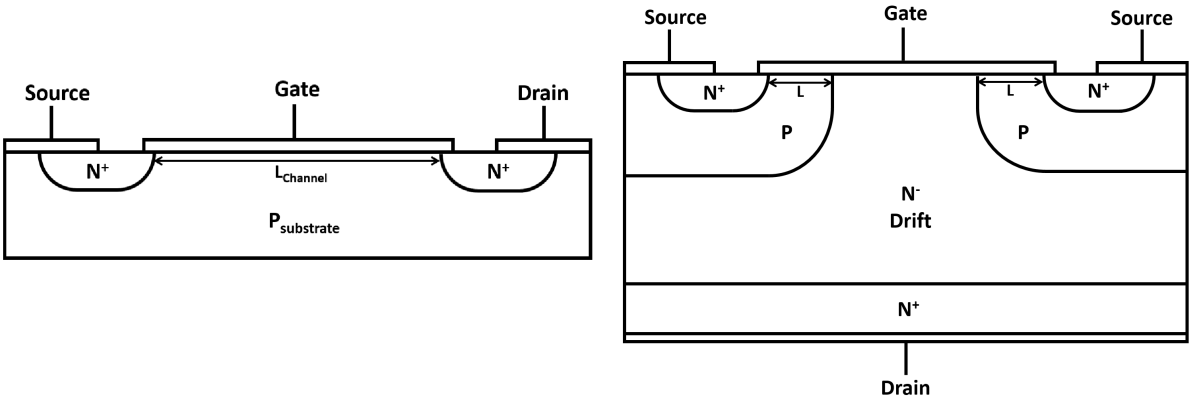


Figure 2.8: The cross-section of a (L) lateral and (R) vertical power MOSFET.

practical in most power applications. On the other hand, if a conduction channel is only formed after a positive voltage is connected to the gate, then it is called an enhancement-mode MOSFET. Both the body and drift region of the MOSFETs can be of N-type or P-type; however as in other devices discussed due to higher mobility of electrons, they are selected as carriers of choice and hence most power MOSFETs are fabricated as nMOS type. Therefore, the discussion here is focused on enhancement-mode nMOS.

2.2.4.1 Fundamentals

Looking at Figure 2.8, it can be seen that the presence of the P-body region has caused two reverse junctions, where conduction is blocked in either direction. However, a conduction layer can be formed between the source and the drain, using a gate bias voltage (V_{GG}) as shown in Figure 2.9. When a small positive voltage is applied on the gate, the field created between the metal and semiconductor repels the majority carriers (holes) and depletes the area in close vicinity of the gate oxide, leaving an area of immobile negatively-charged ions. Further increase in the gate voltage absorbs more of the negative charge carriers and brings them closer to the gate oxide layer. These electrons are either the minority carriers

in the P-body, or are absorbed through the highly doped drain and source regions. Strong increase in the applied voltage further modulates the conductivity of the MOSFET channel (not to be mistaken with the conductivity modulation in bipolar devices) and provides a low resistance conduction band between the two N-doped regions. The voltage where the density of negative charge carriers in this so-called *inversion layer* becomes equal to the density of majority carriers in the P-body is called the *threshold voltage*.

The gate voltages below the threshold voltage only modulate a sub-threshold leakage current, while increasing it beyond the threshold voltage well enhances the channel width and facilitates the high current conduction. When there is no applied voltage between the drain and the source of the MOSFET, a small depletion region as a result of the P-N junction is naturally formed. However, should the V_{DS} voltage start to increase, the depletion region expands from the drain with higher voltage. This voltage reduces the impact of the gate voltage on the area close to the drain, and reduces the width of the channel. When V_{DS} equals to the difference between the applied gate-source voltage and the threshold voltage of the MOSFET, the channel in immediate vicinity of the drain is removed, or *pinched off*. Any further increase in the voltage results in decrease of the length of the channel. It should be noted that the current between the drain and the source continues to conduct regardless of the channel pinch off, since the electric field between the pinch off point and the drain is strong enough to attract the electrons through the negatively-charged depletion region while the carriers might reach saturation velocity.

2.2.4.2 Modes of Operation

As was discussed, the variation of the applied gate voltage determines the degree of the formation of conduction channel between the drain and the source regions. Additionally, the pinch-off phenomenon occurred closed to the drain region also impacts the saturation

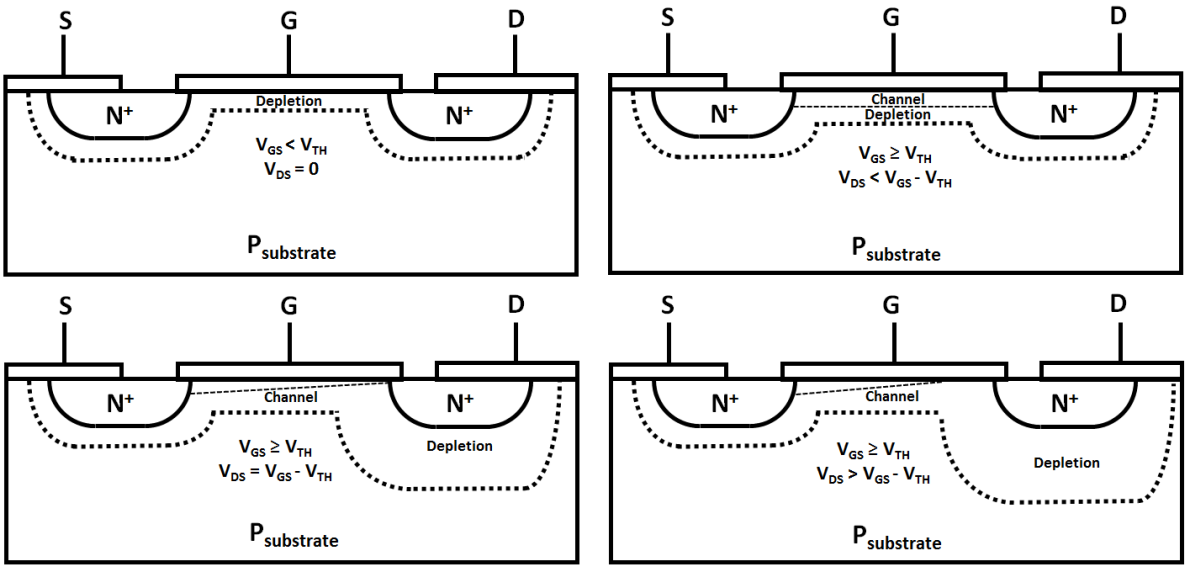


Figure 2.9: Channel formation and its pinch-off with different drain-source voltages.

of the flowing current. Therefore, one expects to see different modes of operation for the MOSFET, depending on the levels of applied gate-source and drain-source voltages. There are three modes of operation for a MOSFET. These are cut-off mode where the applied gate-source voltage (V_{GS}) is lower than the threshold voltage (V_{TH}) and consequently except for a subthreshold leakage current, no further current can flow between the drain and the source; the linear mode where V_{GS} is higher than that of V_{TH} and the V_{DS} is lower than the difference of the two and the saturation mode, where the V_{DS} is higher than the difference of V_{GS} and V_{TH}. The cut-off mode is where the MOSFET is mainly blocking, therefore is not the matter of discussion here. Starting from the linear mode of operation, assuming that the V_{DS} (and consequently $\mathscr{E}$) across the channel is constant, the speed of carriers and the time it takes to move across the channel, can be written as:

$$v = \mu\mathscr{E} = \mu\frac{V_{DS}}{L} \tag{2.33a}$$

$$t = \frac{L}{v} \tag{2.33b}$$

The drain-source current can be in the form of total channel charge per unit time [5] as:

$$I_{DS} = -Q_{inv}\frac{WL}{t} \tag{2.34}$$

and where the charge per unit and gate capacitance per unit are:

$$Q_{inv} = -C_{ox}(V_{GS} - V_{TH}) \tag{2.35a}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.35b}$$

This results in having the drain-source current as:

$$I_{DS} = \mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{2.36}$$

However, this assumption is only applicable when V_{DS} is significantly lower than the value of $V_{GS} - V_{TH}$ and the channel is fairly uniform between the source and drain and the device is in the linear mode. Therefore, in most MOSFETs (and especially in case of power MOSFETs), the change in the conduction channel as a result of high V_{DS} should be considered. Hence the current in a very small section of the channel as a factor of the voltage on that area of the channel can be written as:

$$I_{DS} = \mu C_{ox}\frac{W}{dx}(V_{GS} - V_{TH} - V_{CH})dV_{CH} \tag{2.37}$$

and for the full length of the channel (L), where the V_{DS} is applied we have:

$$\int_0^L I_{DS}dx = \mu C_{ox}W\int_0^{V_{DS}}(V_{GS} - V_{TH} - V_{CH})dV_{CH} \tag{2.38}$$

So the current in the linear mode of operation, considering the impact of V_{DS} on the conduction of channel, where V_{DS} is still lower than V_{GS}-V_{TH} can be determined as:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{2.39}$$

In the saturation mode of operation (pinch-off) the current can be calculated as:

$$I_{DS_{SAT}} = \mu C_{ox} \frac{W}{L} \times \frac{(V_{GS} - V_{TH})^2}{2} \tag{2.40}$$

One might want to consider other impact factors, such as the 'Drain Induced Barrier Lowering' or DIBL as well which will still cause a slight increase in saturation current with the applied V_{DS}. This will add a coefficient of $1 + \lambda V_{DS}$ to the above equation. These equations will be used in later point of discussion to understand the behaviour of the devices in operation.

2.2.4.3 Parasitic Elements

Looking at the structure of a power MOSFET, several parasitic elements can be identified which have a determining role in the switching speed and operational reliability of the device. The main elements seen can be listed as:

- Parasitic capacitances
- Parasitic BJT
- Integral body diode
- Parasitic JFET

These are described as follows:

1. Parasitic capacitances between contacts

   MOSFETs have multiple parasitic capacitances which are due to the overlapping of doped semiconductor areas, or the doped semiconductor and the gate polysilicon with the oxide acting as the dielectric. These capacitances will be charged and discharged during each switching cycle, and therefore are critical in understanding the dynamic performance of the device. There are three main capacitances to be considered: Gate-Source capacitance (C_{GS}), Gate-Drain capacitance (C_{GD}) and Drain-Source capacitance (C_{DS}). However these capacitances are often shown in datasheets in terms of input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}). The C_{iss} has normally the highest value and has a determining role in the switching speed of MOSFETs. They can be calculated as:

$$C_{\text{iss}} = C_{\text{GD}} + C_{\text{GS}} \tag{2.41a}$$

$$C_{\text{oss}} = C_{\text{GD}} + C_{\text{DS}} \tag{2.41b}$$

$$C_{\text{rss}} = C_{\text{GD}} \tag{2.41c}$$

   The C_{GS} is constituted by three capacitances: a capacitance between the metal contact of the source and the gate, a capacitance between the gate overlap on the N^+ region and a capacitance between the gate overlap with P-base region. This capacitance is normally the highest of the three and is relatively independent of the applied V_{DS}. The second capacitance is the C_{GD} (which is also called the Miller capacitance) and has a determining role on extent of crosstalk in power MOSFETs during switching as it is between the drain and the gate and be directly affected by the dV/dt of the MOSFET. The details of this will be discussed at a later stage. The third capacitance is C_{DS} which also varies with the applied voltage.

2. Parasitic BJT

   Integral to the power MOSFETs structure a parasitic BJT exist which may cause a reliability issue for the operation of device. This BJT exist between the N^+PN^- region, where its base is in the P-region, its emitter is in the N^+ region and its collector is in the drift region. If the resistance of the P-base region is substantial, high levels of displacement current flow can lead to unwanted turn-on of this BJT which in most cases has destructive consequences as the device continues to conduct through the BJT path. To reduce the probability, the P-base is internally connected to the source through the source-metallization. Although this helps to reduce the risk of turn-on of parasitic BJT or 'latch-up', it does not completely eliminate it. This issue will be investigated in depth in subsequent chapters.

3. Integral body diode

   As was seen, a common approach to reduce the probability of latch-up of the parasitic BJT is the connection of the base to the source-metallization. However this itself will cause another parasitic element in a MOSFET; an integral body diode. This diode is formed between PN^-N^+ regions, and acts very similar to a PiN diode. This element, might on the first sight, be considered as a useful anti-parallel diode in the device; however later it will be seen that this diode is not optimized and might have high reverse recovery charge. Hence, it is best to avoid its operation in the circuit by using an externally-connected fast recovery anti-parallel diode.

4. Parasitic JFET

   When the MOSFET is in the conduction mode, an accumulation of P-type carriers forms adjacent to the P-body regions as a result of positive gate voltage and the drain potential. As V_{DS} across the device increases, the depletion region and accumulation

of P-type carriers further extends. Expansion of the depletion region in the drift region is similar to the operation principle of a JFET, hence it can be looked at as a parasitic JFET within the MOSFET. The presence of this parasitic JFET contributes to the increase of the on-state resistance of the device, as the current flow in the drift region becomes restricted. To counter this, different device structures are developed. For instance, the VDMOS has reduced the JFET effect compared to DMOS and the UMOS effectively removes it as in Figure 2.10.

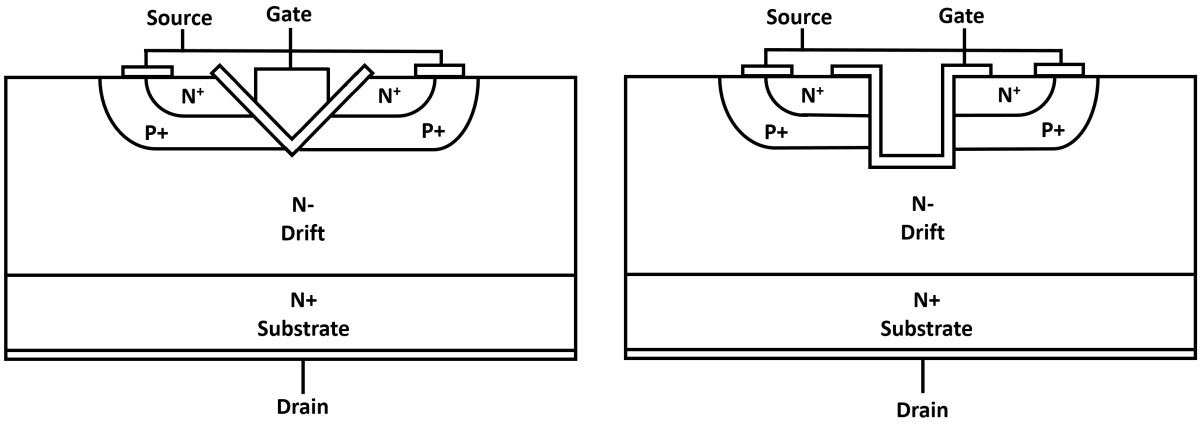


Figure 2.10: Cross-section of typical (L) V-groove and (R) U-Trench power MOSFET.

2.2.5 Power IGBTs

As was discussed, the power MOSFET has one main drawback: high on-state resistance and consequent voltage drop. However, it still exhibits many interesting characteristics, first and foremost, fast switching speed and low power loss during switching transients as well as the voltage-controlled switching. Hence extensive efforts were made to combine the conductivity modulation phenomenon seen in the bipolar devices with the voltage-controlled switching performance of MOSFETs and develop a hybrid power device. As a result, many different types of devices have been developed, the most successful of which is the Insulated Gate Bipolar Transistor or IGBT.

2.2.5.1 Fundamentals

IGBTs are made by adding a layer of highly doped P-region beneath the MOSFET structure. They are bipolar devices, which rely on the minority carrier injection, while their switching is governed by a MOS gate forming a conductive channel. Hence they exhibit higher switching rates than most other bipolar devices and lower conduction losses than unipolar devices. The basic structure of IGBTs is shown in Figure 2.11. It is seen that the gate structure is identical to a MOSFET; as when the gate voltage is biased the channel in the P-body region is formed and the electrons from the source (now the emitter in the IGBT) will find a path to flow toward the N^--layer drift region. Presence of high levels of negative charge carriers in the drift region attracts the holes in the P^+-region of the IGBT toward the drift region; hence a diffusion current by the P-region carriers also flows toward the emitter. The inverted channel causes a gradient of concentration for negatively charged carriers, which leads the minority carriers to move toward it.

The consequent conductivity modulation will significantly reduce the on-state resistance in the device, enabling thicker widths of drift region for blocking higher voltages compared with MOSFETs. Hence the on-state resistance will be more dependent on the level of modulation and carriers lifetime than actual dimensions of the drift layer.

Two main types of IGBTs are shown in Figure 2.11. The first is the non-punch-through (NPT) IGBT while the second is the punch-through (PT) IGBT. The difference is mainly the presence of N^+ buffer layer between the N^--drift region and P^+-collector region in the PT device. This layer acts as field-stop, hence similar to the case of PiN diodes, making the field into a trapezoidal form. Advantages of this are shorter widths of drift region compared to the NPT devices of the same rating and further reducing the on-state resistance; however it reduces the reverse blocking capability of IGBTs. In an NPT

IGBT, the forward blocking voltage drops on the reverse-biased junction between the P-body and N^--drift layer, while extended nearly on its entirety in the drift region. The reverse blocking voltage also drops between the P^+-anode region and the drift layer; again almost entirely extending in the drift region. Therefore the voltage blocking capability in both directions is available should the junction termination be applied. However, in the PT-IGBT, the presence of the highly doped N^+-buffer layer causes a narrow depletion region; hence the reverse blocking voltage is significantly reduced. This, though, is not a major issue in most applications, as despite the absence of a body diode, they are normally coupled with anti-parallel discrete diodes to bypass the reverse conduction mode.

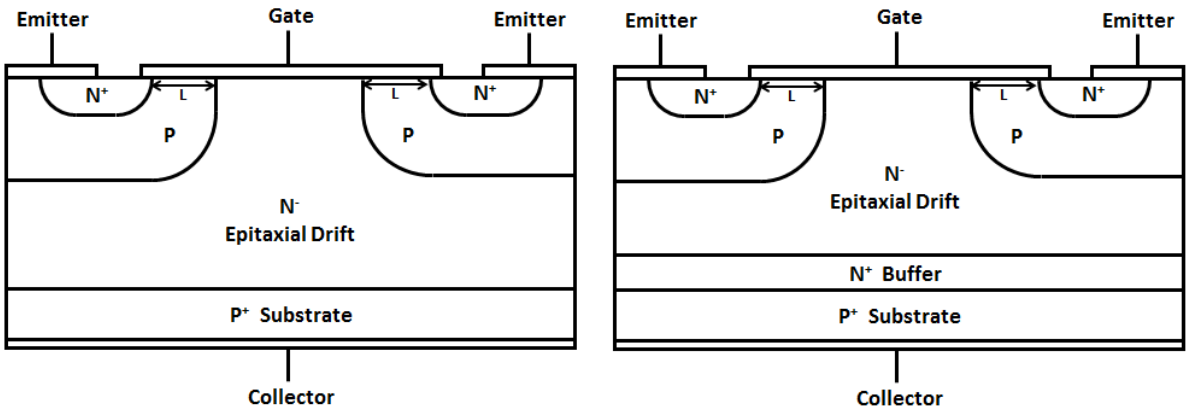


Figure 2.11: Typical cross-section of (L) NPT IGBT and (R) PT IGBT.

2.2.5.2 Reliability

The additional P^+-layer in an IGBT forms a parasitic Thyristor in the device, which might latch up with destructive consequences. This can be explained as such: the carriers injected from the P^+-anode region during the conduction phase will flow toward the emitter contact, although part of them recombine in the buffer layer and the drift region. As minority carriers, they flow into the P-body region, and act as a displacement current

which combined with the resistance of the body, will induce a voltage on the base of the parasitic NPN transistor. If the induced voltage exceed the junction voltage between the P-body and N^+-region, the junction will be in forward bias and the parasitic BJT turns on. Since the PNP BJT is already on (as the device is in the conduction state), simultaneous turn-on of both BJTs causes the turn-on of the parasitic Thyristor. Triggering of this Thyristor should be avoided since once it turns-on, the MOS gate is no more in control of the conduction and it will continue to pass the current through until the device fails due to thermal stress. The possibility of latch-up increases with higher injection of carriers at high conduction levels; so to reduce the risk, similar to the case of power MOSFETs, the P-body and N-emitter are connected to each other through overlapping of the emitter (source) contact on both regions to reduce the effect of P-body resistance.

The conductivity modulation in the IGBTs is not without consequences. The minority carrier charges stored during conduction in the N^--drift region of device should be removed so that the device fully turn-off. These charges must be recombined in the drift region, resulting in a high tail current; the length of which is shorter in PT-IGBTs compared to NPT ones, although it has a higher amplitude. This is due to the fact that presence of the N^+-layer in PT IGBTs causes a faster recombination of holes. It must be noted that contrary to the high voltage MOSFETs where the on-state resistance is dominated by the resistance of the drift region, in IGBTs the determining factor is the narrow channel resistance where no modulation takes place. When it comes to SiC MOSFETs and IGBTs, two important factors must be considered. Firstly, the two times higher electron saturation velocity in SiC compared with silicon may result in even faster switching. However low channel mobility due to SiC/SiO_2 interface has hindered the utilization of this advantage. Additionally the low carrier lifetime in SiC is major challenge in fabrication of desirable bipolar devices, i.e. SiC IGBTs. Further discussion on SiC properties is next.

2.3 Silicon vs. Silicon Carbide

Silicon has conventionally been the semiconductor of choice for power devices. However, the increase of the on-state resistance with increase of the drift region width, especially in unipolar power devices, has been the main barrier impeding the development of unipolar power devices with high voltage blocking capability. To overcome this and aim for high voltage applications, bipolar power devices were developed. However, these also exhibit a relatively long switching transient, followed by a tail current due to the recombination phase. Hence, to develop a high voltage and fast switching device, the only option available is to move towards the use of unipolar devices employing wider bandgap materials.

Wide bandgap semiconductors come in the form of different elements or compounds of which Silicon Carbide (SiC) and Gallium Nitride (GaN) are among the most developed ones. SiC, which is the dominant commercially-available WBG semiconductor technology, is a compound formed between silicon and carbon with a strong covalent bond and can be formed in different polytypes. Unfortunately most of these polytypes are difficult to

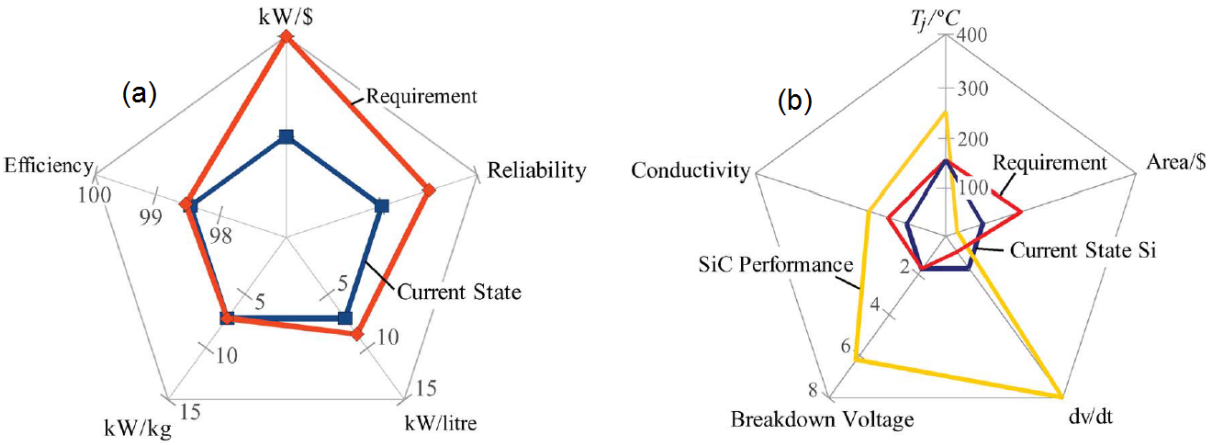


Figure 2.12: (a) Technical requirements and current state of power converters, (b) Comparison of typical properties of silicon and SiC devices; Courtesy of [8].

crystalize in extensive diameters, hence for large wafer diameters, three main polytypes namely 4H-SiC, 6H-SiC and 3C-SiC are chosen, among which 4H-SiC is the dominant due to higher mobility and breakdown field. SiC as the trendiest choice of WBG materials, has many advantages which can be beneficial for the development of power devices. Some of these are shown in Table 2.1 obtained from [9]. As can be seen, SiC has over 8 times higher critical electrical field capability compared with silicon; hence it can deliver a significantly higher blocking voltage for the same width of drift region. This is because of the wider band gap between its bands, hence the electrical field that is required to initiate the impact ionization is significantly higher. SiC can also maintain its characteristics at higher temperatures. This is because firstly, it has a higher melting temperature point, meaning that it can withstand higher temperatures without losing its physical characteristics. More importantly, it maintains its semiconductor properties at high temperatures, since the generation of carriers require significantly higher energy. In silicon, the relatively lower bandgap means that the rate of carrier generation with temperature renders the semiconductor degenerate thereby losing its semiconducting properties.

Table 2.1: Comparison of main material properties of silicon and SiC polytypes [9].

Parameter	Unit	Silicon	4H-SiC	6H-SiC	3C-SiC
Bandgap (E_g)	eV	1.12	3.26	3.02	2.36
Electrical Breakdown Field ($\mathscr{E}$) (N_D=3×10^{16} cm^{-3})	MV cm^{-3}	0.37	2.8	3	1.4
Intrinsic Carriers Concentration	cm^{-3}	1.5×10^{10}	5×10^{-9}	1×10^{-6}	0.1
Electron Mobility (μ_n)	cm^2 V^{-1} s^{-1}	1350	1020	450	1000
Hole Mobility (μ_p)	cm^2 V^{-1} s^{-1}	480	120	100	100
Thermal Conductivity (λ)	W cm^{-1} K^{-1}	1.49	3.3-5	3.3-5	3.3-5
Relative Dielectric Constant (ε_r)	(–)	11.7	9.76	9.66	9.72

Also the higher thermal conductivity in SiC means it can remove the heat generated from the junction more quickly, resulting in a lower junction temperature. Table 2.2 of [10] provides an estimated comparison between properties of silicon and SiC devices with the same voltage range. It can be seen that the thickness of drift region of device is significantly lower in SiC while its doping is higher. This simply means a considerable reduction in the on-state resistance and conduction losses compared to the silicon counterparts. Implementation of SiC in unipolar devices also means that the fast switching capabilities are maintained thereby switching losses are also low. These advantages as well as a few important challenges of SiC devices will be discussed in subsequent chapters.

It can be seen in Figure 2.12 of [8] that reliability and price are important factors that still require significant improvements. Unfortunately these two factors are significant drawbacks in front of the broad application of newly developed SiC power devices, where the reliability issues hinder performance. The price also is considerably more expensive than silicon devices, although it is reducing rapidly as the utilization of the devices becomes more widespread. By overcoming these constraints, it is expected that SiC devices will replace silicon power devices in high and medium voltage applications; i.e. in electric vehicle applications where this has already started to take place.

Table 2.2: Doping and thickness of silicon and SiC devices with the same ratings [10].

Breakdown Voltage	*Silicon*		*Silicon Carbide (4H-SiC)*	
	Doping (cm^{-3})	Thickness	Doping (cm^{-3})	Thickness
500 V	5×10^{14}	36	1×10^{17}	2.2
1000 V	2×10^{14}	81	4×10^{16}	5.3
2000 V	8×10^{13}	183	1.6×10^{16}	12
3000 V	5×10^{13}	294	1×10^{16}	20
5000 V	2×10^{13}	530	4.4×10^{15}	35
10000 V	9×10^{12}	1200	1.7×10^{15}	80

2.3.1 Latest Devices

The very first SiC devices were unipolar to provide a narrow drift region. Among these, the SiC Schottky Barrier diode was one of the initial devices to be developed, commercialized with CREE® and Semisouth® in 2001. Compared to conventional silicon Schottky diodes where the blocking voltage could not exceed 200 volts due to the very high (and unacceptable) on-state resistance, SiC Schottky diodes with 1.2 kV ratings have relatively low on-state resistance. Among the transistors, SiC JFETs were also become commercially available in 2005, however due to the normally-on characteristics of these devices, they were not very practical. Development of normally-off SiC JFETs removed these disadvantages in 2008, however by then SiC MOSFETs were the main research topic worldwide. These devices, with good reliability and performance became commercially available by CREE® in 2011 and ROHM® in 2012 which eventually overshadowed the normally-off SiC JFETs. SiC MOSFETs reduced the on-state resistance of silicon power MOSFETs significantly, with the integral body diodes showing a much better switching performance with almost no reverse recovery. This, too, will be investigated in depth later in subsequent chapters. However, SiC MOSFETs have higher internal gate resistance (due to the smaller die size) and require high gate voltage (due to lower transconductance).

SiC bipolar devices, including SiC PiN diodes and SiC IGBTs are also in development in research facilities, although they have not been commercially available yet mainly due to the problems with low carrier lifetime in SiC. Unlike SiC unipolar devices, which aim for applications with medium voltage ratings such as EVs, the SiC bipolar devices aim for extremely high voltages, normally 10 kV and beyond, where the main application is deemed to be in high voltage transmission systems. Devices such as SiC Thyristors are also in development, although their point of application is still vague.

2.4 Summary

In this chapter, a brief overview of three fundamental aspects of power electronics was provided, namely the application of power devices in systems, the fundamentals of power devices performance, and the emergence of SiC as a replacement for the conventional semiconductor materials. Power devices are seen as the beating heart of the future electrical systems by enabling power electronics circuits to provide an enhanced control over system parameters. The applications where these can be utilized could be very high voltages such as in transmission systems, or medium voltages such as in electric vehicles. For different utilizations, depending on the rating and switching characteristics required, different power devices are to be used. Hence, the variety of these structures were also explored by studying the fundamentals of their performance. Last but not least, the potential impacts of emerging wide bandgap material as a replacement for the silicon wafers was discussed. In the later chapters, these impacts are discussed in further details.

Chapter

3 Performance Evaluation of Power Transistors and Diodes

Different applications of power semiconductor devices require certain characteristics, hence not all device categories are suitable for all areas. An example would be the fact that devices such as Thyristors are not fully controllable, meaning that not both the turn-on and turn-off transients can be initiated and controlled on will through the gate driver pulses. This is a major disadvantage for applications in medium voltage converters. Additionally, some devices are not voltage driven, and hence require a significant gate current to turn-on, i.e. BJTs are falling in this category. This complexes the gate drive design for high power applications. As a result, until recently the major power transistor of choice for medium voltage applications has been silicon IGBTs and the main power rectifiers has been silicon PiN diodes. As explained in former chapter, with emergence of SiC technology it is now possible for unipolar devices to also withstand higher voltages, while providing a comparable on-resistance as the lack of conductivity modulation has been compensated by narrower drift regions. To this end, to explore these theoretical breakthroughs, these devices must also be characterized and their performance to be evaluated by means of experimental measurements; this includes exploring both the benefits and challenges.

To understand the superiority and drawbacks of the latter devices, they have been evaluated in the context of their performance in a VSC. The VSCs are important since they provide a higher controllability and hence it is necessary to understand how devices can impact their operation. An interesting and rapidly growing area of power converters where VSCs can be useful is the medium voltage applications such as in an electric vehicle (EV) drive-train. Hence, this chapter provides a comparative analysis between the 1.2 kV SiC MOSFET/Schottky diodes and similarly rated silicon IGBT/PiN diode technologies.

In this regard, the switching performance of devices have been tested in a wide range of temperatures while the measurements are repeated at different switching rates for each temperature. The temperature impact on the electromagnetic oscillations in SiC technologies and reverse recovery in silicon bipolar technologies is analyzed, showing improvements with increasing temperature in SiC unipolar devices whereas those of the silicon bipolar technologies deteriorate. These measurements are then used in an EV drive-train model where the temperature rise and conversion efficiency is studied. It is seen that at a given switching frequency, the SiC unipolar technologies outperform silicon bipolar technologies in terms of switching losses, operating temperature and conversion efficiency. These can enable lighter cooling and more compact vehicle systems.

3.1 Principles of Performance Evaluation

Power electronics for electric vehicle drive-trains is essential for high efficiency energy conversion [11] and transiting from slow switching silicon bipolar to fast switching SiC unipolar technologies is theoretically expected to improve the performance and efficiency of EVs [12]. The higher thermal conductivity of these devices will make them more temperature rugged and the wider bandgap means less leakage currents and reduced

probability of thermal runaway in high temperature applications. As a result 1.2 kV SiC MOSFETs and Schottky diodes have been manufactured by CREE® and ROHM® (amongst others) while devices with blocking voltages as high as 10 kV [13, 14] and with increasingly higher currents have also been demonstrated [15]. The feasibility of SiC technology for energy conversion in fully rated power converters in applications such as wind turbine energy conversion and fuel-cell systems was also explored in [16] and the implementation of SiC devices in motor control drives has been explored in [17]. The SiC unipolar devices might impact the EVs on the system level performance by enhancing the compactness of the drive trains and the reduction in passive sizes [18]. The use of SiC devices in on-board chargers can reduce the charging time and the thermal stress [19].

In this chapter, impact of SiC unipolar devices in EVs has been explored. To ensure high fidelity of results, the power devices in the converter have been parameterized by results of extensive experimental measurements. The temperature dependency of transients is analyzed and the impact of switching rate on oscillations and reverse recovery is discussed. A 3-phase NPC VSC is used as in [20] together with a PMSM motor model as in [21,22] to emulate the EV drive-train. In this regard, first the experimental test set-ups are provided along with the devices transients, and then the impacts of implementation of these results in the EV drive-train model are presented.

3.2 Clamped Inductive Switching Measurements

First the details of the measurement set-ups are presented. Two separate test rigs have been used in these measurements, a low voltage test rig and a higher voltage test rig. The low voltage test rig is equipped with an advanced environmental chamber which is used to set the ambient temperature for the measurements at a specified level defined by

the operator through the controller. This is a 'Tenney Environmental' thermal chamber (Series 942) which can vary the temperature to a range of min –75 °C to max 200 °C. As the devices in test had packaging thermal limitations of –55 °C to 175 °C, the tests are performed in conditions close to the operation range of devices in –75 °C to 175 °C.

Figure 3.1 shows the circuit schematic of the standard clamped inductive switching test rig using a classic double-pulse method while Figure 3.2 shows the experimental system diagram, showing how the measurements system is organised for measurements of chapter 3,chapter 4 and chapter 5. The design schematic in Figure 3.1 and system diagram in Figure 3.2 is the same for both test rigs shown in Figure 3.3 and Figure 3.5. The pulse provided by the Tektronix signal generator AFG3252C is sent to the gate driver inside the enclosure, which will then send the appropriate voltage (here 18 volts) to the gate of the switching device located inside the thermal chamber. The values for the circuit elements are shown in Table 3.1. Figure 3.3 shows the picture of the low voltage experimental set-up alongside the environmental chamber and Figure 3.4 shows the connection of the transistor and diode inside the thermal chamber.

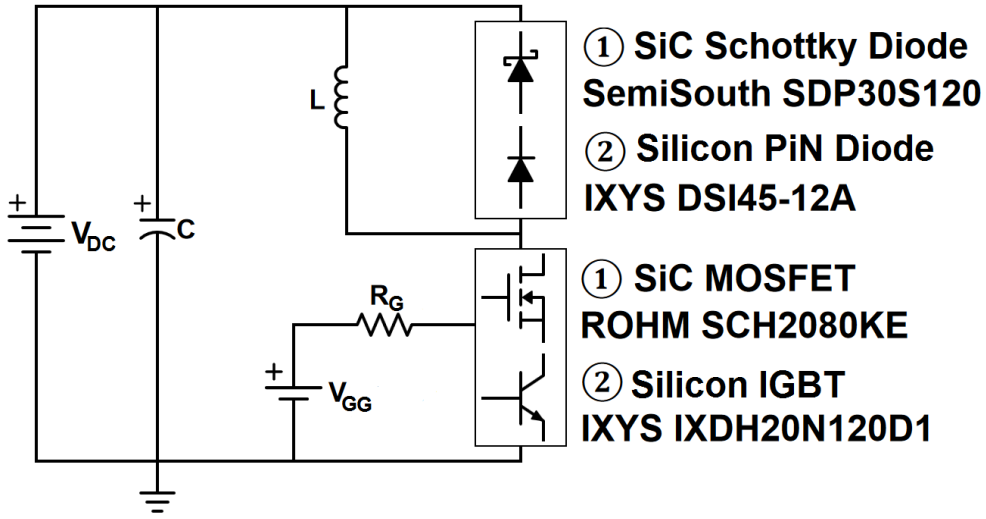


Figure 3.1: Schematic of the clamped inductive switching test rig.

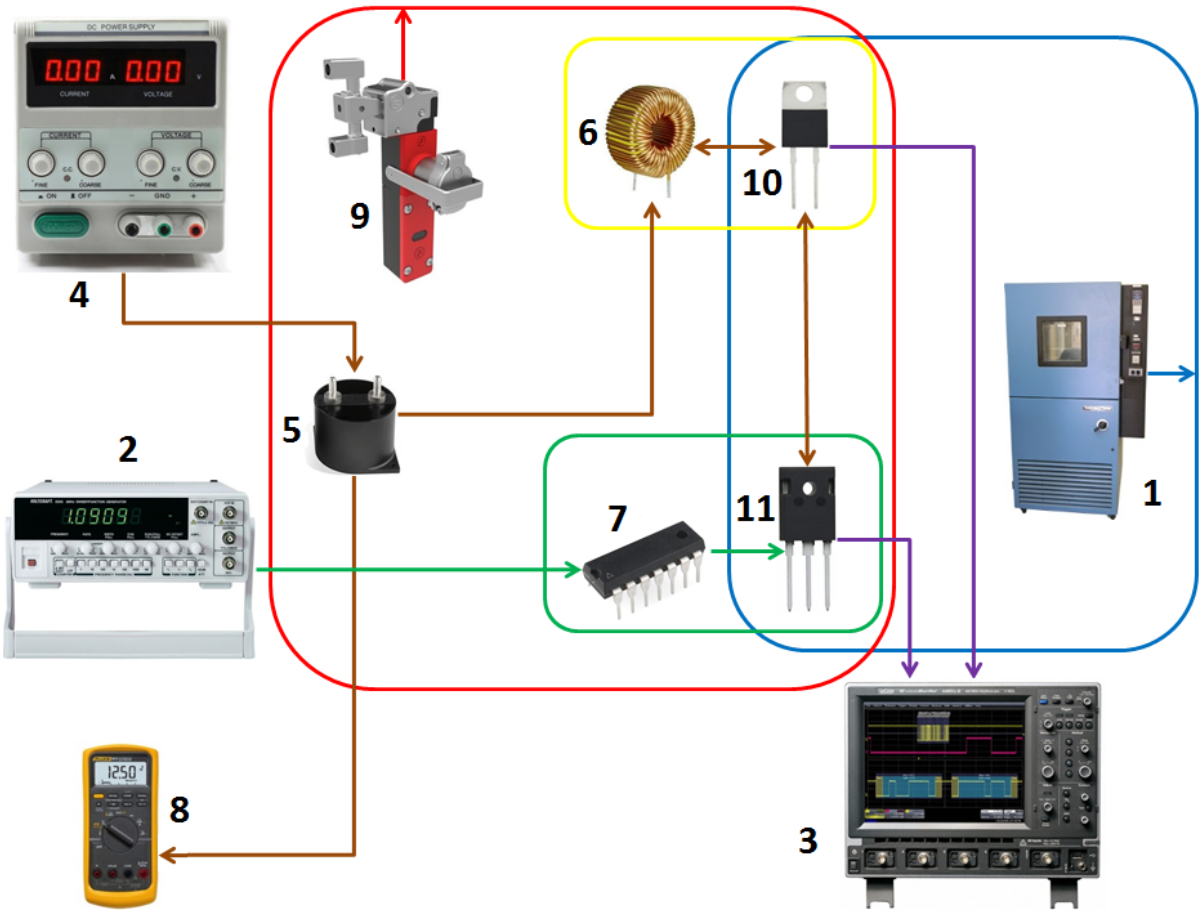


Figure 3.2: Experimental system diagram, showing how the measurements system is organised for measurements of chapter 3,chapter 4 and chapter 5. The components shown are as follows: 1- Thermal chamber 2- Function generator 3- Oscilloscope 4- Power supply 5- Bank capacitors 6- Bank Inductors 7- Gate drive system 8- Multimeter 9- Safety Interlock 10- Power diode 11-Power transistor.

As seen in Figure 3.3, due to the significantly long wires that are inevitably used to connect the test rig to the distanced environmental chamber, this test rig have had considerable parasitic inductances and series resistance. High parasitic elements result in oscillations and will adversely impact the performance of circuits. It will be seen in the measurements that impact of presence of parasitic elements is more pronounced in unipolar devices with high switching rates. Switching waveforms are captured on a

Tektronix TDS5054B digital oscilloscope which has a bandwidth of 500 MHz. The current is measured using a Tektronix TCP303 (rated 150 A) current probe useful for measuring AC/DC current which is connected to the oscilloscope through a TCPA300 amplifier with 100 MHz bandwidth. The current amplifier is calibrated on a 20 mV/A scale. The voltage probes are also from Tektronix model P5210A and are scaled on a basis of 1/100 with 50 MHz bandwidth. The accuracy and capability of the used equipment forms an important part of validity of the measurements results, therefore full details of the specifications of all the equipment used in the measurements are provided in section 3.2.1.

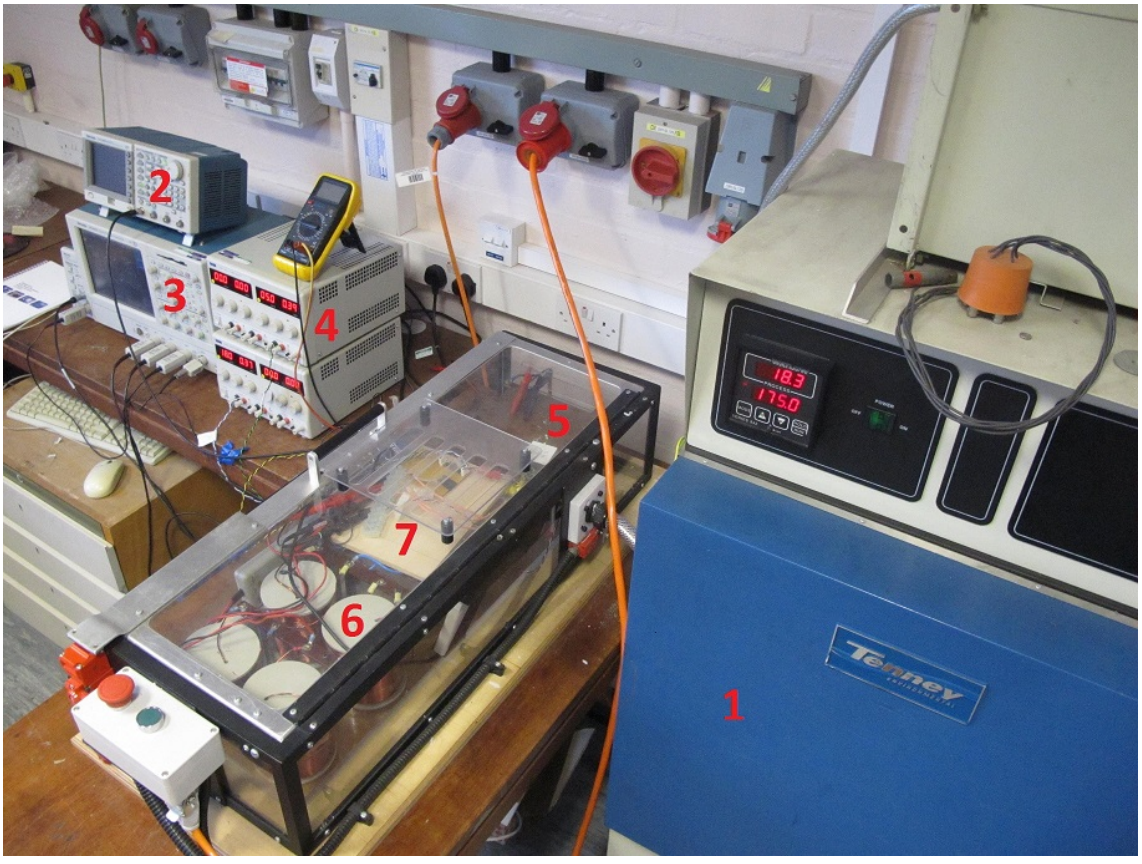


Figure 3.3: Components of LV inductive switching test rig: 1- Thermal chamber 2- Function generator 3- Digital oscilloscope 4- Gate drive power supplies 5- Bank capacitors 6- Inductors 7- Gate drive system.

Figure 3.4: Devices connection for LV measurements: 1- Transistor 2- Diode.

The second test rig which is used to perform the measurements in high voltages have overcame the high parasitics by using copper plates and rods, instead of wires. Hence the results of the high voltage measurements as shown in section 3.2.3 have less oscillations. The high voltage test rig is also equipped with a hot plate and capacitors/inductors with higher ratings. The equipments distance have also became minimal to reduce parasitics.

Figure 3.5 shows the picture of the high voltage experimental set-up fabricated and Figure 3.6 shows the connection arrangement of the transistor and diode. The switching waveforms are captured on a Tektronix TDS5054B digital oscilloscope with a bandwidth of 500 MHz. The current in this test rig is measured using a 'Pearson Electronics' wide band current monitor (Model 6656) calibrated on a scale of 1 A/V and the voltage is measured using Tektronix (P5210) differential voltage probes scaled on a basis of 1/100.

The low parasitic elements of this circuit is beneficial in an ideal application but is not always feasible to achieve. This is specifically the case where there are significant distance

between the components of a large circuit. As a result, it is important to investigate the impact of the circuit parasitic elements, and hence the results of the transients with presence of such stray components are in primary objectives of this investigation.

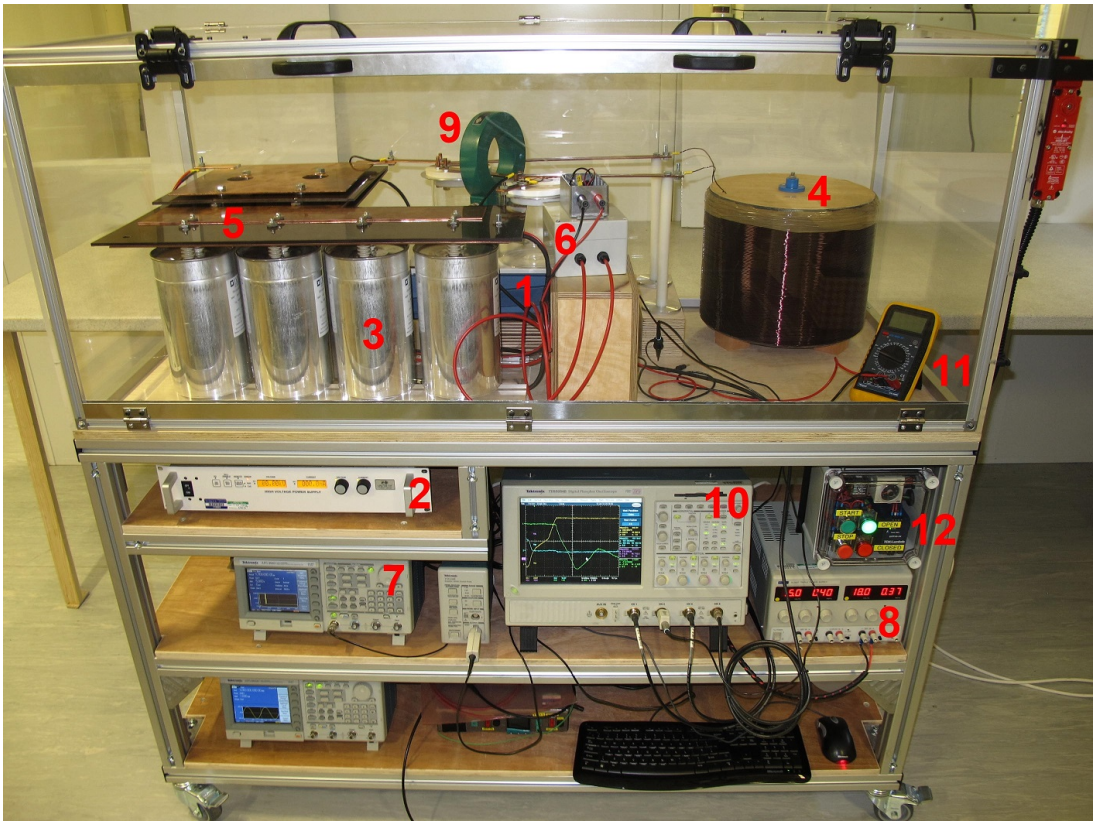


Figure 3.5: Components HV test rig: 1- Thermal conditioner 2- 12 kV power supply 3- 6.5 kV bank capacitors 4- 75mH inductor 5- Copper plates 6- Gate driver 7- Signal generator 8- Gate supply 9- Current probe 10- Oscilloscope 11- Voltmeter 12- Interlock.

The SiC MOSFETs used in these measurements are ROHM® SCH2080K rated at 1.2 kV and 35 A at T_C = 25 °C and 22 A at T_C = 100 °C whereas the SiC diodes are Semisouth® SDP30S120 rated as 46 A at T_C<100 °C. The IGBTs are IXYS® IXDH20N120D1 similarly rated as at 1.2 kV and 38 A at T_C = 25 °C and 25 A at T_C = 90 °C and the PiN diodes are IXYS® DSI45-12A similarly rated as 45 A at T_C = 130 °C. The values of the circuit components for both test rigs and the model parameters

used in the next section to emulate the EV drive-train converter are provided in Table 3.1. The switching tests are done using standard double-pulse method, i.e. the low-side transistor is switched on to charge the inductor to a pre-defined current level depending on the length of the first pulse and when the transistor is switched off, the current commutates to the diode and free-wheels, after which the transistor is switched on again and the diode turns-off and its current returns to the transistor with a reverse polarity.

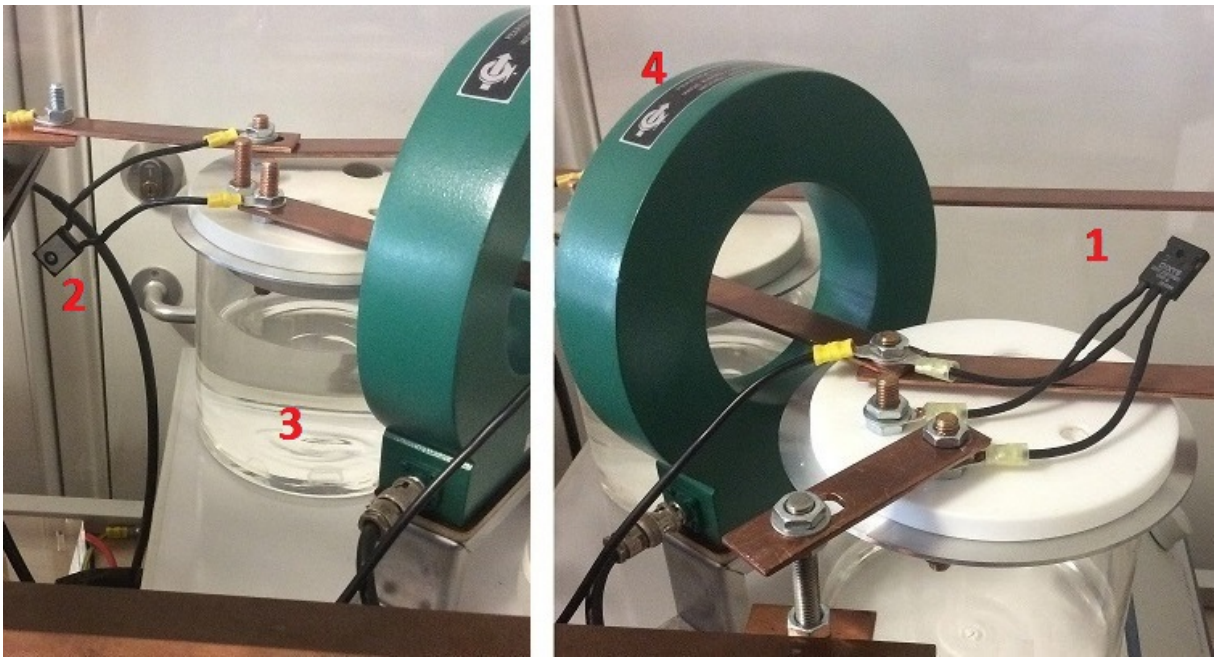


Figure 3.6: Devices connection arrangement for HV measurements showing:
1- Transistor 2- Diode 3- Hot plate oil container 4- Current monitor.

The circuit forces current commutation between the devices and is able to test the switching energies of the transistors and diodes. Figure 3.7 is showing the general classic double pulse test waveforms [23] where reverse recovery of PiN diode is clear.

Transistor switching is performed with a range of gate resistors from 10 Ω to 1 kΩ (with an incrementally increase on a logarithmic basis, thereby focusing more on lower gate resistances) correlating with dI_{DS}/dt ranging from 10 A/μs to 400 A/μs.

Table 3.1: Performance evaluations measurements: Parameters, units and their values.

Symbol	Description	Values
T	Temperature range	–75 °C - 175 °C
R_G	Gate resistances range	10 Ω - 1 kΩ
$L_{E\text{-}LV}$	Inductance of the LV test rig inductors	7.4 mH
$L_{E\text{-}HV}$	Inductance of the HV test rig inductors	75 mH
$C_{E\text{-}LV}$	Capacitance of the LV test rig capacitors	940 μF
$C_{E\text{-}HV}$	Capacitance of the HV test rig capacitors	94 μF
C_{DC}	Converter DC link capacitor	320 μF
C_{HF}	High frequency de-coupling capacitor	100 nF
$V_{DC\text{-}LV}$	Source DC voltage in LV test rig	100 V
$V_{DC\text{-}HV}$	Source DC voltage in HV test rig	1000 V
V_{PP}	Peak voltage on devices (as overshoot)	1120 V
$I_{DC\text{-}LV}$	Source DC current in LV test rig	3 A
$I_{DC\text{-}HV}$	Source DC current in HV test rig	125 mA
I_{PP}	Peak current by inductive/capacitive banks	30 A
P_{load}	Load power rating	1 kW
R_{th}	Thermal resistance of the heat sink	0.32 m^2K/W
C_{th}	Thermal capacitance of the heat sink	3.93 J/K
t_{Q1}	Duration of inductive signal	250 μs
t_{Q2}	Duration of gate switching signal	20 μs
f_{SW}	Switching frequency	5 - 15 kHz
V_{GG}	Gate voltage	18 V

The high gate resistance are beneficial to understand behaviour of power devices in case of slow commutations [24]. This wide range of gate resistances was also selected so as to ensure sufficient measurement information was obtained for investigating phenomena like the temperature dependency of device transients in both high and low switching rates, the dependency of the diode oscillation frequency and reverse recovery on switching rate.

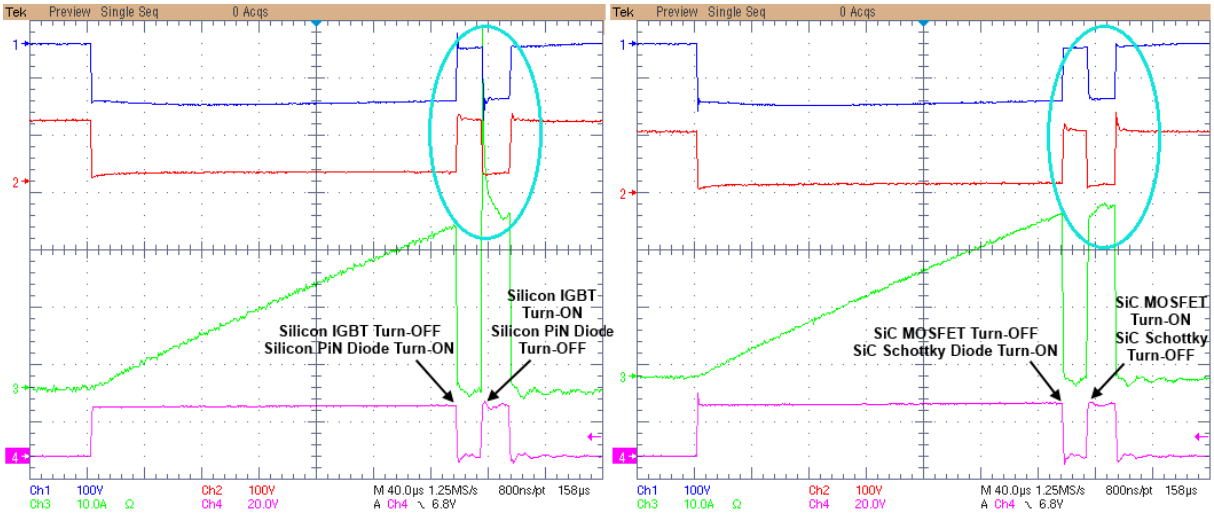


Figure 3.7: Double-pulse clamped inductive measurements
(L) Silicon devices, (R) SiC devices.

3.2.1 Specifications of Equipment

To perform accurate measurements, reliable and precise equipment are required. Therefore, an important part of every experimental measurement is to choose the equipment correctly and according to the requirements. In the next table, the equipment used in the measurements of this research are listed, along with all the vital details of their performance. These details include the resolution of measurements, the accuracy of output waveforms, the bandwidth of measurement devices and its correlation with temperature variations along with many other factors. Knowing these parameters assist in understanding how does the waveforms are captured and what has been the limitations and restrictions in the measurements. The equipment include two 4-channel digital oscilloscopes of different brands, two separate sets of high voltage probes, two versions of high current probes, a signal generator, a thermal chamber to vary the temperature and a thermal camera to record the change of temperature as a result of the performance of devices, along with passive components such as de-coupling capacitors and gate resistors.

Table 3.2: Specifications of all equipment used for the experimental measurements.

Equipment	Specifications	Appearance
Tenney Thermal Chamber Watlow 942	Range: –75 °C to +200 °C Accuracy: ±0.3 °C Workspace Dimenstions: 40 W × 28 D × 30 H Centimeters Controller: ¼ DIN profiling type Sensor type: RTD with dual outputs Current rating: 18 A Voltage rating: 100 / 240 V Frequency: 50 / 60 Hz Power: 1 PH	
Thermal Camera FLIR A320	Resolution: 320 × 240 pixels FOV: 25° 18.8° IFOV: 1.36 mrad F-number: 1.3 Sepctral range: 7.5-13 μm Focal length: 18 mm Thermal sensitivity: 50 mK (at +30C) Image frequency: 9 Hz / 30 Hz Detector pitch: 25μm Temperature range: –50 °C to +180 °C	

Table 3.2: Specifications of all equipment used for the experimental measurements.

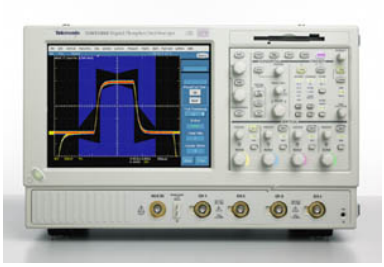
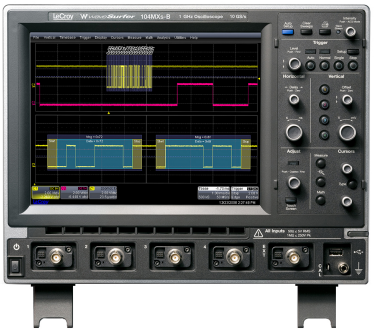
Tektronix 5054B Oscilloscope	Resolution: 8 bits DC Gain Accuracy: 1.5% (offset: 0 V) Bandwidth: 500 MHz Temperature Correlation: Upper limit derate to 30% relative humidity at 45°C Sample rate: 5 GS/s Rise time: 800 ps Time-base Accuracy: 15 ppm	
Lecroy 104mxs-b Oscilloscope	Resolution: 8 bits DC Gain Accuracy: ±1% Bandwidth: 1 GHz Temperature Correlation: Upper limit derate to 55% relative humidity at 40°C Sample rate: 5 GS/s Rise time: 350 ps Time-base Accuracy: $\leq$ 5 ppm	
Tektronix AFG3252C Function Generator	Overall Resolution: 14 bits Frequency Resolution: 1μHz Accuracy: 1±ppm Bandwidth: 120-240 MHz Sample rate: 2 GS/s Temperature Correlation: Upper limit derate to 80% relative humidity at 40°C	

Table 3.2: Specifications of all equipment used for the experimental measurements.

Tektronix Voltage Probe P5210A	Rating: ±5600 V Resolution: <150mV RMS at 100X Gain Accuracy: ±3% Bandwidth: 50 MHz Temperature Correlation: Upper limit derate to 85% relative humidity at 35°C Rise time: 7 ns CMRR at DC: >80 dB CMRR at 50 MHz: >30 dB	
GW INSTEK Voltage Probe GDP-100	Rating: ±7000 V Gain Accuracy: ±2% Bandwidth: 100 mHz Temperature Correlation: Upper limit derate to 70% relative humidity at 50°C Rise time: 3.5 ns CMRR: 80 dB at 60Hz, 50 dB at 1MHz	
Tektronix Current Probe TCP303	Rating: 150 A DC Resolution: Up to 5 mA Accuracy: ±3% of reading (10°C-50°C) Bandwidth: 15 MHz Temperature Correlation: Upper limit derate to 85% relative humidity at 50°C Rise time: ≤ 23 ns	

Table 3.2: Specifications of all equipment used for the experimental measurements.

Tektronix Current Amplifier TCPA300	Current rating: 150 A DC Volatge rating: 600 V_{rms} CAT I & II High-current sensitivity range: 50 A/V Low-current sensitivity range: 5 A/V Resolution: Up to 5 mA Accuracy: ±1% of reading(typical) Bandwidth: 15 MHz Insertion Impedance: 0.1 Ω at 15 MHz Temperature Correlation: Upper limit derate to 85% relative humidity at 50°C Range: 50 A/V	
PEARSON 6656 Current Monitor	Resolution: 1 Volt/Ampere Accuracy: ±1% Bandwidth: 100 MHz Temperature range: 0°C - 65°C Maximum current: 500 Amperes RMS current: 10 Amperes Drrop rate: 0.14% microseconds Rise time: 3.5 ns Current time product: MAX 0.01 Ampere-second Low Frequency 3 dB point: 200 Hz I^2t per pulse: 30 A^2s max	

Table 3.2: Specifications of all equipment used for the experimental measurements.

VISHAY MKP386 M410200JT5 Decoupling Capacitor	Capacitance: 0.1 μF Voltage: 2000 Volts Max current: 200 A Dielectric: Polypropylene film Accuracy: $\pm$5% MAX Temperature: 105 °C MAX dV/dt: 2000 $V/\mu s$
Gate Resistors	Range: 10 Ω - 1 kΩ Accuracy: $\pm$5% (Gold) Power: 250 mW Max voltage: 250 Volts Temperature range: 25 °C - 85 °C MAX pulse temperature: 105 °C

3.2.2 Calibration and Deskewing

For an experimental measurement to be accurate, certain condition must be met. These include a long list, however some of them are vital, an example of which is accurate measurement equipments, i.e. oscilloscopes and probes. A good oscilloscope with an adequate bandwidth along with a high sampling rate and resolution is extremely important if accurate measurements at high frequency are to be performed. The same stands for high voltage and high current probes which have the required bandwidth according to the

frequency of switchings. However, even the most expensive and hi-tech oscilloscope might go out of calibration. Therefore, having an high-end measurement equipment does not necessarily mean that the measurements have in fact been accurate. Therefore, to ensure on the precision of the results, it is necessary that the measurement equipment to be calibrated and tested before the measurements. Calibration of the oscilloscope and probed must be done on a routine basis according to the recommendation of the manufacturer, and in most cases cannot be done by the user. However there are certain techniques that a user can apply to remove possible temporary de-calibration from the oscilloscope and/or probes in high frequency measurements. The most important of these is 'deskewing'.

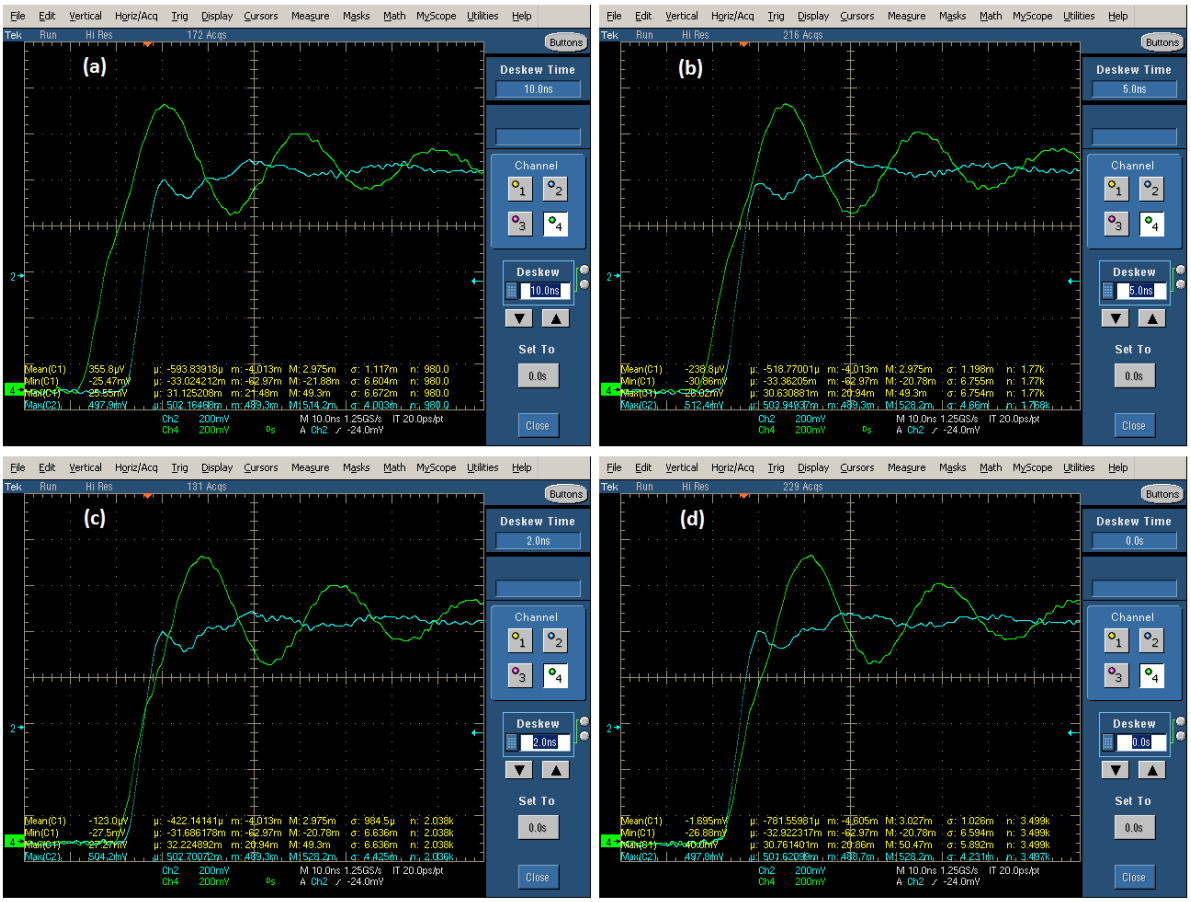


Figure 3.8: Oscilloscope voltage deskew with 10 ns, 5 ns, 2 ns and 0 ns phase shift.

Figure 3.8 shows the deskewing of the voltage waveforms. This is done mainly to ensure that different voltage probes connected on different channels of the oscilloscope are in the same phase shift for measurements. Should this not to be the case, the measurements of one channel with a given voltage probe will be different than the same measurement with another probe using a different channel. Hence, before any measurement, the voltage probes are connected to the fixed-signal-output of the oscilloscope and the results are shown on the oscilloscope screen as seen in Figure 3.8. This enables the user to ensure that all probes/channels are receiving the same standard waveform and their output can be compared accurately. It can be seen that in this particular case, there is no need for manual deskewing as the two voltages are well in-phase with each other as seen in Figure 3.8(d), while inserting a 10 ns, 5 ns and 2 ns delay will result in the waveforms to become out of phase. However, if the initial voltages were not in phase, the deskewing option would have enable the user to manually shift them to become in-line.

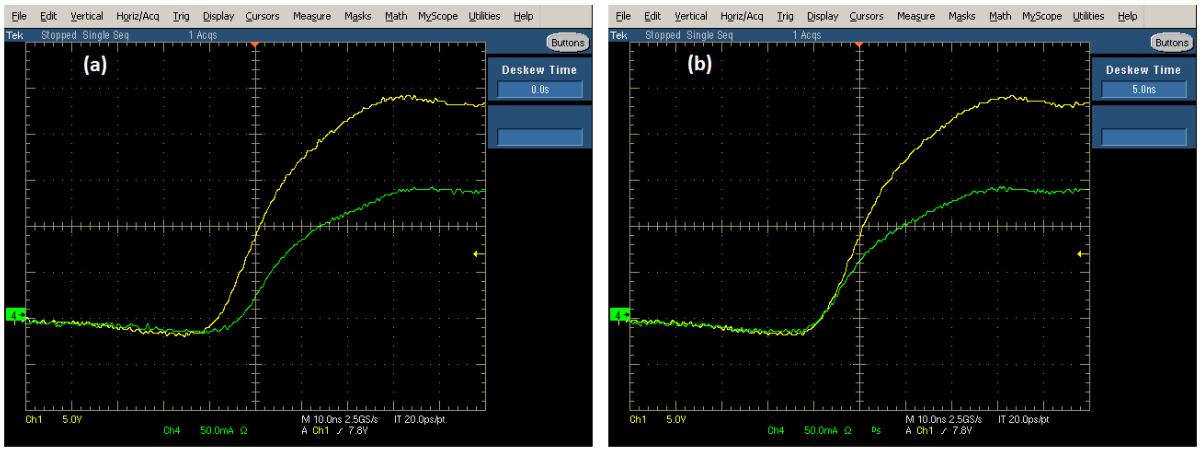


Figure 3.9: Current deskew of the oscilloscope with 5ns, fixing the phase difference between the voltage and current.

Figure 3.9 is showing the deskew of the current which is of even higher importance. This can be done by different techniques, some of which use complicated equipments to

provide an in-phase voltage and current for the oscilloscope to measure and compare. However, a basic method would be use a pure resistive load, where the applied voltage would result in an in-phase current. This technique has been used in Figure 3.9 where it can be seen that there is 5 ns delay between voltage and current. It must be emphasized that this technique is only reliable if the load is of a pure resistive nature, and even an slight inductive behaviour of the load would result in a natural phase shift which must not be confused with the oscilloscope error. Here, the delay as a result of de-calibration when using a pure resistive load can be corrected using the deskew function by inserting a 5 ns manual phase shift to make the waveforms in-line. This is seen in Figure 3.9(b).

3.2.3 The 1 kV Measurements

Figure 3.10(a) shows the voltage turn-on characteristics of Si-IGBT and SiC MOSFET switched with a gate resistance of $R_G = 15\ \Omega$ whereas Figure 3.10(b) shows the current turn-on characteristics. As seen in Figure 3.10(a) and (b), the IGBT voltage takes a significantly longer time to turn-off. It should be noted that the time-axis is scaled on a logarithmic basis, thereby the slopes of the waveforms do not represent a linear trend. This is done because in all cases, the Si-IGBT device has taken significantly longer to complete the transient and shouldn't it be for the logarithmic scale of the x-axis, it would not be possible to compare the two waveforms on the same figure. Likewise the previous case, Figure 3.10(c) shows the voltage turn-on characteristics of the devices when switched with $R_G = 150\ \Omega$ whereas Figure 3.10(d) shows the current turn-on characteristics. Both devices are switched at 1 kV at room temperature under identical conditions.

Figure 3.11(a) to 3.11(d) show the corresponding plots for turn-off. As was expected, the waveforms in higher R_G are shifted to the right of the figure on the logarithmic scale,

meaning a higher duration for the transients. The peak overshoot in Figure 3.10(b) and (d) in the Si-IGBT are the result of PiN diode reverse recovery, while in the SiC MOSFET are the result of oscillations as a consequence of parasitic elements. It is seen that the on-state conduction current (which is the forward current of the diodes) is the same for the case of both devices. The level of this forward current depends on the length of the charging pulse defined by gate driver which is identical in both cases.

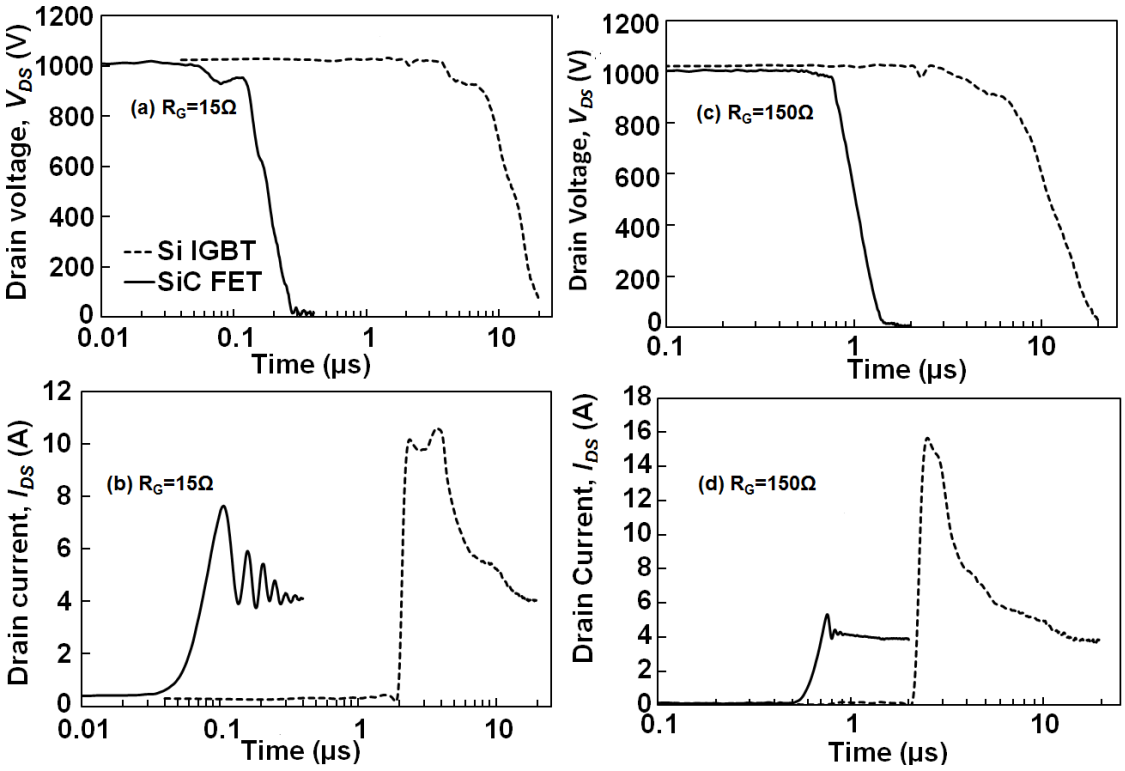


Figure 3.10: Turn-on waveforms of silicon IGBT / SiC MOSFET with 15 Ω and 150 Ω gate resistances respectively at 1 kV voltage rating.

As seen, the oscillations in the output current of SiC device in Figure 3.10(b) are damped with increasing R_G as was expected. In both Figure 3.10 and Figure 3.11 the forward current on the devices are intentionally reduced significantly by reducing the charging pulse length to instead increase the voltage to the 1 kV rating (given the possible

parasitics in the circuit, operating the device in the nominal rating of voltage and current simultaneously might result in destruction of the device). Hence, it is seen that the reverse recovery charge in the case of silicon device is slightly increased when switched slower.

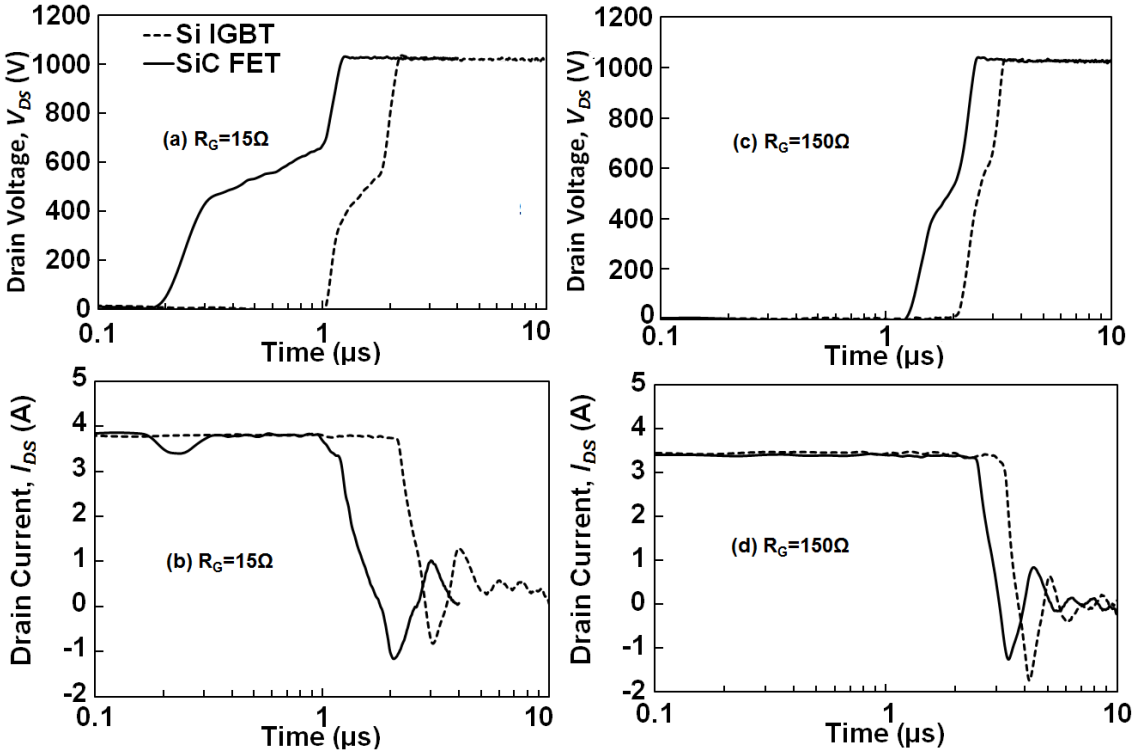


Figure 3.11: Turn-off waveforms of silicon IGBT / SiC MOSFET with 15 Ω and 150 Ω gate resistance respectively at 1 kV voltage rating.

As seen in Figure 3.11(a) and (c), the voltage transients at turn-off do not exhibit any voltage overshoot which would normally occur as a result of dI/dt of switching coupled with the parasitic inductance of the circuit/packaging. This happens due to the very low degree of parasitic elements in this circuit as would have been expected from Figure 3.5. Also as explained earlier, the current levels in this circuit are intentionally low to enable increasing the voltage levels to the nominal value. This is in contrast with Figure 3.3 where the lengthy wires in the circuit are resulting in high parasitic inductances. So the

overshoots will be more evident in the high current transients as the measurements in the low voltage circuit are performed at nominal current levels with lower voltages.

Figure 3.12 shows the switching energy for all gate resistances for the silicon IGBT and the SiC MOSFET where it can be seen that the SiC MOSFET exhibits an average of 80% lower switching energy. This significant reduction is more obtainable in low parasitic switchings, since no significant voltage overshoot or ringing is present here, especially for the case of the SiC devices. As will be seen in the next section, presence of high parasitic elements deteriorate the superiority of SiC MOSFET switching energy, although its overall switching energy is still lower. Despite the lower mobility and carrier lifetime in SiC compared with silicon, as unipolar devices they switch fast and hence coupled with the parasitic elements of the circuit can generate considerable switching energies. This phenomenon can be seen more clearly in higher parasitic circuits, and is pronounce in SiC Schottky diodes. Should this be the case, the Figure 3.12 should be amended. This will be done in Figure 3.40 and Figure 3.41 for a wide temperature range.

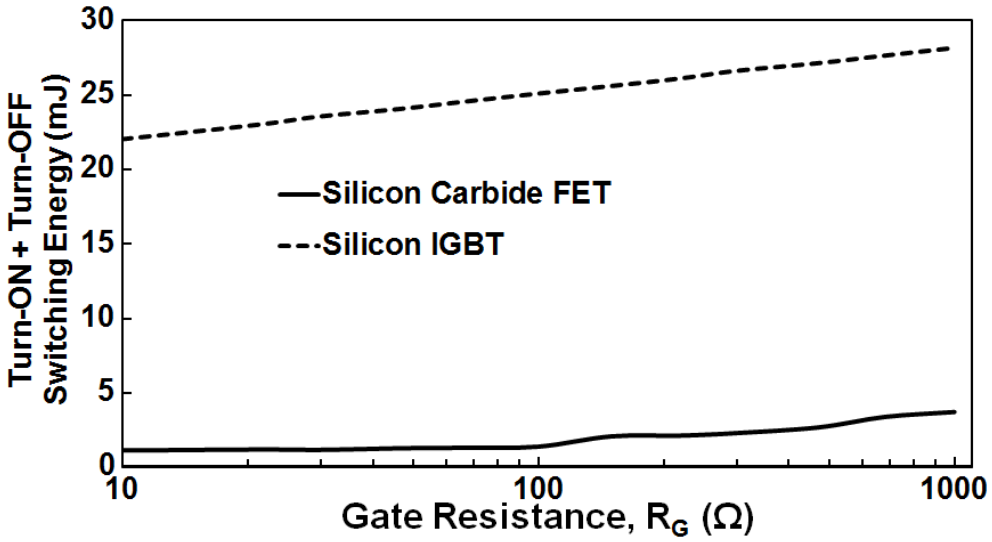


Figure 3.12: Switching energy as a function of R_G for the SiC MOSFET and Si-IGBT showing significantly better performance of the SiC MOSFET, at 25 °C with 1 kV.

Figure 3.13 shows the switching energy as a function of the applied voltage on the DC bus. The switching energy has been normalized by the current so it is presented in mJ per Amp. This has been done since as seen in the measurements, by increasing the voltage on the device, the current is also increased proportionally. Hence to provide the possibility of understanding the trends with voltage, and to keep the current as a constant value, the figure is presented as normalized by current. Figure 3.13 shows that the switching energy per Amp increases in a relatively linear manner with the increase of voltage for both devices at turn on and turn off transients. Therefore, the improved performance and superior behaviour of the SiC transistors can be extended to higher voltages, should the parasitic elements of the circuit be minimized or their impact on the transient of devices to be mitigated. In the following, the switchings are assessed using the low voltage test rig set-up for temperatures between –75 °C and 175 °C.

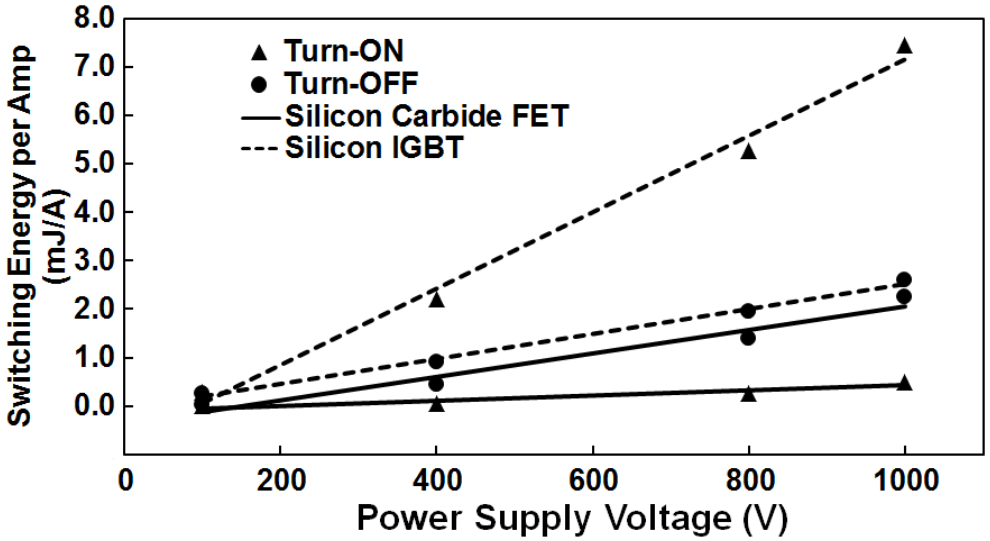


Figure 3.13: Switching energy per Amp of silicon IGBT/SiC MOSFET following a linear trend on a range of voltages tested up to 1 kV with $R_G = 15\ \Omega$ at 25 °C.

3.2.4 Error Analysis

To estimate how much a phase shift can impact the results' accuracy, an error analysis is performed. Here, the switching energy of silicon PiN diode in Figure 3.14 and the SiC Schottky diode in Figure 3.15 are calculated in two different switching rates (with R_G of 10 Ω and 100 Ω) and three different temperatures (–75 °C, 25 °C and 175 °C) and an intentional time delay as the phase shift (from –20 ns to +20 ns) is also imposed, while the margin of difference compared with reference value is calculated as the error percentage.

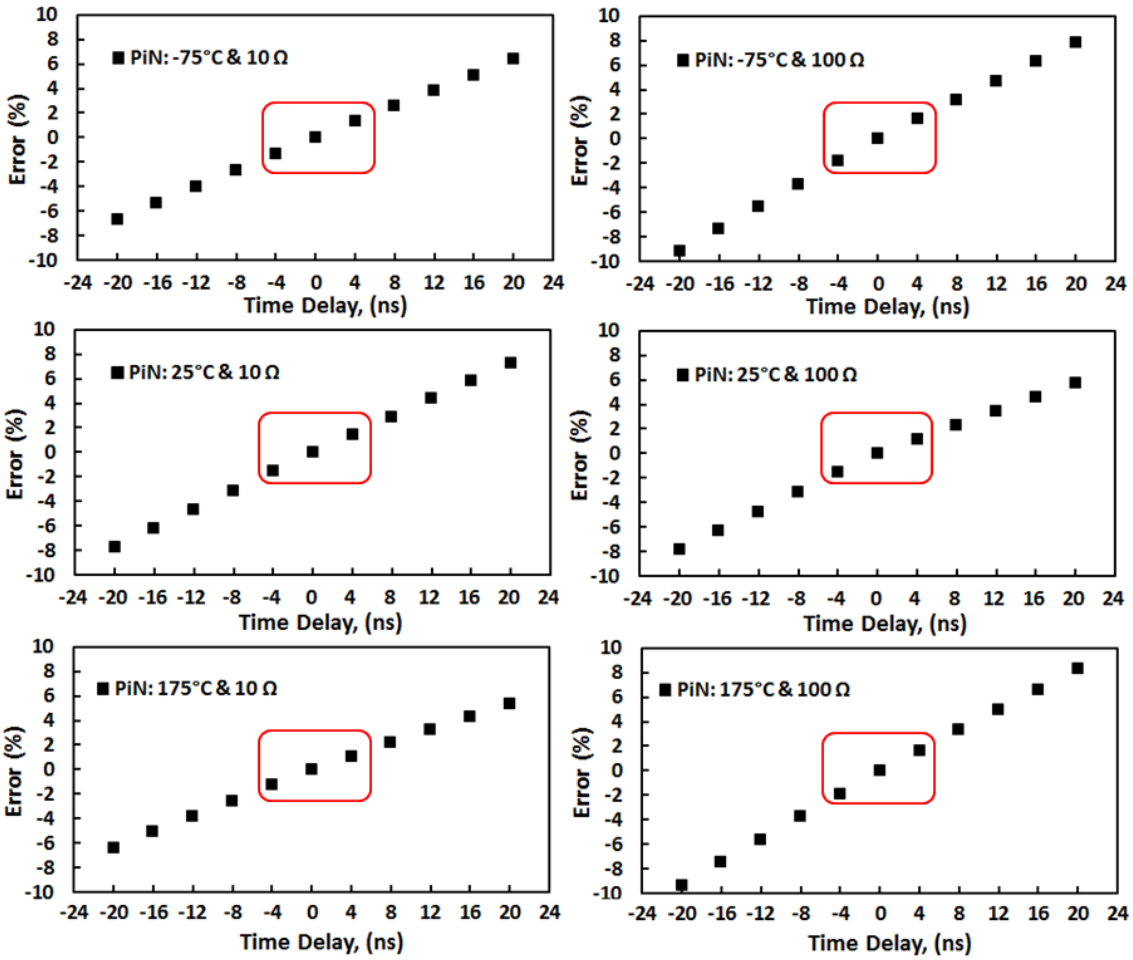


Figure 3.14: Error analysis of Si-PiN diode switching energy based on time delay between voltage and current for different switching rates and temperatures.

It is seen in Figure 3.15 and Figure 3.14 that the time delay has increased or decreased the calculated switching energy, where due to the more significant value of switching energy in PiN diode, its variation is also higher. It is also seen that in all cases, regardless of the switching rate or temperature, as long as the time delay (phase shift error) is within the 5 ns margin (shown with red box) which was seen in section 3.2.2 as the possible phase shift of the oscilloscope/probe combination used in these measurements without deskewing, the maximum error is within 2% margin which is a trivial value.

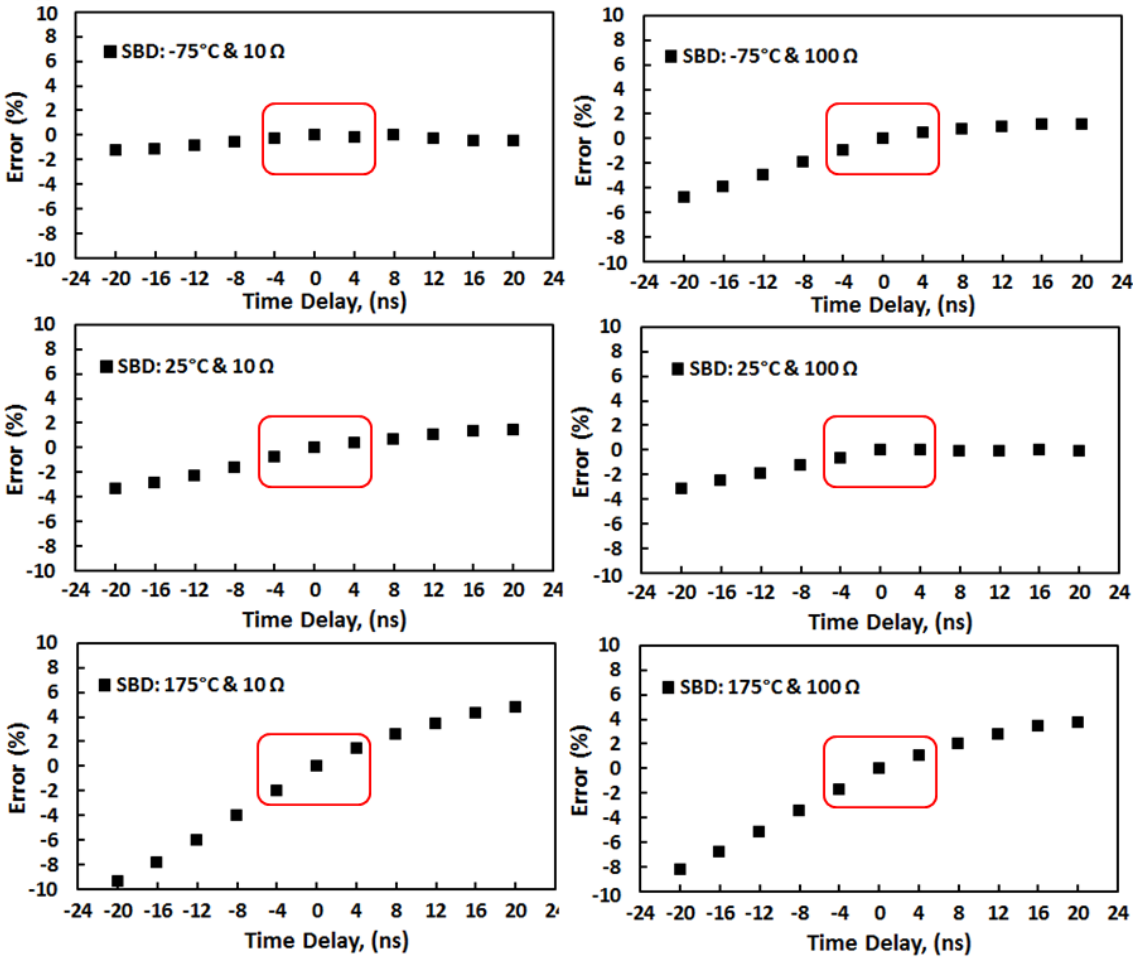


Figure 3.15: Error Analysis of SiC-SBD diode Switching Energy based on time delay between voltage and current for different switching rates and temperatures.

3.3 Temperature Dependency of Switching Energy

In device measurements, the ambient temperature set by the chamber, is not exactly the junction temperature due to switching energy dissipated as heat. However, self-heating can be excluded as the dissipated heat of a single switching event is insignificant. Additionally to reassure on the results of individual tests, sufficient time is given so as to allow the devices remain in equilibrium with the ambient temperature. Next, the turn-on and turn-off transients of the transistors and diodes are shown with two cases of fast and slow switching in three different temperatures. This is along the 3D presentation of the switching energy. Note that all dI/dt values on 3D graphs are samples taken at 25 °C.

3.3.1 Transistors Turn-on

Figure 3.16 shows the turn-on switching energy of the SiC MOSFET as a function of the dI_{DS}/dt (determined by the gate resistance) and temperature. It can be seen from Figure 3.16 that the best turn-on performance of the SiC MOSFET is when it is driven at high switching rate and in higher temperatures. The switching energy decreases with increasing temperature and dI_{DS}/dt (decreasing R_G). The negative temperature coefficient of the switching energy in the SiC MOSFET is due to the fact that dI_{DS}/dt increases with temperature during turn-on. This can be seen in Figure 3.17 and Figure 3.18 where the turn-on voltage and current transients are shown at different temperatures for the 15 Ω and 150 Ω switchings respectively. A comprehensive analysis of the switching rate of the SiC MOSFET will be shown in next chapter in Figure 4.34 and Figure 4.35 where the trend of the dI_{DS}/dt with temperature and R_G is clear. Higher dI_{DS}/dt generally reduces the duration of the switching transient, thereby reducing the switching energy.

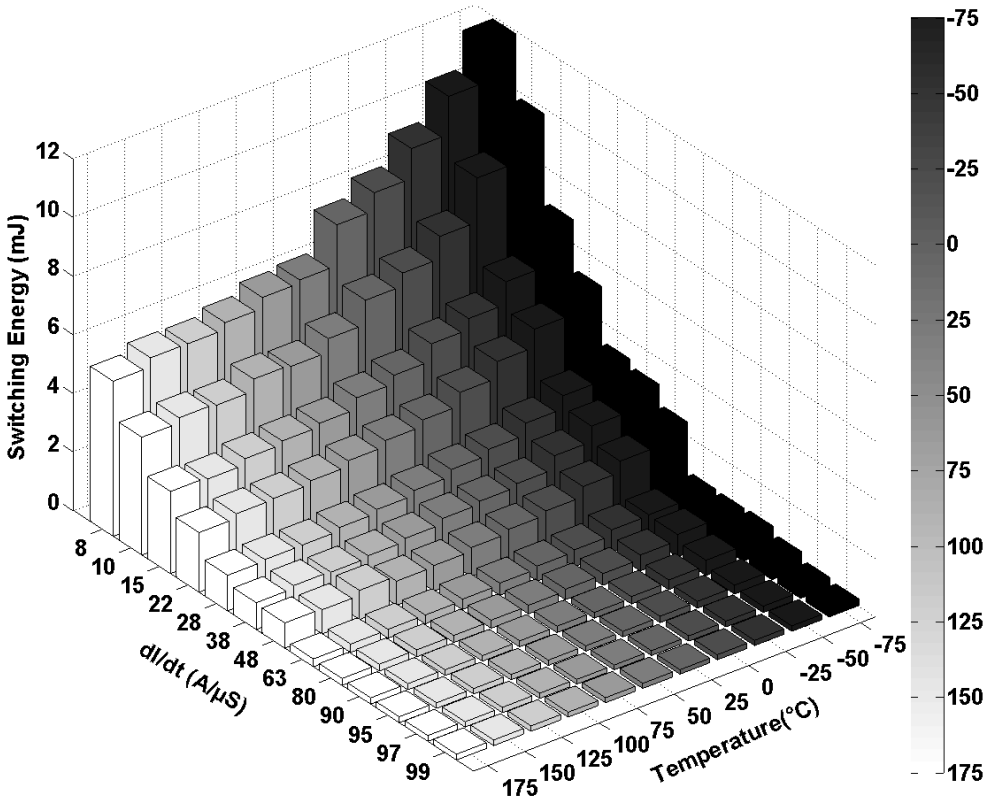


Figure 3.16: Switching energy of SiC MOSFET at turn-on.

The dI_{DS}/dt varies from 100 $A/\mu s$ for 10 Ω gate resistance and reduces with increasing R_G. The negative temperature coefficient of the threshold voltage of the SiC MOSFET is the main reason of faster switching at higher temperatures, where the expected threshold voltage is lower, i.e. the V_{GG} will reach the V_{TH} faster. This will also be qualitatively explained in Equation 4.36 in the next chapter. The rate of change of the dI_{DS}/dt with temperature increases for the larger gate resistances. Hence, for example at turn-on of SiC MOSFET with $R_G = 15\ \Omega$ (as is shown in Figure 3.16), the switching energy decreases by 20% when the temperature is increased from –75 °C to 175 °C, whereas at $R_G = 150\ \Omega$, the switching energy decreases by 40% for the same range of temperature change. This means that the SiC devices are temperature-invariant only if they are switched at high enough switching rates. Analysis of transients will also be discussed in next chapter.

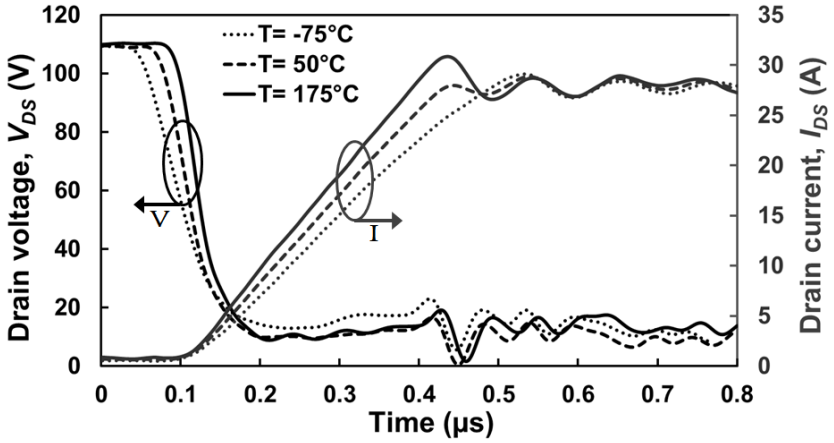


Figure 3.17: SiC MOSFET turn-on voltage and current with R_G of 15 Ω.

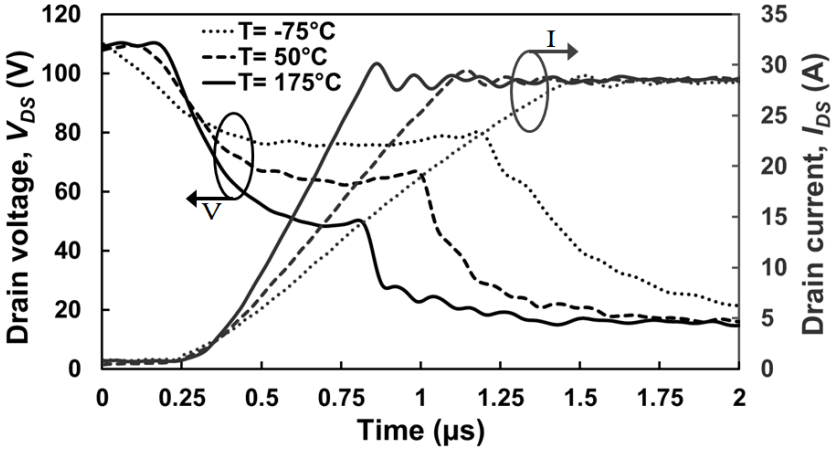


Figure 3.18: SiC MOSFET turn-on voltage and current with R_G of 150 Ω.

Figure 3.19 shows the turn-on switching energy as a function of the temperature and switching rate for the silicon IGBT. Unlike the case of the MOSFET, it is seen that the switching energy increases with temperature for all switching rates. This is due to the bipolar nature of IGBTs, i.e. impact of mobility of carriers on formation of conductivity modulation and the turn-off reverse recovery current of the PiN diode. Figure 3.20 and Figure 3.21 show the voltage and current of turn-on transients in the silicon IGBT at different temperatures with $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$ respectively.

In bipolar devices, in this case the IGBT and PiN diode, increase of temperature will decrease the mobility of carriers while it increases the lifetime of the carriers present in the conductivity modulation region. Hence, as temperature is increased the switching duration is prolonged. This means that the voltage drop will take longer in higher temperatures, and the reverse recovery current of complementing PiN diode is increased both in terms of its amplitude and duration as shown in Figure 3.20 and Figure 3.21.

This impact of temperature in this case is pronounce both for high and low switching rates, therefore unlike the SiC MOSFET, the performance of the silicon IGBT is more temperature dependant regardless of the driving R_G. For the silicon IGBT with $R_G = 10$ Ω, the switching energy increases by 10% when the temperature is increased from –75 °C to 175 °C, whereas at $R_G = 150$ Ω, the switching energy increases by around 25% for the same temperature range. The impact of temperature and the gate resistance on the switching rate of the Si-IGBT at turn-on will be shown in Figure 4.12 and Figure 4.13.

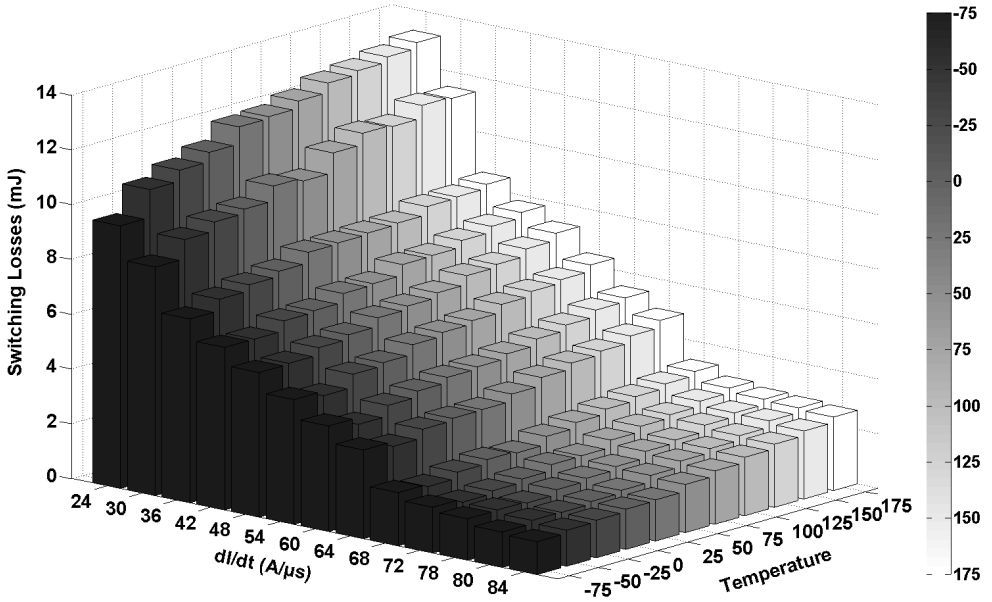


Figure 3.19: Switching energy of silicon IGBT at turn-on

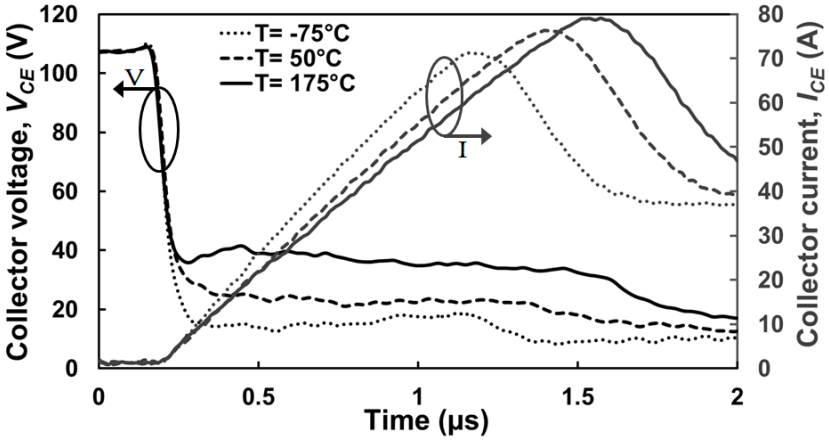


Figure 3.20: Silicon IGBT turn-on voltage and current with R_G of 15 Ω.

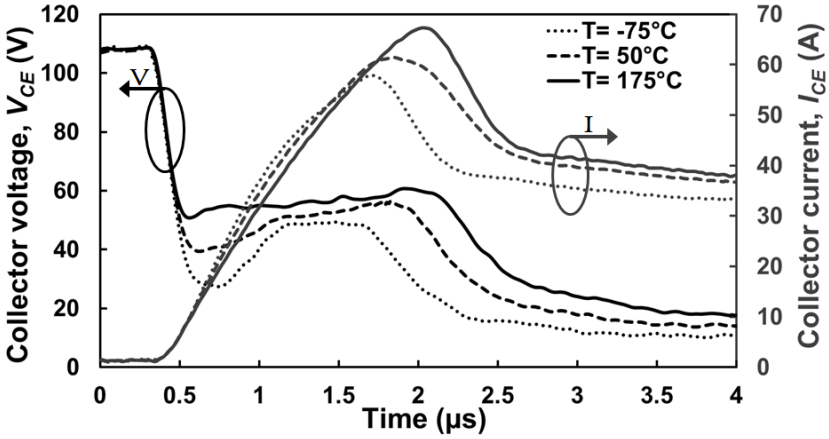


Figure 3.21: Silicon IGBT turn-on voltage and current with R_G of 150 Ω.

3.3.2 Transistors Turn-off

Figure 3.22 shows the turn-off switching energy of the SiC MOSFET at different temperatures and switching rates. Unlike the turn-on characteristics, the switching energy increases with temperature during turn-off. This trend is due to the fact that dI_{DS}/dt increases with decreasing temperature during turn-off which is opposite to the trend during turn-on. Figure 3.23 and Figure 3.24 show transient turn-off current and voltage characteristics for the SiC MOSFET with $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$ respectively.

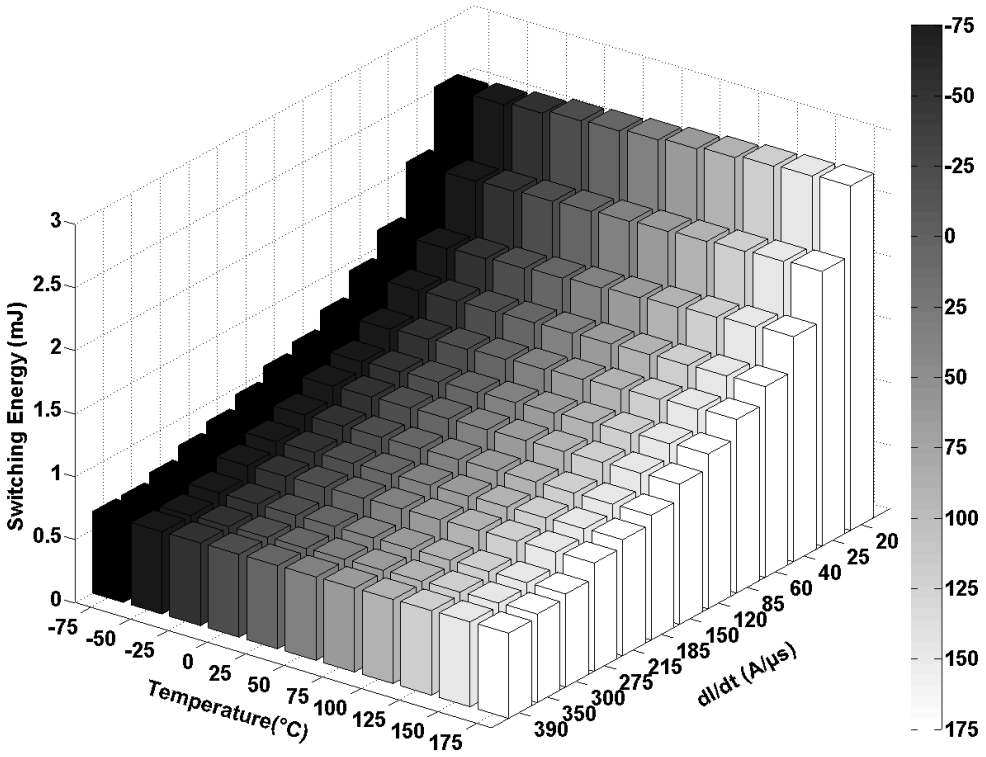


Figure 3.22: Switching energy of SiC MOSFET at turn-off.

It can be seen from Figure 3.23 and Figure 3.24 that the currents and voltages switch faster at lower temperatures. This is due to the negative temperature coefficient of the MOSFET's threshold voltage, hence, as the gate is driven from 18 V to zero, the higher threshold voltage of the colder ambient causes the device to turn-off quicker. Also, the peak voltage overshoot in the drain voltage is higher when the device is switched faster. As seen in these figures, the high parasitic value of the circuit is pronounce in the voltage overshoot of the device at turn-off. In Figure 3.23 the peak rises to 460 V for $R_G = 15\ \Omega$ and in Figure 3.24 the peak voltage is 270 V for $R_G = 150\ \Omega$. It can also be seen that the peak voltage overshoot increases as the temperature decreases as a result of the negative temperature coefficient of dI_{DS}/dt during MOSFET turn-off. The switching energy of SiC MOSFET during turn-off shows a slight increase with temperature rise [25].

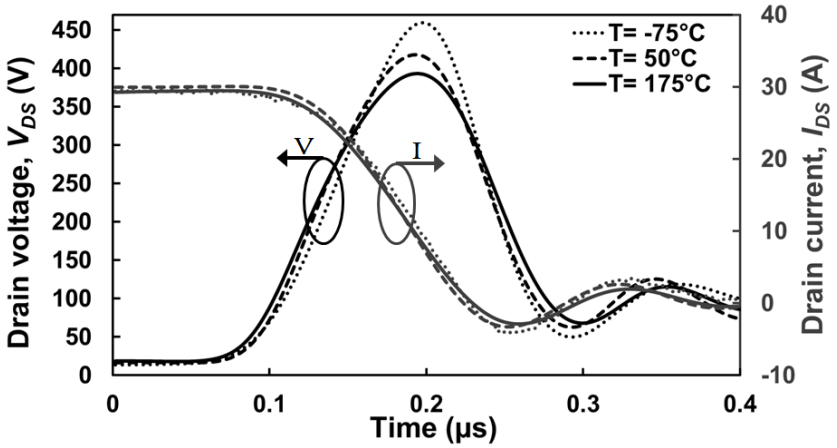


Figure 3.23: SiC MOSFET turn-off voltage and current with R_G of 15 Ω.

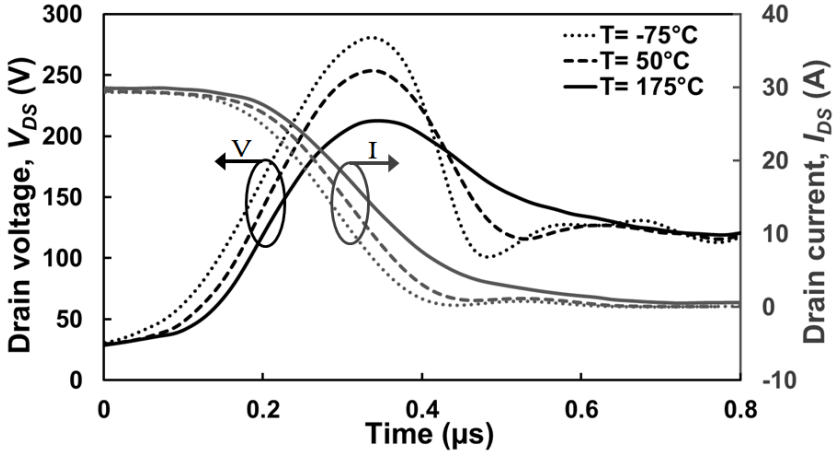


Figure 3.24: SiC MOSFET turn-off voltage and current with R_G of 150 Ω.

This is due to the fact that oscillations are damped and the voltage overshoot is decreased, but the transient duration is also prolonged. The impact of temperature on the switching rate of the SiC MOSFET at turn-off will be shown in Figure 4.36 and 4.37.

Figure 3.25 shows the turn-off switching energy of the IGBT. The switching energy increases with temperature during turn-off because the dI_{CE}/dt at a given R_G decreases as temperature increases. An slower current transient, although reduces the voltage peak, but results in coinciding between the voltage overshoot and a higher turn-off current.

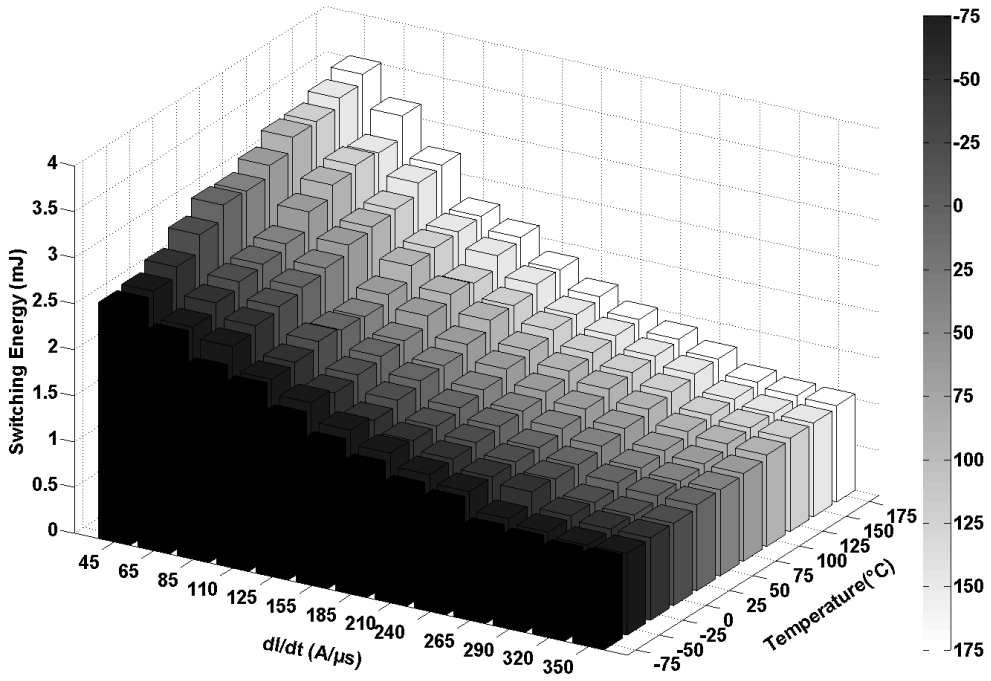


Figure 3.25: Switching energy of the silicon IGBT at turn-off.

Figure 3.26 and Figure 3.27 show the IGBT's V_{CE} and I_{CE} transients at different temperatures switched with $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$ respectively. Similar to the case of turn-off in the MOSFET, the IGBT peak V_{CE} overshoot increases as the temperature is reduced because of the negative temperature coefficient of dI_{CE}/dt. The impact of temperature and the switching rate of the Si-IGBT at turn-off will be shown in Figure 4.10 and Figure 4.11. As can be seen here, the IGBT does not present a significant tail current at turn-off. The usual tail current is due to minority carrier recombination in the drift region as the device is turned off. However, the IGBT used is a Non-Punch-Through (NPT) device which has been optimized for low switching losses. Because there is no highly doped N^+ layer between the voltage blocking drift region and the P^+ body, minority carrier injection is lower than the punch-through IGBTs [26–28]. Hence, the tail current is of a significantly lower value, although will last longer than the PT IGBTs [29]. The lower tail current in NPT-IGBTs also makes the device more temperature invariant.

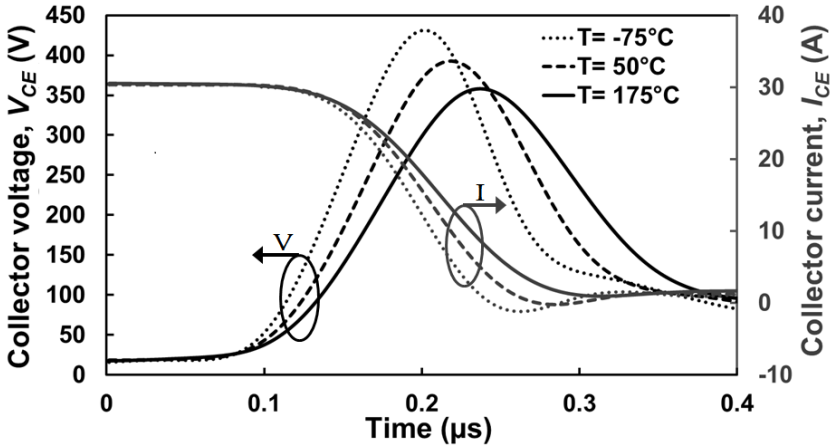


Figure 3.26: Silicon IGBT turn-off voltage and current with R_G of 15 Ω.

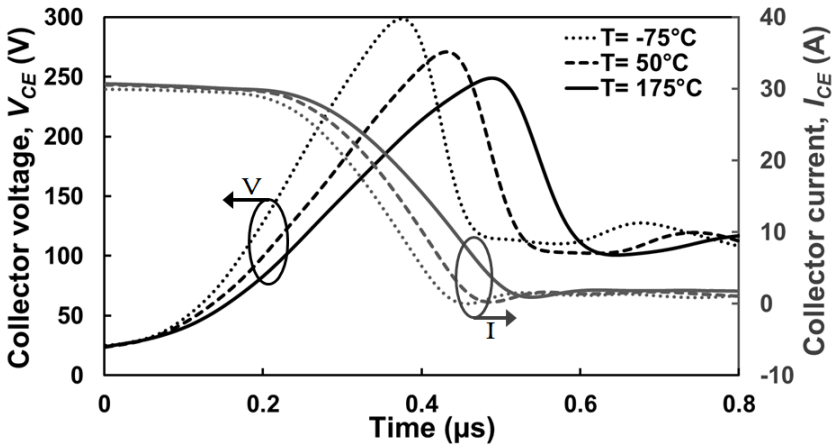


Figure 3.27: Silicon IGBT turn-off voltage and current with R_G of 150 Ω.

3.3.3 Diodes Turn-on

Figure 3.28 shows the turn-on switching energy of the SiC Schottky diode at different temperatures and MOSFET dI_{DS}/dt. Since the turn-on of diode coincides with the turn-off of the SiC MOSFET, the dI_{AK}/dt of current through the diode decreases as the temperature increases. The U-shaped characteristic of the switching energy is due to the trade-off happening between the impact of higher switching rates on oscillations (overshoots, undershoots) and the overlapping period of the waveforms with the transient duration.

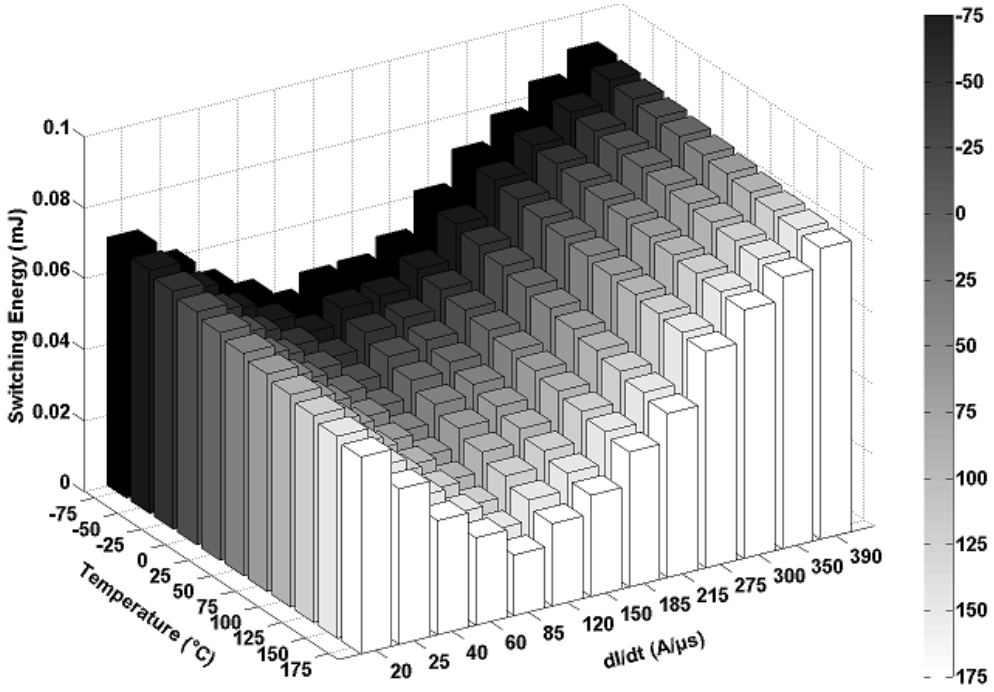


Figure 3.28: Switching energy of SiC SBD at turn-on.

Figure 3.29 and Figure 3.30 show the diode turn-on current and voltage transients for $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$ respectively. It can be seen from Figures 3.29 and Figure 3.30 that the dI_{AK}/dt and dV_{AK}/dt increase as the temperature is reduced. It can also be seen that the rate of increase is higher for $R_G = 15\ \Omega$ than for $R_G = 150\ \Omega$. As seen in these figures, at lower dI_{AK}/dt there is less overlapping between the current and voltage transients, hence reducing the switching energy. However, at very high gate resistances, the increased duration of switching becomes the dominant factor in determining the switching energy and hence it again increases. Overall the impact of temperature in turn-on is small. The SiC Schottky diode has smaller switching energy at turn-on compared to its turn-off transient. Also the turn-on transient does not impose a reliability stress to the circuit, in contrary to the turn-off which has higher switching energy and significant ringing in the output. This is seen in the following section.

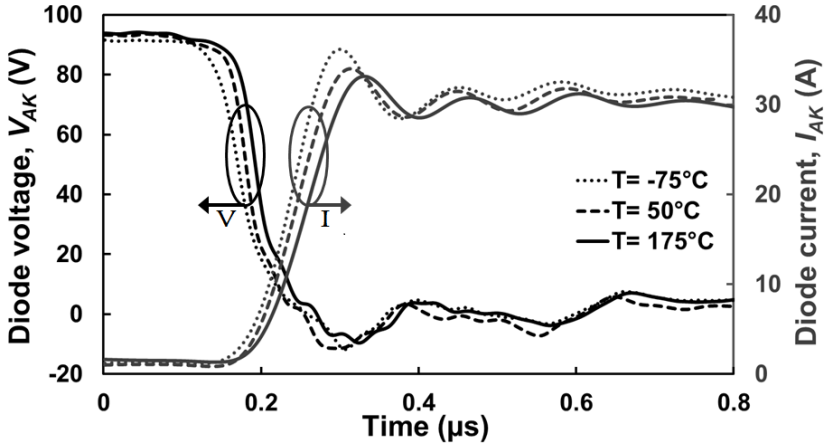


Figure 3.29: SiC SBD at turn-on voltage and current with R_G of 15 Ω.

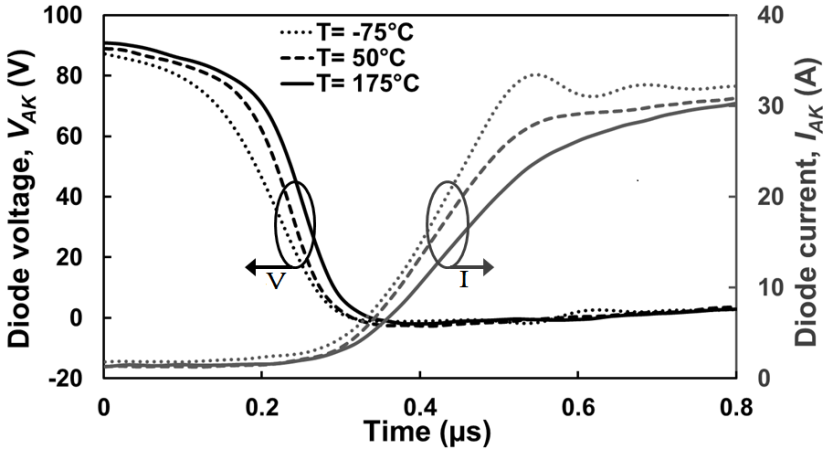


Figure 3.30: SiC SBD at turn-on voltage and current with R_G of 150 Ω.

Figure 3.31 shows switching energy of the silicon PiN diode at different temperatures and different IGBT dI_{CE}/dt during turn-on. The switching energy increases with temperature as expected because of the temperature dependent mobility and lifetime of the minority carriers in the conductivity modulated region, meaning that by increase of temperature, the mobility of the carriers forming the conductivity modulation in the drift region of the PiN diode is decreased despite their life time is increased. As a result, upon diode turn-on (IGBT turn-off) the plasma formation in PiN diode takes longer at higher temperature, hence extended transients and higher switching energy.

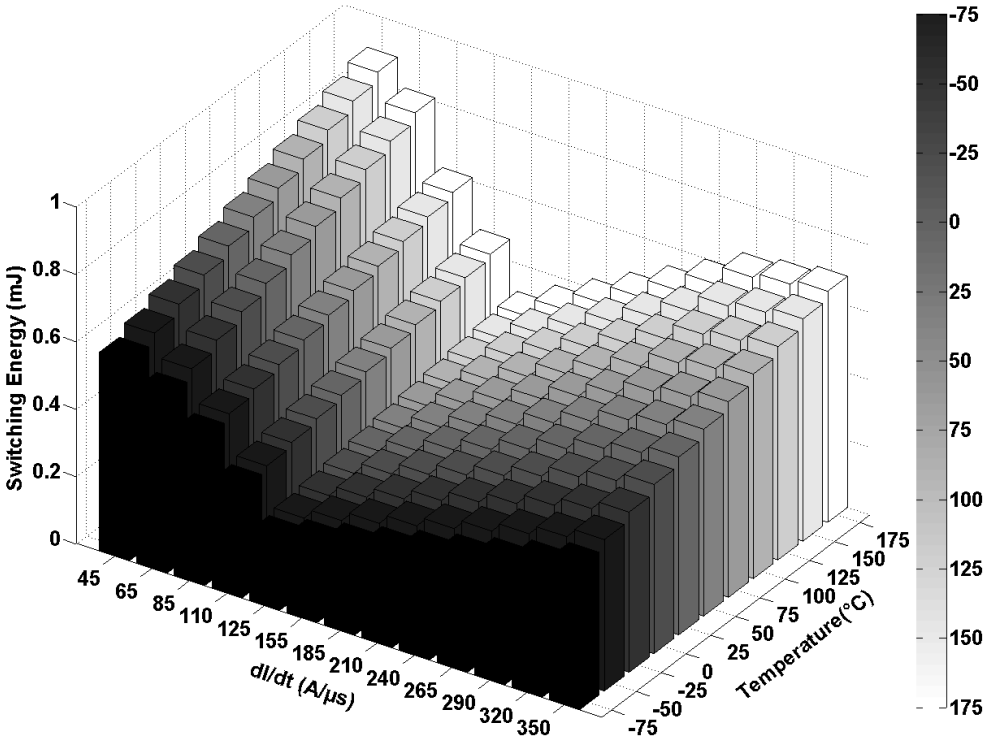


Figure 3.31: Switching energy of silicon PiN diode at turn-on.

Figure 3.32 and Figure 3.33 show the PiN diode voltage and current transients at different temperatures for $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$ respectively. It can be seen from Figures 3.32 and 3.33 that the dI_{AK}/dt increases as the temperature is reduced similar to the IGBT currents. At high switching rates, the switching energy is dominated by current overshoots whereas at low switching rates, the switching energy is dominated by the transient delay. Hence, the device have an optimum point for the dI/dt where the switching energy is minimized. As seen in Figure 3.28, increasing the gate resistance from $R_G = 15\ \Omega$ to $R_G = 150\ \Omega$ has damped the oscillations on the voltage and current waveforms, although at the expense of prolonging the duration of the switching. This results in a trade-off between the two factors.

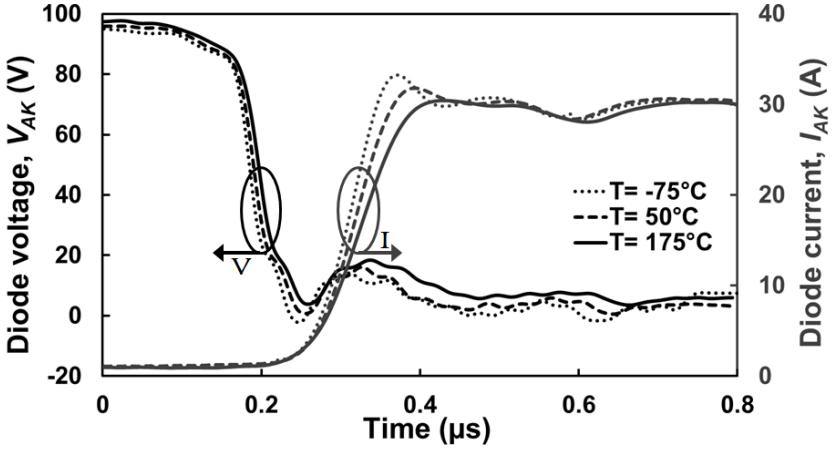


Figure 3.32: Silicon PiN diode turn-on voltage and currents with R_G of 15 Ω.

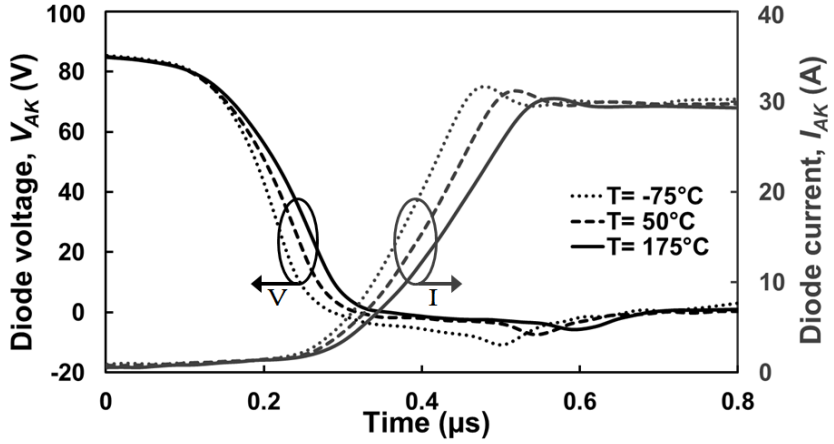


Figure 3.33: Silicon PiN diode turn-on voltage and currents with R_G of 150 Ω.

3.3.4 Diodes Turn-off

Figure 3.34 shows the SiC Schottky diode switching energy as a function of temperature and MOSFET dI_{DS}/dt during turn-off. Similar to the case of the diode turn-on, the switching energy exhibits a U-shaped characteristic as a function of the MOSFET's dI_{DS}/dt. This happens since at high switching rates, the ringing of the Schottky diode dominates the switching losses while at lower switching rates, the duration of the transient is the dominant source of increase in switching energies.

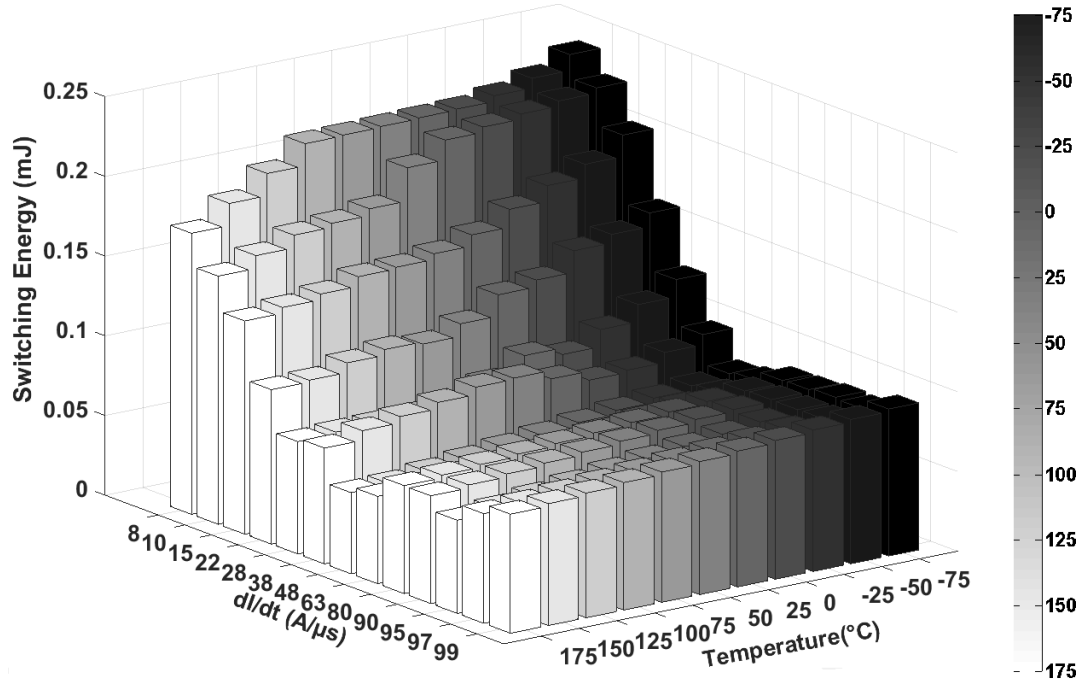


Figure 3.34: Switching energy of SiC SBD at turn-off.

Figure 3.35 shows the diode turn-off voltage transient as a function of temperature for $R_G = 15\ \Omega$ while Figure 3.36 shows the same plot for $R_G = 150\ \Omega$. It can be seen from Figures 3.35 and Figure 3.36 that the damping of the diode ringing during turn-off reduces with increasing temperature and the peak voltage overshoot increases with temperature, i.e. ringing becomes more sustained at high temperatures during diode turn-off. This is due to the positive temperature coefficient of the MOSFET dI_{DS}/dt at turn-on, hence faster switching at high temperatures contributes to the ringing. It can also be noticed in Figures 3.35 and 3.36 that the temperature dependence of ringing and its damping reduces at higher MOSFET dI_{DS}/dt (lower R_G) and increases as the dI_{DS}/dt is reduced, i.e. at high dI_{DS}/dt, the diode characteristics become more temperature invariant compared to low dI_{DS}/dt (higher R_G). It can be seen from Figure 3.36 that there is a significant variation of the V_{AK} transient as the temperature is changed.

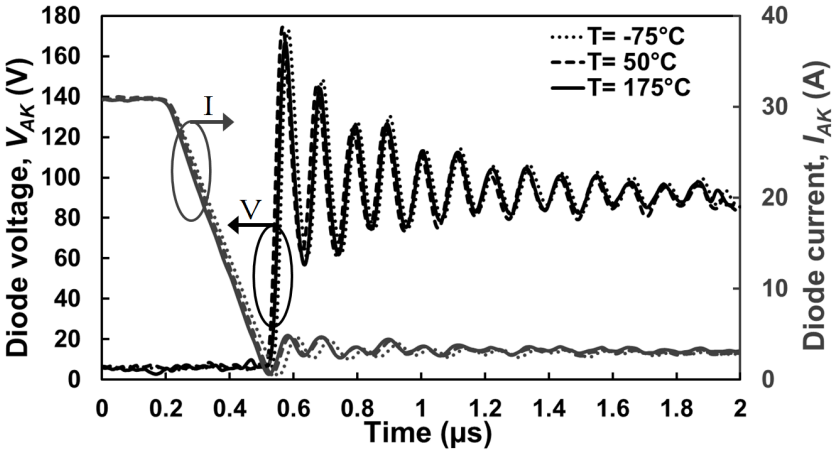


Figure 3.35: SiC SBD turn-off voltage and currents with R_G of 15 Ω.

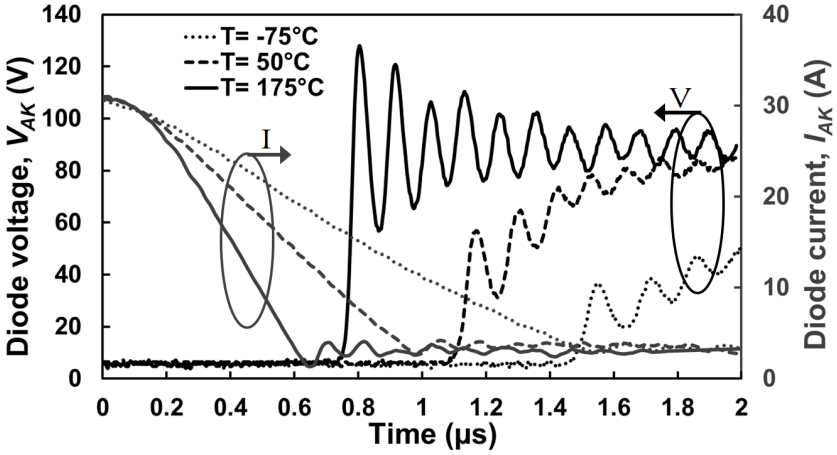


Figure 3.36: SiC SBD turn-off voltage and currents with R_G of 150 Ω.

This ringing in the SiC Schottky diodes is a major reliability concern in the application of unipolar SiC devices which switch with high rates, as the ringing will be transferred to the DC link voltage and can therefore unstable the entire circuit. This will be shown with more details in the following chapters and mitigation techniques will also be employed to remove this ringing from the DC link. Additionally the ringing causes significant thermal losses on the system, and hence requires to be accurately predicted. Analytical models in the next chapter will also be developed to provide this diagnostic tool.

Figure 3.37 shows the switching energy of the silicon PiN diode at different temperatures and IGBT dI_{CE}/dt. It can be seen from this figure that the switching energy increases as the temperature increases for a given gate resistance. This is due to the increased minority carrier lifetime with temperature thereby increasing the reverse recovery charge of the PiN diode during turn-off. Hence, the switching performance of the PiN diode deteriorates as the temperature increases.

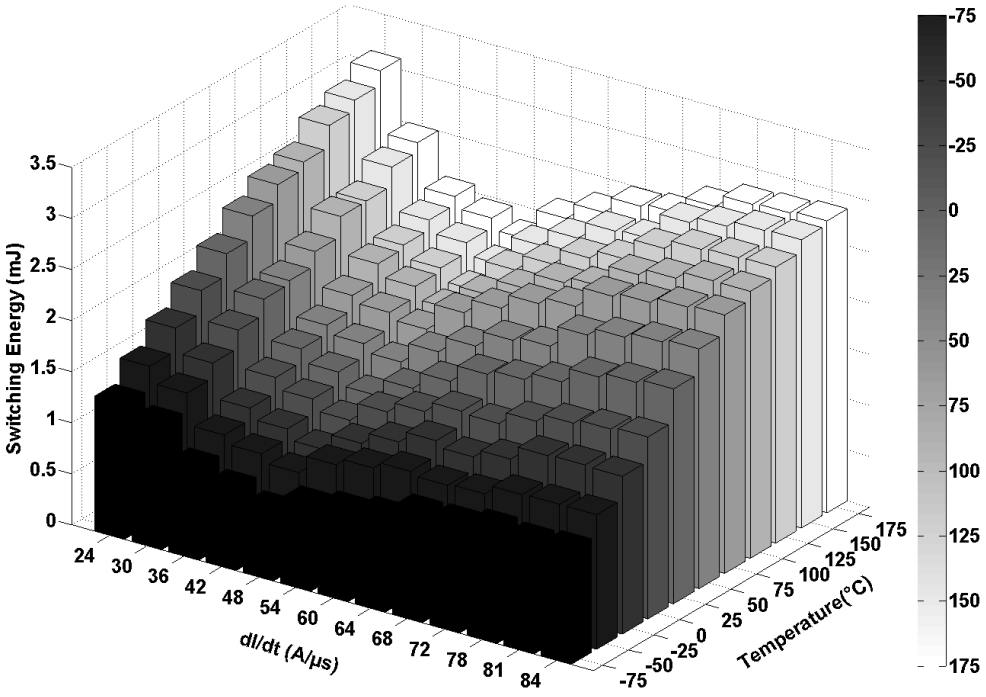


Figure 3.37: Switching energy of silicon PiN diode at turn-off.

Figure 3.38 and Figure 3.39 show the PiN diode voltage and current transients for $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$. It can be seen from these figures that the peak reverse recovery current and the transient duration increases as R_G is decreased (dI_{CE}/dt is increased). It can also be observed from Figure 3.38 and Figure 3.39 that the peak diode voltage overshoot increases with reducing R_G, hence fast switching using PiN diodes (similar to SiC SBDs) in presence of stray inductances may in fact increase the power losses.

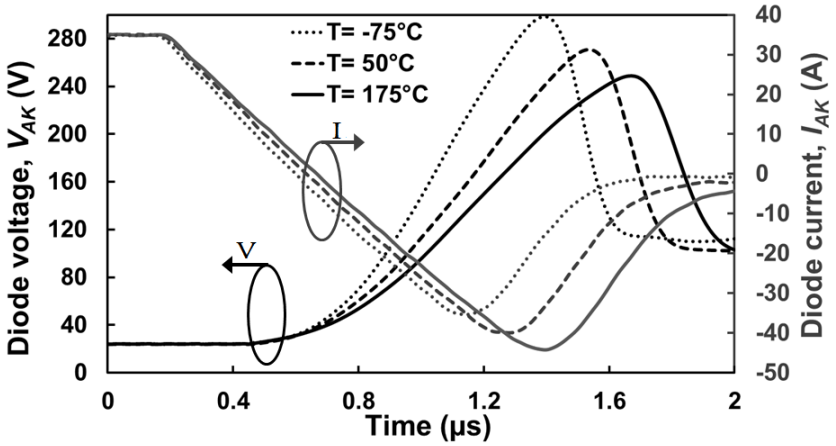


Figure 3.38: Silicon PiN diode turn-off voltages and currents with R_G of 15 Ω.

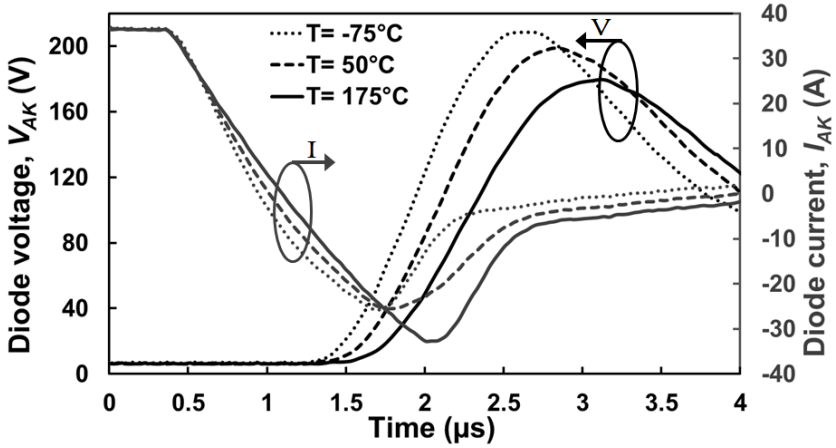


Figure 3.39: Silicon PiN diode turn-off voltages and currents with R_G of 150 Ω.

As the turn-on dI_{CE}/dt of the IGBT increases with decrease of temperature (refer to Figure 4.12), the peak voltage overshoot of PiN diode reduces with increasing temperature. The result of all this is that the switching energy as a function of R_G, especially in diodes, exhibits a U-shaped characteristics at all temperatures. At low R_G, the switching energy is dominated by high peak reverse recovery currents and large diode voltage overshoots while at higher R_G, the switching energy is dominated by the longer switching duration which results in a further increase in switching losses.

Figure 3.40 shows a comparison of the SiC MOSFET and Si-IGBT switching energies as a function of temperature with $R_G = 15\ \Omega$ for both turn-on and turn-off. The SiC MOSFET shows less switching energy compared with the Si-IGBT at high switching rates. The switching energy also shows less temperature dependency in the SiC MOSFET compared with the Si-IGBT. Figure 3.41 also shows that the switching energy of the SiC Schottky diode is significantly less than that of the silicon PiN diode.

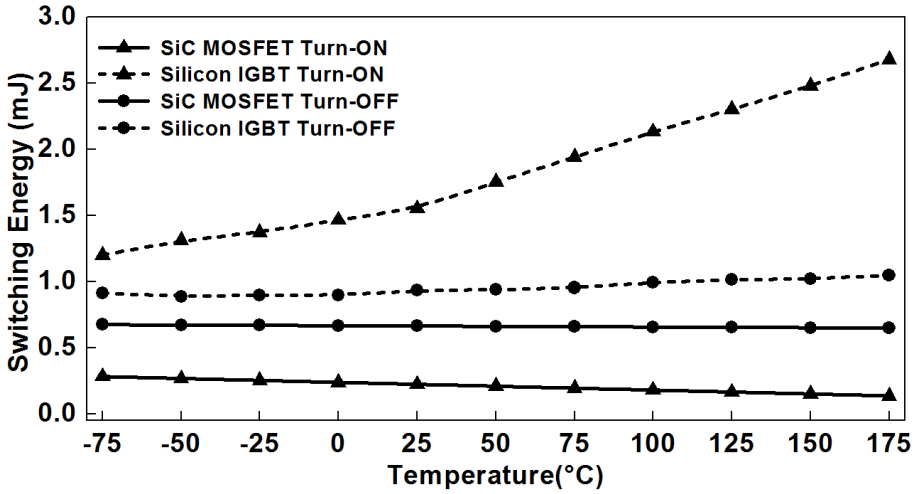


Figure 3.40: Transistors switching energy as function of temperature, $R_G = 15\ \Omega$.

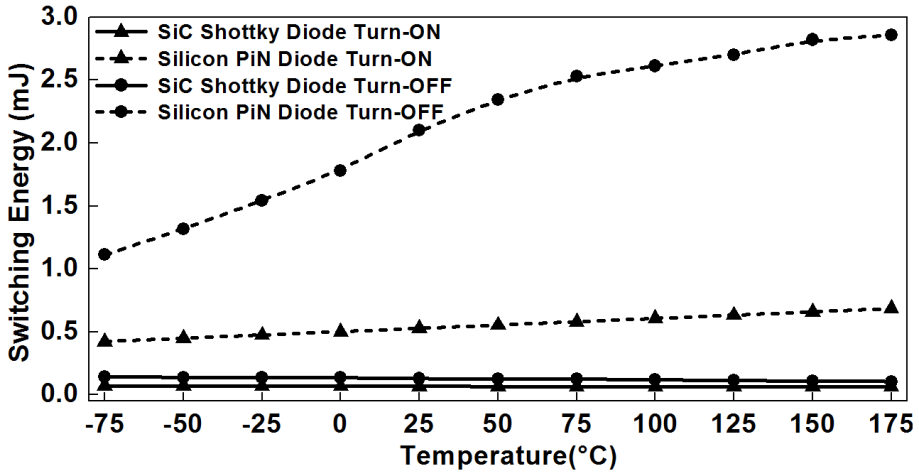


Figure 3.41: Rectifiers switching energy as function of temperature, $R_G = 15\ \Omega$.

3.4 Electric Vehicle Drive-Train Model

3.4.1 SiC in EVs and HEVs

To date, the voltage level of the commercial SiC devices, except the samples made in research laboratories, still has not reached beyond 1.7 kV. This is already beyond the requirements of low voltage applications and hence the silicon devices will still suit those areas. On the other hand, it is too low for applications where the power and voltages are at grid level. These, for example, include grid-connection of offshore wind farms through HVDC systems. Hence, a suitable application for this medium-voltage devices should be sought. A recent area in this level is the power converters in electric vehicles.

Electric vehicles require at least three main power converters with voltages at approximately 600-800 volts. The first one, is the on-board charging solution. This charger is required so as to facilitate the direct mains connection of the vehicle without the need of a dedicated charger station. This converter should convert the mains AC power to around 400 volts DC for storage in the battery. The second converter is a DC-DC converter to bring the voltage down to 12 volts for low voltage electronics. And the third one is the DC-AC inverter to provide the power for drive-train of the vehicle. So the level of voltages in an EV are ideal for the application of the 1.2 kV SiC devices. In this regard, the SiC devices explored here will be deployed in the latter type of EV converters (drive-train) and their performance will be examined in a case-study approach.

3.4.2 Implementation of Measurements in EV Model

As stated, to understand what does the previous measurements really mean, they have been used as inputs into a 3-level 3-phase NPC VSC model in PLECS where the drive-train

of the electric vehicle is modeled by connecting the converter output to a 3-phase 8 pole permanent magnet synchronous machine [30, 31]. The transistors and diodes switching energies as functions of the supply voltage, current and temperature were used to parameterize the switching devices. Other input parameters for the converter models were the switching frequency, the calculated turn-on/off time delay (dI/dt) with different pulse width modulation (PWM) techniques. Figure 3.42 shows a schematic of the model converter connected to the electrical motor [32]. The switching energy measurements at different temperatures were inserted into a look-up table in the device model and used to determine the performance of the electric drive-train in different conditions.

Hence, depending on the switching frequency and the dI/dt of the devices used in the converter, the corresponding switching energy is used to perform the simulation. The rate of change of current with time (dI_{DS}/dt or dI_{CE}/dt) is specific to the device technology (SiC MOSFET or Si-IGBT). For each switching instance, the device is conducting (with the conduction losses incorporated according to datasheets values) for at least 10 times the sum of the turn on/off periods or longer if dictated by the PWM drive. Figure 3.43 shows the output line-to-line voltage waveform of the NPC VSC prior filtering.

Different modulation techniques were used in model including the Sinusoidal PWM (SPWM) [33], sawtooth PWM [34], Carrier-Based Space Vector PWM (CB-SVPWM) [35, 36], Third Harmonic Injection PWM with a coefficient of 25% of carrier (THIPWM(4)) [37], Third Harmonic Injection PWM with a coefficient of 16% of carrier (THIPWM(6)) [38] and Triple Harmonic Injection PWM (TRIPWM) [39]. Many of these PWM techniques are conventionally used in the electric vehicle's converters [40]. Examples may be SPWM, SVPWM and THIPWM. The thermal resistance and thermal capacitance of the heat sink in the model was selected on the basis of published thermal parameters for sample commercial heat-sinks and are used as inputs into the converter's thermal model. The

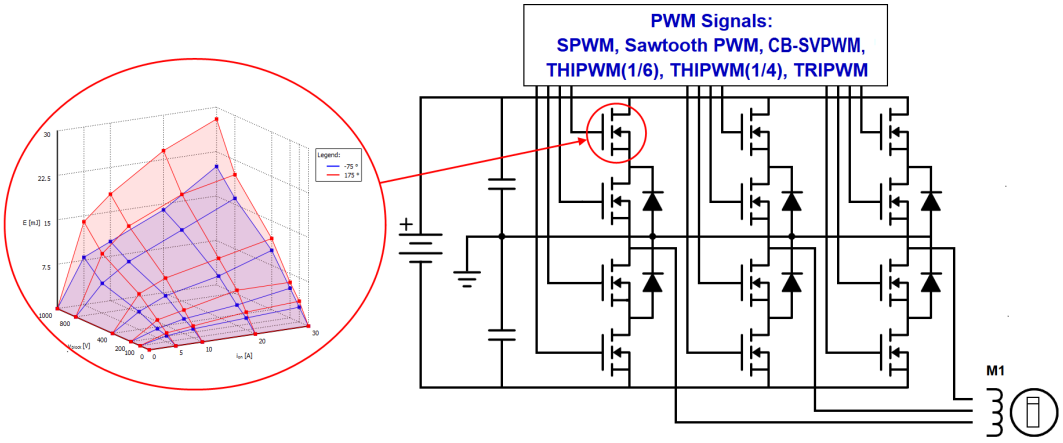


Figure 3.42: The 3-level NPC VSC with 600 V and 30 A; the heatsink is connected to all devices with Table 3.1 parameters. For further details please refer to Figure B.1.

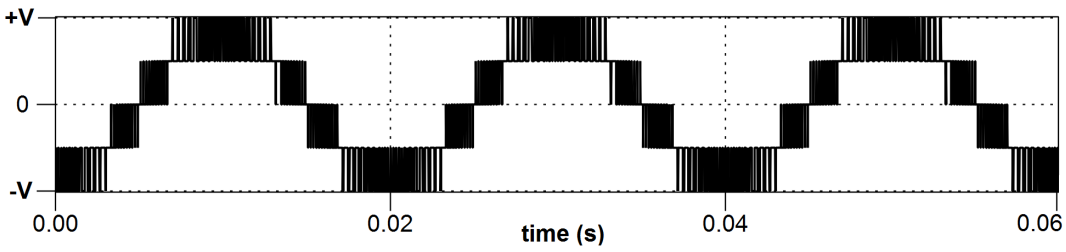


Figure 3.43: The line-to-line voltage of the 3-Level NPC VSC model before filtering.

thermal impedances of the devices were also obtained from the datasheets and used as inputs into the thermal elements of each device as a cauer type thermal network.

Figure 3.44 shows the steady state temperature rise of the converter for different PWM techniques with the carrier frequency of 5 kHz and the gate resistance at 15 Ω. The SiC MOSFET and Si-IGBT were distinguished in the model by different turn-on/off delays that were experimentally measured, i.e. longer delays represent a lower switching rate. It should be noted that the power devices used in EVs are typically not discrete, but bare dies soldered onto DBC substrates. The heatsink is also water cooled, not natural convection. Hence, the temperature excursions due to the losses are rapidly and effectively removed by heat conduction through the substrates with the water flow-rate in the cooling

system used to regulate the ambient temperature of the devices. Although these simulations do not capture that, they can however be used as an indicator for the temperature excursions (ΔT). The ΔTs generated from the switching transients will impose thermo-mechanical stresses between the wire-bonds and the dies as well as between the dies, the solder and the substrate. These thermo-mechanical stresses arise from Coefficient-of-Thermal-Expansion (CTE) mismatch between the different materials that make up the DBC system and will hence, degrade the thermal impedance of the converter by degrading the mechanical integrity of the system. For example, wire-bond lift-off [41] is a well known failure mode in power devices that undergo thermal cycling in power conversion applications like EV drive-trains. As the devices operate with higher thermal resistances due to power cycling induced thermo-mechanical degradation, the junction temperatures rises in spite of the applied cooling system. Hence, the simulations provided here can act as a first approximation of system reliability using the ΔT generated by the respective devices as an indication for operation of different semiconductor technologies.

The smaller switching energy of the SiC MOSFET is translated into a smaller temperature rise compared with the Si-IGBT as can be seen in Figure 3.44. It should be noted that the level of the temperature rise depends directly on the number of devices connected to the heat sink and the power dissipation of each of the devices and also the size of the attached heat sink. Hence, here a smaller heat sink will result in a higher temperature rise, and therefore making the comparison between the two cases easier.

The conversion efficiency calculated here is simply the effect of losses on the reduction of the output energy compared to the input. Hence, the switching energy of devices in each cycle compared to the input power shows how much energy is lost due to switching transients and conduction losses due to the on-state resistance. The results are shown in Figure 3.45 where the conversion efficiency is calculated for the different PWM techniques

for both technologies. It clearly shows that the SiC devices outperform the silicon devices in terms of conversion efficiency by $\approx 3\%$ as a result of smaller switching energies.

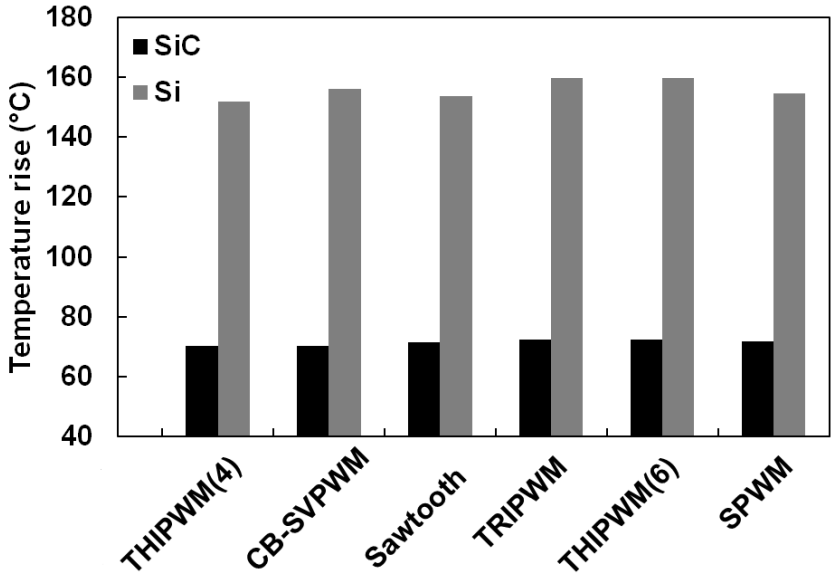


Figure 3.44: Modelled temperature rise of the VSC with different PWM techniques, R_G of 15 Ω and 5 kHz carrier frequency.

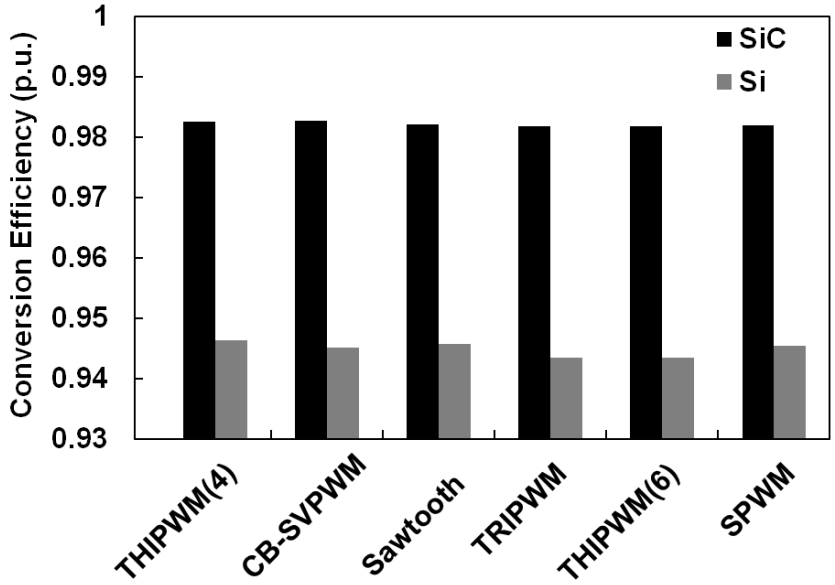


Figure 3.45: Modelled conversion efficiency of the 3-Level NPC VSC with different PWM techniques, R_G of 15 Ω and 5 kHz carrier frequency.

The impact of changing the R_G and switching frequency on the temperature rise is also modeled for both technologies. Faster switching is usually desirable as it can reduce the filtering requirements. Figure 3.46 shows the converter temperature and motor speed (in rpm) of the drive-train as a function of time modeled with SiC MOSFET and Si-IGBT switching parameters. The reference frequency in the PWM modulation is kept constant at 60 Hz (this varies in EVs by the control circuit) while the modulation frequency is ranged between 5 kHz and 15 kHz. The final motor speed attained is constant 900 rpm. Figure 3.46 shows that increasing the PWM switching frequency from 5 kHz to 15 kHz increases the operating temperature of the converter by 72% for the one with Si-IGBTs and 50% for the one with SiC MOSFETs. However, at 15 kHz and 5 kHz, the steady state operating temperature of the modeled SiC converter is 53% and 50% lower than that of the modelled Si-IGBT converter, respectively. This reduction can lead to simpler cooling systems, more efficient and compact electric vehicle drive-trains as well as better device robustness since reliability is usually strongly affected by temperature.

Figure 3.47 shows the model's results of converter with SiC MOSFET and Si-IGBT with 2 different gate resistances connected (R_G = 15 Ω and R_G = 150 Ω). The gate resistances used will govern the maximum possible switching frequency and will also determine the electromagnetic oscillations in the output characteristics of the devices. Figure 3.47 shows that the converter modeled with SiC MOSFETs exhibits a smaller temperature rise as a result of the smaller switching energy. What can also be observed in Figure 3.47 is the fact that increasing the gate resistance for slower switching increases the temperature rise as a result of the increased switching energy. It is sometimes desirable to slightly increase the gate resistance so as to reduce the electromagnetic stress imposed on the device, i.e. fast switching can cause oscillations in output characteristics [42]. It is also known that increasing the switching frequency will simplify removal of harmonics

by using smaller filters. However, this will come at the expense of increased switching losses and higher operating temperature as shown in Figure 3.46. The use of SiC can nevertheless relax this trade-off since the temperature rise associated with faster switching is less for SiC unipolar compared with silicon bipolar technologies. This is advantageous in applications where weight or size of passive elements is critical like off-shore wind turbines [43], marine or aviation [44].

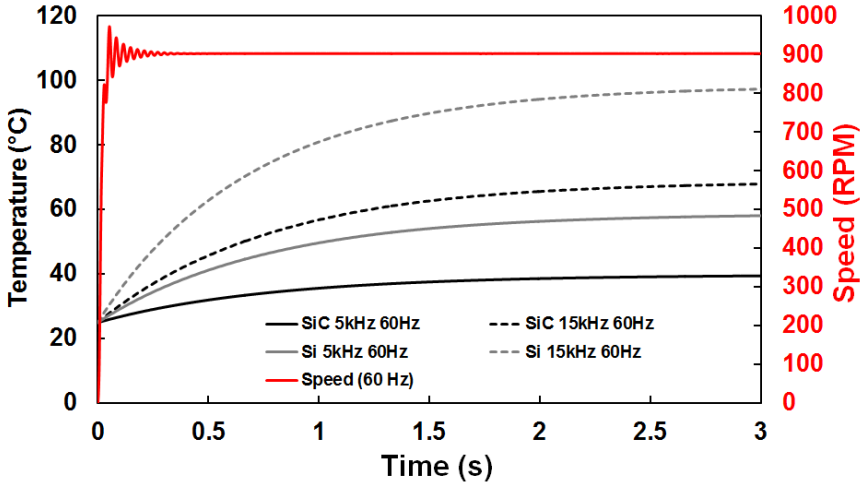


Figure 3.46: Effect of frequency on temperature rise of Si/SiC VSC ($R_G = 15\ \Omega$).

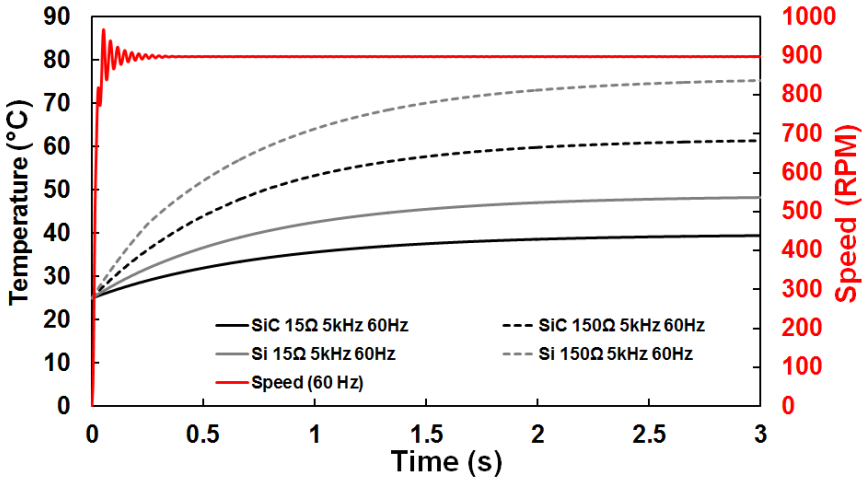


Figure 3.47: Effect of R_G on temperature rise of Si/SiC VSC ($f = 5$ kHz).

3.5 Summary

This chapter explored the impact of SiC devices as a wide bandgap semiconductor technology on energy conversion through a model of an EV drive-train converter with implementation of experimental measurements of power devices. The temperature dependency of switching energy in SiC MOSFETs/Schottky diode pairs have been compared to that of silicon IGBT/PiN diode pairs. This was experimentally measured for 1.2 kV devices for a temperature range of –75 °C and 175 °C using a range of R_G to vary switching rates.

The switching rates were shown to be temperature dependent with SiC MOSFET's switching rate showing a positive temperature coefficient at turn-on and a negative temperature coefficient at turn-off. The IGBT switching rates decreased with temperature for both turn-on and turn-off. Hence, the switching energy of the SiC MOSFET has been shown to decrease with temperature in turn-on whereas that of the Si-IGBT increases. The switching energy of diodes was U-shaped as a function of R_G. At small R_G, the switching energy of the PiN diode is dominated by the peak reverse recovery charge and voltage overshoots. In SiC diodes, the switching energy is dominated by diode ringing.

The EV drive-train model as a 3-level 3-phase NPC VSC showed significant improvements when it was parameterized with SiC unipolar devices measurements compared with silicon bipolar ones. The model with SiC parameters exhibited less operating temperatures at the same switching frequency thus implying a reduction of cooling requirements. Also, the VSC model with SiC MOSFETs exhibited smaller steady state temperature excursions while running at twice the switching frequency compared with silicon IGBT thereby signifying that energy density can be increased considerably with SiC. This technology can therefore improve the VSCs in terms of cooling requirements and energy density all of which contribute significantly to the efficiency and performance of EVs.

Chapter

4 Analytical Modeling for Switching Performance of Power Diodes

As was seen in chapter 3, the switching energy of power devices is a major factor in determining the conversion efficiency of power converters. Therefore, it is important to understand the parameters that can potentially impact it and to be able to predict these. The switching energy is generated in both the transistors and the diodes. In the former case, the switching occurs directly by activating the gate of the device, while in the latter case, it occurs indirectly through commutation of current/voltage. The characteristics of the transients and switching energy in MOSFETs and IGBTs have already been discussed extensively [5]. However, power diodes (mainly silicon PiN and SiC Schottky) also play an important role in the performance of converters and therefore require analytical review. Detailed analytical modeling of their transient waveforms as functions of the current/voltage commutation rates, parasitic elements and temperature will thus contribute significantly towards evaluating the performance of power converters.

As seen in chapter 3, the switching energy of both types of diodes are higher during the turn-off transient, hence have a higher contribution to the total thermal losses. As a result, in this chapter, analytical models for the turn-off transient switching energy

of silicon PiN and SiC Schottky diodes will be proposed and validated by comparing to experimental results obtained. These diodes have different charge carrier mechanisms and therefore, exhibit different characteristics and should be analyzed accordingly.

Although SiC Schottky diodes have increasingly become popular as a replacement for silicon PiN diodes, as far as power conversion at high power levels and medium frequencies are concerned, silicon PiN diodes remain unrivalled in delivering low on-state energy dissipation. However, PiN diodes are known to contribute significantly to switching energy as a result of the reverse recovery charge during the turn-off transient. At high switching rates, the overlap between the high peak reverse recovery current and the high peak voltage overshoot contributes significantly to switching energy. The peak of this reverse recovery current depends on temperature and switching rate whereas the peak diode voltage overshoot depends additionally on the significance of circuit stray inductance.

On the other hand, SiC Schottky barrier diodes do not exhibit reverse recovery but are prone to electromagnetic oscillations and are known to ring in the output terminal when used as free-wheeling diodes in voltage-sourced converters. This ringing is due to RLC resonance between the diode capacitance, stray inductance and parasitic resistance of both the switching circuit and device. The oscillation frequency, peak voltage overshoot and damping are shown to depend on the ambient temperature and the MOSFET switching rate (dI_{DS}/dt). In this chapter, it will be shown experimentally and theoretically that dI_{DS}/dt increases with temperature for a given gate resistance in MOSFET turn-on and reduces with increasing temperature during turn-off. As a result, the oscillation attenuation and peak voltage overshoot of the SiC SBD increases with temperature during diode turn-off (coinciding with MOSFET turn-on). This temperature dependency of the diode ringing reduces at higher dI_{DS}/dt and increases at lower dI_{DS}/dt. It is also shown that the rate of change of dI_{DS}/dt with temperature ($d^2I_{DS}/dtdT$) is strongly dependent on

R_G and by using fundamental device physics equations, this behavior is predictable. As expected, the damping of the oscillations increases by decreasing the switching dI_{DS}/dt.

The analytical model developed for the switching energy of the SiC SBD shows:

- The total switching energy can be sub-divided into 3 components namely the current switching phase, the voltage switching phase and the ringing phase.
- Although the switching energy in the current switching phase decreases with increasing dI_{DS}/dt, the switching energy of the voltage and ringing phase increase.
- As a result of these different components, the losses at low switching rates are dominated by the switching transient duration and losses at high switching rates are dominated by the overshoots. This in turn determines the switching energy of the diode which initially decreases with decreasing dI_{DS}/dt to a certain point and then subsequently increases with further decrease of dI_{DS}/dt.
- This U-shaped characteristic of the switching energy with respect to dI_{DS}/dt indicates an optimal dI_{DS}/dt for minimum switching energy.

In this chapter, the aforementioned are studied in two different parts. Part one focuses on the performance of PiN power diodes, where an analytical model for calculating the switching energy at different switching rates and temperatures is presented. The models are validated by ultra-fast and standard recovery diodes with different current ratings. The characteristics of the main rectifiers modeled in this chapter are provided in Table 4.1. As will be seen, the model is able to correctly predict the switching rate and temperature dependence of the PiN diode switching energy. In the second part of this chapter, SiC Schottky Barrier Diodes (SBDs) are also modeled in terms of dynamics of switching and performance, by using fundamentals of semiconductor devices and analytical methods.

Similar to PiN diodes, a model has also been developed for calculating the switching energy of SiC Schottky diodes as a function of the switching rate (dI_{DS}/dt of the commutating SiC MOSFET) and temperature, hence can be used to predict the behavior of SiC SBDs. The results obtained are important for predicting EMI, reliability and temperature rise.

Table 4.1: Comparison of determining parameters of the main Si-PiN and SiC-Schottky power diodes used in modelings validation.

Parameter	Unit	Si-PiN	SiC-Schottky
Voltage	V	1200	1200
Forward Current	A	45	40
Forward Voltage	V	1.26	1.8
Junction Capacitance	pF	18	150
Thermal Resistance Junction-Case	°C/W	0.55	0.48

4.1 Carriers Plasma in PiN Rectifier

As stated in chapter 2, a PiN diode is comprised of a lowly doped voltage blocking drift layer sandwiched between a heavily N-doped cathode and a heavily P-doped anode. The principle of charge neutrality ensures that the depletion width falls entirely in the drift region in the off-state which also supports conductivity modulation in the on-state. Switching the PiN diode between on-state and off-state will involve the filling and clearance of the drift layer with/from minority carriers. The impact of temperature and minority carriers lifetime on this are covered in the next section.

4.1.1 Plasma State in PiN Diodes at Turn-on

When the PiN power diodes start the turn-on procedure, initially no conductivity modulation is formed in the device. Hence the resistance of the device, seen by the initial

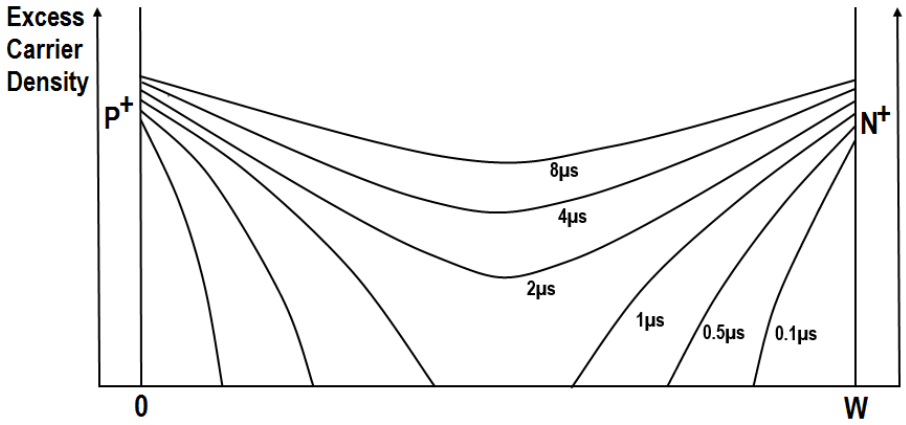


Figure 4.1: Typical plasma formation for the conductivity modulation in the drift region of a power PiN diode (Impact of carriers mobility difference not considered) [6].

in-rush current is far higher than the on-resistance during conduction at the rated current levels. This is because the actual resistance of the device is calculated according to its geometry and the absence of mobile carriers means that the off-state resistance is high. Hence, as the device turns-on for the conductivity modulation to form, there is a considerably higher forward voltage drop present as a result of this high resistance. This peak in forward voltage drop has become more important recently as it is more substantial in value in newer devices with higher voltage ratings as the geometry of drift region (and its resistance) becomes even wider to accommodate the extended depletion widths.

Figure 4.1 shows a typical time delay for the formation of conductivity modulation, where carrier concentration levels are at a few orders of magnitude higher than the actual doping of drift region. This corresponds to the time that the forward voltage drop is higher. Fortunately in most cases, this peak is not substantial; although in devices with very high voltage ratings, it can cause some reliability problems by reverse biasing the top side transistor. Figure 4.2 shows the approximate current and voltage transient waveforms, which shows how the peak forward voltage drop is generated and then collapses [6].

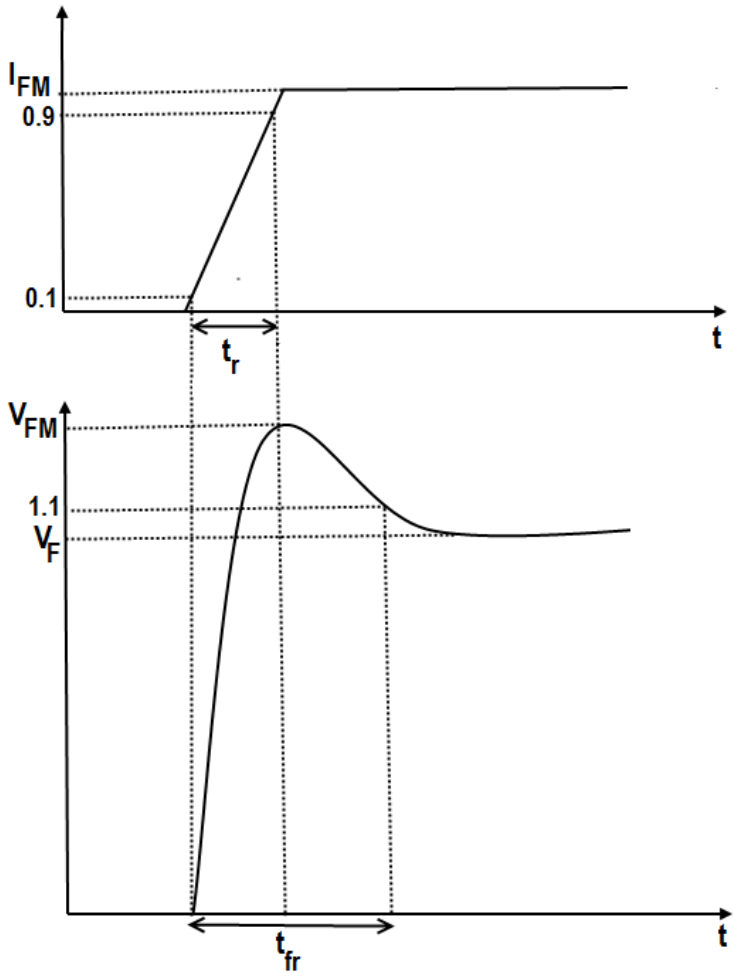


Figure 4.2: Linearized waveforms for typical turn-on procedure of PiN diode [6].

The voltage peak happens when the forward current has reached to $\approx 90\%$, as after this point excess carriers in drift region are sufficient to reduce the on-state resistance.

4.1.2 Plasma State in PiN Diodes at Turn-off

At turn-off, the reverse procedure of plasma formation takes place. In this case, the excess carriers in the drift region should be removed. However, since the diode is conducting current supplied to an inductive load, the current does not instantaneously falls to zero.

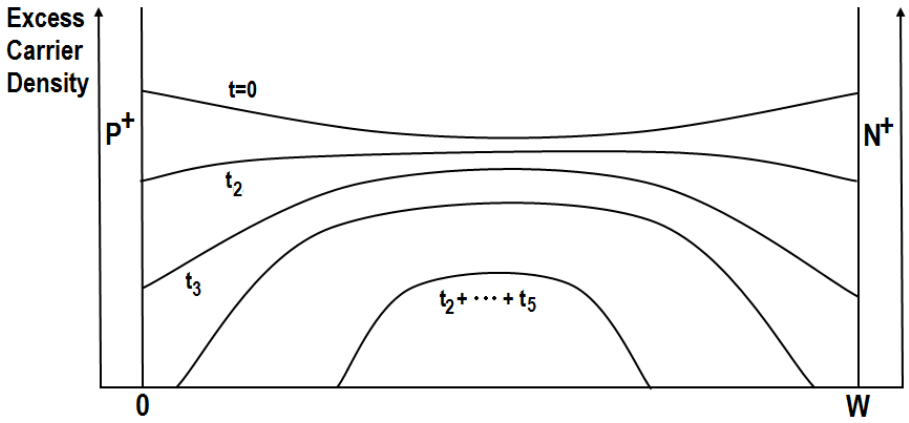


Figure 4.3: Typical plasma removal from the drift region of a power PiN diode at turn-off (Impact of carriers mobility difference not considered) [6].

Depending on the inductor size, the current falls with a constant rate. The time instant that the voltage crosses the zero mark coincides with/or is shortly before the peak reverse recovery current. It is the voltage zero-crossing that cuts off the supply of carriers into the drift region, thereby initiating the reverse recovery until it reaches its peak.

At this point, charge removal goes into the recombination phase. The charge profile within the diode becomes unable to support the current as a result of the extending depletion regions formed by the reverse bias voltage; hence the current starts returning to zero. As a result, the slope of the current changes polarity and the diode goes into recovery until the value of the current reaches zero. The tail current of the reverse recovery profile will depend on the minority carrier lifetime. Figure 4.3 is showing a typical time frame for removal of the carriers in the drift region corresponding to Figure 4.4 where the waveform of a typical reverse recovery turn-off is shown. As seen, t_2 is when injection of carriers is stopped, while t_3 is when the depletion regions begin to form. Additionally t_5 is showing a significant portion of the recovery current where the carriers are recombining and is between the peak voltage overshoot and the peak reverse recovery current of device. These time marks are used later in the model developments in section 4.2.2.

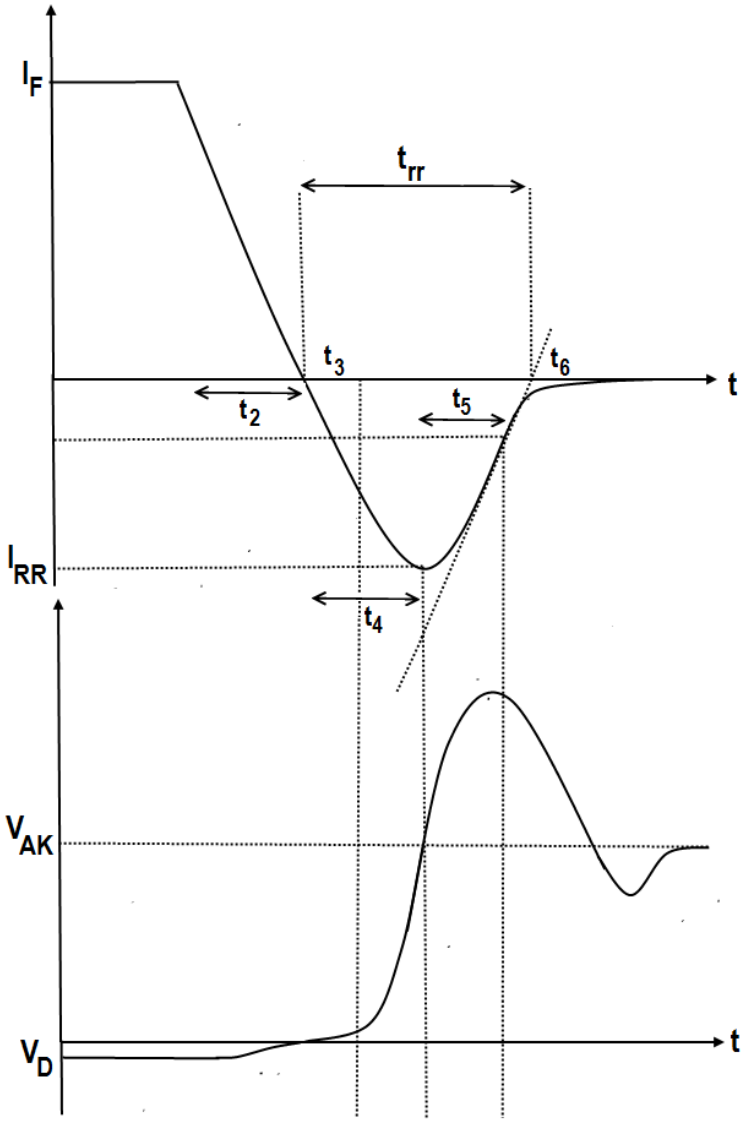


Figure 4.4: Linearized waveforms for a typical turn-off procedure of a PiN diode [6].

4.1.3 Parameters Impacting the Recovery Switching Energy

The PiN diode voltage overshoot arising from the stray inductance also significantly contributes to the switching energy. Both the peak reverse recovery current and voltage overshoot increase with dI/dt which is controlled by the RC time constant of the IGBT

and temperature. The diode parasitic capacitance and circuit stray inductance will also determine the rate that the diode ramps down the current. Therefore, when developing a model, all these details must be included in the considerations.

4.1.4 Different Models for PiN Charge Transients

Models developed for the PiN diode's reverse recovery transients fall mainly into two categories; physics-based SPICE models (which require device physics parameters) and analytical models that are based on waveform characterizations. The physics of PiN diodes is described in [45, 46] whereas some of the SPICE models are provided in [47, 48]. SPICE models are accurate in modelling the PiN diodes, although prior knowledge of all device parameters is required which may be hindered by the fact that some of them are not available on the manufacturers' datasheet. Hence, although SPICE models are useful in understanding the PiN diodes' transient performance [49] and reliability [50], waveform based approaches can also be a fast and reliable method of predicting the switching performance of PiN diodes under different conditions given a few initial measurements [51]. Hence, this chapter focuses on deriving these analytical models. Implementing such analytical models will require dI/dt, dV/dt and their temperature dependencies as input parameters which may mean that some experimental characterization is required at the outset if not known. However, once known, the model is capable of predicting the switching energy accurately for different conditions without using detailed device parameters.

4.2 Analytical Model Development

An accurate analytical model should be able to correctly predict the switching of devices according to experimental measurements. Hence, in this section, the conventional

basic models are first studied, then the model is developed. Afterward, the PiN diode measurements are analyzed and finally the results of the model are validated.

4.2.1 PiN Diode Transients

Figure 4.5 shows a typical turn-off switching transient of a 1.2 kV/40 A silicon PiN diode switched at 2 different rates. It can be seen that the reverse recovery current and the diode voltage overshoot will contribute significantly to the switching energy. In the on-state, the voltage across the diode is determined by the carrier distribution profile within the drift region and the voltage drop across the P^+-N^- and N^--N^+ junctions. As explained earlier, as the diode is turned-off, the excess charge is reduced by extraction and recombination. During the reverse recovery phase, the lifetime of the minority carriers in the drift region of the diode determines the duration of the switching transient. For the purpose of this analysis, the switching energy (E_{SW}) is defined by:

$$E_{SW} = \int_0^t V_{AK}(t) i_D(t) dt \tag{4.1}$$

where t is the total duration of the switching transient. Here, 0 is the time instant at which the current starts ramping down whereas t is defined as the time instant when the reverse recovery current returns to zero (this is shown clearer in the model development section). It should be noted that this model only studies the turn-off transient; therefore, due to the possible stored energy in the PiN diode, the supplied power cannot be considered to be exactly equal to the dissipated heat, hence result in a negligible contribution to the model error. When modelling the switching energy of a PiN diode, it has previously been assumed that dI/dt is always uniform before and after the zero-crossing of the reverse current and the dI/dt is constant throughout the recombination phase.

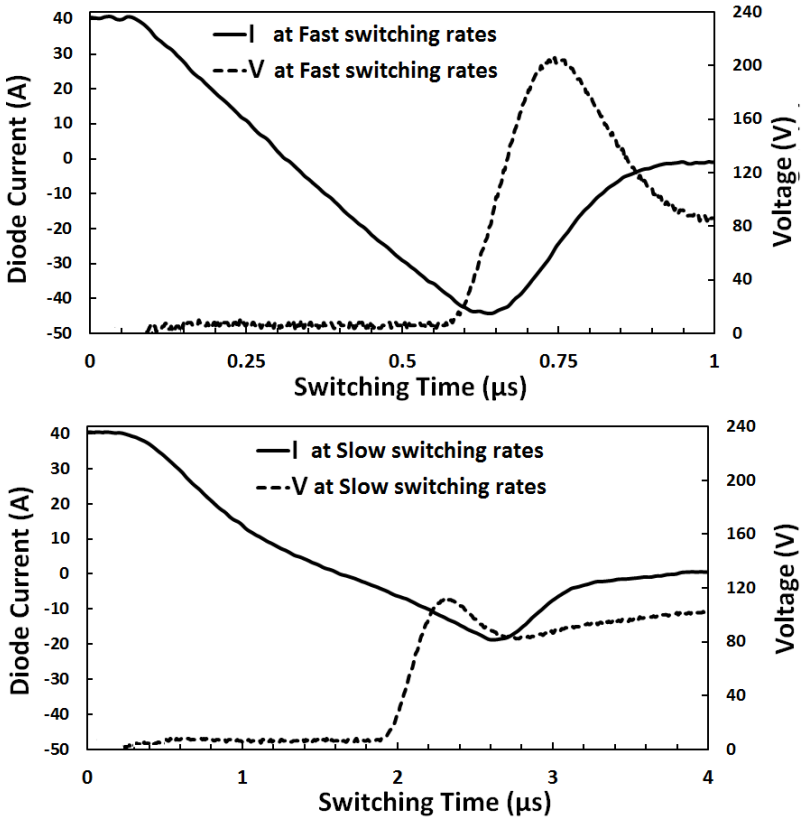


Figure 4.5: Typical turn-off transients of PiN diode in different switching rates.

However, the experimental measurements in chapter 3 showed that when the IGBT is switched at lower rates, the slope of the current is no more constant. Figure 4.5 shows the measured diode current for the same PiN diode with two different switching rates. It can be seen from Figure 4.5 that the turn-off current at a slow switching rate has 2 distinctive slopes, approximately separated by the zero-crossing of the current whereas that at a high switching rate has a singular slope. Also the voltage across the diode is assumed to be equal to the supply voltage since the devices on-state voltage drop is insignificant.

It has also previously been assumed that the voltage and current waveforms can be considered linear and the energy can be calculated from the area of the overlapping current/voltage [52]. Hence, the switching energy (E_{SW}) is simply the area of the triangle

formed by the linear over-lapping transients. This switching energy has sometimes been expressed in terms of the capacitance charge ($0.5Q_cV$) or IV ($0.5IVt$). Applying this method to the calculation of the turn-off switching energy of PiN diode normally results in a considerable margin of error. This is shown in Figure 4.6. This method yields the following expressions for the peak reverse current (I_{RR}) [53].

$$I_{RR} = \sqrt{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}\frac{2k_Q\sqrt{I_F}}{1+S}} \quad \text{and} \quad V_{AK} = V + L\frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \tag{4.2}$$

which results in:

$$E_{SW} = \frac{1}{2}V_{AK}I_{RR}t_{SW} \tag{4.3a}$$

$$= \frac{1}{2}\sqrt{\frac{2k_Q\sqrt{I_F}}{1+S}}\sqrt{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}}\left(V + L\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}\right)\left(\frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}}\right) \tag{4.3b}$$

Equation 4.2 expresses the peak reverse recovery current (I_{RR}) as a function of the turn-off switching rate (dI_{TF}/dt), the derivation of which is in [54]. In Equation 4.2, S is a measure of snappiness of the diode's recovery as the ratio of the time between the zero crossing of the current and the peak reverse current to the time between the peak of the current and zero. Also k_Q is a function that defines the relationship between the stored charge and the forward current (I_F) [53]. It also accounts for the diode voltage (V_{AK}) plus the peak inductive voltage overshoot (LdI_{RR}/dt) resulting from the product of the switching rate and parasitic inductance. Equation 4.3a is diode's switching energy (E_{SW}) expressed as a product of the peak reverse current, peak diode voltage and switching time. The total switching time is expressed as the sum of the time required for the current to fall from I_F to the peak reverse current, i.e. (I_F+I_{RR})/(dI_{TF}/dt) and the time taken for the

current to go from the peak reverse current back to zero, i.e. $I_{RR}/(dI_{RR}/\mathrm{dt})$. Figure 4.6 shows the result of this plain method in comparison with an actual measurement taken from a PiN diode switched with $R_G = 22\ \Omega$ connected on the low side transistor.

As seen in Figure 4.6, there is a significant error as a result of the simplistic triangular approximation of the switching power. This results in an over-estimation of the switching energy. Therefore to have a more accurate analytical calculation of PiN diode's switching energy during reverse recovery, a less simplistic linearized waveform model is used.

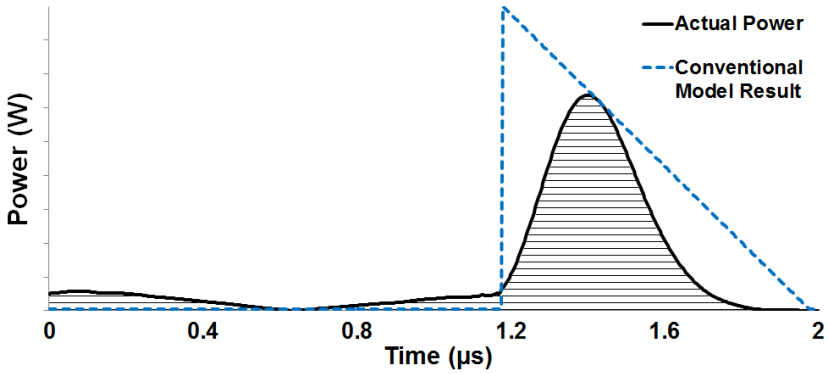


Figure 4.6: Conventional methods of transient energy calculations showing inconsistency with actual power output of P-i-N diode.

4.2.2 Development of Switching Energy Model

As explained in section 4.2.1, the slopes of the waveform might be variable throughout the whole transient. Considering the switching rates as constant values will simplify the model, although at the cost of increased margins of error. Hence, two versions of the models are developed here to provide a solution for both cases. Figure 4.7 shows the simplified model with linearized current and voltages switching waveforms including the reverse recovery and voltage overshoot at high switching rates. The instantaneous power is calculated by simply multiplying the transients as shown in Figure 4.5 and the switching

energy is calculated by integrating the switching power over time. The current and voltage transients shown in Figure 4.7 have been divided into a few different areas, where each section is characterized by a change in one of the switching waveforms.

Between t_1 and t_2, the current through the diode is ramping down at a defined and constant rate that depends on the gate resistance and input capacitance of the low side switching transistor. During this phase, diode voltage remains constant at the on-state value which depends on the diode's on-resistance. At time t_2, the diode current reaches zero and becomes negative while the diode voltage still remains constant at its on-state value. Between time t_2 and t_3, the diode current continues on its negative ramp with a fixed slope. At time t_3, the diode voltage starts to increase as the electric field forms at the junctions. As the depletion regions form at the junctions of the PiN diode, the device becomes incapable of supporting the current, so the negative current reaches its peak (marked by time t_4) and the remaining minority carriers in the drift region start recombining. Between time t_4 and t_5, the diode recombination current sustains its positive ramp back to zero while the diode voltage reaches its peak value which depends on the supply voltage and the peak inductive overshoot. At time t_5, the diode voltage reaches its nominal value set by the supply and at time t_6, the diode current reaches zero.

The switching power plot shown in Figure 4.7 is divided into distinct areas corresponding to the different switching phases. The total switching energy is the sum of all switching energies as in Equation 4.5 while Equations 4.6 and 4.7 show the derived switching energies E_{SW1} and E_{SW2} which correspond to the current switching phase where the diode voltage is still in on-state. The calculated switching energy corresponding to other sections of the switching transient can be determined by Equation 4.8 where the limits of the integration will depend on the section being integrated. The limits of the integration are shown next for t_1 to t_6. The coefficients of each integration are also provided.

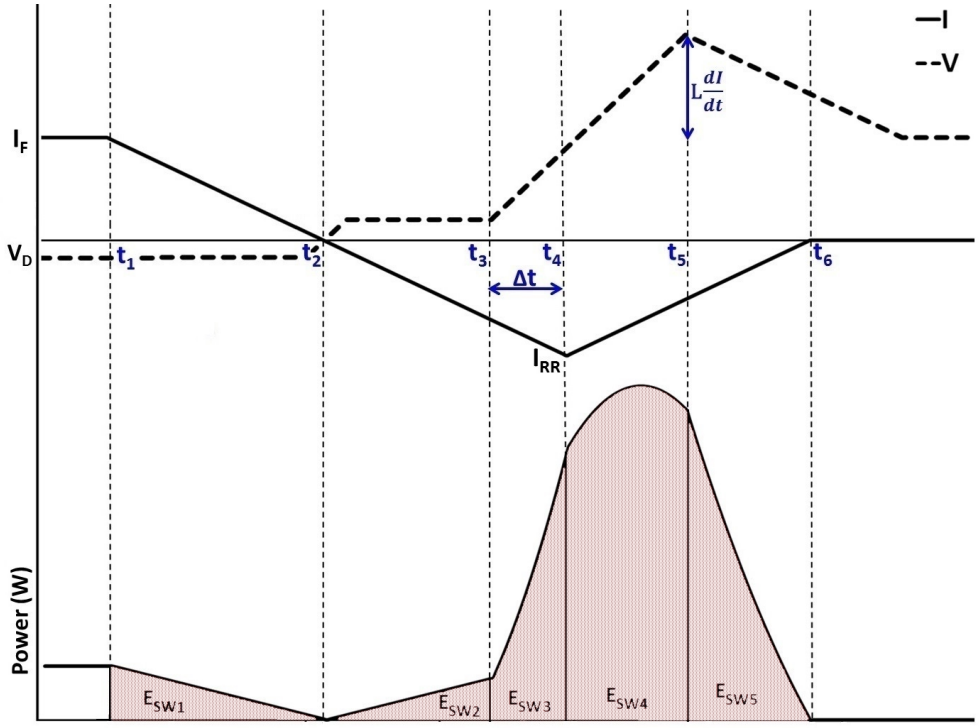


Figure 4.7: Power areas of the simplified model.

The result of this approach can be calculated using the equations as follows:

$$E_{SW} = \int_{t_1}^{t_6} V_{AK}(t) i_D(t) dt \tag{4.4}$$

$$E_{SW} = E_{SW_1} + E_{SW_2} + \sum_{n=3}^{5} E_{SW_n} \tag{4.5}$$

$$E_{SW_1} = \frac{I_F^2 V_D}{2\left(\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}\right)} \tag{4.6}$$

$$E_{SW_2} = \frac{V_D}{2} \cdot \left(I_{RR} - \Delta t \frac{\mathrm{d}I_{RR}}{\mathrm{d}t}\right) \cdot \left(\frac{I_{RR}}{\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}} - \Delta t\right) \tag{4.7}$$

$$E_{SW_n} = \frac{a_n b_n}{3}\left(t_{n+1}^3 - t_n^3\right) + \frac{a_n d_n + b_n c_n}{2}\left(t_{n+1}^2 - t_n^2\right) + b_n d_n \left(t_{n+1} - t_n\right) \tag{4.8}$$

The switching time intervals defined in Figure 4.7 can be calculated as:

$$t_1 = 0 \quad \text{and} \quad t_2 = \frac{I_F}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} \tag{4.9a}$$

$$t_3 = \frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} - \Delta t \quad \text{and} \quad t_4 = \frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} \tag{4.9b}$$

$$t_5 = \frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} - \Delta t + \frac{V + \left(L\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}\right) - V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} \quad \text{and} \quad t_6 = \frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}} \tag{4.9c}$$

and the equation coefficients of Figure 4.7 can be calculated as:

$$a_3 = -\frac{\mathrm{d}I_{TF}}{\mathrm{d}t} \;\;,\;\; b_3 = I_F \;\;,\;\; c_3 = \frac{\mathrm{d}V}{\mathrm{d}t} \;\;,\;\; d_3 = V_D - \frac{\mathrm{d}V}{\mathrm{d}t} \cdot \left(\frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} - \Delta t\right) \tag{4.10a}$$

$$a_4 = \frac{\mathrm{d}V}{\mathrm{d}t} \;\;,\;\; b_4 = V_D - \frac{\mathrm{d}V}{\mathrm{d}t} \cdot \left(\frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} - \Delta t\right) \tag{4.10b}$$

$$c_4 = \frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \;\;,\;\; d_4 = -\frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \cdot \left(\frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}}\right) \tag{4.10c}$$

$$a_5 = \frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \;\;,\;\; b_5 = -\frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \cdot \left(\frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}}\right) \;\;,\;\; c_5 = \frac{\mathrm{d}V'}{\mathrm{d}t} \approx -\frac{\mathrm{d}V}{2\mathrm{d}t} \tag{4.10d}$$

$$d_5 = V + L\frac{\mathrm{d}I_{TF}}{\mathrm{d}t} + \frac{\mathrm{d}V}{2\mathrm{d}t} \cdot \left(\frac{I_F + I_{RR}}{\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}} + \frac{V + \left(L\frac{\mathrm{d}I_{TF}}{\mathrm{d}t}\right) - V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} - \Delta t\right) \tag{4.10e}$$

Figure 4.8 shows the more accurate linear approximation of the voltage and current waveforms of Figure 4.5 and the resultant approximation of the instantaneous power. Similar to Figure 4.7, in Figure 4.8 the negative dV'/dt is approximated as half of the positive dV/dt slope (this is an empirical estimation from the measurements) and Δt accounts for the time difference between the peak reverse current and the rise of the diode voltage. This model is developed to take into account of the changes in switching rates and slopes. As can be seen from Figure 4.8, the switching power here is comprised of 6 areas (as oppose to previous model with 5 areas), the sum of which will yield the total switching energy of the PiN diode. It is clear that the profile of the switching power in Figure 4.8 is a closer approximation of the actual measurement in Figure 4.6.

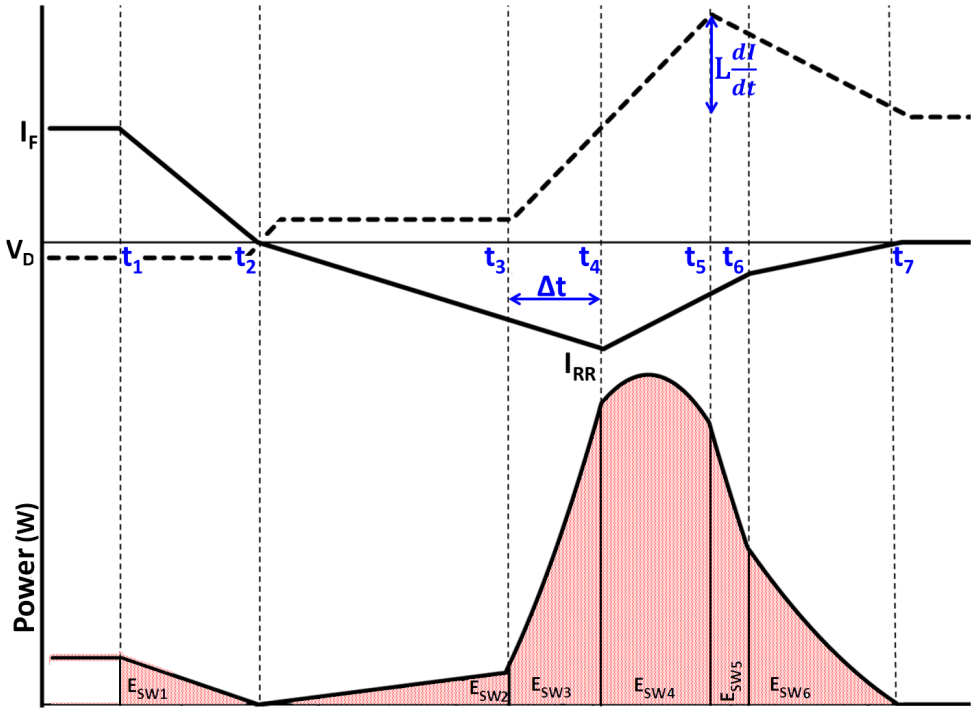


Figure 4.8: Linearized current and voltage waveforms showing reverse recovery, inductive voltage overshoot and the profile of the dissipated power.

The total switching energy can be calculated using equations below:

$$E_{SW} = E_{SW_1} + E_{SW_2} + \sum_{n=3}^{6} E_{SW_n} \tag{4.11}$$

$$E_{SW_1} = \frac{I_F^2 V_D}{2\left(\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}\right)} \tag{4.12}$$

$$E_{SW_2} = \frac{V_D}{2} \cdot \left(I_{RR} - \Delta t \frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}\right) \cdot \left(\frac{I_{RR}}{\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}} - \Delta t\right) \tag{4.13}$$

$$E_{SW_n} = \frac{a_n b_n}{3}\left(t_{n+1}^3 - t_n^3\right) + \frac{a_n d_n + b_n c_n}{2}\left(t_{n+1}^2 - t_n^2\right) + b_n d_n \left(t_{n+1} - t_n\right) \tag{4.14}$$

The switching time intervals defined in Figure 4.8 can be calculated as:

$$t_1 = 0 \quad \text{and} \quad t_2 = \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} \tag{4.15a}$$

$$t_3 = \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{dI_{TF-}}{dt}} - \Delta t \quad \text{and} \quad t_4 = \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{dI_{TF-}}{dt}} \tag{4.15b}$$

$$t_5 = \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{dI_{TF-}}{dt}} - \Delta t + \frac{V + L\frac{\mathrm{d}I_{RR}}{\mathrm{d}t} - V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} \tag{4.15c}$$

$$t_6 = \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{dI_{TF-}}{dt}} + \frac{\frac{\mathrm{d}I_{Tail}}{\mathrm{d}t} \cdot \left(\frac{V + \frac{3}{2}\left(L\frac{\mathrm{d}I_{RR}}{\mathrm{d}t}\right) - V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} - \Delta t \right) - I_{RR}}{\frac{\mathrm{d}I_{Tail}}{\mathrm{d}t} - \frac{\mathrm{d}I_{RR}}{\mathrm{d}t}} \tag{4.15d}$$

$$t_7 = \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{dI_{TF-}}{dt}} - \Delta t + \frac{V + \frac{3}{2}L\frac{\mathrm{d}I_{RR}}{\mathrm{d}t} - V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} \tag{4.15e}$$

and the coefficients of Equation 4.14 can be calculated as:

$$a_3 = -\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t} \quad , \quad a_4 = \frac{\mathrm{d}V}{\mathrm{d}t} \quad , \quad a_5 = \frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \quad , \quad a_6 = -\frac{\mathrm{d}V}{2dt} \tag{4.16a}$$

$$c_3 = \frac{\mathrm{d}V}{\mathrm{d}t} \quad , \quad c_4 = \frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \quad , \quad c_5 = -\frac{\mathrm{d}V}{2dt} \quad , \quad c_6 = \frac{\mathrm{d}I_{Tail}}{\mathrm{d}t} \tag{4.16b}$$

$$b_3 = \frac{\mathrm{d}I_{TF-}}{\mathrm{d}t} \cdot \left(\frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}} \right) - I_{RR} \tag{4.16c}$$

$$b_4 = d_3 = V_D - \frac{\mathrm{d}V}{\mathrm{d}t} \cdot \left(\frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}} - \Delta t \right) \tag{4.16d}$$

$$b_5 = d_4 = -\frac{\mathrm{d}I_{RR}}{\mathrm{d}t} \cdot \left(\frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}} \right) - I_{RR} \tag{4.16e}$$

$$b_6 = d_5 = \frac{3}{2}\left(V + L\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}\right) + \frac{\mathrm{d}V}{2dt} \cdot \left(\frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}} - \frac{V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} - \Delta t \right) \tag{4.16f}$$

$$d_6 = -\frac{\mathrm{d}I_{Tail}}{\mathrm{d}t} \cdot \left(\frac{V + \frac{3}{2}L\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t} - V_D}{\frac{\mathrm{d}V}{\mathrm{d}t}} + \frac{I_F}{\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t}} + \frac{I_{RR}}{\frac{\mathrm{d}I_{TF-}}{\mathrm{d}t}} - \Delta t \right) \tag{4.16g}$$

To make the models temperature compliant, the temperature dependence of the PiN diodes has to be incorporated. The slope of the diode turn-off current (dI_{TF}/dt) reduces with increasing temperature and the peak reverse current increases with temperature due to the higher carrier lifetime. These dependencies can be modelled from experimental measurements of diode reverse current waveforms at different temperatures. The diode peak voltage overshoot due to the parasitic inductance is reduced as the temperature is increased. This happens since the negative temperature coefficient of switching rate has a direct impact on the peak voltage overshoot. The equations that will account for these temperature dependencies of the switching rate, the peak diode voltage overshoot and peak reverse recovery current are as shown below in Equations 4.17a, 4.17b and 4.17c:

$$\frac{\mathrm{d}I_{TF}}{\mathrm{d}t} = \frac{\mathrm{d}I_{TF}}{\mathrm{d}t}^{(25^{\circ}\mathrm{C})} + \frac{\mathrm{d}^2 I_{TF}}{\mathrm{d}t\,\mathrm{d}T}\,(T-25) \tag{4.17a}$$

$$V_{AK} = V^{(25^{\circ}\mathrm{C})} - \frac{\mathrm{d}V}{\mathrm{d}T}\,(T-25) \tag{4.17b}$$

$$I_{RR} = I_{RR}{}^{(25^{\circ}\mathrm{C})} + \frac{\mathrm{d}I_{TF}}{\mathrm{d}T}\,(T-25) \tag{4.17c}$$

Figure 4.5 shows that the slope of the PiN diode's turn-off current is constant at high switching rates. Hence, the model developed in Figure 4.8 can be simplified to the state of Figure 4.7, provided that the following constraints are implemented as:

$$\frac{\mathrm{d}I_{TF+}}{\mathrm{d}t} = \frac{\mathrm{d}I_{TF-}}{\mathrm{d}t} \quad \text{and} \quad \frac{\mathrm{d}I_{Tail}}{\mathrm{d}t} = 0$$

This will effectively remove the E_{SW5} from Figure 4.8. The difference between accuracy of the two developed models will be examined in the next section where the experimental measurements will be used to validate the developed models.

4.2.3 PiN Diode Measurements

Chapter 3 has already detailed parts of the measurements used for validation of the model in this chapter. For the remainder of measurements, the same classical clamped inductive switching circuit shown in Figure 3.3 is used to determine the switching energy and reverse recovery characteristics of the PiN diodes. Figure 4.9 shows the circuit schematic and part number of all devices under test. This arrangement comprises of a low side switching IGBT and a high side PiN diode. The IGBT is switched on initially to charge the inductor after which it is switched off so the current can free-wheel through the PiN diode. The IGBT is then switched on so that the current can commutate from the diode to the IGBT and turn-off characteristics of the diode can be observed. Similar to the measurements in chapter 3, the procedure is repeated for different switching rates (by using different gate resistances) and in different ambient temperatures.

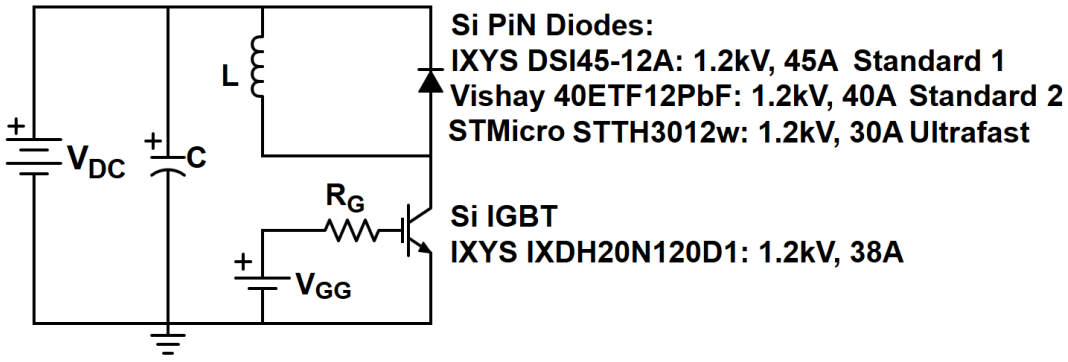


Figure 4.9: Schematic of the 2-Pulse clamped inductive switching rig, DUTs are 3 different PiN diodes with part numbers as shown.

4.2.3.1 Diode Temperature Dependencies

Figure 4.10 shows the measured switching rate as a function of the gate resistance for different temperatures during turn-off of the IGBT which coincides with turn-on of the

diode. As can be seen, increasing the gate resistance has the effect of reducing dI/dt which is expected since the electrical time constant (product of R_G and the input capacitance) increases with the gate resistance. It is also seen that the dI/dt decreases with increasing temperature which is similar to MOSFETs where turn-off dI/dt decreases with temperature. This is due to the reduction of threshold voltage of the device along with the reduced mobility of carrier in higher temperatures.

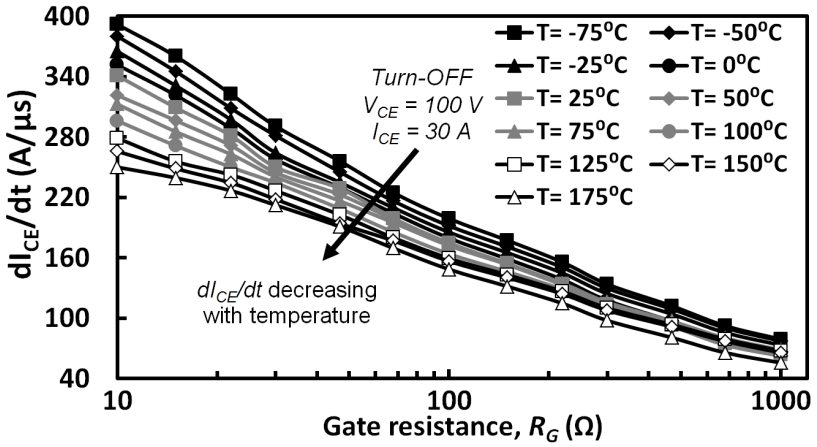


Figure 4.10: Turn-off dI/dt of IGBT (turn-on of PiN diode) as a function of R_G.

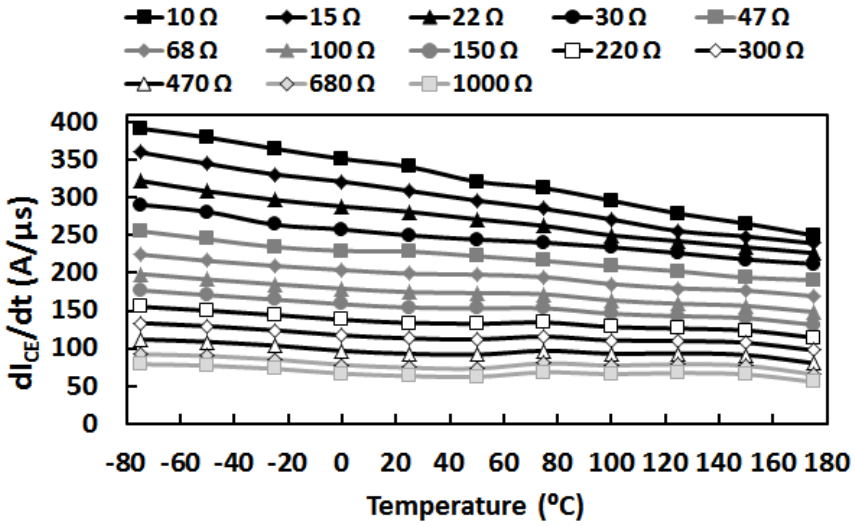


Figure 4.11: Turn-off dI/dt of IGBT (PiN turn-on) as a function of Temperature.

These factors are the carrier lifetime which increases with temperature and especially the carriers mobility which decreases with temperature. Hence, the overall rate at which the IGBT turns-off decreases with temperature. Figure 4.11 shows this as a function of temperature. In other words, the rate of stored charge formation in the drift region decreases as the temperature is increased. This temperature dependency has more influence in determining the switching rate at higher dI/dt (where a low R_G is used to switch the low-side IGBT), however with an increase in gate resistance, the R_G becomes more dominant in determining the dI/dt thereby suppressing the temperature effect.

Figure 4.12 shows the turn-on dI/dt of the IGBT (turn-off of the diode) as a function of the gate resistance for different temperatures. As can be seen from Figure 4.12, the switching rate reduces with increasing temperature in contrast with the case of the MOSFET turn-on characteristics. This is due to the reduced mobility at higher temperatures which will impact the charge extraction rate as well as the reduced threshold voltage at higher temperatures. Figure 4.13 also shows this switching rate as a function of temperature where it is seen that the dI/dt is reduced with increase of temperature.

Temperature dependency of switching rate is also used to parameterize Equation 4.17a. The rate of change of the switching rate with temperature is extracted from the experimental measurements by taking the derivative of dI/dt with respect to temperature, thereby yielding the 2^{nd} order derivative of the current with respect to time and temperature ($d^2I/dtdT$). This parameter is plotted as a function of the gate resistance in Figure 4.14 for the 3 discrete PiN diodes in Figure 4.9. Because dI/dt decreases as temperature increases as a result of increased carrier lifetime and decreased mobility with temperature, $d^2I/dtdT$ is negative as can be seen in Figure 4.14. It can also be seen from Figure 4.14 that the magnitude of $d^2I/dtdT$ slightly decreases with gate resistance. The reduction is due to the effect of large R_G dominating over the impact of temperature.

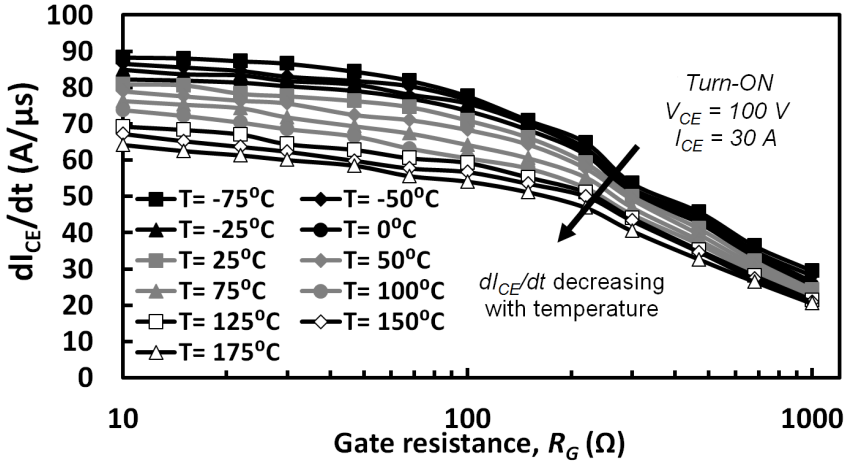


Figure 4.12: Turn-on dI/dt of IGBT (turn-off of PiN diode) as a function of R_G.

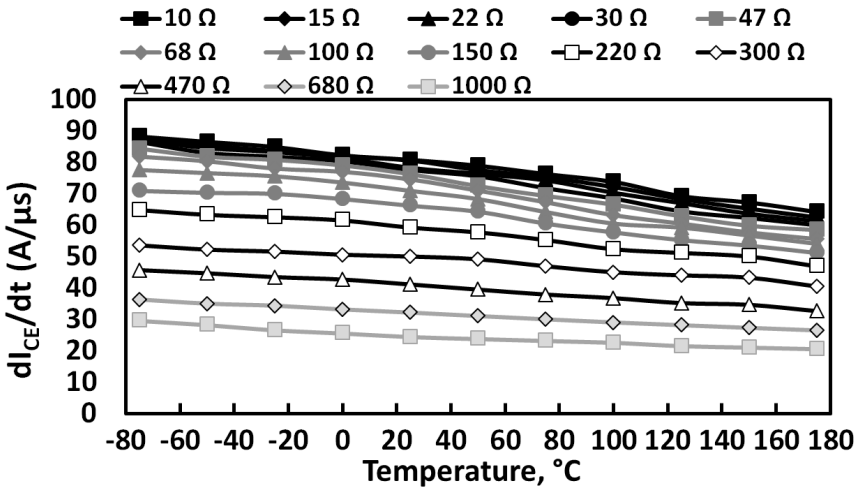


Figure 4.13: Turn-on dI/dt of IGBT (PiN turn-off) as a function of temperature.

The rate of change of $d^2I/dtdT$ with R_G is low enough for it to be considered constant without reducing the accuracy of the model. Subsequent comparisons of the model's results with experimental measurements in the validation section of this chapter will show this to be the case. The implication is as follows: if the rate of change of switching rate (dI/dt) with temperature is known, this can be used to accurately predict the switching energy of diode when it is switched at different rates and temperatures. Hence, Figure 4.14 is used to parameterize Equation 4.17a.

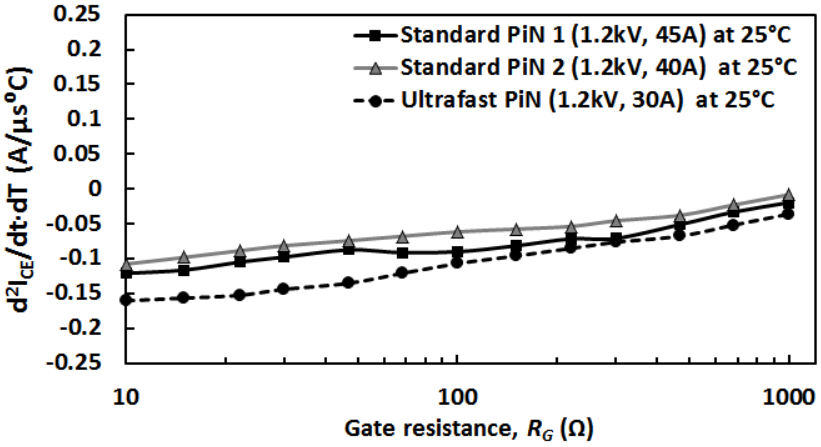


Figure 4.14: The $d^2I/dtdT$ as a function of gate resistance for IGBT turn-on.

Figure 4.15 shows the temperature dependency of the peak reverse recovery current and the peak diode voltage overshoot of the PiN diode when the low side IGBT is switched with a sample gate resistance of 22 Ω. As can be seen in Figure 4.15, the peak reverse recovery current has a positive temperature coefficient whereas the peak diode voltage overshoot has a negative temperature coefficient. The peak diode voltage overshoot dependence on temperature is used to parameterize Equation 4.17b whereas the temperature dependence of peak reverse current is used to parameterize Equation 4.17c.

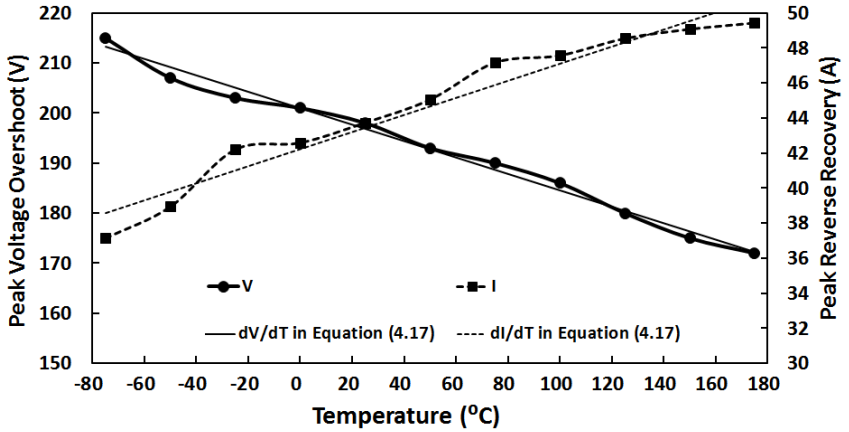


Figure 4.15: Peak reverse recovery current and the peak diode voltage overshoot as functions of temperature for $R_G = 22\ \Omega$.

4.2.3.2 Diode Switching Rate Dependencies

Next, the dependence of the peak currents/voltages and power transients on the switching rates is investigated for the case of standard diode 1 at 300 V measurements. The wide range of R_G used in measurements provides a wide range of dI_{TF}/dt that can be used for the purpose of validating the model. Figure 4.16 shows the impact of increasing the switching rate on the reverse recovery characteristics of the PiN diode. It is seen that the peak reverse recovery current (I_{RR}) increases with the dI_{TF}/dt and the recovery time reduces with increasing dI_{TF}/dt, i.e. the diode snappiness increases with dI_{TF}/dt.

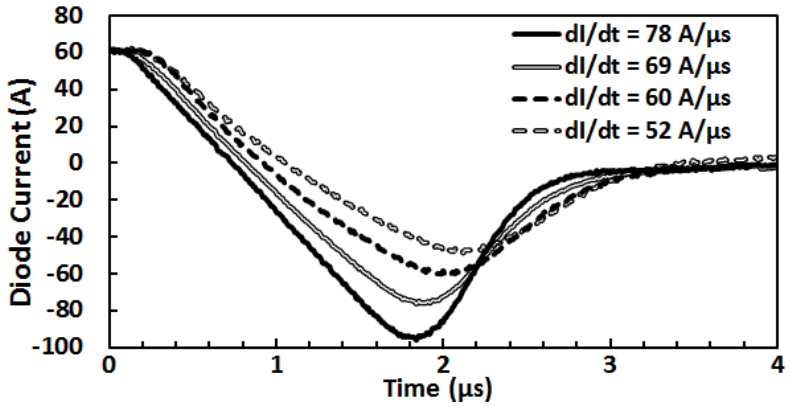


Figure 4.16: PiN diode reverse recovery current as a function of the switching rate at 25 °C with $I_F = 60$ A for standard diode 1 (IXYS® DSI45-12A).

Figure 4.17 shows the diode voltage transients as a function of the dI_{TF}/dt. It is seen that the peak diode voltage overshoot also increases with dI_{TF}/dt. Figure 4.18 shows a plot of the switching power for different switching rates. It is seen that the peak power increases with dI_{TF}/dt, although the width of the power pulse increases as dI_{TF}/dt is reduced. Furthermore, at some point the increase in the width of the power pulse causes the switching energy to start increasing, hence, there is an optimum switching rate for the minimization of switching energy.

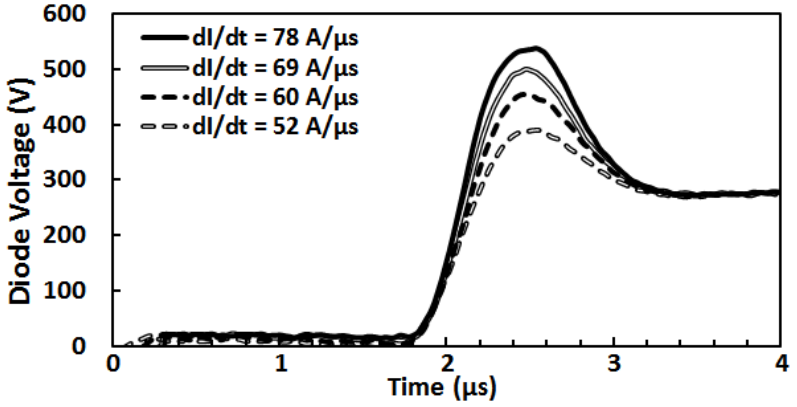


Figure 4.17: PiN diode switching voltage as a function of the switching rate at 25 °C at 300 V for standard diode 1 (IXYS® DSI45-12A).

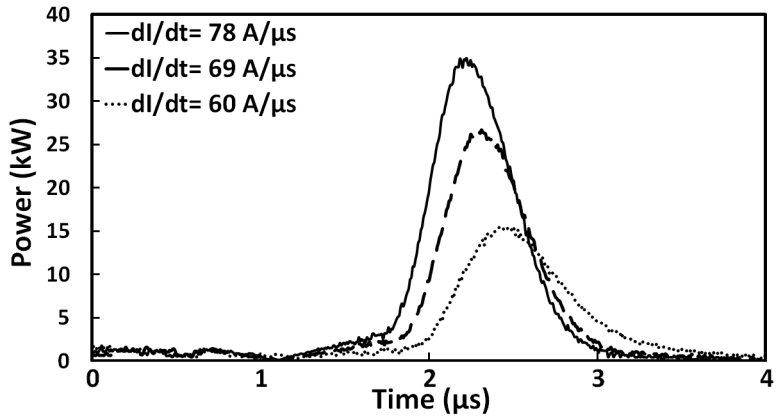


Figure 4.18: PiN diode turn-off switching power at different switching rates at 25 °C with 300 V and 60 A for standard diode 1 (IXYS® DSI45-12A).

Overall, a higher switching rate might cause a higher switching energy due to the increased peak power while a lower switching rate might also result in higher switching energy due to the increased time duration of the power pulse. Additionally, Figure 4.19 shows the switching power pulse as a function of time for different temperatures. It is seen that the peak of the power pulse increases with temperature, due to the increased peak reverse recovery current by the positive temperature coefficient of carrier lifetime.

Equation 4.2, which expresses the peak reverse recovery current as a function of the square root of dI_{TF}/dt was developed as a model to predict the peak reverse recovery

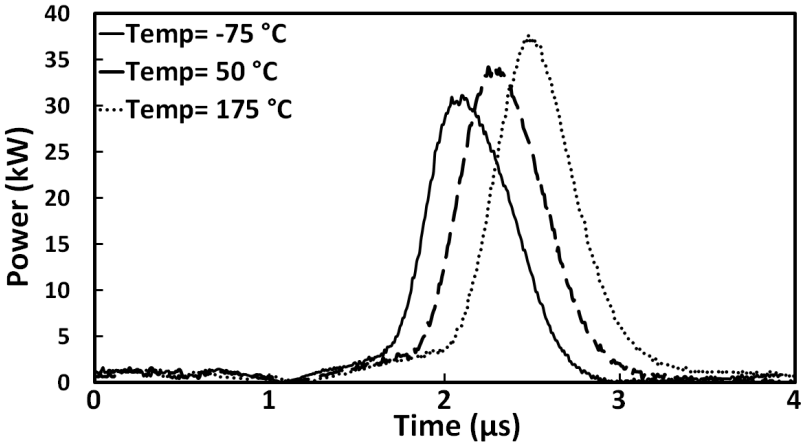


Figure 4.19: PiN diode turn-off power at different temperatures ($R_G = 10\ \Omega$).

current as a function of the diode parameters [54]. The model suggests that the plot of square root of the switching rate against the peak reverse recovery current (I_{RR}) yields a straight line. Figure 4.20 shows this plot using the experimental measurements at 3 different temperatures where a constant slope can be observed. By using the slope of this line, the value of parameter k_Q can be derived relating to the charge stored in the diode [53]. Hence, if k_Q is experimentally extracted for a specific diode, the model's I_{RR} can be substituted by the I_{RR} in 4.2. Here, k_Q is approximately equal to 15 $C/A^{0.5}$.

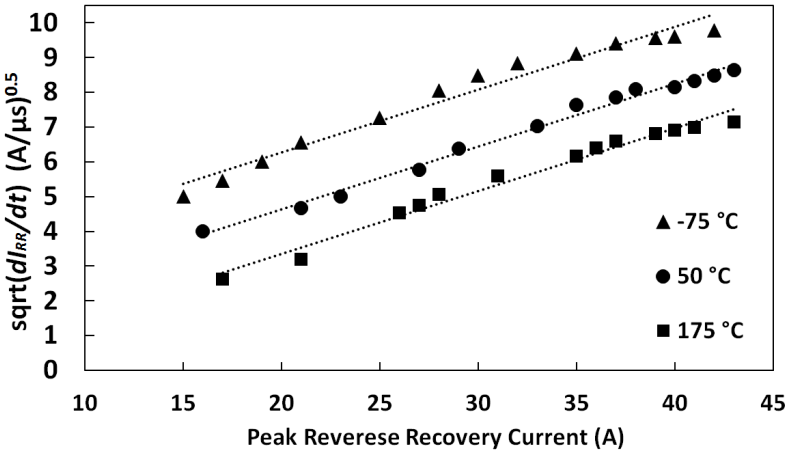


Figure 4.20: Square root of dI_{TF}/dt as a function of the peak reverse current.

4.2.3.3 Snappiness of the Diode's Reverse Recovery

The snappiness (or softness when referring to the opposite) of a PiN diode is a measure of how quickly the reverse recovery current of the diode returns to zero from the peak negative value [53] and is an important reliability measure. Diode snappiness can be defined as the ratio of the duration of the recombination phase to extraction phase and depends on parameters like lifetime and mobility of minority carriers as well as circuit parameters such as the switching rate. Some publications have defined this metric as the ratio of time taken for the current to go from I_{RR} (the peak reverse recovery current) to 0 to the time taken for it to go from 0 to I_{RR} [54]. In Figure 4.8, this is $(t_7 - t_4)/(t_4 - t_2)$.

However, this is not accurate in all cases [55]. Therefore, other publications have better defined this metric as the ratio of the dI/dt of the positive slope (recovery) and the negative slope (turn-off) or $(dI_{RR}/dt)/(dI_{TF}/dt)$ in the reverse recovery transient [56]. Overall, snappy diodes switch quicker and exhibit less switching energy, however this can be at the cost of reliability issues like excessive voltage spikes and EMI. Soft recovery diodes generally have higher switching energy although are less of a reliability concern.

Here, the dependency of diode snappiness on temperature has been assessed by the measurements. The snappiness factor is calculated as the ratio of dI_{RR}/dt to dI_{TF}/dt meaning that a small number (normally less than 1.25 [57]) is soft whereas a larger number is snappy. Should the snappiness to be defined by time rather than switching rates, this definition would have been reversed, i.e. a larger number means softer recovery.

Figure 4.21(a), (b) and (c) shows the impact of temperature on the snappiness of the diodes reverse recovery at 3 different temperatures. The square symbols represent the measured dI/dt of the diode turn-off current when the carriers are being extracted in the opposite direction to conventional current flow, i.e. the negative slope current. The lines

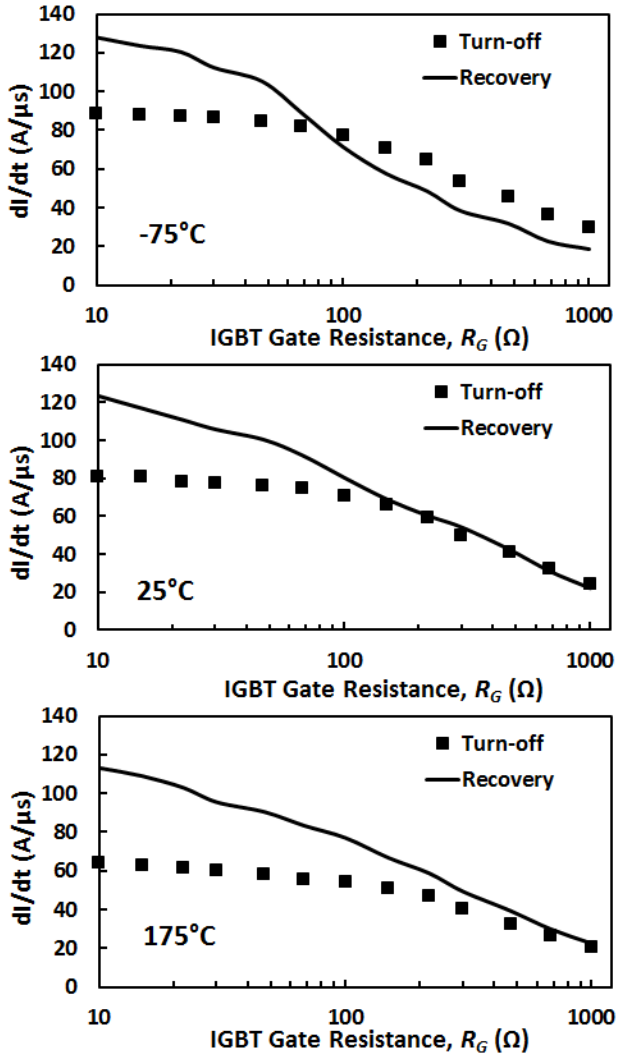


Figure 4.21: Turn-off and recovery dI/dt varied by temperature.

in this figure represent the measured dI/dt between the peak reverse recovery current and zero, i.e. the positive slope current that is formed by minority carrier recombination in the charge storage region. Because excessively snappy diodes can cause reliability problems during hard commutation with high dI/dt, fabrication steps can be taken to ensure soft recovery. It can be seen from Figure 4.21 that at small gate resistances, the recovery dI/dt is higher than the turn-off dI/dt and as the gate resistance is increased, the recovery dI/dt becomes equal or even smaller than the turn-off dI/dt.

It can also be seen from Figure 4.21 that an increase in temperature results in an increase in the snappiness. This is due to the fact that snappiness is a relative measure and depending on both the turn-off and recovery slopes. The calculations presented in Figure 4.22 also show that the snappiness of the diode increases with both the temperature and switching rate similar to what has been stated in [58] for fast recovery diodes.

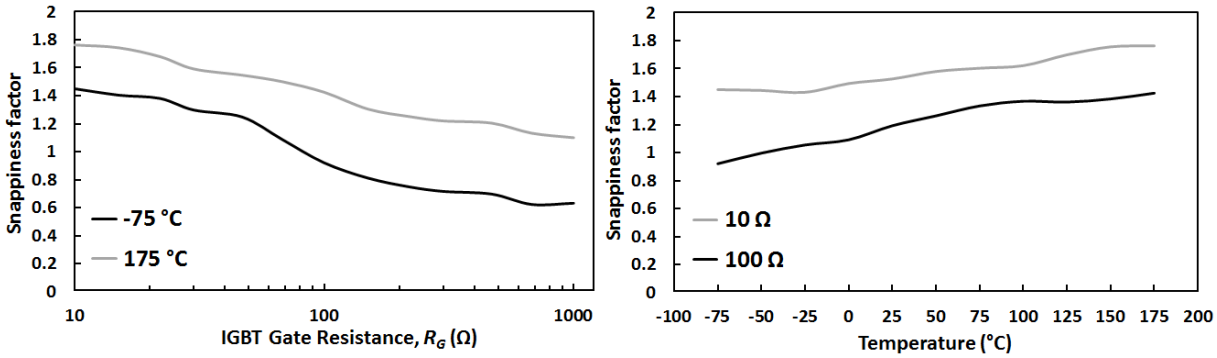


Figure 4.22: Snappiness factor as a function of the gate resistance and temperature.

4.2.4 Model Validation

The model output has been validated by comparison of the results with the measurements obtained through current commutation between the low side IGBT and the high side PiN diode. The validity of the model is tested by applying it to 3 PiN diodes with different characteristics; an ultra-fast diode rated at 1.2 kV and 30 A and two standard recovery PiN diodes rated at 1.2 kV and 40 A and 45 A. These diodes have been experimentally characterized with different switching rates and in the same range of temperatures.

Figure 3.37 has shown a 3-D plot of measured switching energy of standard diode 1 (IXYS® DSI45-12A) as a function of the switching rate and temperature. It can be seen in Figure 3.37 that the switching energy is lowest at intermediate switching rates. At high switching rates, the switching energy increases due to high peak reverse recovery currents

and especially high peak diode voltage overshoots which is a direct product of switching rate. Hence, the switching power pulse is higher. The switching energy also increases with increasing temperature. The measurements are also repeated on an ultrafast diode with superior recovery performance, although this is at the cost of implementing higher density of recombination centers in the drift region of the device, hence higher forward voltage drop during conduction as a result of lower carrier lifetime. The reverse recovery of the diodes used to validate the model is shown in Figure 4.23 where the reduced reverse recovery charge of the ultra-fast diode can be observed relative to the standard diodes.

Next, the ability of the model to correctly predict the trends seen in Figure 3.37 is examined. The model was parameterized using the values of measurements. The inputs to the model included the measured turn-off and reverse recovery dI/dt, the dV/dt, the forward current, the peak reverse current, the temperature dependencies of the peak reverse current, dI_{TF}/dt and diode voltage overshoot as well as parameters like on-state voltage drop. These parameters are obtainable by analyzing any given transient waveform.

Figure 4.24(a) shows the results of comparison between the experimental measurements and the models developed for calculating the switching energy. Figure 4.24(a) shows the measured switching energy of the 3 devices on a logarithmic scale and as a function of switching rate whereas Figure 4.24(b) shows the modeled results. As can be seen from Figure 4.24, the proposed model correctly predicts the turn-off switching energy of the PiN diode including the minimum switching energy and overall switching rates.

In Figure 4.25, unlike Figure 4.24 where the switching energy was plotted on a logarithmic basis, the model and measurements results are plotted on a non-logarithmic mode only for the standard recovery diode 1 for both the simple and complex models to compare how the two models differ in terms of the accuracy of the outputs. It can be seen that the calculated switching energy of the simple model is on average within 20% margin of

error of the experimentally measured switching energies, while the margin of error in the complex model is reduced to approximately below 10%. Figure 4.26(a) shows the measured switching energy as a function of temperature for the same devices switched with a gate resistance of 10 Ω whereas Figure 4.26(b) shows the calculated switching energy derived from the model. Again, it can be seen that the calculated and measured switching energies are within an acceptable margin of error. Hence, although some experimental characterization of the diode is required to parameterize the model, the advantage of the model is that once this is done, the switching energy at different switching conditions can be easily predicted. This enables predicting the switching energy (and consequently temperature rise as a result of these losses) in different application scenarios.

Since the model is considering a non-oscillatory mode for the reverse recovery transient, in the ultrafast diodes switched at lower temperatures, the accuracy of the model output might be slightly reduced since excessively snappy recovery currents are known to occur at low temperatures. However, as these oscillations are normally small (when compared to the amplitude of the peak reverse recovery), the portion of the switching energy they represent is significantly smaller relative to the actual reverse recovery waveform. Hence, the accuracy of the model is only slightly reduced. This model can also be used to predict the switching energy of the body diodes of power MOSFETs since body diodes also exhibit reverse recovery characteristics during turn-off. This is especially the case with the reverse recovery performance of body diodes in the silicon power MOSFET and CoolMOS™ due to the high level of stored charge in these devices. This will be discussed more in chapter 5. SiC Schottky diodes also exhibit oscillations during turn-off and since the model is not designed to predict such conditions, it cannot account for their switching energy. Subsequent models in this chapter address the switching energy and ringing characteristics of SiC Schottky diodes during turn-off.

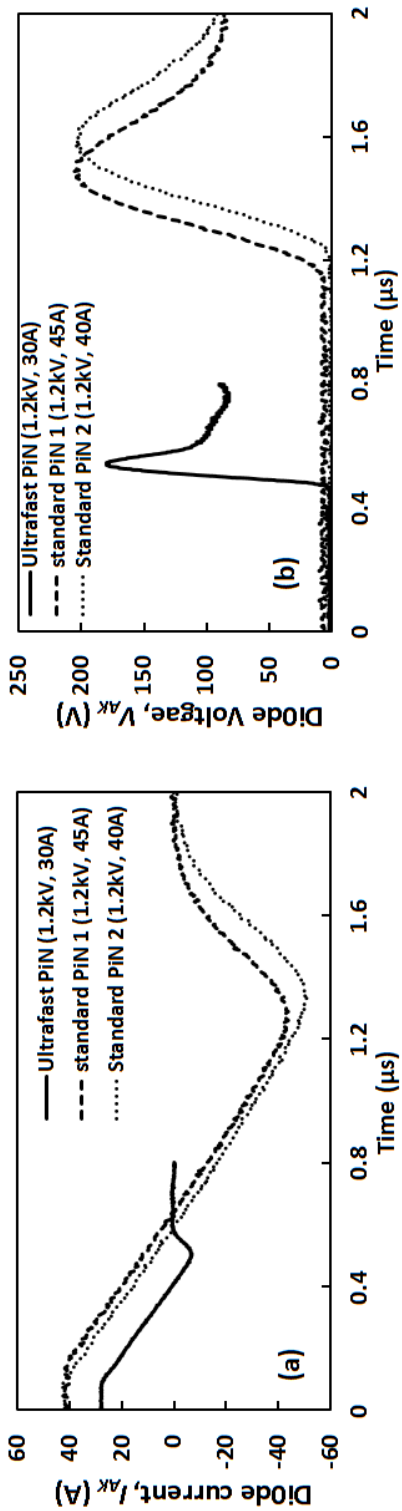


Figure 4.23: Reverse recovery and voltage overshoot for model validation of the model with $R_G = 10\ \Omega$ at 25 °C.

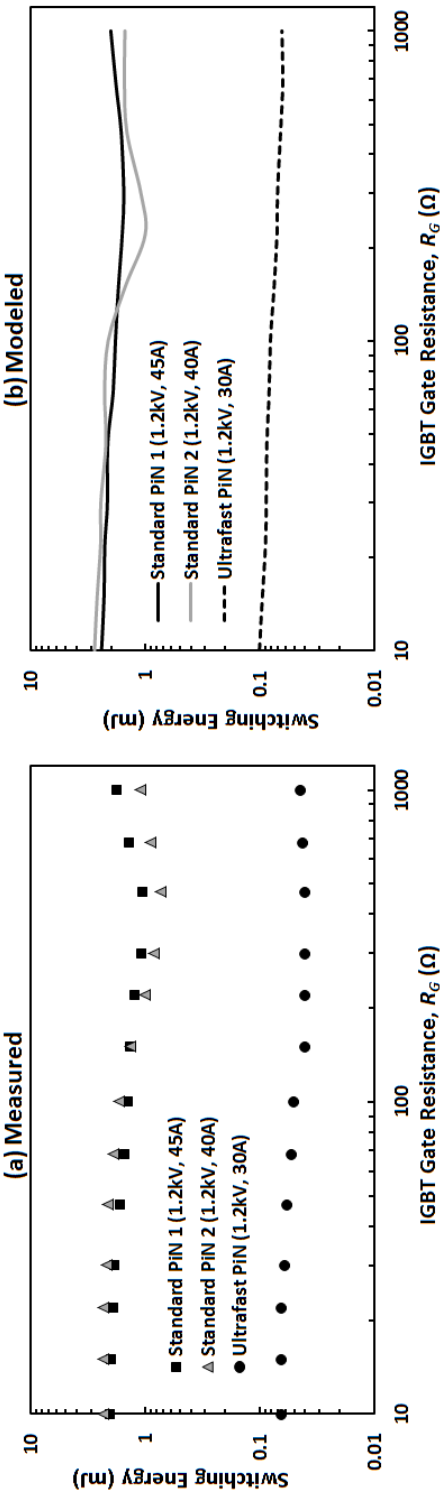


Figure 4.24: Measured and modeled switching energy as a function of the gate resistance performed at room temperature (25 °C) presented on a logarithmic basis.

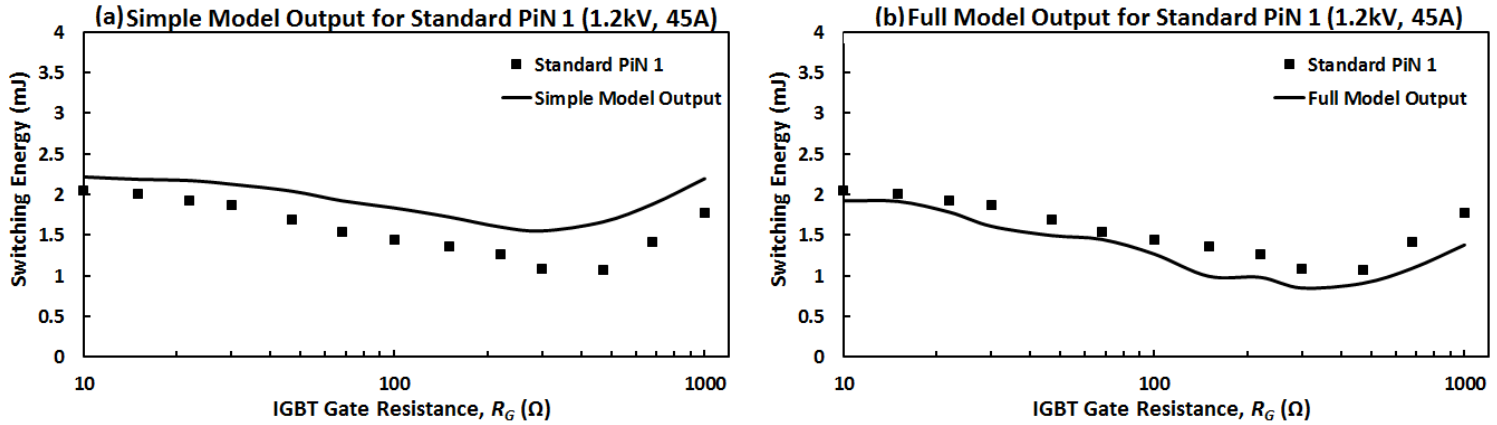


Figure 4.25: Measured and modeled switching energy as a function of the gate resistance performed at room temperature (25 °C) presented on a non-logarithmic basis for the two different modeling techniques.

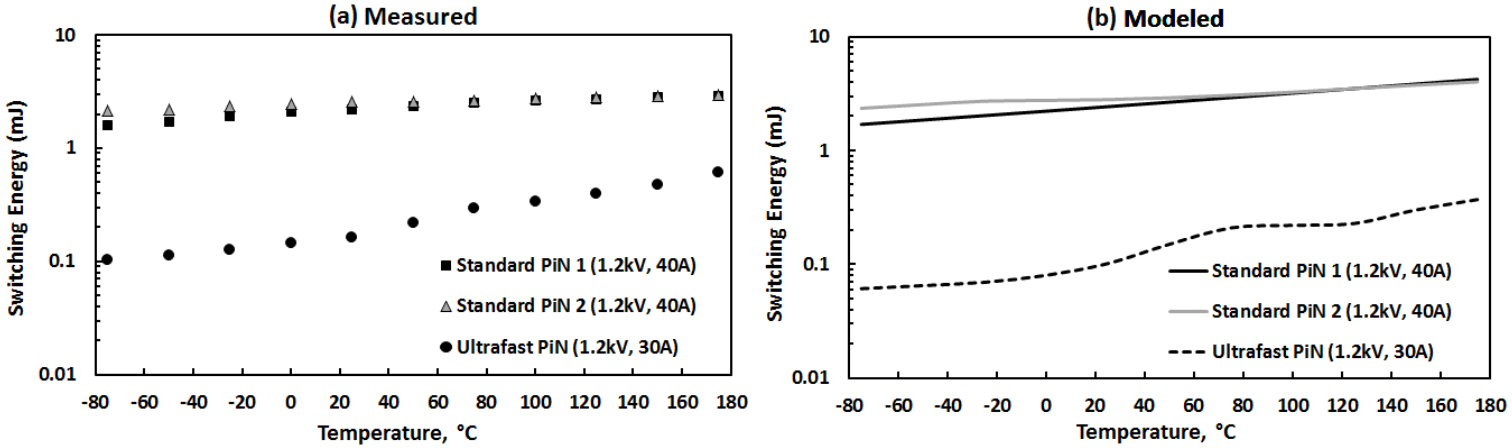


Figure 4.26: Measured and modeled switching energy as a function of the temperature (with $R_G = 10\ \Omega$) presented on a logarithmic basis.

4.3 Interactions between SiC MOSFETs and SBDs

SiC Schottky barrier diodes which were discussed in chapter 2 have particularly shown significant improvements in the performance of rectifiers compared with traditional silicon PiN diodes. It has been previously demonstrated that the use of these temperature rugged and power dense devices as rectifiers rather than conventional silicon PiN diodes can significantly reduce thermal stress, lower power losses [59] and enhance the conversion efficiency in power converters by removing the reverse recovery of the PiN diodes [60]. As a result, their application as rectifiers in power converters is getting more popular [61]. These include power converters for a range of applications [62] such as power factor correction circuits [63] and also in harsh environments such as in space applications [64].

The physics and structure of the SiC SBD is presented in [65] where better electro-thermal performance in harsh environments have been presented [66]. Due to lower voltage drop in low voltage Schottky diodes, they can also be used to block the unwanted conduction of the MOSFET's body diodes in converters [67]. The importance of this application will be discussed in chapter 5. In addition switching of SiC Schottky diodes in combinations with silicon power MOSFETs [68], CoolMOS™ [69], SiC MOSFETs [70] and JFETs [71] have shown advantages compared to the combinations with PiN diodes [72].

However, advances in packaging technologies are not catching up with devices. Parasitic inductances in power modules and circuit current paths/wires induce oscillations in output characteristics which can be detrimental through additional losses and reduced reliability [73]. These parasitic inductances depend strongly on the architecture of the power module and the circuit layout [73]. SiC Schottky diodes are prone to such ringing and as the switching frequency increases, even small parasitic inductances cannot be ignored because of the high dI_{DS}/dt. This ringing is due to the interaction between the

diode depletion capacitance and stray inductance of the circuit wiring and packaging [74].

The ringing characteristics are sensitive to temperature variations and the switching rate of the commutating transistor. Previously reported research on the switching characteristics of SiC SBDs has focused on temperature invariance at high switching rates [75] whereas as will be seen here, at lower switching rates, the switching characteristics of SiC SBDs becomes more temperature sensitive. In other words, the damping of the oscillations is strongly temperature dependent when switched slower. Hence, in the case of SiC SBDs, there is a need for accurate switching energy modeling techniques that can account for the ringing in the diodes output. In the first instance, modeling these devices seems less complex as they are unipolar, however, there are modeling challenges arising from the dependence of diode ringing on the parasitic elements, temperature and the commutation rate of the transistor. The dependence of this ringing on the ambient temperature and the rate of change of current with time (dI_{DS}/dt) of the switching MOSFET has not been fully characterized. A potential solution to this ringing problem could be the use of soft switching techniques where zero current and/or zero voltage switching can be implemented. However, this will increase the cost and complexity of converters at the power levels targeted by SiC. Additionally de-coupling capacitors can be employed to assist in damping the oscillations as will be seen in chapter 6, but this is also not always a feasible option, especially in higher power cases which require high voltage capacitors.

Therefore the deployment of SiC power devices in hard-switched applications will require more understanding in the dependence of switching energy on temperature and switching rate [76]. To explore these concepts, the results of the measurements of SiC MOSFET and SiC Schottky diode provided in chapter 3 are analyzed. In the remainder of this chapter, using fundamental device equations, the dependence of dI_{DS}/dt on the temperature and gate resistance is derived and shown to fairly replicate the experimental

measurements. This temperature dependency is then used to explain the performance of the Schottky diode and to predict its switching energy.

4.3.1 SiC Unipolar Device Pairs

As diodes cannot switch independently, their switching transients are influenced by the transistors. Hence, to take advantage of the high switching rates, both the diodes and transistors must be unipolar; otherwise the slow switching of either will result in the lagging of the other. So in this case, SiC MOSFETs are switched along with the SiC Schottky diodes to understand how the fast switching rates impact their performance.

4.3.1.1 Schottky Diodes Elements

When it comes to the total energy loss, normally the calculations are made for the switching energy of devices together with the on-state losses. However, Schottky diodes are one category of devices where the off-state losses might also get important [6]. This is due to their significant temperature-dependant leakage current. Therefore, a high barrier height might be necessary in certain applications where the temperature is too high to reduce the leakage current, although this increases the forward voltage drop of device.

An important element in SBDs is the device depletion capacitance present as a result of the depletion region formed at the metal/semiconductor junction and depends on the semiconductor material through the dielectric constant (ε_r). This was previously determined in equation 2.31 in chapter 2. Biasing the device with V_R will increase it as:

$$W_D = \sqrt{\frac{2\varepsilon_r}{qN_D}(V_R + V_{bi})} \tag{4.18}$$

hence, the voltage-dependant depletion capacitance of SBDs can be calculated from:

$$C_{AK} = \frac{\varepsilon_r}{W_D} \tag{4.19}$$

This parameter will have a determining role in explaining the behaviour of SiC SBD and in developing models to predict it.

4.3.1.2 Gate Voltage Operation in MOSFETs

To turn-on a MOSFET, a voltage from the gate driver, namely V_{GG} must be applied to the gate. The gate driver design used in the measurements is provided in Appendix E. This gate voltage can be considered as a step voltage to the MOSFET gate, and by using the equivalent circuit of the MOSFET, the transients can be determined accordingly [5].

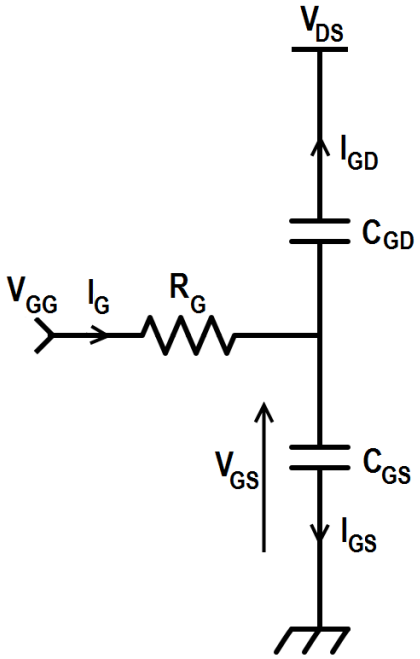


Figure 4.27: Equivalent elements of the MOSFET connected to its gate terminal.

For the turn-on transient, by looking at Figure 4.27 and assuming a constant V_{DS} and based on the Kirchhoff's law , the voltage and current are determinable as:

$$I_G = \frac{V_{GG} - V_{GS}}{R_G} \tag{4.20a}$$

$$I_G = I_{GS} + I_{GD} \tag{4.20b}$$

$$I_{GS} = C_{GS}\frac{\mathrm{d}V_{GS}}{\mathrm{d}t} \tag{4.20c}$$

$$I_{GD} = C_{GD}\frac{\mathrm{d}\left(V_{GS} - V_{DS}\right)}{\mathrm{d}t}\bigg|_{V_{DS}=const.} = C_{GD}\frac{\mathrm{d}V_{GS}}{\mathrm{d}t} \tag{4.20d}$$

Hence, it can be seen that:

$$\frac{V_{GG} - V_{GS}}{R_G} = C_{GS}\frac{\mathrm{d}V_{GS}}{\mathrm{d}t} + C_{GD}\frac{\mathrm{d}V_{GS}}{\mathrm{d}t} \tag{4.21a}$$

$$\frac{dV_{GS}}{V_{GG} - V_{GS}} = \frac{dt}{R_G(C_{GS} + C_{GD})} \tag{4.21b}$$

$$-ln(V_{GG} - V_{GS}) = \frac{t}{R_G(C_{GS} + C_{GD})} + k \tag{4.21c}$$

$$V_{GS} = V_{GG} - \left(e^{\dfrac{-t}{R_G(C_{GS} + C_{GD})}} \cdot e^{-k} \right) \tag{4.21d}$$

and since initially (at t=0) V_{GS} is also zero, so e^{-k} must be equal to V_{GG}, hence:

$$V_{GS} = V_{GG} - V_{GG} \cdot e^{\dfrac{-t}{R_G(C_{GS} + C_{GD})}} \tag{4.22}$$

As C_{iss} was previously determined in 2.41a, Equation 4.22 can be simplified [77] to:

$$V_{GS} = V_{GG}\left(1 - exp\left(-\frac{t}{R_G C_{iss}}\right)\right) \tag{4.23}$$

For the turn-off transient, the charged capacitors must be discharged through the R_G. The stored charge, the resulting discharge current and capacitor voltage are related as:

$$V_{GS} = \frac{q_{iss}}{C_{iss}} \tag{4.24a}$$

$$V_{GS} = -R_G \frac{\mathrm{d}q_{iss}}{\mathrm{d}t} \tag{4.24b}$$

$$-R_G \frac{\mathrm{d}q_{iss}}{\mathrm{d}t} = \frac{q_{iss}}{C_{iss}} \tag{4.24c}$$

where arranging the parameters in order results in:

$$\frac{\mathrm{d}q_{iss}}{\mathrm{d}t} = -\frac{q_{iss}}{R_G C_{iss}} \tag{4.25a}$$

$$\frac{\mathrm{d}q_{iss}}{q_{iss}} = -\frac{dt}{R_G C_{iss}} \tag{4.25b}$$

And by integrating both sides of 4.25a, we have:

$$ln(q_{iss}) = -\frac{t}{R_G C_{iss}} - k \tag{4.26}$$

Since at turn-off, the capacitor voltage (and consequently its charge) are at applied gate potential, Equation 4.26 can be expended as:

$$q_{iss} = q_{GG} \cdot exp\left(-\frac{t}{R_G C_{iss}}\right) \tag{4.27}$$

and as the stored charge in a capacitor has a linear relation with its capacitance as in 4.24a, the voltage transient at turn-off can be derived [77] as:

$$V_{GS} = V_{GG}\, exp\left(-\frac{t}{R_G C_{iss}}\right) \tag{4.28}$$

When the MOSFET is off, current is free-wheeling in the charged inductor and the FWD. As the transistor is switching on, current commutates from the diode to the transistor at a rate depending on the RC time constant of the MOSFET. Hence, the voltage across the diode rises from the on-state voltage drop to the supply voltage. In this regard, Equations 4.23 and 4.28 can be used to understand the transients of the device.

Looking at Figure 4.28, when the gate voltage rises, no channel is present until V_{GS} reaches the threshold voltage (V_{TH}), hence the output characteristics are unaffected. This will be until t_1 in Figure 4.28.

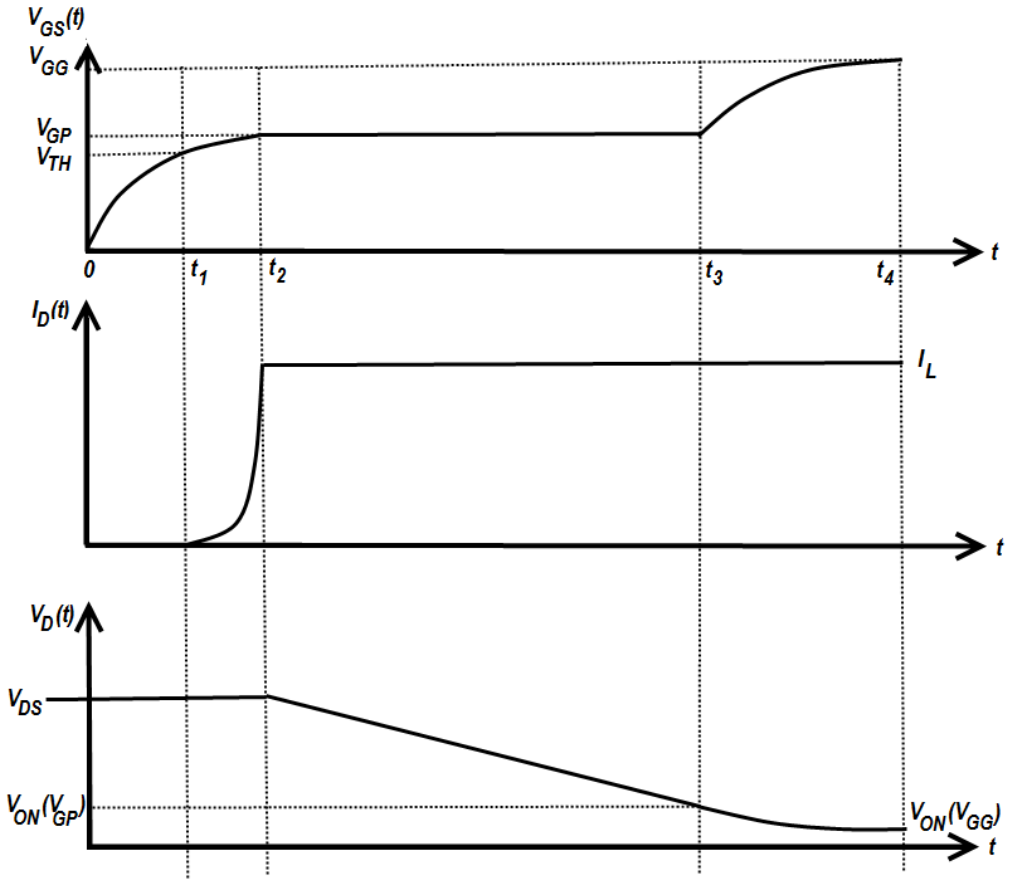


Figure 4.28: The gate voltage and drain-source voltage and current transients of a MOSFET at turn-on.

When the device reaches the V_{TH}, the inversion layer of channel is formed and the current starts to flow from the drain-to-source (in fact electrons are flowing from source-to-drain). The current reaches the load current while the voltage is still in blocking mode since the conducting current in diode must first be extracted before the diode can transit into the blocking mode (in a MOSFET/SBD pair, no reverse recovery in the diode occurs). At this time, V_{GS} has reached the plateau stage and remains constant while the drain voltage drops to on-state voltage drop. Up to this point (t_2), the gate current has mainly been charging C_{GS}. When V_{GS} reaches V_{GP}, it starts to charge the Miller capacitance C_{GD}, hence the value of V_{GS} remains constant since C_{GS} is not being charged at this time. This happens as a result of the fact that the value of voltage-dependant Miller capacitance C_{GD} increases during the drain voltage transient, hence C_{GD} requires more charge. This trend continues until t_3 where V_{DS} drops to on-state and the Miller capacitance reaches its highest value, at which time V_{GS} once again starts to increase to complete charging both capacitors, although at a lower rate since the value of C_{GD} is now closer to that of C_{GS}. This continues until t_4 when the V_{GS} reaches V_{GG}. At this time the gate channel resistance becomes even lower (as the higher gate voltage forms a more conductive channel) and hence the overall device voltage drop is further reduced.

By the end of this process, and when the MOSFET is to be switched off, majority of the supply voltage falls across it hence the FWD is to be forward biased and conducting. The voltage drop across the FWD during this phase will be due to its on-state resistance. When the MOSFET is switched on and starts conducting, the current is commutated away from the FWD and the voltage across the MOSFET starts to fall to its on-state voltage drop. This causes the FWD to become reverse biased and blocking. The turn-off sequence is very similar to the turn-on, and can be described in reverse order of turn-on as in Figure 4.29 as the parasitic capacitances will discharge in the gate resistance. In this

case, the V_{GS} drops from V_{GG} to V_{GP}, and until this happens the voltage and current of the device remains the same, except for the slight increase in on-state voltage drop due to increase in the channel resistance. When the gate voltage reaches V_{GP}, the drain voltage rises (to turn-on the diode) and reaches the off-state voltage. Until this happens, the V_{GS} remains at the plateau level, while the Miller capacitance discharges (as V_{DS} rises, the C_{GD} becomes smaller). At this stage, finally the current drops (and flows into the diode) and the discharge of parasitic capacitances continues with even a faster rate, due to smaller Miller capacitance, until zero.

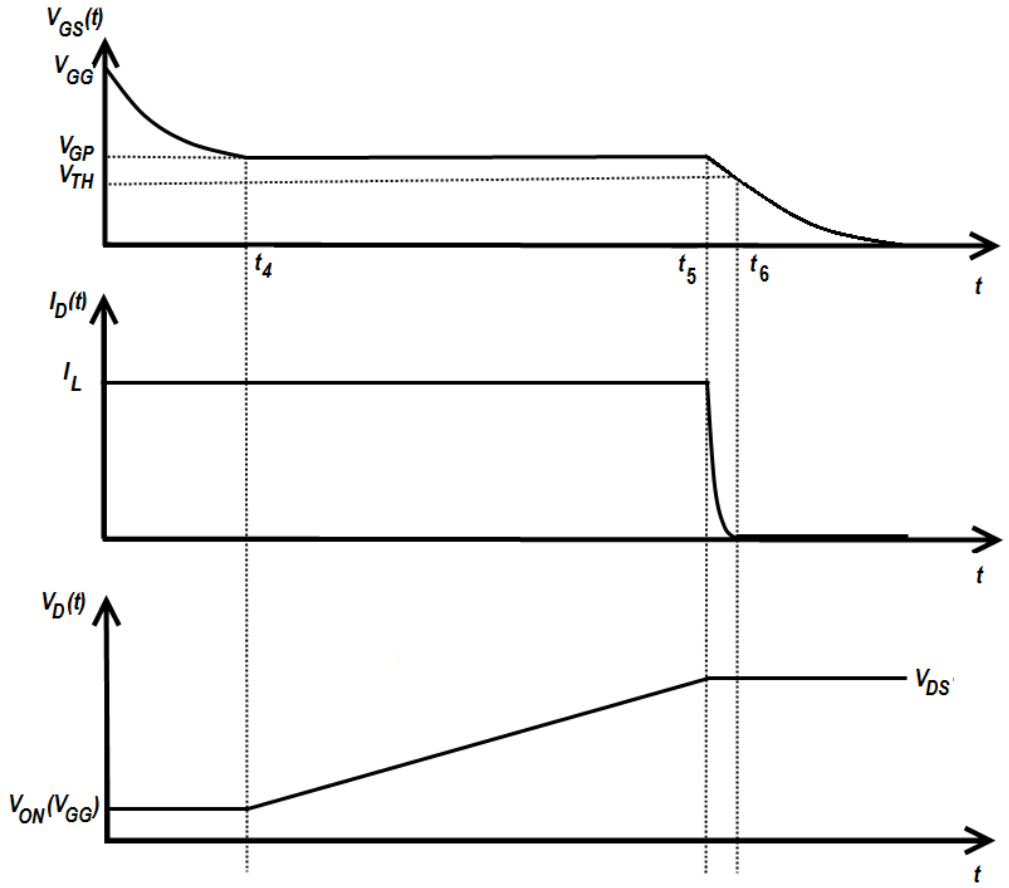


Figure 4.29: The gate voltage and drain-source voltage and current transients of a MOSFET at turn-off.

4.3.2 Impact of Ringing in VSCs with SBDs

The above mentioned transients represent a semi-ideal situation where no reverse recovery and/or ringing is present in either device voltage or current. However, this is not the case in the measurements. As was seen in previous sections, in the case of silicon PiN diodes at turn-off, the reverse recovery of the diode causes the transistor current in Figure 4.28 to experience a significant overshoot, contributing to its switching energy. However, the situation is worse in the case of SiC SBDs. These devices have a high switching rate which coupled by the device capacitance and the parasitic inductance of the circuit results in a significant ringing in the diode output which can in turn affect the device current and the DC link voltage. This is seen in chapter 6.

4.4 Analytical Model of SiC SBD

To understand the behavior of the SiC MOSFET switching with a SiC SBD, the device equations derived in sections 2.2.4.2 and 4.3.1.2 are to be used to replicate the results of the experimental measurements performed in chapter 3. Results of the matching models with the measurements are provided here.

4.4.1 Measurements of Switching Transients

Details of the design and operation of the test rigs are presented in Figures 3.1, Figure 3.3 and Figure 3.5. The measurements used a clamped inductive switching test rig comprising of the devices under test, commutation inductors, gate drive system and power supplies. This circuit emulates one phase-leg of a 3 phase voltage source converter in which free-wheeling diodes (FWD) conduct current in the opposite direction to the MOSFET, i.e.

the diodes rectify while the MOSFETs invert. It should be noted that emergence of SiC devices have raised the high temperature expectations considerably as they are proven to act better in such conditions compared to their silicon counterparts [78]. However, the temperature here is the highest temperature allowed by the device datasheet (175 °C) due to their packaging restrictions and not the semiconductor device itself. Therefore, for higher temperatures and harsh environments such as in aeronautical applications, bare dies should be packaged exclusively. The power supply provides the charge voltage and the inductor is pre-charged to enable continuous current through the MOSFET/FWD arrangement. The gate of the MOSFET is driven by a gate drive circuit comprising of a voltage source, a pulse generator and an optocoupler chip jointly supplying 18 V through the gate resistor for a period of 20 μs. Details of this can be found in Appendix E.

4.4.2 Development of the Model

The dependence of the turn-on dI_{DS}/dt on temperature can be accounted for using the fundamental device equations as was derived in Equation 4.23 and 4.28. The MOSFET and the diode share the same total inductor current, hence, the turn-on of the MOSFET and turn-off of the diode occurs within the same switching transient. Equation 4.29a is the gate charging transient characteristic during turn-on (Equation 4.29b is for turn-off); we have:

$$V_{GS} = V_{GG}\left(1 - exp\left(-\frac{t}{R_G C_{iss}}\right)\right) \tag{4.29a}$$

$$V_{GS} = V_{GG}\, exp\left(-\frac{t}{R_G C_{iss}}\right) \tag{4.29b}$$

The rate of change of V_{GS} with time (dV_{GS}/dt) is evaluated simply by taking the derivative of 4.29a with time for turn-on and 4.29b for turn-off which results in:

$$\left.\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}\right|_{ON} = \frac{V_{GG}}{R_G C_{iss}} exp\left(-\frac{t}{R_G C_{iss}}\right) \tag{4.30a}$$

$$\left.\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}\right|_{OFF} = -\frac{V_{GG}}{R_G C_{iss}} exp\left(-\frac{t}{R_G C_{iss}}\right) \tag{4.30b}$$

Additionally, Equation 4.31 is the well-known equation for the drain current of a fully inverted MOSFET in pinch-off. This was proved earlier in Equations 2.33 to 2.40 of section 2.2.4.2 of chapter 2 as:

$$I_{DS} = \frac{B}{2}\left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS}\right) \tag{4.31}$$

However, since a long channel device is considered, the Channel Length Modulation Factor (with similar impact of the so-called Early Effect in bipolar devices) is negligible and Equation 4.31 can be simplified to:

$$I_{DS} = \frac{B}{2}\left(V_{GS} - V_{TH}\right)^2 \tag{4.32}$$

where

$$B = \frac{W \mu C_{ox}}{L}$$

in which the V_{TH} is the threshold voltage, W is the width of the device, μ is the effective mobility of the carriers, C_{ox} is the effective capacitance density of the gate insulator and L is the channel length of the device. Taking the derivative of 4.32 with respect to time

results in:

$$\frac{\mathrm{d}I_{DS}}{\mathrm{d}t} = B\left(V_{GS} - V_{TH}\right)\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}$$

and substituting dV_{GS}/dt yields dI_{DS}/dt as in 4.33a for turn-on and 4.33b for turn-off:

$$\left.\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\right|_{ON} = B\left(V_{GS} - V_{TH}\right)\frac{V_{GG}}{R_G C_{iss}}\,exp(\frac{-t}{R_G C_{iss}}) \tag{4.33a}$$

$$\left.\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\right|_{OFF} = B\left(V_{GS} - V_{TH}\right)\frac{-V_{GG}}{R_G C_{iss}}\,exp(\frac{-t}{R_G C_{iss}}) \tag{4.33b}$$

where the threshold voltage (V_{TH}) and the plateau voltage (V_{GP}) are given by [5] as:

$$V_{TH} = V_{FB} + \frac{2KT}{q}\,ln(\frac{N_A}{n_i}) + \frac{\sqrt{4\epsilon_{si}KTN_A ln(\frac{N_A}{n_i})}}{C_{ox}} \tag{4.34a}$$

$$V_{GP} = V_{TH} + \frac{I_D}{g_{fs}} \tag{4.34b}$$

As the ambient temperature of the MOSFET increases, the bandgap of the semiconductor becomes narrower thereby increasing the number of electrons that can attain sufficient thermal energy to move across the bandgap of the semiconductor. Hence, this increases the electron concentration in the conduction band and causes a current to start flowing across the device at lower levels of channel inversion thereby resulting in a smaller threshold voltage. Devices datasheet are used to determine the values of the equations parameters.

Equations 4.33a and 4.33b predict that dI_{DS}/dt will increase with temperature during turn-on and decrease with temperature during turn-off which can be physically explained by the negative temperature coefficient of the threshold voltage which means that MOSFET turn-on occurs sooner at higher temperatures. On the other hand, at turn-off, the V_{GS} (which is at V_{GG}) will take a longer time to reach the reduced value of V_{TH} and

hence the dI_{DS}/dt at turn-off is decreased. This temperature dependency will be seen in Figure 4.35 for turn-on and Figure 4.37 for turn-off following the same trends. Also the experimental measurements of dI_{DS}/dt in Figure 4.30 for turn-on and Figure 4.31 for turn-off agree with the trends predicted by Equations 4.33a and 4.33b where by increasing the R_G, the dI_{DS}/dt is reduced. In these figures, the ambient temperature is 25 °C and the calculations are done from the measurements presented in Figure 3.10 and Figure 3.11.

Figure 4.30 shows measurements and calculations of the turn-on dI_{DS}/dt as a function of R_G for the SiC MOSFETs derived from Figure 3.10. The calculations are based on values taken from the SCH2080KE datasheet with C_{iss} = 2nF, the threshold voltage at 25 °C is 5 V and B ranges from 0.5 to 1. The values of t used in the calculations in 4.33a and 4.33b correspond to the switching time value at which dI_{DS}/dt is calculated and V_{GS} is calculated from the equation of the plateau voltage (V_{GP}). The plateau voltage is calculated using the standard equation of 4.34b from [5] and it is assumed that the current switches between the time taken for V_{GS} to rise from V_{TH} to V_{GP} during turn-on and fall from V_{GP} to V_{TH} during turn-off. The measurements and calculations show good agreement over the wide range of R_G as can be seen in Figure 4.30.

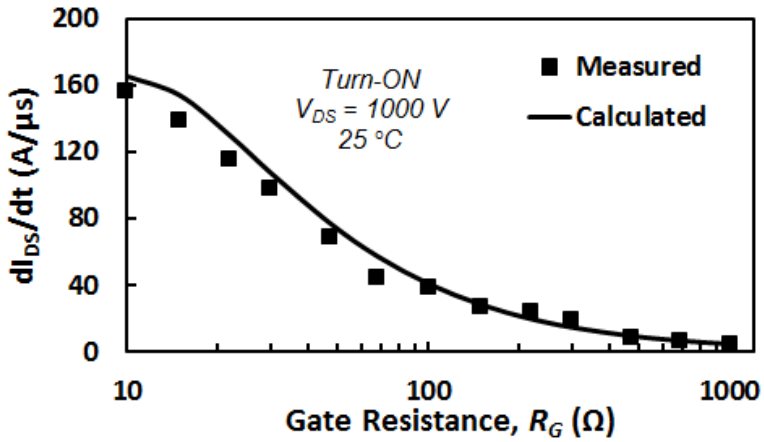


Figure 4.30: Turn-on dI_{DS}/dt as a function of R_G for measurements at 25 °C.

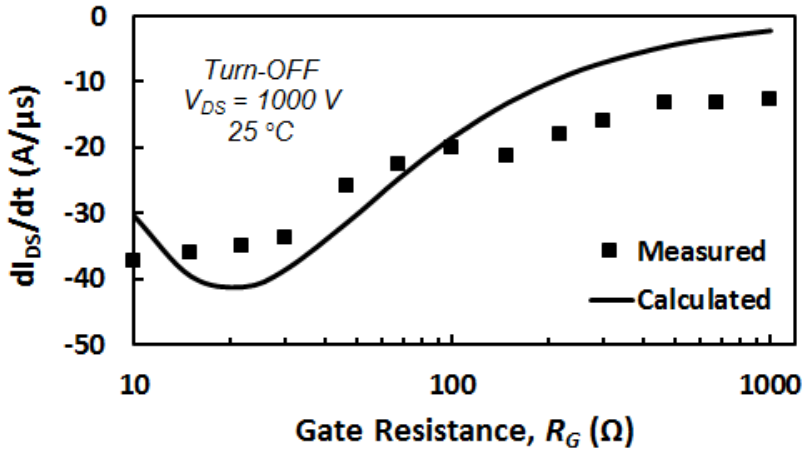


Figure 4.31: Turn-off dI_{DS}/dt as a function of R_G for measurements at 25 °C.

Figure 4.31 shows the measurements and calculations of dI_{DS}/dt as a function of R_G during turn-off. There is reasonably good agreement between the measured and calculated trends however, there is some measurement noise which introduces some error. The rate of change of dI_{DS}/dt with respect to R_G can be evaluated by taking the derivative of 4.33a with respect to the R_G. This derivative is shown in Equation 4.35 below for the turn-on. In the case of the turn-off, 4.35 is simply multiplied by –1.

$$\frac{\mathrm{d}^2 I_{DS}}{\mathrm{d}t\mathrm{d}R_G} = B\left(V_{TH} - V_{GS}\right)\frac{V_{GG}}{R_G^2\, C_{iss}} exp\left(-\frac{t}{R_G C_{iss}}\right)\left(\frac{t}{R_G C_{iss}} - 1\right) \tag{4.35}$$

The dependence of $d^2I_{DS}/dtdR_G$ on R_G can be observed by plotting the former as a function of the latter which is shown for the measurements and calculations in Figure 4.32 for turn-on and Figure 4.33 for turn-off; showing how the incremental increase of R_G impacts the dI_{DS}/dt. Similarly, in this case there is good agreement between the experimental measurements and calculations for turn-on based on Equation 4.35 in Figure 4.32. In Figure 4.33, there is some disparity at low R_G as a result of the error seen in Figure 4.31.

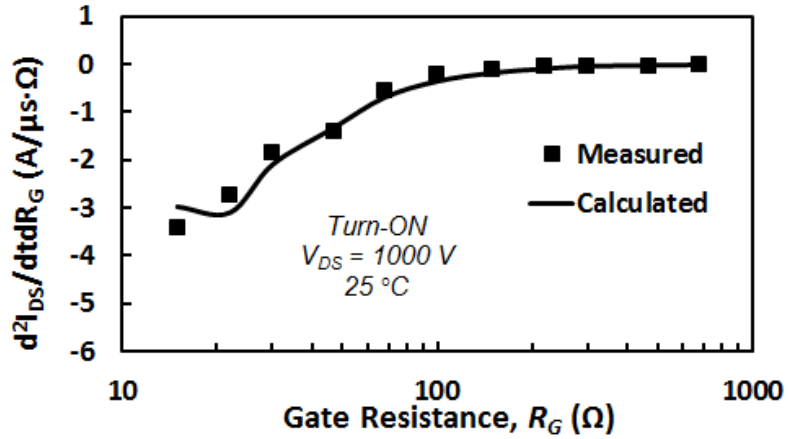


Figure 4.32: Turn-on $d^2I_{DS}/dtdR_G$ as a function of R_G for measurements at 25 °C.

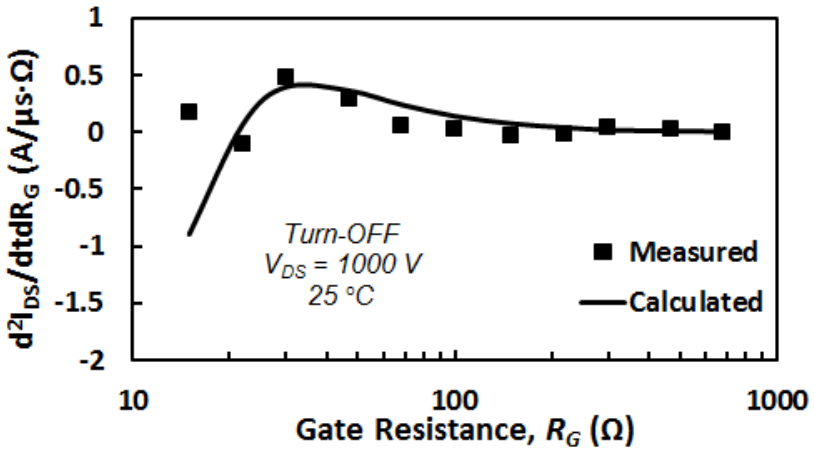


Figure 4.33: Turn-off $d^2I_{DS}/dtdR_G$ as a function of R_G for measurements at 25 °C.

The temperature dependence of dI_{DS}/dt can be evaluated by taking the derivative of 4.33a with respect to temperature noting that V_{TH} is temperature dependent through the intrinsic carrier concentration as shown in 4.34a and B is temperature dependent through the effective mobility. For turn-on, the derivative of 4.33a with respect to temperature (T) is 4.36 below. For turn-off, 4.36 can simply be multiplied by –1.

$$\frac{\mathrm{d}^2 I_{DS}}{\mathrm{d}t\,\mathrm{d}T} = \frac{V_{GG}}{R_G\,C_{iss}}\,exp\left(-\frac{t}{R_G\,C_{iss}}\right)\left((V_{GS}-V_{TH})\,\frac{\mathrm{d}B}{\mathrm{d}T} - B\frac{\mathrm{d}V_{TH}}{\mathrm{d}T}\right) \tag{4.36}$$

According to 4.34a, V_{TH} reduces as n_i increases. Also at higher temperatures dB/dT is negative as a result of the temperature dependence of the effective mobility, i.e. phonon scattering induced mobility degradation reduces the effective mobility of the electrons in the MOSFET channel as the temperature is increased. Hence, at lower temperatures, the temperature dependency of the threshold voltage dominates the temperature dependency of the effective mobility and 4.36 can be re-written as:

$$\frac{\mathrm{d}^2 I_{DS}}{\mathrm{d}t\,\mathrm{d}T} = \frac{V_{GG}}{R_G\,C_{iss}}\,exp\left(-\frac{t}{R_G\,C_{iss}}\right)\left(B\left|\frac{\mathrm{d}V_{TH}}{\mathrm{d}T}\right|\right) \tag{4.37}$$

Because the overall sign of Equation 4.37 (which is the 2$^{\mathrm{nd}}$ order derivative of dI_{DS}/dt against temperature) is positive, this means that the switching rate (dI_{DS}/dt) during MOSFET turn-on increases with increasing temperature as has already been demonstrated experimentally in Figure 4.34 and Figure 4.43. In case of turn-off, Equation 4.37 is multiplied by –1, meaning that the switching rate (dI_{DS}/dt) decreases with increasing temperature during MOSFET turn-off. This also matches the measurements.

Figure 4.34 shows the measured turn-on dI_{DS}/dt as a function of R_G for different temperatures whereas Figure 4.35 shows the measured turn-on dI_{DS}/dt as a function of temperature for different gate resistances on a logarithmic basis. It can be seen from Figure 4.34 and 4.35 that dI_{DS}/dt increases with temperature during turn-on in agreement with 4.36 and 4.37; however, the rate of change of dI_{DS}/dt with temperature is not uniform for all gate resistances. This trend can also be observed in other published reports on the performance of SiC MOSFETs at different temperatures where dI_{DS}/dt can be seen to increase with temperature during turn-on [79] or $|dV_{DS}/dt|$ (meaning the absolute value, i.e. the magnitude of dV_{DS}/dt) is shown to increase with temperature at turn-on [80].

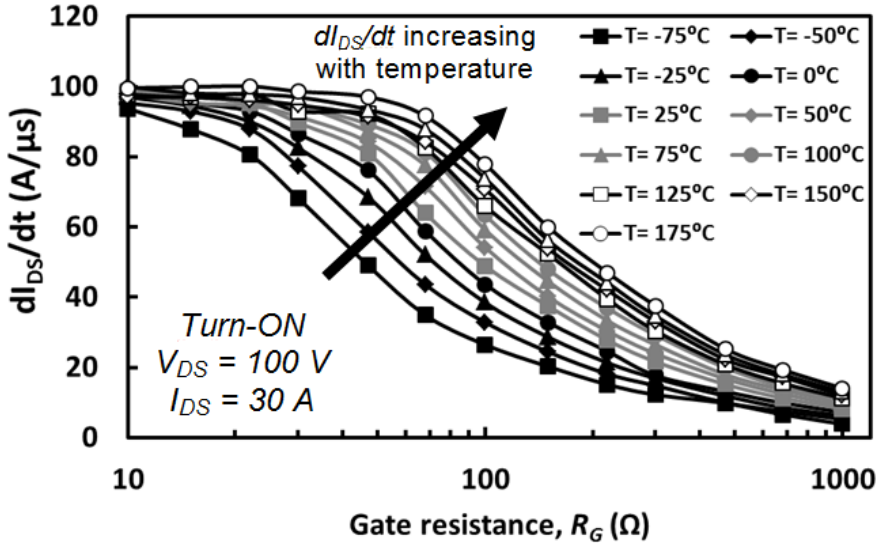


Figure 4.34: Measured dI_{DS}/dt as a function of R_G at different temperatures in turn-on.

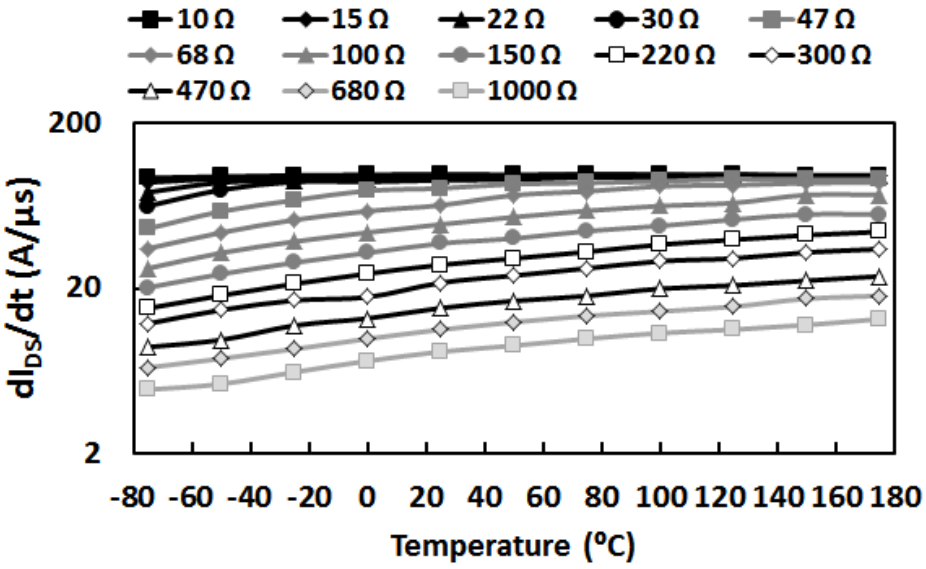


Figure 4.35: Measured dI_{DS}/dt as a function of temperature for different R_G in turn-on.

Figure 4.36 also shows the turn-off $|dI_{DS}/dt|$ (meaning the absolute value, i.e. the magnitude of dI_{DS}/dt) as a function of R_G for different temperatures where it can be seen that dI_{DS}/dt decreases with increasing temperature as predicted by Equation 4.36 and 4.37. Figure 4.37 also shows the turn-off dI_{DS}/dt as a function of temperature for

different R_G, where the same trend is also clear. Similar to Figure 4.35, this figure is also scaled on a logarithmic basis, to provide a better view over the trend of the dI_{DS}/dt with temperature in high R_G (low switching rates) in contrast with Figure 4.36 where the temperature dependency trend is more clear in low R_G (high switching rates).

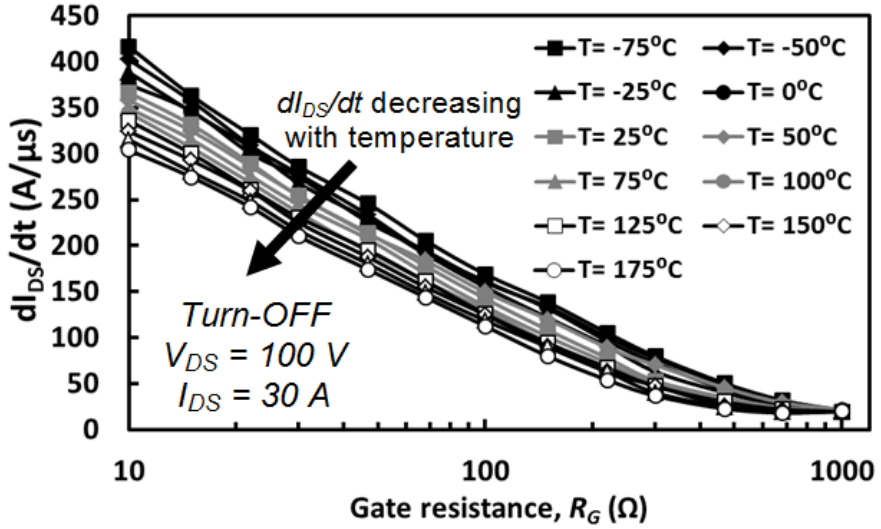


Figure 4.36: Measured dI_{DS}/dt as a function of R_G at different temperatures in turn-off.

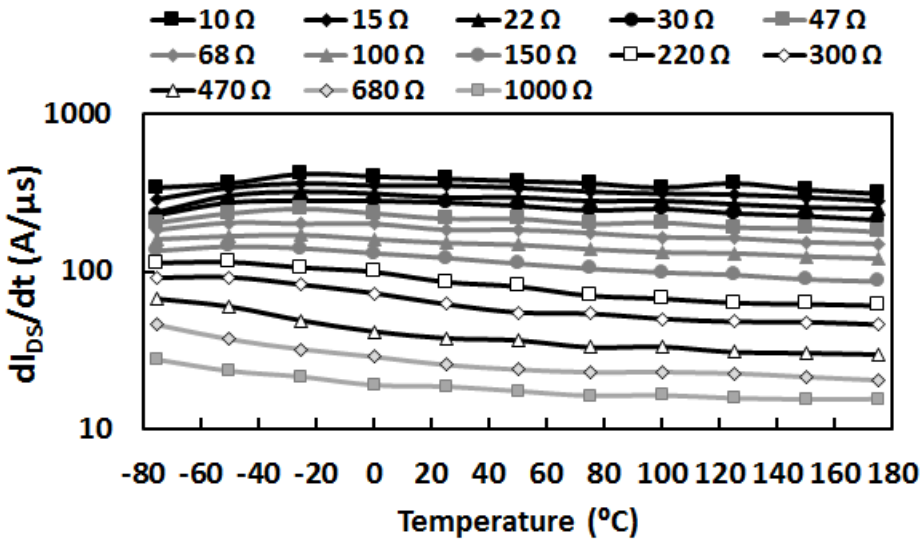


Figure 4.37: Measured dI_{DS}/dt as a function of temperature for different R_G in turn-off.

The dependence of $d^2I_{DS}/dtdT$ on R_G can be further considered by looking at how the former changes with respect to the latter. In this regard, Figure 4.38 shows experimental measurements of the turn-on $d^2I_{DS}/dtdT$ as a function of R_G for the different ambient temperatures. It can be seen from the measurements in Figure 4.38 that the variation of dI_{DS}/dt with temperature is small at larger and smaller values of R_G ($d^2I_{DS}/dtdT$ is small) and is much larger at intermediate values of R_G ($d^2I_{DS}/dtdT$ is larger), i.e. $d^2I_{DS}/dtdT$ as a function of R_G exhibits a bell shaped characteristic. Figure 4.39 shows the calculated $d^2I_{DS}/dtdT$ as a function of R_G at different temperatures using 4.37 where the same bell shaped characteristic can be observed at different temperatures. It can also be seen from Figure 4.38 that the maximum turn-on $d^2I_{DS}/dtdT$ decreases as temperature increases. Equations 4.36 and 4.37 explain this behavior where it can be seen that as R_G is reduced, V_{GG}/R_GC_{iss} rises and $exp(-t/R_GC_{iss})$ reduces. Hence, a plot of $d^2I_{DS}/dtdT$ as a function of R_G will show a bell shaped characteristic as a result of the competing effects. This is seen in Figure 4.34 as well; where change of dI_{DS}/dt with respect to temperature is more pronounced in intermediate R_G.

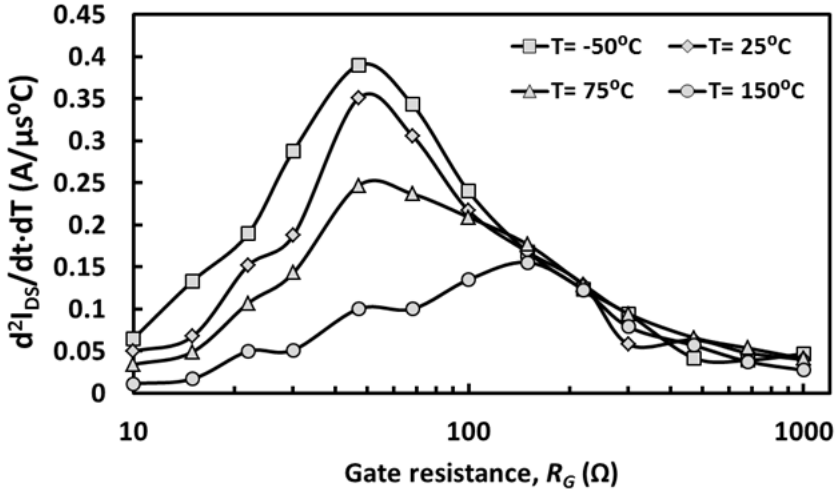


Figure 4.38: Measured turn-on $d^2I_{DS}/dtdT$ as function of R_G at different temperatures.

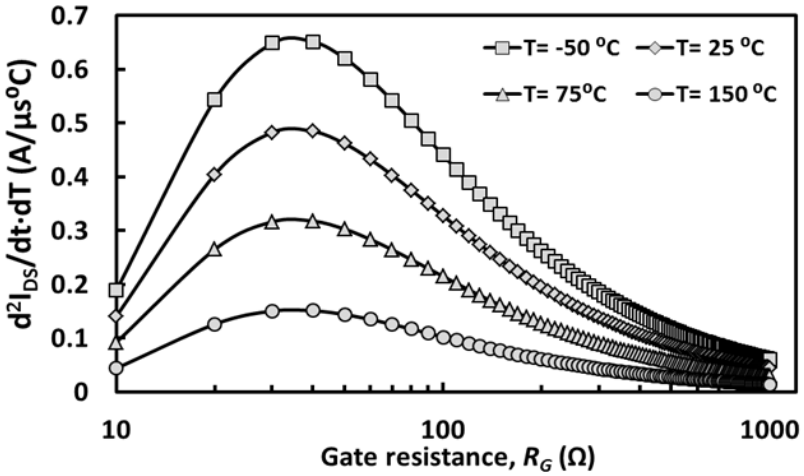


Figure 4.39: Calculated turn-on $d^2I_{DS}/dtdT$ as function of R_G at different temperatures.

4.4.3 Diode Switching Analysis

The response of the diode output voltage characteristics to the MOSFET switching is determined primarily by the transfer function of the switching diode, the gate resistance of the gate driver and the junction temperature of the device. The transfer function of the diode can be determined by the equivalent circuit of the diode [81] which is represented by a series parasitic resistance (R_S), diode depletion capacitance (C_{AK}), diode depletion resistance (R_{AK}) and the overall stray inductance (L_{Stray}) as shown in Figure 4.40. The parasitic capacitance arises from the depletion capacitance of the diode due to the voltage dependent depletion width (between the Schottky metal and the voltage blocking semiconductor) at turn-off, the series resistance arises from the resistance of the circuit wiring and packaging as well as the resistance of the drift region of the device during switching and the stray inductance arises from the packaging and wiring of the circuit.

The depletion capacitance is significantly voltage dependant since it decreases as the voltage across the diode increases. The corresponding depletion resistance is also due to the finite resistance of the depletion width, i.e. the depletion capacitance is modeled as a

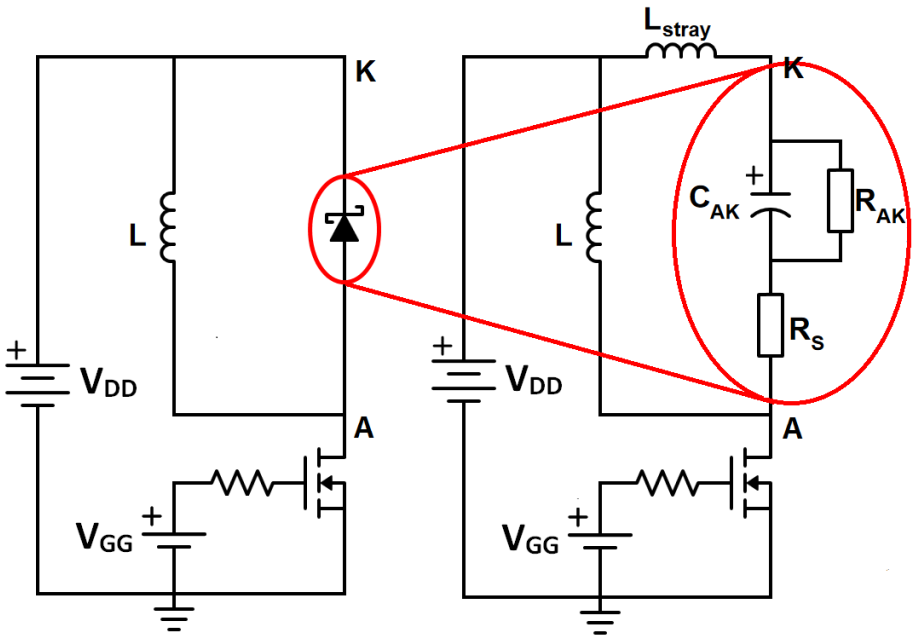


Figure 4.40: Circuit schematic of the experimental test rig showing the equivalent circuit of the SBD.

lossy capacitor (there is a non-zero conductance). This is due to pre-breakdown avalanche multiplication caused by free carriers under the influence of the increasing electric field and by thermionic emission across the Schottky interface and acts as the leakage current during the diode blocking state. The highest depletion capacitance across the diode is formed when the voltage across it is at a minimum, i.e. at the instant that reverse voltage starts increasing. As this capacitance varies with the voltage across the diode through the depletion width, the value of C_{AK} as shown in Figure 4.40 is considered as an average capacitance over a wide voltage range. This average junction capacitance is used to determine the behaviour of the devices [55, 82, 83]. The diode depletion capacitance is normally measured by the Capacitance-Voltage (CV) curves and is often provided on the device datasheet. For the case of the device in the measurements of this section, the device datasheet has provided the depletion capacitance as shown in Figure 4.41. As seen,

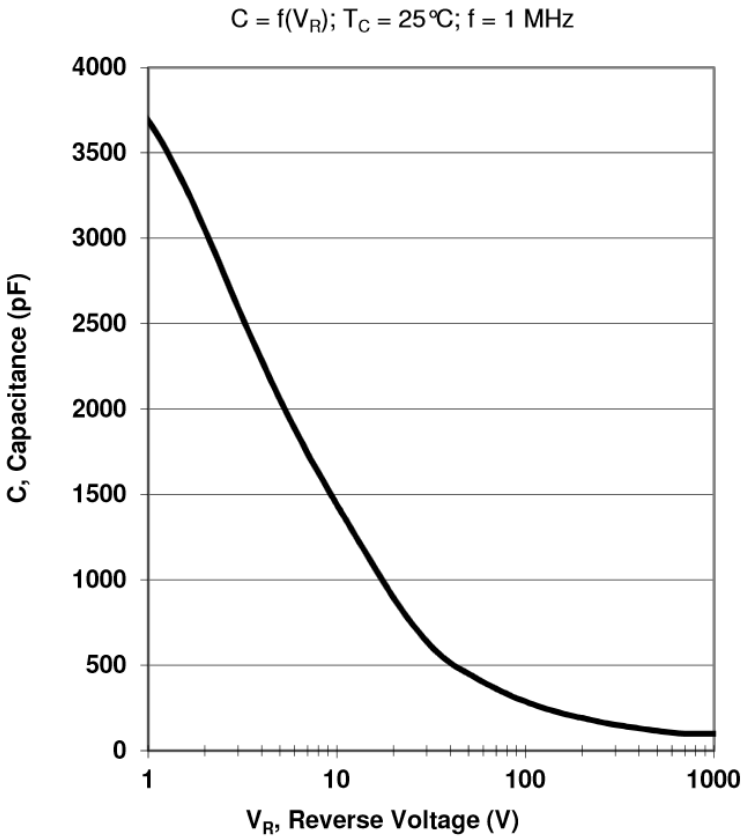


Figure 4.41: Typical Depletion Capacitance of the SiC SBD, varying with voltage. The plot is the result of CV measurements based on the datasheet in Appendix F.

the value of diode changes significantly. For the sake of the modeling requirements of this section, the value of the capacitance at the nominal input voltage (100 V) is chosen as the median value which is approximately 250 pF. This is significantly higher than that of PiN diodes. The diode ringing is very significant in turn-off compared to turn-on. One reason for this is the fact that that instant of turn-off the voltage across the diode is still low due toe the conduction phase and hence, the depletion capacitance is significant.

The diode equivalent circuit has been modeled in a circuit simulator (Multisim 12.0) using these parameters to provide a matching diode characteristics for the experiments, where other parameters (such as stray inductance) are varied within reasonable margins

to obtain agreement between the model and the measurements. It should be noted that the behaviour of diode, including its ringing frequency at turn-off, as will be seen in the next section, depends strongly on the parasitic inductances which are unique for a power module and experimental rig. However, the equivalent circuit shown in Figure 4.40 is universal for power converters. The diode voltage (V_{AK}) can be calculated as the product of the diode transfer function and an input function that represents the switching of the MOSFET as:

$$
\begin{aligned}
H(s) &= \frac{Output\ Voltage}{Input\ Voltage} \\
&= \frac{R_S + R_{AK} \parallel \dfrac{1}{sC_{AK}}}{R_{AK} \parallel \dfrac{1}{sC_{AK}} + R_S + sL_{Stray}} \\
&= \frac{R_S + \dfrac{R_{AK}}{sR_{AK}C_{AK}+1}}{\dfrac{R_{AK}}{sR_{AK}C_{AK}+1} + R_S + sL_{Stray}} \\
&= \frac{R_S(sR_{AK}C_{AK}+1) + R_{AK}}{R_S(sR_{AK}C_{AK}+1) + R_{AK} + sL_{Stray}(sR_{AK}C_{AK}+1)} \\
&= \frac{sR_SR_{AK}C_{AK} + R_S + R_{AK}}{s^2R_{AK}C_{AK}L_{Stray} + sL_{Stray} + R_{AK} + sR_SR_{AK}C_{AK} + R_S} \\
&= \frac{\dfrac{sR_SR_{AK}C_{AK} + R_S + R_{AK}}{R_{AK}C_{AK}L_{Stray}}}{s^2 + \dfrac{s(R_SR_{AK}C_{AK} + L_{Stray})}{R_{AK}C_{AK}L_{Stray}} + \dfrac{R_{AK} + R_S}{R_{AK}C_{AK}L_{Stray}}} \\
&= \frac{s\left(\dfrac{R_S}{L_{Stray}}\right) + \dfrac{R_{AK} + R_S}{R_{AK}C_{AK}L_{stray}}}{s^2 + s\left(\dfrac{R_{AK}R_SC_{AK} + L_{stray}}{R_{AK}C_{AK}L_{stray}}\right) + \dfrac{R_{AK} + R_S}{R_{AK}C_{AK}L_{stray}}}
\end{aligned}
$$

Therefore, this transfer function can be represented by the equation shown below:

$$\begin{aligned} V_{AK} &= \frac{V_{DD}}{1+sR_GC_{GD}} \cdot H(s) \\ &= \frac{V_{DD}}{1+sR_GC_{GD}} \times \frac{s\left(\frac{R_S}{L_{Stray}}\right) + \frac{R_{AK}+R_S}{L_{stray}R_{AK}C_{AK}}}{s^2 + s\left(\frac{R_{AK}R_SC_{AK}+L_{stray}}{L_{stray}R_{AK}C_{AK}}\right) + \frac{R_{AK}+R_S}{L_{stray}R_{AK}C_{AK}}} \end{aligned} \tag{4.38}$$

As the MOSFET turns-on, the majority of the supply voltage (V_{DD} in Figure 4.40) which initially was across the MOSFET now falls across the diode; thereby reverse biasing the diode. Hence, the switching of this voltage across the diode can be modeled as an input into the transfer function of the diode. The action of the MOSFET, does not appear across the diode as a step function (instantaneously). Rather, it is considered to be identical to an exponential voltage rise where the rate of change of voltage with time depends on the MOSFET switching time constant (R_GC_{GD}). The product R_GC_{GD} is approximately the time required for the Miller capacitance of the MOSFET to charge during the plateau stage of the gate voltage transient at turn-on as was shown in Figure 4.28. Similar to the diode's depletion capacitance, the Miller capacitance of the MOSFET also changes with the voltage during the diode turn-off transient; therefore C_{GD} in 4.38 also represents an average value of the variable Miller capacitance [82]. The Miller capacitance is charged when the drain voltage (V_{DD}) across the low side MOSFET falls from the supply voltage to the on-state voltage (as its value increase as the voltage is lowered) and the voltage across the diode rises from the on-state voltage drop to the input voltage.

The switching rate of the low side MOSFET (dI_{DS}/dt) is also the rate at which current is commutated away from the high side diode, hence, the rate at which the SBD is turned off. The transfer function of the diode is basically that of a second order circuit which can respond as over-damped, under-damped or critically damped depending on the

attenuation present. The diode output voltage is the product of the input voltage and the transfer function. The denominator of 4.38 is in form of:

$$s^2 + 2\alpha s + \omega^2 = 0$$

Therefore from the coefficients of the denominator in Equation 4.38, the attenuation or Neper frequency (α_V), the frequency of the oscillations (ω) and the damping factor (ζ) of SiC Schottky diode voltage can be derived as:

$$\alpha_V = \frac{R_{AK}R_S C_{AK} + L_{stray}}{2L_{stray}R_{AK}C_{AK}} \tag{4.39a}$$

$$\omega = \sqrt{\frac{R_{AK} + R_S}{L_{stray}R_{AK}C_{AK}}} \tag{4.39b}$$

$$\zeta = \frac{\alpha_V}{\omega} = \frac{R_S R_{AK} C_{AK} + L_{Stray}}{2\sqrt{R_{AK}L_{Stray}C_{AK}(R_S + R_{AK})}} \tag{4.39c}$$

Experimentally it is seen that the oscillation frequency of the diode current has approximately the same value as its voltage for all switching rates while its attenuation is approximately two times higher. The dI_{DS}/dt of the MOSFET at turn-on will determine the nature of the diode response since the same current flows through both devices. Hence, the diode response will depend on the gate resistance and the temperature. Figure 4.42 and 4.43 show the MOSFET turn-on current transient at different temperatures for R_G = 15 Ω in Figure 4.42 and R_G = 150 Ω in Figure 4.43, respectively.

From these figures, it can be seen that the dI_{DS}/dt is more temperature invariant at R_G = 15 Ω than at R_G = 150 Ω; i.e. $d^2I_{DS}/dtdT$ is larger at R_G = 150 Ω in agreement with Figure 4.38 and Equation 4.36. It can also be seen from Figure 4.43 that the turn-on dI_{DS}/dt increases with temperature in agreement with the equations developed previously.

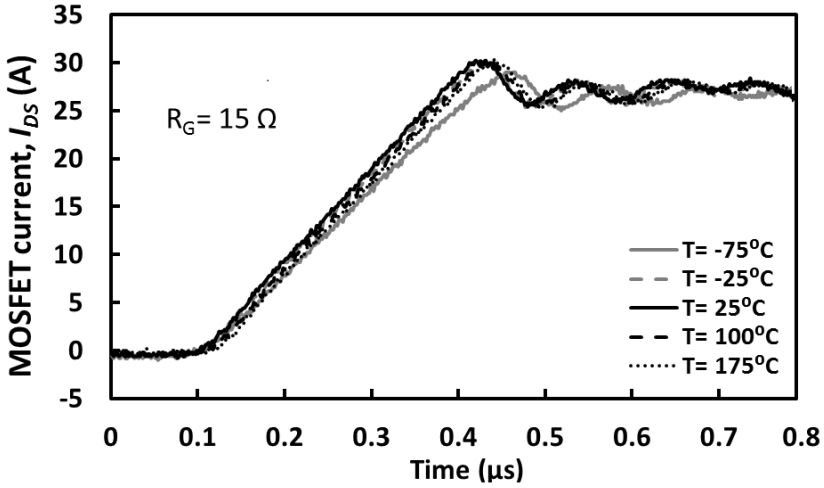


Figure 4.42: MOSFET drain current as a function of time during turn-on at different temperatures with $R_G = 15\ \Omega$.

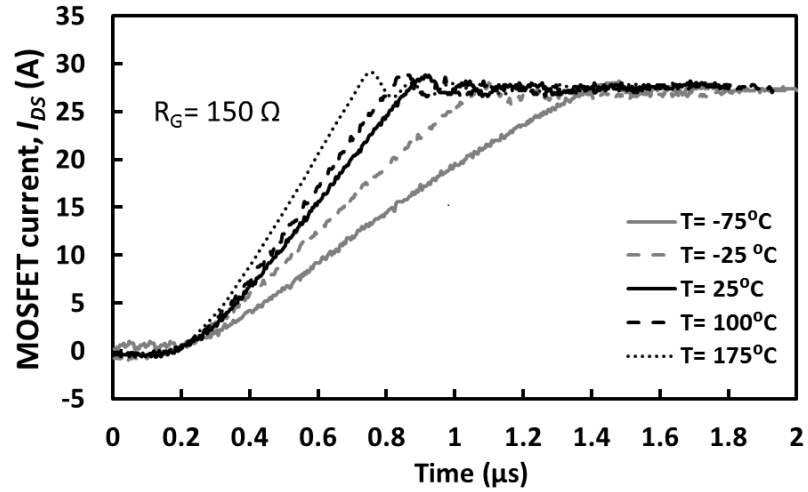


Figure 4.43: MOSFET drain current as a function of time during turn-on at different temperatures with $R_G = 150\ \Omega$.

As can be seen, the increased temperature results in reduction of the transient duration, while it increases the overshoot peak; which are two competing effects in determining switching energy. Figure 4.44 and 4.45 show the diode voltage response at $R_G = 15\ \Omega$ and $R_G = 150\ \Omega$, respectively. The most obvious difference is the higher V_{AK} variation with temperature exhibited by the $R_G = 150\ \Omega$ measurements, i.e. the $R_G = 15\ \Omega$ mea-

surements show less dependence of diode voltage on temperature. The diode peak V_{AK} overshoot increases with temperature and the ringing develops with higher values of overshoot at higher temperatures. This is due to the increase of MOSFET's turn-on dI_{DS}/dt with temperature, so the current commutates away from the diode at a faster rate.

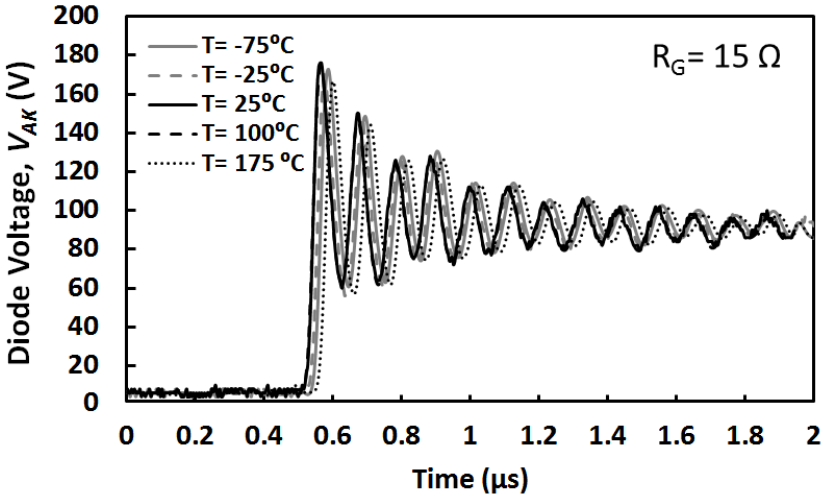


Figure 4.44: Measured diode output voltage as a function of time during MOSFET turn-on at different temperatures with $R_G = 15\ \Omega$.

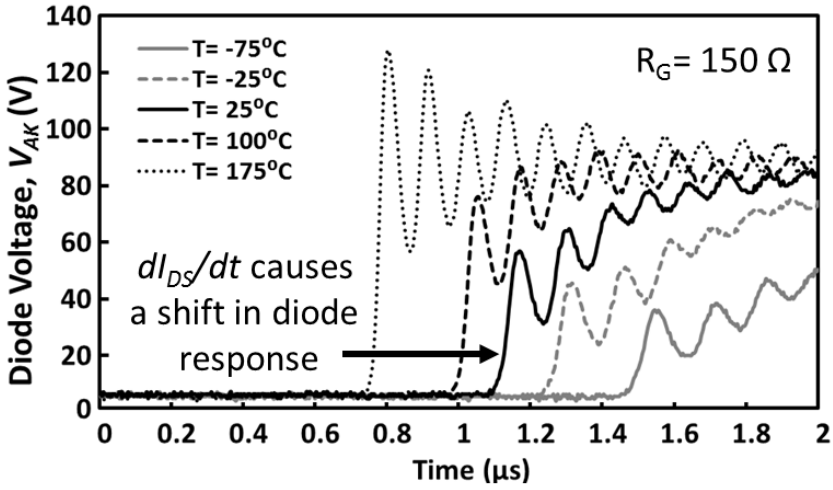


Figure 4.45: Measured diode output voltage as a function of time during MOSFET turn-on at different temperatures with $R_G = 150\ \Omega$.

The dependence of the current commutation rate on temperature results in the ringing of the diode to also become a temperature dependent parameter. This is because the diode responds to the dI_{DS}/dt of the MOSFET. Previous publications have argued that the turn-off characteristics of the SiC Schottky diode is temperature invariant [84]; however, this is only the case in commonly used low gate resistances (high switching rates) as in Figure 4.44. At slower switching rates (larger gate resistances), the dependence of dI_{DS}/dt on temperature affects the diode temperature characteristics as shown in Figure 4.45. In other words, the rate at which the transistor switches will determine the response of the diode to the discharge of the free-wheeling current. If the diode is discharged very rapidly (high dI_{DS}/dt from low R_G), then the diode will ring with higher overshoots and the circuit is excited by a larger $|dV/dt|$) compared to when the current is discharged more slowly. The temperature dependence of the diode response increases as the switching rate is reduced as seen in Figure 4.34. Figure 4.42 and Figure 4.43 can be explained by the fact that $d^2I_{DS}/dtdT$ is higher at intermediate R_G values and reduces as R_G is reduced. This follows the same bell-shaped trend which was seen previously in Figure 4.38.

Also, as can be noticed in Figure 4.45, the dI_{DS}/dt dependence on temperature causes a time shift in the diode response with the high temperature V_{AK} occurring faster. This is due to the negative temperature coefficient of the MOSFETs threshold voltage which means that switching time is delayed at low temperatures (because of the higher V_{TH} at lower temperatures). Hence, the MOSFET switches slower as seen in Figure 4.43 thereby taking a longer time for the voltage to transfer from the MOSFET to the diode (in other words, looking at Figure 4.28, time t_2 and consequently the voltage drop are delayed). Additionally, it can be seen from these figures that the peak voltage overshoots of the oscillations for the 15 Ω measurements is higher and the temperature dependence is less compared to the oscillations at 150 Ω gate resistance. It should be noted that, as seen in

Figure 4.44 and Figure 4.45, although temperature has a considerable impact on the level of output overshoot of the device, its influence on the damping and natural frequency of oscillations is significantly less as these parameters are defined by the values of parasitic elements of the device and circuit, which have minimal temperature-dependent properties. Figure 4.46(a) and 4.46(b) show the modeled ringing characteristics of the diode output voltage switched at 2 different rates using median values for the parasitic elements in the device and the circuit. In Figure 4.46(a), the low side SiC MOSFET is switched with a 15 Ω gate resistor (for high switching rates) whereas in Figure 4.46(b), the low side MOSFET is switched with 68 Ω (this R_G is chosen as it was in the peak proximity of Figure 4.38). It can be seen from Figure 4.46 that there is reasonably good matching between the measured and modeled characteristics. Figure 4.46 shows, as expected, that the peak voltage overshoot during turn-off increases with the increase in switching rate (i.e. a higher $L{\cdot}dI_{DS}/dt$) and the damping is less when the switching rate is higher.

As in 4.33a, the switching rate decreases as the switching time increases. At the point of maximum dI_{DS}/dt, 4.33a can be re-written (assuming that t is small enough with respect to $R_G C_{iss}$ for the exponential to be unity) in terms of R_G in 4.40 as:

$$R_G = \frac{B\left(V_{GS} - V_{TH}\right) V_{GG}}{C_{iss}\left(\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\right)} \tag{4.40}$$

To understand the dependence of diode's V_{AK} and MOSFET's dI_{DS}/dt, Equations 4.38 and 4.33a are combined yielding:

$$V_{AK} = A \ \times \frac{s\left(\frac{R_S}{L_{Stray}}\right) + \frac{R_{AK}+R_S}{L_{stray}R_{AK}C_{AK}}}{s^2 + s\left(\frac{R_{AK}R_S C_{AK} + L_{stray}}{L_{stray}R_{AK}C_{AK}}\right) + \frac{R_{AK}+R_S}{L_{stray}R_{AK}C_{AK}}} \tag{4.41}$$

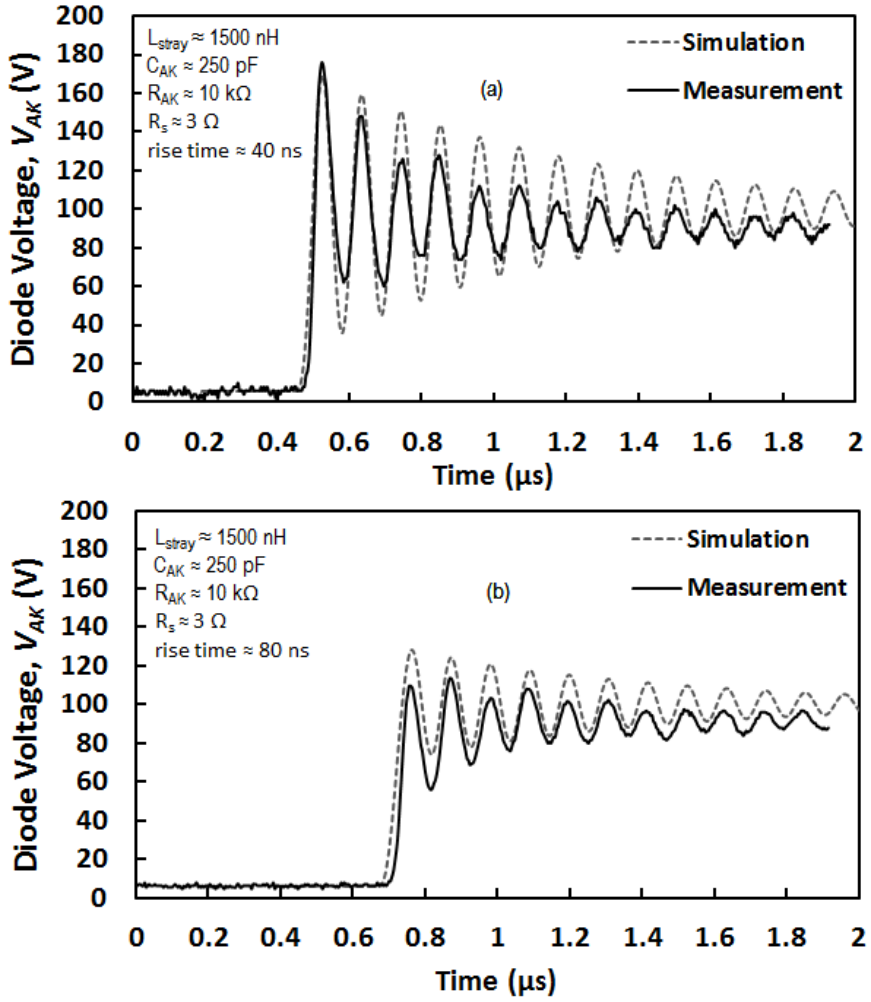


Figure 4.46: Measured and modeled voltage at turn-off of SiC Schottky diode where switching speeds are modulated by (a) $R_G = 15\ \Omega$ and (b) $R_G = 68\ \Omega$.

where

$$A = \frac{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \cdot V_{DD}}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t} + s\left(\frac{BV_{GG}\left(V_{GS} - V_{TH}\right)}{C_{iss}} \cdot C_{GD}\right)}$$

Equation 4.41 is very useful because it relates the turn-on dI_{DS}/dt of the MOSFET to the diode output voltage which as seen in measurements directly influences the severity

of its ringing. It will be instrumental in the development of the switching energy model for the SiC SBD as it is needed to determine the characteristics of the oscillations.

Figures 4.47 shows the simulated plot of Equation 4.41 using dI_{DS}/dt values similar to what was measured (between 10 and 100 A/μs). The effect of R_S and R_{AK} is to dampen the oscillations, while C_{AK} and L_{stray} affect the oscillation frequency. Figures 4.47 is a reasonably accurate simulation of the diode's switching behavior, however, because all of these parasitic components vary during switching and are difficult to measure, an exact replica of the experimental measurements is difficult to achieve. Figures 4.47 also shows that increasing turn-on dI_{DS}/dt (which can result from either a lower gate resistance or higher ambient temperature) causes higher V_{AK} peak overshoots and more diode ringing.

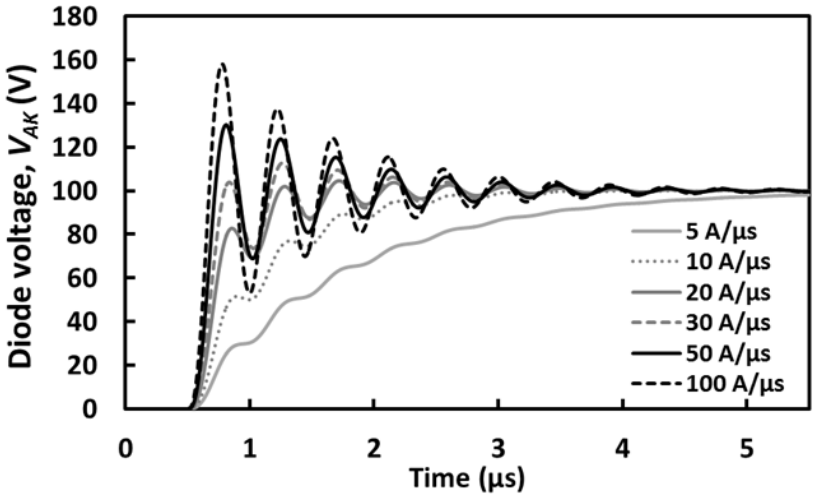


Figure 4.47: Calculated diode output voltage as a function of time during MOSFET turn-on at different dI_{DS}/dt.

Figures 3.28 and 3.34 have shown the measured switching energy at turn-on and turn-off for the SiC Schottky diode at different dI_{DS}/dt and temperatures. It should be reminded that the dI_{DS}/dt shown in these figures is calculated at 25 °C and is provided as a sample rate to provide a comparable value for each gate resistance. It can be seen

from these figures that the diode turn-off energy is larger than the turn-on energy, which is due to the ringing exhibited in the transients. It can also be seen from Figure 3.34 that for a given dI_{DS}/dt (or gate resistance), the switching energy reduces with increasing temperature during diode turn-off. This is due to the fact that MOSFET switching rates increase with temperature as shown in Figure 4.34 and the response of the diode is determined by the switching of the MOSFET as shown in Equation 4.41. Figures 3.28 and 3.34 show that the dependence of the switching energy on the gate resistance exhibits a U-shaped characteristic with the lowest switching energies at intermediate R_G values. At the lowest R_G, the switching energy is dominated by additional losses from diode ringing, whereas at the highest R_G, the switching energy is due to the prolonged transient. Hence, although using small gate resistances increases the dI_{DS}/dt, the resulted ringing can increase the switching energy. The next section in this chapter addresses how to model the switching energy of SiC Schottky diodes taking the ringing into account.

4.4.4 Modeling of Switching Energy of SiC SBD

The models that have previously been developed to understand the transient behavior of silicon PiN diodes during reverse recovery, including physics-based models [85], analytical models [86, 87], Saber Models [88] and SPICE Models [45] are not extendable to SiC Schottky diodes since the latter is unipolar [89] and therefore presents different switching characteristics. Also, models developed for parameter extraction in SiC Schottky diodes [90] provide valuable information on understanding the physics of the diodes; however, they lack the capability of modeling dynamic ringing and switching energy. In this section, using previously defined and validated equations, an analytical model for turn-off switching energy of Silicon Carbide Schottky barrier diodes is presented, eval-

uated and validated. The model is dedicated to the turn-off characteristics as it is the dominant contributor to the total switching energy compared to the turn-on. The model is shown to be able to accurately predict the switching energy of the SiC Schottky diodes over a wide range of temperatures and switching rates determined by the Silicon Carbide MOSFET acting as the low-side transistor as was shown previously. The next sections show details of development of the model and its validation.

4.4.4.1 Switching Energy Model

The expressions developed previously for diode output oscillation frequency - ω - (4.39a) and attenuation - α - (4.39b) will be used in the development of the diode switching energy model. In this regard, Figure 4.48(a) shows the experimental measurements of the diode current and voltage during turn-off overlapping with the low side SiC MOSFET switched with a gate resistance of 15 Ω. Figure 4.48(b) shows experimental measurements of the diode current and voltage when the low side SiC MOSFET is switched more slowly with a gate resistance of 150 Ω. When comparing Figure 4.48(a) and Figure 4.48(b), it can be seen that the ringing is dramatically reduced as the switching rate (dI_{DS}/dt) is reduced, however, simultaneously the switching duration of the current increased.

Figure 4.49(a) shows the switching power transient as a function of time for $R_G = 15\ \Omega$ whereas Figure 4.49(b) shows the same plot for $R_G = 150\ \Omega$. It is seen from Figure 4.49(a) that when the diode is switched with a higher MOSFET dI_{DS}/dt, the oscillations in the diode voltage causes additional power peaks beyond the main peak. These power peaks will significantly add to the switching energy of diode. In Figure 4.49(b) where the device is switched slower, the switching power transient does not contain such additional power peaks due to lack of overshoots, although the dissipated power associated with the switching current is higher as the transient is longer. In order to correctly model the

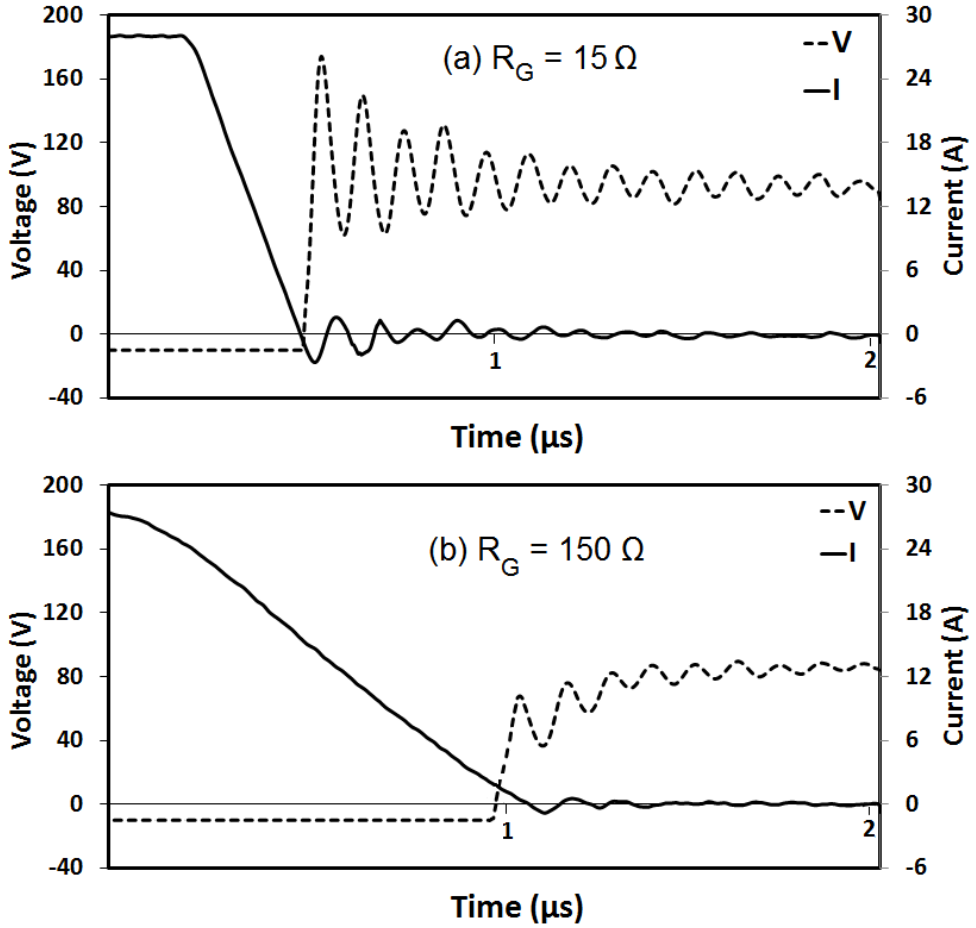


Figure 4.48: Current and voltage waveforms of SiC SBD at turn-off at 25 °C with (a) $R_G = 15\ \Omega$ and (b) $R_G = 150\ \Omega$.

switching energy of the diode, it is important to capture these peaks in the modeling and account for how the peaks change with the switching rate and temperature. The integration of these power peaks over time will yield the total switching energy.

Figure 4.50(a) shows measurements of the 15 Ω switching power transients at different temperatures showing that the switching energy is largely temperature invariant in Schottky diodes at high switching rates. Figure 4.50(b) also shows a similar plot for the $R_G = 150\ \Omega$ where more temperature dependency is seen.

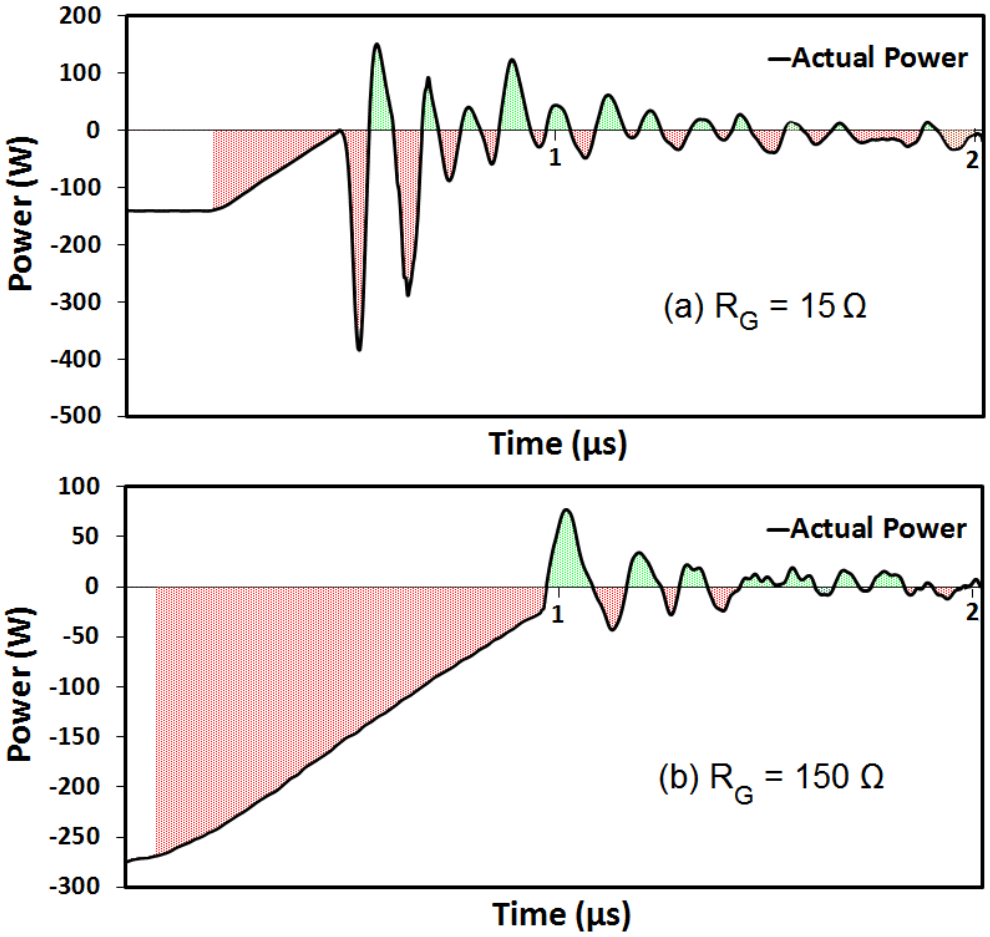


Figure 4.49: Comparison of waveforms of the transient power of SiC SBD with (a) $R_G = 15\ \Omega$ and (b) $R_G = 150\ \Omega$ at 25 °C.

The analytical model for the switching energy is based on approximating the waveforms by mathematical functions and equations and integrating these over the transient duration. Figure 4.51 shows these approximations for the current and voltage waveforms of the SiC SBD. The switching energy is divided into 3 sections namely the current switching phase, the voltage switching phase and the ringing phase. In section 1 (the current switching phase), between t_1 and t_2, the current is approximated as a linear function with a negative derivative while the diode voltage is constant at the on-state voltage drop.

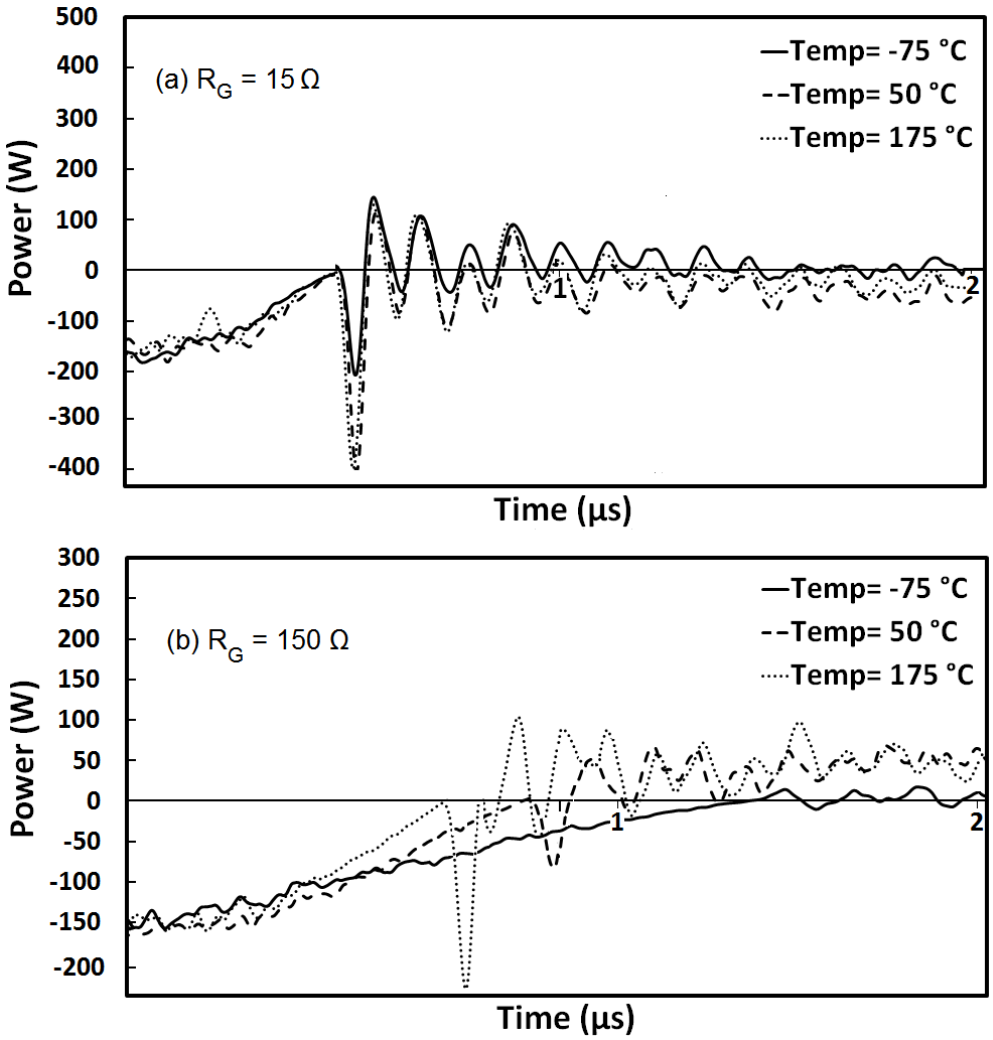


Figure 4.50: Measured transient power at different temperatures of SiC SBD with (a) $R_G = 15\ \Omega$ and (b) $R_G = 150\ \Omega$ (The difference in power transient in (b) with temperature is due to the time shift seen in Figure 4.45).

It is assumed that the current crosses zero with the same rate and at the same instant that the diode voltage starts to rise to charge the depletion capacitance. This is based on that fact that the low side MOSFET attains the load current at the instant that the Miller capacitance starts to charge and at this time the drain-source voltage across the MOSFET falls from the input voltage to the on-state voltage as was seen in Figure 4.28.

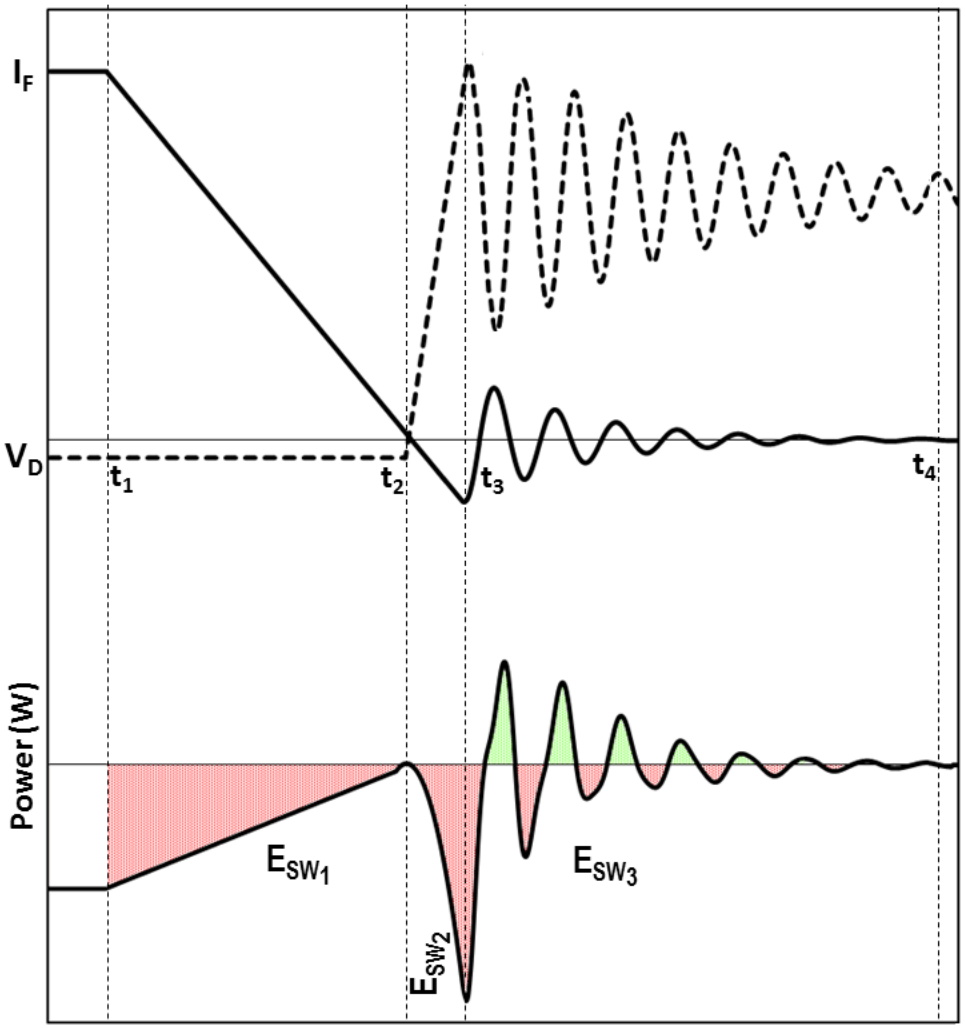


Figure 4.51: Switching power in the model is divided into 3 distinct sections.

The measured waveforms in Figure 4.48 show that this is indeed the case. The switching energy calculated for section 1, which is E_{SW1} (the current switching phase) is simply the integration of the switching power from t_1 (the initial point) to t_2.

$$E_{SW1} = \int_{t_1}^{t_2} \left(I_F - \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} t \right) \cdot V_d \, dt = \frac{V_d \cdot I_F^2}{2\dfrac{\mathrm{d}I_{DS}}{\mathrm{d}t}} \tag{4.42}$$

where

$$t_1 = 0 \quad and \quad t_2 = \frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} \quad and \quad t_3 = \frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}$$

In section 2 (the voltage switching phase), which spans from t_2 to t_3, the diode voltage is approximated as a linear function with a positive derivative that rises from the on-state voltage of the diode to the peak voltage which is the sum of the input voltage and the inductive overshoot. It is also assumed that the current through the diode reaches its peak negative value at the same instant having the same dI_{DS}/dt. The equation for the switching energy in the voltage switching phase (E_{SW2}) is simply the integration of the switching power from t_2 to t_3 which is shown as:

$$\begin{aligned} E_{SW2} &= \int_{t_2}^{t_3} \left(I_F - \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} t \right) \cdot \left(\frac{\mathrm{d}V_{AK}}{\mathrm{d}t} t - \frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} \frac{\mathrm{d}V_{AK}}{\mathrm{d}t} + V_d \right) dt \\ &= \frac{-t^3}{3} \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \frac{\mathrm{d}V_{AK}}{\mathrm{d}t} + \frac{t^2 \left(V_d \left(\frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \right)^2 - 2 I_F \frac{\mathrm{d}V_{AK}}{\mathrm{d}t} \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \right)}{2 \frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} \\ &\qquad - \left. \frac{t \left(\frac{\mathrm{d}V_{AK}}{\mathrm{d}t} I_F^2 - V_d \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} I_F \right)}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} \right|_{t_2}^{t_3} \\ &= \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \frac{(V_{AKpk} - V_d)^2 (2V_{AKpk} + V_d)}{6 \left(\frac{\mathrm{d}V_{AK}}{\mathrm{d}t} \right)^2} \end{aligned} \tag{4.43}$$

As seen, the current equations in E_{SW1} and E_{SW2} are the same while the voltage enters a new phase. Based on analyzing the experimental measurements, additional terms such as peak reverse current (I_{PR}) and peak voltage overshoot (V_{AKpk}) are introduced to assist in determining the switching energy.

In section 3 (the ringing phase) which is from t_3 to t_4, both the diode current and voltage are modeled as damped cosine waveforms with a defined oscillation frequency and attenuation. The oscillation frequency and damping of the diode voltage was determined previously.

$$\begin{aligned} E_{SW3} &= \int_{t_3}^{t_4} I_{PR} e^{-\alpha_I t} cos\left(\omega t\right) \cdot \left(V_{DD} + L\frac{\mathrm{d}I_{DS}}{\mathrm{d}t} e^{-\alpha_V t} cos\left(\omega t\right)\right) dt \\ &= -\frac{I_{PR} V_{DD}\left(\alpha_I sin(\omega t) + \omega cos(\omega t)\right)}{e^{\alpha_I t}(\alpha_I^2 + \omega^2)} \\ &+ \frac{2\omega sin(2\omega t) - I_{PR} L\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\left((\alpha_I + \alpha_V) cos(2\omega t)\right)}{2e^{(\alpha_I+\alpha_V)}\left((\alpha_I + \alpha_V)^2 + 4\omega^2\right)} - \frac{I_{PR} L\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}}{2e^{(\alpha_I+\alpha_V)t}(\alpha_I + \alpha_V)}\Bigg|_{t_3}^{t_4} \end{aligned} \tag{4.44}$$

The limits for the integration over section 3 is taken to be the 5 times the time constant of the oscillations decaying exponential, so:

$$t_4 = \gamma + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}}$$

in which γ is:

$$\gamma = \frac{5}{\alpha_V} = \frac{10 L_{stray} R_{AK} C_{AK}}{R_{AK} R_S C_{AK} + L_{stray}}$$

The ringing in the circuit is determined by the parasitic inductance and capacitance associated with the Schottky diode, hence, will depend on parameters such as α and ω.

The equation for switching energy in section 3, after the insertion of the limits in 4.44 is:

$$E_{SW3} = \sum_{i=1}^{9} E_{SW3_i} \tag{4.45}$$

where:

$$E_{SW3_1} = I_{PR} \cdot V_{DD} \cdot \left(\frac{\alpha_I sin\left(\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)\right)}{(\alpha_I^2 + \omega^2) e^{\alpha_I\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)}} \right) \tag{4.46a}$$

$$E_{SW3_2} = I_{PR} \cdot V_{DD} \cdot \left(\frac{\omega cos\left(\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)\right)}{(\alpha_I^2 + \omega^2) e^{\alpha_I\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)}} \right) \tag{4.46b}$$

$$E_{SW3_3} = -I_{PR} \cdot V_{DD} \cdot \left(\frac{\alpha_I sin\left(\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)\right)}{(\alpha_I^2 + \omega^2) e^{\alpha_I\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)}} \right) \tag{4.46c}$$

$$E_{SW3_4} = -I_{PR} \cdot V_{DD} \cdot \left(\frac{\omega cos\left(\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)\right)}{(\alpha_I^2 + \omega^2) e^{\alpha_I\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk} - V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)}} \right) \tag{4.46d}$$

$$E_{SW3_5} = \frac{LI_{PR}}{2} \cdot \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \cdot \left(\frac{e^{(\alpha_I+\alpha_V)\left(\frac{V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)} (e^{(\alpha_I+\alpha_V)\gamma} - 1)}{(\alpha_I+\alpha_V)e^{(\alpha_I+\alpha_V)\gamma + \frac{(\alpha_I+\alpha_V)I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{(\alpha_I+\alpha_V)V_{AKpk}}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}}} \right) \tag{4.46e}$$

$$E_{SW3_6} = \frac{LI_{PR}}{2} \cdot \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \cdot \left(\frac{(\alpha_I+\alpha_V)cos\left(2\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)\right)}{((\alpha_I+\alpha_V)^2+4\omega^2)e^{(\alpha_I+\alpha_V)\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)}} \right) \tag{4.46f}$$

$$E_{SW3_7} = \frac{LI_{PR}}{2} \cdot \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \cdot \left(\frac{(\alpha_I+\alpha_V)cos\left(2\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)\right)}{((\alpha_I+\alpha_V)^2+4\omega^2)e^{(\alpha_I+\alpha_V)\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)}} \right) \tag{4.46g}$$

$$E_{SW3_8} = -LI_{PR} \cdot \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \cdot \left(\frac{\omega sin\left(2\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)\right)}{((\alpha_I+\alpha_V)^2+4\omega^2)e^{(\alpha_I+\alpha_V)\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}}\right)}} \right) \tag{4.46h}$$

$$E_{SW3_9} = -LI_{PR} \cdot \frac{\mathrm{d}I_{DS}}{\mathrm{d}t} \cdot \left(\frac{\omega sin\left(2\omega\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)\right)}{((\alpha_I+\alpha_V)^2+4\omega^2)e^{(\alpha_I+\alpha_V)\left(\frac{I_F}{\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}} + \frac{V_{AKpk}-V_d}{\frac{\mathrm{d}V_{AK}}{\mathrm{d}t}} + \gamma\right)}} \right) \tag{4.46i}$$

The total switching energy ($E_{SWtotal}$) in the diode will be the sum of E_{SW1}, E_{SW2} and E_{SW3} as presented in 4.47 and Figure 4.51. Given the diode current, voltage, dI_{DS}/dt, dV_{AK}/dt and RLC values of the diode equivalent circuit, the switching energy can be calculated as a function of the switching rate.

$$E_{SWtotal} = E_{SW1} + E_{SW2} + E_{SW3} \tag{4.47}$$

Figure 4.51 shows the modeled switching power transient, of which the area beneath the waveform is the switching energy; now defined in Equation 4.47 as a good approximation of the measurements in Figure 4.50.

4.4.4.2 Incorporating Temperature Dependency

To incorporate the temperature dependency of the transients into the switching energy model, the temperature dependency of the switching rate should be determined. In this regard, the temperature dependency of dI_{DS}/dt of the low side MOSFET (which is the determining factor of switching rate in the diode as seen in Equation 4.41) can be provided using Equation 4.36 which was developed by simply taking the derivative of 4.33a with respect to temperature. Using dI_{DS}/dt at room temperature as the reference switching rate, Equation 4.48 is developed which makes the dI_{DS}/dt a temperature dependent parameter by incorporating $d^2I_{DS}/dtdT$ of Equation 4.36 as:

$$\frac{\mathrm{d}I_{DS}}{\mathrm{d}t} = \left.\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\right|_{T=25^{\circ}C} + \frac{\mathrm{d}^2I_{DS}}{\mathrm{d}t\mathrm{d}T}\,(T-25) \tag{4.48}$$

The switching energy model will be able to take into account the temperature dependency of transients by substituting 4.48 as described above into each part of $E_{SWtotal}$ in 4.47.

4.4.5 Model Validation

The accuracy of the model is validated by comparing the predictions of the model output with actual switching energy measurements. Figure 4.52 shows the measured and calculated switching energy for the Schottky diode as a function of the switching rate (controlled by the gate resistances). It can be seen from Figure 4.52(a) that the switching energy initially decreases as the switching rate is decreased. This is due to the fact that the diode overshoots is better damped as the switching rate is reduced, hence, the additional power peaks arising from the overshoots/undershoots are reduced. In this case, the switching energy of the voltage switching phase and the ringing phase (E_{SW2} and E_{SW3}) in the developed model are the more important factors in determining the total switching energy of the diode. As has been shown earlier, the contribution of the voltage switching phase to switching energy decreases with decreasing dI_{DS}/dt. However, as the switching rate is further reduced, the switching energy starts to rise again. In this case the overshoots are completely damped, so the total switching energy is now more dependent on the switching energy of the current switching phase (E_{SW1}) which increases as the switching rate is reduced. This is also predictable from the equations in the developed model for the switching energy. As seen, in Equation 4.42 which describes the switching energy of the current switching phase, the dI_{DS}/dt is inversely proportional to the switching energy thereby causing it to decrease as the switching rate is increased (lower R_G is used). On the contrary, Equation 4.43 predicts that as dI_{DS}/dt and the voltage overshoot (V_{AKpk}) is decreased, switching energy of voltage switching phase is also decreased. Measurements have shown that this is also correct since an increase in R_G results in a corresponding decrease in the dI_{DS}/dt and V_{AKpk}. Figure 4.50 has also shown that the significance of ringing is reducing as the gate resistance increases due to damping of the oscillations.

These characteristics are clear in Figure 4.52(b) where it shows the total calculated switching energy, broken down into the 3 components (E_{SW1}, E_{SW2} and E_{SW3}). It can be seen from Figure 4.52(b) that the E_{SW1} increases as the switching rate is reduced while E_{SW2} and E_{SW3} decrease as the switching rate is decreased. The margin of error seen in the model output is mainly due to the fact that the variable parameters are approximated with constant values. This error was reflected in Figure 4.46. Despite the error margin, all the components of the switching energy and its overall shape is correctly predicted.

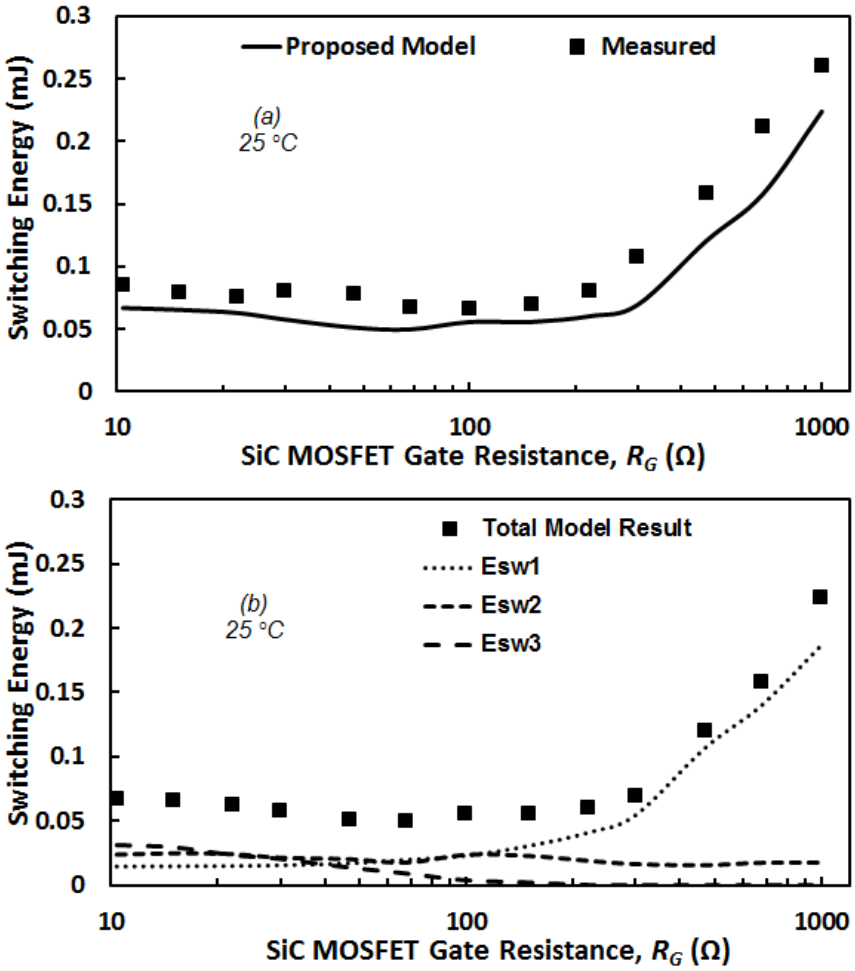


Figure 4.52: Measured and modeled switching energy as a function of the switching rate for each switching energy component (E_{SW1}, E_{SW2} and E_{SW3}) performed at 25 °C.

Figure 4.53 shows the measured and calculated switching energy as a function of temperature. The switching energy is shown to be nearly temperature invariant at high switching rates and reasonably good agreement exist between the model and measurements. The model correctly predicts this because the temperature dependence of the switching rate has been incorporated into the diode switching energy model as in 4.48.

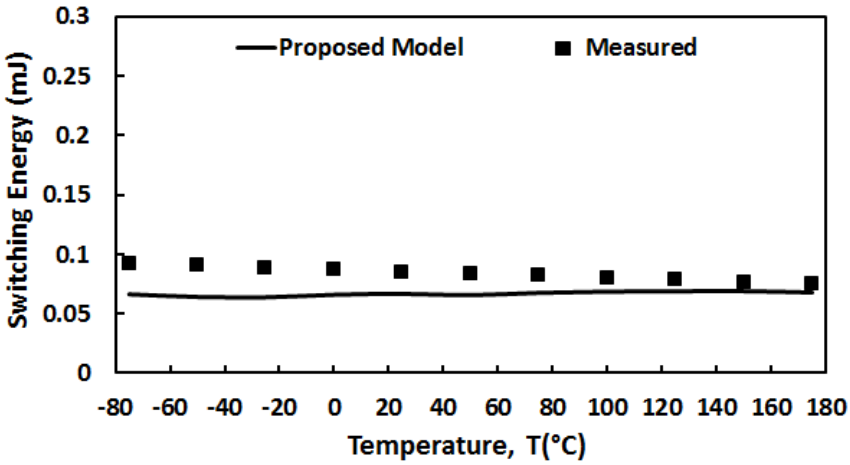


Figure 4.53: Measured and modeled E_{SW} as a function of temperature ($R_G = 15\ \Omega$).

It can be seen from the measurements that the contribution of the switching energy of the current switching phase (E_{SW1}) increases with the gate resistance whereas that of the voltage switching phase and the ringing phase (E_{SW2} and E_{SW3}) generally decreases as R_G is increased. The measurements show good agreement with the modeling. Similar trends were also previously shown in Figure 3.34 where the impact of switching rate and temperature on the switching energy of the SiC Schottky diode at turn-off is evident and the U-shaped characteristics of switching energy's dependence on the switching rate can be seen as that switching energy increases with reducing temperature at a rate that increases as dI_{DS}/dt reduces, i.e. as the switching rate is reduced, the switching energy shows more temperature dependency. The dependence of the MOSFET's turn-on switching

energy on temperature also increases as the gate resistance increases. Hence, temperature dependence of the SiC MOSFET's turn-on switching performance directly affects the diode's turn-off switching performance and the waveforms transient.

4.5 Summary

In this chapter, accurate analytical models have been developed for predicting the performance and switching energy of power rectifiers. In this regard, first an accurate analytical model was developed that correctly emulates the measurements of PiN diode switching energies as a function of the switching rate and temperature. The model is capable of correctly predicting the switching energy of PiN diodes switched at different rates and temperatures and can account for non-linear dI/dt in the current that occurs at low switching rates. Measurements of current commutation between a low side IGBT and a high side PiN diode at different switching rates and temperatures have shown that the switching energy at high switching rates is dominated by the peak reverse recovery current and especially the diode voltage overshoot whereas at low switching rates, the switching energy is dominated by the duration of the switching transient. Measurements also show that the slope of the diode's recombination current is as critical as reverse recovery in determining the switching energy because the diode is in recombination phase at the time when the diode voltage is at its peak. The model developed was validated through experimental measurements on a range of switching rates and temperatures using discrete devices and the outputs show good agreement with the measurements. The model can be used as a diagnostic tool for predicting the switching performance of PiN diodes.

Then, the dI_{DS}/dt and temperature dependence of the switching performance of SiC Schottky diodes was presented over a wide range of temperature and dI_{DS}/dt range. Diode

turn-off voltage ringing has been shown to increase with temperature for a fixed gate resistance due to the fact that the dI_{DS}/dt increases with temperature during MOSFET turn-on. It was also shown that the rate of increase of the turn-on dI_{DS}/dt with temperature increases with the gate resistance. This resulted in greater diode V_{AK} dependence on temperature for higher gate resistances. Physics based models that explain the experimental observations were developed and were shown to account for the measurements. Additionally, a comprehensive model for the switching energy of the SiC Schottky diode was developed and validated. The results show convergence between the measurements and the model output with a considerably small margin of error. It was shown that the switching energy as a function of the gate resistance exhibits a U-shaped characteristic with switching energy at low R_G dominated by diode overshoot losses and at high R_G dominated by transient overlap between V_{AK} and I_{AK}. Hence, the switching energy of the diode is shown to be a combination of 3 switching phases namely the current switching phase, the voltage switching phase and the ringing phase. While the switching energy of the current switching phase decreases with increasing switching rate, the switching energy of the voltage switching phase and the ringing phase increases with the switching rate (this is due to the fact that damping reduces as the switching rate increases, so the overshoot losses dominate at high switching speeds). Hence, as the gate resistance which determines the switching speed of the low side MOSFET is increased, the switching energy initially decreases as the overshoots become better damped. However, beyond an optimum gate resistance, the switching energy starts increasing again because the switching energy of the current switching phase (which increases as the switching rate is reduced) starts to dominate the total switching energy. These results are important because they can account for electromagnetic oscillations as a function of temperature and dI_{DS}/dt, which in turn is important for determining EMI, operating temperature and reliability.

Chapter

5 Performance and Robustness of Power MOSFETs Body Diodes

As stated earlier, the first generations of silicon MOSFETs were not useful in high voltage applications due to thicker and more resistive epitaxial layers. Recent advances in fabrication of MOSFETs have enabled silicon power MOSFETs with higher blocking voltages, however, due to the silicon limit, these still do not meet the standards for efficient power conversion. As a result, silicon IGBTs are the devices of choice in higher voltage applications (>600 V). Hence, the use of power MOSFETs in power converters is limited to high frequency and low voltage applications where conduction losses are less of an issue.

However, two innovative breakthroughs in power MOSFETs have enabled new application opportunities in power conversion. First, just a decade ago a novel device structure called 'Superjunction' MOSFETs (which became commercially available in 1999 by Infineon® under the brand CoolMOS™) significantly reduced the on-state resistance of power MOSFETs, thereby suppressing the so-called silicon limits. This concept provided a solution to increase the blocking voltage without using thick and highly resistive drift layers. By using alternate P and N pillars, lateral as well as vertical depletion resulted in high blocking voltages with less resistive drift layers, hence, the trade-off between block-

ing voltage and on-state resistance is relaxed [91]. Details of this will be shown later. However, this device technology, although superior in medium voltage applications (up to 0.9 kV), has not been able to exceed this limit due to the complexities involved in the fabrication of pillars required to block higher voltages [92] while maintaining adequately low on-state resistance. Another avenue through which the performance of the power MOSFETs was improved was the transition to wide bandgap semiconductors, mainly SiC where the higher critical electric field results in a thinner and less resistive drift layer.

As stated in chapter 2, all MOSFETs regardless of the material or structure, have one additional component integral to them; a PiN body diode. This is inevitably present to avoid a floating base on the parasitic BJT of the MOSFETs to reduce the probability of latch-up. As a result, unlike IGBTs where such diode does not exist, the PiN body diode of power MOSFETs must be evaluated both in terms of performance and robustness. Hence in this chapter, the trade-off between the switching energy and electro-thermal robustness is explored for 1.2 kV SiC MOSFET and silicon power MOSFET and 900V CoolMOS™ body diodes with similar current ratings at different temperatures and voltages.

The maximum forward current for dynamic surging breakdown is seen to decrease with increasing supply voltage and temperature for all technologies. The CoolMOS™ exhibited the largest latch-up current followed by the SiC MOSFET and silicon power MOSFET; however when expressed as current density, the SiC MOSFET comes first followed by the CoolMOS™ and silicon power MOSFET. For the CoolMOS™, the alternating P and N pillars of the superjunctions minimized lateral currents and provided low resistance paths for carriers. Hence, the temperature dependence of the latch-up current for CoolMOS™ was the lowest. The switching energy of the CoolMOS™ body diode is the largest because of its superjunction architecture which means the drift region has higher doping, hence more reverse charge. In spite of having a higher thermal resistance, the SiC MOSFET

has approximately the same latch-up current while exhibiting the lowest switching energy because of the least reverse charge. The silicon power MOSFET exhibits intermediate performance on switching energy with the lowest dynamic latching current.

5.1 Body Diodes and Common Points of Failure

Traditionally, independent discrete diodes are used as reverse conducting or anti-parallel diodes so as to enable bi-directional power flow. The foremost characteristic of PiN diodes is in the turn-off transient where reverse recovery can be observed as a result of minority carrier extraction from the drift layer. Integral to MOSFET is the body diode with a structure of a PiN diode because of the lightly doped voltage blocking drift layer between the N^+ drain and P body. Due to this, similar plasma formation and extraction mechanisms explained in the previous chapter for discrete PiN diodes is applicable. As current is ramped down during the turn-off process in the PiN diode, the carrier distribution profile supports the current through the zero crossing until the voltage across the diode causes depletion widths at the diode PN^- and N^-N^+ junctions. Once this space charge region forms, the reverse current reaches its peak value (which is the peak reverse recovery current) and then the turn-off current starts to recover to zero.

Although it is generally desirable for the PiN diode to have a minimum reverse recovery time, it can be hazardous if the rate of change of the current with time is very high in the presence of parasitic inductances. As was discussed in the earlier chapter, a PiN diode's reverse recovery characteristics can be considered to be soft or snappy depending on the ratio of slopes for the current to change [53]. When the voltage across the diode increases to the supply voltage there is usually a peak voltage overshoot due to parasitic inductance and a time varying current. The peak voltage overshoot occurs at the time

when the diode is in reverse recovery, hence, snappy diodes can cause high peak voltages and dV/dt induced breakdown capable of destroying the diode. The well-known parasitic NPN BJT in the MOSFET can be activated by the displacement current of the drain-body depletion capacitance (C_{db}), which is proportional to the dV/dt. It is also possible for the reverse recovery current to trigger bipolar latch-up in the device [93]. If sufficient current flows through the body of the MOSFET to increase the potential difference between the P-body and the N-source beyond the built-in junction voltage, the parasitic BJT inherent in the device may latch with destructive consequences [94]. Because the latch-up current has a positive temperature coefficient, also a thermal runaway may ensue [95].

In SiC MOSFETs, the low minority carrier lifetime in the drift layer coupled with the smaller capacitances means that the body diode switching is faster (i.e. dV/dt is higher) and the reverse charge is significantly smaller; whereas in the CoolMOS™ devices, the alternate P and N doped pillars in the drift region means that the anti-parallel body diode will be a parallel combination of PN^-N^+ and PP^-N^+ diodes. Hence, during reverse recovery, electrons will be minority carriers in PP^-N^+ diodes whereas holes will be minority carriers in PN^-N^+ diodes where electrons have higher carrier lifetimes. CoolMOS™ devices will hence exhibit higher reverse recovery charge which will be made worse by virtue of the fact that the P and N pillars will be more highly doped when the superjunctions enable high voltage blocking, i.e. reverse recovery charge increases with the doping of the drift layer. Figure 5.1 shows schematic diagrams of a standard vertically diffused power MOSFET and CoolMOS™ with the inherent body diode and parasitic BJT.

In low voltage applications, to avoid unintentional conduction of the PiN body diode, a low voltage Schottky diode is placed in series with the body diode (with opposite polarity) while a further dedicated PiN diode is placed as the effective anti-parallel diode [96]. This approach assists both the performance and the robustness of the circuit. This is because

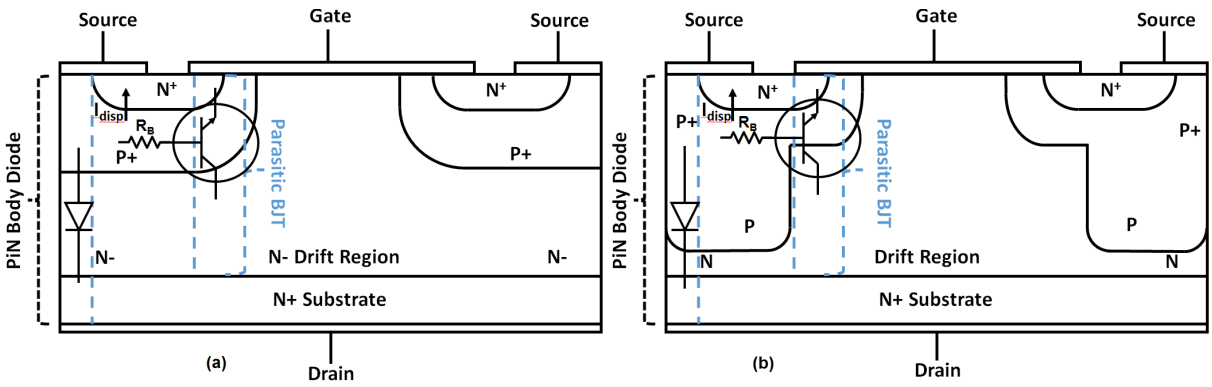


Figure 5.1: Cross-sectional schematic of (a) standard vertical D-MOSFET and (b) superjunction power MOSFET (CoolMOS™) with parasitic BJT and intrinsic diode.

the dedicated anti-parallel PiN diode can be a fast diode with low minority carrier lifetime and hence low reverse recovery. The reverse recovery of the body diode can also be reduced by introducing certain recombination centers (such as platinum), however this will make the diode snappier as the charge will recombine faster. Snappy reverse recovery (as will be seen later) is a determining factor in triggering the parasitic BJT into latch-up and hence should be avoided. Therefore it is best to block the body diode (using a diode with low forward voltage drop) and conduct through an anti-parallel diode. This, although feasible in low voltages, is not practical in high voltage power applications as the continuous power losses as a result of the conduction losses of the blocking diode becomes too high. So, the best approach is to provide a low resistive path through a dedicated anti-parallel diode to reduce the current flow into the body diode without having to block it.

Hence in power MOSFETs, it is not possible to block the body diode's conduction and some degree of current will inevitably flow through it. Thereby especially with emergence of advanced devices, i.e. SiC MOSFETs and CoolMOS™ superjunctions, it has become even more crucial to investigate the performance and robustness of the body diodes under hard commutation as they are now more likely to replace IGBTs in medium voltages [97].

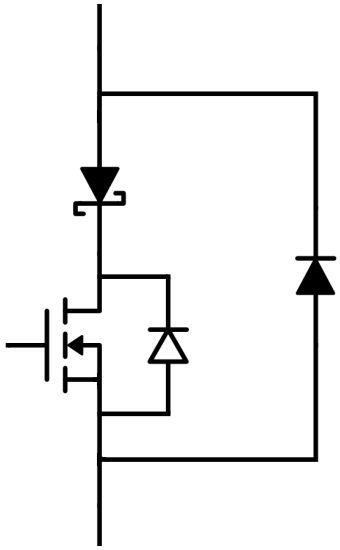


Figure 5.2: Conduction of MOSFET body diode blocked by a reverse series Schottky diode, replacing it with an extra anti-parallel diode.

It has been previously shown that the body diode can be utilized as a replacement for the PiN diodes in soft switching converters such as zero-voltage switching [98]; however, the use of the body diode may create a significant robustness issue when it comes to hard commutation switching [99]. To overcome this, different MOSFET designs were considered including lateral Power MOSFET (LDMOS) [100], VDMOSFT [101], V-groove MOS [102], TrenchMOS or UMOS [103, 104], semi superjunction [105] and eventually superjunction MOSFETs or CoolMOS™ [106, 107] some of which showed certain improvements, however could not help the overall poor reverse recovery performance of the body diodes during hard commutation. Though certain efforts were made to use methods such as 'active channel freewheeling' to minimize the effect of the recovery charge, the performance of the body diode could not be improved [108]. Recently developed SiC MOSFETs contain body diodes that have reduced the magnitude of the recovery charge [109] which is a considerable step forward, however it also creates robustness concerns [110].

To explore these concepts and to provide a comprehensive understanding of the impact of the superjunction structure and wide bandgap materials properties on the performance and robustness of body diodes, the next sections detail the experiments and analysis that have been performed. The first two sections discuss the fundamentals of the parasitic BJT latch-up mechanisms as well as the basis of superjunction MOSFETs. Subsequent sections explore the measurements on reverse recovery of body diodes as functions of switching rate, temperature and forward current in silicon power MOSFETs, CoolMOS™ and SiC MOSFETs. In the robustness evaluation section, current is conducted through the free-wheeling body diode, which is subsequently commutated at incremental levels thereby eventually going into breakdown [111]. This also depends on the commutation rate, temperature, forward current and supply voltage. Hence, a range of forward current in different conditions are applied until the device fails destructively under latch-up.

5.1.1 Power MOSFETs Body Diode

The body diode of the MOSFET is formed as a result of efforts to reduce the probability of pre-mature breakdown, however conduction of this diode can also become the cause of the breakdown of the device. This is because it acts similar to a PiN diode however with very poor reverse recovery. This is due to the fact that a MOSFET is a majority carrier unipolar device, hence, carrier lifetime is not a critical consideration as is the case in bipolar devices. Therefore, the minority carrier lifetime in MOSFETs is not specifically adjusted. The carrier lifetime, however, becomes very important when it comes to the conduction of the MOSFET's body diode. Reducing the carrier lifetime in the drift region of the MOSFET by introducing recombination centers is possible and normally will not impact the resistance of the drift region of the device (if Pt is used), however this requires

an extra step in the fabrication process. Unfortunately, these recombination centers may as well act as generation centers in the blocking mode, enhancing the leakage current and the blocking state losses. This is specially important in silicon devices with narrower bandgap. Therefore, this option should also be exercised with care. Additionally, another major problem is the snappiness of the reverse recovery of the body diodes. This increases with reduction of the carrier lifetime as recombination is happening faster. Therefore, although introducing recombination centers will improve the performance of the device through reducing reverse recovery charge, but it will not help to increase the device's robustness since the latch-up possibility is increased by the increased snappiness as a result of faster recombination of carriers. The next section will explain different paths for triggering of the parasitic BJT into latch-up in further details.

5.1.2 BJT Latch-up Mechanisms in Power MOSFETs

In an N-channel vertical power MOSFET (which is the fundamental structure of majority of power MOSFETs), a parasitic BJT is formed between the N^+ Source, the P-body and the N^- drift region. In this case, the emitter of the NPN BJT is connected to the source, the base is on the P-body and the collector is on the drift region. As a result, it is clear that if this parasitic BJT turns-on, the electrons will start to flow from the emitter to the collector, bypassing the channel. In this case, the gate of the MOSFET, which initially modulated the channel is no more in control of the current flow since the electrons bypass it and flow through the BJT path. This means the MOSFET cannot be turned-off anymore and may eventually go into thermal runaway due to the positive temperature coefficient of the latching process. In this case, the parasitic BJT is 'latched-up' and it is important to make sure that this does not happen. For an NPN BJT to turn-on, apart from presence

of a potential on the collector-emitter (where in the case of power MOSFET refers to the drain compared with source) there should be enough voltage on the base compared with the emitter to forward bias the base-emitter PN junction. The value of this built-in potential in silicon is approximately 0.7 volts and in 4H-SiC is approximately 2.8 volts. Clearly, in this case, SiC has an advantage over silicon since a higher V_{BE} makes the BJT latching less likely. However, other factors such as high switching rates (dV/dt) in SiC MOSFETs are also as important (which is partly due to the higher saturation velocity of electrons in SiC compared with silicon and partly due to the smaller parasitic capacitances of SiC MOSFETs which results from the smaller die area). Therefore to avoid latch-up of the parasitic BJT, presence of base-emitter voltage must be suppressed. The necessary voltage on the base-emitter PN junction can be produced in a few paths:

- First, the parasitic capacitance between the body and drain of the MOSFET coupled with the dV/dt at turn-off causes a displacement current to flow into the P-body which has a finite resistance and will hence induce a voltage drop across the base-emitter terminals of the parasitic BJT. If this voltage increases beyond the built-in potential of its base-emitter PN junction, latch-up may be induced.

- The second process may be due to the reverse recovery current in the PiN body diode when it turns-off at the end of the conduction period [95]. This turn-off current of the body diode also flows into the P-body and the same phenomenon happens.

- A third avenue for generation of this current is due to excessive snappiness of the PiN body diode [112]. In this case, the snappiness of the recovery current imposes an even higher dI/dt on the parasitic inductance of the circuit, which induces a high voltage overshoot with a high dV/dt. This dV/dt once again coupled with the C_{db} causes a displacement current to flow into the P-body.

As will be seen in this chapter, the first case is more probable in SiC devices due to the high switching rates of these devices and negligible reverse recovery current from very low minority carrier lifetime in SiC; the second case is more probable in silicon power MOSFET devices with higher reverse recovery charge while the third case is more pronounced in superjunction MOSFETs where snappy recovery results in high dV/dt.

As a general solution, and to reduce latch-up probability, P-body resistance is required to be as small as possible. A common practice, which causes the presence of the body diode, is shorting the base and the emitter of the parasitic BJT through connecting MOSFET's P-body to the source metallization. This reduces the voltage drop but cannot completely eliminate it as the P-body is not an absolute conductor. Hence, to increase the quality of the connection, the P doping can be increased to reduce the body resistance. To avoid increasing the threshold voltage as a result of higher P-body doping, a highly doped P^+-region in body is designed with sufficient space from the channel where a targeted P-doping is used to set the threshold voltage. However increasing the P-body doping, i.e. Boron in SiC, is not straightforward due to the low diffusion constant of P-dopants.

5.1.3 Superjunction Power MOSFETs (CoolMOS™)

In conventional silicon devices, the on-state resistance increases with the off-state blocking voltage capability. This limitation is known as the silicon limit and it can be explained through the blocking voltage capability of a P-N junction.

For a PiN diode the on-state resistance per unit area can be written as:

$$R_{ON} = \frac{W}{q\mu_n N_D} \tag{5.1}$$

while from the poisson's equation, assuming a full ionization of dopants, it can be derived as:

$$\frac{\mathrm{d}\mathscr{E}}{\mathrm{d}x} = \frac{\mathscr{E}_{BR}}{W} = \frac{qN_D}{\varepsilon_S} \tag{5.2}$$

For an abrupt junction, the width of the triangular electric field, resulting in the maximum depletion area for the breakdown voltage (BV) can be calculated as:

$$W = \frac{2BV}{\mathscr{E}_{BR}} \tag{5.3}$$

and the doping of the drift region is:

$$N_D = \frac{\varepsilon_S \mathscr{E}_{BR}^2}{2qBV} \tag{5.4}$$

Hence, the relationship between the on-state resistance and the blocking voltage can be defined as:

$$R_{ON} = \frac{4BV^2}{\mu\varepsilon_S \mathscr{E}_{BR}^3} \tag{5.5}$$

which initially was thought to be the silicon limit.

However, the critical electric field of silicon changes slightly with the level of the doping in the material according to [113] as:

$$\mathscr{E}_C = f(N_D^{1/8}) \tag{5.6}$$

and

$$N_D = f(BV^{-4/3}) \tag{5.7}$$

will result in the

$$\mathscr{E}_C^3 = f(BV^{-1/2}) \tag{5.8}$$

Hence, Equation 5.5 for silicon can be re-written as:

$$R_{ON} \approx 8.3 \times 10^{-9} BV^{2.5} \ \Omega.cm^2 \tag{5.9}$$

However, in superjunction MOSFETs the on-state resistance differs. Superjunction MOSFETs introduce deep P pillars into the N drift region of the device; hence a lateral depletion region is also formed in addition to the vertical space charge as a result of the blocking voltage. Hence, the electric field across the width of the drift region is distributed evenly. This has a simple result; the triangular formation of the electric field in drift region of power MOSFETs becomes rectangular with penetration in both P and N pillars.

As the blocking voltage is simply the area below the electric field with respect to the drift region width, a rectangular electric field can block the same voltage with a lower width and higher doping, hence lower on-state resistance. In this regard, it can be seen that the breakdown voltage can now be derived from:

$$BV = \mathscr{E}_C \times W \tag{5.10}$$

in which, by considering the cp/2 (cell pitch) as the width of each of the N and P pillars, the critical electric field for the superjunction pillars is:

$$\mathscr{E}_C = qN\frac{\frac{cp}{2}}{\varepsilon} \tag{5.11}$$

which for the doping level translates into:

$$N = 2\varepsilon\mathscr{E}_C/(q \times cp) \tag{5.12}$$

As we had previously for on-state resistance,

$$R_{ON} = \frac{W}{q\mu_n N_D} \tag{5.13}$$

which by replacing Equation 5.12, we will get:

$$R_{ON} = \frac{cp \times BV}{2\varepsilon\mu_n\mathscr{E}_C^2} \tag{5.14}$$

This means that theoretically the thinner the superjunction pillars, the lower will be the on-state resistance. However practical constraints restricts the possibility of fabrication of very narrow pillars. Comparing Equation 5.9 with 5.14, it can be seen that on-state resistance is now linearly dependent on the breakdown voltage compared with previous case. This is a great achievement in reduction of on-state resistance for high breakdown voltages. In addition to superjunction MOSFETs, high breakdown voltages with low on-state resistance can also be achieved by the use of wide bandgap semiconductors.

5.2 Measurement of Performance of the Body Diodes

In order to investigate the performance and reliability of the body diodes of the different MOSFET technologies, experimental measurements have been performed on SiC MOSFET, silicon power MOSFET and CoolMOS™ devices with the dual objectives of comparing the switching energies and the robustness by testing to failure. The measurements were performed in clamped inductive switching test rig described in chapter 3, the schematic of which is shown in Figure 5.3 and the pictures of the LV and HV test rigs were shown in Figure 3.3 and 3.5. For measurements that require a pre-defined ambient temperature, the environmental chamber also shown in Figure 3.3 is used to monitor and maintain the ambient temperature within the specified levels. The ambient temperature is critical in that it sets the headroom for the junction temperature excursion during the breakdown experiment. Higher ambient temperature thus leaves less headroom. To ensure that the body diode conducts during the measurement, the gate of the high side transistor is connected to the source thereby making the transistor an open circuit, hence, only the body diode appears in the circuit. The body diode of the device under test is used to free-wheel current through a pre-charged inductor and a low-side transistor is used to commutate current away from it thereby initiating reverse recovery.

Figure 5.4(a) to (d) shows the different stages of the double pulse test and the direction of current flow in the circuit. When the low side transistor is switched on as shown in the circuit schematic in Figure 5.4(a), the inductor is charged with a current from the power supply and when it is switched off as shown in Figure 5.4(b), current commutates from the low side transistor into the body diode of the high side transistor. As the low side transistor is switched on again as shown in Figure 5.4(c), the body diode of the high side transistor switches off and goes into reverse recovery. As the low side transistor is

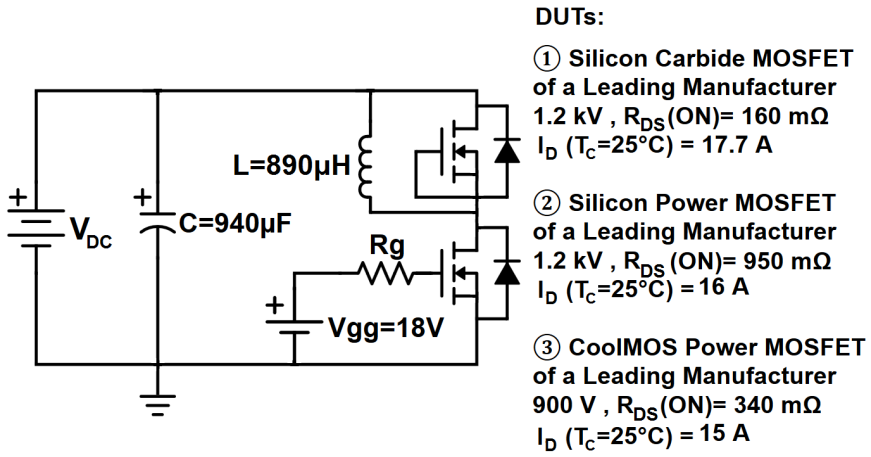


Figure 5.3: Schematic of the double pulse circuit and devices under test.

Table 5.1: Comparison of determining parameters of the superjunction (CoolMOS™), silicon and SiC power MOSFETs used in the body diode measurements.

Parameter	Unit	Silicon	CoolMOS™	SiC
Voltage	V	1200	900	1200
Current	A	16	15	17.7
Input Capacitance	pF	6900	2400	527
On-Resistance	mΩ	950	340	160
Internal Gate Resistance	Ω	1.4	1.3	6.5
Gate Charge	nC	120	94	34
Maximum Gate Source Voltage	V	±30	±20	−5/+20
Body Diode Forward Voltage	V	1.5	0.8	3.3
Thermal Resistance Junction-Case	°C/W	0.2	0.6	1

switched off again in Figure 5.4(d), current commutates into the body diode where it eventually damps to 0. Therefore, similar to measurements of chapter 3, duration of the gate pulse on the low side transistor determines the magnitude of the current.

Both transistors for any given test are of the same technology. As expected the SiC MOSFET has the lowest on-state resistance, followed by CoolMOS™ and silicon power MOSFET. The current ratings of the MOSFETs range closely between 15 and 17 A

whereas the voltage ratings are 1.2 kV for the silicon power MOSFET and SiC MOSFET and 900 V for the CoolMOS™ device (this is the highest voltage rating for a commercially available superjunction MOSFET). Due to the fact that body diodes are not necessarily optimized for the forward current, the initial measurements of the body diode switching performance started from a forward current of 2 A and then gradually increased beyond the current rating until breakdown was observed. Similar to chapter 3, measurements are performed over a wide range of temperatures between –75 °C and 175 °C, R_G between 10 Ω and 1 kΩ and forward currents starting from 2 A to destruction of body diodes.

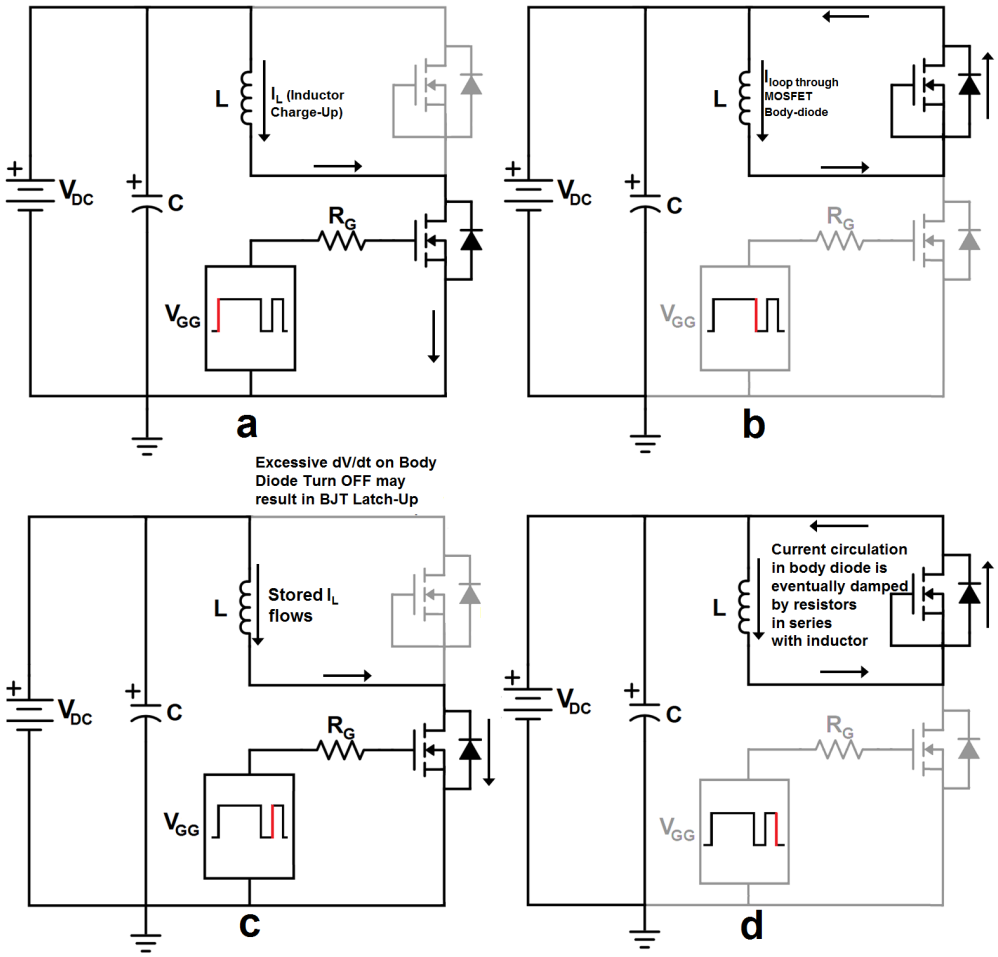


Figure 5.4: The dynamic surging sequence in a clamped inductive circuit.

5.2.1 Reverse Recovery Trends

Figure 5.5 show the body diode reverse recovery currents of the silicon power MOSFET when switched with a forward current of 2 A. For a given PiN diode, the reverse recovery charge is related to the forward current as was determined previously in Equation 2.25, i.e. in these measurements at 25 °C and with a forward current of 2 A, the total reverse charge is 2.07 μC. For the body diode of all power MOSFETs, due to the smaller diode active area, the current density in the body diode is higher than a discrete PiN diode.

The peak reverse recovery current is primarily determined by the commutation rate set by the external circuit (i.e. gate resistance), the temperature dependent minority carrier lifetime as well as forward current. The increase in forward current is expected to lead to an increase in the peak reverse recovery current in addition to the stored reverse recovery charge as will be seen in the next figures. However at high temperatures such as 175 °C, the increase in the minority carrier lifetime becomes the dominant factor over the effect of forward current, hence, the rate of increase of peak reverse recovery current with forward current decreases. Despite this, such high temperatures result in an increase in reverse recovery charge due to the increased minority carrier lifetime in the drift region; hence, lower recombination rates during the recovery phase of charge extraction.

The silicon power MOSFET exhibits some oscillations during turn-off when switched at lower temperatures due to the reduced minority carrier lifetime. Hence, a more snappy reverse recovery characteristics is observed since the recombination rate is increased. These oscillations are damped as temperature increases and might become a robustness issue because an snappy reverse recovery can induce BJT latch-up from excessive voltage spikes associated with them. However, as will be seen in next sections, at higher temperatures, the parasitic BJT in silicon power MOSFETs latches-up at lower forward currents.

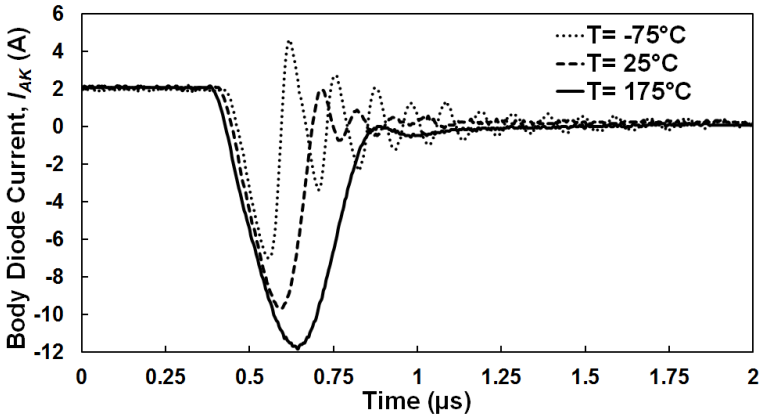


Figure 5.5: The reverse recovery of the silicon power MOSFET body diode with 2 A at different temperatures. It can be seen that reverse charge increases with temperature and low temperatures can induce snappy recovery.

Hence, the impact of temperature on increasing the body resistance and reducing the built-in emitter base junction voltage of the parasitic BJT supersedes the effect of lower recombination rates (higher carrier lifetime) induced by higher temperatures.

Figure 5.6 shows the reverse recovery current of the CoolMOS™ body diode with 2 A forward current. As can be seen, the reverse recovery current is much higher. An slight increase in the reverse recovery would have been expected since it is a lower voltage rated device with higher drift layer doping. However, such significant reverse recovery is mainly due to the superjunction architecture's contribution to the reverse charge firstly by enabling a higher drift layer doping for delivering lower on-state resistance while maintaining a relatively high blocking voltage and secondly, by virtue of the fact that electrons will also participate as stored minority carrier charge in the reverse recovery process because of the presence of the P pillars in the N doped drift region. Also as a result of the fact that electrons have higher carrier lifetimes than holes, there will be higher reverse recovery in CoolMOS™ compared with silicon power MOSFETs [114]. The impact of temperature on the reverse charge is similar to that in the silicon power MOSFET shown in Figure 5.5.

Again, this is as a result of the higher carrier lifetime at higher temperatures. On closer observation, the shape of the reverse current is different in the CoolMOS™ device compared with the silicon power MOSFET. The slope of the recovery current (positive slope from the peak reverse current to 0) is higher than that of the extraction current (negative slope from 0 to the peak reverse current). This is due to rapid charge recombination in the N and P doped columns in the drift region which causes snappy recovery [107].

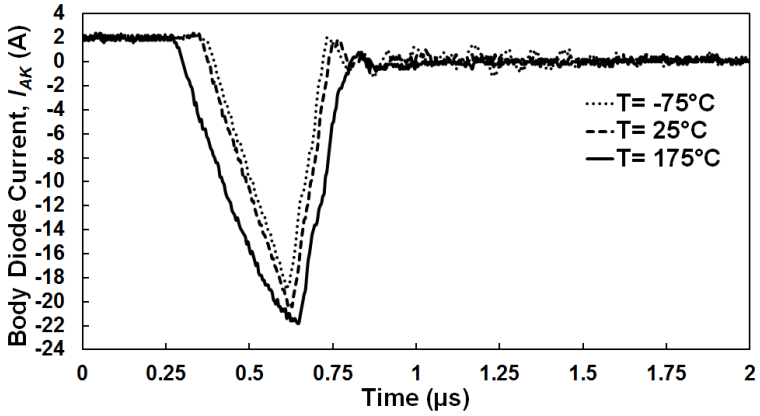


Figure 5.6: Reverse recovery current of CoolMOS™ body diode with 2 A at different temperatures where is seen that total reverse charge increases with temperature.

Figure 5.7 shows the reverse recovery current of the SiC MOSFET body diode also switched with a forward current of 2 A. As can be seen from Figure 5.7, the dI/dt of the SiC MOSFET is much higher and temperature has an insignificant effect on the switching characteristics. Also, there is little or no reverse charge and only current oscillations with small amplitudes are evident. What is interesting to note about the switching characteristics of the SiC MOSFET body diode is the fact that the turn-off characteristics are independent of temperature thereby indicating that there is little or no charge storage mechanism. This is seen clearly in the next section and is due to two reasons; firstly the fact that minority carrier lifetime is very low in SiC MOSFET and secondly that the

physical area of the die is smaller, hence, there is much smaller area for stored charges. The SiC MOSFET will deliver the most energy efficient switching performance since the switching energy will be the smallest as a result of the fastest transients. The robustness implication of this is investigated in the next section.

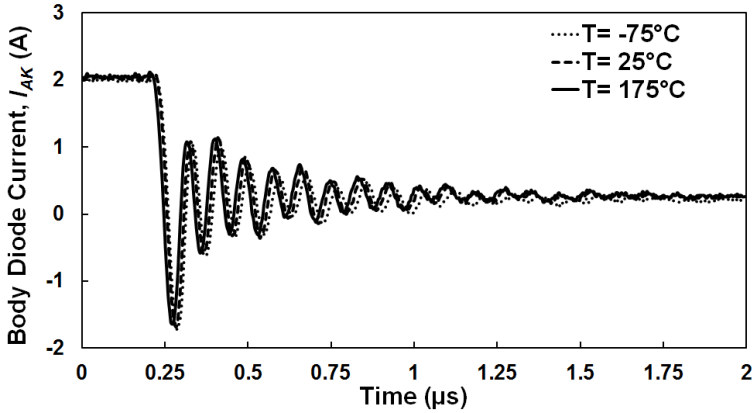


Figure 5.7: Reverse recovery current of SiC MOSFET body diode with 2 A at different temperatures where is seen that total reverse charge is invariant with temperature.

Figure 5.8(a) shows the effect of the gate resistance or the switching rate on the switching characteristics of the body diode for the SiC MOSFET whereas Figure 5.8(b) and Figure 5.8(c) show similar characteristics for the silicon power MOSFET and CoolMOS™. As expected, increasing the switching rate increases the snappiness in the reverse recovery characteristics of the SiC MOSFET and silicon power MOSFET in Figure 5.8(a) and Figure 5.8(b). As the switching rate is increased, the peak reverse recovery current increases and the recovery current has a higher dI/dt, i.e. it is more snappy. This snappy recovery is potentially capable of causing parasitic bipolar transistor to latch-up by inducing large voltage overshoots in combination with parasitic inductances. These measurements are not destructive because of the low currents and voltages involved, however, increasing the switching rates at higher voltages will have destructive consequences.

In the case of the CoolMOS™ device as shown in Figure 5.8(c), increasing the switching rate does not make the recovery snappier or cause oscillations in the turn-off current. This is due to the fact that the superjunction structure has a different mechanism of charge extraction from that in the silicon and SiC power MOSFETs. This will also account

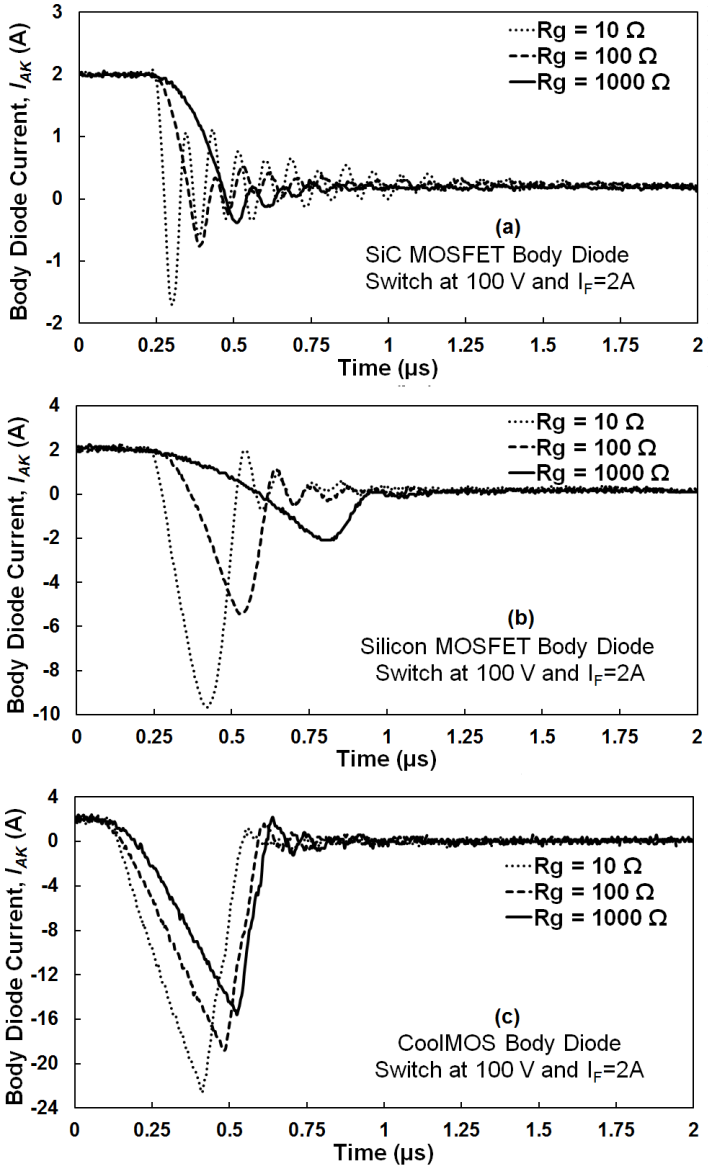


Figure 5.8: Reverse recovery current of (a) SiC MOSFET, (b) silicon Power MOSFET and (c) CoolMOS™ body diode with 2 A forward current and 100 V supply.

for why the CoolMOS™ has the highest latch-up current. Figure 5.9(a) shows the body diode switching characteristics of the three technologies at –75 °C whereas Figure 5.9(b) shows it at 175 °C. It is clear that the reverse recovery of SiC is superior compared with other device technologies in terms of the least recovery charge and the least temperature dependency. The reverse recovery of the CoolMOS™ device is very significant (≈ 20 A peak with $I_F = 2$ A) which further increases with temperature. The silicon MOSFET suffers from snappy recovery due to reduced carrier lifetime at low temperatures and its recovery charge increases with temperature.

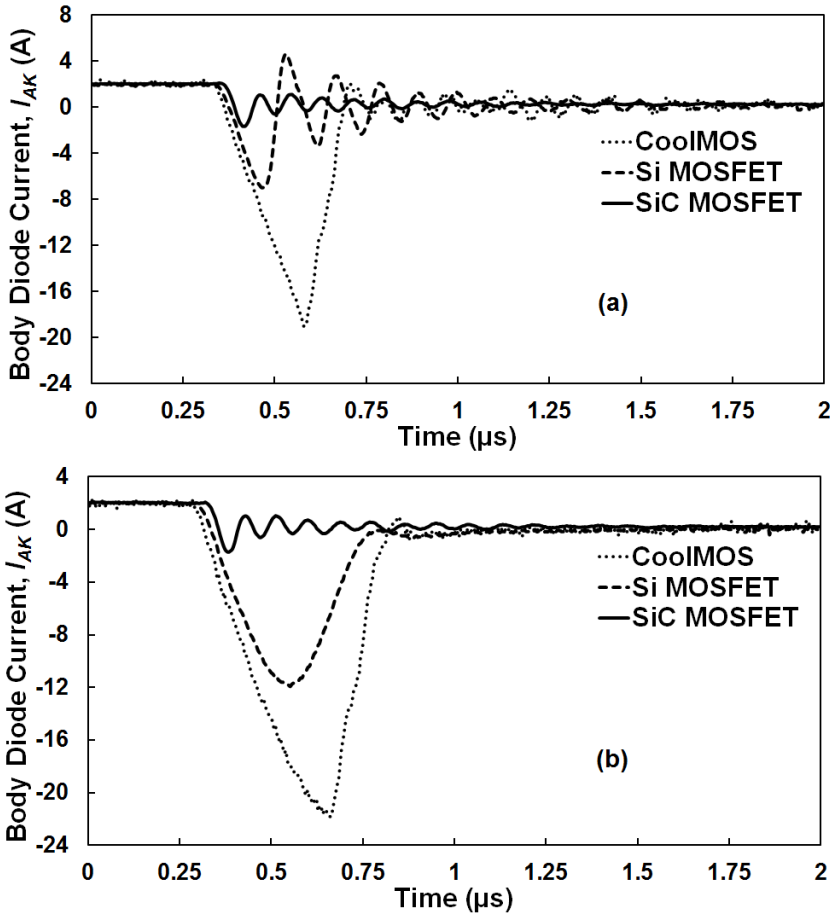


Figure 5.9: Comparison of reverse recovery current of SiC MOSFET, silicon Power MOSFET and CoolMOS™ body diodes with $I_F = 2$ A at (a) –75 °C to (b) 175 °C.

5.2.2 Recovery Charge and Switching Energy

Figure 5.10(a) shows the measured reverse recovery charge as a function of temperature for the 3 device technologies where it can be seen that the reverse charge increases with temperature for both the silicon power MOSFET and CoolMOS™ whereas is temperature invariant (with negligible value) for the SiC MOSFET as was expected from Figure 5.9. Since current is simply defined as charge flow rate, the total reverse recovery charge can be calculated by the integration of the reverse recovery current over its corresponding transient duration. This integration is done numerically using the reverse recovery waveforms

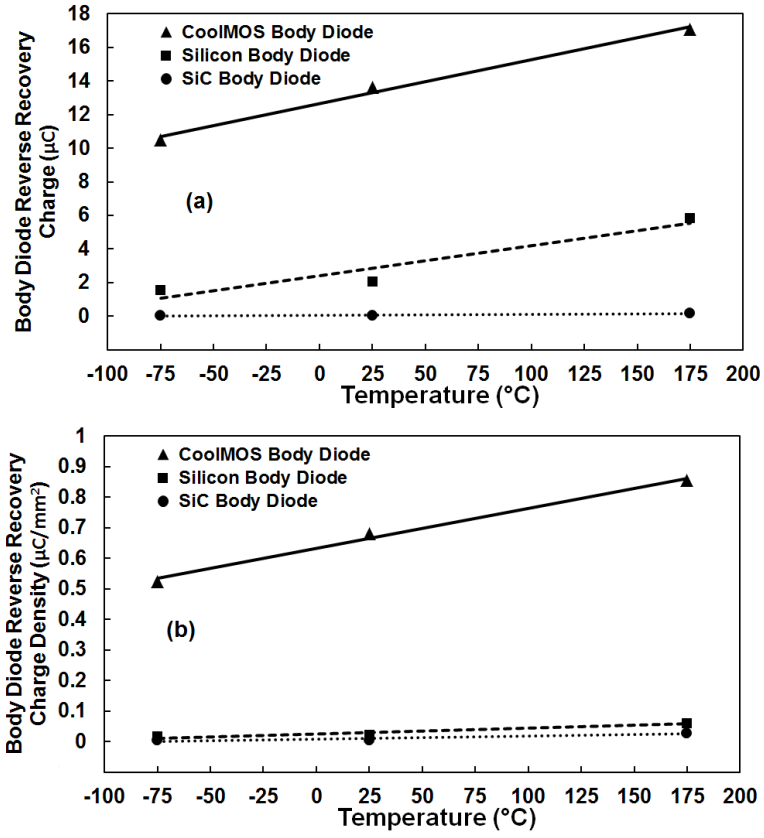


Figure 5.10: Reverse recovery (a) charge and (b) charge density stored in the body diode as a function of temperature for all 3 technologies with a forward current of 2 A.

(where the reverse recovery current is negative). The reverse recovery charge density is also the calculated reverse recovery charge per unit area of device die from Figure 5.16.

In Figure 5.10(b) the reverse charge density is shown as a function of temperature in terms of μC/mm^2 where it can be seen that the silicon power MOSFET (due to its large die area) and SiC MOSFET (due to its negligible recovery charge) have low reverse charge per unit area compared with the CoolMOS™ device. Due to very significant charge and intermediate die area, the CoolMOS™ device exhibits the highest reverse charge density.

Figure 5.11(a) shows the body diode switching energy as a function of temperature for the 3 technologies switched with a gate resistance of 15 Ω whereas Figure 5.11(b) shows a similar characteristic for the device switched at 150 Ω. As can be seen in this figure,

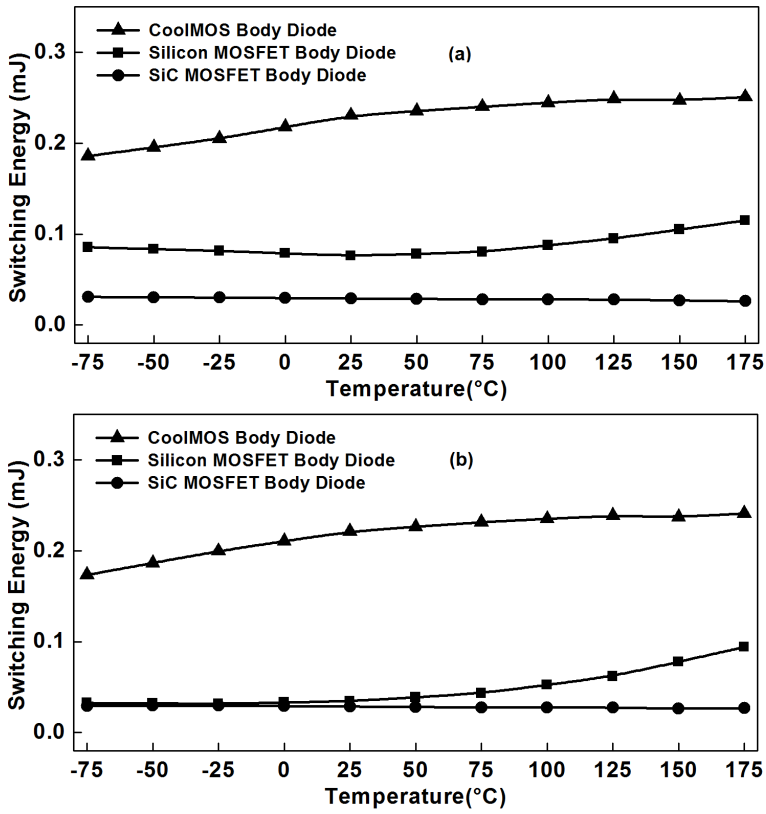


Figure 5.11: The switching energy of body diodes with low-side MOSFET switching with (a) $R_G = 15\ \Omega$ and (b) $R_G = 150\ \Omega$.

the switching energy of SiC device is nearly temperature invariant as would have been expected from its reverse recovery performance as seen in Figure 5.7 while the switching energy of the CoolMOS™ is increasing with temperature. It is also seen that change of dI/dt by means of the low-side R_G has smaller impact on the switching energy of the SiC and CoolMOS™ device as would have been expected from Figure 5.8(a) and Figure 5.8(c). This is in contrast with the switching energy of the silicon power MOSFET which has significantly reduced with increasing the R_G since the slower switching rates significantly reduces the peak reverse recovery and is inline with the trend seen in Figure 5.8(b). This is also seen for discrete PiN diode where a U-shaped characteristics for the switching energy was observed. Hence, SiC MOSFET and CoolMOS™ device exhibit body diode switching energies that are less dependent of the commutation rate because of the low carrier lifetime in the SiC and the superjunction architecture in the CoolMOS™.

Figure 5.12 shows the calculated body diode switching energy for the 3 device technologies as a function of temperature and switching rate for the (a) SiC MOSFET, (b) silicon power MOSFET and (c) CoolMOS™. As can be seen, the SiC MOSFET body diode has the least switching energy and shows a slight decrease as temperature is increased. This slight change is due to the fact that the switching rate in SiC MOSFET increases with temperature hence, the switching is more efficient. The body diode of the silicon power MOSFET has a higher switching energy that generally increases with temperature and the switching rate, i.e. increases as the gate resistance is reduced due to increasing peak reverse recovery current. As the switching rate is increased, the peak voltage overshoot and the peak reverse recovery both increase, hence, the switching energy of the silicon power MOSFET body diode generally increases with the switching rate. The switching energy of the body diode in the silicon power MOSFET also exhibits the highest temperature dependency as a result of temperature dependent minority carrier lifetime.

The CoolMOS™ body diode exhibited the highest switching energy that is generally increased with temperature and switching rate. The R_G determines the switching rate, (the $R_G C_{iss}$ can be regarded as the electrical time constant) thereby resulting in higher peak reverse recovery currents [54] at higher rates as was seen in Figure 5.8. This peak reverse recovery current coupled with the peak voltage overshoot causes significant instantaneous power which increases the switching energy at high switching rates. The increase in switching energy with temperature is due to enhanced carrier lifetime increasing the stored charge. This trend is not affected by the magnitude of current and voltage.

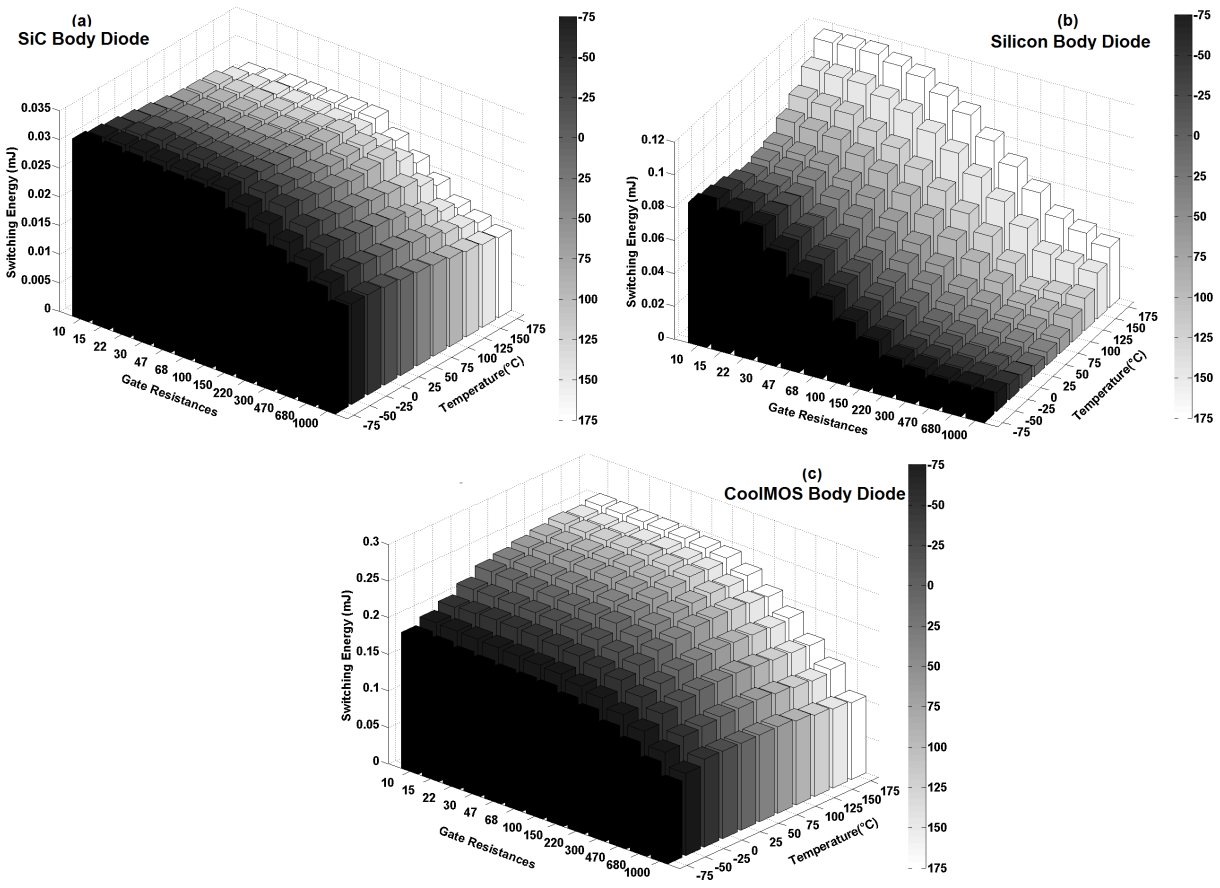


Figure 5.12: Body diodes switching energies as functions of temperature and R_G with 2 A and 100 V; (a) SiC MOSFET, (b) silicon power MOSFET and (c) CoolMOS™.

5.3 Dynamic Surging and Breakdown of Body Diodes

In the converter applications, MOSFET's body diodes may conduct during dead times. This is especially the case in synchronous rectifiers. An example is the replacement of the diode in an asynchronous buck converter with a second transistor to switch. This will help the conversion efficiency of the converter by removing the diode voltage drop. However, in this case there should be a dead time between switching of the transistors, and the inductor's current will flow through the antiparallel diode and/or the body diode of MOSFET. As seen in the previous section, the body diode of silicon power MOSFET and CoolMOS™ is not suitable in these applications due to the slow switching and significant recovery charges. Hence, in these cases, an antiparallel diode is necessary for conduction.

Contrary, SiC MOSFETs have very good recovery performance with low recovery charge and significantly faster transients. Additionally, the switching energy of SiC MOSFET body diodes is also smaller than their discrete PiN diode counterparts, thereby potentially making them a better choice in terms of speed and temperature invariability. If SiC body diodes are utilized in circuits similar to standalone discrete devices, there is also a cost saving as they are already implemented within the MOSFET at no extra expense. However, should the SiC body diodes are to be used as antiparallel diodes, their robustness must be investigated. In this section, robustness of the body diodes has been studied through a range of dynamic surging breakdown tests under hard switching commutation in thermally stressed conditions. The breakdown limits of the technologies are compared under different temperatures, forward current and drain-source voltages.

Figure 5.13 shows how the gate pulse duration can determine the magnitude of current that is stored and eventually forced into the devices during switching. The duration of the charging gate pulse on the low side transistor has been varied from 50 μs to 1000 μs while

the switching pulse has a fixed duration of 20 μs. The inductor size and the pulse length determine the level of the current, which in the case of Figure 5.13 is 450 μH. Hence, the current through the device is changed from just a few Amperes to current magnitudes capable of destroying the device. The tests are performed in –75 °C, 25 °C and 175 °C so as to understand the effect of temperature on the technologies breakdown limits.

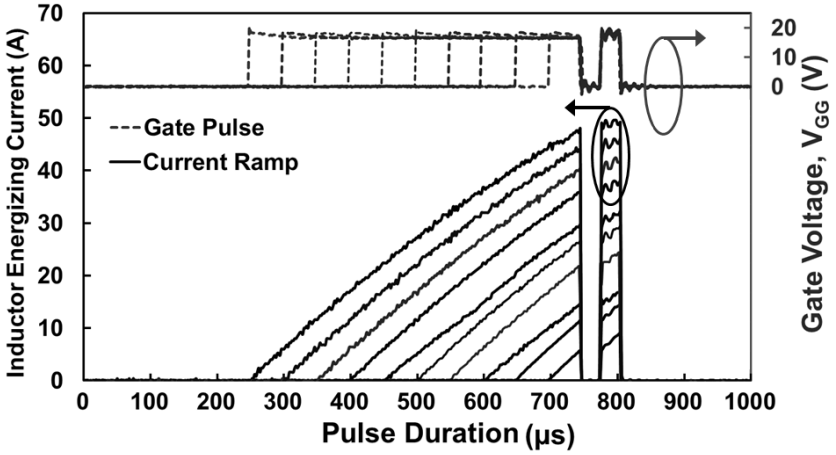


Figure 5.13: Pulse length of the lower-side MOSFET's gate voltage will determine the current; here with a 450 μH inductor.

The results of these measurements are shown in Figure 5.14(a) for the SiC MOSFET, Figure 5.14(b) for the silicon power MOSFET and Figure 5.14(c) for the CoolMOS™ device all switched at 25 °C with 100 V. In Figure 5.14(a), the results show that the SiC MOSFET body diode fails during reverse recovery with a forward current of 42 A. Subsequent checks on the failed device showed that the body diode terminals were short circuited. As can be seen from Figure 5.14(a), the increase in the forward current does not have any significant impact on the negligible reverse recovery charge of the SiC device. Figure 5.14(b) shows a similar set of measurements for the body diode of the silicon power MOSFET. As can be seen in Figure 5.14(b), the current level for the destruction of the body diode has decreased to 34 A. Figure 5.14(b) also shows that unlike the

case of SiC device; the increase in the forward current has a considerable impact on the level of the reverse recovery current in the body diode of the silicon power MOSFET. Figure 5.14(c) shows the same measurements for the CoolMOS™ device where it can be seen that the latching current is approximately equal to that of the SiC MOSFET. The same trend for failure mechanism in superjunction MOSFETs is also previously seen in [115]. These measurements were also performed at different supply voltages for the 3 device technologies. The R_G used in all the measurements shown in Figure 5.14 is 10 Ω. Reducing the gate resistance will increase the turn-off dV/dt across the body diode, thereby increasing the displacement current of the drain to body depletion capacitance. This will cause a higher voltage drop across the source to body parasitic resistance which can further trigger body diode failure through parasitic BJT latch-up. Hence switching at faster rates will increase the likelihood of device failure. Very low minority carrier lifetime and small die area in Silicon Carbide means that there is minimal recovery charge during turn-off. Hence, the primary cause of failure in Silicon Carbide MOSFET body diode is the high dV/dt in hard commutation conditions due to high switching rates. These high switching rates will lead the device to failure based on the first path of BJT latch-up described in section 5.1.2 since the high dV/dt during body diode turn-off results in a displacement current through the drain-body capacitance which coupled with the body resistance induces a gate voltage which might trigger the parasitic BJT. Also higher thermal resistance of SiC device (due to smaller size) causes high junction temperatures and increase of body resistance and hence is detrimental to the robustness of device.

In silicon Power MOSFET, where the thermal resistance is lower than SiC MOSFET, the high reverse recovery charge is the primary cause of failure based on the second path of BJT latch-up described in section 5.1.2. This is in addition to the high instantaneous power where the peak voltage overshoot and peak reverse recovery current coincide. Here,

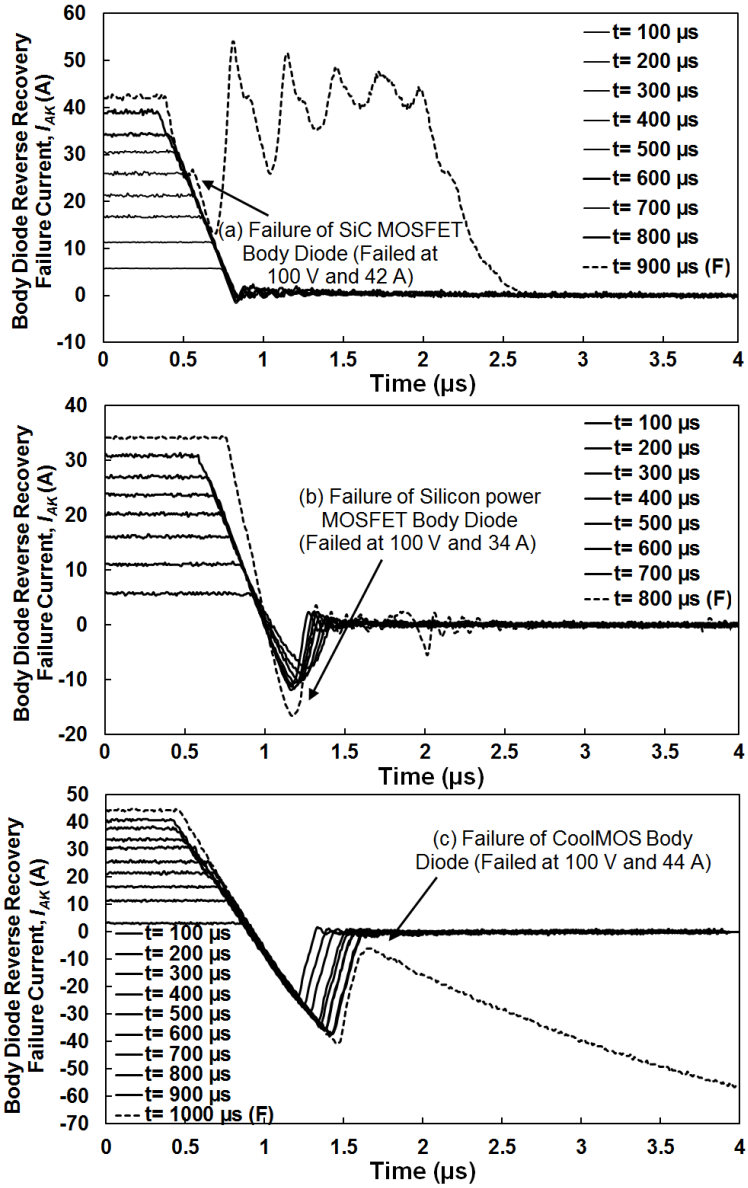


Figure 5.14: Point of failure in body diode forward and reverse currents for the body diode of (a) SiC MOSFET (fail at 42 A), (b) silicon power MOSFET (fail at 34 A) and (c) CoolMOS™ (fail at 44 A), all at 100 V.

the high recovery current flows laterally in the P-body and triggers the parasitic BJT. On the other hand, in the case of CoolMOS™ device, the excessive snappy recovery of the device will result in high peak voltage overshoots and associated dV/dt which is the

primary basis for failure according to the third path of latch-up described in section 5.1.2.

Hence in SiC MOSFET, the device failure is during body diode turn-off whereas in silicon Power MOSFET and the CoolMOS™, the failure is due to the reverse recovery in body diode. This is beneficial for SiC devices as it is easier to control the turn-off dV/dt of the device than to control the amplitude and snappiness of the reverse recovery current.

Figure 5.15(a) shows the maximum forward current at different supply voltages for the 3 device technologies at 100 V and 25 °C. It can be seen from Figure 5.15 that the latching current reduces with increasing supply voltage for all technologies. This is

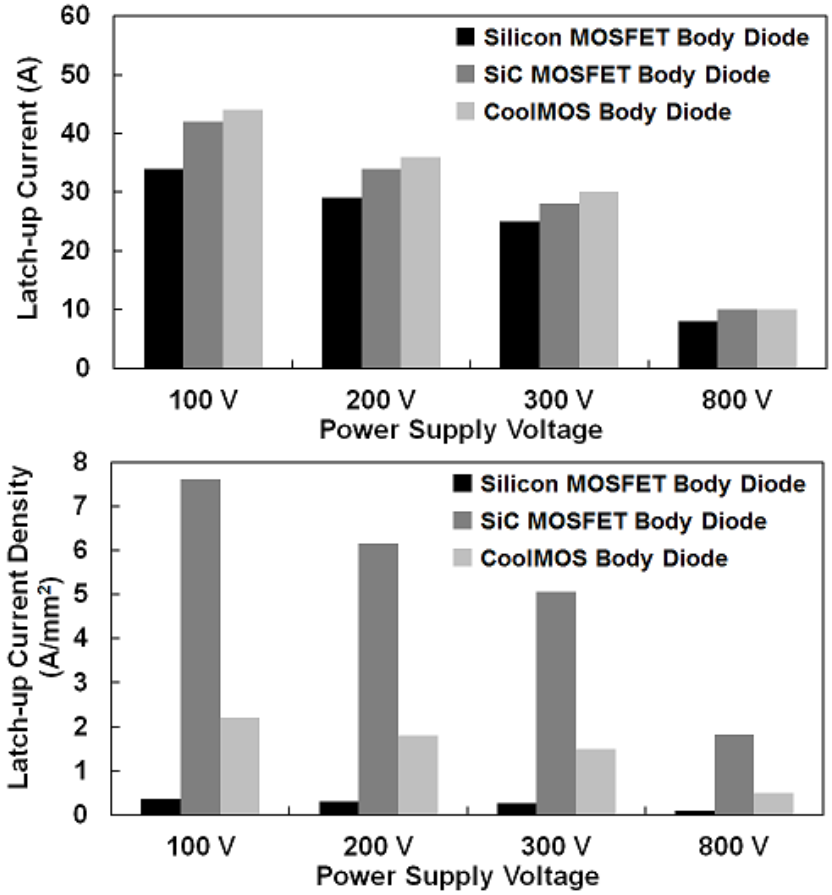


Figure 5.15: (a) The latch up current and (b) The latch-up current density, both as a function of supply voltage for the 3 technologies at 25 °C.

due to the enhanced electrical stress in terms of higher dV/dt and dI/dt with increasing voltage. The latching currents are in close proximity between the CoolMOS™ and the SiC MOSFET (within about 4% margin of difference) for all supply voltages. Figure 5.15(b) shows that the SiC MOSFET has the highest latch-up current density followed by the CoolMOS™ device and the silicon power MOSFET. This is due to the fact that in the case of the SiC MOSFET, in spite of having the smallest active area the device exhibits as much robustness as the CoolMOS™ device. At the 800 V measurements, the latch-up current of body diodes of both the SiC MOSFET and CoolMOS™ device are measured as matching at 10 A, despite the slightly lower ratings of the CoolMOS™ device.

Figure 5.16 shows the picture of the physical die sizes which correlates with the thermal resistance and input capacitances stated on the datasheets. The SiC MOSFET device, due to its wide bandgap characteristics and therefore lower on-resistance per cell, has the smallest die area which in turn is responsible for its high thermal resistance. This means that the device has a smaller thermal mass which results in higher temperature excursions. Hence, in the case of SiC devices with smaller areas, the current density is also a critical

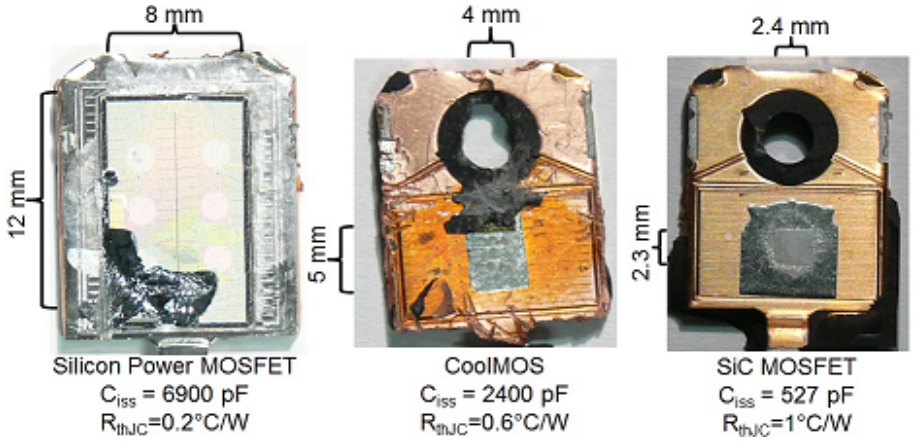


Figure 5.16: Die sizes of the 3 technologies showing that the SiC MOSFET has the smallest die area, followed by the CoolMOS™ device and the silicon power MOSFET resulting in the highest thermal resistance in SiC MOSFET.

parameter in determining BJT latch-up during the turn-off transient in the body diode, since the higher temperature further increases the body resistance. Similar to the silicon power MOSFET, the CoolMOS™ device is also made of silicon, however partly due to its slightly lower ratings as well as benefiting from advanced superjunction technology, the CoolMOS™ device has a smaller die size compared to its silicon counterpart. The silicon power MOSFET has the largest die area which can fit in a TO-247 device packaging.

The impact of temperature on the latch-up current for different voltages is plotted in Figure 5.17(a) and Figure 5.17(b) respectively for 100 V and 200 V measurements of silicon power MOSFET, SiC MOSFET and the CoolMOS™ body diodes as the maximum forward current prior latch-up at –75 °C, 25 °C and 175 °C. It can be seen from these figures that increasing the temperature significantly reduces the latch-up current for the silicon power MOSFET and SiC MOSFET while the temperature dependency of the CoolMOS™ is less. In the case of the SiC device, the reduction of the maximum forward current for latch-up is purely due to the increase of body resistance. This is because as seen previously in Figure 5.7, temperature has negligible effect on reverse recovery of the SiC device and as will be seen in Figure 5.18, the dV/dt is also temperature invariant in the SiC device (at least in high switching rates which are prone to latch-up). Hence, the latch-up is mainly impacted by the body resistance. This is not the case for silicon power MOSFET and superjunction CoolMOS™ where considerable reverse recovery is present.

In the case of the silicon power MOSFET, the reduction of the latch-up current with temperature can be accounted for by the significant temperature dependency of reverse recovery of the device as shown in Figure 5.5. As can be seen, the CoolMOS™ device is the least temperature dependent. This is due to the fact that neither reverse recovery nor its snappiness exhibit a significant change with temperature increase as was seen in Figure 5.6. Also, the P-body is more highly doped compared with the SiC device due to

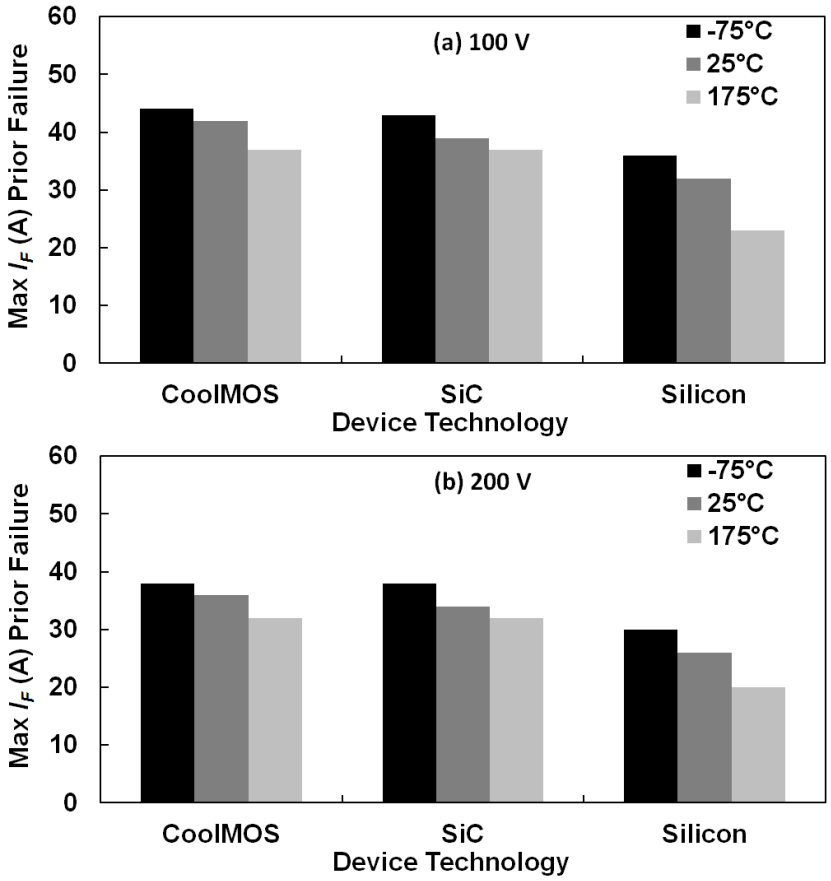


Figure 5.17: Maximum forward current prior latch-up at –75 °C, 25 °C and 175 °C for all 3 devices body diodes at (a) 100 V and (b) 200 V power supplies.

the superjunction structure and hence is less temperature variant. This is because the mobility is reduced at higher doping levels. It also reduces with an increase of temperature. Therefore, at higher doping levels, the impact of temperature is less pronounced [5].

The temperature dependence of dV/dt has been determined through measurements and is shown in Figure 5.18(a) for the silicon power MOSFET, Figure 5.18(b) for the SiC MOSFET and Figure 5.18(c) for the CoolMOS™ body diodes when switched with a 100 V supply. It can be seen from Figure 5.18(a) that dV/dt decreases as temperature increases in silicon power MOSFET. At –75 °C, there is significant voltage overshoot across the diode with oscillations. This correlates with Figure 5.5 where the snappiness of

the reverse recovery characteristics can be seen to increase as temperature reduces for the silicon power MOSFET. The reason for the increasing dV/dt with reduced temperatures is the carrier lifetime dependence on temperature. It is known from the physics of PiN diodes that the voltage across the diode starts rising at the point when the minority carriers have been extracted from the drift region which forms a negative current. At this point, the charge density in the diode can no longer support the current through it and electric fields start to form at the P^+N^- and N^-N^+ junctions thereby depleting them of carriers. As this occurs, the remaining charges in the drift region recombine at a rate that depends on the minority carrier lifetime. At low temperatures, where the lifetime is reduced, the tail current in the reverse recovery characteristic is snappy and can cause oscillations. At high temperatures, where the lifetime is high, there is a long tail current. This is evident in Figure 5.5 for the silicon power MOSFET. However, BJT latch-up also depends on the resistance of the P-body which increases with temperature. Hence, as the temperature is increased, although dV/dt reduces (which on one hand will make the BJT latch-up less probable), the P-body resistance increases (which makes the BJT latch-up more probable). Therefore, the conclusion from the measurements in Figure 5.18(a) is that in the case of silicon power MOSFET, the positive temperature coefficient of the P-body resistance is the primary determinant of the temperature dependence of BJT latch-up. This also agrees with the theory previously explained in section 5.1.2.

Figure 5.18(b) shows that dependence of the body diode dV/dt on temperature in SiC MOSFET is small enough for it to be considered temperature invariant. This correlates with the body diode turn-off currents presented in Figure 5.7, which was also temperature invariant. Again, this is as a result of the significantly smaller minority carrier lifetime in SiC and the minimum reverse charge stored in the device, hence, the dependence of the turn-off characteristics on temperature is negligible. However, the dependence of the

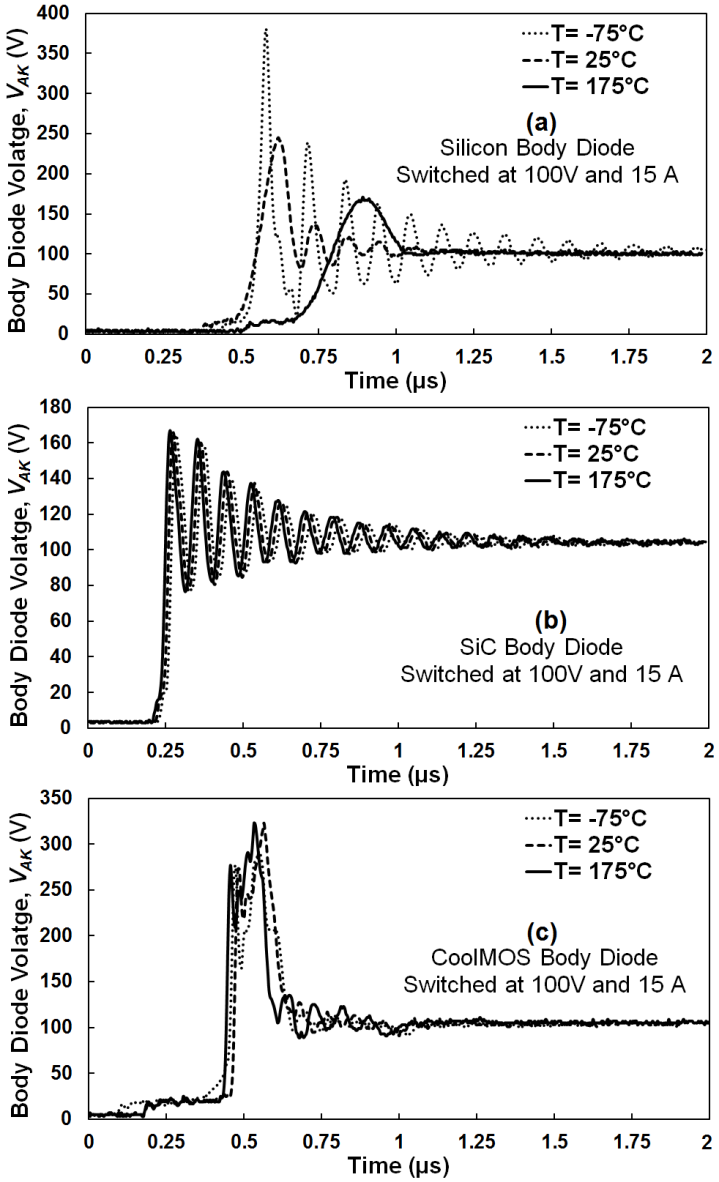


Figure 5.18: Turn-off voltage transients of (a) silicon power MOSFET, (b) SiC MOSFET and (c) CoolMOS™ body diode showing temperature dependency of silicon power MOSFET while SiC MOSFET and CoolMOS™ are temperature invariant.

latch-up current on temperature is more evident as shown in Figure 5.17(b). This is due to the temperature dependence of the P-body resistance which increases with temperature thereby forward biasing the parasitic BJT quicker.

The ringing in the body diode of the SiC MOSFET is similar to that of SBDs, simply because the lack of reverse charge makes it to act somewhat similar to a unipolar diode. Figure 5.18(c) shows that the dV/dt characteristic of the CoolMOS™ body diode is also relatively temperature invariant which again correlates with Figure 5.6. The high voltage overshoot and dV/dt alongside the significant reverse recovery charge of the superjunction technology is also seen in [115]. As previously shown in Figure 5.16, the CoolMOS™ device has a larger die (and smaller thermal resistance) compared with the SiC MOSFET. Although its thermal resistance is higher than the silicon die (and die area is smaller), it still maintains a higher latch-up current compared to the silicon power MOSFET. This is because in standard MOSFETs, the hole current generated by charging of the depletion capacitance flows laterally through the P-body resistance and if it is large enough it latches up the BJT. In contrast, in superjunction technology, the hole current flows upward through the P-type pillar before it reaches the metallization and the lateral current in the P-body is reduced and consequently the possibility of triggering the BJT is also reduced.

Figure 5.19(a) and Figure 5.19(b) show the voltage and current transient characteristics of the three body diode technologies switched at 25 °C and $R_G = 10\ \Omega$ with 800 V supply using the test rig shown in Figure 3.5. The difference in latch-up current seen in Figure 5.15 can be explained here. In the case of the CoolMOS™, the higher forward latching current compared to silicon power MOSFET is due to the effect of the superjunction structure on the suppression of lateral current flow needed to trigger the parasitic BJT. This is despite having a higher recovery charge and more snappy reverse recovery and shows the significant impact of the superjunction structure on delaying the BJT latch-up. In the case of the SiC MOSFET, the higher forward latching current is due to the lower instantaneous switching power resulting from insignificant reverse recovery charge and lower voltage overshoot (this is in spite of having a larger thermal resistance than

the silicon power MOSFET). It can be seen from Figure 5.19 that the CoolMOS™ device has the highest voltage overshoot at 800 V followed by the silicon power MOSFET which confirms the low voltage measurements in Figure 5.18. Figure 5.19(b) shows the reverse recovery characteristics of the three technologies at 800 V with a forward current of 5 A. Again, the CoolMOS™ device has the largest reverse charge while the SiC MOSFET has the smallest. The highest switching energy of the CoolMOS™ device does not have a negative effect on its immunity to BJT latch-up because of the superjunction structure which suppresses lateral currents during reverse recovery [116]. The same oscillations/ringing in the SiC device is also seen here, as well as the semi-snappy recovery of the silicon power MOSFET and snappy recovery of the CoolMOS™.

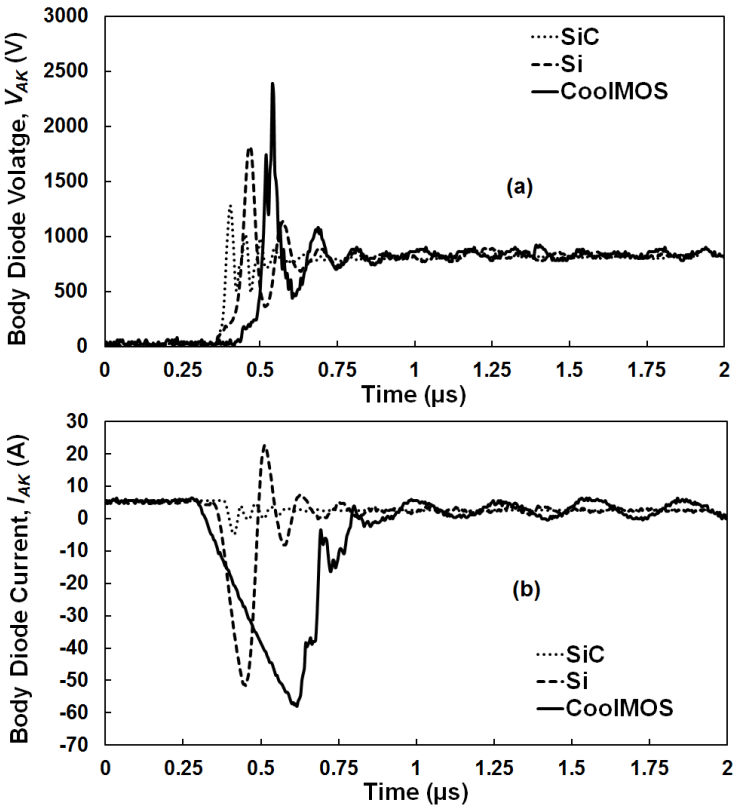


Figure 5.19: The 800 V measurements showing body diode's (a) voltage and (b) current.

5.4 Summary

The body diode switching performance and electro-thermal robustness of 1.2 kV SiC MOSFET and silicon power MOSFET as well as 900 V CoolMOS™ devices were compared experimentally. The body diode reverse recovery characteristics were also compared at different switching rates, temperatures and supply voltages. It was seen experimentally that SiC MOSFETs exhibit the lowest switching energy followed by the silicon power MOSFET and the CoolMOS™ device. This is due to the fact that the carrier lifetime in SiC MOSFET is the lowest; hence, the PiN body diode stores the least amount of charge during forward conduction mode. The reverse recovery charge in the CoolMOS™ device was also the largest as a result of the superjunction structure resulting in excess minority carrier storage. Additionally it was seen that the total reverse charge and peak reverse current in silicon power MOSFET and CoolMOS™ devices increase with the temperature and forward current, whereas in the SiC MOSFET, these parameters are temperature invariant. In addition, the robustness of the body diodes was studied during hard turn-off at different temperatures. This was investigated by increasing the forward current until latch-up was achieved. The results showed that the CoolMOS™ and SiC MOSFETs had the highest latch-up current followed by the silicon power MOSFET. Furthermore, the SiC MOSFET showed the highest latch-up current density (since it has the smallest die area) followed by the CoolMOS™ and the silicon power MOSFET.

Chapter

6 Analysis of Crosstalk in Silicon and SiC Power Converters

An important characteristic in the application of Si-IGBTs in power converters which may also occur in high voltage SiC MOSFETs is crosstalk. Hence it is important to investigate the possibility and the effect of crosstalk in SiC MOSFETs as well and to provide a comparison with Si-IGBTs. In this chapter, the temperature and dV/dt dependence of crosstalk will be analyzed for silicon IGBT and SiC MOSFET power modules with similar rating. As will be discussed, due to smaller Miller capacitance resulting from a smaller die area, the SiC module exhibits smaller shoot-through currents compared with similarly rated Si-IGBTs in spite of switching with a higher dV/dt and with lower threshold voltage. However, due to high voltage overshoots and ringing from the SiC Schottky diode, SiC modules exhibit higher shoot-through energy density and induce voltage oscillations in the DC-link. Measurements show that the shoot-through current exhibits a positive temperature coefficient for both technologies the magnitude of which is higher for the Si-IGBT, i.e. the shoot-through current and energy shows better temperature stability in the SiC power module. This has also been validated through thermal measurements evaluating the temperature rise as the result of shoot-through.

The effectiveness of common techniques for mitigating shoot-through, including application of bipolar gate drives, multiple gate resistance switching paths as well as external gate-source and high frequency de-coupling capacitors have been evaluated for both technologies at different temperatures and switching rates by connection of a range of R_G. The results show that some solutions are less effective for SiC MOSFETs because of lower threshold voltages and smaller margins for negative gate bias on the SiC MOSFET. The smaller negative offset of the gate voltage in SiC devices is due to the less stable gate dielectric (SiC/SiO_2) interface which means there is potentially more threshold voltage shifting and fixed oxide charge trapping under high temperature negative bias. Good and reliable SiC/SiO_2 interfaces is still a research goal for SiC device manufacturers. This is not an issue in silicon devices, where a more stable and defect-free gate dielectric interface means that negative voltages as high as 20 to 30 V can be used to mitigate crosstalk.

Models for evaluating the parasitic voltage have also been developed for diagnostic purposes and shown to provide accurate means of predicting the crosstalk severity. These results are important for converter designers seeking to use SiC technology.

6.1 Principles of Crosstalk

Crosstalk is an important factor that must be evaluated when using power semiconductor devices in converters. It has also been referred to as parasitic turn-on, false turn-on, self-turn-on, misfiring, etc [117]. Crosstalk occurs when the device is unintentionally switched on as a result of the intentional switching of a device in the same phase leg. This unwanted turn-on can impose serious reliability concerns since it can result in semi-short-circuits with high currents flowing through the power devices thereby resulting in high thermal losses and unnecessary electro-thermal stress on the device wire-bounds and die [118].

Crosstalk normally happens in synchronous DC-DC converters or in three-phase DC-AC inverters where the devices are intended to turn on with appropriate dead-times allocated between the switching edges [119, 120]. As one device is turned on, the dV/dt imposed on the complementing device in the same phase leg results in charging Miller capacitance and a consequent current flow into the gate resistance, causing an induced voltage capable of triggering the device to on-state if it is greater than its threshold voltage [121].

The main contributors to the magnitude of the shoot-through current resulting from crosstalk are the Miller capacitance and its ratio compared with the input capacitance of the device, the gate resistance connected to the device (which includes the internal gate resistance of the module), the switching rate, the threshold voltage of the device and its operating temperature. Similar to the Equation 4.23 derived earlier, Equation 6.1 shows the parasitic gate-source (V_{GS} for MOSFET) or gate-emitter (V_{GE} for Si-IGBT) voltage as a function of the gate resistance (R_G), Miller capacitance (C_{GD}) and turn-on dV/dt.

$$V_{GS} = R_G \cdot C_{GD} \cdot \frac{\mathrm{d}V_{DS}}{\mathrm{d}t} \cdot \left(1 - e^{\frac{-t}{R_G \cdot (C_{GD} + C_{GS})}} \right) \tag{6.1}$$

Figure 6.1 shows an example of a parasitic (unintended) gate voltage across a SiC MOSFET during turn-on and turn-off of a complementing device. The induced positive spike in V_{GS} during turn-on and the negative spike during turn-off is due to the polarity of the Miller capacitance charge and discharge current. The mechanism is explained in [122]. To mitigate this problem, techniques like negative gate bias through a bipolar driver and multiple resistive paths for turn-on/turn-off have been developed.

This chapter aims to evaluate the problem of crosstalk as well as the effectiveness of the solutions for SiC MOSFETs compared with silicon IGBTs. The desire to maximize

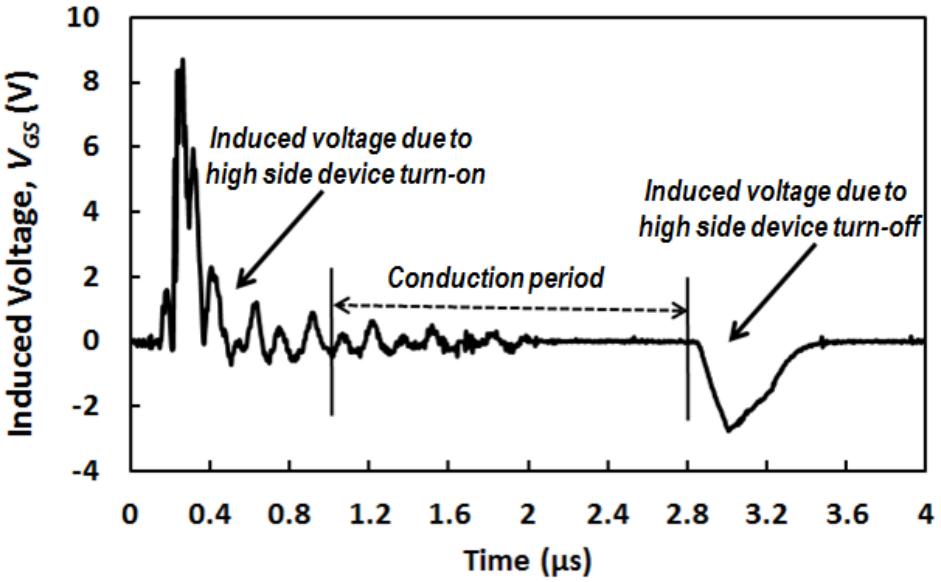


Figure 6.1: Measured induced gate voltage on a Si-IGBT with dV/dt of 10 $kV/\mu s$.

power density and increasing the switching frequency gives SiC an advantage, however, crosstalk will cause problems since the shoot-through energy is proportional to the switching rate [123]. SiC MOSFETs have lower threshold voltages and switch with higher dV/dt both of which may contribute to higher shoot-through currents. However, the Miller capacitance in SiC MOSFETs is significantly smaller than that in silicon IGBTs because of its smaller die area [124]. The temperature coefficients of the threshold voltages in both technologies will also be critical for the impact of crosstalk on the performance at higher temperatures. Furthermore, the impact of oscillations in the SiC Schottky diode on the DC link voltage and the shoot-through energy also needs further characterization.

In this regard, this chapter presents a comprehensive analysis of crosstalk in both technologies by providing modeling approaches for predicting crosstalk, and experimental measurements for evaluation of the power devices response to crosstalk conditions. These are used to analyze the switching rate (dV/dt) and temperature dependence as well as to compare the technologies. Additionally, the effectiveness of the mitigation techniques

that are applicable to crosstalk is investigated as well as the impact of crosstalk on power converters performance, if not mitigated, in terms of module temperature rise.

6.2 Crosstalk Models

To develop a diagnostic tool for the prediction of the crosstalk, several modeling approaches are considered, all of which are based on the capacitive divider in the device.

- The first modeling approach is described in [125] where the maximum possible voltage at turn-on as V_m of the device is utilized in Equation 6.1, along with time instance it occurs as T_m. This approach is the simplest method of modeling the induced voltage and does not consider the parasitic elements in the circuit like the stray inductance. Also it does not consider the changes in the dV/dt of the circuit. Hence due to its simplicity, it lacks accuracy. An example of this method output is shown in Figure 6.2 where the induced gate voltage is shown together with the experimental measurements. This method results in following expression for V_{GS}:

$$V_{GS} = R_G \cdot C_{GD} \cdot \frac{V_m}{T_m} \cdot \left(1 - e^{\frac{-t}{R_G \cdot (C_{GD} + C_{GS})}} \right) \tag{6.2}$$

- The second approach involves the use of the measured dV/dt across the device to estimate the induced gate voltage, i.e. the measured dV/dt is used in 6.1. This method is more accurate as it considers the dynamic changes of the dV/dt of the device in the circuit and also indirectly considers the impact of parasitic elements on the switching rate. However, using this method requires having the voltage transient measurements of the circuit which necessitates some initial characterisations. An example of this method output is shown in Figure 6.3.

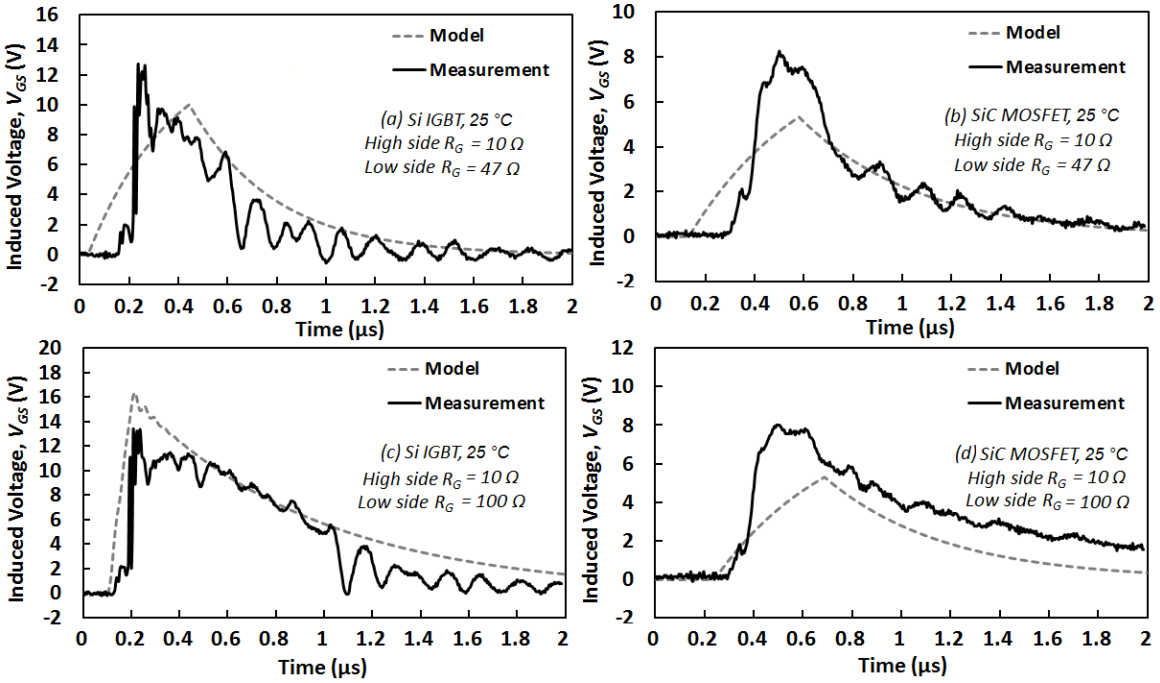


Figure 6.2: Modeled and measured induced gate voltage by first modeling approach.

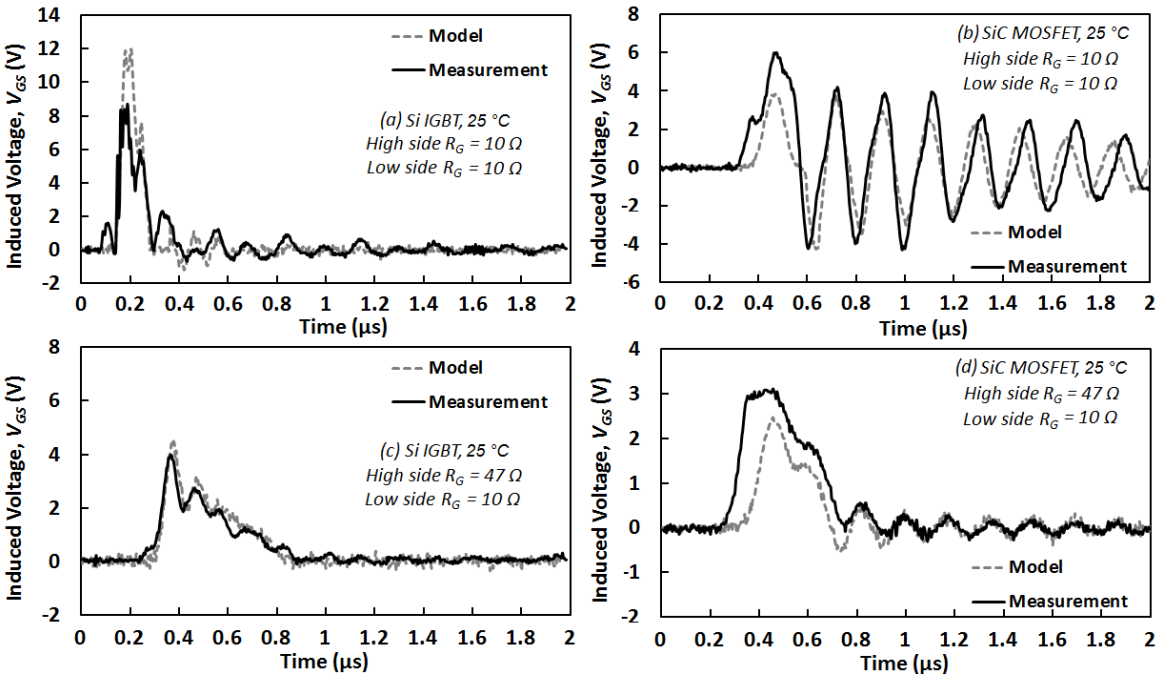


Figure 6.3: Modeled and measured induced gate voltage by second modeling approach.

- The third method, which is common, uses simulation software such as PLECS or SPICE to model the characteristics of the device in a circuit emulator. This method is capable of providing the characteristics of the induced gate voltage as a function of the circuit parasitic components (inductances and capacitances) and is user friendly. However, the temperature dependency of the shoot-through current is not modelled accurately because the temperature coefficient of the threshold voltage and on-state resistance is not properly accounted for. Also these software do not provide an standalone solution independent of application of software packages. An example of this method output is shown in Figure 6.4. The high side and low side gate resistances of the complementing devices are specified in the figures.

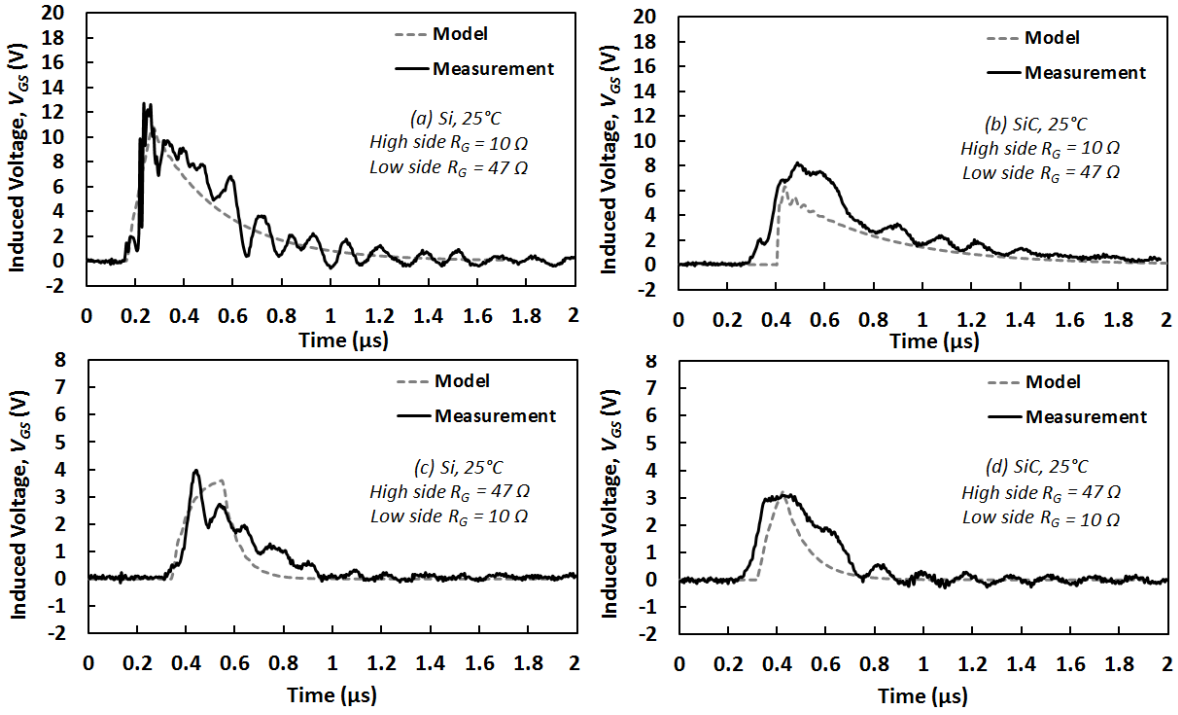


Figure 6.4: Modeled and measured induced gate voltage by third modeling approach (circuit simulator).

- The last method is the method proposed here. The parasitic voltage is modeled by developing a transfer function of the equivalent circuit shown in Figure 6.5. In this figure, the power device that is intentionally switched is modeled as an ideal switch however with a finite dV/dt that falls on the low side power device causing it to be parasitically triggered. In this case, first the equations for the V_G are developed. This is done by using the Kirchhoff's laws in the circuit. Then, having the numerator and denominators of the transfer function, and by using the dV/dt of the intentionally switched device as an input to the transfer function, the induced voltage can be calculated. Details of this method will be described next.

The circuit shown in Figure 6.5 includes the parasitic capacitances of the device, the stray inductances as well as the parasitic resistances and inductances resulting from the circuit layout. These parasitic elements are critical for accounting the possible oscillations in the parasitic voltage transient characteristics [126]. Hence, the model developed can be used to predict the possibility of crosstalk, if a voltage above the threshold voltage of the device is induced on the gate. The model can be used to predict the severity of the shoot-through current (to a certain extent) by comparing the level of the V_{GG} with V_{TH}. The average values for the parasitic elements are used for the development of the model [82], and are applicable when no mitigation technique is applied.

Applying KCL at the gate, source and drain terminals of the circuit in Figure 6.5 will yield 3 equations as shown in Equations 6.3a to 6.3c.

$$\frac{V_G}{R_G + sL_G} + (V_G - V_S)sC_{GS} + (V_G - V_D)sC_{GD} = 0 \tag{6.3a}$$

$$(V_S - V_G)sC_{GS} + \frac{V_S}{sL_S} + (V_S - V_D)sC_{DS} = 0 \tag{6.3b}$$

$$(V_D - V_G)sC_{GD} + (V_D - V_S)sC_{DS} + \frac{V_D - V_{DD}}{R_{Cr} + sL_{Cr}} = 0 \tag{6.3c}$$

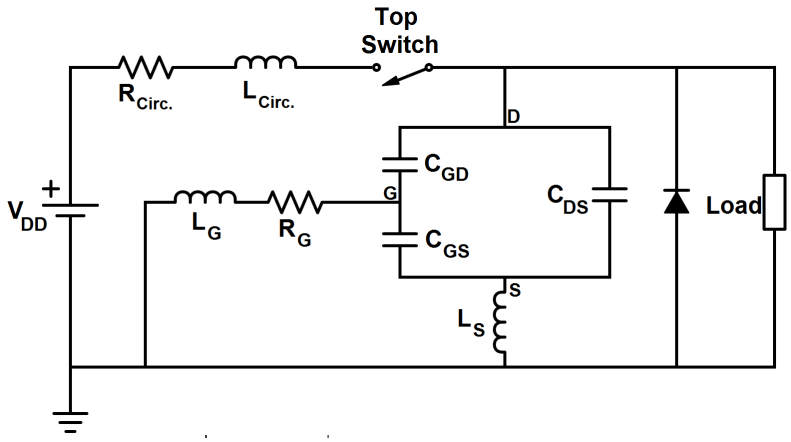


Figure 6.5: Equivalent circuit for modeling the induced gate voltage.

Solving the equations above for the gate voltage will yield the transfer function as shown in Equation 6.4 as:

$$V_G = \frac{N_4 s^4 + N_3 s^3 + N_2 s^2 + N_1 s}{D_4 s^4 + D_3 s^3 + D_2 s^2 + D_1 s + 1} \tag{6.4}$$

where the numerators and denominators are given by:

$$N_4 = L_G L_S V_{DD} \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$

$$N_3 = L_S R_G V_{DD} \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$

$$N_2 = C_{GD} L_G V_{DD}$$

$$N_1 = C_{GD} R_G V_{DD}$$

$$D_4 = (L_{Cr}L_G + L_{Cr}L_S + L_S L_G) \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$

$$D_3 = (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS}) \times (L_{Cr}R_G + L_G R_{Cr} + L_S R_{Cr} + L_S R_G)$$

$$D_2 = L_{Cr}(C_{DS} + C_{GD}) + L_G(C_{GS} + C_{GD}) + L_S \times (C_{DS} + C_{GS}) + R_{Cr}R_G \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$

$$D_1 = R_{Cr} \times (C_{DS} + C_{GD}) + R_G \times (C_{GS} + C_{GD})$$

Table 6.1: Crosstalk model parameters and their values.

Parameter	Unit	Value
C_{GC} (Si-IGBT)	nF	≈ 0.15
C_{GE} (Si-IGBT)	nF	≈ 7.2
C_{GD} (SiC MOSFET)	nF	≈ 0.08
C_{GS} (SiC MOSFET)	nF	≈ 10
L_S	nH	≈ 5
L_G	nH	≈ 5
L_{Cr}	nH	≈ 100
R_{Cr}	Ω	≈ 1
V_{DD}	V	650

The value of dV/dt of the intentionally switched device is implemented as an input to the model. The values of the capacitances used in the model are obtained from the datasheets and the inductances are measured with approximation from the test rig. The results of the model are shown together with experimental measurements in Figure 6.6(a) and 6.6(b) for silicon IGBT and SiC MOSFET half-bridge power modules respectively switched with a high side gate resistance of 10 Ω (resulting in switching dV/dt of up to 10 $kV/\mu s$) and a low side gate resistance of 47 Ω. Moreover, Figure 6.6(c) and 6.6(d) show the results of the model with experimental measurements made with a lower switching dV/dt (by connecting it to a high side gate resistance of 47 Ω) with a low side gate resistance of 10 Ω. It can be seen from Figure 6.6 that the model is able to replicate experimental measurements with good accuracy in both cases. The measurement conditions, where the high side R_G is low (i.e. 10 Ω) and the low side R_G is high (i.e. 47 Ω or higher) are representative of the worst case scenarios for evaluating crosstalk.

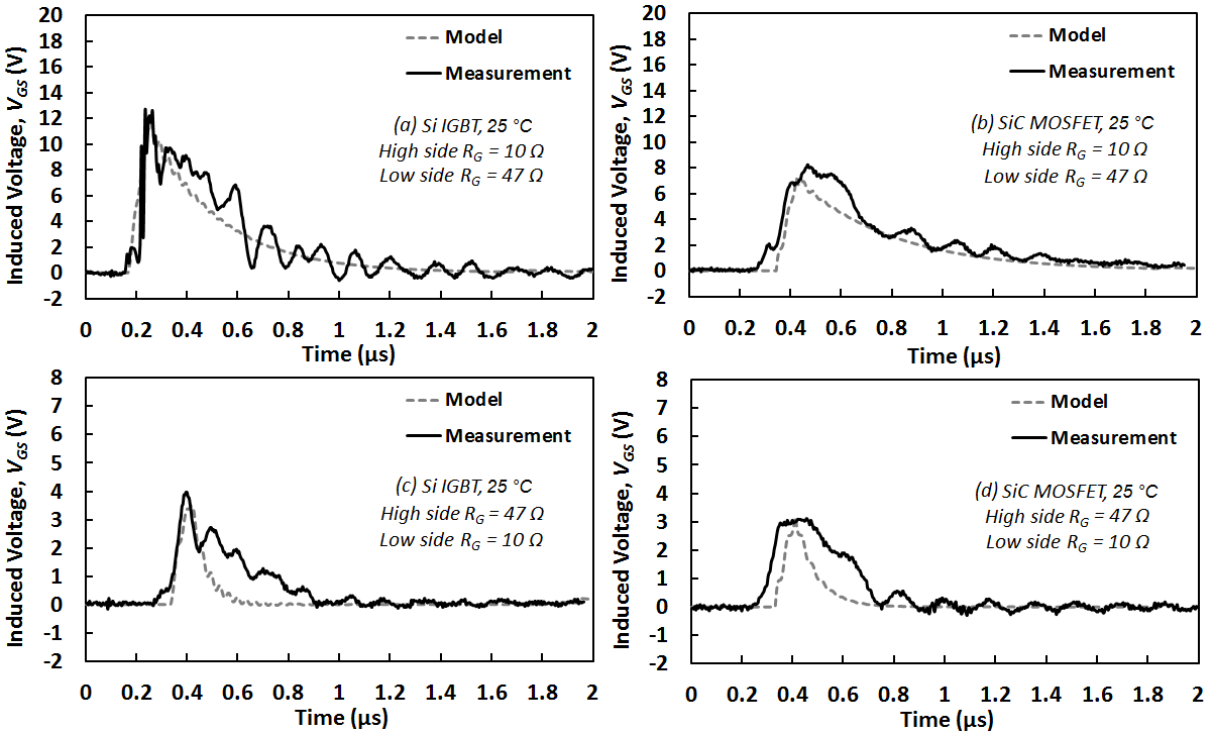


Figure 6.6: Results of the proposed model and measured induced gate voltage transients for Si-IGBT and SiC MOSFET with (a,b) high side $R_G = 10\ \Omega$ and low side $R_G = 47\ \Omega$ and in (c,d) high side $R_G = 47\ \Omega$ and low side $R_G = 10\ \Omega$.

6.3 Experimental Measurements

To evaluate the temperature and switching rate dependence of crosstalk in silicon IGBT and SiC MOSFET power modules, a dedicated test rig has been developed and equipped with a hot plate as well as temperature control and measurement equipment. Since crosstalk entails short-circuiting, a high voltage power supply and extra protection has been applied to the test rig. In the following subsections, first the details of the set-up is presented and then the analysis of the switching rate dependence of the crosstalk is discussed. This is done by changing the range of R_G on both high side and low side devices to vary the applied dV/dt and the induced gate voltage.

The rate at which the output voltage rises/falls (dV_{DS}/dt for MOSFETs and dV_{CE}/dt for IGBTs) depends on the rate at which the Miller capacitance is charged/discharged through the gate resistance. Hence, dV/dt is inversely related to $R_G \cdot C_{GD}$ [5], since the $V_{DS}/\,V_{CE}$ transients occur while the Miller capacitance is being charged/discharged. The Miller capacitance is dependent on the output voltage through the depletion width which is determined by the output voltage. The value of R_G directly impacts the dV/dt and dI/dt rates [127]. The temperature dependence of crosstalk is also analyzed by mounting the modules to a thermal plate to vary the temperature. Additionally, to evaluate the die areas and power densities, the failed power modules are opened up as in Figure 6.7.

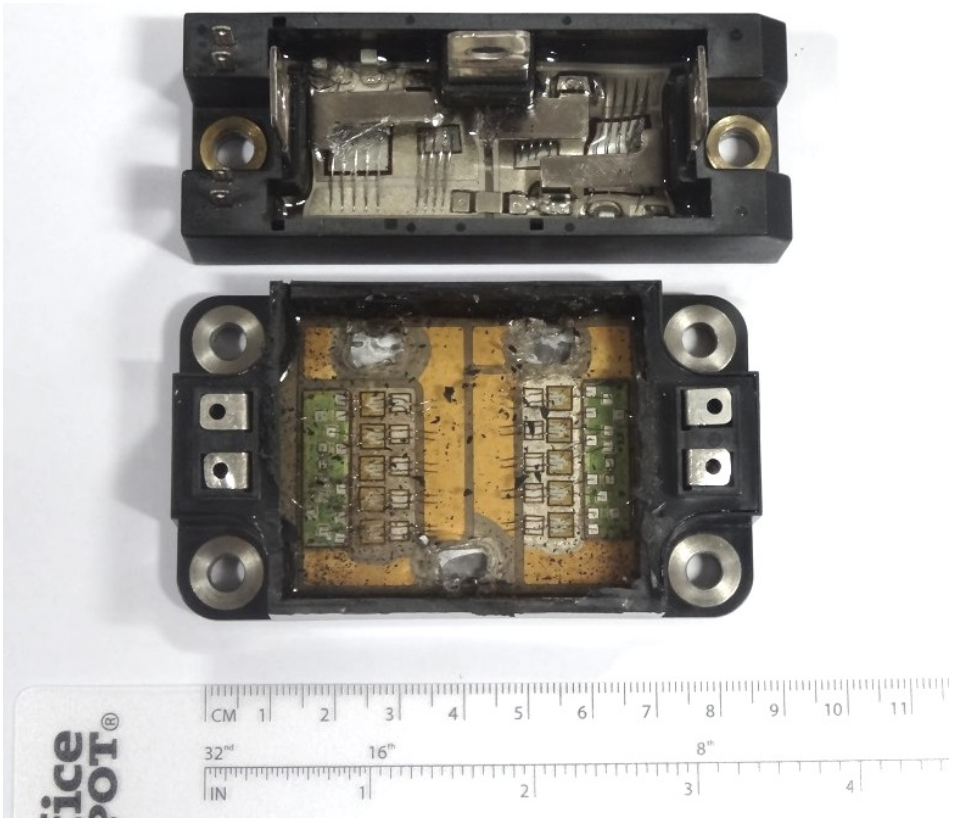


Figure 6.7: The opened packaging of power modules,
(top) Si-IGBT module (bottom) SiC MOSFET module.

As can be seen, the SiC MOSFET module is comprised of 5 dies per device connected in parallel with each die having an area of 16.6 mm^2 thereby resulting in a total die area of approximately 83 mm^2 (0.83 cm^2), whereas the Si-IGBT module comprises of a single die per device with a die area of approximately 105 mm^2 (1.05 cm^2). Given that the modules are of the same rating, this shows that the SiC module has a higher power density.

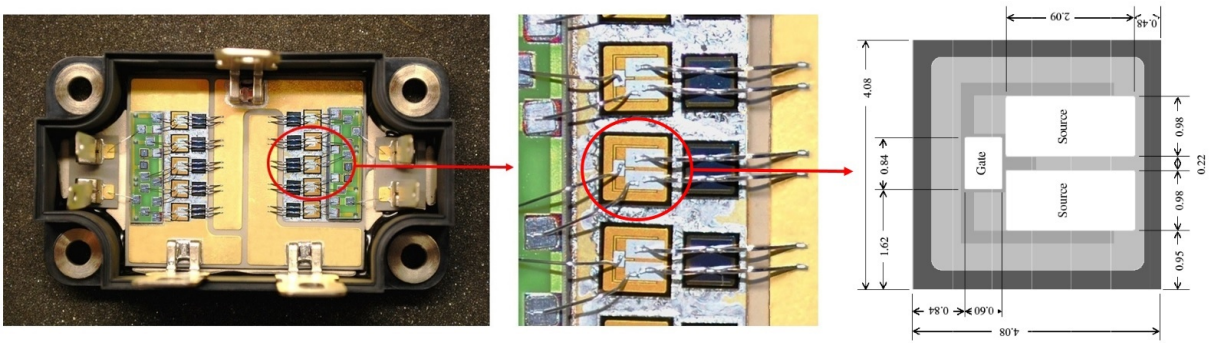


Figure 6.8: Calculation of dies size of the SiC device according to datasheet values.

In the next sections, this information has been used to estimate the shoot-through energy per die area of the devices for a comparable evaluation.

6.3.1 Set Up

The schematic of the test rig is shown in Figure 6.9. The temperatures is varied from room temperature to 120 °C while the switching rate is controlled by a range of R_G from 10 Ω to 100 Ω. This range of R_G is intentionally chosen wide because, as will be analysed in the next sections, the shoot-through current increases with the applied dV/dt and the Miller capacitance of the low side device as well as the gate resistance connected to it. The peak parasitic gate voltage is given by $R_G \cdot C_{GD} \cdot dV_{DS}/dt$ and hence, an increase in any one of the parameters will affect the shoot-through current in a similar way. While further increase of the dV/dt or changing the device's Miller capacitance has not been an option,

to investigate the performance of the device and also the effectiveness of the mitigation techniques at higher shoot-through currents, the low side R_G has been increased from 10 Ω to 100 Ω to replicate these situations [128].

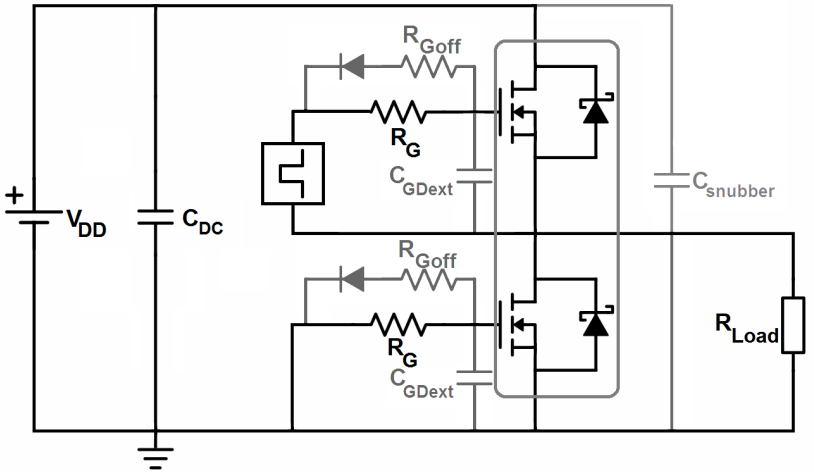


Figure 6.9: The design schematic of the half-bridge measurement circuit along with the possible crosstalk mitigation techniques.

Figure 6.10 shows the experimental system diagram, showing how the measurements system is organised for measurements of chapter 6 based on the circuit schematic provided in Figure 6.9 and is used as the design concept in manufacturing the test rig seen in Figure 6.11. The safety precautions applied are the interlock system, which enforces a mandatory delay to provide enough time for the DC link capacitors to discharge through some discharge resistors in interlock system. Additionally, a multimeter is applied across the DC link capacitor so that its voltage can be read before the door is opened. The applied voltage is 650 volts and the load is a 1 kΩ resistor with a 1 kW power rating connected in parallel to the low side device. The high side device is switched while the low side device is monitored for induced switching. The DC link capacitors have a total capacitance of 320 μF with a voltage rating of 1.2 kV. The silicon IGBT half bridge module is DM2G100SH12AE with a Miller capacitance (C_{GC}) of 0.15 nF and the SiC half

bridge module is CAS100H12AM1 with a Miller capacitance of 0.08 nF. The threshold voltage of the silicon IGBTs range from 5 to 8 V, whereas in the SiC MOSFET it ranges around 2 V. More information on device's parameters can be found in Table 6.2. The gate signal is generated by Agilent AFG3022C controller while the waveforms are captured by LeCroy 104MXs-B digital oscilloscope. The current and voltage waveforms are also captured via calibrated current clamped (Tektronix TCP303 15 MHz) and differential high voltage probes (Rapid GDP-100 100 MHz) as in Figure 6.11 and Figure 6.12.

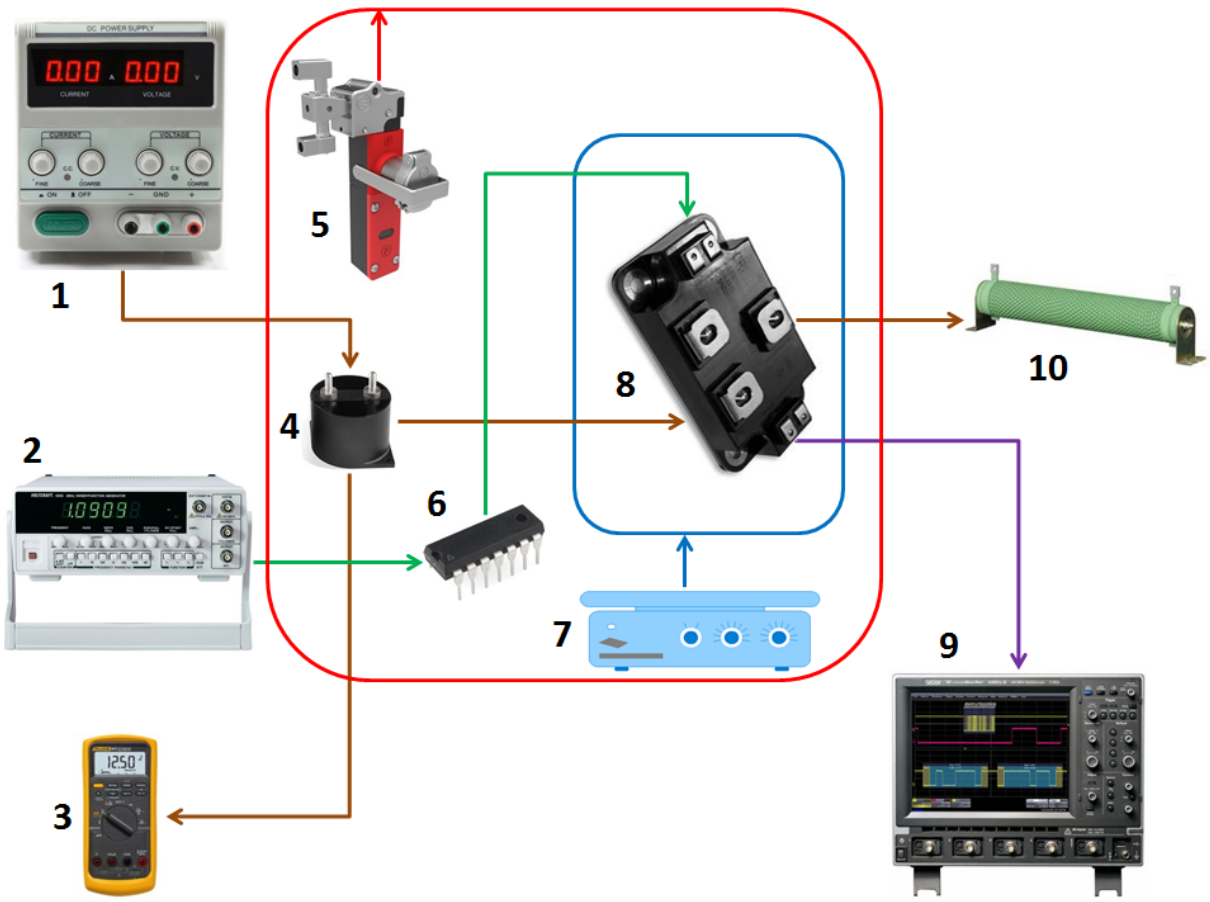


Figure 6.10: Experimental system diagram, showing how the measurements system is organised for the measurements of the chapter 6. The components shown are as follows: 1- Power supply 2- Function generator 3- Multimeter 4- DC link capacitor 5- Interlock 6- Gate drive system 7- Hotplate 8- Power module 9- Oscilloscope 10- Resistive load.

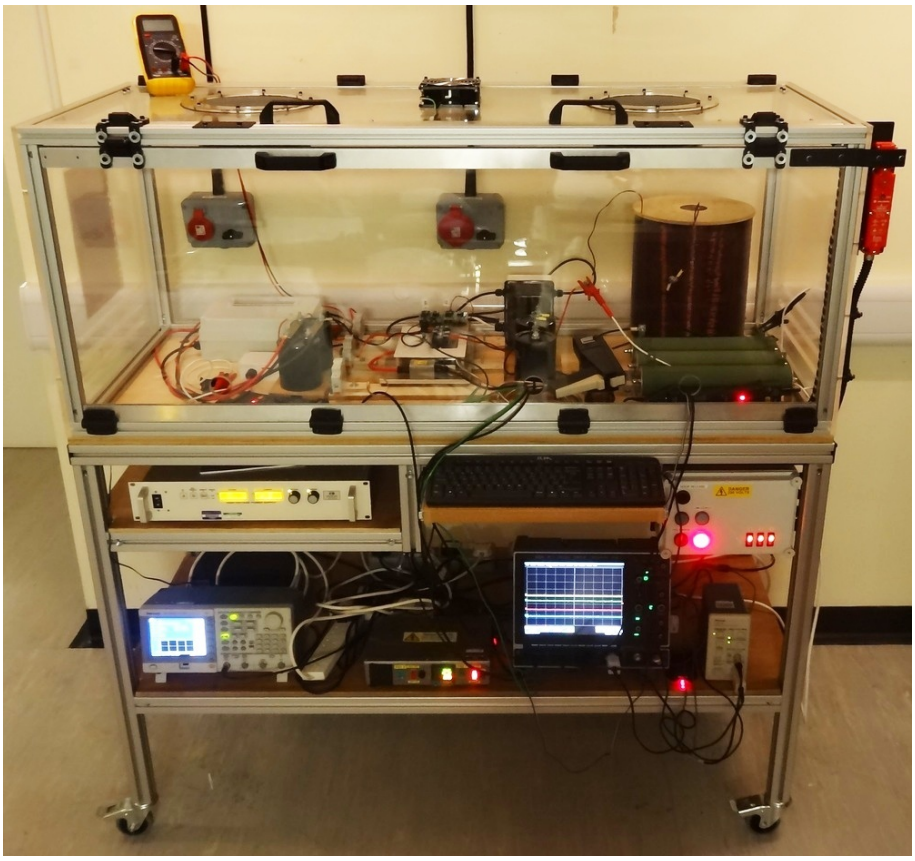


Figure 6.11: The test rig set-up dedicated to crosstalk measurement including the oscilloscope, power supply, the function generator and passive elements of the circuit.

Table 6.2: Comparison of determining parameters of the Si-IGBT and SiC MOSFET power modules used in crosstalk measurements.

Parameter	Unit	Si-IGBT	SiC MOSFET
Voltage	V	1200	1200
Current	A	100	105
Miller Capacitance	nF	0.15	0.08
Threshold Voltage	V	5-8	2-3
Gate Charge	nC	1050	490
Maximum Gate Source Voltage	V	±20	–5/+20
Thermal Resistance Junction-Case	°C/W	0.18	0.16

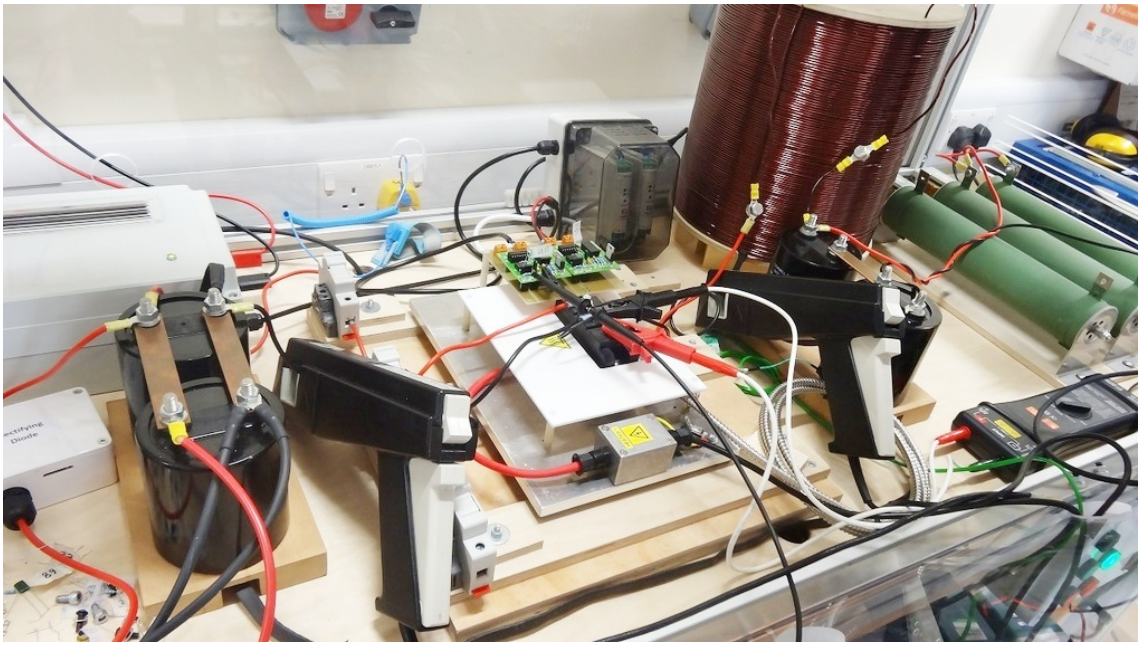


Figure 6.12: The power module connected to gate drives along with the current and voltage measurement probes, the load resistors and the passive elements of the circuit.

6.3.2 Switching Rate Dependence

Figure 6.13 shows the results of the measurements for the switching rate dependence of crosstalk where dV/dt is determined by a single gate resistance on the high side device (which is intentionally switched) and the induced voltage is measured on the low side device. The magnitude of the induced gate voltage is varied by the range of R_G on the low side device. Figure 6.13(a) shows the induced gate voltage in the Si-IGBT module while the high side device switches with a high dV/dt due to a gate resistance of 10 Ω. Figure 6.13(b) shows the corresponding shoot-through current. It can be seen that increasing the low side R_G at a constant dV/dt causes a corresponding increase in the peak and duration of the induced voltage with peaks of 12-14 V which are well above the threshold voltage of 5 V. Figure 6.13(c) shows the induced parasitic voltage on the low side SiC MOSFET while Figure 6.13(d) shows the corresponding shoot-through current.

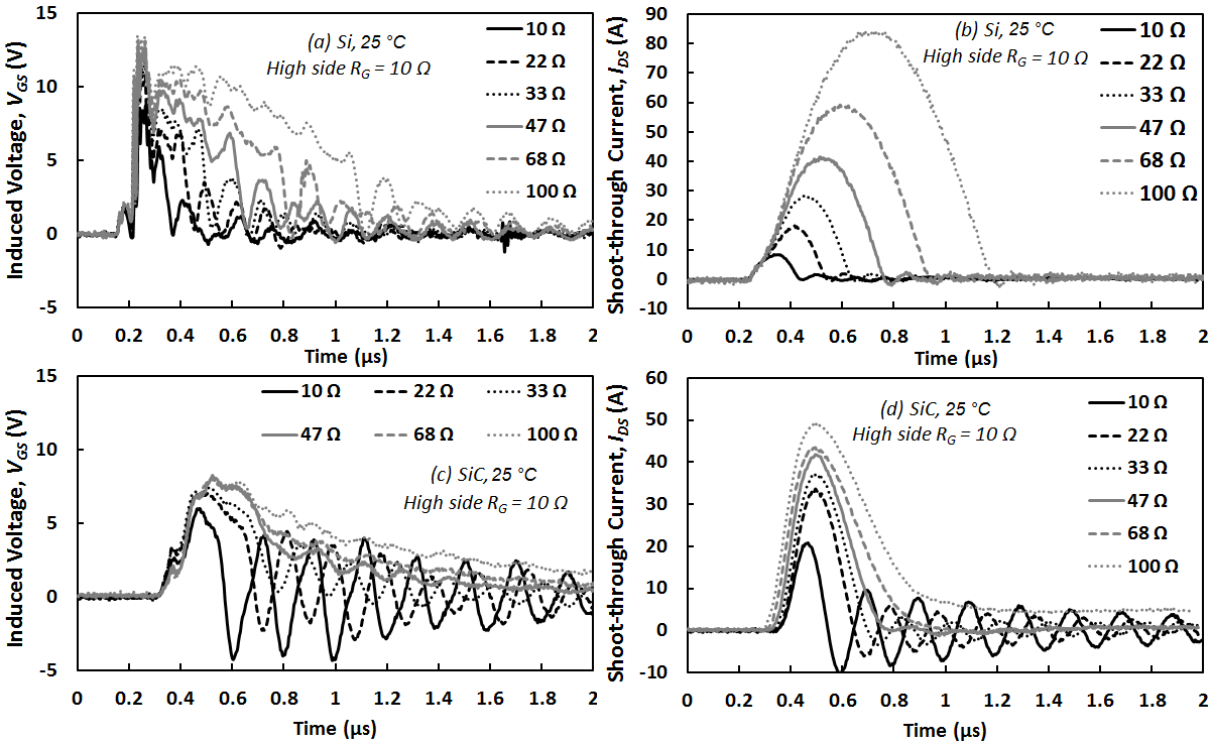


Figure 6.13: (a) The induced parasitic turn-on voltage on the Si-IGBT module at different R_G with a constant turn-on dV/dt. (b) The corresponding shoot-through current through the Si-IGBTs at different R_G. (c,d) The same figures for SiC MOSFET.

For the SiC MOSFET power module, oscillations occur in the gate characteristic due to the ringing in the low side V_{DS} which feeds back to the gate drive through the Miller capacitance. This ringing, which is due to RLC resonance, has an attenuation that is proportional to the switching dV/dt. It can be seen from Figure 6.13 that the peak shoot-through current is approximately 70% higher for the Si-IGBT power module compared to the SiC MOSFET power module. This is due to the higher Miller capacitance in the Si-IGBT which according to Equation 6.1 will cause a higher parasitic gate voltage.

Figure 6.14 shows the impact of reducing the turn-on dV/dt by increasing the high side R_G when the low side R_G is connected to a high value. As seen in Figure 6.14(a), reducing the high side R_G has resulted in a decrease in the induced gate voltage in the

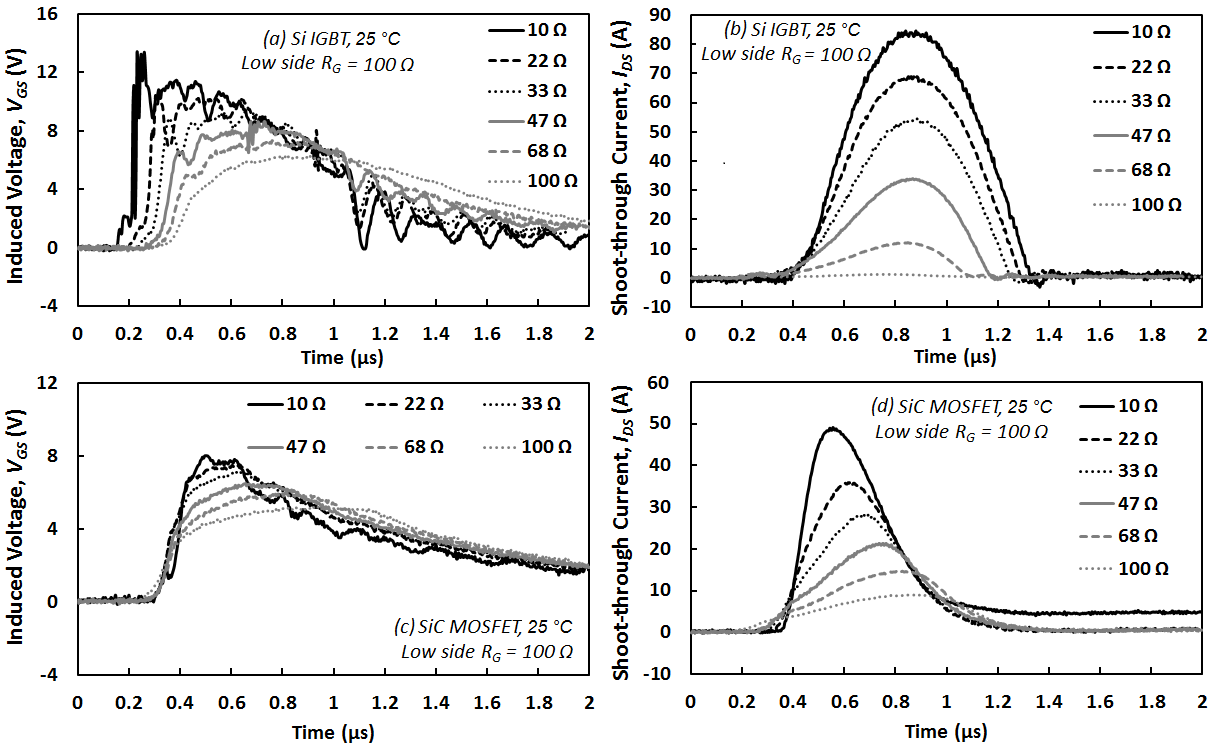


Figure 6.14: (a) The induced gate voltage on the Si-IGBT module at different turn-on dV/dt with low side R_G constantly 100 Ω, (b) The corresponding shoot-through current in the Si-IGBTs at different high side R_G. (c,d) The same figures for SiC MOSFET.

silicon IGBT module with a reduction from peak 12 V to 5 V. This has resulted in a reduced shoot-through peak from 80 A to less than 5 A. The same characteristics are also seen in Figure 6.14(c) where the peak induced gate voltage of 8 V has been reduced to 5 V. This has also resulted in a decrease of peak shoot-through from 50 A to 10 A. Due to the smaller size of the Miller capacitance in the SiC module, the dependency on the high side dV/dt is less pronounced. This will be shown in the next sections. The impact of shoot-through on the DC link voltage and the diode voltage is shown in Figure 6.15.

Figure 6.15(a) shows the voltage measured across the low side Si-IGBT/PiN diode for the different gate resistances at room temperature while Figure 6.15(b) shows the measured DC-link voltage during the short circuit. Similarly, Figure 6.15(c) shows the

measured voltage across the low side SiC MOSFET/Schottky diode while Figure 6.15(d) shows the measured corresponding DC link voltage. It can be seen that the SiC device exhibits ringing (exacerbated by higher dV/dt) which is similar to the ringing seen in the gate characteristics and shoot-through currents in Figure 6.13(c) and Figure 6.13(d).

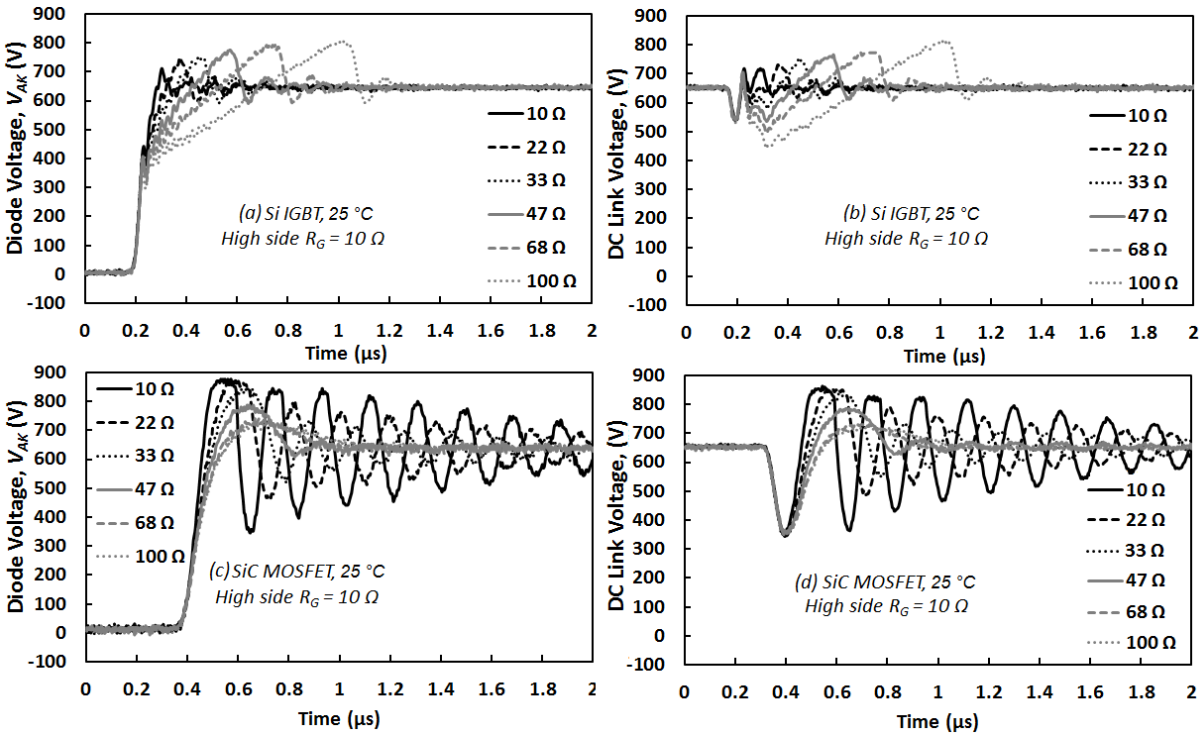


Figure 6.15: Low side diode and DC link voltage with measurements at 650 volts and 25 °C, (a,b) Si-IGBT (c,d) SiC MOSFET.

Figure 6.16(a) shows the shoot-through energy density for the Si-IGBT power module for a combination of gate resistances ranging from 10 Ω to 100 Ω while Figure 6.16(b) shows the same for the SiC MOSFET. The shoot-through energy density is calculated by integrating the measured instantaneous power over the duration of the short circuit and normalized by the measured device area. At high switching rates the shoot-through energy density is higher for the SiC power module because of the diode turn-off voltage

overshoot. The best combination to achieve the smallest shoot-through energy density is obtained when the turn-on of device is slower than its turn-off. This observation will form the basis of one of the corrective measures that can be used to mitigate shoot-through.

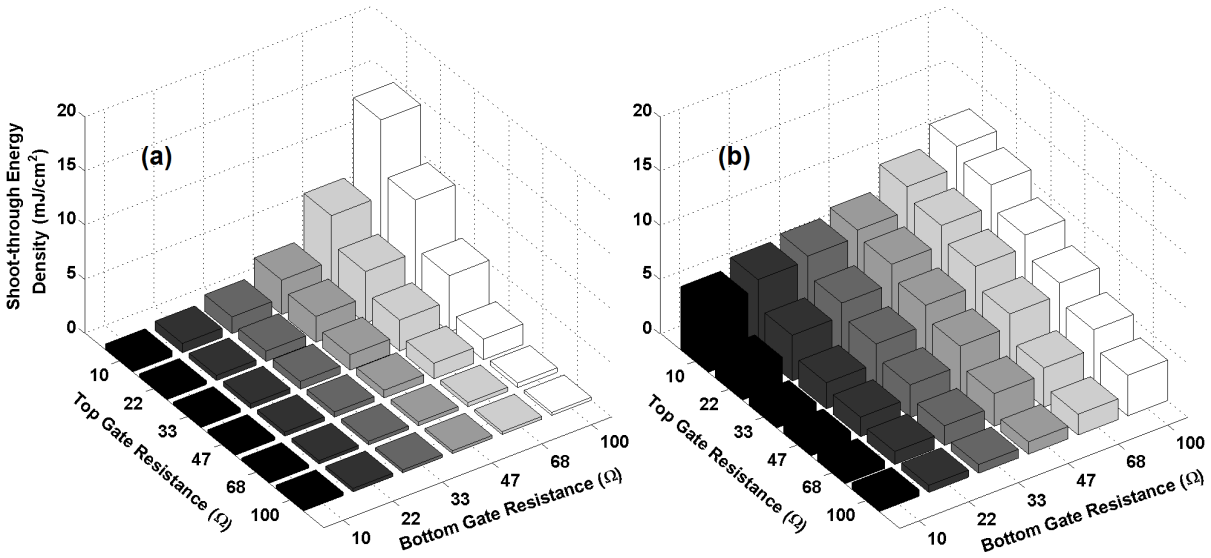


Figure 6.16: The shoot-through energy density for different combinations of gate resistances in (a) Si-IGBT power module and (b) SiC MOSFET power module.

6.3.3 Temperature Dependence

The temperature dependence of the shoot-through current and energy has also been investigated experimentally for both technologies. Figure 6.17(a) shows the parasitic induced voltage on the gate of the Si-IGBT at different temperatures and Figure 6.17(b) shows the corresponding shoot-through current at different temperatures. Similar measurements are shown for the SiC power MOSFET module in Figure 6.17(c) and Figure 6.17(d). As can be seen in Figure 6.17(a), the parasitic voltage characteristics are nearly temperature invariant whereas in Figure 6.17(b), the peak shoot-through current can be seen to increase by over 60% (80 A to 130 A) as the temperature is increased from room temperature

(25 °C) to 120 °C. This is due to the negative temperature coefficient of the threshold voltage in the silicon IGBT which means that the shoot-through currents are higher and occur over a longer duration at higher temperatures. Figure 6.17(c) shows the induced parasitic voltage in the SiC power module where it can be seen to be temperature invariant. Figure 6.17(d) shows the corresponding shoot-through currents where it is seen that the shoot-through in the SiC power module is less. For the same temperature range, the peak shoot-through current in the SiC power module increases from 40 A to 60 A. By comparing the temperature dependence of the shoot-through currents in the SiC MOSFET module with the silicon IGBT module, it can be seen that the SiC MOSFET module exhibits less temperature sensitivity. This is due to the threshold voltage in SiC MOSFETs having a smaller negative temperature coefficient compared to the silicon IGBTs. Hence, although the threshold voltage is lower in SiC MOSFETs, it is more stable over temperature. This is attributable to the wide bandgap characteristics of SiC. Figure 6.18 also shows the temperature dependency of the shoot-through in both power modules for the case that the high side device also switches slowly. This slower switching means lower induced gate voltages in Figure 6.18 compared with the Figure 6.17 which consequently translates into lower shoot-through currents. However, as seen the temperature dependency is still pronounced in both the Si-IGBT and SiC MOSFET modules.

The trend seen in Figure 6.17 where the Si-IGBT was more temperature dependent compared to the SiC MOSFET module is also seen in Figure 6.18. In the Si-IGBT module, by increase of temperature from the room ambient temperature to 120 °C, the shoot-through current has increased from 1 A to 30 A. The very low initial current in room temperature is due to the fact that the peak induced gate voltage is very close to the threshold voltage in such conditions. However, by increase of temperature, the threshold voltage drops and the peak shoot-through rapidly increases. In the SiC MOSFET module,

the initial shoot-through current in room temperature is higher (5 A) as the threshold voltage at room temperature is lower. However, similar to the case of Figure 6.17, the rate of increase in shoot-through current is lower than that of the Si-IGBT module, due to the wide bandgap characteristics of the SiC device.

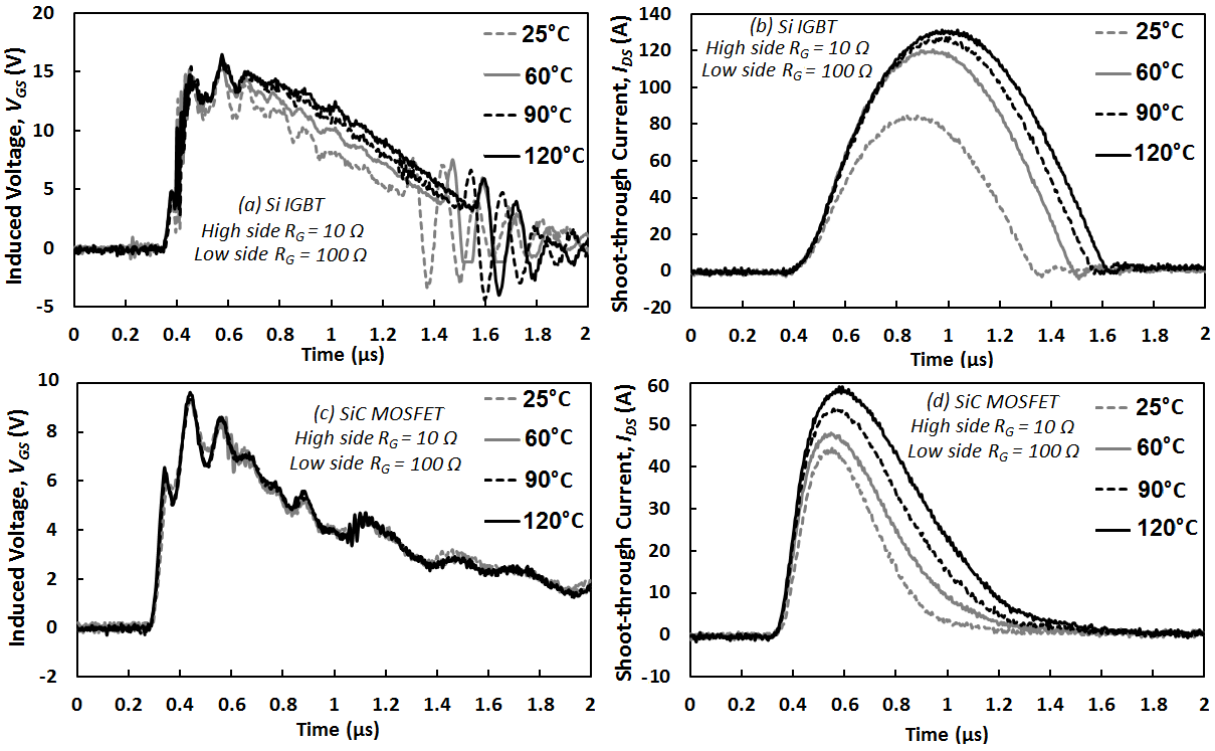


Figure 6.17: (a) Induced gate voltage on the Si-IGBT module at different temperatures with constant dV/dt. (high side $R_G = 10\ \Omega$, low side $R_G = 100\ \Omega$) (b) Corresponding shoot-through current in Si-IGBTs. (c,d) The same figures for SiC MOSFET.

Figure 6.19 shows the low side diode voltage and its consequent DC link voltage for both silicon and SiC power modules where both devices are connected to low R_G, resulting in high switching rates. It is seen that they are nearly temperature invariant at high switching rates as was expected [74]. The ringing characteristics are evident in Figure 6.19 in the output voltage of the SiC MOSFETs. This is as was explained in previous chapters regarding SiC Schottky diode turn-off where RLC resonance causes ringing. The ringing

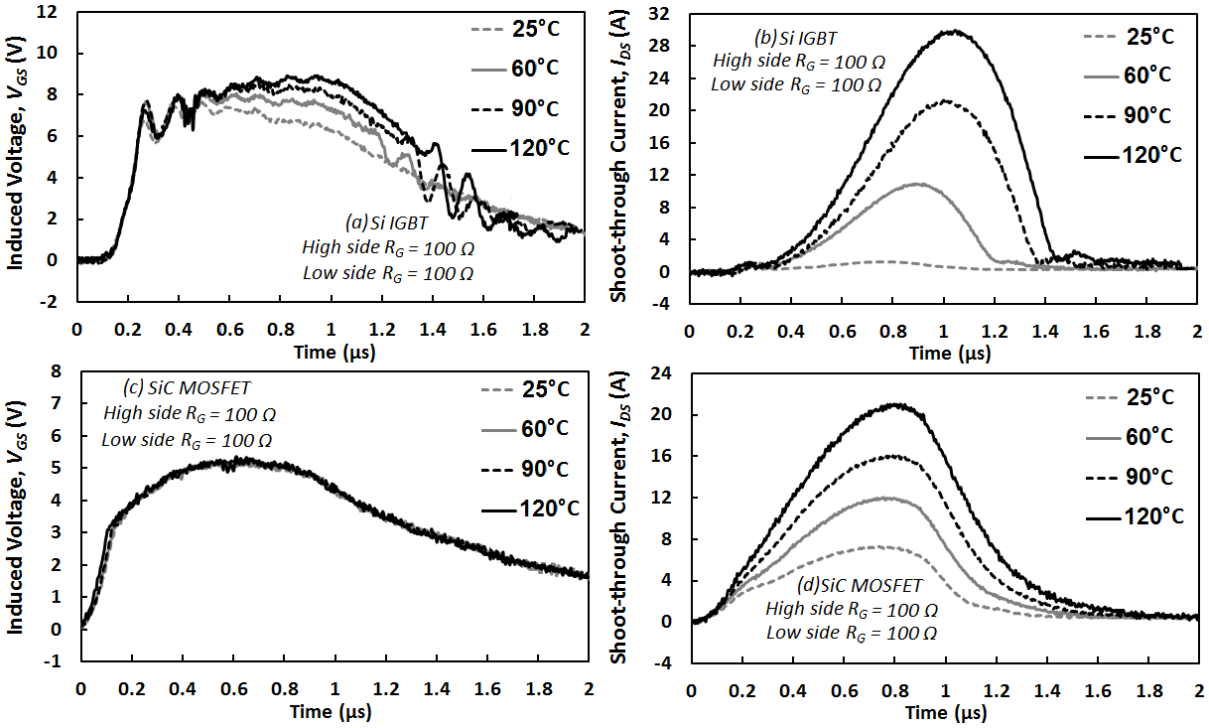


Figure 6.18: (a) The induced parasitic turn-on voltage on the Si-IGBT module at different temperatures with constant dV/dt (both high and low side $R_G = 100\ \Omega$) (b) The corresponding shoot-through current. (c,d) The same figures for SiC MOSFET.

damping will decrease with increase in the switching rate and contribute to the shoot-through energy density and temperature rise as will be shown later. The ringing causes instability in the DC link voltage which does not occur in the Si-IGBT module. However, as was seen in Figure 6.13, when the low side R_G increases the shoot-through current increases as well. Also, as seen in Figure 6.17 the shoot-through current is very temperature dependent. Hence, the impact of an increase in temperature when shoot-through current is high is more pronounced. This results in even longer shoot-through durations which translates into longer instability in DC link voltages as seen in Figure 6.20, the duration of which is longer for Si-IGBT module. The DC link voltage of the Si-IGBT module is more temperature dependent which follows the same trend of shoot-through current.

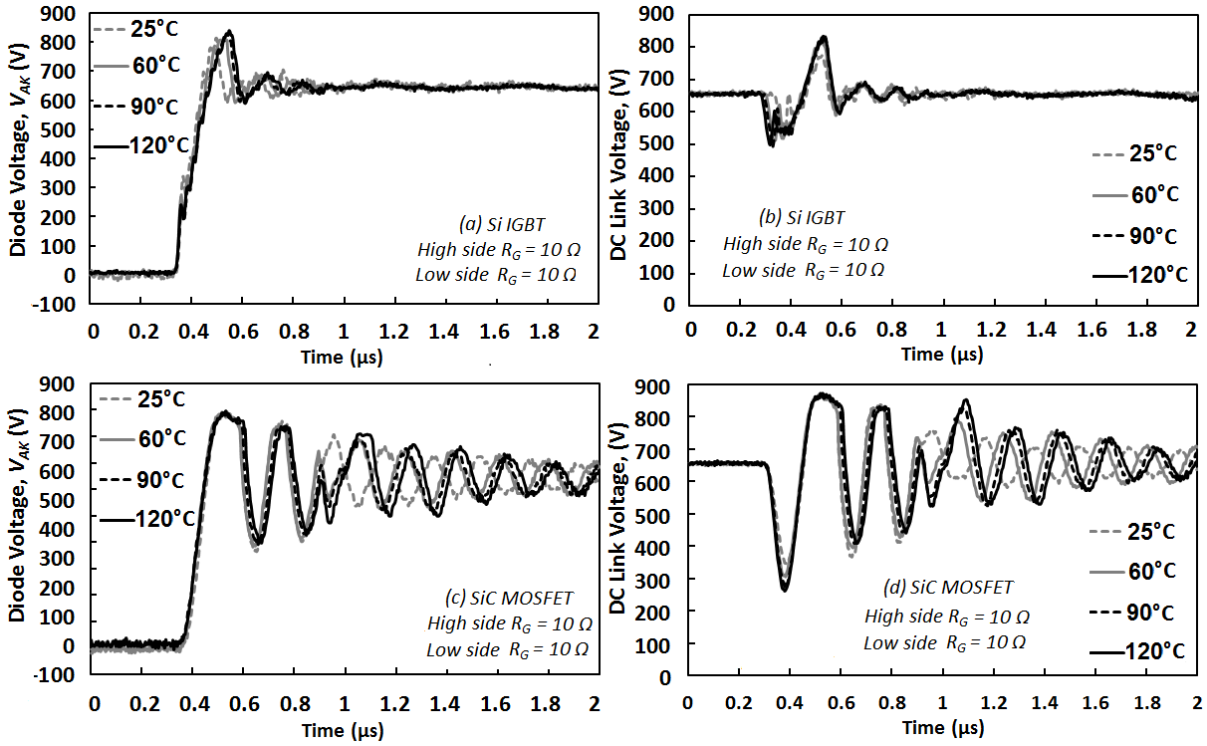


Figure 6.19: The impact of temperature on the diode and DC link voltage at high switching rates (both high/low side devices are connected to $R_G = 10\ \Omega$) (a,b) Si-IGBT (c,d) SiC MOSFET showing invariance with temperature at high switching rates.

The shoot-through switching energy density is shown in Figure 6.21 as a function of temperature for the 2 technologies with different low side R_G. The shoot-through energy density is calculated by integrating the measured shoot-through power over the short-circuit duration and then dividing the calculated energy by the active area of the dies in the power module. In these measurements, the low side gate resistance is used to control the severity of the parasitic turn-on and the shoot-through current magnitude and duration. It can be seen from Figure 6.21 that the SiC MOSFET module on average shows less shoot-through energy density since the peak currents are lower and the temperature sensitivity is lower. The lower peak currents are due to the smaller Miller capacitances and the smaller temperature sensitivity is due to the wider bandgap. At high switching rates,

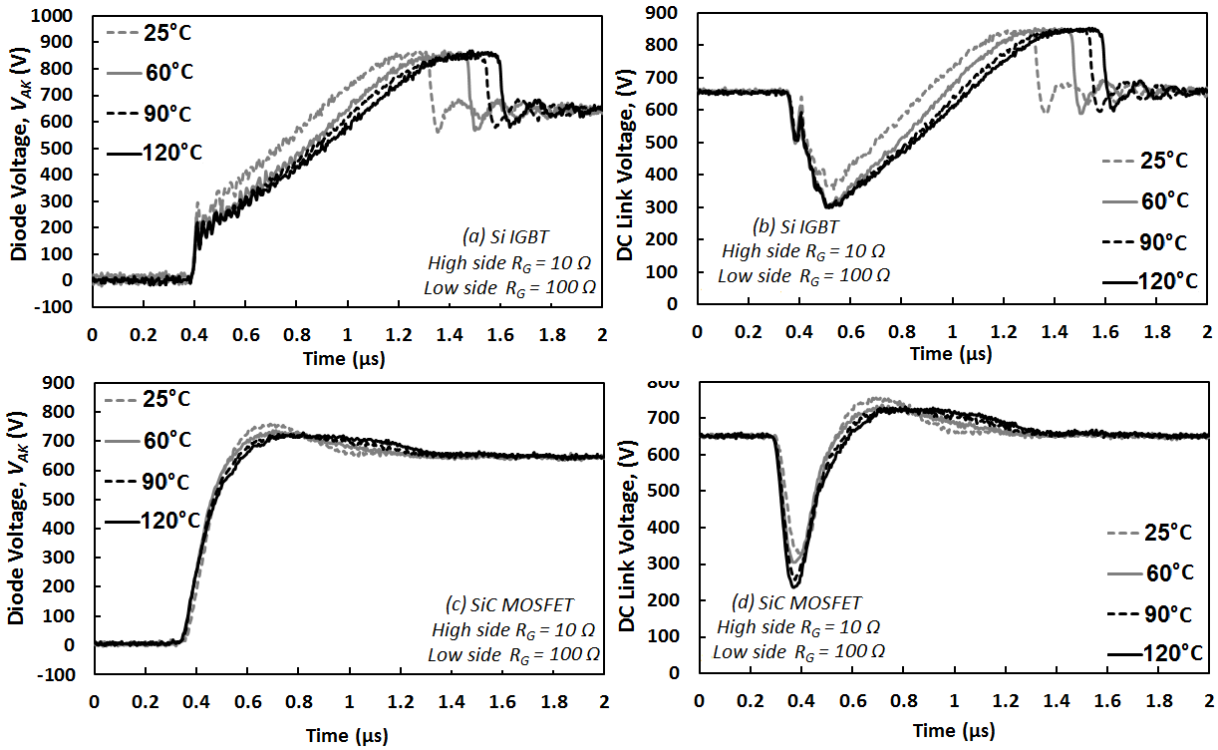


Figure 6.20: The impact of temperature on the diode and DC link voltage at high shoot-through currents (a,b) Si-IGBT module (c,d) SiC MOSFET module.

the SiC device exhibits a higher shoot-through energy density due to the contribution of the ringing in the voltage transient characteristics which increases with switching rate.

Crosstalk can be investigated by different approaches. The direct approach is to evaluate it through shoot-through current in the device. This shoot-through current can cause, for example, the circuit protection to activate. However the amplitude of the current is not a sufficient method for understanding the consequences of crosstalk, since the duration of the shoot-through current is also a critical parameter. Hence, the shoot-through charge which incorporates both the peak current amplitude and the transient short-circuit duration should be used to understand the severity of crosstalk. Also the shoot-through energy density, as a result of the dissipated power during crosstalk should be analyzed, since reliability issues and device failures are often caused by the excessive

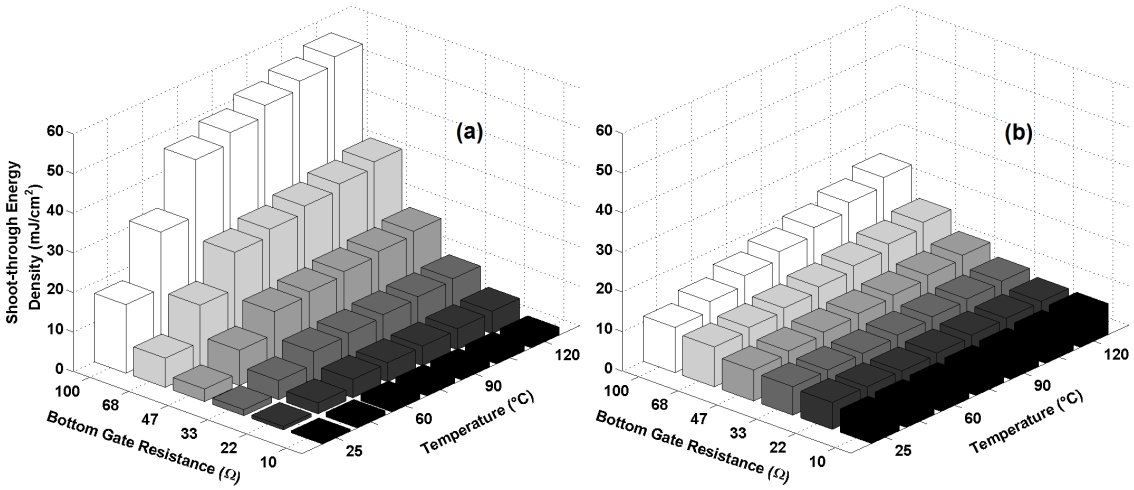


Figure 6.21: The shoot-through energy density at different temperatures and low side gate resistances in (a) the Si-IGBT (b) the SiC MOSFET power module.

heat generated within the device junction. That rate of change of shoot-through charge with temperature has been calculated so as to evaluate the temperature dependence for both technologies. Figure 6.22 shows a comparison of the shoot-through charge (integrated shoot-through current over time) temperature coefficient for both technologies where it can be seen that the SiC MOSFET module is more temperature stable.

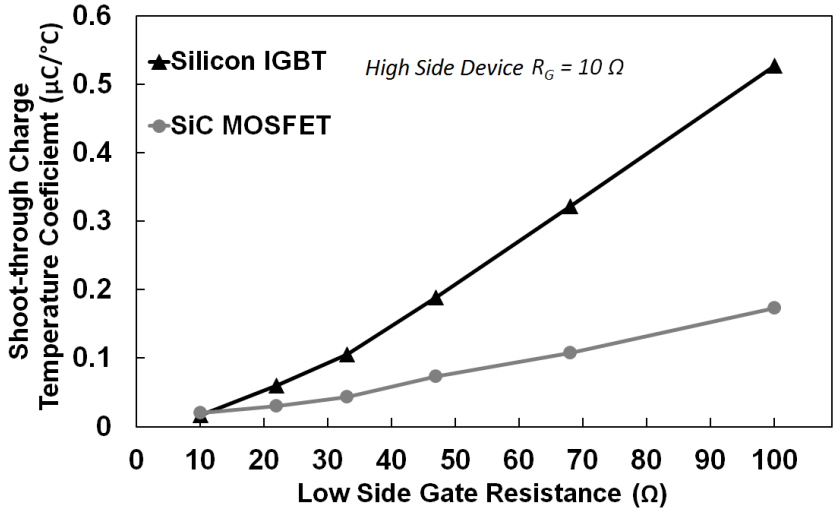


Figure 6.22: Shoot-through charge temperature coefficient (μC/°C) as a function of R_G.

Figure 6.23 shows the corresponding shoot-through energies. It can clearly be seen that the SiC module exhibits better R_G stability compared to the Si-IGBT module.

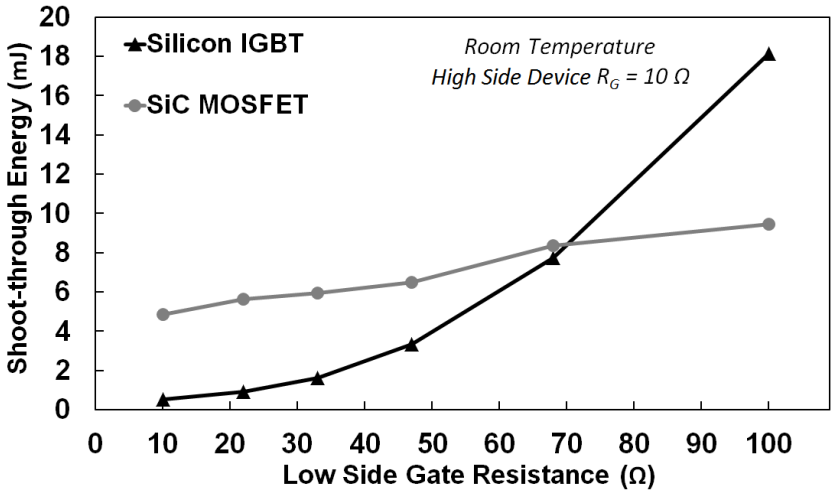


Figure 6.23: Shoot-through energy of silicon device compared with SiC counterpart.

6.4 Evaluation of Crosstalk Mitigation Techniques

To mitigate the induced parasitic voltage and its subsequent consequences, including the shoot-through current and the DC link voltage ripple, several correction techniques can be employed [129, 130]. However not all these techniques are applicable in all cases. The correction techniques to be analyzed for effectiveness includes (i) the use of a bipolar gate driver instead of a unipolar driver (negative voltage offset) (ii) using two different gate resistors for turn-on and turn-off (iii) using an external gate-source capacitor and (iv) using a DC link high frequency de-coupling capacitor capacitor. Other correction techniques include the use of the Miller clamp which is not suitable for SiC power modules [130]. Several publications proposed advanced gate drive techniques to mitigate the crosstalk. However the optimum goal here is to compare the effectiveness of the basic techniques applied to the ordinary gate drivers for both device technologies.

6.4.1 Negative Offset Gate Bias by Bipolar Gate Drives

The basic idea behind the negative gate bias is to increase the margin required for current flow from the threshold voltage V_{TH} to the sum of the negative gate bias and the threshold voltage (V_{GB}+V_{TH}). However, this requires gate driver circuits capable of providing negative bias (bipolar gate drivers) which are more complicated and expensive compared to unipolar gate drivers. The design schematic of the bipolar gate driver used in these measurements is shown in Appendix E. Furthermore, subjecting SiC power MOSFETs to negative stress across the gate oxide is a reliability concern since threshold voltage shift can cause the devices to become normally on or increase the sub-threshold leakage current. Higher levels of trap densities in the SiC/SiO_2 interface compared with the Si/SiO_2 interface makes charge trapping more of a problem in SiC MOSFETs. The higher interface trap density is due to the presence of carbon atoms in SiC which do not oxidize readily to form SiO_2 [131]. Overall more defects present in the channel interface of the SiC/SiO_2 results not only in a possible threshold voltage shift, but also a significant reduction in the mobility of carriers in the channel region of SiC devices.

The limits for maximum applied gate voltage are shown in Table 6.2. Here, the effectiveness of this correction technique is evaluated for both technologies. The negative bias voltage applied to both devices is equally set as –5 volts and the same unipolar and bipolar drives are used in both cases to provide a fair comparison. This voltage is chosen as it is the maximum negative gate voltage that SiC device can withstand during continued operation based on the device datasheet. The Si-IGBT, on the other hand, is capable of withstanding negative voltages with magnitudes as high as $|-20\,V|$.

Figure 6.24(a) shows the induced parasitic voltage on the low side Si-IGBT for both unipolar and bipolar gate drives whereas Figure 6.24(b) shows the shoot-through current.

Similar plots are shown for the SiC module in Figure 6.13(c) and Figure 6.13(d). It can be seen that the induced voltage is suppressed and the peak shoot-through current is significantly reduced (from 80 A to 5 A) for the Si-IGBT module whereas for the SiC module, the peak shoot-through current is reduced from 45 A to 20 A. Hence, while the bipolar gate drive assists the Si-IGBT module, it does not completely solve the issue for the SiC module. This is thought to be due to the higher dV/dt associated with switching of MOSFET coupled with the lower threshold voltage of the SiC module. Again, the ringing in the induced gate voltage characteristics of the SiC MOSFET is due to ringing in the drain voltage being coupled with the gate voltage through the Miller capacitance.

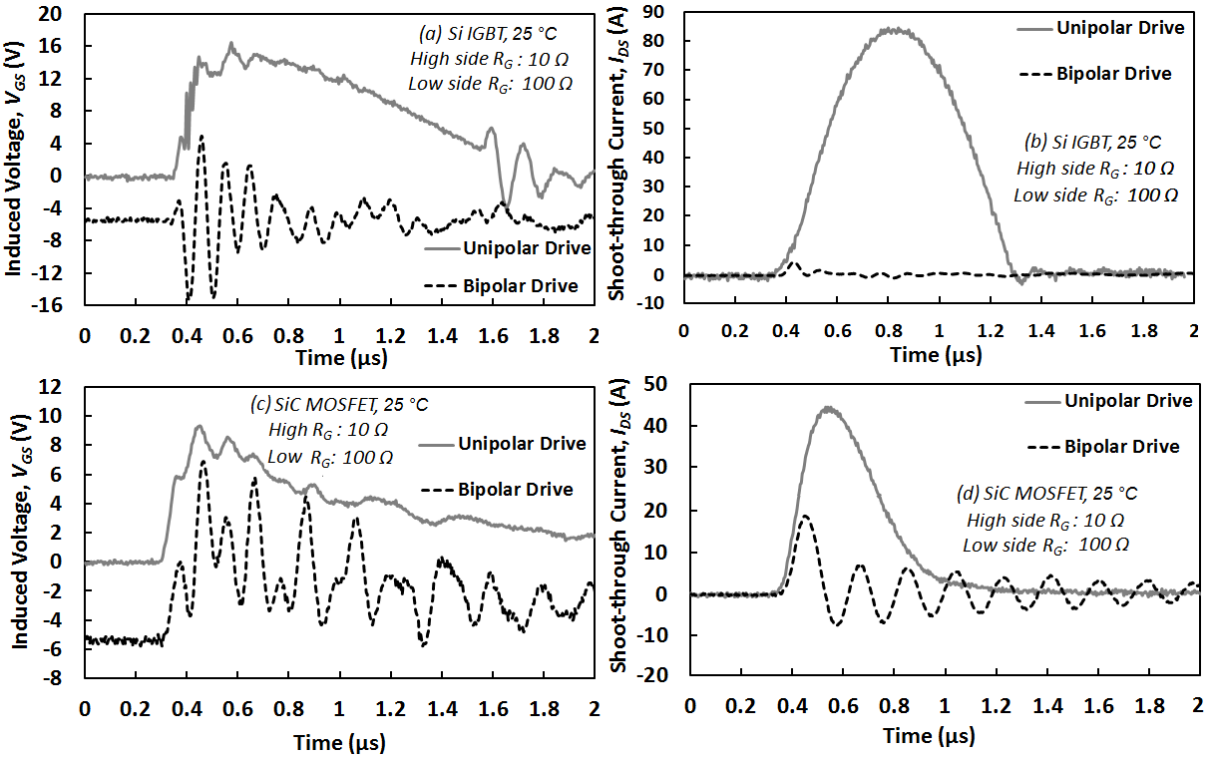


Figure 6.24: Measurements in 25 °C with high side $R_G = 10\ \Omega$ and low side $R_G = 100\ \Omega$
(a) Impact of the bipolar driver on the biasing the induced voltage on Si-IGBT
(b) Impact of biased induced voltage on the shoot-through current on Si-IGBT
(c,d) The same for SiC MOSFET.

6.4.2 Use of Two Resistive Paths for Turn-on and Turn-off

The basic concept behind this technique is using two different resistive paths for turn-on (R_{GON}) and turn-off (R_{GOFF}) as shown in Figure 6.9. The result of applying this on the gate voltage is shown in Figure 6.25.

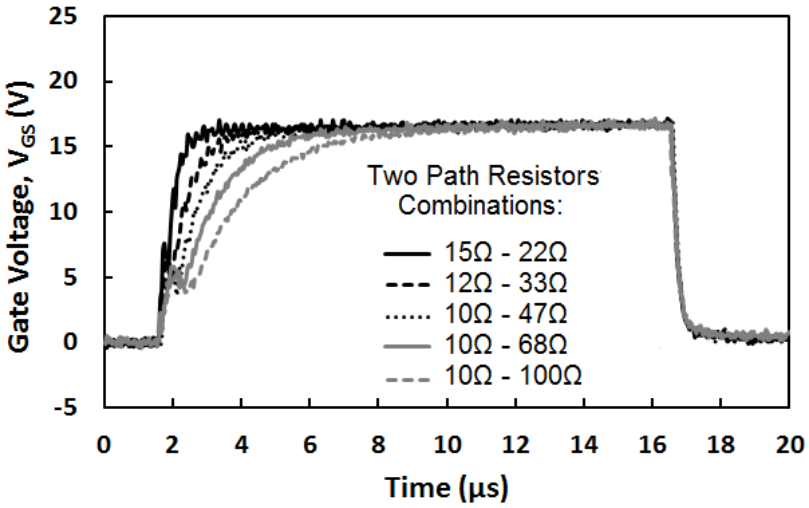


Figure 6.25: The gate signal for two resistive paths technique. As seen the turn-on is done by different rates, while the turn-off is consistently fast.

As can be seen, the turn-on and turn-off rates are controlled by the different gate resistances. This is because the direction of gate current flow during turn-on and turn-off are different. This technique requires a modification in the design of the gate driver and is a less costly option compared to the bipolar gate drivers. This is shown in Appendix E. A lower parasitic voltage is obtained by using a diode to ensure that the capacitive Miller current flows through the lower R_{GOFF}. Using this technique, it is seen that if necessary, the turn-on procedure can be slowed down by using a high gate resistance without inducing a higher gate voltage on the low side device. This is due to the fact that the turn-on dV/dt is inversely proportional to the turn-on R_G.

Looking at Figure 6.26(a) and (b) for Si-IGBT and Figure 6.26(c) and (d) for SiC MOSFET module, it is seen that this technique has significantly lowered the shoot-through current. As seen in Figure 6.26(b), the shoot-through current has been on the verge of initiation since the induced gate voltage levels out with the threshold voltage. However, using the two resistive paths has decreased the induced gate voltage and consequently its shoot-through current is once again suppressed. This is even of higher importance for high temperatures. Similar to observation in Figure 6.17, it is also seen in Figure 6.27 (for up to 120 °C) that the temperature increase will impact the threshold voltage, and not the induced gate voltage. In this case, despite the significantly higher shoot-through current compared to Figure 6.26, it is still been successfully mitigated by using two resistive paths. Therefore, due to its simplicity and effectiveness, this technique is very practical.

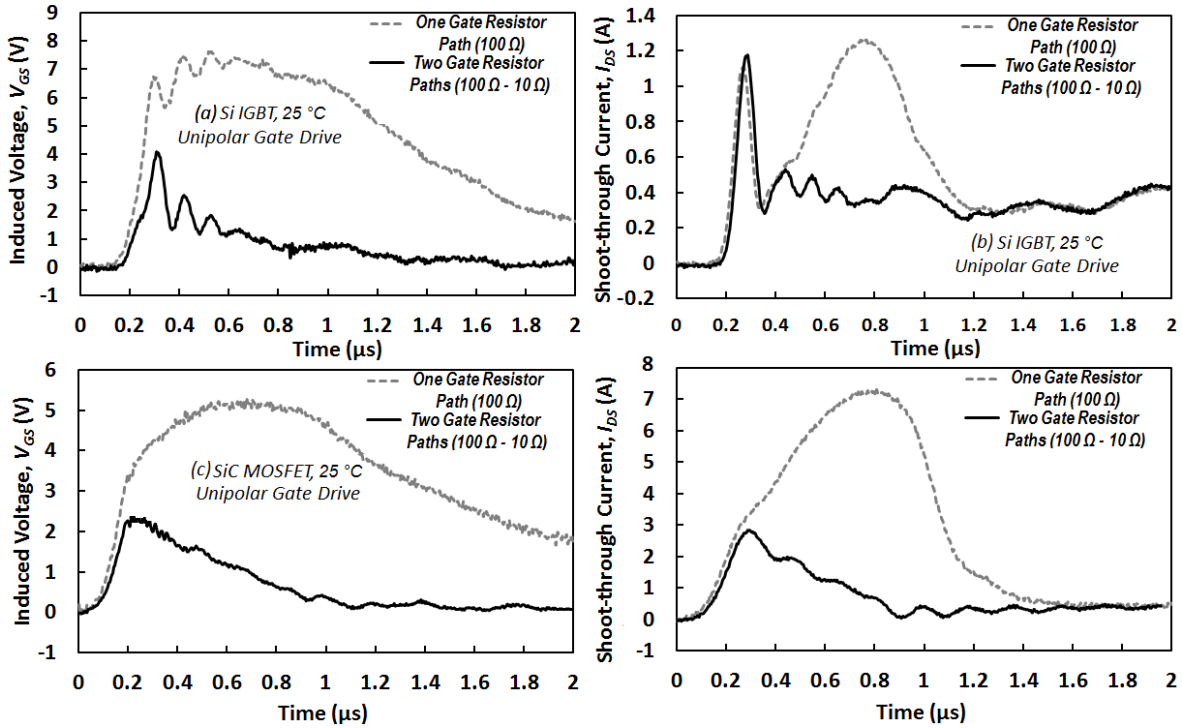


Figure 6.26: Impact of the two resistive paths technique on (a) the induced voltage and (b) the shoot-through current of Si-IGBT (c,d) the same for SiC MOSFET, at 25 °C.

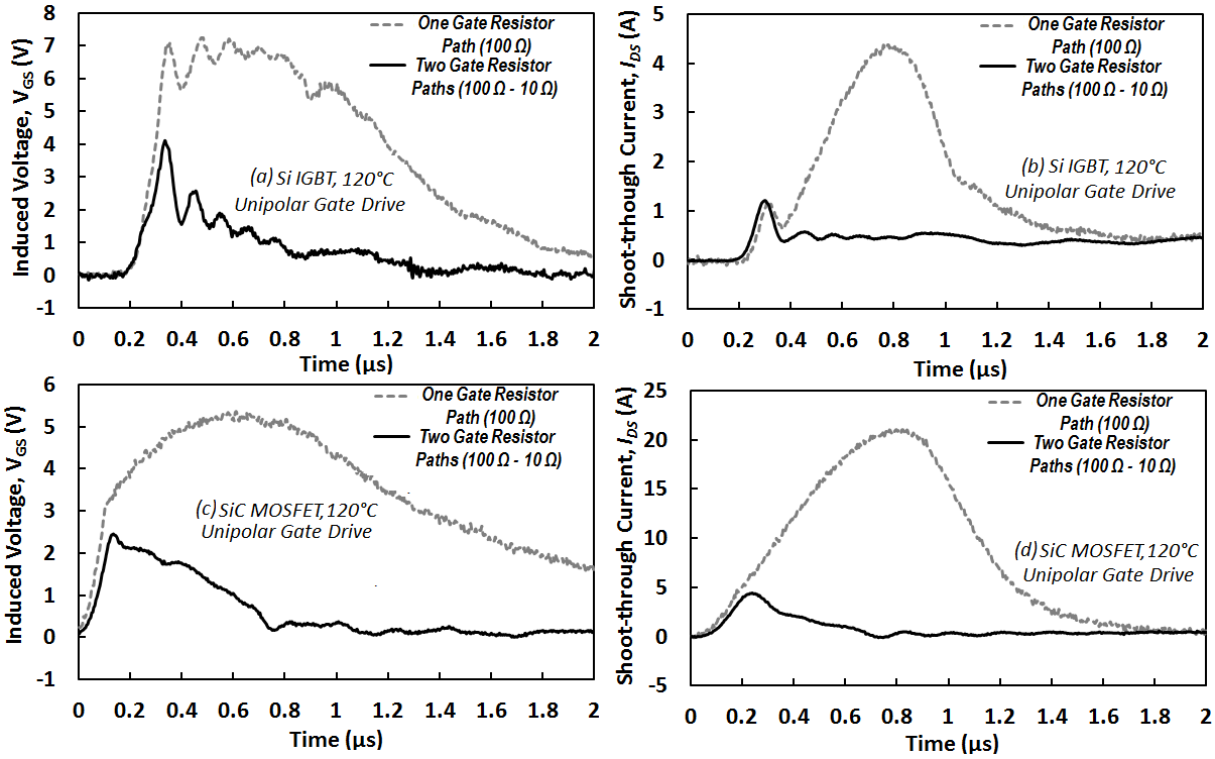


Figure 6.27: Impact of the two resistive paths technique on (a) the induced voltage and (b) the shoot-through current of Si-IGBT (c,d) the same for SiC MOSFET, at 120 °C.

6.4.3 External C_{GS}

An external gate-source capacitance can be used to reduce the induced voltage since it will consume part of the current through the Miller capacitance thereby resulting in lower currents flowing through the gate resistance, ensuring a lower induced voltage. This method also causes a lower dV/dt on high side device turn-on since the external capacitance slows down the switching rate by increasing the RC time constant. This is particularly important for higher values of external C_{GS}. As a result, this may not be preferable in SiC MOSFETs where the switching rate is normally designed to high values.

Looking at Figure 6.28(a), (b) and (c) for the Si-IGBT and (d), (e) and (f) for the SiC MOSFET, it is seen that selection of a low value for external C_{GS} (10 nF) to keep the high

switching rates has reduced the induced parasitic voltage and shoot-through current by a small degree and the impact is relatively low compared with other correction techniques examined. Increasing the external C_{GS} beyond such limits for a better crosstalk mitigation causes lower dV/dt and higher switching energies, hence, depending on the application, this may not be the preferred mitigation technique.

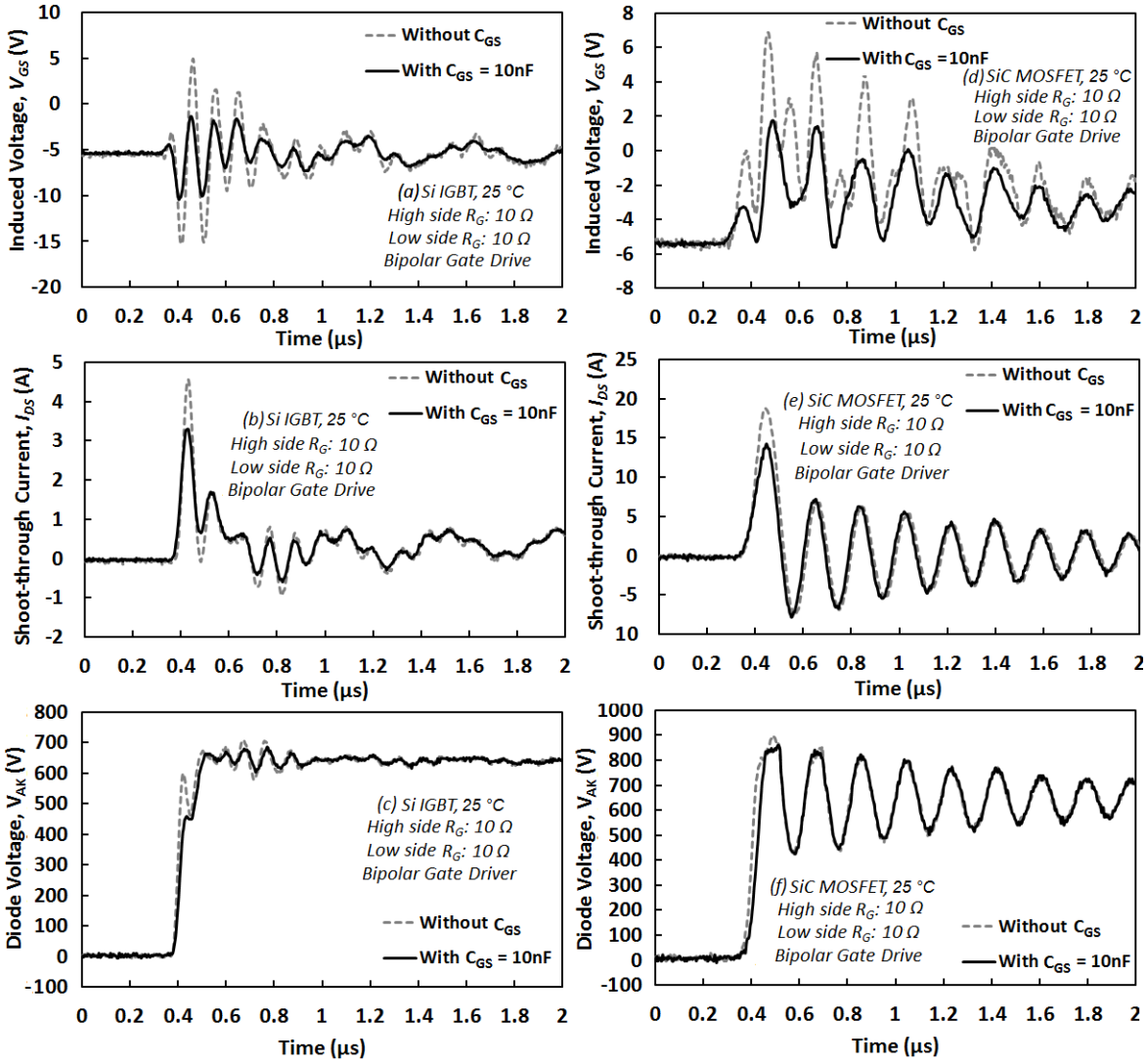


Figure 6.28: Measurements in 25 °C with a bipolar driver for impact of external C_{GS} on (a) the induced gate voltage of Si-IGBT, (b) the shoot-through current of Si-IGBT (c) the switching dV/dt of Si-IGBT. (d,e,f) the same figures for SiC MOSFET.

6.4.4 High Frequency De-coupling Capacitor

High shoot-through currents induce significant voltage dips on the DC link which destabilizes the voltage on the DC link capacitors. Stabilizing the DC link voltage using a high frequency de-coupling capacitor on the half bridge module can reduce the high frequency ringing in the shoot-through current and also results in less oscillation in the induced voltage. This in turn will reduce the shoot-through switching energy as well. The de-coupling capacitor selected for these measurements, shown in Figure 6.29 installed on the DC link connections of SiC power MOSFET module, is a polypropylene film capacitor (VISHAY MKP386M410200JT5), with a capacitance value of 100 nF and voltage rating of 2 kV. The voltage rating is chosen to be higher than device ratings to enable the capacitor withstand possible overshoot voltages on the DC link, especially in the case of the SiC device. The value of the de-coupling capacitor is calculated according to [132].

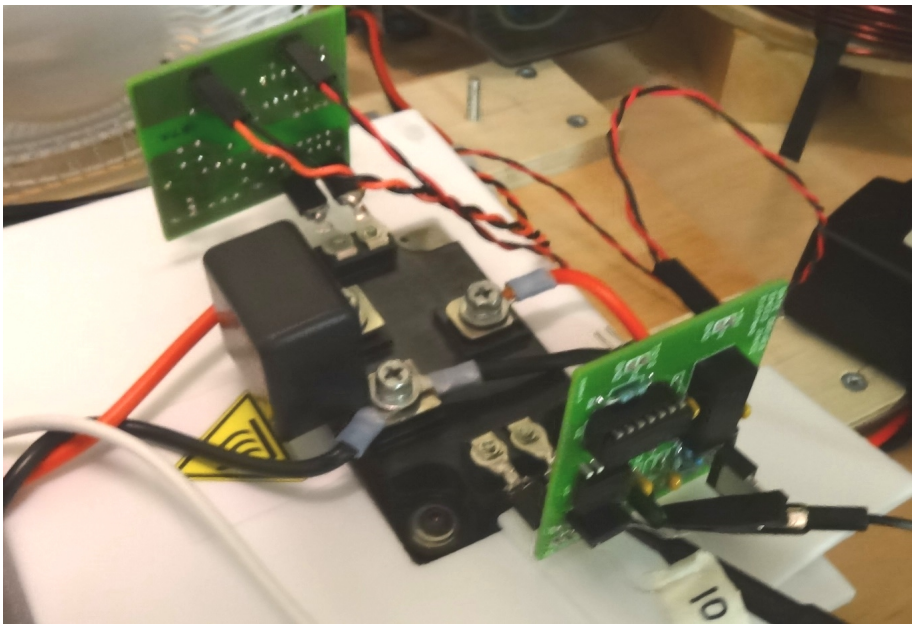


Figure 6.29: Connection of the 100 nF high frequency de-coupling capacitor on the DC link contacts of the SiC power module.

As seen in Figure 6.30, the de-coupling capacitor has stabilized the DC link and consequently, the overshoot in the voltage of the silicon module's diode. The de-coupling capacitor is particularly effective for the SiC power module since as seen in Figure 6.17(c) and (d), the oscillation on the DC link voltage of the SiC module is significant. Figure 6.30(c) and (d) shows that the de-coupling capacitor filters out the oscillations and stabilizes the DC link as well as the low side SiC MOSFET/SBD voltage. This also stabilizes the induced parasitic voltage as well as the DC link current as in Figure 6.31. In this figure, it is seen that the induced gate voltage is reduced, and its noise is also damped. Hence, the current overshoot is damped, and the frequency of the oscillations is reduced. The reduced peaks in the voltage/current important in reducing the corresponding energy and hence will reduce the crosstalk losses. The impact of this is seen in the next sections.

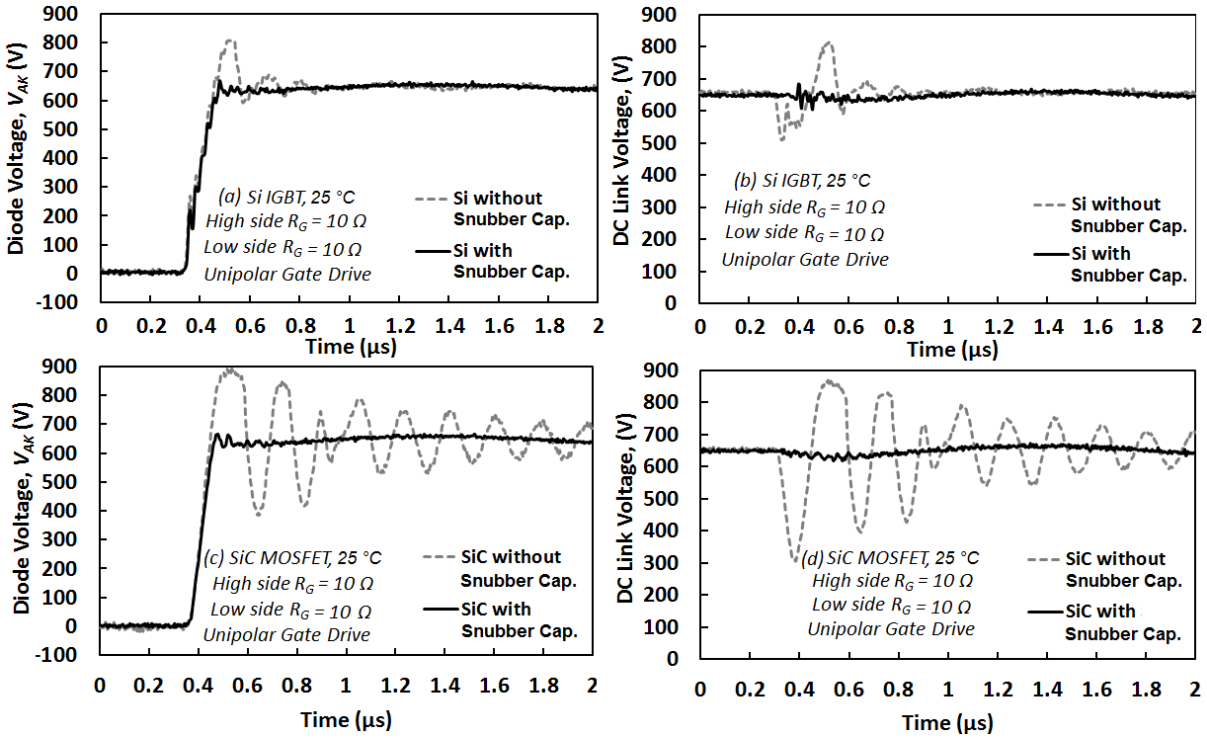


Figure 6.30: Impact of the decoupling capacitor on DC link voltage oscillations.

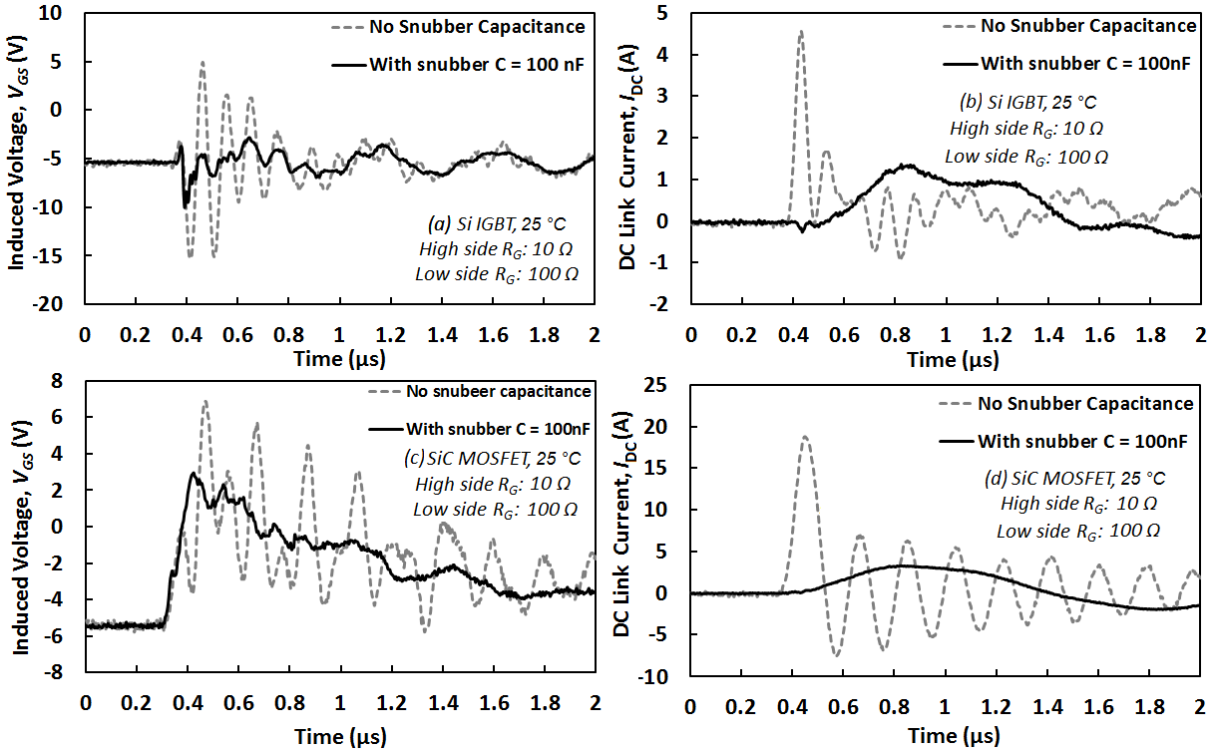


Figure 6.31: Measurements in 25 °C with a bipolar driver (a) Impact of the de-coupling capacitor on the induced voltage fluctuations on Si-IGBT (b) Impact of the de-coupling capacitor on shoot-through current of Si-IGBT (c,d) The same figures for SiC MOSFET.

6.4.5 Analysis of Effectiveness of Mitigation Techniques

To provide a comprehensive and comparative analysis on the effectiveness of the applied correction techniques, Figures 6.32 to 6.35 have been produced. Figure 6.32 shows the effectiveness of using (a) unipolar gate driver compared with (b) bipolar driver for two low side gate resistances (10 Ω and 100 Ω) while the high side switch is switched at a high rate with R_G of 10 Ω. It is seen here that the Si-IGBT module has a higher shoot-through charge compared with the SiC MOSFET module when the low side R_G is set to 100 Ω. However, the charge is lower when the low side device is connected to R_G of 10 Ω. It can also be seen that the shoot-through charge of the SiC MOSFET module is less dependent

on R_G as is expected due to its lower Miller capacitance. By applying a bipolar gate driver as seen in Figure 6.32(b), the shoot-through charge is reduced in both devices; however, the effectiveness of the bipolar gate drive is less in the SiC MOSFET module as a result of its lower threshold voltage and higher dV/dt. As can be seen from Figure 6.32(b), the shoot-through charge for both R_G cases of Si-IGBT is smaller compared to the more significant values present with the SiC MOSFET module.

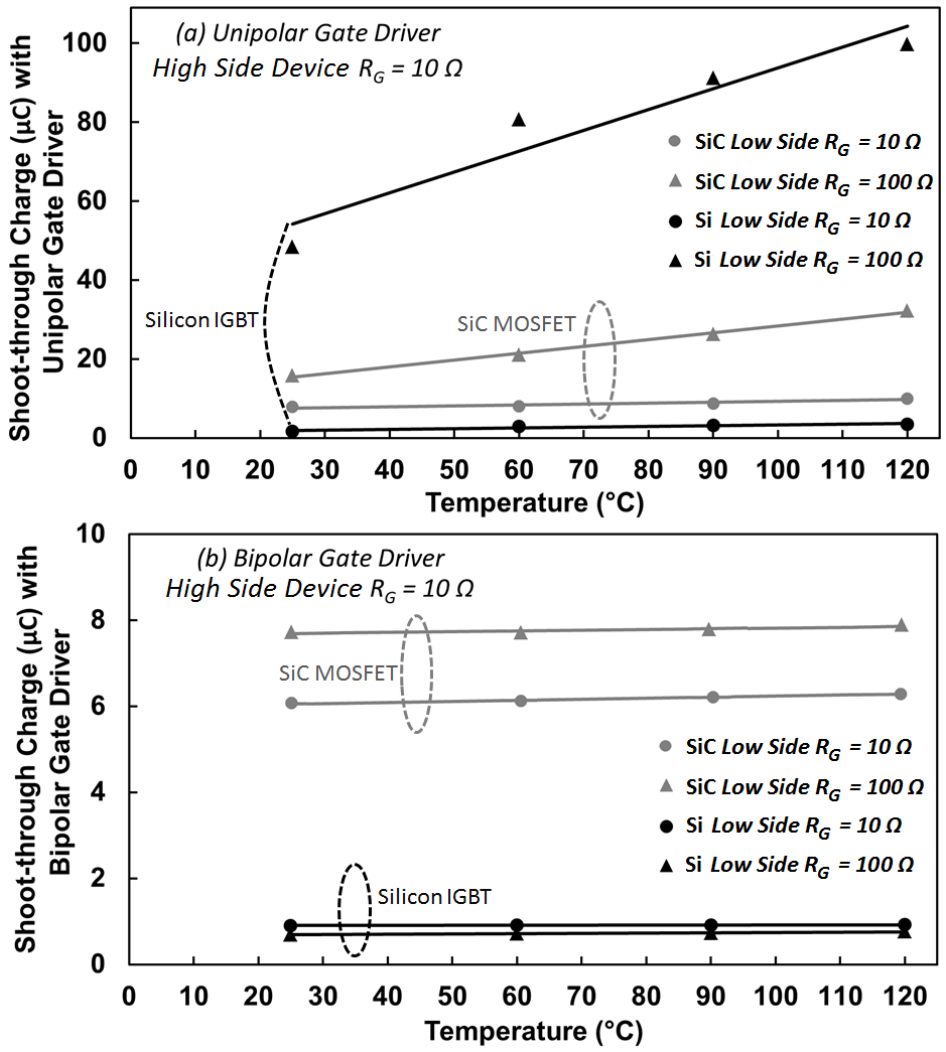


Figure 6.32: Shoot-through charge of different R_G on low side device, with (a) Unipolar and (b) Bipolar gate drivers in silicon and SiC devices.

Figure 6.33 shows the percentage reduction of shoot-through charge from the use of the bipolar gate drive for both technologies, i.e. a measure of the effectiveness of the bipolar gate drive when both devices are connected to R_G of 10 Ω. It can be seen from this figure that reduction of charge in the Si-IGBT module is higher than that of the SiC MOSFET module. This can be seen by comparing Figure 6.24(b) and 6.24(d). Hence, it has been demonstrated that this crosstalk mitigation technique is more effective in Si-IGBT modules compared with SiC MOSFET modules.

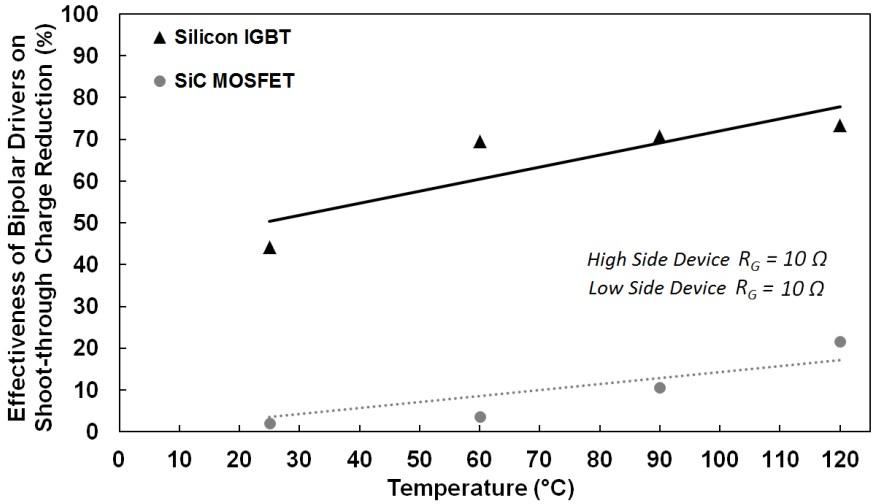


Figure 6.33: Percentage reduction of shoot-through charge in both silicon and SiC devices with $R_G = 10$ Ω showing that using a bipolar driver has a better impact on silicon IGBT device than the SiC device.

Figure 6.34 and Figure 6.35 show the results of all correction techniques applied to each device technology at 25 °C and 120 °C using the shoot-through switching energy density as the indicator. As was explained in the previous sections, to provide a fair comparison the shoot-through is evaluated by the energy density (mJ/cm^2) instead of energy (mJ). As can be seen from Figure 6.32, although the Si-IGBT module initially exhibits a higher shoot-through charge, using a bipolar gate drive is more effective in reducing this unwanted

charge and consequent dissipated energy. By comparing these figures, it can be seen that the mitigation techniques are less effective at higher temperatures which is expected since the magnitude and duration of the short circuit current increases with temperature. As it was seen previously, the use of the high frequency de-coupling capacitor mainly in the SiC MOSFET module is required for preventing ringing/oscillations in the turn-on of the low side device. As these figures show, the use of two resistive paths in the Si-IGBT module result in a significant reduction of the shoot-through energy density and is as effective as the use of a bipolar gate drive. This is beneficial from the perspective of minimizing the cost and complexity of the gate drive circuit for Si-IGBT modules. However, for the SiC MOSFET module, both techniques together with the use of a de-coupling capacitor across the DC link are required to reduce the severity of crosstalk since one technique by itself is not capable of reducing the losses appreciably. Hence, the issue of crosstalk is more persistent in fast switching SiC power modules and more research is required into effective corrective measures that do not sacrifice the switching speed of the device.

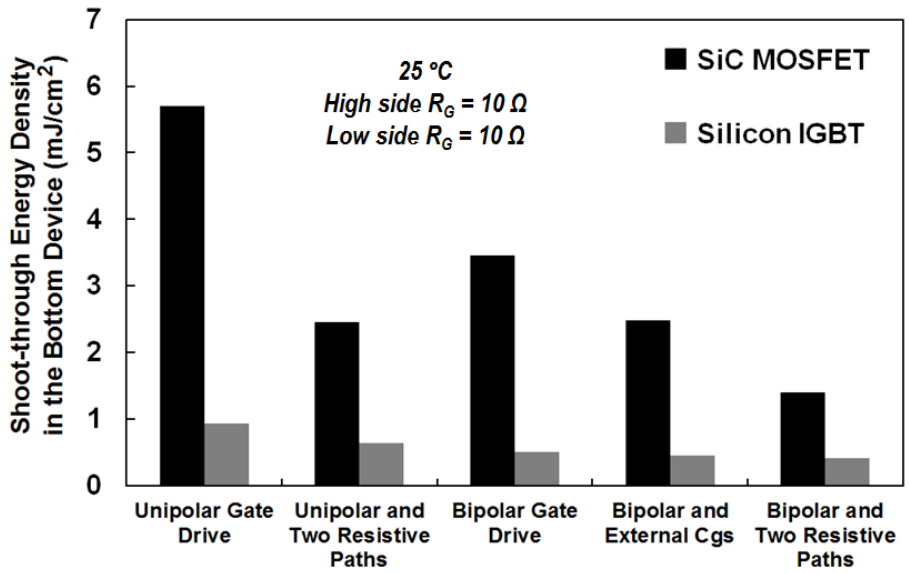


Figure 6.34: Shoot-through energy in low device with high/low $R_G = 10\ \Omega$ (25°C).

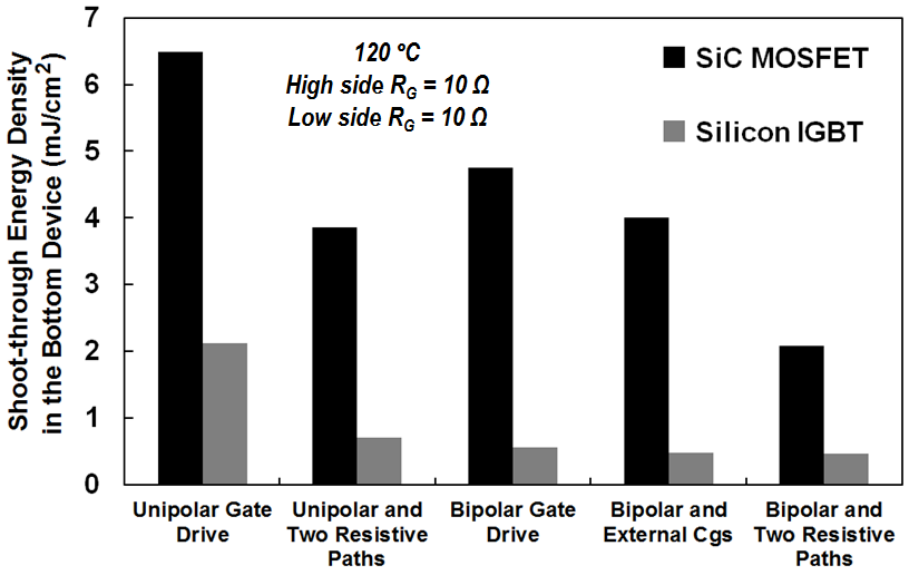


Figure 6.35: Shoot-through energy in low device with high/low $R_G = 10\ \Omega$ (120°C).

6.5 Impact of Crosstalk on Performance of Power Modules in Converters

The shoot-through energy as was shown in Figure 6.16 can result in serious consequences on the performance of power modules. This shoot-through energy can potentially lead the device to thermal runaway (as it has a positive temperature coefficient) and can cause reliability issues within the packaging. For example, for the case of the measurements presented in the past sections, the voltage has been set to 650 V and the load resistance is 1 kΩ. This results in a device current equivalent to 0.65 A which is very low for a module rated at 100 A. Hence, the switching energy on its own can not result in a significant temperature rise. However as will be seen in the next sections, the temperature rise as a result of the shoot-through energy can be very high if the module is not cooled. To evaluate the significance of the shoot-through energy on the performance of the silicon and SiC

power modules, experiments are performed on a step-down buck converter. The switching frequency is set to 8 kHz, the duty cycle is 50% (with deadtime) and the input voltage is 650 V, similar to the previous sections. The load is 500 ohms, the filter inductor is 15 mH and the filter capacitor is 80 μF. The impact of the crosstalk mitigation techniques are also evaluated through temperature rise. A thermal camera is used to precisely measure the module temperature through crosstalk occurrence as it heats up in around 8 minutes.

In this regard, Figure 6.36 shows the thermal image of the power module exhibiting the temperature rise as a result of the two different gate resistances connected to the non-switching low side device in the SiC module with R_G of 10 Ω and 100 Ω. For the measurements in Figure 6.36, the high side device is continuously switched with R_G of 10 Ω in the full buck converter topology. It is seen that in a few minutes, the temperature of device with a low side R_G of 100 Ω is raised to 150 °C while the temperature on the other device is still at room temperature.

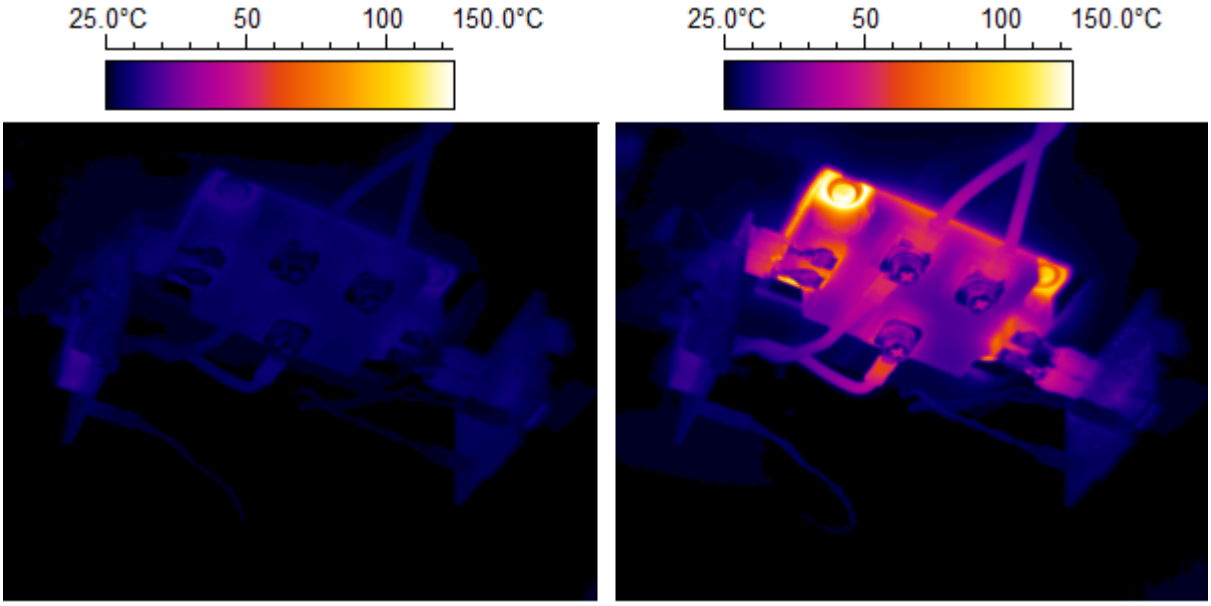


Figure 6.36: Thermal camera image of the SiC MOSFET module switching at 8 kHz with low R_G of (left) 10 Ω and (right) 100 Ω with high side device switch with 10 Ω.

Having a low input current (less than 1 A) and high switching frequency (8 kHz) which increases the occurrence of crosstalk and considering the fact that the conduction and switching losses of both situations are identical and low, the entire temperature rise can be accounted for as a result of the continued occurrence of crosstalk.

To reduce the crosstalk, one method could be to reduce the dV/dt on the low side device by means of increasing the R_G on the high side device to slow down the device during turn-on. Figure 6.37 shows the impact of such approach which causes lower shoot-through currents, resulting in lower temperature rises. It is seen that slowing down the high side device commutation rate reduced the dV/dt on low side device thereby causing smaller shoot-through currents resulting in lower shoot-through energy and a smaller temperature rise. This has the disadvantage of slowing down the device and causing higher switching losses. Since high switching rates are preferred in the devices with SiC technology, this is not a preferred correction method.

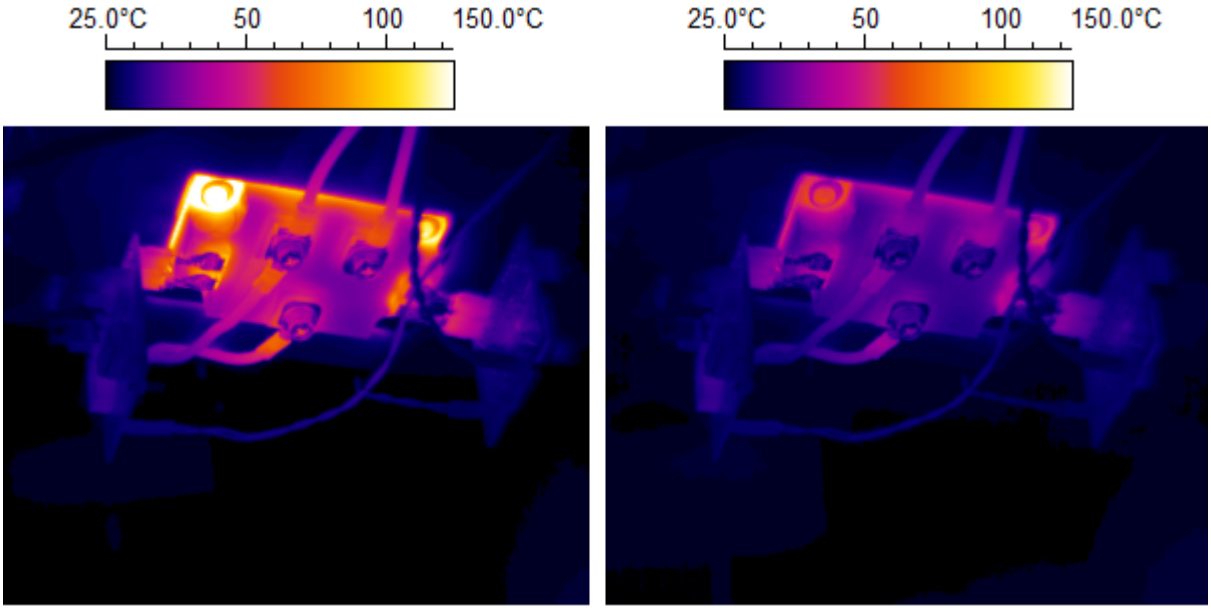


Figure 6.37: Thermal camera image of the SiC MOSFET module switching at 8 kHz with high side R_G of (left) 10 Ω and (right) 100 Ω - low side device is connected to 100 Ω.

As was seen in Figure 6.15, there are considerable oscillations associated with application of SiC power devices. These oscillations, if not dealt with, will cause even higher losses due to the continued occurrence of voltage and current overshoots. To counter this, a high frequency de-coupling capacitor must be connected on the DC link connection of the power module, ensuring that the oscillations are effectively removed. This de-coupling capacitor will reduce the elevated shoot-through energy and will slightly reduce the temperature rise. It should be noted that as was explained earlier, the de-coupling capacitor does not remove the crosstalk but only reduces its consequences. In this case, the de-coupling capacitor is sized as 100 nF and its impact is seen in Figure 6.38.

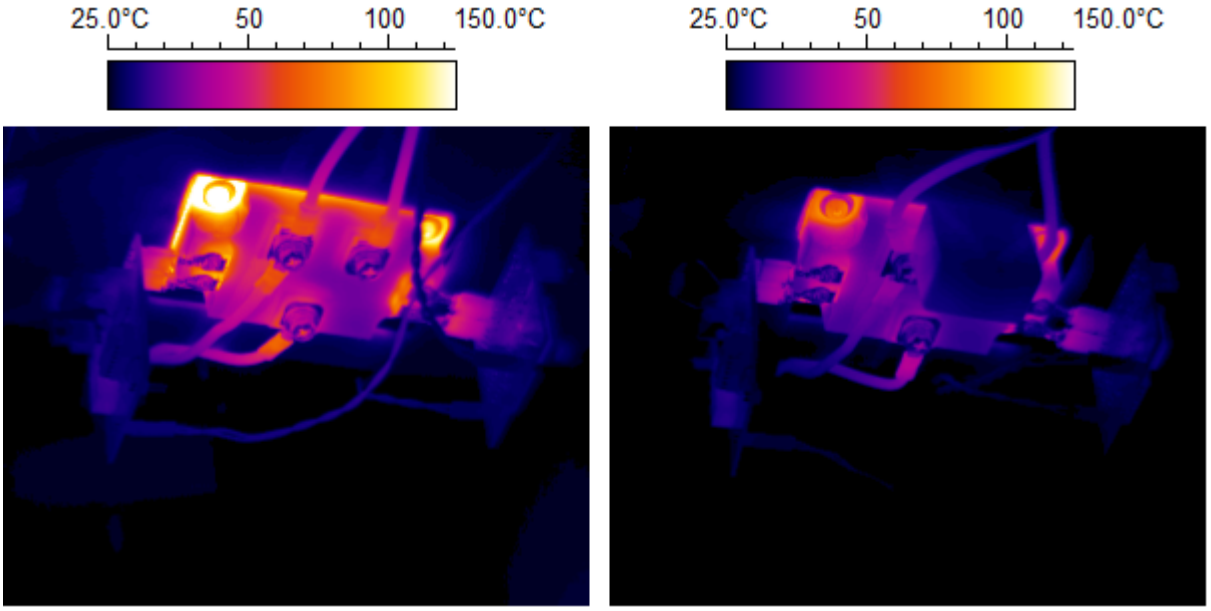


Figure 6.38: Thermal camera image of the SiC MOSFET module switching at 8 kHz with high side R_G of 10 Ω and low side R_G of 100 Ω with de-coupling capacitor only connected on right module.

As was expected, the two resistive paths solution is also needed to damp the shoot-through current, especially in the case of the SiC MOSFET module. To provide a fair comparison, the thermal images of two cases with gate resistances with a value of 100 Ω

are presented in Figure 6.39. The left figure shows the thermal image of the module with a single resistive path while the right figure shows a thermal image of the module switching with two resistive paths. As can be seen, using the two resistive paths solution has significantly reduced the temperature rise of the module. Hence, if required, it is possible to reduce the turn-on switching rate by increasing the gate resistance without concerning about the increased possibility of crosstalk occurrence. Here, the turn-on has been done using a high value with 100 Ω resistance, while the turn-off has been through a 10 Ω resistance. This is unlike the simple gate driver where both the turn-on and turn-off are done through the same single gate resistance, here with a value of 100 Ω.

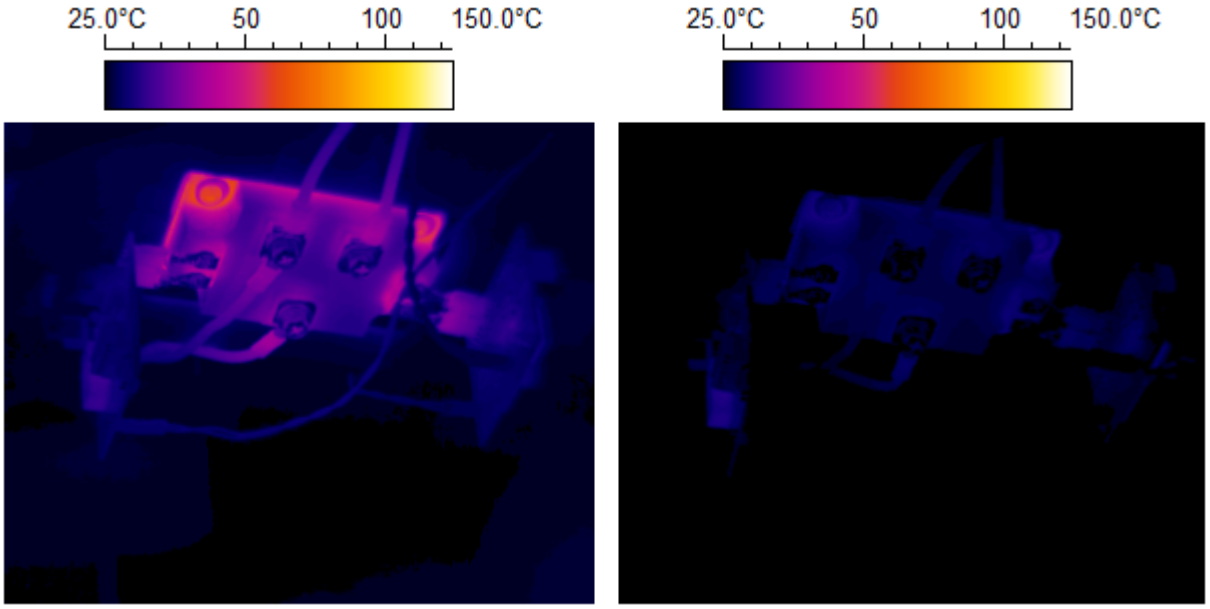


Figure 6.39: Thermal camera image of the SiC MOSFET module switching at 8 kHz with using the two resistive paths when both devices are connected to R_G of (left) 100 Ω or (right) its equivalent in two resistive paths.

The turn-off gate resistance provides a pathway for the Miller capacitance charging current and will result in induced gate voltage. Therefore its value is a determining factor in severity of crosstalk. Hence the use of two resistive paths is a very practical approach to

mitigate the possible effect of crosstalk on the non-switching power devices in a module. It should be noted that this method has its own limitations as well. The minimum value for the turn-off gate resistance should be determined according to the datasheet of the gate driver, since a too low value causes a high return (sinking) gate current and can lead to destruction of the gate driver during normal operation. Figure 6.40 shows the impact of using the unipolar and bipolar gate drivers with the combination of high device switched with R_G of 10 Ω while low device is connected to R_G of 100 Ω. This combination represents the worst case scenario for shoot-through currents. It can be seen from Figure 6.40 that the bipolar gate driver has assisted in the significant reduction of the temperature rise on the module as a result of the repetitive shoot-through currents.

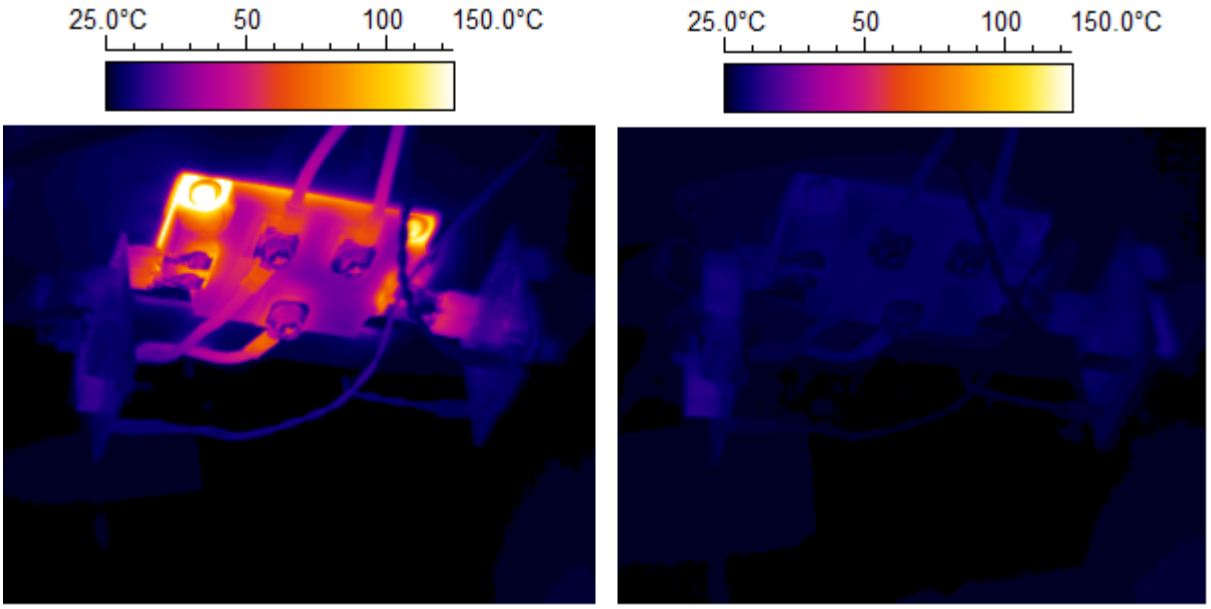


Figure 6.40: Thermal camera image of the SiC MOSFET module switching at 8 kHz with (left) unipolar and (right) bipolar drives with high side device R_G of 10 Ω and low side device R_G of 100 Ω.

It should be noted that as was seen in Figure 6.34 (for both devices switched with 10 Ω), in SiC modules the use of a bipolar gate driver will not remove the shoot-through

energy completely. However increasing the low side R_G from 10 Ω to 100 Ω causes enough impact to see an actual reduction. This solution is also not trivial on its own as the power converters are normally in operation for long periods of time, and the temperature rise as a result of the shoot-through energy might eventually become too high. This can be seen in greater detail through the temperature plots in the next section.

6.5.1 Thermal Profiles

To understand the significance of crosstalk on the operating temperature of a converter, thermal profiles are provided. Figure 6.41 shows the plot of temperature rise of the base of the silicon IGBT and SiC MOSFET power modules. As can be seen in Figure 6.41, increasing the low side gate resistance has increased the rate at which the temperature of the modules rises. It can also be seen that the increase is more uniform in SiC MOSFET module compared with the silicon IGBT module. This is in agreement with the trend seen in Figure 6.23. It is observed that although the temperature rise in the SiC MOSFET module in most cases is higher than that of the silicon IGBT module, however the change of the temperature slopes is more uniform and the slope in the temperature rise in the silicon module is higher, i.e. where the low side device is connected to 100 Ω, the silicon device reaches the thermal runaway point faster. The SiC module, due to the wider bandgap and more advanced packaging can cope with temperatures up to 150 °C easier, while in the case of silicon device, it failed after reaching a temperature around 120 °C.

Figure 6.42 provides a clearer comparison between the temperature rise of the silicon IGBT and SiC MOSFET modules. In this figure, the low side gate resistance is fixed to 100 Ω for all cases while the high side gate resistance is varied between 10 and 100 Ω for both the silicon IGBT and SiC MOSFET modules. As can be seen in Figure 6.42, the

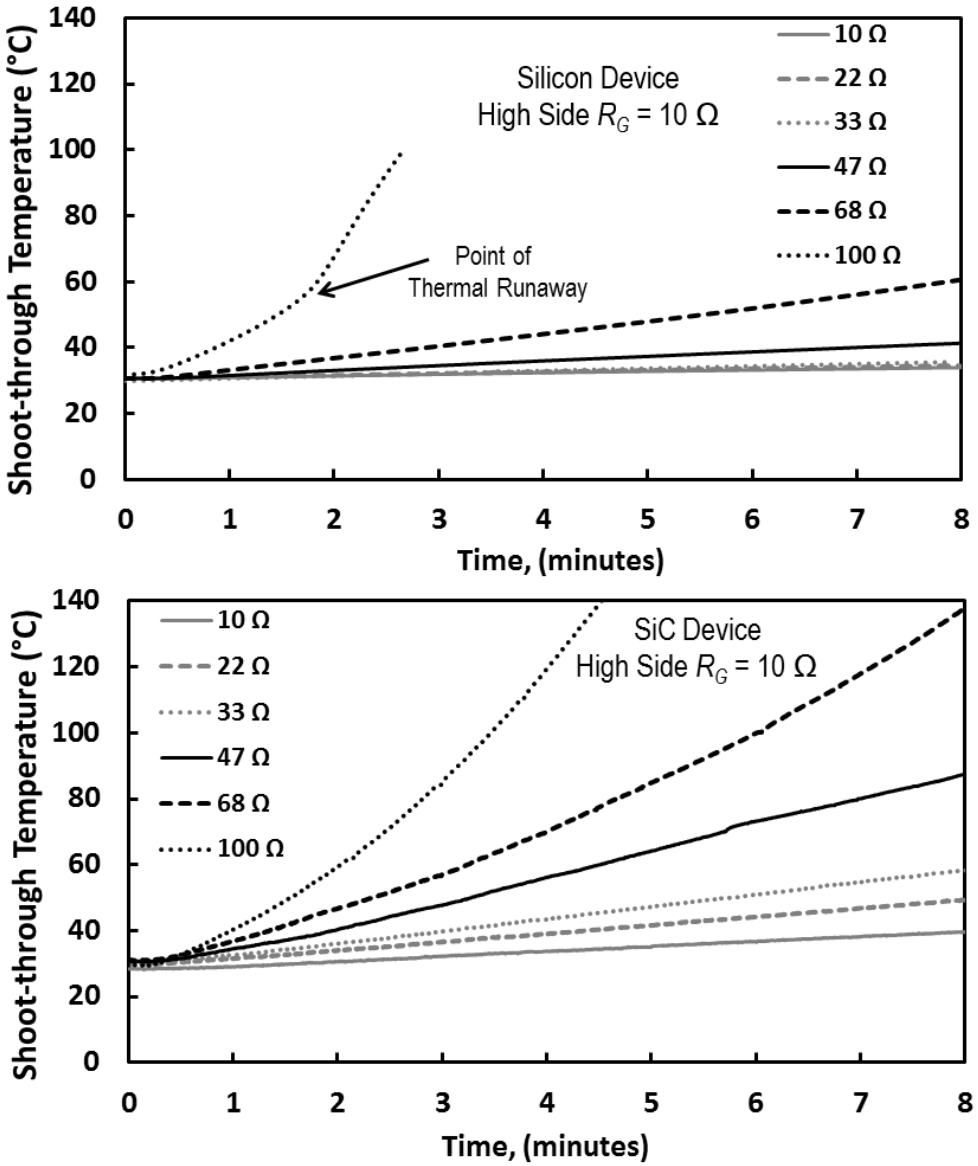


Figure 6.41: The temperature rise in the (a) Si-IGBT and (b) SiC MOSFET module as a result of the increasing the low side gate resistance.

difference between the temperature rise in the two cases of gate resistance combinations is higher for the silicon module compared to the case of the SiC module. The reason for this difference is the more pronounced slope of change of shoot-through energy with gate resistance in the silicon IGBT module. This is clear in the Figure 6.16.

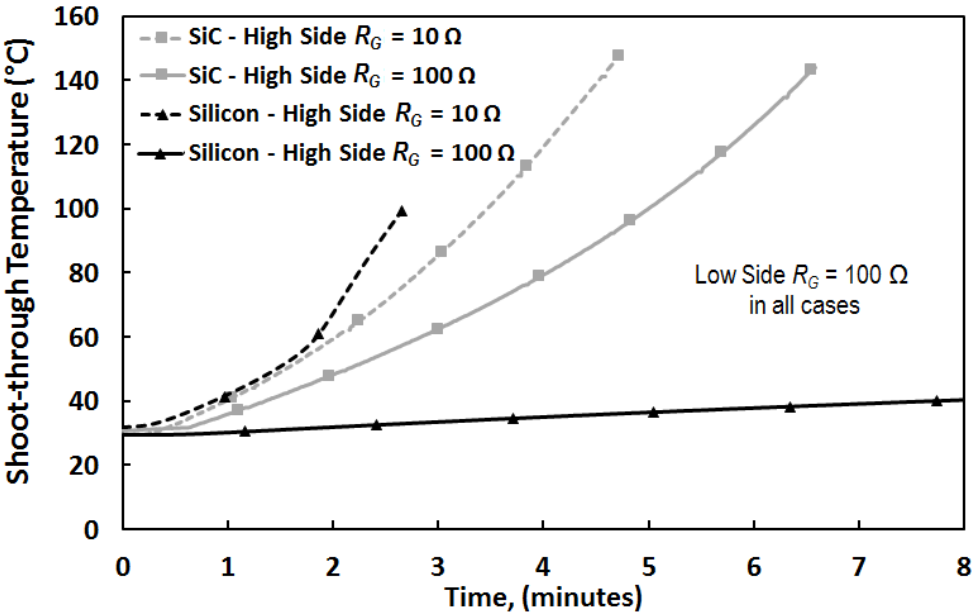


Figure 6.42: The temperature rise due to shoot through currents in both modules with the low side R_G of 100 Ω in all cases.

Figure 6.43 shows the temperature rise in both modules (a) for the silicon module and (b) for the SiC module, where a de-coupling capacitor and a bipolar drive is connected. Again, these measurements have been done for the worst case scenario with a higher dV/dt from a 10 Ω high side gate resistance and a 100 Ω low side gate resistance. The presence of the bipolar drive in both cases has considerably reduced the temperature rise, although the reduction is more significant in the case of the silicon module. The de-coupling capacitor has also reduced the temperature slope, which is due to the reduction of the shoot-through energy through damping the overshoots and ringing of the voltages.

Hence it is recommended that in all cases, especially where SiC modules are to be used, the two resistive paths method to be applied along with the use of a bipolar gate driver with a negative value in-line with datasheet requirements and a high frequency de-coupling capacitor to be placed on the DC link connection of the module with similar voltage rating and appropriate capacitance to damp the oscillations.

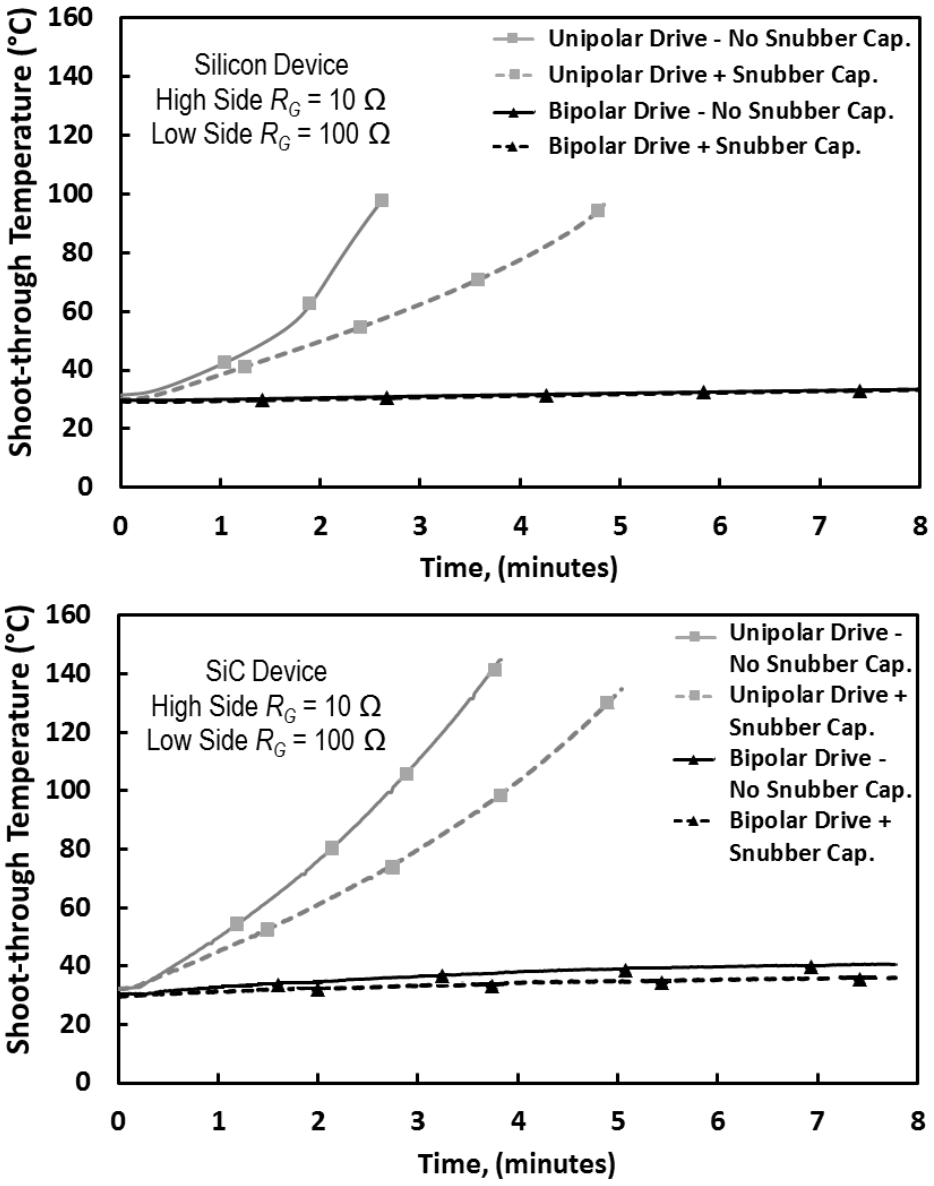


Figure 6.43: The temperature rise due to shoot-through currents in (a) Si-IGBT and (b) SiC modules with and without de-coupling capacitors and bipolar gate drives.

6.6 Summary

Crosstalk is modeled and experimentally characterized for SiC MOSFET and Si-IGBT power modules. It is demonstrated that SiC devices in some cases have a lower shoot-

through charge although often exhibit higher shoot-through energy. The lower shoot-through charge is due to a smaller Miller capacitance in SiC MOSFETs compared with Si-IGBTs in spite of switching with higher dV/dt and a lower threshold voltage. However, cases with higher shoot-through energy in SiC MOSFET modules are due to the ringing in the Schottky diode turn-off transient resulting in oscillations in the DC link voltage. It has also been demonstrated that the shoot-through charge in Si-IGBT module has a higher temperature coefficient, i.e. it is more sensitive to ambient temperature rise. The temperature coefficient of the shoot-through charge in SiC is lower as a result of the lower threshold voltage temperature coefficient resulting from the wide-bandgap properties.

A variety of techniques have been examined to mitigate the problem. For Si-IGBT modules, the traditional solutions of negative gate bias and/or two resistive paths are sufficient for mitigation; however for the SiC MOSFET modules, the bipolar gate driver is not adequate to completely remove the crosstalk since the threshold voltage of SiC devices is low and the dV/dt remains high. Furthermore, negative bias rating of the SiC MOSFET is lower than that of the Si-IGBTs, hence, margins for negative bias are smaller. Additionally, it has been shown that the presence of the high frequency de-coupling capacitor is required to damp the high frequency oscillations in the DC link resulting from the ringing in the case of SiC devices. Several measurements were done to investigate the self-heating issue of the modules as a result of the crosstalk and as was seen, if the issue is not mitigated, it can lead to high temperatures on the module with serious reliability consequences. It is seen that for the Si-IGBT modules, the conventional bipolar gate driver with a negative bias value of at least five volts would suffice to mitigate the shoot-through, whereas in the case of SiC devices, due to the restrictions over the negative bias gate voltage, the two resistive paths method in conjunction with the bipolar gate driver and the high frequency de-coupling capacitor are recommended.

Chapter

7 Conclusions and Future Work

This chapter outlines the conclusions that have arisen from this research. These conclusions provide a better understanding on how SiC devices are superior to their silicon counterparts and where are the possible weak points which still need to be addressed. Hence, upon drawing the conclusions, possible future work is also discussed, to provide a pathway for future studies.

7.1 Conclusions

This research study, in its own capacity, has tried to explicate the performance superiority of SiC devices as well as to address the reliability concerns regarding this emerging device technology. As was discussed in earlier chapters, although SiC devices are promising in theory and there is some good evidence to demonstrate this, they exhibit certain challenges in application that must be further evaluated. Some of these drawbacks are already known to various degrees while others have not been adequately characterized/comprehended.

The research presented in this thesis shows that the switching rates of power devices are temperature dependent as the switching rate of the SiC MOSFETs exhibits a positive

temperature coefficient at turn-on and a negative temperature coefficient at turn-off while Si-IGBTs show a negative temperature coefficient for both turn-on and turn-off. Hence, the switching energy of the SiC MOSFET at turn-on has been shown to decrease with temperature whereas that of the Si-IGBT increases. At high switching rates, the switching energy of the PiN diode is dominated by the peak reverse recovery charge stored in the drift region and high diode voltage overshoots while in SiC diodes, the switching energy at small gate resistances is dominated by diode ringing. To predict the impact of these characteristics and the expected trends, accurate analytical models were developed.

First, a fairly accurate analytical model was developed that correctly emulates the measurements of PiN diode switching energies as a function of the switching rate and temperature. The model is capable of predicting the switching energy of PiN diodes switched at different rates and temperatures. Measurements also showed that the slope of the diode's recombination current is critical during turn-off in determining the switching energy because the diode current is in recombination at the time when its voltage is at its peak. For SiC Schottky barrier diodes, the turn-off voltage ringing has been shown to increase with temperature for a fixed gate resistance due to the fact that the switching rate increases with temperature during MOSFET turn-on. It was also shown that the rate of increase of the turn-on switching rate with temperature (the temperature coefficient of the switching rate) increases with the gate resistance up to an optimum point, after which it again decreases. This resulted in greater diode voltage dependence on temperature for intermediate switching rates. Hence, the switching energy of the SiC SBD is shown to be a combination of 3 switching phases namely the current switching phase, the voltage switching phase and the ringing phase. While the switching energy of the current switching phase decreases with increasing switching rate, the switching energy of the voltage switching phase and the ringing phase increases with the switching rate (this is due to

the fact that damping reduces as the switching rate increases hence, the overshoot losses dominate at high switching speeds). Thereby, as the gate resistance which determines the switching speed of the low side MOSFET is increased, the switching energy initially decreases as the overshoots become better damped. However, beyond an optimum R_G, it starts increasing again since the switching energy of the current switching phase (which increases as the switching rate is reduced) starts to dominate the total switching energy.

Aside ringing, another reliability concern regarding high voltage SiC MOSFETs is the ability of the body diode to reverse conduct without triggering the parasitic BJT into latch-up. Here, the body diode reverse recovery characteristics of silicon and SiC devices were also compared at different switching rates, temperatures and supply voltages. It was seen experimentally that 1.2 kV SiC MOSFETs exhibit the lowest switching energy followed by the 1.2 kV silicon power MOSFET and the 900 V silicon superjunction MOSFET (CoolMOS™). This is very promising, since unlike the silicon devices, the SiC devices do not have significant reverse recovery and can thus be used in applications as anti-parallel diodes (although the use of body diodes as alternatives to external discrete diodes is usually not recommended). The lower switching energy is possible due to the fact that the minority carrier lifetime in the voltage blocking drift layer of the SiC MOSFET is lowest; hence, the PiN body diode stores the least amount of charge during forward conduction mode. The reverse recovery charge in the CoolMOS™ was also the largest as a consequence of the superjunction structure resulting in excess minority carrier storage.

Additionally it was seen that the total reverse charge and peak reverse current in silicon power MOSFET and superjunction devices increase with the temperature, whereas in the SiC MOSFET, these parameters are nearly temperature invariant. This temperature-invariance can also be counted as another advantage of the SiC devices, over silicon devices. In terms of the robustness of the body diodes, it was shown that the CoolMOS™

and SiC MOSFETs exhibited the highest latch-up current followed by the silicon power MOSFET. Here, the latch-up current was defined as the minimum forward current through the body diode capable of inducing parasitic BJT latch-up during turn-off at a fixed supply voltage, temperature and switching rate. Furthermore, the SiC MOSFET showed the highest latch-up current density (since it has the smallest die area) followed by the silicon superjunction MOSFET and the silicon power MOSFET. The promising points of the SiC MOSFETs demonstrated here confirm that the body diode of the SiC MOSFETs exhibits the least reverse recovery, as well as acceptable robustness under hard commutation.

Another application consideration of SiC MOSFETs investigated in this thesis is crosstalk between complementary power devices in converter phase legs. The short-circuit current resulting from crosstalk is directly proportional to the Miller capacitance, the voltage commutation rate, the gate resistance of the unintentionally switched device while it is inversely proportional to the threshold voltage. The short-circuit current has also been shown to increase with temperature as a result of the negative temperature coefficient of the threshold voltage. It has been experimentally demonstrated that SiC devices normally have a lower shoot-through current/charge although often exhibit higher shoot-through energy. The lower shoot-through charge/current is due to a considerably smaller Miller capacitance in SiC MOSFETs compared with Si-IGBTs in spite of switching with higher dV/dt and having a lower threshold voltage. However, the higher shoot-through energy in SiC MOSFET modules is due to the ringing in the Schottky diode turn-off transient (as was explained earlier) which results in oscillations in the DC link voltage.

It has also been demonstrated that the shoot-through charge in Si-IGBT module has a higher temperature coefficient for all conditions, meaning that it is more sensitive to ambient temperature rise. The temperature coefficient of the shoot-through charge in SiC is lower as a result of the lower threshold voltage temperature coefficient resulting

from the wide-bandgap characteristics. The effectiveness of various correction techniques have been examined for SiC MOSFET and Si-IGBT modules. For the Si-IGBT modules, the traditional solutions of negative gate bias and/or 2 resistive paths are sufficient in mitigating the problem. However, for the SiC MOSFET modules, the bipolar gate driver is not adequate to completely resolve the crosstalk since the threshold voltage of SiC devices is low and the dV/dt remains high. Furthermore, negative bias rating of the SiC MOSFET is lower than that of Si-IGBTs, hence, the margins for negative bias are smaller. It is also shown that presence of the de-coupling capacitor is required to damp the high frequency oscillations in the DC link resulting from the low side SiC SBD ringing.

Hence, crosstalk as a problem is less in the SiC MOSFET module compared to the Si-IGBT module, however, the common mitigation techniques employed to correct it are less effective in the SiC MOSFET module. The recently announced improvement in the negative voltage rating of CREE® SiC MOSFETs shows that this is a problem that they recognize and are actively trying to solve. This is an active research problem currently being tackled by academia and industry as evidenced by the recent research papers.

7.2 Future Work

As has been demonstrated in this thesis, medium voltage SiC devices exhibit different characteristics compared to their silicon counterparts. While SiC clearly demonstrates lower switching energies and improved conduction losses compared to silicon IGBTs, MOSFETs and CoolMOS™ devices, there are some practical problems (like ringing, body diode robustness and crosstalk) regarding how these advantages can be exploited in applications. This opens up avenues for further research in the performance and application of these devices in power converters, etc. Very high voltage SiC devices (>10kV) are cur-

rently being developed in specialist laboratories and are expected to become commercially available in near future [13]. While 10 kV MOSFETs have been demonstrated, SiC bipolar devices like the 15 kV SiC IGBT reported by CREE® are also under research [133]. These devices are targeted for grid connected power conversion like HVDC and FACTS.

However, as of today, silicon IGBTs and Thyristors are still the devices of choice for such high voltage applications. These schemes normally have a long lifetime expectancy, i.e. a minimum of 40 years of operation. Since the SiC devices, especially those aiming at voltages above a few kilo-volts, are recently emerged, the lack of historical reliability data means that potential customers are hesitant to deploy the technology into application spaces where robustness is critical. Unlike the low and medium voltage power industries, the high voltage grid related electronics industry is very conservative and as a consequence, is quite slow in adopting new technologies. Hence, the reliability issues of SiC must be demystified for confidence to increase in the semiconductor.

7.2.1 Performance Evaluation of Unipolar SiC Devices

As the voltage ratings of power devices increase, inevitably, the drift region thickness also increases and its doping level is reduced. This is the well-known silicon limit that arises from the fact that less resistive epitaxial layers are needed to block higher voltages. Such limit applies to SiC as well although to a lesser extent. This can hinder the performance advantages gained by the SiC devices as the voltage capability is increased to higher levels. The silicon limit is why silicon MOSFETs are not the preferred technology for 1 kV applications and why IGBTs and SiC have taken up that application space.

Hence, in SiC unipolar devices which aim to block voltage ratings above a few kV, it is vital that the on-state conduction of the devices to be evaluated. This can be done

using the classic double pulse switching set-up to analyze the transients, and continuous switching schemes for temperature rise, condition monitoring and power cycling purposes. The latter topic is of extra importance since it will help to understand the degradation of the device performance and whether or not continues thermal losses impact their long-term characteristics. Investigation of the performance of SiC unipolar devices is also important as the next generation of SiC devices are emerging; an example of which is the industry's first commercially available 1.2 kV SiC Trench MOSFET by ROHM® industries which was announced on 26 May 2015 (BSM180D12P3C007) which compared to its planar counterpart (BSM180D12P2C101) claims to have 42% less switching losses [134]. Such structures are potentially feasible to achieve for higher voltage ratings as well.

7.2.2 Performance Evaluation of Bipolar SiC Devices

Recently, there has been a lot of effort to fabricate high voltage SiC bipolar devices since theoretically, they may provide many advantages in applications. Applications like modular multilevel converters in VSC-HVDC systems will benefit from higher voltage rated power devices since it can potentially reduce the number of levels for a given DC transmission voltage. However, the issue of high on-state resistance is not only limited to unipolar devices. One of the main challenges impeding the fabrication of high voltage SiC bipolar devices is the low carrier lifetime of SiC, which causes the lack of an acceptable level of conductivity modulation formed in their drift region. Hence, high voltage SiC PiN diodes and IGBTs also exhibit high on-state resistances and therefore their practicality in applications is questioned. Hence, more research effort is required to overcome the limitation of low minority carrier lifetime in SiC bipolar devices so that conductivity modulation in SiC may take the devices to even higher voltage levels.

7.2.3 Reliability Studies

Another avenue for future studies, which is of high importance, is reliability analysis in SiC devices. These studies can focus on different aspects of the device application, one of which is the analysis of the robustness of gate oxide. Fortunately the gate dielectric insulator in SiC MOSFETs, similar to silicon devices, is fabricated by the thermal oxidation of the semiconductor; however, despite having a native oxide, there are still issues with the performance of the gate oxide in SiC. Degradation of the oxide in SiC devices causes a permanent drift of the threshold voltage, which in turn can be detrimental when it comes to paralleling the devices (as devices will switch with different rates) as well as limiting off-state power dissipation. This is due to a non-ideal interface between SiC and SiO_2 at the point of contact. This also limits the magnitude of negative gate bias applicable on the device, keeping in mind that negative biasing is needed to mitigate crosstalk. Hence, due to the high dV/dt ranges of SiC MOSFET and low margins for negative gate bias, it is necessary that further research is done to address the problem of crosstalk in SiC power modules designed for fast switching. At the root of the issue is the negative/positive charge trapping in the defects of the SiC/SiO_2 interface which requires further investigation.

Another reliability concern of SiC devices which requires more investigation is the avalanche breakdown limits along with the robustness of the body diode at high voltages. These have already been demonstrated for 1.2 kV SiC MOSFETs under unclamped inductive switching compared to silicon IGBTs and the characteristics of the body diode were also investigated in this thesis. However, as devices with higher voltage ratings are released, it will be necessary to extend these investigations. Parallel application of SiC devices with silicon devices can also be an area of interest which should be further investigated. For instance, the interaction between silicon IGBTs and SiC Schottky diodes or

SiC MOSFETs and silicon PiN diodes. Reliability of SiC superjunction devices, if they become commercially available, is also another subject matter which merits investigation.

7.2.4 Modeling

This thesis provided accurate analytical models for switching energy of silicon PiN and SiC Schottky barrier diodes. The devices analysed here are the leading technologies used in current rectifiers. However, these analytical models can be also extended to other power devices in many practical areas of power electronics. As an example, SiC Thyristors are already being fabricated for high voltage applications and can practically replace silicon Thyristors in areas such as HVDC power transmission. In this case, management of power losses and the excessive heat generated is of extra importance and hence, it is necessary for engineers to have accurate analytical models to estimate the switching energy of these devices as well as the conduction losses from the on-state resistance. These models can enable the determination of the switching energy of power devices without requiring details of semiconductor device physics and hence are practical. Therefore, further research into the extension of the analytical models is necessary.

7.3 Final Words...

The future of power electronics will depend on efficiency, power density, cost and reliability. From this perspective, SiC power devices are very promising, since they enable lower losses in the power converters while switching higher levels of energy in smaller die areas. This has translated into higher efficiency and higher power density compared to silicon devices. Therefore, despite all challenges ahead both in terms of fabrication and application of these power devices, SiC remains as an attractive choice for power electronics.

Appendix

A Publications Titles

For the sake of future reference of the readers, the publications online access links along with the title page of the IEEE Transactions and conference papers extracted from this thesis (in their original published form) are provided here, in order of presented chapters, respectively. The citation details of the papers are mentioned in the publication list on page xiii and the full version of these publications are available on online databases accessible via the links provided here on [135–147].

I. Journal Papers

IEEE Journal of Emerging and Selected Topics on Power Electronics

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6746003

IEEE Transactions on Industrial Electronics

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6878448
- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6822585
- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7299666

IEEE Transactions on Power Electronics

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6844877
- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6853362

An Evaluation of Silicon Carbide Unipolar Technologies for Electric Vehicle Drive-Trains

Saeed Jahdi, *Member, IEEE*, Olayiwola Alatise, *Member, IEEE*, Craig Fisher, *Member, IEEE*, Li Ran, *Senior Member, IEEE*, and Philip Mawby, *Senior Member, IEEE*

***Abstract*— Voltage sourced converters (VSCs) in electric vehicle (EV) drive-trains are conventionally implemented by silicon Insulated Gate Bipolar Transistors (IGBTs) and p-i-n diodes. The emergence of SiC unipolar technologies opens up new avenues for power integration and energy conversion efficiency. This paper presents a comparative analysis between 1.2-kV SiC MOSFET/Schottky diodes and silicon IGBT/p-i-n diode technologies for EV drive-train performance. The switching performances of devices have been tested between −75 °C and 175 °C at different switching speeds modulated by a range of gate resistances. The temperature impact on the electromagnetic oscillations in SiC technologies and reverse recovery in silicon bipolar technologies is analyzed, showing improvements with increasing temperature in SiC unipolar devices whereas those of the silicon-bipolar technologies deteriorate. The measurements are used in an EV drive-train model as a three-level neutral point clamped VSC connected to an electric machine where the temperature performance, conversion efficiency and the total harmonic distortion is studied. At a given switching frequency, the SiC unipolar technologies outperform silicon bipolar technologies showing an average of 80% reduction in switching losses, 70% reduction in operating temperature and enhanced conversion efficiency. These performance enhancements can enable lighter cooling and more compact vehicle systems.**

***Index Terms*— Electric vehicles (EVs), power semiconductor devices, pulsewidth modulation (PWM) converters, silicon carbide, switching circuits.**

I. Introduction

POWER electronics for electric vehicle (EV) drive-trains is essential for high efficiency energy conversion [1], [2]. Transiting from slow switching silicon bipolar to fast switching SiC unipolar technologies is expected to improve the performance and efficiency of EVs [3]. Silicon carbide technology has increased the voltage range of MOSFETs. The wide-bandgap and higher critical electric field means that higher voltages can be blocked with thinner and more conductive epitaxial layers. The higher thermal conductivity will make them more temperature rugged and the wider bandgap means less leakage currents and reduced probability of thermal runaway in high temperature applications. Thus, 1.2-kV SiC MOSFETs and Schottky diodes have been manufactured by CREE and ROHM (among others) with very low conduction losses and are now commercially available. SiC MOSFETs with blocking voltages as high as 10 kV [4]–[6] and with increasingly higher currents have also been demonstrated [7]. The feasibility of SiC technology for energy conversion in fully rated power converters for wind turbine energy conversion and fuel-cell systems was explored in [8] and [9] and the implementation of SiC devices in motor control drive-trains has been explored in [10]. The impact of SiC unipolar devices on the system level performance of hybrid EV power-trains was investigated in [11], where it was observed that system efficiency as well as compactness was improved. The use of SiC devices in an on-board EV battery charger was also investigated in [12] with results showing improved efficiency.

The goal of this paper is to investigate the impact of SiC unipolar devices in EVs through both simulations and experimental characterization of switching transients. To ensure high fidelity of model results, the power device switching models in the converter have been parameterized by extensive experimental measurements over a wide range of temperatures (−75 °C and 175 °C) and switching rates. The temperature dependency of the current and voltage transients will be analyzed and the impact of the switching rate on voltage oscillations and reverse recovery will be discussed. 1.2-kV SiC MOSFETs and Schottky diodes are compared with similarly rated silicon Insulated Gate Bipolar Transistors (IGBTs) and p-i-n diodes and a three-level three-phase neutral point clamped (NPC) voltage source converter is used together with a PMSM motor model to emulate the EV drive-train. Section II presents the experimental test setup and preliminary measurement results, Section III discusses the temperature behavior of the power devices, Section IV discusses the EV drive-train models while Section V concludes this paper.

II. Clamped Inductive Switching Measurements

Fig. 1 shows circuit schematic of the clamped inductive switching test rig using a standard double-pulse method while Fig. 2 shows the picture of the experimental setup designed for this purpose. The SiC MOSFETs are ROHM devices (SCH2080KE) rated 35 A at $T_C = 25$ °C and 22 A at $T_C = 100$ °C whereas the SiC diodes are semisouth

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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Accurate Analytical Modeling for Switching Energy of PiN Diodes Reverse Recovery

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***Abstract*—PiN diodes are known to significantly contribute to switching energy as a result of reverse-recovery charge during turn-OFF. At high switching rates, the overlap between the high peak reserve-recovery current and the high peak voltage overshoot contributes to significant switching energy. The peak reverse-recovery current depends on the temperature and switching rate, whereas the peak diode voltage overshoot depends additionally on the stray inductance. Furthermore, the slope of the diode turn-OFF current is constant at high insulated-gate bipolar transistor (IGBT) switching rates and varies for low IGBT switching rates. In this paper, an analytical model for calculating PiN diode switching energy at different switching rates and temperatures is presented and validated by ultrafast and standard recovery diodes with different current ratings. Measurements of current commutation in IGBT/PiN diode pairs have been made at different switching rates and temperatures and used to validate the model. It is shown here that there is an optimal switching rate to minimize switching energy. The model is able to correctly predict the switching rate and temperature dependence of the PiN diode switching energies for different devices.**

***Index Terms*—Analytical modeling, PiN diodes, reverse recovery, switching energy, switching transient.**

NOMENCLATURE

I_F	Forward current (A).
I_{RR}	Peak reverse recovery current (A).
dI_{TF}/dt	Overall dI/dt of turn-OFF current at high dI/dt (A/s).
$dI_{\mathrm{TF}+}/dt$	dI/dt of turn-OFF current before zero-crossing (A/s).
$dI_{\mathrm{TF}-}/dt$	dI/dt of turn-OFF current after zero-crossing (A/s).
dI_{RR}/dt	Primary dI/dt of recovery current (A/s).
dI_{Tail}/dt	Secondary dI/dt of recovery tail current (A/s).
$d^2I_{\mathrm{TF}}/dtdT$	Primary dI/dt of recovery current (A/s°C).
E_{SW}	Switching energy (J).
V	Absolute value of the switching voltage (V).
V_{AK}	Diode peak overshoot (V).
V_{D}	Absolute value of the diode on-state voltage drop (V).
L	Stray parasitic inductance (H).
K_Q	Function of junction temperature $(\mathrm{C/A}^{0.5})$.
K	Ratio of dI/dt of recovery current to turn-OFF.
S	Ratio of the recovery time to the turn-OFF time as a measure of the diode snappiness [1].
t	Time (s).
T	Temperature (°C).

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I. INTRODUCTION

POWER PiN diodes are a critical device technology for power conversion both for automotive and grid-connected applications. Although SiC Schottky diodes have increasingly become popular as a replacement for silicon PiN diodes, as far as power conversion at very high levels and medium frequencies are concerned, silicon PiN diodes remain unrivaled in delivering low-conduction ON-state energy dissipation. These diodes are commonly used as antiparallel diodes with insulated-gate bipolar transistors (IGBTs) or metal–oxide–semiconductor field-effect transistors (MOSFETs) in self-commutated voltage-source converters [2]. In power conversion applications where low switching frequencies are to be used, e.g., modular multilevel converter voltage-source converter for offshore wind power transmission, PiN diodes remain the technology of choice for low-conduction ON-state energy dissipation. Moreover, SiC PiN diodes have been demonstrated with very high voltage-blocking capability [3]. PiN diodes are bipolar devices that rely on conductivity modulation from minority carrier injection to deliver low-conduction ON-state energy dissipation. As a result, minority carrier recombination and recovery during switching periods limits the maximum switching frequency that can be used in power conversion. The reverse-recovery charge during the turn-OFF of the PiN diode is known to be the highest contributing factor to switching energy in PiN diodes [4]. Furthermore, the diode voltage overshoot arising from stray inductances also contributes to the switching energy. Both the peak reverse-recovery current and voltage overshoot increase with dI/dt, which is controlled by the RC time constant of the IGBT. The diode parasitic capacitance and circuit stray inductance will also determine the rate at which the diode ramps down the current [5].

Models developed for the PiN diode's reverse-recovery transients fall mainly into two categories: physics-based SPICE models (which require device physics parameters) and

The Impact of Temperature and Switching Rate on the Dynamic Characteristics of Silicon Carbide Schottky Barrier Diodes and MOSFETs

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***Abstract*—Silicon carbide Schottky barrier diodes (SiC-SBDs) are prone to electromagnetic oscillations in the output characteristics. The oscillation frequency, peak voltage overshoot, and damping are shown to depend on the ambient temperature and the metal–oxide–semiconductor field-effect transistor (MOSFET) switching rate ($dI_{\rm DS}/dt$). In this paper, it is shown experimentally and theoretically that $dI_{\rm DS}/dt$ increases with temperature for a given gate resistance during MOSFET turn-on and reduces with increasing temperature during turn-off. As a result, the oscillation frequency and peak voltage overshoot of the SiC-SBD increases with temperature during diode turn-off. This temperature dependence of the diode ringing reduces at higher $dI_{\rm DS}/dt$ and increases at lower $dI_{\rm DS}/dt$. It is also shown that the rate of change of $dI_{\rm DS}/dt$ with temperature ($d^2I_{\rm DS}/dtdT$) is strongly dependent on R_G and using fundamental device physics equations, this behavior is predictable. The dependence of the switching energy on $dI_{\rm DS}/dt$ and temperature in 1.2-kV SiC-SBDs is measured over a wide temperature range (-75 °C to 200 °C). The diode switching energy analysis shows that the losses at low $dI_{\rm DS}/dt$ are dominated by the transient duration and losses at high $dI_{\rm DS}/dt$ are dominated by electromagnetic oscillations. The model developed and results obtained are important for predicting electromagnetic interference, reliability, and losses in SiC MOSFET/SBDs.**

***Index Terms*—Oscillation, power metal–oxide–semiconductor field-effect transistor (MOSFET), Schottky diodes, silicon carbide (SiC), temperature.**

I. Introduction

SILICON carbide (SiC) unipolar devices have now become commercially available with voltage ratings of 1.2 kV, and higher voltage ratings are expected in the near future [1]–[4]. These temperature-rugged and power dense devices have repeatedly demonstrated improved energy conversion efficiency and reduced losses when implemented in power converters [5]–[12]. Since these devices are unipolar and are therefore not limited by minority carrier storage from conductivity modulation, they are fast switching and can be thus implemented in high-frequency applications. High switching frequency can enable size reduction of passive components, which is a significant advantage in applications, where space or size is critical to cost. This may include aeronautical and marine applications. However, advances in packaging technologies are not catching up with devices. Parasitic inductances in power modules induce electromagnetic oscillations in output characteristics, which can be detrimental through the additional losses and reduced reliability [13]–[17]. These parasitic inductances depend strongly on the architecture of the power module and its layout. However, as the switching frequency increases, even small parasitic inductances cannot be ignored because of the high $dI_{\rm DS}/dt$. It is well understood that SiC Schottky diodes are particularly prone to ringing as parasitic capacitances and inductances interact to cause *RLC* resonance [18]. The dependence of this ringing on the ambient temperature and the rate of change of current with time ($dI_{\rm DS}/dt$) of the switching metal–oxide–semiconductor field-effect transistor (MOSFET) has not been fully characterized and understood. The deployment of these 1.2-kV SiC power devices in hard-switched high-temperature modules will require more understanding in the dependence of switching energy on temperature and switching rate [19]. A solution to this ringing problem could be the use of soft-switching techniques, where zero-current and/or zero-voltage switching can be implemented. However, this will increase the cost and complexity of converters at the power levels targeted by SiC.

In this paper, 1.2-kV SiC MOSFETs and SiC Schottky diodes have been tested in a clamped inductive switching test rig. The devices have been tested with a wide range of gate resistances (10–1000 Ω) at ambient temperatures ranging from -75 °C to 200 °C. Using fundamental device equations, the dependence of $dI_{\rm DS}/dt$ on the temperature and gate resistance is derived and shown to accurately replicate the experimental measurements. This temperature dependence is used to explain the performance of the Schottky diode in terms of energy losses. In Section II of this paper, the experimental measurements are presented. In Section III, the MOSFET switching and diode models are presented and compared with the experimental measurements. In Section IV, the switching performance of the SiC-Schottky barrier diode is analyzed, whereas Section V concludes this paper.

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Analytical Modeling of Switching Energy of Silicon Carbide Schottky Diodes as Functions of $dI_{\rm DS}/dt$ and Temperature

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***Abstract*—SiC Schottky Barrier diodes (SiC SBD) are known to oscillate/ring in the output terminal when used as free-wheeling diodes in voltage-source converters. This ringing is due to RLC resonance among the diode capacitance, parasitic resistance, and circuit stray inductance. In this paper, a model has been developed for calculating the switching energy of SiC diodes as a function of the switching rate ($dI_{\rm DS}/dt$ of the commutating SiC MOSFET) and temperature. It is shown that the damping of the oscillations increases with decreasing temperature and decreasing $dI_{\rm DS}/dt$. This in turn determines the switching energy of the diode, which initially decreases with decreasing $dI_{\rm DS}/dt$ and subsequently increases with decreasing $dI_{\rm DS}/dt$ thereby indicating an optimal $dI_{\rm DS}/dt$ for minimum switching energy. The total switching energy of the diode can be subdivided into three phases namely the current switching phase, the voltage switching phase, and the ringing phase. Although the switching energy in the current switching phase decreases with increasing switching rate, the switching energy of the voltage and ringing phase increases with the switching rate. The model developed characterizes the dependence of diode's switching energy on temperature and $dI_{\rm DS}/dt$, hence, can be used to predict the behavior of the SiC SBD.**

***Index Terms*—Analytical modeling, device characterization, Schottky barrier diode (SBD), silicon carbide, switching energy.**

NOMENCLATURE

$V_{\rm AK}$	Diode voltage (V).
$V_{\rm AKpk}$	Peak diode voltage overshoot (V).
$V_{\rm DD}$	Supply (input) voltage (V).
$V_{\rm d}$	Diode on-state voltage drop (V).
$V_{\rm TH}$	Diode threshold voltage (V).
$V_{\rm GG}$	MOSFET gate voltage (V).
$V_{\rm GS}$	MOSFET gate source voltage (V).
$dV_{\rm AK}/dt$	*dV/dt* of turn-OFF voltage of diode (V/s).
$I_{\rm AK}$	Diode current (A).
$I_{\rm F}$	Diode forward current (A).
$I_{\rm PR}$	Diode peak reverse current (A).
$I_{\rm DS}$	MOSFET current (A).
$dI_{\rm DS}/dt$	*dI/dt* of turn-ON current of mosfet (turn-OFF of diode) (A/s).
$L_{\rm STRAY}$	Stray parasitic inductance (H).
$L_{\rm E}$	Circuit energizing inductor (H).
$C_{\rm iss}$	MOSFET input capacitance (F).
$C_{\rm GD}$	MOSFET Miller capacitance (F).
$C_{\rm AK}$	Diode depletion capacitance (F).
$R_{\rm AK}$	Diode depletion resistance (Ω).
$R_{\rm S}$	Parasitic series resistance (Ω).
$R_{\rm G}$	MOSFET gate resistance (Ω).
α	Neper frequency (attenuation factor) of diode response (s^{-1}).
ω	Oscillations (swing) frequency (rad/s).
ζ	Damping factor of diode responde (–).
L	Channel length in device (μm).
W	Channel width in device (μm).
μ	Effective mobility of carriers (cm^2/Vs).
$C_{\rm OX}$	Effective capacitance density ($fF/\mu m^2$).
$E_{\rm SW}$	Switching energy (J).
T	Temperature (°C).
t	Time (s).

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I. INTRODUCTION

SILICON Carbide Schottky barrier diodes (SiC SBD) have shown significant improvements in the performance of rectifiers compared with traditional silicon PiN diodes. The physics and structure of the SiC SBD is presented in [1]–[3], where considerable advantages in terms of higher switching speed, significant reduction in reverse recovery, and better electrothermal performance in harsh environments have been presented [4]. It has previously been shown that the application of SiC SBDs as rectifiers rather than conventional silicon PiN diodes can significantly reduce thermal stress, lower power losses, [5] and enhance the conversion efficiency by removing the reverse recovery of the PiN in the switching transients [6]. As a result, their application as rectifiers in power converters is getting more popular [7]. These include power converters for a range of applications [8] such as power factor correction circuits [9], high power converters [10], [11], and also in harsh environments such as in space applications [12]. Schottky diodes are also used to block the unwanted conduction of the MOSFET body diodes during dead times in power converters [13]. In addition, switching combinations of SiC Schottky diodes with various transistors including silicon power MOSFETs [14], CoolMOS [15], SiC MOSFETs [16], [17], and JFETs [18] have shown significant advantages compared to that of combinations with silicon PiN diodes [19].

An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation

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***Abstract*—The tradeoff between the switching energy and electro-thermal robustness is explored for 1.2-kV SiC MOSFET, silicon power MOSFET, and 900-V CoolMOS body diodes at different temperatures. The maximum forward current for dynamic avalanche breakdown is decreased with increasing supply voltage and temperature for all technologies. The CoolMOS exhibited the largest latch-up current followed by the SiC MOSFET and silicon power MOSFET; however, when expressed as current density, the SiC MOSFET comes first followed by the CoolMOS and silicon power MOSFET. For the CoolMOS, the alternating p and n pillars of the superjunctions in the drift region suppress BJT latch-up during reverse recovery by minimizing lateral currents and providing low-resistance paths for carriers. Hence, the temperature dependence of the latch-up current for CoolMOS was the lowest. The switching energy of the CoolMOS body diode is the largest because of its superjunction architecture which means the drift region have higher doping, hence more reverse charge. In spite of having a higher thermal resistance, the SiC MOSFET has approximately the same latch-up current while exhibiting the lowest switching energy because of the least reverse charge. The silicon power MOSFET exhibits intermediate performance on switching energy with lowest dynamic latching current.**

***Index Terms*—Body diode, electrothermal ruggedness, MOSFET, reverse recovery, robustness.**

I. Introduction

POWER MOSFETs can provide the advantage of faster switching compared to IGBTs which use conductivity modulation from minority carrier injection to limit conduction losses. Conventional high-voltage silicon power MOSFETs have a considerably high on-state resistance which increases the conduction losses. Hence, their use in power converters is limited to high-frequency and low-voltage applications. To improve the conduction losses of the high-voltage silicon power MOSFETs, the concept of the superjunction was introduced as a way of increasing the blocking voltage without using thick and highly resistive drift layers. By using alternate n and p pillars in the drift region, lateral as well as vertical depletion resulted in high blocking voltages with less resistive drift layers, hence, the tradeoff between blocking voltage and on-state resistance is relaxed [1], [2]. Another avenue through which the performance of the power MOSFET was improved was the transition to wide bandgap semiconductors like SiC, where the wider bandgap and higher critical field results in a thinner and less resistive drift layer that can block significantly higher voltages while maintaining a low on-state resistance.

Traditionally, independent discrete diodes are used as reverse conducting or antiparallel diodes so as to enable bidirectional power flow. Integral to the design of the MOSFET is the body diode which has the structure of a PiN diode because of the lightly doped voltage blocking drift layer between the n^+ drain and the p body. The foremost characteristic of PiN diodes is in the turn-off transient where reverse recovery can be observed as a result of minority carrier extraction from the drift layer. As the current is ramped down during the turn-off process in the PiN diode, the carrier distribution profile supports the current through the zero crossing until the voltage across the diode causes depletion widths at the diode PN and NN^+ junctions. Once this space charge region forms, the reverse current reaches its peak value (which is the peak reverse recovery current) and then starts to recover to zero. The time it takes for the current to return to zero depends on the rate of minority carrier recombination in the drift region, which in turn is a function of the temperature-dependent carrier lifetime amongst other parameters. Although it is generally desirable for the PiN diode to have a minimum reverse recovery time, it can be hazardous if the rate of change of the current with time is very high in the presence of parasitic inductances. PiN diode reverse recovery can be considered to be soft or snappy depending on the ratio between the time taken for the current to change between 0 and the peak reverse current and the time taken to return from that peak reverse current to 0. The voltage across the diode moves from the on-state voltage to the supply voltage, although there is usually a peak voltage overshoot due to parasitic inductance and a time varying current. The peak voltage overshoot occurs at the time when the diode is in reverse recovery, hence, snappy diodes can cause high-peak voltages and *dV/dt* induced avalanche breakdown capable of destroying the diode. The well-known parasitic npn BJT in the MOSFET can be activated by the displacement

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Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules

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***Abstract*—The temperature and dV/dt dependence of crosstalk has been analyzed for Si-IGBT and SiC-MOSFET power modules. Due to a smaller Miller capacitance resulting from a smaller die area, the SiC module exhibits smaller shoot-through currents compared with similarly rated Si-IGBT modules in spite of switching with a higher dV/dt and with a lower threshold voltage. However, due to high voltage overshoots and ringing from the SiC Schottky diode, SiC modules exhibit higher shoot-through energy density and induce voltage oscillations in the dc link. Measurements show that the shoot-through current exhibits a positive temperature coefficient for both technologies, the magnitude of which is higher for the Si-IGBT, i.e., the shoot-through current and energy show better temperature stability in the SiC power module. The effectiveness of common techniques of mitigating shoot-through, including bipolar gate drives, multiple gate resistance switching paths, and external gate–source and snubber capacitors, has been evaluated for both technologies at different temperatures and switching rates. The results show that solutions are less effective for SiC-MOSFETs because of lower threshold voltages and smaller margins for negative gate bias on the SiC-MOSFET gate. Models for evaluating the parasitic voltage have also been developed for diagnostic and predictive purposes. These results are important for converter designers seeking to use SiC technology.**

***Index Terms*—Crosstalk, insulated-gate bipolar transistor (IGBT), SiC MOSFET, silicon carbide, temperature.**

I. Introduction

CROSSTALK is an important factor that must be evaluated when using power semiconductor devices in converters. Crosstalk has also been referred to as parasitic turn-on, false turn-on, self-turn-on, etc. [1]. Crosstalk occurs when a device is unintentionally switched on as a result of the intentional switching of the device in the same phase leg. This unwanted turn-on can impose serious reliability concerns since it can result in semi-short-circuits with high currents flowing through the power devices, thereby resulting in high thermal losses and unnecessary electrothermal stresses on the device wire bounds and die [2]. Crosstalk normally happens in synchronous dc–dc converters or in three-phase dc–ac inverters where the devices are intended to turn on with appropriate deadtimes allocated between the switching edges [3], [4]. As one device is turned on, the dV/dt imposed on the complementing device in the same phase leg causes the Miller capacitance to discharge a current into the gate resistance which causes a voltage drop capable of triggering the device if it is greater than its threshold voltage [5]. The main contributors to crosstalk are the magnitude of the Miller capacitance and its ratio compared with the input capacitance of the device, the gate resistance connected to the device (which includes the internal gate resistance of the module), the switching rate, the threshold voltage of the device, and its operating temperature. Equation (1) shows the parasitic gate–source ($V_{\rm GS}$ for MOSFET) or gate–emitter ($V_{\rm GE}$ for IGBT) voltage as a function of the gate resistance (R_G), Miller capacitance ($C_{\rm GD}$), and turn-on dV/dt

$$V_{\rm GS} = R_G C_{\rm GD} \frac{dV_{\rm DS}}{dt} \left(1 - e^{\frac{-t}{R_G(C_{\rm GD}+C_{\rm GS})}}\right). \quad (1)$$

Fig. 1 shows an example of a parasitic (unintended) gate voltage across a SiC MOSFET during turn-on and turnoff of a complementing device.

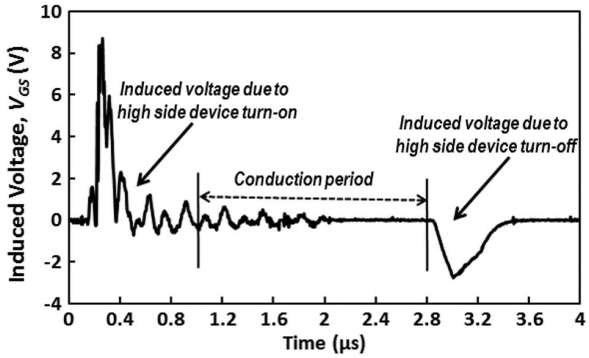

Fig. 1. Measured parasitic gate voltage across a Si-IGBT switched with a dV/dt of up to 10 kV/μs.

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II. Conference Papers

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On the Performance of Voltage Source Converters based on Silicon Carbide Technology

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Abstract

The energy conversion efficiency of voltage source converters based on 1.2 kV silicon carbide MOSFETs and Schottky diodes have been assessed by device measurements and converter simulations. A similar measurement and simulation study has also been performed on a similarly rated 1.2 kV silicon IGBT and PiN diode pair. Transistor to diode current commutation measurements have been performed in a clamped inductive switching test rig for a temperature range between -75^{o}C to 175^{o}C. The measurements have also been performed with different switching rates modulated by a range of gate resistances between 10Ω to 1000Ω. The measurements show that the switching energy of the SiC MOSFETs/SBD pair generally exhibits a negative temperature coefficient whereas that of the silicon IGBT/PiN diode pair exhibits a positive temperature coefficient. Furthermore, the switching energy of the SiC devices are 80% lower than the silicon bipolar technologies. The measurements have been used as inputs into the simulation of a 3 phase, 3-level neutral point clamped voltage source converter. Results from the converter simulations show that the SiC NPC-VSC exhibits 5% higher energy conversion efficiency, 3% less THD and 500% higher maximum switching frequency on average.

1 Introduction

Power electronic converters will become more ubiquitous for future power systems where the connection of distributed renewable energy sources and flexible AC transmission systems (FACTS) will become more common [1]. Variable voltage and variable frequency AC power will need to be converted to fixed voltage and fixed frequency AC power for seamless integration into the electrical grid. These converters will undertake the role of interface with the power system and will be implemented by power semiconductor devices. Currently, silicon bipolar technologies like Thyristors, insulated gate bipolar transistors (IGBTs) and PiN diodes dominate in high voltage applications. They can be series connected for very high voltage applications like HVDC systems or can be arranged in multi-level topologies [2, 3]. The high voltage operability of these devices requires that they rely on the conduction of both carrier types (electrons and holes) via conductivity modulation hence, they switch at slower rates because of long tail currents and reverse recovery charge. MOSFETs are unipolar devices, hence, rely on conduction of only one carrier type. This means they switch faster however are not useable for high voltage applications. This is because thicker and less conductive epitaxial layers are required for blocking higher voltages during the off-state. These layers make the on-state conduction losses unacceptable. Although innovative techniques like super-junction charge balance has improved this on-state resistance breakdown voltage trade-off, this has not extended beyond 1000 V.

Silicon carbide technology has taken MOSFETs into high voltage applications. The wide bandgap and higher critical electric field means that higher voltages can be blocked with thinner and more conductive layers. The higher thermal conductivity makes them temperature rugged and the wider bandgap means less leakage and reduced probability of thermal runaway at higher temperature. As a result, 1.2 kV SiC MOSFETs and Schottky diodes have been manufactured by CREE and ROHM with very low conduction losses and are now commercially available. SiC MOSFETs with blocking voltages as high as 10 kV have also been demonstrated [4-6]. Hence, SiC MOSFETs are poised to penetrate the high voltage energy conversion market for power systems. The high voltage operability of SiC technology can be combined with the high frequency capability of MOSFETs to deliver energy dense power electronics for the future power system. It is therefore important to quantify the impact that SiC can have in this application.

Grid connected converters are required to be more power dense, efficient, reliable and have good power system indices. Power electronics has been cited to be a significant source of harmonics in power systems. Power converters usually have output filters required for filtering out the harmonics generated by the switching of the semiconductors. The sizes of these filters usually depend on the switching frequency of the devices although in multi-level converter topologies this relationship doesn't always hold true. However, in 2 level and 3 level VSCs, fast switching can make a significant difference in the size of the output filters required for meeting the THD compliance of the grid. By using fast switching SiC MOSFETs and SBDs in converters, the filtering requirement can be reduced. The wide bandgap of SiC technology also means that the devices will be more temperature rugged. In this paper, 1.2 kV SiC FETs and SBDs are compared with 1.2 kV Si IGBTs and PiNs over a considerable temperature and dI_{DS}/dt range. The measurements parameters have been implemented in a simulation of a 3 level NPC VSC and the performance is studied. Section II presents the practical test rig

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The Impact of Silicon Carbide Technology on Grid-Connected Distributed Energy Resources

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Abstract— **Distributed Energy sources can be connected to the electrical grid using power electronic converters traditionally implemented in silicon insulated gate bipolar transistors (IGBTs), gate turn-off thyristors (GTOs) and PiN diodes. However, recently developed SiC technology can improve energy conversion efficiency as well as power density. To investigate the benefits provided by SiC technology, experimentally calibrated SiC MOSFET models have been modeled in multilevel voltage sourced converters (VSCs) to analyze the generated harmonics, converter temperature rise, switching losses and filtering requirements. Models show that converters implemented in SiC MOSFETs operate at 25-75% less temperature compared with silicon IGBTs, potentially simplifying cooling. Also, SiC MOSFETs generate ~2% less THD for the same switching frequency and can reduce the switching loss by up to 82% compared to silicon devices.**

***Index Terms*-- Silicon Carbide FETs, Voltage Source Converters, Total Harmonics Distortion, Switching Losses**

I. INTRODUCTION

RECENT advances in wide band-gap semiconductors have opened up new possibilities in the efficiency of power conversion. Silicon carbide (SiC) by virtue of its wider bandgap, higher critical field and higher thermal conductivity can block higher voltages, switch faster and deliver better electrothermal performance under harsh conditions [1]. SiC technology has therefore been studied extensively. The switching performance of SiC power devices in converters has been studied in [2-8] and the combination of SiC power devices and Schottky barrier diodes (SBDs) have been studied in [9-12].

To this end, SiC schottky diodes and MOSFETs have become commercially available at 1.2 kV break-down with increasing current ratings. SiC devices with breakdown voltage ratings as high as 10 kV have been demonstrated in literature with excellent switching characteristics. Researchers have already reported power modules in SiC with at least 19% less switching losses compared with silicon IGBTs. [13] Other researchers have reported a 25% increase in energy density for SiC modules compared with modules implemented in silicon devices for the same frequency. [14-15] An important advantage of SiC devices is the fact that thinner epitaxial layers can block higher voltages thereby delivering high voltage devices with low conduction losses. Furthermore, enabling unipolar devices at higher blocking voltages where bipolar devices are dominant means higher switching frequencies can be used. Unlike bipolar devices like PiN diodes and IGBTs, where charge storage from conductivity modulation means slow switching speeds, unipolar devices (e.g. FETs) are capable of fast switching.

The use of SiC devices for high efficiency and compact power conversion in renewable energy systems is a very promising prospect. Voltage Source Converters (VSCs) are among the most important converters used to integrate power electronics to power systems. VSCs can be applied in HVDC systems as well as flexible AC transmission systems like static VAR compensators. Currently, VSCs are implemented in silicon IGBTs and PiN diodes. Since IGBTs and PiN diodes have limited switching speeds due to long tail currents and high reverse recovery charge, there are limits to the switching frequencies of the VSCs. In some applications, high switching speeds are desirable so that filter sizes can be reduced especially where weight/space come at a premium e.g. off-shore converters in wind energy systems. Filters are in important part of power converters because they mitigate harmonic injection into the grid [16-18]. However, faster switching causes higher base temperatures from higher losses and possibly reduced reliability from increased electro-thermal and thermo-mechanical stress cycling.

In this paper, experimentally measured SiC FET/SBD and silicon IGBT/PiN diode clamped inductive switching results are fed into a 3-level neutral point clamped VSC model. The impact of the technologies on generated harmonics and operating temperature is analyzed. Section II discusses the experimental set-up, section III discusses the measured results while section IV discusses the converter model.

Modeling of turn-OFF Transient Energy in IGBT Controlled Silicon PiN Diodes

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Keywords

<<PiN Diode>>, <<Reverse Recovery>>, <<Switching Energy>>, <<Modeling>>.

Abstract

Silicon PiN diodes are the most widely used rectifying technology in industry especially in voltage source converters. The PiN diodes are usually used as anti-parallel diodes across silicon IGBTs where they conduct current in the reverse direction as the current commutates between the phases of the converter. They tend to generate a considerable amount of energy losses during the turn-OFF transient due to the reverse recovery characteristics. The rate at which the diode is switched will determine the switching energy and will affect EMI, electrothermal stresses and reliability. Hence, it is vital to be able to predict the switching energy of the diode during its turn-OFF transient given the switching conditions so as to have a realistic approach towards predicting the operating temperature. The switching energy of PiN diodes is determined by the peak reverse recovery current, the peak diode voltage overshoot, the time displacement between them as well as the temperature dependency of these peaks. In this paper, a model is presented and validated over a temperature range of –75 °C to 175 °C and with switching speeds (*dI/dt*) modulated by the gate resistance on the low side IGBT ranging from 10 Ω to 1000 Ω. Comparisons show consistency between model prediction and measurements result. The model is a novel method of accurately predicting the switching energy of PiN diodes at different switching rates and temperatures using the measurements of a single switching rate at different temperatures.

Nomenclature

peak reverse recovery current at 25 °C	$I_{RR}{}^{(25\ °C)}$	(A)
Forward Current	I_F	(A)
Diode Voltage 25 °C	$V_{AK}{}^{(25\ °C)}$	(V)
Diode Current	i_D	(A)
Diode on-state Voltage Drop	V_D	(V)
turn-OFF Switching Rate	dI_{TF}/dt	(A/ μ s)
Recovery switching Rate	dI_{RR}/dt	(A/ μ s)
Voltage Recovery Rate	dV/dt	(V/ μ s)
Switching Energy of the Diode	E_{SW}	(mJ)
Circuit Parasitic Inductance	L	(H)

Introduction

PiN diodes are the most widely used rectifying devices in power converters in industry [1]. They deliver low conduction losses because of conductivity modulation from minority carrier injection however they tend to have significant switching energy losses due to reverse recovery [2, 3]. The extraction of minority carriers in the voltage blocking drift layer during turn-OFF results in a large reverse current with a peak current and time duration that depends on the rate at which the PiN diode is switched off. These switching energy losses are considerable due to the overlap between the peak reverse recovery current and the peak

Electrothermal Modeling and Characterization of SiC Schottky and Silicon PiN diodes Switching Transients

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***Abstract*— Schottky diodes are known to have lower conduction and switching losses compared to PiN diodes, however, are prone to ringing in the output characteristics. In this paper, analytical models have been developed to calculate the turn-off switching energy of SiC Schottky and silicon PiN diodes. The models account for the reverse recovery current and diode voltage overshoot in the case of the PiN diode as well as the output oscillations for the Schottky diodes. PiN diodes during turn-off exhibit significant reverse current which increases with the switching rate and temperature whereas Schottky diodes exhibit output oscillations due to RLC resonance in the circuit. By combining these models with thermal networks derived from transient thermal impedance curves of the diodes, a fast and accurate method of predicting the temperature transient for different switching frequencies and electrical time constants has been developed. These models can be used by application engineers to predict the energy dissipation when designing converters and can take account of temperature and switching rate dependencies of the diodes.**

Index Terms— Modeling, Switching Energy, Silicon Carbide, Power Devices

NOMENCLUTURE

V_D	On-state voltage drop
dI_{RR+}/dt	Slope of current before peak reverse recovery
dI_{RR-}/dt	Slope of current after peak reverse recovery
I_{RR}	peak reverse recovery
Δt	Time difference between voltage rise and I_{RR}
C_{AK}	depletion capacitance
R_{AK}	depletion resistance
L_{stray}	stray inductance parasitic
R_S	series resistance
E_{SW}	Switching energy
T	Temperature
t	Time

I. INTRODUCTION

Silicon PiN and SiC Schottky diodes are routinely used as free-wheeling diodes in voltage source converters that require bi-directional power flow [1-2]. Each technology exhibits certain characteristics in the turn-off transient. The silicon PiN diode suffers from high reverse recovery charge due to the fact that it is a bipolar device that relies on conductivity modulation via charge storage in the drift region [3-5]. Hence, when the diode is turned off, the stored charge must first be extracted via a negative current and after the diode starts blocking, the excess charge must recombine in the diode. Fig. 1(a) shows the measured switching voltage and current waveforms for a 1.2 kV PiN diode whereas 1(b) shows the switching power transient. Parasitic inductance and high *dI/dt* will contribute to higher peak diode voltage overshoot, which coupled with the peak reverse recovery current, causes high instantaneous power dissipation in the diode [6].

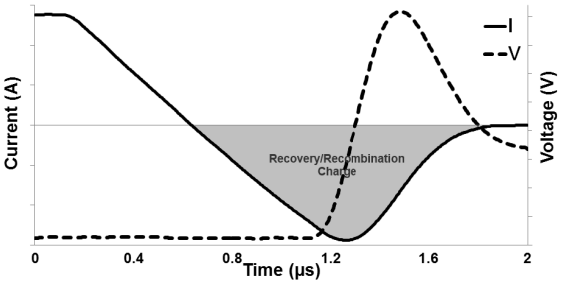

Fig. 1(a). Measured silicon PiN diode transient voltage and current

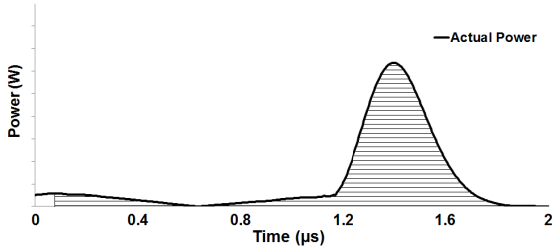

Fig. 1(b). Measured silicon PiN diode instantaneous power

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Temperature and dI_{DS}/dt Dependence of the Switching Energy of SiC Schottky Diodes in Clamped Inductive Switching Applications

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Keywords: Silicon Carbide, Schottky Barrier Diodes, Clamped Inductive Switching, Temperature Dependence, Switching Energy

Abstract. This paper presents the temperature and switching rate dependence of 1.2 kV/30 A SiC Schottky diode energy losses in clamped inductive switching circuits with 1.2 kV/30 A SiC MOSFETs as the switching transistors. The devices are tested under an ambient temperature range that spans from -75^{0}C to 175^{0}C and with switching rates that span from 10 to 100 A/µs. Due to the abruptness of the diode turn-OFF, low series resistance and the lack of reverse recovery, SiC SBDs are known to exhibit ringing or electromagnetic oscillations in the presence of parasitic inductances and high switching rates [1]. The impact of these electromagnetic oscillations on the switching energy, the dependence of the switching energy on temperature and the switching rate (dI_{DS}/dt) is the purpose of this paper's investigation.

Introduction

Silicon carbide (SiC) Schottky diodes have become a mainstream technology that is fast replacing silicon PiN diodes as rectifiers in power electronic applications. They can be used in power factor correction circuits, high voltage DC-DC converters and as reverse conducting anti-parallel diodes in voltage sourced converters that require bi-directional power flow. The voltage and current ratings exhibited by these diodes are increasing as a result of advancements in the fabrication technology of SiC, with CREE and ROHM as the main industrial manufacturers. Unlike PiN diodes, SiC Schottky diodes do not exhibit high reverse recovery charge which has been a main contributor to switching losses at higher frequencies. Schottky diodes are unipolar devices based on the drift of majority carriers whereas PiN diodes are bipolar devices based on the diffusion of minority carriers. Hence, Schottky diodes are not affected by minority carrier charge storage in the drift layers or by recombination currents that contribute to reverse recovery charges [2].

Schottky diodes can thus be used in applications where fast switching is advantageous for reducing the size and volume of the passive components required for filtering since they are not limited by the reverse charges associated with PiN diodes. Furthermore, the wide bandgap, high thermal conductivity and high critical field makes SiC Schottky diodes significantly more efficient rectifiers in high temperature applications. The wide bandgap and high critical field of SiC ensures that thinner and less resistive epitaxial layers can block higher voltages thereby improving the conduction loss performance of the devices compared with PiN diodes [3]. The combination of Schottky diodes with fast switching transistors can cause some problems related to electromagnetic oscillations. SiC diodes are prone to ringing under fast switching conditions as a result of RLC resonance between depletion capacitances, parasitic resistances and stray inductances. This ringing phenomenon has been shown to cause additional switching losses, hence, in applications with high switching frequencies, the temperature dependence of the ringing losses must be examined. In this paper, the ringing phenomenon in 1.2 kV SiC Schottky diodes is examined as a function of temperature and switching rates.

Clamped Inductive Switching Experiments

The switching performances of the SiC diodes are examined using the clamped inductive switching circuit that emulates current commutation between a high side diode and a low side transistor. The switching rate of the transistor/diode pair is modulated by the gate resistance used

Comparative Analysis of False Turn-ON in Silicon Bipolar and SiC Unipolar Power Devices

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***Abstract*— The temperature and *dV/dt* dependence of false turn-ON has been analyzed for Silicon Carbide (SiC) Unipolar and Silicon Bipolar transistors, with switching rates varied by the gate resistances while temperature is varied by a hot plate connected to power modules. Self-heating is also investigated by measuring the temperature rise of the modules at high switching frequencies (8 kHz). This has resulted in continuous false turn-on occurrence in the device which has increased the device junction temperature significantly due to the repetitive shoot-through energy. Temperature rises of up to 150°C within just a few minutes have been observed as a result of repetitive shoot-through currents at high frequencies. To understand the impact of different mitigation techniques, the temperature rise is also observed after applying the corrections. It is seen that using the correction methods in the devices reduces the temperature rise significantly and therefore is vital for the applications of both Silicon and SiC devices.**

Keywords*— *Silicon Carbide, MOSFETs, False turn-ON, Half Bridge, Temperature

I. INTRODUCTION

Half bridge topologies are the simplest, though the most popular topology of semiconductor devices in converter applications. The power devices in this topology often switch in turn, with respect to certain defined dead-times. In the past couple of years, silicon IGBT devices have been the most popular choice of semiconductor devices in these converters for medium voltage applications. However the recent development of SiC devices have also opened up new avenues in converter applications where high switching speeds are required. However, high switching speeds have certain disadvantages which should be investigated. An example could be the repetitive occurrence of false turn-on in power devices, which can lead to excessive temperature rises, thermal runaway and eventually destruction of the device. In a half bridge topology, when the high side device turns on, the DC link voltage drops on the low side device, imposing a significant *dV/dt* which in turn coupled with the miller capacitance and gate resistance of the low side device, will induce a voltage to the gate of the low device [1]. This voltage drop is rapid and its speed depends on many factors, most importantly the gate resistance connected to the gate of the high side device. The induced voltage on the low side device can exceed the threshold voltage of the devices, especially in case of SiC MOSFETs, resulting in a partial turn-on. This causes a semi-short-circuit condition thereby allowing a shoot-through current to flow through the devices [2]. This can have a significant reliability impact [3]. To investigate this problem, measurements have been done to understand how the false turn-on occurs in different operating conditions and how mitigation techniques can reduce its impact. Additionally, the self-heating problem has been investigated to understand how false turn-on contributes to temperature stresses and how the mitigation technique can reduce the self-heating. In this paper, two similarly-rated silicon and SiC power modules are used to perform the measurements with different switching rates and the shoot-through energy is analyzed as a function of temperature. Using a thermal camera, the temperature rise of the modules is also studied before and after the correction methods are applied.

II. THE MEASUREMENTS SET-UP

Fig. 1 shows the schematic of the measurement test rig where the half bridge topology and possible correction methods are shown and Fig.2 shows the experimental set up where the silicon bipolar (DM2G100SH12AE) and SiC unipolar (CAS100H12AM1) modules are tested with a range of external R_G connected on the gate drivers on both modules. An electric hot-plate is connected to the heat sink of the modules and is used to vary the junction temperature of the device under test. As seen in Fig.1, both the high side and low side devices are connected to a gate resistance. The gate resistances in these measurements are varied between 10 to 100 Ω. This is done for two purposes as follows.

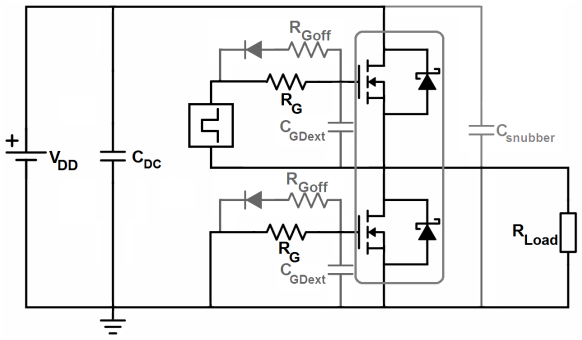

Fig. 1. The schematic of the test rig set-up.

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Investigation of Parasitic Turn-ON in Silicon IGBT and Silicon Carbide MOSFET Devices: A Technology Evaluation

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Acknowledgements

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Keywords

« Device application », « Device characterization », « Silicon Carbide (SiC) », « High temperature electronic »

Abstract

This paper investigates the switching rate and temperature dependence of parasitic (false) turn-on of power transistors when switched in power converters implemented in silicon IGBTs and Silicon Carbide (SiC) MOSFETs. It is shown that although high switching rates are normally desirable for minimizing the switching losses, this can result in shoot-through arm currents due to the combination of a Miller capacitance and high *dV/dt*. The power losses arising from this can be significantly larger than the normal switching losses since the device will still be blocking a considerable voltage. Even though SiC MOSFETs have a significantly smaller Miller capacitance compared with silicon IGBTs, this problem is no less of an issue due to higher switching speeds and lower threshold voltages. Additionally it is seen that the overshoot current increases with temperatures due to the negative temperature coefficient of the threshold voltage in both device technologies. Various solutions to overcome this have been analyzed for both device technologies. It is seen that the effectiveness of the mitigation techniques differs, and in general due to the lower threshold voltage of the SiC device, the solutions proposed are less effective.

I. Introduction

In 3-phase power inverters or synchronous DC converters, power devices are employed in half bridge legs. Ideally it is expected that each device switches individually without affecting the other device in the same phase, however in reality there is some electrical interference between the devices [1,2]. During the turn-on transient of the high-side device in power module leg, the DC link voltage drops on the lower device with a rate corresponding to the *dV/dt* of the top device. This *dV/dt* causes a current to flow through the Miller capacitance of the low-side device [3]. The current will flow through the internal and external gate resistances of the device and will induce a voltage on the gate of the low device [4]. If this induced voltage is higher than the threshold voltage of the low device, the low side device is unintentionally switched on thereby resulting in a short-circuit of the DC link [5]. The implication is that both devices are in the on-state while a significant voltage is applied on the DC link of the module, resulting in a significant shoot-through current. The level of this current depends on different factors such as the threshold voltage of the device, the parasitic induced voltage, the ambient temperature and performance of the device with low gate voltages. The induced voltage also depends

Appendix

B PWM Block Diagrams

Different pulse width modulation techniques were used in section 3.4.2 of chapter 3 to evaluate the performance of silicon and SiC power devices in an electric vehicle drive-train application. These PWM techniques, which are common in converter applications, are produced using block diagrams in PLECS software [148] as in Figure B.1. For the references of the reader, their block diagrams are provided here, as follows, respectively:

- Sinusoidal PWM - SPWM [33] in Fig. B.2
- Saw-tooth PWM [34] in Fig. B.3
- Carrier-Based Space Vector PWM - CB-SVPWM [35] in Fig. B.4
- Third Harmonic Injection PWM - 25% of main carrier - THIPWM(4) [37] in Fig. B.5
- Third Harmonic Injection PWM - 16% of main carrier - THIPWM(6) [38] in Fig. B.6
- Triple Harmonic Injection PWM - TRIPWM [39] in Fig. B.7

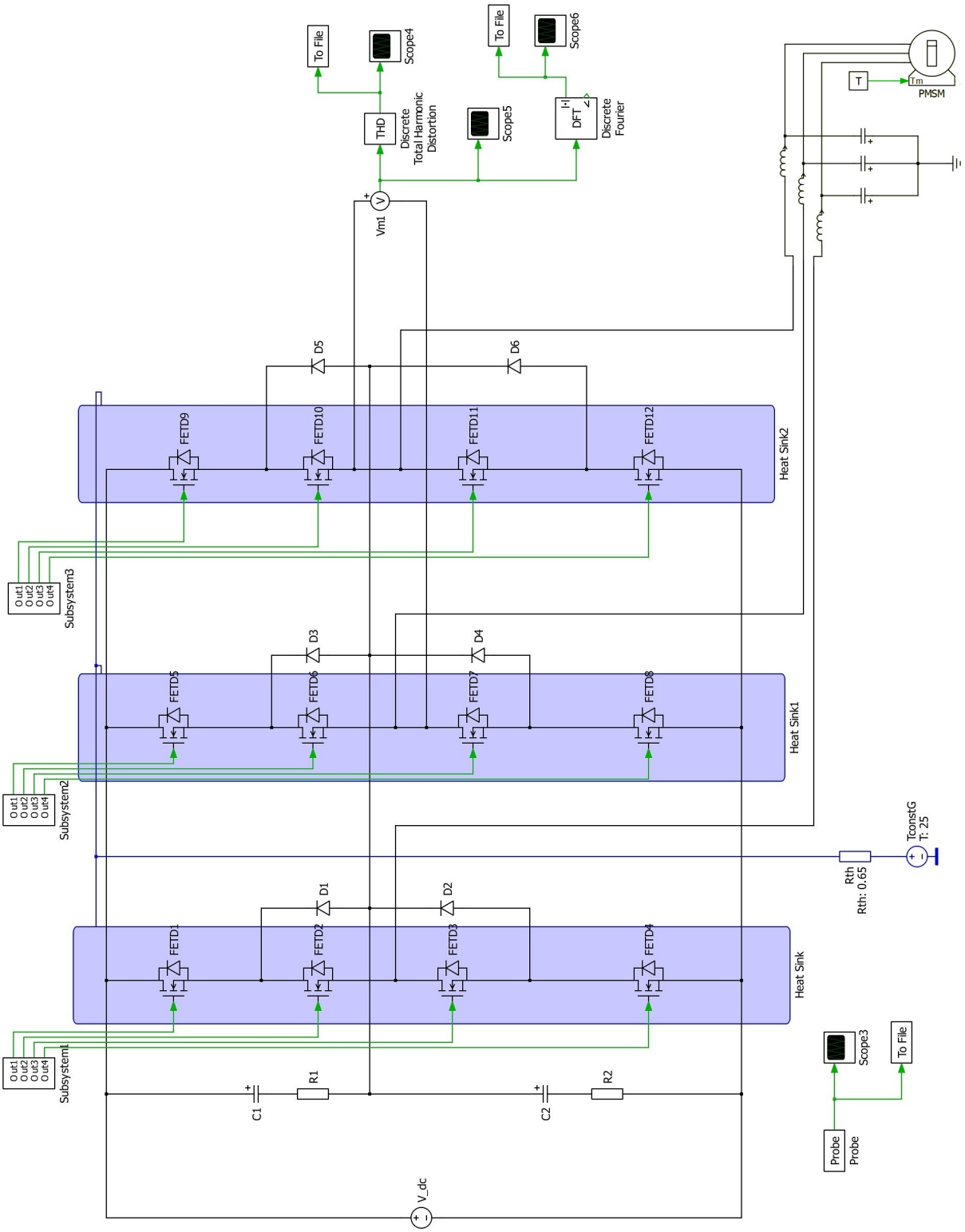


Figure B.1: The schematic of the NPC VSC converter, where the results of the switching energy of devices are used as an input.

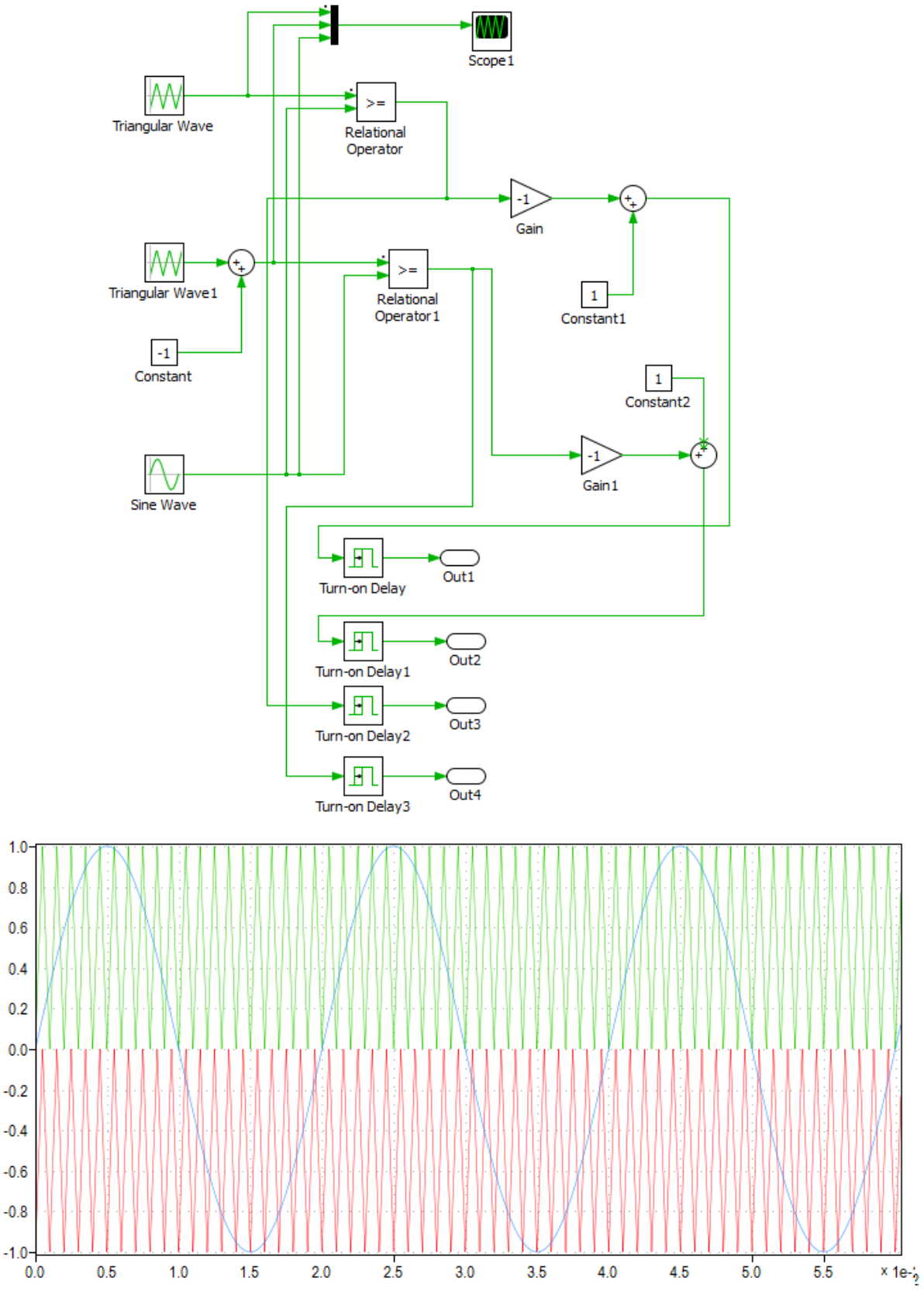


Figure B.2: The block diagram of the sinusoidal PWM technique.

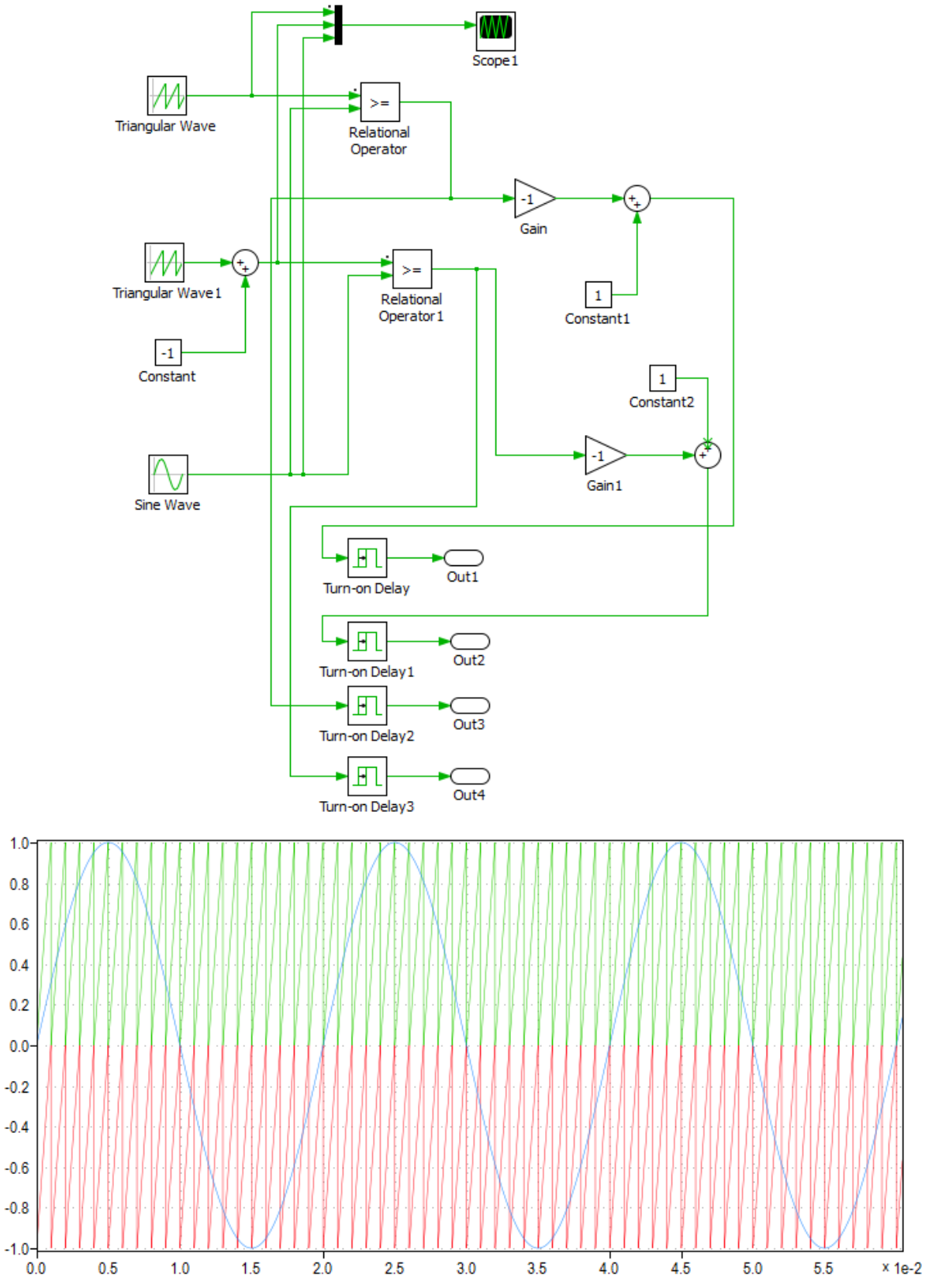


Figure B.3: The block diagram of the sawtooth PWM technique.

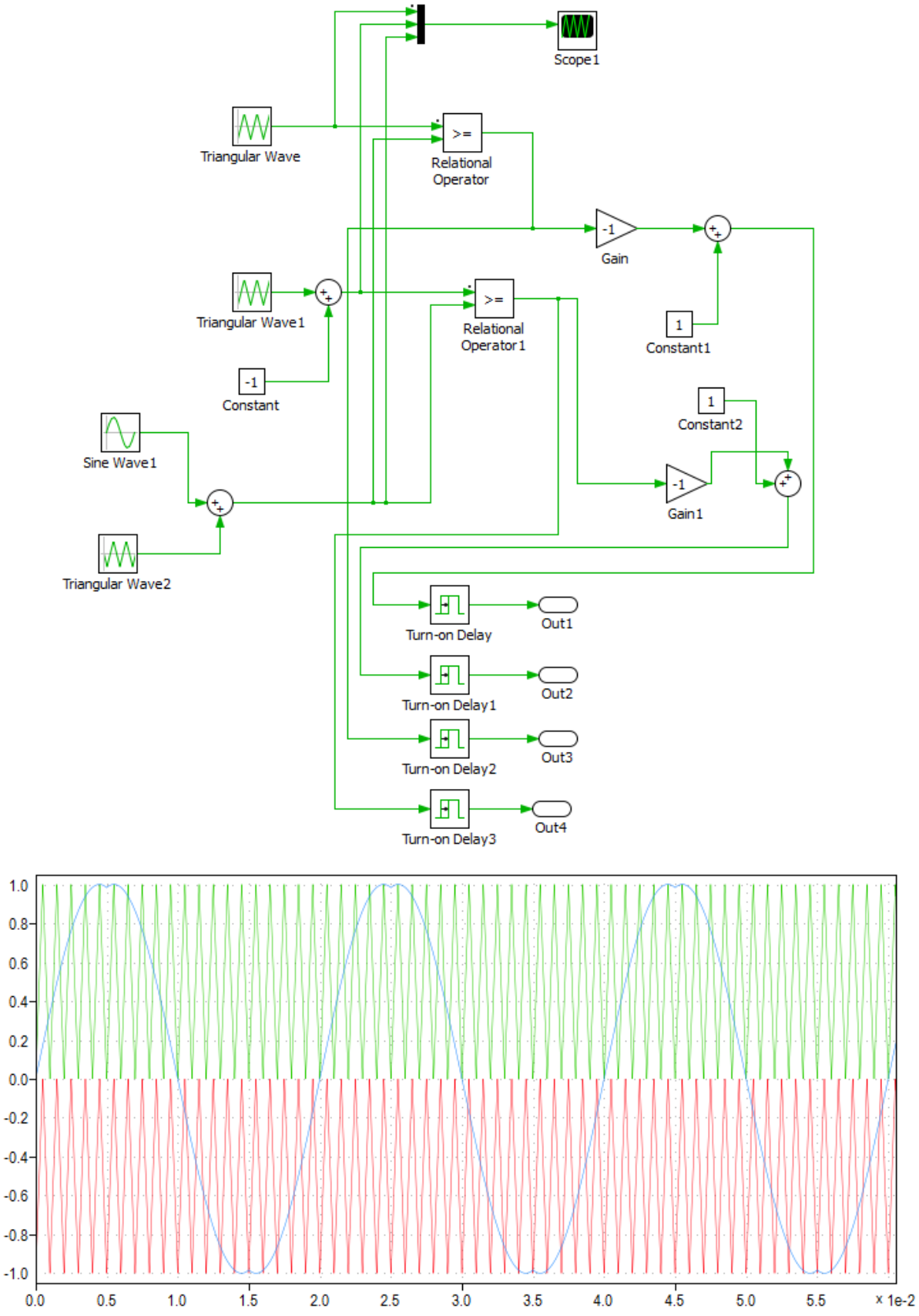


Figure B.4: The block diagram of the carrier-based space vector PWM technique.

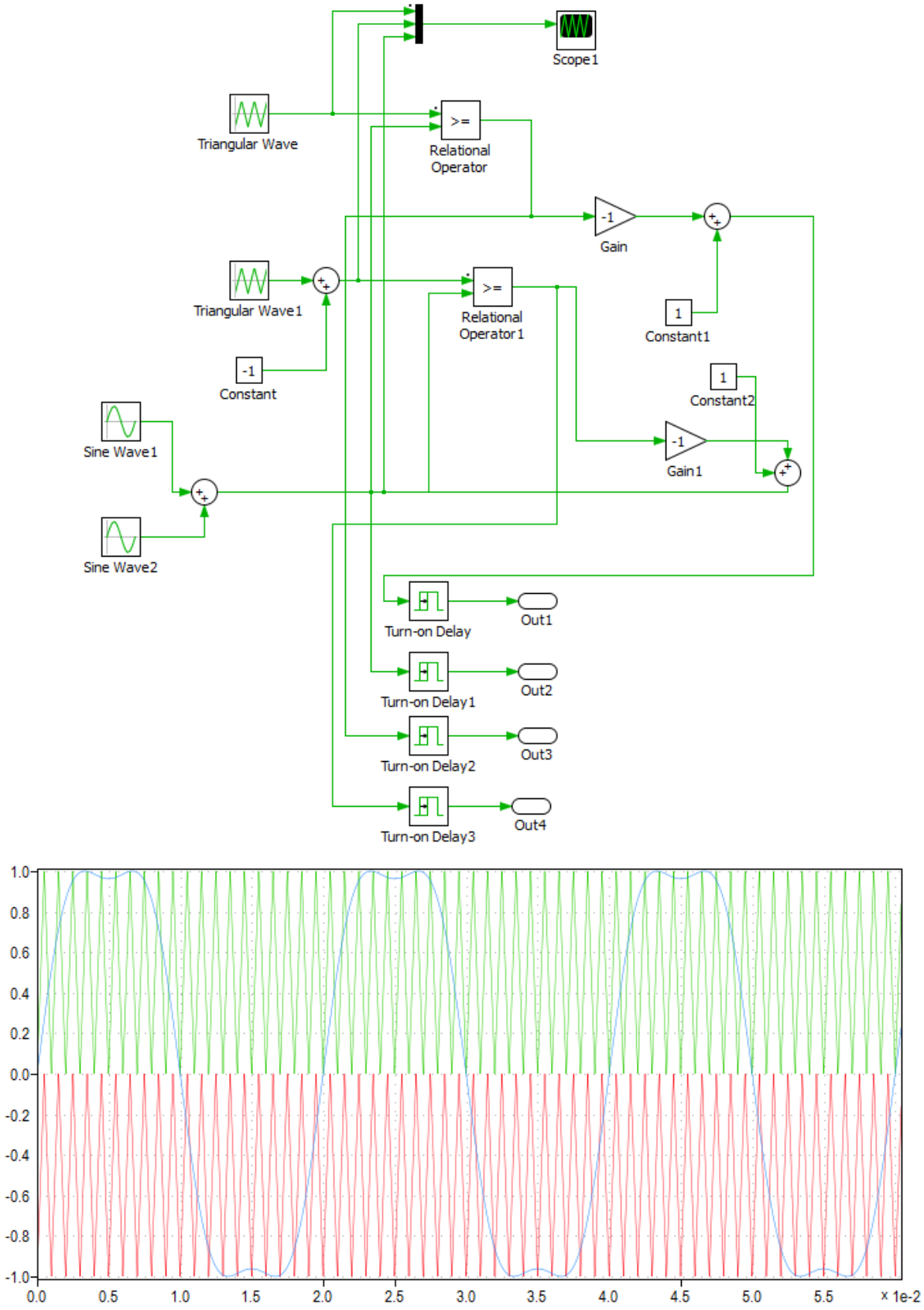


Figure B.5: The block diagram of the third harmonic injection PWM technique (with third harmonic having a relative value of 16% of the main carrier).

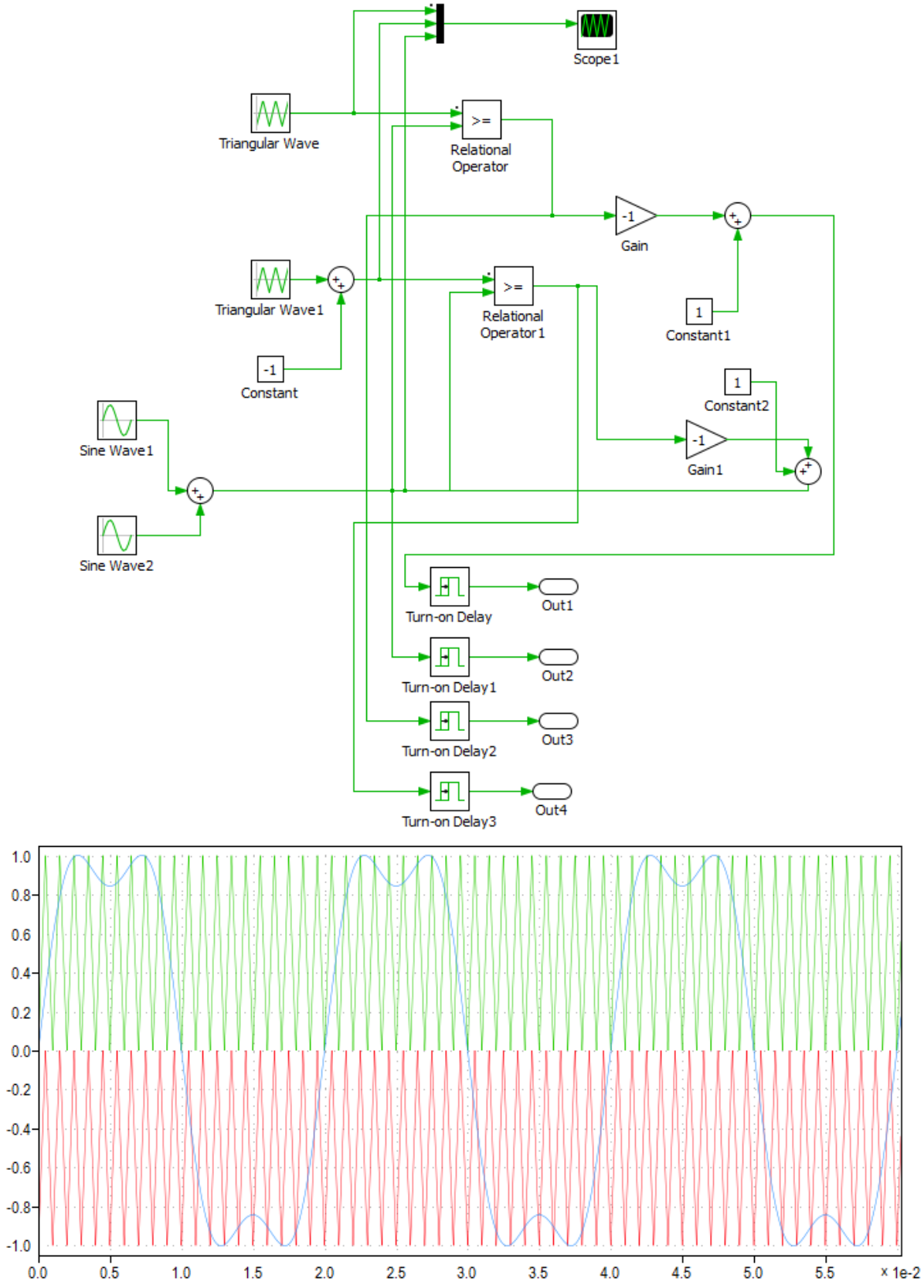


Figure B.6: The block diagram of the third harmonic injection PWM technique (with third harmonic having a relative value of 25% of the main carrier)

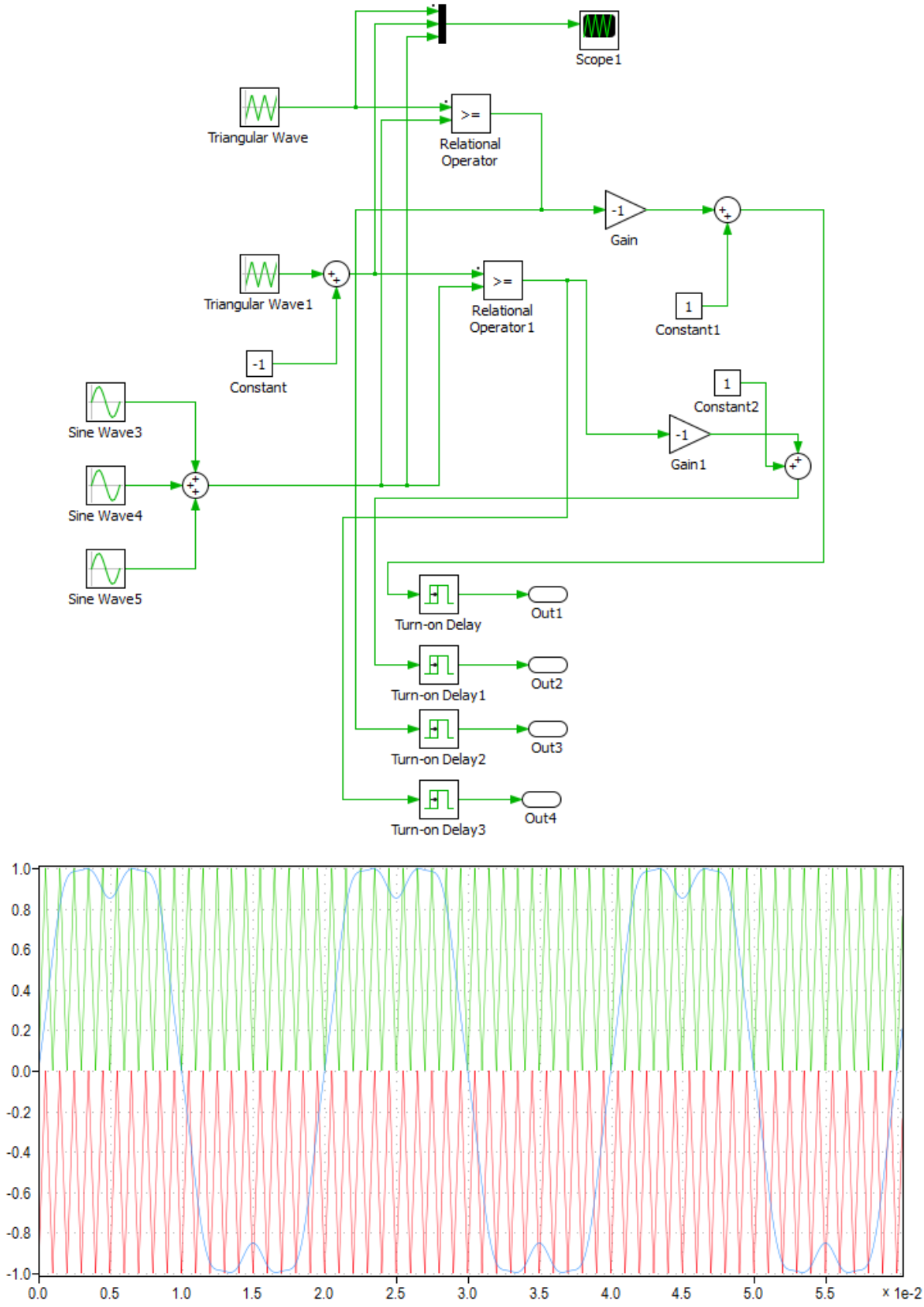


Figure B.7: The block diagram of the triple harmonic injection PWM technique

Appendix

C MATLAB Code for Si-PiN Diode Switching Energy Integrations

This MATLAB code validates equations of PiN diode switching energy as was explained in equations 4.4 to 4.16 of chapter 4:

```
Syms V ; Syms Vmax ; Syms Vd ; Syms t1 ; Syms dIdt1 ;
Syms dIdt2 ; Syms dIdt1p ; Syms dIdt1n ; Syms dIdt2p ; Syms dIdt2n ;
Syms dVdt; Syms dVdt1; Syms dVdt2 ; Syms Irr ; Syms If;
L = (Vmax-V)/(dIdt1);

fprintf(2,'\n')
fprintf(2,'The integrations of two lines is as:\n')
fprintf(2,'\n')
Syms a; Syms b; Syms c; Syms d; Syms t; Syms y1; Syms y2;
y1 = a*t+b;
y2 = c*t+d;
fprintf(2,'\n')
fprintf(2,'where it results in :\n')
fprintf(2,'\n')
```

```
int(y1*y2,t)
L=(Vmax-V)/(dIdt1);

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 1 is:\n')
fprintf(2,'\n')
% Area 1 in Figure 4.7
Area1=(If*Vd*0.5)*(If/dIdt1);
pretty(simplify(Area1))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 2 is:\n')
fprintf(2,'\n')
% Area 2 in Figure 4.7
Area2=(Vd*0.5)*(Irr-(t1*dIdt1))*((Irr/dIdt1)-t1);
pretty(simplify(Area2))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 3 is:\n')
fprintf(2,'\n')
% a & c : Line Slopes , b & d: Line Constant (a&b of Line 1 , c&d of ...
    Line 3 , Area 3 in Figure 4.7)
a3= -dIdt1;
b3= If;
c3= dVdt1;
d3= V+(L*dIdt1)-(dVdt1*(((V+(L*dIdt1)-Vd)/dVdt1)+(((If+Irr)/dIdt1)-t1)))
X31= ((Irr+If)/dIdt1)-t1;
X32= (Irr+If)/dIdt1;
Area3 = (((a3*c3)/3)*(((X32)^3)-((X31)^3)))
      + ((((a3*d3)/2)+((b3*c3)/2))*(((X32)^2)-((X31)^2)))
```

```
      + (b3*d3*((X32)-(X31)));
pretty(simplify(Area3))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 4 is:\n')
fprintf(2,'\n')
% a & c : Line Slope , b & d: Line Constant (a&b of Line 2 , c&d of ...
    Line 3 , Area 4 in Figure 4.7)
a4= dIdt2;
b4= (-dIdt2)*(((If+Irr)/dIdt1)+((Irr)/dIdt2));
c4= dVdt1;
d4= V+(L*dIdt1)
   -(dVdt1*(((V+(L*dIdt1)-Vd)/dVdt1)+(((If+Irr)/dIdt1)-t1)));
X41= (Irr+If)/dIdt1;
X42= ((Irr+If)/dIdt1)-t1+((V+(L*dIdt1)-Vd)/dVdt1);
Area4 = (((a4*c4)/3)*(((X42)^3)-((X41)^3)))
      + ((((a4*d4)/2)+((b4*c4)/2))*(((X42)^2)-((X41)^2)))
      + (b4*d4*((X42)-(X41)));
pretty(simplify(Area4))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 5 is:\n')
fprintf(2,'\n')
% a & c : Line Slope , b & d: Line Constant (a&b of Line 2 , c&d of ...
    Line 4 , Area 5 in Figure 4.7)
a5= dIdt2;
b5= (-dIdt2)*(((If+Irr)/dIdt1)+((Irr)/dIdt2));
c5= dVdt2;
d5= (V+(L*dIdt1))
   -(dVdt1*(((If+Irr)/dIdt1)+((V+(L*dIdt1)-Vd)/dVdt1)-t1));
```

```
X51= ((If+Irr)/dIdt1)-t1+((V+(L*dIdt1)-Vd)/dVdt1);
X52= ((If+Irr)/dIdt1)+(Irr/(dIdt2));
Area5 = (((a5*c5)/3)*(((X52)^3)-((X51)^3)))
      + ((((a5*d5)/2)+((b5*c5)/2))*(((X52)^2)-((X51)^2)))
      + (b5*d5*((X52)-(X51)));
pretty(simplify(Area5))

% Total Switching Energy:

fprintf(2,'\n')
fprintf(2,'Total Switching Energy is:\n')
fprintf(2,'\n')

%ESw= Area1 + Area2 + Area3 + Area4 + Area5
TotalAreamJ=(abs(Area1)+abs(Area2)+abs(Area3)+abs(Area4)+abs(Area5))*1000


fprintf(2,'\n')
fprintf(2,'Now, the integrations of the complete method is shown as ...
    in:\n')
fprintf(2,'\n')

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 1 is:\n')
fprintf(2,'\n')
% Area 1 in Figure 4.8
Area1=(If*Vd*0.5)*(If/dIdt1p);
pretty(simplify(Area1))

fprintf(2,'\n')
```

```
fprintf(2,'General Integral of the Area 2 is:\n')
fprintf(2,'\n')
% Area 2 in Figure 4.8
Area2=(Vd*0.5)*(Irr-(t1*dIdt1n))*((Irr/dIdt1n)-t1);
pretty(simplify(Area2))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 3 is:\n')
fprintf(2,'\n')
% a & c : Line Slopes , b & d: Line Constant (a&b of Line 2 , c&d of ...
    Line 5 , Area 3 in Figure 4.8)
a3= -dIdt1n;
b3= (dIdt1n*((If/dIdt1p)+(Irr/dIdt1n)))-Irr;
c3= dVdt1;
d3= Vd-(dVdt1*((If/dIdt1p)+(Irr/dIdt1n)-t1));
X31= ((Irr/dIdt1n)+(If/dIdt1p))-t1;
X32= (Irr/dIdt1n)+(If/dIdt1p);
Area3 = (((a3*c3)/3)*(((X32)^3)-((X31)^3)))
      + ((((a3*d3)/2)+((b3*c3)/2))*(((X32)^2)-((X31)^2)))
      + (b3*d3*((X32)-(X31)));
pretty(simplify(Area3))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 4 is:\n')
fprintf(2,'\n')
% a & c : Line Slopes , b & d: Line Constant (a&b of Line 3 , c&d of ...
    Line 5 , Area 4 in Figure 4.8)
a4= dVdt1;
b4= Vd-(dVdt1*((If/dIdt1p)+(Irr/dIdt1n)-t1));
c4= dIdt2p;
```

```
d4= -(dIdt2p*((If/dIdt1p)+(Irr/dIdt1n)))-Irr;
X41= (Irr/dIdt1n)+(If/dIdt1p);
X42= ((Irr/dIdt1n)+(If/dIdt1p))-t1+((V+(L*dIdt2p)-Vd)/dVdt1);
Area4 = (((a4*c4)/3)*(((X42)^3)-((X41)^3)))
      + ((((a4*d4)/2)+((b4*c4)/2))*(((X42)^2)-((X41)^2)))
      + (b4*d4*((X42)-(X41)));
pretty(simplify(Area4))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 5 is:\n')
fprintf(2,'\n')
% a & c : Line Slopes , b & d: Line Constant (a&b of Line 3 , c&d of ...
    Line 6 , Area 5 in Figure 4.8)
a5= dIdt2p;
b5= (-dIdt2p*((If/dIdt1p)+(Irr/dIdt1n)))-Irr;
c5= (-dVdt1)/2;
d5= (1.5*(V+(L*dIdt1n)))
   +(dVdt1*((If/dIdt1p)+(Irr/dIdt1n)-(Vd/dVdt1)-t1)/2);
X51= ((Irr/dIdt1n)+(If/dIdt1p))-t1+((V+L*dIdt2p-Vd)/dVdt1);
X52= ((Irr/dIdt1n)+(If/dIdt1p))
    +(((dIdt2n*((V+1.5*(L*dIdt2p)-Vd)/dVdt1)-t1))-Irr)/(dIdt2n-dIdt2p);
Area5 = (((a5*c5)/3)*(((X52)^3)-((X51)^3)))
      + ((((a5*d5)/2)+((b5*c5)/2))*(((X52)^2)-((X51)^2)))
      + (b5*d5*((X52)-(X51)));
pretty(simplify(Area5))

fprintf(2,'\n')
fprintf(2,'General Integral of the Area 6 is:\n')
fprintf(2,'\n')
% a & c : Line Slopes , b & d: Line Constant (a&b of Line 4 , c&d of ...
```

```
      Line 6 , Area 6 in Figure 4.8)
a6= (-dVdt1)/2;
b6= 1.5*(V+(L*dIdt1n))
   +(dVdt1*((If/dIdt1p)+(Irr/dIdt1n)-(Vd/dVdt1)-t1)/2);
c6= dIdt2n;
d6= -dIdt2n*(((V+(1.5*L*dIdt1n)-Vd)/dVdt1)+(If/dIdt1p)+(Irr/dIdt1n)-t1);
X61= ((Irr/dIdt1n)+(If/dIdt1p))
    +(((dIdt2n*((V+1.5*(L*dIdt2p)-Vd)/dVdt1)-t1))-Irr)/(dIdt2n-dIdt2p);
X62= ((Irr/dIdt1n)+(If/dIdt1p))-t1+((V+(1.5*L*dIdt2p)-Vd)/dVdt1);
Area6 = (((a6*c6)/3)*(((X62)^3)-((X61)^3)))
      + ((((a6*d6)/2)+((b6*c6)/2))*(((X62)^2)-((X61)^2)))
      + (b6*d6*((X62)-(X61)));
pretty(simplify(Area6))

% Total Switching Energy:
fprintf(2,'\n')
fprintf(2,'Total Switching Energy is:\n')
fprintf(2,'\n')

%ESw= Area1 + Area2 + Area3 + Area4 + Area5 + Area6
ESw=(abs(Area1)+abs(Area2)+abs(Area3)
                          +abs(Area4)+abs(Area5)+abs(Area6))*1000
pretty(simplify(ESw))
```

Appendix

D MATLAB Code for SiC SBD Switching Energy Integrations

This MATLAB code validates equations of SiC Schottky barrier diode switching energy as was explained in equations 4.42 to 4.47 of chapter 4:

```
1  syms a ; syms b ; syms c ; syms d ;
2  syms Vdd ;
3  syms Ipr ;
4  syms AI ;
5  syms AV ;
6  syms w ;
7  syms t ;
8  syms L ;
9  syms Ga ;
10 syms dIdsdt ;
11 syms dVakdt ;
12 syms Vakpk ;
13 syms If ;
14 syms Vd ;
```

```
15
16 %The Time Intervals are:
17 fprintf(2,'\n')
18 fprintf(2,'The Time Intervals are:\n')
19 fprintf(2,'\n')
20 t1 = 0
21 t2 = If/dIdsdt
22 t3 = (If/dIdsdt)+((Vakpk-Vd)/dVakdt)
23 t4 = (If/dIdsdt)+((Vakpk-Vd)/dVakdt)+Ga
24
25 %Switching Area 1 is calculated as:
26 fprintf(2,'\n')
27 fprintf(2,'Switching Area 1 is calculated as:\n')
28 fprintf(2,'\n')
29 Esw1 = int(Vd*(If-t*dIdsdt),t)
30 fprintf(2,'\n')
31 fprintf(2,'considering the time, it becomes:\n')
32 fprintf(2,'\n')
33 Esw1 = int(Vd*(If-t*dIdsdt),t,t1,t2)
34 pretty(simplify(Esw1))
35
36 %Switching Area 2 is calculated as:
37 fprintf(2,'\n')
38 fprintf(2,'Switching Area 2 is also calculated as:\n')
39 fprintf(2,'\n')
40 fprintf(2,'\n')
41 fprintf(2,'General Integral of the area 2 is:\n')
42 fprintf(2,'\n')
43 int((a-b*t)*(c*t-d),t)
44 pretty(ans)
```

```
fprintf(2,'\n')
fprintf(2,'Therefore\n')
fprintf(2,'\n')
Esw2 = 0.5*((t3)^2)*((a*c)+(b*d))-(a*d*(t3))-(b*c*((t3)^3)/3)
      -0.5*((t2)^2)*((a*c)+(b*d))-(a*d*(t2))-(b*c*((t2)^3)/3)
pretty(simplify(Esw2))
fprintf(2,'\n')
fprintf(2,'So if\n')
fprintf(2,'\n')
a = If
b = dIdsdt
c = dVakdt
d = (If*dVakdt/dIdsdt)-Vd
fprintf(2,'\n')
fprintf(2,'Then:\n')
fprintf(2,'\n')
Esw2 = 0.5*((t3)^2)*((a*c)+(b*d))-(a*d*(t3))-(b*c*((t3)^3)/3)
     -(0.5*((t2)^2)*((a*c)+(b*d))-(a*d*(t2))-(b*c*((t2)^3)/3))
pretty(simplify(Esw2))
fprintf(2,'\n')
fprintf(2,'This can also be drived using the following method:\n')
fprintf(2,'\n')
R1 = (((If/dIdsdt)+((Vakpk-Vd)/dVakdt))^2)*(If*dVakdt
   - (dIdsdt * (Vd-(If*(dVakdt)/dIdsdt))))/2
pretty(expand(R1))
R2 = -(((If/dIdsdt)^2)*((If*dVakdt)-(dIdsdt*(Vd-(If*dVakdt/dIdsdt)))))/2
pretty(expand(R2))
R3 = If*((If/dIdsdt)+((Vakpk-Vd)/dVakdt))*(Vd-((If*dVakdt)/dIdsdt))
pretty(expand(R3))
R4 = -If*(If/dIdsdt)*(Vd-(If*dVakdt/dIdsdt))
```

```
pretty(expand(R4))
R5 = -dIdsdt*dVakdt*(((If/dIdsdt)+((Vakpk-Vd)/dVakdt))^3)/3
pretty(expand(R5))
R6 = dIdsdt*dVakdt*((If/dIdsdt)^3)/3
pretty(expand(R6))
fprintf(2,'\n')
fprintf(2,'Adding R1 to R6 to each other results in:\n')
fprintf(2,'\n')
Esw2 = R1+R2+R3+R4+R5+R6
fprintf(2,'\n')
fprintf(2,'Or:\n')
fprintf(2,'\n')
pretty(simplify(Esw2))

%Switching Area 3 is calculated as:
fprintf(2,'\n')
fprintf(2,'Switching Area 3 is also calculated as:\n')
fprintf(2,'\n')
Esw3 = int((Vdd*Ipr*exp(-AI*t)*sin(w*t))
      +(0.5*L*Ipr*dIdsdt*exp(-(AI+AV)*t))
      +(0.5*L*Ipr*dIdsdt*exp(-(AI+AV)*t)*cos(2*w*t)),t)
pretty(simplify(Esw3))
fprintf(2,'\n')
fprintf(2,'Which results as:\n')
fprintf(2,'\n')
Esw3 = int((Vdd*Ipr*exp(-AI*t)*sin(w*t))
      +(0.5*L*Ipr*dIdsdt*exp(-(AI+AV)*t))
      +(0.5*L*Ipr*dIdsdt*exp(-(AI+AV)*t)*cos(2*w*t)),t,t3,t4)
pretty(simplify(Esw3))
```

Appendix

E Gate Driver Design Schematic

For the measurements of this thesis, especially in the case of chapter 6, two basic gate drivers are designed. First, a unipolar gate driver is designed as shown in Figure E.1 where an external power supply is providing the main 5 volts input to power up the circuit, while a built-in DC-DC power supply (RJZ-0524S-ND) scales this up to 24 volts. The output of this power supply is connected to a voltage regulator (LM317-ADJ) which by using external resistances will determine the output voltage level of the gate driver. In the case of these measurements, this level is set to 18 volts to drive the modules. In this regard, calculations of the R_1, R_4 and R_5 resistances are done according to the voltage regulator datasheet to obtain the required output voltage, are here set to 390 Ω, 15 kΩ and 8.2 kΩ, respectively. The output voltage is then connected to a gate-drive chip (HCNW-3120-000E) to provide the drive supply according to the input signal. This signal is applied to the circuit using the trigger input socket, which according to the gate-drive chip datasheet, is then supposed to be connected to a non-inverting open-collector buffer (SN74ALS1035N) before connection to the signal input part of the gate-drive chip. Also according to the datasheets of the components, several filter capacitors are placed

in the circuit to remove the possible noise. Finally the output voltage is connected to the headers which eventually will provide the 18 volts signal to the gate of the power devices through the interface PCB as will be shown in the Figure E.5.

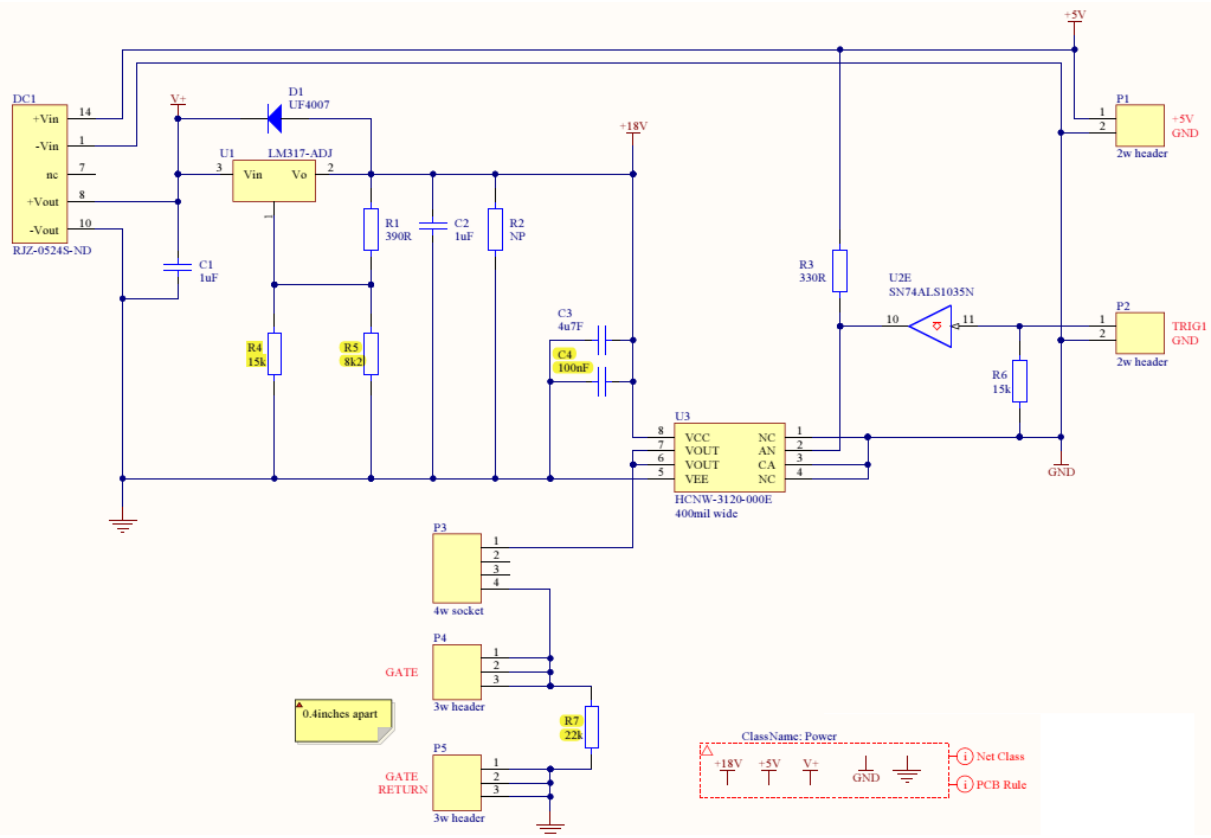


Figure E.1: The design schematic of the unipolar gate driver.

In some cases, as shown in chapter 6, it is not acceptable to have a unipolar gate driver as issues such as crosstalk remain. Hence, to remove the possible induced gate biases, it is necessary to use a bipolar gate driver with normal on-state voltage of a negative value. The design of such bipolar gate driver is shown in Figure E.2. The only difference with what was described for the unipolar gate driver above is the fact that the ground connection (which was the zero potential in the unipolar drive) is now biased to -5 volts

using an additional built-in DC-DC power supply (RP-0505S). This connection provides a constant negative value. Hence, in this case, the output voltage of the power supply is connected to the ground connection of gate-drive chip in reverse polarity to bias it.

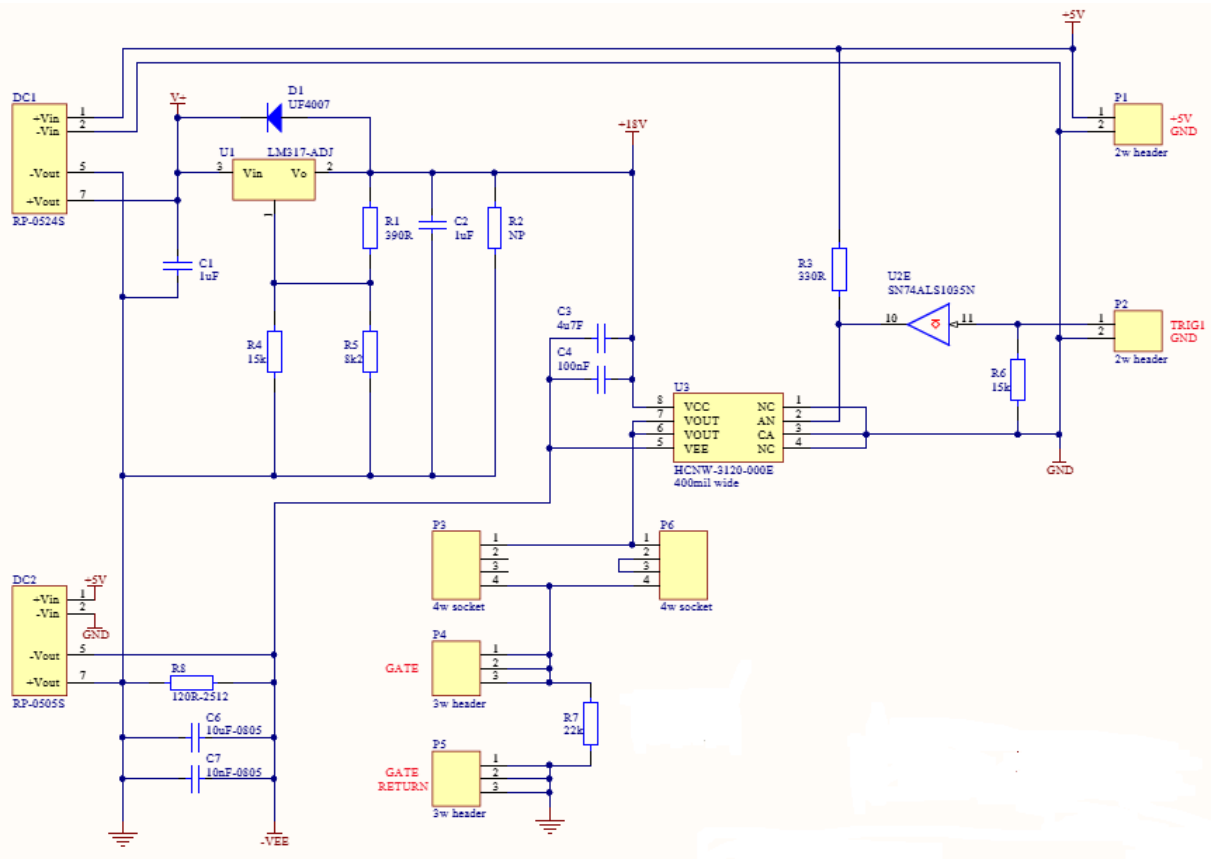


Figure E.2: The design schematic of the bipolar gate driver.

Figure E.3 is showing the PCB design of the above design schematics. These PCB designs are showing how does the components in each circuits placed on the PCB board. In the left side, the PCB of the unipolar gate driver is seen, where it is clear that there is an isolation gap between the two sides of the driver. This is to protect the control circuit from possible faults on the power circuit, and to avoid such faults being transferred back into the control equipments. Hence, it has been necessary for both the light-triggered

optocoupler gate-drive chip and the built-in DC-DC power supplies to be of isolated types to provide required level of protection. The isolation rating of these components depends on the model number, and in this case, according to their datasheet is at least 1100 volts, while the measurements are done using a 650 volts supply with a maximum voltage overshoot of 900 volts in the worst case scenario.

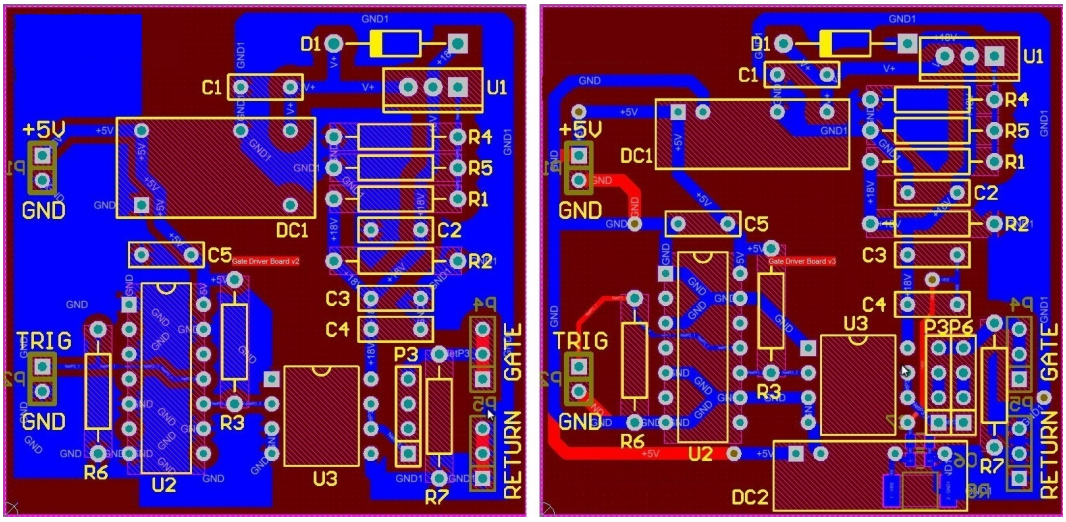


Figure E.3: The PCB design schematic of the gate drivers; Left: Unipolar driver, Right: Bipolar driver with extra gate resistance slots for two resistive paths.

The two resistive paths method, used in the chapter 6 can be applied as shown in Figure E.4. Here, the second resistor is in series with an external diode so that it is in circuit only during turn-on of high side device. To connect the assembled gate drivers to the modules, an intermediate board has been necessary to provide an interface between the gate drivers and the power module gate connections. This is shown in Figure E.5 where the mains connection of the external power supply as well as the trigger sockets are connected to the gate drivers using this intermediate board. The output connection is directly connected to the power module. The interface PCB board is identical for both unipolar and bipolar gate drivers.

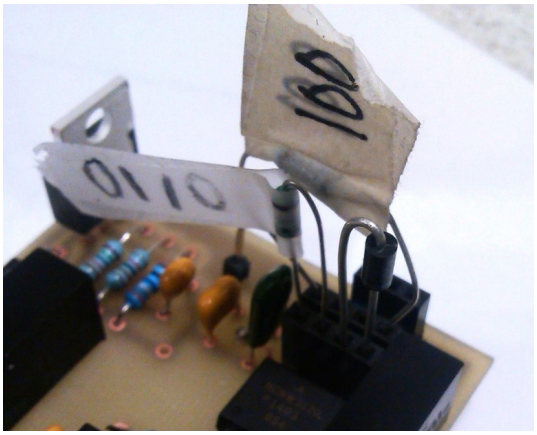


Figure E.4: The two resistive paths gate resistors and diode connected on the PCB.

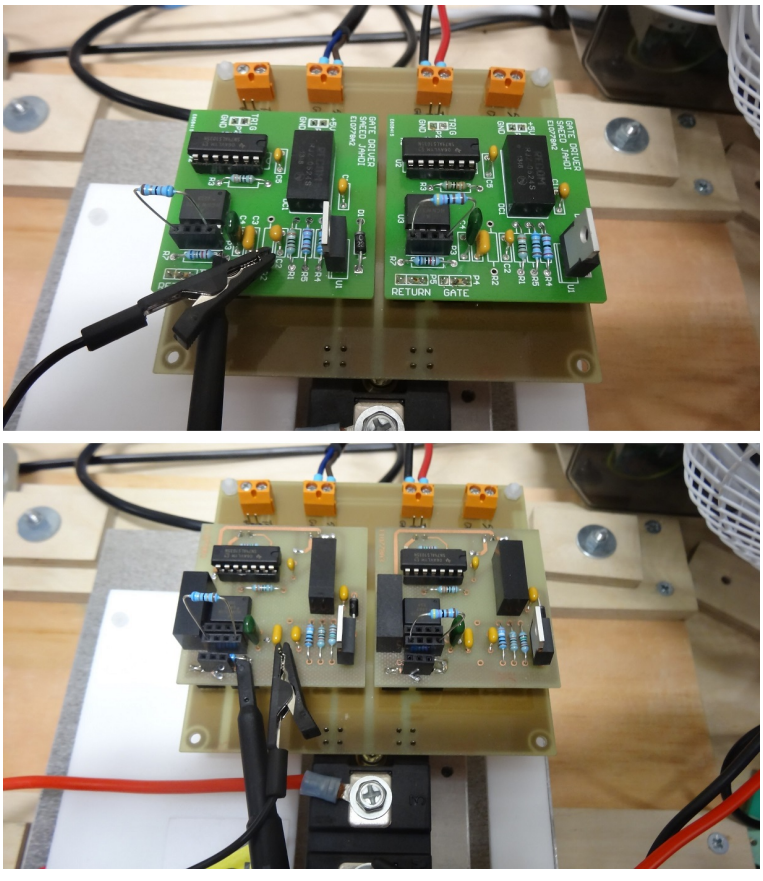


Figure E.5: The gate drivers assembled on a power module; Top: Unipolar gate driver, Bottom: Bipolar gate driver with extra gate resistance slots for two resistive paths.

Appendix

F Devices Datasheets

For the sake of future reference of the readers, the main characteristics of the devices used in the measurements of this thesis are presented here by means of providing the main page of the datasheets. The full version of these datasheets are available online.

SCH2080KE

N-channel SiC power MOSFET co-packaged with SiC-SBD Datasheet

V_{DSS}	1200V
$R_{DS(on)}$ (Typ.)	80mΩ
I_D	35A
P_D	179W

●**Outline**

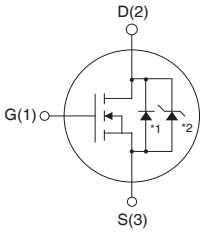
TO-247

(1) (2) (3)

●**Features**

1) Low on-resistance
2) Fast switching speed
3) Fast reverse recovery
4) Low V_{SD}
5) Easy to parallel
6) Simple to drive
7) Pb-free lead plating ; RoHS compliant

●**Inner circuit**



(1) Gate
(2) Drain
(3) Source

*1 Body Diode
*2 SBD

●**Application**

・Solar inverters
・DC/DC converters
・Induction heating
・Motor drives

●**Packaging specifications**

Type	Packing	Tube
	Reel size (mm)	-
	Tape width (mm)	-
	Basic ordering unit (pcs)	30
	Taping code	-
	Marking	SCH2080KE

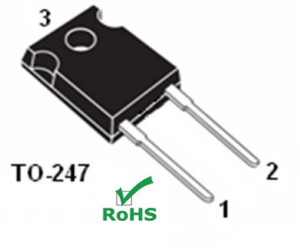
●**Absolute maximum ratings** (T_a = 25°C)

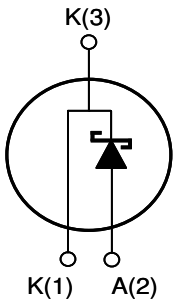
Parameter		Symbol	Value	Unit
Drain - Source voltage		V_{DSS}	1200	V
Continuous drain current	T_c = 25°C	I_D *1	35	A
	T_c = 100°C	I_D *1	22	A
Pulsed drain current		$I_{D,pulse}$ *2	80	A
Gate - Source voltage		V_{GSS}	−6 to 22	V
Power dissipation (T_c = 25°C)		P_D	179	W
Junction temperature		T_j	150	°C
Range of storage temperature		T_{stg}	−55 to +150	°C

Silicon Carbide Power Schottky Diode

Product Summary		
V_{DC}	1200	V
I_F	30	A
Q_c	130	nC

Features:
- Positive Temperature Coefficient for Ease of Paralleling
- Temperature Independent Switching Behavior
- 175 ℃ Maximum Operating Temperature
- Zero Reverse Recovery Current
- Zero Forward Recovery Voltage





Internal Schematic

Applications:
- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive

MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Repetitive Peak Reverse Voltage	V_{RRM}	T_j = 25 ℃	1200	V
DC Blocking Voltage	V_{DC}		1200	
Continuous Forward Current	I_F	T_C < 145 ℃	30	A
		T_C < 100 ℃	46	
Peak Repetitive Forward Current	I_{FRM}	T_C = 125 ℃, D = 0.1	120	
Non-Repititive Surge Forward Current	I_{FSM}	T_C = 25 ℃, t_P = 10 ms	110	
		T_C = 25 ℃, t_P = 10 us	700	
Power Dissipation	P_{TOT}	T_C = 25 ℃	313	W
Operating and Storage Temperature	T_j, T_{stg}		-55 to +175	℃

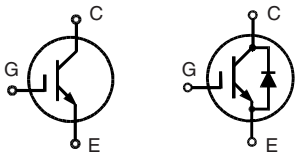
IXYS

High Voltage IGBT with optional Diode

IXDH 20N120
IXDH 20N120 D1

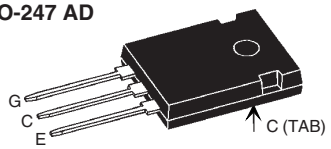
V_{CES} = 1200 V
I_{C25} = 38 A
$V_{CE(sat)\ typ}$ = 2.4 V

Short Circuit SOA Capability
Square RBSOA



IXDH 20N120 IXDH 20N120 D1

TO-247 AD



G = Gate, E = Emitter
C = Collector , TAB = Collector

Symbol	Conditions		Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C		1200	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 20 kΩ		1200	V
V_{GES}	Continuous		±20	V
V_{GEM}	Transient		±30	V
I_{C25}	T_C = 25°C		38	A
I_{C90}	T_C = 90°C		25	A
I_{CM}	T_C = 90°C, t_p = 1 ms		50	A
RBSOA	V_{GE} = ±15 V, T_J = 125°C, R_G = 82 Ω Clamped inductive load, L = 30 µH		I_{CM} = 35 V_{CEK} < V_{CES}	A
t_{SC} **(SCSOA)**	V_{GE} = ±15 V, V_{CE} = V_{CES}, T_J = 125°C R_G = 82 Ω, non repetitive		10	µs
P_C	T_C = 25°C	IGBT Diode	200 75	W W
T_J			-55 ... +150	°C
T_{stg}			-40< ... +150	°C
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s			300	°C
M_d	Mounting torque		0.8 - 1.2	Nm
Weight			6	g

Symbol	Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
$V_{(BR)CES}$	V_{GE} = 0 V		1200			V
$V_{GE(th)}$	I_C = 0.6 mA, V_{CE} = V_{GE}		4.5		6.5	V
I_{CES}	V_{CE} = V_{CES}	T_J = 25°C T_J = 125°C		 2	1	mA mA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				± 500	nA
$V_{CE(sat)}$	I_C = 20 A, V_{GE} = 15 V			2.4	3	V

Features

- NPT IGBT technology
- low saturation voltage
- low switching losses
- square RBSOA, no latch up
- high short circuit capability
- positive temperature coefficient for easy paralleling
- MOS input, voltage controlled
- optional ultra fast diode
- International standard package

Advantages

- Space savings
- High power density

Typical Applications

- AC motor speed control
- DC servo and robot drives
- DC choppers
- Uninteruptible power supplies (UPS)
- Switch-mode and resonant-mode power supplies

418

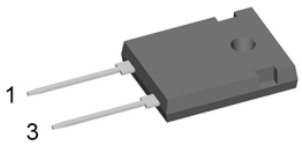
Standard Rectifier

V_{RRM}	=	1200V
I_{FAV}	=	45A
V_F	=	1.23V

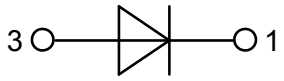
Single Diode

Part number

DSI45-12A



Backside: cathode



Features / Advantages:

- Planar passivated chips
- Very low leakage current
- Very low forward voltage drop
- Improved thermal behaviour

Applications:

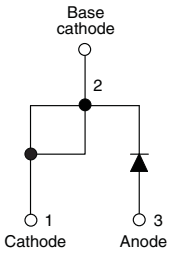
- Diode for main rectification
- For single and three phase bridge configurations

Package: TO-247

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

High Voltage, Input Rectifier Diode, 40 A

TO-247AC modified



FEATURES

- Very low forward voltage drop
- 150 °C max. operating junction temperature
- Designed and qualified according to JEDEC®-JESD47
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Input rectification
- Vishay Semiconductors switches and output rectifiers which are available in identical package outlines

DESCRIPTION

High voltage rectifiers optimized for very low forward voltage drop with moderate leakage.

These devices are intended for use in main rectification (single or three phase bridge).

PRODUCT SUMMARY	
Package	TO-247AC modified (2 pins)
$I_{F(AV)}$	40 A
V_R	800 V to 1200 V
V_F at I_F	1.1 V
I_{FSM}	475 A
T_J max.	150 °C
Diode variation	Single die

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Sinusoidal waveform	40	A
V_{RRM}	Range	800/1200	V
I_{FSM}		475	A
V_F	40 A, T_J = 25 °C	1.1	V
T_J		-40 to 150	°C

VOLTAGE RATINGS			
PART NUMBER	V_{RRM}, MAXIMUM PEAK REVERSE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM} AT 150 °C mA
VS-40EPS08PbF, VS-40EPS08-M3	800	900	1
VS-40EPS12PbF, VS-40EPS12-M3	1200	1300	

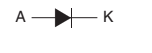
ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	T_C = 105 °C, 180° conduction half sine wave	40	A
Maximum peak one cycle non-repetitive surge current	I_{FSM}	10 ms sine pulse, rated V_{RRM} applied	400	
		10 ms sine pulse, no voltage reapplied	475	
Maximum I^2t for fusing	I^2t	10 ms sine pulse, rated V_{RRM} applied	800	A^2s
		10 ms sine pulse, no voltage reapplied	1131	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied	11 310	$A^2\sqrt{s}$

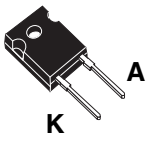
STTH3012

Ultrafast recovery - 1200 V diode

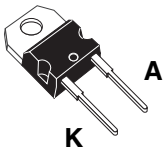
Main product characteristics

$I_{F(AV)}$	30 A
V_{RRM}	1200 V
T_j	175° C
V_F (typ)	1.30 V
t_{rr} (typ)	57 ns





DO-247
STTH3012W



TO-220AC
STTH3012D

Features and benefits

- Ultrafast, soft recovery
- Very low conduction and switching losses
- High frequency and/or high pulsed current operation
- High reverse voltage capability
- High junction temperature

Description

The high quality design of this diode has produced a device with low leakage current, regularly reproducible characteristics and intrinsic ruggedness. These characteristics make it ideal for heavy duty applications that demand long term reliability.

Such demanding applications include industrial power supplies, motor control, and similar mission-critical systems that require rectification and freewheeling. These diodes also fit into auxiliary functions such as snubber, bootstrap, and demagnetization applications.

The improved performance in low leakage current, and therefore thermal runaway guard band, is an immediate competitive advantage for this device.

Order codes

Part Number	Marking
STTH3012D	STTH3012D
STTH3012W	STTH3012W

C2M0160120D

Silicon Carbide Power MOSFET
Z-FET™ MOSFET

N-Channel Enhancement Mode

V_{DS}	1200 V
$I_{D(MAX)}$ @ 25°C	17.7 A
$R_{DS(on)}$	160 mΩ

Features

- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low $R_{DS(on)}$
- Easy to Parallel and Simple to Drive
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased System Switching Frequency

Applications

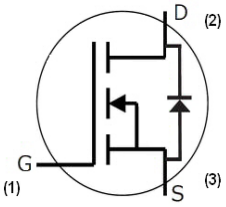
- Auxiliary Power Supplies
- Solar Inverters
- High Voltage DC/DC Converters
- High-frequency applications

Package

TO-247-3

Halogen-Free

RoHS COMPLIANT



Part Number	Package
C2M0160120D	TO-247-3

Maximum Ratings (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
$I_{DS\ (DC)}$	Continuous Drain Current	17.7	A	V_{GS}@20 V, T_C = 25°C	Fig. 19
		11		V_{GS}@20 V, T_C = 100°C	
$I_{DS\ (pulse)}$	Pulsed Drain Current	45	A	Pulse width t_P = 50 µs duty limited by T_{jmax}, T_C = 25°C	
V_{GS}	Gate Source Voltage	-10/+25	V		
P_{tot}	Power Dissipation	125	W	T_C=25°C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

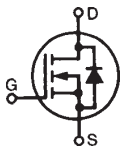
IXYS

Polar™ HiPerFET™ Power MOSFETs

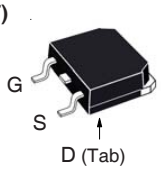
IXFT16N120P
IXFH16N120P

V_{DSS} = 1200V
I_{D25} = 16A
$R_{DS(on)}$ ≤ 950mΩ
t_{rr} ≤ 300ns

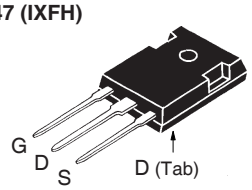
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



TO-268 (IXFT)



TO-247 (IXFH)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1200	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	1200	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25°C	16	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	35	A
I_A	T_C = 25°C	8	A
E_{AS}	T_C = 25°C	800	mJ
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
P_D	T_C = 25°C	660	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062in.) from Case for 10s	300	°C
T_{sold}	Plastic Body for 10 seconds	260	°C
M_d	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in.
Weight	TO-268	4	g
	TO-247	6	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	1200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1mA	3.5		6.5	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			25	μA
	T_J = 125°C			2.5	mA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1			950	mΩ

Features

- International Standard Packages
- Fast Recovery Diode
- Avalanche Rated
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Switch-mode and Resonant-Mode Power Supplies
- High Voltage Pulse Power Applications
- High Voltage Discharge Circuits in Lasers Pulsers, Spark Igniters, RF Generators
- High Voltage DC-DC converters
- High Voltage DC-AC inverters

CoolMOS™ Power Transistor

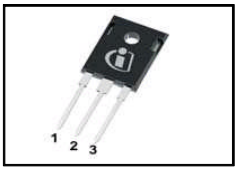
Features

- Lowest figure-of-merit R_{ON} x Q_g
- Extreme dv/dt rated
- High peak current capability
- Qualified for industrial grade applications according to JEDEC[1)]
- Pb-free lead plating; RoHS compliant
- Ultra low gate charge

Product Summary

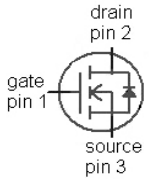
V_{DS} @ T_J = 25°C	900	V
$R_{DS(on),max}$ @ T_J=25°C	0.34	Ω
$Q_{g,typ}$	94	nC

PG-TO247



CoolMOS™ 900V is designed for:

- Quasi Resonant Flyback / Forward topologies
- PC Silverbox and consumer applications
- Industrial SMPS



Type	Package	Marking
IPW90R340C3	PG-TO247	9R340C

Maximum ratings, at T_J=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	15	A
		T_C=100 °C	9.5	
Pulsed drain current [2)]	$I_{D,pulse}$	T_C=25 °C	34	
Avalanche energy, single pulse	E_{AS}	I_D=3.1 A, V_{DD}=50 V	678	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=3.1 A, V_{DD}=50 V	1	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		3.1	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...400 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	208	W
Operating and storage temperature	T_J, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

Please note the new package dimensions arccording to PCN 2009-134-A

High Power SPT+ & Lugged Type IGBT Module

Description

DAWIN'S IGBT 7DM-1 Package devices are optimized to reduce losses and switching noise in high frequency power conditioning electrical systems. These IGBT modules are ideally suited for power inverters, motors drives and other applications where switching losses are significant portion of the total losses.

Features

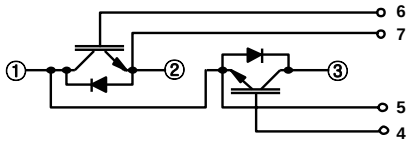
- ☞ High Speed Switching
- ☞ BV_{CES} = 1200V
- ☞ Low Conduction Loss : $V_{CE(sat)}$ = 1.8 V (typ.)
- ☞ Fast & Soft Anti-Parallel FWD
- ☞ Short circuit rated : Min. 10uS at T_C=100℃
- ☞ Reduced EMI and RFI
- ☞ Isolation Type Package

Applications

Motor Drives, High Power Inverters, Welding Machine, Induction Heating, UPS , CVCF, Robotics , Servo Controls

Equivalent Circuit and Package

Equivalent Circuit



Package : 7DM-1 Series

Please see the package out line information

Absolute Maximum Ratings @ T_j=25℃ (Per Leg)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	-	1200	V
V_{GES}	Gate-Emitter Voltage	-	±20	V
I_C	Collector Current	T_C = 25℃	150	A
		T_C = 80℃	100	A
$I_{CM\ (1)}$	Pulsed Collector Current	-	200	A
I_F	Diode Continuous Forward Current	T_C = 100℃	75	A
I_{FM}	Diode Maximum Forward Current	-	150	A
T_{SC}	Short Circuit Withstand Time	T_C = 100℃	10	uS
P_D	Maximum Power Dissipation	T_C = 25℃	700	W
T_j	Operating Junction Temperature	-	-40 ~ 150	℃
T_{stg}	Storage Temperature Range	-	-40 ~ 125	℃
V_{iso}	Isolation Voltage	AC 1 minute	2500	V
	Mounting screw Torque :M6	-	4.0	N.m
	Power terminals screw Torque :M5	-	2.0	N.m

CAS100H12AM1

1200V, 100A Silicon Carbide Half-Bridge Module

Z-FET™ MOSFET and Z-Rec™ Diode

V_{DS}	1200 V
I_D (T_C= 100°C)	100 A
$R_{DS(on)}$	16 mΩ

Features

- Ultra Low Loss
- High Ruggedness
- High-Frequency Operation
- Zero Reverse Recovery Current from Diode
- Zero Turn-off Tail Current from MOSFET
- Positive Temperature Coefficient on V_F and V_{DS}(on)

System Benefits

- Enables compact and lightweight systems
- High efficiency operation
- Mitigate over-voltage protection
- Ease of transistor gate control
- Reduces thermal requirements

Applications

- High Power Converters
- Motor Drives
- Solar Inverters
- UPS and SMPS
- Induction Heating

Package

Part Number	Package	Marking
CAS100H12AM1	Half-Bridge Module	CAS100H12AM1

Maximum Ratings (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Notes
V_{DS}	Drain - Source Voltage	1200	V		
V_{GS}	Gate - Source Voltage	-5/+20	V		
I_D	Continuous Drain Current	165	A	V_{GS} = 20V, T_C=25°C	
		105		V_{GS} = 20V, T_C=100°C	
$I_{D(pulse)}$	Pulsed Drain Current	400	A	Pulse width t_P = 1ms Limited by T_{jmax}, T_C = 25°C	
T_J	Junction Temperature	150	°C		
T_C , T_{STG}	Case and Storage Temperature Range	-55 to +125	°C		
V_{isol}	Case Isolation Voltage	6000	V	AC, t=1min	
L_{Stray}	Stray Inductance	<15	nH	Measured along maximum path from pad to Lug	
M	Mounting Torque	2.94	Nm		
G	Weight	200	g		
	Clearance Distance	12.2	mm	Terminal to terminal	
	Creepage Distance	17.3	mm	Terminal to terminal	
		20.2	mm	Terminal to base plate	

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