GaN-based HEMTs on Low Resistivity Silicon Technology for Microwave Applications

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Abstract— This paper investigates the effect of insertion AlN spacer between the GaN channel and buffer in a sub-micron gate (0.3 um) AlGaN/GaN HEMTs on a low-resistivity (LR) (σ < 10 Ω .cm) silicon substrates on RF performance. Enhancement in short circuit current gain (f_T) and maximum frequency of oscillation (f_{MAX}) was observed in the HEMT with a 1 nm AlN spacer, where (f_T) and (f_{MAX}) were increased from 47 GHz to 55 GHz and 79 GHz to 121 GHz, respectively. Small-signalmodelling analysis was carried out to study this improvement in performance. We found that the AlN interlayer played a crucial role in reducing the gate-source capacitance, C_{gs} , by 36 % and delay, τ , by 20 % under the gate, as a result of an increase in mobility and a reduction in trap-related effects.

INTRODUCTION:

Due to the superior material properties of Gallium Nitride, AlGaN/GaN high-electron-mobility transistors (HEMT) are emerging as promising candidates for high-power and high frequency applications [1]. Recent work on the integration of GaN HEMT based gate drivers and buck converters on insulating SiC substrates has achieved envelope tracking

bandwidths of 20 MHz [2] with power device switching frequencies up to 200 MHz. The potential use of this circuit for 5G applications using GaN on LR Si substrates, where both power and RF GaN are on the same chip, will offer the additional benefit of cost effective technology. Currently, GaN HEMT structures grown on LR Si substrates of diameters of up to 150 mm have been successfully realized, showing an RF performance with fr/fmax of 55 GHz/121 GHz respectively [3]. However, microwave performance of GaN HEMTs grown on LR Si is limited, mainly due to the RF signal coupling to the lossy Si substrate [4].

MATERIAL AND DEVICES:

Two different types of AlGaN/GaN HEMTs materials, with and without AlN interlayer, were grown on a 675 μ m thick 150 mm diameter P-type LR Si (σ < 10 Ω .cm) substrate by Metal-Organic Chemical Vapor Deposition (MOCVD). The layer stack, from the substrate up, consists of a 250 nm AlN nucleation layer followed by a 850 nm Fe-doped AlGaN graded buffer (to accommodate the lattice and thermal expansion mismatch), a 1.4 μ m insulating Fedoped GaN buffer layer and a GaN channel layer. The barrier layer consists of a 1 nm AlN

spacer layer, a 25 nm Al_{0.25}Ga_{0.75}N barrier and a 2 nm GaN cap. A detailed description of the growth procedure and parameters were mentioned in [3]. Hall measurements showed carrier density of 8.1×10^{12} cm⁻² and 7.1×10^{12} cm⁻², with associated mobility of 1700 cm²/V.s and 1580 cm²/V.s and sheet resistivity of 412 Ω /sq. and 552 Ω /sq., for epilayers with and without AlN interlayer, respectively.

Both device structures were simultaneously fabricated, with identical fabrication and dielectric passivation techniques, for accurate comparison. Electron beam (e-beam) lithography was adapted for all levels of device definition. Detailed fabrication process for both device structures are described elsewhere [3]. Transmission-Linemeasurements (TLMs) revealed that the AlN interlayer has no obvious effect on the ohmic contact, R_C formation. An R_C of 0.6 Ω .mm and specific contact resistivity, ρ_C of 5.71 \times 10⁻⁶ Ω .cm² were obtained.

RESULTS AND DISCUSSION

A. DC CHARACTERISITCS

Typical DC output characteristics of an L_g = 0.3 μ m, $W_g = 2 \times 100 \mu$ m wide devices are shown in Fig. 1a. Since the alloy scattering of binary compounds (AlN) is less than ternary compounds (AlGaN) [5], the insertion of AlN spacer layer at the heterojunction increases the quantum well depth and reduces alloy scattering, resulting in improvement in mobility of the charge carriers in the 2-DEG channel [6]. Hence, the HEMT with AlN spacer layer exhibits comparatively higher drain current density, IDS by 18% conventional AlGaN/GaN HEMT. maximum I_{DS} of 1.4 A/mm at $V_{DS} = 10$ V and $V_{GS} = +1$ V was obtained. However, the insertion of an AlN space layer caused a slight degradation in the switching performance,

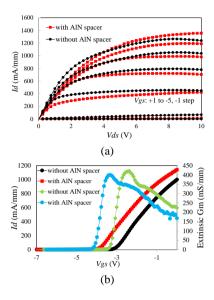


Fig. 1. (a) I_{DS} - V_{DS} characteristics of 2 x 0.3 μ m² x 100 μ m wide device and (b) Transfer characteristic of AlGaN/AlN/GaN HEMT on p-type LR Si (111) substrate.

with on-resistance, RoN of 2.76 Ω .mm compared to 2.24 Ω .mm for conventional AlGaN/GaN HEMTs without the AlN spacer.

Fig. 1b shows device transfer characteristics. Good pinch-off was achieved in all devices, with a -0.8 V shift in pinch-off voltage for device with an AlN spacer. A maximum G_M , of 433 mS/mm was obtained at $V_{DS} = 5$ V and $V_{GS} = -2.4$ V compared to 425 mS/mm at $V_{DS} = 5$ V and $V_{GS} = -3.2$ V when the AlN spacer layer was included.

B. RF CHARACTERISITICS

On-wafer small-signal S-parameters measurements were carried out from 0.1 to 67 GHz using an Agilent PNA network analyzer (E8361A). The system was calibrated with an

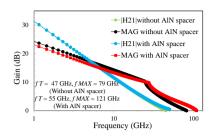


Fig. 2. Small-signal gain characteristics based on extracted S-parameters of a 0.3 μ m × 100 μ m AlGaN/GaN HEMTs on P-type LR Si (111) substrate at $V_{DS} = 5$ V.

off-wafer short-open-load-thru (SOLT) calibration technique. Devices were biased at the maximum G_M , where the highest values of current gain $|H_{21}|$ and maximum available gain (MAG) exist. Fig. 2 shows the deembedded small-signal gain characteristics of 0.3 μ m T-gate GaN-based HEMTs on LR Si, with and without the AlN spacer. Significant improvements in RF performance were observed when incorporating the AlN spacer in the layer structure. A maximum f_T of 55 GHz and f_{MAX} of 121 GHz were achieved for

the AlGaN /GaN HEMT with AlN spacer in comparison to an f_T of 47 GHz and f_{MAX} of 79 GHz for the conventional AlGaN/GaN HEMTs.

The effect of the AlN interlayer on RF performance was characterized based on the bias-dependent equivalent-circuit elements values, as summarized in table I [7]. The observed enhancement in microwave performance is mainly attributed to a reduction of the electron trap effect, which rises from local trap states at the device surface, at heteroiunction or in the bulk semiconductor [8]. This reduction in trapped charges caused a decrease of 36 % in device intrinsic capacitance C_{gs} (from 145 fF to 92 fF), which has a significant influence on f_T and f_{MAX} . Consequently, the modulated signal and electrical field under the gate edge towards the drain were increased despite the 11 % deterioration in the channel current modulation efficiency, G_M .

We believe that the insertion of AlN interlayer is very efficient in confining the electrons to the 2-DEG, preventing them from overflowing

TABLE I OPTIMIZED VALUES FOR ALL MODEL PARAMETERS USED IN THE EQUIVALENT CIRCUIT FOR A L_G = 0.3 µm and W_G = (2 × 100) µm transistors.

Extrinsic Parameters				Intrinsic Parameters			
Without AlN spacer		With AlN spacer		Without AlN spacer		With AlN spacer	
$C_{pg} = 43.9$	$C_{pgd} =$	$C_{pg} =$	$C_{pgd} =$	$C_{gd} =$	$G_M = 602$	$C_{gd} =$	$G_{M} = 530$
fF	16 fF	43.9 fF	15 fF	9.1 fF	mS/mm	10.5 fF	mS/mm
$C_{pd} = 43.1$	$R_s =$	$C_{pd} =$	$R_s =$	$C_{gs} =$	$R_{in} =$	$C_{gs} =$	$R_{in} =$
fF	10.5Ω	43.8 fF	10.5Ω	145.4 fF	20.3Ω	92.4 fF	13.11Ω
$L_s =$	$R_g =$	$L_s =$	$R_g =$	$C_{ds} =$	$R_{gd} =$	$C_{ds}=$	$R_{gd} =$
0.03pH	17.9Ω	0.03pH	17.9Ω	15.6 fF	500Ω	11.8 fF	500Ω
$L_g =$	$R_d =$	$L_g =$	$R_d =$	au =		au =	
23pH	12.3Ω	23pH	12.3Ω	1.5ps		1.2ps	
$L_d =$		$L_d =$					
25pH		25pH					

into the buffer and toward the conductive Si substrate. This is due to a modified band structure caused by the large conduction band off set, high polarization field and high barrier of AlN [9]. Therefore, access of carriers to electron traps and crystalline defects were reduced.

CONCLUSION

We have reported the influence of AlN interlayer between the GaN channel and AlGaN buffer of 0.3 μ m T-gate AlGaN/GaN HEMTs on a LR Si substrate on RF performance. f_T and f_{MAX} were improved by 17% and 53%, respectively when incorporating the AlN interlayer in layer structure; $f_T = 55$ GHz and $f_{MAX} = 121$ GHz. Small signal model analyses indicates that the enhancement in RF performance is mainly due to the trap reduction and increase in the mobility in the channel and confinement of the carriers reducing C_{gs} , and delay τ under the gate.

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