Self-Consistent Physical Modeling of SiO*x*-Based RRAM Structures

Toufik Sadi[a], Liping Wang[a], Louis Gerrer[a], Vihar Georgiev[a], and Asen Asenov[a,b]
[a] Device Modeling Group, School of Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK. [b] Gold Standard Simulations Ltd, Glasgow G3 7JT, Scotland, UK.
e-mail: Toufik.Sadi@glasgow.ac.uk

***Abstract*— We apply a unique three-dimensional (3D) physics-based atomistic simulator to study silicon-rich (SiO*x*, *x*<2) resistive switching nonvolatile memory (RRAM) devices. We couple self-consistently a simulation of ion and electron transport to the 'atomistic' simulator GARAND and a self-heating model to explore the switching processes in these structures. The simulation model is more advanced than other available phenomenological models based on the resistor breaker network. The simulator is calibrated with experimental data, and reconstructs accurately the formation and rupture of the conductive filament in the 3D space. We demonstrate how the simulator is useful for exploring the little-known physics of these promising devices, and show that switching is an intrinsic property of the SiO*x* layer. In general, the simulation framework is useful for providing efficient designs, in terms of performance, variability and reliability, for memory devices and circuits. The simulator validity is not limited to SiO*x*-based devices, and can be used to study other promising RRAM systems based, e.g., on transition metal oxides.**

Keywords*— *Resistive switching nonvolatile memory (RRAM) devices; Si-rich silica (SiO_x) RRAMs; charge transport; self-heating;

I. Introduction

Nonvolatile memories based on resistive switching (RRAMs) – also referred to as memristors – offer excellent controllability of charge in small semiconductor memory devices [1]–[14]. RRAM technology allows low cost-per-bit, low power dissipation, and high endurance, as discussed in the ITRS report of 2010 on emerging research devices [12]. In addition, RRAM devices can be integrated in crossbar arrays stacked in multiple levels in the 3D space. The development of SiO*x* RRAM technology, in particular, may result in a breakthrough in low-cost on-chip integration with Si microelectronics [1]. In this work, we present a self-consistent electrothermal simulation of intrinsic resistive switching in SiO*x* RRAM devices.

While memristors have been suggested theoretically in 1971 [15], it was only until 2008 that the first experimental demonstration of these structures was reported, using titanium dioxide (TiO_2) [13]. Since 2008, many RRAM technologies have been explored, including phase-change materials [10], silicon oxides [1] and metal oxides [13]. In RRAM systems based on oxides, resistance is switched through the formation and destruction of conductive filaments (CFs), controlled by the field- and temperature-driven redistribution of oxygen ions. Most work focuses on resistive switches based on transition metal oxides (TMO), such as hafnia (HfO_2), which are currently considered very promising. However, they face a serious challenge related to on-chip integration on silicon.

We employ a newly-developed self-consistent physical simulator for charge transport and self-heating to study intrinsic switching in SiO_x-based RRAM devices. Intrinsic resistive switching has been demonstrated experimentally, in SiO*x* RRAM structures, under ambient conditions by Kenyon and co-workers [1]; they reported devices that can be cycled between a high resistance state (HRS) and a low resistance state (LRS) with a resistance contrast of more than 10,000, for relatively long periods. Previous RRAM simulation work has relied on phenomenological models based on the resistor breaker network [14]. These models do not calculate self-consistently the electric fields and do not consider accurately the heat diffusion phenomenon. Our simulator uses a powerful combination of tools, to correctly reconstruct the conductive filament formation and destruction in the three-dimensional space, by coupling self-consistently oxygen ion and electron transport simulations to the local electric field and temperature distributions determined from physical models.

II. The Simulation Model

In the three-dimensional space, we couple a kinetic Monte Carlo (KMC) simulation of oxygen ion and an electron transport solver to GARAND [16] and a time-dependent heat diffusion equation (HDE) solver, to capture switching in the SiO*x* structure illustrated in Fig. 1 [1]. Within the simulation framework, the positions of oxygen ions and vacancies are tracked in time, the traps occupancies are updated regularly, and the electric field **E** is updated self-consistently according to the resulting charge distribution using GARAND. The solver GARAND evaluates accurately the electric field and potential distributions by coupling the solutions of Poisson's and density-gradient equations. Electrothermal coupling is achieved by solving the time-dependent HDE.

The local heat generation (fed into the HDE) is determined by the dot product of the field and current density vectors **J**•**E**, assuming Joule heating is the dominant mechanism for dissipation. Temperature rise due to self-heating is calculated by the resolution of the time-dependent HDE

$$\nabla \bullet \left[\kappa(\vec{r},T)\nabla T(\vec{r},t)\right] + g(\vec{r},t) = \rho C \frac{\partial T(\vec{r},t)}{\partial t}, \qquad (1)$$

978-0-692-51523-5/15/$31.00 ©2015 IEEE

using a more advanced in-house solver, as compared to time-independent HDE solvers employed for example in [18]–[20]. In equation (1), $T(\vec{r}, t)$ and $g(\vec{r}, t)$= **J**•**E** are the temperature and heat generation, respectively, at a given position $\vec{r}$ and time t, $\kappa(\vec{r},T)$ is the temperature-dependent thermal conductivity, ρ is the material density and C is the specific heat capacity. The field and temperature distributions are updated regularly, and are in turn used to update the ion-vacancy configuration and the traps occupancies.

Ion transport is governed by the following equation:

$$\frac{\partial n(\vec{r},t)}{\partial t} = \nabla \bullet \left[D\nabla n(\vec{r},t) - V_{ion} n(\vec{r},t) \right] + G \,, \qquad (2)$$

where n is the oxygen ion concentration, D is the diffusivity, V_{ion} is the ion velocity, and G is the net ion generation. The attempt-to-escape rate of oxygen (P_g) and ion velocity are given by:

$$P_g = f_0 \exp\left[-\frac{(E_a - \gamma eE)}{k_b T} \right] \qquad (3)$$

and

$$V_{ion} = a f_0 \exp\left(-\frac{E_m}{k_b T} \right) \sinh\left(\frac{eaE}{2k_b T} \right). \qquad (4)$$

In this case, f_0 is the vibration frequency, E_a is the formation energy, E_m is the oxygen migration barrier, γ is the contribution of the bond polarization to the local electric field E, and k_b is the Boltzmann constant. Accurate field and temperature distributions are also crucial for evaluating the hopping rates between the traps (Mott hopping), and the tunneling rates between the traps and the electrodes using the Wentzel-Kramers-Brillouin (WKB) approximation. The occupancies and tunneling rates are used to evaluate the steady-state electric current through the device using a solver similar to that proposed in [9]. Fig. 2 illustrates the simulation procedure. The simulator is validated against experimental trends of Si RRAM structures [1]. One exceptional aspect of the simulator is the use of an advanced structure editor, allowing the generation of a device structure of arbitrary geometry and material composition. This is especially useful when studying realistic SiO_x RRAM structures incorporating silicon-rich areas (e.g. with Si nano-inclusions) in the oxide.

The full experimental structures usually consist of a thin (10-120nm) layer of SiO_x between *n*-type electrodes (poly-Si) and a *p*-Si substrate with a Cr/Au electrode at its base. While the electrode plates have a typical area of 125µm×125µm [1], it is only necessary to study a smaller area (30nmx30nm in this paper), corresponding to a grain boundary region. Indeed, experiments suggest the existence of only one CF per plate.

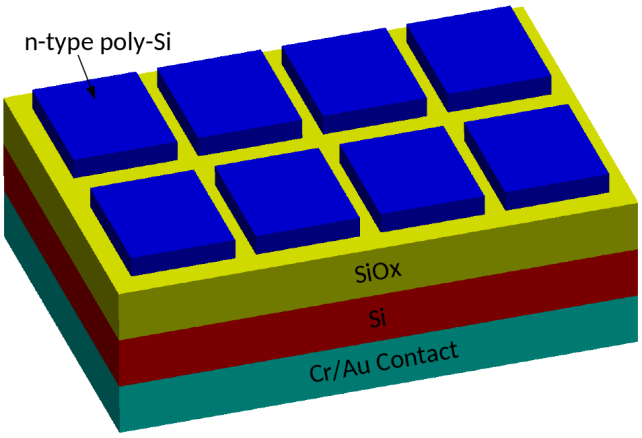


Fig. 1. The experimental RRAM structure from Ref. [1].

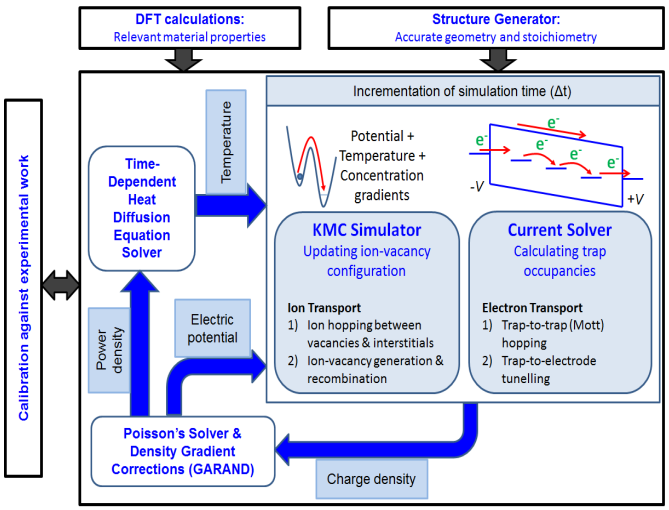


Fig. 2: The simulation framework, coupling self-consistently oxygen ion and electron transport to the local electric field and temperature distributions.

III. Results and Discussion

A 3D volume under a poly-Si plate has been simulated, by considering an oxide thickness of 15nm and a simulated contact area of 30nm long and 30nm wide. Fig. 3 shows the *I-V* characteristics of the device, obtained during the electroforming process. As the bias is increased from zero volts, and the conductive filament is formed, we impose a current compliance limit. As the bias is gradually reduced after filament formation, the device is maintained at a low resistance state (LRS) for a large bias range before it switches back to a high resistance state (HRS), at low biases. Therefore, and considering this behavior, the two-terminal device is

characterized by a variable resistor, whose effective resistance value depends on the current flowing through it, giving rise to its memristive characteristics.

Fig. 4 shows the vacancy distributions up to the CF formation. The initial structure includes defect/Si-rich areas in the form of a pillar [as illustrated in Fig. 4(a)]. At low biases, few vacancies are created, giving very low currents, as highlighted in Fig. 3. At around 5V, filament seeds appear and grow significantly as bias is increased to 10V. At around 11V, an accelerated generation of oxygen vacancies occurs, forming a CF and bridging the *p*-Si substrate and the poly-Si terminal. The CF formation gives rise to an abrupt jump in the current, as shown in Fig. 3, corresponding to the transition from the HRS to the LRS.

Figs. 5 and 6 show typical electric field and lattice temperature distributions, respectively, for low and high biases. Temperature rise due to self-heating is significant (300K or even higher) when the CF is formed, as a significant electric current starts to flow. Self-heating at the LRS plays a major role, as it affects the oxygen ion/vacancy generation probability and diffusion. The temperature maps are much less strongly localized than the electric field maps. Indeed, while percolation paths are characterized by very high power densities, temperature can still be high outside these paths due to heat diffusion. Fig 7 shows typical trap occupancy distributions, highlighting the 3D nature of percolation paths in real devices.

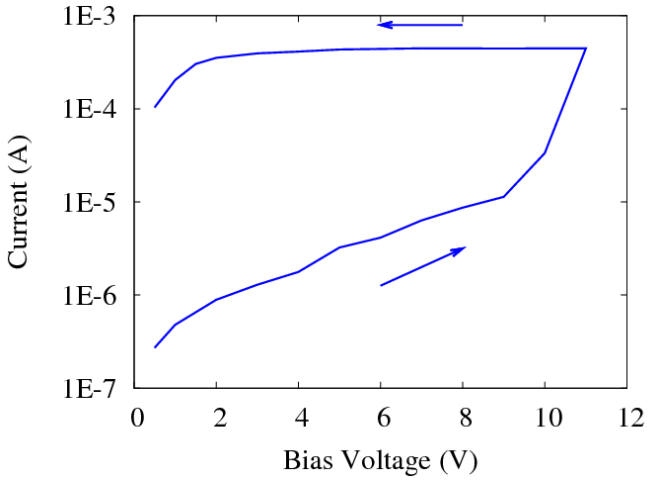


Fig. 3. The *I–V* characteristics of the device, during the conductive filament formation process.

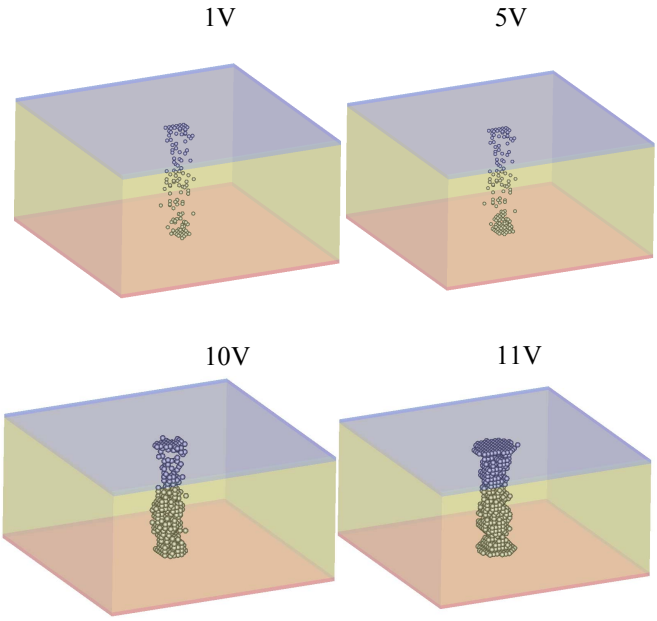
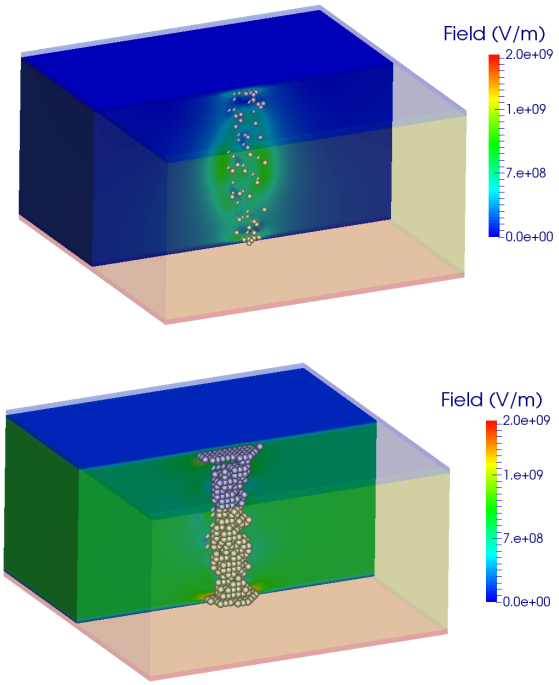


Fig. 4. The vacancy distribution through the filament formation process in the oxide (yellow volume). The Poly-Si electrode starts at z=15nm (blue volume) while the *p*-Si substrate ends at 0nm (red volume). The shown volume has an area of 30nm×30nm. (a) At low biases (1V in this case), only a small number of oxygen vacancies are generated. (b) As the bias voltage is increased (5V in this example), more vacancies are generated and seeds start to appear. (c) As the voltage is increased (10V here), filament seeds grow in a visible fashion. (d) At approximately 11V, an accelerated generation of oxygen vacancies occurs and forms a complete conductive filament, bridging the poly-Si plates to the *p*-Si substrate. Percolation paths are created, which are translated by the abrupt jump in the device current.



Figs. 5. typical electric field distributions, for (top) low (HRS) and (bottom) high (LRS) biases.

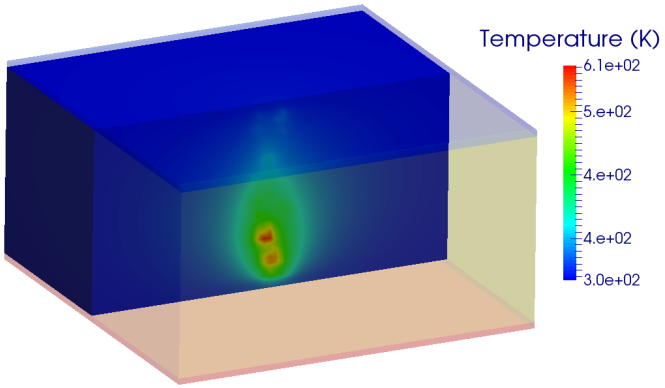


Fig. 6. A typical temperature distribution, at a given instant, during the CF formation.

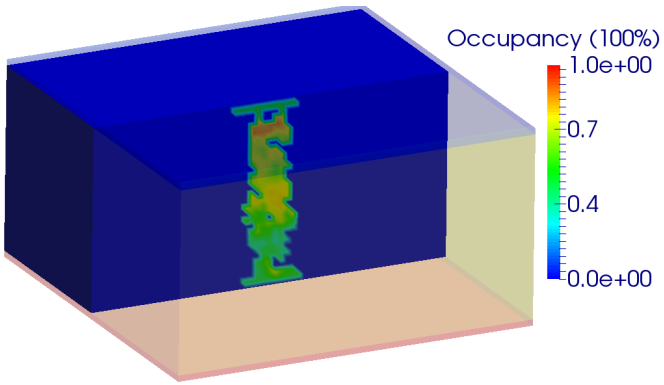


Fig. 7. A typical trap occupancy distribution, at a given instant, during the CF formation.

IV. Conclusions

We have developed and employed a 3D physical simulator for resistive switches to investigate the operation of silicon-rich silica (SiO_x) devices. The results reinforce the hypothesis that switching is an intrinsic property of the SiO*x* layer. Switching is due to the forming of conductive filaments in a highly substoichiometric oxide, governed by the applied field and temperature (due to self-heating) which re-arrange oxygen vacancy distributions in the oxide. In addition to providing insight into device physics, our simulator will prove useful in facilitating efficient designs in terms of performance, variability and reliability in RRAM devices and circuits.

Acknowledgment

We would like to thank the EPSRC (UK) for funding under the grant EP/K016776/1.

References

[1] A. Mehonic *et. al.*, "Resistive switching in silicon sub-oxide films," J. Appl. Phys., vol. 111, pp. 074507–1–9, 2012.

[2] L.O. Chua, "Resistance switching memories are memristors," Appl. Phys. A, vol. 102, pp. 765–783, 2011.

[3] M. Buckwell *et. al.*, "Microscopic and spectroscopic analysis of the nature of conductivity changes during resistive switching in silicon-rich silicon oxide," physica status solidi (c), vol. 12, pp. 211–217, 2015.

[4] A. Mehonic *et. al.*, "Quantum Conductance in Silicon Oxide Resistive Memory Devices," Scientific Reports, vol. 3, pp. 2708–1–7, 2013.

[5] A. Mehonic *et. al.*, "Electrically tailored resistance switching in silicon oxide," Nanotechnology, vol. 23, pp. 455201–1–9, 2012.

[6] J. Yao *et. al.*, "In situ imaging of the conducting filament in a silicon oxide resistive switch," Scientific Reports, vol. 2, pp. 242–1–5, 2012.

[7] A. Chanthbouala *et. al*., "A ferroelectric memristor," Nat. Mater., vol. 11, pp. 860–864, 2012.

[8] J. Yao *et. al.*, "Intrinsic resistive switching and memory effects in silicon oxide," Applied Physics A, vol. 102, vol. 835–839, 2011.

[9] S. Yu *et. al.*, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," In Electron Devices Meeting (IEDM), 2011 IEEE International, pp. 17.3., 2011.

[10] R. E. Simpson *et. al*., "Interfacial phase-change memory," Nature Nanotechnology, vol. 6, pp. 501–505, 2011.

[11] J. Yao *et. al.*, "Resistive Switches and Memories from Silicon Oxide," Nano Lett., vol. 10, pp. 4105–4110, 2010.

[12] The ITRS 2010 report [Online]. Available: http://www.itrs.net/

[13] D. B. Strukov *et. al.*, "The missing memristor found," Nature, vol. 453, pp. 80–83, 2008.

[14] S. C. Chae *et. al.*, "Random circuit breaker network model for unipolar resistance switching," Advanced Materials, vol. 20, pp. 1154-1159, 2008.

[15] L.O. Chua *et. al.*, "Memristor-The missing circuit element," IEEE Trans. Circuit Theory, vol. 18, pp. 507–519, 1971.

[16] GARAND Statistical 3D TCAD Simulator [Online]. Available: http://www.goldstandardsimulations.com/

[17] Y. Wang *et. al.*, "Resistive switching mechanism in silicon highly rich SiO_x (x<0.75) films based on silicon dangling bonds percolation model," Appl. Phys. Lett., vol. 102, pp. 042103–1–5, 2013.

[18] T. Sadi, J.-L. Thobel and F. Dessenne, "Self-Consistent Electrothermal Monte Carlo Simulation of Single InAs Nanowire Channel MISFETs," J. Appl. Phys., vol. 108, pp. 084506–1–7, 2010.

[19] T. Sadi and R. W. Kelsall, "Monte Carlo Study of the Electrothermal Phenomenon in SOI and SGOI MOSFETs," J. Appl. Phys., vol. 107, pp. 064506–1–9. 2010.

[20] T. Sadi, R.W. Kelsall and N. J. Pilgrim, "Electrothermal Monte Carlo Simulation of Submicrometer Si/SiGe MODFETs". IEEE Transactions on Electron Devices, vol. 54, pp. 332-339, 2007.