Direct Fabrication of Functional Ultrathin Single-Crystal Nanowires from Quasi-One-Dimensional Van Der Waals Crystals

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ABSTRACT:

Micromechanical exfoliation of 2D van der Waals materials has triggered an explosive interest in 2D material research. The extension of this idea to 1D van der Waals materials, possibly opening a new arena for 1D material research, has not yet been realized. In this paper we demonstrate that 1D nanowire, with sizes as small as 6 molecular ribbons, can be readily achieved in the Ta_2(Pd or Pt)$_3Se_8$ system by simple micromechanical exfoliation. Exfoliated $Ta_2Pd_3Se_8$ nanowires are n-type semiconductors, whereas isostructural $Ta_2Pt_3Se_8$ nanowires are p-type semiconductors. Both types of nanowires show excellent electrical switching performance as the channel material for a field-effect transistor. Low temperature transport measurement reveals a defect level inherent to $Ta_2Pd_3Se_8$ nanowires, which enables the observed electrical switching behavior at high temperature (above 140K). A functional logic gate consisting of both n-type $Ta_2Pd_3Se_8$ and p-type $Ta_2Pt_3Se_8$ field-effect

transistors has also been successfully achieved. By taking advantage of the high crystal quality derived from the parent van der Waals bulk compound, our findings about the exfoliated Ta_2(Pd or Pt)$_3Se_8$ nanowires demonstrate a new pathway to access single-crystal 1D nanostructures for the study of their fundamental properties and the exploration of their applications in electronics, optoelectronics, and energy harvesting.

KEYWORDS: *1D nanostructure, nanowire, van der Waals material, mechanical exfoliation, field-effect transistor*

The application of micromechanical exfoliation to obtain graphene has demonstrated the convenience of achieving few-layer or even single-layer atomic sheets with unsurpassed quality and largely protected intrinsic properties.[1,2] Such success has led to a surge of interest in so-called 2D "van der Waals (vdW)" material, often referred to as layered compounds with the building blocks of 2D atomic sheets bonded together by weak vdW interaction. Thinned down to atomic level micromechanically, 2D material in this category often exhibit extraordinary electrical, optical, thermal, mechanical, chemical and biological properties due to quantum confinement and surface effects from the reduced dimension, exemplified by graphene which exhibits extremely high electron mobility and room temperature quantum Hall effect[3]. Monolayer and few-layer semiconducting 2D vdW materials including transition metal dichalcogenides[4,5] and black phosphorus[6] have shown admirable electrical switching performance. Moreover, indirect- to direct-band gap transition[7] from bulk to monolayer and the "valley" nature of the conduction carriers[8] in transition metal dichalcogenides show great potential for the application of optoelectronics and spintronics. Recently, stacking various types of 2D vdW atomic sheets together to form heterostructures has produced even more exotic

properties, such as the strong coulomb drag in graphene-hBN structure[9], the record-high mobility and quantum oscillation in MoS_2-hBN[10] and black phosphorus-hBN structure[11], and more.

Although micromechanically prepared 2D vdW material has led to an explosion of discoveries and exciting physics, the extension of exfoliation from 2D vdW materials to 1D has remained unproven. Previously, to obtain 1D nanostructured material, various synthesis methods have been adopted, such as Arc-Discharge,[12] Vapor–Liquid–Solid (VLS) Mechanism,[13] Chemical Vapor Deposition (CVD),[14] Hydrothermal Reaction,[15] Molecular Beam Epitaxy (MBE),[16] Laser Ablation[17] and Electroless Metal Deposition and Dissolution (EMD)[18]. However, these methods often bring complexity to the resulting 1D nanostructures compared to the bulk, such as surface contaminations, lattice defects, and poor chemical stability (degradation in ambient environment). These issues alter or obscure intrinsic properties and limit potential applications. Especially in the case of semiconducting materials, one would expect nanowires to provide excellent controllability of electrical and optical properties originating from the semiconducting band gap. However, regardless of the various synthesized semiconducting nanowires, there are only a few types of nanowires whose synthesis issues are resolved and show promise with regard to functional electrical or optical devices, such as the quantum devices of single-wall carbon nanotube[19-21], the high-performing field-effect transistors of silicon nanowire[22], light emitting device based on direct-gaped group III-V/nitride compound[23,24] or ZnO[25] nanowires. Therefore, new methodology to prepare high quality 1D nanostructures is needed to further advance 1D materials research.

Here we propose a new strategy of obtaining 1D nanostructure with direct fabrication from high quality bulk material, in order to avoid the problems inherent in conventional synthesis. Indeed, like the aforementioned 2D vdW materials[26,27] a wide range of materials can be viewed

as 1D vdW material, for example, the binary tetradymite M_2X_3 (M=Sb, Bi, X=S, Se), the ternary chalcogenides $M_2X_3Y_8$ (M=Ta, Nb, X=Ni, Pd, Pt, Y=S, Se) and more. These materials have an essentially linear crystal structure with bonding strengths between and within the linear structures (which we here call 'ribbons' to reflect their geometry) that can differ by ~20 times. The feasibility of separating atomic-level thin ribbons from the bulk using micromechanical exfoliation has been theoretically predicted.[28]

In this paper, we use isostructural $Ta_2Pd_3Se_8$ (TPdS) and $Ta_2Pt_3Se_8$ (TPtS) to demonstrate that, high quality 1D nanowires composed of a few molecular ribbons can be obtained with simple micromechanical exfoliation, avoiding conventional chemical synthesis steps. Moreover, we show that the semiconducting properties of the resulting 1D nanowire can be controlled through the careful selection of bulk materials. TPdS nanowire appears to be an n-type semiconductor, while TPtS nanowire is p-type. Given easy accessibility of different thicknesses from exfoliation, our electronic band structure calculation for TPdS nanowire reveals that from multi-ribbon to single-ribbon the band gap transforms from indirect to direct with a gap size about 1eV for single ribbon. The field-effect transistor (FET) fabricated based on both nanowires show commendable performance with a high on/off ratio, high mobility and ultralow standby current. Both electrical transport and high resolution transmission electron microscopy (TEM) indicate excellent stability for these nanowires. Combining both n- and p-type FETs of TPdS and TPtS, a functional logic gate can also be easily realized.

First reported by Keszler et.al,[29,30] in the bulk, the quasi-1D structured TPdS and TPtS belong to the isostructure group of $M_2X_3Se_8$ (M=Ta or Nb, X=Ni, Pd or Pt)[30] with an orthorhombic space group of $D_{2h}^{9} - Pbam$, and the crystal structure can be viewed as a framework of molecular ribbons extending along the *c* axis as shown in Figure 1a (Since TPdS

and TPtS are isostructures, we will mainly focus on TPdS in the following sections). Each ribbon contains two chains of Ta centered edge-sharing Se trigonal prisms that are jointed at the ribbon midline and capped at the two sides by Pd atoms. The zigzag edge of TPdS ribbon is similar to the molecular ribbon structure of WS_2[31] that has been synthesized chemically using single wall carbon nanotubes as a template. Such zigzag edges are popular often found in the grain boundaries[32] of CVD-grown atomic sheets of TMDs. Unlike WS_2 ribbons with broken mirror symmetry and edges terminated by either W or S atoms, a TPdS single ribbon has mirror symmetry with both edges terminated by Pd atoms only. TPdS molecular ribbons are connected to each other in the bulk via weak binding between the edge-terminating Pd atoms and trans-Se atoms, which slightly distorts the corresponding Se-prisms. Four interconnected ribbons form a 4-blade "windmill" unit with a large channel in the center. Although bulk TPdS was successfully synthesized 20 years ago, its fundamental physical properties have not been studied. Notably, its potential to produce one-dimensional nanostructures has never been considered or explored prior to our work.

High quality needle-like bulk crystals were synthesized using a chemical vapor transport (CVT) method (see details in supplementary information). The average length was about 1 cm along the extended direction (crystal *c*-axis) as shown in the insert of Figure 1b. The crystal structure was determined by X-ray Diffraction (XRD) as shown in Supplementary Figure S2. The temperature dependence of bulk resistivity from 300 K to 16 K was measured and showed nonmetallic behavior, i.e. resistivity increases with decreasing temperature as shown in Supplementary Figure S3, implying possible semiconducting electronic properties. It has a low resistivity value, ~0.054 Ω·cm at room temperature, close to the value of heavily doped silicon and germanium.[33-35] The bulk crystals appear to have a fibroid nature, and they separate easily

into microscopically thin wires if pressed between two microscope slides. The resulting thin wires can be clearly seen with scanning electron microscope (SEM) as shown in Figure 1b.

To understand such structurally dissociative behavior, the spatial distribution of charge density for bulk TPdS was simulated as shown in Figure 1c. The molecular-ribbons in TPdS bulk have an inter-ribbon bonding energy of 0.34 eV/atom, whereas the average intra-ribbon bonding energy is about 5.7 eV/atom, i.e. seventeen times stronger. This large difference in bonding strength is also consistent with the difference in bond lengths for inter-ribbon Pd-Se (2.6 Å) and intra-ribbon Pd-Se (2.47 Å), as labeled in Figure 1a. Although the inter-ribbon bonding strength is about 30 times stronger than the weakest form of vdW bonding, (London dispersion bonding ~0.01 eV/atom), it is comparable to hydrogen-bond type vdW forces; for example, hydrogen bonding between water molecules is about 0.24 eV/atom. Therefore, we expect that the existence of the weak vdW bonding between molecular-ribbons provides an opportunity to cleave bulk crystal into thinner wires mechanically, similar to the exfoliation of other 2D vdW materials.[2,36]

Indeed, atomically thin TPdS nanowires can be obtained using microexfoliation. We used adhesive tape to split a bulk TPdS crystal several times before press-transferring onto a thermally oxidized silicon wafer (285 nm SiO_2). The TPdS nanowires left on the substrate after the exfoliation process can be easily identified with an optical microscope. TPdS nanowires exhibit different colors corresponding to different thickness as shown in Supplementary Figure S4, similar to the case of exfoliated 2D vdW material.[37,38] Nanowires with diameters ranging from hundreds to a few nanometers (as thin as 1.2 nm) can be further identified by atomic force microscopy (AFM) as shown in Figure 1d. The majority of the identifiable exfoliated nanowires on Si substrate possess a length/diameter ratio larger than 100.

Aberration-corrected scanning transmission electron microscopy (STEM) was used to analyze the crystal structure and morphology of TPdS nanowires in detail. Figure 2a shows a low magnification annular dark field (ADF) image of TPdS nanowires with a broad distribution of thicknesses. The elementary map of Pd and Ta for high quality TPdS single crystal structure is atomically resolved and mapped by energy-dispersive X-ray spectroscopy (EDX) (see supplementary information). High quality nanowires with various thicknesses can be easily found and identified with STEM. Figure 2b shows a set of atomic resolution images of nanowires with thickness ranging from 15.8 nm to 2.87 nm. The clean and smooth surface of nanowire crystal suggests that high level of crystallinity has been preserved in exfoliated TPdS nanowires. We note that these samples were prepared and stored in ambient environment for more than 10 days before STEM analysis. Surprisingly, we did not observe any sign of surface degradation in high resolution STEM images after this exposure to air. The thinnest nanowire in this STEM study is about 2.1 nm, as shown in Figure 2c. The crystal orientation and elemental arrangement can be identified simply by comparing crystal structure with the STEM image. For this specific 2.1 nm thick nanowire, the zone axis (marked by red arrows) lies in the direction of [120] for most of the wire, but there is a small twist of 2.5^{o} on the top left of the image.

Density functional theory (DFT) calculations of the energy of low index surfaces were conducted to predict a TPdS nanowire's equilibrium shape using the Wulff construction (see Supplementary Information) and provide details on the accessible surfaces for thick wires. Large nanowires minimize their energy by adopting the shape shown in Figure 2d, which is constructed with the facets of (100), (010), (110) and (210). We have surveyed various nanowires with STEM and concluded that most of the observed surface facets in thick nanowires (>10nm) do indeed belong to the four listed orientations from calculation as shown in Figure 2e.

Since bulk TPdS shows a semiconducting behavior, we expect the conductivity of an exfoliated nanowire may be modulated electrostatically if an appropriate energy band gap exists. The band structure of TPdS nanowire and its evolution upon reducing diameter have been calculated with DFT within the PBE-PAW approximation. Figure 3a shows the electronic band structure of bulk TPdS with an indirect band gap of 0.525 eV between the maximum of the valence band at the Γ point and the minimum of the conduction band, between the Γ and Z points. Band energy dispersions for nanowires with nine-, six- and four-ribbon structures are presented in the Figure 3b. As the number of ribbons contained in a nanowire decreases, the band gap increases; the bottom of the conduction band between the Γ and Z points, formed by Pd and Se edge atoms, shifts up and becomes higher than the Γ point, whereas the top of the valence band remains at the Γ point. Thus we expect a transition from an indirect band gap in bulk material to a direct band gap in a single ribbon. The band gap of a single ribbon is about 1.038 eV, nearly double the size of the bulk band gap, as shown in Figure 3c. The estimated electron effective masses at the Γ-point are $m_e^* = 1.23m_e$, $1.21m_e$, $1.10m_e$ and $1.10m_e$ for nine-, six-, four- and single ribbon respectively, which is comparable to that of MoS_2 nanoribbons[39] (~$1.2m_e$). According to our calculations, with a proper size of the band gap TPdS nanowire is expected to be a good candidate as a channel material for field-effect transistor (FET).

In order to study the semiconducting properties of TPdS nanowire, we fabricated FETs with a back gate layout, in which the SiO_2 layer is used as the dielectric layer separating the back gate, i.e., the heavily doped silicon underneath. Contacts to the TPdS nanowires, acting as source drain electrodes, were 30 nm Pd fabricated using electron beam lithography followed by electron beam evaporation. Figure 4a shows the AFM image of a typical TPdS FET device, which is based on a 13.8 nm TPdS nanowire. Before the electrical transport measurements, TPdS FET devices were

annealed at 180 °C in argon for 2 hours to improve contact quality and to remove any possible organic residue. Gate sweeps at room temperature for this specific TPdS device are displayed in Figure 4b, showing an n-doped characteristic. At 1 V source-drain bias, the device can be switched off, with an off-state current near 2×10^{-11} A at back gate voltage (V_{bg}) of -60 V. When the back gate is set to +60 V, the on-state current reaches 1.75×10^{-7} A, which corresponds to a current density of 1.0×10^{5} A/cm^2 comparable to the reported value of silicon nanowires.[40,41] The maximum I_{On}/I_{Off} ratio exceeds 10^4. The corresponding I-V measurements at different gate voltages are plotted in the insert of Figure 4b. The linearity in all I-V curves at room temperature indicates an essentially Ohmic contact between the TPdS nanowire and Pd. Based on gate sweeps, the field effect carrier mobility μ_{FE} can be extracted from the standard FET model $\mu_{FE} = [dI_{ds}/dV_{bg}]\times[L/(WC_{ox}V_{ds})]$, where L is the channel length, W is the channel width, and C_{ox} is the capacitance per unit area. The mobility of TPdS nanowire exhibits strong thickness dependence as shown in Supplementary Figure S8. Nanowires with diameters ranging from 12 to 30 nm show the highest mobility, around 80 cm^{2}V^{-1}s^{-1}. The lower mobility in thinner nanowires may originate from increased surface scattering. For nanowires thicker than 30nm the inter-ribbon conductivity increases, which results in an underestimation of the extracted mobility.[5] This effect is similar to the underestimation of mobility in other semiconductor systems when Schottky barriers are present.[42]

To better understand electrons' transport mechanism in TPdS nanowires, transport measurements at temperatures spanning from 90 K to 300 K were performed. Figure 4c shows gate sweeps at different temperatures for a 28 nm thick device with a source-drain bias set to 0.2 V. At 280 K a clear turn-on behavior can be seen with a threshold voltage (V_{th}) around -20 V and a subthreshold slope of 10 V/dec in the weak inversion region (marked as a yellow dashed

line). The relatively large subthreshold slope is due to the low gating efficiency from the thick dielectric layer of SiO_2. From the gate sweeps at various temperatures, it can be seen that V_{th} increases significantly with decreasing temperature down to 140 K, below which the device operates in a subthreshold region with a diminishing threshold voltage. As shown in the insert of Figure 4c, I-V sweeps at higher temperatures (280 K and 180 K) are linear, while nonlinearity becomes noticeable at low temperatures (100 K and 50 K). The nonlinearity in I-V sweeps at low temperatures indicates a Schottky barrier is present between the Pd contacts and TPdS nanowires, which becomes small enough to be unnoticeable at room temperature.

In Figure 4d, we plot the temperature dependence of source-drain current at different fixed gate voltages from +30 V to +80 V and the source-drain bias set to 0.2 V. We notice that, for all gate voltages, the temperature dependence of the current has two distinct behaviors above and below 140 K. This implies that carrier transport in these two regimes is governed by different mechanisms. Above 140 K, the temperature dependence of current follows a thermal activation model, which can be verified by fitting the data with $I = A_0 e^{-\frac{E_a}{k_B T}}$ (black solid line in the plot). Here, A_0 is the fitting constant, E_a is the thermal activation energy and k_B is Boltzmann's constant. The activation energy E_a decreases monotonically with increasing gate voltage as shown in Supplementary Figure S9d. At a gate voltage of 26 V, the flat-band condition is satisfied and the corresponding thermal activation energy E_a is about 58 meV indicating a shallow defect level below the conduction band edge.

For temperatures below 140 K, thermal activation of electrons to the conduction band is suppressed and the transport is dominated by hopping conduction.[43] In disordered 1D systems at low temperature several different hopping models, including Mott's variable range hopping, nearest neighbor hopping and Efros and Shklovskii variable range hopping (ES-VRH), have

been proposed.[44-46] We notice strong coulomb interaction between electrons exists in our TPdS nanowires, evidenced by a differential conductance anomaly at low bias (see Supplementary Figure S10). Therefore we expect the ES-VRH model, with characteristic equation[47-50] $I = A_0' e^{-\frac{\sqrt{T^*}}{\sqrt{T}}}$ should be appropriate for our data, where A_0' and T^* are fitting parameters. As shown by the red solid lines in Figure 4d, the ES-VRH model produces an excellent fit to our data. The estimated localization length *a* (see Supplementary Information for details of the fitting) is about 9 nm in our TPdS nanowires, which is an acceptable value for 1D materials, such as disordered single wall carbon nanotube.[49]

As mentioned in the TEM study, we find that as-exfoliated TPdS nanowires are stable in air with preservation of good crystallinity. To further test their stability, an uncoated TPdS FET device (with 14.5 nm TPdS nanowire) was examined repeatedly over a period of 40 days by recording its transconductance as shown in Supplementary Figure S11. Unlike other types of nanowire, the TPdS FET exhibits nearly unchanged performance while exposed to air over this time period.

With the same process, we also fabricated FETs using TPtS nanowires and characterized their room temperature performance. As indicated in Figure 4e, the transconductance for a 18-nm-thick TPtS nanowire FET with fixed source-drain bias (V_{ds} = 2, 1, 0.5, 0.2, and 0.1 V) indicates a p-type semiconducting behavior with an on/off ratio approaching 10^5 at V_{ds} = 2 V and a field effect mobility reaching 19.2 $cm^2V^{-1}s^{-1}$. The apparent linearity in I-V sweeps at different gate voltages (V_{bg} = -60, -20, 20, and 20 V) shown in the top right insert indicates good contacts formed between the TPtS nanowire and the Pd metal. To further illustrate the functionality of both n-type TPdS and p-type TPtS nanowire FETs, we built a logic circuit of NOT gate, i.e. an

inverter, by selecting devices with comparable performance factors, such as the on/off ratio and the value of conductance, as indicated by the transconductance data in the top left of Figure 4f. The schematic drawing of an inverter circuit is shown in the top right of Figure 4f, where n-type TPdS and p-type TPtS FETs are connected in series through source-drain terminals. When the device is in operation, bias voltage V_{DD} is set to 1 V and the back gates of both FET devices are connected together acting as the signal input terminal (V_{in}) which can be switched between -10 V and +10 V (normalized to 0 and 1 in the plot) every 5 seconds. The output signal (V_{out}) is measured at the midpoint where both FETs join together. The signal response of the inverter is shown in the bottom plot of Figure 4f exhibiting a clear signal-inverting functionality.

In summary, we have demonstrated that, by exploiting the weak vdW bonding between 1D molecular-ribbons in TPdS and TPtS, semiconducting single-crystal nanowires can be fabricated with single-step micromechanical exfoliation. This fabrication technique produces chemically stable and robust TPdS and TPtS nanowires. Thicknesses down to a few molecular-ribbons can be achieved while preserving excellent crystal quality. Band structure calculations show that the band gap expands from indirect 0.53 eV in the bulk to direct 1.04 eV in a single ribbon. FETs fabricated using both individual TPdS and TPtS nanowire exhibit excellent room temperature switching performance. Our low-temperature transport study reveals that carrier transport in TPdS nanowires is dominated by thermally activated electrons from a shallow defect level above 140 K and variable range hopping at lower temperatures. A functional logic gate that combines both n-type TPdS and p-type TPtS FETs was also successfully made. By taking advantage of the high crystal quality derived from the parent vdW bulk, our results provide a new pathway to access single-crystal 1D nanostructures for the study of fundamental properties and the exploration of applications in electronics, optoelectronics, and energy harvesting.

ASSOCIATED CONTENT

Supporting Information

Bulk TPdS crystal growth and resistivity temperature dependence, atomic and electronic structure calculation details, optical identification of exfoliated TPdS nanowires, atomic resolution STEM analysis and EDX analysis of TPdS nanowires, Wulff construction, FET mobility versus thickness histogram, energy band diagram of TPdS FET with different gate voltages, differential conductance at different temperatures, environmental stability test with transport characterization.

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Author Contributions

X.L. and J.L. contributed equally to this work.

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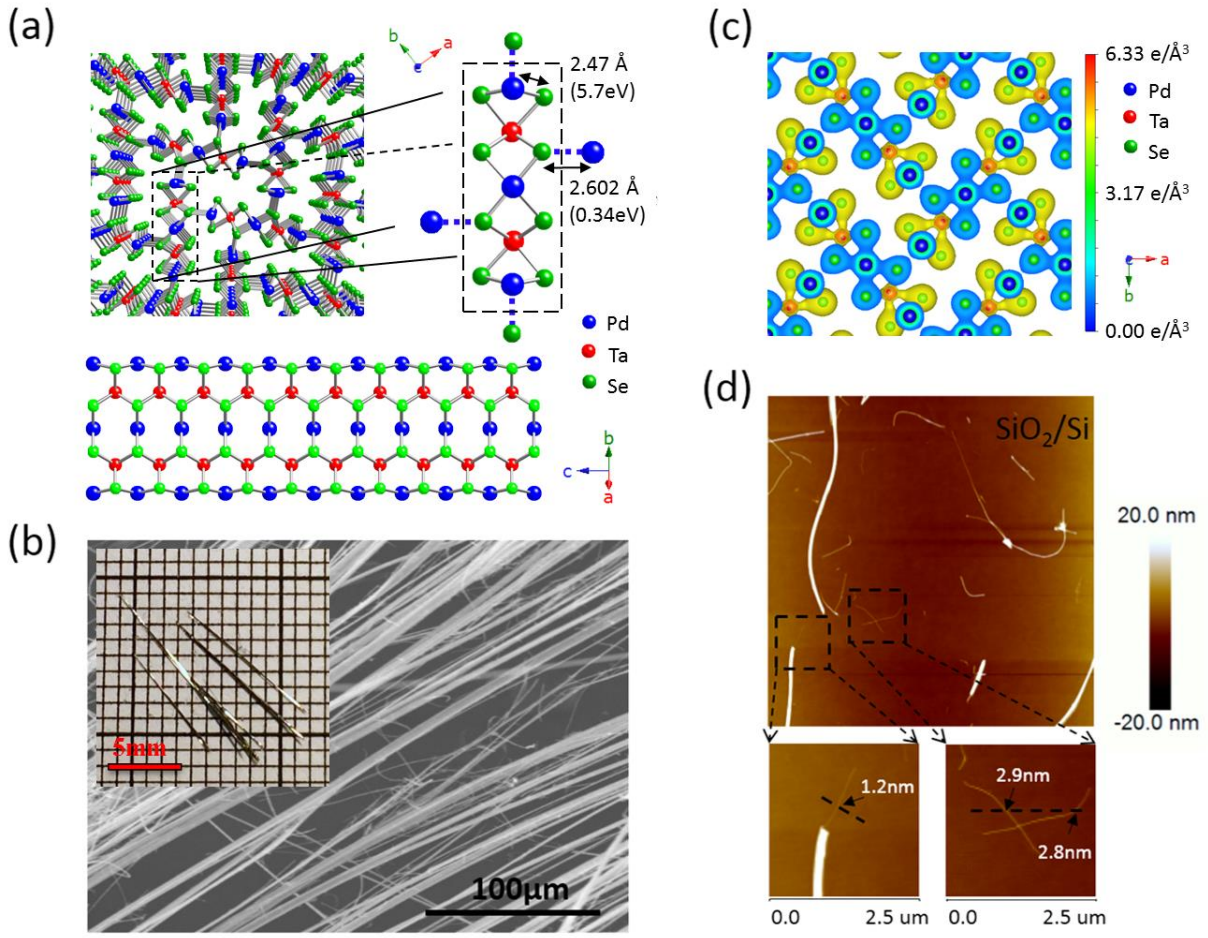

Figure 1 | (a) TPdS crystal structure. Top left: perspective view of bulk TPdS projected along the *c*-axis. Top right: cross section view of a single ribbon (inside the dashed rectangle). The length and bonding energy for intra (solid line) and inter (blue dashed line) bonds are 2.47 Å/5.7 eV and 2.602 Å/0.34 eV respectively. Bottom: top view of a single ribbon that extends along the c direction. (b) Scanning electron microscope image of the bulk crystal. The insert shows the as-grown needle-like single crystals. (c) Isosurface map (set at 0.05 e/Å^3) of the simulated spatial distribution of charge density (001 surface), the positions of Pd, Ta, and Se atoms are indicated by blue, red, and green spheres, respectively. (d) AFM images of TPdS nanowires prepared by micromechanical exfoliation. Extremely thin nanowires (1.2 nm, 2.8 nm and 2.9 nm) can be found in two highlighted regions.

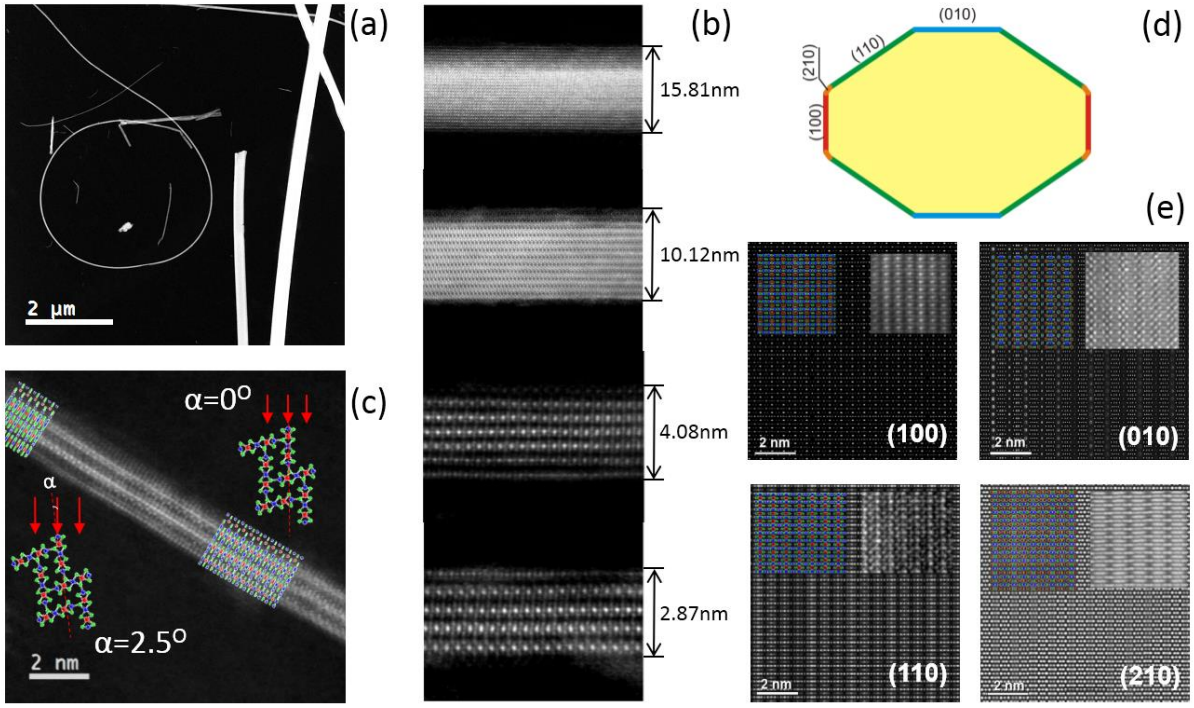

Figure 2 | STEM study of exfoliated TPdS nanowires. (a) Low magnification ADF image of TPdS nanowires. (b) Atomic resolution ADF images of nanowires with thickness ranging from 15.8 nm to 2.87 nm. (c) ADF image of a nanowire with 2.1 nm thickness. Top right and bottom left inserts are the simulated cross section view of a corresponding six-ribbon structure for upper and lower parts of this wire respectively. Red arrows indicate the electron beam direction. (d) Cross section view of the simulated equilibrium shape of TPdS nanowire constructed with four preferred facets, (100), (010), (110), (210). (e) Four simulated STEM images overlapped with crystal structure (top left) and obtained STEM image (top right) corresponding to the facets indicated in (d).

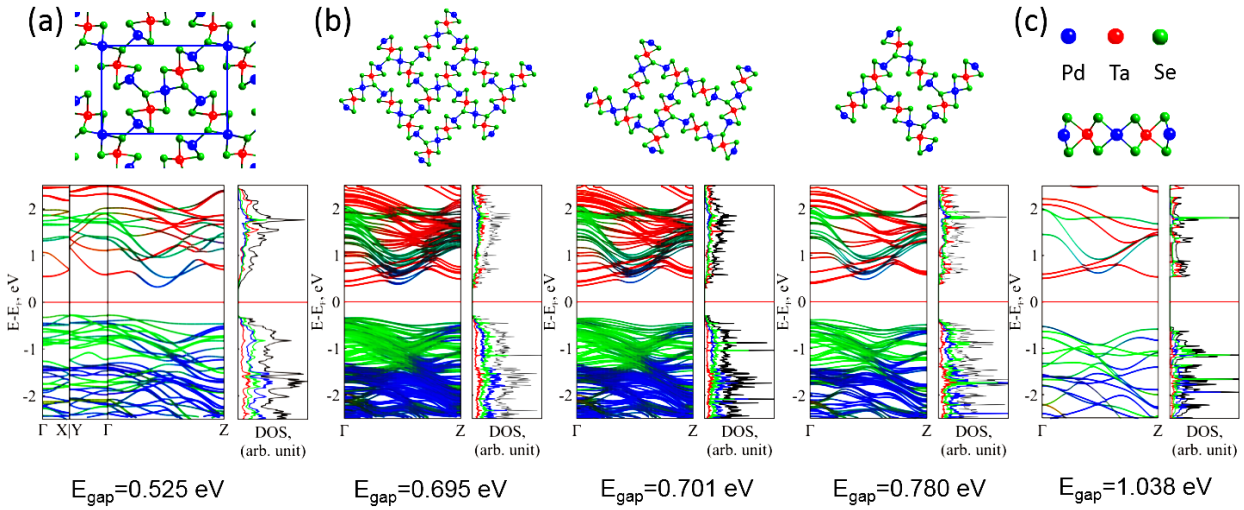

Figure 3 | Projected electronic band structure, density of states and cross-section view of TPdS. (a) bulk structure and nanowires consist of (b) nine-, six-, four- and (c) single ribbon. The red, blue and green colors correspond to the contributions from Ta, Pd and Se atom respectively, while the black curves in the DOS structure represent total density of states. The Fermi level is shifted to zero and marked by the horizontal red line.

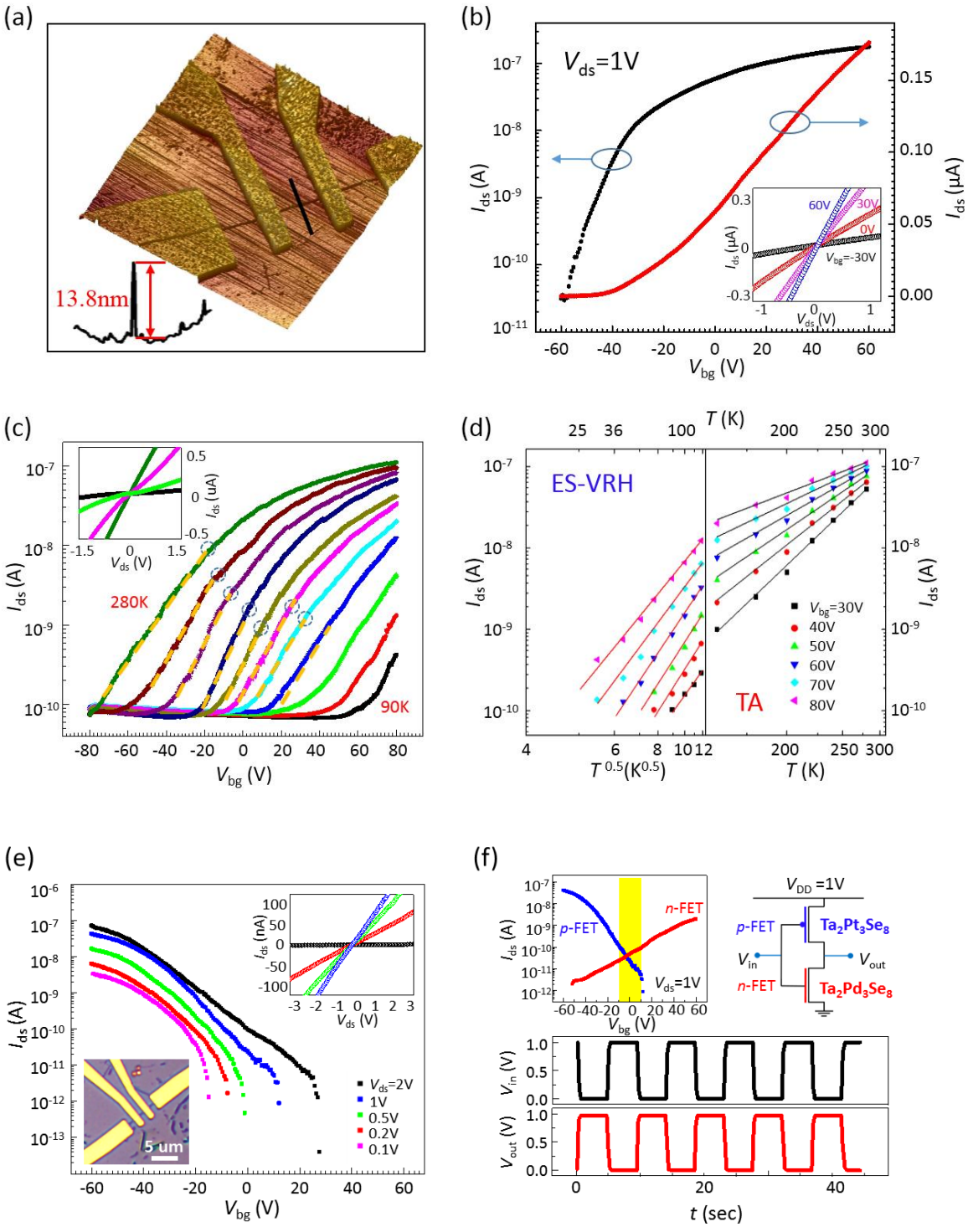
(a)
13.8nm
(b)
V_{ds}=1V
I_{ds} (A)
I_{ds} (μA)
V_{bg} (V)
60V
30V
0V
V_{bg}=-30V
V_{ds}(V)
(c)
280K
90K
I_{ds} (A)
V_{bg} (V)
I_{ds} (uA)
V_{ds} (V)
(d)
ES-VRH
TA
T (K)
$T^{0.5}$(K$^{0.5}$)
V_{bg}=30V
40V
50V
60V
70V
80V
(e)
I_{ds} (A)
V_{bg} (V)
I_{ds} (nA)
V_{ds} (V)
5 um
V_{ds}=2V
1V
0.5V
0.2V
0.1V
(f)
p-FET
n-FET
V_{ds}=1V
V_{bg} (V)
V_{DD} =1V
V_{in}
V_{out}
$Ta_2Pt_3Se_8$
$Ta_2Pd_3Se_8$
V_{in} (V)
V_{out} (V)
t (sec)

Figure 4 | Transport study of the exfoliated TPdS nanowires. (a) AFM image of a typical field-effect transistor fabricated based on TPdS nanowire with 13.8 nm thickness. (b) Transconductance for FET shown in (a) with gate sweeping from -60 V to 60 V at V_{ds}=1 V plotted both in linear (red dotted line) and logarithmic (black dotted line). Insert: I-V sweeps at different gate voltages (V_{bg}= -30, 0, 30 and 60 V). (c) Gate sweeps at different temperatures from 90 K to 280 K and fixed source drain bias V_{ds}=0.2 V. For each sweep, subthreshold region and threshold voltage is marked by dashed yellow lines and dotted circle respectively. Insert shows I-V sweeps at four different temperatures 90 K, 140 K, 180 K and 280 K with V_{bg}=60 V. The thickness of this specific device is 31 nm. (d) Temperature dependence of source drain current plotted in the scale of $(T^{0.5})^{-1}$ (below 140 K on the left side) and T^{-1} (above 140 K on the right side) with fixed gate voltages (30, 40, 50, 60, 70 and 80 V). Data of this plot (dots) is directly derived from (c). Two different mechanisms have been used to fit our data, ES-VRH at low temperature (red lines) and thermal activation (TA) at high temperature (black lines). (e) Room temperature transconductance for a FET fabricated with a 28-nm-thick TPtS nanowire with gate voltage sweeping from -60V to +60V at V_{ds}=2, 1, 0.5, 0.2 and 0.1V. Bottom left Insert: optical image of the device. Top right insert: I-V sweeps at different gate voltages, V_{bg}= -60V (blue), -20V (green), 20V (red) and 60V (black). (f) Top left: Room temperature transconductance for a p-type 18-nm-thick TPtS nanowire FET (blue dotted line) and an n-type 15-nm-thick TPdS nanowire FET (red dotted line). Top right: schematic drawing of the inverter circuit (NOT gate) built with the two FETs mentioned in (e). The gate voltage, ranging from -10V to +10V as highlighted in the top left figure of (e), serves as the input signal and the voltage at the connection point of both FETs acts as the output signal. Bottom: Measured input-output signal response for the inverter circuit.

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