A FREQUENCY CONVERTER TO POWER A SOUDRONIC VAA20 WELDING MACHINE

Prepared by: R. Jacques

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ABSTRACT

This thesis covers the design, manufacture and testing of a frequency converter, that transforms three phase AC 380V, into one phase AC 50 to 120Hz, 100 to 650V. The inverter output is intended to power a Soudronic VAA20 welding machine.

The input to the converter was stepped down and rectified to generate an unregulated DC bus of 250V. A full bridge transistorised inverter was controlled by a 6809 microprocessor that generated pulse width modulated waveforms to derive a desired inverter output current and frequency.

A base drive was developed to control the power transistor in the inverter. It facilitates the rapid switching of the transistors and provides them with overcurrent protection.

The inverter was originally constructed in push-pull configuration. At 20KVA this type of inverter was found to be undesirable, so a full bridge configuration was used in the final design. The converter has been installed and is operating successfully.

Many recommendations are made for the improvement of future converters. The changes will improve the operation of the converter and can also reduce the size, cost and weight of it.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

NOMENCLATURE

B	-	Transistor current Gain
BCD	-	Binary Coded Decimal
BJT	-	Bipolar Junction Transistor
EPROM	-	Erasable Programmable Read Only Memory
f_t	-	Frequency at which the Transistor Gain is Unity
IB	-	Transistor Base Current
IC	-	Integrated Circuit Chip
I_C	-	Transistor Collector Current
IGBT	-	Insulated Gate Bipolar Transistor
IH	-	Interrupt Handler
I_{pk}	-	Peak Current
I_{RMS}	-	RMS Current
$I_{RMS\ fb}$	-	Full Bridge RMS Current
$I_{RMS\ pp}$	-	Push-Pull RMS Current
JFET	-	Junction Field Effect Transistor
LED	-	Light Emitting Diode
MOSFET	-	Metal Oxide Silicone Field Effect Transistor
PCB	-	Printed Circuit Board
P_{cond}	-	Transistor Conduction Power Losses
Pfb	-	Power in the Full Bridge Inverter Windings
PIO	-	Parallel Input/Output
P_{off}	-	Switch Off Transistor Power Losses
P_{on}	-	Switch On Transistor Power Losses
Ppp	-	Power in the Push-Pull Inverter Windings
P_{tot}	-	Total Transistor Power Losses
PWM	-	Pulse Width Modulation
RAM	-	Random Access Memory
RC	-	Resistor Capacitor
RCD	-	Resistor Capacitor Diode

RMS	-	Root Mean Squared
$R_{th\ CH}$	-	Transistor Thermal Resistance Case to Heatsink
$R_{th\ JA}$	-	Transistor Thermal Resistance Junction to Ambient
$R_{th\ JC}$	-	Transistor Thermal Resistance Junction to Case
SKKD	-	Semikron Double Diode Power Module
t_d	-	Delay Time
t_f	-	Transistor Collector Current Fall Time
tj	-	Maximum Transistor Junction Temperature
t_s	-	Transistor Storage Time
V/F	-	Voltage/Frequency
V_{CBO}	-	Transistor Maximum permissible Collector Base Voltage (base open)
V_{CE}	-	Transistor Collector Emitter Voltage
$V_{CE\ SAT}$	-	Transistor on State Collector Emitter Voltage
V_{CEO}	-	Transistor Maximum permissible Collector Emitter Voltage (emitter open)
V_{CEX}	-	Transistor Maximum permissible Collector Emitter Voltage
VCO	-	Voltage Controlled oscillator
V_{pk}	-	Peak Voltage
V_{RMS}	-	RMS Voltage

CHAPTER 1

INTRODUCTION

The aim of this thesis is to design and construct a frequency converter, for the purpose of supplying power to a tin can welding machine, in order to facilitate its faster operation. The welding machine is a Soudronic VAA 20. This welder is the main component in a production line that manufactures pressurised deodorant cans. The can production rate is limited by the 50Hz mains frequency.

The convertor modifies the three phase, 380V, 50Hz, to one phase, 600V, 120Hz. This higher frequency is used to power the Soudronic so that the can production rate can be doubled. It is not only necessary to increase the voltage and frequency, but the voltage must also cycle through three different levels per can.

The converter consists of a three phase rectifier, a full bridge transistor inverter, a computer controller and the power transistor drivers.

An existing alternative method of increasing the frequency to the Soudronic is available. Other welding machines use "motor-generator sets" that have a controlled DC motor on the same shaft as a single phase generator. A motor-generator set is expensive and requires constant maintenance. A solid state converter offers low maintenance and does not cost as much as the existing motor-generator sets.

The converter was ordered by Carnaud in Spain, from Metal Box S.A. MLT Drives, who financed the project, was contracted to manufacture the converter. The project was started in March 1988. By June 1988 a converter with a push-pull inverter, using a DC bus voltage of 125V, was completed. The design was subsequently modified to a 250V full bridge inverter. The project was finally completed in April 1990 and the converter has been operational in Carnaud, Spain, since October 1990.

CHAPTER 2

THE WELDER AND ITS POWER REQUIREMENTS

The converter is used to supply the power to a Soudronic VAA 20 welding machine. The speed at which the welding machine operates is limited by the frequency of the mains supply. The converter changes the frequency of the welding current from 50 Hz to 120 Hz. This enables the speed of the welding machine to be increased. When the frequency is increased, the voltage and power must also be raised according to certain requirements.

The discussion on the welder has been divided into two sections, first the Soudronic operation and then the Frequency converter specifications. The discussion on the Soudronic welder is only necessary to give an understanding of the specifications and operation of the converter. The section on the converter specifications gives the general electrical requirements for the inverter, that were set out before the project began, or that were added during the project.

2.1 THE SOUDRONIC VAA 20 WELDING MACHINE

The Soudronic VAA 20 is a tin can welding machine. The machine welds the can on the seam along the length of the can. The type of cans that are welded by the Soudronic are pressurised deodorant cans. The welder must therefore produce a consistently good weld along the entire length of the can otherwise the can might leak. Different types of cans have a variety of lengths and metal thickness'.

2.1 1 The welding operation

The can enters the welding machine as a flat, rectangular sheet of metal. The sheet is bent in a circle to form a tube. A diagram of a folded metal sheet can be seen in figure 2.1.

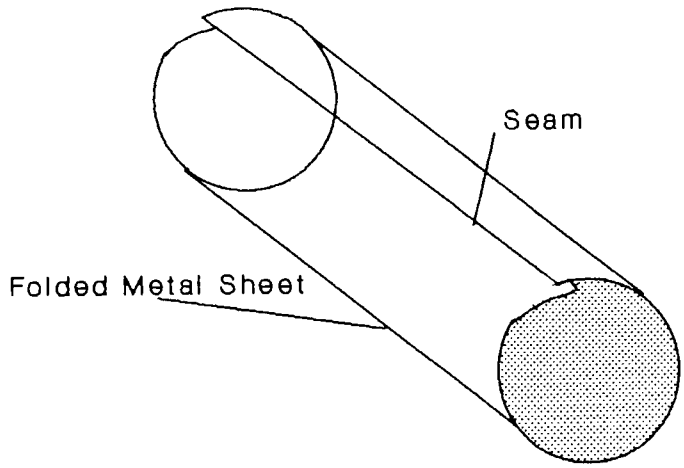


Figure 2.1 The unwelded can

A pair of "pincher" rollers pull the can through the machine along the seam. The rollers pass a current in the order of a few thousand amps through the seam of the can. This high current melts the metal and causes the two surfaces of the can to bond and form a weld. A diagram of how the can is pulled through the machine can be seen in figure 2.2.

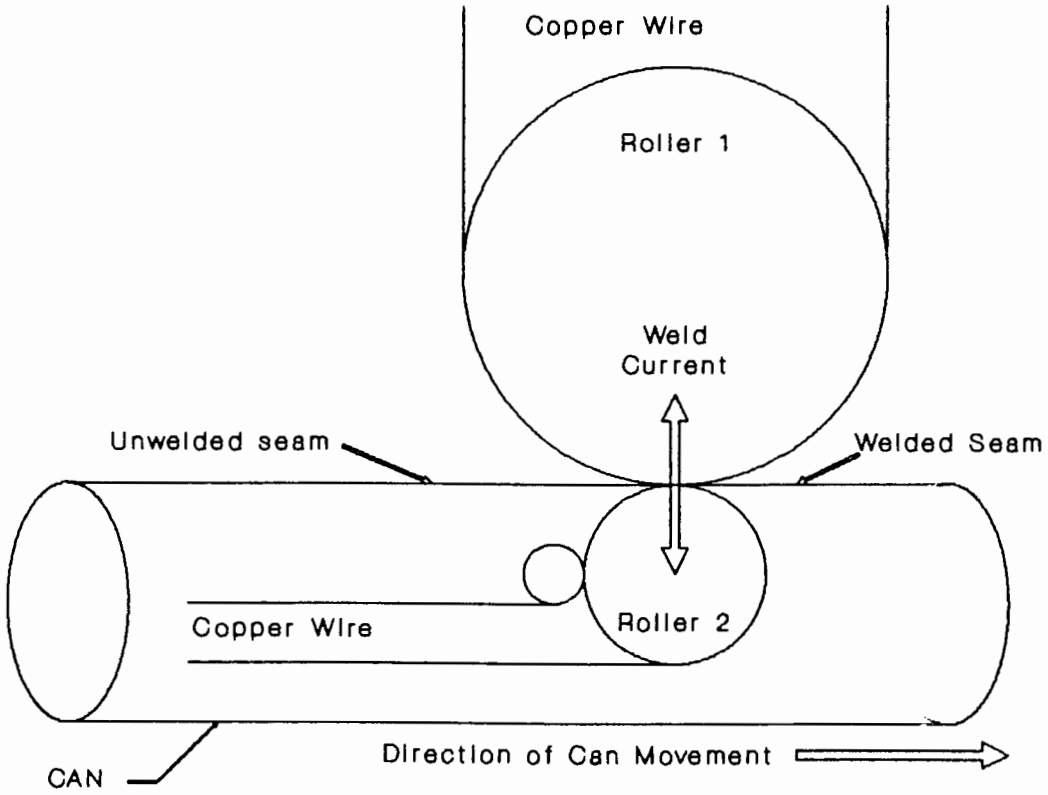


Figure 2.2 The can in between the welding rollers

A constant flow of chilled water is pumped through the rollers. This removes the heat that is generated during the welding process. The water is chilled to approximately $4^{o}C$. If the water temperature rises above $14^{o}C$, or if water flow ceases, the Soudronic will switch off.

2.1.2 Power to the Soudronic

The input to the welder requires a single phase supply. The single phase is used to power a step-down transformer. On the output of the step-down transformer there is a low voltage winding that supplies the 5000 Amp welding current.

The input to the Soudronic is supplied either by a single phase thyristor phase angle control unit (under normal operation), or by a frequency converter. A switch was added to the Soudronic to select between the two power

sources. A diagram showing this can be seen in figure 2.3.

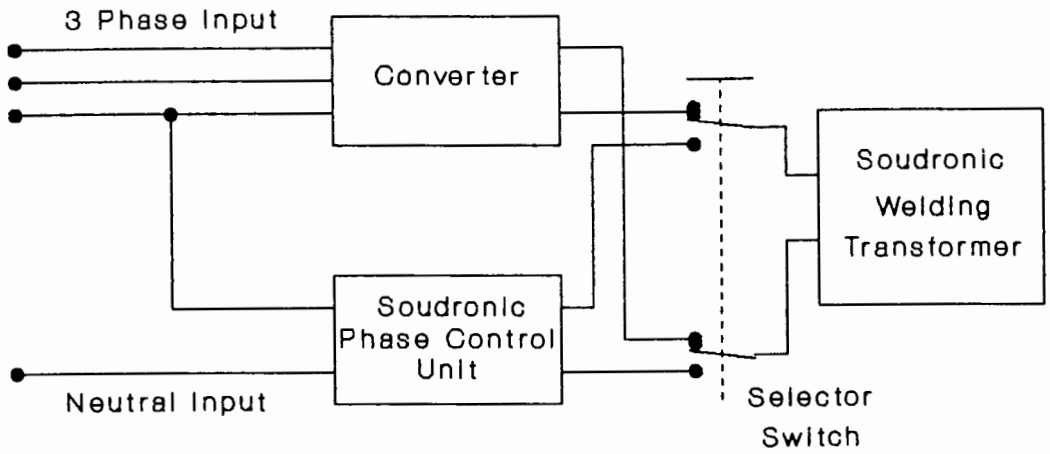


Figure 2.3 Input Power selection to the Soudronic.

Under normal operation, the welding current is phase controlled on the primary of the step down transformer. When used with the converter, the phase controller is bypassed and the output of the converter is fed directly into the step-down transformer.

2.1.3 The voltage cycles

During the welding process, heat is being transferred away from the weld in all directions (360^{o}). This cools the weld down. At the start and at the end of a can, heat transfers through 180^{o}. The welding current must therefore be reduced, to prevent the edges of the can from overheating and burning. To reduce the welding current the inverter must decrease the voltage.

There is a small time between consecutive cans when there is no can between the rollers. Also, when a malfunction occurs during the bending of a can for example, there is a long interval when there is no can between the rollers. In the absence of a can, the resistance between the rollers decreases and welding current increases. This is wasteful, as energy is dissipated in the inverter, the welding transformer and the rollers. Hence, if the can is

not between the rollers, the welding current should be inhibited.

The welding cycle therefore has four stages: reduced weld at the start of a can (can-start); normal weld for the length of a can (full-weld); reduced weld at the end of a can (can-end); and no-weld when there is no can. A profile of welding current versus time (can length), can be seen in figure 2.4.

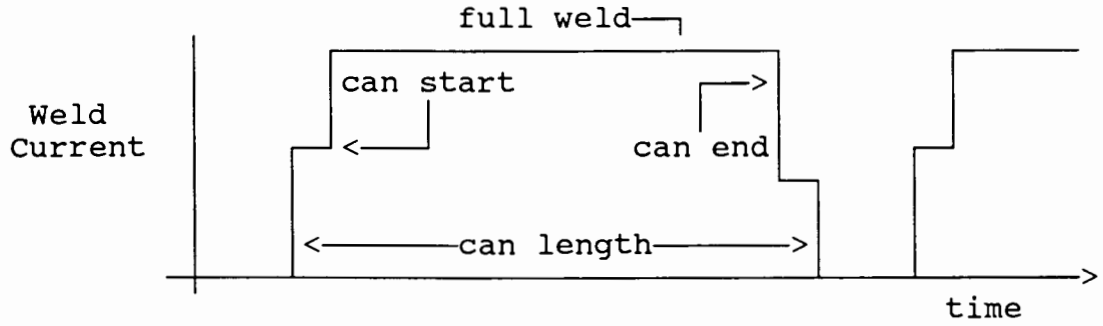


Figure 2.4 Graph of welding current versus time

2.1.4 Signals from the welder to the Converter

The signals for the various welding stages are derived from an optical sensor that is able to sense the position of the can. The output of the optical sensor is decoded to give four output codes, on three separate connections. Each connection can be in one of two states, either high (10mA), or low (0mA). Each connection represents a welding stage, either can-start, full-weld, or can-end. If a high is present on one of these connections, then the appropriate weld state is required. When the no-weld stage is required, all three outputs go high. A truth table of the logic states is shown in table 2.5.

OUTPUT STATE	INPUT CONNECTION NUMBER		
	1	2	3
Can-start	1	0	0
Full Weld	0	1	0
Can-end	0	0	1
No Weld	1	1	1
Same as previous state	All other possible combinations		

Table 2.5 Truth table of the logic states from the Soudronic

The pincher rollers do not weld the can. A copper wire that runs over the rollers, is in contact with the can. This wire is rectangular so that there are two large, flat surfaces that can weld the can. The copper wire runs constantly at the same speed as the can. Each side of the wire comes into contact with the can only once, as the wire deforms due to the heat of the weld.

Occasionally this wire breaks due to a defect in either the copper or an adjustment problem in the Soudronic. If the wire breaks, the rollers come into contact with the can to perform the weld. This causes excessive wear on the rollers. There is an emergency button on the Soudronic that inhibits the welding current even if the optical sensors sense a can between the rollers. A normally open relay connection, carrying 220V AC is used to signal to the converter to inhibit the welding current.

2.1.5 The welding frequency

The can is welded using Alternating Current. During each cycle, there are two points at which no current flows (the zero's of the current sine wave). At these zero's, the area that is being welded, cools down. There are also two current peaks, one positive and one negative. When a peak current flows the area being welded is very hot and a firm

weld results. As the can is being pulled between the rollers there are areas of hot and cold weld. The areas of hot weld that have a cold weld on either side are called nuggets. The nuggets form when current peaks pass through the weld, which occurs twice per AC cycle. Under normal operation, the welder uses 50Hz, which leaves 100 nuggets per second.

If the speed with which the can moves through the rollers is increased, the nuggets become more spaced out. These areas between the nuggets can be too cold to perform a correct weld and holes in the weld can occur. This is obviously unacceptable, hence a minimum number of nuggets per length of weld are specified. As an example, for a specific length of can it might be sufficient to have 100 nuggets down the length of the can. This means that the can will take one second to weld. This factor limits the production rate of the Soudronic welding machine.

The frequency converter is designed to allow the Soudronic welder to increase in speed by a factor of two. If the time the can spends in the welder is reduced to 0.5 seconds, the number of nuggets per can must remain at 100. To obtain 100 nuggets per 0.5 seconds, the welding current frequency must be increased to 100Hz. Thus, if the can production rate is to be doubled, the welding current frequency must be increased from 50Hz to a minimum of 100Hz.

The welding current must be precise, otherwise the weld may either be hot or cold. A hot weld occurs when there is too much current and the weld burns. A cold weld occurs when there is not enough current and the seam does not seal properly. Both types of fault weaken the weld to an extent that the can may rupture when under pressure. The welding current must therefore be constant for the entire length of the full weld and must also be constant from can to can.

2.2 THE CONVERTER SPECIFICATIONS

The converter specifications were written by Metal Box SA (Pty) Ltd for MLT Drives CC. Metal Box engineers based the specifications on their knowledge of the Soudronic welder, but there was an understanding by both parties that the specifications were liable to change slightly during the design. The specifications given in this section are the final specifications that the converter complied with.

2.2.1 Frequency

In section 2.1.4 it was stated that the welding current frequency should be a minimum of 100Hz. If the nuggets are close together, the areas of cold weld between the nuggets become small and can even disappear if the nuggets are very close together. This results in a superior weld. The upper frequency limit was set at 120Hz, so that the converter would give a superior weld even at the increased production rate. It was specified that the frequency should be controllable from 50Hz to 120Hz.

2.2.2 Voltage and Power

The output power requirement of the inverter was set at 20KVA. The power factor was not specified . This caused problems during the design as the power factor was determined to be approximately 0.6 lagging. The output voltage range was specified to be variable between 200V and 700V AC, single phase. The input voltage was specified as 3 phase, 380V.

2.2.3 Settings

The voltage and frequency settings were to be set via dials on the front panel. The frequency dial ranges from 0 to 9, and the voltage dials ranges from 00 to 99. The three voltage settings for can-start, full-weld and can-end had to be independent of each other, all having a

range from 00 to 99. The front panel was also to have indications of the converter output current and output voltage, one phase of input current and the DC bus voltage.

The four states, no-weld, can-start, full-weld and can-end were to be derived from three wires carrying 10mA for an "on" state and 0mA for an "off" state . For no weld, all inputs were high. The signals had to be isolated from the electronics of the converter by means of optical isolators. A fourth wire, the negative return for the three signals, was also supplied. A further input, to inhibit the welding current in the case of an emergency was also supplied. This was a 0 / 220V signal intended to power the coil of a relay.

2.2.4 Voltage and Frequency stability

No specifications were given for the voltage and frequency stability. It was understood that the output was derived by means of pulse width modulation to simulate a sine wave current. No specifications were given as to the harmonic content of the sine wave. It was understood that the pulse width modulation was to be derived from a computer that is crystal controlled.

CHAPTER 3

THE COMPLETE CONVERTER

This chapter provides the reader with an overall view of the converter, to ease the understanding of the purpose and function of each element. The physical layout of each component in the converter is discussed. The design stages and testing procedures are also noted.

3.1 AN OVERALL VIEW

The converter consists of four major components. They are: the input rectifier, the inverter, the control electronics and the base drive. A block diagram of the complete converter and its control can be seen in figure 3.1 The solid black lines represent the main power flow and the hollow lines represent signal flows.

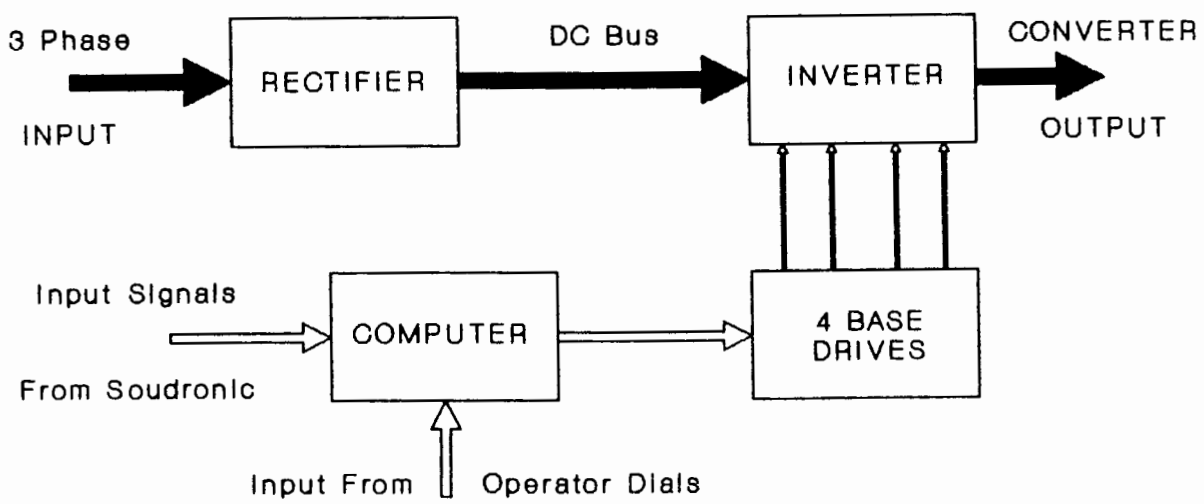


Figure 3.1 The Complete Converter

The input rectifier is an isolated 25KVA, 250V DC power supply. It converts the input 50HZ, three phase AC into DC. It supplies the main power to the inverter. The DC supply is not controlled, but is an unregulated diode rectifier. It is a 6 phase, 12 pulse bridge, with a voltage ripple of approximately 5%. The rectifier is discussed in chapter 5.

The inverter converts the 250V DC back to AC, with a frequency ranging from 50HZ to 120HZ. The inverter is controlled by a sine-weighted Pulse Width Modulation (PWM) to regulate the voltage on the output of the inverter. The final inverter design was in a full bridge configuration. The output of the inverter drives a transformer that steps the voltage up to between 200 and 700V AC. The inverter is discussed in great depth in chapter 4.

The PWM signal that is used to control the power transistors is generated by a computer. The computer controls the shape of the PWM (level of modulation), according to voltage and frequency settings that are made by the operator of the Soudronic. The computer interprets isolated inputs from the Soudronic, as well as the dials set by the operator, to give an appropriate PWM to the transistors. The computer controller is discussed separately in chapter 7.

The circuit that converts the computer logic signal, to a power signal that is able to control the power Darlington transistors of the inverter, is called a base drive. A base drive isolates each transistor from the computer and increases the current of the signal. It also provides the transistor with protection and the requirements for it to perform correctly. The base drive is discussed in great depth in chapter 6.

3.2 THE MECHANICAL ASSEMBLY

The converter was constructed inside a steel cabinet. This cabinet was divided horizontally in the middle. All the magnetic components (the transformers and the choke) were mounted in the lower half. The top section was reserved for the electronic components, e.g. the power transistors, the base drives and the computer. A photograph taken from the rear of the converter is shown in figure 3.2. Note that the doors are open for the photograph and a cover is over the computer controller. The converter is approximately 2 meters high.

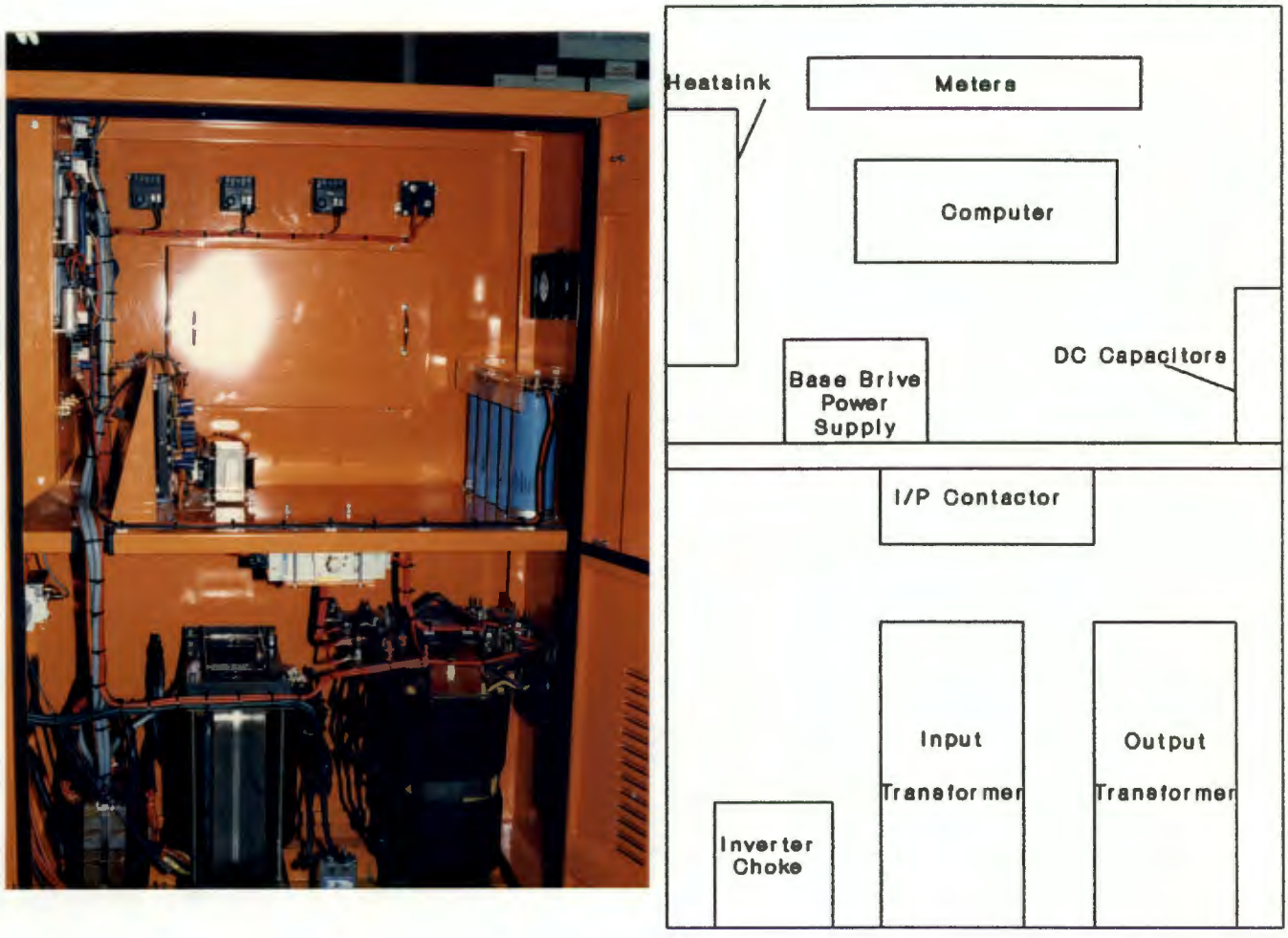


Figure 3.2 Photograph and diagram of the converter.

The transformers are separated from the electronics to reduce eletromagnetic interference in the electronics. The computer is housed in a steel and aluminium compartment to reduce interference that could be generated

by any of the power components in the upper section. The paths and positioning of the wiring is a very important aspect of designing a power electronic machine [1]. Notes on wiring, that were adhered to during the design, can be found in Appendix I.

On the front of the converter there are voltage and current meters to monitor the power through the converter. Also on the front are the dials to adjust the voltage and frequency settings of the inverter. A photograph and a diagram of the front of the converter is shown in figure 3.3.

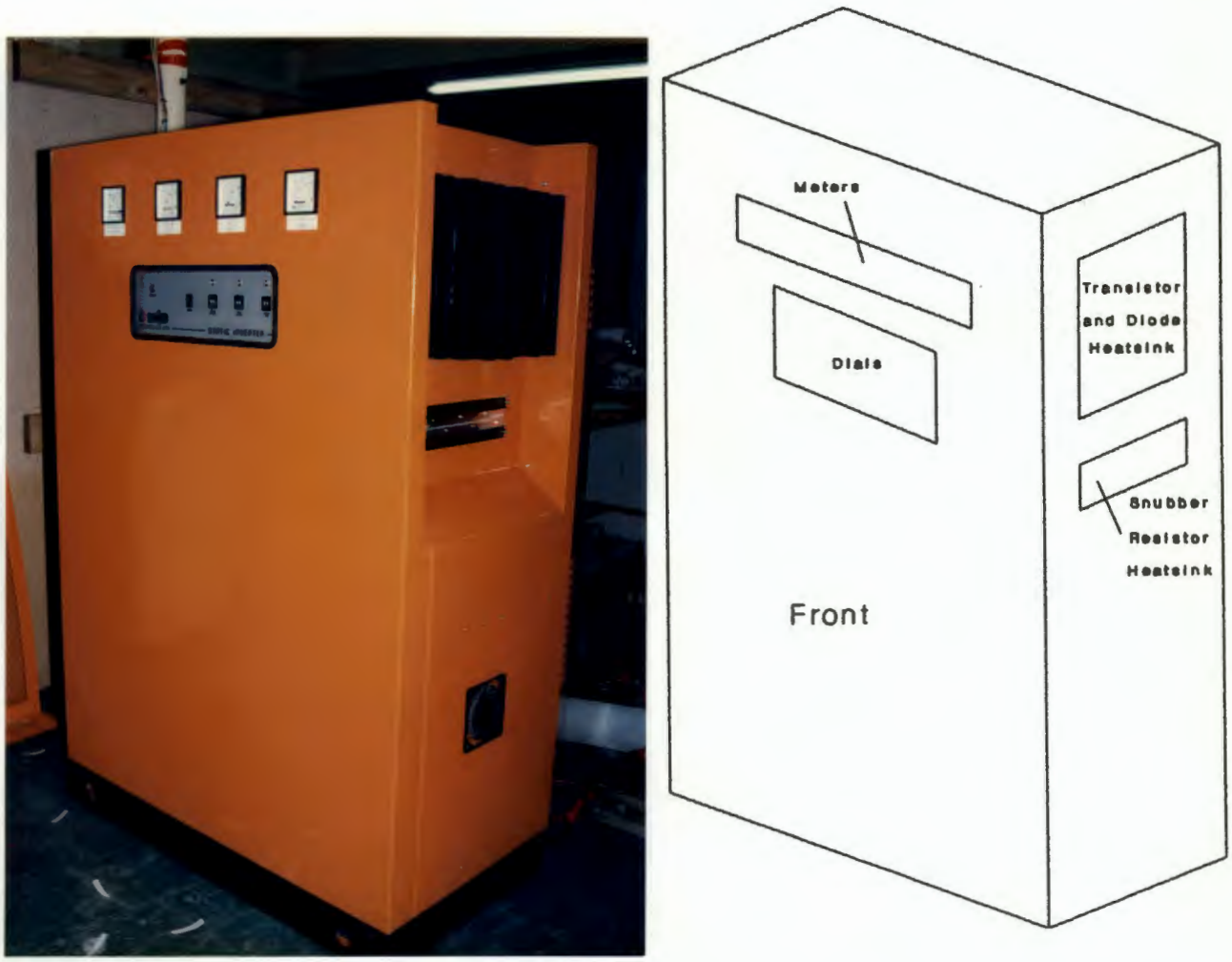
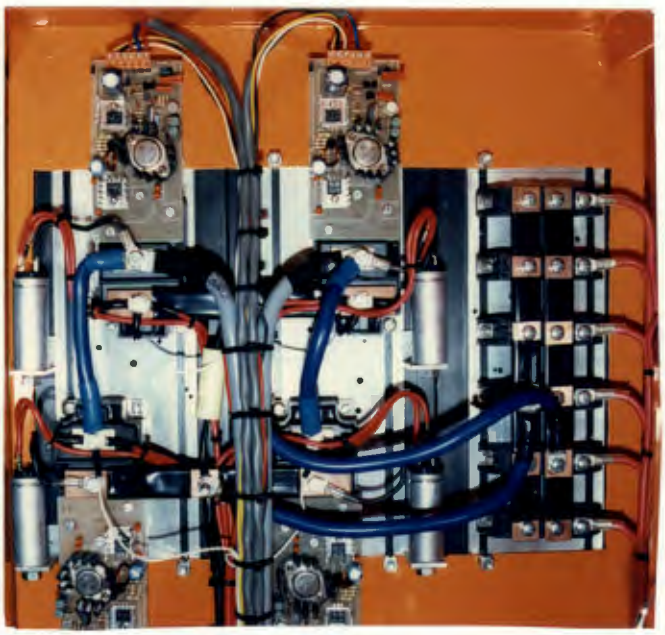


Figure 3.3 Photograph and diagram of the front of the converter

In figure 3.3 it can be seen that the heatsinks are mounted outside the cabinet. This was done to aid the cooling of the heatsink on which the transistors and

diodes are mounted. The chilled water that is pumped into the Soudronic is also used to cool the heatsinks. The water pipe is connected to the converter heatsinks, in series with the Soudronic.

The power transistors and rectifier diodes are mounted on three separate water-cooled heatsinks. It is not necessary to watercool the snubber resistor heatsink. A photograph and a diagram of the components mounted on the water-cooled heatsink can be seen in figure 3.4.



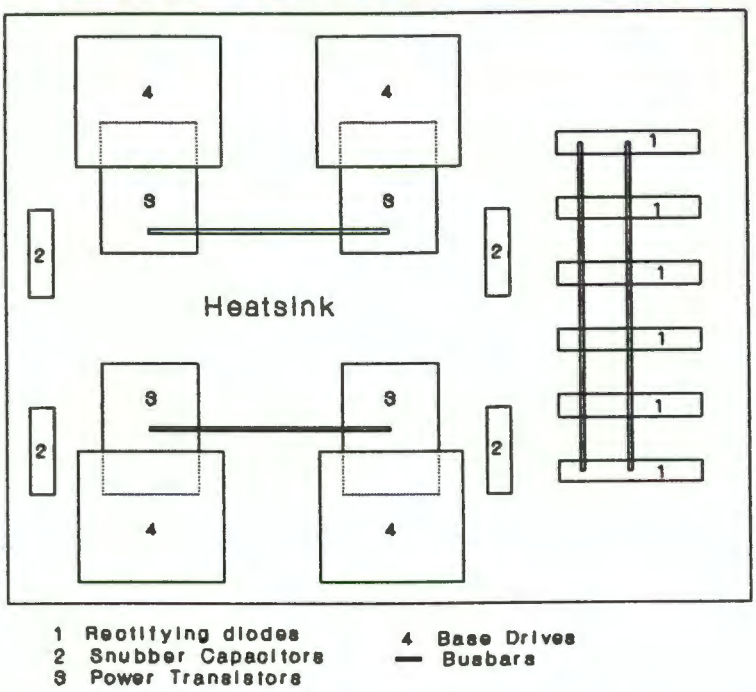


Figure 3.4 Photograph and diagram of the components on the heatsink

the transistor drivers. This was found to be an incorrect assumption and that the transistor drivers had to be isolated. The fundamental differences between the push-pull and full bridge inverters are listed in table 4.8.

Push-Pull	Full Bridge
needs only 2 transistors	needs 4 transistors
transistor carries twice current of Full Bridge	transistor carries half the current of Push-Pull
High voltage overshoots	Low voltage overshoots
Bad transformer utilisation	Good transformer utilisation

Table 4.8 Differences between the Push-Pull and Full Bridge Inverters

In a full bridge inverter, if a transistor is on when it should be off, a path from the positive rail to the negative rail could exist. The path would be through two transistors in the same leg, if they were both on at the same time. This is called a shoot-through. In the event of a shoot-through, current will rise rapidly, which could result in the destruction of the transistors. A shoot-through could occur when a transistor is falsely triggered on, or when it does not switch off as rapidly as it should. A shoot-through is not possible with a push-pull inverter.

4.4 SNUBBER NETWORKS

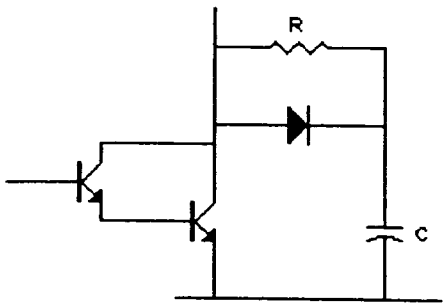
Snubber networks perform two fundamental tasks; a) to reduce switching losses and b) to keep the voltage overshoot to a minimum. Snubber networks can either assist the turn-off or the turn-on. The turn-on of a Darlington transistor is rapid, but the turn-off is slow [4]. The turn on time of the AEG transistor was found to be approximately 2us and the turn-off time approximately

20us. The switch-on losses are thus in the order of 10 times less than the switch-off losses. For this reason, no switch-on snubber was used.

4.4.1 The RCD Snubber

The switch off assisting snubber that was used for both the push-pull and the full bridge inverter was the conventional RCD snubber. The snubber component calculations[1] can be found in Appendix B. To calculate the snubber capacitance value, the peak collector current immediately prior to turn-off and the rate of voltage rise need to be known. The resistor value is calculated according to the resistor-capacitor (RC) discharge time constant. The references [3,5,6] all recommend different discharge times, ranging from 0.7 to 0.25 times the minimum on state time.

It is obviously impractical for sine weighted pulse width modulation, to base the snubber design on the minimum on state time, as the pulse widths become very small. Fortunately, the small pulse widths occur during the portion of the sine wave when the transistor does not carry the worst case current value. This means that a value for the minimum pulse duration must be approximated. A diagram of the RCD snubber circuit and its component values is given in figure 4.9.



COMPONENT	PUSH PULL	FULL BRIDGE
C1	2.5uF	1uF
R1	23 Ohms	47 Ohms

Figure 4.9 RCD Snubber for the Push-Pull and Full Bridge inverters

1 - References 3, 5 and 6 assisted with the snubber design.

4.4.2 DC Bus capacitors

A range of capacitors were used on the DC bus to remove oscillations that arose because of parasitic inductances in the wiring of the inverter. The push-pull inverter used a bank of 10x4700uf electrolytic capacitors to remove these oscillations. The high frequency oscillations were only slightly reduced.

The full bridge inverter used a bank of 6x3600uf electrolytic capacitors, one 50uf polyester capacitor and one 1uf polypropolene capacitor to remove the oscillations. Each type of capacitor has a different frequency response. By using the three types, nearly all the oscillations on the DC bus were removed.

4.4.3 Additional Snubbers used in the Push-Pull Inverter

The full bridge inverter required only the RCD snubber on each transistor and the DC bus capacitors to limit the voltage overshoot. The push-pull inverter did not only have the simple RCD snubber, but two other snubbers as well. These snubbers are shown in figure 4.10.

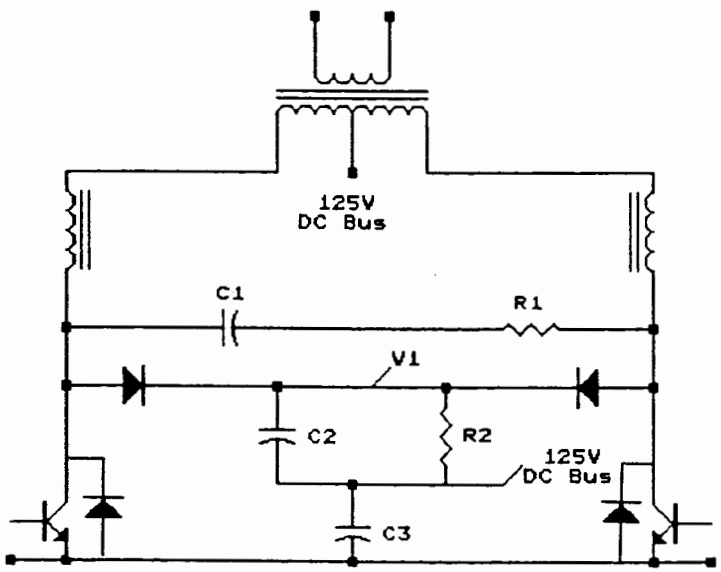


Figure 4.10 The additional push-pull snubbers

The snubber[2] that consists of R1 and C1 is small and has little effect on the switching. When a transistor switches off, the rate of voltage rise is limited by the discharging of the capacitor (C1). The capacitor is charged up again when the other transistor switches on. The resistor limits the current into the capacitor. This snubber has the same effect for both transistors.

The second snubber removes the voltage overshoot only[3]. C3 is constantly charged up to the DC bus voltage. C3 removes oscillations that are present on the DC bus. In a push-pull configuration the collector voltage of the transistor that is off is twice that of the DC bus. The lowest voltage across C2, during the inverter operation is thus equal to the DC bus voltage. The lowest voltage measured at V1 is therefore twice the DC bus voltage. If a voltage overshoot occurs on either transistor, C2 charges up and limits the rate of voltage rise. R2 discharges capacitor C2 back to the DC bus level. A diagram of the voltages in the snubber is shown in figure 4.11

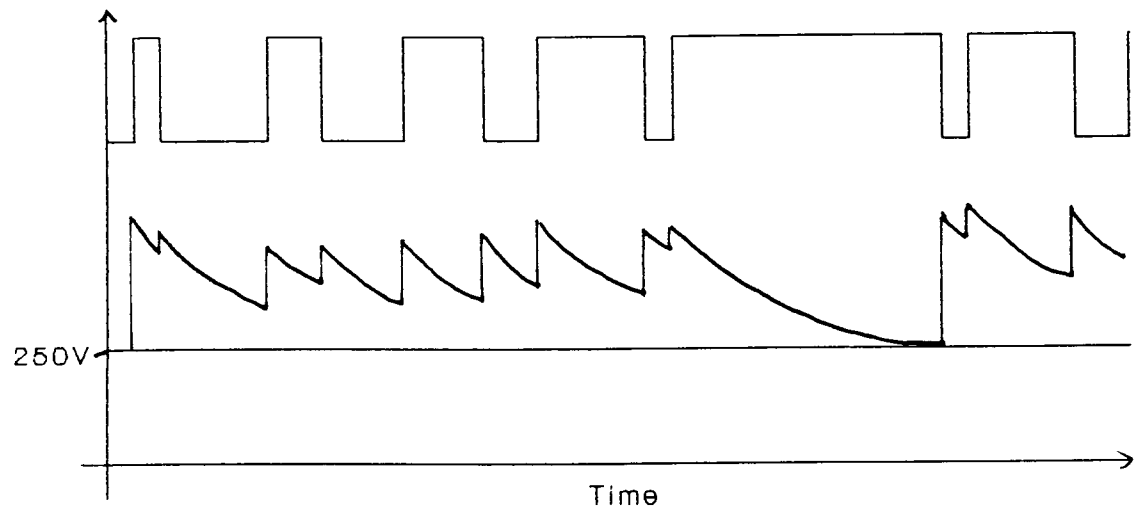


Figure 4.11 Voltages in the Snubber
a) Voltage on the collector of a Transistor
b) Voltage between point V1 and 0V[4]

2 - This snubber is suggested by Chopra [7].
3 - Similar "spike removers" are dealt with in Bosterling [8].
4 - Note that the DC bus is only 125V, but the voltage that appears across each transistor is twice this, because of the effect of the push-pull transformer.

The full circuit diagrams of the inverters with their snubbers are in Appendix C.

4.5 INVERTER SWITCHING CURVES

This section gives graphs of current and voltage waveforms of readings taken from various converters.

4.5.1 Validity of Results

Graphs and measurements were taken at various stages during the design process. The curves that are presented in this dissertation have been obtained from two different oscilloscopes. A Gould digital storage oscilloscope was borrowed from Metal Box to obtain graphs of the push-pull and full bridge converters. These graphs were not detailed enough to observe the transistor switching times though.

Further curves were obtained using a Iwatsu DMS 6430 oscilloscope and a Technicorder Type 3077 plotter. These graphs show the curves of 10KVA Uninterruptable Power Supply (UPS), not one of the converters. The UPS inverter is in a full bridge configuration, with a DC Bus of 250V, as in the final converter design. The power in the UPS is half that of the converters. AEG 150A, 600V power transistors were driven by the same base drive as in the final converter. The curves are thus the same in the UPS as for the converter, except that they are half the magnitude of the converter currents.

The Gould oscilloscope has a maximum sampling rate of 100M samples per second, which gives a maximum frequency of 50MHz, thus showing curves as dots with 10ns spacing. A plotter is built into the oscilloscope, so the printed graphs are a true reproduction of the data that was captured.

The same level of definition was not obtained from the Iwatsu-Technicorder system however. The Iwatsu oscilloscope has a maximum sampling rate of 1M sample per second, thus showing levels (dots) with 1us spacing. It is therefore difficult to measure switching times with this oscilloscope. The plotter adds further inaccuracies to the printed waveforms, as the plotter response is slow and straight vertical lines appear either curved or sloped.

The curves produced by the Iwatsu oscilloscope were varified with a Nicolet Model 204-A storage oscilloscope that samples at 20 Msamples/second, or 1 dot per 50ns. It was not possible to obtain a printout of the graphs from the Nicolet. Where the output of the Technicorder plotter differs widely from the readings taken from the Nicolet, comments are made in the text.

4.5.2 Inverter PWM Waveforms

The output of the inverter is a pulse width modulated approximation of a sine wave. The graphs shown in this section were taken from the 10 KVA UPS and printed by the Technicorder plotter.

For the two graphs in figures 4.12 and 4.13, the upper trace shows the inverter current and the lower trace represents the voltage across the inverter transformer primary and its series inductor. The voltage trace in the graphs is distorted due to the plotter. The vertical lines should be straight and not sloped as they appear. Also the voltage spikes on the rising edge have been removed by the platter.

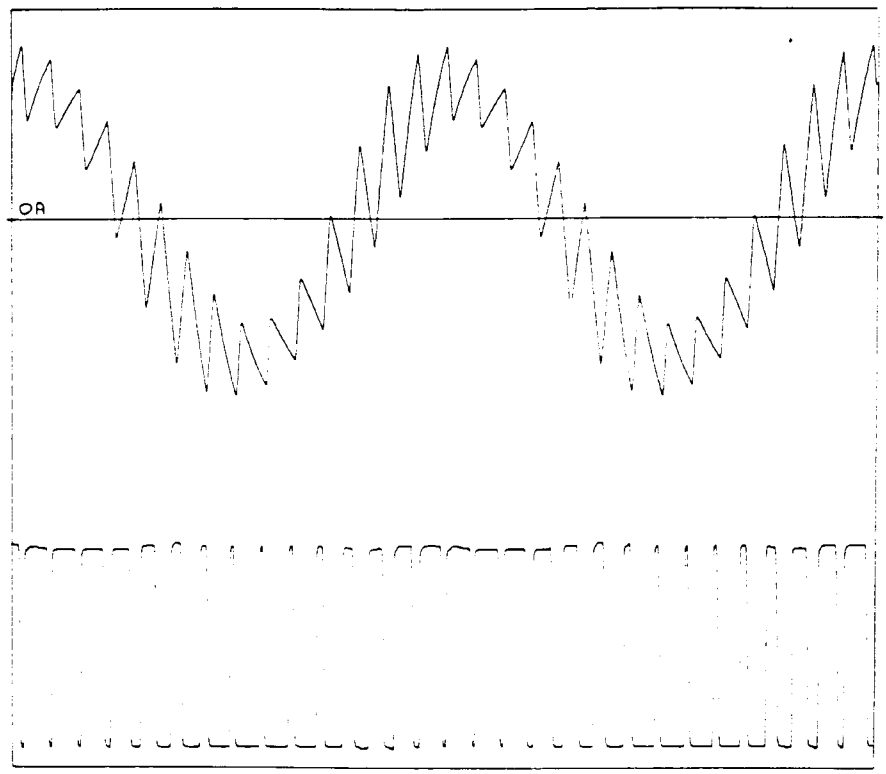


Figure 4.12 Inverter current and voltage (Table 25)

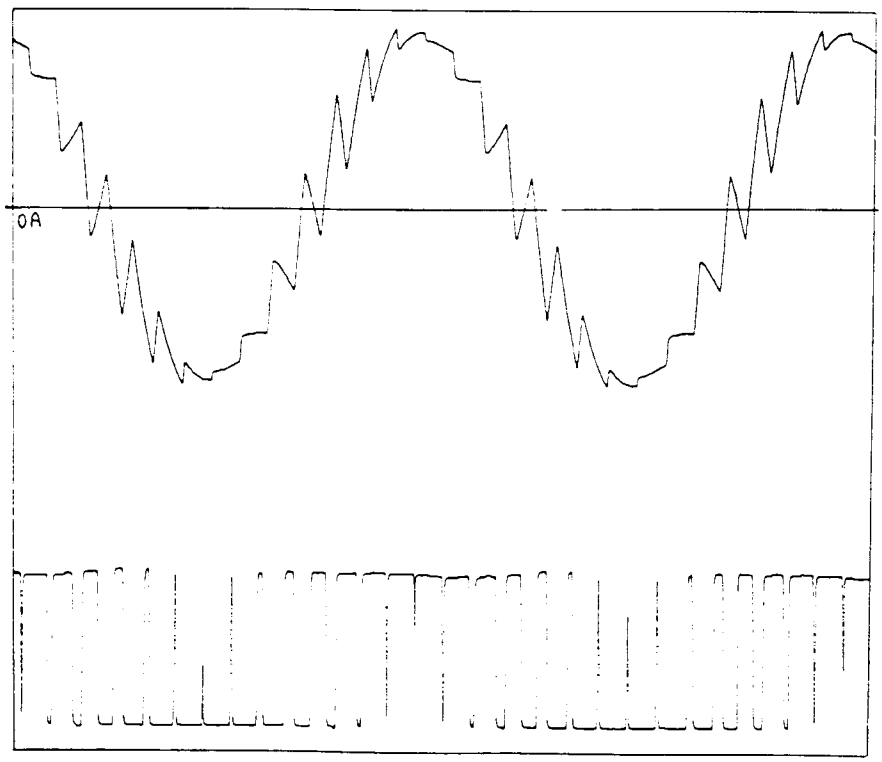


Figure 4.13 Inverter current and voltage (Table 45)

In figure 4.12, the modulation factor is approximately 0.45, which represents table number 23 in the converter. With this PWM the UPS was delivering 5KVA (half full

load). The ripple current is high, but the UPS has a resonant filter on the output that reduces this ripple. The converter does not have any filtering except for the current filtering of the series inductance.

Figure 4.13 shows the UPS delivering full load (10KVA) with a modulation factor of 0.95 or table 47 for the converter. The UPS was tested on resistive load, which is the reason for the current waveform rounding at the peaks. For the converter, the load is very inductive, so the rounding of the peaks would not be as apparent.

4.5.3 Push-pull inverter switching waveforms

As has been stated earlier, the push-pull inverter configuration was not used in the final design. This section shows two graphs that motivate the reasons why the push-pull inverter design was not used. Both were taken with the Gould oscilloscope.

The graph in figure 4.14 shows the collector emitter voltage as the transistor turns-off. Oscillations appear across the transistor. The initial peak reaches 575V and is 15us wide. This peak is obviously too high for a transistor with a V_{CEO} rating of 550V, but is acceptable for the higher voltage transistors with a V_{CEO} rating of 880V.

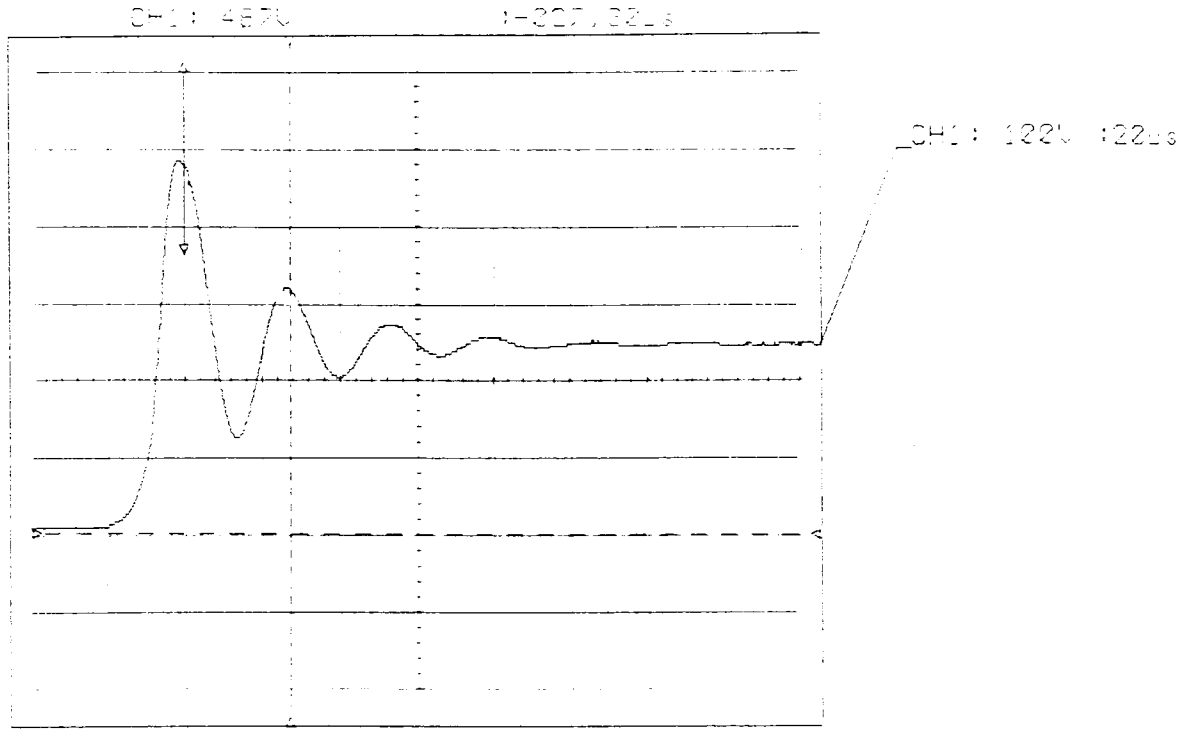


Figure 4.14 Collector emitter voltage of a push-pull transistor

Figure 4.15 shows the voltage across the RDC snubber capacitor. The peak voltage reaches 500V, just below the voltage of the transistor's collector emitter voltage. It is important to note that the capacitor is fully discharged when a large voltage spike occurs, as at point 1. At point 2, the capacitor is not fully discharged but the voltage spike is small.

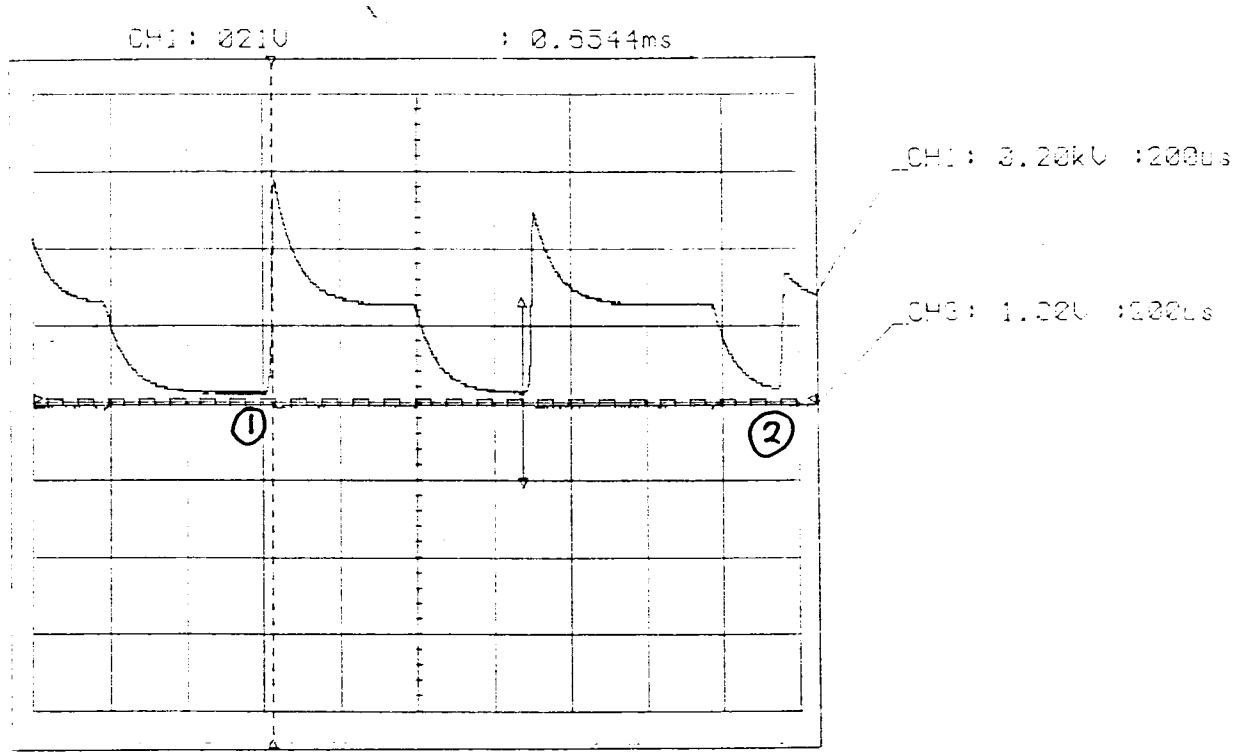


Figure 4.15 Snubber Capacitor Voltage

4.5.4 Full Bridge Switching Waveforms

All the graphs on this section were taken from the 10KVA UPS using the Iwatsu oscilloscope. The traces were all obtained at full load and at the peak of the sine wave, which is the worst case.

4.5.4.1 PWM waveform in the power transistor

The graph in figure 4.16 shows the current in the power transistor and associated free-wheeling diode (upper trace), and the same transistor's collector emitter voltage (lower trace). The current that appears above the zero line was conducted by the transistor and below the line was freewheeled by the diode[5]. The DC bus voltage was reduced so that the UPS would increase the modulation factor to maintain a constant output voltage. A modulation factor of 1.2 (table 60) can be seen. It should again be stated that the rounding effect at the current peak is due to the resistive load.

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5 - Note that the spikes on the rising edges have been rounded off by the plotter and also the current in the free-wheeling diode had been clipped by the oscilloscope.

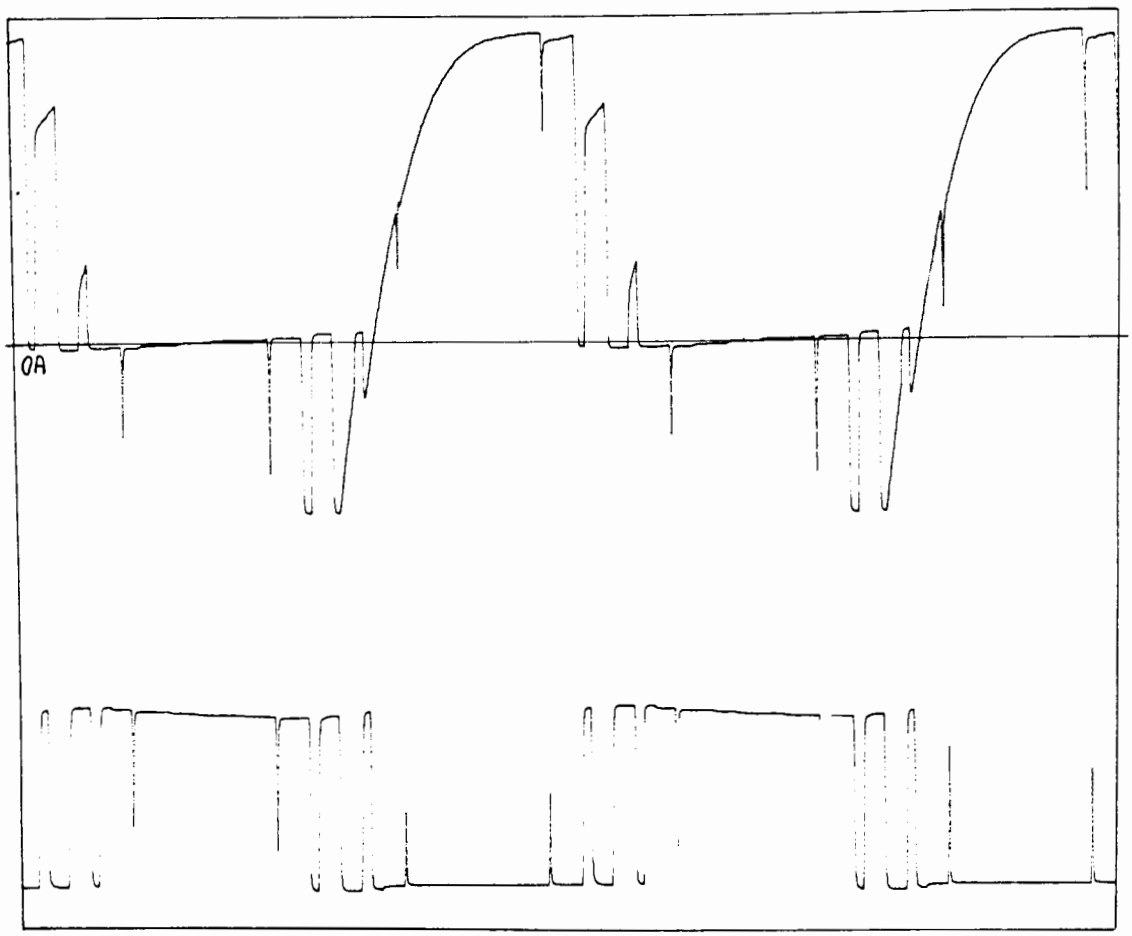

Figure 4.16 I_C and V_{CE} of a Power Transistor

4.5.4.2 Transistor Turn-On

Figure 4.17 shows an expanded view of the collector current (upper trace) and the collector voltage (lower trace) when the transistor turns on. Each step in the digital waveform is 1us long, and the total trace length is 60us. This time scale applies to all the remaining graphs in section 4.5.4.

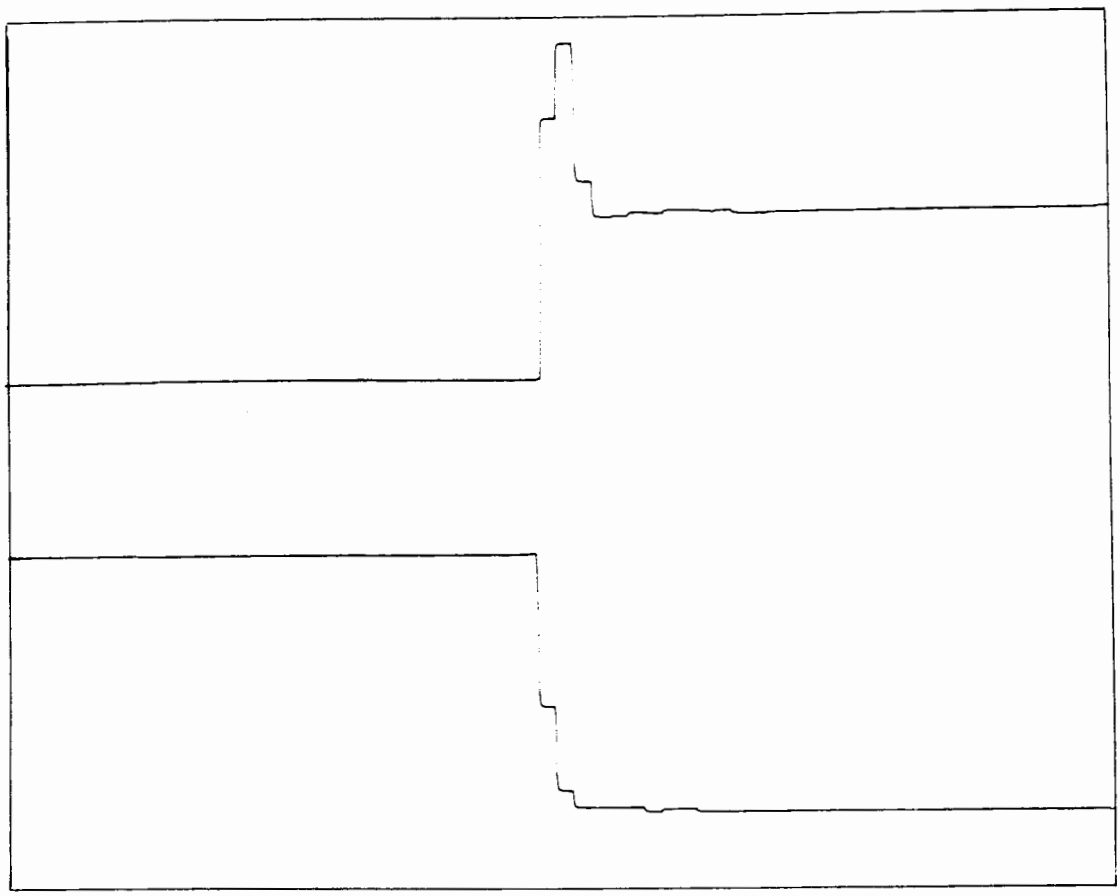

Figure 4.17 I_C and V_{CE} at switch-on

As the transistor switches on[6] a current overshoot occurs. This overshoot is 70 Amps above the 70 Amps of continuous current. The discharging of the snubber capacitor through the snubber resistor is partially responsible for the current spike.

When the transistor switches on after the free wheeling diode of the other transistor in the same leg has been conducting, a short shoot-through occurs. A diagram of the shoot through path is shown in fig 4.18. This shoot-through is due to the long reverse recovery time of the free wheeling diode, which can add a peak of around 40 amps above the normal pulse, in the case of the UPS.

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6 - A transistor reaches an "on" state when its collector voltage drops below 90% of its pre-switch-on value. Likewise, a transistor is off when its collector current drops below 90% of its pre-switch off value [22].

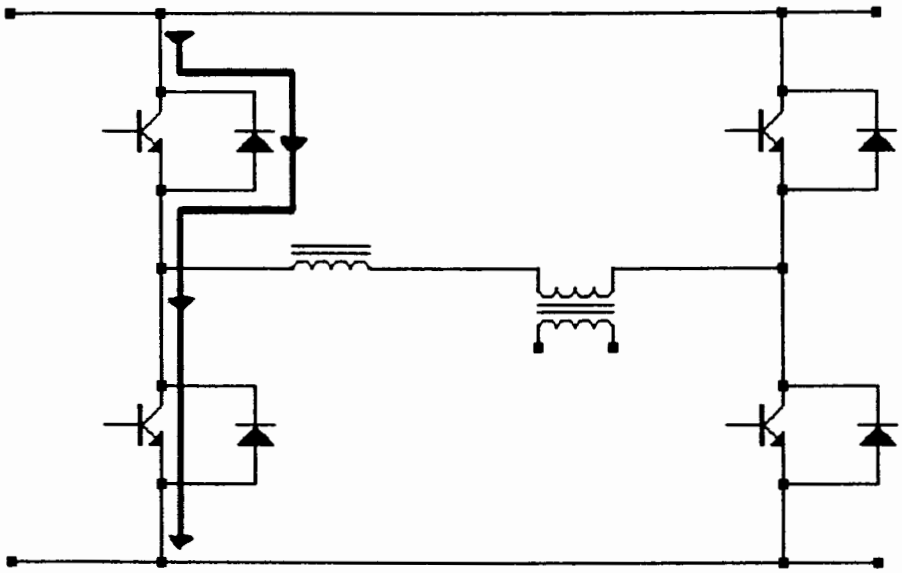

Figure 4.18 A shoot-through path

4.5.4.3 Transistor Turn-Off

Figure 4.19 shows the collector current (upper trace) and collector voltage when a transistor turns off (lower trace). The Iwatsu oscilloscope has only two channels, so it is difficult to show when the base drive begins to switch the transistor off. A letter A in the graph signifies when the base drive starts to switch the transistor off.

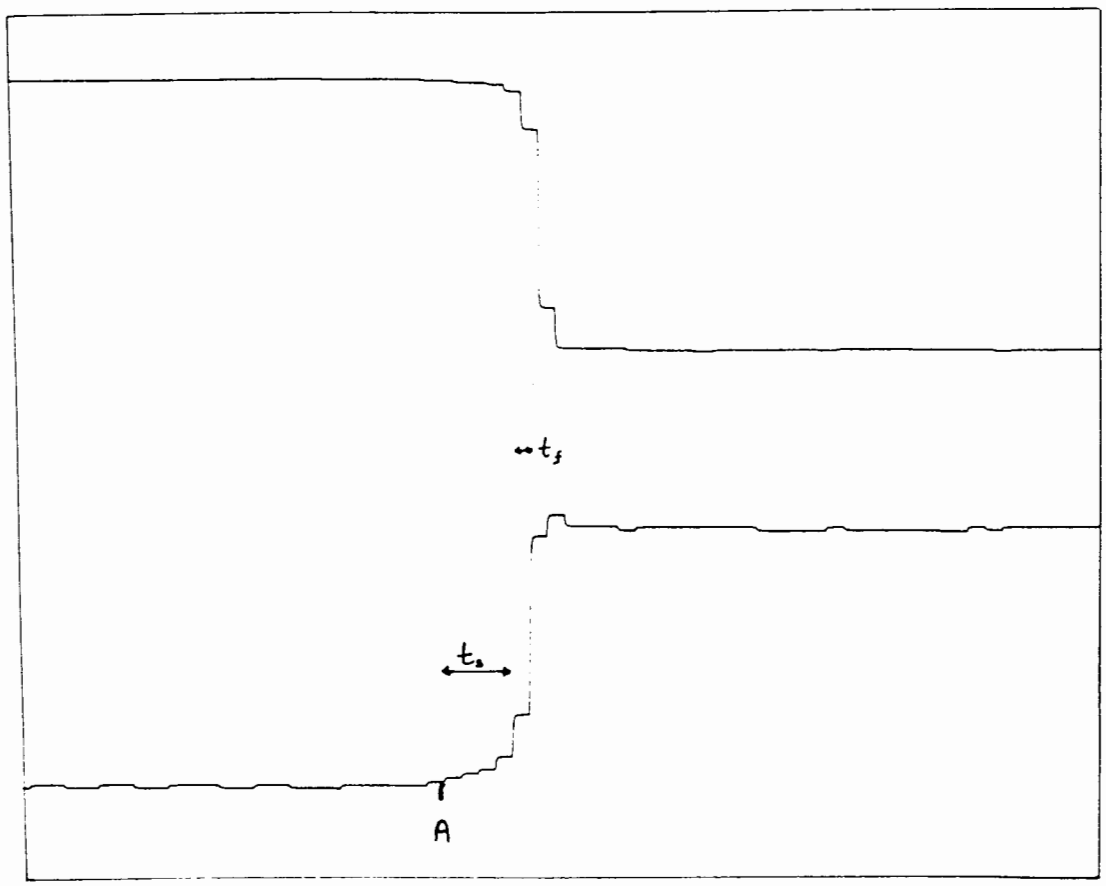

Figure 4.19 I_C and V_{CE} at switch-off

The transistor is conducting 80 Amps before it is switched off. A storage time (t_S) of approximately 4us can be seen before the current begins to fall rapidly (t_f), which takes a further 2us. During the storage time, V_{CE} rises slowly. This is due to the slow down circuit in the output of the base drive. A comprehensive explanation is given in section 6.2.3.

After the storage time, I_C falls sharply and V_{CE} rises sharply, with almost no overlap. The delay in rise of V_{CE} is caused by the snubber circuit. It should be noted that the graph shows almost no voltage overshoot. This is incorrect as there is a 50V overshoot for approximately 1.5us[7].

7 - Measured on the Nicolet oscilloscope.

4.5.4.4 Snubber Voltage waveforms

Figure 4.20 and 4.21 show the snubber capacitor voltage (upper trace) relative ton V_{CE} (lower trace), for the turn off and turn on.

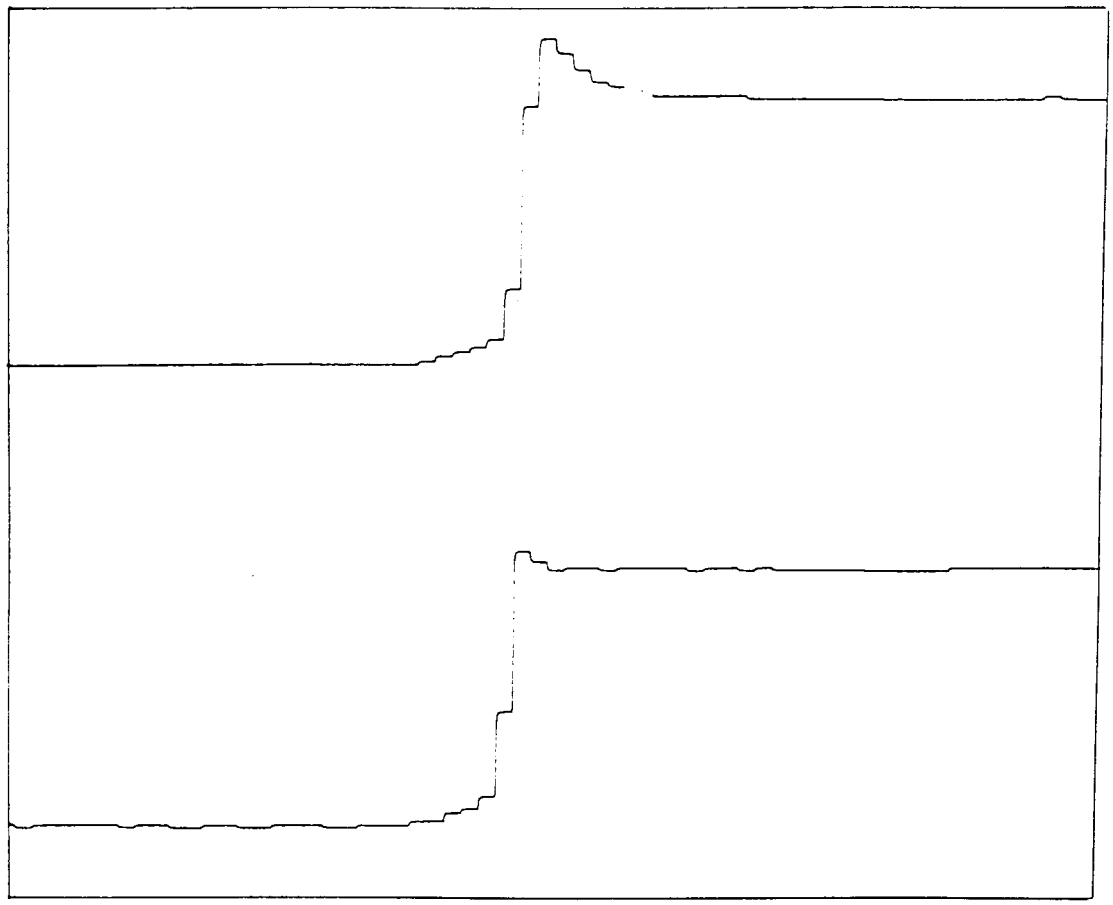

Figure 4.20 Snubber voltage and V_{CE} at turn-off

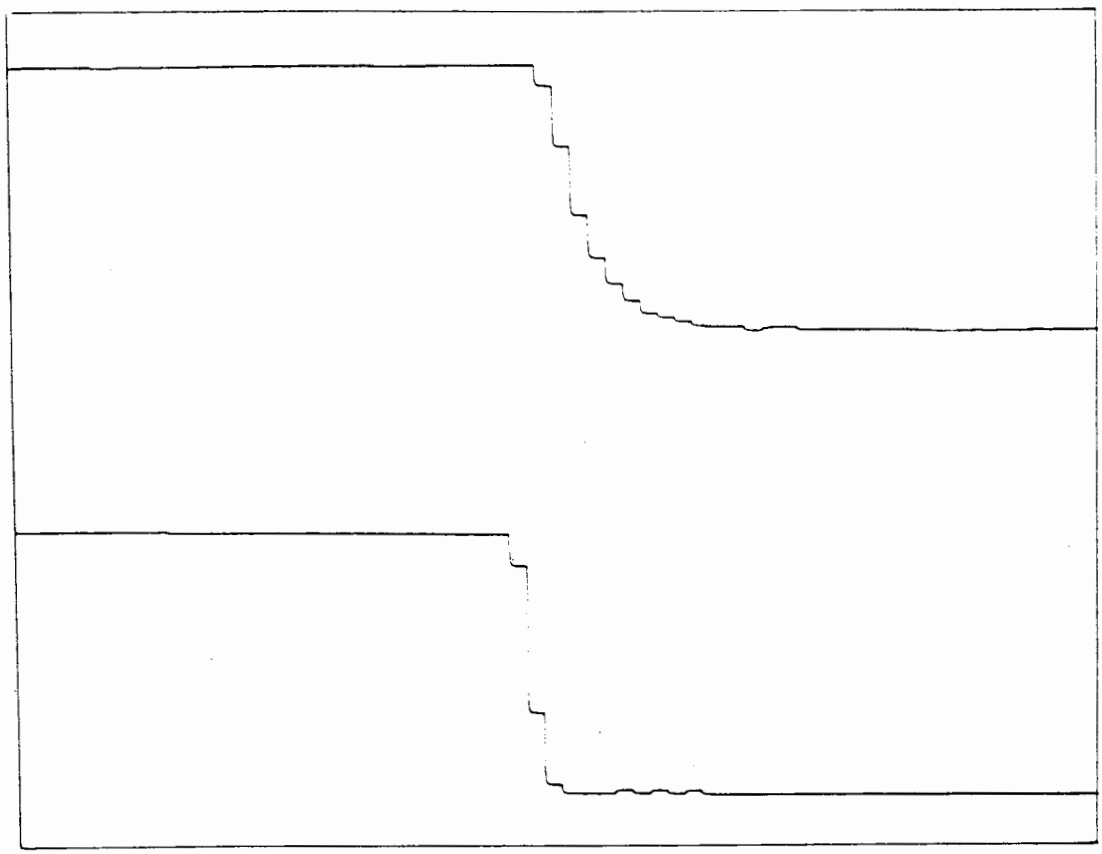

Figure 4.21 Snubber voltage and V_{CE} at turn-on

At turn off, the snubber capacitor appears to charge up to above V_{CE}. This is obviously incorrect and is an error in the oscilloscope reading. The actual over-shoot is the same as the peak voltage that the snubber capacitor changes to[8]. When the transistor switches off, the capacitor voltage rises rapidly, and follows V_{CE}. At switch-on, the capacitor discharges slowly through the snubber resistor.

8 - Measured on the Nicolet oscilloscope.

CHAPTER 5

THE INPUT RECTIFIER AND TRANSFORMERS

As mentioned earlier, the inverter changed during the design process, from a 125V DC push-pull configuration to a 250V DC full bridge configuration. The Rectifier supplies this DC power to the inverter. Consequently, the rectifier had to be converted from 125V to 250V. It was modified from a half bridge to a full bridge configuration. As the transformers form the major cost in the converter, it was necessary to use the same transformers in the 250V converter. The most effective way of applying the same transformers was to raise the DC voltage from 125V to 250V. This is the reason for choosing a 250V DC bus for the full bridge inverter. Both rectifier designs and the input and output transformers are discussed in the following sections. The power output requirement for both rectifiers was 25KVA.

5.1 THE TRANSFORMERS

This section discusses the transformer winding configurations, to enable a better understanding of the rectifiers. Both transformers were originally constructed for the 125V push-pull inverter, but were later adapted to the 250V full bridge inverter.

5.1.1 The Output Transformer

5.1.1.1 Construction of the Transformer

The transformer has two primary windings and five secondary windings. The two primary windings are required for push-pull operation in an inverter. The transformer

was constructed with five output windings so that it was possible to obtain a wide range of output voltages. In the final design, all the windings were connected in series to obtain the highest possible voltage. A diagram of the transformer and the winding voltage ratios is shown in figure 5.1.

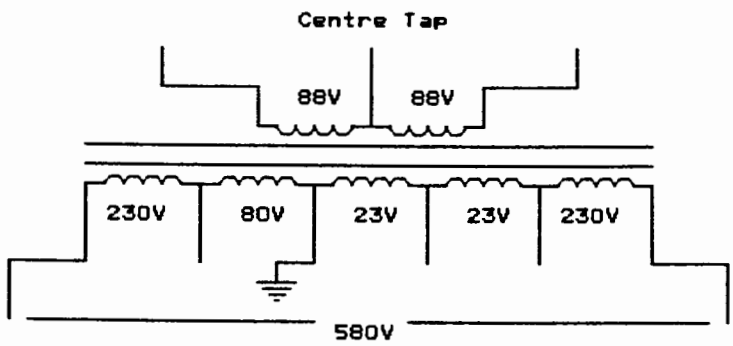

Figure 5.1 The Output Transformer Windings

The primary voltage was chosen to be 88V, approximately 2/3 of the DC bus voltage. This gives an acceptable level of modulation at full power, with an acceptable primary current. MLT Drives uses this voltage ratio in the design of their inverters. In the full bridge inverter, the two windings were connected in series, to give a single winding of 176V.

In the push-pull inverter, the secondary did not have a 80V winding. With all the windings in series, the secondary voltage summed up to 500V. This is the voltage that was originally specified by Metal Box. An extra winding of 80V was inserted in the transformer to increase the voltage, as 500V was found to be too low.

The transformer core was constructed of grain oriented silicon steel. With this core, the transformer is capable of transferring 20KVA at 50Hz. The full 20KVA is only consumed at 120Hz [9]. At 120Hz, this core can transmit more than 20KVA. The transformer was thus designed conservatively.

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9 - In section 2.1.5, it is shown that at a low frequency, the Soudronic's maximum operating speed is limited, therefore the power consumption is low.

5.1.1.2 Power Loss in the Windings

In the push-pull configuration, the full inverter current alternates between the two windings, whereas in the full bridge configuration a smaller current flows continually through both windings. The power dissipated in both of the primary windings of the push-pull inverter can thus be derived from the equation :

$P_{pp} = 2 \times (I^2 \times R)$ where: **I** is the RMS current through each winding and **R** is the resistance of one winding

In the full bridge inverter the peak current is halved, so the RMS current is $1/\sqrt{2}$ of the Push-pull inverter[10]. The same current flows through both windings. The total winding resistance is also doubled, because two windings are connected in series. The power loss therefore becomes :

$$P_{fb} = (1/\sqrt{2} \times I)^2 \times (2 \times R)$$

or

$$P_{fb} = I^2 \times R$$

The power losses in the primary winding of the full bridge inverter are thus reduced by a factor of 2. The transformer is therefore better utilised in the full bridge inverter than in the push-pull inverter.

5.1.2 The Input Transformer

This transformer is a three phase transformer with a 380V, delta connected primary. It has three primary and two secondary windings per phase. The primary has three windings so that it is possible to vary the voltage either up or down by a total of 10%. A diagram of the transformer and the winding voltage ratios is shown in

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10 - The calculation that derives this can be found in Appendix B.

figure 5.2.

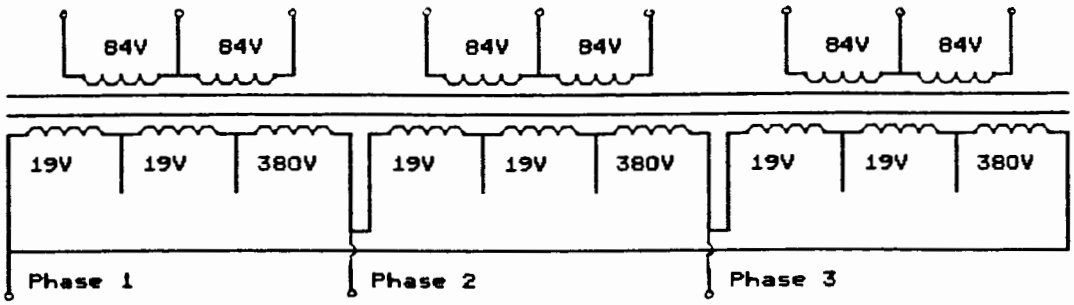

Figure 5.2 Input transformer

The three phase transformer is constructed in such a way that it generates six secondary phases. This type of secondary was chosen, because a six phase, half bridge rectifier gives a low ripple, six pulse DC waveform. This rectifier not only gives low current ripple, but current only conducts through one diode at a time, resulting in low semiconductor losses. The transformer was eventually used in the full bridge configuration to generate the 250V DC bus. The transformer primary winding losses were thus reduced by a factor of 2 for the same reasons as discussed in the previous section.

The main secondary winding was connected in series, but out of phase with the two 5% windings. This has the effect of subtracting 10% from the primary, or adding 10% to the output. This was done to increase the DC bus voltage to the highest possible voltage.

The transformer core was made from grain oriented silicon steel. The core has a three phase, 50Hz power rating of 25KVA.

5.2 THE HALF BRIDGE RECTIFIER

The half bridge rectifier converts 25KVA, 90V, 6 phase into 6 pulse, 125V DC, 200 Amps. A 6 phase, 6 pulse rectifier generates an RMS voltage ripple of 4% and has an input power factor of 0.95 [10]. These perameters were

considered adequate for the converter. The half bridge uses 6 diodes, one connected to each phase. A diagram of the rectifier can be seen in figure 5.3.

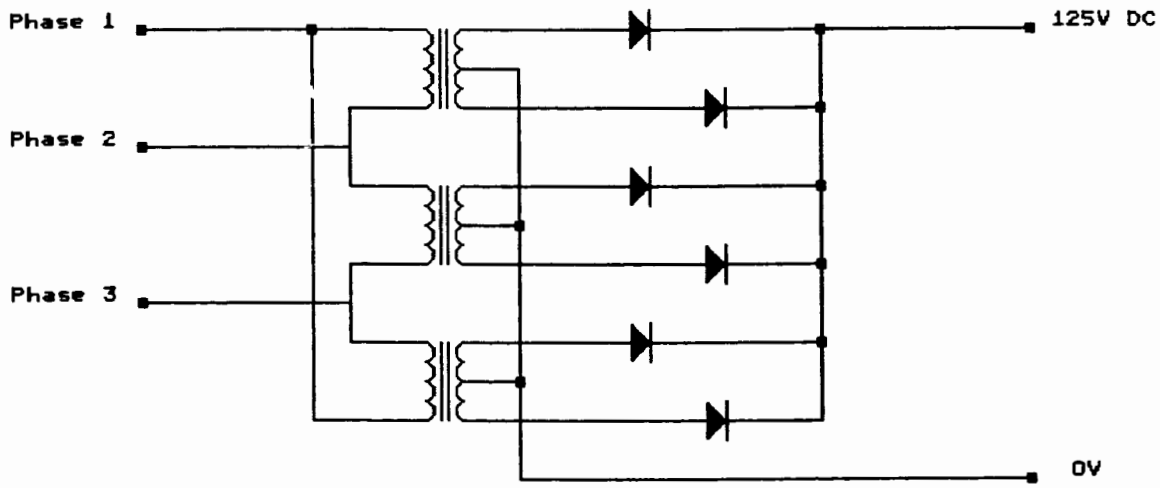

Figure 5.3 The 125V Rectifier

The diodes that were used, were Semikron SKKD 81/06, 81 Amp 600 Volt, double diode modules [11]. The data sheet for these diodes can be found in Appendix A. An SKKD module is intended for use in a full bridge inverter. The internal structure of these diode modules is shown in figure 5.4.

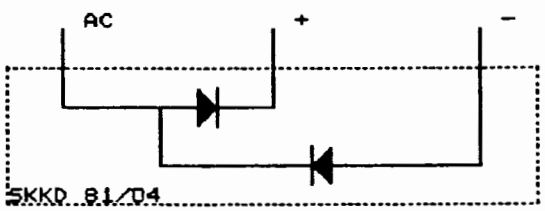

Figure 5.4 The Structure of the SKKD module

At this time, this was the only isolated module configuration available in South Africa. Isolated single diode or common cathode diode packs were not available unless a large quantity of modules was required. It was thus necessary to use these modules in the half bridge rectifier. The internal structure of the modules made it

possible to use only one diode per pack, or 6 modules in total.

All six phases on the secondary are connected in a star configuration. When the voltage on a phase rises above the DC bus voltage, it conducts current to the DC bus. The current returns through the load to the star point. Each diode conducts once per 20ms (50Hz cycle).

5.3 THE FULL BRIDGE RECTIFIER

The full bridge, unlike the half bridge rectifier, generates 250V at 100 Amps with 12 pulses per 20us. A 12 pulse, 6 phase rectifier has an RMS ripple of 3.4% and an input power factor of 0.99 [10]. Both of these perameters are an improvement on the 6 pulse rectifier.

The rectifier uses 12 diodes, 6 connected between a phase and the positive of the DC bus, and 6 connected between the negative of the DC bus and a phase. A circuit diagram of the rectifier is shown in figure 5.5.

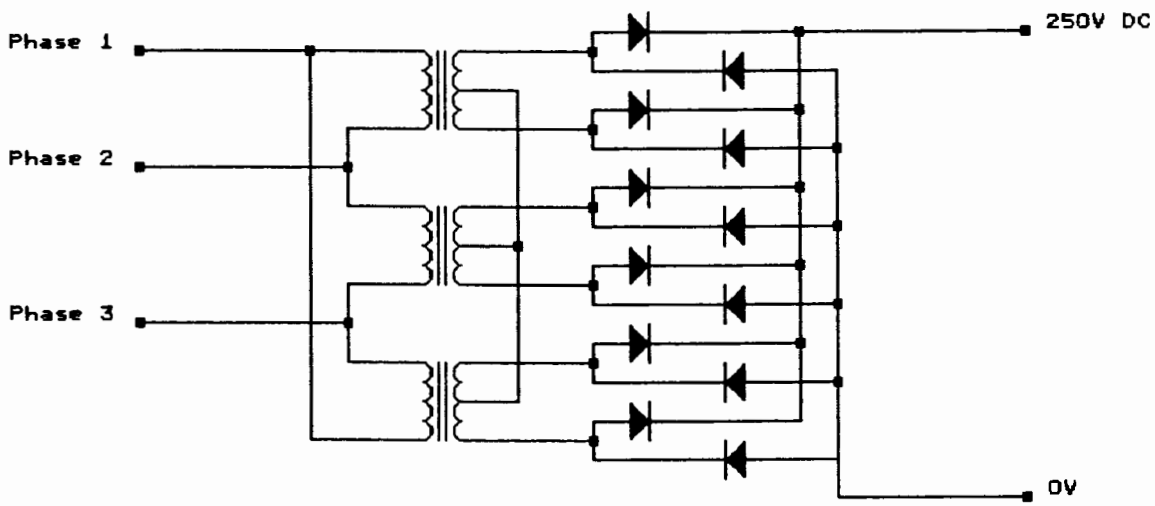

Figure 5.5 The 250V Rectifier

The same diode modules were used in the full bridge as in the half bridge inverter. As the modules were constructed

for use in a full bridge inverter, all twelve diodes could be used and it was not necessary to purchase more.

The three centre taps of the transformer secondary were connected together. This is not critical, but it assists in balancing the current through each transformer winding and diode. If the transformer and phase voltages are correctly balanced no current will flow between centre tap connections.

When the voltage on a phase rises above the DC bus voltage, a diode conducts current to the DC bus. The current returns through the load, to the negative bus. Current then flows back through the diode connected to the winding that has the lowest voltage. Current therefore always passes through two diodes. The current through the diodes is half that of the half bridge rectifier. The losses in the diodes thus remain approximately the same.

CHAPTER 6

THE BASE DRIVE

The base drive is the interface between the computer and the power transistor. It not only amplifies the signal, but also includes power transistor protection features. The base drives are isolated from each other as well as from the computer. This chapter discusses the final base drive design that was used in the full bridge inverter.

6.1 OBJECTIVES OF THE BASE DRIVE DESIGN

The base drive has to perform two important tasks, they are: a) to switch the transistor in the most efficient manner, and b) to protect the transistor in the case of a fault. It was decided that the base drives for all four transistors should be the same, to keep the amount of spare parts for the converter to a minimum. The base drives were to be isolated from each other and have separate power supplies. A block diagram of the functional components of the base drive is shown in figure 6.1.

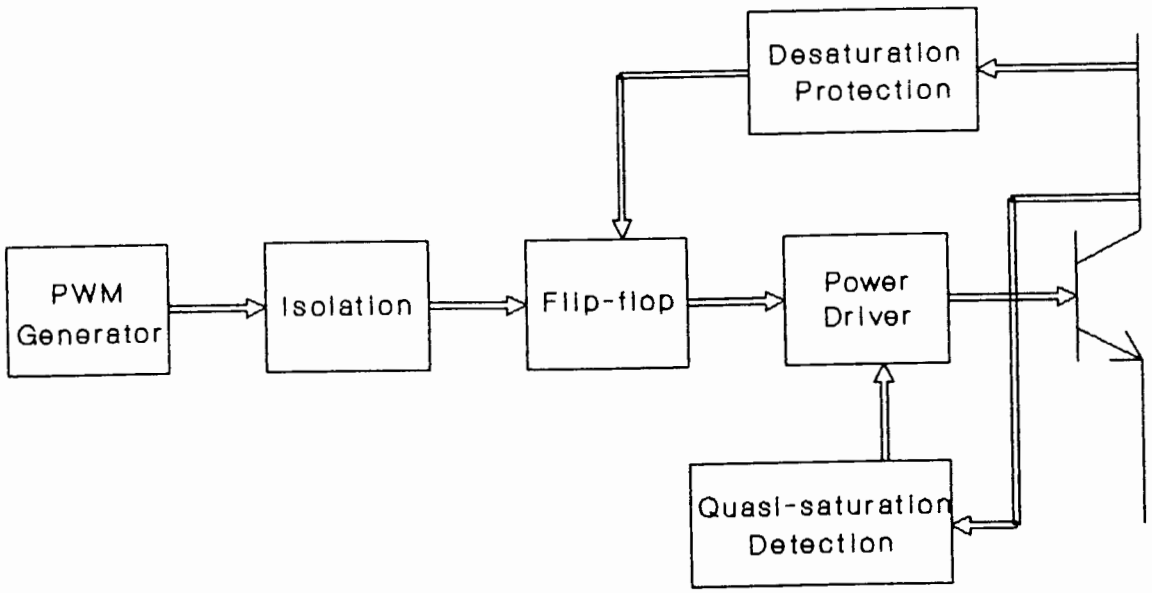

Figure 6.1 Block Diagram of the Base Drive

6.1.1 Base Drive Features

The isolation stage has to transfer a signal from the computer at a voltage near to earth potential, to the base drive, at a voltage between earth potential and 600V above earth potential. While the transistor is switching, the rate of voltage change relative to the input signal is very high and can lead to common mode problems. The isolator must be able to operate under this condition. The isolation can be implemented by means of a pulse transformer or an optical isolator.

The flip-flop is a latch for the pulse width modulation. The latch is triggered on and off by the rising and falling edges of a pulse width modulated signal. For circuit details see sections 6.2.1 and 6.2.2. The signal is buffered to give a fast switching output to the output drive stage.

A desaturation protection network is closely linked to the flip-flop. The collector-emitter voltage of the power transistor is monitored. If this voltage rises above a set level, the flip-flop is unlatched and the power transistor is switched off. The flip-flop is thus

necessary to store the fault state. If a fault condition has occurred, the transistor must be switched on again only at the next PWM rising edge. The desaturation protection network also serves as a current limit for the power transistor. If the current through the collector-emitter junction rises, the associated collector-emitter voltage will rise. This will cause the desaturation to unlatch the flip-flop.

The function of the power output driver is to keep the switching and conduction losses of the power transistor to a minimum. The power transistor is switched on and off rapidly by means of a push-pull transistor pair driving into its base. It is also held in quasi-saturation by means of a Baker clamp. See section 6.2.3.5 for details.

6.1.2 Possible Additional Features of the Base Drive

Base drive circuits can vary in complexity and operating features. The drive can have many protection functions, but at the expense of more complex circuitry. The base drive that was designed for use in the converter has only one protection feature, the desaturation protection (current limit). Other features that could be added into the circuit are [12, 13]:

- power supply monitoring
- overvoltage monitoring
- power transistor thermal overload
- permanent latch for a fault condition

The power supply could be over designed so that a power supply failure is unlikely, if not, the base drive should be able to protect the power transistor in the case of a power supply failure. The transistor should not latch on in the event of a low positive supply voltage. If the negative supply voltage drops, the transistor should be switched off and should not be allowed to come on again until the negative supply recovers. This is discussed further in chapter 9.

An overvoltage on the power transistor can occur because of a snubber failure, a component failure in the inverter bridge circuit, or from interference in the mains supply. Under normal operation, the highest overshoot occurs when the transistor is switched off. If an overshoot occurs, the transistor should not be allowed to switch on again, until the fault has been rectified.

Power transistors have a maximum allowable junction temperature rating. Each base drive could include a sensor that senses if the maximum temperature has been exceeded. If the maximum temperature has been exceeded, the transistor should be switched off, until the temperature falls below a specified level again. The temperature monitoring could also be performed by the computer controller, using one sensor for all the transistors.

For a fault condition it may be necessary to determine the extent of the fault and if necessary, to permanently disable the inverter. This will force service personnel to determine the source of the fault and to restart the converter by means of a reset button, or by switching the converter off and on again.

6.2 OPERATION OF THE BASE DRIVE

To understand how the base drive operates it is necessary to give a description of the function of every component in the circuit. This section gives the reasons for choosing the components, how the component parameters were specified and then describes the function of the components.

The base drive was developed from a circuit that was proposed in a paper written by Rischmueller [14]. The isolation method was substituted for a circuit suggested by other authors such as Entl, Keuter, Lovatt [12, 15,

16]. A number of other articles and books were used to assist in the modifications to the original circuit proposal. These papers are referenced throughout this section. A full circuit diagram of the base drive and how it connects to the transistors in the bridge is shown in figure 6.2. A larger copy of this diagram is in Appendix C.

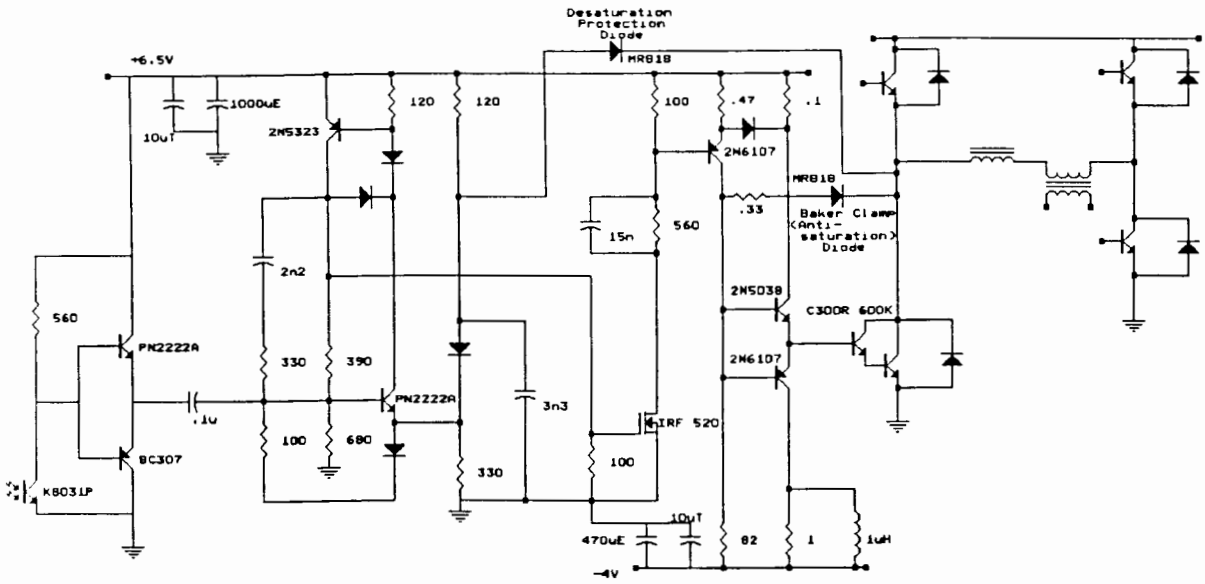

Figure 6.2 A complete Base Drive Circuit Diagram.

6.2.1 Isolation of the Base drive

The most common methods of achieving isolation is by means of either an optocoupler, or a pulse transformer. A pulse transformer is only able to transfer short pulses across the isolation[11], whereas an optocoupler is able to transfer a pulse of any width [15]. Three isolation circuits were considered during the design process. The circuit diagrams of these methods are shown in figure 6.3.

11 - Longer pulses can be transferred across a large pulse transformer, but this results in practical difficulties.

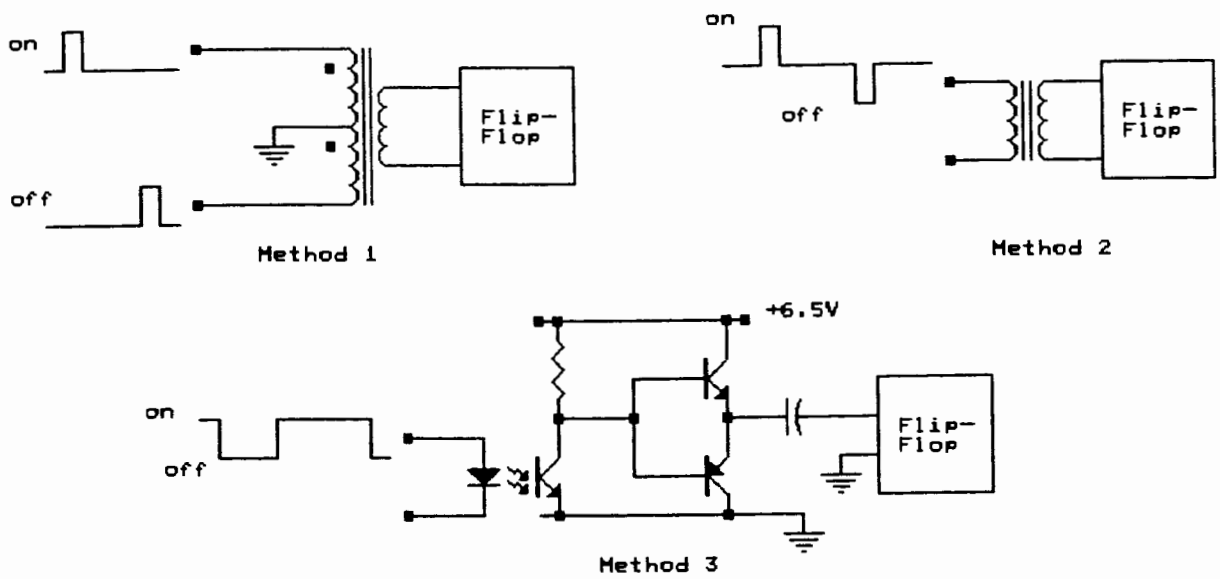

Figure 6.3 Three isolation methods

6.2.1.1 Method 1 and 2

The first and second methods both use pulse transformers to isolate the base drive. A positive pulse is transferred across the isolation to latch the flip-flop and a negative pulse to unlatch the flip-flop. Problems were encountered using pulse transformers, as they caused oscillations in the latching circuit. If a stray pulse was picked up by the leads leading to the pulse transformer, the flip-flop could be latched on falsely, with disastrous results. This problem is discussed further in section 8.3.

6.2.1.2 Method 3

The third method used an optocoupler to isolate the base drive. A discussion on the dv/dt rating of the optocoupler can be found in Appendix H. The entire PWM signal is transferred across the isolation, and the pulses for the flip-flop are generated at the output of the optocoupler. The optocoupler LED is driven directly from a buffer I.C. via a resistor. The optocoupler has an open collector, Schmitt-trigger output. The open collector is pulled up by a resistor, connected to the 6.5V rail. The high impedance pull up is buffered by a push-pull transistor pair to give a low impedance source. This low

impedance output is fed through a capacitor to generate positive pulses off the rising edge and negative pulses off a falling edge, thus latching and unlatching the flip-flop.

The third isolation method was used in the final base drive design. The problems that were experienced with the first two designs are discussed further in section 8.3.1.

6.2.2 The Latching Flip-flop

The flip-flop regenerates the PWM, using the positive and negative pulses from the isolation section to latch it in the high or low state. This PWM is then boosted by the power output driver (section 6.2.3) to drive the power transistor. The flip-flop also forms part of the protection, as it is forced to unlatch if the base drive senses the power transistor desaturating. A circuit diagram of the flip-flop and associated components is shown in figure 6.4.

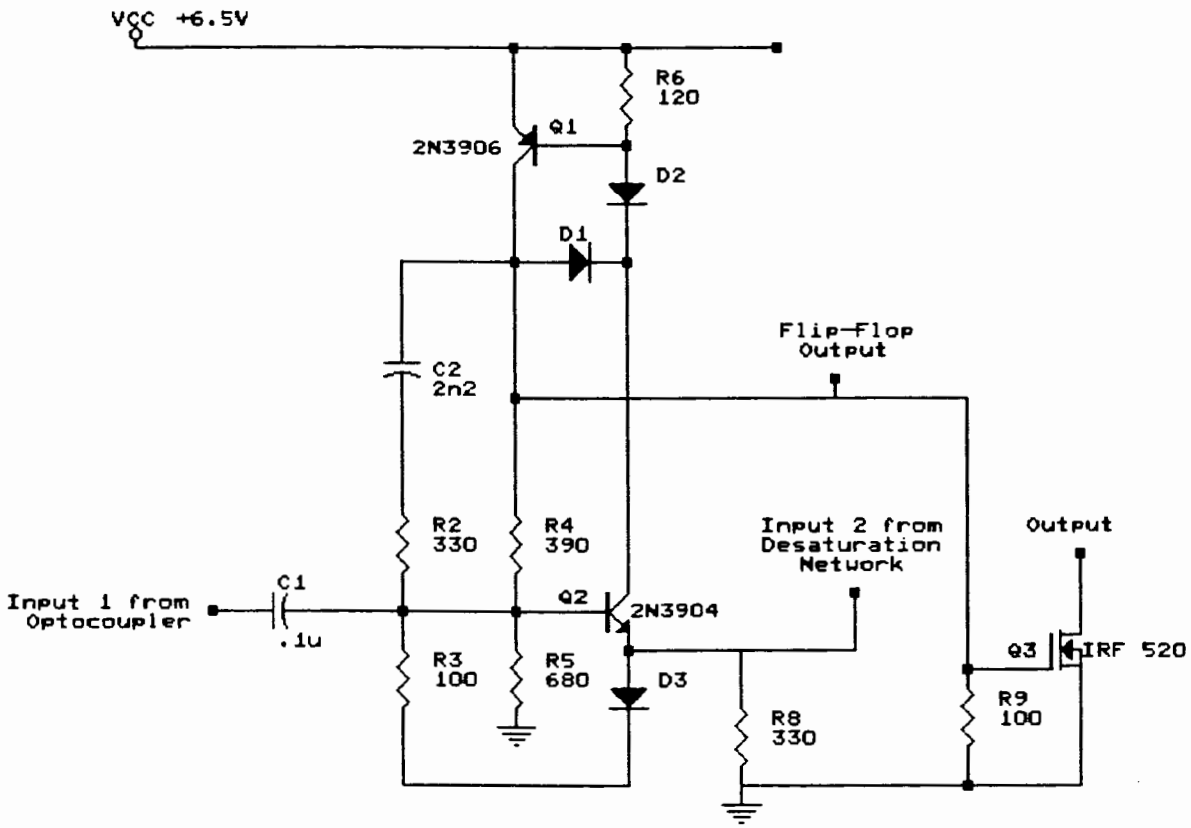

Figure 6.4 Circuit diagram of the flip-flop

6.2.2.1 The circuit operation

The circuit has two inputs and one output, as well as a +6.5V power supply. Input 1 is in the form of decoupled positive and negative pulses, that are formed by the isolation circuit. Input 2 is used by the collector-emitter desaturation protection circuit, to unlatch the flip-flop when desaturation occurs. The output of the flip-flop drives the gate of a MOSFET, that buffers the output to give a rectangular pulse to the power stage.

The two transistors that form the latch are Q1 and Q2. To latch the flip-flop in a high state, a positive pulse is applied to the base of Q2 from input 1. The positive pulse switches Q2 on, which supplies the current to the base of Q1, thus switching Q1 on. Q1 in turn supplies the base current to Q2 to hold it on, thus latching the flip-flop.

The output of the flip-flop will not change to a high state until both Q2 and Q3 have switched on. R2 and C2 is a speed-up circuit, to provide a low impedance path from the input of the flip-flop to the output of the flip-flop. C2 and R2 were chosen to have the lowest impedance that does not distort the input waveform.

D3 and R3 is a pulse limiting circuit, that limits the voltage of the negative pulses to the base of Q2. They also assist in the discharge of capacitor C1. D1 and D2 form a Baker clamp on Q1, to limit the state of saturation of Q1 and consequently to enable Q1 to switch off rapidly.

The output of the flip-flop is taken from the collector of Q1. This voltage is switched from around 1V in the low state, to around 5.5V in the high state. This signal drives the gate of the MOSFET (Q3), that has a threshold voltage of 4V. The output of Q3 is thus inverted and switches from 0V to 6.5V

6.2.2.2 Unlatching the flip-flop

R4 and R5 form a potential divider that sets the voltage that input 2 must rise above, in order to unlatch the flip-flop. If the latch is in the high state, the emitter voltage of Q2 will be 0.65V (a diode drop) below the voltage set by potential divider R4 and R5. If input 2 is pulled high, i.e. above the emitter voltage of Q2, then Q2 will switch off and the flip-flop will unlatch. Thus, in a fault condition, if the input 2 is pulled high, the flip-flop will unlatch and cause the transistor to be switched off.

6.2.3 The Power Output Driver

This circuit amplifies and shapes the signal generated by the flip-flop to enable the power transistor to operate efficiently. The circuit employs a Baker clamp (Q5 and D6), to keep the power transistor in quasi saturation, so that it is able to be turned off rapidly. The Baker clamp decreases the switch off losses at the expense of an increase in conduction losses. The conduction losses can be minimized though, by ensuring a correct level of saturation in the power transistor. The driver also limits the maximum current that is delivered to the base of the power transistor.

The circuit has two inputs and one output, as well as a +6.5, 0, -4V supply. Input 1 is the PWM signal from the flip-flop and input 2 is connected to the collector of the power transistor. The output is the PWM current to drive the base of the power transistor. A circuit diagram of the driver is shown in figure 6.5.

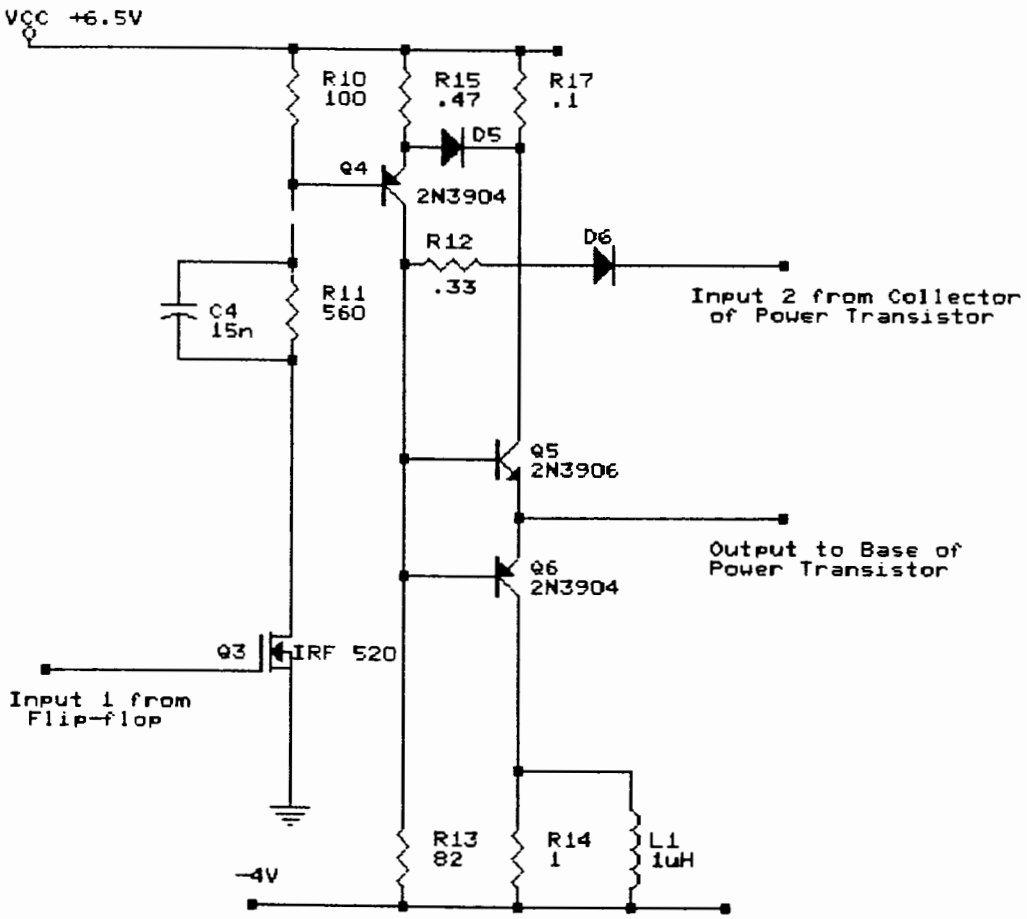

Figure 6.5 Circuit diagram of the Power Output driver

6.2.3.1 The Pre-Driver

When Q3 is on, R10 and R11 form a potential divider that provides enough current to the base of Q4 to bias it on. Q4 is biased in its linear mode, so that it is able to provide the peak current demanded by Q5 when the power transistor is conducting. Q4 re-inverts the signal from Q3 and gives an output of up to 6V in the high state. R14 pulls the base of both Q5 and Q6 to -4V, when Q4 is off.

6.2.3.2 Power Transistor turn-on Pulse Generator

If a high current pulse is applied to the base of a power transistor to turn it on, the transistor will switch rapidly and low switch-on losses will result [17].

C4 is a speed-up capacitor and a pulse generator. It has little effect on the turn-off of the power transistor, but

it provides a means of generating a current pulse to switch the power transistor on. In a steady state condition C4 is not charged. When Q3 is switched on, C4 charges up by drawing current through R10, or through R15 and the base-emitter junction of Q4. As R10 is 100 Ohms and R15 is 0.47 ohms, most of the current flows through R15 and Q4. This drives Q4 into saturation for the time it takes C4 to charge up and thus provides a high current pulse to the base of Q5 and the power transistor. This is illustrated in a Pspice model of the base drive in figure 6.6. The upper trace is the voltage of the junction between C4 and R10 and the lower trace is the voltage on the output of the base drive. See section 6.4 for more details on the Pspice model.

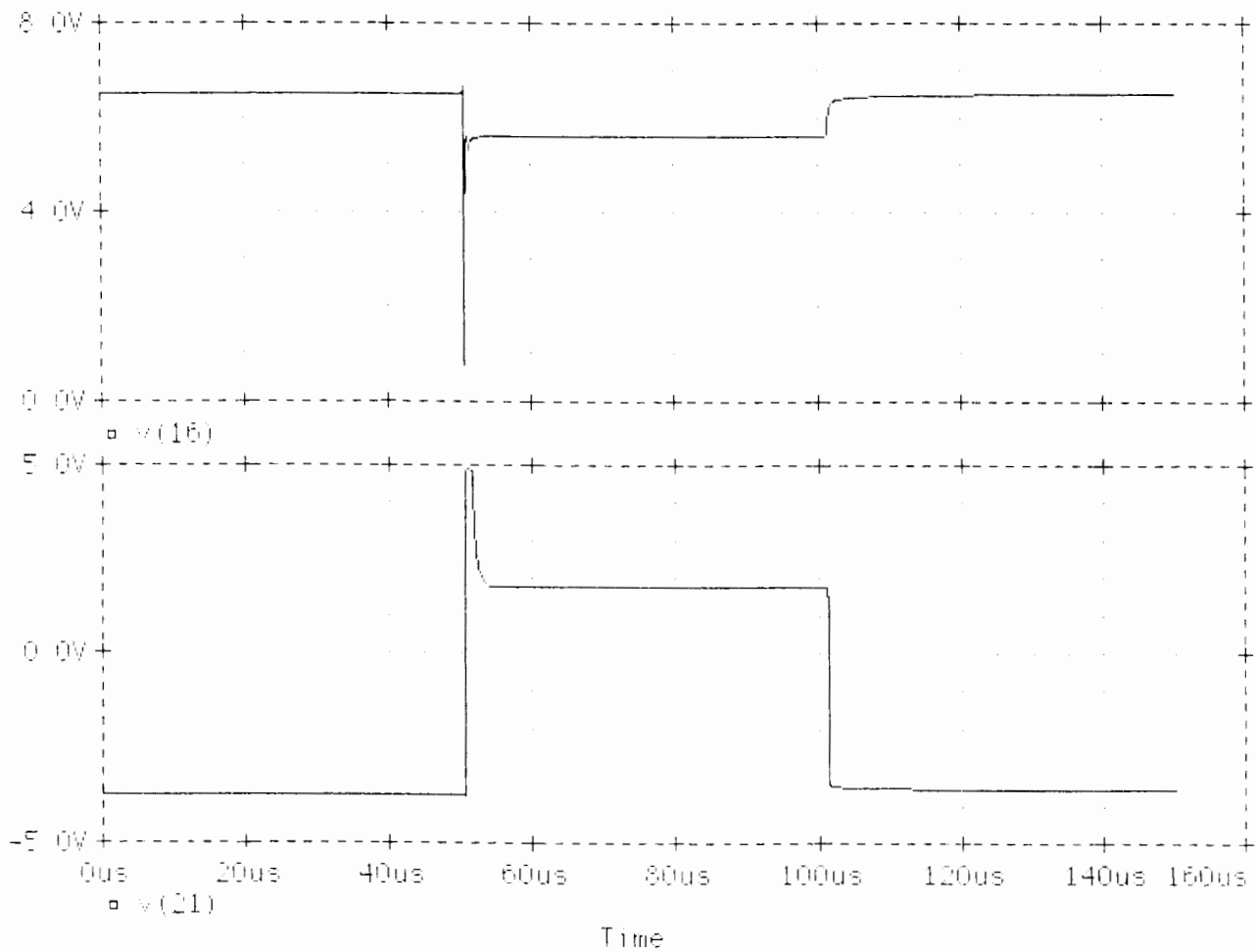

Figure 6.6 Model of the Base Drive Output.

The short pulse on the rising edge of the PWM can be seen in figure 6.6. The high current pulse into the base of

the power transistor is necessary to switch the transistor on rapidly.

6.2.3.3 Maximum base current Limit

The most destructive parameter of a power transistor is the maximum base current [18]. It is therefore important to limit the output current of the base drive.

R17, D5 and R15 form a current limit circuit, that limits the maximum current the power transistor can draw. If the current through R17 reaches 8 amps, D5 will conduct and draw the current from Q4 that supplies the base of Q5. Q5 will thus limit the current into the base of the power transistor, which will cause it to desaturate. If a fault caused this high current and the fault persists, the desaturation will cause the collector-emitter voltage to rise. The desaturation protection circuit will then switch the power transistor off.

6.2.3.4 Base Drive Output Switch-off circuit

To switch the power transistor off rapidly it is necessary to apply a negative voltage to its base [19]. A negative voltage on the transistor base also allows a higher collector-emitter voltage, by raising the V_{CE} rating of the Darlington from V_{CEO} to V_{CEX} [19, 20, 21]. For the AEG 300 R 600K V_{CEO} is 550V and V_{CEX} is 600V.

When Q3 switches off, R12 pulls the base of the Q6 negative, which switches it on. This switches the power transistor off. Q6 pulls the base of the power transistor negative through L1 and R16. L1 is used to minimise the switch off losses, by momentarily decreasing the reverse base current drawn from the power transistor. This decreases the switch off losses [14].

6.2.3.5 Antisaturation Network[12]

D6 in conjunction with Q4 form a Baker clamp, that keeps the power transistor in quasi-saturation, which can reduce

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12 - The term "antisaturation network" is synonymous with the term "Baker clamp".

the transistor storage time to negligible values [22]. When Q4 is on, it conducts a constant current from its collector to its emitter. The Baker clamp works by limiting the current into the base of Q5, by diverting excess current away from Q5 via D6. Limiting the current into the base of Q5 also limits the current into the base of the power transistor. This limits the depth of saturation of the power transistor. R13 was added to remove oscillations that occurred in the Baker clamp. More is said about this in section 8.3.2.

6.2.4 The Desaturation Protection Network

The desaturation protection network should not be confused with the antisaturation network, that holds the transistor in quasi saturation. The desaturation protection network monitors the collector-emitter voltage drop (state of saturation), and unlatches the flip-flop in the case of a high collector-emitter voltage drop. The network is shown in figure 6.7.

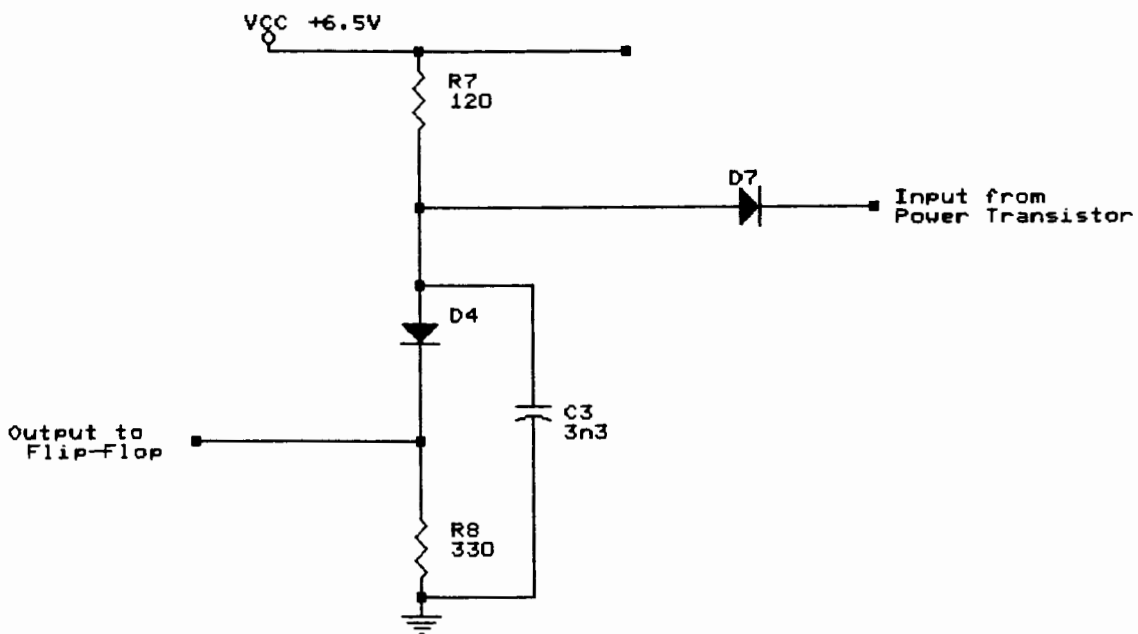

Figure 6.7 The Desaturation protection network

6.2.4.1 Protection Network Operation

A potential divider is formed by R7 and R8. This potential divider provides a voltage high enough to unlatch the flip-flop if input 1 is high. When the

transistor conducts, D7 holds the divider voltage low, which enables the flip-flop to remain latched. If the collector-emitter voltage rises, diode D7 will no longer hold the potential divider voltage low, so the flip-flop will unlatch. C3 and R7 provide a low pass filter to filter the signal from the collector of the transistor. This has the disadvantage of slowing the protection response time down. In the case of the collector-emitter, saturation voltage being low, D4 prevents current from flowing from the flip-flop through D7 and the power transistor.

6.2.4.2 Protection disable

The protection network is disabled whilst the power transistor switches on, because the optocoupler provides a high positive pulse to the flip-flop, that has a higher voltage than that set by potential divider R7 and R8. This is necessary, as when the power transistor is switched on V_{CE} takes a few microseconds to fall below the potential divider voltage set by R7 and R8. These few microseconds must elapse before the desaturation protection network should be allowed to operate.

6.2.5 The Base Drive Power Supplies

Each base drive operates from a separate +6.5, 0, -4V power supply. The base drive will operate with a positive supply voltage ranging from around 5V to around 8V, and a negative supply voltage ranging from -3V down to -6V. The power supplies had to deliver a peak average current of 2 Amps on the positive rail and an average of 0.5 Amps on the negative rail. The calculations for these currents can be found in Appendix B

In a full bridge there are four base drives, two of which have a busbar linking their 0V rails together. The busbar must be expected to take up to 300A peaks. With these high current pulses, a small parasitic inductance in the busbar generates potential differences across it. This means that even though the 0V rails are connected, they

are not always at the same voltage. The power supplies for these two base drives must therefore be isolated. A diagram of a full bridge inverter and its wiring configuration is shown in figure 6.8.

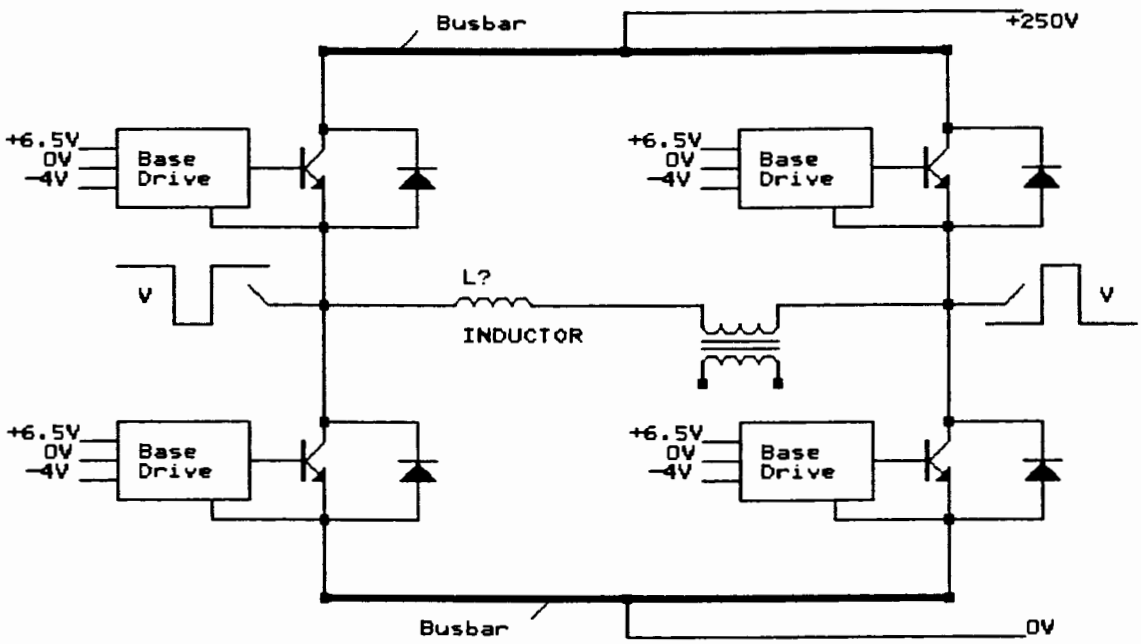

Figure 6.8 Full Bridge Wiring Configuration

For this project, overall efficiency was of no concern, but reliability and simplicity were regarded as high priorities. A linear power supply was thus chosen, as it is the most reliable and simple form of power supply.

The circuit used the common LM350 and the LM337 adjustable voltage regulating integrated circuits. The power was derived from a 50Hz transformer, with four centre-tapped, isolated and screened output windings The outputs were full wave rectified, filtered and passed through the regulators to give a stable supply. A circuit diagram of the power supply is shown in figure 6.9.

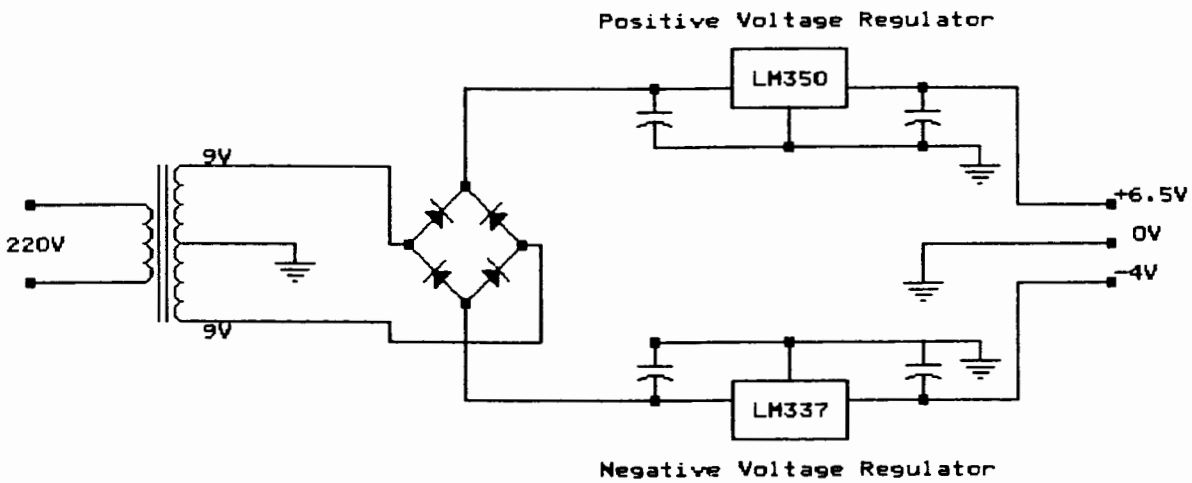

Figure 6.9 The linear power supply

6.3 BASE DRIVE OSCILLOGRAPHS

This section contains graphs that were taken from the 10KVA UPS using the Iwatsu oscilloscope, as described in section 4.5.1. All the traces were taken with the base drive connected to a power transistor, but with no collector current flowing.

6.3.1 Optocoupler output

Figure 6.10 shows the output of the optocoupler (upper trace) and the output of the series capacitor linking the optocoupler and the flip-flop. The positive and negative latching pulses that latch the flip-flop on and off can be seen.

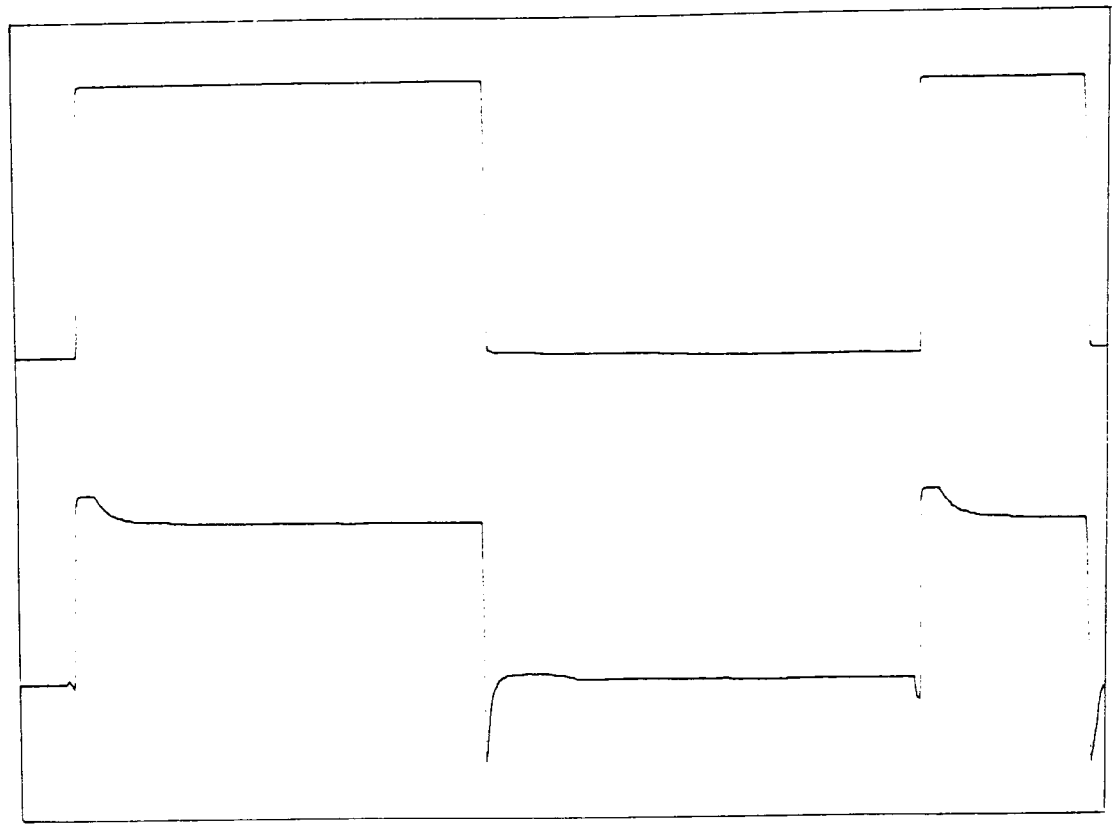

Figure 6.10 Flip-flop latching pulses

6.3.2 Optocoupler to flip-flop output delay

In figure 6.11 a graph of optocoupler output (upper trace) and the gate source voltage of the Mosfet (lower trace) can be seen. The optocoupler output rises sharply, but the output of the flip-flop at the gate of the Mosfet rises slowly, giving a 3us delay.

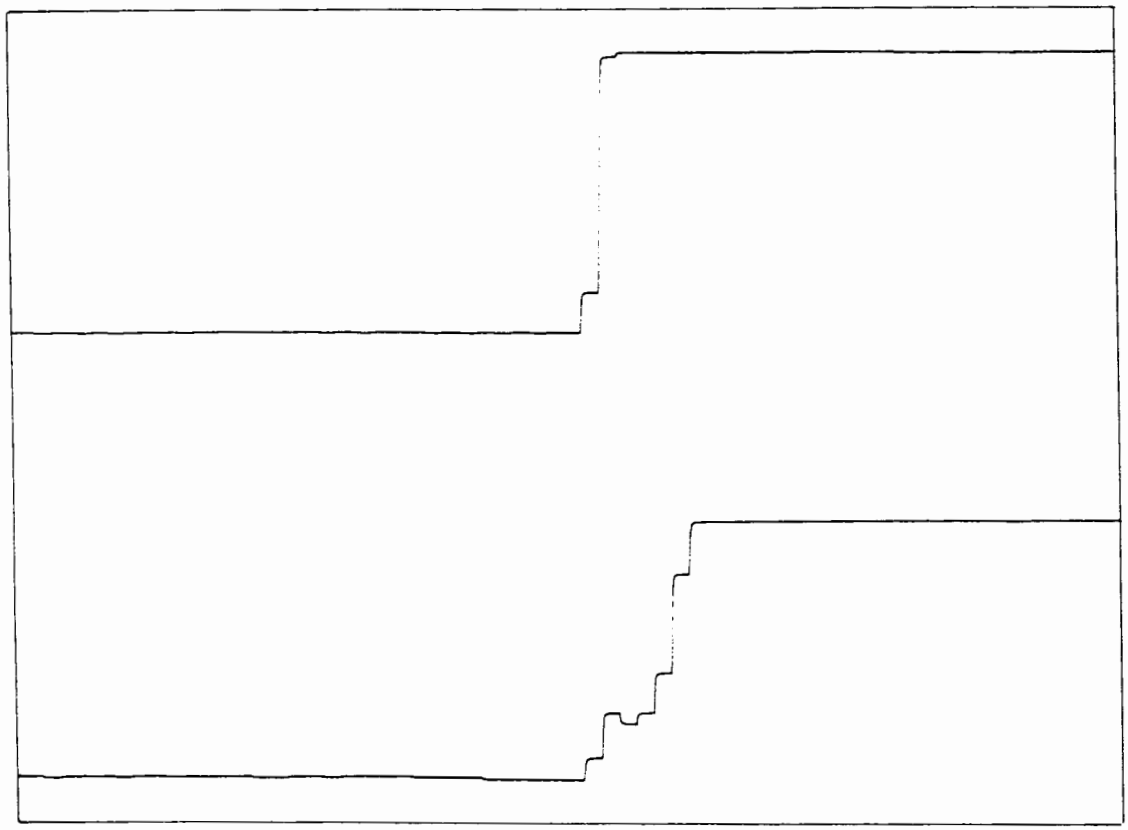

Figure 6.11 Optocoupler and flip flop outputs

From the output of the optocoupler to the output of the base drive, the signal is delayed 4us (shown in the following section). A 3us delay is thus the largest portion of the total delay. The slow rise of the gate voltage is due to the high input capacitance of the Mosfet. Methods for decreasing this delay time are suggested in section 9.4.

6.3.3 Optocoupler to Base drive output delay

A short "on" pulse of 7us long was injected into the optocoupler of the base drive to observe the differences in the input and output waveforms of the base drive. Figure 6.12 shows the output of the optocoupler (upper trace) and the output of the base drive (lower trace). The optocoupler output swings from 0V to 6.5V and the base drive output from -4V to 2.5V (peak).

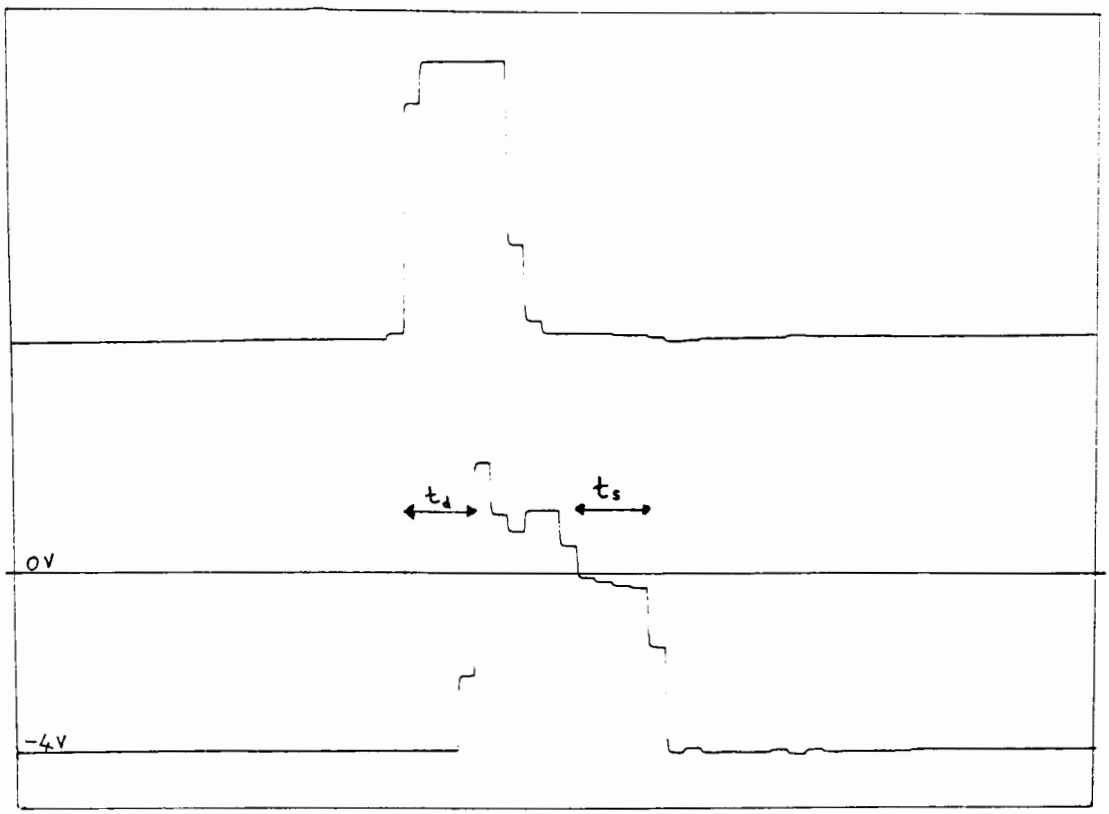

Figure 6.12 Optocoupler and base drive outputs

When the base drive is switched on, a delay of 4us passes before the output responds to the input pulse. The output pulse width is 6us long, but takes 4us to switch off, once the base voltage has started falling, due to the storage time of the power transistor. This results in an output pulse 3us longer than that of the input pulse. A short peak can be seen at the beginning of the output pulse. This is caused by the base drive, that generates a high current pulse to switch the power transistor on.

6.3.4 Base drive unlatching

The base drive circuit was modified to show it switching on with the desaturation protection network enabled. This shows the longest time the desaturation network can take to switch the power transistor off. The desaturation protection network is disabled as the transistor switches on for the reasons described in section 6.2.4.

The desaturation and Baker clamp diodes, (diodes D7 and D6 on page C4 of Appendix C) were removed from the base drive, so that the desaturation protection network sensed a permanently high V_{CE} and the Baker clamp drives the power transistor into saturation. The power transistor remained in the bridge, to show the collector voltage falling when the transistor switches on. Figure 6.13 shows V_{CE} (upper trace) and V_B of the power transistor (lower trace).

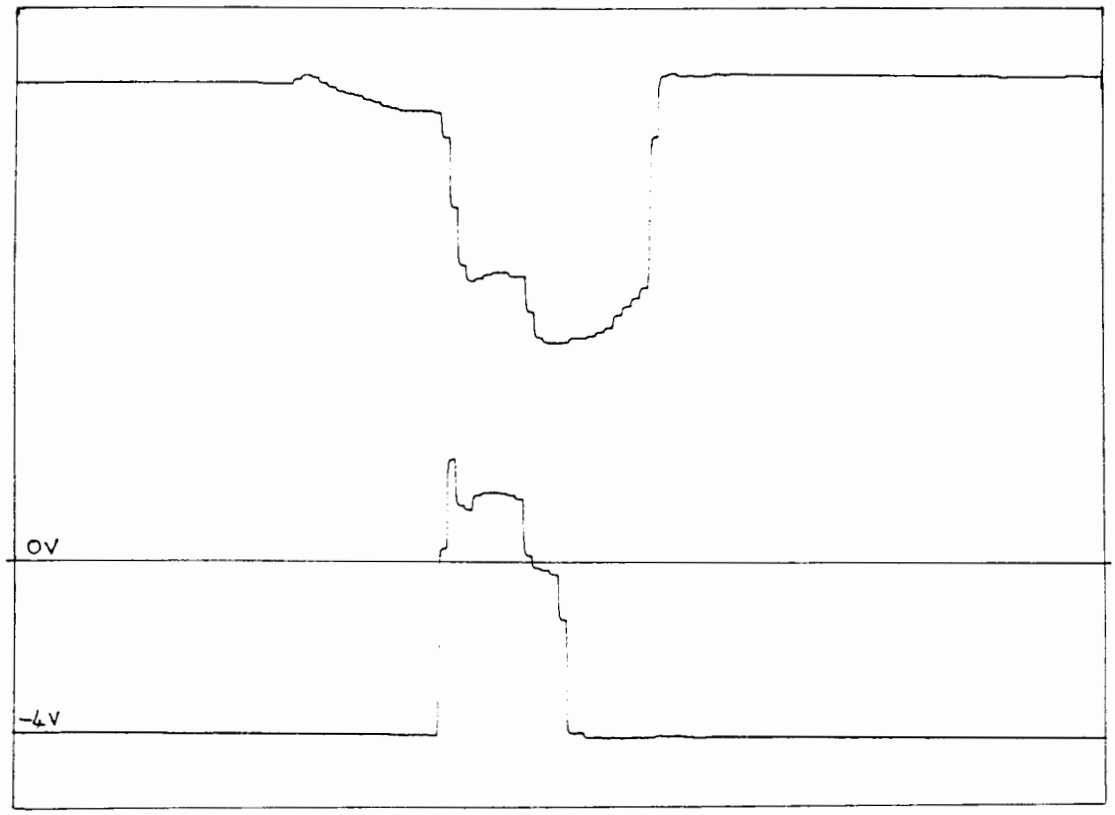

Figure 6.13 Base Drive Unlatching

The pulse width that results from this set up is 9us long, with a 4us storage time, totalling 13us. The longest time that the base drive will take to switch the transistor off under a fault condition is thus 13us.

The collector voltage falls when the transistor switches on and rises only when the other transistor in the same leg of the bridge switches on again. In between the two transistors being on, the collector voltage floats between 0V and rail voltage.

6.4 PSPICE SIMULATION OF THE BASE DRIVE

A Pspice program was written so that the operation of the base drive could be simulated by a computer. This allows the voltages and currents in the circuit to be determined by the computer simulation. The advantages of using a computer to simulate the base drive operation are:

- do not need the hardware, e.g. power supplies, PWM generator, etc.
- Can obtain current and voltages at all points without interrupting the current paths
- Can modify the circuit easily and obtain new results (especially good for designing new features into the base drive)
- Can simulate fault conditions easily.

This section discusses how the program was designed, how good the simulation is and gives an application of the use of the program.

6.4.1 The program design

Two versions of Pspice are currently available, the full production version and the evaluation version. Pspice consists of a number of programs; Pspice circuit simulation, a graphics post processor, a shell and a library of standard components. The full production version was not available, so the evaluation version was used. This version contains the same programs as the full production version, except the library consists of only a few basic components and the circuit size is limited. These limitations led to a few approximations in the circuit design.

6.4.1.1 Limitations of the Pspice Demonstration Version.

The Pspice demonstration version is public domain software. It is used to show a prospective Pspice purchaser the features of the program. It is therefore intended to be used only for small circuits. There is a

total of only 23 components in its library. The components that could be relevant to the base drive are: eight transistors, two diodes and one optocoupler. The library also includes pot cores, operational amplifiers and logic gates. A list of the relevant components [23] appear in table 6.14

COMPONENT	USE
2N2222A	NPN BJT Amplifier
2N2907A	PNP BJT Amplifier
2N3904	NPN BJT Switch
2N3906	PNP BJT Switch
2N3819	N-Channel JFET
2N4393	P-Channel JFET
IRF150	N-Channel MOSFET
IRF9140	P-Channel MOSFET
1N4148	Switching Diode
BD101	Switching Diode
4N25	Optocoupler

Table 6.14 Pspice component list

This version is not only limited in library size, but is also limited to the amount of components and nodes (component connections) that may be used per circuit. A total of only 25 nodes and a maximum of only 10 transistors may be used.

6.4.1.2 Component Substitution.

There are only two NPN, two PNP and one N-channel MOSFET in the library, which limits the choice of transistors that can be used in the base drive. The 2N3904 and the 2N3906 are both switching transistors that are similar to the transistors used in the low power circuits of the base drive. The power transistors on the output driver and the power Darlington have to be simulated by using these

transistors also. The output current must therefore be limited, otherwise these transistors will perform incorrectly. The N-channel MOSFET that is in the Pspice library, is the IRF150. This is a high current MOSFET with a high gate capacitance. This capacitance along with other values were altered in an attempt to create a model of the IRF520.

6.4.1.3 Circuit Limitations

The base drive requires eleven transistors, which is more than the evaluation version of Pspice allows. The input optocoupler and the push-pull pair on its output were omitted. This reduced the number of transistors in the circuit to eight. A voltage source was inserted in place of these components. This is discussed further in the following section.

The power Darlington was simulated by connecting two 2N3904 transistors in a Darlington configuration. The current at which the Darlington will saturate at, is around 200mA. The desaturation protection was connected to a voltage source, to simulate a variety of power transistor saturation situations.

6.4.1.4 Input Signal

The input signal was created by using a pulsed voltage source. This creates a pulse of any specified width or period. The rise and fall times of the switch can also be specified. The signal was used to substitute for the isolated PWM input. A pulse of arbitrary length was chosen to simulate one PWM pulse only. This rectangular wave can be treated as a pure voltage source, with no series resistance. A series resistance of 50 ohms was thus connected in series with the voltage source and the capacitor that produces the on and off pulses on the input of the flip-flop.

6.4.2 How close the Pspice model represents the Base Drive

Before using the model it is necessary to determine how accurately the results can be expected to represent the base drive. Plots were taken from both the computer model and the base drive to enable them to be compared. A circuit diagram of the Pspice model appears in Appendix C and a program listing appears in Appendix D. All components are numbered on the diagram. A plot of the input signal produced by V3 and the corresponding output signal (base of the power transistor), of the model is shown in figure 6.15.

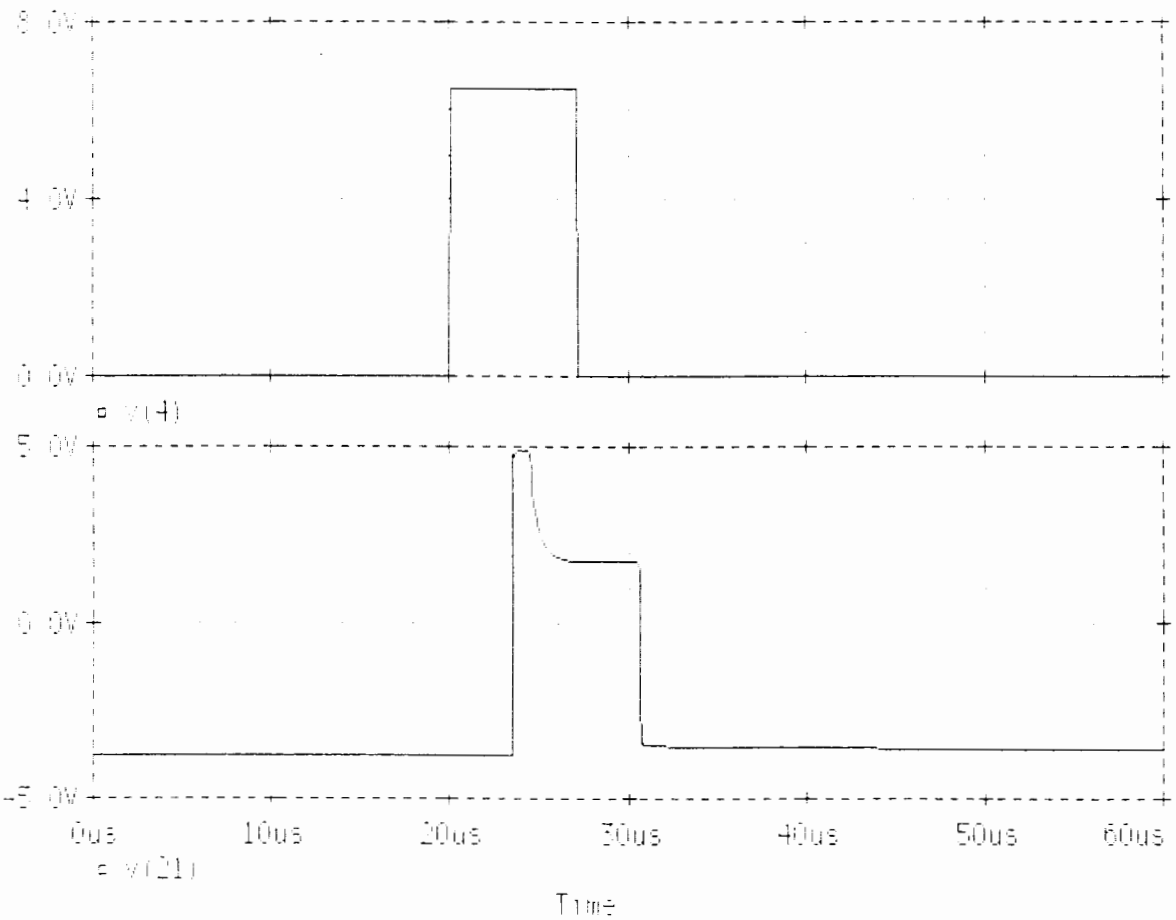

Figure 6.15 Pspice model of base drive input/output

A pulse was injected into the base drive model. The equivalent input/output signal of the actual base drive in

operation can be seen in figure 6.12. The input signals to both the base drive and the model are 7us long.

The output of the model is delayed for 4us, which is correct. A high voltage pulse then appears on the output due to the turn-on pulse generator (section 6.2.3.2). The "power Darlington" is two 2N3904's. These transistors do not have the same properties as a 150 Amp transistor. On switch-on, 8 Amps are injected into the base of the 150 Amp transistor. The base-emitter junction of the 2N3904's can obviously not conduct such a high current, which is the reason for the increase in the base-emitter junction voltage.

The model's output switch-off is delayed by 3.5us. In the base drive the delay is 3us, before a further 4us storage time delay. The 2N3904 does obviously not store the same charge and therefore has a reduced storage time.

From this example, the only differences to be observed between the simulation and the actual base drive are caused by the low current capability of the Darlington. The general operation of the base drive circuitry appears to be correct.

6.4.3 The Desaturation Protection Model

The Pspice model of the base drive has various uses. Some of these uses are listed below.

- It can anticipate results for a change in a design. Examples of this can be seen in section 9.4.
- It can model fault conditions such as desaturation of the power transistor, without having to cause a transistor to desaturate (at 400A).
- It can model the response of the base drive component tolerances, such as power supply fluctuation, resistance inaccuracies etc.

- It can acquire current and voltage measurements that could otherwise be difficult to obtain.
- It can model the stresses on components for transient waveforms e.g. current pulses in a transistor.

In this thesis the model is used to simulate a number of different situations. These simulations are: the desaturation of the power transistor, a loss in power supply and a change in base drive design. This section shows the result when the power transistor desaturates. The other simulations are presented in section 9.4.

6.4.3.1 The Model

This model possesses the same limitations that are discussed in section 6.4.1.1. A listing of the Pspice program and its associated circuit diagram is shown in Appendix D. Desaturation is simulated by disconnecting the desaturation protection network and connecting it to a voltage source (V4 at node 23). The operation of the desaturation protection network is discussed in section 6.2.4. The collector voltage at which the antisaturation protection network will switch the transistor off, is approximately 2.3V. How this voltage was derived will be discussed in the next section. The voltage source should thus switch from below 2.3V to above 2.3V at a time when the flop-flop is latched. This will cause the transistor to unlatch. Two cased have been simulated and appear in the following two sections.

6.4.3.2 Output waveforms: Case 1

The first simulation shows a transistor that saturates marginally above the 2.3V level. The rest of the base drive circuit voltages and currents are in a steady state condition. The graph in figure 6.16 show the waveforms on the output, in the flop-flop, and the simulated voltage on the collector of the power transistor.

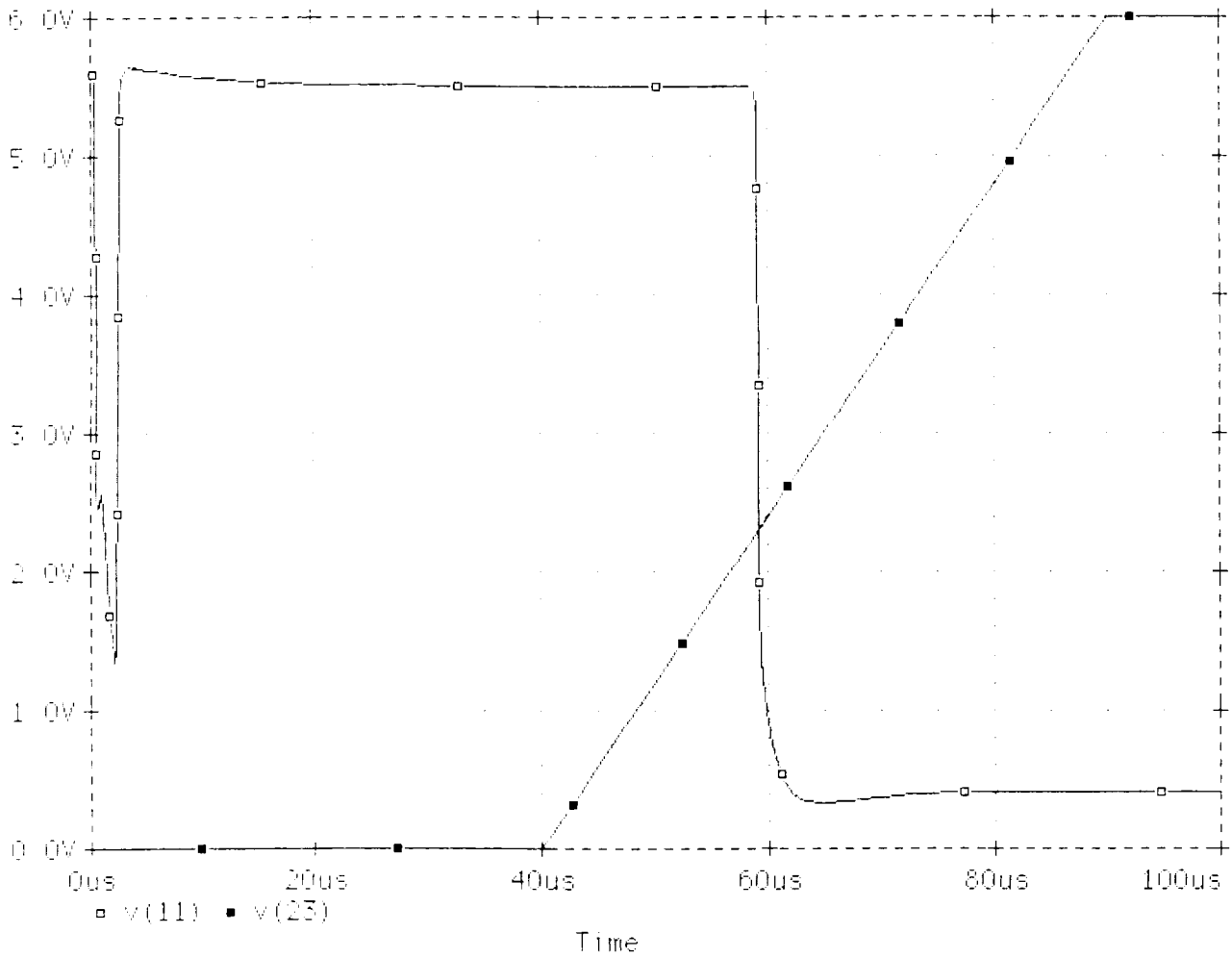

Figure 6.16 Simulated saturation after conducting for 50us
Node 11) Flip-flop status
Node 23) Simulated collector voltage.

From the transistor datasheets it can be seen that the saturation voltage may vary from a typical of 1.7V up to a maximum of 2.8V, at the maximum junction temperature. To enable the base drive to function correctly and to give adequate protection, it was decided that the desaturation protection cut-off voltage should be set at 2.3V.

This case simulates a transistor that reaches saturation, which could occur, for example, when the output of the inverter is slightly overloaded. The result is that the base drive unlatches when the voltage rises above 2.3V.

6.4.3.3 Output waveforms: Case 2

The collector voltage at which the base drive unlatches is not always constant at 2.3V. When the power transistor is switched on it takes a few microseconds for the collector voltage to fall. During this time, the desaturation protection must be disabled. The capacitor that conducts the pulse from the optocoupler to the flip-flop (C1) performs this function. When C1 conducts a pulse to latch the flip-flop on, the 2.3V cut off voltage set by the potential divider (R4 R5), is momentarily increased to approximately 6V. At this voltage the flip-flop cannot be unlatched by the desaturation protection network. The voltage on the potential divider then decreases as the capacitor is discharged. There is a time when the flip-flop can be unlatched, but a higher saturation voltage than 2.3V. This voltage decay is set by the time constant created mainly by C1, and R5.

This example considers the case when the power transistor collector voltage never falls. This could occur, if for example, a short circuit has occurred within the bridge and the DC bus is short circuited through a transistor. The simulated collector voltage is held constantly at 6V even after the transistor has switched on. Figure 6.17 shows the graph of the flip-flop voltage, the power transistor collector voltage and the base drive output voltage.

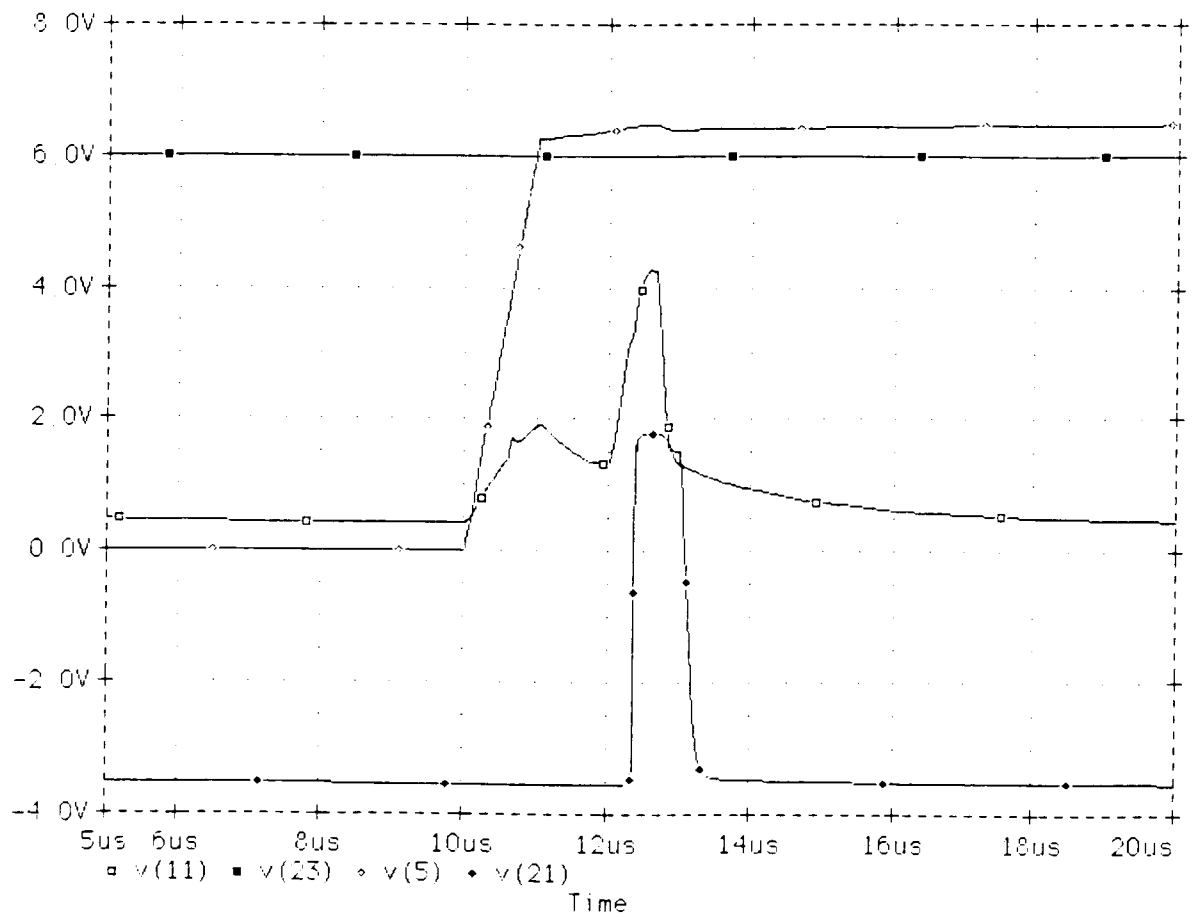

Figure 6.17 Simulated saturation when the transistor switches on
Node 11) Flip-flop status
Node 23) Simulated collector voltage
Node 21) Base drive output
Node 5) Rising PWM edge

From the graph it can be seen that the output of the base drive is high for around 1us. The flip-flop then unlatches and switches the output off.

This simulation means that when a short circuit occurs in the bridge, the transistor will turn on for 1us per rising edge of the PWM pulse. From the data sheets it can be seen that the transistor is capable of withstanding 600 Amps for 50us at a voltage of 250V.

From the transistor datasheets, the time the transistor can withstand 3.5 times rated current is 50us [24]. The 1us pulse is therefore well within the specifications. The amount of times that this can be repeated is obviously dependant on the severity of the fault.

At maximum junction temperature[13], the transistor takes 4us to reach 300A when switched on. After 1us the transistor is therefore not conducting the full 300A. This reduces the storage and fall times.

6.5 MECHANICAL MOUNTING AND STRUCTURE OF THE BASE DRIVE

The physical structure and the mounting of the Base drive are both very important to the operation of the base drive. Problems were encountered with the base drive in the push-pull inverter, that would not have occurred, had a few basic construction principles been adhered to.

The original base drive was mounted in a cabinet, separate from the power transistor to screen the electronics from electromagnetic interference. The cables linking the two components were almost one metre long. These cables conduct high current pulses to switch the power transistor on and off. Potential difference along the length of the cable, lead to the incorrect operation of both the Baker clamp and the desaturation protection network.

The base drive for the full bridge inverter was constructed so that the circuit board could be mounted directly onto the power transistor by means of screws. This eliminated the cables linking the two components along with the problems associated with it. A photograph and an explanatory diagram of the base drives mounted on the transistors, in the converter, can be seen in figure 3.4.

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13 - Exceeding the transistor junction temperature will cause the destruction of the transistor under these conditions.

With careful wiring and component layout electromagnetic interference can be minimised so that it has no significant effect on the circuit operation. Electromagnetic interference can also be reduced by careful positioning of the components on the circuit board [1]. Tracks connecting components should be short, direct and their return paths should encircle as little area as possible. This will reduce the flux area. If the circuit is designed to take a high current, e.g. in potential dividers, the circuit will be less susceptible to interference. Any currents induced by interference will be small relative to the existing current and will thus cause only insignificant voltage changes.

The isolation should be separated from the driver, to reduce input to output capacitive coupling. A capacitor represents a low impedance path to high frequencies. A low capacitance coupling is thus necessary to maintain the high impedance from output to input that the optocoupler provides. Physical separation between input and output is also necessary, to maintain the high voltage isolation that the optocoupler provides. The 600V DC isolation must be maintained even when dust and moisture settles on the circuit board. A photograph of the base drive mounted on a transistor can be seen in figure 6.18.

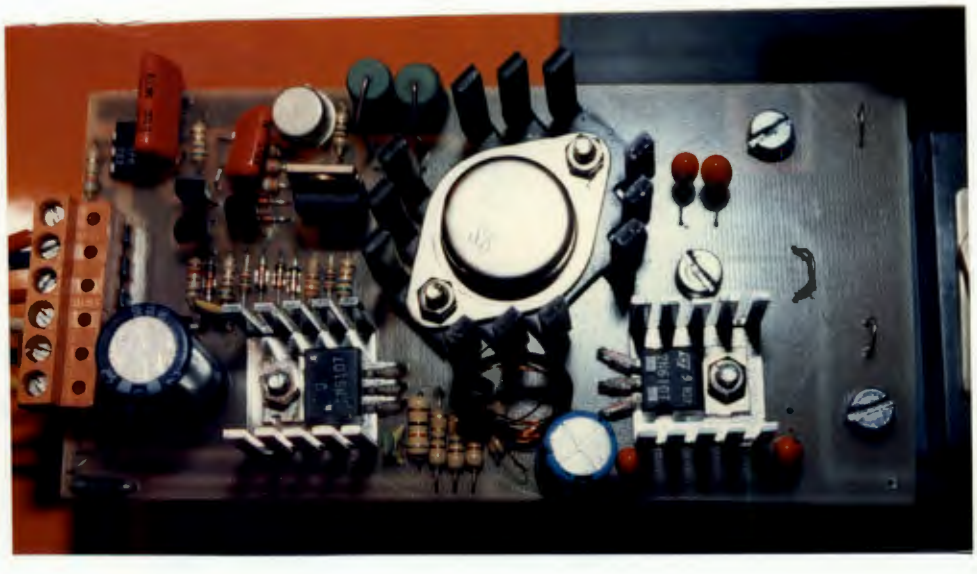


Figure 6.18 The Base Drive

The component positioning and the circuit layout was done on Smartwork, a computer program. A diagram of the components and the Smartwork layout is shown in Appendix C.

CHAPTER 7

THE COMPUTER HARDWARE AND SOFTWARE

The inverter is controlled by a computer. This computer interprets signals from the Soudronic and from the dials on converter, to generate an appropriate sine weighted pulse width modulated (PWM) signal. The PWM signals are used to control the transistors in the inverter. The inverter generates a sine wave from the PWM, at a specified frequency and voltage.

7.1 THE COMPUTER HARDWARE

The computer is based on the Motorola 6809 microprocessor. This section discusses the microprocessor and its support components.

7.1.1 The Microprocessor and its Circuit Board

The 6809 IC is an eight bit microprocessor. The version of 6809 that was used is driven by an 8 MHZ clock. A 6809 prototyping circuit board was used. This board was developed by the department of chemical engineering of the University of Cape Town. The board consists of blank spaces where a wide range of microprocessor support components can be inserted. It is not necessary to insert all the components in the board, but only the specific components that are required for each particular use. A diagram of the circuit board layout is shown in Appendix C.

7.1.2 The Programmable Interrupt Timers

The PWM is generated in real time. It is therefore necessary to maintain a real time reference when the computer is operational. This reference is produced by two Programmable interrupt timers. The timers are given a number, which represents a length of time. The timer uses the 8 MHz crystal as a reference and counts for the specified time. Once the timer has completed counting the time, it interrupts the microprocessor.

Two timers are used to generate the pulse widths and the time intervals between consecutive PWM pulses. There are two PWM signals. Each timer controls the pulse width of one of the two PWM signals. Whilst one timer is generating the pulse for one PWM signal, it is also generating the time between two pulses for the opposing PWM signal.

7.1.3 Parallel and Serial ports

The communication between the microprocessor and the external circuitry is controlled by two 16 bit parallel input/output (PIO) ports, and one serial (RS232) port. The serial port was intended to be used to communicate with an external computer. This was later deemed unnecessary and the serial port became redundant. The parallel ports can be configured as either inputs or as outputs. If a bit is configured as an output, the microprocessor will set this bit either high or low. The port will hold this state until the microprocessor changes it. If a bit is configured as an input the microprocessor may access the state of this input at any time.

The parallel ports control the inputs from the Soudronic and the frequency and voltage dials on the converter, as well as the two PWM outputs to the inverter. The two PWM signals from the parallel port were connected to an inverting buffer (7404), to provide the current drive for the optocouplers on the base drives.

The voltage and frequency dials have binary coded decimal (BCD) outputs each ranging from 0000 to 1001 (0-9), thus requiring 4 bits per decimal digit. The voltage dials ranges of 00 to 99 decimal, or 0000 0000 to 1001 1001 BCD. Each voltage input thus requires eight bits. The frequency dial has only three inputs available. These inputs were connected to the three least significant bits of the dial. The frequency thus has a range of 0 to 7 or 000 to 111. The parallel port connection for the two chips is shown in figure 7.1

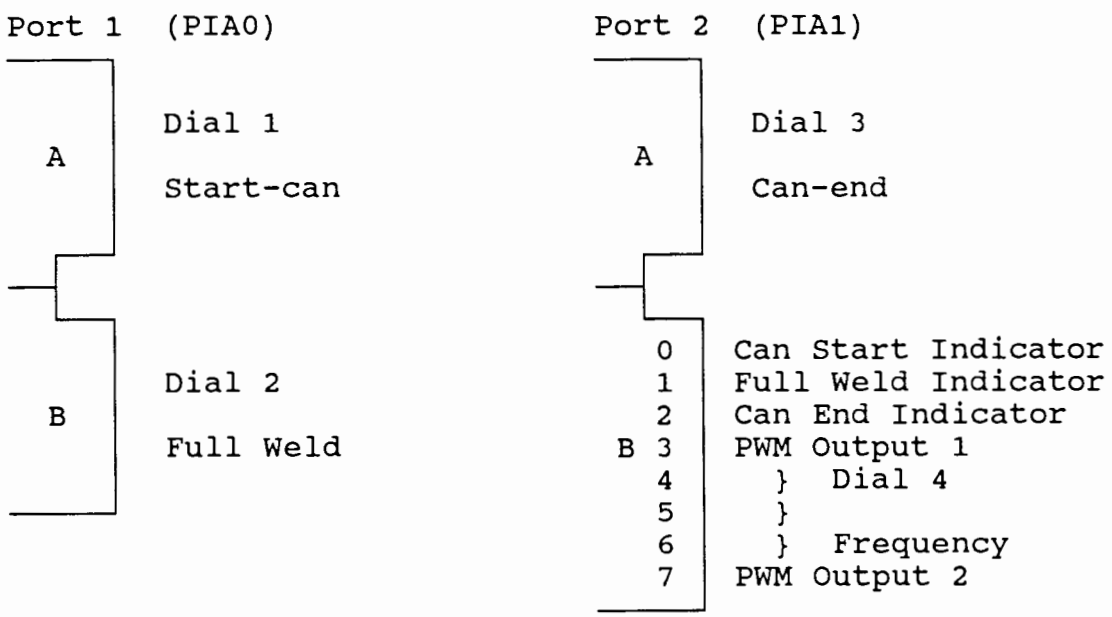


Figure 7.1 Parallel Port Connections

7.1.4 The Memory

The program was written in Motorola 6809 assembler, and programmed onto an EPROM (2764 IC). One EPROM contained the entire program. This IC was changed many times during the design and testing of the program, until the program was regarded as satisfactory. A RAM IC (6254) was used as a memory for variables and the stack during the program operation.

7.2 THE PROGRAM STRUCTURE

This section discusses the final program design that was used in the full bridge inverter and does not discuss the design process. Section 8.4 discusses the dominant problems that occurred during the software design process. A program listing, as well as an explanatory flow chart, is shown in Appendix E. All discussion on areas of the program associated with the serial port have been omitted, as it was not used in the final converter.

7.2.1 Initialising the computer

The program begins by initialising the parallel ports and the timers. The program variables are loaded and are stored in the RAM. The parallel ports are configured so that 2 bits are outputs and the remaining 30 bits are inputs.

7.2.2 The Main Program Loop

The program then starts a continuous loop. For every can the program is executed once. At the end of every can the ports are read to acquire the voltage and frequency dial settings. If any setting has changed since they were last read, all the PWM tables are re-calculated. The tables are re-calculated by first reading the appropriate PWM tables from the EPROM. All the numbers on the table are then multiplied by the number set by the frequency dial. This provides for the frequency adjustments. The modified tables are then stored in allocated sectors in the RAM. An in depth description of how the PWM is generated is given in Appendix F.

At this stage the converter is waits for the Soudronic to signal that a can is ready to be welded. So far it has been assumed that the weld cycle always has a can-start, a full weld and a can-end. This is however incorrect. When the Soudronic is being set up, the operators remove the can start and can end, to set the full weld accurately.

The can-start and can-end are added later. The computer is idle until the Soudronic signals for one of the three weld states. When a state is signalled, a flag is used to signal that a can has arrived, the interrupts are enabled and the timers are initialised. A pointer is then set to point at the table that represents the weld state (e.g. can start) and the PWM is generated. The computer continues in this weld state until another legal state occurs. The pointer is then changed to point at the next table (e.g. full weld). If the next state is no-weld, the flag will be changed to signal that the can has passed. The interrupts and timers are then disabled and the PWM ceases. The dials on the converter are read again and the program continues from the start of the loop.

7.2.3 The Interrupt Handler

The interrupt handler (IH) is only operational when the converter is in one of the three welding states. There are two PWM outputs. The IH toggles both the outputs and resets the timers so that they can re-interrupt the program. A pointer is set by the main program to point at a number in the table that is currently in use. Each time the IH is activated, the value that the pointer is currently pointing to, is output to a timer. The pointer is then changed, to point at the following value in the table. If the next value in the table is a zero, i.e. the table has ended, the pointer is reset to point at the beginning of the table.

7.3 SOUDRONIC-COMPUTER ISOLATION

Isolation between the Soudronic and the computer is achieved by means of optocouplers. Three outputs from the Soudronic, can-start, full weld, and can-end are coupled optically. There are therefore three optocouplers. There is also one input that drives the coil of a relay, that disables the converter in an emergency.

7.3.1 Optocoupled isolation

The Soudronic provides a 10mA current for a high state and no current for a low state. This 10mA is intended to drive the LED of an optocoupler. The cable linking the two machines is approximately 10 metres long. A screen around the three signal wires protect the signals from interference, but this is not sufficient. so the signals are filtered. A diagram of the optocoupler circuit is shown in figure 7.2.

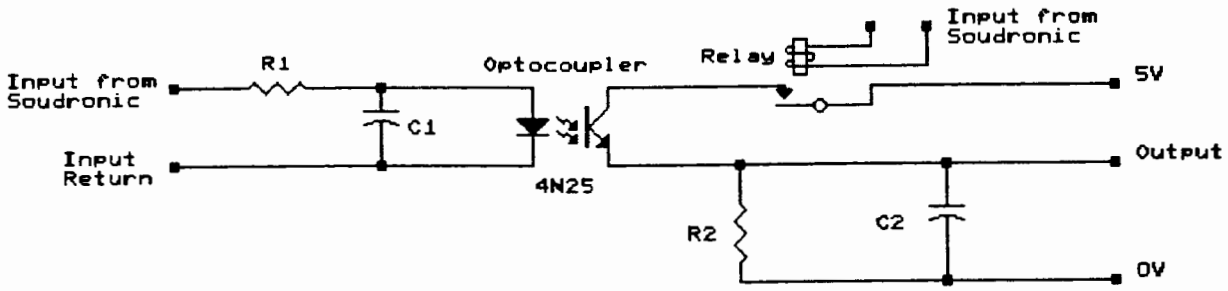


Figure 7.2 Diagram of the Optocoupler circuit.

The speed at which the optocoupler switches is not critical, as long as the computer interprets the switching correctly. The optocoupler that was used is a 4N25, with turn on and off times both below 10us. The delay from when a weld state is requested, until the weld occurs, is irrelevant, as long as this delay is constant. There are settings on the Soudronic that vary the times at which the different weld states occur. The circuit may therefore have filters that constantly delay the signals, as the settings on the Soudronic can be adjusted to compensate for it.

The circuit diagram shows two RC filters, one on the input of the optocoupler and one on the output. R1 was used to limit the current into the LED. The outputs of the Soudronic are current limited, but R1 was necessary to limit the current in the case of interference. R1 and C1 provide a low pass filter for this interference. When the Soudronic gives a high output, the LED and the

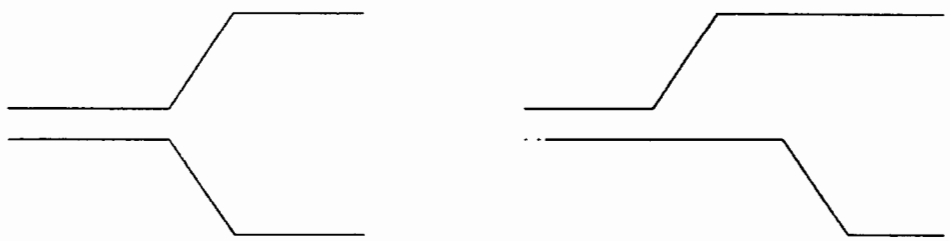
opto-transistor both switch on. When the transistor is on, there is a voltage of around 4.5V on the output. When the transistor switches off R2 discharges C2 and the output voltage drops to 0V. R2 and C2 form a low pass filter when the transistor is on and gives a delay when the transistor switches off. When the transistor switches on there is little delay.

7.3.2 The Converter Emergency Disable

Switch SW1 is operated if the converter is to be disabled urgently. It provides the emergency disabling function explained in section 2.1.4. The switch is a relay that is operated off a 220V AC signal. The power to all the optocouplers is removed when the relay is activated. This forces all the output voltages of the optocouplers to fall to 0V, being pulled low by the resistors (R2). The computer senses this and disables the outputs.

7.3.3 Signal overlaps

The delays that are generated by the capacitors on the output of the optocoupler cause two consecutive signals from different optocouplers to overlap. If the outputs are not overlapped, there is a transition zone, when one output is rising and one is falling. The waveforms of two outputs, both with and without an overlap, are shown in figure 7.3.

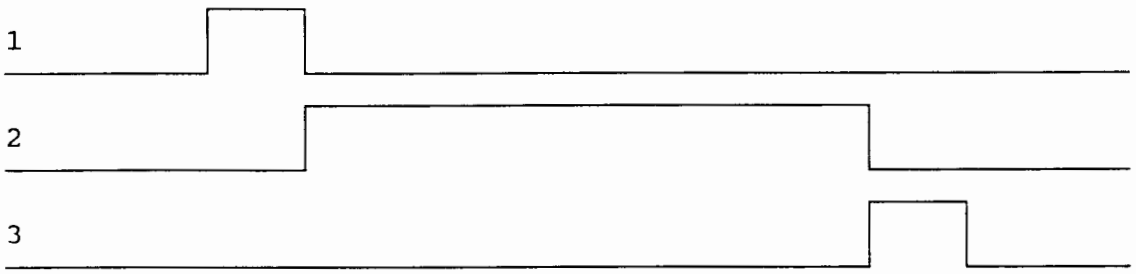


a) Without Overlap b) With Overlap

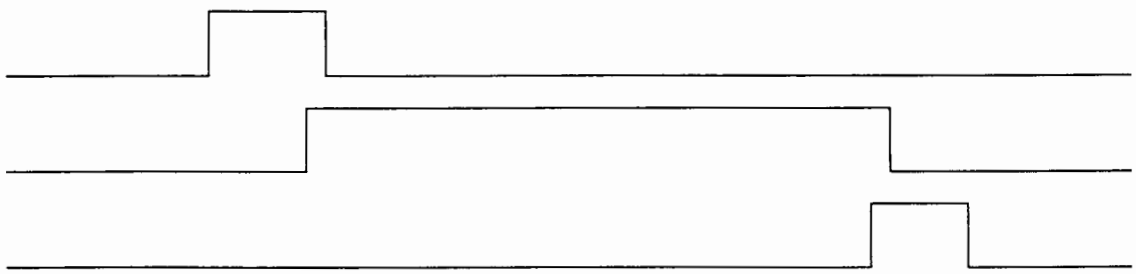
Figure 7.3 Waveforms of two outputs

If a transition occurs without an overlap, there is a time when the states of both signals are undefined. This could mean that all signals are interpreted as being low. This state is the same as when switch SW1 is open. The computer will thus interpret the transition as the end of a can. The computer will thus cease producing the PWM. The parallel ports will be read and after a short time, when the states are again defined, the computer will start to produce the PWM. There is thus a period of time when the can is not welded. This leaves a gap in the weld.

If a transition occurs when there is an overlap, it is not possible for all the outputs to be low at any time. This overlap produces an illegal state, when two inputs are high and one output is low. When the computer detects an illegal state it continues in the previous legal state. When the delay has passed and the state becomes legal again, the computer will change state. The overlap thus prevents a no-weld state occurring, but produces a delay. The input and output signals that result from the optocoupler circuit are shown in figure 7.4.



a) Input



b) Output

Figure 7.4 Signals from the optocoupler circuit

CHAPTER 8

DIFFICULTIES EXPERIENCED DURING THE DESIGN PROCEDURE

Throughout the explanation of the converter, some of the design problems have been mentioned. This section brings together all the major obstacles that arose during the design and discusses them in detail. It is necessary to be aware of the faults and their solutions, to ensure that they do not re-occur in future converters and to complete the learning experience.

8.1 OUTPUT TRANSFORMER SATURATION

The output transformer was constructed by an outside contractor. As has been mentioned earlier, the transformer was constructed out of "C" cores. Normally "C" core inverter transformers are constructed with an air gap in the magnetic path, between the two cores. This airgap is necessary as it allows a DC current offset to decay [26]. A current offset occurs in an inverter because of an imbalance, for example in the PWM, or for the reasons discussed later in section 8.4.3. If the airgap is large, the DC offset decays rapidly, but losses associated with the airgap increase.

The inverter transformer was originally constructed without an airgap. This resulted in a DC current build-up in the inverter. An oscillogram of the current in the primary winding of the full bridge output transformer can be seen in figure 8.1. The centre of the graph is the 0 Amp level and the current scale is 100 Amps per division.

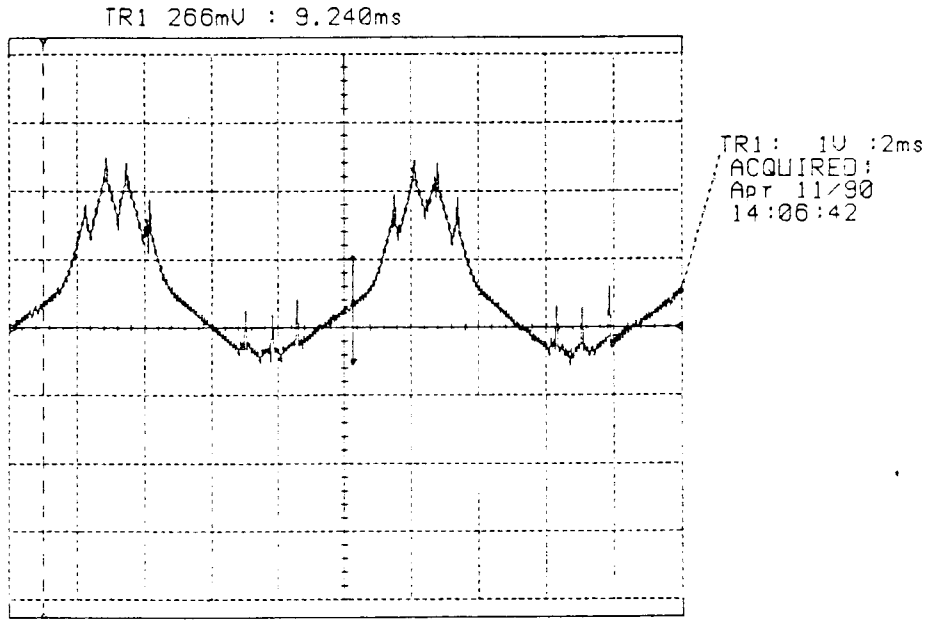


Figure 8.1 DC offset Current in primary winding of the output transformer

The trace shows a DC offset of approximately 80 amps. This caused extensive overheating of the inverter transformer, choke, and two of the transistors. An airgap of approximately 0.8mm was inserted in each of the four legs of the core. This reduced the DC offset to below 10Amps, which was considered acceptable.

8.2 EARTHING, NEUTRAL AND SIGNAL NOISE

Earthing in power electronic equipment is of upmost importance. Often, not enough consideration is given to ensure that it is correct. This was certainly the case for the original push-pull converter. By the time the full bridge converter was constructed, enough experience had been gained to avoid these earthing difficulties.

8.2.1 Noise on the Inverter 0V rail

In the push-pull converter, all the electronics shared a common 0V rail, i.e. the computer, both base drives and both transistor emitters were connected to the inverter

negative bus. The various components were not connected to the same junction. This created earth loops, which resulted in problems with the latching circuit of the base drive.

The full bridge converter was constructed so that the base drives and the computer were isolated from each other and also from the DC bus. No earthing problems were detected on the full bridge inverter.

8.2.2 Neutral-earth noise

Both the earth and neutral wires for the converter were taken from the Soudronic. The two machines are approximately 5 meters apart. This resulted in cables of almost 10 meters linking them.

The chassis of the converter was connected to earth, to comply with safety regulations and absorb electrical interference. The neutral wire (along with a phase) was primarily required to supply 220V AC to power to the control electronics transformers. For the push-pull inverter, it was also connected to the star point of the input transformer's secondary windings. The connection was made to prevent the inverter voltage from drifting from earth potential. This had the effect of connecting the inverter negative bus, along with the computer, transistor emitters and the base drives to the neutral wire. The factory earth and neutral were not at the same potential, instead, a large amount of noise existed between them. An oscillogram of the potential difference between earth and neutral can be seen in figure 8.2.

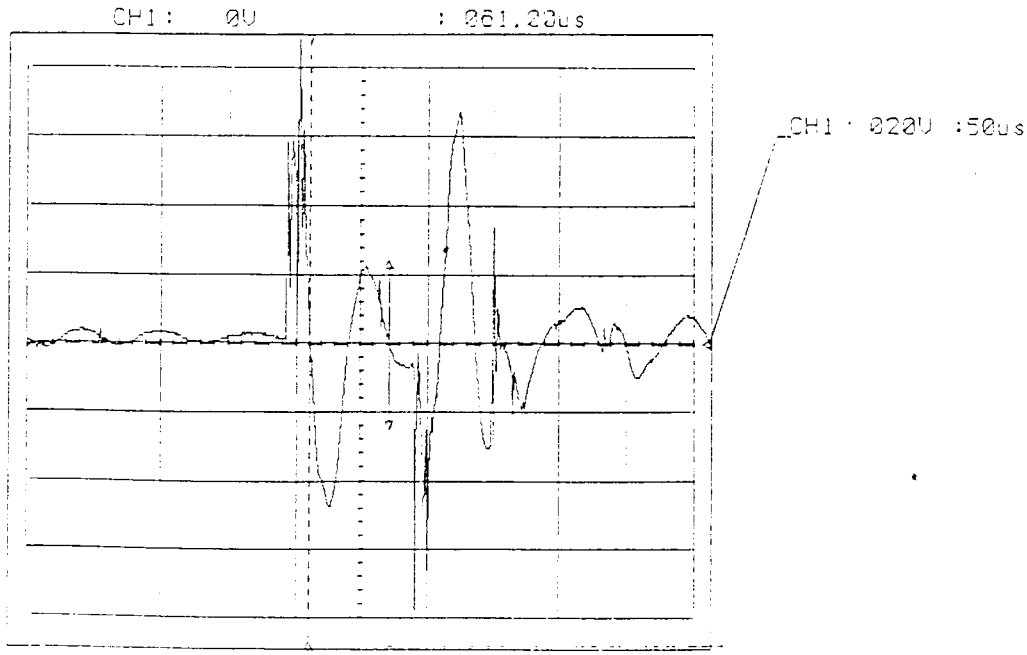


Figure 8.2 Potential difference between Earth and Neutral

From the trace, it can be seen that voltage differences of up to 90V existed between earth and neutral. The PWM waveforms from the computer distorted, because of capacitive coupling between the circuit and the chassis. This caused the base drives to latch on falsely, with obviously undesirable results. For the full bridge inverter, the neutral connection was removed from the DC Bus and was replaced with an earth connection. This removed all capacitive coupling.

8.2.3 Soudronic Signal Noise

The can start, full weld and can end signals are transmitted from the Soudronic to the converter along a screened cable that is 10 metres in length. All the cables connecting the Soudronic and the converter are in the same truncking, i.e. the signal cables run parallel to the power cables for 10 metres. Even though the signals were screened, interference was still transferred to them. A graph of the output of two optocouplers is shown in figure 8.3.[14]

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14 - A digital storage oscilloscope was set to max-min glitch capture to obtain this trace.

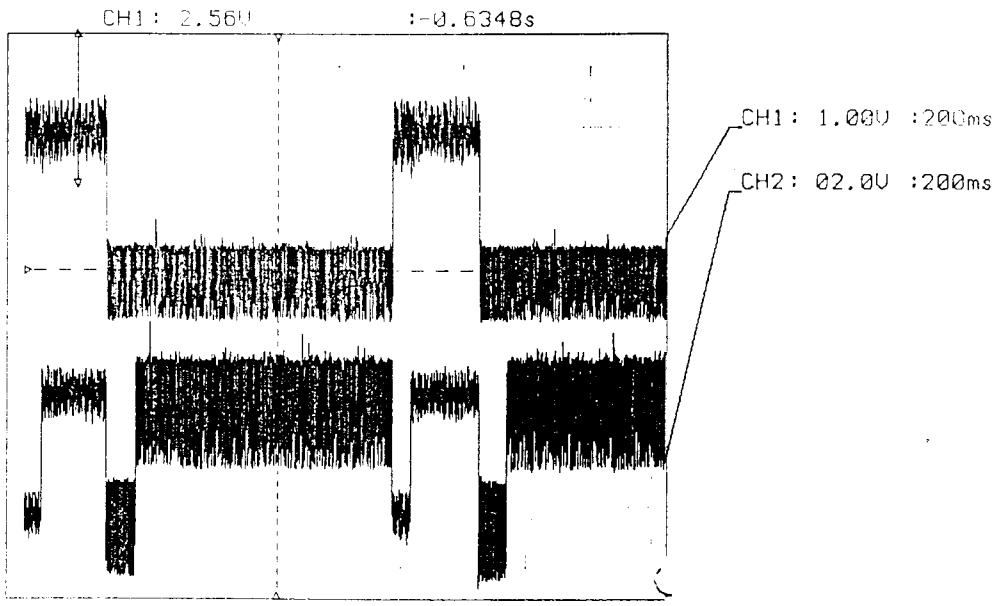

Figure 8.3 Noise on the Output of the Optocoupler

The interference on these weld signals caused illegal states. The illegal states had the effect of creating areas on the can where that were not welded[15]. A resistive load was connected to the signals on the input of the converter to increase the signal current. This has the effect of increasing the signal to noise ratio. A low pass filter was also connected to the signals on the input of the optocouplers. The output of two optocouplers after the circuit was modified, can be seen in figure 8.4. Once the modifications had been made, no further illegal states occurred.

15 - A discussion of how illegal states can cause areas of no-weld is given in section 7.3.3.

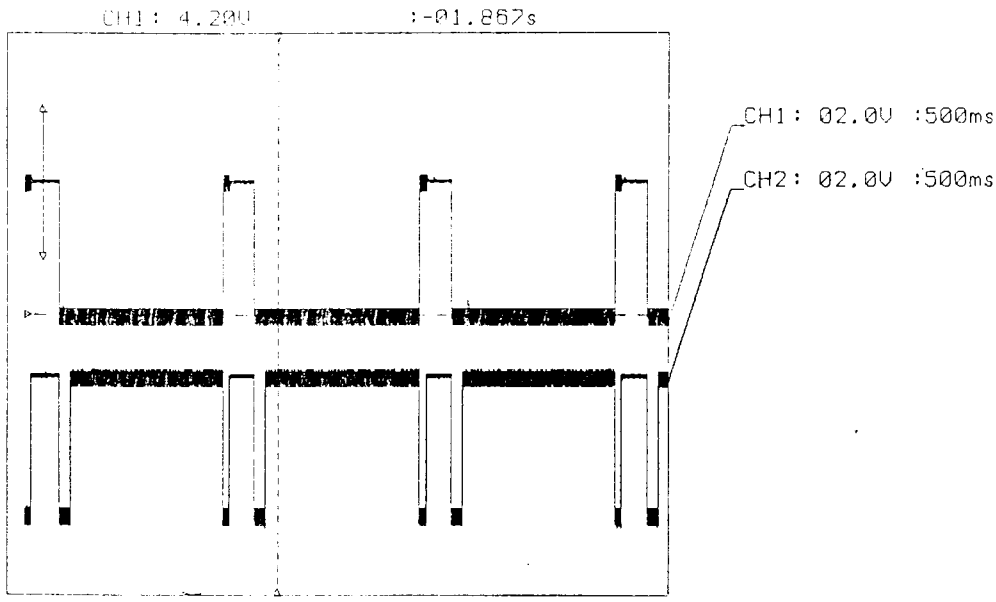

Figure 8.4 Corrected output of the optocoupler

8.3 BASE DRIVE PROBLEMS

Two major difficulties were experienced with the base drive, firstly with the signal input isolation and secondly with the Baker clamp. The input isolation used on the full bridge inverter base drives, was initially in the form of pulse transformers, but was later changed to optocouplers. This change took place because pulse transformers were found to have problems associated with them. The input isolation is discussed further in section 6.2.1. The Baker clamp was found to cause oscillation in the level of saturation of the power transistor.

8.3.1 Pulse transformer v/s Optocoupler

A pulse transformer represents a low impedance path in both directions, input to output and output to input. When the flip-flop latched on, a pulse was transferred from output to input. This caused oscillations in the latching circuit. If a stray pulse was generated due to interference on the leads connecting the computer to the pulse transformer, the flip-flop could be latched on

falsely, with devastating results. An optocoupler does not have either of these problems for two reasons:

a) - it represents a low impedance from input to output and a high impedance from output to input and

b) - it transfers the entire PWM signal[16].

If a stray pulse appears on the input of the pulse transformer, the flip-flop will latch on, whereas if a pulse appears on the input to the optocoupler, the flip-flop will latch on, then off again when the pulse disappears. If the pulse is short enough, the power transistor may not even switch on.

8.3.2 Baker Clamp Oscillations

The purpose of the base drive is to maintain the power transistor in a state of quasi saturation. The Baker clamp did not hold the transistor in a constant level of saturation, but it oscillated between being heavily saturated to being de-saturated. The oscillations were enough to cause the antisaturation network to eventually switch the power transistor off. An oscillogram of the base voltage of the power transistor can be seen in figure 8.5.

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16 - A pulse transformer transfers the PWM only in short pulses, whereas the optocoupler transfers the unmodified waveform.

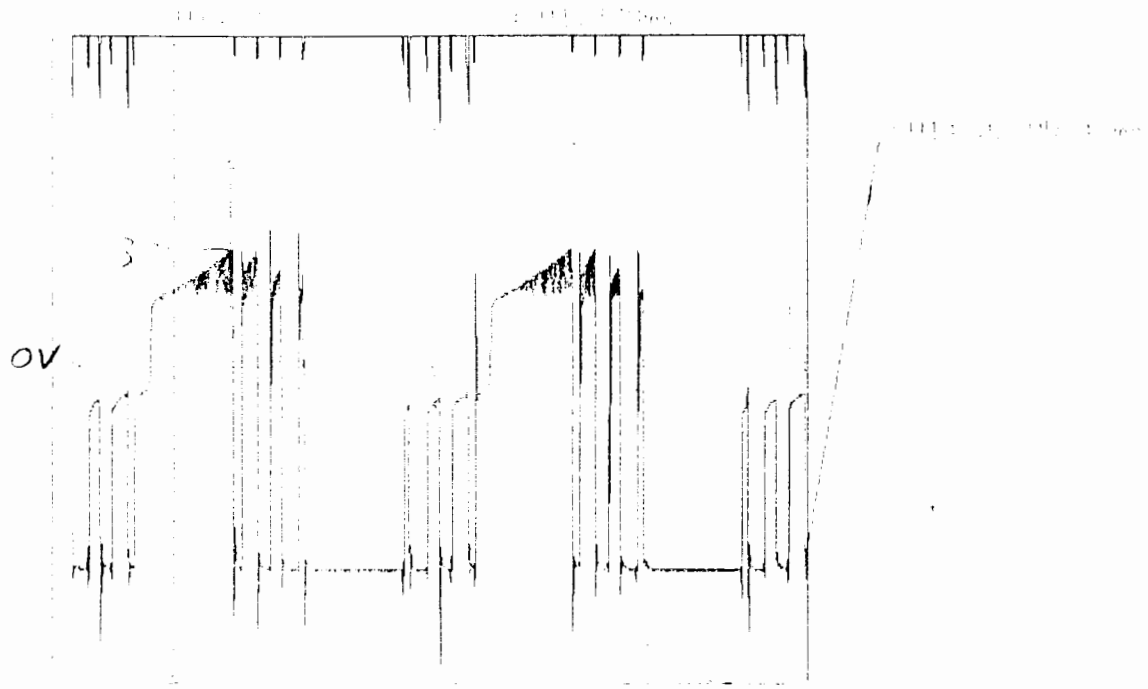

Figure 8.5 Oscillation on the base of the power transistor

The oscillations were caused by a delay in the response of the Baker clamp which gave rise to positive feedback. This delay was caused by a slow Baker clamp diode (D6), a slow driving transistor (Q5) and 0.5m cables linking the transistor and driver. See section 6.2.3 for circuit details. Due to the limited availability of high powered switching components at that time, the diode and transistor could not be replaced by faster equivalents,

The oscillations caused two undesirable effects, firstly, the antisaturation network switched the power transistor off at low collector-emitter currents and secondly, the power transistor RMS conduction voltage and thus total conduction losses were high.

A resistor (R12) was connected in series with the Baker clamp diode. A resistor connected in series with the feedback diode is recommended by Ripple [26], to improve the conduction losses. A resistor in the feedback loop dampened the oscillations and decreased the amplitude of the feedback positive feedback. With a resistance of 0.33 Ohms all oscillations were removed. An oscillogram

of the base voltage of the power transistor, with a 0.33 Ohm resistor in the Baker clamp, can be seen in figure 8.6.

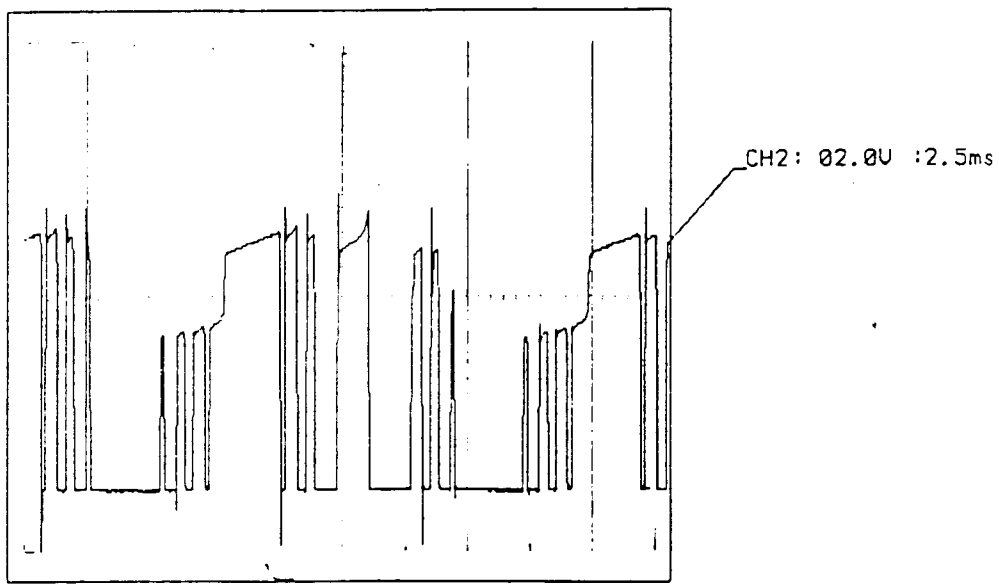

Figure 8.6 Corrected base drive output voltage

The 0.33 Ohm resistor has little effect on the normal operation of the circuit. The current through the resistor ranges from 0 to approximately 100 mA. The highest current in the diode occurs when the least current flows through the collector-emitter junction. This current gives rise to a 33mV drop across the resistor, which reduces the collector-emitter voltage drop by approximately 33mV.

8.4 SOFTWARE MODIFICATION

The original version of the program was written by and outside contractor. Difficulties were experienced with the computer, as the program was not suited to a power electronics environment with the Soudronic. For an explanation of the software, see section 7.2.

8.4.1 PWM Overlap

At first, only one PWM output was generated by the computer. This output was inverted externally to provide the two 180^{o} out of phase PWM waveforms. One problem with this is that the computer can not disable both outputs, as one of the outputs will always be in the high state. Both the signals therefore, have to be buffered to create two low outputs when a no weld is desired.

The next problem is that there is no dead time between one transistor being switched off, and the other being switched on. A dead time of approximately 20us is necessary, to ensure that the conducting transistor switches off.

The program was re-designed so that two bits of the parallel port were reconfigured to be PWM outputs, 180^{o} out of phase from each other. A dead time of 20us, between pulses was created.

8.4.2 PWM Modification

The PWM is generated by converting 100 different pre-calculated tables of 15 values into pulse high and low times. These tables were constructed to create a 15 pulse sine weighted PWM. In the case of overmodulation, (modulation factor > 1), the PWM should have less than 15 pulses per cycle. An example of a PWM signal with a modulation factor of two is shown can be seen on page F4 of Appendix F.

The program had a fault that made it create a PWM which always had 15 pulses per cycle. Each table contains 16 values, the 16th value being zero (to indicate the end of a table). As a zero signals the end of a table, it cannot be used in the middle of a table. When it was necessary to delete a pulse, the value was not set to one. This can be seen in the tables in Appendix E. If the PWM is inverted, even for a unit of one, the delay of 20us per switch still occurs, i.e a minimum pulse width is 40us.

An example of the PWM resulting from table 100 before the program was modified is shown in figure 8.7.

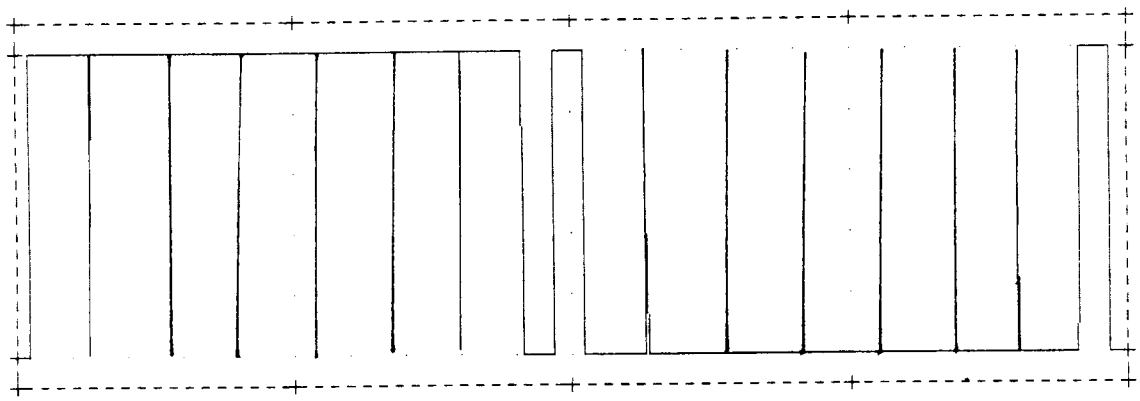

Figure 8.7 Incorrect computer generated PWM

This type of PWM gave rise to two problems. Firstly, the transistors had to switch excessively, generating high switching losses. Secondly, the total time the transistors were conducting for was greatly reduced, which decreased the maximum output current and voltage.

The program was modified to detect a value of one in the table. If this value is one, the next value in the table is obtained and transmitted to a timer. The PWM output remains in its previous high or low state. This has an effect of bypassing values of one, which results in a correct PWM output.

8.4.3 DC Offset

This section is closely linked to section 8.1 in that the DC offset gives rise to the transformer saturating. This section points out two problems that cause the DC offset. Appendix G describes how a DC offset gives rise to saturation in a transformer.

8.4.3.1 Start of a can

In between cans the converter is off and no current is produced. As soon as a can reaches the rollers of the Soudronic, the inverter energises the transformer and load with an AC current. Appendix G shows that if an inductive

load, such as the welding transformer, is switched on at a voltage zero, a DC offset occurs. The peak transient current can reach as much as twice the peak steady state current [27]. This can cause the transformer to saturate.

When the PWM is activated, it starts at the beginning of a table, which is also a voltage zero. A DC offset thus occurred at the beginning of each can.

To resolve this problem the voltage start of a can was set low for the first half cycle. This has the effect of creating a small DC offset both positively and negatively, which resulted in a low combined offset. This was probably not the most desirable solution, and another approach is suggested in section 9.1.

8.4.3.2 During the Weld

Along the length of a can, the inverter generates three voltages. The Soudronic signals when the voltage should change from one state to another. Each time the table was changed, the PWM would re-start from the beginning of the next table. This could cause two consecutive half-waves to both be either positive or negative. An example of this is shown in figure 8.8. Note the DC offset.

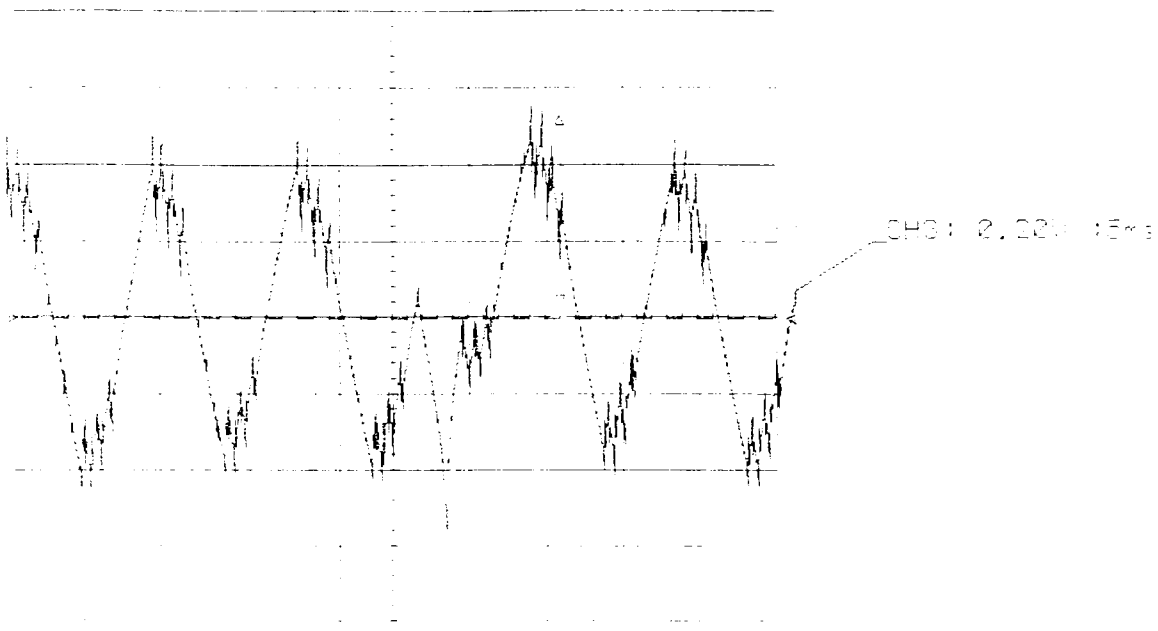

Figure 8.8 Inverter current at change over

The program was modified so that when the computer begins reading another table, it starts at the following value in the next table, e.g. if the program was reading value number 10 of table 50, the following value read would be value number 11 of table 70, assuming table 70 is the new table to be read. This eliminated the possibility of having two consecutive positive half cycles. The corrected inverter current can be seen in figure 8.9.

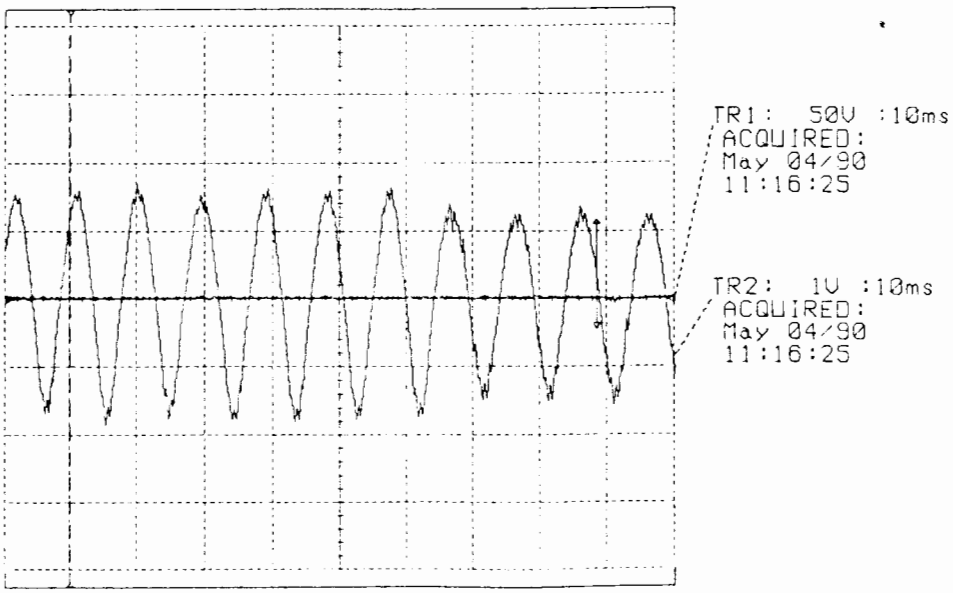

Figure 8.9 Inverter Current after the Modifications

CHAPTER 9

SUGGESTIONS FOR FUTURE CONVERTER DESIGNS

Since the completion of the converter, research continued into the design of similar converters, used in Uninterruptible power supplies. This research has revealed certain areas in the converter that could be improved upon. This section discusses the changes that could be made to the converter to improve upon the overall performance.

9.1 SOFTWARE MODIFICATION RECOMMENDATIONS

Later on in this chapter a suggestion is made to replace the computer with an analogue PWM generator. This section assumes that the computer is to be used in the converter. The modification suggestions are accompanied by an untested software alteration that should achieve the desired goals.

9.1.1 DC offset at start of can

Section 8.4.3.1 discusses the problem of switching an inductive load on and the resulting DC offset that can occur. A DC offset arises when an inductive load is switched on at a zero crossing. The problem was reduced by decreasing the voltage for the first half cycle. This does not solve the problem, but reduces it to an acceptable level.

The problem should be solved by removing the DC offset altogether. To remove this offset, the PWM must start at

a voltage peak.[17] This can be achieved by either changing the program to begin reading from the middle of the selected table, of by re-ordering the elements of all the tables. The second suggestion is probably the easiest. An example of a selected few modified tables is given in figure 9.1.

Table 1 :
121,119,121,119,121,119,120,120,120,120,119,121,119,121,119,0

Table 49 :
178,63,173,73,159,91,138,114,114,138,91,159,73,173,63,0

Table 99 :
250,1,250,1,195,1,200,100,99,201,1,250,1,250,1,0

Figure 9.1 Modified tables to remove the DC offset

With this modification, the first half cycle can be at full voltage and does not have to be reduced as the previous solution required.

9.1.2 DC offset during the weld.

A DC offset also occurs when the converter changes from one voltage to another. This is discussed in section 8.5.3.2. The problem was again solved only partially. To completely solve the problem the obvious solution is to allow a change in voltage only at a voltage peak.

To show a modification that will achieve this, it is first necessary to assume that the modification recommended in the previous section has already been made, i.e. the tables begin at the voltage peaks.

The program must only allow a change of table when the end of a table has been sensed. In the main program, the microprocessor continually loops, awaiting a change of weld state. When a change occurs, the program immediately shifts from one table to another. A precondition to changing state should be introduced, that allows a change

17 - See Appendix G for the justification.

of state only at the end of a table. This will ensure that the table changes only at a voltage peak. The section that was changed can be found on page E6 of Appendix E and the modification that were made are shown in figure 9.2.

```
CONTIN
          CLR       FFLOP     CLEAR TIMER FLIP-FLOP
          LDA       #15
          STA       ITABOFF
          LDA       #$FF
          STA       SWITCH    INDICATE INTERRUPTS NOT RUNNING
TSTINP
          LDA       ITABOFF
          CMPA      #15
          BNE       TSTINP
          LDA       PIA1B     GET INPUTS
          ANDA      #$70      CLEAR HIGH BIT
          LSRA                SHIFT TO LOWER BITS 0,1,2.
          LSRA
          LSRA
          LSRA
*================================================*

          CMPA      #$07      ARE THEY ALL SET TO HIGH?
          BEQ       CLEAR     CLEAR THE OUTPUTS & TIMERS.

          CMPA      #$00      ARE THEY ALL SET TO LOW?
          BEQ       CLEAR     CLEAR THE OUTPUTS & TIMERS.

          CMPA      #$01      IF YES, WE ARE AT THE START AND
WE
          BEQ       SETT1     WILL SET THE POINTER TO TABLE 1.

          CMPA      #$02      IF YES, WE ARE IN THE MIDDLE AND
WE
          BEQ       SETT2     WILL SET POINTER TO TABLE 2.

          CMPA      #$04      IF YES WE ARE AT THE END AND WE
          BEQ       SETT3     WILL SET POINTER TO TABLE 3.

          BRA       TSTINP    LEAVE IN PREVIOUS STATE.
```

Figure 9.2. Program Modification that removes DC offset during the weld

9.1.3 Voltage/Frequency curve

The converter supplies power to an inductive load. The impedance of this load varies with frequency. At present, when the frequency is changed, the PWM modulation level

(output voltage) remains constant. This has the effect of changing the output power as the frequency is varied. Before the output voltages are set, the frequency must thus be chosen and can also not be changed once in operation, unless the voltage is reset . This is obviously undesirable and there was a request from Carnaud in Spain to improve upon it.

One method of generating a voltage/frequency curve is to make the requested input table number represent a table number adjusted by a constant value dependant on the frequency. The amount by which the table number should be adjusted can be pre-calculated and later tuned experimentally. An example of a modification to the program that would achieve this can be found in figure 9.3. This section of program would fit into that shown in page E4 of Appendix E.

```
OFF1  EQU         0     (If the Freq is number1 set Offset to 0)
OFF2  EQU         5     (If the Freq is number2 set Offset to 5)
OFF3  EQU         10    (If the Freq is number3 set Offset to
10)
OFF4  EQU         20    (If the Freq is number4 set Offset to
20)

......etc. up to OFF7

FSTOR1      INCA
      STA   FREQ
      CPA         02
      JNE         NOT1
      LDY         OFF1
      STY         OFFSET
NOT1  CPA         03
      JNE         NOT2
      LDY         OFF2
      STY         OFFSET
NOT2
......etc up to NOT7

TABTST
      LDA         PIAOA
      COMA
      JSR         BCD2BIN
      ADD         B,OFFSET
      STB         TABSW1
....etc. for all three inputs.
```

Figure 9.3 Program modification that adds a V/F curve

9.2 GENERAL INVERTER AND RECTIFIER IMPROVEMENTS

There are some changes that can be made to the power components of the converter that will decrease the overall cost, size and weight of the machine. In a prototype, factors such as cost, size and weight are not important (within limits), but for future converters, these factors should be considered more closely.

There are also other general improvements that can be made to the converter, such as an increase in frequency, that will at most add only a marginal amount to the cost.

The size of the converter is important as it occupies space on the factory floor. The weight is also significant as the transportation costs will be reduced and the converter will be easier to move, once in site.

9.2.1 Remove Triple Isolation

There are two isolating transformers in the converter and one in the Soudronic. The converter was manufactured so that it could be connected directly to the existing Soudronic transformer. This transformer isolates the cans from the mains supply. It may also be considered necessary for the high voltage power cables connecting the converter to the Soudronic to be isolated, i.e. either the output or rectifier transformer of the converter should remain isolated. As the rectifier transformer is more expensive and heavier than the inverter transformer, it would be the transformer to make a non-isolating auto-transformer. This means that at least one transformer can be reduced to approximately half the size, weight and cost.

9.2.2 Raise the DC Voltage

There are various reasons why a higher DC bus voltage would be beneficial. Some of these reasons are listed

below:

- Better overall efficiency
- Can remove input transformer altogether if the DC bus is approximately 550V
- Can use smaller, and thus cheaper diodes and heatsinks
- Without an input transformer and smaller components, the overall converter size and weight is reduced.

There are, of course, some disadvantages which are:

- More research time is necessary to develop a transistor switch to operate on a 550V DC bus.
- Greater safety precautions need to be taken with a high voltage DC bus.

9.2.2.1 Increased efficiency

When the DC bus voltage is raised, the current is reduced proportionally. Less current thus passes through the semiconductor components. There is little difference in the voltage drop across high and low voltage diodes. The power loss with a higher DC bus is thus greatly reduced. To operate off a DC bus of 550V, the power transistors will require a voltage rating of either 1000V or 1200V. The 600V transistor is a two transistor Darlington, whereas the 1000 and 1200V types are three transistor Darlingtons. The typical collector-emitter voltage drop of an AEG 600V 300Amp transistor is 1.7V and the voltage drop of an AEG 1200V, 150A transistor is marginally higher at 2V. Thus, if the DC bus voltage is increased to 550V and three transistor Darlingtons are used, the conduction losses will still decrease.

Switching losses should not vary substantially with voltage. The switching times of the two transistors concerned are almost identical. Switching losses are dependant on the amount of current being cut off and the voltage across the collector-emitter junction immediately after switch-off. If the voltage is doubled and the

current is halved, the power lost during switching remains approximately constant [19].

9.2.2.2 Remove input transformer

If the DC bus voltage can be raised enough, so that rectified three phase mains can be used (approximately 550V), the input transformer can be removed altogether. The largest, heaviest and most expensive single component in the 250V DC converter is the rectifier transformer. To remove it, would obviously be a tremendous advantage.

9.2.2.3 Reduced component costs

The costs of components such as the diodes, heatsinks cabling and base drive components could be drastically reduced if a higher DC bus is used. The cost of high powered rectifying diodes is almost entirely proportional to the current rating, the voltage rating having little effect on their price.

As the efficiency of the transistors and diodes will improve, the length of aluminium extrusion necessary to dissipate the heat can be reduced.[18] The cost of the heatsink will thus decrease proportionally.

The base drive and associated power supply will be required to supply a reduced quantity of current into the base of the power transistor. This means that the power supply transformer regulators, smoothing capacitors and the output drivers[19] of the base drive can be reduced in current carrying capability and thus cost.

The price difference between two AEG 600V, 300 Amp transistors and one pack of two AEG 1200V, 150A transistor is minimal. An advantage of using the higher voltage transistor is that there are two transistors per package,

---

18 - This assumes that the heatsink should be capable of dissipating all the heat under normal circumstances. Water cooling is only required when the ambient temperature rises or when a large amount of power is required from the converter

19 - It should also be noted that as the current rating of transistors is reduced, other specifications, such as switching frequency can improve

already connected as one leg of a full bridge. This allows a far more compact and simple connection procedure[20].

On the connections between the rectifier and the primary winding of the output transformer, the current is halved, so the cable diameters can also halve. This not only makes the wires easier to handle, but it also reduces the cost marginally.

9.2.3 Step up output voltage

The voltage tappings on all transformers were adjusted to give a maximum output voltage. This is obviously undesirable as the converter output voltage should be adjustable. The output voltage can be increased by simply increasing the output transformer voltage ratio.

Increasing the output voltage has two main effects, firstly it allows the converter to supply more power to the welder and secondly, the PWM modulation level can be decreased, which reduces the harmonic content of the output current waveforms. As the load of the converter is almost entirely inductive, the output power is limited by the maximum output voltage of the converter.

If the voltage ratio of the output transformer increases, so will the current ratio. The current in the inverter components will thus increase proportionally.

To achieve the same output voltage, once the ratio has been increased, the input voltage must be lower, i.e the PWM modulation index must be lower. The full weld voltage of the converter was set to approximately 80% of the full power, which is a modulation index of 1.6. This is an overmodulated PWM waveform. If the overmodulation is reduced, so will the harmonic content of the output wave.

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20 - The more compact the assembly the smaller the flux "holes", thus making the snubbing simpler.

9.2.4 Increase Frequency

As explained in section 2.1.5, the higher the weld frequency, the better the weld. It may therefore be desirable to have a higher maximum frequency.

The real power required to weld a can is independent of the frequency. The load seen by the converter is dependant on frequency though, as it is approximately 50% reactive. Thus for the frequency to increase by 25% to 150Hz, the inverter output power must increase by 12.5% reactive.

9.2.5 Increase Modulation Frequency

It may be feasible to increase the PWM modulation frequency. A higher modulation frequency will decrease the harmonic content of the output current waveform. This could result in a reduction of the filter inductance size. If the frequency was increased, it may be necessary to consider the use of the IGBT as a switch, and not the BJT [28, 29]. The IGBT switches rapidly, so it could maintain low switching losses, even at a higher modulation frequency.

9.3 AN ANALOGUE PWM CONTROLLER

An analogue PWM generator can offer advantages over a computerised controller. These advantages are given later in this section. Research into the design of an analogue controller was recommended early in the project, but the idea was dismissed as further design time would be necessary.

The controller that is suggested is simple and requires no complex circuit design. It has not been constructed nor tested and therefore remains as a theoretical design, to serve only as an example of the type of circuit that could be made.

9.3.1 Suggested PWM generating circuit

The circuit requires the same inputs from the Soudronic, voltage and frequency adjustment dials. All the inputs from the Soudronic are isolated in the same manner as in the completed converter. Ten turn potentiometers (pots) are recommended for the voltage and frequency dials, that give infinitely variable settings (not digital). PWM outputs are buffered by the same IC as in the computer controller. A block diagram of the circuit is shown in figure 9.4.

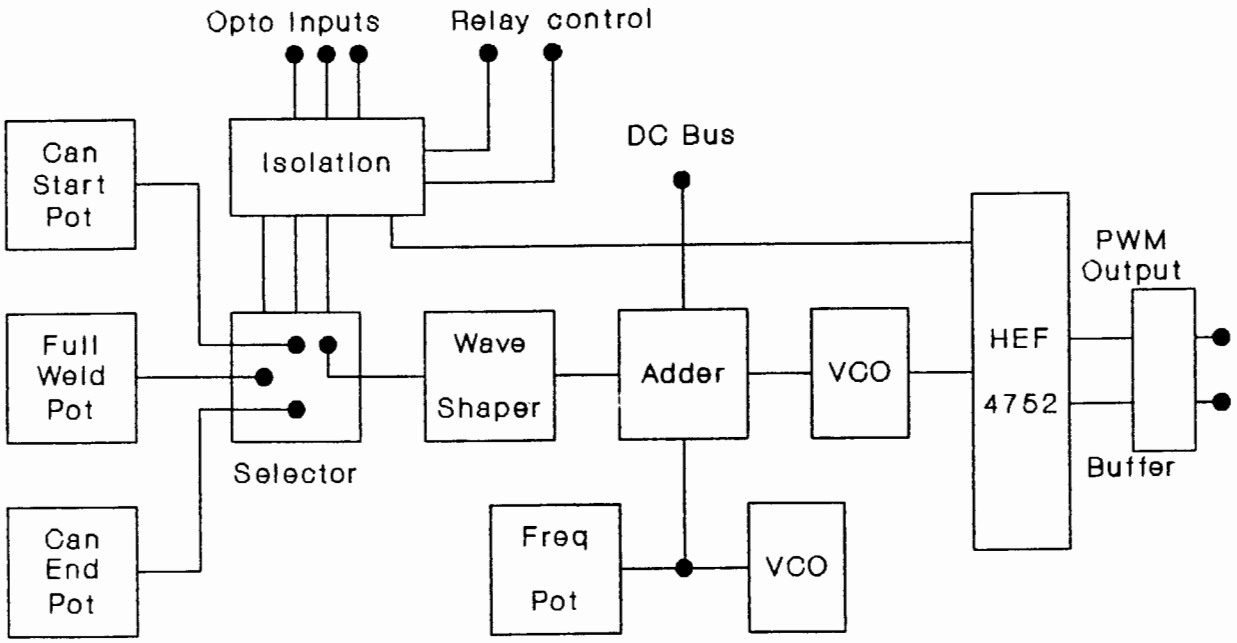

Figure 9.4 Block diagram of the analogue controller

9.3.1.1 Selector Potentiometer

Each pot is connected to the positive (+5V) and negative supply (0V) rails via external resistors. These resistors set the range through which the pot output voltage will vary. The resistance values should all be low, so that the output represents a low impedance voltage source. A diagram of one of the pot circuits is shown in figure 9.5.

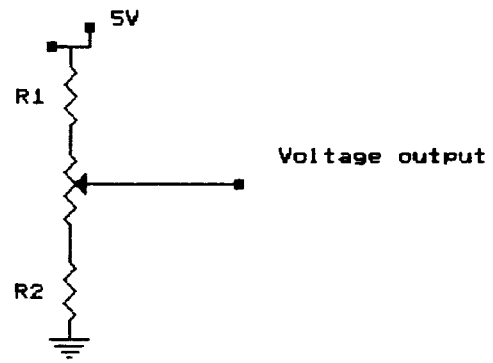

Figure 9.5 Voltage/Frequency adjustment circuit

The resistance values of R1 and R2 are the same for the three voltage adjustment pots, but the resistors on the frequency pot can be different. A single turn pot could be used for the frequency pot, depending on the accuracy required.

9.3.1.2 Optocouplers and the emergency cutout

Each optocoupler transistor in parallel with a pull-up resistor provides a low output when it is selected. For a no-weld state, when all outputs are selected, all are low and a wired NAND gate gives a low output. This output is connected to enable pin of the PWM generator IC. In series with the wired NAND output is the emergency cutout relay, that opens when activated and allows the enable pin to be pulled low. A circuit diagram of the isolation circuit is shown in figure 9.6.

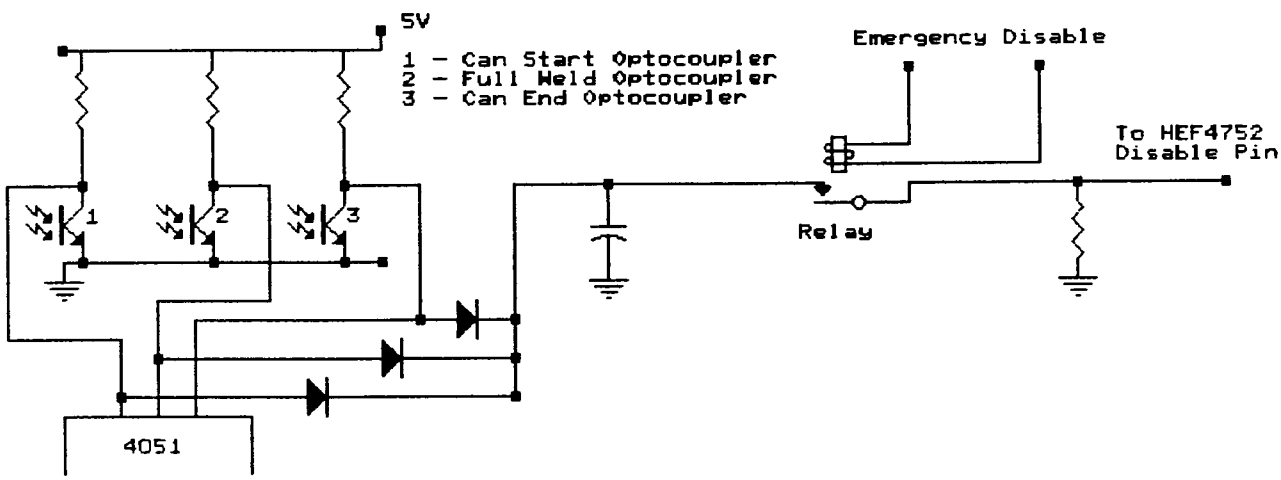

Figure 9.6 Isolation Circuit

9.3.1.3 Voltage Selector Switch

The voltage selection is performed using an analogue switch IC, such as the 4051. A three bit binary coded input specifies which of the eight inputs should be connected to the common output. Only one connection can be made at a time, and it will continue in that state for as long as the code remains the same. The switching is performed by MOSFETS, with a low on resistance. A diagram of how the IC is configured is shown in figure 9.7.

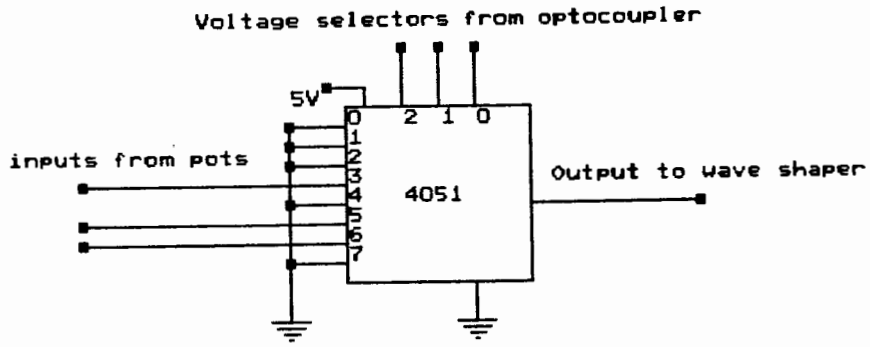

Figure 9.7 Voltage selector switch

9.3.1.4 Voltage Envelope shaping

During the project Metal Box requested a refinement, that the transitions between the various weld voltages should be sloped and not instantaneous. With the computer controller, the extra programming that would be required to improve the transition is extensive and major modifications would have to be made. A diagram of the type of envelope that was requested is shown in figure 9.8.

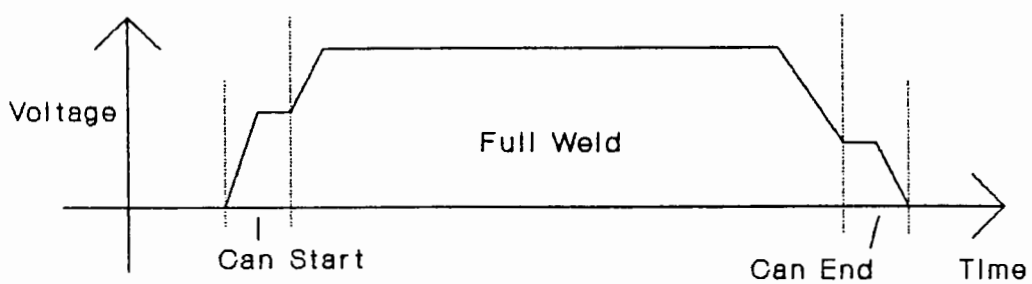

Figure 9.8 Weld Voltage envelope

An analogue circuit that creates a slope between transitions is simple to construct. How close the envelope represents the desired shape depends on how complex the circuit should be. Simple circuits that give a sloped transition are shown in figure 9.9.

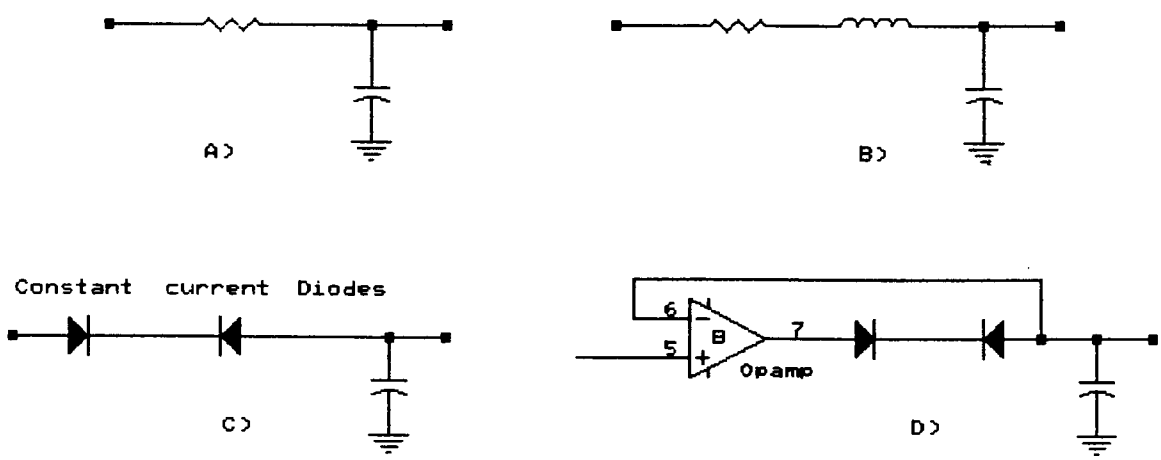

Figure 9.9 Circuits that generate a sloped envelope

The circuit could consist of a simple RC filter, (as in circuit 9.9a) or could be more complex (as in circuit 9.9d), that produces an almost perfectly linear ramp. Circuit 9.9d could also require an extra power supply for the op-amp, to enable the output to swing up to 5V.

9.3.1.5 HEF 4752 PWM Control IC

The HEF4752 is a 3 phase PWM generator intended for use in a variable speed motor drive. It has four control inputs, that are all frequencies. These frequencies control the PWM modulation factor (VCT), the output fundamental frequency (FCT), the modulation factor (RCT) and the dead time between the two PWM frequencies (OCT).

OCT is a constant frequency, as it depends on the transistor switching times.[21] The output of the voltage envelope shaping circuit drives the voltage input of a voltage controlled oscillator (VCO), (e.g. 74LS629). This

21 - If the same power transistor are used, the dead time can be set to 20us.

VCO supplies the frequency to the VCT input of the PWM IC. FCT is driven by a VCO that derives its voltage input from the frequency pot.

If the FCT and RCT inputs are connected together, 15 pulse PWM always results. If RCT is connected to a constant oscillator, the modulation frequency remains within a set bandwidth and the quantity of pulses per fundamental cycle is determined by the PWM IC. For the converter it is recommended that the OCT pin is connected to a constant frequency source that generates a 1.8kHz PWM, as it gives 15 pulse PWM at 120HZ.

A circuit diagram of the HEF 4752 and the VCOs is shown in figure 9.10. The outputs have been buffered to increase the current so that they can drive the base drive optocouplers.

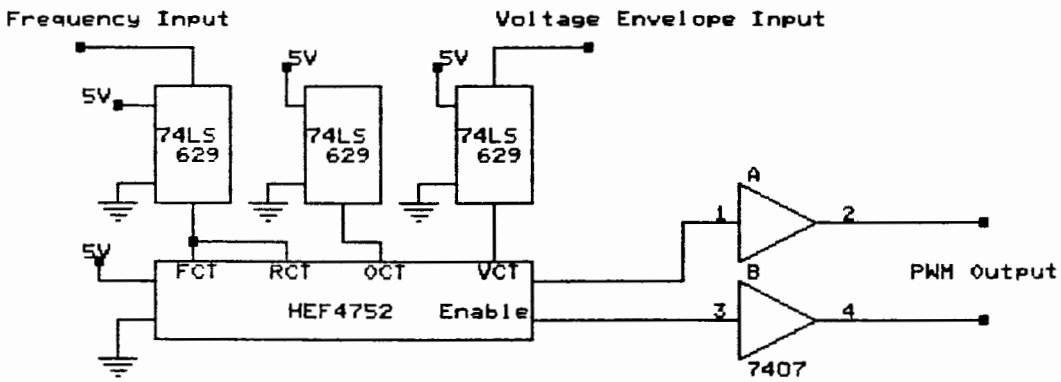

Figure 9.10 The HEF 4752 and support components

9.3.1.6 Voltage/Frequency curve shaping

The HEF 4752 has a built in voltage/frequency curve. The curve is linear and doubles the modulation factor (output voltage) for a doubling in frequency. This curve is intended for an entirely reactive load, such as an induction motor. As the load of the welder is resistive as well as reactive, a less steep curve is required.

A corrective circuit is thus required to reduce the voltage as the frequency increases. This can be achieved by adding an inverting amplifier and a summer into the

circuit. The inverting amplifier gives an output proportional to the inverse of the frequency pot voltage. This voltage adds (subtracts) to the overall envelope voltage. A circuit diagram of the shaping circuit is shown in figure 9.11.

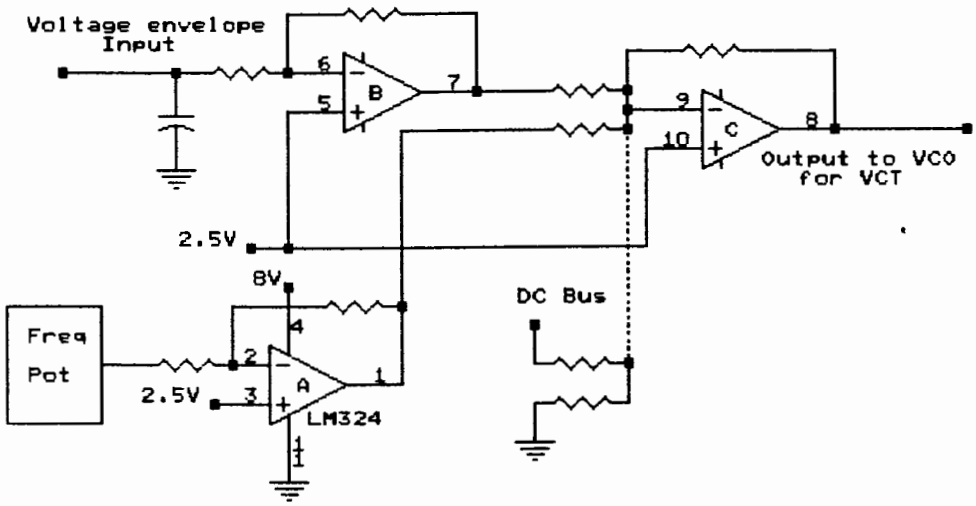

Figure 9.11 Voltage/Frequency curve shaping circuit

9.3.1.7 DC bus voltage feedback

At present the converter's controller has no feedback to correct the output voltage for a change in the DC bus voltage. The effect is that the weld current fluctuates as the mains voltage fluctuates. Dips and surges in the mains can thus result in an incorrect weld. This however, did not appear as a serious problem because the voltage supply in the Spanish factory was constant. Such favorable conditions may not apply for the next installation.

A potential divider can be included to the summer suggested in section 9.3.1.6. The impedance of the potential divider should be chosen carefully, to obtain the correct ratio, so that the output voltage remains constant when the DC bus voltage changes.

9.3.2 Analogue vs Computer generated PWM

A change from the computer based PWM generation to an analogue PWM generating circuit has been suggested.

Before the new circuit is developed, it is necessary to Consider what advantages and disadvantages it could have. Some of these are listed below.

Advantages
- Cheap
- Smaller circuit and PCB
- Simple to design and maintain
- Constantly varying variable voltage and frequency (not digital)
- Simple V/F curve correction
- Can increase frequency and voltage easily by changing resistors
- Easy to design PCB, not necessary to make modifications to the computer prototype PCB
- PCB can contain optocoupler circuit
- Easy to shape can welding power envelope
- DC voltage "feedback"

Disadvantages
- Circuit has yet to be designed
- Cannot do additional operations, e.g can counting
- It is no longer "computer controlled", which was an advertising feature.

9.4 BASE DRIVE MODIFICATIONS

Since the converter was completed, work continued on the base drive and the application of it to an IGBT gate driver. Changes were made to the original driver that improved its performance. This section suggest possible modifications to it and gives the benefits of making the alterations. A diagram of the base drive, showing all the modifications, can be seen in Appendix C.

9.4.1 Negative Supply Protection

If the negative supply to any of the base drives in the converter fails, it will not be able to switch the transistor off. This could lead to the destruction of one or more of the power transistors. A simple circuit modification can achieve negative supply protection.

The change is made to the buffer between the flip-flop and the power output driver. A circuit diagram of the buffer after the modification, is shown in figure 9.12.

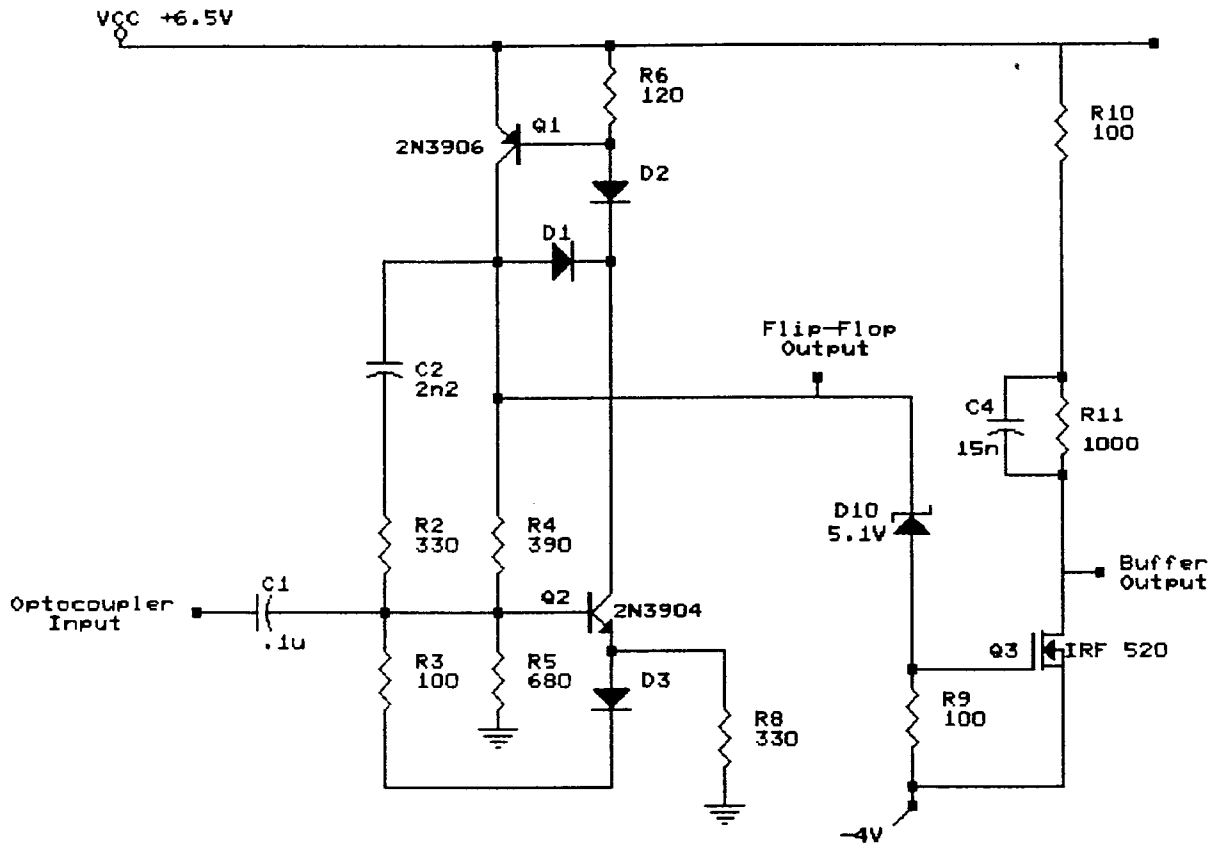

Figure 9.12 Modified Flip-flop Buffer

The fundamental difference is that the source of the Mosfet and the pull down resistor on its gate are connected to the negative rail. Zener diode D10 reduces the flip-flop output signal from 6V/1V to 1V/-4V. The flip-flop output voltage is independent of the negative supply voltage. A "high" output of the flip-flop will thus always be 1V.

The gate-source junction of the Mosfet requires 4V to maintain conduction from drain to source. If the negative

supply fails and the voltage on the source of the Mosfet rises to above -3V, the gate-source junction voltage is too low to maintain drain-source conduction. The Mosfet will switch off, which will force the output transistors to switch the power Darlington off. The Mosfet can not switch on again if the power supply voltage is above -3V.

R11 must be increased to bias Q4 so that the current source remains the same. The negative supply should also not be allowed to rise too rapidly. A 1000uF electrolytic and a 10uF tantalum capacitor connected from the negative rail to ground are on the current base drives. These capacitors should remain in the circuit, as they will supply the energy required to switch the transistor off, if the supply fails.

A Pspice programme was written to stimulate a loss of the negative supply on the modified circuit. The programme listing can be found in Appendix D. The addition of a zener diode and another node, resulted in the programme being too large to run. The two transistors that form the Power Darlington were removed to reduce the program size. The PSpice output can be seen in figure 9.13 and the programme listing can be found in Appendix D.

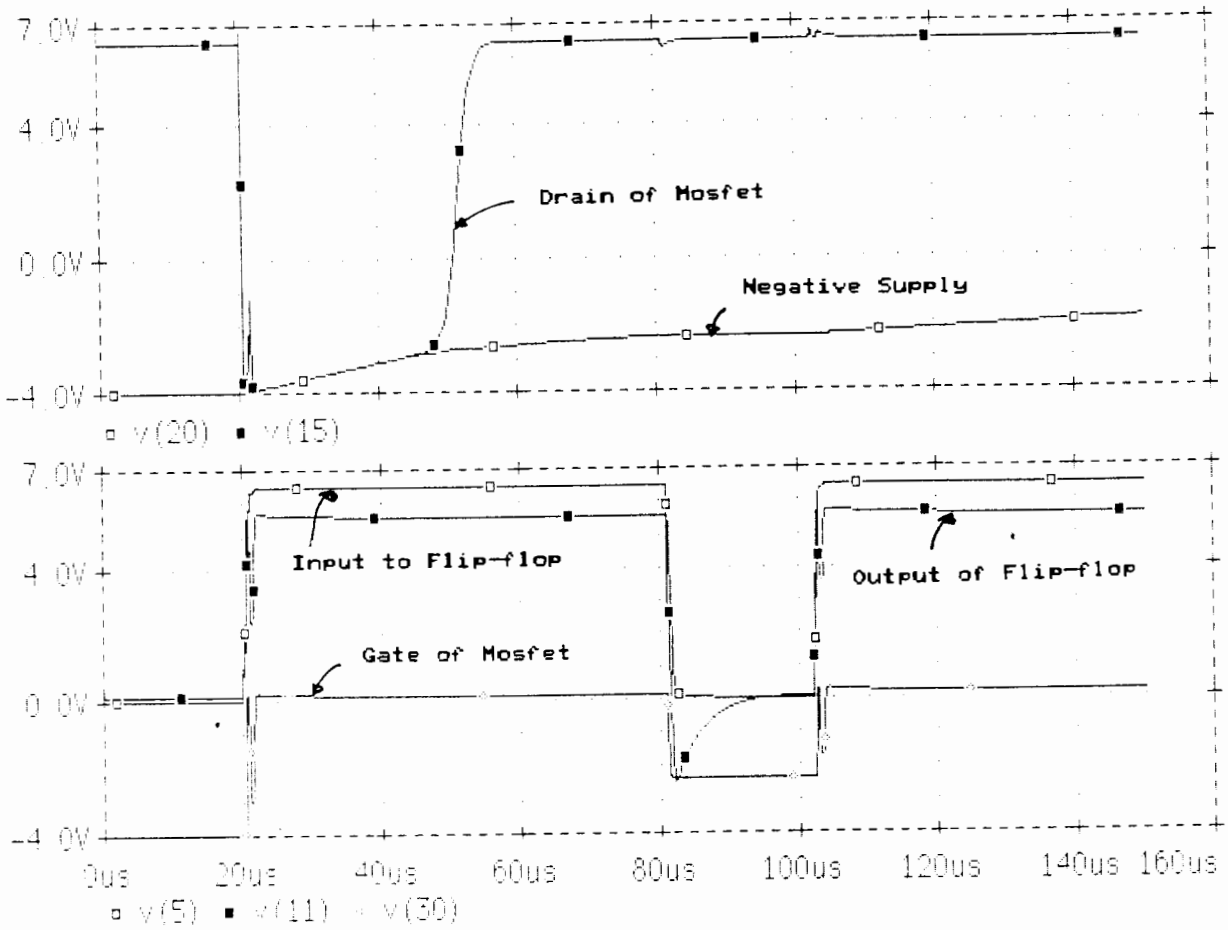

Figure 9.13 Base drive Output with a loss of negative Supply

9.4.2 Simple Circuit Modifications

Five circuit modifications are suggested in this section. None of these changes are critical to the operation of the inverter, but rather remove unnecessary components and to replace inferior components with better substitutes.

9.4.2.1 Optocoupler Buffer.

The open collector output of the optocoupler is buffered by a push pull transistor pair. A peak current in the region of 50 mA is pulled down through the PNP transistor. The optocoupler is capable of sinking more current than this.

A simple modification, that removes a transistor and replaces it with a diode, could be made. The circuit change is shown in figure 9.14.

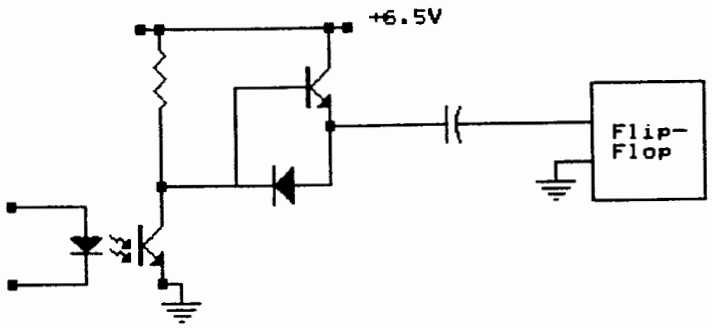

Figure 9.14 Modification to Optocoupler Buffer

When the optocoupler output transistor is off, R1 pulls Q1 on and it works as before. When the optocoupler is on, Q1 is held off and the output capacitor is pulled to ground through D10.

9.4.2.2 Flip-Flop Baker Clamp

The Baker clamp associated with Q1 is intended to limit its level of saturation, so that it can be switched off rapidly. The response time of the flip-flop is dependant on Q1 switching rapidly. A Baker clamp is not the only method of ensuring the prompt switching of Q1.

The level of saturation could be set correctly by choosing R6 and R8 correctly. A lower value of R6 and a higher value of R8 will reduce Q1's depth of saturation. Alternatively, if Q1 is replaced with a faster switching transistor, no circuit modification may be necessary, except to remove D1 and short D2.

9.4.2.3 Remove D3 and R3

The purpose of D3 and R3 is to limit the reverse current and voltage through the base-emitter junction of Q2. This current can also be limited by creating a higher impedance circuit. The capacitance value of C1 could then be reduced, which would limit the average current generated by it (but not the peak). D3 and R3 could then be removed.

9.4.2.4 Replace the IRF520

Q3 is an 8 Amp Mosfet, that carries a peak current of around a few hundred milliamps. The IRF520 was used because choice of Mosfets was limited at the time of the original design. A transistor, such as the 2N7000 (now available) would be far more suitable. This Mosfet has less than one-tenth of the gate capacitance of the IRF520 [30, 31]. A reduced gate capacitance will result in a faster response. Alternatively higher impedance components can be used in the flip-flop, to charge and discharge this capacitance.

9.4.2.5 Replace the Output transistors

The three power transistors, Q4, Q5 and Q6 should all be high speed switching devices. Due to the limited choice of high current transistors when the base drive was designed, inferior devices were used. These transistors could however, be replaced with more suitable versions.

For example, the BUP30 is a 20 Amp switching device with a high gain and an f_t rating of 120MHZ [32]. This transistor could replace the 2N5038. It would still appear to be difficult to obtain in South Africa though. Similar specification transistors could be sought after to replace the 2N6107's

CHAPTER 10

CONCLUSIONS

A 20KVA converter has been designed, manufactured and tested. It supplies 120Hz power to a welding machine, to enable it to operate at twice its normal speed. The converter has been operational in Spain since October of 1990.

The inverter was first designed in a push pull configuration. This design was found to be unreliable and inefficient. For high power, around 20KW, it was concluded that a push-pull configuration is undesirable. The inverter was then modified into a full bridge configuration. This design was found to be more reliable and was applied in the final converter.

A base drive was developed to control power Darlington transistors. It enabled the transistors to switch rapidly and also offered overcurrent protection. Recommendations were made to refine the operation and features of the base drive.

Further design changes could be made to future converters that would improve it remarkably. The weight, size and cost of the converter could be drastically reduced by raising the DC bus up to 550V. The PWM generator could also be improved upon by adding features that would facilitate easier control of the converter.

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APPENDIX

APPENDIX TABLE OF CONTENTS

APPENDIX A

COMPONENT DATASHEETS

AEG C300R600K Darlington Transistor

C 300 R 600 K

Transistor **Transistor**

Elektrische Eigenschaften **Electrical properties**

Höchstzulässige Werte		Maximum permissible values		
V_{CEX}	i_C = 1 A, v_{EB} = 2 V		600	V
V_{CEO}	i_C = 0.5 A, L_C = 40 mH		550	V
V_{CBO}			600	V
V_{EBO}			6	V
I_C			300	A
I_{CRM}	t_p = 1 ms		600	A
I_{CAVM}	DC, t_C = 85°C, I_{FB} = 8 A		220	A
I_{FB}	t_p = 10 ms		40	A
	t_p = 1 ms		80	A
I_{RB}	t_p = 20 µs		80	A

Charakteristische Werte		Characteristic values		
$v_{CE\,sat}$	i_{CM} = 300 A, i_{FBM} = 8 A, t_{vj} = 25°C	typ.	1,7	V
	i_{CM} = 300 A, i_{FBM} = 8 A, t_{vj} = t_{vjmax}	max.	2,8	V
$v_{BE\,sat}$	i_{CM} = 300 A, i_{FBM} = 8 A, t_{vj} = 25°C	typ.	2,2	V
	i_{CM} = 300 A, i_{FBM} = 8 A, t_{vj} = t_{vjmax}	max.	2,7	V
i_{CBO}	v_{CB} = V_{CBO}, t_{vj} = 25°C	typ.	2	mA
	v_{CB} = V_{CBO}, t_{vj} = t_{vjmax}	max.	100	mA
i_{EBO}	v_{EB} = 6 V, t_{vj} = 25°C	typ.	600	mA
	v_{EB} = 6 V, t_{vj} = t_{vjmax}	max.	1	A
B	i_C = 300 A, v_{CE} = 5 V, t_{vj} = 25°C	typ.	150	
	i_C = 300 A, v_{CE} = 5 V, t_{vj} = t_{vjmax}	min.	40	
t_{on}	i_{CM} = 300 A, v_{CE} = 0,5 · V_{CEX}			
	i_{FBM} = 8 A, t_a = 0,3 µs, t_{vj} = 25°C	typ.	1,5	µs
	i_{CM} = 300 A, v_{CE} = 0,5 · V_{CEX}			
	i_{FBM} = 8 A, t_a = 0,3 µs, t_{vj} = t_{vjmax}	max.	4	µs
t_s	i_{CM} = 300 A, v_{CE} = 0,5 · V_{CEX}			
	i_{FBM} = i_{RBM} = 8 A, t_{vj} = 25°C	typ.	10	µs
	i_{CM} = 300 A, v_{CE} = 0,5 · V_{CEX}			
	i_{FBM} = i_{RBM} = 8 A, t_{vj} = t_{vjmax}	max.	25	µs
t_f	i_{CM} = 300 A, v_{CE} = 0,5 · V_{CEX}			
	i_{FBM} = i_{RBM} = 8 A, t_{vj} = 25°C	typ.	0,4	µs
	i_{CM} = 300 A, v_{CE} = 0,5 · V_{CEX}			
	i_{FBM} = i_{RBM} = 8 A, t_{vj} = t_{vjmax}	max.	2	µs
V_{ISOL}	RMS		2,5	kV

Bedingungen für den Kurzschlußschutz	Conditions for protection against short circuits
	t_W = 40 µs, i_{FBM} = 8 A, i_{RBM} = 8 A
	oder / or
	t_W = 50 µs, i_{FBM} = 4,8 A, i_{RBM} = 7,2 A
	bei / at
	V_{CC} = 350 V, v_{CEM} = 500 V
	t_{vj} = t_{vjmax}
	$i_{CMK} \approx 3,5 \cdot I_C$

Thermische Eigenschaften **Thermal properties**

R_{thJC}	DC, pro Baustein / per module	≤ 0,089	°C/W
R_{thCK}	pro Baustein / per module	0,03	°C/W
t_{vjmax}		125	°C
t_{vjop}		-40 / +125	°C
t_{stg}		-40 / +125	°C

Mechanische Eigenschaften **Mechanical properties**

G		490	g
M1		3	Nm
M2	terminals M4 / M6	2 Nm / 3 Nm	

Antiparallele Diode **Antiparallel diode**

Elektrische Eigenschaften **Electrical properties**

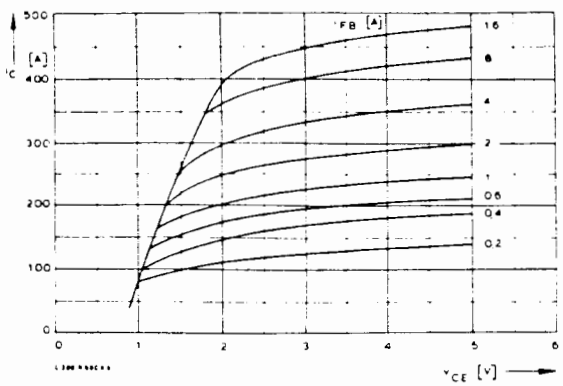
Höchstzulässige Werte		Maximum permissible values		
$I_{F\,(max)}$			300	A
I_{FRM}	t_p = 1 ms		600	A
I_{FAVM}	DC, t_C = 85°C		106	A
I_{FSM}	t_p = 10 ms, t_{vj} = 25°C		1900	A
	t_p = 10 ms, t_{vj} = t_{vjmax}		1600	A
$\int i^2 dt$	t_p = 10 ms, t_{vj} = 25°C		18000	A^2s
	t_p = 10 ms, t_{vj} = t_{vjmax}		12800	A^2s

Charakteristische Werte		Characteristic values		
v_F	i_F = 300 A, t_{vj} = 25°C	typ.	1,3	V
	i_F = 300 A, t_{vj} = t_{vjmax}	max.	1,7	V
I_{RRM}	i_{FM} = 300 A, -di_F/dt = 150 A/µs			
	v_{EB} = 3 V, t_{vj} = 25°C	typ.	48	A
	i_{FM} = 300 A, -di_F/dt = 150 A/µs			
	v_{EB} = 3 V, t_{vj} = t_{vjmax}	max.	83	A
Q_{rr}	i_{FM} = 300 A, -di_F/dt = 150 A/µs			
	v_{EB} = 3 V, t_{vj} = 25°C	typ.	14	µAs
	i_{FM} = 300 A, -di_F/dt = 150 A/µs			
	v_{EB} = 3 V, t_{vj} = t_{vjmax}	max.	60	µAs

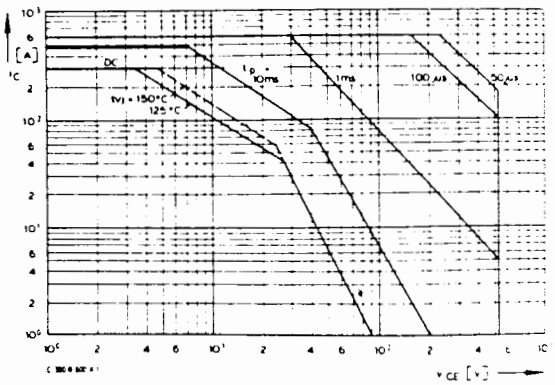
Thermische Eigenschaften **Thermal properties**

R_{thJC}	DC, pro Baustein / per module	≤ 0,325	°C/W
R_{thCK}	pro Baustein / per module	0,06	°C/W
t_{vjmax}		125	°C
t_{vjop}		-40 / +125	°C
t_{stg}		-40 / +125	°C

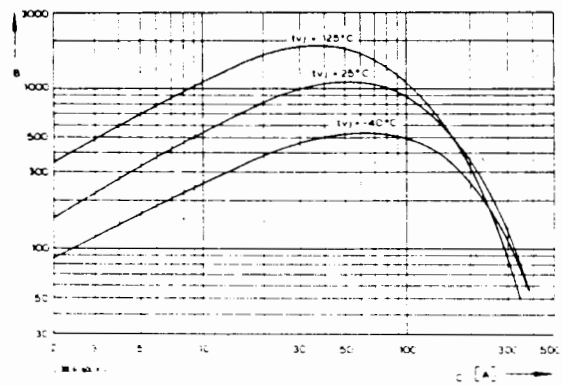
C 300 R 600 K



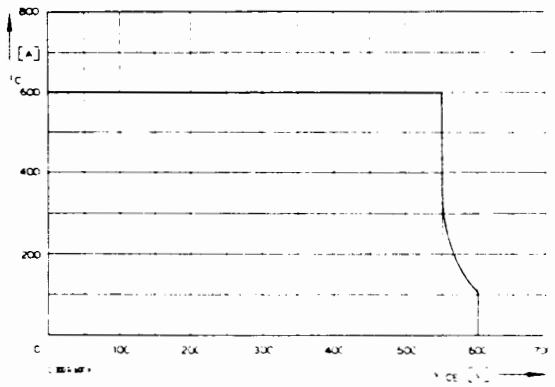
1 Kollektor-Emitter-Sättigungsspannung in Abhängigkeit vom Kollektorstrom (typisch)
Collector-emitter-saturation voltage versus collector current (typical)
$t_v = 25°C$



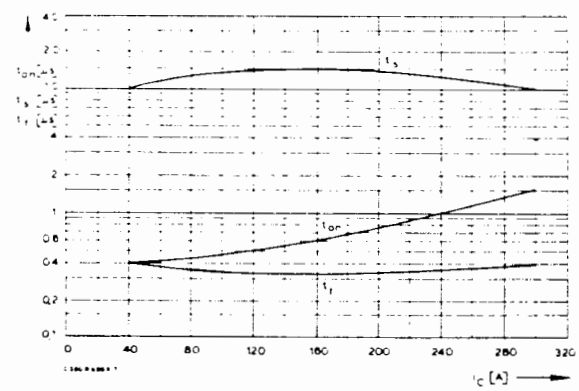
4 Erlaubter Arbeitsbereich in Vorwärtsrichtung (Einzelimpuls, nicht periodisch)
Forward biased safe operating area (single pulse, non repetitive)
$t_C = 25°C$
(Reduzierung bei höheren Temperaturen gemäß Technische Erläuterungen Abschnitt 5.1
Derating at higher temperatures according to Technical Information paragraph 5.1.



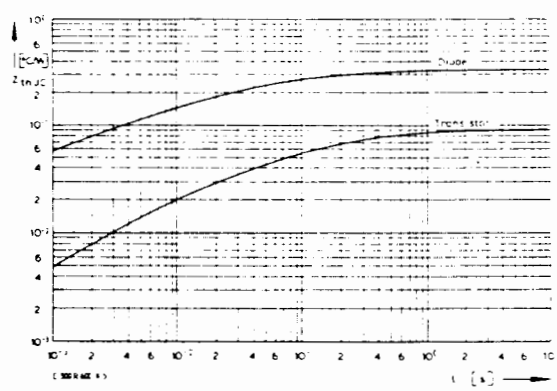
2 Kollektor-Basis-Gleichstromverhältnis in Abhängigkeit vom Kollektorstrom (typisch)
DC current gain versus collector current (typical)
$V_{CE} = 5$ V



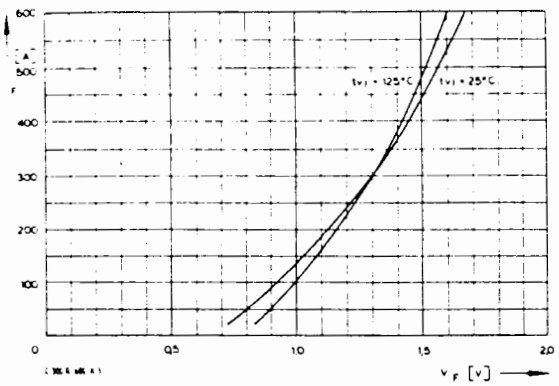
5 Erlaubter Arbeitsbereich in Rückwärtsrichtung
Reverse biased safe operating area
$t_v = 125°C$ $V_{CE} = 6$ V $I_{BM} = 16$ A



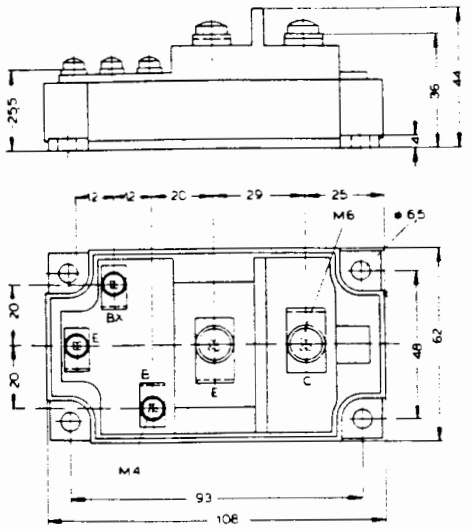
3 Einschalt-, Speicher- und Fallzeit in Abhängigkeit vom Kollektorstrom (typisch)
Turn-on time, storage time and fall time versus collector current (typical)
$t_v = 25°C$ $V_{CE} = 0.5$ $V_{CE\,s}$ $I_{BM} = 8$ A $I_{BM} = 8$ A
t_{on} ohmsche Last, resistive load
t_s, t_f ohmsch-induktive Last, resistive-inductive load



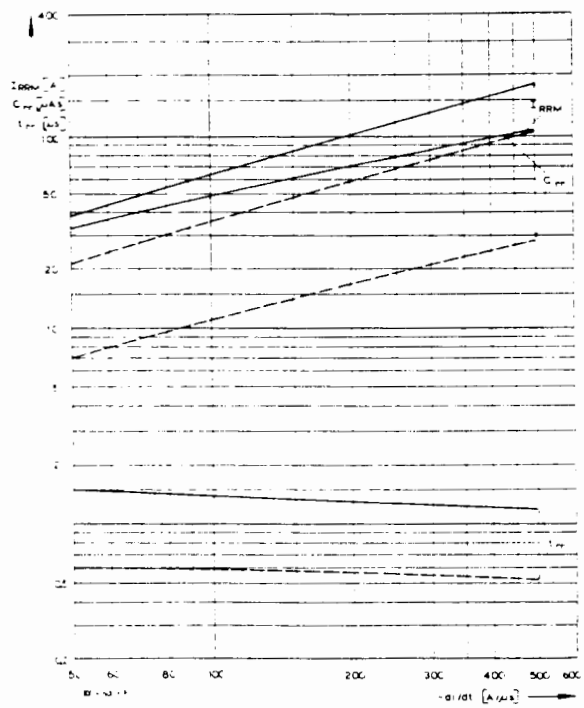
6 Transienter innerer Wärmewiderstand je Zweig (DC)
Transient thermal impedance per arm (DC)



7 Durchlaßkennlinie der Inversdiode (typisch)
Forward characteristic of the inverse diode (typical)



9 Maßbild Schaltbild
Outline, circuit



8 Rückstromspitze, Sperrverzugsladung und Sperrverzugszeit der Inversdiode in Abhängigkeit von der abkommutierenden Stromsteilheit
Peak reverse recovery current, recovered charge and reverse recovery time of the inverse diode versus rate of decay of current
T_{FM} = 10 A, V_{EE} = 30 V
——— T_{vj} = 125°C max – – – – T_{vj} = 25°C typ.

AEG C300R1000K Darlington Transistor

C 300 R 1000 K

Transistor **Transistor**

Elektrische Eigenschaften **Electrical properties**

Höchstzulässige Werte		Maximum permissible values	
V_{CEX}	$i_C = 1$ A, $v_{EB} = 2$ V	1000	V
V_{CEO}	$i_C = 1$ A, $L_C = 40$ mH	880	V
V_{CBO}		1000	V
V_{EBO}		7	V
I_C		300	A
I_{CRM}	$t_p = 1$ ms	600	A
I_{CAVM}	DC, $t_C = 85°C$, $i_{FB} = 6$ A	220	A
I_{FB}	$t_p = 10$ ms	30	A
	$t_p = 1$ ms	60	A
I_{RB}	$t_p = 20\ \mu s$	60	A

Charakteristische Werte		Characteristic values		
$v_{CE\,sat}$	$i_{CM} = 300$ A, $i_{FBM} = 6$ A, $t_{vj} = 25°C$	typ.	2	V
	$i_{CM} = 300$ A, $i_{FBM} = 6$ A, $t_{vj} = t_{vjmax}$	max	3	V
$v_{BE\,sat}$	$i_{CM} = 300$ A, $i_{FBM} = 6$ A, $t_{vj} = 25°C$	typ.	2,8	V
	$i_{CM} = 300$ A, $i_{FBM} = 6$ A, $t_{vj} = t_{vjmax}$	max.	3,5	V
i_{CBO}	$v_{CB} = V_{CBO}$, $t_{vj} = 25°C$	typ.	3	mA
	$v_{CE} = V_{CBO}$, $t_{vj} = t_{vjmax}$	max	120	mA
i_{EBO}	$v_{EB} = 7$ V, $t_v = 25°C$	typ	600	mA
	$v_{EB} = 7$ V, $t_v = t_{vjmax}$	max	1	A
B	$i_C = 300$ A, $v_{CE} = 5$ V, $t_v = 25°C$	typ.	160	
	$i_C = 300$ A, $v_{CE} = 5$ V, $t_v = t_{vjmax}$	min.	60	
t_{on}	$i_{CM} = 300$ A, $v_{CE} = 0.5 \cdot V_{CEX}$			
	$i_{FBM} = 6$ A, $t_r = 0.3\ \mu s$, $t_v = 25°C$	typ.	0.8	μs
	$i_{CM} = 300$ A, $v_{CE} = 0.5 \cdot V_{CEX}$			
	$i_{FBM} = 6$ A, $t_r = 0.3\ \mu s$, $t_v = t_{vjmax}$	max.	4	μs
t_s	$i_{CM} = 300$ A, $v_{CE} = 0.5 \cdot V_{CEX}$			
	$i_{FBM} = i_{RBM} = 6$ A, $t_v = 25°C$	typ.	12	μs
	$i_{CM} = 300$ A, $v_{CE} = 0.5 \cdot V_{CEX}$			
	$i_{FBM} = i_{RBM} = 6$ A, $t_v = t_{vjmax}$	max.	28	μs
t_f	$i_{CM} = 300$ A, $v_{CE} = 0.5 \cdot V_{CEX}$			
	$i_{FBM} = i_{RBM} = 6$ A, $t_v = 25°C$	typ.	0.5	μs
	$i_{CM} = 300$ A, $v_{CE} = 0.5 \cdot V_{CEX}$			
	$i_{FBM} = i_{RBM} = 6$ A, $t_v = t_{vjmax}$	max.	2	μs
V_{ISOL}	RMS		2.5	kV

Bedingungen für den Kurzschlußschutz	Conditions for protection against short circuits
$t_K = 40\ \mu s$, $i_{FBM} = 6$ A, $i_{RBM} = 6$ A	
oder / or	
$t_K = 50\ \mu s$, $i_{FBM} = 4$ A, $i_{RBM} = 6$ A	
bei / at	
$V_{CC} = 0.5 \cdot V_{CEX}$, $v_{CEM} = 0.75 \cdot V_{CEX}$	
$t_{vj} = t_{vjmax}$	
$i_{CM} = 4 \cdot I_C$	

Thermische Eigenschaften **Thermal properties**

R_{thJC}	DC, pro Baustein / per module	≤ 0.078	°C/W
R_{thCK}	pro Baustein / per module	0.03	°C/W
t_{vjmax}		125	°C
t_{vjop}		-40 / + 125	°C
t_{stg}		-40 / + 125	°C

Mechanische Eigenschaften **Mechanical properties**

G		490	g
M1		3	Nm
M2	terminals M4 / M6	2 Nm / 3 Nm	

Antiparallele Diode **Antiparallel diode**

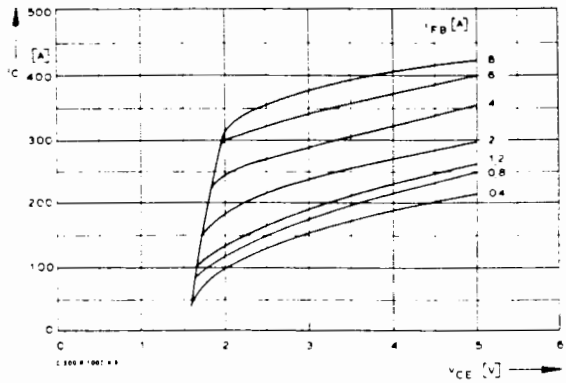
Elektrische Eigenschaften **Electrical properties**

Höchstzulässige Werte		Maximum permissible values	
$I_{F\,(max)}$		300	A
I_{FRM}	$t_p = 1$ ms	600	A
I_{FAVM}	DC, $t_C = 85°C$	106	A
I_{FSM}	$t_p = 10$ ms, $t_{vj} = 25°C$	2700	A
	$t_p = 10$ ms, $t_{vj} = t_{vjmax}$	2270	A
$\int i^2 dt$	$t_p = 10$ ms, $t_{vj} = 25°C$	36500	A^2s
	$t_p = 10$ ms, $t_{vj} = t_{vjmax}$	25700	A^2s

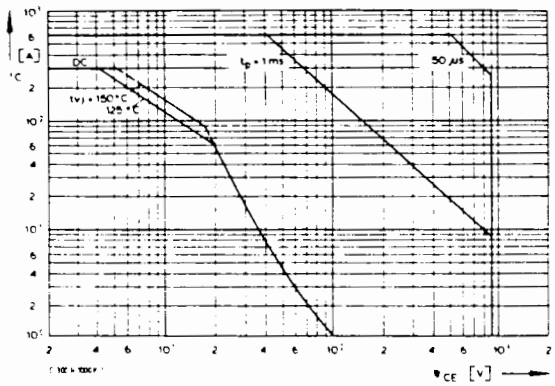
Charakteristische Werte		Characteristic values		
v_F	$i_F = 300$ A, $t_{vj} = 25°C$	typ.	1.3	V
	$i_F = 300$ A, $t_{vj} = t_{vjmax}$	max.	1.6	V
I_{RRM}	$i_{FM} = 300$ A, $-di_F/dt = 150$ A/μs			
	$v_{EB} = 3$ V, $t_{vj} = 25°C$	typ.	56	A
	$i_{FM} = 300$ A, $-di_F/dt = 150$ A/μs			
	$v_{EB} = 3$ V, $t_{vj} = t_{vjmax}$	max.	130	A
Q_r	$i_{FM} = 300$ A, $-di_F/dt = 150$ A/μs			
	$v_{EB} = 3$ V, $t_{vj} = 25°C$	typ.	17	μAs
	$i_{FM} = 300$ A, $-di_F/dt = 150$ A/μs			
	$v_{EB} = 3$ V, $t_{vj} = t_{vjmax}$	max.	100	μAs

Thermische Eigenschaften **Thermal properties**

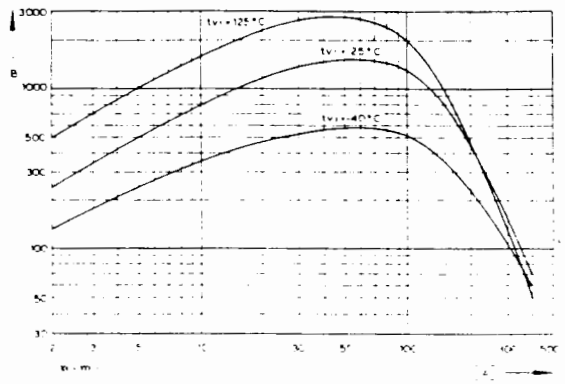
R_{thJC}	DC, pro Baustein / per module	≤ 0.325	°C/W
R_{thCK}	pro Baustein / per module	0.06	°C/W
t_{vjmax}		125	°C
t_{vjop}		-40 / + 125	°C
t_{stg}		-40 / + 125	°C



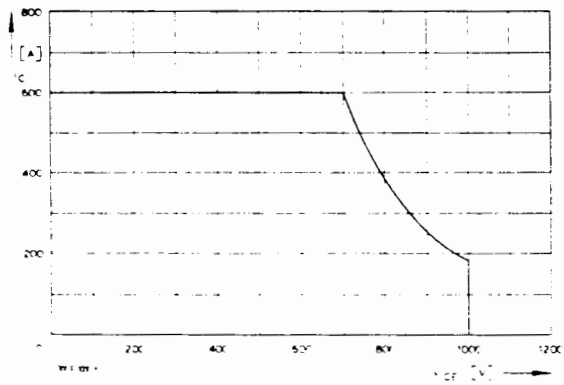
1 Kollektor-Emitter-Sättigungsspannung in Abhängigkeit vom Kollektorstrom (typisch)
Collector-emitter-saturation voltage versus collector current (typical)
$t_v = 25°C$



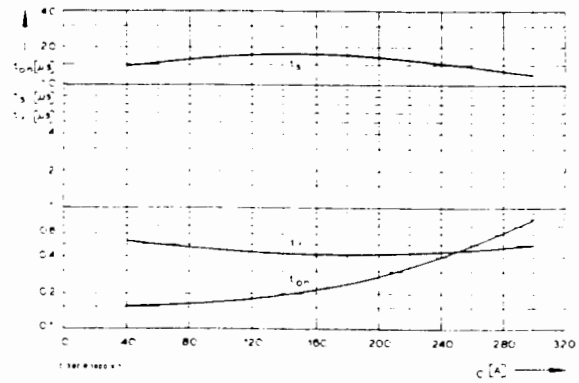
4 Erlaubter Arbeitsbereich in Vorwärtsrichtung (Einzelimpuls, nicht periodisch)
Forward biased safe operating area (single pulse, non repetitive)
$t_C = 25°C$
(Reduzierung bei höheren Temperaturen gemäß Technische Erläuterungen Abschnitt 5.1
Derating at higher temperatures according to Technical Information, paragraph 5.1)



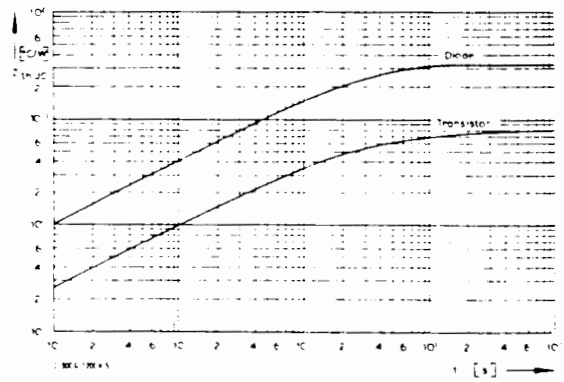
2 Kollektor-Basis-Sperrschichtkapazität in Abhängigkeit vom Kollektorstrom (typisch)
DC current gain versus collector current (typical)
$V_{CE} = 5$ V



5 Erlaubter Arbeitsbereich in Rückwärtsrichtung
Reverse biased safe operating area
t_{vj} = 125 °C V_{CE} = 7 V I_{BEV} = -1 A

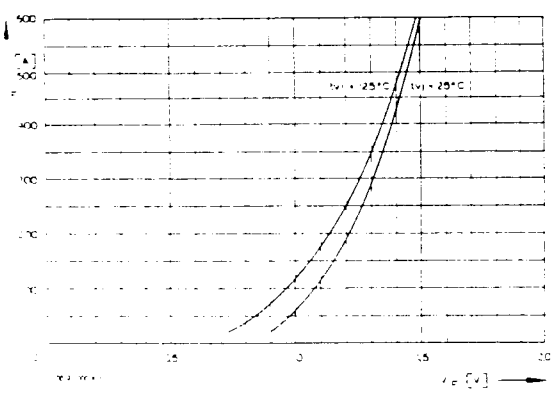


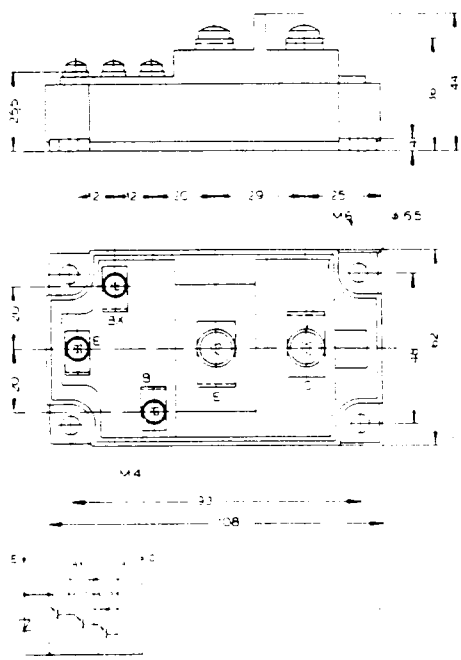
3 Einschalt-, Speicher- und Fallzeit in Abhängigkeit vom Kollektorstrom (typisch)
Turn-on time, storage time and fall time versus collector current (typical)
$t_v = 25°C$ $V_{CE} = 0.5$ V_{CEX} $I_{BEV} = 5$ A $R_{BM} = 6$ A
t_{on} ohmsche Last: resistive load
t_s, t_f ohmsch-induktive Last: resistive-inductive load

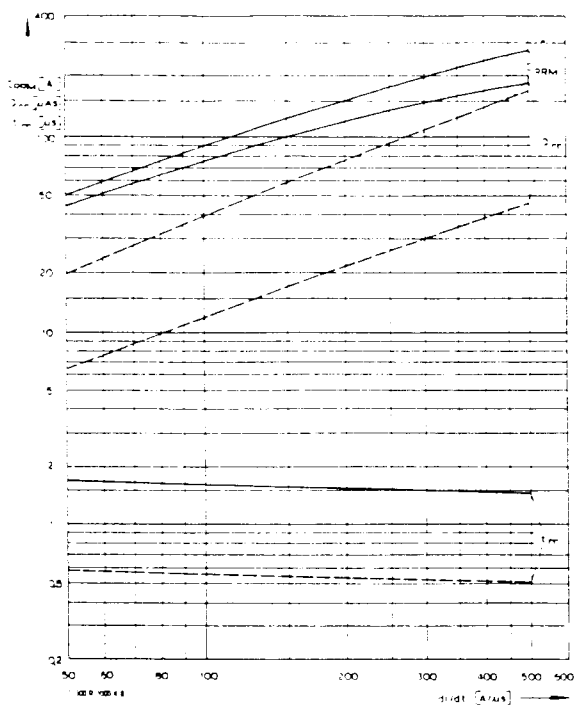


6 Transienter innerer Wärmewiderstand je Zweig (DC)
Transient thermal impedance per arm (DC)

C 300 R 1000 K



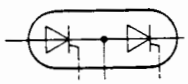




Maßbild. Schaltbild
Outline. Circuit

Rückstromspitze, Sperrverzugsladung und Sperrverzugszeit der Inversdiode in Abhängigkeit von der abkommutierenden Stromsteilheit
Peak reverse recovery current, recovered charge and reverse recovery time of the inverse diode versus rate of decay of current
$v_R = V_C$, $v_{EB} \geq 3$ V
——— $t_{vj} = 125$ °C, max - - - - $t_{vj} = 25$ °C, typ.

Semikron SKKD 81/04



SEMIPACK®
Thyristor/Diode Modules

SEMIPACK®
Thyristor/Dioden-Bausteine

SEMIPACK®
Modules à thyristors/diodes

isolated metal bases. V_{isol} = 2500 V~

Types All data apply to one single valve device (thyristor or diode)	V_{RSM} V	V_{DRM} V_{RRM} V	I_{TRMS} I_{FRMS} A	I_{TAV} I_{FAV} (T_{Case}) A	I_{TSM} I_{FSM} 25 °C 10 ms A	i^2t 25 °C 10 ms A²s	$\left(\frac{dv}{dt}\right)_{cr}$ V/µs	V_T, V_F max. (I_T, I_F) V	$V_{T(TO)}$ $V_{F(TO)}$ V	r_T mΩ	I_H max. mA	I_L max. mA	V_{GT} min. (t_p = 100 µs) V	I_{GT} min. mA
SKKD 15/04	500	400	28	15 (82 °C)	320	510	–	1.85 (75 A)	0.85	15	–	–	–	–
/06	700	600												
/08	900	800												
/12	1300	1200												
/14	1500	1400												
/16	1700	1600												
SKKD 46/04	500	400	90	45 (86 °C)	700	2450	–	1.95 (250 A)	0.85	5	–	–	–	–
/06	700	600												
/08	900	800												
/12	1300	1200												
/14	1500	1400												
/16	1700	1600												
SKKD 81/04	500	400	140	80 (87 °C)	1750	15000	–	1.55 (300 A)	0.85	1.8	–	–	–	–
/06	700	600												
/08	900	800												
/12	1300	1200												
/14	1500	1400												
/16	1700	1600												
SKKD 162/08	800	800	250	160 (85 °C)	6000	180000	–	1.25 (500 A)	0.85	0.6	–	–	–	–
/12	1200	1200												
/16	1600	1600												
SKKD 201/08	800	800	315	200 (85 °C)	6000	180000	–	1.35 (600 A)	0.8	0.8	–	–	–	–
/12	1200	1200												
/16	1600	1600												
SKKD 260/08	800	800	410	260 (85 °C)	11000	605000	–	1.25 (750 A)	0.9	0.37	–	–	–	–
/12	1200	1200												
/16	1600	1600												
SKKE 15/06	700	600	28	15 (82 °C)	320	510	–	1.85 (75 A)	0.85	15	–	–	–	–
/08	900	800												
/12	1300	1200												
/14	1500	1400												
/16	1700	1600												
SKKE 81/04	500	400	140	80 (87 °C)	1750	15000	–	1.55 (300 A)	0.85	1.8	–	–	–	–
/06	700	600												
/08	900	800												
/12	1300	1200												
/14	1500	1400												
/16	1700	1600												
SKKE 162/12	1200	1200	250	160 (85 °C)	6000	180000	–	1.25 (500 A)	0.85	0.6	–	–	–	–
/16	1600	1600												
SKKE 201/08	800	800	315	200 (85 °C)	6000	180000	–	1.35 (600 A)	0.8	0.8	–	–	–	–
/12	1200	1200												
/16	1600	1600												
SKKE 260/12	1200	1200	410	260 (85 °C)	11000	605000	–	1.25 (750 A)	0.9	0.37	–	–	–	–
/16	1600	1600												
SKKH 15/04	500	400	28	15 (75 °C)	320	510	500	2.45 (75 A)	1.1	20	120	300	3	100
/06	700	600												
/08	900	800												
/12	1300	1200												
/14	1500	1400												
/16	1700	1600												
SKKH 26/04 D	500	400	50	25 (85 °C)	470	1100	500	1.8 (75 A)	0.9	12	200	400	3	150
/06 D	700	600												
/08 D	900	800												
/12 D	1300	1200												
/14 D	1500	1400												
/16 D	1700	1600												
SKKH 41/04 D	500	400	75	40 (85 °C)	1000	5000	500	1.95 (200 A)	1.0	4.5	250	600	3	150
/06 D	700	600												
/08 D	900	800												
/12 D	1300	1200												
/14 D	1500	1400												
/16 D	1700	1600												
SKKH 56/04 D	500	400	95	55 (80 °C)	1500	11000	500	1.65 (200 A)	0.9	3.5	250	600	3	150
/06 D	700	600												
/08 D	900	800												
/12 D	1300	1200												
/14 D	1500	1400												
/16 D	1700	1600												
SKKH 71/04 D	500	400	125	70 (85 °C)	1600	13000	500	1.9 (300 A)	0.9	3.5	250	600	3	150
/06 D	700	600												
/08 D	900	800												
/12 D	1300	1200												
/14 D	1500	1400												
/16 D	1700	1600												

SEMIPACK®
Moduli a tiristori/diodi

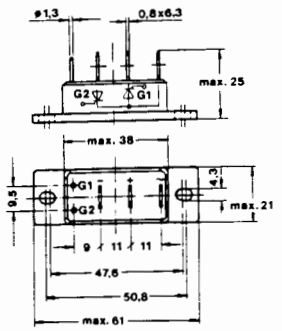
Types All data apply to one single valve device (thyristor or diode)	T_{vj} max. °C	R_{thjc} sin. 180 °C/W	R_{thch} °C/W	Case Page	Circuit
SKKD 15/04 /06 /08 /12 /14 /16	125	2.0	0.2	A 3 15	
SKKD 46/04 /06 /08 /12 /14 /16	125	0.6	0.2	A 10 15	
SKKD 81/04 /06 /08 /12 /14 /16	125	0.4	0.2	A 10 15	
SKKD 162/08 /12 /16	125	0.23	0.1	A 23 19	
SKKD 201/08 /12 /16	130	0.19[1]	0.06	A 16 17	
SKKD 260/08 /12 /16	130	0.14[1]	0.04	A 27 17	
SKKE 15/06 /08 /12 /14 /16	125	2.0	0.2	A 4 15	
SKKE 81/04 /06 /08 /12 /14 /16	125	0.4	0.2	A 12 15	
SKKE 162/12 /16	125	0.23	0.1	A 24 19	
SKKE 201/08 /12 /16	130	0.19[1]	0.06	A 17 17	
SKKE 260/12 /16	130	0.14	0.04	A 28 17	
SKKH 15/04 /06 /08 /12 /14 /16	125	1.3	0.2	A 2 15	
SKKH 26/04 D /06 D /08 D /12 D /14 D /16 D	125	0.95	0.2	A 6 15	
SKKH 41/04 D /06 D /08 D /12 D /14 D /16 D	125	0.69	0.2	A 6 15	
SKKH 56/04 D /06 D /08 D /12 D /14 D /16 D	125	0.6	0.2	A 6 15	
SKKH 71/04 D /06 D /08 D /12 D /14 D /16 D	125	0.37[1]	0.2	A 6 15	

innovation + service

SEMIPACK®
Módulos de tiristores/diodos

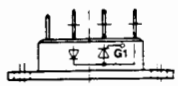
SEMIPACK®
Módulos de tiristores/diodos

Case A 1 **SEMIPACK® 0**



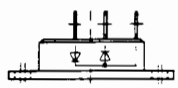
SKKT 15 M_1 = 2 Nm w = 50 g

Case A 2



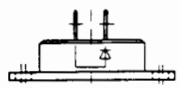
SKKH 15

Case A 3



SKKD 15

Case A 4



SKKE 15

Dimensions in mm

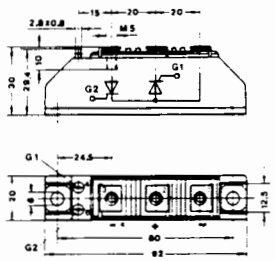
M_1 Case to heatsink
M_2 Busbars to terminals

1 Nm ≈ 0.1 mkp ≈ 9 lb. in.

1) Internal insulation: beryllium oxide

Case A 5 **SEMIPACK® 1**

TO-240 AA

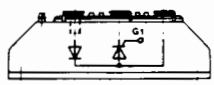


UL approved
No. E 63532

M_1 = 5 Nm ± 15%
M_2 = 3 Nm ± 15%

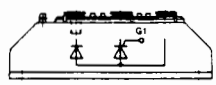
SKKT 19...105 w = 120 g

Case A 6



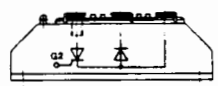
SKKH 26...105

Case A 7



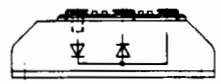
SKNH 19...56

Case A 9



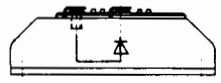
SKKL 56, SKKL 91

Case A 10



SKKD 46, SKKD 81

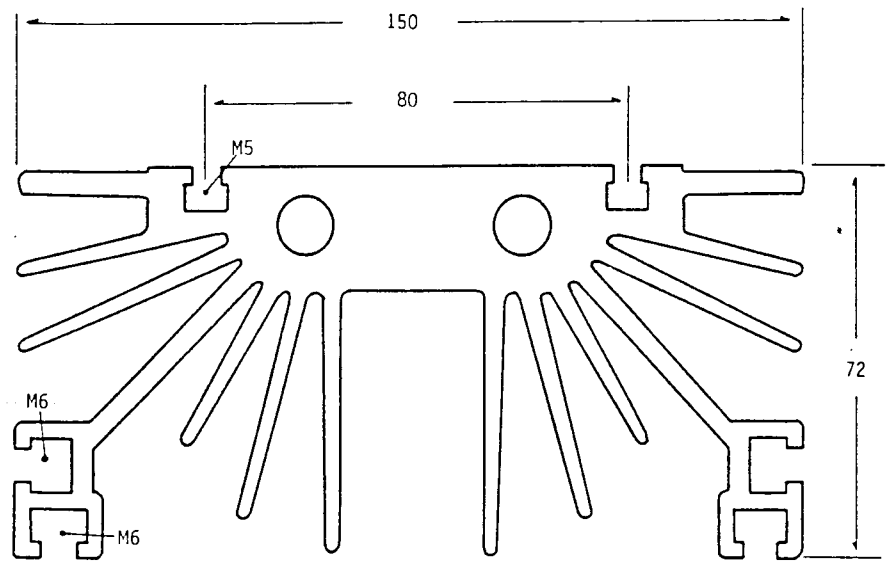
Case A 12



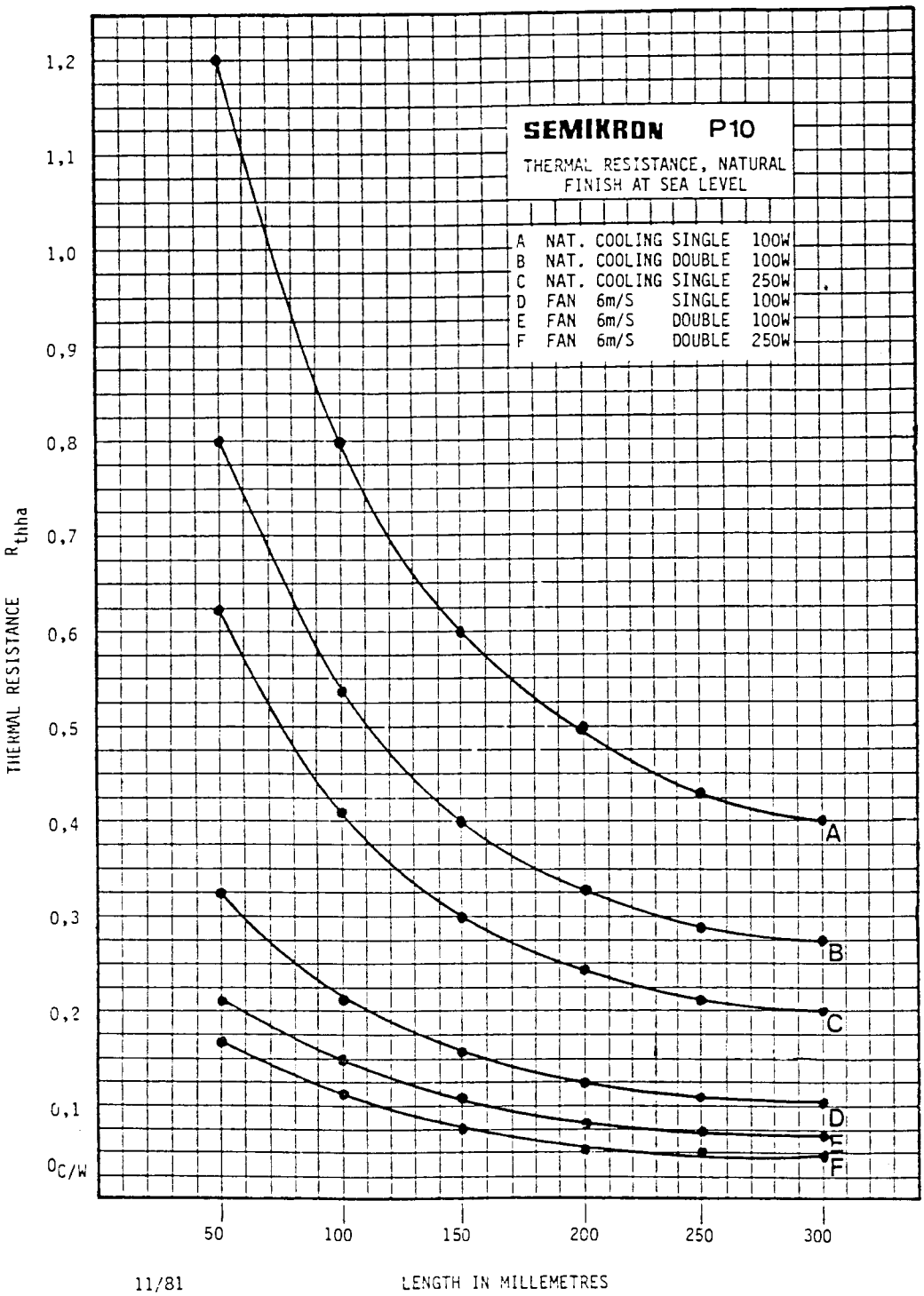
SKKE 81

Semikron P10 Heatsink

P 10



DEVICE	COND/CONFIG	P10/50	P10/100	P10/150	P10/200	P10/300
BRIDGES - ISOLATED BASE MODULES						
SKB 25	R	14A	15A	16,5A	-	-
	C	12A	13A	14A	-	-
SKB 30	R	21A	24A	28A	-	-
	C	18A	21A	24A	-	-
SKB 50	R	-	29A	32A	36A	-
	C	-	24A	28A	31A	-
SKD 25	R/C	16A	17,5A	19A	-	-
SKD 30	R/C	-	25A	30A	-	-
SKD 50	R/C	27A	31A	38A	42A	-
SKB 33	Sin 180	-	19A	21A	23A	-
DEVICE	CONDUCTION	P10/115	P10/150	P10/200	P10/250	P10/150 FAN
DIODES - DOUBLE-SIDED COOLING						
SKN 500	Sin 180	240A	260A	280A	320A	580A
	Rec 120	220A	240A	260A	300A	550A
SKN 870	Sin 180	240A	260A	280A	330A	700A
	Rec 120	220A	240A	260A	310A	670A
THYRISTORS - DOUBLE-SIDED COOLING						
SKT 230	Sin 180	95A	115A	140A	152A	275A
	Rec 120	85A	105A	130A	140A	250A
SKT 330	Sin 180	115A	135A	155A	170A	350A
	Rec 120	105A	125A	145A	160A	320A
SKT 450	Sin 180	120A	145A	170A	180A	400A
	Rec 120	110A	135A	155A	170A	370A
SKT 630	Sin 180	145A	175A	200A	210A	550A
	Rec 120	135A	160A	185A	200A	520A


SEMIKRON P10
THERMAL RESISTANCE, NATURAL FINISH AT SEA LEVEL
A NAT. COOLING SINGLE 100W
B NAT. COOLING DOUBLE 100W
C NAT. COOLING SINGLE 250W
D FAN 6m/S SINGLE 100W
E FAN 6m/S DOUBLE 100W
F FAN 6m/S DOUBLE 250W
THERMAL RESISTANCE R_{thha}
1,2
1,1
1,0
0,9
0,8
0,7
0,6
0,5
0,4
0,3
0,2
0,1
0°C/W
A
B
C
D
E
F
50
100
150
200
250
300
11/81
LENGTH IN MILLEMETRES

HEF 4752 PWM Controller

A.C. MOTOR CONTROL CIRCUIT

The HEF4752V is a circuit for a.c. motor speed control utilizing LOCMOS technology. The circuit synthesizes three 120° out of phase signals, of which the average voltage varies sinusoidally with time in the frequency range 0 to 200 Hz. The method employed is based upon the pulse width modulation principle, in order to achieve a sufficient accuracy of the output voltages over the whole frequency range. A pure digital waveform generation is used.

All outputs are of the push-pull type. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

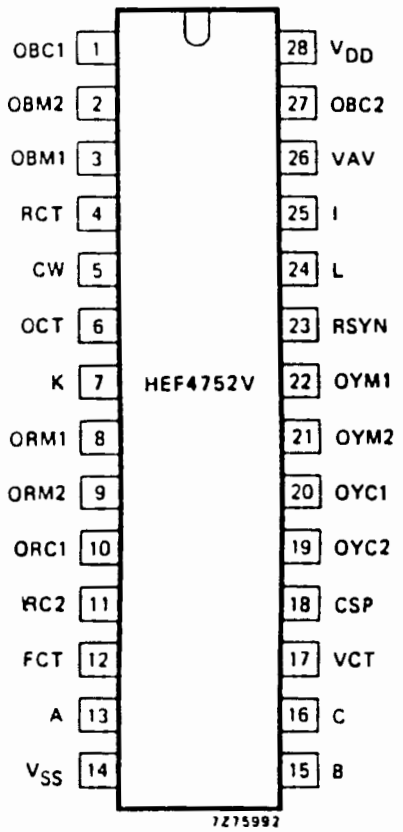


Fig. 1 Pinning diagram.

HEF4752VP: 28-lead DIL; plastic (SOT-117).
HEF4752VD: 28-lead DIL; ceramic (SOT-135).

PINNING

Inputs; group I		Inputs; group II	
24 = L	data	12 = FCT	frequency clock
25 = I	data	17 = VCT	voltage clock
7 = K	data	4 = RCT	reference clock
5 = CW	data	6 = OCT	output delay clock
13 = A	data		
15 = B	data		
16 = C	data		

Outputs; group I

23 = RSYN	R-phase synchronization
26 = VAV	average voltage
18 = CSP	current sampling pulses

Outputs; group II

8 = ORM1	R-phase main
9 = ORM2	R-phase main
10 = ORC1	R-phase commutation
11 = ORC2	R-phase commutation
22 = OYM1	Y-phase main
21 = OYM2	Y-phase main
20 = OYC1	Y-phase commutation
19 = OYC2	Y-phase commutation
3 = OBM1	B-phase main
2 = OBM2	B-phase main
1 = OBC1	B-phase commutation
27 = OBC2	B-phase commutation

SUPPLY VOLTAGE

	rating	recommended operating
HEF4752V	−0,5 to 18	4,5 to 12,5 V

FAMILY DATA see Family Specifications

D.C. CHARACTERISTICS V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 max.	+ 85 min.	+ 85 max.	unit	conditions
Quiescent device current	5	I_{DD}	–	50	–	50	–	375	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		–	100	–	100	–	750	μA	
Input leakage current	10	$\pm I_{IN}$	–	–	–	0,3	–	1	μA	V_I = 0 or 10 V
Input voltage HIGH	5	V_{IH}	3,5	–	3,5	–	3,5	–	V	inputs: group I
	10		7,0	–	7,0	–	7,0	–	V	
Input voltage LOW	5	V_{IL}	–	1,5	–	1,5	–	1,5	V	inputs: group I
	10		–	3,0	–	3,0	–	3,0	V	
Output voltage HIGH	5	V_{OH}	4,95	–	4,95	–	4,95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	10		9,95	–	9,95	–	9,95	–	V	
Output voltage LOW	5	V_{OL}	–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	10		–	0,05	–	0,05	–	0,05	V	
Input tripping level; input voltage increasing	5	V_{ti}	1,5	4,0	1,5	4,0	1,5	4,0	V	inputs: group II
	10		3,0	8,0	3,0	8,0	3,0	8,0	V	
Input tripping level; input voltage decreasing	5	V_{td}	1,0	3,5	1,0	3,5	1,0	3,5	V	inputs: group II
	10		2,0	7,0	2,0	7,0	2,0	7,0	V	
Output current LOW	5	I_{OL}	0,45	–	0,38	–	0,3	–	mA	V_{OL} = 0,4 V; outputs: groups I and II
	10		1,4	–	1,17	–	0,9	–	mA	V_{OL} = 0,5 V
Output current HIGH	5	$-I_{OH}$	0,3	–	0,25	–	0,2	–	mA	V_{OH} = 4,6 V; outputs: group I
	10		0,9	–	0,75	–	0,6	–	mA	V_{OH} = 9,5 V
Output current HIGH	5	$-I_{OH}$	0,9	–	0,75	–	0,6	–	mA	V_{OH} = 2,5 V; outputs: group I
Output current HIGH	5	$-I_{OH}$	0,6	–	0,5	–	0,4	–	mA	V_{OH} = 4,6 V; outputs: group II
	10		1,8	–	1,5	–	1,2	–	mA	V_{OH} = 9,5 V
Output current HIGH	5	$-I_{OH}$	1,8	–	1,5	–	1,2	–	mA	V_{OH} = 2,5 V; outputs: group II
Total supply current	10	I_{tot}	–	–	typ. 2		–	–	mA	$I_{OL} = I_{OH} = 0$; frequency applied to inputs; FCT = 700 kHz; VCT = 400 kHz; RCT = 400 kHz

APPLICATION INFORMATION

Figure 2 shows the functional block diagram of a 3-phase a.c. motor speed control system using a thyristorized inverter with variable frequency output. The inverter control signals are generated by the HEF4752V (PWM-IC). A special feature of the PWM (Pulse-Width Modulation) - IC is here, that the motor is supplied by sinnoidally modulated pulses, hence the resulting motor current will approach a sine-wave with a minimum on higher harmonics. In this way, an optimum speed drive with high performance is obtained.

Furthermore, the HEF4752V contains all logic circuitry required for this special waveform generation, so that the amount of control circuit components is reduced considerable. The speed drive system in Fig. 2 is controlled by the analogue control section.

The FCT and VCT clock pulse oscillators are driven in such a way, that a fast response speed control of the a.c. motor is obtained, depending on: the reference values for speed; motor voltage; motor current (Limited by the measured motor current via DCCT - d.c. current transformer -); the increasing value of V_{Cb} during braking action.

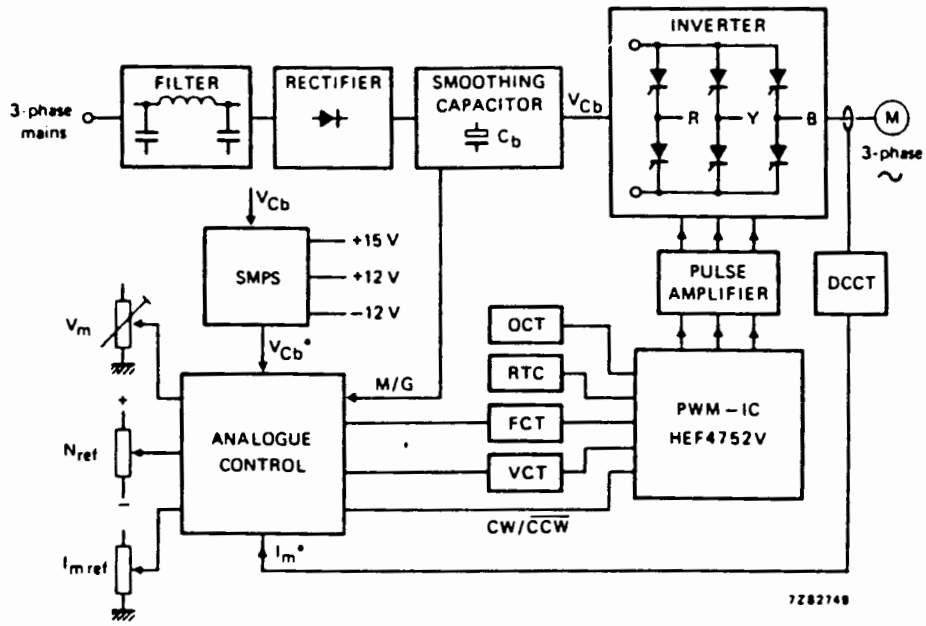


Fig. 2 PWM motor speed control system using HEF4752V.

MORE APPLICATION INFORMATION SUPPLIED ON REQUEST

APPENDIX B

CALCULATIONS

1 PEAK CURRENT IN THE POWER TRANSISTOR

This section calculates the RMS and peak currents that can be expected in the power transistor.

Transformer ratio => 176V : 580V
=> 1 : 3,29

The Maximum RMS output voltage of the converter at full load and PWM modulation factor 2 (table 100) is 650V.

The RMS input voltage is therefore:

$$V_{RMS} = 650V / 3.29$$
$$= 198V$$

If we assume an inverter efficiency of 85%, with an output power of 20KVA, the power delivered by the inverter is:

$$\frac{20kVA}{0.85} = 23.5kVA$$

The RMS current into the primary of input transformer is therefore:

$$I = \frac{P}{V} = \frac{23,5KVA}{198V} = 119 \text{ Amps}$$

If a sinusoidal waveform is assumed (best case), the peak current is:

$$I_{pk} = 119 \times \sqrt{2} = 168A$$

If a square wave voltage driving into an inductance is assumed, i.e. a triangular wave current (worst case).

$$I_{pk} = 1{,}75^{1} \text{ X } I_{RMS}$$

$$\Rightarrow \quad I_{pk} = 207 \text{ Amps}$$

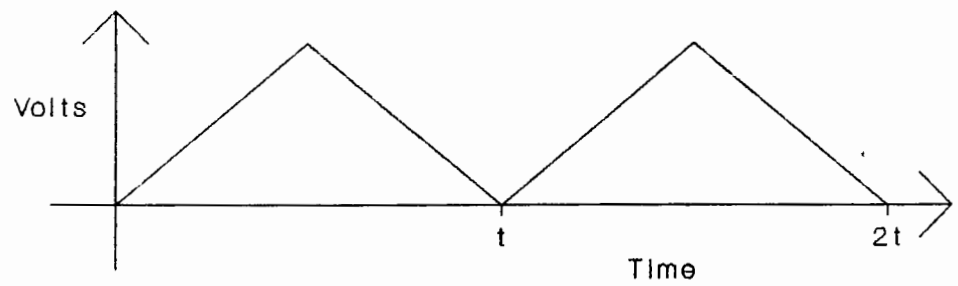
To be realistic the actual current peak under normal operation will be between the sine and triangular wave peak. With a modulation factor of 2 (not a square wave) and a load that is resistive as well as inductive, the peak current can be approximated to be 190A. Graphs of the collector current can be found in section 4.5.

---

1 - This figure is derived in the following section.

2 CALCULATION OF PEAK VS RMS RATIO OF A TRIANGULAR WAVEFORM

Assume a triangular wave, with a peak voltage of V_{pk} and a period of 1s, as in the diagram below.



The function of the rising slope is:

$$f(t) = V_r = 2t \times V_{pk}$$

and for the falling slope is:

$$f(t) = V_f = (-2t + 2) Vpk$$

The RMS voltage is therefore

$$V_{RMS} = \sqrt{ \left(\int_0^{0.5} (Vpk \times 2t)^2 \, dt + \int_{0.5}^{1} (Vpk \, (-2t + 2))^2 \, dt \right)}$$

$$= \sqrt{ \left(V_{pk}^2 \int_0^{0.5} 4t^2 \, dt + \int_{0.5}^{1} (4 - 8t - 4t^2) \, dt \right)}$$

$$= V_{pk} \sqrt{ \left(\left[4/3 \, t^3 \right]_0^{0.5} + \left[4t - 8/2 \, t^2 + 4/3 \, t^3 \right]_{0.5}^{1} \right)}$$

$$= V_{pk} \sqrt{(4/3 \times .5^2 + 4 - 4 + 4/3 - 2 + 4 \times .5^2 - 4/3 \times 0.5^2)}$$

$$= V_{pk} \sqrt{ (1.33 - 2 + 1)}$$

$$= V_{pk} \sqrt{ 0.33}$$

$$= V_{pk} \times 0.574$$

$$\Rightarrow \quad V_{pk} = 1.74 \times V_{RMS}$$

3 CURRENT DRAWN FROM THE POWER SUPPLY

Most of the current is used to drive the base of the Power Transistor, which is calculated as follows:

Peak collector current in the Power Transistor is 190 Amps

To be conservative, assume a constant current of 250 Amps, to account for:

- worse efficiency than expected
- current imbalance
- current spikes

From the datasheets in Appendix A, there is no value for the gain of the transistor for:

$$V_{CE} = 3V$$
$$t_{vj} = 125^{o}C$$

An approximation from the graph in the data sheet gives:

$$B \approx 150 \quad \text{(for a 300R600K}^{2}\text{)}$$

The Current drawn through R15 to the power transistor is therefore:

$$I_B = 250/150 = 1,67A$$

To calculate the current through the other resistors connected to the positive supply rail, the lowest impedance current path was chosen, as an approximation.

Current through R10	≈	6.5V/(100 + 560)	= 10mA
Current through R7	≈	6.5V/(120 + 330)	= 15mA
Current through R6	≈	6.5V/(120 + 100)	= 30mA
Current through Q1	≈	6.5V/100	= 65mA
Current through R12		(current source)	≈ 200mA[3]
		Total	= 320mA

---

2 - Note that the gain of the 300R1000K is higher.

3 - Note that most of this current will go into the base of Q5 and into the base of the power transistor.

The total peak current drawn from the supply is thus ≈ 2A

This figure is the total current drawn when the base drive is "on". When it is "off" it draws almost no current at all. The average power is thus just over half of the peak current.

The power supply was conservatively designed to supply 3 Amps continuously, to enable it to supply the peak current of 2 Amps at all times, and still have a reserve capacity.

4 CALCULATION OF RCD SNUBBER COMPONENTS

A diagram of the RCD snubber is shown in figure 4.9 in Chapter 4. The following equations are given by AEG [3] to calculate the snubber component values.

$$\text{Equation 1 -} \qquad C \geq \frac{I_{CM}}{dV_{CE}/dt}$$

$$\text{Equation 2 -} \qquad R \geq \frac{V_{CE}}{I_{CRM}}$$

$$\text{Equation 3 -} \qquad R \leq \frac{t_{fg\ min}}{4 \times C}$$

Where:

I_{CM}	highest value of collector current to be turned off
dV_{CE}/dt	rate of voltage rise at turn-off
V_{CE}	collector-emitter voltage immediately prior to turn on
I_{CRM}	maximum permissible repetitive peak collector current
$t_{fg\ min}$	minimum collector-emitter conduction duration

Equation 1, used to calculate the snubber capacitance, is based on the amount of energy that is to be absorbed by the capacitor, to increase the collector voltage rise time. The pre-cut-off current is re-directed from the transistor to the capacitor via the diode. The rate at which the collector voltage rises depends upon the amount of current that was cut off and the capacitor size.

Equation 2 is used to calculate the minimum discharge resistance. The minimum resistance is limited by the

maximum current the transistor can withstand. This is calculated when the capacitor is discharging through the transistor, immediately when it switches on.

The resistance must also be low enough to ensure that the capacitor discharges rapidly enough. The maximum resistance value is thus calculated using equation 3. An RC time constant of 1/4 of the minimum pulse width has been chosen. This enables the capacitor to discharge to 1.8% of the DC bus, in this case to 4,5V.

The pulse widths vary in size, from 40us to around 8ms. An approximation must therefore be made as what pulse width should be used in the calculations. A minimum pulse width of 250us[4] was approximated.

For the convertor

I_{CM} = 200 Amps
d_{VCE}/dt = 250 V/us
V_{CE} = 250 Volts
I_{CRM} = 600 Amps
$t_{fg\ min}$ = 250 us

From the equations:

$$C = \frac{250V}{250V/us} = 0.8uF \quad \text{(1uF was used)}$$

$$R \geq \frac{250V}{600A} = 2.2\ \text{Ohms}$$

$$R \leq \frac{250us}{4 \times 1uF} = 61\ \text{Ohms}$$

A resistance of 47 Ohms was chosen

Graphs of snubber waveforms can be seen in section 4.5.4.4

---

4 - Because of the nature of sine weighted PWM, the capacitor has long times to discharge when the transistor has conducted a high current, which is when it is most needed.

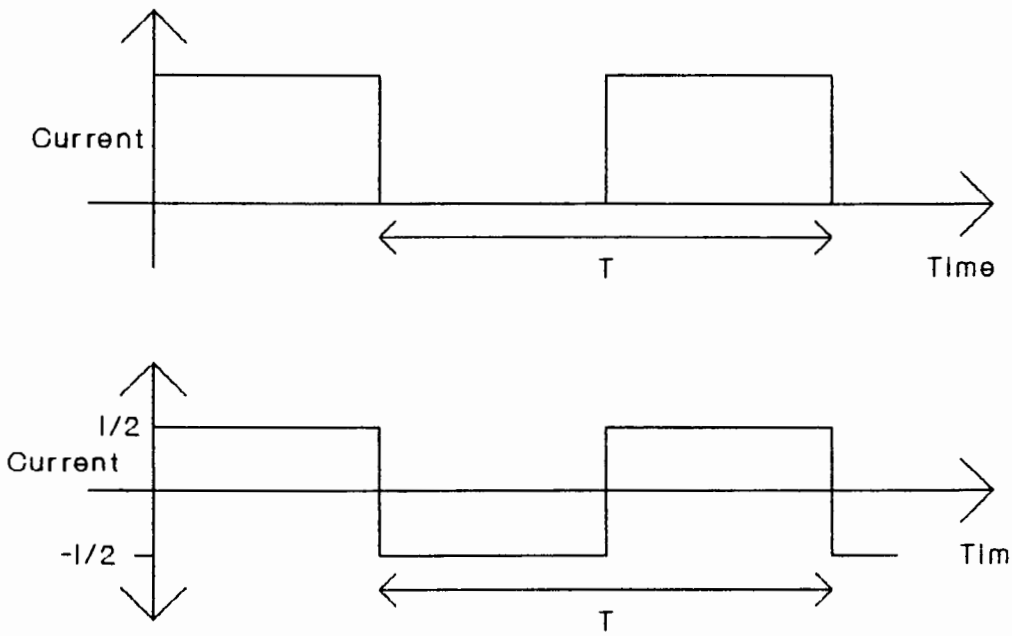
5 RMS CURRENT DIFFERENCE BETWEEN THE PUSH-PULL AND THE FULL BRIDGE TRANSFORMER WINDINGS

To calculate the current in each winding, a square wave current is assumed to represent the PWM waveform. In practice the waveform is not square, but any waveform can be represented by smaller square waves.

For the push-pull inverter, each PWM current pulse passes through one winding. For every pulse in one winding there is an equal pulse in the other winding.

In a full bridge inventor, half the current is continually passing through both windings. For each PWM pulse in one direction, an equal pulse conducts in the opposite direction.

The waveforms that would result in a square wave current are thus:



a) Push-pull
b) Full bridge

A period of 1 is assumed.

The RMS current in a push-pull inverter winding is:

$$I_{RMS\ pp} = \sqrt{\left(\int_0^{0.5} I^2\, dt + \int_{0.5}^{1} 0\, dt \right)}$$

$$= \sqrt{\left[I^2 \times t \right]_0^{0.5}}$$

$$= I \times \sqrt{0.5}$$

$$= 0.707 \times I_{pk}$$

and for the full bridge inverter, the RMS current in each winding is :

$$I_{RMS\ fb} = \sqrt{\left(\int_0^{0.5} (0.5 \times I)^2\, dt + \int_{0.5}^{1} (0.5 \times I)^2\, dt \right)}$$

$$= I \times \sqrt{(0.25x0.5 + 0.25x1 - 0.25x0.5)}$$

$$= I \times \sqrt{0.25}$$

$$= 0.5 \times I$$

Therefore: $I_{RMS\ pp} = I_{RMS\ fb} \times 0.707/0.5$

$$= I_{RMS\ fb} \times \sqrt{2}$$

6 POWER DISSIPATION IN THE HEATSINK

Power Dissipation arises from different components for different reasons. On the main heatsink, losses are generated by the transistor conduction voltage drop, switching and the freewheeling diode conduction voltage drop. These calculations assumes that the water cooling has not been connected.

Conduction Losses

For the C300R600K:

$V_{CE\ SAT}$ (at 190 Amps and I_B = 1.5 Amps) $\approx$ 1.5 Volts

It is assumed that the voltage drop is constantly at its maximum of 1.5V. The conduction losses are therefore:

$$\Rightarrow P_{cond} = I_{RMS} \times V_{CE}$$
$$= 119A \times 1{,}5V$$
$$= 179W$$

A transistor is on for half the time, but there are two transistors per heatsink. The power to be dissipated by a heatsink, due to the two transistor's heating effect, is therefore 285W.

Switching losses

Switching losses are difficult to predict, as switching times vary, depending how effective the base drive is. Linear approximations to the waveforms must also be made. The switching times used in these calculations were derived from the datasheet, but they can be varified by comparing them to the graphs in section 4.5.

The calculations are performed assuming a modulation factor of around 1.8 (Table 90). There are therefore six on and off switches per cycle. It is assumed that for half of the switches the transistor does not carry any current (current is negative and freewheels) and that it

carries the full current for the remaining three switches. There are therefore six switches per cycle per heatsink.

The following figures are used:

DC voltage	=	250V
I_{RMS}	=	119A
Period	=	8.33ms

Switch on losses

The time it takes the collector voltage to fall, and the current to rise is around 0.5us. During this time the current and voltage can be assumed to rise and fall linearly. The peak power dissipated is where the two curves cross, at 125V and 60amp. This peak is assumed for the 0.5us.

Instantaneous power loss per switch is thus

$$125V \times 60A = 7500W$$

Occurring 6 times per cycle, each 0.5us long, the average power loss is:

$$P_{on} = 6 \times 7500 \times (0.5 / 8333)$$

$$= 3W$$

This is minute, but is to be expected, as switch on losses are usually very small.

Switch off losses

The turn-off time is in the region of 10us. During this time, both the voltage and current remain constant, for around 3us. The voltage then rises and towards the end of the storage time the current falls. The snubber capacitor also limits the rate of rise of the voltage.

To approximate the switching, it has been assumed that the full DC bus is across the transistor as well as the full collector current, for 5us.

Instantaneous power loss per switch is thus:

$$P = 250V \times 119A = 30KW$$

Occurring 6 times per cycle, each 5us long, the average power loss is:

$$P_{off} = 6 \times 30kW \times (5 / 8333)$$
$$= 108W$$

Power loss in freewheeling diode

When current flows through the diode, no current flows through the transistor. As the voltage drop across the transistor is higher than that of the diode, it is therefore conservative for calculation purposes, to assume that no current flow through the diode, and that current only flows through the transistor.

Heatsink temperature rise

From the graph of Semikron P10 heatsink found in Appendix A, double cooling, 300W, 300mm, gives an approximate thermal resistance of 0,15 $^{o}C/W$

From the transistor datasheets

$$R_{th\ JC} = 0,078\ ^{o}C/W$$
$$R_{th\ CH} = 0,03\ ^{o}C/W$$

Therefore : $R_{th\ JA} = 0.15 + 0.078 + 0.03$
$= 0,268\ ^{o}C/W$

The Total Power Loss is:

$$P_{tot} = 179 + 3 + 108$$
$$= 290\ W$$

The temperature rise is thus:

$$T = 290\ W \times 0,268\ ^{o}C/W = 78\ ^{o}C$$

Max ambient temperature was specified as 40 ^{o}C.

=> Junction temp = 40 + 78 = 117 ^{o}C

From the datasheets the maximum allowable junction temp is 125 ^{o}C. It was decided though, to be conservative and to add water cooling.

When the converter was tested in Van der Bijl Park, the heatsink temperature, directly next to the transistor, rose to approximately 60^{o}C, 32^{o}C above the ambient temperature of 28^{o}C.

The power produced by the transistors is thus:

$$P = \frac{T}{R_{th\ HA}} = \frac{32}{0.15} = 213W$$

And the junction temperature

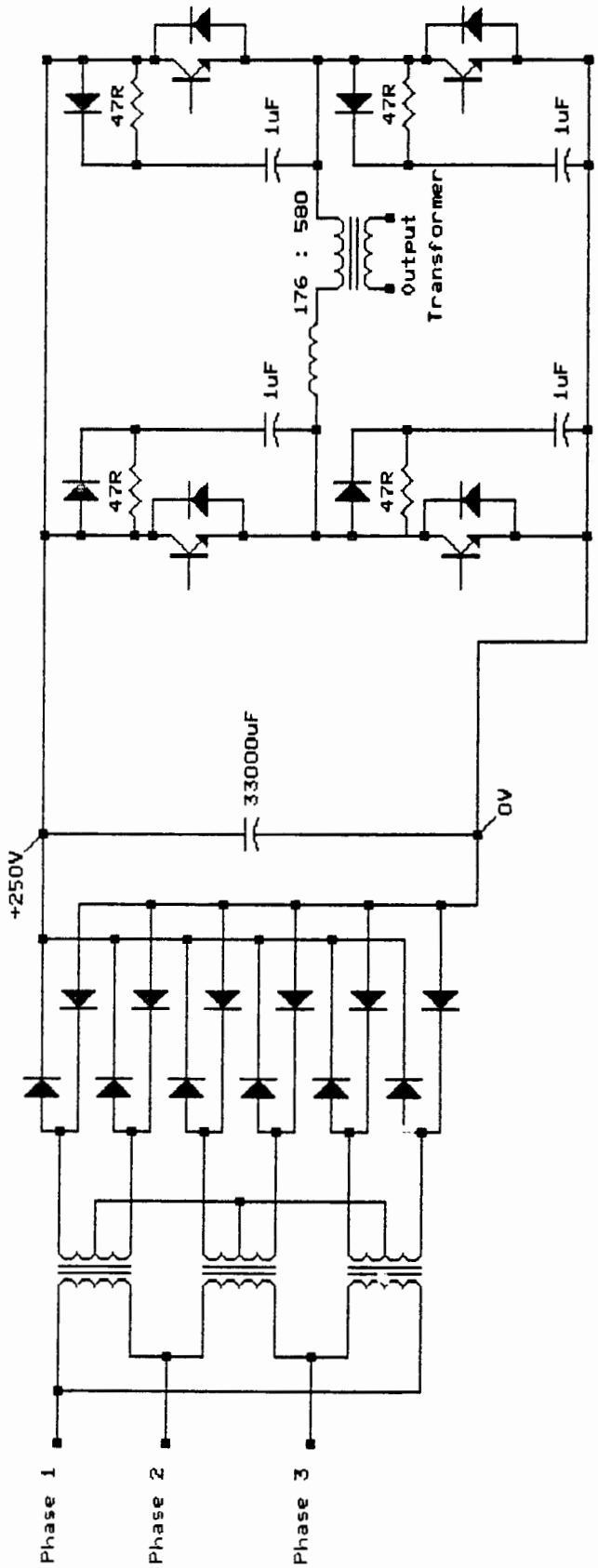
$$t_j = 28 + (213 \times 0.268) = 85^{o}C$$

This is lower than expected, but the converter was expected to run at a higher power in Spain. Water cooling was added, but because of the high humidity in Durban, moisture condensed on the heatsink. A thermal switch and a valve were added to the water inlet, to allow the cooling water to flow only when the heatsink temperature rose above 50^{o}C.

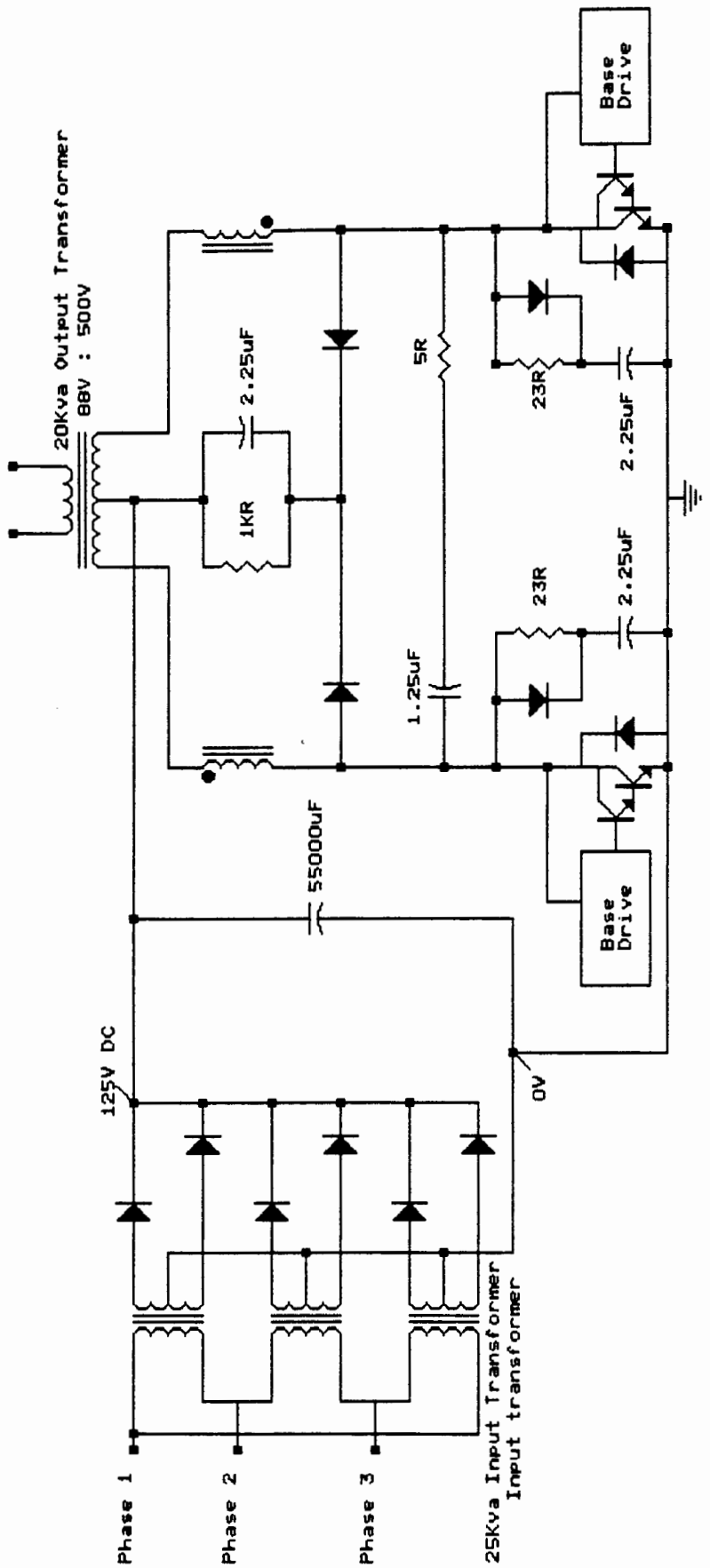
APPENDIX C

CIRCUIT DIAGRAMS

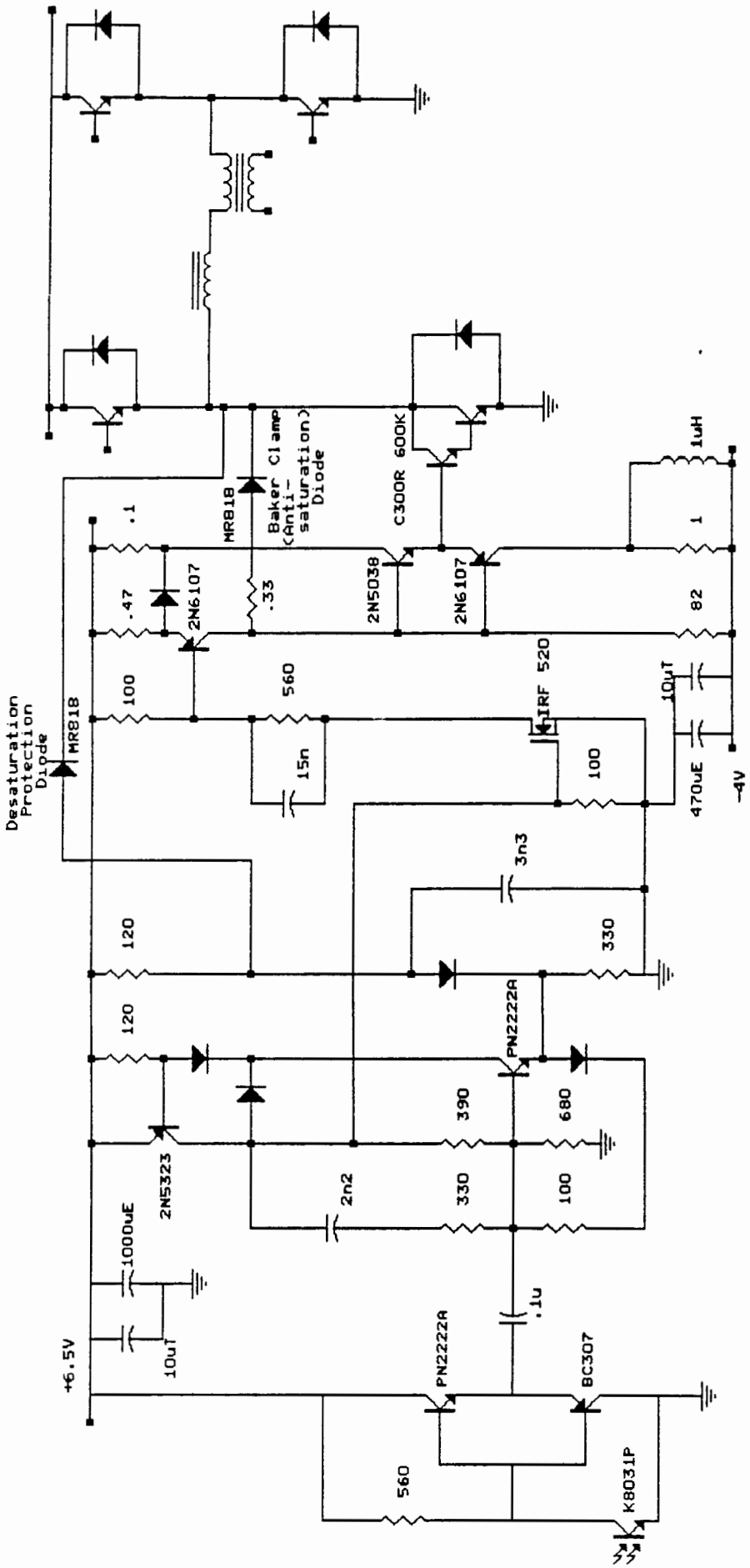
Complete Converter Diagram (Full Bridge configuration)



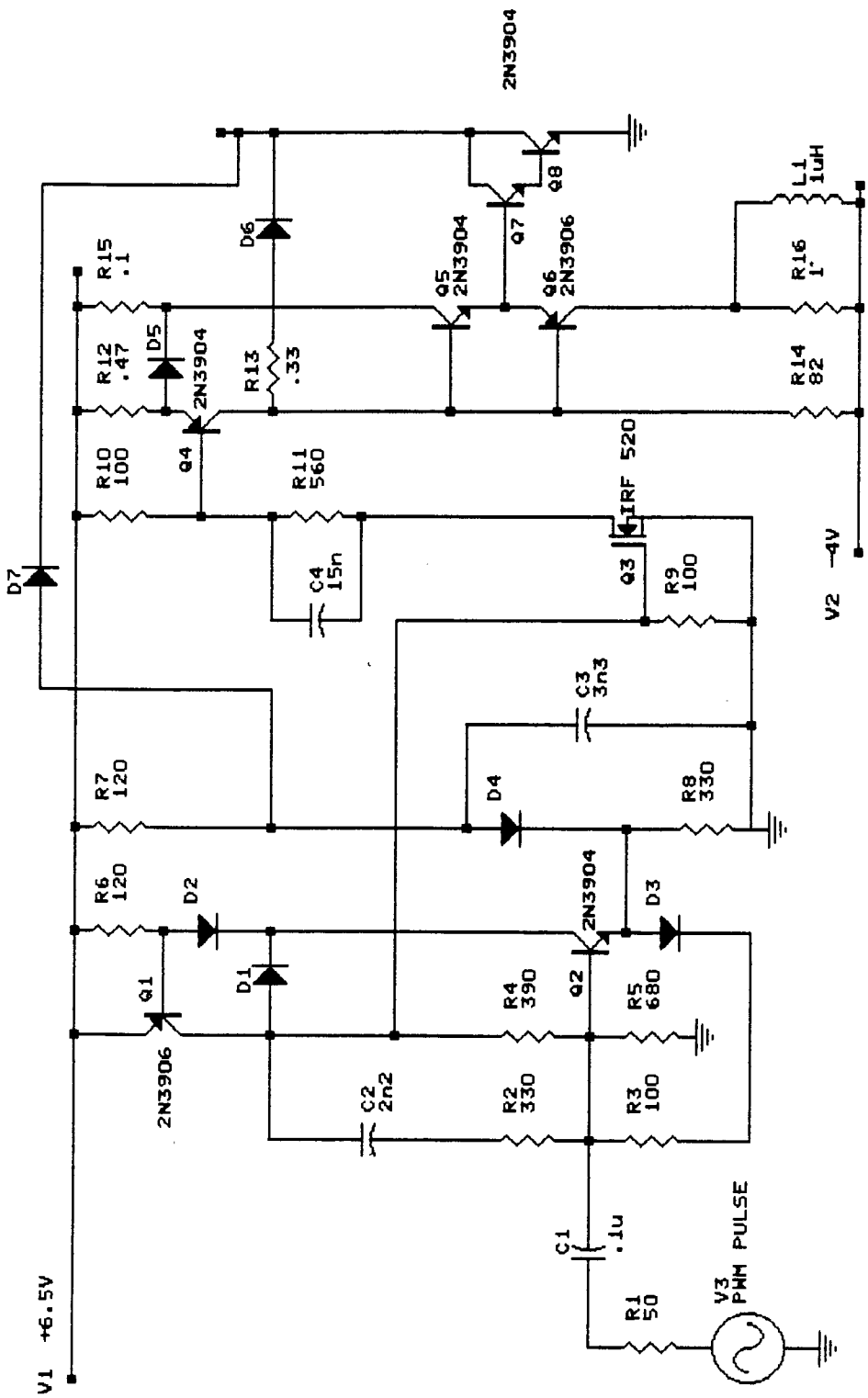
Complete Converter Diagram (Push-Pull configuration)



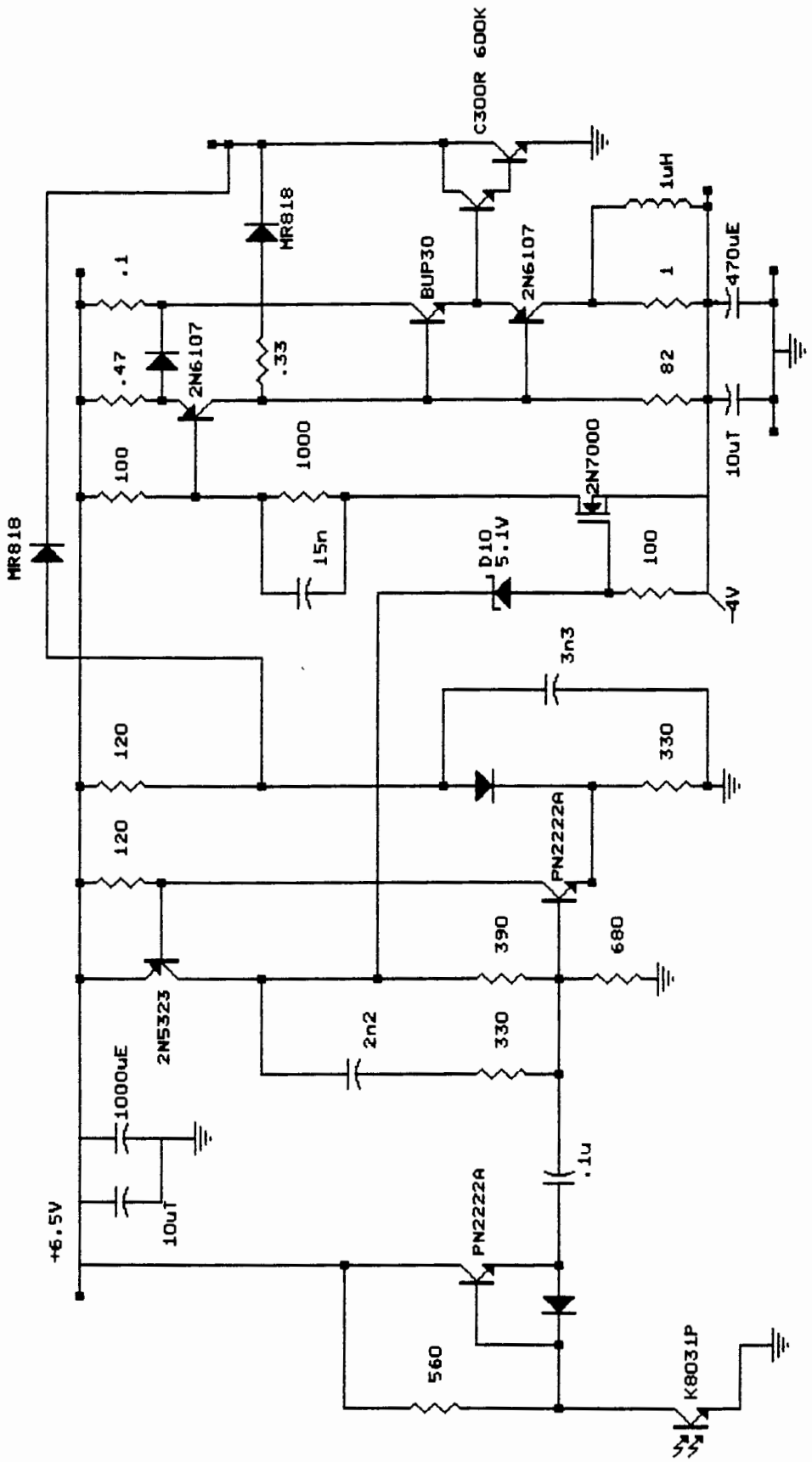
Base Drive Circuit (As it was in the Converter)



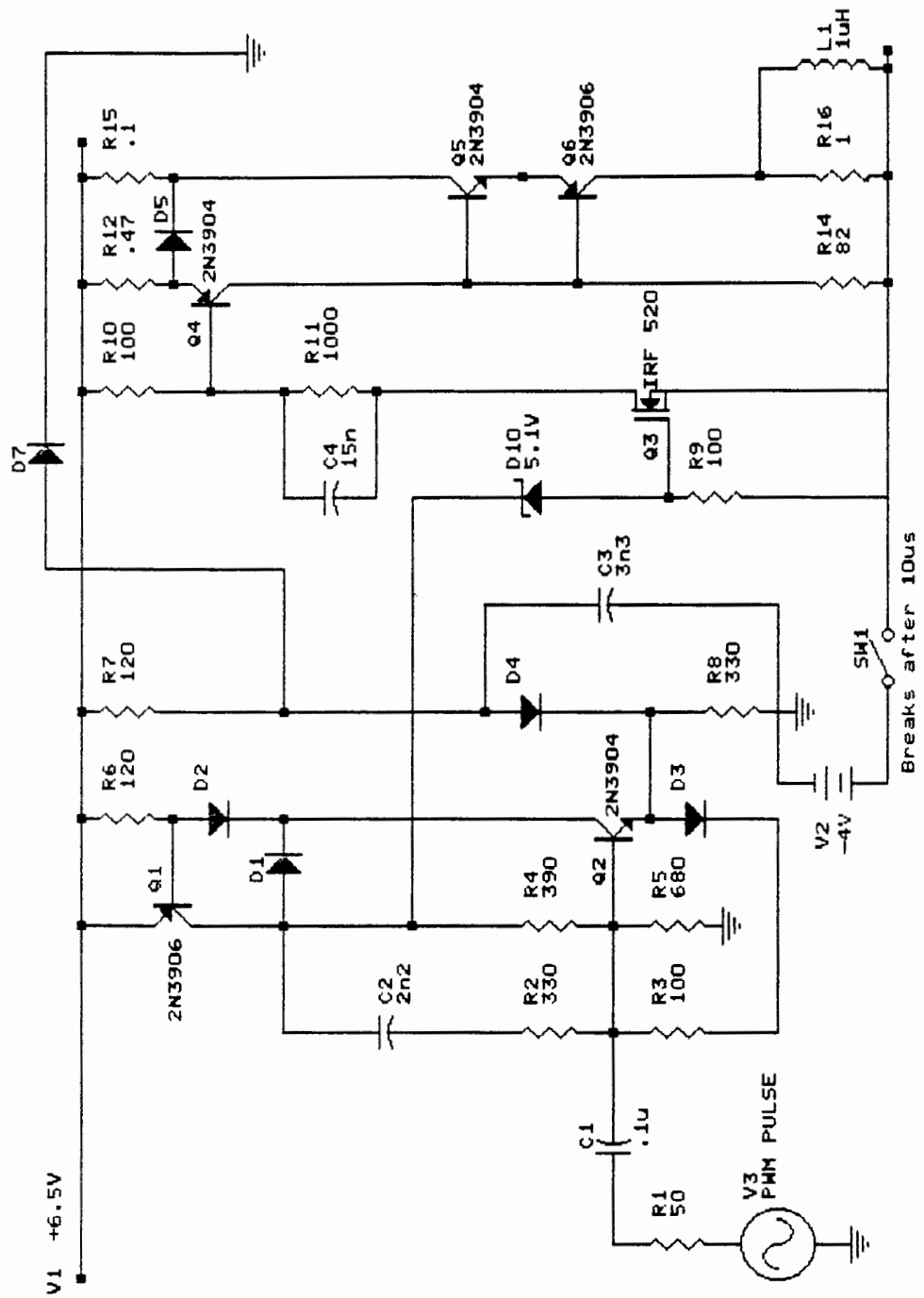
Pspice Model of the Base Drive Circuit



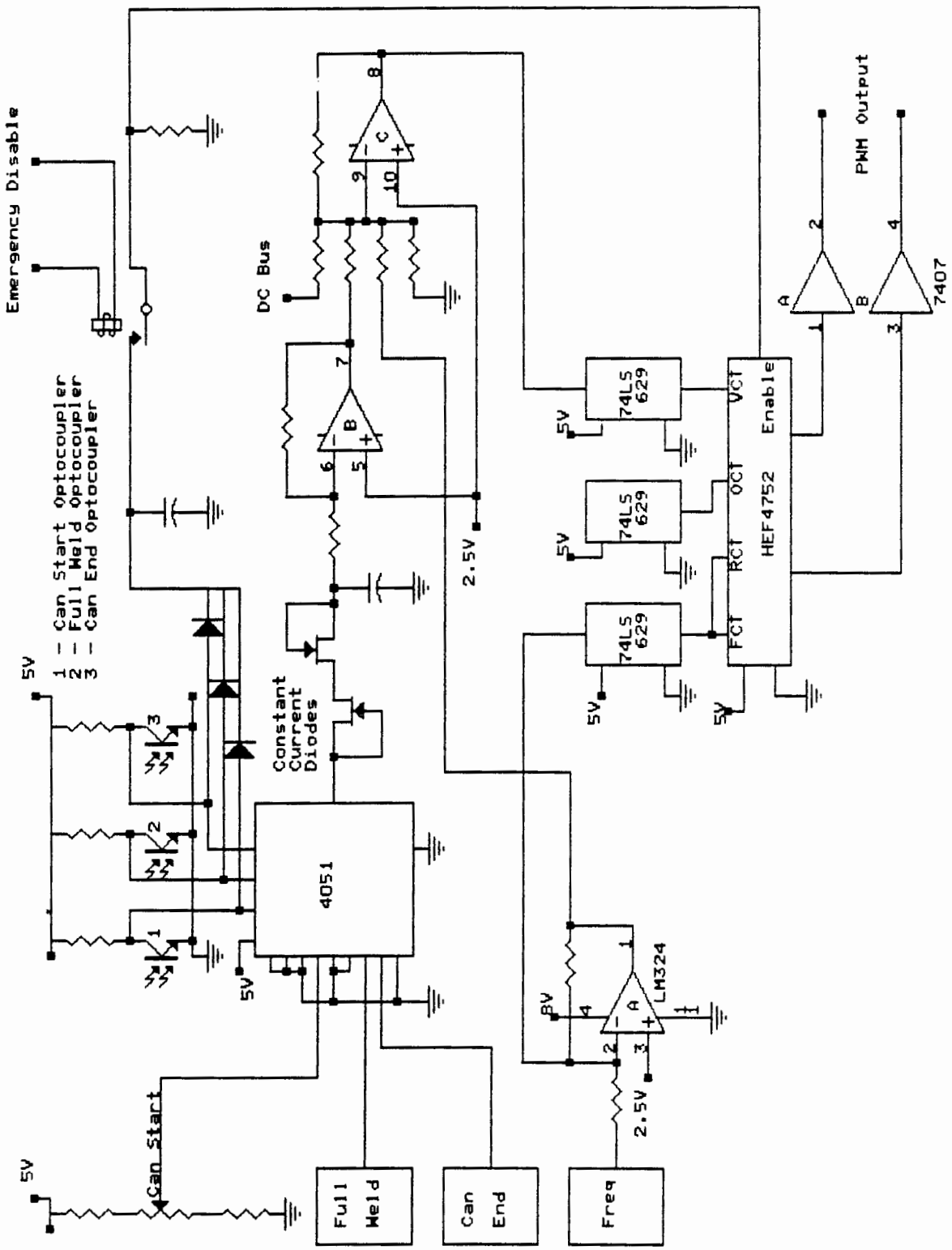
Base Drive Circuit with Modifications



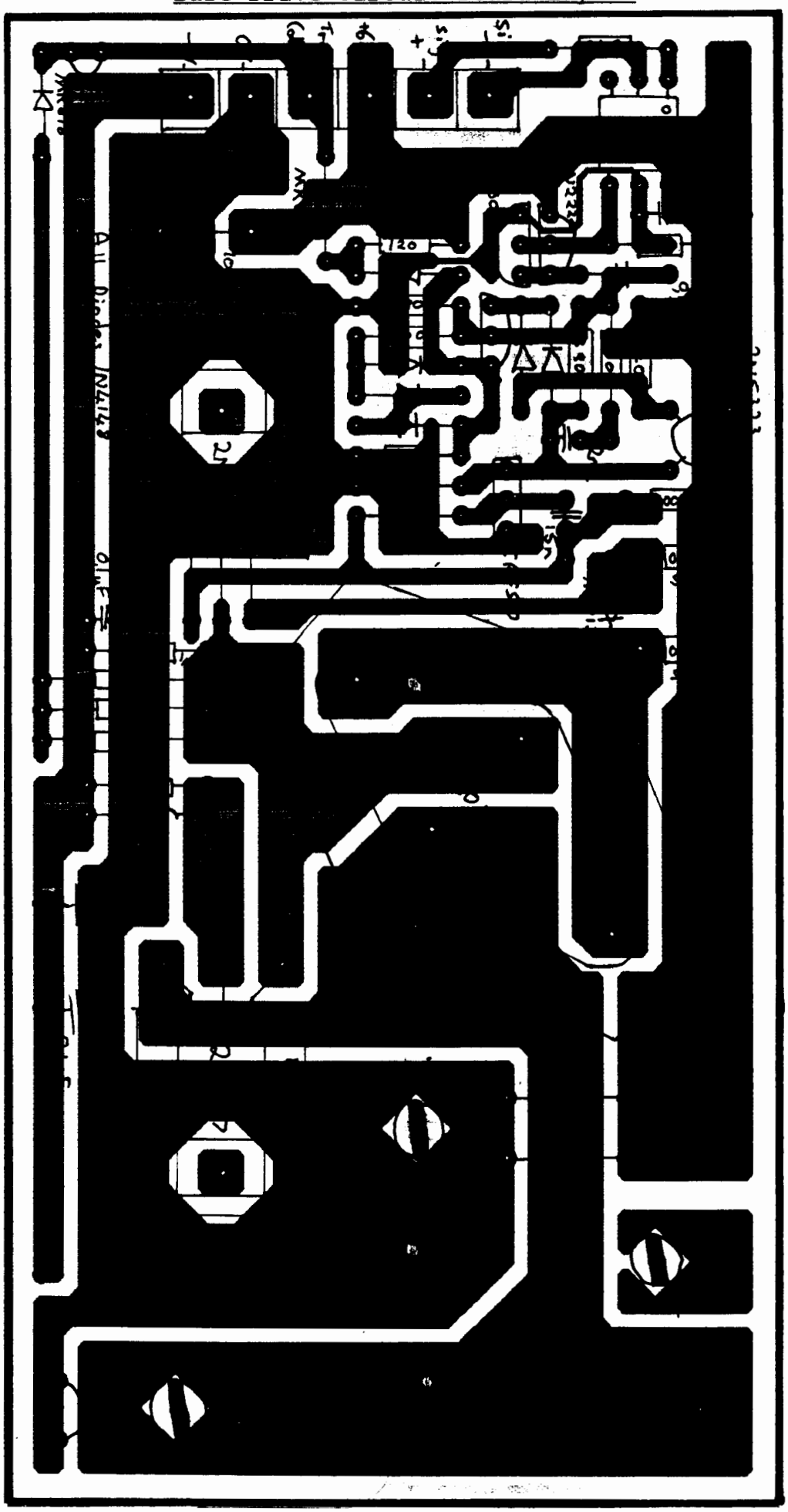
Pspice Model of the Base Drive Circuit with Modifications



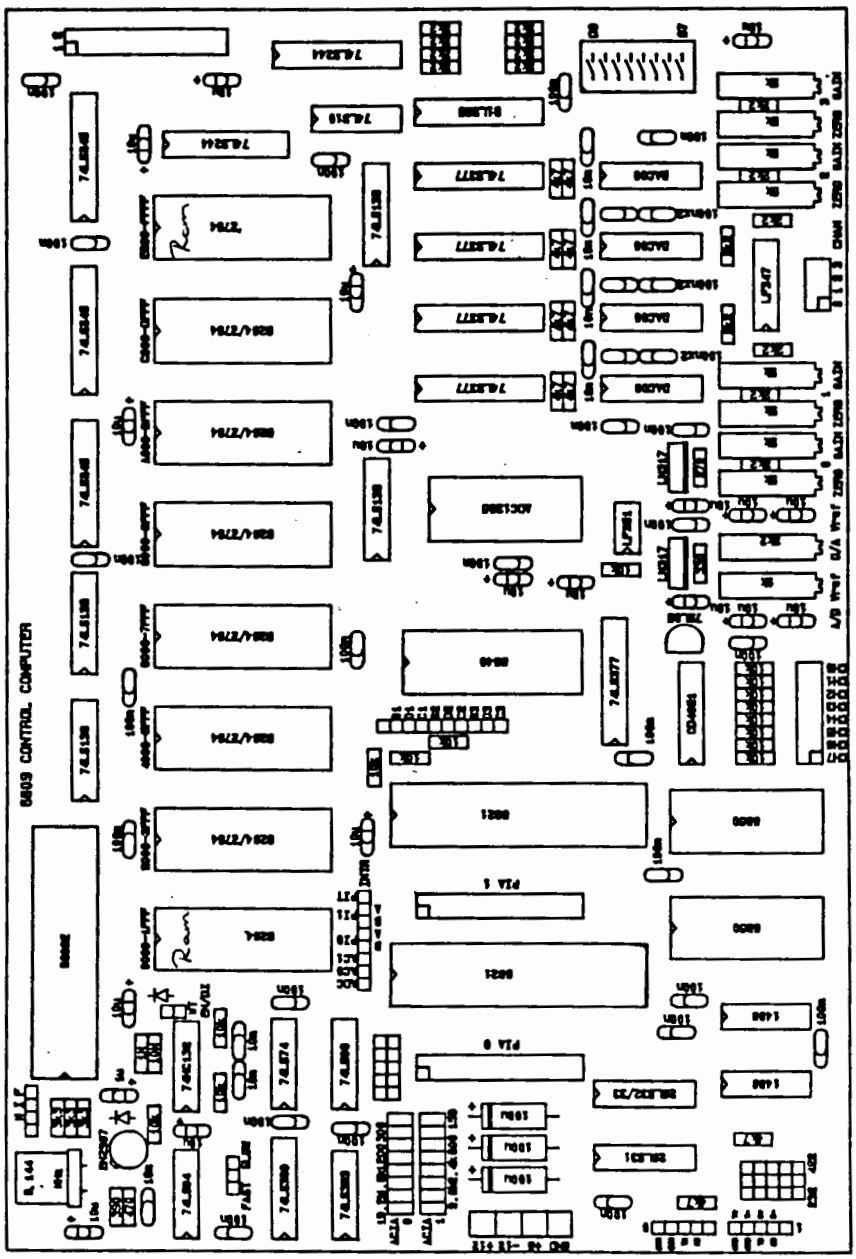
Analogue PWM Generator



Base Drive Circuit Board Layout



Computer Circuit Board Layout



APPENDIX D

PSPICE PROGRAM LISTINGS

Base Drive Without Modifications

```
* Base Drive Program listing *
******************************
R1    3     4     50
R2    6     5     330
R3    5     11    100
R4    7     10    390
R5    10    0     680
R6    1     8     120
R7    1     13    120
R8    12    0     330
R9    7     0     100
R10   1     15    100
R11   15    14    560
R12   1     16    .33
R13   17    23    82
R14   17    2     1
R15   1     18    .47
R16   20    2     .1

C1    4     5     .1u
C2    7     6     2n2
C3    13    0     3n3
C4    15    14    15n

D1    7     7     D1N4148
D2    8     9     D1N4148
D3    12    11    D1N4148
D4    13    12    D1N4148
D5    16    18    D1N4148
D6    23    24    D1N4148
D7    13    25    D1N4148

Q1    8     7     1     1     Q2N3906
Q2    10    9     12    12    Q2N3904
Q3    7     14    0     0     MIRF520
Q4    15    17    16    16    Q2N3906
Q5    17    18    19    19    Q2N3904
Q6    17    20    19    19    Q2N3906
Q7    21    24    22    22    Q2N3904
Q8    22    24    0     0     Q2N3904

V1    1     0     DC 6.5
V2    2     0     DC -4
V3    3     0     PULSE(0 6.5 10u 1u 1u 50u 1110u)
V4    25    0     PULSE(2 6 11u 1u 1u 100u 300u)
```

```
.Tran 2u 40u
.Probe

Model Q2N3904    NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03
+ Bf=416.4 Ne=1.259 Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371
+ Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5
+ Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4
+ Vtf=4 Xtf=2 Rb=10)

.Model Q2N3906    PNP(Is=1.41f Xti=3 Eg=1.11 Vaf=18.7
+ Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2
+ Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5
+ Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4
+ Vtf=4 Xtf=6 Rb=10)

.Model D1N4148    D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100
+ Ibv=0.1p)

.Model MIRF520    NMOS(Level=3 Gamma=0 Delta=0 Eta=0
+ Theta=0 Kappa=0 Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6
+ Rs=1.624m Kp=20.53u W=.3 L=2u Vto=2.831 Rd=1.031m
+ Rds=444.4K Cbd=3.229n Pb=.8 Mj=.5 Fc=.5 Cgso=1.027n
+ Cgdo=0.379n Rg=13.89 Is=194E-18 N=1 Tt=288n)

.End
```

Base Drive with negative protection

```
* Base Drive Program with negative protection *
**********************************************
R1    3     4     50
R2    6     5     330
R3    5     11    100
R4    7     10    390
R5    10    0     680
R6    1     8     120
R7    1     13    120
R8    12    0     330
R9    26    2     100
R10   1     15    100
R11   15    14    1000
R13   17    23    82
R14   17    2     1
R15   1     18    .47
R16   20    2     .1
R17   27    0     1000

C1    4     5     .1u
C2    7     6     2n2
C3    13    0     3n3
C4    15    14    15n

D1    7     7     D1N4148
D2    8     9     D1N4148
D3    12    11    D1N4148
D4    13    12    D1N4148
D5    16    18    D1N4148
D7    13    0     D1N4148
D10   26    7     D1N750

Q1    8     7     1     1     Q2N3906
Q2    10    9     12    12    Q2N3904
M3    26    14    2     2     MIRF520
Q4    15    17    16    16    Q2N3906
Q5    17    18    19    19    Q2N3904
Q6    17    20    19    19    Q2N3906

SW1   27    2     28    0     SW1

V1    1     0     DC 6.5
V2    27    0     DC -4
V3    3     0     PULSE(0 6.5 10u 1u 1u   50u 1110u)
V4    28    0     PULSE(7   0  1u 1u 1u 1000u 1000u)

.Tran 2u 40u
.Probe

Model Q2N3904     NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03
+ Bf=416.4 Ne=1.259 Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371
+ Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5
+ Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4
+ Vtf=4 Xtf=2 Rb=10)

.Model Q2N3906     PNP(Is=1.41f Xti=3 Eg=1.11 Vaf=18.7
+ Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2
```

```
+ Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5
+ Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4
+ Vtf=4 Xtf=6 Rb=10)

.Model MIRF520    NMOS(Level=3 Gamma=0 Delta=0 Eta=0
+ Theta=0 Kappa=0 Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6
+ Rs=1.624m Kp=20.53u W=.3 L=2u Vto=2.831 Rd=1.031m
+ Rds=444.4K Cbd=3.229n Pb=.8 Mj=.5 Fc=.5 Cgso=1.027n
+ Cgdo=0.379n Rg=13.89 Is=194E-18 N=1 Tt=288n)

.Model D1N4148    D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100
+ Ibv=0.1p)

.Model D1N750     D(Is=1u Rs=2 Bv=5.1 Ibv=1u)

.Model SW1 VSwitch(Von=4 Voff=3 Ron=.1 Roff=1Meg)

.End
```

PWM Generator

```
* PWM Generator *
*****************

R1    1     0     1k
R2    2     0     1k

R10   11    12    5
L10   12    13    10m   IC=1.2

S10   0     11    1     2     SW1
S11   11    10    2     1     SW1
S12   0     13    2     1     SW1
S13   13    10    1     2     SW1

V1 10 0 DC 10
V2 1  0 Sin(0 10 50 333.34u 0)
V3 2  0 Pulse(-5 5 0 666.67u 666.66u 0.01u 1333.34u)

.Tran 20u 20m UIC
.Probe
.Model SW1 VSwitch (Von=.1 Voff=-.1 Ron=.001 Roff =100000)
.End
```

DC Component

```
* DC Component  (Switch closes on negative voltage peak) *
*********************************************************
R1    2     3     .5
L1    3     0     10m
S1    1     2     10 0 SW1
V1    1     0     SIN(0 1 50)
*
* Switch Circuit *
Vsw 10 0 Pulse(0 1 15m .2m 1m 1 2)
R5    10    0     10k
*
.MODEL SW1 VSWITCH(Ron=.001m Roff=1k Von=.5 Voff=.4)
.TRAN 5m .1 0 1m
.PROBE
.END
```

```
* DC Component  (Switch closes on zero voltage) *
************************************************
R1    2     3     .5
L1    3     0     10m
S1    1     2     10 0 SW1
V1    1     0     SIN(0 1 50)
*
* Switch Circuit *
Vsw 10 0 Pulse(0 1 20m .2m 1m 1 2)
R5    10    0     10k
*
.MODEL SW1 VSWITCH(Ron=.001m Roff=1k Von=.5 Voff=.4)
.TRAN 5m .1 0 1m
.PROBE
.END
```

APPENDIX E

COMPUTER PROGRAM LISTING AND FLOW CHARTS

```
NAM METROM
*************************************************
* ROM BASED PULSE WIDTH MODULATION SOFTWARE *
* FOR METAL BOX INVERTER                        *
* ***********************************************

* 6850 ACIA (Serial I/O) *

ACIAS1  EQU     $E080           Status Register
ACIAD1  EQU     $E081           Data Register

* 6821 PIA (Parallel I/O) *

PIA0A   EQU     $E100           Port A
PIA0B   EQU     $E102           Port B
PIA1A   EQU     $E180           Port A
PIA1B   EQU     $E182           Port B


* M6840 registers *
* --------------- *

* Note : Read and Write to same address
*        access different registers.

* Note : Control registeres of T1 and T3 at same address
*        Selected by CR2 bit 0
*        CR2 bit 0 = 0 -----> CR3 selected
*        CR2 bit 0 = 1 -----> CR1 selected

BASE  EQU $E200 Base address M6840

CRT13 EQU BASE    Write only

CR12   EQU BASE+1 Write only
STATUS EQU BASE+1 Read only (Status all timers)

T1MSB  EQU BASE+2 Write only (buffer)
T1CNT  EQU BASE+2 Read only

T1LAT  EQU BASE+3 Write only
LSBT1  EQU BASE+3 Read only (buffer)

T2MSB  EQU BASE+4 Write only (buffer)
T2CNT  EQU BASE+4 Read only

T2LAT  EQU BASE+5 Write only
LSBT2  EQU BASE+5 Read only (buffer)

T3MSB  EQU BASE+6 Write only (buffer)
T3CNT  EQU BASE+6 Read only

T3LAT  EQU BASE+7 Write only
LSBT3  EQU BASE+7 Rea only (buffer)


        ORG     $E800

START
* SETUP STACK *
        LDS     #STACK

* INITIALISATION *
* Initialise 6850 ACIA *
        LDA     #$03            Code to reset ACIA
        STA     ACIAS1          Reset ACIA0
        LDA     #%00010001      8 bits, no parity, 2 stop bits, /16
        STA     ACIAS1          Set mode

* Initialise 6821 PIA *
* PIA0 * (Primary PIA)
        LDX     #PIA0A          Digital Inputs
        LDA     #$00            0 --> Inputs
        JSR     PIASET
        LDX     #PIA0B          Digital Inputs
        LDA     #$00            0 --> Inputs
        JSR     PIASET
```

```
* PIA1 * (Secondary PIA)
        LDX     #PIA1A          Digital Inputs
        LDA     #$00            0 --> Inputs
        JSR     PIASET
        LDX     #PIA1B          Digital Inputs
        LDA     #%10001000
        JSR     PIASET
        CLR     PTABSW1
        CLR     PTABSW2
        CLR     PTABSW3
        CLR     PFREQ
        CLR     SFLAG
        JMP     MAINLUP

* TABLES *
*--------*
* TABLES OF PULSE WITH INTERVALS
* THE MOD INDEX VARIES FROM 0.01 TO 2.0 IN STEP OF 0.02
        OPT     NOL
TABBAS
*MOD.01 *TAB1   FCB 120,120,119,121,119,121,119,121,119,121,119,121,119,120,120,0
*MOD.03 *TAB2   FCB 120,121,118,122,117,123,116,124,116,123,117,122,118,121,120,0
*MOD.05 *TAB3   FCB 119,122,117,124,115,125,114,126,114,125,115,124,117,122,119,0
*MOD.07 *TAB4   FCB 119,123,116,126,113,128,112,128,112,128,113,126,116,123,119,0
*MOD.09 *TAB5   FCB 119,123,115,127,111,130,109,131,109,130,111,127,115,123,119,0
*MOD.11 *TAB6   FCB 119,124,113,129,109,132,107,133,107,132,109,129,113,124,119,0
*MOD.13 *TAB7   FCB 118,125,112,130,107,134,105,135,105,134,107,130,112,125,118,0
*MOD.15 *TAB8   FCB 118,126,111,132,106,136,102,138,102,136,106,132,111,126,118,0
*MOD.17 *TAB9   FCB 118,126,110,134,104,139,100,140,100,139,104,134,110,126,118,0
*MOD.19 *TAB10  FCB 118,127,109,135,102,141, 98,143, 98,141,102,135,109,127,118,0
*MOD.21 *TAB11  FCB 117,128,107,137,100,143, 95,145, 95,143,100,137,108,128,117,0
*MOD.23 *TAB12  FCB 117,129,106,138, 98,145, 93,147, 93,145, 98,138,106,129,117,0
*MOD.25 *TAB13  FCB 117,129,105,140, 96,147, 91,150, 91,147, 96,140,105,129,117,0
*MOD.27 *TAB14  FCB 117,130,104,142, 94,149, 88,152, 88,149, 94,142,104,130,117,0
*MOD.29 *TAB15  FCB 116,131,103,143, 92,152, 86,154, 86,152, 92,143,103,131,117,0
*MOD.31 *TAB16  FCB 116,132,102,145, 90,154, 84,157, 84,154, 90,145,102,132,116,0
*MOD.33 *TAB17  FCB 116,132,100,146, 88,156, 81,159, 81,156, 88,146,100,132,116,0
*MOD.35 *TAB18  FCB 116,133, 99,148, 86,158, 79,162, 79,158, 86,148, 99,133,116,0
*MOD.37 *TAB19  FCB 116,134, 98,150, 84,160, 77,164, 77,160, 84,150, 98,134,116,0
*MOD.39 *TAB20  FCB 115,135, 97,151, 82,162, 74,166, 74,162, 82,151, 97,135,115,0
*MOD.41 *TAB21  FCB 115,135, 96,153, 80,165, 72,169, 72,165, 80,153, 96,135,115,0
*MOD.43 *TAB22  FCB 115,136, 94,154, 78,167, 70,171, 70,167, 78,154, 94,136,115,0
*MOD.45 *TAB23  FCB 115,137, 93,156, 76,169, 67,173, 67,169, 76,156, 93,137,115,0
*MOD.47 *TAB24  FCB 114,138, 92,158, 75,171, 65,176, 65,171, 75,158, 92,138,114,0
*MOD.49 *TAB25  FCB 114,138, 91,159, 73,173, 63,178, 63,173, 73,159, 91,138,114,0
*MOD.51 *TAB26  FCB 114,139, 90,161, 71,175, 60,180, 60,175, 71,161, 90,139,114,0
*MOD.53 *TAB27  FCB 114,140, 88,162, 69,178, 58,183, 58,177, 69,162, 89,140,114,0
*MOD.55 *TAB28  FCB 114,141, 87,164, 67,180, 56,185, 56,180, 67,164, 87,141,114,0
*MOD.57 *TAB29  FCB 113,141, 86,166, 65,182, 53,187, 53,182, 65,166, 86,141,113,0
*MOD.59 *TAB30  FCB 113,142, 85,167, 63,184, 51,190, 51,184, 63,167, 85,142,113,0
*MOD.61 *TAB31  FCB 113,143, 84,169, 61,186, 48,192, 48,186, 61,169, 84,143,113,0
*MOD.63 *TAB32  FCB 113,144, 83,170, 59,188, 46,195, 46,188, 59,170, 83,144,113,0
*MOD.65 *TAB33  FCB 112,145, 81,172, 57,190, 44,197, 44,190, 57,172, 81,144,112,0
*MOD.67 *TAB34  FCB 112,145, 80,174, 55,193, 41,199, 41,193, 55,174, 80,145,112,0
*MOD.69 *TAB35  FCB 112,146, 79,175, 53,195, 39,202, 39,195, 53,175, 79,146,112,0
*MOD.71 *TAB36  FCB 112,147, 78,177, 51,197, 37,204, 37,197, 51,177, 78,147,112,0
*MOD.73 *TAB37  FCB 112,148, 77,178, 49,199, 34,206, 34,199, 49,178, 77,148,112,0
*MOD.75 *TAB38  FCB 111,148, 75,180, 47,201, 32,209, 32,201, 47,180, 76,148,111,0
*MOD.77 *TAB39  FCB 111,149, 74,182, 45,203, 30,211, 30,203, 45,182, 74,149,111,0
*MOD.79 *TAB40  FCB 111,150, 73,183, 43,205, 27,213, 27,205, 44,183, 73,150,111,0
*MOD.81 *TAB41  FCB 111,151, 72,185, 41,208, 25,215, 25,208, 42,185, 72,151,111,0
*MOD.83 *TAB42  FCB 110,152, 71,187, 40,210, 23,218, 23,210, 40,186, 71,151,111,0
*MOD.85 *TAB43  FCB 110,152, 69,188, 38,212, 20,220, 20,212, 38,188, 70,152,110,0
*MOD.87 *TAB44  FCB 110,153, 68,190, 36,214, 18,222, 18,214, 36,190, 68,153,110,0
*MOD.89 *TAB45  FCB 110,154, 67,191, 34,216, 16,225, 16,216, 34,191, 67,154,110,0
*MOD.91 *TAB46  FCB 110,155, 66,193, 32,218, 13,227, 13,218, 32,193, 66,155,110,0
*MOD.93 *TAB47  FCB 109,155, 65,195, 30,220, 11,229, 11,220, 30,195, 65,155,110,0
*MOD.95 *TAB48  FCB 109,156, 64,196, 28,223,  8,232,  9,222, 28,196, 64,156,109,0
*MOD.97 *TAB49  FCB 109,157, 62,198, 26,225,  6,234,  6,225, 26,198, 62,157,109,0
*MOD.99 *TAB50  FCB 109,158, 61,199, 24,227,  4,236,  4,227, 24,199, 61,158,109,0
*MOD1.01*TAB51  FCB 109,159, 60,201, 22,229,  1,239,  1,229, 22,201, 60,159,109,0
*MOD1.03*TAB52  FCB 108,159, 59,203, 20,250,  1,250,  1,199, 20,203, 59,159,109,0
*MOD1.05*TAB53  FCB 108,160, 58,204, 18,250,  1,250,  1,201, 18,204, 58,160,108,0
*MOD1.07*TAB54  FCB 108,161, 56,206, 16,250,  1,250,  1,203, 16,206, 57,161,108,0
*MOD1.09*TAB55  FCB 108,162, 55,208, 14,250,  1,250,  1,205, 14,207, 55,162,108,0
*MOD1.11*TAB56  FCB 108,163, 54,209, 12,250,  1,250,  1,207, 12,209, 54,163,108,0
*MOD1.13*TAB57  FCB 107,164, 53,211, 10,250,  1,250,  1,208, 10,211, 53,163,108,0
*MOD1.15*TAB58  FCB 107,164, 52,212,  8,250,  1,250,  1,210,  8,212, 52,164,107,0
*MOD1.17*TAB59  FCB 107,165, 50,214,  6,250,  1,250,  1,212,  7,214, 51,165,107,0
*MOD1.19*TAB60  FCB 107,166, 49,216,  4,250,  1,250,  1,214,  5,216, 49,166,107,0
*MOD1.21*TAB61  FCB 107,167, 48,217,  3,250,  1,250,  1,216,  3,217, 48,167,107,0
*MOD1.23*TAB62  FCB 106,168, 47,219,  1,250,  1,250,  1,217,  1,219, 47,167,107,0
*MOD1.25*TAB63  FCB 106,168, 46,250,  1,250,  1,250,  1,250,  1,155, 46,168,106,0
*MOD1.27*TAB64  FCB 106,169, 44,250,  1,250,  1,250,  1,250,  1,157, 45,169,106,0
*MOD1.29*TAB65  FCB 106,170, 43,250,  1,250,  1,250,  1,250,  1,158, 43,170,106,0
*MOD1.31*TAB66  FCB 106,171, 42,250,  1,250,  1,250,  1,250,  1,159, 42,171,106,0
*MOD1.33*TAB67  FCB 105,172, 41,250,  1,250,  1,250,  1,250,  1,160, 41,172,106,0
*MOD1.35*TAB68  FCB 105,173, 40,250,  1,250,  1,250,  1,250,  1,161, 40,172,105,0
*MOD1.37*TAB69  FCB 105,173, 38,250,  1,250,  1,250,  1,250,  1,162, 39,173,105,0
*MOD1.39*TAB70  FCB 105,174, 37,250,  1,250,  1,250,  1,250,  1,163, 37,174,105,0
*MOD1.41*TAB71  FCB 105,175, 36,250,  1,250,  1,250,  1,250,  1,165, 36,175,105,0
```

```
*MOD1.43*TAB72 FCB 104,176, 35,250,  1,250,  1,250,  1,250,  1,166, 35,176,105,0
*MOD1.45*TAB73 FCB 104,177, 34,250,  1,250,  1,250,  1,250,  1,167, 34,177,104,0
*MOD1.47*TAB74 FCB 104,178, 32,250,  1,250,  1,250,  1,250,  1,168, 33,177,104,0
*MOD1.49*TAB75 FCB 104,178, 31,250,  1,250,  1,250,  1,250,  1,169, 31,178,104,0
*MOD1.51*TAB76 FCB 104,179, 30,250,  1,250,  1,250,  1,250,  1,170, 30,179,104,0
*MOD1.53*TAB77 FCB 104,180, 29,250,  1,250,  1,250,  1,250,  1,171, 29,180,104,0
*MOD1.55*TAB78 FCB 103,181, 28,250,  1,250,  1,250,  1,250,  1,172, 28,181,104,0
*MOD1.57*TAB79 FCB 103,182, 26,250,  1,250,  1,250,  1,250,  1,173, 27,182,103,0
*MOD1.59*TAB80 FCB 103,183, 25,250,  1,250,  1,250,  1,250,  1,174, 25,182,103,0
*MOD1.61*TAB81 FCB 103,184, 24,250,  1,250,  1,250,  1,250,  1,176, 24,183,103,0
*MOD1.63*TAB82 FCB 103,184, 23,250,  1,250,  1,250,  1,250,  1,177, 23,184,103,0
*MOD1.65*TAB83 FCB 102,185, 21,250,  1,250,  1,250,  1,250,  1,178, 22,185,103,0
*MOD1.67*TAB84 FCB 102,186, 20,250,  1,250,  1,250,  1,250,  1,179, 20,186,102,0
*MOD1.69*TAB85 FCB 102,187, 19,250,  1,250,  1,250,  1,250,  1,180, 19,187,102,0
*MOD1.71*TAB86 FCB 102,188, 18,250,  1,250,  1,250,  1,250,  1,181, 18,188,102,0
*MOD1.73*TAB87 FCB 102,189, 17,250,  1,250,  1,250,  1,250,  1,182, 17,188,102,0
*MOD1.75*TAB88 FCB 101,190, 15,250,  1,250,  1,250,  1,250,  1,183, 16,189,102,0
*MOD1.77*TAB89 FCB 101,190, 14,250,  1,250,  1,250,  1,250,  1,184, 14,190,102,0
*MOD1.79*TAB90 FCB 101,191, 13,250,  1,250,  1,250,  1,250,  1,185, 13,191,101,0
*MOD1.81*TAB91 FCB 101,192, 12,250,  1,250,  1,250,  1,250,  1,186, 12,192,101,0
*MOD1.83*TAB92 FCB 101,193, 10,250,  1,250,  1,250,  1,250,  1,187, 11,193,101,0
*MOD1.85*TAB93 FCB 101,194,  9,250,  1,250,  1,250,  1,250,  1,188,  9,194,101,0
*MOD1.87*TAB94 FCB 100,195,  8,250,  1,250,  1,250,  1,250,  1,189,  8,195,101,0
*MOD1.89*TAB95 FCB 100,196,  7,250,  1,250,  1,250,  1,250,  1,190,  7,196,101,0
*MOD1.91*TAB96 FCB 100,197,  6,250,  1,250,  1,250,  1,250,  1,191,  6,196,100,0
*MOD1.93*TAB97 FCB 100,198,  4,250,  1,250,  1,250,  1,250,  1,192,  5,197,100,0
*MOD1.95*TAB98 FCB 100,198,  3,250,  1,250,  1,250,  1,250,  1,193,  3,198,100,0
*MOD1.97*TAB99 FCB 100,199,  2,250,  1,250,  1,250,  1,250,  1,194,  2,199,100,0
*MOD1.99*TAB100 FCB 99,201,  1,250,  1,250,  1,250,  1,250,  1,195,  1,200,100,0
         OPT    LIS

* SUBROUTINES *
*
* CONVERT PACKED BCD IN A TO BINARY IN B
*
BCD2BIN
         TFR    A,B
         ANDB   #$0F            MASK HIGH NIBBLE
         STB    TEMP            STORE IT
         LSRA
         LSRA
         LSRA
         LSRA
         LDB    #10
         MUL
         ADDB   TEMP            ADD TO A
         RTS

PIASET
         CLR    1,X             Select DDR
         STA    0,X             Specify Ins (0) or OUTs (1)
         LDB    #4              Select Data Reg
         STB    1,X
         RTS

OUTCH    PSHS    A              Character to stack
OUTLB    LDA     ACIAS1         Poll ACIA status reg
         ANDA    #$02           Test bit
         BEQ     OUTLB          Not ready - wait
         PULS    A              Retrive from stack
         STA     ACIAD1         Write to data reg
         RTS                    Return to caller
*
* CONVERT 16 BIT VALUE IN D TO ASCII DECIMAL STRING
* X - POINTER TO BUFFER.
* D - CONTAINS VALUE.
*
BINASCD
         STX    TEMP1           SAVE OUTPUT BUFFER POINTER
         INX
         INX
         INX
         INX
         STD    DVDN            STORE VALUE . OR DIVIDE
         LDA    #10             GET DIVISOR
         STA    DVSR            STORE AS DIVISOR
DIVLUP   STX    TEMPC           SAVE FOR DIVIDE
         JSR    UNSFD           DIVIDE BY 10
         LDX    TEMPC           RESTORE X
         LDA    RMNDR           GET  REMAINDER
         ADDA   #$30            ADD ASCII BIAS
         STA    0,X             STORE CHARACTER
         DEX                    POINT TO NEXT
         CPX    TEMP1           TEST FOR DONE
         BGE    DIVLUP          CONTINUE IF NOT DONE
         LDX    TEMP1           RETRIEVE INDEX
         INX
         INX
         INX
         INX
         INX                    POINT TO LAST+1
         RTS                    RETURN TO CALLER
```

```
;
; UNSIGNED SINGLE PRECISION DIVIDE
;
UNSPD   CLR     RMNDR           CLEAR REMAINDER
        LDX     #17             SETUP COUNT
        BRA     DSTART          START
UDIVLUP LDA     RMNDR           GET CURRENT
        SUBA    DVSR            SUBTRACT
        BPL     NREST           GO IF NO RESTORE
DSTART  CLC                     CLEAR CARRY
        BRA     MERGQ           GO TO SET Q
NREST   STA     RMNDR           NEW PARTIAL Q
        SEC                     SET C FOR Q=1
MERGQ   ROL     DVDN+1          MERGE Q
        ROL     DVDN
        DEX                     DECREMENT COUNT
        BEQ     DRTN            RETURN IF DONE
        ROL     RMNDR           SHIFT BIT
        BRA     UDIVLUP         CONTINUE
DRTN    RTS                     RETURN TO CALLER

                        *************
                        * MAIN LOOP *
                        *************

MAINLUP


        LDA     #$FF            SET SWITCH FLAG
        STA     SWFLAG
* READ CLOCK FREQENCY THUMBWHEEL SWITCH *
    LDA         PIA1B           Get switch value
        COMA                    Invert bits
        ANDA    #$07            MASK IT
        CMPA    #$01            IS IT LESS THAN 1?
        BHS     FSTOR1          No - just store it
        LDA     #$01            YES - SET IT TO 1
FSTOR1
        INCA                    ADD ONE
        STA     FREQ            Store it
        CMPA    PFREQ           SAME AS PREVIOUS
        BEQ     TABTST          YES - TEST OTHER SWITCHES
        STA     PFREQ           STORE AS PREVIOUS
        CLR     SWFLAG          INDICATE CHANGE
TABTST

* READ TABLE THUMB WHEEL SWITCHES & STORE TABLE POINTERS *
         LDA    PIA0A           Read switch 1
         COMA                   Invert bits
         JSR    BCD2BIN         Convert to binary
         STB    TABSW1          Store it
         LDA    PIA0B           Read switch 2
         COMA                   Invert bits
         JSR    BCD2BIN         Convert to binary
         STB    TABSW2          Store it
         LDA    PIA1A           Read switch 3
         COMA                   Invert bits
         JSR    BCD2BIN         Convert to binary
         STB    TABSW3          Store it

        LDA     TABSW1          GET SWITCH 1
        CMPA    PTABSW1         SAME AS PREVIOUS
        BEQ     SWTST2          YES - CHECK NEXT
        STA     PTABSW1         SAVE AS PREVIOUS
        CLR     SWFLAG          INDICATE CHANGE
SWTST2
        LDA     TABSW2          GET SWITCH 2
        CMPA    PTABSW2         SAME AS PREVIOUS
        BEQ     SWTST3          YES - TEST NEXT
        STA     PTABSW2         STORE AS PREVIOUS
        CLR     SWFLAG          INDICATE CHANGE
SWTST3
        LDA     TABSW3          GET SWITCH 3
        CMPA    PTABSW3         SAME AS PREVIOUS
        BEQ     TESTFLG         YES - CHECK FOR ANY CAHNGES
        STA     PTABSW3         SAVE AS PREVIOUS
        CLR     SWFLAG          INDICATE CHANGE
TESTFLG
        TST     SWFLAG          ANY CHANGES?
        LBNE    CONTIN

* SET TABLE POINTER TO TABLE SELECTED BY SWITCH 1 *
        LDB     TABSW1          Get switch value
        LDA     #$10            Get multiplier - table entry length
        MUL                     Form offset
        ADDD    #TABBAS         Add table base
        TFR     D,X             Get result into X
```

```
* COPY TO TEMPTAB1 *
        LDY     #TEMPTAB1
TAB1LUP
        LDA     0,X+ get value
        CMPA    #0              End of table?
        BNE     MULT
        LDD     #0
        STD     0,Y             Store table terminator
        BRA     SETTAB2
MULT
        LDB     FREQ            Get frequency
        MUL
        STD     0,Y++           Store value
        BRA     TAB1LUP         Loop until done

* SET TABLE POINTER TO TABLE SELECTED BY SWITCH 2 *
SETTAB2
        LDB     TABSW2          Get switch value
        LDA     #$10            Get multiplier - table entry length
        MUL                     Form offset
        ADDD    #TABBAS         Add table base
        TFR     D,X             Get result into X

* COPY TO TEMPTAB2 *
        LDY     #TEMPTAB2
TAB2LUP
        LDA     0,X+ get value
        CMPA    #0              End of table?
        BNE     MULT1
        LDD     #0
        STD     0,Y             Store table terminator
        BRA     SETTAB3
MULT1
        LDB     FREQ            Get frequency
        MUL
        STD     0,Y++           Store value
        BRA     TAB2LUP         Loop until done

* SET TABLE POINTER TO TABLE SELECTED BY SWITCH 3 *
SETTAB3
        LDB     TABSW3          Get switch value
        LDA     #$10            Get multiplier - table entry length
        MUL                     Form offset
        ADDD    #TABBAS         Add table base
        TFR     D,X             Get result into X

* COPY TO TEMPTAB3 *
        LDY     #TEMPTAB3
TAB3LUP
        LDA     0,X+ get value
        CMPA    #0              End of table?
        BNE     MULT2
        LDD     #0
        STD     0,Y             Store table terminator
        BRA     OUTREQ
MULT2
        LDB     FREQ            Get frequency
        MUL
        STD     0,Y++           Store value
        BRA     TAB3LUP         Loop until done

* CHECK FOR OUTPUT REQUEST *
OUTREQ
        LDA     ACIAS1          Check for character
        ANDA    #$01
        LBNE    CONTIN          No character available
        LDA     ACIAD1          Get the character
        ANDA    #$7F            Strip parity
        CMPB    #$23            Is it a '#'?
        BNE     TRYNXT          No - try next value
        LDD     #0
        STD     CANCNT          Reset can count
        BRA     CONTIN
TRYNXT
        CMPB    #$40            Is it an '@'?
        LBNE    CONTIN

* OUTPUT DATA ON SERIAL PORT *
* SWITCH 1 IN ASCII FORMAT *
        LDA     PIA0A           Read switch 1 (tens digit)
        LSRA                    Shift it right
        LSRA
        LSRA
        LSRA
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it
        LDA     PIA0A           Read switch 1 (units digit)
        ANDA    #$0F            Mask it
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it
```

```
* SWITCH 2 IN ASCII FORMAT *
        LDA     PIA0B           Read switch 1 (tens digit)
        LSRA                    Shift it right
        LSRA
        LSRA
        LSRA
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it
        LDA     PIA0B           Read switch 1 (units digit)
        ANDA    #$0F            Mask it
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it

* SWITCH 3 IN ASCII FORMAT *
        LDA     PIA1A           Read switch 1 (tens digit)
        LSRA                    Shift it right
        LSRA
        LSRA
        LSRA
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it
        LDA     PIA1A           Read switch 1 (units digit)
        ANDA    #$0F            Mask it
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it

* OUTPUT FREQUENCY SWITCH IN ASCII FORMAT
        LDA     PIA1B           Read switch 1 (tens digit)
        ANDA    #$0F            Mask it
        ADDA    #$30            Add ascii bias
        JSR     OUTCH           Output it
        LDA     ','             Get comma
        JSR     OUTCH           Output it

* OUTPUT CAN COUNT IN ASCII FORMAT *
        LDX     #ACANCNT        POINT TO STRING
        LDD     CANCNT          GET VALUE
        JSR     BINASCD         CONVERT BINARY TO ASCII DECIMAL
        LDA     #0              GET TERMINATER
        STA     STERM           STORE STRING TERMINATER
        LDX     #ACANCNT        POINT TO STRING
OUTSTR  LDA     0,X             GET CHARACTER
        CMPA    #0              END OF STRING?
        BEQ     OUTCR           YES
        JSR     OUTCH           OUTPUT CHARACTER
        INX                     BUMP POINTER
        JMP     OUTSTR          OUTPUT NEXT CHARACTER

* OUTPUT CARRIAGE RETURN *
OUTCR
        LDA     #$0D            Get carriage return
        JSR     OUTCH           Output it

CONTIN
        CLR     FFLOP           CLEAR TIMER FLIP-FLOP
        LDA     #2
        STA     ITABOFF
        LDA     #$FF
        STA     SWITCH          INDICATE INTERRUPTS NOT RUNNING
TSTINP
        LDA     PIA1B           GET INPUTS
        ANDA    #$70            CLEAR HIGH BIT
        LSRA                    SHIFT TO LOWER BITS 0,1,2.
        LSRA
        LSRA
        LSRA
*=======================================================*

        CMPA    #$07            ARE THEY ALL SET TO HIGH?
        BEQ     CLEAR           CLEAR THE OUPUTS & TIMERS.

        CMPA    #$00            ARE THEY ALL SET TO LOW?
        BEQ     CLEAR           CLEAR THE OUPUTS & TIMERS.

        CMPA    #$01            IF YES, WE ARE AT THE START AND WE
        BEQ     SETT1           WILL SET THE POINTER TO TABLE 1.

        CMPA    #$02            IF YES, WE ARE IN THE MIDDLE AND WE
        BEQ     SETT2           WILL SET POINTER TO TABLE 2.

        CMPA    #$04            IF YES WE ARE AT THE END AND WE
        BEQ     SETT3           WILL SET POINTER TO TABLE 3.

        BRA     TSTINP          LEAVE IN PREVIOUS STATE.

*=======================================================*
```

```
CLEAR
* DISABLE TIMERS & CLEAR OUTPUTS *
* Clear CRT1 (shared CRT3) bit 0 *

        LDA     #$00            Sets both PWM outputs to zero
        STA     PIA1B
        LDA     #%00000001      BIT 0 = 1 selects CRT1
        STA     CRT2            when stored in CRT2
        STA     CRT13           Bit 0 = 1 disables all

* BUMP CAN COUNTER *
        INC     CANCNT
        SEI                     Disable interrupts
        JMP     MAINLUP         Process next can

SETT1
* SET POINTERS TO TABLE 1 *
        LDX     #TEMPTAB1
        STX     ITABBAS

        BRA     ONOFF

SETT2
* SET POINTERS TO TABLE FOR PHASE 2 *
        LDX     #TEMPTAB2
        STX     ITABBAS

        BRA     ONOFF

SETT3
* SET POINTERS TO TABLE FOR PHASE 3 *
        LDX     #TEMPTAB3
        STX     ITABBAS


ONOFF
        TST     SWITCH
        BEQ     TSTINP          SYSTEM IS RUNNING
        CLR     SWITCH          START SYSTEM RUNNING
* 6840 Initialization *
* ------------------- *

* Timer 1 - One-shot mode - Clock ex E
* Timer 2 - One-shot mode - Clock ex E
* Timer 3 - Not used

* Disable all timers while presetting *
* i.e. Clear CRT1 (shared CRT3) bit 0 *

        LDA     #%00000001      BIT 0 = 1 selects CRT1
        STA     CRT2            when stored in CRT2
        STA     CRT13           Bit 0 = 1 disables all

* Load Timer Latches *

        LDX     ITABBAS         Get table base
        LDY     0,X             First value from slow start table
        STY     T1MSB           Loads 16 bit T1 latch
        INC     ITABOFF         BUMP POINTER
        INC     ITABOFF         BUMP POINTER

* Set Timer modes *

* Select CR timer 3 i.e Clear Bit 0 in CRT2   *
* (Note : CR1 and CR3 share an address        *

* LDA #%00000000
        CLR     A
        STA     CRT2            CRT3 selected in shared address

* Timer 3 first - Not used *

* B0 = 0 Enable prescaler (div 8)
* B1 = 0 Enable external clock (150 baud)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 0 } IRQ flag disabled
* B7 = 1 } Timer output enabled

        LDA     #%10100000      Functions above
        STA     CRT13           CR3 selected above

* Timer 2 second - (Pulse output)   *
```

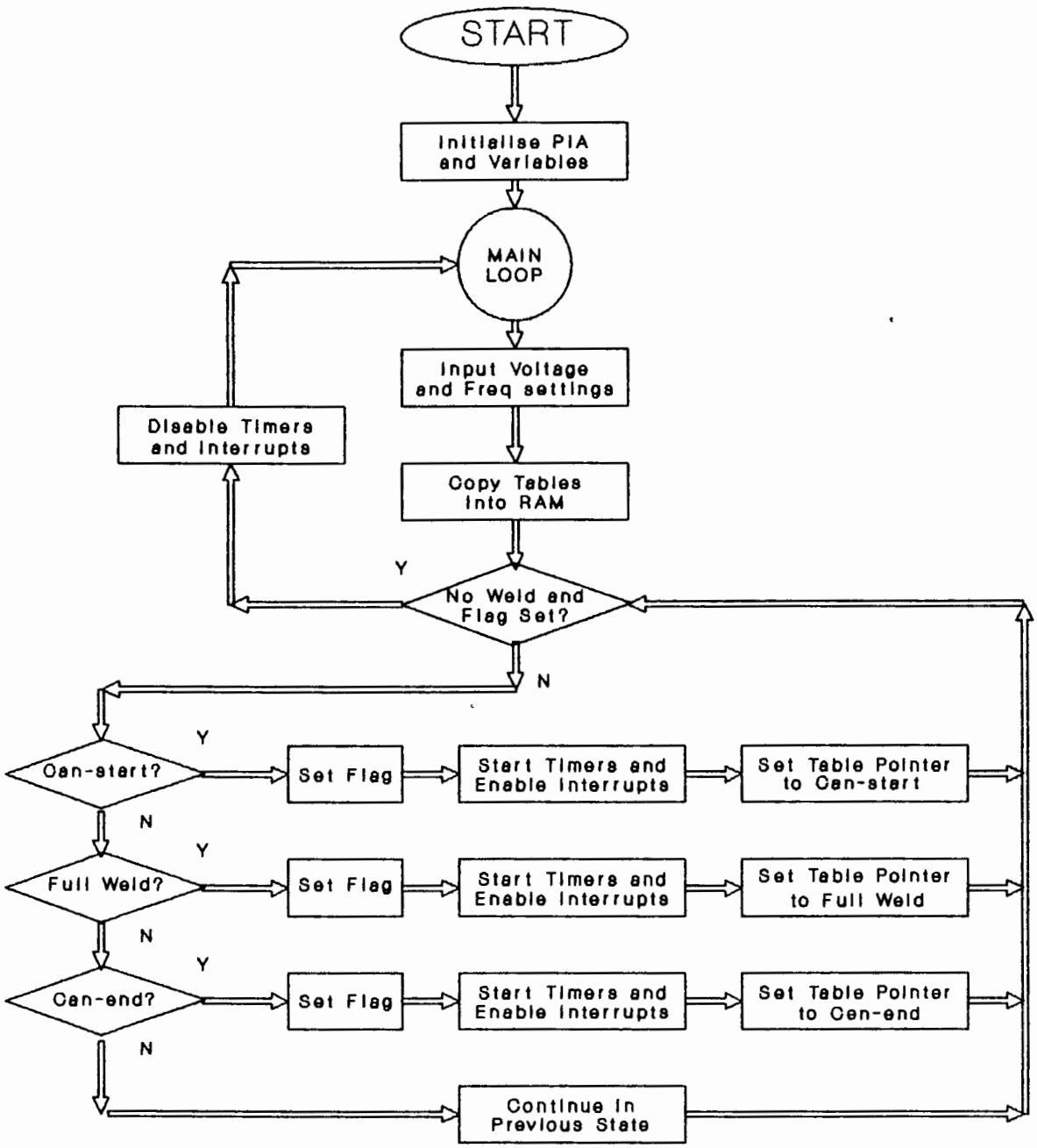
```
* B0 = 1 Allows CRT1 to be selected
* B1 = 1 Enable internal clock (ex E)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 )
* B4 = 0 ) One shot mode
* B5 = 1 )
* B6 = 0 ) IRQ flag disabled
* B7 = 0 Timer output disabled

          LDA     #%00100011      Functions above
          STA     CRT2

* Timer 1 third - (Pulse output) *

* B0 = 0 Enable all timers
* B1 = 1 Enable internal clock (ex E)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 )
* B4 = 0 ) One shot mode
* B5 = 1 )
* B6 = 1 IRQ flag enabled
* B7 = 1 Timer output enabled

         LDA      #%11100010      Functions above
         STA      CRT13           selected above

* Timer now initialised *

         CLI                      Clear mask at start

         JMP      TSTINP

************************************
* I N T E R R U P T  H A N D L E R *
************************************
INTRTN

* PIT INTERRUPT HANDLER *
*-----------------------*
* ITABBAS - HAS CURRENT TABLE BASE *
* ITABOFF - HAS CURRENT OFFSET *


* SETUP POINTERS *

         LDX      ITABBAS         Get table base
         LDB      ITABOFF         Get table offset
         LDY      B,X             Get value

* TEST FOR END OF TABLE *
         CMPY     #0
         BNE      SETVAL

* END OF TABLE RESET TO BEGINNING *
         LDA      #0
         STA      ITABOFF         Reset offset value
         BRA      INTRTN          Get next value

SETVAL

* WHICH TIMER CAUSED INTERRUPT? *
         TST      FFLOP
         BNE      TIM2INT         Timer 2 caused interrupt

* TIMER 1 CAUSED INTERRUPT *
TIM1INT

* SET OUTPUT HIGH *
         TST      SFLAG
         BNE      NOLO
         LDA      #$00
         STA      PIA1B
         STA      PIA1B
         STA      PIA1B
         STA      PIA1B

         STA      PIA1B
NOLO
         CLR      SFLAG
         LDA      #$80
         STA      PIA1B

* Disable all timers while presetting *
* i.e. Clear CRT1 (shared CRT3) bit 0 *

         LDA #%00000001  BIT 0 = 1 selects CRT1
         STA      CRT2            when stored in CRT2
         STA      CRT13           Bit 0 = 1 disables all

* Load Timer Latches *
         STY      T2MSB           Loads 16 bit T2 latch
```

```
* Set Timer modes *

* Select CR timer 3 i.e Clear Bit 0 in CRT2   *
* (Note : CR1 and CR3 share an address        *

* LDA #%00000000
        CLR     A
        STA     CRT2            CRT3 selected in shared address

* Timer 3 first - (Not used) *

* B0 = 0 Enable prescaler (div 8)
* B1 = 0 Enable external clock (150 baud)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 0 } IRQ flag disabled
* B7 = 1 } Timer output enabled

         LDA    #%10100000      Functions above
         STA    CRT13           CR3 selected above

* Timer 2 second - (Pulse output)   *
* CR2 has unique address            *

* B0 = 1 Allows CRT1 to be selected
* B1 = 1 Enable internal clock (ex E)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 1 } IRQ flag enabled
* B7 = 1 Timer output enabled

        LDA     #%11100011      Functions above
        STA     CRT2

* Timer 1 third - (Pulse output) *

* B0 = 0 Enable all timers
* B1 = 1 Enable internal clock (ex E)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 0 IRQ flag disabled
* B7 = 0 Timer output disabled

        LDA     #%00100010      Functions above
        STA     CRT13           selected above

        LDA     #$FF
        STA     FFLOP           Toggle flip-flop

* Timer now initialised *
         INC    ITABOFF         Bump pointer
         INC    ITABOFF         Bump pointer

* Check next value *
        LDX     ITABBAS         Get table base
        LDB     ITABOFF         Get table offset
        LDY     B,X             Get value
        CMPY    #0              End of table?
        BEQ     INTEX1          Yes - just exit
        CMPY    #$0A            Is value < 10?
        BHS     INTEX1          No - just exit
        INC     ITABOFF         Skip
        INC     ITABOFF         this value
        LDA     #$FF
        STA     SFLAG
        CLR     FFLOP           Use same timer
INTEX1
         RTI

* TIMER 2 CAUSED INTERRUPT *
TIM2INT
* SET OUTPUT LOW *
        TST     SFLAG
        BNE     NOLO1
        LDA     #$00
        STA     PIA1B
        STA     PIA1B
        STA     PIA1B
        STA     PIA1B
        STA     PIA1B
        STA     PIA1B
NOLO1
        CLR     SFLAG
        LDA     #%00001000
        STA     PIA1B
```

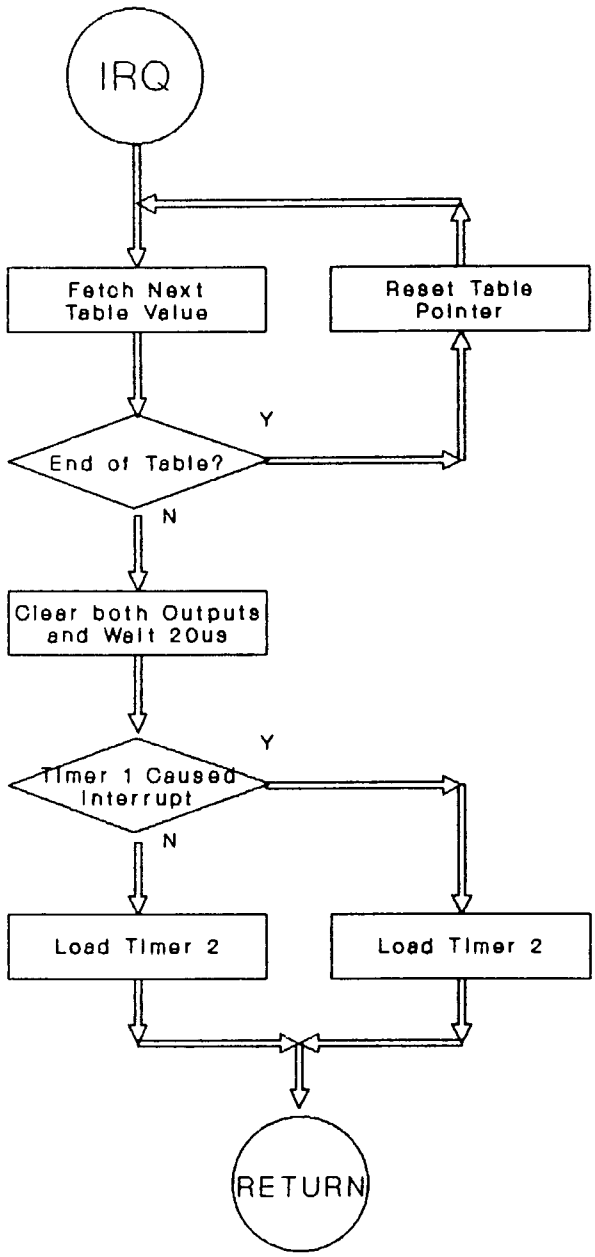
```
* Timer 1 - Pulse output - Clock ex E
* Timer 2 - Pulse output - Clock ex E
* Timer 3 - Not used

* Disable all timers while presetting *
* i.e. Clear CRT1 (shared CRT3) bit 0 *

        LDA     #%00000001      BIT 0 = 1 selects CRT1
        STA     CRT2            when stored in CRT2
        STA     CRT13           Bit 0 = 1 disables all

* Load Timer Latches *

        STY     T1MSB           Loads 16 bit T2 latch

* Set Timer modes *

* Select CR timer 3 i.e Clear Bit 0 in CRT2   *
* (Note : CR1 and CR3 share an address        *

* LDA #%00000000
        CLR     A
        STA     CRT2            CRT3 selected in shared address

* Timer 3 first - (Not used) *

* B0 = 0 Enable prescaler (div 8)
* B1 = 0 Enable external clock (150 baud)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 0 } IRQ flag disabled
* B7 = 1 } Timer output enabled

        LDA     #%10100000      Functions above
        STA     CRT13           CR3 selected above

* Timer 2 second - (Pulse output) *
* CR2 has unique address          *

* B0 = 1 Allows CRT1 to be selected
* B1 = 1 Enable internal clock (ex E)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 0 } IRQ flag disabled
* B7 = 0 Timer output disabled

        LDA     #%00100011      Functions above
        STA     CRT2

* Timer 1 third - (Pulse output) *

* B0 = 0 Enable all timers
* B1 = 1 Enable internal clock (ex E)
* B2 = 0 Normal 16 bit count mode
* B3 = 0 }
* B4 = 0 } One shot mode
* B5 = 1 }
* B6 = 1 IRQ flag enabled
* B7 = 1 Timer output enabled

        LDA     #%11100010      Functions above
        STA     CRT13           selected above

        CLR     FFLOP           Toggle flip-flop

* Timer now initialised *
        INC     ITABOFF         Bump pointer
        INC     ITABOFF         Bump pointer

* Check next value *
        LDX     ITABBAS         Get table base
        LDB     ITABOFF         Get table offset
        LDY     B,X             Get value
        CMPY    #0              End of table?
        BEQ     INTEX2          Yes - just exit
        CMPY    #$0A            Is value < 10?
        BHS     INTEX2          No - just exit
        INC     ITABOFF         Skip
        INC     ITABOFF         this value
        LDA     #$FF
        STA     FFLOP           Toggle flip-flop
        STA     SFLAG
INTEX2
        RTI
*********************************
* E N D  O F  I N T E R R U P T *
*       H A N D L E R           *
*********************************
```

```
* High memory vectors *

ORG     $FFF6

FIRQ    FDB     INTRTN
IRQ     FDB     INTRTN
SWIV    FDB     START
NMIV    FDB     INTRTN
BEGIN   FDB     START

ORG     $1FFF
STACK   RMB 1


ORG     $0000

* DATA AREAS *
*-----------*
SFLAG     RMB     1
FFLOP     RMB     1               Current timer flip-flop
SWITCH    RMB     1               Running/idle switch
ITABOFF   RMB     1               Current table offset
ITABBAS   RMB     2               Current table base
TABSW1    RMB     1
TABSW2    RMB     1
TABSW3    RMB     1
PTABSW1   RMB     1
PTABSW2   RMB     1
PTABSW3   RMB     1
FFREQ     RMB     1
SWFLAG    RMB     1
CANCNT    RMB     2
TEMPTAB1  RMB     32
TEMPTAB2  RMB     32
TEMPTAB3  RMB     32
FREQ      RMB     1               Frequency divisor
TEMP      RMB     1
TEMP1     RMB     2
TEMPC     RMB     2
DVDN      RMB     2
DVSR      RMB     1
RMNDR     RMB     1
ACANCNT   RMB     5
STERM     RMB     1
*=========================================================*
NEWVAL    RMB     1
*=========================================================*
          END
```

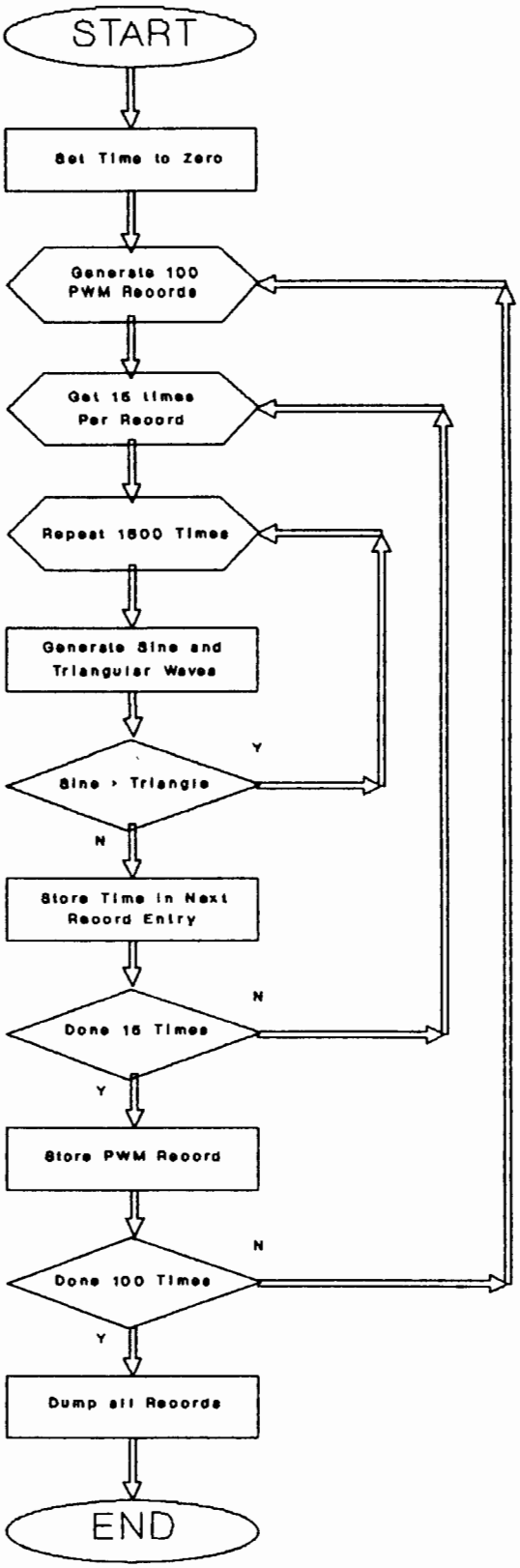
Program flow chart



Interrupt Handler Flow Chart



PWM Table Generating Program



APPENDIX F

COMPUTER GENERATED PULSE WIDTH MODULATION

The Pulse Width Modulation (PWM) is generated by the computer, from pre-calculated tables that contain the values of time for each pulse width. There are a maximum of 15 pulses and 15 pulse-breaks per fundamental cycle. There is therefore 30 units of time per cycle to be calculated. The positive cycle of a PWM signal is the same as the inverse of the negative cycle, i.e every pulse in the positive cycle is a pulse-break in the negative cycle, 180^{o} away. Only 15 values thus need to be stored, as the waveform is repeated. The pulses and pulse-breaks are inverted after each time the table is read. An example of a table and the resulting PWM is given in figure 1.

Table 52:

108,159,59,203,20,250,1,250,1,199,20,203,59,159,109,0

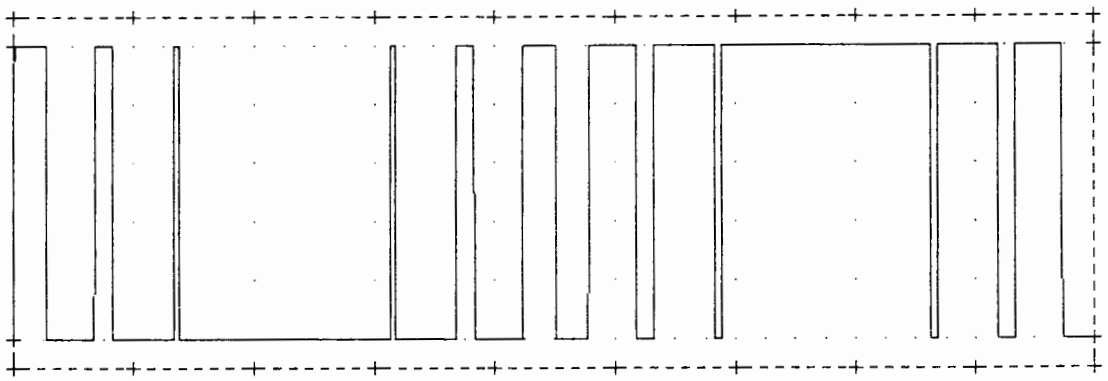


Figure 1 Table 52 and the resulting PWM.

The 0 at the end of the table indicates that the table has come to an end and that the table must be continued from the start again. The value 1 in the middle of the table is omitted when the table is read. It is used to signal that the PWM should remain in its previous state, either high or low. Figure 1 shows this. The program automatically assumes that if a number represents the width of a positive pulse, then the following number represents a pulse-break. There is an odd amount of numbers in the table, thus each time a table is read, the positive and negative pulses are automatically inverted.

A total of 100 tables were pre-calculated and stored in the EPROM. These 100 tables represent 100 different PWM waveforms, that result in 100 different output voltages. Each voltage dial (e.g. can start etc), selects a table number, from 0 to 99. The three voltage dials select three different table numbers. The current tables being used are read from the EPROM and are stored in the RAM.

The pre-calculated tables

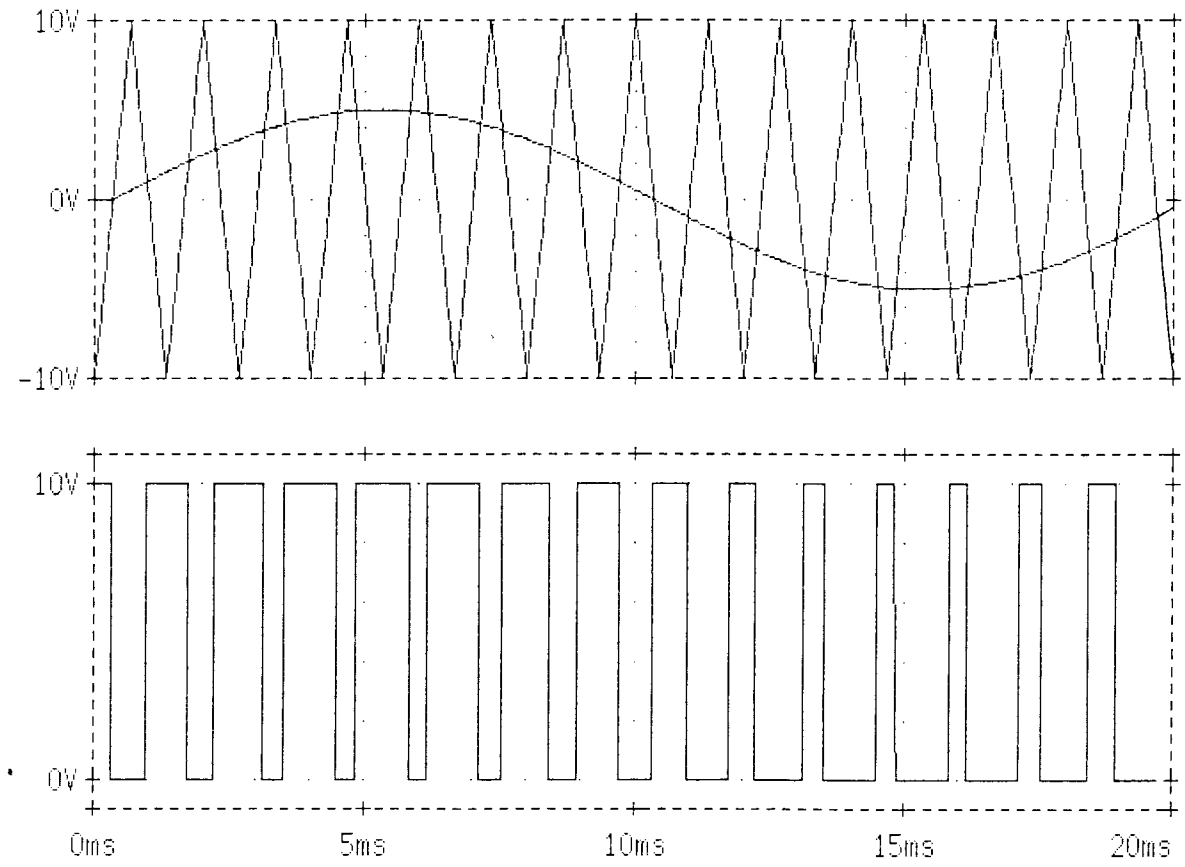
The tables were pre-calculated on a computer. A program was written to simulate a pulse width modulation generator and to give 100 table outputs over modulation range. A flow chart of a program that would achieve this is shown at the end of this appendix.

The pulse width modulation is generated by comparing a sine wave with a triangular wave. The frequency of the triangular wave is 15 times that of the sine wave. Each pulse width can vary from 0 to 255 (or 28-1). To achieve a the best accuracy, the average number of units per pulse was chosen to be 120. This means that for every table there are 1800 (15 x 120) units of time. The square and triangular waves are thus compared in steps of 1/1800 units per half wave. The simulation needs to run only for half a cycle for the reasons described earlier.

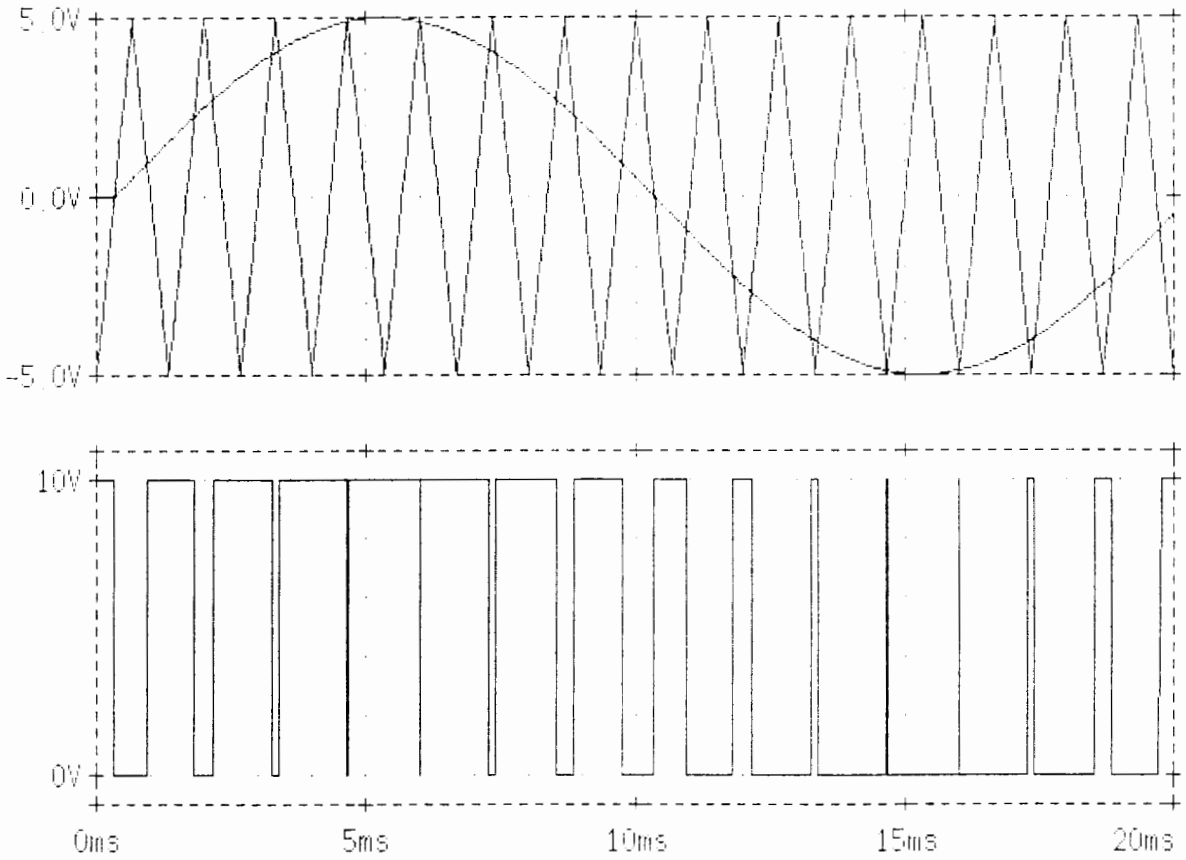
The different PWM waveforms are created by modulating the amplitude of the sine wave with a constant triangular wave. The modulation index is defined as [33]:

$$\text{Modulation index} = \frac{\text{Peak amplitude of sine wave}}{\text{Peak amplitude of triangular wave}}$$

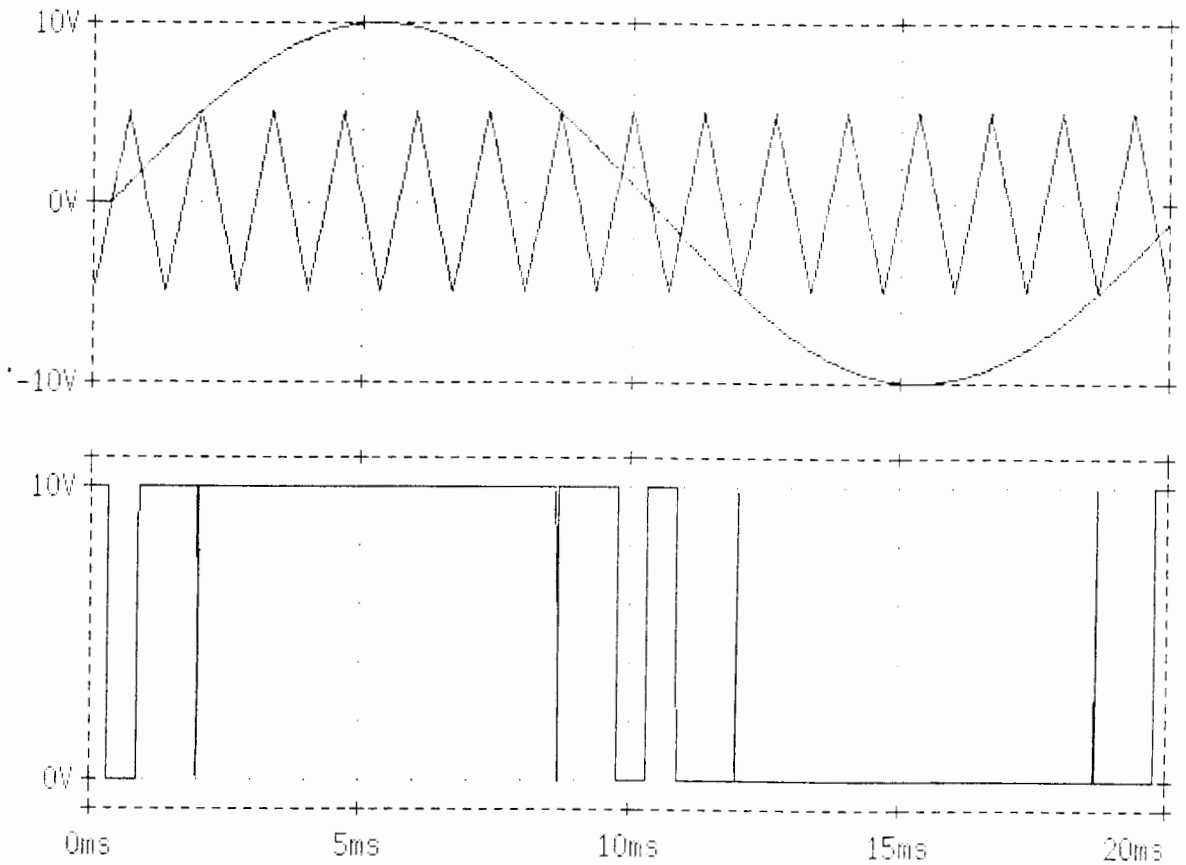
The modulation index was chosen to run form 0.01 to 1.99 in steps of 0.02, thus creating 100 tables. Examples of three significant modulations indices are shown in the following three graphs.



Modulation factor of 0.25



Modulation factor of 1

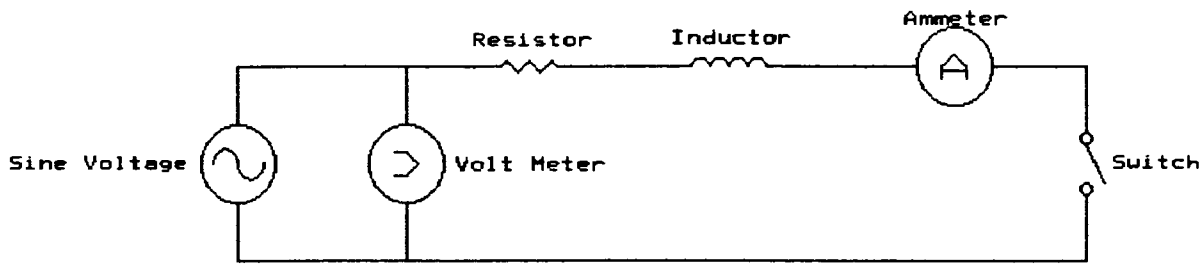


Modulation factor of 2

APPENDIX G

THE DC COMPONENT

The response of an inductive circuit to sudden change in load is composed of unidirectional (DC) current, and a steady state sinusoidal current. Examples of where this DC current occurs is in electrical machines, transformers and transmission lines. The DC current arises because the flux linkage of a circuit must not change instantaneously. i.e. the current in an inductance must not change instantly.

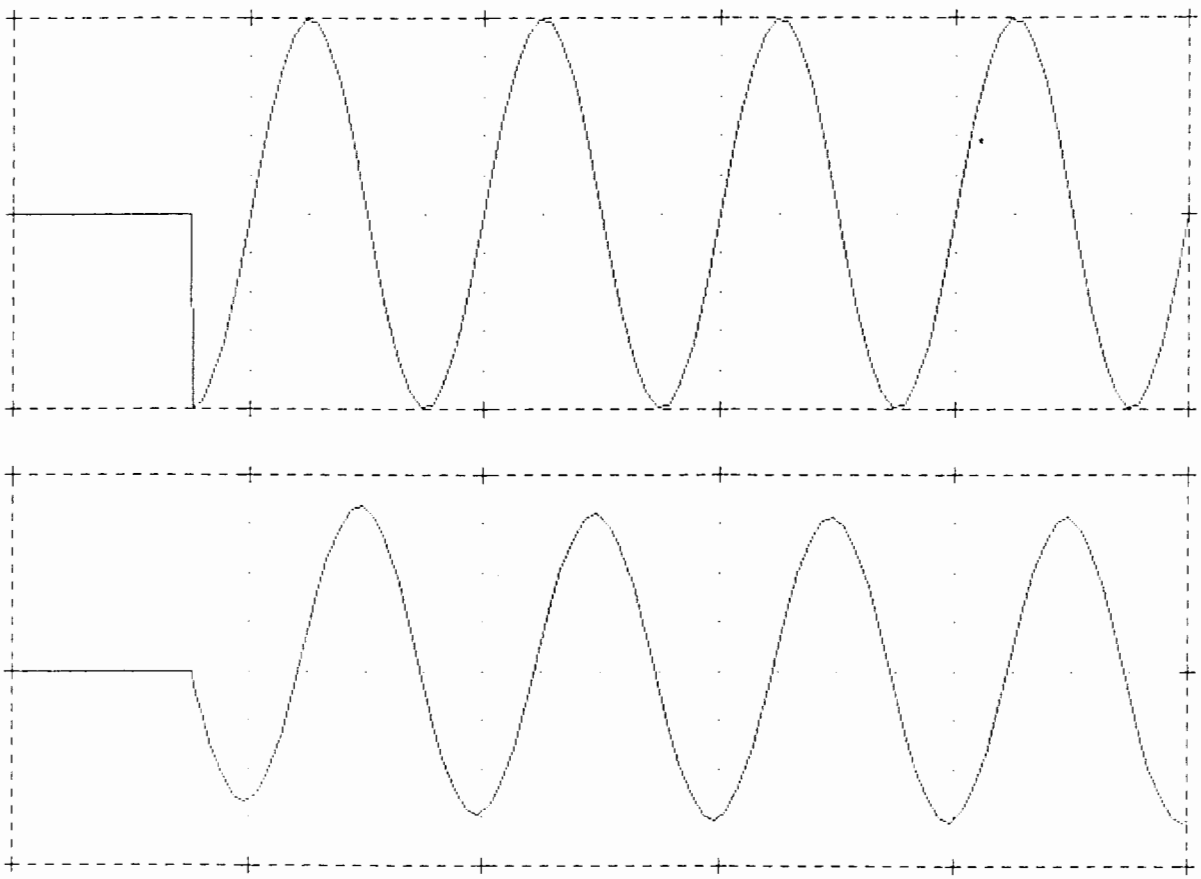


Circuit used to show the DC offset effect

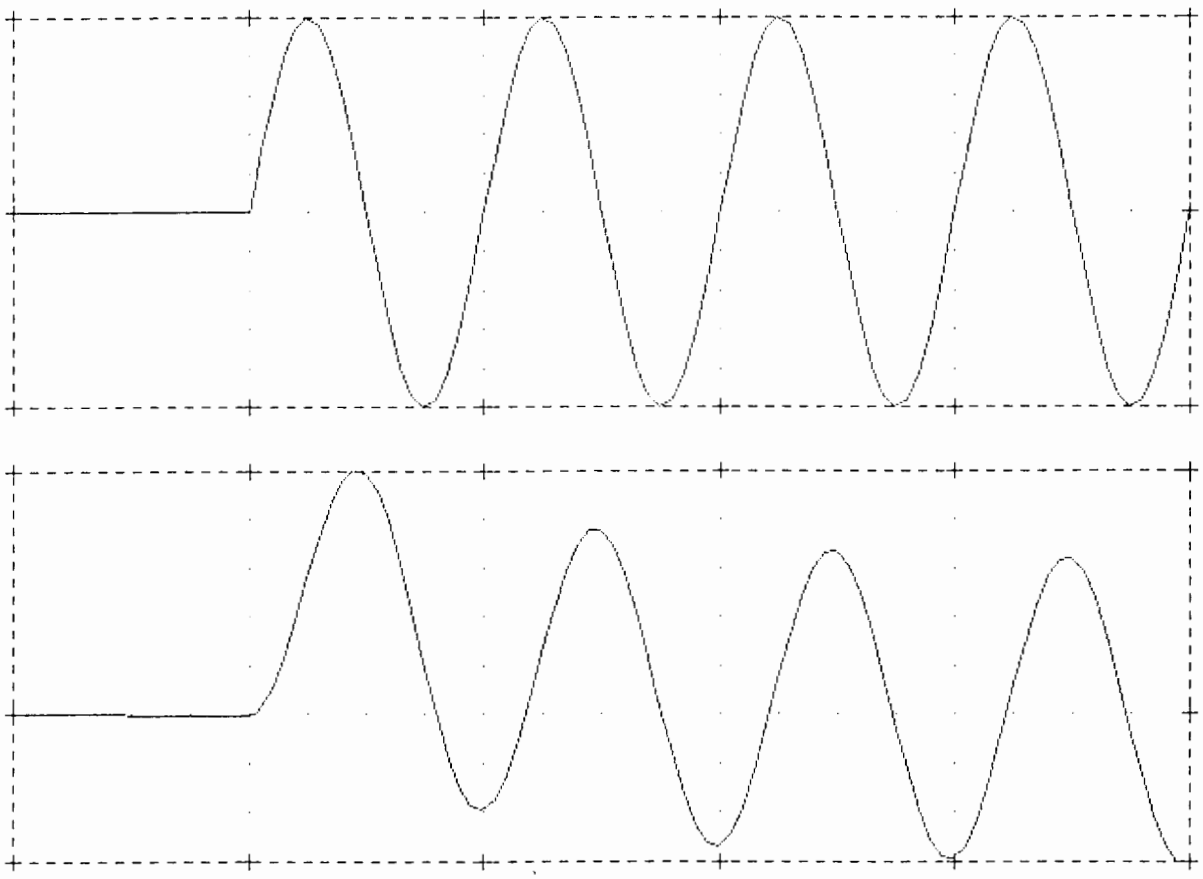
Assume for the circuit in shown above, that the switch closes at a time when the voltage is at a peak. The steady state current at a peak voltage is zero, so the current has already reached steady state and there is no transient DC component.

Now assume the switch close at a time when the voltage is zero. The steady state current at zero voltage is a peak. the current may not jump to this peak, but will start from zero. The current waveform will therefore be offset by a DC value equal to the peak current. This DC offset decays to zero with a time constant equal to L/R [27].

A Pspice Model have been made of a switch connecting a sine wave voltage source to an inductive load. Two simulations were done to show the switch closing at a voltage peak and a voltage zero. Their output is shown below. The upper trace is the voltage and the lower trace is the current. The Pspice program listing can be found in Appendix D.



Switch closes at a voltage peak



Switch closes at a voltage zero

APPENDIX H

THE OPTOCOUPLER CHOICE

The optocoupler that is chosen to isolate the base drive from the control circuitry should possess certain parameters to facilitate its correct operation. The standard parameters, such as peak isolation voltage, current transfer ratio and output rise and fall times are of primary importance. Most of the optocouplers manufactured today have specifications that meet the base drive's requirements.

One parameter that can be overlooked is the optocoupler dV/dt rating[1]. When the transistor switches on, under low power conditions, the voltage can drop within 0.5us. If the voltage drops from 250V to 0V within 0.5us, the dV/dt is 500 V/us.

The common 6N137 as well as the K8031P optocoupler have a dV/dt rating of 50V/us [35]. Optocouplers with a higher dv/dt rating are available, but are both difficult to obtain and expensive.

During the research many papers were obtained that pointed out the need for high dV/dt ratings in optocouplers that isolate base drives[2]. None of this material explained what would happen if the dV/dt rating was to be exceeded. Some authors suggested that the capacitive coupling across the isolation would cause the optocoupler to trigger on and off falsely, but no evidence was given.

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1. - The optocoupler dV/dt rating is the maximum allowable rate of voltage change across the isolation.
2. - These papers are listed in References 8, 12, 13, 15, 16, 36.

Since the completion of the final converter, the base drive was modified to drive the gate of an IGBT using the same optocoupler as before. The IGBT switches from 350V to 0V within 200ns, giving a dV/dt of 1750V/us, 35 times the rating of the optocoupler! No false triggering or any other effects due to capacitive coupling occurred.

Some unanswered questions that arose during this project are: Does a high dV/dt on the optocoupler have a permanently damaging effect on its operation? If the dV/dt rating is to protect against false triggering, will an optocoupler operate above its rating for ever if it has proved itself on the test bench?

In all the literature researched these questions remain unanswered. The optocouplers in the converter are operating outside their rating and have been for approximately 6 months. This could mean that high dV/dt's do not damage the optocoupler.

APPENDIX I

CONTROLLING ELECTRICAL INTERFERENCE BY CORRECT WIRING

During the course of the project, the importance of correct wiring became very apparent. When designing a power electronic machine the physical positioning of wires and components is often overlooked. This Appendix points out common wiring mistakes, that may seem obvious, but are not always avoided. Two papers helped to compile this information. They are: the VAA4002 base drive application notes written by Thomson semiconductors and the book by Michel Mandiguian, "How to control Electrical noise".

1 CONNECT ALL COMMON WIRES TO ONE POINT

On the negative rail, for example, one physical point should be assumed to be 0V. All 0V connections should be made to this point. A length of wire should not be expected to have the same voltage anywhere along it. In the environment of high power switched currents, a small inductance in a wire can produce potential differences across the wires.

2 AVOID EARTH LOOPS

Do not make connections so that current can pass through more than one wire (in parallel). If this does happen more current than anticipated could pass through a wire, producing increased potential differences across that wire.

3 AVOID ENCIRCLING ANY AREA BETWEEN WIRES.

By encircling area between wires, a "fulx loop" is created. Any area between wires creates a path for flux, making a one turn air core inductor. The greater the area, the greater the flux. The larger the area, the larger the inductance along the two wires.

4 DO NOT ENCIRCLE A WIRE BETWEEN OTHERS

Creating a loop around another wire is effectively a one turn current transformer. Current in one pair of wires will give rise to an induced current in the other set of wires and vice versa.

5 RUN POWER CABLES SEPARATE FROM SIGNAL CABLES

Cables that run parallel to each other induce a current in each other. If a signal wire runs next to a high current cable, any high frequency noise will be transferred from the high current cable to the signal cable.

6 USE SHORT WIRES

At all times the shortest possible wires should be used. Short wires have a low self inductance, and are also less prone to interference from other sources. This means that components in a machine should be placed as physically close together as possible. For sunbber capacitors and DC bus capacitors this is of extreme importance.