A Power and Time Efficient Radio Architecture for LDACS1 Air-to-Ground Communication

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***Abstract*—L-band Digital Aeronautical Communication System (LDACS) is an emerging standard that aims at enhancing air traffic management by transitioning the traditional analog aeronautical communication systems to the superior and highly efficient digital domain. The standard places stringent requirements on the communication channels to allow them to coexist with critical L-band systems, requiring complex processing and filters in baseband. Approaches based on cognitive radio are also proposed since this allows tremendous increase in communication capacity and spectral efficiency. This requires high computational capability in airborne vehicles that can perform the complex filtering and masking, along with tasks associated with cognitive radio systems like spectrum sensing and baseband adaptation, while consuming very less power. This paper proposes a radio architecture based on new generation FPGAs that offers advanced capabilities like partial reconfiguration. The proposed architecture allows non-concurrent baseband modules to be dynamically loaded only when they are required, resulting in improved energy efficiency, without sacrificing performance. We evaluate the case of non-concurrent spectrum sensing logic and transmission filters on our cognitive radio platform based on Xilinx Zynq, and show that our approach results in 28.3% reduction in DSP utilisation leading to lower energy consumption at run-time.**

I. Introduction

Air traffic has seen tremendous growth over the last decade, pushing the need for efficient communication between aircraft and air traffic control terminals (or ground base-stations). Traditional aeronautical communications use the VHF band for commanding of and reporting by aircraft and but this is now becoming saturated preventing further expansions in this frequency band. L-band Digital Aeronautical Communication System (LDACS) is being proposed as a solution that can co-exist with legacy L-band systems and aims to explore digital radio techniques to enable efficient communication for next-generation global air traffic management system [1]. Of the two specifications that are being reviewed for LDACS, the type-1 (LDACS1) specification defined by EUROCONTROL [2] is gaining traction as the preferred model for final deployment.

Traditional aeronautical communication schemes use static spectrum allocation requiring the ground stations and aircraft to synchronise and agree on a common frequency beforehand. Since these must be allocated in advance of use, and remain so for a period of time, this results in inefficient spectrum usage, especially in congested airspaces. Furthermore, legacy aeronautical communication systems predominantly used analog processing modules in the baseband and RF sections resulting in limited capabilities compared to modern digital radio systems that offers intelligent mechanisms for efficient use of the radio spectrum. The introduction of LDACS1 will open up possibilities for introducing dynamic frequency allocation which can offer numerous advantages in terms of spectral efficiency, seamless connectivity and enhanced capacity [3]. Using cognitive radio based dynamic spectrum access in LDACS1 would enable the communicating entities (aircraft as well as ground base-stations) to opportunistically access suitable L-band channel(s) that meet Quality of Service (QoS) requirements.

However, enabling dynamic spectrum access requires the use of efficient signal processing techniques that can perform spectrum sensing and channelization. With dynamic spectrum access, an aircraft that needs to communicate with the ground base-station has to first identify the vacant frequency bands, determine a suitable channel amongst them and then initiate an LDACS1 transmission. While ground base-stations can employ powerful processing systems to support LDACS1 requirements, the limited power/size budget on aircraft demands efficient architectures that can conserve power while meeting the high processing throughput and flexibility requirements. Furthermore, LDACS1 specifications place stringent requirements on the transmitted LDACS1 channel to ensure that legacy L-band systems are unaffected by the presence of LDACS1 communication [2]. The spectrum sensing, channelisation and masking filters require significant computational resources to operate in tandem, resulting in large area and high power consumption when they are implemented directly.

Alternatively, since these blocks operate non-concurrently, they can be enabled only when the transmit path needs to be actived, thus reducing run-time power consumption. Using advanced techniques available on modern Field Programmable Gate Arrays (FPGAs), this could be further extended by loading the required modules as and when they are needed through run-time reconfiguration, reducing resource requirements for the baseband modules. In this paper, we present an efficient radio architecture for realizing dynamic spectrum access enabled LDACS1 air-to-ground communication. The proposed architecture makes use of a hybrid Zynq FPGA-based radio platform [4], which offers high-speed reconfiguration and a

tunable radio front-end. We show that the architecture reduces the DSP resource utilization by 28.3% and power consumption by up to 28.5% by consolidating non-concurrent processing blocks using partial reconfiguration, compared to a fully static implementation.

The remainder of this paper is organised as follows. Section II provides an overview of the LDACS1 standard and the key requirements that are established by the standard for allowing co-existence with legacy L-band systems. Section III discusses related work in FPGA-based cognitive radio approaches, spectrum sensing, and filter banks. Section IV presents an implementation of the channel filter blocks (transmit path) and the spectrum sensing blocks (receive path) for LDACS1 and their integration into the radio platform. In Section V, we evaluate the proposed architecture using a Xilinx ZC702 evaluation board. Finally we conclude the work in Section VI, outlining our future research directions.

II. Background

Following recommendations from the International Civil Aviation Organisation (ICAO), one of the options being considered for LDACS1 deployment is an inlay approach between adjacent channels of the Distance Measuring Equipment (DME) which operates in the frequency range 962–1213 MHz. The proposed LDACS1 standard provides two isolated data-links: the LDACS1 ground-to-air (called forward) and air-to-ground (called reverse) data-links, which provide a total of 46 communication channels with a bandwidth of 500 kHz each. Each LDACS1 channel is offset by 500 kHz with respect to the adjacent DME channels to avoid interference, as shown in Fig. 1. Stringent requirements on the transmitted LDACS1 are needed to support such an inlay approach.

To ensure the non-interfering co-existence of LDACS1 and DME channels, spectral mask specifications in terms of relative attenuation at particular frequencies away from the center frequency of a LDACS1 channel are specified in the LDACS1 specification document [2]. Following are the frequencies away from the center frequency of a LDACS1 channel and the corresponding attenuations required {(249.025 kHz, 0 dB), (336.184 kHz, -40 dB), (622.563 kHz, -56 dB), (771.978 kHz, -76 dB), (1245.125 kHz, -76 dB)}. These spectral mask specifications have to be satisfied in order to use LDACS1 channels for communication.

Traditionally, communication channels for forward and reverse links are allocated statically; the aircraft that wishes to communicate with a specific ground station must manually switch to the allocated frequency before initiating a communication. However, this static assignment results in highly inefficient use of the limited available spectrum. Dynamic spectrum allocation strategies based on cognitive radio based spectrum sensing have recently been proposed to achieve efficient aviation spectrum management [3], [5]. This would also reduce the load on the ground stations, which would otherwise have to manage and keep track of different channels that are allocated to the communicating parties.

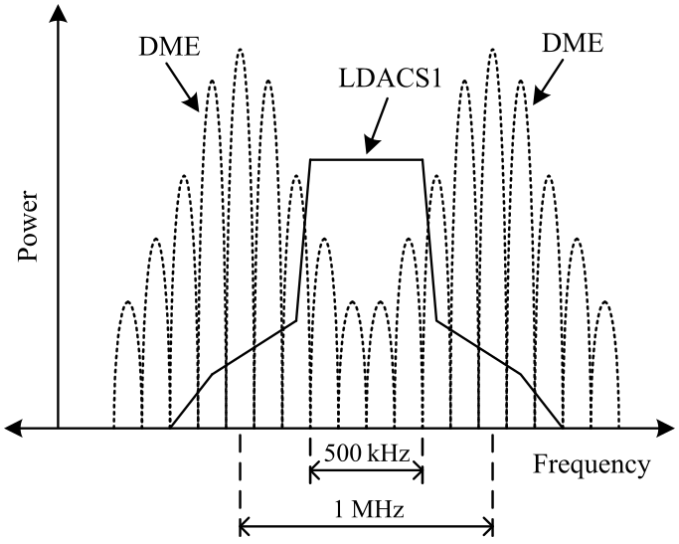

Fig. 1: Frequency domain view of the proposed LDACS1 deployment, interspersed within existing DME channels in L-band spectrum.

We have considered the following dynamic spectrum access enabled LDACS1 communication scenario in our work – with dynamic spectrum access, an aircraft that needs to communicate with the ground base-station has to first identify vacant frequency bands, determine a suitable channel amongst them and then initiate a LDACS1 transmission. To detect the vacant frequency bands, energy detector based spectrum sensing can be performed using variable cutoff digital filters or filter banks [6], [7]. Once a suitable frequency band is chosen, an LDACS1 transmission may be initiated, which needs to pass through a channel filter to meet the stringent LDACS1 spectral mask specifications. Each of these operations is complex: the filter bank and channel filter when implemented statically, consume large energy and area. However, since these blocks are non-concurrent, it should be possible to implement them in a manner that the blocks can be loaded as and when they are needed. Therefore, a major research challenge involved in the realization of this LDACS1 communication scenario is to achieve an area and energy efficient architecture to implement the LDACS1 radio system.

III. Related Work

Evolving commercial radio standards rely on flexibility to make efficient use of the limited communication spectrum, requiring radio platforms to support run-time adaptability for baseband as well as RF systems. Cognitive radio platforms like GNU Radio [8] and Iris [9] focussed on software-driven platforms and modularity. Software-based approach enables the baseband and the MAC layers to be easily adapted at run-time. However, the processing overheads due to software-based radios on general purpose platforms limit their usability in low-power and constrained environments like aircraft.

To overcome these limitations, the advanced capabilities of modern FPGAs have been explored in multiple radio platforms

like WARP [10] and Iris [11], where it was shown that the flexibility of FPGA-based platforms can help minimize power consumption in the baseband processing path in response to dynamically varying channel conditions. Other platforms like CRUSH [12] and CRKIT [13] also demonstrated the benefits of offloading complex baseband processing to custom hardware on FPGAs. With faster adapting standards, increasing flexibility requirements, and hard constraints on space and power, FPGAs offer the performance benefits of custom hardware with some of the flexibility of software. They have been exploited in the design of adaptive architectures for spectrum sensing using filter banks [14] and in general architectures for channel filtering to meet emission mask specifications for multiple standards [15], where software implementations would have been unfeasible within embedded constraints.

Numerous works have explored the use of low complexity variable digital filters and filter banks in software defined radio platforms [16], [17], [18] for both spectrum sensing and channelisation. The usage of filter banks for spectrum sensing was proposed in [16]. We have recently proposed a low complexity variable digital filter [18] and a filter bank [17] which can be used for multi-standard channelization in software defined radios. Use of such filters and filter banks offers the ability to realize low power reconfigurable radio architectures which can be efficiently implemented using FPGAs.

Beyond the performance enhancements, partial reconfiguration (PR) has also been explored for reprogramming hardware sub-modules to adapt baseband functions at run-time [11], [4]. PR is an advanced technique that allows parts of the hardware to be modified at runtime while other parts continue to run, enabling designers to swap modules at any given time. Iris has explored the use of partial reconfiguration, but the software portions of the radio are deployed on a PowerPC hard processor on the Virtex 5 FPGA, resulting in low performance [11]. In [4], a more efficient approach is described using the hybrid Zynq platform, which offers tight coupling between the software and hardware sections of the radio system and integrates a high-speed reconfiguration management system that abstracts the low-level details associated with PR. Our experiments in this paper leverage the capabilities of this platform for enabling dynamic spectrum access in the LDACS1 scenario.

IV. Platform Architecture

A. Filter architecture

In the LDACS1 radio platform presented in this paper, we use a digital filter bank and a channel filter in the LDACS1 transmitter chain for spectrum sensing and shaping respectively. The digital filter bank is based on the fast filter bank (FFB) design technique as proposed in [6]. The FFB design method proposed in [6] is a low complexity filter bank design technique which provides multiple uniform subbands which satisfy the stringent LDACS1 spectral mask specifications as discussed in Sec. II. When used in the receiver chain of an aircraft, the FFB can be used to perform energy detector based spectrum sensing to detect the vacant frequency bands. We consider a sampling frequency of 4 MHz and design an 8-channel FFB to be used in our radio platform. Out of the 8 subbands provided by the designed FFB, 4 alternate subbands are used for LDACS1. Fig. 2 shows the frequency responses of these 4 subbands of the FFB. As can be noted from Fig. 2, each of the obtained subbands satisfies the desired LDACS1 spectral mask specifications. The FFB used in our LDACS1 radio platform requires a total of 70 coefficient multipliers which can be efficiently implemented on an FPGA using the available DSP blocks.

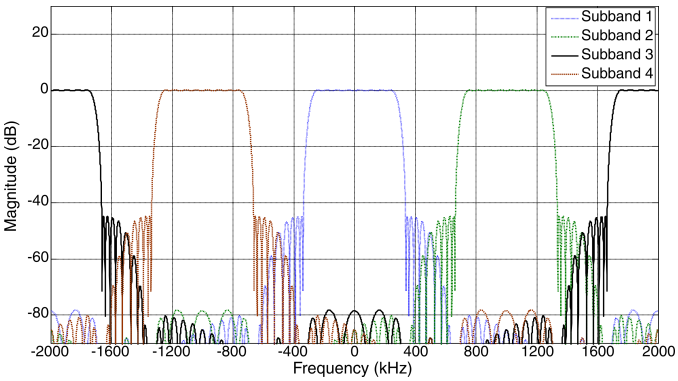

Fig. 2: Filter response of the Fast Filter Bank design used for channelisation.

The FFB architecture follows a tree structure as shown in Fig. 3. For a k-stage FFB, the interpolation factor (M_i) of $2^{(k-i)}$ is used on the prototype lowpass filter of i^{th} stage (where $i = 1, 2...k$) to get a multiband response. For the case $k = 3$ shown in Fig 3, we get M_1 = 4, M_2 = 2, M_3 = 1. Frequency shifted versions of the interpolated prototype filter response and their complementary responses are used at every stage as shown in Fig 3. Frequency shifted filters are denoted as F_{ij} in Fig 3, where i refers to the number of stage and j refers to the frequency shift index. A k-stage FFB generates total $N = 2^k$ subbands. Transition bandwidth of each channel is $t_{\text{bw}}/2^{(k-1)}$, where t_{bw} is transition bandwidth of prototype filter in first stage.

The digital channel filter is designed using MATLAB Filter Design and Analysis Tool. Similar to the case of the FFB, a sampling frequency of 4 MHz is considered and the edge frequencies are accordingly computed for a low-pass filter. To ensure that all of the different attenuation specifications for an LDACS1 spectral mask are satisfied, we consider the most stringent attenuation specification, i.e., -76 dB and design the channel filter to satisfy the same. Fig. 4 shows the frequency response of the channel filter used in our LDACS1 radio platform. The order of the filter used is 200 and it requires 101 coefficient multipliers for its implementation using the transposed direct-form implementation architecture, which are then mapped to FPGA DSP blocks.

Note: The LDACS1 specifications proposal [2] recommends an oversampling factor of at least four while performing channelization, to help mitigate the impact of inference while operating LDACS1 as an inlay system. Therefore, as the

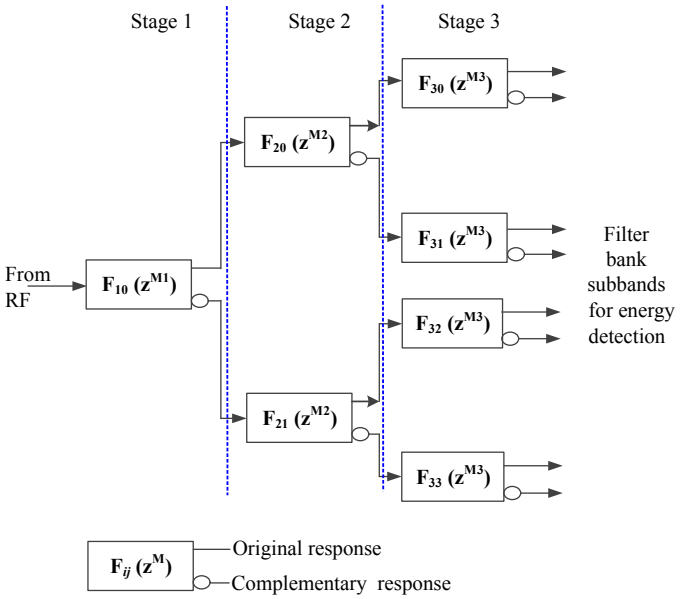

Fig. 3: Architecture of the Fast Filter Bank used for channelisation.

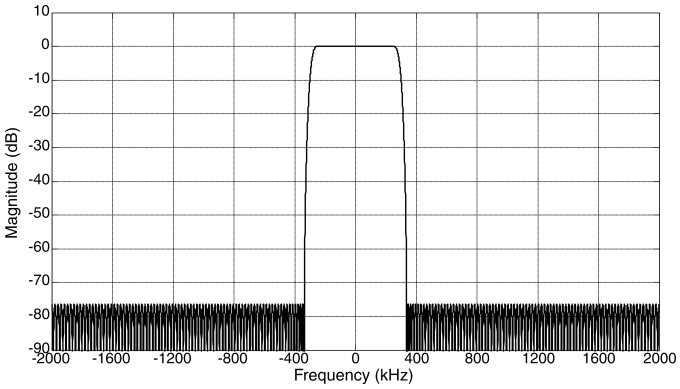

Fig. 4: Filter response of the Channel Filter used for shaping the transmission spectrum.

channel bandwidth of LDACS1 is approximately 500 kHz, we have chosen the sampling frequency as 4 MHz for the FFB as well as the channel filter.

B. LDACS1 Radio Platform

Hybrid FPGAs like the Xilinx Zynq present a compact and efficient architecture for building cognitive radio systems that integrate cognitive software to interact and manage high performance processing datapaths built in hardware. The Zynq platform tightly couples a highly capable dual-core ARM processing system with a reconfigurable fabric, providing computational capability and flexibility for both the control path in software and the processing blocks in hardware. However, managing hardware adaptation on FPGAs at runtime requires integration of low-level control tasks and knowledge of the underlying hardware.

Our radio platform abstracts such low-level details from the user while also integrating efficient high-speed dynamic

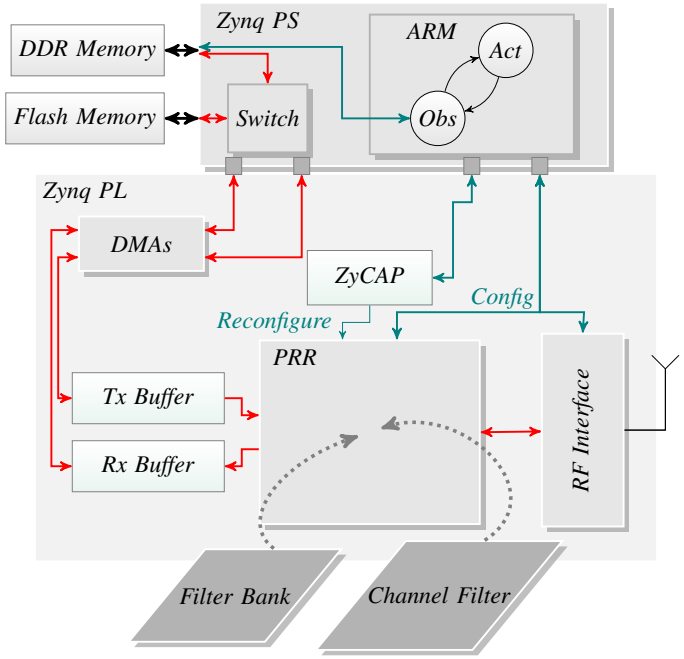

Fig. 5: Architecture of the proposed LDACS1 radio platform on the Xilinx Zynq FPGA.

partial reconfiguration for hardware-level support of baseband adaptation [4]. The simplified diagram in Fig. 5 shows the architecture of the radio platform and the integration of LDACS1 filter blocks into the baseband section. Data movement from/to software or external interfaces (like DRAM memory or Ethernet interfaces) is handled using dedicated direct memory access (DMA) controllers. The baseband functionality and antenna interfaces are implemented in the programmable logic (PL) region of the Zynq, and use dedicated interfaces for interaction with the software tasks running on the arm core.

The antenna interface connects to an off-the-shelf Analog Devices AD-FMCOMMS4-EBZ board (based on the AD9364) using an FPGA Mezzanine Card (FMC) connector. The FMCOMMS4-EBZ offers an operating range of up to 6 GHz with tunable parameters that can be configured by the software application or directly from the baseband modules. This adaptability, called parametric reconfiguration, offers a method to quickly alter the performance of the system without any changes in the physical design of the processing blocks. Further, the platform supports high-speed partial reconfiguration through ZyCAP [20], that allows the physical implementation to be modified at runtime with low latency. We make use of PR to reduce the area overhead and power consumption in case of LDACS1 scenario by implementing the non-concurrent functionality in a partially reconfigurable region (PRR), which can then be reconfigured on-the-fly when needed.

As shown in Fig. 5, the PRR can hold either the FFB module, which detects spectrum gaps and determines the best downlink frequency for transmission, or the CF module that performs spectral shaping on the transmitted LDACS1 channel to minimize interferance to adjacent channels (DME

as well as other LDACS1 channels). During normal receive operation (ground-to-air link), the PRR region is loaded with bypass logic that streams data from the antenna interface to the upstream baseband modules in the LDACS1 chain. The receiver of the RF interface can be tuned to the specific LDACS1 channel (frequency and bandwidth) for receiving the ground-to-air communication. LDACS1 uses Orthogonal Frequency Division Modulation (OFDM) as the baseband modulation technique, for which numerous implementations are available.

When the aircraft is to initiate a transmission to the ground station, the air-to-ground link must be sensed to determine the free channel(s) available. For this, the RF interface is tuned to the air-to-ground band covering the entire bandwidth and the PRR region is loaded with the FFB module to determine spectrum gaps. Double buffers are placed prior to the FFB module to accumulate the received samples, which alternatively feed the FFB module with a burst of received samples. The FFB module analyses 4 LDACS1 frequency bands at a time, with an energy detector at each subband to determine the presence or absence of an LDACS1 signal in the chosen channel. Once all the 23 channels are analysed, the list of available channels for transmission and their energy levels are presented to the software application which can then determine the best channel for transmission. The buffers combined with the high-speed operation of the FFB modules allows the operations to be overlapped, minimising the latency associated with spectrum sensing.

To transmit data, the PRR region is loaded with the CF module. The channel filter shapes the transmission stream to meet the LDACS1 requirements before passing it to the antenna interface. The channel filter also operates at high frequencies allowing the LDACS1 frame to be streamed to the RF interface with minimal latency. FIFOs are integrated at the input and output ports of the channel filter to adapt to the different data/clock rates. The different modules are loaded into the PRR by the cognitive software application using the function call `set_basesband(spectrum_sense)` from software running on the PS. The PR manager integrated into the platform handles all the low-level steps needed for physical reconfiguration. Hence, it would be possible to modify the adaptive behaviour purely by changing the software.

V. Results

To evaluate the efficiency of the approach, we implement the radio architecture targeting the Xilinx ZC702 development platform, which houses a low-end Zynq device (XC7020CLG484-1). The device features dual ARM A9 cores that can run at 667 MHz as the PS while the PL region offers 53k Look Up Tables (LUTs), 106k Flip Flops (FFs) and 220 DSP blocks for implementing the radio baseband modules. We have used Xilinx Vivado 2014.2 as the tool flow for our implementation process. For comparison, a static implementation is generated on the ZC-706 platform that uses a mid-range Zynq device (XC7045FFG900-2) that offers sufficient DSP blocks for a fully static implementation.

TABLE I: Resource utilisation on XC7020 and comparison with the fully static implementation on the XC7045.

Function	LUTs	FFs	BRAMs (36/18)	DSPs
Channel Filter	6672	6388	2/0	96
Fast Filter Bank	3397	3148	4/0	65
RF I/F	14915	23882	6/4	69
Reconfig	664	767	1/1	0
Total	22609	30287	12/5	165
(%)	42.7%	28.6%	6.07%	75%
F_{MAX}		250 MHz		
Fully Static	25722	32348	11/4	230

Table I shows the resources consumed by the different modules of the design. It can be seen that the CF and FFB modules are DSP intensive and cannot be implemented concurrently on the XC7020 device. Our approach of using PR for loading these functional modules as and when needed, reduces the number of DSP blocks needed (highest of the two), resulting in a 28.3% reduction in DSP block requirements compared to a fully static implementation. The lower DSP block requirement also allows us to target a low-power device as the implementation target, cutting down on the static power consumption of the platform. As observed from Table I, the implemented blocks consume only up to 43% of the logic resources (LUTs and FFs), leaving aside resources for implementing OFDM modulator/demodulator chain of the LDACS1 baseband. Also, the efficient implementation of the filter blocks allows us to obtain a maximum operating frequency of 250 MHz.

Table II details the power estimates generated using the Power Analyser tool available within the Vivado design suite. To provide accurate estimates, we have used the post place and route simulation activity of the modules at 250 MHz operating frequency as the activity file input to the Power Analyser. This allows the tool to evaluate the activity of the internal signals and predict the power consumption with high accuracy. It can be observed that the DSP intensive channel filter results in a power consumption of 1012 mW, of which 36% is contributed by the DSP blocks. In comparison, the fast filter bank that performs spectrum sensing consumes 508 mW of power. By loading these modules only when needed, we can lower the power consumption of the platform under normal operation by up to 1.02 W, compared to a fully static implementation on a larger XC7045 device.

Finally, we also measured the time taken to detect the vacant LDACS1 channels and activate the different modules from the application at run-time. We consider the case of using 20000 samples (at 4 MHz sampling rate) to detect the presence or absence of LDACS1 communication. The PR operation to load the FFB module is overlapped with the data acquisition process to hide the latency of PR operation. Our simulation results show that entire process to scan the 23 LDACS1

TABLE II: Power consumption on XC7020.

Function	DSP Power	Module Power
Channel Filter	360 mW (36%)	1012 mW
Fast Filter Bank	111 mW (22%)	508 mW
RF I/F	–	708 mW
ARM Cores	–	1343 mW
Platform Power	–	3063/2559 mW
Fully Static (XC7045)	–	3583 mW

channels and detect the spectral energy of each channel using our FFB module consumes 30.08 ms. A further reconfiguration operation is required to enable the channel filter, which consumes 1.88 ms using our high-speed reconfiguration interface (98% of theroetical maximum). This allows our platform to achieve a low turnaround time of 31.96 ms starting from the spectrum sensing phase to the activation of transmission chain on a vacant LDACS1 channel.

VI. Conclusion

Aeronautical communication is being upgraded to handle the ever increasing volume of information and to offer new pathways for communicating with critical systems on-board aircrafts. LDACS1 is an upcoming L-band aeronautical communication standard that aims to enable improved air-traffic management while ensuring non-interfering co-existence with the legacy L-band systems like DME. Techniques like dynamic spectrum access are being considered for this upcoming standard, that would allow efficient use of the spectrum; however, the operations associated with dynamic spectrum access are complex and computationally intensive, requiring an efficient approach to implement them.

In this paper, we presented the case for incorporating dynamic spectrum access in LDACS1 air-to-ground communication leveraging partial reconfiguration on FPGAs. We showed that our proposed approach results in over 28.5% reduction in dynamic power consumption and 28.5% reduction in resource utilisation, while offering high-speed switching between the different modes of operation in real-time. We aim to extend this approach to other aircraft communication systems that operate in different modes along the various phases of the flight, thus providing improved consolidation and energy efficiency. We are also integrating our full OFDM baseband for an end-to-end demonstration.

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