Impact of carbon in the buffer on power switching GaN-on-Si and RF GaN-on-SiC HEMTs

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This article addresses the impact of the buffer doping on the critical performance issues of current-collapse and dynamic R_{ON} in GaN high electron mobility transistors. It focusses on the effect of carbon, either incorporated deliberately in GaN-on-Si power switches, or as a background impurity in iron doped RF GaN-on-SiC devices. The commonality is that carbon results in the epitaxial buffer becoming p-type and hence electrically isolated from the 2-dimensional electron gas by a P-N junction. Simulations which incorporate a model for leakage along dislocations are used to show that a remarkably wide range of experimental observations can be explained including dynamic R_{ON} and the complex time dependence of drain current transients in power switches. In RF GaN-on-SiC devices, the current-collapse, the drain current dynamics, kink effect, pulse-IV and electric field distribution in the gate-drain gap can all be explained.

1. Introduction

GaN based high electron mobility transistors (HEMTs) are now dominant in RF application areas such as base-station power amplifiers and increasingly are entering the power switching marketplace in application areas such as fast chargers[1)]. This superiority to silicon based components arises due to basic materials benefits such as the wide bandgap giving high breakdown field, the ability to form a heterojunction leading to high mobility and carrier density, and good thermal conductivity especially when grown heteroepitaxially on substrates such as SiC. However GaN HEMTs are vulnerable to a variety of charge trapping related instabilities which include dynamic R_{ON} and current-collapse following high off-state bias, respectively an increase in resistance in the on-state and a decrease in saturation current capability. These instabilities can either be surface effects or can be due to trapping in the bulk below the 2 dimensional electron gas (2DEG)[2)]. Surface trapping can be largely controlled by a combination of passivation layers and electric field control using field plates, however bulk trapping continues to be an issue which impacts even commercial devices[3)], and it is bulk trapping which is the subject of this article. The normal way of discussing this trapping is in terms of the density of traps, their capture cross-sections and their energy levels, however we will show that this is not sufficient or even a useful approach in many cases.

Conventional GaN HEMTs require a semi-insulating layer below, and spaced away from, the 2DEG to suppress off-state leakage and short-channel effects. This is normally achieved by adding a deep acceptor such as iron or carbon, with the assumption that this will pin the Fermi level and allow the buffer to be treated as an insulator. The density of added traps in the bulk of the epitaxy is often regarded as commercially sensitive information and so it is omitted from publications, although typical values might be ~10^{19}cm^{-3} of carbon for power switches[4, 5)] and ~10^{18}cm^{-3} iron for RF HEMTs[6)]. Especially for power switches this far exceeds the density required to explain the observed bulk trapping effects, with only a small proportion of the acceptors ever ionized[4)]. We will show that many of the observed trapping effects can be better explained in terms of electrostatics and transport in the buffer[4)]. The location and magnitude of the ionized trapped charge is determined quantitatively by the electrostatics of the device[7)], and the dynamics largely determined by the transport to the small proportion of those traps which are changing their charge state via dislocation leakage,

3D hopping or band edge conduction[8]. Hence a better way of describing the vulnerability of a device to bulk trap effects is in terms of the distribution of incorporated and background dopants and the transport properties of the multilayer epitaxy.

Power switching HEMTs (and here we will consider the current primary market niche of 650V switches) use a buffer structure below the 2DEG which consists of a nominally undoped GaN channel, a heavily carbon doped GaN layer, and then a set of (Al,Ga)N strain relief layers all grown on a Si substrate. By contrast RF power devices which are less cost sensitive often use a GaN buffer which is iron (Fe) doped and grown on an insulating SiC substrate[9]. At first sight these architectures are quite distinct, however metal-organic chemical vapour deposition (MOCVD) epitaxial growth is used in almost all cases for commercial devices and inevitably incorporates a background of carbon impurities into the epitaxy. Carbon when substituted on the nitrogen site has its acceptor level 0.9eV above the valence band[10], energetically far below that of the Fe acceptor which is located ~0.7eV[6] below the conduction band. If, as is frequently the case, the density of carbon exceeds the density of any background donors, the Fermi level will reside on the lowest acceptor level and will be close to the C_N level in the lower half of the gap[7]. It has long been recognized that unintentionally doped semi-insulating buffers can be majority carrier p-type but with very low hole density, resulting in substrate bias induced threshold instability[11]. Hence the factor in common between power switching and RF epitaxy is the presence of carbon and the fact that it results in the buffer becoming p-type.

In this paper we review the transport mechanisms in the GaN buffer layers and discuss in detail the consequences of a p-type floating buffer for GaN HEMTs; it is partly based on recent conference papers[12-14]. It has been incontrovertibly shown using substrate ramp measurements that the negative charge build-up responsible for dynamic R_{ON} in GaN-on-Si devices is controlled and suppressed by vertical band-to-band leakage from the 2DEG into the floating region, almost certainly along dislocations[15, 16]. Until recently this dislocation leakage could not be modelled directly in technology computer aided design (TCAD) simulations, and leakage paths were included only under contacts[4, 17, 18], nevertheless giving a convincing explanation for the bias dependence of dynamic R_{ON} and pulse IV results. Here we include for the first time the effect of dislocation induced leakage in GaN HEMT TCAD simulations which incorporate realistic distributions of deep acceptors and their

compensating donors in both power switching and RF devices. We show that a remarkably wide range of trap related phenomena can be explained including the complex bias dependence of dynamic R_{ON}, its time dependent behaviour, as well as the kink effect, all based on the impact of carbon together with a reasonably realistic representation of the leakage paths in the device.

2. Simulation Environment

Device simulations were undertaken using the Silvaco Atlas TCAD software suite version 5.29.0.C. The main advance in HEMT simulation reported here compared to previous studies comes from the inclusion of a new model for vertical leakage along dislocations allowing for the first time the impact of band-to-band leakage to be included. The model uses a non-local 1D nearest neighbour hopping model and can successfully predict the reverse bias leakage in GaN p-n diodes[19-21], and model dynamic R_{ON} in GaN-on-Si power devices[12]. The hopping current is given by

$$J = \frac{N_{TD} q v_0}{1 + \frac{2\exp\left(qE_\sigma/kT\right)}{\exp(qbF/kT) - 1}}$$

where N_{TD} is the dislocation density, v_0 is the hopping frequency (set to 10^{11}Hz), E_σ is the energetic width of the defect band (120meV), b is the separation of hopping sites along the dislocation (1.1nm), and F is the electric field. For fields up to a few hundred kV/cm, this expression predicts Ohmic conduction. This model assumes that all dislocations are active, identical, and the occupation of the defect band is exactly 0.5, none of which are likely to be entirely accurate. Hence the number density of dislocations used in the simulations reported later should be taken as nominal, although it should be useful for comparative purposes.

The conventional models employed were Fermi-Dirac and Shockley-Read-Hall statistics, and a simple Caughey-Thomas velocity saturation law, $\mu = \mu_0(1 + (\mu_0 F/v_{sat})^\beta)^{1/\beta}$, where μ is mobility, v_{sat}=1.9x10^7cm/s is the saturated velocity and β=2.3. No self-heating, impact ionization, surface trapping, or gate leakage models were included so that the results were only sensitive to epitaxial doping effects. A positive polarization charge was incorporated at the AlGaN barrier/GaN interface and adjusted to give the desired pinch-off voltage under the gate. A negative charge was then placed at the surface and adjusted to place

the Fermi level about 0.5eV below the conduction band. No polarization charges were incorporated at the heterojunction at the bottom of the GaN layer. This was done to prevent any hole gas forming, which although it can arise in practice[22, 23], was not the main objective of the simulation study. Convergence was a major issue when using this hopping model requiring careful meshing and a numerical precision of at least 80 bits, and in some regimes such as at high dislocation density and high drain bias in off-state, even using 256 bits was insufficient to ensure convergence.

The key parameters employed were 2DEG mobility 1450cm^2/Vs, bulk hole mobility 8cm^2/Vs. For carbon substituted on the nitrogen site (C_N), electron and hole cross-sections were 10^{-15}cm^2, acceptor level 0.75eV above the valence band (this value rather than 0.9eV[10] was used to improve convergence by increasing the free hole density in the buffer). For iron, electron capture cross-section was 10^{-13}cm^2 and hole cross-section 10^{-15}cm^2, with acceptor level 0.7eV below the conduction band[6].

3. GaN-on-Si Power HEMTs

3.1 Transport and charging in carbon doped GaN

Fig. 1 shows the typical architecture for a 650V GaN-on-Si power switching transistor[1]. At the low to medium electric fields which are relevant to normal device operation, the thick AlGaN or superlattice SRL from an electrical point of view primarily serves as an insulator which isolates the active upper part of the device from the Si ground plane, with most of the applied drain voltage dropped across this layer. It is the nominally undoped (UID) channel layer and the heavily carbon doped layer below this that act to screen the 2DEG from the back-gating field from the Si ground and to suppress charge trapping and dynamic R_{ON}. The mechanisms by which this occurs were described in [4], and here we will give a brief review of transport mechanisms.

The carbon doped layer (GaN:C) is heavily doped typically with a density of about 10^{19}cm^{-3}, most of which resides substitutionally on the nitrogen site (C_N) and has an energy level 0.9eV above the valence band[10], however it is also heavily self-compensated with donors[24]. It is unclear whether these donors are carbon incorporated on the Ga site or whether they are the result of defect complexes, however their density has been inferred to be at least 40% of the C_N density[5, 24]. The carbon strongly pins the Fermi level to the C_N

level, with charge almost confined to narrow (10's of nm scale) depletion regions at the top and bottom of the carbon doped layer. The majority carrier is hence holes, but with a low density at room temperature of only around 10^4-10^6cm^{-3}. The high C_N density is reasonably close to the Mott transition[25] and as a result defect band (hopping) conduction is found to dominate over conduction by activation of free holes to the valence band[26], nevertheless the bulk resistivity is well above 10^{10}ohm.cm. The defect band conduction seems to be consistent with a 3D variable range hopping law[8], and as a result shows an apparent activation energy which is dependent on the measurement temperature range and can vary between 50meV and 0.9eV[26].

The GaN:C layer is essentially resistive, but isolated from the 2DEG by a P-N diode. Under normal drain bias conditions this diode is reverse biased, and its leakage properties have been found to be crucial to the suppression of dynamic R_{ON}[15]. The leakage in reverse biased GaN P-N diodes was first investigated for LEDs and was found to be associated with preferential conduction along mixed and screw dislocations[27-29], with strong indications of impurity band conduction[30]. In power switching HEMTs, it has been found that the leakage obeys a nearest neighbour hopping law, but with non-ohmic behaviour at low bias which may be associated with the barrier between the dislocation and the 2DEG[8].

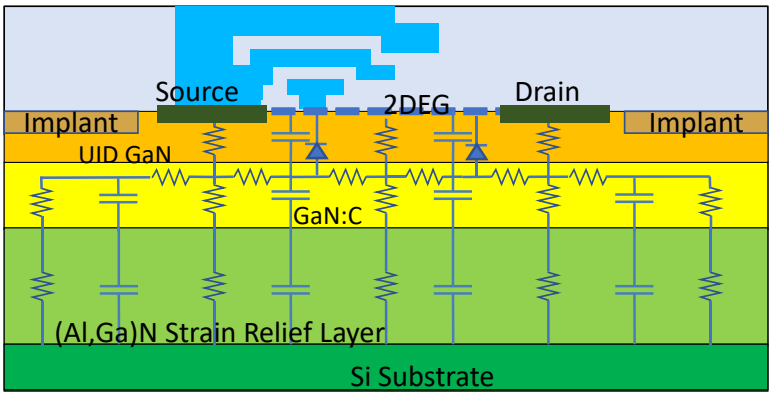

Figure 1. Schematic cross-section of a 650V GaN-on-Si power HEMT showing an overlaid equivalent circuit for transport within the device.

These transport mechanisms in the epitaxial layers can be represented as an equivalent circuit as shown in Fig. 1. In contrast to the traditional approach which represents the buffer as a single layer with traps, this network of resistors and capacitors allows an understanding of the operation of the device under both static and dynamic conditions. Under static bias

conditions, current flows through the resistive network and accumulates fixed charges at any discontinuities in resistivity (the Maxwell-Wagner effect[31]), which in this case are primarily at the upper and lower interfaces of the GaN:C layer. Under dynamic bias conditions the network will behave capacitively, however stored charge will impact the resulting change in charges in the 2DEG and the currents in the external terminals.

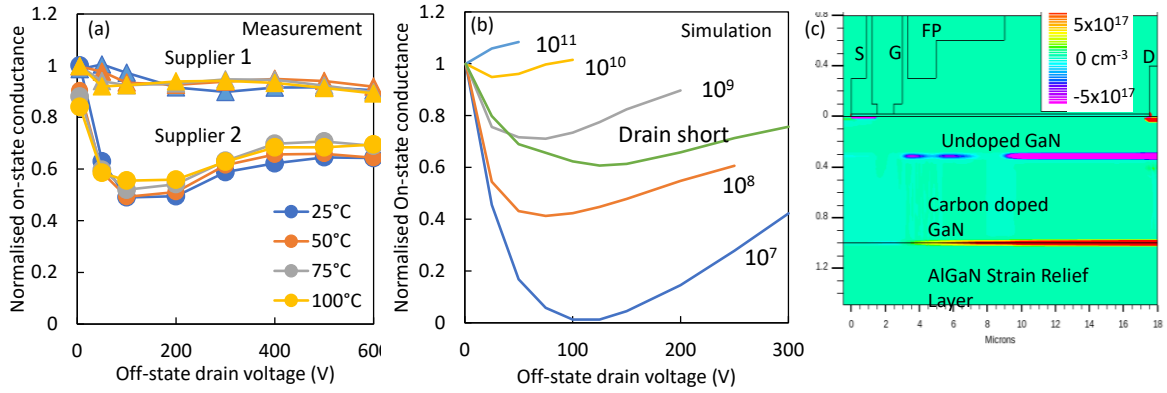

Figure 2. (a) ON-state conductance ie inverse dynamic R_{ON} for two different 30A, 650V GaN HEMTs replotted from Ref. [3]. (b) Simulated inverse dynamic R_{ON} as a function of off-state stress for varying dislocation density. (c) Net charge density with V_{DS}=1V, V_{GS}=0V 1µs following off-state stress at V_{DSQ}=300V, V_{GSQ}=-5V with 10^8cm^{-2} dislocations and 25ºC.

3.2 Dynamic R_{ON}

Dynamic R_{ON} is the change in on-state resistance following operation at an off-state bias, and is a key instability of GaN power devices. There are many definitions and measurement approaches although there is now a JEDEC standard[32], however here we consider a worst-case corresponding to the change in on-state conductance (or resistance) after applying off-state bias for sufficiently long period that the conductance change has saturated (typically hundreds of seconds). We will use conductance in all the graphs since in contrast to resistance, its magnitude stays in a range which is easily plotted on a linear scale.

The GaN-on-Si power switching transistor simulations used an epitaxial layer stack[4] which consisted of 20nm AlGaN barrier resulting in ~6x10^{12}cm^{-2} 2DEG charge, a 0.3µm unintentionally doped (UID) GaN layer containing 10^{15}cm^{-3} shallow donors, a 0.7µm GaN:C layer containing 10^{19}cm^{-3} C_N acceptors compensated with 3x10^{18}cm^{-3} shallow donors, on a strain relief layer (SRL) of thickness 3µm. The SRL we represented with undoped AlN and which forms an insulating layer with blocking heterojunction to the GaN:C layer. The

transistor simulated had a double field plate, gate length 1μm and L_{SD} of 17.5 μm as seen in Fig. 2c. The band-to-band hopping mechanism was enabled across the UID GaN layer, effectively providing a resistive path between the 2DEG and the top edge of the GaN:C layer.

Fig. 2a shows the change in on-state conductance change (ie inverse dynamic R_{ON}) as a function of off-state bias stress for two 30A, 650V commercial packaged switches sourced in 2017[3]. Supplier 1 showed less than a 10% change, whereas supplier 2 had unacceptable behaviour with a factor of two reduction in conductance. The minimum in conductance seen Fig. 2a at 150V was explained using a leaky dielectric model, discussed in the following, which was developed based on detailed substrate ramp and dynamic R_{ON} measurements[4]. Let us consider first the case corresponding to supplier 2 where it is presumed that there is only a small vertical leakage through the UID GaN layer. Under high positive drain bias there is a high vertical field between the drain and the Si ground. The GaN:C layer has lower resistivity than the UID GaN layer above or the SRL below and so current can only flow internally within the electrically isolated GaN:C layer resulting in the formation of a dipole with a positive charge at the GaN:C/SRL interface and a negative charge at the GaN:C/UID GaN interface. These charges will reside in narrow depletion regions of ionized donors and acceptors, respectively, and can be seen in Fig. 2c. The field also drops laterally from drain to gate/source, with a small lateral resistive current flow within the GaN:C layer resulting in a gradual increase in the potential difference between the 2DEG and the GaN:C as one moves from drain towards the field plates[18]. This back-biasing of the 2DEG by the GaN:C results in an accumulation in negative charge at field plate edges. The minimum in conductance (maximum in dynamic R_{ON}) in Fig. 2a arises from a competition between the negative going contribution which arises from the negative charged region and the positive going part which comes from the screening effect of the positive charged region near the drain.

The impact of leakage along dislocations through the UID GaN region is illustrated in Fig. 2b, where the dislocation density has been varied from 10^7 to 10^{11}cm^{-2}. At low dislocation density the back bias from the GaN:C is sufficiently high to achieve full pinch-off of the 2DEG, as can be seen for 10^7cm^{-2} dislocations at 100V where the conductance becomes zero. However as the leakage through the UID GaN increases, the vertical voltage drop across the UID GaN decreases, the negative charge at the top of the GaN:C layer reduces, the change in 2DEG density reduces, until eventually there is complete suppression

of dynamic conductance change following bias stress. Eventually at 10^{11}cm^{-2} the conductance changes sign when the negative charge is fully suppressed leaving the positive charge and resulting in an enhancement in performance, something which is observed experimentally[33]. The suppression of conductance change (dynamic R_{ON}) in devices with higher leakage current is well established. In some cases there has been a direct measurement of the presence of leakage using the substrate ramp technique[15, 16], with both proton implantation induced leakage[34] and surface passivation[35, 36] demonstrating a direct link between UID GaN leakage and dynamic R_{ON} suppression.

In the leakage model described here, the distribution of charge in the buffer that is responsible for dynamic R_{ON} is determined primarily by the ratio of the leakage resistivity of the UID GaN layer and the GaN:C layer. Suppression occurs when the UID GaN channel has lower resistivity than the GaN:C layer. The time constants for charge transport through these layers have recently been measured[8] for an IMEC wafer stack using a combination of substrate ramp and transient measurements. Different field and temperature dependences were observed for the transport through the two layers meaning that the ratio will be temperature and field dependent. Experimentally different temperature dependences for dynamic R_{ON} have been observed, ranging from the temperature independence seen in Fig. 2a, to an increase in magnitude with increasing temperature[37]. This variation presumably reflects epitaxy/process generated differences in the carrier transport in these different fabrication processes.

Some devices show preferential leakage under the drain to the GaN:C layer, and it was this situation which was simulated in previous papers from our group[4, 17, 18]. This corresponds to published solutions for dynamic R_{ON} such as a photonic drain[38], or a p-GaN gate hole injector[39] which provide a source of holes at the drain terminal. In Fig. 2b, a simulation of a short between the drain and the GaN:C with no dislocation leakage, shows a minimum in conductance similar to an intermediate dislocation density. Hence this model suggests that a short between the drain and the GaN:C layer alone can only reduce the dynamic R_{ON}, with leakage across the entire gate-drain gap required for full suppression. The magnitude of this leakage required for suppression is very small. Fig. 3 shows that for the case simulated, the current is less than 10pA/mm device width even for the highest dislocation density.

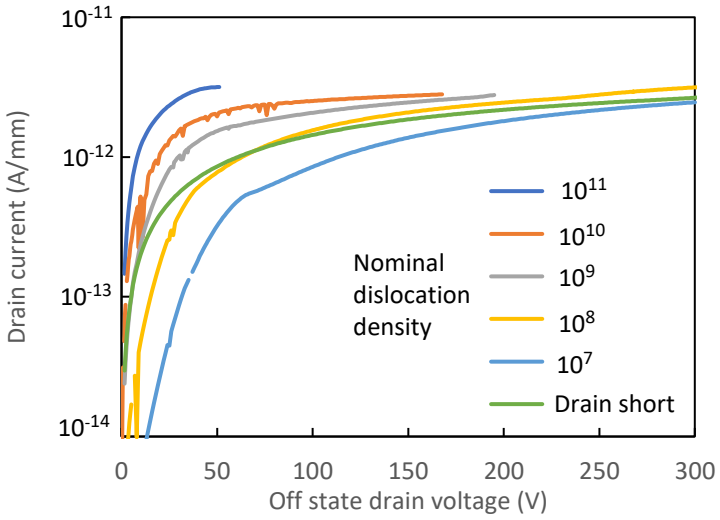

Figure 3. Off-state drain leakage current with V_{GSQ}=-5V for varying dislocation density (cm^{-2}), or a short between the drain and the p-type buffer. The noise on some curves is the result of slow convergence in the simulation.

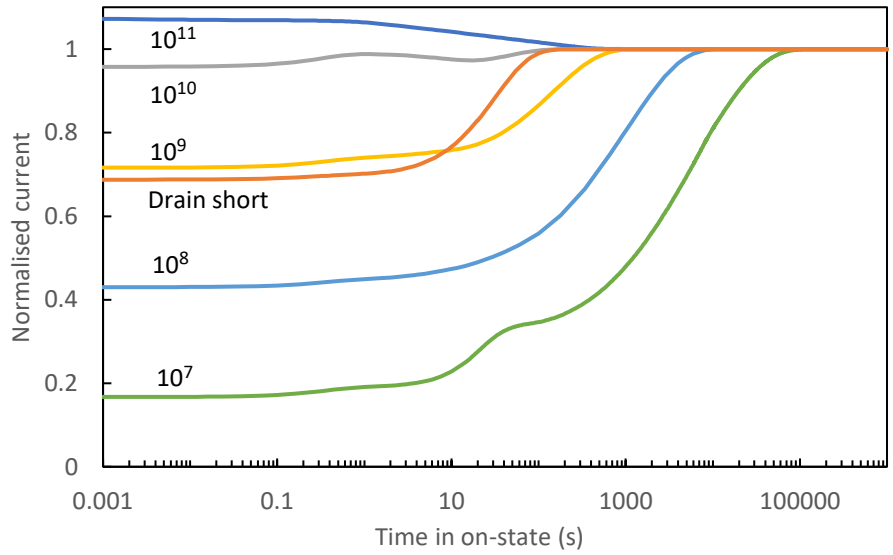

Figure 4. Drain current transient after stress at V_{DSQ}=50V, V_{GSQ}=-5V for varying dislocation density (cm^{-2}), or drain-buffer short.

3.3 Drain current transient spectroscopy

A commonly used procedure for reliability analysis of GaN HEMTs is drain current transient (DCT) analysis, where the on-state drain current is measured as a function of time following an off-state stress,. The transient is usually modelled by a superposition of

exponential responses and each response is then associated with a different trap with sign, activation energy and capture cross-section used to identify the trap[40]. This analysis is based on classical deep-level transient spectroscopy (DLTS) analysis where the trap emission results in a change in depletion charge, and implicitly relies on a majority carrier ohmic contact to the edge of the depletion layer. In the power switching HEMT, the buffer is semi-insulating and separated from the 2DEG by P-N diodes, so charging and discharging of depletion charge can be dominated by the transport to and from the depletion layer rather than by the trap emission. Fig. 4 shows how the simulated DCT changes with dislocation density, with a strong dependence seen which even changes sign. If analyzed conventionally, some transients would be interpreted as showing at least 3 different trap responses, with both electron and hole traps present, whereas in reality there are only C_N acceptors and the dislocations active in the simulated device so there should not be more than two responses.

The origins of the different contributions are illustrated in Fig. 5 for the example of $10^9 cm^{-2}$ dislocations and 150V off-state stress, with the DCT shown in the inset. At 10^{-3}s after stress the resulting positive and negative charged regions of Fig. 5d lead to the built-in potential distribution shown in Fig. 5a, with primarily a vertical field within the GaN:C layer. This leads to the vertical hole current indicated by the red arrows in Fig. 5d, and the band-to-band leakage indicated by the black arrows. After 1s (Fig. 5b,e), the positive charged region has been almost completely neutralized leaving a negatively charged region associated with each field plate edge and explaining the response with time constant of ~0.5s in the inset of Fig. 5. The localized nature of the negative charges now results in a lateral component to the field which drives a lateral hole current which spreads the negative charge across the entire length of the device as can be seen at 100s (Fig. 5c,f). This spreading of the charge results in the small drop in current seen in the Fig. inset between 1 and 10s. Finally the remaining negative charge leaks away through the dislocations to the 2DEG leading to the ~100s response, and explaining the strong time constant dependence on dislocation density seen in this part of the DCT in Fig. 4. Hence a 0.5s and a 10s response is predicted from exactly the same deep C_N level – the two time constants arise because there are two different paths by which transport can occur to and from the location of the traps. Complex DCT responses have been observed experimentally[41] which correspond closely to the family of curves seen in Fig. 4, demonstrating that this effect occurs in practice. Changing the hole

capture cross-section of the C_N acceptor has little effect on the 0.5s response until it drops well below $10^{-16}cm^2$ (not shown), because the generation/recombination process for holes is less significant than the resistive transport between traps. The key message here is that multiple time constant responses can arise due to geometric effects in devices wherever the rate limiting step is the transport to the trapping location. Simply measuring an Arrhenius plot and extracting activation energy or its capture cross-section is not necessarily sufficient to identify a trap unless you have a sufficiently low resistance contact to the depletion region containing the trap. In GaN-on-Si power devices, such as those discussed here, this criterion is clearly not met.

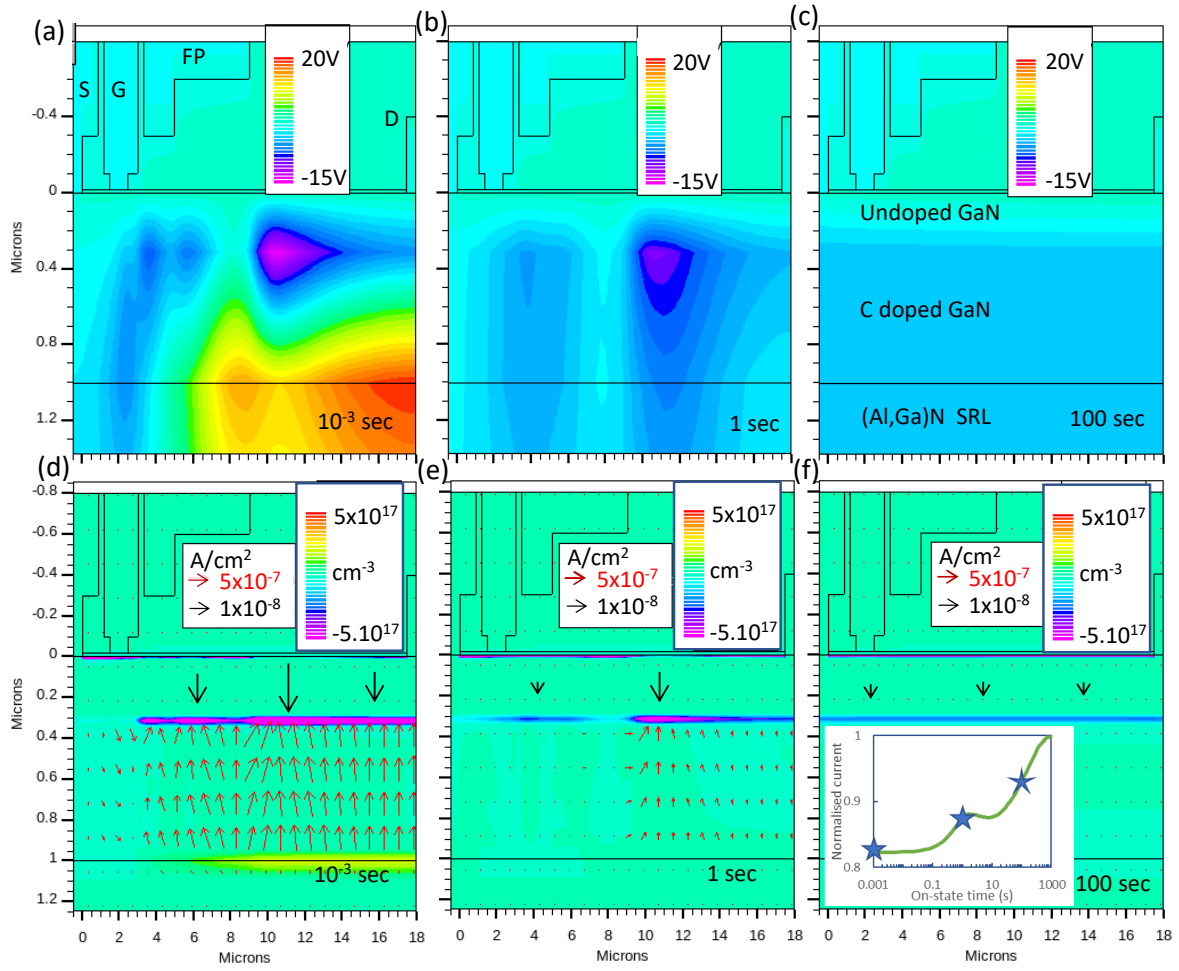

Figure 5. Time dependence of (a, b, c) potential and (d, e, f) net charge density with V_{DS}=1V, V_{GS}=0V at (a, d) 10^{-3}s, (b, e) 1s and (c, f) 100s after voltage stress of V_{DSQ}=150V, V_{GSQ}=-5V. Nominal dislocation density 10^9cm^{-2}. For (d-f) the overlaid red arrows show the hole current flow direction and density (length of arrow) within the GaN:C layer. The black arrows show the band-to-band current density in the UID GaN channel region. The inset shows the normalized current transient and the stars the timings corresponding to the contour

plots.

4. Fe doped GaN-on-SiC HEMTs

4.1 Carbon Background in Fe doped GaN

Iron has been used as a deep acceptor to suppress punchthrough[42, 43] and short channel effects in RF power devices and when combined with field plates has delivered record output power[44, 45]. However it has also been associated with DC-RF dispersion, and current collapse[46]. Fe has an energy level 0.5-0.7eV below the conduction band and a strong memory effect during growth so there is always an exponentially decaying tail to the doping distribution[47, 48]. Here we are principally concerned with the impact of the background of carbon inevitably incorporated during MOCVD growth. It was first pointed out in Ref. [7] that small amounts of C_N can neutralize the Fe acceptors provided the C_N density exceeds the density of any background donors. This is actually a very likely circumstance. However the density of Fe and C is rarely reported, and the impact of a known density of C on device performance has only been discussed in Refs. [49, 50] where 0.25μm gate length devices were fabricated on two wafers with different C density (the secondary ion mass spectrometry - data for Fe and C are replotted in Fig. 6). The key experimental observations in those publications were:

- C density did not impact the DC IV characteristics significantly.
- At higher C density there was a strong kink effect.
- Higher C density led to significant current collapse and dynamic R_{ON} in pulse IV (PIV) measurements, but the RF power and efficiency at class AB were unaffected.
- Drain transient measurements showed three different time constants, one linked to Fe and two to C.
- For high C density, off-state drain bias led to an increase in drain resistance, but surprisingly a decrease in source resistance.

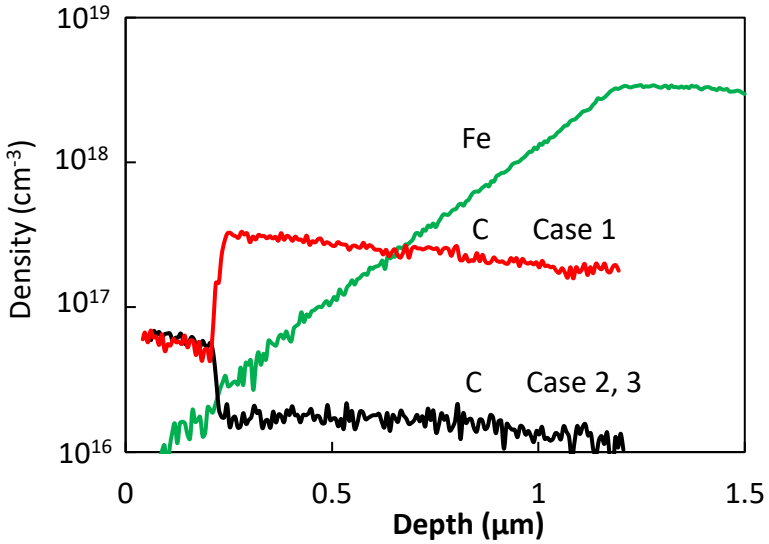

Figure 6. SIMS data for Fe and C for the two different growth recipes used to fabricate devices in [49, 50]. Case 1 to 3 correspond to the simulated structures of Table I.

In order to explain these results, simulations were originally undertaken in Ref. [49] which assumed that the background C_N could result in a floating p-type buffer region, and as for the earlier GaN-on-Si simulations, leakage was represented by a short between the drain and the p-type buffer. Here we go beyond that model and include a distributed band-to-band leakage path along the entire gate-drain region[13]. The device geometry was a simple T-gate and corresponds to those used in the experiments of [49-51] with L_{SD} 3.75µm, L_G 0.25µm. Threshold voltage was about −2V. The AlGaN barrier was 22nm thick, the Fe doped GaN was 1.8µm thick on an insulating SiC substrate.

For consistency with Ref. [49], and since the background donor density and the proportion of the carbon residing on Ga or N sites are unknown we consider three different cases in the simulation as detailed in Table 1. First considering Cases 2 and 3 which correspond to the low C wafer shown in Fig. 6, two situations are possible: either the background donor density is greater than the C_N density resulting in a n-type buffer (Case 3), corresponding to what would normally be assumed for the effect of Fe doping, or alternatively in Case 2, the donor density is less than the C_N density and the buffer becomes p-type. On the other hand, Case 1 corresponds to the high C concentration wafer ($3x10^{17}cm^{-3}$ in Fig. 6) and is assumed to be p-type since the C density far exceeds any likely intrinsic or extrinsic donor density. A concentration of $3x10^{17}cm^{-3}$ is fairly representative of commercial epitaxy; SIMS data for a

Cree Fe doped wafer reported in [52] showed a C density of $10^{17}cm^{-3}$ in the bulk. In all three cases the top 200nm channel region of the GaN was doped $3x10^{16}cm^{-3}$ with C_N and $2x10^{16}cm^{-3}$ donors. The band-to-band hopping region was set to correspond to the channel region, providing a resistive path between the 2DEG and the top of the main part of the buffer 0.2µm below the surface.

	Case 1 High C, C_N>donor	**Case 2 Low C, C_N>donor**	**Case 3 Low C, C_N<donor**
	P-type	**P-type**	**N-type**
Fe acceptor E_C-0.7eV	$7x10^{15}$ increasing exponentially with depth to $3x10^{18}cm^{-3}$ at 1.1µm		
C acceptor E_V+0.75eV	$2x10^{17}$ cm^{-3}	$1.5x10^{16}cm^{-3}$	$1.5x10^{16}$ cm^{-3}
Donor E_C-0.03eV	$1x10^{17}$ cm^{-3}	$0.5x10^{16}$ cm^{-3}	$2.5x10^{16}$ cm^{-3}

Table 1. Simulated dopant density in the bulk of the GaN.

The impact of the C on the band diagram and equivalent circuit for the device is shown in Fig. 7. For Case 3, the Fermi level is close to the Fe level, the buffer is n-type, and the equivalent circuit for the buffer is resistive (Fig. 7a,b). However for Cases 1 and 2, except close to the surface, the Fe acceptor level is above E_F and is hence neutral taking very little part in the operation of the device. It is primarily the C_N acceptors that provide the buffer charge, resulting in a P-N junction between the 2DEG and result in the diode elements shown in Fig. 7d. One significant difference from the power switching epitaxy is the C density typically is much lower in RF epitaxy, and hence it is far less capable of pinning the Fermi level, meaning that depletion regions can be wide and significant charge densities can arise within the bulk of the buffer rather than just at the surfaces.

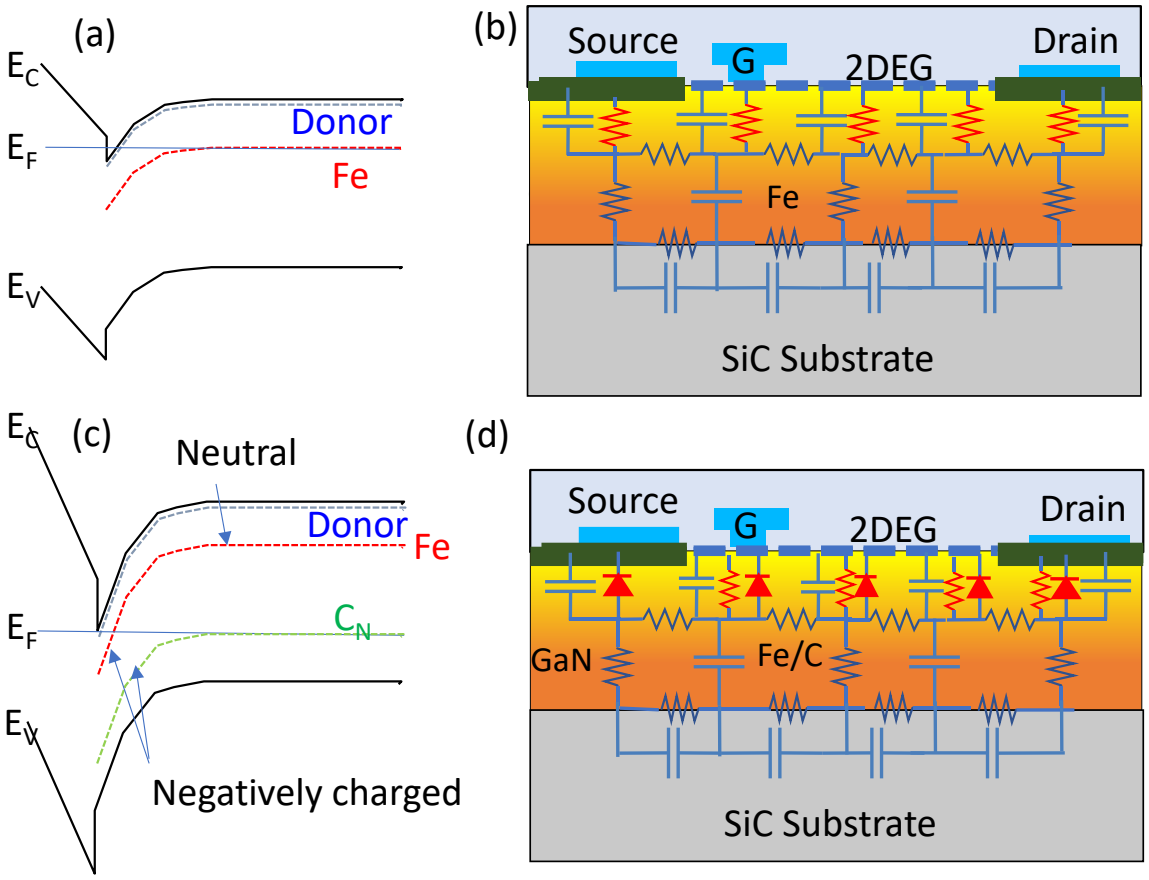

Figure 7. (a) Schematic band diagram for case 3 (C_N density less than donor density), and (b) corresponding equivalent circuit. (c) Schematic band diagram for cases 1 and 2 (C_N density greater than donor density) and (d) equivalent circuit.

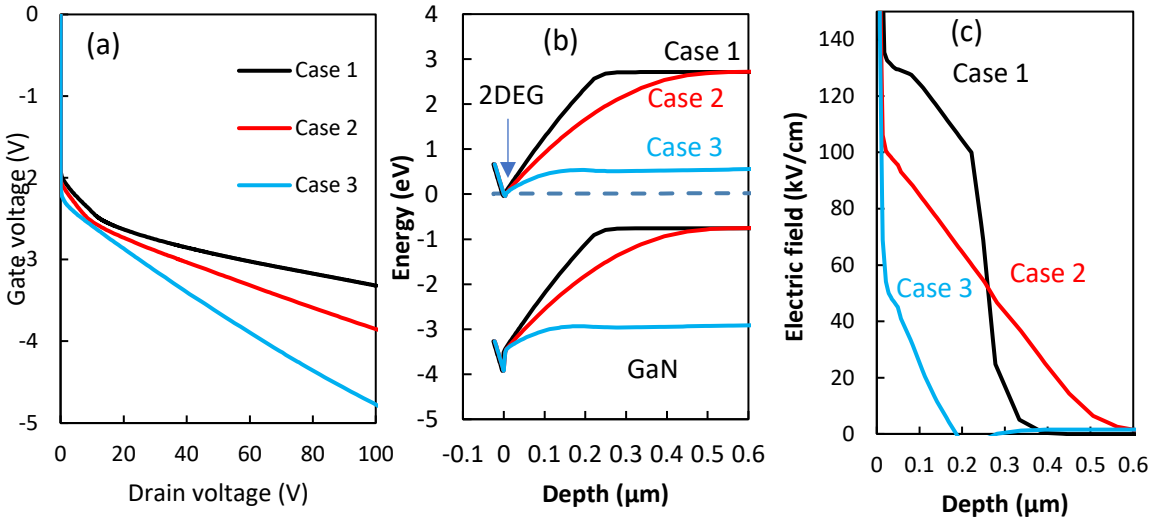

Figure 8. (a) Simulated 3-terminal breakdown measurement at constant I_D=100μA/mm as V_{GS} is swept from 0 to −5V. (b) Y-direction band diagrams and (c) electric field at V_{GS}=V_{DS}=0V.

4.2 Breakdown behaviour

The simulated impact of these doping distributions on the off-state breakdown due to punch-through in the buffer[42] are shown in Fig. 8a, which shows the drain voltage required to force a constant drain current of 100μA/mm as the gate is swept from 0 to -5V. It can be seen that the n-type Case 3 shows much worse behaviour than the p-type Cases 1 and 2. The reason is quite straightforward since the p-type buffer has a larger built-in potential and hence higher confining electric field as seen in Fig. 8b,c. This simulation only includes the effect of the buffer doping, so in reality the effect of C doping density may differ since it is often dominated by Schottky contact, crystal defects and passivation.

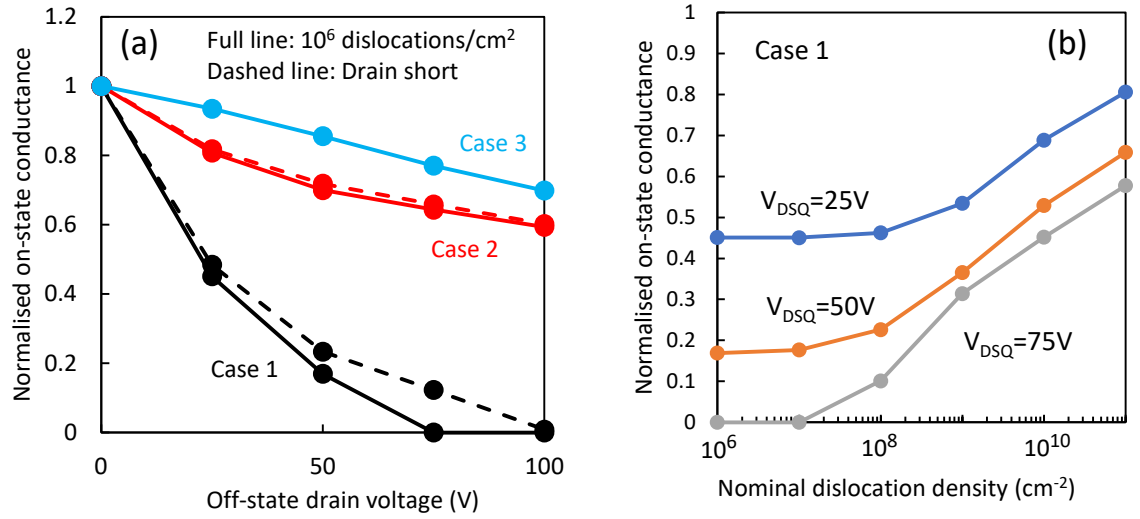

Figure 9. (a) Impact of off-state V_{DS} on normalised on-state conductance for Cases 1, 2, 3, either with a nominal $10^6 cm^{-2}$ (solid line) or with a short under the drain (dashed line). (b) For Case 1, impact of varying dislocation density on on-state conductance.

4.3 On-state conductance

Let us now consider the impact of off-state bias stress on on-state conductance (inverse dynamic R_{ON}) as shown in Fig. 9. Fig. 9a shows the situation where there is very low dislocation density and hence little band-to-band leakage. It is immediately apparent that the high C Case 1 is far more vulnerable to off-state stress showing complete pinch-off at only 75V V_{DSQ}, whereas by contrast the low C Cases 2 and 3 both show a much smaller dependence with a slightly larger effect in the p-type Case 2. Interestingly, having a short under the drain has almost no effect on the simulated result and it is the doping that determines the vulnerability to stress. Adding additional leakage through the P-N diode for Case 1 by increasing the dislocation density (Fig. 9b) results in the gradual suppression of the on-state conductance degradation.

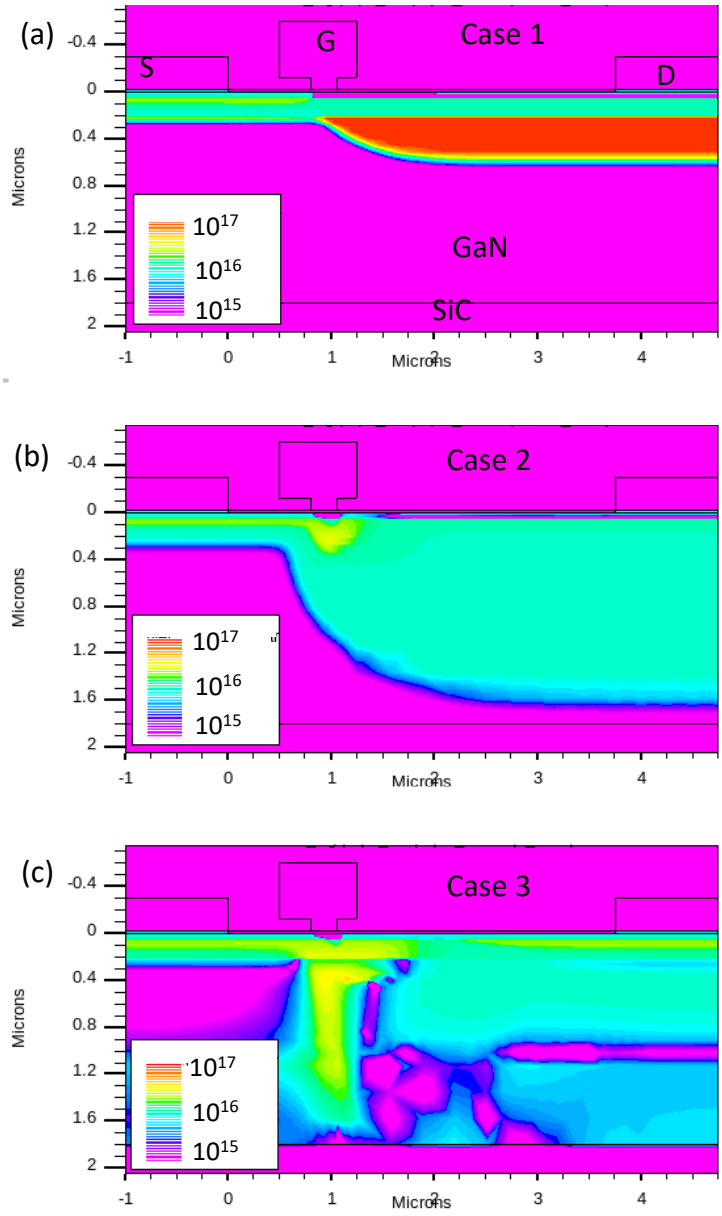

Figure 10. Net charge density (log contour scale from 10^{15} to 10^{17}cm^{-3}) in the quiescent state at V_{DSQ}=25V, V_{GSQ}=-3V for (a) Case 1, (b) Case 2 and (c) Case 3. Dislocation density is 10^{8}cm^{-2} for (a), (b).

The mechanisms are illustrated in Fig. 10 and Fig. 11 which show net charge density stored at 25V in off-state. Fig. 10 shows the situation for a low dislocation density of 10^{8}cm^{-2}. For Cases 1 and 2, the reverse biased diode under the drain results in a depletion region with 10^{17}cm^{-3} or 10^{16}cm^{-3} ionized charge, respectively, under the entire gate-drain gap. This depletion charge reduces the 2DEG density, reduces the drain conductance G_D and increases on-state conductance G_{ON}. For Case 2 the total depletion charge is much lower than for Case 1 and so its effect on G_{ON} is much smaller. For Case 2 and Case 3, ionized Fe of density of

a few times 10^{16}cm^{-3} can be seen as the yellow region under the gate. This charged region under the gate is essentially a geometrical electrostatic effect and arises as described in Refs. [7, 53] due to the lateral electric field between the gate and the 2DEG during off-state bias. Charges on the output capacitor are positive on the drain side and due to exposed polarization charge, and negative on the gate side and due to ionized acceptors under the gate as well as negative charge on the gate. For Cases 2 and 3, the required charge density under the gate exceeds the C_N density so Fe is ionized, whereas for Case 1 this charge can be almost entirely accommodated by ionization of C. It is this negative charge under the gate which is responsible for most of the fall in G_{ON} seen for Cases 2 and 3 in Fig. 9a.

When there is significant leakage through the P-N diode, the result is that there is a resistive voltage drop in the semi-insulating GaN buffer, which reduces the voltage drop across the P-N diode. This effect is shown in Fig. 11 for Case 1 with 10^{11}cm^{-2} dislocations. The result is a thinning of the depletion region compared to Fig. 10a, a reduction in the negative charge in the gate-drain depletion region and hence an improvement in on-state conductance as seen in Fig. 9b.

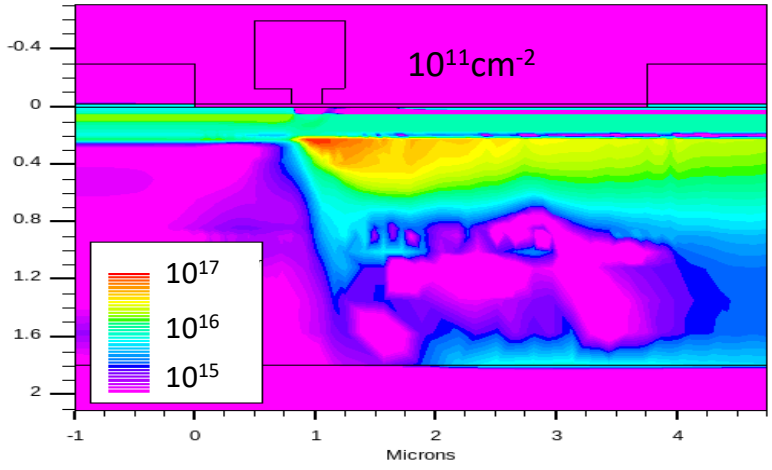

Figure 11. Net charge density (cm^{-3}) for Case 1 with conditions as in Figure 10a, but with dislocation density of 10^{11}cm^{-2}.

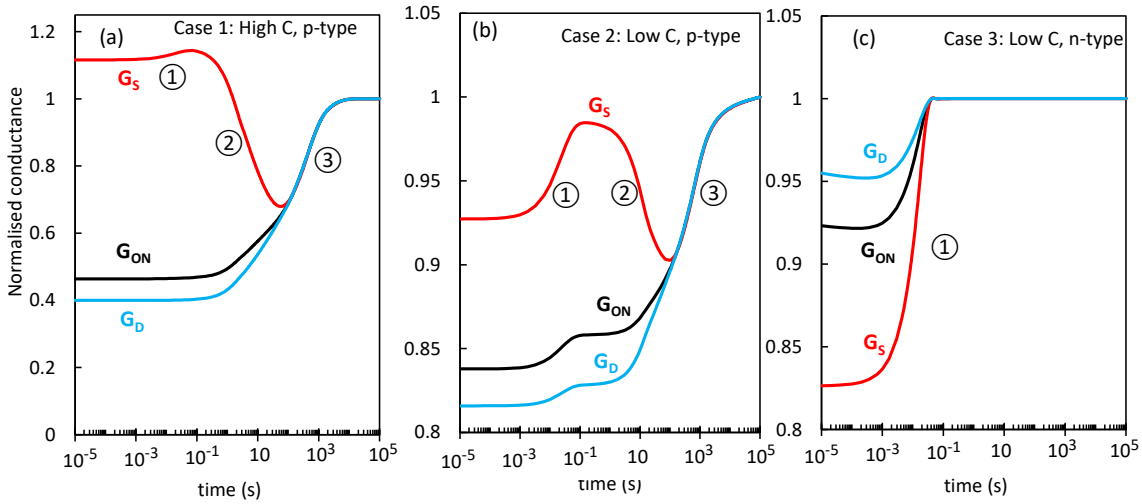

Figure 12. Drain transient simulations for Cases 1 to 3 showing G_{ON}, G_S and G_D normalised to the value at 10^5s. Here $1/G_{ON}=1/G_S+1/G_D$. Dislocation density is 10^8cm^{-2} for Cases 1, 2. Quiescent condition is V_{DSQ}=25V, V_{GSQ}=−3V and transient starts after a 10ns ramp to V_{DS}=1V, V_{GS}=0V.

4.4 Drain current transients

Fig. 12 shows an example simulated DCT for a relatively low nominal dislocation density of 10^8cm^{-2} and with off-state drain stress of 25V. Here the conductance contributions from the source (G_S) and drain (G_D) side of the gate have been plotted as well as the overall G_{ON} where ($1/G_{ON}=1/G_S+1/G_D$). The simulation for the n-type Case 3 showed a single time constant response characteristic of emission of electrons from Fe acceptors, however the p-type Case 1 and 2 showed complex responses which can be fitted with three different time constants as indicated by ①, ②, and ③. The presence of three responses is at first sight surprising since there are only two traps which are changing their occupation in the simulation. However, as for the power devices, two of the responses arise due to the transport path to and from the same C_N acceptors. The mechanism can be explained with the help of Fig. 13 which shows the net charge density for Case 2 at various times after V_{DSQ}=25V stress. After 1μs, a wide depletion region of ionized C_N is present under the gate and extending under the drain contact. Also present under the gate is the small region of ionized Fe discussed in the previous section. After 0.1s, the Fe has become neutral by emission of electrons and resulting in response ①. Over the next 100s, the p-type buffer is effectively isolated from the 2DEG and so emission of holes from the C_N acceptors provides the free holes which flow laterally driven by the field from the stored depletion charge. This spreads the depletion charge across the entire device, and decreases G_S and increases G_D in process

②. At long times, the small leakage by band-to-band hopping allows the stored charge in the buffer to leak away to the 2DEG resulting in process ③. As for the power devices, charge redistribution within the floating buffer caused by background carbon can result in two time constants from a single trap and can explain some of the DCT complexity seen in Ref [49]. We note that measurements in Ref. [49] have shown that G_S actually temporarily increased immediately following drain stress for the high carbon doped wafer, entirely consistent with the simulation in Fig. 12a. This arises because the depletion region under the source is actually thinner during stress than at equilibrium for Case 1 as a result of forward biasing of the P-N junction by the small hole flow from the dislocation leakage, thus reducing G_S (not shown).

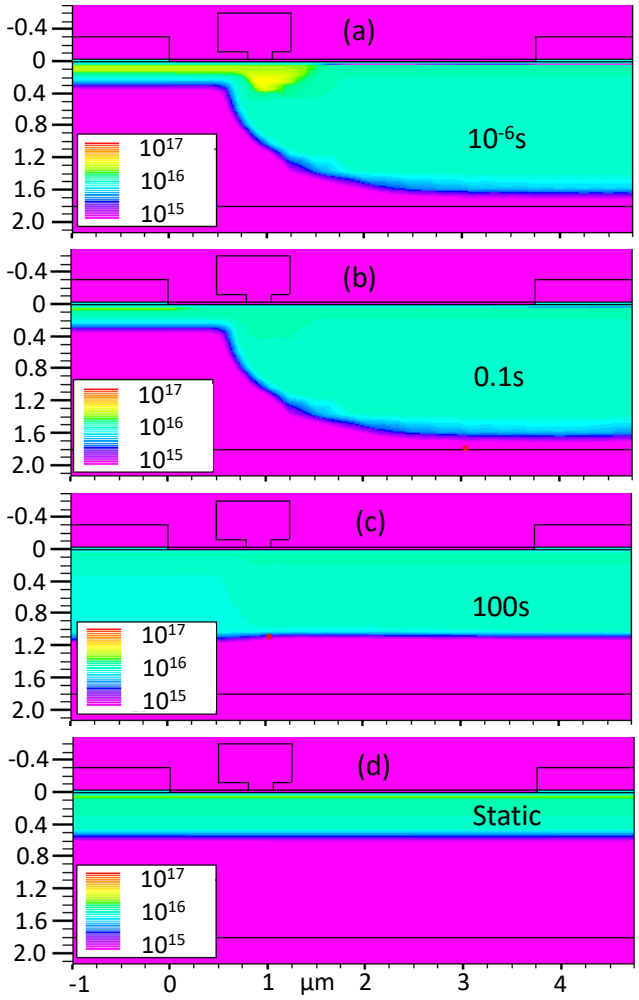

Figure 13. Net charge density (log contour scale from 10^{15} to 10^{17}cm^{-3}) during transient for Case 2 following a quiescent bias of V_{DSQ}=25V, V_{GSQ}=-3V with V_{DS}=1V, V_{GS}=0V. (a) 10^{-6}s, (b) 10^{-1}s, (c) 100s, (d) infinity. Dislocation density is 10^{8}cm^{-2}.

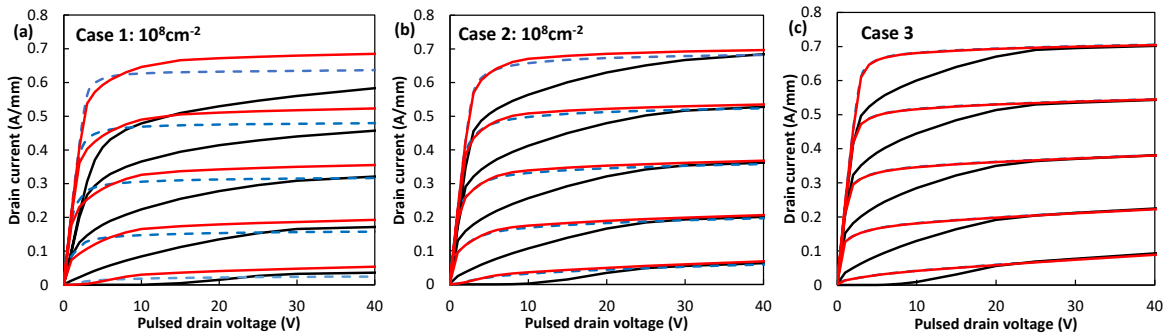

Figure 14. Pulse and DC IV simulations. V_{GS}=-2 to 0V in 0.5V steps. Blue dashed lines are DC (static) IV. Red lines are pulsed from quiescent points of V_{DSQ}=0V, V_{GSQ}=-3V and black lines from V_{DSQ}=25V, V_{GSQ}=-3V and are 1μs after pulsing from the quiescent point. (a) Case 1 dislocation density 10^8cm^{-2}. (b) Case 2 dislocation density 10^8cm^{-2}. (c) Case 3.

4.5 Pulsed current-voltage measurements

Pulsed IV (PIV) is a standard technique for the assessment of RF HEMTs and can be simulated by undertaking a set of transient simulations (here 75 per plot) from a quiescent bias point V_{DSQ}, V_{GSQ} to each V_{DS}, V_{GS} on the IV plane, and extracting the current after 1μs[7]. The results are shown in Fig. 14 for Cases 1, 2 and 3. For all cases, the DC IV curves are similar to the PIV when V_{DSQ}=V_{GSQ}=0V, i.e., there is essentially no charge stored during the quiescent bias. However when pulsed from off-state with V_{DSQ}=25V, there is a large decrease in G_{ON} seen below the knee for Case 1, and a pulsed drain bias dependent fall in the conductance in the saturation regime compared to the DC case, a current-collapse. The magnitude of this current-collapse is very similar for the low carbon Cases 2 and 3, but is significantly larger for the high C Case 1 at V_{GS} of 0V. The current-collapse for pulsed gate bias close to threshold is largely the result of a shift in threshold voltage which gets larger the bigger the negative pulse voltage step. This is illustrated in Fig. 15 which shows the shift in threshold voltage V_T for two different values of V_{DSQ}, and demonstrates that the shift is essentially independent of the buffer doping. As discussed earlier, this shift in V_T is essentially a geometric effect and results from the back-gating capacitive coupling between the 2DEG near the drain and the 2DEG under the gate caused by the negative step in voltage on the drain terminal[7, 53]. It arises because for negative steps the trapped charge cannot respond on the timescale of the pulse. For positive voltage steps, the P-N diode is forward biased and so electrons are rapidly injected into the buffer suppressing and screening the

effect faster than the μs timescale of the PIV measurement.

For Case 1, Fig. 16 shows the PIV at V_{GS}=0V for varying V_{DSQ}. It is entirely consistent with the on-state conductance measurements of Fig. 9a, showing a decrease in G_{ON} and a drop in saturation current as V_{DSQ} increases due to the impact of the increasing depletion charge in the drain access region.

In Ref [50], it was shown that although the higher C density wafer showed stronger current-collapse than the low C wafer when measured by PIV, there was little difference in the saturated RF output power at 1GHz under DC or pulsed conditions. No satisfactory explanation could be found at that time, however Fig. 9b provides the basis for a possible model[13]. We note that under PIV conditions the duty cycle was only 0.1% and a soft-switching mode was employed (ie the drain is switched before the gate so there was never a high current at high drain bias). By contrast, in a class AB RF mode the device loadline will always pass through the high-current, high bias regime and hence there will be impact ionization generating a hole current. This may well be sufficient to suppress the voltage drop across the depletion region as in Fig. 11 and suppress the current-collapse. This suggestion requires further study.

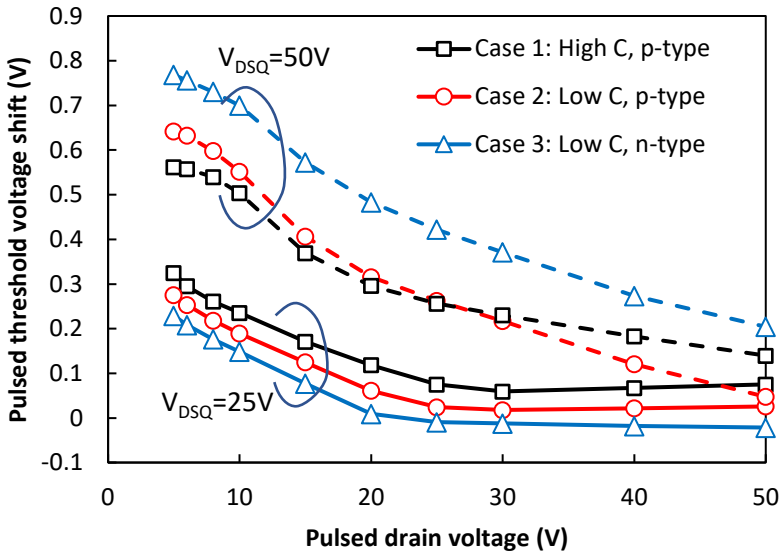

Figure 15. Difference between threshold voltages as a function of pulsed drain voltage for quiescent voltages of V_{DSQ}=0V and V_{DSQ}=25V or 50V all with V_{GSQ}=-3V. Solid lines are for V_{DSQ}=25V and dashed lines are for V_{DSQ}=50V. V_T was extracted from PIV curves by fitting a spline curve to $I_D(V_{GS})$ and taking V_T as the V_{GS} where I_D=50mA/mm. Dislocation density 10^8cm^{-2}.

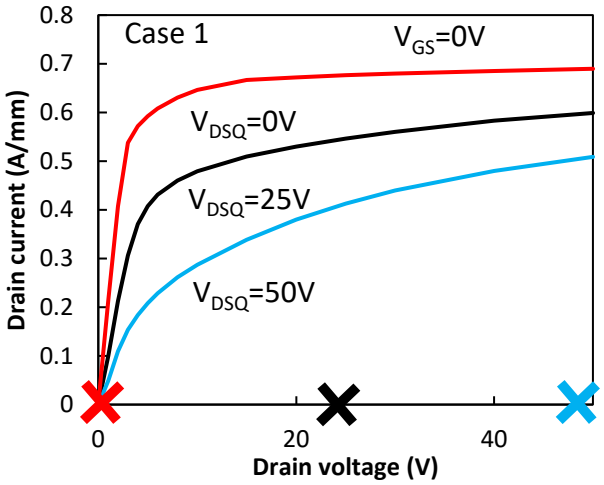

Figure 16. Pulse IV for V_{GS}=0V from V_{DSQ}=0V (red), 25V (black), and 50V (blue) for Case 1 with 10^8cm^{-2} dislocation density.

4.6 Kink effect

The kink effect is a widely observed instability in RF devices which takes the form of a hysteresis that is only observed at low drain bias and for slow ramps of the drain bias. It also is only observed after the first up-sweep ie it requires a sweep to a high drain bias before trapping can occur. It is normally ascribed to deep level traps with unusual bias dependent characteristics[54-56], however it was shown in Ref. [49] that a floating buffer can also explain the kink effect. In that paper the simulation used a shorting contact between the drain and the buffer, however here we improve on that model by including dislocation leakage, resulting in a much more convincing simulation. The result is shown in Fig. 17 for the three doping cases considered here, and reproduces the drain bias sweep experiment which produces kink, here using 0.01V/s voltage sweeps. For the initial up-sweep from 0V with V_{GS}=0V, there is no charge stored and so the IV shows no current-collapse, whereas for subsequent up-sweeps, there will be a stored charge primarily under the gate, but also in the gate-drain region, which will reduce the current by shifting V_T and to some extent decrease G_{ON}. During the slow up-sweep, the charge recovers and eventually results in the suppression of the kink. For the down-sweep, the sweep is sufficiently slow for the charge to remain in quasi-equilibrium and there is no significant current-collapse in the knee region. As expected, for Case 3 on the slow timescale of the measurement, the Fe traps can respond and there is no hysteresis. However for both Case 1 and 2 there is a significant hysteretic kink effect

predicted, with the relative magnitude of the effect determined by the proportion of the charge under the gate residing in C_N rather than Fe acceptors.

There are two interesting features of this model. First it predicts a small kink effect should be present even for a relatively low C density provided the buffer is p-type. Second, the model predicts a linear increase in current below the kink representing a constant time constant for the charge recovery. In reality the time constant for the recovery is non-linear and decreases rapidly with increasing V_{DS}. The linear increase is an artefact of the implemented model for dislocation leakage which assumes an ohmic process, whereas it is experimentally found to be strongly non-ohmic[8]. Implementing such a non-ohmic dislocation path in the simulation would lead to much improved agreement with experiment.

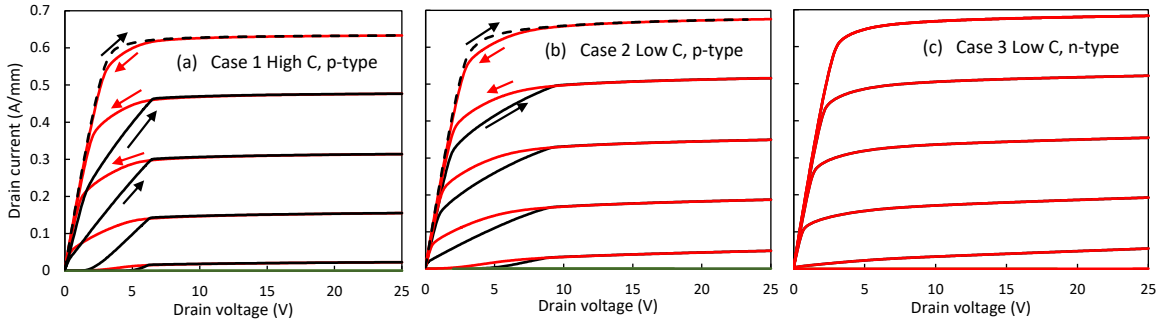

Figure 17. Simulation of kink effect for (a) Case 1, (b) Case 2, (c) Case 3. Sweep rate is 0.01V/s. V_{GS}=0 to −2.5V in -0.5V steps and dislocation density is 10^8cm^{-2}. Black dashed line is initial sweep from V_{DS}=0 to 25V. Black line is up-sweep from V_{DS}=0 to 25V, but immediately after 10ns ramp to 0V from quiescent state at V_{DS}=25V. Red lines are for down-sweep from quiescent point at V_{DS}=25 to 0V.

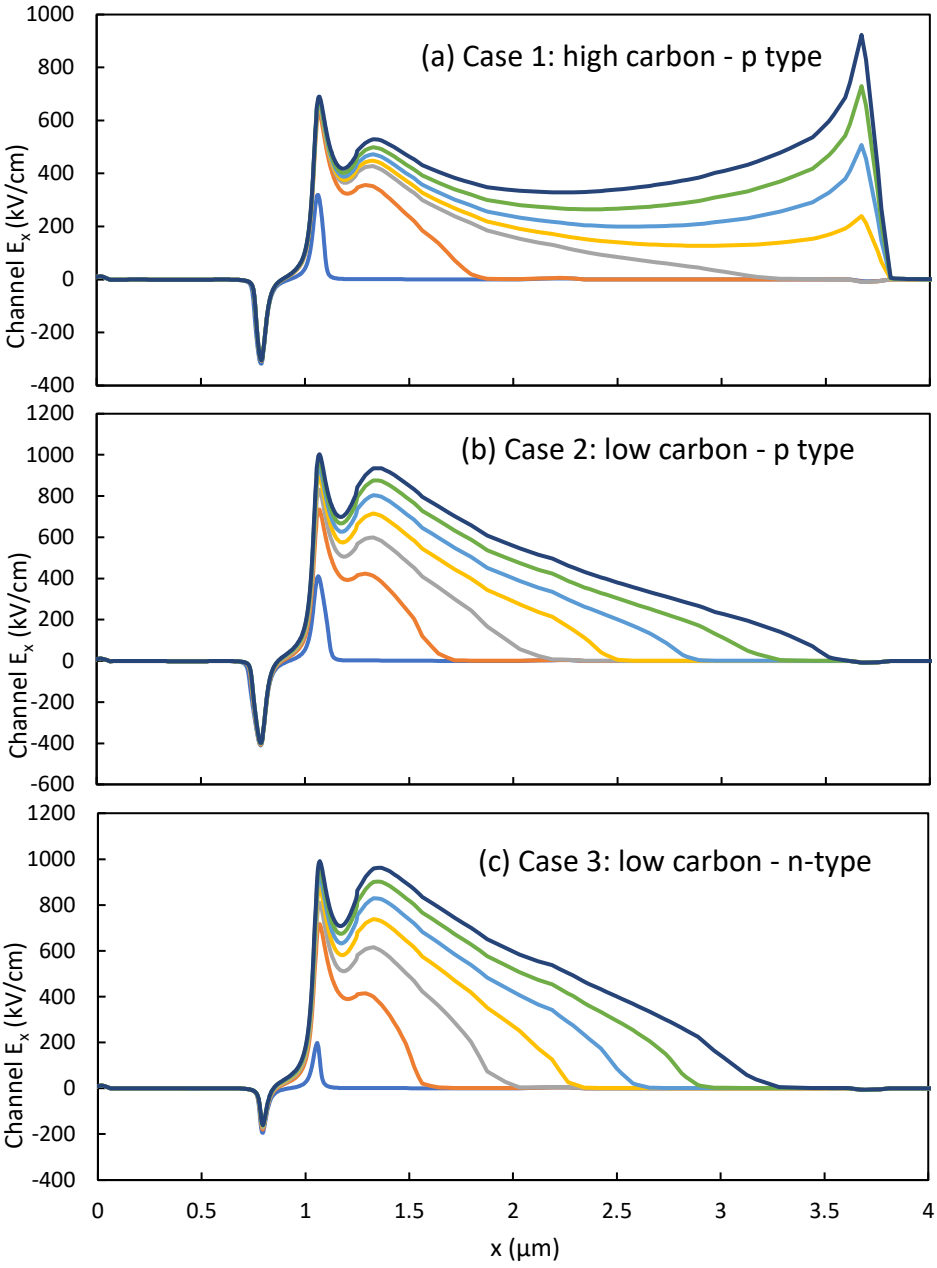

Figure 18. Simulated x-component of the electric field in the 2DEG for V_{DS}=20V to 120V in 20V steps in off-state with V_{GS}=-3V. The dislocation density is 10^8cm^{-2}. (a) Case 1, (b) Case 2, (c) Case 3.

4.7 Impact on channel electric field

The floating p-type buffer has been predicted to result in a reduction in the channel electric field for GaN-on-Si devices where the drain is shorted to the substrate[18]. This arises by a so-called RESURF effect, where the 2DEG charge is matched by the charge stored in the buffer resulting in an extension of the depletion region at the gate edge towards the drain. Here we show that a related effect can arise in a high C doped device as a result of the back-

biasing effect of the buffer.

Fig. 18 shows the channel electric field as the drain bias is increased in 20V steps. Cases 2 and 3, where the C_N density is low, show a gradual extension of the depletion region towards the drain with a peak field at the gate edge which continues to increase with bias. However for Case 1, the high C_N density starts to result in full pinch-off of the 2DEG for bias greater than about 80V. This then allows the field to be distributed across the entire gate-drain gap, leading to an increase in the voltage dropped at the drain edge.

Remarkably, exactly these electric field distributions have been observed in an optically based experiment based on electric field induced second harmonic generation[51]. All the features seen in Fig. 18 are reproduced, including the difference between high and low C density, the reduction in peak field in the high C device, and the transfer of the high field peak from gate edge to the drain at high bias. This provides strong support for the model presented here.

5. Key mechanisms

The approach discussed in this paper to analyzing the dynamics of GaN HEMTs is remarkably successful in explaining a wide range of different trap related buffer instabilities. It relies on an understanding of the key features of the structures, including the presence of blocking layers, the acceptors and their compensating donors, leakage along dislocations, and transport within the semi-insulating GaN layer. All these features are required to understand the device behaviour. Fig. 19 summarizes the four different low-field mechanisms discussed here for changes in depletion charge that result in bias stress induced change in on-state conductance G_{ON}. Processes (a), (c), (d)) apply to the RF GaN-on-SiC devices and (b), (c), (d) to the GaN-on-Si power switching HEMTs.

(a) This involves conventional emission of electrons from Fe acceptors located directly below the 2DEG. This process would be assessable using DLTS/DCT spectroscopy approaches, however the magnitude of the response can be strongly reduced if there is a significant density of C present.

(b) Vertical charge redistribution between the top and bottom of the isolated GaN:C layer, with transport being dominated by free holes, leakage along dislocations, or bulk 3D hopping depending on C_N density and the specifics of the epitaxy.

(c) Lateral charge redistribution within the isolated GaN:C layer, with transport being either by free holes in the bulk, free holes at the lower heterojunction (a 2DHG), or by bulk 3D hopping.

(d) Neutralization of excess ionized C_N acceptors by a band-to-band process involving hopping along dislocations between the 2DEG and the bulk GaN. Here there are likely to be barriers between the 2DEG and the dislocation and perhaps the dislocation and the bulk acceptors.

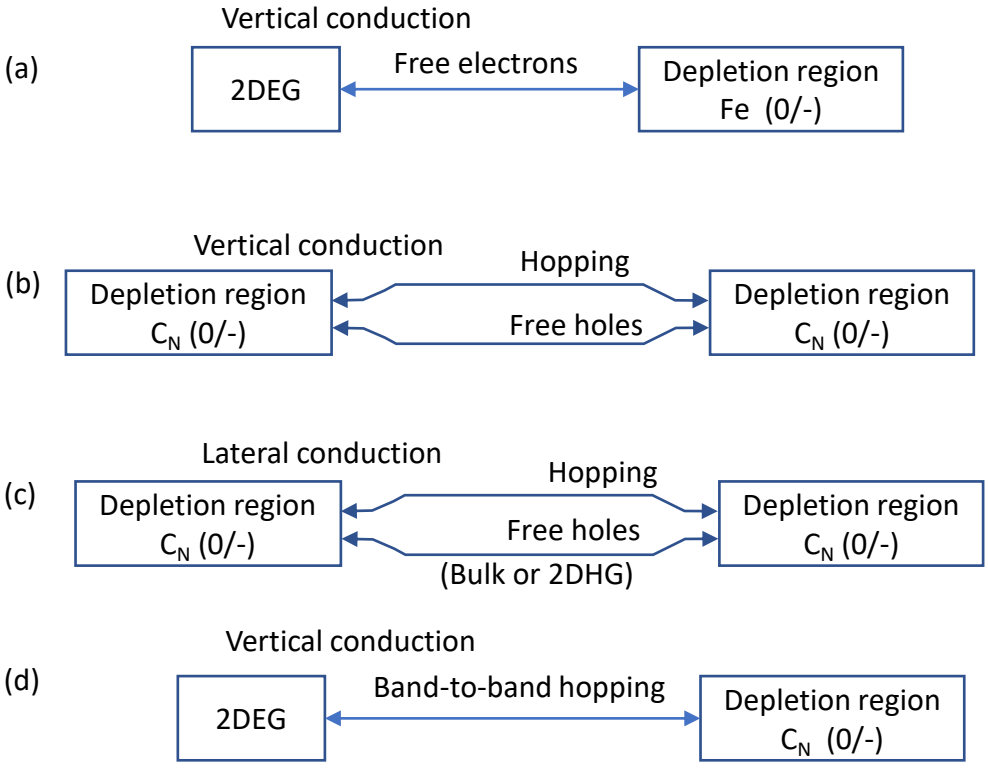

Figure 19. Mechanisms leading to bias stress induced drain conductance change (dynamic R_{ON}). (b,c,d) apply to the GaN-on-Si power switches and (a,c,d) to the Fe doped GaN-on-SiC HEMTs.

In the simulation presented here only a minimum subset of mechanisms has been incorporated in order to demonstrate the principles by which the device dynamics may occur. Bulk 3D hopping, 2DHG conduction at buried heterojunctions, barriers between the dislocation and the 2DEG are all excluded, and would be required to provide a full quantitative model of the time dependence of the dynamics. However, the magnitude of the effects are largely dictated by the electrostatics of the device and so they should be

reasonably quantitative. Nevertheless, to determine an accurate electrostatic model requires a detailed knowledge of the relative densities of acceptors and donors, and this is still very poorly known to date, especially for the GaN-on-SiC RF devices, so further experimental input is required to build a fully quantitative device model.

6. Conclusions

Buffer trap related instabilities are a serious issue for all GaN HEMT devices. Dynamic R_{ON} and current-collapse degrade switch efficiency, and impact RF power capability and efficiency as well as affecting more subtle issues such as those related to basestation linearization. A detailed understanding leading to minimization, suppression and control is required for full uptake into applications ranging from power switching through to RF systems. In this review, we have shown how a simulation methodology based on an understanding of the device structure, the details of the key dopants and background impurities, and the transport mechanisms, can explain a wide range of different experimental observations including dynamic changes in on-state conductance (dynamic R_{ON}), pulse IV, current-collapse, kink effect and electric field redistribution within the gate-drain gap. A key point is that especially for high carbon density, it is the transport within the structure to and from depletion regions where charge accumulates that is the rate limiting step which controls the dynamics rather than trap capture/emission. The acceptor trap density is also generally far higher than the density required by electrostatics to explain the trapped charge, so suppression and control is not concerned with minimizing trap density, rather optimization is achieved by management of the device geometry and by careful control of transport and leakage paths. It is clear that in 650V power switching devices, there needs to be an emphasis on controlling all the leakage paths, especially through the undoped region directly below the 2DEG. For Fe doped RF GaN HEMTs, the background carbon density is a crucial parameter together with the background donor density, and should be measured and included in any model of bulk trap related instabilities.

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References

1) K.J. Chen, O. Häberlen, A. Lidow, C.l. Tsai, T. Ueda, Y. Uemoto and Y. Wu: IEEE Trans. Elec. Dev. **64** [3](2017)779.
2) S.C. Binari, P.B. Klein and T.E. Kazior: Proc. IEEE. **90** [6](2002)1048.
3) S. Karboyan, M.J. Uren, M. Singh, J.W. Pomeroy and M. Kuball: Microelectronics Reliability. **81** (2018)306.
4) M.J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee and M. Kuball: IEEE Trans. Elec. Dev. **64** [7](2017)2826.
5) B. Rackauskas, M.J. Uren, S. Stoffels, M. Zhao, S. Decoutere and M. Kuball: IEEE Trans. Elec. Dev. **65** [5](2018)1838.
6) M. Silvestri, M.J. Uren and M. Kuball: Appl. Phys. Lett. **102** [7](2013)073501.
7) M.J. Uren, J. Möreke and M. Kuball: IEEE Trans. Elec. Dev. **59** [12](2012)3327.
8) F. Wach, M.J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball: IEEE Elec. Dev. Lett. **41** [12](2020)1754.
9) R.S. Pengelly, S.M. Wood, J.W. Milligan, S.T. Sheppard and W.L. Pribble: IEEE Transactions on Microwave Theory and Techniques. **60** [6](2012)1764.
10) J.L. Lyons, A. Janotti and C.G. Van de Walle: Phys. Rev. B. **89** [3](2014)035204.
11) M.J. Uren, D. Herbert, T. Martin, B.T. Hughes, J. Birbeck, R. Balmer, A.J. Pidduck and S.K. Jones: Physica Status Solidi (A) Applied Research. **188** [1](2001)195.
12) M.J. Uren, S. Dalcanale, F. Yang, A. Nejim, S.P. Wilson and M. Kuball: CS-MANTECH, 2020, p. 253.
13) M.J. Uren and M. Kuball: IEEE BCICTS, 2020, p. 3B.1.
14) M.J. Uren and M. Kuball: Ext. Abstr. Solid State Devices and Materials, 2020, p. 277.

15) M.J. Uren, M. Silvestri, M. Cäsar, G.A.M. Hurkx, J.A. Croon, J. Šonský and M. Kuball: IEEE Elec. Dev. Lett. **35** [3](2014)327.

16) M.J. Uren, M. Cäsar, M.A. Gajda and M. Kuball: Appl. Phys. Lett. **104** [26](2014)263505.

17) M.J. Uren, M. Silvestri, M. Cäsar, J.W. Pomeroy, G.A.M. Hurkx, J.A. Croon, J. Šonský and M. Kuball: CS-MANTECH, 2014, p. 317.

18) M.J. Uren, M. Caesar, S. Karboyan, P. Moens, P. Vanmeerbeek and M. Kuball: IEEE Elec. Dev. Lett. **36** [8](2015)826.

19) H. Cordes, S.D. Baranovskii, K. Kohary, P. Thomas, S. Yamasaki, F. Hensel and J.H. Wendorff: Phys. Rev. B. **63** [9](2001)094201.

20) V. Moroz, H.Y. Wong, M. Choi, N. Braga, R.V. Mickevicius, Y. Zhang and T. Palacios: ECS J. Sol. State Sci. Tech. **5** [4](2016)P3142.

21) S. Dalcanale, M.J. Uren and M. Kuball: Silvaco Standard. **28** (2018)7.

22) I. Chatterjee, M.J. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee and M. Kuball: IEEE Trans. Elec. Dev. **64** [3](2017)977.

23) M. Singh, S. Karboyan, M.J. Uren, K.B. Lee, Z. Zaidi, P.A. Houston and M. Kuball: Microelectronics Reliability. **95** (2019)81.

24) R. Piotrzkowski, M. Zajac, E. Litwin-Staszewska and M. Bockowski: Appl. Phys. Lett. **117** [1](2020)012106.

25) N.F. Mott and E.A. Davis: *Electronic Processes in Non-Crystalline Materials* (Oxford University Press, 2012).

26) C. Koller, G. Pobegen, C. Ostermaier and D. Pogany: IEEE Trans. Elec. Dev. **65** [12](2018)5314.

27) M. Meneghini, A. Tazzoli, G. Mura, G. Meneghesso and E. Zanoni: IEEE Trans. Elec. Dev. **57** [1](2010)108.

28) Q.F. Shan, D.S. Meyaard, Q. Dai, J. Cho, E.F. Schubert, J.K. Son and C. Sone: Appl. Phys. Lett. **99** [25](2011)253506.

29) X.A. Cao, J.A. Teetsov, F. Shahedipour-Sandvik and S.D. Arthur: J. Crystal Growth. **264** [1–3](2004)172.

30) B. Rackauskas, S. Dalcanale, M.J. Uren, T. Kachi and M. Kuball: Appl. Phys. Lett. **112** [23](2018)233501.

31) J.R. Jameson, P.B. Griffin, J.D. Plummer and Y. Nishi: IEEE Trans. Elec. Dev. **53** [8](2006)1858.

32) JEDEC: JEP173 Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices, Version 1.0. **JEP173** (2019)

33) P. Moens, M.J. Uren, A. Banerjee, M. Meneghini, B. Padmanabhan, W. Jeon, S. Karboyan, M. Kuball, G. Meneghesso, E. Zanoni and M. Tack: ISPSD, 2017, p. 97.

34) A. Stockman, A. Tajalli, M. Meneghini, M.J. Uren, S. Mouhoubi, S. Gerardin, M. Bagatin, A. Paccagnella, G. Meneghesso, E. Zanoni, P. Moens and B. Bakeroot: IEEE Trans. Elec. Dev. **66** [1](2019)372.

35) W.M. Waller, M. Gajda, S. Pandey, J.J.T.M. Donkers, D. Calton, J. Croon, J. Šonský, M.J. Uren and M. Kuball: IEEE Trans. Elec. Dev. **64** [10](2017)4044.

36) F. Yang, S. Dalcanale, M. Gajda, S. Karboyan, M.J. Uren and M. Kuball: IEEE Trans. Elec. Dev. **67** [3](2020)869.

37) M. Meneghini, A. Tajalli, P. Moens, A. Banerjee, E. Zanoni and G. Meneghesso: Materials Science in Semiconductor Processing. **78** (2018)118.

38) X. Tang, B. Li, Y. Lu, H. Wang, C. Liu, J. Wei and K.J. Chen: IEDM, 2015, p. 35.3.1.

39) S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, H. Okita, T. Morita, K. Tanaka, M. Hikita, Y. Uemoto, S. Takahashi and T. Ueda: ISPSD, 2015, p. 41.

40) D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso and E. Zanoni: IEEE Trans. Elec. Dev. **60** [10](2013)3166.

41) P. Moens, A. Banerjee, A. Constant, P. Coppens, M. Caesar, Z. Li, S. Vandeweghe, F. Declercq, B. Padmanabhan, W. Jeon, J. Guo, A. Salih, M. Tack, M. Meneghini, S. Dalcanale, A. Tajilli, G. Meneghesso, E. Zanoni, M.J. Uren, I. Chatterjee, S. Karboyan and M. Kuball: ECS Transactions. **72** [4](2016)65.

42) M.J. Uren, K.J. Nash, R.S. Balmer, T. Martin, E. Morvan, N. Caillas, S.L. Delage, D. Ducatteau, B. Grimbert and J.C. De Jaeger: IEEE Trans. Elec. Dev. **53** [2](2006)395.

43) M.J. Uren, D.G. Hayes, R.S. Balmer, D.J. Wallis, K.P. Hilton, J.O. Maclean, T. Martin, C. Roff, P. McGovern, J. Benedikt and P.J. Tasker: European Microwave Integrated Circuits Conference, 2006, p. 65.

44) Y.F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder,

U.K. Mishra and P. Parikh: IEEE Elec. Dev. Lett. **25** [3](2004)117.

45) Y.F. Wu, M. Moore, A. Saxler, T. Wisleder and P. Parikh: IEEE Device Research Conference Digest. (2006)151.

46) O. Axelsson, S. Gustafsson, H. Hjelmgren, N. Rorsman, H. Blanck, J. Splettstoesser, J. Thorpe, T. Roedle and M. Thorsell: IEEE Trans. Elec. Dev. **63** [1](2016)326.

47) R.S. Balmer, D.E.J. Soley, A.J. Simons, J.D. Mace, L. Koker, P.O. Jackson, D.J. Wallis, M.J. Uren and T. Martin: Phys. Stat. Sol. (c). **3** [6](2006)1429.

48) S. Heikman, S. Keller, T. Mates, S.P. DenBaars and U.K. Mishra: J. Crystal Growth. **248** (2003)513.

49) M. Singh, M.J. Uren, T. Martin, S. Karboyan, H. Chandrasekar and M. Kuball: IEEE Trans. Elec. Dev. **65** [9](2018)3746.

50) H. Hirshy, M. Singh, M.A. Casbon, R.M. Perks, M.J. Uren, T. Martin, M. Kuball and P.J. Tasker: IEEE Trans. Elec. Dev. **65** [12](2018)5307.

51) Y. Cao, J.W. Pomeroy, M.J. Uren, F. Yang and M. Kuball: Submitted for publication. (2020).

52) K.R. Bagnall, E.A. Moore, S.C. Badescu, L. Zhang and E.N. Wang: Review of Scientific Instruments. **88** [11](2017)113111.

53) D.C. Tripathi, M.J. Uren and D. Ritter: IEEE Trans. Elec. Dev. **67** [12](2020)5460.

54) G. Meneghesso, F. Zanon, M.J. Uren and E. Zanoni: IEEE Elec. Dev. Lett. **30** [2](2009)100.

55) G. Meneghesso, F. Rossi, G. Salviati, M.J. Uren, E. Munoz and E. Zanoni: Appl. Phys. Lett. **96** [26](2010)263512.

56) M.J. Wang and K.J. Chen: IEEE Elec. Dev. Lett. **32** [4](2011)482.

Figure Captions

Figure 1. Schematic cross-section of a 650V GaN-on-Si power HEMT showing an overlaid equivalent circuit for transport within the device.

Figure 2. (a) ON-state conductance ie inverse dynamic R_{ON} for two different 30A, 650V GaN

HEMTs replotted from Ref. [3]. (b) Simulated inverse dynamic R_{ON} as a function of off-state stress for varying dislocation density. (c) Net charge density with V_{DS}=1V, V_{GS}=0V 1μs following off-state stress at V_{DSQ}=300V, V_{GSQ}=-5V with 10^8cm^{-2} dislocations and 25ºC.

Figure 3. Off-state drain leakage current with V_{GSQ}=-5V for varying dislocation density (cm^{-2}), or a short between the drain and the p-type buffer. The noise on some curves is the result of slow convergence in the simulation.

Figure 4. Drain current transient after stress at V_{DSQ}=50V, V_{GSQ}=-5V for varying dislocation density (cm^{-2}), or drain-buffer short.

Figure 5. Time dependence of (a, b, c) potential and (d, e, f) net charge density with V_{DS}=1V, V_{GS}=0V at (a, d) 10^{-3}s, (b, e) 1s and (c, f) 100s after voltage stress of V_{DSQ}=150V, V_{GSQ}=-5V. Nominal dislocation density 10^9cm^{-2}. For (d-f) the overlaid red arrows show the hole current flow direction and density (length of arrow) within the GaN:C layer. The black arrows show the band-to-band current density in the UID GaN channel region. The inset shows the normalized current transient and the stars the timings corresponding to the contour plots.

Figure 6. SIMS data for Fe and C for the two different growth recipes used to fabricate devices in [49, 50].

Figure 7. (a) Schematic band diagram for case 3 (C_N density less than donor density), and (b) corresponding equivalent circuit. (c) Schematic band diagram for cases 1 and 2 (C_N density greater than donor density) and (d) equivalent circuit.

Figure 8. (a) Simulated 3-terminal breakdown measurement at constant I_D=100μA as V_{GS} is swept from 0 to −5V. (b) Y-direction band diagrams and (c) electric field at V_{GS}=V_{DS}=0V.

Figure 9. (a) Impact of off-state V_{DS} on normalised on-state conductance for Cases 1, 2, 3, either with a nominal 10^6cm^{-2} (solid line) or with a short under the drain (dashed line). (b) For Case 1, impact of varying dislocation density on on-state conductance.

Figure 10. Net charge density (log contour scale from 10^{15} to 10^{17}cm^{-3}) in the quiescent state at V_{DSQ}=25V, V_{GSQ}=-3V for (a) Case 1, (b) Case 2 and (c) Case 3. Dislocation density is 10^8cm^{-2} for (a), (b).

Figure 11. Net charge density (cm^{-3}) for Case 1 with conditions as in Figure 10a, but with dislocation density of 10^{11}cm^{-2}.

Figure 12. Drain transient simulations for Cases 1 to 3 showing G_{ON}, G_S and G_D normalised to the value at 10^5s. Here $1/G_{ON}=1/G_S+1/G_D$. Dislocation density is 10^8cm^{-2} for Cases 1, 2.

Quiescent condition is V_{DSQ}=25V, V_{GSQ}=-3V and transient starts after a 10ns ramp to V_{DS}=1V, V_{GS}=0V.

Figure 13. Net charge density (log contour scale from 10^{15} to 10^{17}cm^{-3}) during transient for Case 2 following a quiescent bias of V_{DSQ}=25V, V_{GSQ}=-3V with V_{DS}=1V, V_{GS}=0V. (a) 10^{-6}s, (b) 10^{-1}s, (c) 100s, (d) infinity. Dislocation density is 10^{8}cm^{-2}.

Figure 14. Pulse and DC IV simulations. V_{GS}=-2 to 0V in 0.5V steps. Blue dashed lines are DC (static) IV. Red lines are pulsed from quiescent points of V_{DSQ}=0V, V_{GSQ}=-3V and black lines from V_{DSQ}=25V, V_{GSQ}=-3V and are 1μs after pulsing from the quiescent point. (a) Case 1 dislocation density 10^{8}cm^{-2}. (b) Case 2 dislocation density 10^{8}cm^{-2}. (c) Case 3.

Figure 15. Difference between threshold voltages as a function of pulsed drain voltage for quiescent voltages of V_{DSQ}=0V and V_{DSQ}=25V or 50V all with V_{GSQ}=-3V. Solid lines are for V_{DSQ}=25V and dashed lines are for V_{DSQ}=50V. VT was extracted from PIV curves by fitting a spline curve to $I_D(V_{GS})$ and taking V_T as the V_{GS} where I_D=50mA/mm. Dislocation density 10^{8}cm^{-2}.

Figure 16. Pulse IV for V_{GS}=0V from V_{DSQ}=0V (red), 25V (black), and 50V (blue) for Case 1 with 10^{8}cm^{-2} dislocation density.

Figure 17. Simulation of kink effect for (a) Case 1, (b) Case 2, (c) Case 3. Sweep rate is 0.01V/s. V_{GS}=0 to −2.5V in -0.5V steps and dislocation density is 10^{8}cm^{-2}. Black dashed line is initial sweep from V_{DS}=0 to 25V. Black line is up-sweep from V_{DS}=0 to 25V, but immediately after 10ns ramp to 0V from quiescent state at V_{DS}=25V. Red lines are for down-sweep from quiescent point at V_{DS}=25 to 0V.

Figure 18. Simulated x-component of the electric field in the 2DEG for V_{DS}=20V to 120V in 20V steps in off-state with V_{GS}=-3V. The dislocation density is 10^{8}cm^{-2}. (a) Case 1, (b) Case 2, (c) Case 3.

Figure 19. Mechanisms leading to bias stress induced drain conductance change (dynamic R_{ON}). (b,c,d) apply to the GaN-on-Si power switches and (a,c,d) to the Fe doped GaN-on-SiC HEMTs.