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The ATLAS Fast TracKer system

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The ATLAS Fast TracKer system

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ABSTRACT: The ATLAS Fast TracKer (FTK) was designed to provide full tracking for the ATLAS high-level trigger by using pattern recognition based on Associative Memory (AM) chips and fitting in high-speed field programmable gate arrays. The tracks found by the FTK are based on inputs from all modules of the pixel and silicon microstrip trackers. The as-built FTK system and components are described, as is the online software used to control them while running in the ATLAS data acquisition system. Also described is the simulation of the FTK hardware and the optimization of the AM pattern banks. An optimization for long-lived particles with large impact parameter values is included. A test of the FTK system with the data playback facility that allowed the FTK to be commissioned during the shutdown between Run 2 and Run 3 of the LHC is reported. The resulting tracks from part of the FTK system covering a limited η–ϕ region of the detector are compared with the output from the FTK simulation. It is shown that FTK performance is in good agreement with the simulation.

Contents

1   Introduction

The Fast TracKer (FTK) system [1] was foreseen as an evolution of the ATLAS experiment's [2] trigger strategy, designed to bring the tracking of charged particles into trigger decisions at the earliest possible stage in the trigger algorithms. The ATLAS trigger [3, 4] was originally designed around initial signatures based on energy deposits in the ATLAS calorimeters and the tracking of

muons in the muon spectrometer (MS), which surrounds the calorimeters. In Runs 1–3 of the Large Hadron Collider (LHC) the ATLAS first-level (L1) trigger system uses hardware-based algorithms to reduce the 40 MHz rate from the beam-crossings to approximately 100 kHz, which can then be processed in the high-level trigger (HLT) to reduce the rate by another factor of 50 or more before recording events. In 2018, for example, the average event-recording rate was 1200 Hz [5]. Initially, in Run 1, the commodity-computing-based HLT was designed with a first step to process small areas around each of the L1 trigger objects. Within these regions-of-interest (RoIs), software-based tracking occurred as late as possible in the trigger algorithms to minimize the use of HLT resources. In many cases, the RoI approach led to significant inefficiencies, for example in jet finding, because of differences between the online and offline strategies [6, 7]. In addition, the instantaneous luminosity of the LHC increased to 2×10^{34} cm^{-2}s^{-1} and the number of overlapping collisions, pile-up, frequently exceeded 50, leading to large inefficiencies. The FTK was designed to mitigate this by using custom hardware to provide tracks to the HLT at the full L1 trigger rate for events with up to 80 pile-up collisions.

By reconstructing all charged particles in an event with transverse momentum (p_T) down to 1 GeV with good efficiency, it is possible to use algorithms such as particle flow [8] to accurately separate the energy deposited in the target event from that of the pile-up interactions. Such techniques for pile-up mitigation are especially important for final states that require jets to be reconstructed and in events with signatures involving missing transverse momentum (E_T^{miss}) [9]. Examples of areas where ATLAS triggers would benefit from full tracking down to low p_T include di-Higgs production with decays to the four-b-quark final state [10] (tracks are also used to tag jets containing b-hadrons) and exotic [11] and/or supersymmetry [12] signatures involving E_T^{miss}. In addition, full reconstruction of charged tracks in an event, such as the FTK provides, allows for opportunistic use of these tracks in other signatures, e.g. B-physics, outside of RoIs or in other future scenarios.

The following sections present the as-built FTK system, along with the simulation and control software that was used for system commissioning at the end of Run 2 data-taking and during Long Shutdown 2 (LS2) before the project was stopped in 2019. The FTK system will not be used during Run 3. Contributors to this decision were the lower than expected pile-up due to cryogenic limits of the LHC [13], significant gains from optimization of the HLT software-tracking algorithm, and potential resource shortages. Instead, it is envisioned to perform more tracking in the HLT for signatures that benefit the most, e.g. jets and E_T^{miss}.

A comparison of the performance of the hardware with simulation is presented. The paper is organized as follows: an overview of the FTK system is described in section 2; the components of the FTK hardware, including those used for the comparison, are described in more detail in section 3; the online software as well as FTK control and monitoring are described in section 4; the FTK configuration, its optimization using simulation and its performance in a vertical slice, a minimal set of electronics boards to process tracks, are described in section 5; and section 6 contains the conclusion.

2 FTK system overview

The FTK system was developed to provide tracking of charged particles over the full acceptance of the ATLAS inner detector at the full L1 trigger rate of 100 kHz. It was designed to provide

tracking information to the HLT, which operates asynchronously from the LHC clock. Tracking information from the FTK was provided to the HLT and the ATLAS data acquisition system [14] in the same manner as is used for detector readout. These systems do not require a fixed latency. The FTK uses four layers of hits from the silicon pixel (Pixel) system (including the insertable B-layer (IBL) [15, 16] installed in 2015) and eight layers of hits from the four stereo pairs in the silicon microstrip (SCT) system for a total of twelve layers. The inner detector is surrounded by a thin superconducting solenoid providing a 2 T axial magnetic field; it covers the pseudorapidity range $|\eta| < 2.5$ and full range in azimuthal angle ϕ.[1] Tracks in ATLAS are defined by five helix-parameters (d_0, z_0, q/p_T, η, and ϕ), where d_0 and z_0 are the transverse and longitudinal impact parameters respectively. Track quality can be assessed with a χ^2 value from summing over the residuals of the hits and the track. The FTK system performs tracking in two steps. First, initial track candidates are found by using pattern recognition with eight layers of hits. Second, four additional layers of hits are added to the track and the track helix parameters are evaluated. The FTK system does not perform minimizations to fit tracks; instead, it evaluates a system of linear equations to perform a linearized track reconstruction.

Challenges faced by the FTK system include handling, processing, buffering and synchronizing a high bandwidth of data on multiple parallel data paths (towers) in a large heterogeneous system with many interconnects; input hit organization across towers requiring duplication and sharing through multiple interconnects; creating, loading, and validating a large amount of configuration data for the pattern matching and track fitting; and managing and monitoring a large number of high-power-density electronics boards requiring active cooling.

At the core of the FTK is the content-addressable memory [17, 18], the Associative Memory (AM) [19] that performs the initial pattern recognition and forms candidate tracks to be processed further. The FTK AM is an ASIC specifically designed for the FTK system using a 65 nm CMOS technology. It is used to associate the data hits from the tracking detectors with stored patterns. The AM patterns use up to eight layers of hits (three Pixel and five SCT), which are binned with a variable granularity in the azimuthal angle and pseudorapidity. The AM layers were chosen to provide candidate tracks with a sufficient purity to allow downstream processing. The candidate tracks (roads) found by the AM pass a χ^2 selection before proceeding to second-stage processing that extrapolates them to the innermost Pixel layer (the IBL) and to the three additional SCT layers. Figure 1 illustrates the track-finding algorithm used in the FTK, with more details described at the end of this section, after an overview of the FTK system components

The stages of processing in the FTK, clustering, data transport and sharing, pattern matching, and evaluations of track parameters in two stages, are summarized in table 1. These functions are spread across several electronics boards.

The Input Mezzanines (IMs), 128 cards mounted on the Data Formatter (DF) modules, have a total of 512 inputs. The IM cards cluster the hits from the Pixel and SCT sensors. The DF system, which consists of 32 ATCA [20] boards, routes the packets of hits corresponding to individual Pixel

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[1]ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upwards. Cylindrical coordinates (r, ϕ) are used in the transverse plane, ϕ being the azimuthal angle around the z-axis. The pseudorapidity is defined in terms of the polar angle θ as $\eta = -\ln\tan(\theta/2)$. Angular distance is measured in units of $\Delta R \equiv \sqrt{(\Delta\eta)^2 + (\Delta\phi)^2}$.
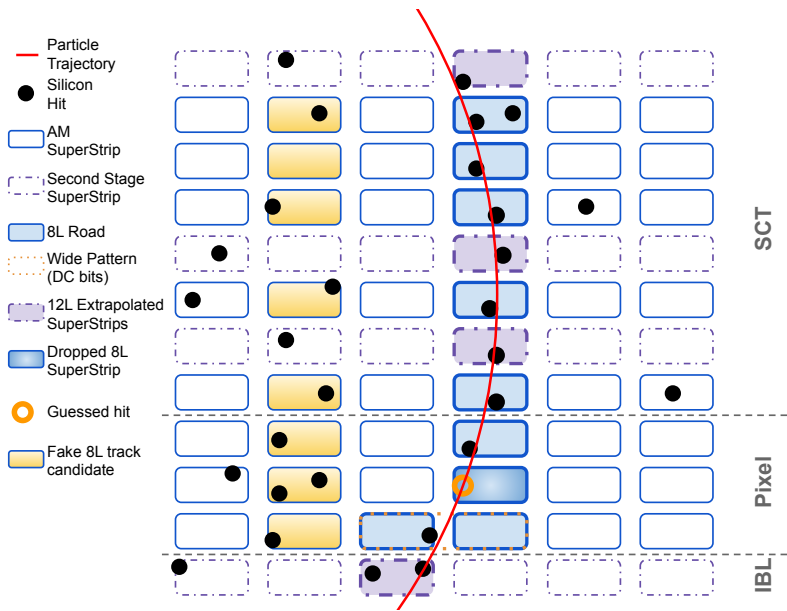
Figure 1. Diagram of the track-finding method used in the FTK. Rounded boxes represent the coarse resolution SuperStrips used to bin the hits from the silicon detectors. Once eight layers (Associative Memory (AM) SuperStrips) with hits match a stored pattern they become a road (solid filled boxes), which is then extrapolated into the remaining four layers (dash-dot filled boxes). One layer may be dropped in the first eight layers used for pattern matching and another in the additional four layers. Fake track candidates (e.g. the gradient-filled boxes to the left) can be rejected because they have a large χ^2 value or fail extrapolation to the additional four layers.

Table 1. Overview of the FTK system in the order in which the data are processed. The AUX appears in the table twice because of its dual functions. The table shows the system as envisioned for Run 3 of the LHC where a direct connection of the SSB to the ATLAS Readout System (ROS) was foreseen. In this case, the FTK-to-High-Level-Trigger Interface Card (FLIC) would not be used.

	Module	Function	Type	Number
IM	Input Mezzanine	Cluster Pixel and SCT hits, format module data	Mezzanine	128
DF	Data Formatter	Transport and duplicate module hit data to η–ϕ towers	ATCA	32
AUX	Auxiliary Card	Transport coarse-resolution 8-layer hit data to AMB	VME	128
AMB	AM Board	Transport hit data to AM	VME	128
AM	Associative Memory	Match hits to patterns	ASIC	8192
AUX	Auxiliary Card	Evaluate track candidates in matched patterns	VME	128
SSB	Second Stage Board	Add remaining hits to 8-layer tracks, fit, remove overlaps	VME	32
FLIC	HLT Interface Board	Interface to ATLAS readout	ATCA	2

and SCT modules to an array of 4 (η) × 16 (ϕ) overlapping regions in the η–ϕ plane called towers. The DF boards duplicate the module packets as needed to allow sharing between overlapping towers. They transmit the packets across the ATCA backplane and over fibres connecting the ATCA shelves to each other. Towers overlap in order to keep the track-finding efficiency high near the boundaries.

Each of the 32 DF boards serves two of the 64 towers and sorts the module hit data by layer before transmitting them to four of the 128 Processing Units (PUs) and one of the 32 Second Stage Boards (SSBs). The system can optionally be configured with two PUs per DF. The segmentation of connectivity of these towers is illustrated in figure 2.

Each PU is composed of an Auxiliary Card (AUX) and an Associative Memory Board (AMB). The AUX receives hits from eight layers in a given tower and converts them to coarse resolution hits, or SuperStrip (SS), which are sent to the AMB to be matched against the stored patterns of SSs in the AM. The eight layers used in pattern matching are drawn in blue in figure 1. An SS is a set of silicon strips or pixels, typically 128 strips or 30 × 76 pixels in size. The strips have a typical pitch of 80 μm and the pixels are 400 × 50 μm in the outer layers, and 250 × 50 μm in the innermost layer. The matching patterns from the AMB correspond to 8-layer tracks. These 8-layer tracks are processed using linearized fits with precomputed constants and filtered by the AUX and then sent to the SSB.

In the SSB, the hits from the remaining four layers are matched to the 8-layer tracks, and tracks with up to 12 layers are formed and processed using linearized fits. Each SSB receives tracks from two adjacent towers. In addition to forming 12-layer tracks, the SSBs provide duplicate-track removal when tracks share more than an allowed number of hits.

The final tracks from the SSB are forwarded to the FTK-to-High-Level-Trigger Interface Card (FLIC), which is in turn interfaced to the ATLAS Readout System (ROS) [21]. Both the AUX and SSB are capable of connecting directly to the ROS system. In the case of the AUX, this feature was used for testing; in the case of the SSB, it would have allowed inter-SSB track-overlap removal to be offloaded to the HLT.

Using a linear system of equations in the hit coordinates allows fast computation of the track helix parameters and χ^2 values on field programmable gate arrays (FPGAs). The same underlying principle is used for both the 8-layer fit performed by the AUX and the 12-layer fit performed by the SSB. The difference is that the AUX computes the χ^2 for the 8-layer track candidate, whereas the SSB computes the same plus the helix parameters for 12-layer tracks. In both cases, one hit may be dropped, or is allowed to be missing, from the fit in order to improve efficiency, i.e. the AUX may drop a hit from its eight considered layers and the SSB may drop a hit in the additional four layers. If hits are found on every layer, the AUX and SSB each perform a nominal fit with hits on each layer and a recovery fit for each permutation of one dropped hit on their respective layers. If the nominal fit does not pass an initial χ^2 requirement, the recovery fit with the smallest χ^2 is used instead. In this case, the best expected hit position on the dropped layer is used in order to compute track parameters, represented by an orange circle as the 'guessed hit' in figure 1.

The AUX uses 8 silicon hits (5 SCT layers and 3 Pixel layers), with a total of 11 coordinates, and 5 helix parameters. Thus, there are 6 degrees of freedom, each of which gives a function of the coordinates that should equal zero. The χ^2 is the sum of the squares of those functions:

$$\chi^2 = \sum_{i=1}^{6} \left(\sum_{j=1}^{11} S_{ij} x_j + h_i \right)^2, \tag{2.1}$$

(a)

Pixel & SCT inputs | Input Mezzanines (IMs) | Data Formatters (DFs) | Processing Units (PUs) | Second Stage Boards (SSBs) | FLICs
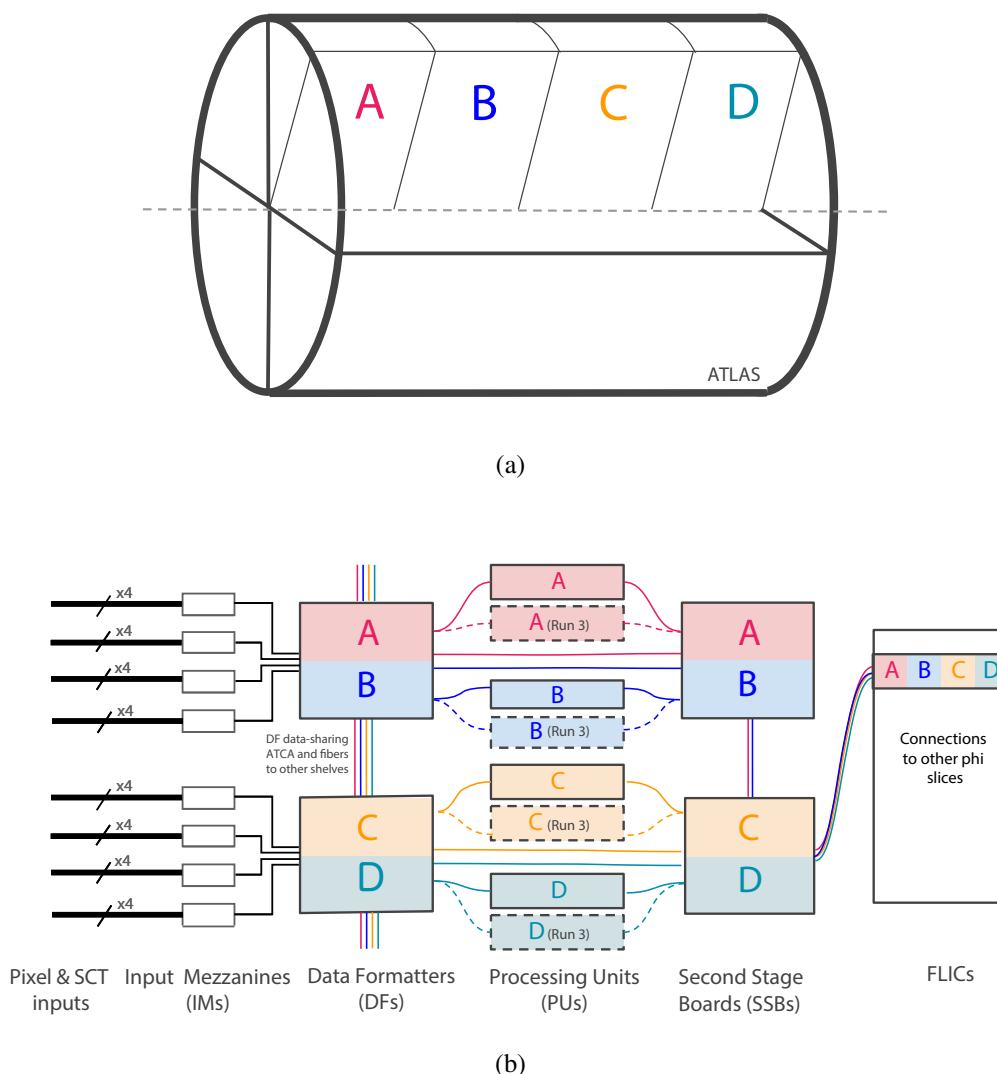
(b)

Figure 2. Figure 2(a) illustrates the tower geometry of the FTK. Two adjacent towers, adjacent in η, are serviced by a single DF board, e.g. A and B. An ATCA shelf containing eight DF boards serves a quadrant of the FTK. Figure 2(b) shows the board layout and interconnections covering one slice in ϕ of the ATLAS detector. Solid lines indicate connections used in the 64-PU configuration, and dashed lines indicate additional connections and boards used in the 128-PU configuration intended for use during Run 3. For Run 3, the SSB could optionally (not shown) connect directly to the ATLAS Readout System (ROS) and have the connection between SSBs omitted.

where x_j is a hit coordinate and S_{ij} and h_i are precalculated constants for each sector. The constants are computed per sector, a small region of the detector containing one silicon module in each layer, typically a few centimeters in size. There are on average 13 000 8-layer and 28 000 12-layer sectors per tower, which may share modules.

The SSB extrapolates the 8-layer candidate track into the additional four layers and evaluates the track with all 12 layers, giving 16 coordinates, using a method similar to that in eq. (2.1). For

the purpose of track fitting, a system of equations is built:

$$y_i = \sum_{j=1}^{16} C_{ij}x_j + q_i,$$ (2.2)

where C and q are a 16×16 matrix and 16×1 array of precalculated constants respectively, x_j is an array of the 16 hit coordinates, and $y_i = (d_0, \ldots, \phi, \chi_1, \ldots, \chi_{11})^{\mathrm{T}}$ is an array of the 5 helix parameters and 11 partial χ-values to be summed as in the previous equation. The SSB extrapolates the 8-layer tracks to the expected hit positions in the additional layers by taking eq. (2.2), dropping the helix parameter indices, assuming the χ-values to be zero, and inverting the equation to solve for the hit positions. Instead of performing all of these computations on the FPGA, separate constants are produced for extrapolation, so that this too is a linear equation, which can be evaluated quickly. Details of these procedures are described in ref. [1].

3 Hardware and firmware

The FTK infrastructure in the ATLAS underground counting room (USA15) is described in section 3.1. This is followed by a description of the data playback system, QuestNP, in section 3.2. The remaining sections, sections 3.3 to 3.9, describe the individual FTK components (previously summarized in table 1): IM, DF, AUX, AMB, AM, SSB, and FLIC.

A common feature of the firmware for all components in the system is that it is data driven. The system was designed so that the main bandwidth limitation occurs on the input links from the Pixel and SCT systems. Each stage of the processing has both input and output buffers. In case the input buffers are in danger of overflowing, it is possible for each component in the system to ask the previous component to pause data transmission by asserting back pressure. Back pressure is asserted using the XOFF feature of the S-LINK [22, 23], a signal sent to the upstream transceiver, or dedicated signal lines.

In much of the system, data can be processed without regard to event synchronization. There are various places where data are buffered until the relevant information for a given event is available: at the input of the DF where data are received from the on-board IMs; at the output of the DF before complete data from individual layers are sent to the AUX and SSB; at the output of the AUX where data are merged from multiple FPGAs; at the input of the SSB where data are received from the AUX and DF; and at the output of the SSB where data from two adjacent towers are combined before being sent to the FLIC or ROS. These synchronizations use the packet structure of the data, specifically an event identifier in the header (packet metadata before the payload).

The firmware designs of the FPGAs used in the system have a shared concept of monitoring. It is based on circular buffers (spybuffers) to sample data as they flow through the system, readout of monitoring registers, and the ability to freeze these monitoring quantities in case of errors for debugging. Additionally, buffers are also used to store synchronized monitoring information and histograms of monitoring values. These blocks use a common firmware design, with some exceptions due to design requirements and FPGA chip architecture. The design of the synchronization blocks in the previous paragraph is also shared between the FTK components.

The testing and commissioning of the FTK system involved a wide array of set-ups from individual components to the full data-processing chain. Individual component testing, normally

involving an entire electronics board, made use of the ability either to self-drive the firmware with test data or to directly drive the board's input connections in a stand-alone configuration. This allowed independent commissioning without waiting for the debugging of upstream data-processing. Other tests of the complete data-processing chain and scaling up of the system were made, some of which are described later. Examples of these tests range from pairs of electronics boards to the set of electronics boards in figure 2(b), to full shelves of DFs or full crates of PUs and SSBs. Near the end of Run 2, a vertical slice of the FTK including each board needed for data-processing (a DF with four IMs, PU, SSB, and FLIC) was regularly included in ATLAS data-taking. This set of boards was used in the collection of the data analysed in section 5.7. A second slice with a PU writing directly to the readout system was also used for testing the upstream boards.

3.1 Infrastructure and interface to the Pixel and SCT detectors

The final layout of the FTK infrastructures is composed of seven racks. Four racks are dedicated to the custom VME [24] core crates hosting the pattern matching and initial fitting, i.e. the PUs. These VME crates also host the boards for the final fitting (SSBs) and their Rear Transition Modules (RTMs). The remaining three racks are used by the five ATCA shelves which host DF boards for data routing and sharing and the FLICs for the interface to the HLT. All racks are located in USA15, in two consecutive rows of three racks each and a third row containing the remaining rack.

The electronics in these seven racks are air cooled with circulation provided by turbines on top of the racks [25] and by additional custom fan trays which are used around the VME crates. As the air passes through and out of the racks, it is cooled by multiple heat-exchangers circulating chilled water.

The layout of the VME racks [26] was optimized to keep the PUs' operating temperature below 80°C, a temperature dictated by the expected lifetime of the AM ASIC. The custom fan trays were designed to minimize the temperature in the VME crates, which each consume about 6 kW. The fan tray design specifications required the usage of high-performance Sanyo-Denki fans (San Ace 9HV1248P1G001 [27]) supplied by 48 V DC. This in turn required a modification of the service voltage of the CAEN Power Supply A3488 [28]. The speed of each fan row is automatically controlled by the Detector Control System (DCS) via temperature sensors on the PUs. In this configuration, the maximum temperature of the AMBs in a fully equipped crate was measured to remain within an acceptable range [29].

The two racks hosting DF boards are equipped with two ATCA shelves each (ASIS Maxum 500 14-Slot [30]) supplied by one AC-DC converter (UNIPOWER Guardian 3U [31]) able to deliver up to 6 kW. Data are delivered to boards in the racks from the Pixel and SCT Readout Drivers (RODs) [32, 33] by means of S-LINK over fibres.

The third ATCA rack hosts the FLICs in an ASIS 6-slot horizontal 6U shelf (ATCA6u-010-3308) powered by a 1.5 kW AC-DC supply. Data are delivered out of the rack to the ROSs using S-LINK over fibres.

3.2 QuestNP

The QuestNP (QNP) card is an S-LINK data source card based on the Common Readout Receiver Card (C-RORC) [34] hardware. It can be used to replay data from the Pixel and SCT detectors.

The ability to replay ATLAS data to the FTK system, as in a data-taking run, is crucial in order to allow full commissioning during a shutdown and complements data-playback features available in individual FTK boards.

The QNP card is implemented by using a dedicated firmware design reusing elements from the firmware of the RobinNP [21] ROS. The C-RORC is a PCI express card using a Xilinx Virtex-6 FPGA [35] as the main component handling the communication through a PCIe Gen 2 (8×5.0 Gb/s) interface and implementing the interfaces to twelve optical links via three Quad Small Form-factor Pluggable (QSFP) transceivers. The QNP card makes it possible for user-defined data to be transferred to remote S-LINK data receivers in parallel on each of the 12 S-LINKs. The QNP card has been successfully used to reliably transmit data to the FTK system at an event rate of 1 kHz and has been used for testing up to 19 kHz. A version of the firmware including a Direct Memory Access (DMA) structure for each of the channels in the card is shown in figure 3. It has reached a fragment rate corresponding to the 100 kHz required by the FTK system.
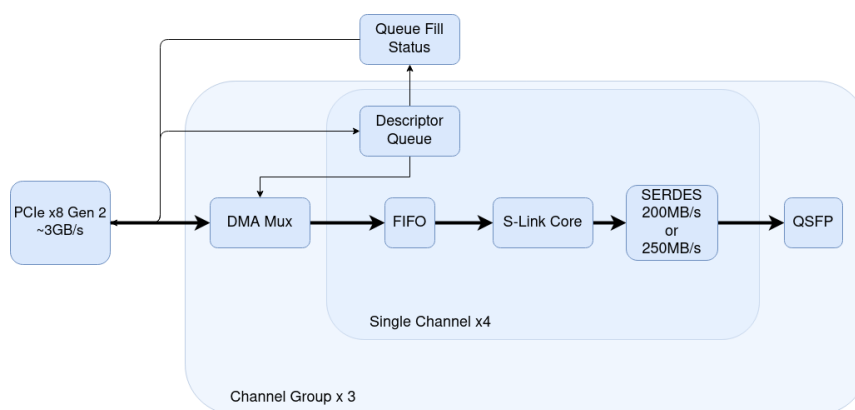

Figure 3. Diagram of the QuestNP firmware design used to input test data into the FTK via the QSFP connection. The SERDES block is a Serializer-Deserializer.

In a possible final implementation of the firmware, the QNP card would be able to synchronize the event header between its 12 internal channels. A daisy chain of the cards using low-voltage differential signalling (LVDS) pairs routed on the eight-position, eight-contact socket (RJ45 connector following the IEC 60603-7 standard) and a dedicated switch would also allow the synchronization of the output of multiple QNP cards. During Run 2, an event arrival-time difference between data from the Pixel and SCT detectors was observed, and the aforementioned synchronization mechanism would have been used to emulate this skew.

Up to three QNP cards can be installed in a 3U rack-mounted server. Five dedicated servers were used to host the 13 QNP cards used to feed data to half of the FTK system. A state-aware sender application, compatible with the ATLAS Run Control [14], is used to configure and control the cards. Monitoring of the application, of the cards' parameters and of the sent data is implemented through the Information Service (IS) [36] and the information is displayed using Grafana [37].

3.3 Input Mezzanine

The IM module receives and processes data from the inner detector. Each input channel, fed by an inner detector readout link, is processed independently of the others and propagated to the DF. The

IM forms inner detector hits into contiguous clusters and computes their centroid positions. SCT data split at the ABCD [38] front-end readout chip boundary are merged into a single cluster.

The key performance requirement for the IM is maintaining Pixel clustering throughput at the full rate of incoming data. In order to achieve this goal, the firmware is built with parallel clustering cores fed with a load balancing mechanism. Pixel clustering reduces the data size by a factor of 2–2.5. Simulation with Pixel data has shown that four cores are needed to achieve the required processing rate. This performance was demonstrated using simulated data with a pile-up of 80 before the boards went into production, as reported in ref. [39]. The implemented firmware instantiates eight cores, allowing for an additional safety margin. Bit-level simulations and debugging were performed by comparing bit-by-bit the Pixel clusters from the IM with those produced within the FTK simulation in order to reach per-bit agreement.

Each IM receives data from four readout fibres using S-LINK. The fibres are distributed to two FPGAs, two links per FPGA, with the output sent to the DF over a parallel DDR LVDS bus, shown in figure 4. The ID_Cluster_SCT and ID_Cluster_Pixel are the two main blocks performing SCT and Pixel clustering respectively. The Serializer-Deserializer (SerDes) plus S-LINK blocks receive data from the inner detector RODs. The SenderDF converts data to LVDS DDR output for the DF. The I^{2}C protocol is used for configuration. An additional SerDes per FPGA is connected to the DF FPGA as a spare 2 Gb/s line. Each FPGA is also connected to an external RAM that can be used to store test data for IM and system testing purposes. The firmware is modular, which allows different versions of the firmware to be compiled, allocating one FPGA for SCT-SCT, or SCT-Pixel, or Pixel-Pixel processing.
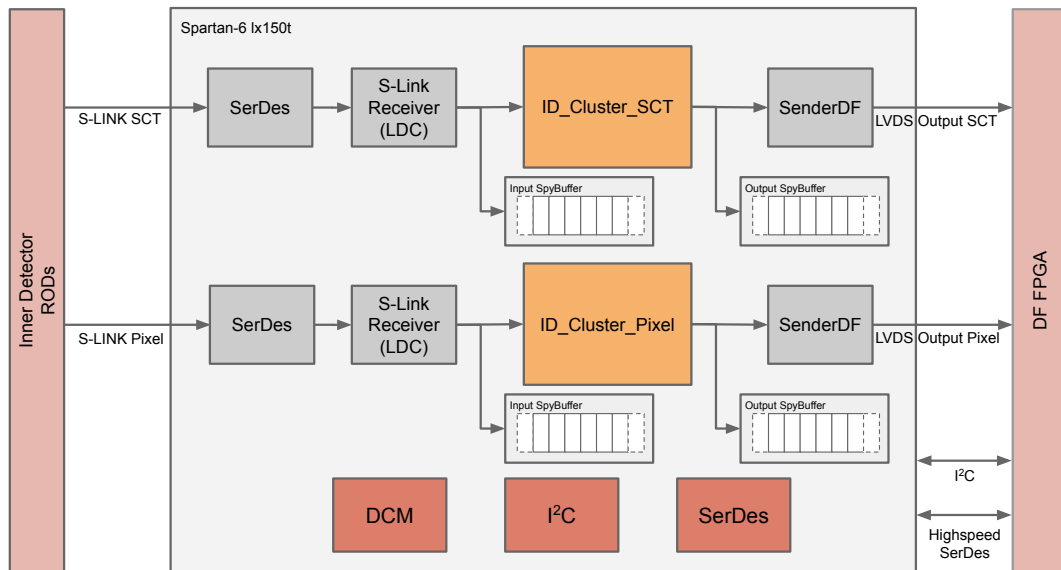
Figure 4. Top-level diagram for each of the two FPGAs on the Input Mezzanine card. The ID_Cluster_SCT and ID_Cluster_Pixel are the two main blocks performing SCT and Pixel clustering respectively. Data flows from the inner detector RODs to the Data Formatter FPGA.

Two versions of the IM cards were produced. The first version is based on the Spartan-6 150T FPGA [40] and is shown in figure 5. It was tuned for Pixel processing during the initial design. The

addition of the IBL required a more powerful FPGA, because the effective input hit rate increased by a factor of 2–2.5. The second half of the production used an updated design with Artix-7 200T FPGAs [41] to provide additional processing power.
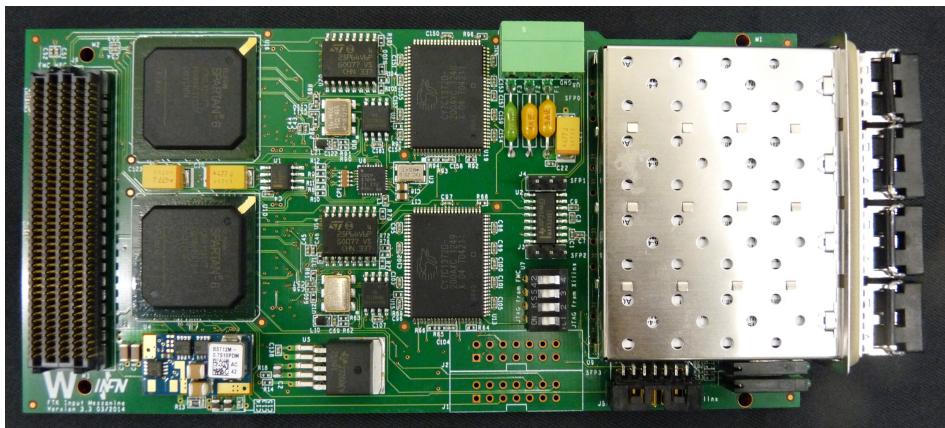

Figure 5. Photo of the Spartan-6 Input Mezzanine card, component side.

The full FTK system requires 128 IMs installed on 32 DFs. This allows for up to 256 Pixel+IBL input links and up to 256 SCT input links. The 256 inputs for Pixel+IBL exceed the original design requirements in ref. [1] and were sufficient to cover increases in the number of Pixel links during Run 2, which were used to achieve higher Pixel output bandwidth. A small additional production of IMs was planned for the LHC LS2 to provide the required connectivity in Run 3.

The Pixel clustering logic is organized into three main blocks, as shown in figure 6: Hit Decoder, Grid Clustering and Centroid Calculation. The Hit Decoder block performs the decoding of incoming data. As a part of decoding, it duplicates hits from the ganged region (merged pixels near the edges) of the Pixel module to avoid an efficiency loss in that area. It also rearranges data that arrive from the 16 front-end ASICs of a single Pixel module so that the data are approximately sorted in increasing column order for the grid of pixels in the module. The Pixel module is read out in pairs of columns. For the eight front-end ASICs on one side of the Pixel module, the columns are read out in increasing order, while for the other side the readout is by decreasing order. The described firmware block reorders the column pairs to have the same order. As described in ref. [39], this is required by the next block, Grid Clustering, described below. Finally, the Centroid Calculation block receives Pixel hits grouped into clusters, calculates the cluster centroid and outputs a single word with the centroid coordinates local to the module and the cluster size projected in two dimensions. This word is the cluster position that is used by the rest of the FTK system for processing.

The IM input logic also allows selective processing of events, by stripping out cluster words, based on the L1 trigger that fired the event and a versatile prescale function. These features are useful for controlling which trigger streams are processed and to control the processing load in the FTK system. For example, it could be used to restrict FTK processing to events where full tracking is required, e.g. those with jets and E_T^{miss}. The prescale has the functionality to send every n^{th} event full or empty, which is useful for debugging problems that only occur in successive events.

The Grid Clustering is the most resource-intensive block of the firmware. It processes incoming data to find hits that are contiguous along horizontal, vertical or diagonal lines. This operation is

performed using a grid that represents an 8×21 portion of the Pixel detector. The grid is aligned to the first hit received, called the seed, and loaded with all other hits present. This grid, replicated in the FPGA, uses local logic to select hit pixels that are contiguous to the seed, or contiguous to selected pixels. In this way, all pixels of the cluster containing the seed are selected. The readout logic then extracts all selected pixels. The output is the sequence of all hits of the clusters, with the last hit identified by an end-of-cluster flag. Next, iterative processing is done to cluster the data present on the grid but not belonging to the seeded cluster.

The logic is organized into parallel cores as described in figure 6. The baseline Pixel clustering firmware instantiates eight parallel engines. Data received from the Hit Decoder block is organized into a sequence of detector modules for each event. For load balancing, the Parallel Distributor assigns data for an entire module to the engine with the smallest load as informed by the Engine Minimum block. Each of the eight parallel engines has enough buffering to compensate for fluctuations in the processing time without causing a significant number of control signals to be sent upstream. Each of these eight parallel engines works in a first-in first-out (FIFO) mode, thus preserving the order in which data blocks flow. A parallel FIFO stores the event identifier which is sent for each data block from the Pixel and SCT detectors. This event identifier is used by the Data Merger at the right side of the diagram to collect the correct data, for a given input S-LINK, for each event from the engines before sending the built event to the DF. The output data are organized into module packets with each packet corresponding to the data from a single Pixel or SCT module. For most of the tests reported in this paper, the output packet size was limited to 32 words including one header and one trailer word. The words are 32 bits long. In the body of the packet, η and ϕ hit-coordinate pairs correspond to one 32-bit word. The IM works independently on data from each S-LINK. Synchronization of data from different S-LINK inputs is performed in the DF.
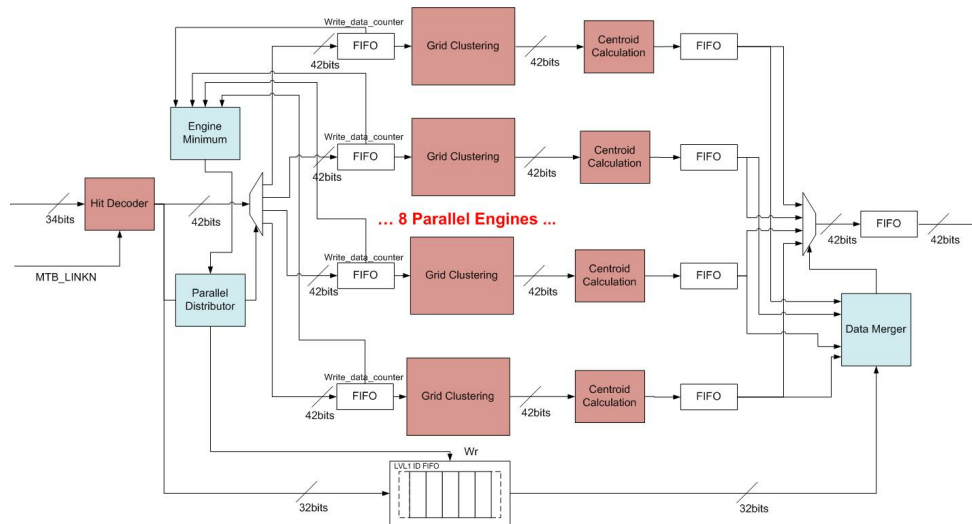
Figure 6. Diagram showing the organization into parallel engines for the Pixel clustering logic. This logic is organized into three main blocks: Hit Decoder, Grid Clustering, and Centroid Calculation.

The firmware used for tests reported here in the Spartan-6 FPGA to handle SCT-Pixel processing with two parallel clustering cores utilized approximately 56% of the logic and 71% of the memory. The equivalent firmware on the Artix-7 FPGA with eight parallel clustering cores utilizes approximately 71% of the logic and 31% of the memory.

3.4 Data Formatter

The DF receives packets of hits from the IMs and other DFs and routes them to downstream boards, sorted by towers, or to other DFs. Its main task is to assign all module data to the appropriate towers, duplicating data where necessary. The DF is based on the Pulsar [42, 43] ATCA board with full mesh connectivity via the backplane to up to ten other modules in the ATCA shelf over dual duplex multi-gigabit-transceiver connections. In addition to the connections to the ATCA backplane, the DF has connections to an RTM that hosts ten QSFP ports that provide up to 40 duplex connections. The DF hosts four mezzanine cards which can transmit data to the DF via LVDS lines. The switching functionality in the DF is performed using a Xilinx Virtex-7 690T FPGA [41]. In the DF application, the Pulsar board uses an Intelligent Platform Management Controller (IPMC) for some module control functions.
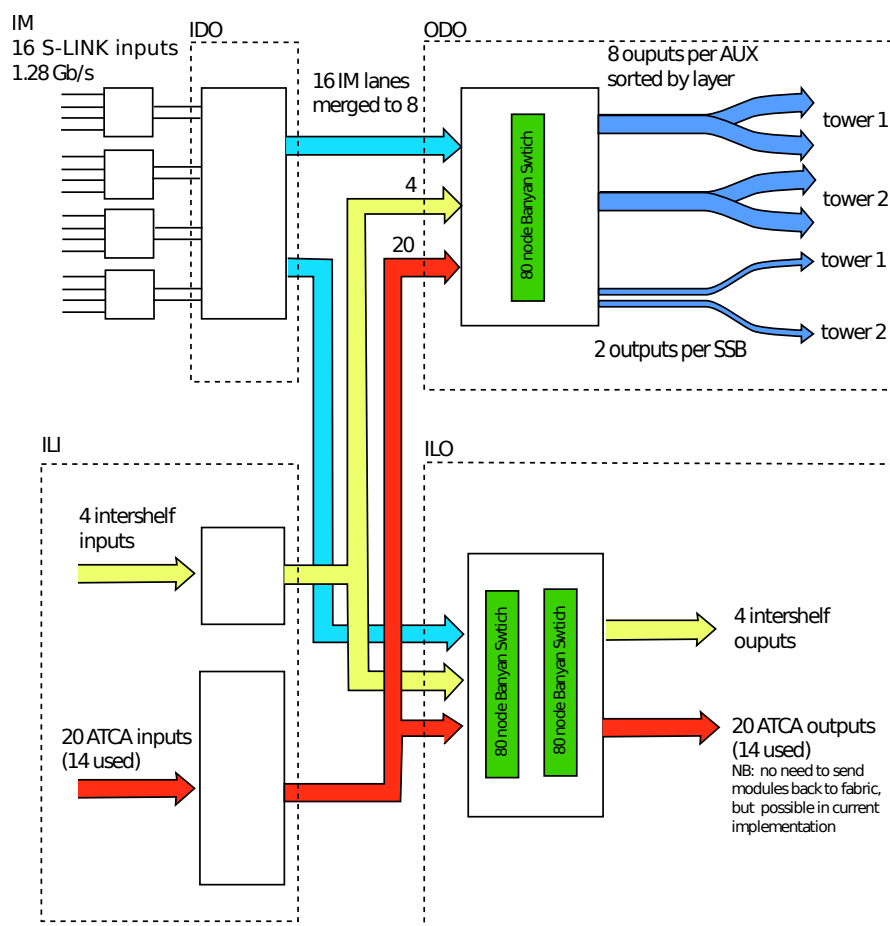
Figure 7. Diagram of dataflow in the Data Formatter firmware design. Clustered hit data from the Input Mezzanines are sent to downstream boards via the Output Data Operator (ODO) block or are shared with other Data Formatters via the Internal Link Output (ILO) block.

Four IM cards described in the previous section are installed in the four mezzanine slots on the DF. Each IM transmits two lanes of hit data over six-bit DDR links operating with a clock speed of

200 MHz. In each clock cycle the DF receives eight data bits, three control bits and one parity bit giving a data transfer rate for each lane of 1.6 Gb/s.

As mentioned in the previous section, module packets from the Pixel and SCT detectors consist of a header, a trailer, and coordinate hits in 32-bit words. The DF switches and duplicates these module packets and does not alter their content. As can be seen in figure 7, data from the IM are received in the DF firmware module called the Input Data Operator (IDO). The IDO detects L1 ID mismatches among the 16 IM inputs and discards inputs with corrupted L1 IDs.

If a module packet has a destination in the tower hosted by the current DF board it is copied into one of eight lanes which are transmitted to the Output Data Operator (ODO) switch via 32-bit-wide FIFO buffers. If a module packet has a destination hosted by another DF board, it is copied into one of a separate set of eight lanes which are transmitted to the Internal Link Output (ILO). It should be noted that the IDO will send some module packets via both connections.

Module data packets from other DF boards are received using 8b10b encoding by the Internal Link Input (ILI). Module data packets from other DF modules in the same shelf are received over the ATCA backplane. Module data packets from other ATCA shelves are received via optical fibres. The data speed for the payload on a single fibre or backplane connection is approximately 5 Gb/s for both backplane and fibre transmission. For both the backplane and fibre connections, there are pairs of duplex fibres, giving a total bandwidth between DF boards, in each direction, of approximately 10 Gb/s.

Figure 8 shows the fraction of data from the IMs of one 'In DF' that is sent to various DFs in the system. Typically, 60% or more of the input data from the IM modules is used by the DF that hosts the IM modules. The rate of data shared with other DFs corresponds to the off-diagonal elements in the figure. The amount of data which must be shared with other ATCA shelves is much smaller than the amount of data which remains in a given ATCA crate. Given the constraints inherent in the Pixel and SCT readout, the cabling was optimized to reduce data sharing between the DF boards and between ATCA shelves. A worst-case scenario of $t\bar{t}$ Monte Carlo simulation with at least one leptonic-decay and an average pile-up of 60 was used to generate the plot in figure 8.

The ILO receives module data packets from the IM cards via the IDO and also receives data from other DF modules for transmission over the backplane or fibres connecting the DFs to different shelves via the ILI. This allows any given module data packet to be routed to any of the 32 DFs in the system. The routing tables and layout of the system were configured to minimize the number of instances in which a module packet requires several hops over fibres and backplanes to reach its final destination. The minimal extra bandwidth needed by these rare extra hops is not reflected in figure 8.

The ODO receives module data packets from the IDO and the ILI. This block is responsible for sending data to the downstream boards, out of the DF system. Module data packets needed by the AUX and SSB are sorted into two towers of eight and four layers each, respectively. Module data packets needed by the SSB are transmitted directly to the SSB. If a given module data packet is needed by more than one tower it will be duplicated by the switch in the IDO.

The data switching in both the ODO and ILO is performed using a Banyan switching network which consists of 16×5 nodes allowing each input module data packet to be switched to one or more of the 32 output nodes. Each node (see figure 9) consists of two buffered inputs and intermediate memory large enough to store the largest module data packets produced by the IM. The nodes can
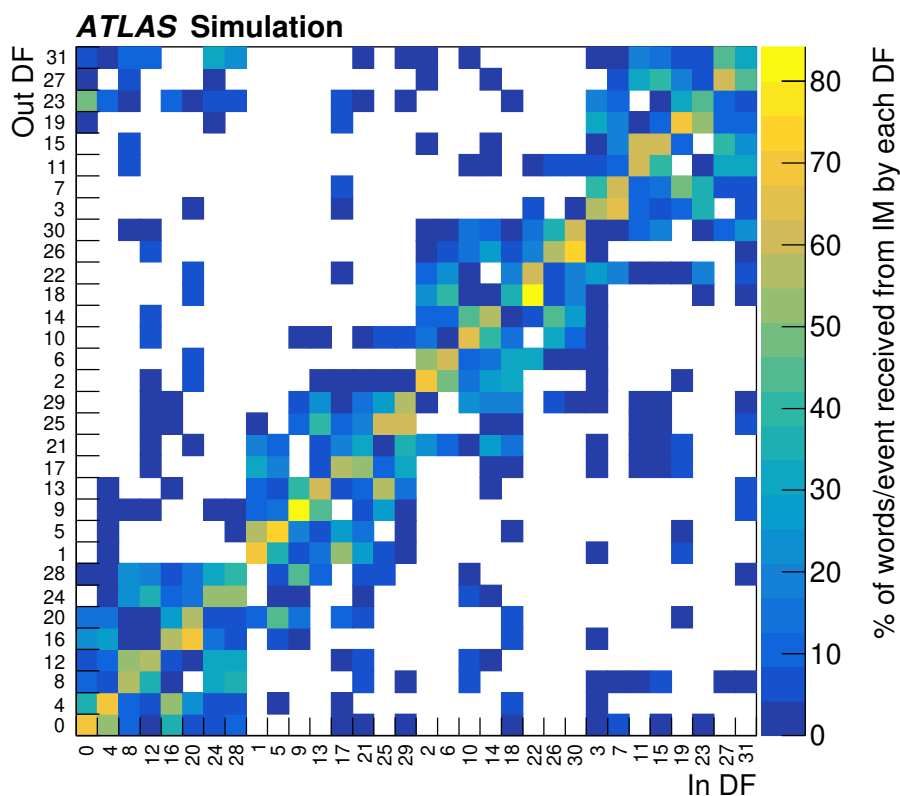
Figure 8. Fraction of input Input Mezzanine module (hosted by Data Formatters labelled 'In DF') data shared with other Data Formatter boards (labelled 'Out DF') for distribution to Auxiliary Cards and Second Stage Boards. Data whose destination is within the same shelf are shared over the ACTA backplane. The board numbers in the figure are arranged in blocks of eight corresponding to one ATCA shelf each. Sharing of data with other Data Formatter shelves requires at least one hop on an optical fibre.
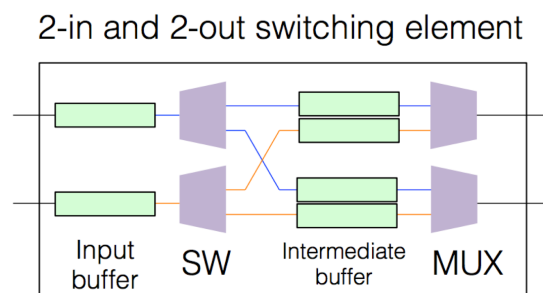
Figure 9. A single node in the Banyan switch showing input buffers and intermediate buffers. The buffers are 32 bits wide.

switch packets to the output nodes according to a 32-bit address mask and duplicate the packet as required by the address mask. The Banyan switching network was simulated using a Unified Verification Method (UVM) simulation and it was demonstrated that the network could handle the expected Run 3 FTK load at the full 100 kHz input rate.

The firmware used in the Virtex-7 690T FPGA on the Pulsar board for the tests reported here uses approximately 78% of the logic lookup tables, 49% of the flip-flops and 70% of the block RAM.

3.5 Auxiliary Card

The AUX transports hit data to the AMB and evaluates the returned track candidates, before sending candidates which pass the selection requirement to the SSB. Each of the 128 PUs is composed of an AUX and AMB pair. The AUX is a 9U VME RTM that is 280 mm deep. It communicates via a P3 connector with the AMB and with the DF and SSB via QSFP connections.

The AUX contains six Altera Aria-V GX FPGAs [44], two FB7H4 for input/output and four FB5H4 processing chips. Each processing chip is connected to one of the AMB Little Associative Memory Boards (LAMBs). The AUX board is shown in figure 10(a) and the dataflow is sketched in figure 10(b). Clusters from eight silicon detector layers are sent from DF boards to the AUX via a QSFP connection; the Input-1 FPGA receives data from three Pixel layers and one SCT layer, while the Input-2 FPGA receives data from the other four SCT layers. Coarse resolution hits, called SuperStrips (SSs), are sent to the AMB for pattern recognition over 12×2 Gb/s lines through the P3 connector. Both the SSs and full resolution hits are sent to the processor chips. The processors also receive from the AMB the addresses of roads (matched SS patterns) that have hits on at least seven of the silicon detector layers over 16×2 Gb/s lines back through the P3 connector. For each of those roads, the Data Organizer (DO) portion of a processor FPGA retrieves all of the full resolution hits in the road. The Track Fitter (TF) portion then fits each track candidate (each combination of one hit per layer) and calculates the χ^2. Those tracks passing a χ^2 cut are sent to the Input-2 FPGA where the four processor streams are synchronized and duplicate-track removal is performed before the remaining tracks are sent to an SSB via S-LINK over a Small Form-factor Pluggable (SFP) connection. All of the data processing is completely pipelined using local control signals for dataflow control.

An overview of the AUX firmware is shown in figure 11. Hits from the DF enter the SS Map in which the 32-bit hit word is converted to a 16-bit SS using lookup tables. The Hit Sort module uses a base-4 radix sort to guarantee that all hits in the same SS are sent out sequentially. Each SS is sent to the AMB while the SS plus full resolution hit (a combined 48-bit word) is sent to all four processor chips.

There are two major functions in a Processor FPGA, the DO and the TF. The DO receives roads from one of the AMB LAMBs on four serial links and uses a round robin to process them with minimum latency. The hits from the eight detector layers are processed in parallel. The DO is a database built on the fly for rapid retrieval of all hits in a road. Three sets of memory are used: the Hit List Memory (HLM) stores each hit sequentially as it arrives; the Hit List Pointer contains a pointer to the first HLM location for each SS; and the Hit Count Memory contains the number of hits in the SS. These databases are replicated for each of the 11 coordinates used in eq. 2.1, as shown in figure 11. There are two copies of the DO which act as a ping-pong buffer. At any instant one is in Write mode, filling the memories with the data for event N, while the other is in Read mode, retrieving hits in roads for event $N - 1$. For each road, the data sent from the DO to the TF consist of the road number, all of the full resolution hits in the road, and a hit mask noting which layers have hits.
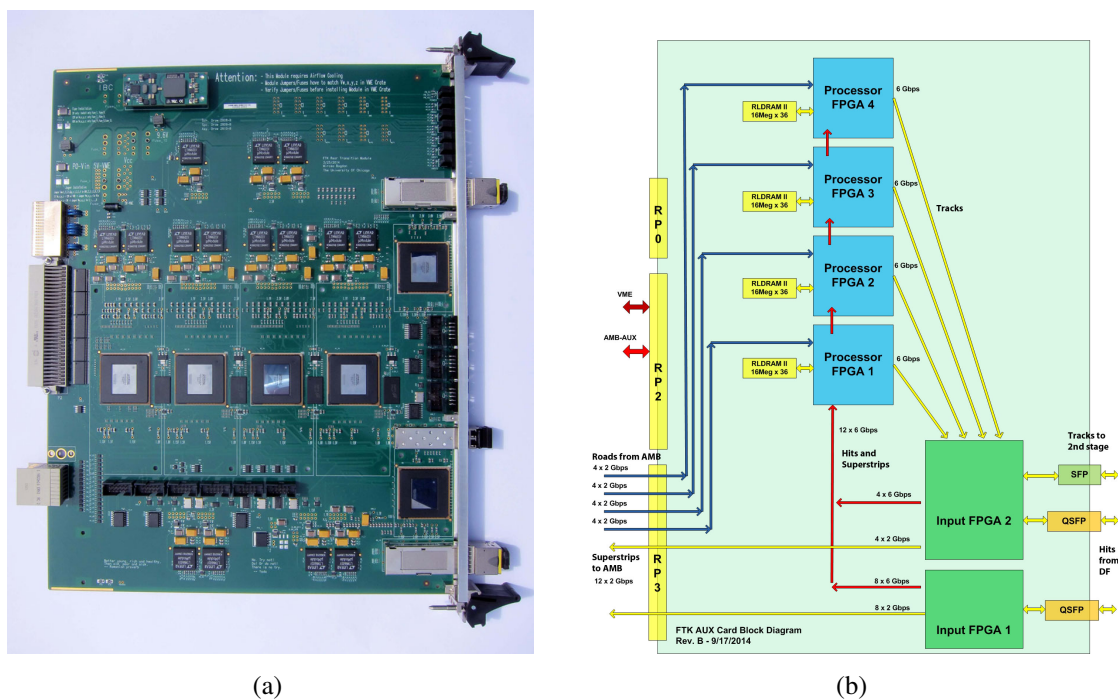
Figure 10. The (a) physical Auxiliary Card and (b) dataflow through the Auxiliary Card, starting from the lower-right.
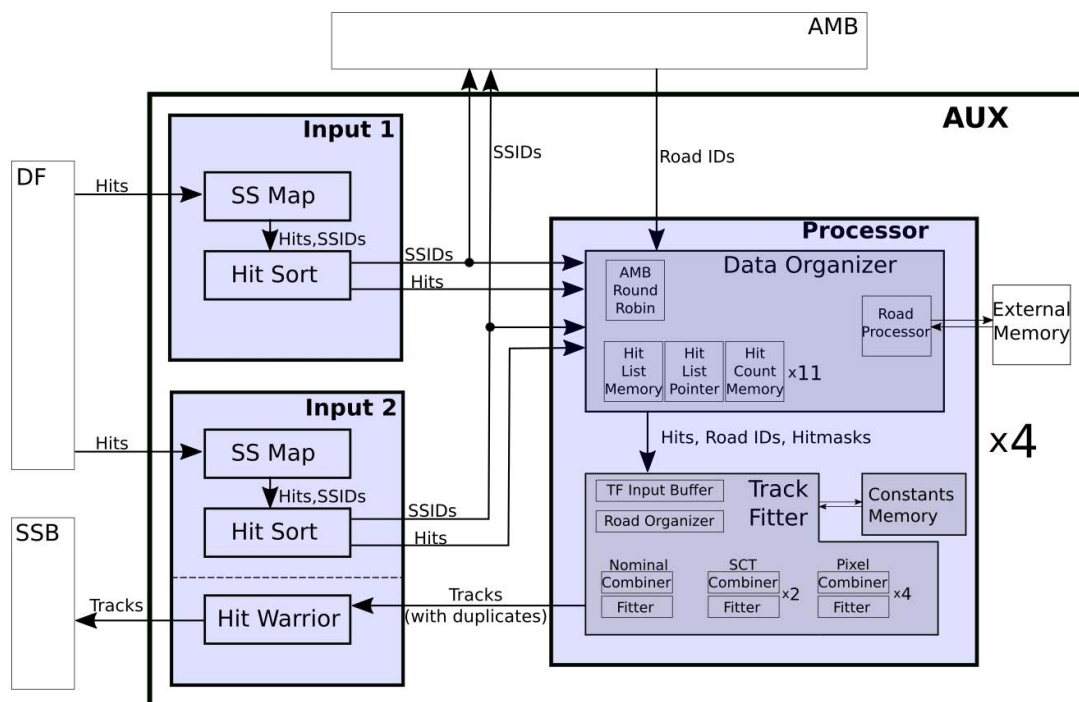

Figure 11. Diagram of the Auxiliary Card firmware design.

The TF block fits each track candidate using a linear approximation and prestored constants, as described in section 2 and eq. (2.1), which take up about 25 Mb per AUX. In the AUX, only the χ^2 is calculated. For each road received from the AMB, the Road Organizer stores the road and hits and initiates the fetching of the fit constants from memory. The data and constants are then sent to the appropriate fitter where each combination of one hit per layer is fit and its χ^2 tested. The tracks that pass the test are sent to the Hit Warrior (HW) in the Input-2 FPGA, which does duplicate-track removal. If two tracks share more than a programmable number of hits, the one with the lower χ^2 is retained.

There are three types of fitters: the SCT Majority Fitter, the Pixel Majority Fitter, and the Nominal Fitter. The Majority Fitters are used if one hit is missing from their respective detectors to improve the track-finding efficiency. For the Nominal Fitter, in parallel with the full fit, eight Recovery Fits are done in which one of the hits is dropped from each layer. If the full fit fails the χ^2 cut but a recovery fit passes the cut, that fit is retained because it is assumed that a good track had a missing hit, but a random hit landed in the dropped layer. Based on analysis of simulated data, the optimal use of FPGA resources are one, two, and four implemented Nominal, SCT Majority, and Pixel Majority fitters respectively. These fitters operate in parallel.

The firmware in the AUX FPGAs used for the tests here, including monitoring and error handling, came close to saturating the available resources. For the processor chips, > 70% of the logic and 75% of the memory are used. For the input FPGAs, about 40% of the logic and > 80% of the memory are utilized.

3.6 Associative Memory Board

The AMB [26], shown in figure 12 is the part of the PU that is devoted to pattern matching between the SSs sent by the AUX and the patterns simulated for each 8-layer road. This functionality is implemented through a custom ASIC: the AM06 described in section 3.7.
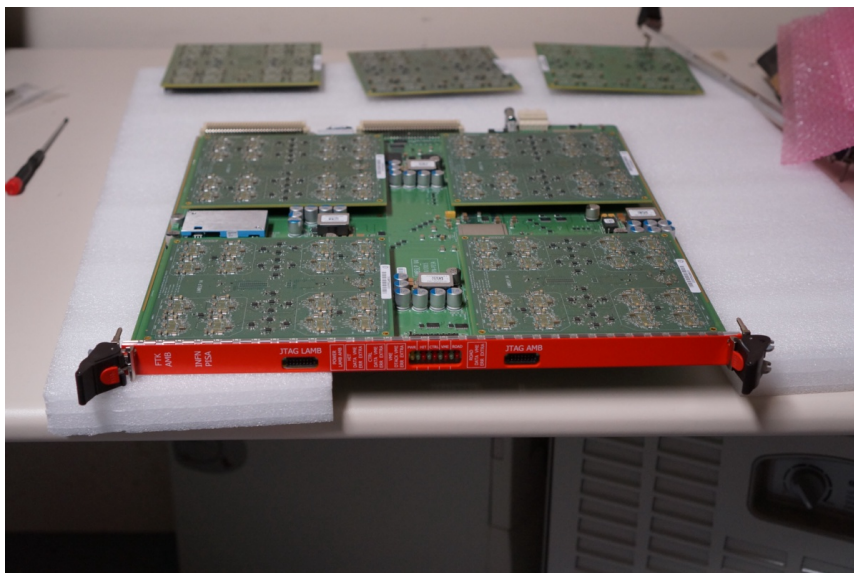

Figure 12. Photo of an Associative Memory Board with four LAMBs mounted. Additional LAMBs can be seen in the background.

An AMB consists of a 9U-VME mainboard and four identical mezzanines, the LAMBs. Four FPGAs are installed on the mainboard: two Xilinx Spartan-6 (45T and 16) [40], which control the VME interface and the state of the board respectively; and two Xilinx Artix-7 200T [41], which control the input and output logic. Each LAMB is equipped with 16 AM chips and a Xilinx Spartan-6 FPGA, dedicated to the configuration and monitoring of the mezzanine.

The AUX and AMB are connected through the VME P3 connector, as shown in figure 13. High-speed serial links provide 12 Gb/s as input from the AUX to the AMB and 16 Gb/s as output from the AMB to the AUX. The SSs provided by the AUX are received by the Xilinx Artix-7 FPGA handling the input, called Hit. This FPGA sends a copy of the SSs to each of the four LAMB mezzanines installed on the AMB. Two sets of eight 1-to-2 fan-out buffers (one per input link) distribute the same data to all the LAMB mezzanines. The Hit FPGA buffers the data and synchronizes the inputs by sending a new event only when all the mezzanines have finished processing the previous one.
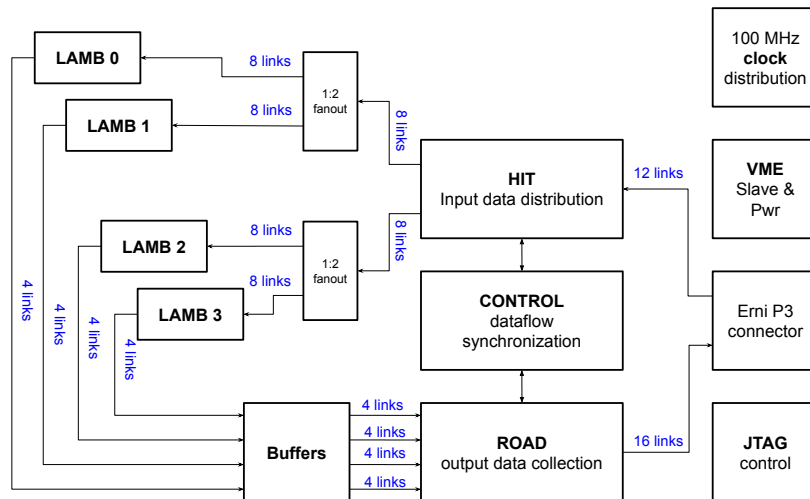
Figure 13. Block diagram of the Associative Memory Board (AMB) structure. The black arrows show the dataflow in the AMB.

On the LAMB, the SSs are distributed to the AM chips. A chain of 1-to-4 fan-out buffers in cascade allows each AM chip to get a copy of the SSs. All of the selected roads are sent to the Xilinx Artix-7 FPGA handling the output, called Road. This FPGA collects all the roads belonging to the same event before sending them to the AUX for the 8-layer fits described in the previous section. A dedicated Spartan-6 FPGA, named Control, controls the dataflow on the board and synchronizes the Hit FPGA and Road FPGA.

A fourth Spartan-6 FPGA, named VME, handles the communication on the VME bus and takes care of the board configuration and monitoring.

An AMB is able to load $\sim 8 \cdot 10^6$ independent patterns and to perform pattern comparisons at a rate of $\sim$ 12 petabytes/s, with a peak power consumption below 250 W (100 W of which is from the AMB). The entire FTK system contains 128 AMB, and it includes more than one billion (1 098 907 648) track patterns. A collection of patterns is referred to as a pattern bank.

During the tests performed in 2018, the AMB demonstrated the ability to process events at a rate greater than 100 kHz. Dedicated high-power tests [29] confirmed the designed power consumption of the AMB, and the ability of the custom cooling system, described in section 3.1, to keep the boards within temperature bounds while in the intended Run 3 configuration.

The firmware used in tests reported here for the Hit, Control, and LAMB FPGAs uses up to 50%, 60%, and 45% of the logic resources respectively. The firmware for the Road FPGA uses approximately 30% and 50% of the logic and memory resources respectively.

3.7 Associative Memory

The AM ASIC is a highly parallel processor for pattern matching, hosted on mezzanines on an AMB, which feeds in SuperStrips and reads out roads. The AM ASIC used by the FTK system, the AM06 [19] shown in figure 14, is designed in 65 nm CMOS technology. The design of the AM chip combines full-custom content-addressable memory arrays, standard logic cells and SerDes IP blocks at 2 Gb/s for input/output communication. The AM chip is able to perform pattern matching in parallel on all the 131 072 patterns stored on its 168 mm^2 die. The stored patterns are composed of a set of eight SSs, one for each detector layer used by the FTK. The 16 bits of each SS are stored on 18 XORAM [45] cells forming an AM cell. The XORAM cell is composed of a conventional six-transistor SRAM cell, which stores the data, merged with an XOR gate executing the matching with the input at a clock rate of 100 MHz. Two XORAM cells can be paired to allow the presence of ternary bits in the pattern to be stored. When two XORAM cells are used to store the value of a single bit, the bit-value can assume three values "0" (or '00'), "1" (or '11'), and "X" (either '01' or '10'). While for the "0" and "1" values the pattern behaves as if no ternary bit is present, the "X" value can be used as a Don't Care (DC) value. The DC bits are bits in the pattern that are always considered matched, regardless of the value of the corresponding bits in the input word. Effectively, these DC bits increase the width of the pattern by a factor of 2^{N_X}, where N_X is the number of DC bits used in a pattern. This provides variable resolution patterns, allowing some patterns to be wider than others. Figure 1 uses a dotted line as a visual representation of this on the second layer. While the configuration used by the FTK uses a 16-bit SS with up to two DC bits, the AM chip can be configured to accommodate from two to nine DC bits for each pattern. The XORAM cell is optimized to achieve a power consumption of 1 fJ/bit-comparison, allowing 64 AM06 to be installed on a single VME board.

As shown in figure 15, SSs are received by the AM06 asynchronously on the eight input serial-buses. The SSs are deserialized and transmitted in parallel to the FILTER module that takes care of correctly encoding ternary bits by mapping the 16-bit input words to 18-bit words. This module can also receive data through the JTAG connection in order to write the pattern data and to test the stored pattern. The 8×18-bit data are propagated to all of the memory locations in the chip where they are compared to the stored pattern. The match status for each of the eight layers in a pattern is held until all the data belonging to the same event are received. At the end of the event, a majority block counts the number of matched layers for each pattern. If the number of matched layers is greater than a selectable threshold, the pattern identifier is sent to the PATT FLUX module. This module adds a chip geographical address to the internal pattern address and handles the chip output. Patterns received from previous chips in the daisy chain are deserialized and sent to the PATT FLUX module, which buffers the data and ensures they are transmitted before the given
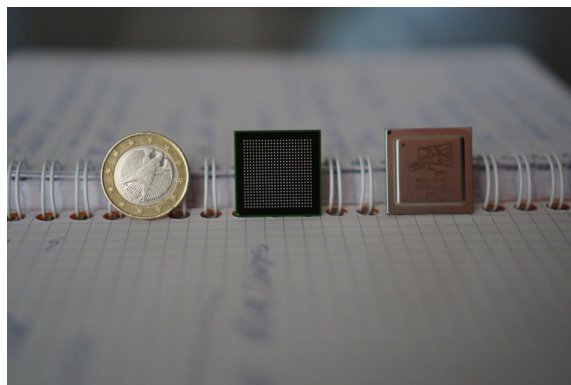
Figure 14. Photo of the bottom (centre) and top (right) of the AM06. On the left a 1-euro coin is shown for size comparison.

chip's data. The end of an event resets all of the AM cells in the ASIC in one clock cycle so that the AM chip can process data belonging to a new event while sending out the matched patterns.
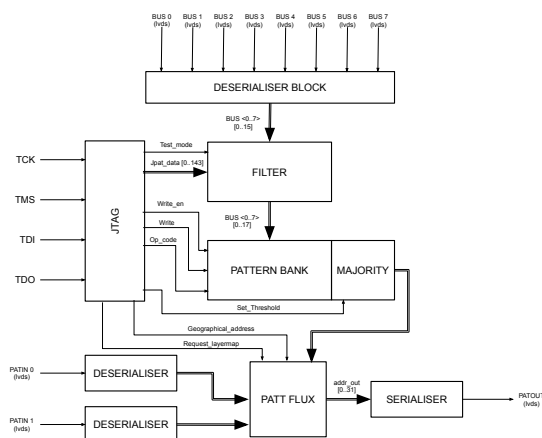
Figure 15. Diagram of the dataflow through the AM06 chip.

The AM chips can be connected in a daisy chain to maximize the number of stored patterns on each AMB while maintaining a simple routing at the board level. Two dedicated inputs are present on each AM06 to receive data from previous AM chips in the chain. The pattern identifiers collected on the two inputs are copied to the AM chip output.

To allow the full system of 128 PUs to be commissioned, more than 9000 AM06 were produced in two production rounds. A first batch of 2159 preproduction chips, including slow corner and fast corner chips,[2] was delivered in 2014 and tested in-house, achieving an estimated yield of 83% for the slow corner and 89% for the fast corner. The production batch composed of 8126 ASICs was delivered in 2016 and tested by an external company. The average yield for the production batch was 83%. AM chips from this batch were split into two groups. Normal chips are required

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[2]The fast corner and slow corner chips are obtained with a variation of fabrication parameters that are optimized for set-up and hold time respectively. This has the effect of producing chips that on average will work at slightly faster or slower clock frequencies.

to pass all functional tests at nominal power consumption and clock speed. High-performance chips are those which pass all functional tests with a 10% increase in clock frequency and 5% decrease in voltage. High-performance chips account for roughly 65% of the produced AM chips, and normal-performance chips account for roughly 15% of the produced AM chips. A correlation of the yield with the mechanical wear of the AM chip socket was observed, with more chips ending up in the lower performance group. Only high-performance chips were expected to be mounted on the production boards. Retesting of chips to recover more of them was planned after having understood the effect of the aging of the test-stand.

3.8 Second Stage Board

The SSB receives 8-layer tracks from the AUXs and clustered hits from the DF on the four layers that are unused in the pattern matching. It extrapolates these tracks into the four layers to search for hits, performs 12-layer track fits and removes duplicate tracks before outputting the final FTK tracks. A full track packet consists of its helix parameters, χ^2 value, and associated cluster coordinates. A schematic description of this functionality and the dataflow through the SSB is shown in figure 16. The second-stage processing hardware consists of a VME main board and RTM, shown in figure 17.
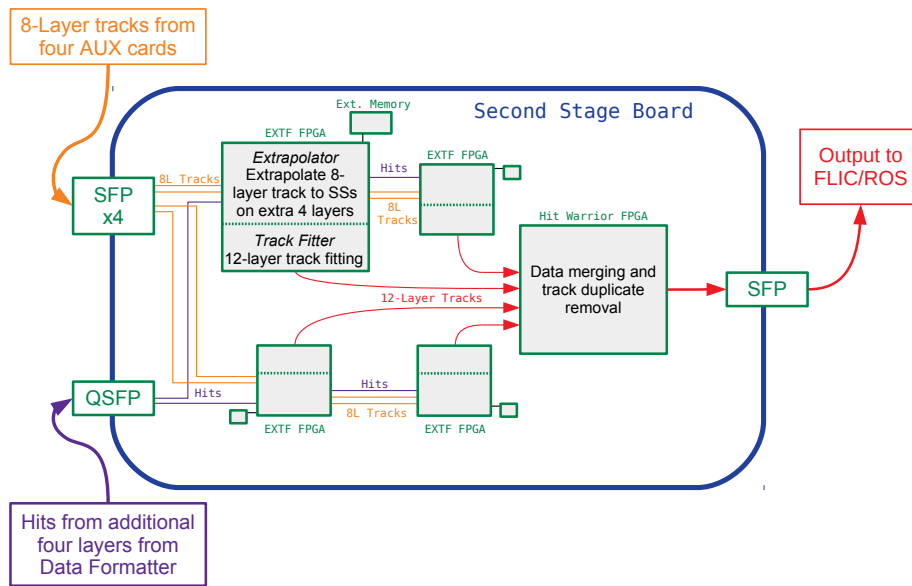
Figure 16. Diagram of the dataflow through the Second Stage Board.

The processing of hits and tracks is performed on the SSB main board (SSB MAIN), which hosts six Xilinx Kintex-7 FPGAs [41] (four 410T-FBG900 and two 410T-FBG676). Four of the FPGAs, Extrapolator and Track Fitters (EXTFs), perform the extrapolation and 12-layer track fitting. One FPGA, the Hit Warrior (HW), merges the streams, performs duplicate-track removal, and sends final tracks to the FLIC or ROS. The remaining FPGA provides the VME interface. The high-speed serial interfaces to the DF, AUX cards, and FLIC are provided by the SSB RTM, which also has serial interfaces to other SSBs intended for duplicate-track removal. Data arrive at the SSB from a DF via a QSFP connection and from AUXs via SFP connections. Two of the QSFP
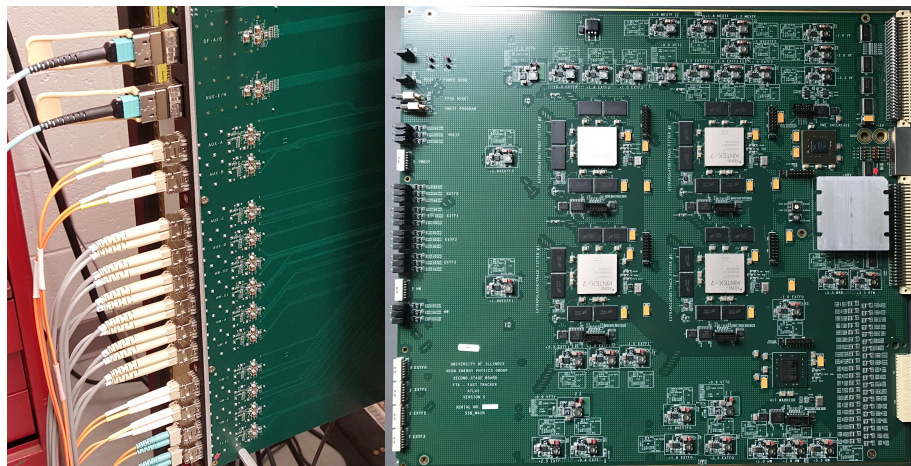
Figure 17. The physical RTM (left) and MAIN Second Stage Boards (right).

channels and two SFP connections are routed to each of the two 'primary' EXTFs, those that are directly connected to the input data streams.

Each EXTF FPGA has three main functions. First, the EXTF synchronizes the data streams from up to two AUXs and one DF covering one FTK tower. Second, 8-layer track information is used to extrapolate the track into SSs on the additional IBL and three SCT layers. The SSs of the most likely hit positions are then retrieved. Last, the clustered hits in the extrapolated SSs are retrieved and combined with the 8-layer track hits to perform full 12-layer track fits, as described in section 2 and eq. (2.2).

Tracks are required to pass a χ^2 selection before being sent to the HW FPGA. Up to one hit in the additional four layers is allowed to be missing or dropped in a recovery fit as in section 3.5. When using all four EXTFs on the board, two of the EXTFs each receive their input data via pass-through from one of the primary EXTFs. Configuration and monitoring data are read in and out through the VME interface. The firmware design is illustrated in figure 18. Up to 80% of the logic resources and 90% of the memory of the FPGA are used in the design.

Constants for extrapolation and track fitting are stored on external RLDRAM, accessed with a 400 MHz DDR clock. Two chips per EXTF, with memory totalling 576 Mb, are available for the extrapolation constants, and four chips per EXTF, totalling 1152 Mb, are available for the track-fitting constants. The constants used during comissioning were at most 70 and 550 Mb in size for the Extrapolator and Track Fitter respectively.

The HW FPGA has two primary functions on the SSB. First, the HW combines the event data streams from up to four EXTF FPGAs. Second, it searches for and removes any duplicate tracks from the combined data stream and outputs the filtered event data stream to either the ROS or FLIC. In addition to its primary functions, the HW also provides monitoring and histogramming of output track parameters. As in the EXTF FPGA, these monitoring data are read out over the VME interface. A top-level block diagram for the firmware is shown in figure 19.

Data arrive from each EXTF FPGA over a parallel LVDS interface operating at 180 MHz. The input logic extracts the event packets and presents them to a multiplexer called the Sync Engine. The Sync Engine combines the event packets pertaining to the same event identifier. The HW track
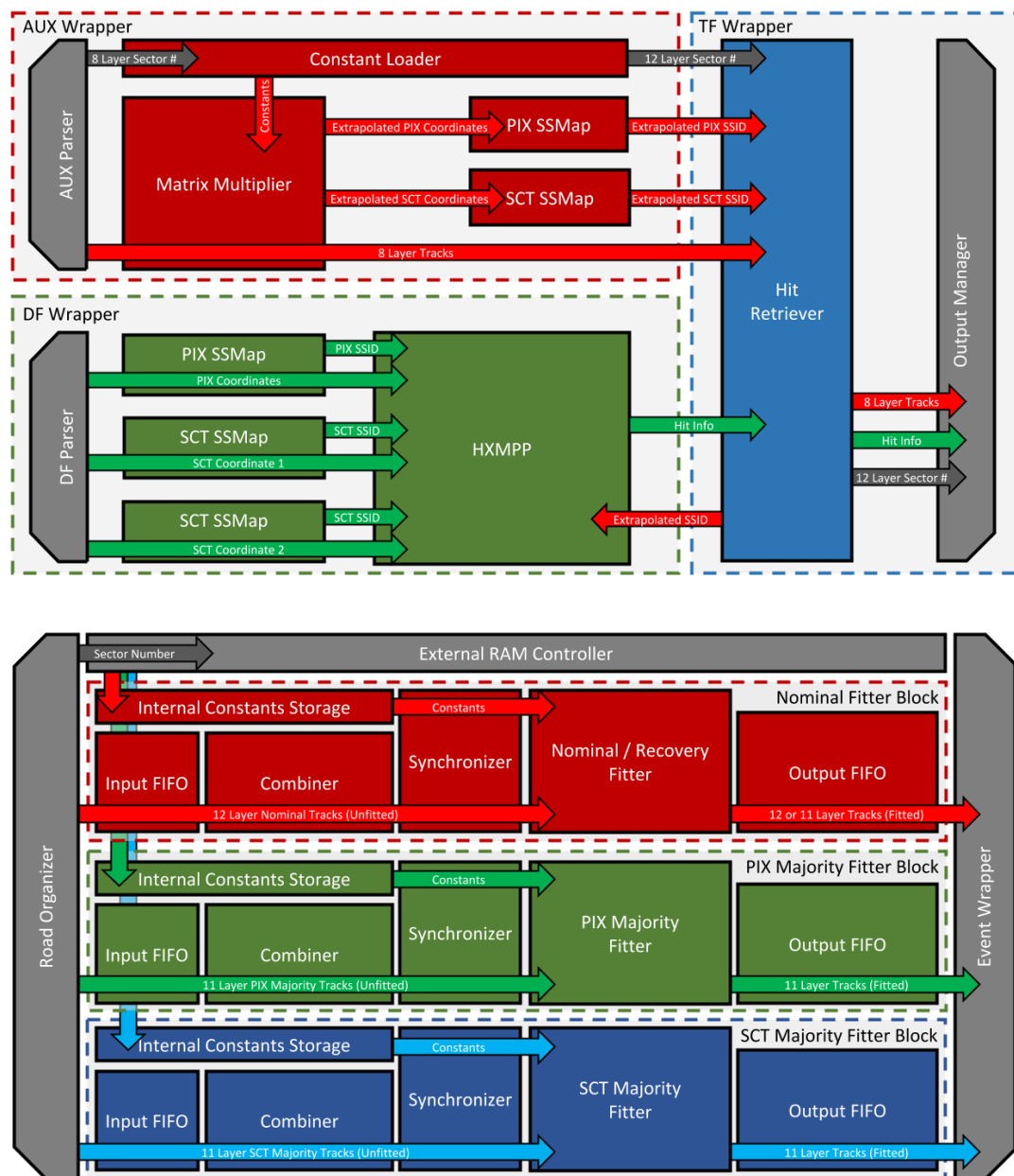
Figure 18. Block diagrams of the firmware in the Extrapolator and Track Fitter (EXTF) FPGA on the Second Stage Board split into the Extrapolator (top) and Track Fitter (bottom) firmware design. The AUX and DF wrappers receive the 8-layer track and additional hits respectively. The Extrapolator's output manager feeds into the Track Fitter's Road Organizer, and the Track Fitter sends tracks to the Hit Warrior via the Event Wrapper.

filter algorithm is then applied. This algorithm writes every incoming track data to its own block of memory with corresponding comparison logic, and a FIFO, not shown in figure 19. When each track arrives, it is simultaneously compared with all previously received tracks for that event. Thus by the time the last track is received, all track comparisons have been performed with minimal
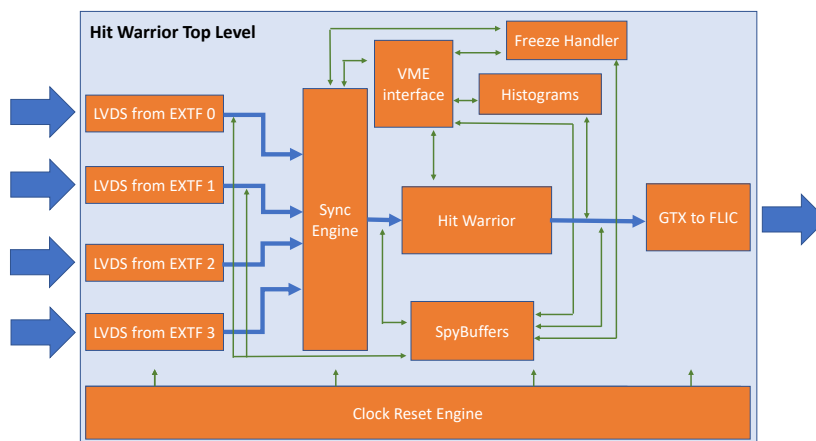
Figure 19. Diagram of the Hit Warrior firmware design for the Second Stage Board.

additional latency. Any detected match is marked. Tracks are considered to be duplicated if the tracks come from the same sector and they have the same hit coordinates for at least eight layers. If a duplicate is found, the track with more hits is kept. If both tracks contain the same number of hits, the track with a smaller χ^2 value is kept.

When the HW algorithm FIFO is read out, any duplicate-track data are removed such that the data leaving the HW only contains unique tracks. These output tracks are formatted to be sent to either the ROS or FLIC. The final version of the HW firmware can handle an average of 141 tracks per SSB at an event rate of 100 kHz. After duplicate-track removal, the HW is able to maintain an average output event size of 28 tracks per SSB at 100 kHz. Up to 20% of the logic resources and memory are used in the FPGA design.

The full FTK system requires 32 SSB MAIN and 32 SSB RTM boards. By the beginning of spring 2019, the required production boards were fully tested for integration at CERN and by the beginning of summer 2019, three additional spare SSB MAIN boards and five additional spare SSB RTM boards were at CERN.

3.9 FTK-to-High-Level-Trigger Interface Card

The FLIC is a custom ATCA card that interfaces the upstream FTK components with the HLT. The FLIC boards receive tracks via the eight 2 Gb/s optical links on the front panel, which are connected to the SSBs. The key functionality of the FLIC is to find and insert the global module IDs into the output by using lookup tables. These are used by the HLT to obtain global coordinates from the local FTK coordinates. In addition, the output packet is formatted to the standard ATLAS event format before it is sent to the HLT farm. This final packet includes an error word to inform the HLT of possible problems with the contents of the output packet. Besides data processing, the FLIC sends data over the backplane to multiple processor blades mounted in the same ATCA shelf in order to perform data quality monitoring.

There are two FLIC boards in the FTK system, hosted in the hub slots of the ATCA shelf, and two processor blades hosted in the payload slots. Event packets can be sent to any of the processor blades via 10 Gb/s Ethernet. The FLIC board consists of the input card and the RTM, shown in

Figure 20. The FTK-to-High-Level-Trigger Interface Card (left) and its RTM (right).

figure 20. The input card has two areas, the data processing area and the management area. Four Xilinx Spartan-6 75T-FGG676 FPGAs [40] are installed in the data processing area. Two of them handle the data processing and the other two communicate with the processor blades over the ATCA backplane. The first two are referred to as the processing FPGAs while the other two are referred to as the interface FPGAs. The four FPGAs are connected to each other via a full internal mesh of high-speed LVDS lines with a designed bandwidth of 4 Gb/s, shown in figure 21.

The management area provides slow control and monitoring of the FLIC board. One small Spartan-3 S400-FG320 FPGA [46], one Microchip Peripheral Interface Controller (PIC), four Flash RAMs, and one IPMC card are located in the management area. The Spartan-3 FPGA provides level translation and bus control logic to interface the microprocessor and Flash RAMs to the Spartan-6 FPGAs. The firmware and lookup tables are stored in the Flash RAM. Commands are sent through the front-panel Ethernet port to the PIC to perform register and data accesses to all other devices by controlling the small FPGA. All monitoring information can be transferred through the IPMC to the shelf manager.
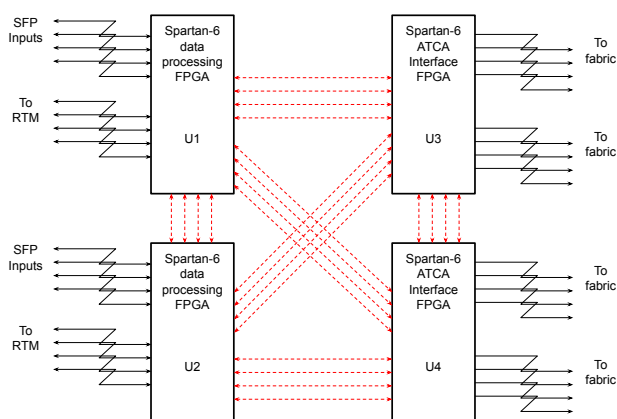

Figure 21. Diagram of the connections including the internal mesh connecting each FTK-to-High-Level-Trigger Interface Card FPGA to the others with four high-speed GTX lines.

Data processing in each processing FPGA has four pipelines. Each pipeline receives data from one SFP connection on the front panel and processes the data. The core data processing functionality, ATLAS global module ID lookup, is performed with the help of 32 Mb of fast SRAM per input link. Each track header has the address for the lookup embedded so that the lookup can be initialized immediately after the track starts being processed. The lookup and track processing are done in parallel to ensure the module IDs are ready to be inserted when the track processing finishes. The merge state machine combines the module IDs and the remaining event packet, formatted in the ATLAS event format. The packets are then sent out from the RTM to the HLT over eight fibres using 2 Gb/s S-LINKs. The data processing pipeline is summarized in figure 22. For stand-alone diagnostic purposes and baseline performance tests, a second version of the firmware that emulates the output of the upstream FTK system can be loaded to either or both of the processing FPGAs. FPGAs with the nominal firmware loaded can receive emulated event packets to perform a loop-back test.
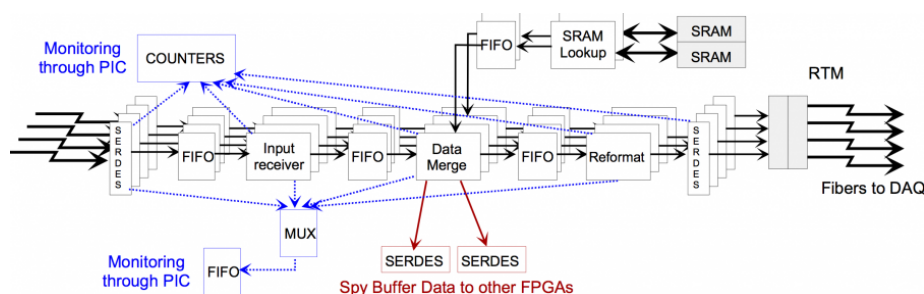
Figure 22. Diagram of the data processing pipeline in the FTK-to-High-Level-Trigger Interface Card processing FPGA. The input lines (left) receive data from the Second Stage Boards.

The FLIC also implements higher-level monitoring functionality where the two interface FPGAs copy selected fragments from the processing FPGAs via the internal mesh. Those fragments are then assembled by using the event identifier and sent to the processor blades using Ethernet. Each pipeline only receives information from a part of the FTK system, while the assembled fragments contain information for the whole system, allowing advanced event-level monitoring.

4 Online software, control and monitoring

The FTK online software integrates the FTK system into the ATLAS trigger and data-taking infrastructure. It provides features to configure, run and monitor the FTK boards from the ATLAS Run Control (RC) infrastructure, and handle the internal commands and synchronization operations.

4.1 Run Control integration

The ATLAS RC is based on a finite-state machine (FSM) guiding the entire ATLAS detector through standby, configuration, and running states. This general behaviour is inherited by the FTK online software.

The FTK software required a dedicated redesign and extension of the ATLAS FSM in order to handle the special cases of the FTK system. For example, it takes about 50 minutes to configure and load the pattern banks into the 16 PUs in one VME crate, which exceeds the time allotted to configure the ATLAS detector. The long configuration time is driven by the need to transfer about

500 MB/board with limited bandwidth and CPU resources. This step was optimized to maximize the usage of the resources on the single-board computer in the VME crate and throughput over the VME backplane. To accommodate this, two configuration transitions were implemented. During the LHC inter-fill, pattern banks and fit constants are loaded onto the boards. During data-taking, only pattern-bank and fit-constant checksums are computed for validation. If a checksum validation failure occurs, the FTK software prevents the FSM transition from completing successfully.

The complexity of operations performed by the FTK boards for different transitions required the development of a multi-threaded approach in order to fit within the ATLAS transition time windows. This is particularly crucial for the AMBs, AUXs, and SSBs hosted in VME crates and controlled by a single-board computer where the bandwidth over the VME bus is a limiting factor. The implemented design provides control of operations per board with options for parallelization, the number of threads, and thread queue management.

Another important aspect of the FTK control software is to handle concurrent access to board resources. In most cases, the firmware does not provide concurrent access management; therefore, access serialization was implemented at the software level by means of mutexes and system semaphores. This approach has the cost of longer delays between operations such as state transitions and monitoring. However, this did not impact data-taking operations.

The software infrastructure allows both the inclusion of the FTK in ATLAS data-taking runs while writing output to the ATLAS data stream and stand-alone parasitic runs writing to an independent data stream. The latter was particularly useful early in the commissioning phase for performing rapid tests, without waiting for an entire LHC fill to retry a test and without negatively affecting ATLAS data-taking. Near the end of Run 2, a vertical slice of FTK was regularly included in ATLAS runs. Using the functionality of the IMs, the FTK system can selectively process events according to the result of the ATLAS L1 trigger. During Run 2 a special trigger was configured to select events with muons that fell within the geometric coverage of the vertical FTK slice that was included in ATLAS data-taking.

4.2 Automated procedures

Two automatic procedures are required for integration into the ATLAS RC framework: Stopless-Removal and Stopless-Recovery. The Stopless-Removal procedure removes a subsystem, or part of it, from the ATLAS FSM when it is interrupting data-taking, without changing the global FSM state. In the FTK software, this was implemented by means of an external application automatically triggered by missing event fragments from the FTK subsystem. This temporary solution proved to be particularly useful during the commissioning phase, where the software infrastructure was rapidly evolving.

Stopless-Recovery consists of a semi-automatic procedure to reinclude components previously excluded from the run, e.g. because of a Stopless-Removal. As implemented in the FTK system, this requires a full reconfiguration of the different boards before reinclusion of the system in the FSM and data-taking. This reconfiguration procedure is managed by an internal ATLAS-like FSM system.

4.3 Monitoring

Another important aspect of the FTK online software is to provide the monitoring functionalities of the board status, on-going operations, and of the quality of the output data. The first is performed

by accessing specific board registers and publishing the information to the IS and the Online Histogramming Service (OH) [14]. Additional information is also propagated to higher-level monitoring applications, such as Grafana. Dedicated functions are used to retrieve monitoring information from the boards. Their parallelization can be controlled by assigning them to separate threads or by forcing serialization of the operations. Easy access (e.g. via Grafana) to monitoring information and its history, ranging from basic counters to detailed firmware states, is extremely useful for commissioning, understanding system performance and tracking down bugs in the system.

Data quality information for each board, such as data snapshots and counters, is stored in dedicated spybuffers, which are read out periodically by online software monitoring functions. The data are then published to the ATLAS Event Monitoring (EMON) service by means of a customized interface which provides temporary storage for multiple spybuffers from different boards that can be accessed on-demand for analysis and evaluation.

A freeze mechanism was implemented in order to block the overwriting of the spybuffers when an error occurs and during readout of spybuffers. This functionality was crucial for accelerating firmware debugging and development by catching problematic events in situ.

5 Configuration, optimization and performance

The FTK uses configuration data in the pattern matching and track fitting. The production of this configuration and its optimization are enabled by a functional simulation of the FTK. This simulation of the hardware provides a way to evaluate the performance and validate the output data from the hardware. The FTK technical design report [1] discusses the required tracking efficiencies for several physics cases.

5.1 Simulation

The simulation software for the FTK [47] serves multiple purposes:

- support of hardware design decisions,

- production and validation of the input pattern banks,

- provision of sectors and constants needed by the hardware,

- enabling of new trigger strategies that make use of the FTK,

- and validation of the output of the FTK hardware, both online and offline.

It must simulate the full FTK chain, including clustering, data organization and distribution, pattern matching, track fitting in both the first and second stages, and any final FLIC processing. The output of the FTK simulation, e.g. FTK tracks at either the first or second stages, can be stored in simple ROOT [48] files as well as ATLAS-specific file formats. The simulation is integrated into the ATLAS Athena software environment [49], and as such, the option to store FTK tracks inside of simulated events as if they were part of the real hardware output was also developed. This integration allows it to run in the ATLAS offline validation framework. It also allows its use in reprocessing data to study trigger algorithms for use in the HLT. The FTK simulation is fully integrated and included by default in such reprocessings.

A big challenge for the FTK simulation is that it is slow to run on commodity hardware such as CPUs that lack the parallelism found in the AM chips for pattern matching and in the FPGAs used to compute linear fits. Moreover, the databases of pattern banks require very large amounts of run-time memory which can only be loaded slowly from the compressed on-disk storage format, making it unfeasible to process all FTK towers for a given event at the same time. Typically, the constants and patterns required to simulate a single tower take up roughly 500 MB of memory.

To get around the challenges above, the FTK simulation uses a multi-step approach. It starts by processing events, before any reconstruction, from the detector to create an intermediate output containing the inputs to the 64 towers of the FTK. Next the full pattern-matching and simulation chain is run as 64 separate jobs. The clustering algorithm can be run in either the first or second step. The separate jobs for each tower are run serially, but configured and controlled by a single command, and their outputs are merged. In this last step, the simulation of the duplicate-track removal in the hardware can also be applied.

The simulated output of the FTK system can also be merged with the original detector-level input file. This creates a combined file including tracks as they might be found by the FTK. This last step is very useful for studying how the FTK can be used as part of the trigger system. The same simulation environment that is used for this full simulation of the FTK system is used to develop FTK pattern banks, as described below.

It is crucial to ensure that the pattern-matching and track-finding codes are robust and efficient, as these two steps are the slowest parts of the FTK simulation. The linear fits and matrix algebra of the track-fitting code use the highly optimized Eigen libraries [50]. The number of patterns matched typically rises linearly with detector occupancy; however, the number of fits rises much faster than this, as it depends on the number of combinations across multiple layers and the number of hits in each SS. The CPU time is dominated by pattern matching at lower pile-up and by track finding at higher pile-up. The exact balance depends on the pile-up value for which the pattern banks were optimized.

In order to simulate a large number of events for trigger studies, a 'fast' simulation to emulate the full FTK performance was also developed. The fast simulation starts with fully simulated tracks as found by HLT-based tracking algorithms, which are always more efficient with respect to offline tracking than the FTK. It works by smearing the track parameters d_0, z_0, q/p_T, η and ϕ to account for the loss of resolution due to using linear approximations and by randomly rejecting tracks using parameterizations from the full simulation to account for any FTK inefficiencies relative to the HLT tracking. In principle, similar fast simulations seeded by offline tracks or a Monte Carlo simulation record could be developed. The limitation of the fast simulation is that it does not account for the true rate of fake tracks, which typically account for 1–2% of reconstructed FTK tracks. The full simulation described above, rather than this fast simulation, is used for the comparison in section 5.7.

5.2 Sectors and constants

The sectors and constants needed by both the FTK hardware and simulation are derived from a full ATLAS simulation of single muons traversing the inner detector. Muons are chosen because they do not scatter and interact as much as electrons and hadrons do. Typically, ten muons per event were used, drawn from uniform distributions in the five track parameters. The same ranges as for the pattern banks, described below, are used, except for a slightly wider η range in order to not lose

any efficiency at the edge of the inner detector. Around one billion muons in total are needed to produce sectors and constants with the highest track finding efficiencies.

When producing the fit constants, the FTK simulation provides an option to measure d_0 relative to either the beamspot or the origin. Nominally, the beamspot option more closely reflects the running conditions, but it also requires the HLT to know which beamspot was used during the single-muon detector simulation. Since the beamspot may shift, it was decided to always compute d_0 relative to the ATLAS coordinate system's origin and then update d_0 in accord with the beamspot in software. During Run 2, the LHC beamspot was around 1 mm from the ATLAS origin in the transverse plane. The best guess of the beamspot position is used when generating the patterns, described below. A change in the beamspot position by 1 mm relative to the one used to produce the pattern banks results in a reduction of the tracking efficiency of up to 5%. Changes in the beamspot position during Run 2 were typically much smaller than this. Over the course of a given year, the position moved by less than about 0.2 mm in the x or y coordinate.

The sectors and constants produced can be validated before beginning the time-consuming pattern-bank production by running the FTK simulation in 'sector as pattern' mode. In this configuration, the nominal pattern matching is not performed, and instead, all combinations of hits that fall within a sector are deemed to have fired a pattern. This can be done for sectors in the first stage only, or sectors in the full 12-layers used by the SSB. This mode can only be used on samples of single particles without pile-up, otherwise the combinatorics of hits within a 'sector as pattern' lead to too many track fits for the simulation to run.

A separate set of sectors and constants is produced to be used in the hardware. This is needed because the nominal ATLAS simulation does not fully reproduce small detector misalignments. Differences in the detector alignment between data and simulation would lead to large losses in efficiency and misreconstructed track parameters. The ATLAS 'data overlay' infrastructure [51], used to add minimum-bias events from real ATLAS zero-bias data to simulated hard-scatter events, is used to simulate single muons in the full ATLAS detector environment observed in data.

5.3 Pattern-bank production

FTK pattern-bank production begins with the generation of approximately 10^{11} pattern candidates (about 10^9 per tower). Each pattern candidate corresponds to eight coarse resolution hit positions on different detector layers which are traversed by a track. The tracks used to produce the candidate patterns are drawn from uniform distributions in the five track parameters: $d_0 \in [-2.2, 2.2]$ mm, $z_0 \in [-120, 120]$ mm, $q/p_T \in [-0.8, 0.8]$ GeV^{-1}, $|\eta| < 3$, and $\phi \in [-\pi, \pi]$. Due to the large number of required pattern candidates, determining the corresponding hit positions using the full ATLAS tracker simulation is not feasible. Instead, the previously determined sectors and fit constants are used to estimate the hit positions of each track.

It is possible that a single track is compatible with multiple valid 8-layer patterns if it traverses a region of overlapping silicon modules. In this case, the pattern corresponding to the sector with the most tracks in the sectors-and-constants production step is selected.

The multiplicity of tracks producing the same pattern is referred to as the pattern's coverage. Patterns with a high coverage are the most important for finding tracks. The full set of unique pattern candidates, ordered by region, coverage, and sector, is called the Thin Space Pattern (TSP) bank.

The standard 128-PU FTK configuration allows 2^{24} (16.8 million) patterns per tower to be stored in the AM chips. The use of DC bits (see section 3.7) increases the effective number of patterns stored in the available hardware. Including a DC bit within a pattern results in that pattern being valid for two hit numbers in the respective layer as that bit is always considered a match. Setting a total number of N_X DC bits across all eight layers increases the effective number of patterns stored in the AM's space for a single pattern to 2^{N_X}. For example if a single DC bit is used on two layers of a single pattern, then it is effectively covering four patterns.

With a larger effective number of patterns stored in the AM chips via the use of DC bits, the FTK's track-finding efficiency will increase. However, patterns with many DC bits will suffer from poorer spatial resolution and a higher rate of combinatorial background (fake tracks). Therefore, the maximum number of DC bits per pattern, summed across all layers, is limited to a fixed number ($N_X \leq N_{X,\text{max}}$). This maximum number is adjusted to ensure that the dataflow is kept within the hardware limits. The maximum number of DC bits per pattern is defined separately for the barrel ($N_{X,\text{max}}^{\text{B}}$) and endcap ($N_{X,\text{max}}^{\text{EC}}$) regions, and both are discussed in the following sections. The barrel region consists of the two innermost towers in η, and the remaining outer towers are in the endcap region.

Patterns are selected for storage on the AM chip in order of decreasing coverage. Where possible, patterns are merged with previously stored patterns using DC bits. This process continues until all AM addresses are filled and there is no room to include further pattern candidates. The full set of 2^{24} patterns including DC bits, determined for each of the 64 regions, is termed the AM pattern bank.

The efficiency of an AM pattern bank, as a function of the number of patterns in the bank, is shown in figure 23. The inclusive curve does not always lie between the others because of the inclusion of the barrel/endcap transition region $1.2 < |\eta| < 1.6$, which has a low efficiency. Mitigation of this is discussed in the next section. With 16.8 million patterns per tower in the 128-PU FTK configuration, the track-finding efficiency is on the plateau of the efficiency curve.

5.4 Pattern-bank optimization

The track-finding efficiency of an AM bank as a function of track η is shown in blue in figure 24. In this example, a pattern bank designed for the 64-PU configuration with $N_{X,\text{max}}^{\text{B}} = 9$ and $N_{X,\text{max}}^{\text{EC}} = 6$ is used. Two drops in efficiency are observed at $\eta \approx \pm 1.2$, which is related to the change in geometry from the barrel ($|\eta| < 1.2$) to endcap disk ($1.6 < |\eta| < 2.5$) detector layers in these regions. To make the efficiency more uniform as a function of η, TSP patterns are reassigned to AM addresses in bins of η. A larger budget of AM addresses is assigned to η bins with low efficiency. To keep the overall number of AM addresses constant, the budget of AM addresses in η bins with a high efficiency is lowered accordingly. This iterative process, called partitioning, is repeated until the track-finding efficiency is roughly constant as a function of η. The track-finding efficiency of the AM bank after partitioning is shown in red in figure 24. The remaining variation in the efficiency is likely due to a binning-like effect of the procedure where the sectors are assigned to one η bin, while in reality they have a shape in η. The relative change in efficiency with more patterns is roughly similar to that shown in figure 23. Thus, in order to improve the efficiency from roughly 80% to 90%, the number of patterns needs to be increased by a factor of 3–4.
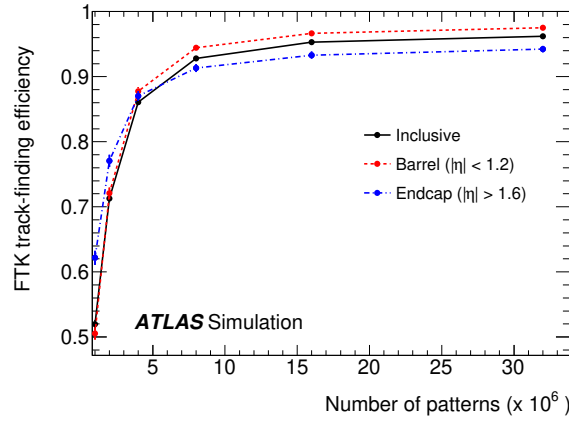
Figure 23. Track-finding efficiency, relative to the Monte Carlo 'truth record', of the Associative Memory pattern bank as a function of the number of patterns in the bank. Tracks are taken from a single-muon Monte Carlo simulation sample and are required to have $|z_0| < 110$ mm and $|d_0| < 2.2$ mm. The efficiency is calculated separately for all tracks with $|\eta| < 2.5$ (black), for tracks in the barrel region with $|\eta| < 1.2$ (red), and for tracks in the endcap region with $1.6 < |\eta| < 2.5$ (blue). The barrel/endcap transition region $1.2 < |\eta| < 1.6$ is excluded from the latter two as it has a low efficiency before mitigation is applied.
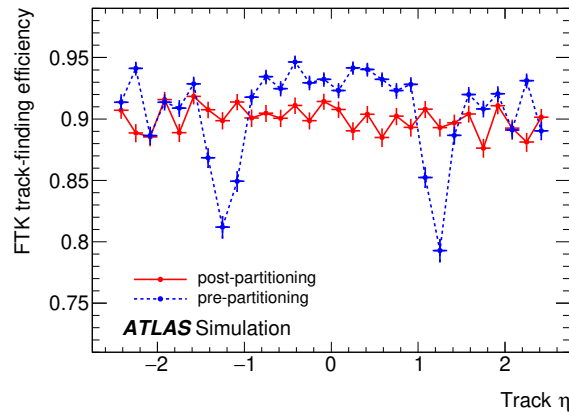
Figure 24. FTK track-finding efficiency, relative to the Monte Carlo 'truth record', as a function of the track η, before and after applying partitioning. Tracks are taken from a single-muon Monte Carlo sample and are required to have $|z_0| < 110$ mm and $|d_0| < 2.2$ mm. The pattern bank is created for a 64-Processing-Unit configuration, with $N_{X,\max}^{\mathrm{B}} = 9$ and $N_{X,\max}^{\mathrm{EC}} = 6$.

5.5 Production of a pattern bank for commissioning of the 128-PU system

In 2018, the FTK was commissioned with a pattern bank compatible with a 64-PU system, with $N_{X,\max}^{\mathrm{B}} = 9$ and $N_{X,\max}^{\mathrm{EC}} = 6$. The full FTK system is designed to have 128-PUs, allowing the storage of twice as many patterns. To facilitate the scaling up of the FTK system from a 64-PU to a 128-PU system, a new pattern bank was created. With more patterns in the pattern bank, a higher track-finding efficiency is expected. However, more patterns also results in a higher dataflow rate. In order to keep the dataflow within the limits of the hardware, the maximum number of DC bits was adjusted.

Two 128-PU pattern banks were created with different DC bit configurations. The configuration with fewer DC bits ($N_{X,\text{max}}^{\text{B}} = 7$ and $N_{X,\text{max}}^{\text{EC}} = 4$) has narrower patterns and therefore a lower dataflow rate, while the configuration with more DC bits ($N_{X,\text{max}}^{\text{B}} = 9$ and $N_{X,\text{max}}^{\text{EC}} = 6$) has wider patterns and a higher dataflow rate. The overall track-finding efficiencies of these two 128-PU banks, compared with the 64-PU bank used previously for commissioning, are listed in table 2. For commissioning, a choice was made to deliberately push the FTK system to its performance limits. The high-dataflow 128-PU bank, with the highest track-finding efficiency, has the highest dataflow rate. Compared to the lower dataflow configuration, at a pile-up of 60, the high-dataflow bank results in about a factor of 2 increase in the number of roads, a factor of 1.4–1.5 increase in the number of 8-layer and 12-layer track candidates, and a factor of 1.1 increase in the number of 12-layer track candidates after overlap removal. To run this configuration at 100 kHz would likely have required reducing the number of track candidates by tuning of the number of fits performed.

The track-finding efficiency of these banks, as a function of track parameter values, is shown in figures 25 and 26. The track-finding efficiency peaks for tracks with low impact parameters (d_0 and z_0) and high p_{T}, and stays roughly constant as a function of track $|\eta|$. The high-dataflow 128-PU bank offers the highest track-finding efficiency across the entire range of all track parameters, with the largest improvement at large d_0 and low p_{T}.

Table 2. Track-finding efficiency of pattern banks with respect to 'truth record' tracks in a single-muon Monte Carlo sample. Only tracks with $|\eta| < 2.5$, $|z_0| < 110$ mm and $|d_0| < 2.2$ mm are considered in the efficiency calculation. Each column indicates the Don't Care bit configuration of the bank $N_{X,\text{max}} = (N_{X,\text{max}}^{\text{B}}, N_{X,\text{max}}^{\text{EC}})$.

Track-finding efficiency of various pattern-bank configurations		
64-PU, $N_{X,\text{max}} = (9,6)$	128-PU, $N_{X,\text{max}} = (7,4)$	128-PU, $N_{X,\text{max}} = (9,6)$
90.0%	91.2%	94.4%

(a)

(b)

Figure 25. FTK track-finding efficiency with respect to the Monte Carlo 'truth record' as a function of the (a) d_0 and (b) z_0 of tracks in a single-muon Monte Carlo sample satisfying $|\eta| < 2.5$, $|z_0| < 110$ mm and $|d_0| < 2.2$ mm. The Don't Care bit configuration, $N_{X,\text{max}} = (N_{X,\text{max}}^{\text{B}}, N_{X,\text{max}}^{\text{EC}})$, and the number of processing units for each pattern bank are specified in the legend.
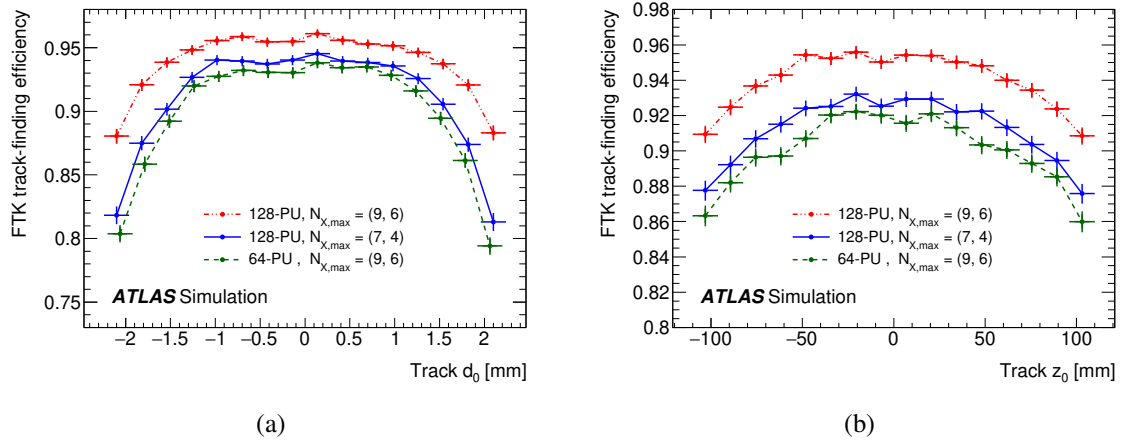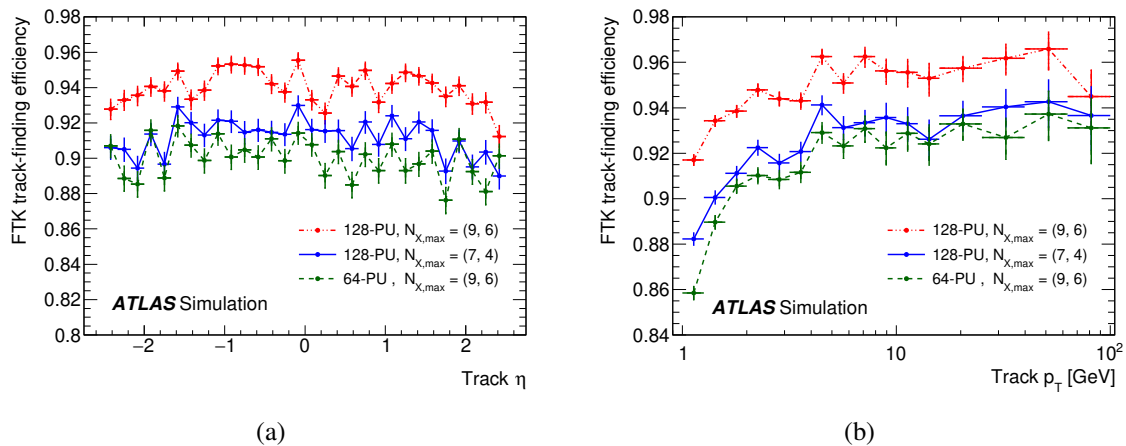
Figure 26. FTK track-finding efficiency with respect to the Monte Carlo 'truth record' as a function of the (a) η and (b) p_T of tracks in a single-muon Monte Carlo sample satisfying $|\eta| < 2.5$, $|z_0| < 110$ mm and $|d_0| < 2.2$ mm. The Don't Care bit configuration, $N_{X,\text{max}} = (N_{X,\text{max}}^{\text{B}}, N_{X,\text{max}}^{\text{EC}})$, and the number of processing units for each pattern bank are specified in the legend.

5.6 Extension of the pattern bank to high-d_0 tracks

As described in section 5.3, the pattern-bank training is performed using a flat distribution of d_0 in order to ensure good coverage for displaced tracks associated with objects such as jets originating from b-hadrons. Since the nominal banks are trained on tracks with $|d_0| < 2.2$ mm, the efficiency is approximately flat for $|d_0| < 1.2$ mm and falls off steeply outside that range, as shown in figure 25(a).

In order to increase the trigger efficiency for possible new long-lived particles, an alternative pattern bank was developed. It has 30% of the patterns dedicated to high-d_0 tracks, extending the coverage to $|d_0| < 10$ mm. This high-d_0 pattern bank was constructed for 128-PUs, a DC bit configuration with $N_{X,\text{max}}^{\text{B}} = 7$ and $N_{X,\text{max}}^{\text{EC}} = 4$ and with nominal detector geometry and conditions. In order to compensate for the increase in the number of patterns required to cover this larger d_0 space, the minimum track p_T was increased to 5 GeV for $|d_0| > 2$ mm.

The resulting track-finding efficiency as a function of both p_T and d_0 is shown in figure 27. In the regions targeted by the training, the FTK track-finding efficiency is over 50%, and for tracks with $|d_0| < 5$ mm and $p_T > 10$ GeV, the efficiency is over 90%.

This bank was produced without reoptimizing the sectors. Sectors correspond to a width of approximately 10 mm, so it is likely that such a reoptimization could increase the efficiency at high d_0, but this was not studied explicitly.

The patterns dedicated to nominal tracks with the highest coverage are preferentially kept, so the 30% reduction in the number of nominal patterns does not translate into a 30% efficiency drop in the nominal low-d_0 region. Figure 28 shows the FTK track-finding efficiency as a function of d_0 for the high-d_0 pattern bank, compared with a pattern bank produced with the exact same configuration but without any high-d_0 patterns. The track-finding efficiency of the high-d_0 bank is reduced by approximately 2% compared to the nominal bank within the nominal $|d_0| < 2$ mm region. For high-p_T tracks, this reduction in efficiency is even smaller.
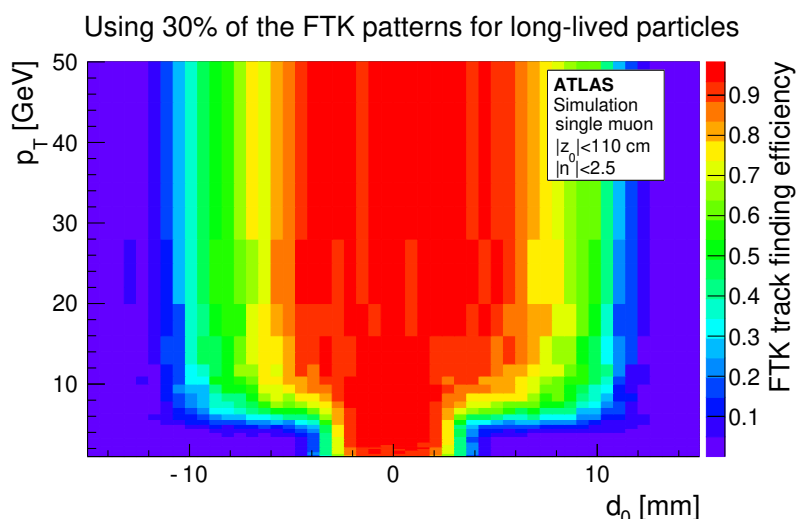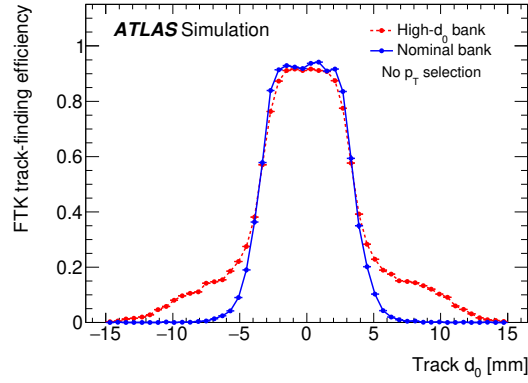
Figure 27. FTK track-finding efficiency with respect to the Monte Carlo 'truth record' as a function of the track p_T and d_0 for the extended d_0 pattern bank. Tracks are taken from a single-muon Monte Carlo sample satisfying $|\eta| < 2.5$ and $|z_0| < 110$ mm. The pattern bank is created with a 128-Processing-Unit configuration, with $N_{X,\max}^{\mathrm{B}} = 7$ and $N_{X,\max}^{\mathrm{EC}} = 4$.

5.7 Comparison of data and simulation

In Run 2, the inputs to the FTK vertical slice were recabled to maximize the track-finding efficiency of a particular central tower without data sharing between multiple DFs. The hardware used corresponds to the boards needed for the 'A' tower data-path in figure 2(b), as described in section 3. This central tower, number 22, covers roughly 1/64th of the ATLAS tracking volume, covering $-1.6 < \eta < 0.1$ and $1.5 < \phi < 2.1$. The data used in the following analysis were collected using 64-PU pattern banks. During LS2, previously recorded data from the ATLAS detector can be replayed via the QNP system (see section 3.2) through the FTK vertical slice in the same way as they would have during Run 2.

Events from an ATLAS run in September of 2018 with an average pile-up of 49 were input into the FTK vertical slice via the QNP system. A total of 192 000 pp collisions were selected for offline analysis. The same ATLAS data were also processed with the FTK simulation in order to compare the output of the hardware with the expectation from simulation. The mean number of FTK tracks found by the hardware per event in the tower is 1.05, compared to an expectation of 1.25 FTK tracks per event from simulation. The distributions of the five track parameters in FTK data vs FTK simulation are compared in figure 29. The shapes of the distributions are well-modelled by the simulation. The small differences seen in these distributions, and in later figures, between FTK data and simulation are likely due to truncations in the hardware (e.g. the number of hits considered per SS) that are not fully replicated in the software.

The FTK tracking efficiency relative to offline tracking is determined by evaluating the probability for each offline track with at least four (six) Pixel (SCT) hits to have a matched FTK track within an angular distance $\Delta R < 0.02$, for offline tracks with $p_T > 2$ GeV in the core of the Tower 22 region defined by $-1.1 < \eta < -0.9$ and $1.6 < \phi < 1.7$. In this region, the average FTK

(a)
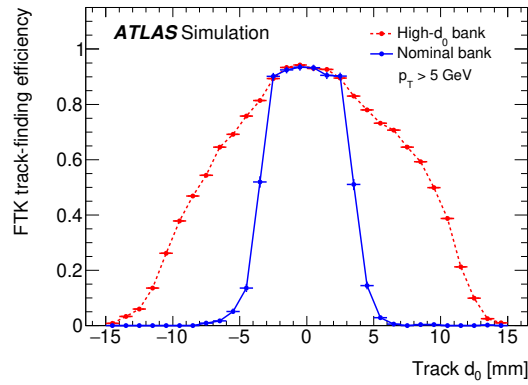
(b)
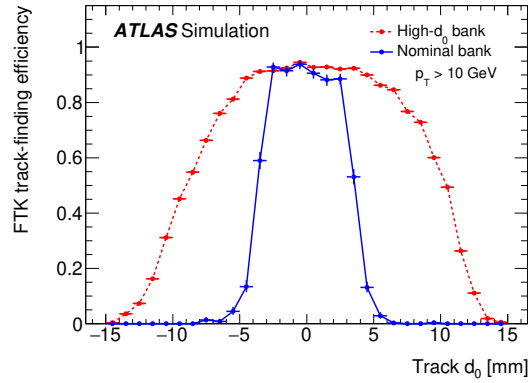
(c)

Figure 28. FTK track-finding efficiency with respect to the Monte Carlo 'truth record' as a function of d_0 for two pattern banks, with (a) no track p_T selection, (b) track $p_T > 5$ GeV and (c) track $p_T > 10$ GeV. Tracks are taken from a single-muon Monte Carlo sample and are required to have $|\eta| < 2.5$, $|z_0| < 110$ mm. The nominal bank (blue) only includes patterns for tracks with $|d_0| < 2$ mm, and the high-d_0 bank (red) has 30% of its patterns dedicated to tracks with $2 < |d_0| < 10$ mm and $p_T > 5$ GeV. Both banks are constructed with 128-Processing-Unit configuration, a Don't Care bit configuration with $N^{\rm B}_{X,\rm max} = 7$ and $N^{\rm EC}_{X,\rm max} = 4$, and with the nominal detector geometry and conditions.
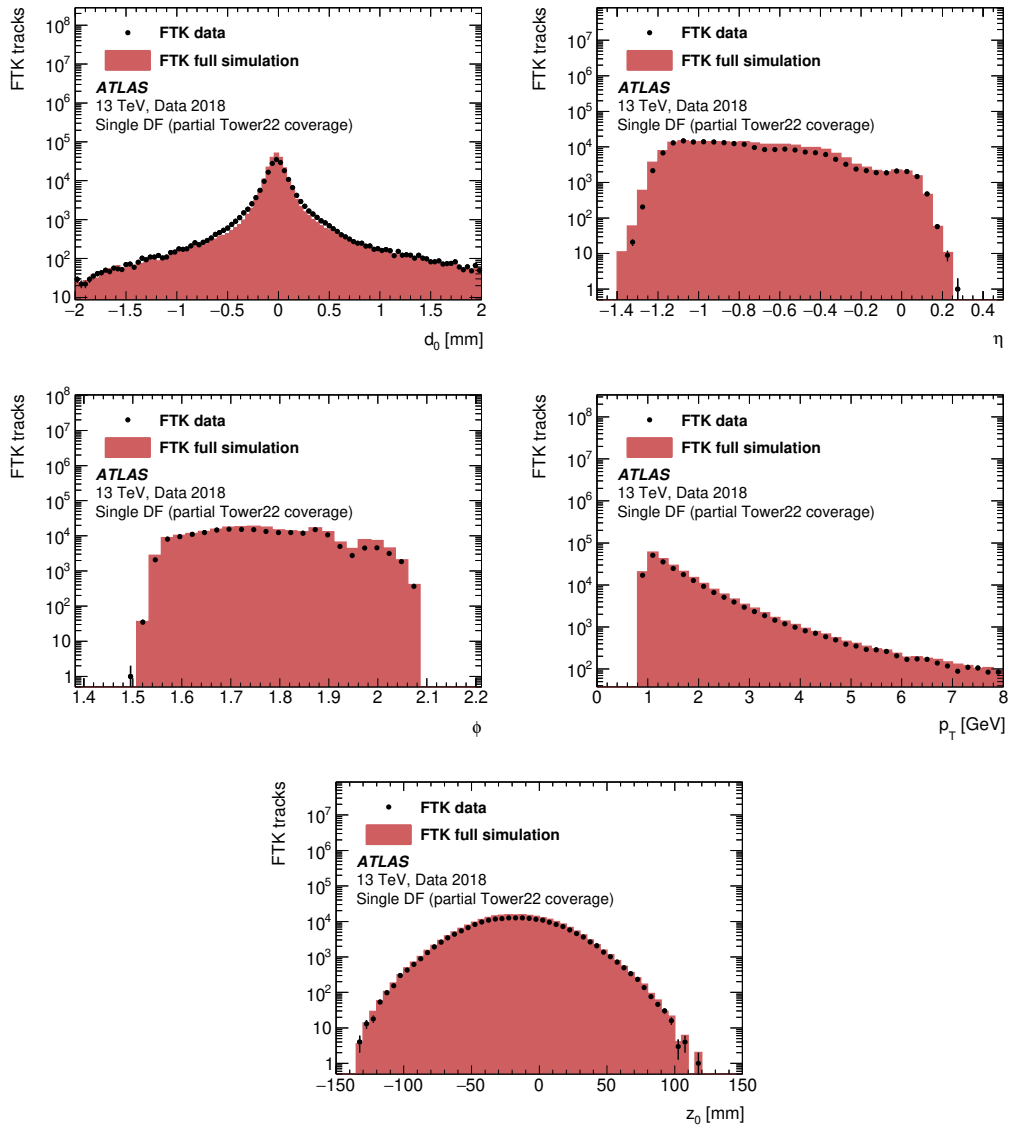
Figure 29. The distributions of the five track parameters in FTK data (solid black circles) and FTK simulation (red histogram) run over the same ATLAS data.

tracking efficiency relative to offline tracks is 67%, compared to an expectation of 69% from FTK simulation. Due to the incomplete geometric coverage and lack of data sharing of the FTK vertical slice, the FTK tracking efficiency is not expected to approach the values given in table 2. The tracking efficiency as a function of the five track parameters is presented in figure 30.

The fraction of FTK tracks matched to offline tracks within $\Delta R < 0.02$ is 98% in FTK data compared to an expectation of 99% in FTK simulation, demonstrating that the FTK is not reconstructing large rates of spurious tracks due to random hit combinations.

The FTK track parameter residuals relative to offline tracks are shown in figure 31, separately for FTK vertical slice data and FTK simulation. The p_T residual in data agrees well with expectations from simulation, while the other track parameters are slightly worse in data than in simulation.
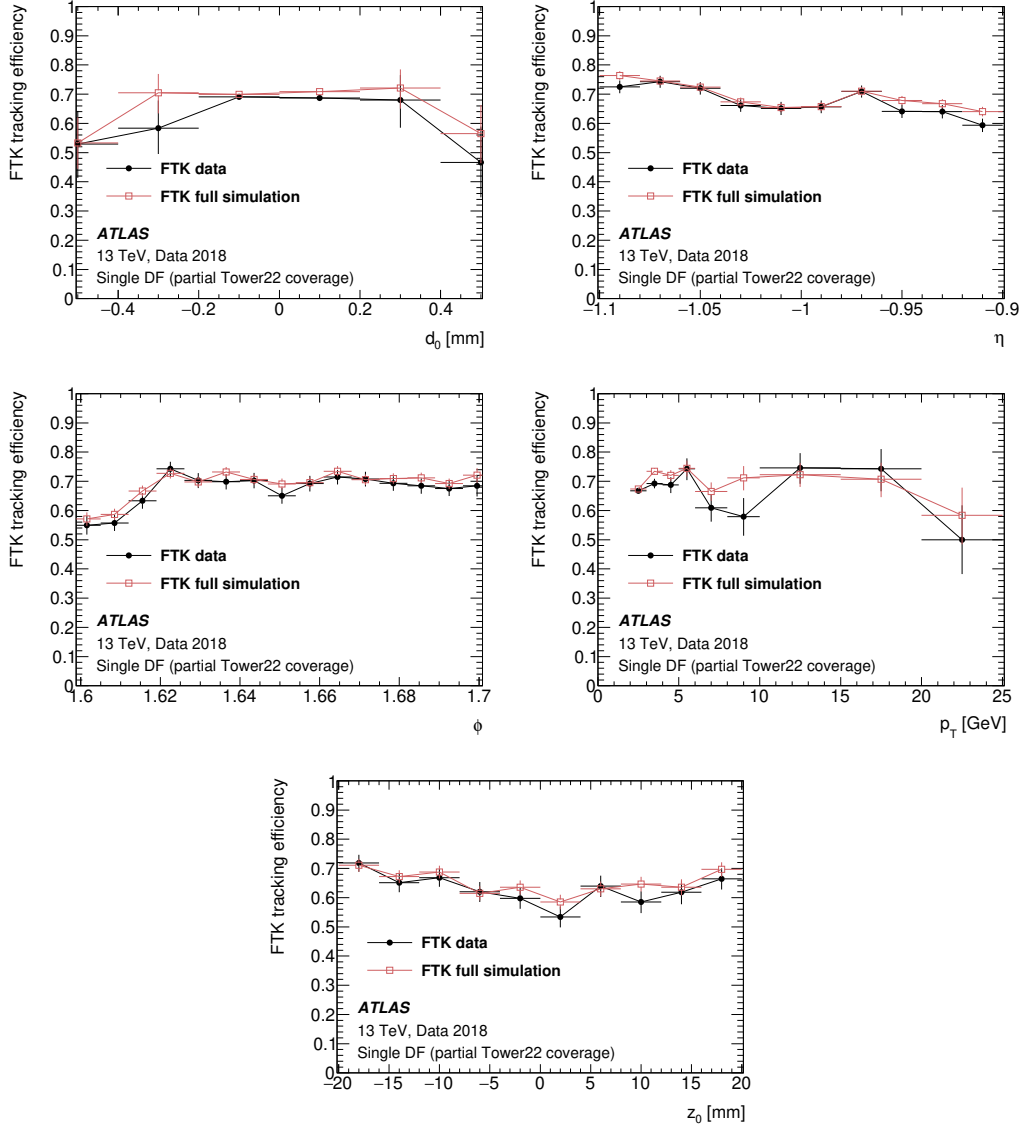
Figure 30. The FTK tracking efficiency relative to offline tracks, as a function of the five track parameters, in FTK data (solid black circles) and FTK simulation (open red squares). An offline track is considered to be matched to FTK tracks with $\Delta R < 0.02$. Only tracks in the core Tower 22 region defined by $-1.1 < \eta < -0.9$ and $1.6 < \phi < 1.7$ are considered here. The error bars show the statistical uncertainties for the data and simulation, which are correlated with each other because the same input data are used.
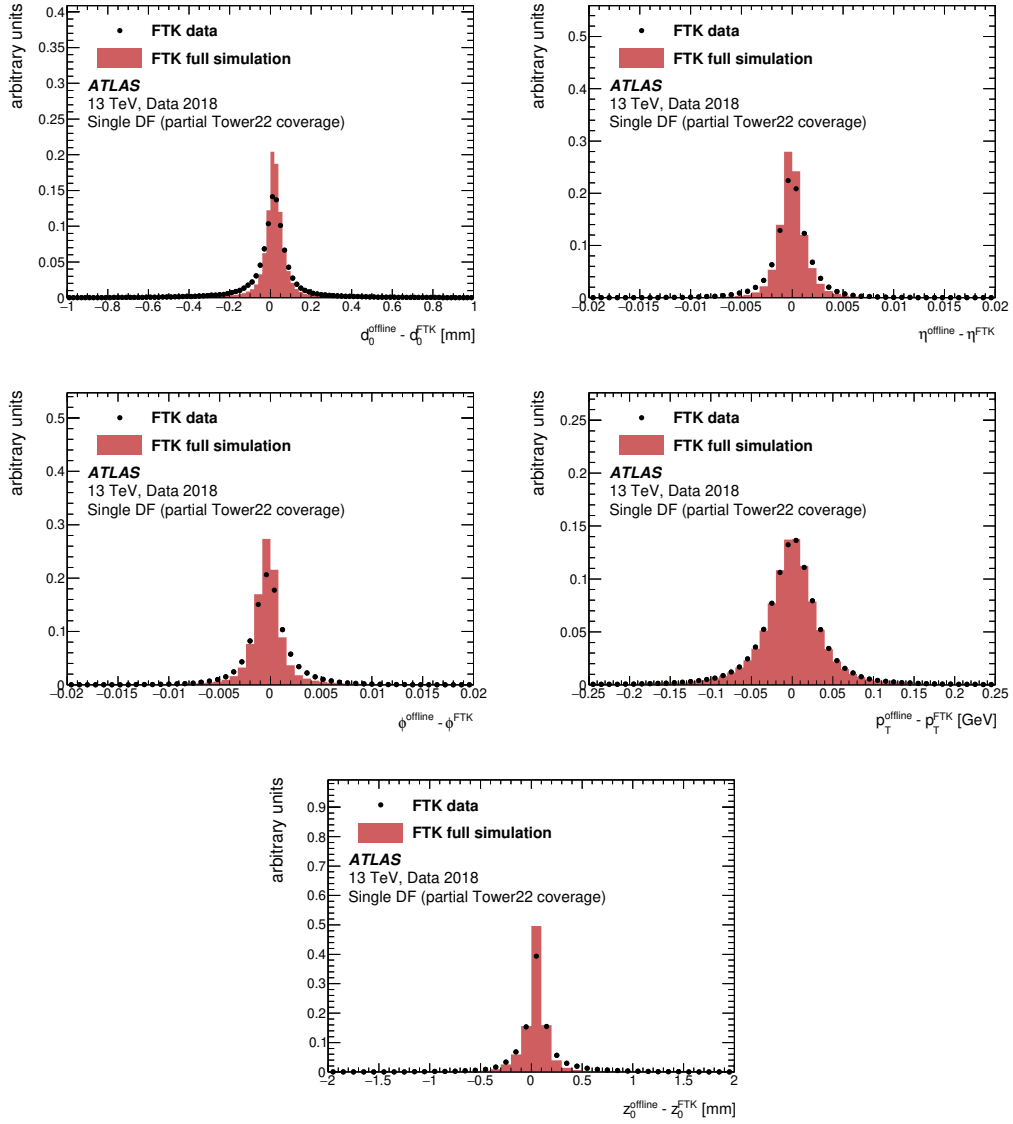
Figure 31. The FTK track parameter residuals relative to offline tracks, as a function of the five track parameters, in FTK data (black dots) and FTK simulation (red histogram). For each quantity, the difference between the FTK and offline track parameter values is shown.

6 Conclusion

The FTK system was designed to provide tracks to the HLT using custom hardware composed of AM chips and FPGAs in order to improve the ATLAS HLT trigger performance. The FTK system, the supporting software and a data playback facility are presented. These systems were used for commissioning at the end of Run 2 data-taking and during LS2, before the project was stopped in 2019. The pattern recognition and track-fitting performance of the FTK system has been demonstrated with a functional simulation of the system and in a vertical slice of the FTK. The vertical slice shows that the as-built performance of the FTK system components and the associated firmware is capable of reproducing the performance expected from the simulation, with only very small differences. Integration of the vertical slice into the ATLAS run control and regular inclusion in data-taking during 2018 demonstrate the functionality of the software, control, and monitoring. Simulation studies of the pattern banks designed to be used in the FTK system show that a track-finding efficiency of 94.4% for muons above 1 GeV without additional pile-up could be reached for a system with the full complement of 128 PUs, as was foreseen for Run 3 of the LHC. For the FTK configuration with 64 PUs, the simulation shows an efficiency of 90.0%. Simulation studies with 30% of the FTK patterns dedicated to high-p_T tracks with large impact parameters (d_0) show that the efficiency for tracks with $|d_0| < 10$ mm could be significantly increased at a cost of 2% in the overall efficiency.

References

[1] ATLAS collaboration, *Fast TracKer (FTK) technical design report*, CERN-LHCC-2013-007 (2013).

[2] ATLAS collaboration, *The ATLAS experiment at the CERN Large Hadron Collider*, 2008 *JINST* **3** S08003.

[3] ATLAS collaboration, *Performance of the ATLAS Trigger System in 2010*, *Eur. Phys. J. C* **72** (2012) 1849 [arXiv:1110.1530].

[4] ATLAS collaboration, *Performance of the ATLAS Trigger System in 2015*, *Eur. Phys. J. C* **77** (2017) 317 [arXiv:1611.09661].

[5] ATLAS collaboration, *Trigger menu in 2018*, ATL-DAQ-PUB-2019-001 (2019).

[6] ATLAS collaboration, *Performance and improvements of the ATLAS jet trigger system*, *Nucl. Instrum. Meth. A* **718** (2013) 253.

[7] ATLAS collaboration, *The performance of the jet trigger for the ATLAS detector during 2011 data taking*, *Eur. Phys. J. C* **76** (2016) 526 [arXiv:1606.07759].

[8] ATLAS collaboration, *Jet reconstruction and performance using particle flow with the ATLAS Detector*, *Eur. Phys. J. C* **77** (2017) 466 [arXiv:1703.10485].

[9] ATLAS collaboration, *Performance of the missing transverse momentum triggers for the ATLAS detector during Run-2 data taking*, *JHEP* **08** (2020) 080 [arXiv:2005.09554].

[10] ATLAS collaboration, *Search for pair production of Higgs bosons in the $b\bar{b}b\bar{b}$ final state using proton-proton collisions at $\sqrt{s} = 13$ TeV with the ATLAS detector*, *JHEP* **01** (2019) 030 [arXiv:1804.06174].

[11] ATLAS collaboration, *Search for heavy charged long-lived particles in the ATLAS detector in 36.1 fb^{-1} of proton-proton collision data at $\sqrt{s} = 13$ TeV*, *Phys. Rev. D* **99** (2019) 092007 [arXiv:1902.01636].

[12] ATLAS collaboration, *Searches for electroweak production of supersymmetric particles with compressed mass spectra in $\sqrt{s} = 13$ TeV pp collisions with the ATLAS detector*, *Phys. Rev. D* **101** (2020) 052005 [arXiv:1911.12606].

[13] B.A. Petersen and C. Schwick, *Experiment requests and constraints for Run 3*, in the proceedings of the 9th *LHC Operations Evian Workshop*, January 30–February 1, Evian Les Bains, France (2019).

[14] ATLAS TDAQ collaboration, *The ATLAS data acquisition and high level trigger system*, 2016 *JINST* **11** P06008.

[15] ATLAS collaboration, *ATLAS insertable B-Layer: technical design report*, ATLAS-TDR-19 (2010).

[16] ATLAS IBL collaboration, *Production and integration of the ATLAS Insertable B-Layer*, 2018 *JINST* **13** T05008 [arXiv:1803.00844].

[17] M. Dell'Orso and L. Ristori, *VLSI structures for track finding*, *Nucl. Instrum. Meth. A* **278** (1989) 436.

[18] J.A. Adelman et al., *The Silicon Vertex Trigger upgrade at CDF*, *Nucl. Instrum. Meth. A* **572** (2007) 361.

[19] A. Annovi et al., *AM06: the associative memory chip for the fast TracKer in the upgraded ATLAS detector*, 2017 *JINST* **12** C04013.

[20] Advanced telecom computing architecture, https://www.picmg.org/openstandards/advancedtca/.

[21] W. Vandelli et al., *Evolution of the ReadOut system of the ATLAS experiment*, PoS(TIPP2014)205.

[22] H. C. van der Bij, R.A. McLaren, O. Boyle and G. Rubin, *S-LINK, a data link interface specification for the LHC era*, *IEEE Nucl. Sci. Symp. Conf. Rec.* **44** (1996) 398.

[23] E. van der Bij, R.A. McLaren and Z. Meggyesi, *S-LINK: a prototype of the ATLAS read-out link*, 4th *Workshop on Electronics for LHC Experiments (LEB 98)*, September 21–25, Rome, Italy (1998).

[24] *IEEE standard for a versatile backplane bus: VMEbus*, ANSI/IEEE Std 1014-1987 (1987).

[25] G. Thomas, *Rack cooling project — Final report*, EPESS-2003-014 (2002).

[26] C.L. Sotiropoulou et al., *The Associative Memory system infrastructures for the ATLAS Fast Tracker*, *IEEE Trans. Nucl. Sci.* **64** (2017) 1248.

[27] Sanyo Denki, *Dc fan san ace 120 9hv1248p1g001*, https://products.sanyodenki.com/en/sanace/dc/dc-fan/9HV1248P1G001/.

[28] Costruzioni apparecchiature elettroniche nucleari s.p.a., https://www.caen.it.

[29] S. Sottocornola et al., *Cooling and timing tests of the ATLAS Fast Tracker VME boards*, ATL-DAQ-PROC-2020-020 (2020).

[30] ASIS-Pro, https://www.asis-pro.com.

[31] Unipower (formerly power-one), https://unipowerco.com/products/300-amp-dc-power-system-guardian-access3u/.

[32] G. Balbi, D. Falchieri, A. Gabrielli, L. Lama, N. Giangiacomi and R. Travaglini, *ATLAS Pixel Detector ROD card from IBL towards Layers 2 and 1*, 2016 *JINST* **11** C01021.

[33] A. Abdesselam et al., *The data acquisition and calibration system for the ATLAS semiconductor tracker*, 2008 *JINST* **3** P01003.

[34] A. Borga et al., *The C-RORC PCIe card and its application in the ALICE and ATLAS experiments*, 2015 *JINST* **10** C02022.

[35] Xilinx Incorporated, *Virtex-6 family overview*, https://www.xilinx.com/support/documentation/data_sheets/ds150.pdf.

[36] S. Kolos, G. Boutsioukis and R. Hauser, *High-performance scalable information service for the ATLAS experiment*, *J. Phys. Conf. Ser.* **396** (2012) 012026.

[37] Grafana Labs, *Grafana*, https://grafana.com.

[38] W. Dabrowski et al., *Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS semiconductor tracker*, *IEEE Trans. Nucl. Sci.* **47** (2000) 1843.

[39] C.L. Sotiropoulou et al., *A multi-core fpga-based 2d-clustering implementation for real-time image processing*, *IEEE Trans. Nucl. Sci.* **61** (2014) 3599.

[40] Xilinx Incorporated, *Spartan-6 family overview*, https://www.xilinx.com/support/documentation/data_sheets/ds160.pdf.

[41] Xilinx Incorporated, *7 series FPGAs data sheet: overview*, https://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf.

[42] J. Olsen, T. Liu and Y. Okumura, *A full mesh ATCA-based general purpose data processing board*, 2014 *JINST* **9** C01041.

[43] Y. Okumura et al., *ATCA-based ATLAS FTK input interface system*, 2015 *JINST* **10** C04032 [arXiv:1411.0661].

[44] Altera, *Arria V FPGA and SoC features*, ttps://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pt/arria-v-product-table.pdf.

[45] L. Frontini, S. Shojaii, A. Stabile and V. Liberali, *A new Xor-based content addressable memory architecture*, *2012 19th IEEE Int. Conf. Electron. Circ. Syst.* (2012) 701.

[46] Xilinx Incorporated, *Spartan-3 family overview*, https://www.xilinx.com/support/documentation/data_sheets/ds706.pdf.

[47] J. Adelman et al., *ATLAS FTK challenge: simulation of a billion-fold hardware parallelism*, *Proc. COmput. Sci.* **66** (2015) 540.

[48] R. Brun and F. Rademakers, *ROOT: an object oriented data analysis framework*, *Nucl. Instrum. Meth. A* **389** (1997) 81.

[49] ATLAS collaboration, *ATLAS computing: technical design report*, CERN-LHCC-2005-022 (2005).

[50] G. Guennebaud et al., *Eigen v3*, http://eigen.tuxfamily.org.

[51] A. Hass, *ATLAS simulation using real data: embedding and overlay*, *J. Phys. Conf. Ser.* **898** (2017) 042004.

[52] ATLAS collaboration, *ATLAS computing acknowledgements*, ATL-SOFT-PUB-2020-001 (2020).

The ATLAS collaboration

G. Aad[101], B. Abbott[127], D.C. Abbott[102], A. Abed Abud[36], K. Abeling[53], D.K. Abhayasinghe[93], S.H. Abidi[29], O.S. AbouZeid[40], N.L. Abraham[156], H. Abramowicz[161], H. Abreu[160], Y. Abulaiti[6], B.S. Acharya[66a,66b,o], B. Achkar[53], L. Adam[99], C. Adam Bourdarios[5], L. Adamczyk[83a], L. Adamek[165], J. Adelman[120], A. Adiguzel[12c,ad], S. Adorni[54], T. Adye[143], A.A. Affolder[145], Y. Afik[160], C. Agapopoulou[64], M.N. Agaras[38], A. Aggarwal[118], C. Agheorghiesei[27c], J.A. Aguilar-Saavedra[139f,139a,ac], A. Ahmad[36], F. Ahmadov[79], W.S. Ahmed[103], X. Ai[18], G. Aielli[73a,73b], S. Akatsuka[85], M. Akbiyik[99], T.P.A. Åkesson[96], E. Akilli[54], A.V. Akimov[110], K. Al Khoury[64], G.L. Alberghi[23b,23a], J. Albert[174], P. Albicocco[51], M.J. Alconada Verzini[161], S. Alderweireldt[36], M. Aleksa[36], I.N. Aleksandrov[79], C. Alexa[27b], T. Alexopoulos[10], A. Alfonsi[119], F. Alfonsi[23b,23a], M. Alhroob[127], B. Ali[141], S. Ali[158], M. Aliev[164], G. Alimonti[68a], J. Alison[37], C. Allaire[36], B.M.M. Allbrooke[156], P.P. Allport[21], A. Aloisio[69a,69b], F. Alonso[88], C. Alpigiani[148], E. Alunno Camelia[73a,73b], M. Alvarez Estevez[98], M.G. Alviggi[69a,69b], Y. Amaral Coutinho[80b], A. Ambler[103], L. Ambroz[133], C. Amelung[36], D. Amidei[105], S.P. Amor Dos Santos[139a], S. Amoroso[46], C.S. Amrouche[54], C. Anastopoulos[149], N. Andari[144], T. Andeen[11], J.K. Anders[20], J.T. Anderson[6], S.Y. Andrean[45a,45b], A. Andreazza[68a,68b], V. Andrei[61a], C.R. Anelli[174], S. Angelidakis[9], A. Angerami[39], A.V. Anisenkov[121b,121a], A. Annovi[71a], C. Antel[54], M.T. Anthony[149], E. Antipov[128], M. Antonelli[51], D.J.A. Antrim[18], F. Anulli[72a], M. Aoki[81], J.A. Aparisi Pozo[172], M.A. Aparo[156], L. Aperio Bella[46], N. Aranzabal[36], V. Araujo Ferraz[80a], R. Araujo Pereira[80b], C. Arcangeletti[51], A.T.H. Arce[49], J-F. Arguin[109], S. Argyropoulos[52], J.-H. Arling[46], A.J. Armbruster[36], A. Armstrong[169], O. Arnaez[165], H. Arnold[119], Z.P. Arrubarrena Tame[113], G. Artoni[133], H. Asada[116], K. Asai[125], S. Asai[162], T. Asawatavonvanich[163], N. Asbah[59], E.M. Asimakopoulou[170], L. Asquith[156], J. Assahsah[35e], K. Assamagan[29], R. Astalos[28a], R.J. Atkin[33a], M. Atkinson[171], N.B. Atlay[19], H. Atmani[64], P.A. Atmasiddha[105], K. Augsten[141], V.A. Austrup[180], G. Avolio[36], M.K. Ayoub[15c], G. Azuelos[109,ak], D. Babal[28a], H. Bachacou[144], K. Bachas[135b], F. Backman[45a,45b], P. Bagnaia[72a,72b], M. Bahmani[84], H. Bahrasemani[152], A.J. Bailey[172], V.R. Bailey[171], J.T. Baines[143], C. Bakalis[10], O.K. Baker[181], P.J. Bakker[119], E. Bakos[16], D. Bakshi Gupta[8], S. Balaji[157], R. Balasubramanian[119], E.M. Baldin[121b,121a], P. Balek[178], F. Balli[144], W.K. Balunas[133], J. Balz[99], E. Banas[84], M. Bandieramonte[138], A. Bandyopadhyay[19], L. Barak[161], W.M. Barbe[38], E.L. Barberio[104], D. Barberis[55b,55a], M. Barbero[101], G. Barbour[94], T. Barillari[114], M-S. Barisits[36], J. Barkeloo[130], T. Barklow[153a], B.M. Barnett[143], R.M. Barnett[18], Z. Barnovska-Blenessy[60a], A. Baroncelli[60a], G. Barone[29], A.J. Barr[133], L. Barranco Navarro[45a,45b], F. Barreiro[98], J. Barreiro Guimarães da Costa[15a], U. Barron[161], S. Barsov[137], F. Bartels[61a], R. Bartoldus[153a], G. Bartolini[101], A.E. Barton[89], P. Bartos[28a], A. Basalaev[46], A. Basan[99], A. Bassalat[64,ah], M.J. Basso[165], C.R. Basson[100], R.L. Bates[57], S. Batlamous[35f], J.R. Batley[32], B. Batool[151], M. Battaglia[145], M. Bauce[72a,72b], F. Bauer[144,*], P. Bauer[24], H.S. Bawa[31], A. Bayirli[12c], J.B. Beacham[49], T. Beau[134], P.H. Beauchemin[168], F. Becherer[52], P. Bechtle[24], H.P. Beck[20,q], K. Becker[176], C. Becot[46], A. Beddall[12d], A.J. Beddall[12a], V.A. Bednyakov[79], C.P. Bee[155], T.A. Beermann[180], M. Begalli[80b], M. Begel[29], A. Behera[155], J.K. Behr[46], F. Beisiegel[24], M. Belfkir[5], G. Bella[161], L. Bellagamba[23b], A. Bellerive[34], P. Bellos[21], K. Beloborodov[121b,121a], K. Belotskiy[111], N.L. Belyaev[111], D. Benchekroun[35a], N. Benekos[10], Y. Benhammou[161], D.P. Benjamin[6], M. Benoit[29], J.R. Bensinger[26], S. Bentvelsen[119], L. Beresford[133], M. Beretta[51], D. Berge[19], E. Bergeaas Kuutmann[170], N. Berger[5], B. Bergmann[141], L.J. Bergsten[26], J. Beringer[18], S. Berlendis[7], G. Bernardi[134], C. Bernius[153a], F.U. Bernlochner[24], T. Berry[93], P. Berta[99], A. Berthold[48], I.A. Bertram[89], O. Bessidskaia Bylund[180], S. Bethke[114], A. Betti[42], A.J. Bevan[92], S. Bhatta[155], D.S. Bhattacharya[175], P. Bhattarai[26], V.S. Bhopatkar[6], R. Bi[138], R.M. Bianchi[138], O. Biebel[113], D. Biedermann[19], R. Bielski[36], K. Bierwagen[99], N.V. Biesuz[71a,71b], M. Biglietti[74a], T.R.V. Billoud[141], M. Bindi[53], A. Bingul[12d], C. Bini[72a,72b], S. Biondi[23b,23a], C.J. Birch-sykes[100], M. Birman[178], T. Bisanz[36], J.P. Biswal[3], D. Biswas[179,j], A. Bitadze[100], C. Bittrich[48], K. Bjørke[132], R.E. Blair[6], T. Blazek[28a], I. Bloch[46], C. Blocker[26], A. Blue[57],

U. Blumenschein[92], G.J. Bobbink[119], V.S. Bobrovnikov[121b,121a], D. Bogavac[14], M. Bogdan[37],
A.G. Bogdanchikov[121b,121a], C. Bohm[45a], V. Boisvert[93], P. Bokan[170,53], T. Bold[83a], M. Bomben[134],
M. Bona[92], J.S. Bonilla[130], M. Boonekamp[144], C.D. Booth[93], A.G. Borbély[57], H.M. Borecka-Bielska[90],
L.S. Borgna[94], A. Borisov[122], G. Borissov[89], D. Bortoletto[133], D. Boscherini[23b], M. Bosman[14],
J.D. Bossio Sola[103], K. Bouaouda[35a], J. Boudreau[138], E.V. Bouhova-Thacker[89], D. Boumediene[38],
R. Bouquet[134], G. Bourlis[135a], A. Boveia[126], J. Boyd[36], D. Boye[33c], I.R. Boyko[79], A.J. Bozson[93],
J. Bracinik[21], N. Brahimi[60d,60c], G. Brandt[180], O. Brandt[32], F. Braren[46], B. Brau[102], J.E. Brau[130],
W.D. Breaden Madden[57], K. Brendlinger[46], R. Brener[160], L. Brenner[36], R. Brenner[170], S. Bressler[178],
B. Brickwedde[99], D.L. Briglin[21], D. Britton[57], D. Britzger[114], I. Brock[24], R. Brock[106], G. Brooijmans[39],
W.K. Brooks[146d], E. Brost[29], P.A. Bruckman de Renstrom[84], B. Brüers[46], D. Bruncko[28b], A. Bruni[23b],
G. Bruni[23b], M. Bruschi[23b], N. Bruscino[72a,72b], P. Bryant[37], L. Bryngemark[153a], T. Buanes[17], Q. Buat[155],
P. Buchholz[151], A.G. Buckley[57], I.A. Budagov[79], M.K. Bugge[132], O. Bulekov[111], B.A. Bullard[59],
T.J. Burch[120], S. Burdin[90], C.D. Burgard[46], A.M. Burger[128], B. Burghgrave[8], J.T.P. Burr[46], C.D. Burton[11],
J.C. Burzynski[102], V. Büscher[99], E. Buschmann[53], P.J. Bussey[57], J.M. Butler[25], C.M. Buttar[57],
J.M. Butterworth[94], W. Buttinger[143], C.J. Buxo Vazquez[106], A.R. Buzykaev[121b,121a], G. Cabras[23b,23a],
S. Cabrera Urbán[172], D. Caforio[56], H. Cai[138], V.M.M. Cairo[153a], O. Cakir[4a], N. Calace[36], P. Calafiura[18],
G. Calderini[134], P. Calfayan[65], G. Callea[57], L.P. Caloba[80b], A. Caltabiano[73a,73b], S. Calvente Lopez[98],
D. Calvet[38], S. Calvet[38], T.P. Calvet[101], M. Calvetti[71a,71b], R. Camacho Toro[134], S. Camarda[36],
D. Camarero Munoz[98], P. Camarri[73a,73b], M.T. Camerlingo[74a,74b], D. Cameron[132], C. Camincher[36],
S. Campana[36], M. Campanelli[94], A. Camplani[40], V. Canale[69a,69b], A. Canesse[103], M. Cano Bret[77],
J. Cantero[128], Y. Cao[171], M. Capua[41b,41a], R. Cardarelli[73a], F. Cardillo[172], G. Carducci[41b,41a], T. Carli[36],
G. Carlino[69a], B.T. Carlson[138], E.M. Carlson[174,166a], L. Carminati[68a,68b], R.M.D. Carney[153a], S. Caron[118],
E. Carquin[146d], S. Carrá[46], G. Carratta[23b,23a], J.W.S. Carter[165], T.M. Carter[50], M.P. Casado[14,g],
A.F. Casha[165], E.G. Castiglia[181], F.L. Castillo[172], L. Castillo Garcia[14], V. Castillo Gimenez[172],
N.F. Castro[139a,139e], A. Catinaccio[36], J.R. Catmore[132], A. Cattai[36], V. Cavaliere[29], V. Cavasinni[71a,71b],
E. Celebi[12b], F. Celli[133], K. Cerny[129], A.S. Cerqueira[80a], A. Cerri[156], L. Cerrito[73a,73b], F. Cerutti[18],
A. Cervelli[23b,23a], S.A. Cetin[12b], Z. Chadi[35a], D. Chakraborty[120], J. Chan[179], W.S. Chan[119], W.Y. Chan[90],
J.D. Chapman[32], B. Chargeishvili[159b], D.G. Charlton[21], T.P. Charman[92], M. Chatterjee[20], C.C. Chau[34],
S. Chekanov[6], S.V. Chekulaev[166a], G.A. Chelkov[79,af], B. Chen[78], C. Chen[60a], C.H. Chen[78], H. Chen[15c],
H. Chen[29], J. Chen[60a], J. Chen[39], J. Chen[26], S. Chen[136], S.J. Chen[15c], X. Chen[15b], Y. Chen[60a],
Y-H. Chen[46], H.C. Cheng[62a], H.J. Cheng[15a], A. Cheplakov[79], E. Cheremushkina[122],
R. Cherkaoui El Moursli[35f], E. Cheu[7], K. Cheung[63], T.J.A. Chevalérias[144], L. Chevalier[144], V. Chiarella[51],
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