A Reduced Single-Phase Switched-Diode Cascaded Multilevel Inverter

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Abstract—The cascaded multilevel inverters are suitable topologies when a high number of voltage levels is needed. Nonetheless, cascaded topologies possess the main drawback of a high number of power switches and gate drivers that make sophisticated control, reducing efficiency, and increasing cost. This paper proposes a new fundamental switched-diode topology which capable of generating five positive voltage levels with only three power switches, three power diodes, and three dc voltage sources. Based on a combination of the n number of new fundamental topology two cascaded topologies are proposed which increase the number of voltage levels and decrease the number of power switches and voltage stress. The proposed cascaded topologies can operate in asymmetric dc sources so different dc voltage source magnitudes are submitted to minimize the number of components. The main advantages of the proposed cascaded topologies are reducing the number of power switches and gate drivers with reasonable dc voltage sources count in comparison with other state-of-the-art cascaded topologies. Furthermore, the proposed topologies reduce the cost in comparison with other recently multilevel inverter topologies. The power loss analysis and the recommended application for the proposed topologies are discussed. The simulation and experimental works are presented to verify the operation correctness of the proposed topologies.

Index Terms—Single-phase multilevel power converter, cascaded configurations, symmetrical and asymmetrical.

I. INTRODUCTION

MULTILEVEL power inverters create a higher number of voltage levels compared to the two level inverters that are widely used in medium-voltage high-power applications. Multi-level inverters (MLIs) generate a staircase waveform at the output using a number of lower voltage DC links. The inverters are therefore capable of generating an output voltage waveform with low total harmonic distortions (THDs). In addition, the voltage rating of power semiconductor devices is lower than the overall output voltage because the topologies use many switches in cascade, meaning that the voltage is shared between many devices. Therefore, MLIs can be applied in medium-voltage applications and have some advantages compared to conventional two level power inverters, particularly in some power system conditions including static synchronous compensator (STATCOM), flexible alternating current transmission system (FACTS) devices, electrical vehicle (EV), AC motor drives, renewable energy sources (RES) [1]-[4]. The basic operation of MLIs can be found in three general topologies: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) multilevel inverters [5]-[7]. Some disadvantages of FC and NPC inverters are the voltage magnitude of some of the devices, unbalanced DC-link conditions and the high capacity capacitors. These drawbacks can be solved by using cascaded connections of converter such as the CHB topology, but they require more power semiconductor switching devices [8],[9]. Therefore, researchers have been improving this type of topology based on proposing the new basic units or sub-module topologies, replacing the H-bridge inverter in the cascaded connection.

Recently a number of studies can be found about new multilevel power inverters topologies with a reduced number of power semiconductor devices and DC power supplies in [8]-[20]. In [9]-[11], the authors have developed three single-phase multilevel inverters topologies. In all of these topologies is used a new topology formed from two half-bridge inverters, for example, a back-to-back inverter with two additional power switches in the circuit. The first topology presented [9] has developed for cascaded MLI applications along with several DC power supplies implementation methods. [10] is a generalized topology of [9], and it has extended for additional voltage levels by expanding the basic structure. In [11], the authors have investigated a topology [9],[10] to increase the number of voltage levels by introducing an optimal arrangement. The resulting topology creates all the additional voltage levels without other circuits by changing the polarity of the output voltage, which is an advantage of these topologies. Still, they require a high number of DC power supplies to achieve a high number of voltage levels. A new single-phase basic unit for a multilevel inverter connected to an H-bridge inverter to change the polarity of output voltage suggested in [12]. This asymmetric configuration creates seven output voltage levels with using three DC-links. The cascaded connection has been extended to generate a high number of voltage levels. The main limitation of this topology is the high value of total standing voltage and the high number of power semiconductor devices as well as DC power supplies. In [13], the authors introduced an Enveloped T-type (E-type) inverter using four DC-links and eight power switches, which generate 13-levels in an asymmetric operation mode. The suggested topology in [14] is an improvement of the MLI topology presented in [13], which adds a bidirectional switch to boost the number of voltage levels from 13-levels to 17-levels. This topology called Square T-Type (ST-Type), which generates the 17-levels by four independent DC power supplies. The topology suggested in [15] is an advanced ST-Type topology called the K-Type module. This module uses two extra switches compared to the ST-Type module. It minimizes the number of DC power supplies to half by replacing just two capacitors, thereby producing 13-levels at the output. In [16]-[18], the authors have suggested three different topologies based on H-bridge modules for general multilevel inverter topologies with a reduced number of power semiconductor devices. The

recommended topology in [16] is an extensive topology that can operate in symmetric and asymmetric modes with a basic unit that can be extended to set up additional voltage levels. The suggested topology in [17] is a reconfiguration [16] with a different arrangement of the power semiconductor devices. The idea of the topology presented in [18] is the same with [16] but it requires only two DC power supplies. Other DC power supplies are replaced with capacitors, and some of the switching power devices are replaced with power diodes. In [19],[20], two generalized multilevel inverters have developed for symmetric and asymmetric multilevel inverters. The presented topology in [19] uses a basic unit that has been developed for symmetric and cascaded configurations. This topology uses four unidirectional switches to reduce the standing voltage on the power switches and leads to reduce the power losses. The topology presented in [20] has the same form with [19] that developed for asymmetric multilevel inverters. This topology generates 17-level with the u-n shaped multi-carrier based PWM modulation method.

Another configuration of multilevel inverters is switched-capacitor based MLIs (SC-MLIs) [21]. These groups of MLIs are introduced to minimizing the number of dc voltage sources because usually, they use one or two dc power supplies in the input and other dc sources are replaced by capacitors that can charge in desired voltages by suitable control strategies. SC-MLIs have some drawbacks, they require multiple sensors (voltage/current), costly controllers, signal processing circuits, and sophisticated control algorithms, to deal with the voltage balancing of capacitors [22]. Hence, recently the researchers have been worked to develop SC-MLIs by introducing new configurations or advanced control strategies to balance the capacitor's voltage and mitigate voltage ripples of capacitors [21]-[24]. The authors have introduced two cascaded SC-MLI configurations in [21]. Both presented cascaded MLIs comprised two-stage, the first stage build-up a basic unit that can be developed based on switched capacitors with one input dc voltage source, and the second part is an H-bridge inverter to create AC voltage. The used H-bridge in each basic unit is led to the number of switches increase. The majority of the SC-MLI uses an H-bridge inverter at the output that makes increases the number of power switches and the voltage stress on switches [21],[22].

A novel SC-MLI topology in [23] has been reported to overcome the aforementioned issues. This topology has removed the H-bridge inverter by a new arrangement of switches that can reduce the stress of voltage and also the number of switches. Recently a new SC-MLI has been presented in [24] that doesn't need H-bridge inverter at the output to overcome interesting switch count when high levels are needed. This topology can be developed for more voltage levels by utilizing more switched capacitors easily. Also, the authors have been applied a hybrid pulse width modulation (PWM) strategy to reduce the voltage ripples of capacitors that usually solved by considering larger capacitors. Switched-capacitor MLIs usually operate in symmetrical dc source and can not operate in the asymmetrical dc source so the number of output voltage levels is less than MLIs uses multiple dc voltage sources. Hence, switched-diode multilevel inverters require still a high

number of power switches to generate a high number of levels.

Another type of MLIs is switched-diode base MLIs. In this regard, a few switched-diode base multilevel inverter topologies have been presented to mitigate the components count in the literature [25]-[30]. A general switched-diode MLI has been addressed in [25],[26] with a different algorithm to determine dc source values. These topologies use a general basic topology along with an H-bridge at the output that can extend to a cascaded multilevel inverter. To produce a large number of levels they still need a high number of switches and discrete diodes. The presented switched-diode MLI topology in [27] is a symmetric configuration that makes a limitation in the asymmetric operation in MLIs. Besides, this topology needs both types of bidirectional and unidirectional switches in its circuits that increase the number of IGBTs. A similar multilevel inverter topology has been investigated in [28],[29] with two different objectives. [28] has removed the back-flow current by adding an extra power switch and [29] has mitigated THD value by PWM switching control. These topologies have not been investigated in the asymmetric and cascaded operation so to generate a large number of levels they require a high number of power switches that make a restriction for medium or high power applications. A new topology for switched-diode base MLI has been reported in [30]. The benefits of this topology are operating in asymmetric dc sources and use discrete diodes to reduces switches count. The disadvantage of this MLI is using a high number of dc voltage sources to make a high number of voltage levels. In addition, It still needs a large number of power switches to generate a high number of voltage levels. In addition to discussed MLIs, references [31]-[34] have been presented reduced MLI topologies to minimize devices count and the stress voltage of power switches.

The contribution of this paper is introducing a switched-diodes cascaded MLI topology to decrease the number of power switches and gate drivers with some advantages over recently published topologies. The rest of this paper is organized as follows. In the first, a fundamental switched-diode base topology is proposed. Then the theoretical concepts of the proposed fundamental topology and its cascaded configurations are explained in detail. In section II, a comparison study is made to show the variations among the number of devices, the variety of DC power sources, and total standing voltage for the same number of levels for the proposed topology and other state-of-art MLI topologies. In section IV the power losses calculation is presented and the medium-voltage application of the proposed topology is investigated in section V. The simulations and experimental results finally are analyzed for two case studies.

II. PROPOSED SWITCHED-DIODE MLI CONFIGURATION

The architecture of the proposed fundamental switched-diode multilevel inverter (SD-MLI) shown in Fig. 1(a). The proposed SD-MLI comprises three DC power supplies, three switching semiconductor devices, and three diodes. The typical output voltage of the proposed SD-MLI is exhibited in Fig. 1(b). As can be seen in Fig. 1(b), the proposed inverter can

generate five positive voltage levels, $V_1, V_2, (V_1 + V_2), (V_2 + V_3), (V_1 + V_2 + V_3)$ and a zero level. The switching states of the proposed basic SD-MLI are specified in Table I. In this table, "1" is on-state, "0" is off-state of the switching devices; "F" is forward-bias and "R" is reverse-bias of the diodes. All the valid operating modes of the proposed SD-MLI are shown in Fig. 1(c).
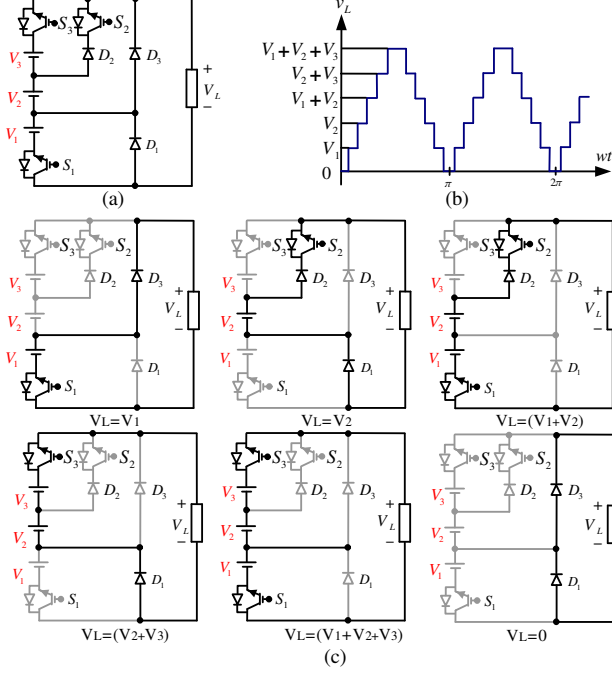

Fig. 1: (a) proposed SD-MLI topology; (b) typical output voltage; (c) operation modes

TABLE I: Switching States of the Proposed SD-MLI

States	S_1	S_2	S_3	D_1	D_2	D_3	V_o
1	1	0	0	R	R	F	V_1
2	0	1	0	F	F	R	V_2
3	1	1	0	R	F	R	$V_1 + V_2$
4	0	0	1	F	R	R	$V_2 + V_3$
5	1	0	1	R	R	R	$V_1 + V_2 + V_3$
6	0	0	0	F	R	F	0

*R: Reverse, F: Forward

In the first mode, switch S_1 is on, and switches S_2, S_3 are off. Hence, diode D_3 is forwarded bias and D_1, D_2 are reversed bias. Therefore, the output voltage level is V_1. In the second operation mode, the voltage level V_2 is generated. For this mode, the switches S_2 is turned on, the switches S_1, S_3 are off. Hence, two diodes D_1, D_2 is forwarding bias, and diode D_3 is in reversed bias. In the third operation mode two switches S_1, S_2 are on, the switch S_3 is off, D_2 is forwarded bias, and two diodes D_1, D_3 are reversed bias. Hence, in this mode, the voltage level of $V_1 + V_2$ is obtained. In the fourth mode, the voltage level of $V_2 + V_3$ is produced. For this mode, the switch S_3 is on, the switches S_1, S_2 are off, D_1 is forwarded bias, and two diodes D_2, D_3 are reversed bias. In the fifth mode, the peak output voltage of $V_1 + V_2 + V_3$ is produced. In this mode, the switches S_1, S_3 are on, the switch S_2 is off, and all three diodes D_1, D_2, D_3 are reversed bias. In the sixth mode, zero

level is produced by turning off all three switches S_1, S_2, S_3. So two diodes D_1, D_3 are forwarded bias and D_2 is reversed bias.

As previously discussed, the proposed SD-MLI can only generate positive voltage levels, so it requires an H-bridge inverter to change the polarity of the output voltage. Besides, the circuit can connect n number of SD-MLIs in series before the H-bridge to increase the number of output levels. The proposed cascaded MLI based on the n number of SD-MLI is displayed in Fig. 2(a). In this topology, each proposed SD-MLI can produce five different voltage levels and a zero level with output voltages of each unit being indicated by $v_{o1}, v_{o2}, \ldots, v_{on}$. Therefore, the total output voltage of the proposed SD-MLI can be calculated as follows:

$$v_o(t) = v_{o1}(t) + v_{o2}(t) + \ldots + v_{on}(t) \tag{1}$$

Table II gives the general output voltage levels of the proposed cascaded MLI. As can be seen from this table, the proposed cascaded topology generates positive levels and requires an H-bridge inverter with four power switches ($H_1 - H_4$) at the output.

Fig. 2(b) shows the proposed cascaded SD-MLI based on the proposed SD-MLI cell. In this topology, with two power switches H_1, H_2 the positive voltage level of $V_L = +V_o$ is created, the negative voltage level of $V_L = -V_o$ is produced with two power switches H_3, H_4 and the zero levels are provided by two pair switches of H_1, H_3 or H_2, H_4. In the proposed cascaded MLI, the number of power switches (or IGBTs) is $3n + 4$, and the number of power diodes is the same with the number of DC power supplies equal to $3n$, which n is the number of basic SD-MLI.

An essential factor in reducing the cost of MLIs is the maximum total standing voltage (TSV). The less TSV leads to the lower price of MLIs as the power electronics devices (IGBTs, diodes) will require a low total standing voltage. However, the maximum TSV of the proposed SD-MLI is the sum of the standing voltages which each power switches and power diodes endure. Regarding Fig. 2(b) the value of TSV for the proposed cascaded MLI can be calculated as follows:

$$TSV = (V_{S1j} + V_{D1j} + V_{S2j} + V_{D2j} \\ + V_{S3j} + V_{D3j}) + (V_{H1} + \ldots + V_{H4}) \tag{2}$$

The magnitude of the maximum standing voltage on each semiconductor device is:

$$V_{S1j} = V_{D1j} = V_{1j} \tag{3}$$

$$V_{S2j} = V_{D2j} = V_{2j} \tag{4}$$

$$V_{S3j} = V_{D3j} = V_{2j} + V_{3j} \tag{5}$$

$$V_{H1} = V_{H2} = V_{H3} = V_{H4} = V_{1j} + V_{2j} + V_{3j} \tag{6}$$

Hence, the total standing voltage on power switches and diodes $S_{1j}, D_{1j}, S_{2j}, D_{2j}, S_{3j}, D_{3j}$ are as follows:

$$V_{standj} = 2(V_{1j} + 2V_{2j} + V_{3j}) \tag{7}$$

The H-bridge inverter will see the full amplitude of the input voltage from the DC power supplies, so the amount of standing voltage seen by the power semiconductor devices is equal to:

$$V_{standH} = 4(V_{1j} + V_{2j} + V_{3j}) \tag{8}$$

TABLE II: Generated Output Voltage Levels Based on Switching States of the Proposed Cascaded SD-MLI (Fig. 2(a))

| No.	V_o	First SD-MLI						Second SD-MLI						...	n^{th} SD-MLI					
		S_{11}	S_{21}	S_{31}	D_{11}	D_{21}	D_{31}	S_{12}	S_{22}	S_{32}	D_{12}	D_{22}	D_{32}	...	S_{1j}	S_{2j}	S_{3j}	D_{1j}	D_{2j}	D_{3j}
1	V_{11}	1	0	0	R	R	F	0	0	0	F	R	F	...	0	0	0	F	R	F
2	V_{21}	0	1	0	F	F	R	0	0	0	F	R	F	...	0	0	0	F	R	F
3	$V_{11}+V_{21}$	1	1	0	R	F	R	0	0	0	F	R	F	...	0	0	0	F	R	F
4	$V_{21}+V_{31}$	0	0	1	F	R	R	0	0	0	F	R	F	...	0	0	0	F	R	F
5	$V_{11}+V_{21}+V_{31}$	1	0	1	R	R	R	0	0	0	F	R	F	...	0	0	0	F	R	F
6	V_{12}	0	0	0	F	R	F	1	0	0	R	R	F	...	0	0	0	F	R	F
7	V_{22}	0	0	0	F	R	F	0	1	0	F	F	R	...	0	0	0	F	R	F
8	$V_{12}+V_{22}$	0	0	0	F	R	F	1	1	0	R	F	R	...	0	0	0	F	R	F
9	$V_{22}+V_{32}$	0	0	0	F	R	F	0	0	1	F	R	R	...	0	0	0	F	R	F
10	$V_{12}+V_{22}+V_{32}$	0	0	0	F	R	F	1	0	1	R	R	R	...	0	0	0	F	R	F
11	$V_{11}+V_{12}$	1	0	0	R	R	F	1	0	0	R	R	F	...	0	0	0	F	R	F
12	$V_{11}+V_{22}$	1	0	0	R	R	F	0	1	0	F	F	R	...	0	0	0	F	R	F
13	$V_{11}+V_{12}+V_{22}$	1	0	0	R	R	F	1	1	0	R	F	R	...	0	0	0	F	R	F
14	$V_{11}+V_{22}+V_{32}$	1	0	0	R	R	F	0	0	1	F	R	R	...	0	0	0	F	R	F
15	$V_{11}+V_{12}+V_{22}+V_{32}$	1	0	0	R	R	F	1	0	1	R	R	R	...	0	0	0	F	R	F
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	...	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
6^n-1	$\sum_{j=1}^{n}V_{1j}+V_{2j}+V_{3j}$	1	0	0	R	R	F	1	0	0	R	R	F	...	1	0	0	R	R	F

*R: Reverse, F: Forward
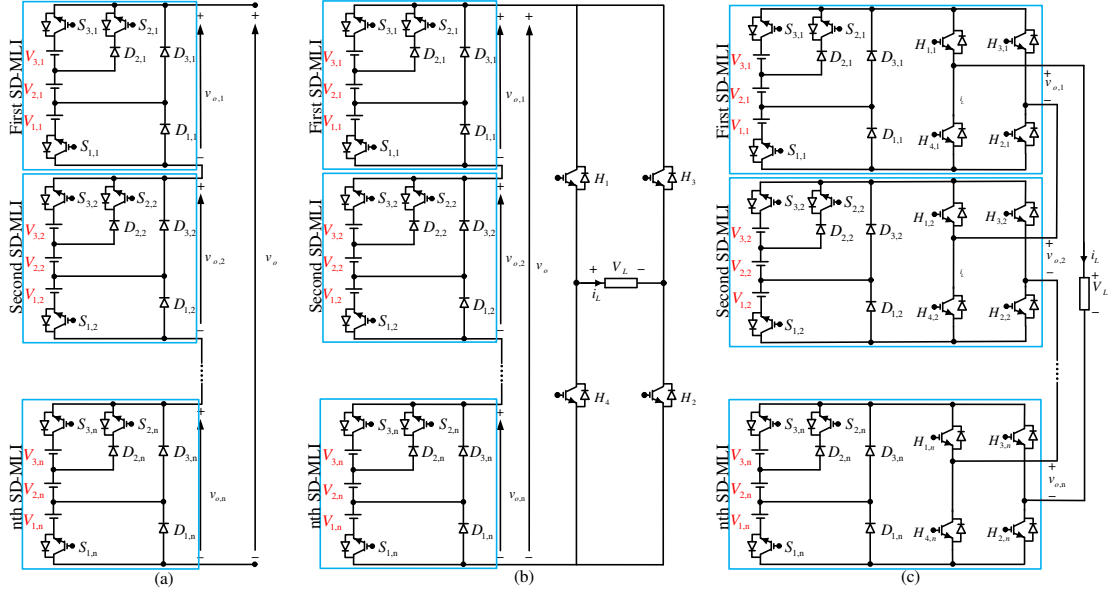
Fig. 2: Extended topology; (a) extended topology based on n SD-MLI topology without h-bridge; (b) extended topology based on n SD-MLI topology with h-bridge; (c) extended topology based on n SD-MLI topology associated with n h-bridge.

Therefore, the maximum standing voltage in the proposed topology is equal to:

$$TSV = \sum_{j=1}^{n} V_{stand\,j} + V_{standH} \qquad (9)$$

As mentioned above, the H-bridge inverter in Fig. 2(b) suffers the peak of output voltage that leads to increase TSV value. Therefore, a recommended cascaded configuration to the reduction of TSV value is proposed in Fig. 2(c). This configuration uses n SD-MLI topology and n H-bridge inverter that leads to increasing the number of power switches with decreasing TSV magnitude.

The proposed extended MLI topology (shown in Fig. 2(b)) can generate different voltage levels at the output, which correspond to the magnitudes of DC power supplies. Furthermore, the proposed extended MLI topology can operate in different modes: symmetric and asymmetric. In the proposed extended MLI topology, three different operation modes are introduced, the first proposed pattern (M1) is symmetrical, and two others (M2, M3) are asymmetrical (given in Table III).

In the first mode (M1), all DC sources magnitudes in the proposed cascaded SD-MLI, are equal with each other, which are equal to a per-unit voltage ($V_{1j} = V_{2j} = V_{3j} = V_{dc}$). For example, by assuming $n = 2$ in the proposed cascaded topology, namely two of the proposed SD-MLIs are connected as a cascaded topology, the number of switching semiconductor devices is ten switches along with six DC sources. All DC sources magnitudes are the same with a value of V_{dc}. Therefore, it can generate 13 voltage levels at the output, as

shown in Table III.

TABLE III: Magnitudes of DC Power Supplies for the Proposed Cascaded Topology

Modes	DC Magnitudes	V_{omax}	N_L	TSV
M_1	$V_{1j} = V_{2j} = V_{3j} = V_{dc}$	$3nV_{dc}$	$6n+1$	$\frac{20}{6}(N_L - 1)$
M_2	$V_{1j} = V_{2j} = V_{3j} = 4^{j-1}V_{dc}$	$[4^n - 1]V_{dc}$	$2(4^n) - 1$	$\frac{20}{6}(N_L - 1)$
M_3	$V_{1j} = 6^{j-1}V_{dc}$ $V_{2j} = V_{3j} = 2(6^{j-1})V_{dc}$	$[6^n - 1]V_{dc}$	$2(6^n) - 1$	$\frac{34}{10}(N_L - 1)$

Proposing symmetrical dc sources in multilevel inverters can generate a low number of levels. Therefore, asymmetrical dc sources in MLIs are presented to create more voltage levels. Hence, two asymmetrical dc sources are presented for the proposed cascaded topology in the following. In the second proposed mode, M2, in the first SD-MLI, the DC power supplies have the same voltage as the per-unit voltage V_{dc}, and the other SD-MLIs have a magnitude 4^{j-1} where j is the number of SD-MLIs. In this mode, assuming $n = 2$ (the number of used SD-MLIs), the number of semiconductor devices and DC power supplies are the same amounts with symmetric mode. This mode can create 31 voltage levels (Table III), twice than the first mode.

In the third proposed mode (M3), the DC power supply voltages in the first SD-MLI are $V_1 = V_{dc}, V_{2j} = V_{3j} = 2V_{dc}$ and for the other SD-MLIs are $V_1 = 6^{j-1}V_{dc}, V_{2j} = V_{3j} = 2(6^{j-1}V_{dc})$ where j is the number of SD-MLIs. Noted if the magnitudes of dc sources $V_2 \neq V_3$, the height/magnitude of steps in the output voltage waveform are not the same, so the created stepped voltage waveform by the proposed topology contains a high harmonic amplitude.

In the third mode, assuming $n = 2$, the number of semiconductor devices and DC power supplies are the same as the first and second modes, but this mode generates 71 voltage levels (Table III). The main objective of the proposed modes is to keep the same number of semiconductor devices and DC power supplies to increase the number of voltage levels.

III. COMPARISON OF THE PROPOSED CASCADED SD-MLI WITH RECENT CASCADED MLIs

The aim of proposing a cascaded topology is to generate a large number of levels with minimizing the number of devices. Therefore, to demonstrate the advantages of proposed cascaded SD-MLI, a comprehensive comparison is made among the proposed MLI topology, conventional MLIs, a well known switched-diode base MLIs. The comparative study is performed in terms of the number of IGBTs, power diodes, DC power supplies, variety of DC power supplies, peak switch voltage (PSV), and the magnitude of (TSV) to validate the new capabilities of the proposed topology compare to other MLI topologies. Table IV gives the parameters of all MLI topologies concerning the number of switches, IGBTs, drivers, DC power supplies, variety, PSV, and TSV against the number of levels.

Fig. 3(a) shows that the proposed cascaded SD-MLI in symmetric and asymmetric modes (M1-M3) to create a large number of levels have a significant difference in the required number of switches than conventional MLIs and have a reasonable difference with presented switched-diode base MLIs [25]-[30]. Fig. 3(b) reports the variation of the number of IGBTs to generate different levels for the proposed cascaded SD-MLI and other MLIs. As can be seen in Fig. 3(b), the proposed cascaded SD-MLI (M1-M3) requires a fewer number of IGBT than other conventional topologies and switched-diode base MLIs. Also, the proposed SD-MLI is reduced the number of driver circuits due to reducing the number of IGBTs because each IGBT uses a gate driver.

Fig. 3(c) compares the required number of power diodes for the proposed SD-MLI topology and other MLIs. As highlighted in Fig. 3(c), the proposed cascaded SD-MLI reduces the number of diodes in comparison to other MLIs based on the suggested third method (M3), which has a low amount in comparison with other MLIs except (R14). Although the proposed topology utilizes discrete diodes instead of power switches still it requires a low number of diodes than other presented MLIs.

From Fig. 3(d), it is evident that the proposed SD-MLI topology in symmetrical dc sources (M1) to create the same voltage levels requires the same number of DC power supplies in comparison to other MLI topologies. For asymmetrical dc source, it reduces dc sources count than [9],[12] except for CHB (R4) and presented topologies in [15], [25].

One of the factors that impact the cost of cascaded multilevel inverters is the variety of dc power supplies. This factor has been introduced in [9] for the first time. After that, it has been using in other publications for comparison. $N_{variety}$ is the variety of dc power supplies or the number of different voltage magnitudes of the used dc power supplies in cascaded multilevel inverters. As can see from Table IV and Fig. 3(e), $N_{veriety}$ for all symmetrical cascaded multilevel inverters is 1.0 because all used dc power supplies have the same magnitude. Asymmetrical cascaded multilevel inverters require multiple dc power supplies with different voltage magnitudes, so these topologies have different variety of dc sources that it is directly related to their amplitudes.

The variation of $N_{variety}$ versus the number of levels for all the MLIs mentioned above is illustrated in Fig. 3(e). According to this figure, all MLIs and proposed SD-MLI (M1) have the same variety for the symmetric mode. For asymmetric dc sources, the proposed SD-MLI in the mode of (M3), CHB (R4), (R13), and (R16) has a more extensive range. The lowest dc source variety is for the proposed SD-MLI in the mode of (M2).

Fig. 3(f) shows the comparison of peak switch voltage of the proposed topology and other MLIs. As can see from this figure, the PSV's value in the most of presented MLIs like the proposed SD-MLI (M1-M3) and (R5, R6, R11, R14-R16) is high because they use an H-bridge inverter in their circuits. Low PSV in symmetrical mode is for conventional topologies (NPC, FC, and CHB) and in symmetrical mode is for (R4) and (R10).

The comparison of TSV's value in the proposed cascaded SD-MLI and all MLIs, as mentioned above, versus the number of levels are indicated in Fig. 3(g). The NPC, FC, CHB, and [9] MLIs have a low TSV's value, the proposed topology (M2),

TABLE IV: The All Required Parameters of Presented Multilevel Inverters for Comparison Study Correspond to on Their Magnitude DC Power Supplies

| Topologies	Methods	N_{switch}	N_{IGBT}	N_{diode}	N_{DC}	$N_{variety}$	PSV	TSV(p.u)
NPC	R1	$2(N_L-1)$	$2(N_L-1)$	N_L+1	$(N_L-1)/2$	1	V_{dc}	$2(N_L-1)$
FC	R2	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	N_L-2	1	V_{dc}	$2(N_L-1)$
CHB	R3	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	1	V_{dc}	$2(N_L-1)$
	R4	$4[\log_2^{(N_L+1)}-1]$	$4[\log_2^{(N_L+1)}-1]$	$4[\log_2^{(N_L+1)}-1]$	$[\log_2^{(N_L+1)}]-1$	$[\log_2^{(N_L+1)}]-1$	$[(N_L+1)/4]V_{dc}$	$2(N_L-1)$
(BUMLI)	R5	$6[(N_L-1)/5]+3$	$6[(N_L-1)/5]+3$	$6[(N_L-1)/5]+3$	$(N_L-1)/2$	1	$[(N_L-1)/2]V_{dc}$	$(7N_L-2)/2$
[12]	R6	$5[\log_2^{(N_L+5)}]-9$	$5[\log_2^{(N_L+5)}]-9$	$5[\log_2^{(N_L+5)}]-9$	$3[\log_2^{(N_L+5)}]-8$	$[\log_2^{(N_L+5)}]-2$	$[(N_L-1)/2]V_{dc}$	$(10N_L-9)/3$
(K-Type)	R7	$12[(N_L-1)/8]$	$14[(N_L-1)/8]$	$14[(N_L-1)/8]$	$(N_L-1)/2$	1	$6V_{dc}$	$32[(N_L-2)/12]+32$
[15]	R8	$12\log_{13}^{N_L}$	$14\log_{13}^{N_L}$	$14\log_{13}^{N_L}$	$4\log_{13}^{N_L}$	$2\log_{13}^{N_L}$	$[6N_L/13]V_{dc}$	$32[(N_L-2)/12]+32$
(DCHB)	R9	$3(N_L-1)/2$	$3(N_L-1)/2$	$3(N_L-1)/2$	$(N_L-1)/2$	1	$2V_{dc}$	$2(N_L-1)$
[9]	R10	$6[\log_2^{(N_L+7/3)}]-6$	$6[\log_2^{(N_L+7/3)}]-6$	$6[\log_2^{(N_L+5/3)}]-6$	$2[\log_2^{(N_L+7/3)}]-2$	$[\log_2^{(N_L+7/3)}]-1$	$[(N_L+7)/4]V_{dc}$	$6(N_L-1)$
[25]	R11	$(N_L+5/2)+3$	$(N_L+5/2)+3$	N_L+3	$N_L-1/2$	1	$[(N_L-1)/2]V_{dc}$	$3(N_L-1)$
	R12	$7\log_{15}^{N_L}$	$7\log_{15}^{N_L}$	$10\log_{15}^{N_L}$	$3\log_{15}^{N_L}$	$3\log_{15}^{N_L}$	$[7N_L/15]V_{dc}$	$3(N_L-1)$
[26]	R13	$7\log_9^{N_L}$	$7\log_9^{N_L}$	$10\log_9^{N_L}$	$3\log_9^{N_L}$	$3\log_9^{N_L}$	$[4N_L/9]V_{dc}$	$3(N_L-2)$
[27]	R14	$[3(N_L-3)+16]/4$	$[3(N_L-3)+16]/4$	N_L+1	$(N_L-1)/2$	1	$[(N_L-1)/2]V_{dc}$	$[13(N_L-3)+24]/6$
[28],[29]	R15	$(N_L+9)/2$	$(N_L+9)/2$	N_L+1	$(N_L-1)/2$	1	$[(N_L-1)/2]V_{dc}$	$(7N_L-9)/2$
[30]	R16	$(N_L+5)/2$	$(N_L+5)/2$	N_L+3	N_L-3	$(N_L-3)/2$	$[(N_L-1)/2]V_{dc}$	$3(N_L)-5$
SD-MLI	M1	$[(N_L-1)/2]+4$	$[(N_L-1)/2]+4$	N_L+4	$(N_L-1)/2$	1	$[(N_L-1)/2]V_{dc}$	$20(N_L-1)/6$
	M2	$3[\log_4^{(N_L+1/2)}]+4$	$3[\log_4^{(N_L+1/2)}]+4$	$6[\log_4^{(N_L+1/2)}]+4$	$3[\log_4^{(N_L+1/2)}]$	$[\log_4^{(N_L+1/2)}]$	$[(N_L-1)/2]V_{dc}$	$20(N_L-1)/6$
	M3	$3[\log_6^{(N_L+1/2)}]+4$	$3[\log_6^{(N_L+1/2)}]+4$	$6[\log_6^{(N_L+1/2)}]+4$	$3[\log_6^{(N_L+1/2)}]$	$2[\log_6^{(N_L+1/2)}]$	$[(N_L-1)/2]V_{dc}$	$34(N_L-1)/10$
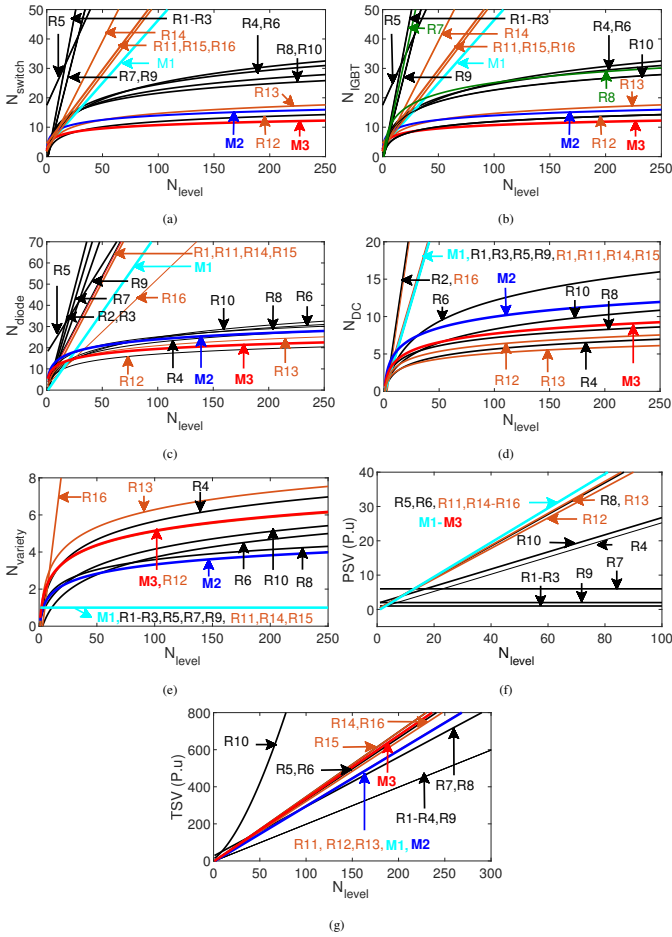
Fig. 3: Comparison studies; (a) variation of N_{level} against N_{switch}; (b) variation of N_{level} against N_{IGBT}; (c) variation of N_{level} against N_{diode}; (d) variation of N_{level} against N_{DC}; (e) variation of N_{level} against $N_{variety}$; (f) variation of N_{level} against $PSV_{P.u}$; (g) variation of N_{level} against $TSV_{P.u}$

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level SD-MLI consists of basic SD-MLI and an H-bridge with three DC sources with magnitudes of 1:2:2. Table V shows the comparison results of 11-level SD-MLI with other MLIs under the same condition. Noted some of the presented multilevel inverter topologies can generate 15 or 17 voltage levels, but in this comparison, the magnitude of DC sources is set to create 11-level. Also, some presented MLIs can not make 11-level accurately and generate 13-level.

TABLE V: Comparison of the number of required components and TSV's magnitude of proposed 11-level SD-MLI and other MLIs

Topologies	N_{level}	N_{driver}	N_{IGBT}	N_{diode}	N_{DC}	N_{cap}	PSV	TSV
2019 [22]	11	17	17	1	1	5	$5V_{dc}$	$33V_{dc}$
CHB	11	12	12	-	3	-	$3V_{dc}$	$20V_{dc}$
2019 [34]	11	12	12	-	1	4	$2V_{dc}$	$33V_{dc}$
2020 [31]	11	9	9	4	3	-	$4V_{dc}$	$18V_{dc}$
2019 [32]	11	8	8	2	4	1	$6V_{dc}$	$30V_{dc}$
SD-MLI	**11**	**7**	**7**	**3**	**3**	**-**	**$5V_{dc}$**	**$34V_{dc}$**
2014 [10]	13	12	12	-	4	0	$3V_{dc}$	$24V_{dc}$
2015 [11]	13	10	10	-	4	0	$6V_{dc}$	$20V_{dc}$
2016 [13]	13	8	10	-	4	0	$6V_{dc}$	$20V_{dc}$
2019 [15]	13	11	14	-	2	2	$6V_{dc}$	$35V_{dc}$
2016 [16]	13	10	12	-	4	-	$6V_{dc}$	$28V_{dc}$
2017 [17]	13	8	10	-	4	-	$6V_{dc}$	$27V_{dc}$
2017 [18]	13	10	10	2	2	2	$6V_{dc}$	$18V_{dc}$
2019 [19]	13	10	10	-	4	-	$6V_{dc}$	$30V_{dc}$
2019 [20]	13	10	10	-	4	-	$6V_{dc}$	$27V_{dc}$
2019 [33]	13	10	10	-	2	2	$6V_{dc}$	$20V_{dc}$

[25],[26], and [15] have an average quantity to generate a large number of levels, and other topologies have high TSV's value.

Besides, a comparison is made among the proposed SD-MLI with other MLIs to create 11-level. The proposed 11-

IV. POWER LOSSES ANALYSIS

The power losses are separated into two types: conduction and switching losses [13]-[20]. Conduction losses are determined by the on-state of switches and diodes in the current path and are defined as follows:

$$P_{L,con}(t) = P_{L,switch}(t) + P_{L,diode}(t) \tag{10}$$

$$P_{L,con}(t) = ([V_T + R_T I_p^{\beta}(t)] + [V_d + R_d I_p(t)])I_p(t) \tag{11}$$

Here V_T, V_d are the threshold voltages of power switches and diodes, R_d, R_T, are the on-state of diode resistances and the equivalent series resistance of capacitor in power switches, I_p is the peak value of output current and β is a constant. By

assuming there are $Z_1(t)$ IGBTs and $Z_2(t)$ anti-parallel and forward-biased diodes in on-state in the current path at any time, the conduction losses of the proposed topology is:

$$P_{L,con}(t) = \int_0^{2\pi} \left(Z_1(t)[P_{L,switch}(t)] + Z_2(t)[P_{L,diode}(t)] \right) I_p(t)d(\omega t) \quad (12)$$

Considering Eq. (12), the conduction losses are the sum of on-state semiconductor devices count that is turned-on to create each level. For example, the proposed 11-level SD-MLI, in the worst case (see Table I and II), requires five semiconductor devices (four switches and one diode or three switches and one diode) in the on-state. In the best case, it needs four semiconductor devices (three switches and one diode) to be in on-state. In an 11-level CHB-MLI (consists of ten H-bridge), the number of on-state semiconductor devices are twenty switches; in comparison with the proposed topology, it uses more on-state switches in current path that leads to high conduction losses.

To calculate the switching losses, first, it is calculated for a power switch and then is developed for the proposed SD-MLI. Turn-on power loss $P_{sw,on}$ for a switch, can be obtained as follows:

$$P_{sw,on,n} = \int_0^{t_{on}} v(t)i(t)dt$$
$$= \int_0^{t_{on}} \left[\frac{I(t-t_{on}) - v_{stand,n}t}{t_{on}} \right] dt = \frac{v_{stand,n}It_{on}}{6} \quad (13)$$

Similarly turn-off power losses $P_{sw,off}$ is:

$$P_{sw,off,n} = \frac{v_{stand,n}It_{off}}{6} \quad (14)$$

Here, $v_{stand,n}$, I, t_{on}, t_{off} are the standing voltage of switches, the flowing current by the switch, and on-state and off-state of switch, respectively. The sum of switching losses ($P_{L,sw,n}$) for each power switch is computed as follows:

$$P_{L,sw,n} = f_s(P_{sw,on,n} + P_{sw,off,n}) = \frac{v_{stand,n}I(t_{on} + t_{off})f_s}{6} \quad (15)$$

Here, f_s is the switching frequency of power switches. Assuming $t_{on} = t_{off}$, (15) can be written as:

$$P_{L,sw,n} = \frac{It_{on}}{3} \times f_s \times v_{stand,n} \quad (16)$$

By considering $\frac{I(t_{on})}{3} = A$ as a constant, (16) can be written as:

$$P_{L,sw,n} = A \times f_s \times v_{stand,n} \quad (17)$$

By using Eqs. (7) and (8), the switching losses for 11-level SD-MLI $P_{L,sw,SD-MLI}$ can be calculated as:

$$P_{L,sw,SD-MLI} = A \times \left(f_s(V_1 + 2V_2 + V_3) + 4f_f(V_1 + V_2 + V_3) \right) \quad (18)$$

Here, f_f is the fundamental frequency that is a low frequency. By considering $V_1 = V_{dc}, V_2 = V_3 = 2V_{dc}$ to generate 11-level at the output, (18) can be written as:

$$P_{L,sw,SD-MLI} = A \times V_{dc} \times (7f_s + 20f_f)$$
$$= 7 \times A \times V_{dc} \times (f_s + \frac{20}{7}f_f) \quad (19)$$

For the reason that $f_s \gg \frac{20}{7}f_f$, (19) can be written as:

$$P_{L,sw,SD-MLI} = 20 \times A \times V_{dc} \times f_s \quad (20)$$

Similarly by using Eq. (17) the switching losses for a 11-level CHB-MLI $P_{L,sw,CHB}$ will be:

$$P_{L,sw,CHB} = 40 \times A \times V_{dc} \times f_s \quad (21)$$

Comparing Eqs. (20) and (21), the switching losses of proposed 11-level SD-MLI is much lower than an 11-level CHB-MLI. Therefore, the total losses of the proposed cascaded SD-MLI considering Eqs. (12) and (17) obtained as follows:

$$P_{Loss} = P_{L,con}(t) + P_{L,sw,n} \quad (22)$$

V. PROPOSED TOPOLOGIES APPLICATIONS

The proposed SD-MLI and its cascaded structure are suitable for photo-voltaic (PV) systems due to requiring less number of power switches and drivers, and low stress of power switches. Fig. 4 shows the proposed 11-level SD-MLI topology is connected to a PV system. In this configuration, three input capacitors are charged with three independent PV panels. Then their low output voltages are boosted by three DC-DC converters in desired magnitudes of DC supplies. The magnitudes of DC sources, in proposed 11-level SD-MLI, will be equal $V_1 = V_{dc}, V_2 = V_3 = 2V_{dc}$. This configuration can be developed for the proposed cascaded SD-MLI by including more PV panels for other input DC source requirements.

In the proposed SD-MLI and cascaded SD-MLI topologies, such as the topologies presented in [12], [27],[28], [30],[32] the H-Bridge converter at the end is used to change the output voltage polarity and create zero levels. The limitation of the proposed topology is requiring H-bridge inverter that their switches should endure peak output voltages. Hence, the proposed topology has any superiority in this regard.
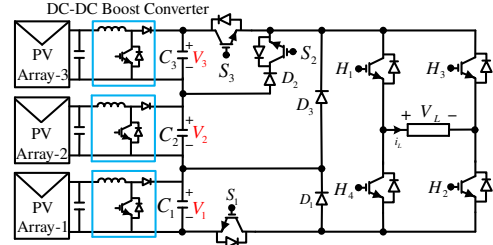

Fig. 4: Proposed 11-level SD-MLI in a PV application.

As a result, the voltage rating of the used power switches in the proposed topologies should determine to clarify the superior advantages of the proposal. Assuming the highest standard commercial voltage of IGBT be $V_{IGBT,ccv}$, so the maximum operating voltage of the proposed multilevel inverter will be equal to $\sqrt{1.5}V_{IGBT,ccv}/\gamma$ and γ is a factor to ensure the safe operation of the IGBT that is typically assumed $\gamma = 1.7$. Therefore, by determination of the maximum IGBT voltage, the operation voltage of the proposed topology is obtained. The determination of IGBTs voltage of the proposed topology is calculated for medium voltage applications for 11-level SD-MLI, and 31-level and 71-level cascaded topologies. By assuming the maximum IGBTs voltage in medium voltage applications is 3.3kV, the operation voltage of 3-phase phase-phase RMS voltage will be 2.3kV. For the single-phase system, the operation phase voltage RMS will be 1328V or maximum voltage 1878V.

TABLE VI: IGBTs and driver circuits price comparison among the proposed 11-level SD-MLI and recent 11-level and 13-level MLIs for medium-voltage applications

IGBTs and Driver Circuits Type	Voltage and Current Rating	Unit Price	[22]-11-level		[31]-11-level		[34]-11-level		[15]-13-level		**Proposed**	
			No.	Price	No.	Price	No.	Price	No.	Price	No.	Price
CM400HA-24A	1200V, 400A	$118	2	$236	6	$708	2	$236	6	$708	1	$118
CM400DU-34KA	1700V, 400A	$516	6	$3,096	-	-	10	$5,160	6	$3,096	1	$516
CM400DY-50H	2500V, 400A	$550	4	$2,200	-	-	-	-	-	-	1	$550
CM400DY-66H	3300V, 400A	$773	4	$3,092	-	-	-	-	2	$1,546	4	$3,092
CM400HB-90H	4500V, 400A	$989	-	-	4	$3,956	-	-	-	-	-	-
SKYPER-32PRO2	Up to 1700V	$92.71	6	$556.26	4	$370.84	3	$278.13	6	$556.26	1	$92.71
1SC0450V2A0-65	Up to 6500V	$267.62	4	$1,070.48	2	$535.24	-	-	1	$267.62	3	$802.86
844-SD303C25S20C	2500V, 350A	$102.50	-	-	4	$410	-	-	-	-	3	$307.50
Total Price			$10,056.32		$5,887.37		$5,952.26		$6,173.88		**$5,479.07**	

Noted, in industrial applications usually, the number of voltage levels of multilevel inverters is limited to 11 or 13-level unless the specific applications that are needed a high-quality waveform. Therefore, the component's cost comparison is conducted among the proposed 11-level SD-MLI and other 11 or 13 levels MLIs for medium-voltage applications.

Therefore, for such an RMS voltage 1328V the DC power supply magnitudes for 11-level SD-MLI will be $V_1 = 375.6V, V_2 = V_3 = 751.2V$. Thus, for the proposed topology the voltage rating of IGBTs is calculated based on Eqs. (3)-(6) and considering $V_{IGBT,cc}$ which are presented in Table VI. The cost of required IGBTs and driver circuits of single-phase proposed 11-level SD-MLI, and recent 11-level and 13-level MLIs [15], [22], [31], [34] are compared in Table VI. The commercial IGBTs voltage with the nominal current of 400A made by MITSUBISHI company. The prices of IGBTs (single pack) and gate driver circuits (Semikron, dual pack) and the power diode (single pack, Mouser Electronics) are in USD as a role example [35].

Viewing this table, by comparing the cost of proposed 11-level topology with other 11 or 13-level MLIs the cost of the proposed SD-MLI is less than the other recently presented MLIs.

The proposed cascaded topologies are consist of two series of basic SD-MLIs (Fig. 2(b)) 31-level (see Table III, M2) and 71-level (see Table III, M3). Therefore, for maximum voltage 1878V, the DC power supply magnitudes for 31-level cascaded topology are, $V_{1,1} = V_{1,2} = V_{1,3} = 125.2V$ for the first SD-MLI and are $V_{2,1} = V_{2,2} = V_{2,3} = 500.8V$ for the second SD-MLI. For 71-level proposed cascaded topology dc power supply magnitudes are: $V_{1,1} = 53.65, V_{1,2} = V_{1,3} = 107.3V$, for the first SD-MLI, and $V_{2,1} = 321.6V, V_{2,2} = V_{2,3} = 643.8V$ for the second SD-MLI. Therefore, based on commercial voltage of IGBTs the different rated voltages of IGBTs for 31-level

TABLE VII: IGBTs Voltages of 31-level and 71-level Cascaded Topologies

Switches	31 − level		71 − level	
	V_{Stand}	$V_{Nominal}$	V_{Stand}	$V_{Nominal}$
$V_{S_{1,1}}$	125.2V	250V	53.6V	250V
$V_{S_{2,1}}$	125.2V	250V	107.3V	250V
$V_{S_{3,1}}$	250.4	600V	214.6V	600V
$V_{S_{1,2}}$	500.8V	1200V	321.6V	600V
$V_{S_{2,2}}$	500.8V	1200V	643.8V	1200V
$V_{S_{3,2}}$	1001.6V	1700V	1287.6V	2500V
V_{H_1}-V_{H_4}	1878V	3300V	1878V	3300V

and 71-level SD-MLIs are illustrated in Table VII.

Both 31-level and 71-level SD-MLIs require six IGBTs for two series SD-MLIs and four IGBTs for the H-bridge converter, which is in the output. According to Table VI, the maximum standing voltage is related to four switches ($H_1 - H_4$). As mentioned before, the four power switches of H-bridge converter ($H_1 - H_4$) operate in fundamental frequency and zero state switching.
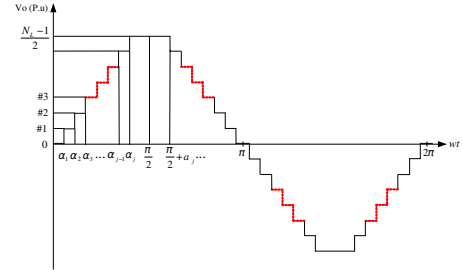

Fig. 5: Output voltage waveform of the multilevel converters based on fundamental frequency technique.

VI. SIMULATION AND EXPERIMENTAL VALIDATIONS

Simulation and experimental results are presented to validate the performance of the proposed topology, in two different case studies. In the first, the performance of 11-level SD-MLI is evaluated, and then 31-level cascaded SD-MLI (consists of two SD-MLIs) is tested. The simulation results are performed in the MATLAB environment. Two prototypes of the proposed 11-level SD-MLI and 31-level cascaded SD-MLI are built using IGBTs as the switching devices. The experimental parameters are listed Table VIII.

Basically, the conventional modulation techniques to commutate multilevel inverters are based on pulse width modulation (PWM), fundamental frequency switching technique or staircase modulation [36], [37]. In this paper, the staircase modulation technique is applied for the proposed SD-MLI and cascaded topology. The staircase strategy uses a sinusoidal stepped waveform with the fundamental frequency that illustrates in Fig. 5. In this method, by considering desired total number of levels N_L in the proposed topologies, the switching angels are calculated for $0 < \alpha_j < \pi/2$ as follows:

$$\alpha_j = sin^{-1}(\frac{j-0.5}{N_L}) \quad for j = 1, 2, \cdots, \frac{N_L - 1}{2} \quad (23)$$

Then, the switching angles generate the switching pulses of the proposed multilevel inverter which are determined separately
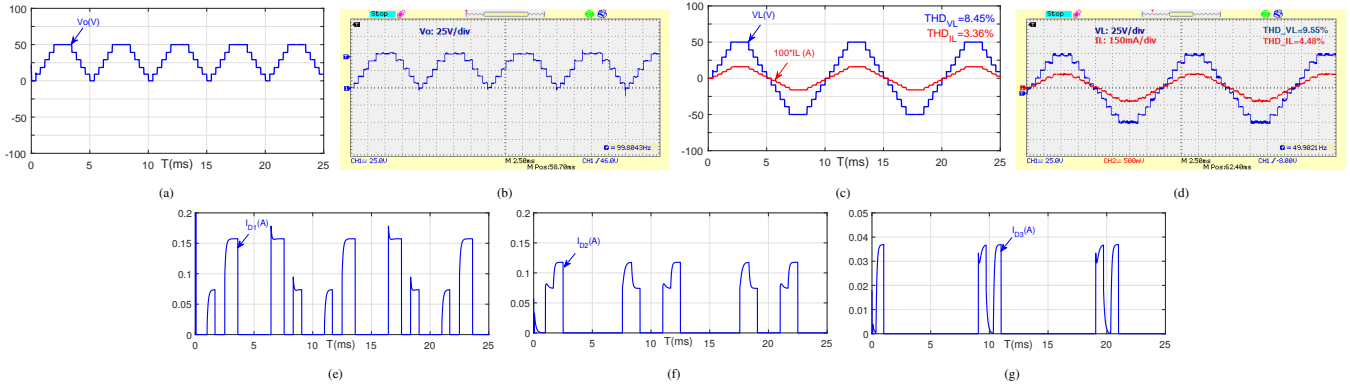
Fig. 6: Simulation and experimental results of the 11-level SD-MLI; (a) simulation results of the output voltage waveforms before H-bridge inverter; (b) experimental results of the output voltage waveforms before H-bridge inverter; (c) simulation results of the load voltage and current waveforms ($THD_{VL} = 8.45\%$, $THD_{IL} = 3.36\%$); (d) experimental results of the load voltage and current waveforms ($THD_{VL} = 9.55\%$, $THD_{IL} = 4.48\%$); (e) simulation results of current waveform of discrete diode of D_1; (f) current waveform D_2; (g) current waveform D_3.

based on the switching states Table II. The step timing is chosen based on the output frequency and it is calculated offline.

The 89C52 micro-controller by ATMEL company is applied to implement this technique. The 11-level and 31-level switching states are programmed in EPROM of the micro-controller. Then, the switching angles transfer to the micro-controller port. Finally, the switching pulses move to IGBTs of prototypes. HGTP10N40CID IGBT power switches are used to switch DC power supplies to deliver the output voltage to 250Ω, 20mH AC load.

A. Proposed 11-level SD-MLI

The proposed 11-level SD-MLI consists of one basic SD-MLI and an H-bridge inverter. Therefore, it has seven IGBTs, three power diodes and three DC power supplies. In the simulation and experimental results, the third proposed operation mode (M3) is applied. In this mode, considering $n = 1$, the values of DC power supplies are $V_1 = 10V$, $V_2 = V_3 = 20V$. Therefore, the proposed SD-MLI generates 11-level with a peak of $50V$ at the output.

The simulation and experimental results of the 11-level SD-MLI are illustrated in Fig. 6. Figs. 6(a), 6(c) and 6(e-g) indicate the simulation results and Figs. 6(b) and 6(d) show the experimental results. Fig. 6(a) and 6(b) show the generated output voltage waveform before H-bridge inverter by the

proposed 11-level SD-MLI in the simulation and experimental tests, respectively. It is observed that the SD-MLI generates only five positive voltage levels. Fig. 6(c) and 6(d) indicate the simulation and experimental tests for the load voltage and load current generated by the proposed 11-level SD-MLI for the AC load. The maximum output voltage for the experimental results is 49V with a maximum current of 198mA, which gives the voltage and current RMS value of 35.2V with 145mA, respectively. The THD's value of the load voltage and current for the simulation results of 11-level SD-MLI is 8.45% and 3.36%, and the experimental results are 9.55% and 4.48%, respectively. Furthermore, the simulation results of the current waveform for three used power diodes D_1, D_2, D_3 are shown in Figs. 6(e-g), respectively.
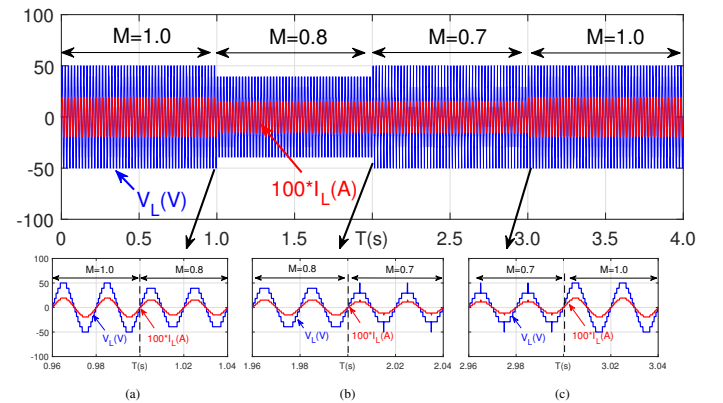

Fig. 7: The response of proposed 11-level SD-MLI to three different modulation index; (a) zoomed view for M=1.0 to M=0.8; (b) zoomed view for M=0.8 to M=0.7; (c) zoomed view for M=0.7 to M=1.0.

The efficiency (η) of the multilevel inverters are obtained based on the input power (P_{in}) and the output power (P_{out}) by measuring them $\eta = \frac{P_{out}}{P_{in}}$. The input and output powers are measured, and the efficiency of 11-level SD-MLI is given in Table IX. The input power is a DC power that is obtained by the summing of three input DC power supplies (5.25W) to produce eleven voltage levels by the proposed SD-MLI, as shown in Table IX. The applied staircase modulation technique has a low switching frequency, which leads to low power

TABLE VIII: The Experimental Parameters

Parameters	Topologies	Description
DC supplies	11-level	1 symmetric & 2 asymmetric
	31-level	3 symmetric & 3 asymmetric
DC Rating	11-level	$V_1 = 10V$; $V_2 = V_3 = 20V$
	31-level	$V_{1,1} = V_{2,1} = V_{3,1} = 20V$, $V_{1,2} = V_{2,2} = V_{3,2} = 80V$
Switches	11-level	7 x IGBT HGTP10N40CID, 400V, 10A
	31-level	10 x IGBT HGTP10N40CID, 400V, 10A
Diodes	11-level	3 x Power Diodes, 500V, 10A
	31-level	6 x Power Diodes, 500V, 10A
Micro-controller	11, 31 levels	89C52, ATMEL Company
R-L values	11, 31 levels	250Ω, 20mH

losses. Therefore, the efficiency of the proposed topology is 94.3%, which is high efficiency for multilevel inverters.

TABLE IX: Efficiency of the Proposed 11-level SD-MLI

V_{in}	P_{in}	P_{out}	R_L, L_L	$\eta\%$
$V_1 = 10V$	$P_{V1} = 1.16W$			
$V_2 = 20V$	$P_{V2} = 1.9W$	4.95W	$250\Omega, 20mH$	94.28%
$V_3 = 20V$	$P_{V3} = 2.19W$			

B. Dynamic test scenarios

The dynamic response of the proposed 11-level SD-MLI is tested in different scenarios: modulation index changes, output frequency changes, operation under nonlinear loading, and sudden load change. The simulation results of modulation index changes are depicted in Fig. 7. Fig. 7(a) shows the output voltage and current waveform for modulation indexes 1.0 to 0.8 with an R-L load at t=1s. As can see from this figure, the output voltage levels are deducted from eleven levels to nine levels. Then, the modulation index is changed from 0.8 to 0.7 at t=2s, and voltage levels are reduced to seven from nine levels, as shown in Fig. 7(b). Finally, the modulation index changing is returned from 0.7 to 1.0 t=3s, the changing output voltage and current for this case are depicted in Fig. 7(c). Simulations of the output frequency changes, operation under nonlinear loading, and sudden load change for the proposed topology are illustrated in Fig. 8. Noted the step changes are occurred at t=50ms for these testes.

The simulation results of output frequency change are presented in Figs. 8(a). The output frequency changes from 50Hz to 100Hz. The proposed topology can operate at frequency 100Hz without any variation in the shape of the output voltage and current waveform. Fig. 8(b) show the operation of the proposed topology under nonlinear loading. The linear load is an R-L load and the nonlinear load is an H-bridge diode that is switched to the output of the inverter at t=50ms. As can see from this figure, the output voltage waveform is generated without any shape changes, but the quality of the output current is declined which contains a high THD's value. Fig. 8(c) presents the simulation results of sudden load change for the proposed topology. The value of the load changes from a pure resistance load 250Ω to an R-L load 250Ω, $100mH$. It is clear that the proposed topology remains in the steady-state, and each output level keeps unchanged.

The proposed topology can not operate in low power factors like other presented MLIs [25]-[27], [30] due to using diodes in its structures. The solution is replacing switch rather than diodes. The simulation results are presented for proposed 11-level SD-MLI under different power factors, as shown in Fig. 9. As can see from this figure, the proposed topology can operate in low power factor and handle the back-flow current.

C. Proposed 31-level Cascaded SD-MLI

The performance of the proposed cascaded SD-MLI is evaluated by the simulation and experimental results for a 31-level. The proposed configuration consists of two proposed SD-MLIs and an H-bridge inverter at the output, which has ten IGBTs, six power diodes, and six DC power supplies. In the simulation and experimental evaluations, the second proposed operation mode (M2) is applied for generating 31-level. Considering the operation mode (M2) with $n = 2$, the values of DC power supplies for the first and second SD-MLIs are given in Table VII. Consequently, the cascaded SD-MLI generates 31-level with a peak of 300V at the output.

Fig. 10 shows both simulation and experimental results of the 31-level cascaded SD-MLI. They correspond to the output voltage waveforms of the first SD-MLI (V_{o1}) (Fig. 10(a) and 10(b)), the output voltage for the second SD-MLI (V_{o2}) (Fig. 10(c) and 10(d)), the total voltage of the first and second SD-MLIs (V_o) (Fig. 10(e) and 10(f)), and the load voltage and current curves (V_L), (I_L) (Fig. 10(g) and 10(h)), respectively. It can see that the experimental results have a good agreement with the simulation results for the proposed cascaded 31-level topology. The maximum output voltage for the experimental results is 298.5V, with a maximum current of 1.18A, which gives the voltage and current RMS value of 214.7V with 0.85A, respectively. The THD percentage of the load voltage and current for the simulation results of 31-level SD-MLI are 1.82% and 1.32%, and the experimental results are 2.1% and 1.46%, respectively.

Table X gives the efficiency of the proposed 31-level cascaded topology. The efficiency of the converter is 96.98%. The comparison of the efficiency in 11-level SD-MLI and 31-level cascaded SD-MLI show that the 31-level cascaded topology has high efficiency. It means that the power losses in 31-level cascaded topology are less than 11-level SD-MLI.

TABLE X: Efficiency of the Proposed 31-level Cascaded Topology

V_{in}	P_{in}	P_{out}	R_L, L_L	$\eta\%$
$V_{1,1} = 20V$	$P_{V1,1} = 1.54W$			
$V_{2,1} = 20V$	$P_{V2,1} = 1.95W$			
$V_{3,1} = 20V$	$P_{V3,1} = 2.61W$	188.17W	$250\Omega, 20mH$	96.98%
$V_{1,2} = 80V$	$P_{V1,2} = 61.76W$			
$V_{2,2} = 80V$	$P_{V2,2} = 62.92W$			
$V_{3,2} = 80V$	$P_{V3,2} = 63.24W$			

VII. DISCUSSION

The performance of the proposed topologies was validated through both simulation and experimental analysis. The proposed topologies can generate all levels based on presented theoretical concepts. The proposed cascaded topology can produce a large number of levels compared to other topologies because it requires a low number of power switches. Using lower power switches makes the proposed topology more efficient, highly reliable, and low cost.

The results findings of comparison studies indicate that the proposed topology can be applied to photovoltaic systems and replace the classical CHB inverter because the final cost has been reduced due to the reduced number of components so that the control of the proposed topology will be simpler.

The proposed topology like other presented switched-diode MLIs [25]-[27], [30] cannot operate in low power factors
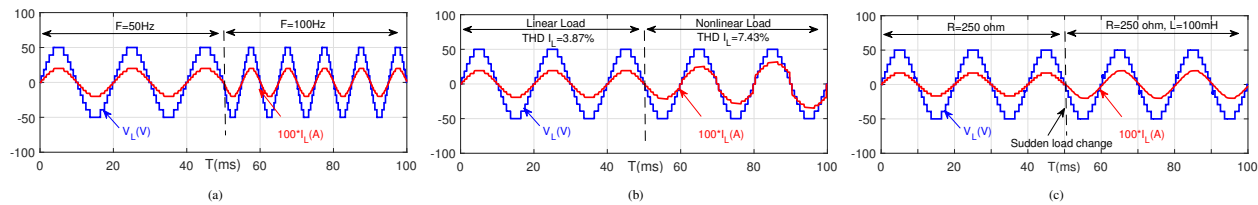
Fig. 8: The dynamic response of proposed 11-level SD-MLI; (a) output frequency change from 50Hz to 100Hz at t=50ms; (b) operation under nonlinear loading at t=50ms; (c) sudden load change from pure R load to an R-L load at t=50ms.
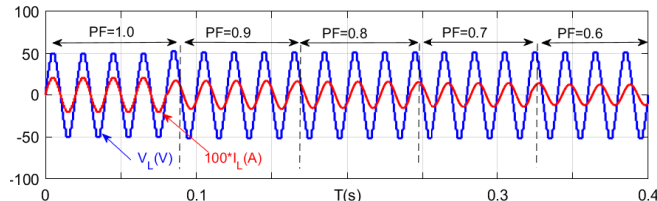

Fig. 9: Operation 11-level SD-MLI under different power factors with replacing switch rather than diode.

due to using the discrete diodes in its power circuits. The back-flow current capability is usually created when multilevel inverters are connected to the grid. The grid-based multilevel inverter systems have a high power factor and need to back-flow current is rare. Replacing the switch rather than the diode is an alternative solution. Therefore, the proposed topology can run and handle the back-flow current to work in a low power factor.

VIII. CONCLUSION

In this paper, a reduced switched-diode base multilevel inverter was proposed fro cascaded configurations. The presented fundamental SD-MLI comprises three power switches, three DC sources, and three power diodes, which generate five positive voltage levels. The proposed topology was developed for cascaded MLIs to create a large number of levels while reducing the number of devices. Based on the presented comparison results of the proposal with other MLIs, the proposed SD-MLI requires fewer components to generate a high number of levels. Besides, this paper has demonstrated that the proposed topology is reduced total standing voltage value than some presented MLIs in literature, too. The proposed topology has some limitations, in particular, it still requires a wider DC voltage source variety for the proposed asymmetric operation mode (M3) in comparison to other MLIs. However, the number of devices deducted, and the solution is using DC/DC converters for the regulation of DC-links.

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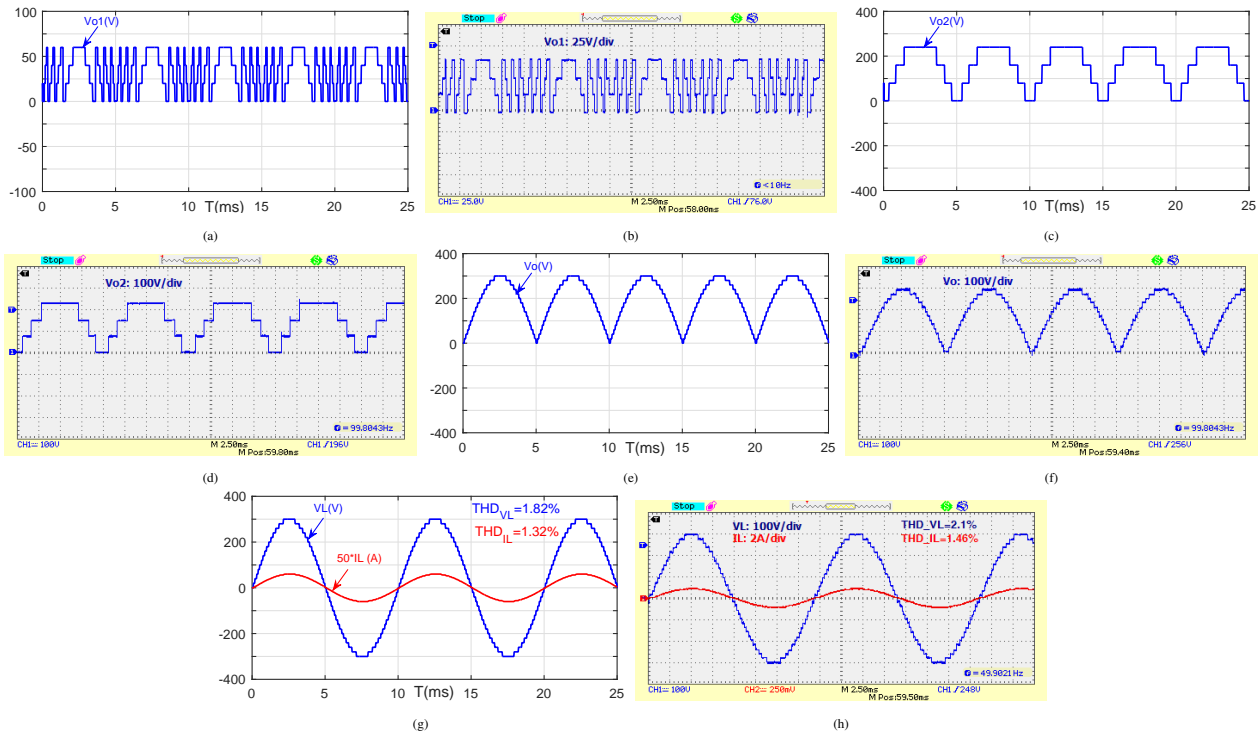
Fig. 10: Simulation and experimental results of the 31-level cascaded SD-MLI; (a) simulation results of the output voltage for the first SD-MLI; (b) experimental results of the output voltage for the first SD-MLI; (c) simulation results of the output voltage for the second SD-MLI; (d) experimental results of the output voltage for the second SD-MLI; (e) simulation results of the output voltage before the H-bridge inverter; (f) experimental results of the output voltage before the H-bridge inverter; (g) simulation results of the load voltage and current waveform ($THD_{VL} = 1.82\%$, $THD_{IL} = 1.32\%$); (h) experimental results of the load voltage and current waveform ($THD_{VL} = 2.1\%$, $THD_{IL} = 1.46\%$)

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