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Understanding of self-terminating pulse generation using silicon controlled rectifier and RC load

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Recently a silicon controlled rectifier (SCR)-based circuit that generates self-terminating voltage pulses was employed for the detection of light and ionizing radiation in pulse mode. The circuit consisted of a SCR connected in series with a RC load and DC bias. In this paper, we report the investigation of the physics underlying the pulsing mechanism of the SCR-based. It was found that during the switching of SCR, the voltage across the capacitor increased beyond that of the DC bias, thus generating a reverse current in the circuit, which helped to turn the SCR off. The pulsing was found to be sustainable only for a specific range of RC values depending on the SCR's intrinsic turn-on/off times. The findings of this work will help to design optimum SCR based circuits for pulse mode detection of light and ionizing radiation without external amplification circuitry. © 2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [<http://dx.doi.org/10.1063/1.4940305>]

I. INTRODUCTION

The silicon controlled rectifier (SCR) is a three terminal p-n-p-n semiconductor device that belongs to the thyristor family. The device is able to switch from a high impedance state (forward blocking mode) to a low impedance state (conduction mode), depending on the external bias across the anode and cathode and/or on the current applied to the gate. As such, the switching ability of these devices have traditionally been leveraged upon in the fields of electrical power and industrial electronics, particularly for power regulation and control, and the provision of excess and low voltage protection and short circuit current protection.¹ More recently, the possible use of the SCR in novel applications has been explored.^{2,3} It has been demonstrated that a SCR, connected in series with a parallel RC circuit under DC bias, was able to generate spontaneous self-terminating voltage pulses, with the pulse rate increasing as the DC bias was increased, and saturating as the pulse period approached the RC time constant of the circuit.² In addition, when a photodiode was connected to the gate terminal of the SCR, the pulse rate was observed to increase with light intensity.² Such a circuit is, essentially, a pulse mode light detector and can potentially be incorporated in applications that require the generation of voltage or current pulses in response to DC stimulations, for example, in pulse mode optical sensing² and in ionizing radiation detection.³ The use of SCR-based pulse generating circuits for pulse mode sensing operations is still in the nascent stages. In this paper, we report on the details of how the pulses are generated including the reverse currents observed during pulsing and the importance of the load resistance and capacitance on sustaining the pulses.

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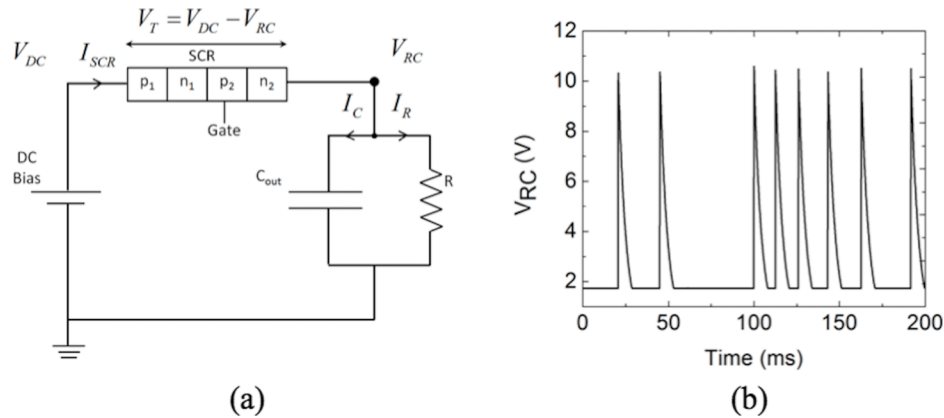


FIG. 1. Schematic diagram of pulse generating circuit with labeling of voltages and currents. (b) Measured pulses generated by the circuit in (a) using MBS 4993 as SCR, $R = 47 \text{ k}\Omega$, $C_{OUT} = 100 \text{ nF}$, and at a DC bias of 10.8 V.

II. SCR-BASED PULSE GENERATING CIRCUIT

The pulse generating circuit consists of a SCR connected in series with a RC load and a DC power supply² as schematically shown in Fig. 1(a). As the DC voltage is increased, the SCR switches and generates self-terminating pulses as depicted in Fig. 1(b).

The dynamics of the pulse can be described as follows: With voltage across the load resistor (R) starting at the threshold voltage (V_T), which is basically the SCR switch current times the Load resistance (R), when switching occurs the voltage across R jumps to near the holding voltage (V_H , see Fig. 2) and decay back to the threshold voltage. The rise time is determined by the switching time of the SCR, specifically the turn-on time, which the mechanism is described in reference,¹ and the fall time is determined by the RC time constant. Since the SCR turn-on time is much shorter than the RC time constant, the pulse shape can be approximated by the multiplication of a Heaviside function (H) by an exponential decay:

$$V_{pulse} = V_T + (V_H + V_T) H(t - t_0) \exp\left(\frac{-(t - t_0)}{RC}\right), \tag{1}$$

where t_0 is the moment when the pulse starts.

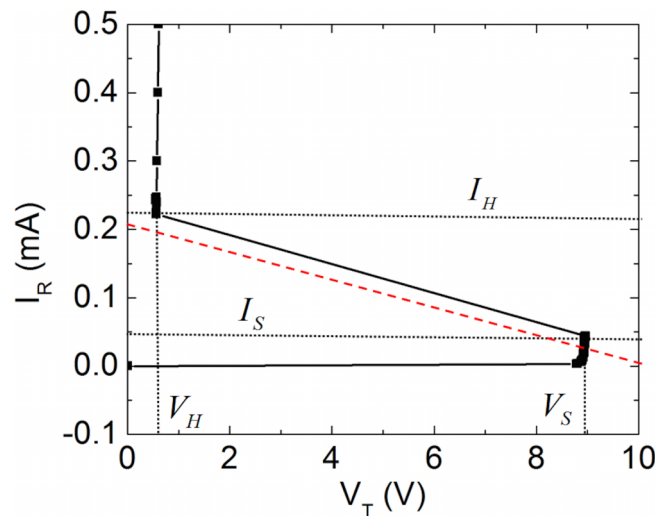


FIG. 2. Measured I-V characteristic of MBS 4993. The I_S and V_S are 0.044 mA and 8.96 V, respectively, while I_H and V_H are 0.223 mA and 0.562 V, respectively.

The pulse rate was found to depend on the DC bias as opposed to the expected periodic pulses with RC time constant. Pulsing starts when the applied bias voltage places the SCR near to the switching point. The interpulse interval can then be decreased as the bias voltage increases. Saturation is achieved when pulse repetition becomes periodic with the period equals to the pulse duration (SCR turn-on time + RC time constant). This process is well described in Ref. 2. The measured static I-V characteristic of the SCR is shown in Fig. 2. The SCR's switching voltage (V_S) and current (I_S) were measured to be 8.96 V and 0.44 mA, respectively, while its holding voltage (V_H) and current (I_H) were 0.56 V and 0.22 mA, respectively. It was initially proposed that for pulsing to occur, the load line has to intersect the SCR's IV characteristic at only one point between the device's holding current and switching current, or within the unstable transition region of the device between its "on" and "off" states, as shown in Fig. 2.⁶ The equation for the DC loadline of the circuit in Fig. 1(a) can be written as:

$$V_{DC} = V_T + I_R R, \quad (2)$$

where V_{DC} is the DC bias, V_T is the voltage across the SCR, I_R is the current in the resistive branch of the circuit and R is the load resistor (see Fig. 1(a)). The slope of the load line is altered by varying the size of the load resistor.

The intersection of the load line anywhere other than the negative resistance region of the I-V characteristic causes the SCR to remain either in the "on" or "off" state without generating pulses. This constraint on the placement of the load line means that the size of the resistive load must be small enough to maintain the steady current above I_S for turning the device on and yet large enough to keep the current below I_H for switching the device off. These requirements can be summarized as

$$\frac{V_{DC} - V_S}{I_S} \geq R \geq \frac{V_{DC} - V_H}{I_H}. \quad (3)$$

However, the requirement in Eqn. (3) does not take into consideration the effect of the capacitor on pulsing, which plays an important role in sustaining the pulses. In order to examine the contribution of the capacitor during the switching-on/off phases of the circuit, a DC bias of approximately 11 V and resistive load of 47 k Ω was chosen based on Eqn. (3) to assure pulsing. The transient voltages and currents at the key nodes of the circuit (current through the SCR, I_{SCR} , output voltage, V_{RC} , currents through the resistor, I_R , and the output capacitor, I_C) were measured as the output capacitor, C_{OUT} , was varied from 1 nF to 1024 nF. The relatively large transient current generated during the switching was measured using a Pearson current monitor which can measure a maximum current of 100 A at a resolution of 2 ns. In addition to varying the capacitance, measurements were also performed by varying the load resistor, R from 800 Ω to 50 k Ω while keeping C_{OUT} at 100 nF.

III. MEASUREMENTS

Figure 3 shows the measured current through the capacitor, I_C , as C_{OUT} was increased from 3 nF to 807 nF, where pulsing was observed. The pulse height (V_P) remained the same for all the capacitors with the magnitude close to $V_S - V_H$. Outside of this range, the SCR switched and remained "on", without generating pulses. The transient current through the capacitor during the switching of the SCR ranged from sub amps to several amps depending on the size of C_{OUT} . The duration of the positive current surge lasted only a few microseconds and increased with the value of the output capacitance as shown in Fig. 3. This is expected since a larger C_{OUT} will undoubtedly draw more charges across the SCR to attain the same pulse height, V_P , whereas the period of positive current surge is governed by the $R_{SCR}C_{OUT}$ time constant, where R_{SCR} is the on-resistance of the SCR (typically a few ohms⁴).

During the period of the positive current surge, nearly all the current passing through the SCR contributes to the charging of C_{OUT} due to its low impedance compared to the load resistor.² This is evidenced by the good agreement obtained between the integration of the measured positive I_C (0.98 μC when $C_{OUT} = 100$ nF) and the estimation of the amount of charge stored on the capacitor ($C_{OUT}V_P = 0.96$ μC , with measured V_P of 9.6 V). In order to understand why pulses were not observed for both, small and large values of the output capacitor, the voltage across the SCR, V_T , was obtained from the measured V_{DC} and V_{RC} and plotted in Fig. 4. The data in Fig. 4 shows that within the

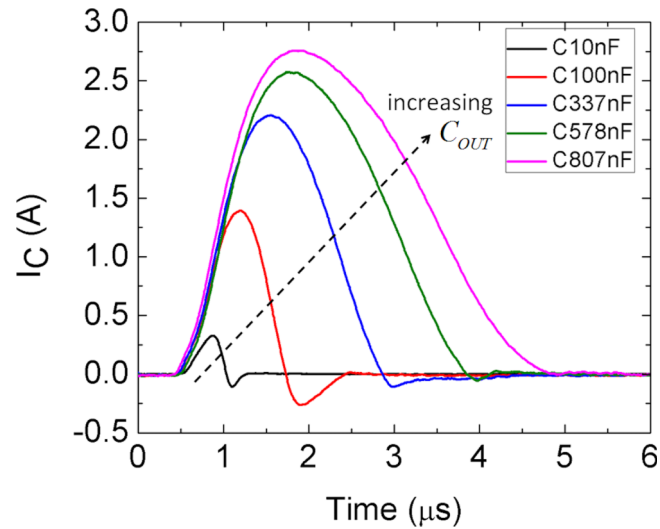


FIG. 3. Measured I_C with time during switching for a set of C_{OUT} . The origin of reverse current is due to charging of capacitor above the applied DC bias. Magnitude of reverse current decreases as C_{OUT} approaches the limits of pulsing.

switching cycle, the voltage across the SCR stays below the holding voltage, V_H , which is necessary for the SCR to switch to its off state. Negative I_C and $V_T < V_H$ was not observed for $C_{OUT} \leq 1\text{nF}$ and $C_{OUT} \geq 1024\text{nF}$, for which no pulsing was observed.

The existence of a negative I_C region when pulsing occurs, and the lack thereof when pulsing cannot be achieved, suggests that the reverse current through the SCR is the trigger for switching the device from its “on” state to the “off” state. The process of switching the SCR via a reverse current is referred as the reverse recovery.⁷ It is known that when the SCR is in its low-impedance, high-current “on” state, all of the device’s junctions (p_1-n_1 , n_1-p_2 and p_2-n_2) are forward biased and a large concentration of free carriers exists in the middle p-n junction. To return the SCR to its “off” state, the middle $n-p$ junction has to return to its reverse-biased state, and the free carriers need to be removed to enable the formation of a depletion region that can support a high electric field.⁷ This is accomplished via the reverse current, which occurs when $V_T < V_H$, and persists till sufficient free carriers are removed.

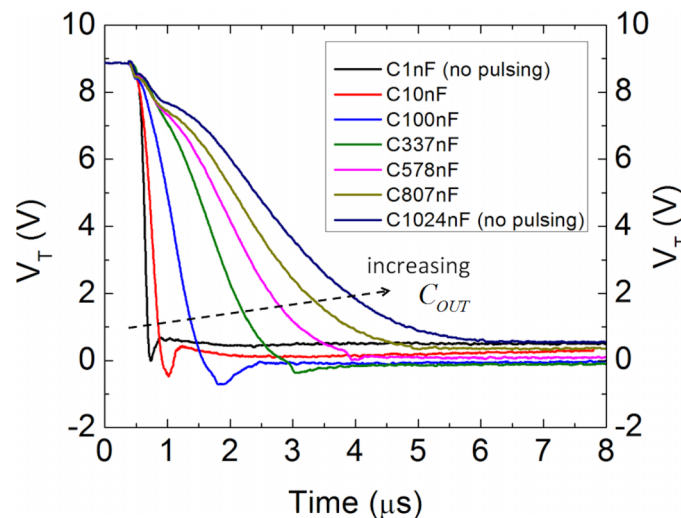


FIG. 4. Dependence of V_T with time during the switching of the SCR for a set of C_{OUT} values. The load resistor was kept constant at $47\text{K}\Omega$.

IV. EFFECT OF CAPACITANCE ON PULSING

Pulsing was observed for all values of C_{OUT} between 1 nF and 1024 nF when the load resistor was kept constant at 47 k Ω . At $C_{OUT} \leq 1$ nF and ≥ 1024 nF, the SCR switched to its “on” state and was unable to revert to its “off” state. For all values of C_{OUT} , V_T first decreases rapidly from the switching voltage (8.9 V) to a minimum when switching occurs and then increases fairly rapidly before flattening out (see Fig. 4) and finally returning to its pre-pulsed value of 8.9 V. Significantly, for C_{OUT} of 1 nF and 1024 nF where pulsing was not observed, the V_T rose above the SCR’s holding voltage, V_H , before the specified time needed for it to turn-off (t_{OFF}) of 30 μs ⁸ as shown in Fig. 5. The SCR’s ability to switch from its “on” state to its “off” state is dependent on V_T staying below V_H , and I_{SCR} decreasing below I_H during the t_{OFF} . The lack of pulsing observed when C_{OUT} is ≤ 1 nF and ≥ 1024 nF is due to the inability of meeting these criteria.

The inability of generating pulsing outside of the lower and upper limits of C_{OUT} can be qualitatively explained by the RC time constants involved in the charging and discharging of C_{OUT} . When the SCR is switched to its “on” state, C_{OUT} is being charged via its on-resistance (R_{SCR}). The SCR commences switching back to its “off” state after C_{OUT} is fully charged and V_T across the device is at its minimum. At this time, C_{OUT} begins to discharge rapidly through the R_{SCR} and then at a slower phase through the load resistor which is governed by the RC_{OUT} time constant as seen in Fig. 5. For a C_{OUT} of 1024 nF or larger, pulsing does not occur since the time it takes for C_{OUT} to fully charge is substantially longer than the turn-on time (t_{ON}) of the SCR of 1 μs ⁸ (i.e., $R_{SCR}C_{OUT} > t_{ON}$). Thus, as seen in Fig. 5, V_T remains above V_H within the entire turn-off time forcing it to remain perpetually in the “on” state. In order to estimate the upper limit of C_{OUT} , the value of the on-resistance of the SCR, R_{SCR} , is needed. This was determined using the data in Fig. 4.

Assuming the rapid decrease of V_T is due to the charging of C_{OUT} , the data shown in Fig. 4 was plotted in the natural log scale and shown in Fig. 6. The plots of $\ln(V_T)$ with time, for a set of C_{OUT} values, show nearly linear dependence after the initial period of the switching process which indicates that the charging of C_{OUT} via the on-resistance of the SCR. The on-resistance of the SCR was estimated using the slopes in Fig. 6 and found to vary from about 36.7 Ω to 1.4 Ω as C_{OUT} is varied from 1 nF to 1024 nF. Using $t_{ON} = 1$ μs , the upper limit of C_{OUT} to ensure the generation of pulses is estimated to be about 700 nF which is in good agreement with the observed value of about 800 nF.

At the lower limit, C_{OUT} is fully charged within the turn-on time (see Fig. 4) but begin to discharge via the load resistor at a much shorter time than the t_{OFF} . Thus, the voltage across the SCR, V_T remains

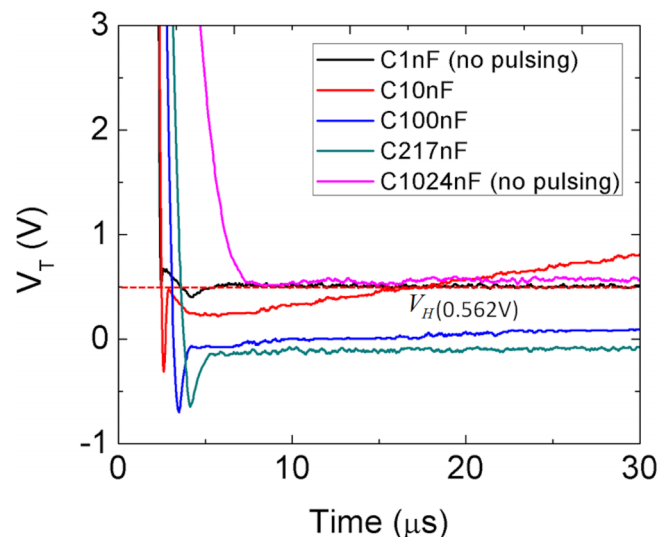


FIG. 5. Dependence of V_T with time for a selected set of C_{OUT} . For output capacitors of ≤ 1 nF and ≥ 1024 nF, V_T does not stay below V_H during the SCR’s turn-off time of 30 μs , which prevents it to switch off to generate pulses. The load resistor was kept constant at 47 k Ω .

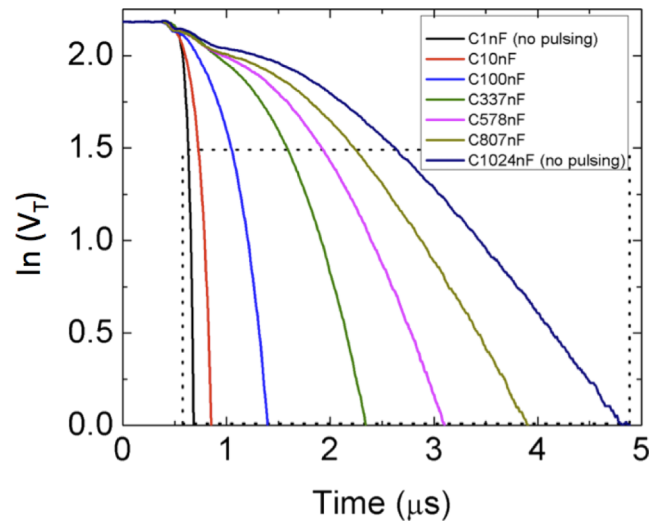


FIG. 6. Variation of $\ln(V_T)$ with time for a set of output capacitor values. Linear dependence observed for values of $\ln(V_T)$ between 0 and 1.5 as indicated by the dotted rectangle.

above V_H during the turn-off time as seen in Fig. 5 when $C_{OUT} = 1$ nF where no pulsing was observed. Based on the $30 \mu\text{s}^8 t_{OFF}$ and a load resistance of $47 \text{ k}\Omega$, the minimum value of C_{OUT} required for pulsing is estimated using $RC_{OUT} > t_{OFF}$ to be about 0.6 nF , which is in close agreement with the experimental value observed for pulsing of $C_{OUT} > 1 \text{ nF}$. It should be noted that the estimation of the range of capacitor values is approximate based on the stated values of the SCR's turn on and off times in Ref. 8.

V. EFFECT OF RESISTANCE ON PULSING

The effect of the load resistance on pulsing was also investigated by varying the resistor values from 800Ω to $50 \text{ k}\Omega$, with C_{OUT} maintained at 100 nF . The variation of load resistor found to have no noticeable impact on the transient current through the SCR when it switches due to the fixed C_{OUT} . On the other hand, the rate of increase of V_T , when the SCR was reverting to its "off" state, was observed to increase for small resistive loads, as shown in Fig. 7 for $R = 800 \Omega$. For sufficiently small resistive

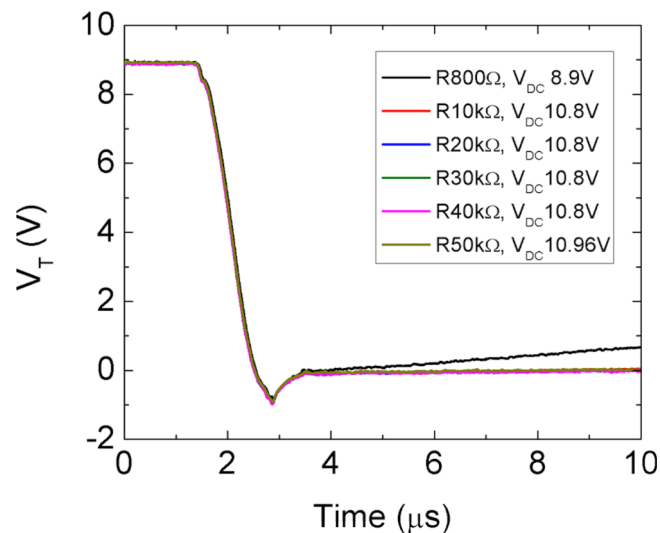


FIG. 7. Measured V_T during the switching of SCR for a set of load resistors (R) while keeping C_{OUT} at 100 nF .

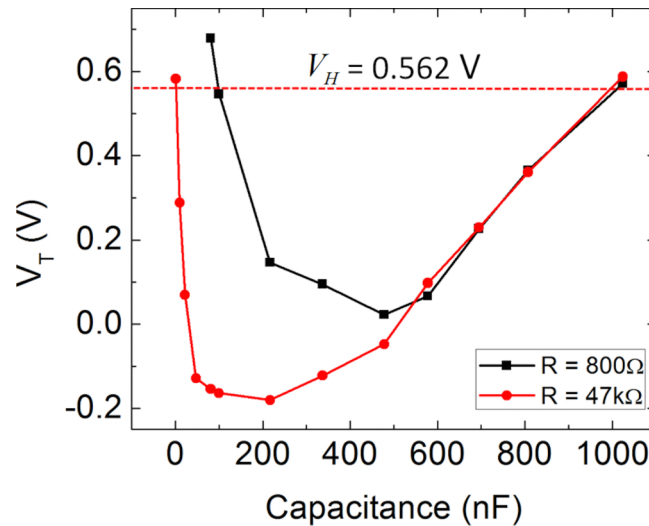


FIG. 8. The minimum values of V_T with C_{OUT} for two different load resistors. The pulsing was observed only when the minimum of V_T below the holding voltage of SCR (V_H). For smaller load resistors, higher capacitors are needed to sustain pulsing.

loads, due to small RC time constant, V_T increases beyond the holding voltage of the SCR within the turn-off time preventing the pulses to occur. Specifically, the pulsing was achieved for C_{OUT} values between 81 nF and 1024 nF when a 800 Ω load resistor was used, whereas a 47 k Ω load resistor enabled us to extend the pulsing for C_{OUT} values slightly above 1 nF.

Figure 8 shows the dependence of minimum voltage observed across the SCR during the switching with C_{OUT} for two different load resistor values. The dashed line in Fig. 8 indicates the holding voltage and pulsing was not observed when the minimum value of V_T lied above that. Notably, the upper limit of the output capacitance required to sustain pulsing was not affected by the value of the load resistor used since it depends only on the “on” resistance of the SCR. These observations are in line with the earlier discussion which indicated that the ability of the SCR to switch off was premised on $RC_{OUT} > t_{OFF}$ being satisfied.

Interestingly, pulsing was achieved for resistor values as low as 800 Ω although these values do not satisfy the static load-line criteria set forth in Eqn. (2). The overlay of the static loadlines with the SCR’s I-V characteristic shown in Fig. 9 indicates that no pulsing should occur for resistor values lower than about 45 k Ω since they each possess two stable operating points (one below I_S and the other above I_H). In this case, the SCR would simply switch from its “off” state to its “on” state and remains there. This disparity with the experimental results is because the static loadline analysis described earlier is applicable for a circuit with no reactive load. With the RC load in our case, the current generated during the switching primarily passes through the output capacitor due to its low impedance at the fast switching speeds. The fact that pulsing occurs for small resistor values can be attributed to the role that the output capacitor plays during the switching process. Notably, it was observed that for all the load resistors for which pulsing occurred, the minimum voltage across the SCR occurred within its specified turn-on time of about 1 μ s (see Fig. 7). This suggests the possibility that C_{OUT} was able to charge up and establish a voltage across the SCR below the holding voltage, before the device could fully turn “on” and reach its stable operating point above I_H , therefore returning the device to its “off” state. This process repeats, allowing the self-generation of pulses.

VI. EFFECT OF GATE CURRENT ON PULSING

The effect of triggering the SCR externally for pulse generation was also investigated since the application of the circuit for sensing involves external triggering via injection of charges to the middle p-n junction. A continuous 5 μ A gate current was injected into the SCR by connecting a photodiode

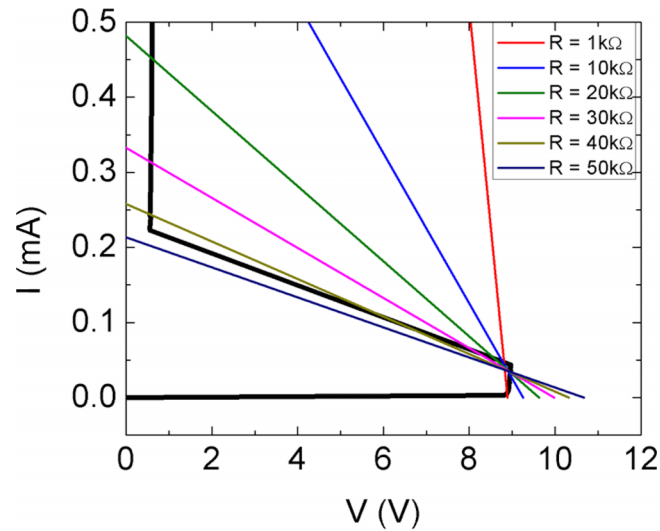


FIG. 9. Loadlines corresponding to a set of load resistors. Pulsing was achieved for resistor values whose loadlines do not satisfy the static loadline criteria for pulsing as described in section II. The DC bias (or intersection point on the horizontal axis) for each resistor was set at the threshold of pulsing to stay close to the static regime.

to the gate of the device in the reverse-biased configuration, and irradiating light onto it. V_T and I_{SCR} were measured with $C_{OUT} = 3$ nF and $R = 47$ k Ω by generating pulses with and without light. Figure 10 shows the measured I_{SCR} with bias triggered pulsing at $V_{DC} = 10.8$ V and light triggered pulsing at $V_{DC} = 10.5$ V. The injection of a gate current enabled pulsing to be sustained at a slightly lower DC bias and the transient I_{SCR} responses were comparable in profile with slight differences in their magnitudes (see Fig. 10). This suggests that the switching mechanism of the SCR is not sensitive to the means by which it is triggered, be it via DC bias or using a gate current. The higher I_{SCR} with gate current triggering is possibly due to an increase of avalanche generation with additional holes injected into the p_2 layer via the gate terminal.

In addition, it has previously been shown that the interpulse duration is intrinsic to the SCR and depend on the DC bias and/or the magnitude of the gate current (I_{GATE}).² It was found that the pulse

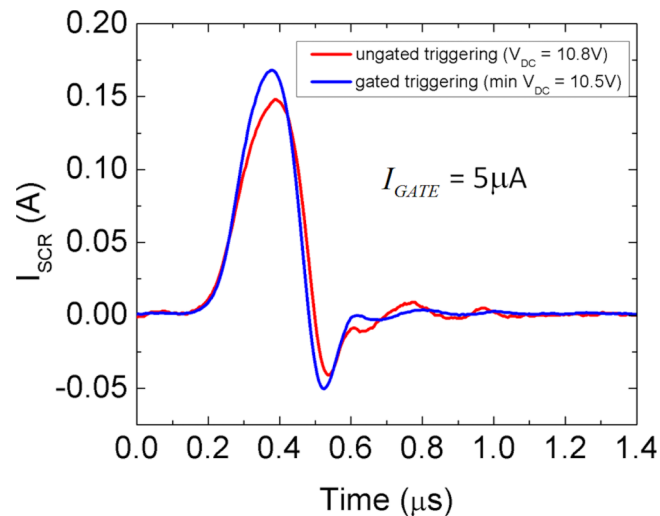


FIG. 10. Comparison of transient of I_{SCR} for triggering with DC bias and triggering with injection of current via the gate. Slightly higher transient current was observed when triggered with gate current most likely due to stronger carrier multiplication within the middle junction of SCR.

rate increased and saturated at the RC_{OUT} time constant as either V_{DC} or I_{GATE} was increased. These observations suggest the possibility of them being used as a means of gain control. Specifically, when high intensity light or ionizing radiation is incident on the circuit, V_{DC} can be adjusted downwards to avoid saturation. The attributes of such a circuit can potentially be extended to applications that require the generation of voltage or current pulses in response to DC stimulations, for example, in pulse mode optical sensing,⁹ in neural stimulators for retinal implants,¹⁰ and in ionizing radiation detection.³

VII. DYNAMIC I-V CHARACTERISTICS

As previously mentioned, a static loadline analysis of the circuit is not applicable when it contains reactive components. Instead, the transient I-V characteristic of the SCR during pulsing is needed to describe the dynamics of the circuit. This was measured using the transient I_{SCR} and V_T data for a set of C_{OUT} , and plotting I_{SCR} vs V_T as shown in Fig. 11.

At a first glance, the dynamic I-V characteristic of the SCR differs significantly from its static I-V profile in Fig. 2. The amplitudes of the currents involved during pulsing ($-0.26 - 1.39$ A) are approximately three orders of magnitude larger than that in the static case ($0 - 0.25$ mA). In addition, the large differences in the I-V characteristic when C_{OUT} is varied clearly emphasize the significant role C_{OUT} plays in the generation of pulses. The impedance of the SCR is obviously not a constant as evidenced by the non-linear behavior of I_{SCR} with V_T .

The dynamic I-V characteristic of the SCR is examined in closer detail using the data for $C_{OUT} = 100$ nF (blue solid line in Fig. 11). When pulsing first initiates at point A, V_T across the SCR start dropping from V_S along the upper branch as the device switches to its “on” state. The C_{OUT} is charged during this period, and from point B to point C, V_T decreases with I_{SCR} as the charging of the output capacitor nears completion. At point C, the charge on C_{OUT} is at its maximum while V_T across the SCR is close to zero. Between points C and D, polarity of current reverses and sends the SCR to its “off” state. The switching of the SCR to its “off” state is depicted by the lower branch of the I-V characteristic from points D to A. When V_T across the device increases beyond V_S , the switching process is repeated and a new pulse occurs. The dynamic I-V characteristic arises from switching of the SCR from high to low voltage within sub microsecond time period. The switching process involves regenerative injection of charges from the outer two forward biased p-n junctions of SCR and subsequently avalanche multiplication of them within the reverse biased middle p-n junction.⁵ The generation and transport of a large amount of charges across SCR within a short period of time is

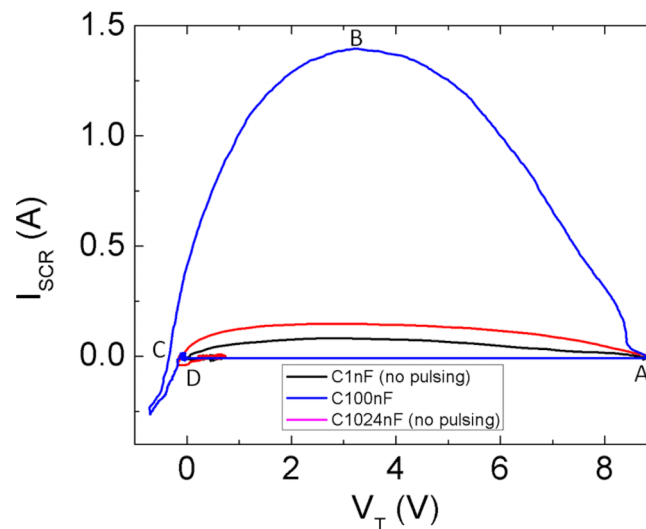


FIG. 11. Dynamic I-V characteristic of the SCR (MBS 4993) for three different C_{OUT} with load resistance of 47 k Ω . Only the 100 nF capacitor produced pulses due to the generation of negative current and voltage during the switching.

responsible for the observed large current during the switching. The steady state current after switching is due to three forward biased p-n junctions where there is no regenerative action to amplify the current in the SCR due to low voltage across it.

VIII. CONCLUSION

The dynamical switching characteristics of a pulse generator circuit that uses a SCR subjected to DC bias and a RC load was investigated experimentally. It was found that pulsing can only occur for a range of output capacitor values for a given load resistor, with the highest pulse rate determined by the reverse recovery time of the SCR. For pulsing, the lower limit of the capacitor is found to depend on the load resistor while the upper limit is associated with the on resistance of the SCR. It was found that the SCR switches from its “on” state” to its “off” state via a reverse recovery current (negative I_{SCR}) that is accompanied by a voltage drop across the device. This reverse recovery current is needed to remove the free carriers in the drift region and return the central $p-n$ junction to its reverse-biased “off” state. Based on the measurements, a dynamic I-V characteristic of the SCR was determined and used for explaining the pulse generating mechanism. This work will help to optimize the SCR based pulse generating circuit for sensor applications.

ACKNOWLEDGMENTS

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- ¹ P. Atkinson, *Thyristors and their Applications*, 1st ed. (Mills and Boon Limited, London, United Kingdom, 1972), pp. 9–11.
- ² G. Karunasiri, *Appl. Phys. Lett.* **89**, 23501-1 (2006) Available: <http://scitation.aip.org/content/aip/journal/apl/89/2/10.1063/1.2220528>.
- ³ F. Alves, C. Smith, and G. Karunasiri, *Sensors and Actuators A: Physical* **216**, 102 (2014) Available: <http://www.sciencedirect.com/science/article/pii/S0924424714002581>.
- ⁴ R. L. Boylestad and L. Nashelsky, *Electronic Devices and Circuit Theory*, 7th ed. (Prentice Hall, Upper Saddle River, New Jersey, 1998), pp. 842–857.
- ⁵ S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (John Wiley and Sons, Hoboken, New Jersey, 2007), pp. 548-574.
- ⁶ B. L. Anderson and R.L. Anderson, *Fundamentals of Semiconductor Devices*, 1st ed. (McGraw-Hill, New York, 2005) pp. 650-657.
- ⁷ B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. (Springer Science, New York, 2008) pp. 625-697.
- ⁸ Semiconductor Technical Data for MBS 4991/4992/4993, Motorola, Phoenix, AZ, 1995, pp. 1-5.
- ⁹ G. de Graaf and R. F. Wolffenbuttel, *Sensors and Actuators A: Physical* **110**, 77 (2004) Available: <http://www.sciencedirect.com/science/article/pii/S0924424703005843>.
- ¹⁰ M. Mahadevappa, J. D. Weiland, D. Yanai, I. Fine, R. J. Greenberg, and M. S. Humayun, *IEEE Trans. Neural Sys. & Rehab. Engr.* **13**, 201 (2005) Available: http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=1439546&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxppls%2Fabs_all.jsp%3Farnumber%3D1439546.