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SEE Analysis of Digital InP-Based HBT Circuits at Gigahertz Frequencies

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***Abstract*—A device/circuit simulation is used to analyze a gigahertz clocked emitter-coupled logic circuit being perturbed by a single event. Results provide an understanding of charge collection in the heterojunction bipolar transistor. A technique for single-event hardening is demonstrated by simulation.**

***Index Terms*—Heterojunction bipolar transistors, indium phosphide integrated circuits, radiation effects, single-event effects (SEEs).**

I. Introduction

THIS paper utilizes heterojunction bipolar transistor (HBT) device simulations coupled with a SPICE-modeled emitter-coupled logic (ECL) circuit to investigate how charge, photocurrents, and voltage potentials react to single-event induced carriers. The single-event effect (SEE) simulations model an HBT ECL inverter circuit operating at a 10-GHz clock rate. Previous work has presented experimental measurements utilizing photoconductive probes showing picosecond resolution of internal waveforms in normal operation and waveforms induced by 100-fs laser pulses [1], [2]. This work is compared to these previous measurements. The simulations in this paper used a technology computer-aided design (TCAD) software package (Silvaco's ATLAS, MIXEDMODE, SmartSpice) to analyze charge transport internal to the HBT while the contact boundary conditions are tied to dynamically changing circuit potentials.

Integrated circuits utilizing InGaAs–InP material system have become the dominant technology for the standard OC-768 (40 Gbit/s) communication links. Several firms have transitioned from GaAs-based devices to InGaAs–InP technologies to obtain higher performance and to utilize the InGaAs material for detectors in 1.55-μm optical links. Due to the increase in commercial applications for digital InGaAs–InP devices, applications operating in space or in alpha environments may experience SEE reliability issues.

The InP-based technology has shown excellent total dose characteristics [3]; however, SEE sensitivity has been an issue not fully investigated or understood. Radiation effects on InGaAs–InP-based ICs have only been reported using optical laser techniques to study voltage transients. There has not been any reported SEE heavy ion or proton experimental results in the open literature on InGaAs-based ICs. Silicon bipolar ECL circuits were studied for SEE by Shoga *et al.* [4] and shown to be insensitive to clock frequency. Dayaratna *et al.*presented data on silicon ECL circuits showing low threshold LETs [5]. Marshall *et al.*performed SEE experiments on SiGe HBT circuits [6]. Due to the differential amplifier inherent in ECL designs, the critical charges are small unless specifically designed for large bias currents.

Discrete device charge collection measurements have been performed on GaAs HBT devices. McMorrow *et al.*examined charge collection in discrete GaAs-based HBTs and did not observe charge enhancement [7]. Yaktieen *et al.*performed single-event upset (SEU) experiments on GaAs-based HBT integrated injection logic (HI^2L) circuits and have shown very low linear energy transfer (LET) thresholds [8].

Earlier results show that a laser-induced single event may temporarily incapacitate a circuit operating in the gigahertz realm for several clock periods [9]. The capability to measure *in situ* voltage transients within various nodes in the circuit is used to provide verification for these simulations.

The goal of this effort was to see if the simulation could mimic the qualitative behavior of previous experimental measurements, understand charge transport, and then examine techniques to decrease SEE sensitivity.

II. Simulations

The computer analysis utilized Silvaco's ATLAS, MIXEDMODE, and SMARTSPICE software for linked device and circuit analysis. The simulation was composed of two HBTs in a differential pair modeled in the device simulator ATLAS and the remaining ECL devices in SMARTSPICE. Both programs share boundary conditions at the ATLAS device contacts. The simulated 10-GHz circuit output was compared to experimental measurements. The circuit schematic of the simulation is shown in Fig. 1. Transistors ahbt1 and ahbt2 (differential pair) are modeled in the two-dimensional (2-D) device simulation to provide perfect matching of the differential pair.

A. Device Characterization

The devices were modeled after the HRL Laboratories InGaAs–InP HBT process [10], [11]. A cross section of the modeled HBT is shown in Fig. 2. Half of the HBT width is modeled due to symmetry of the transistor. The actual HRL HBT includes a superlattice AlInAs–InGaAs emitter–base junction. We choose not to include the superlattice because the ATLAS code presently could not model quantum tunneling through the base-emitter junction. We utilized a technique used by previous researchers modeling the superlattice as a stepped bandgap [10]. The Al concentration and thermionic emission constants were

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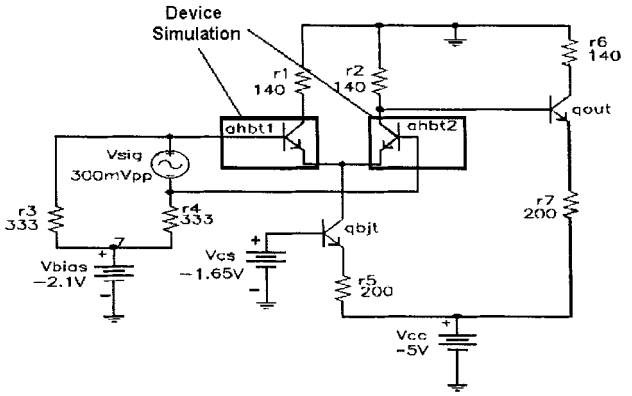

Fig. 1. ECL circuit schematic; devices ahbt1 and ahbt2 are modeled in the device simulator. Note: ahbt2 is modeled with two parallel structures as shown in Fig. 3.

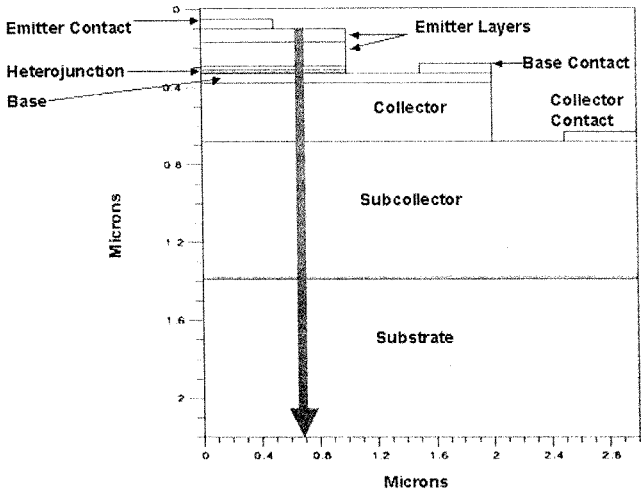

Fig. 2. Cross section of modeled HBT transistor. Dotted line shows location of simulated ionization track.

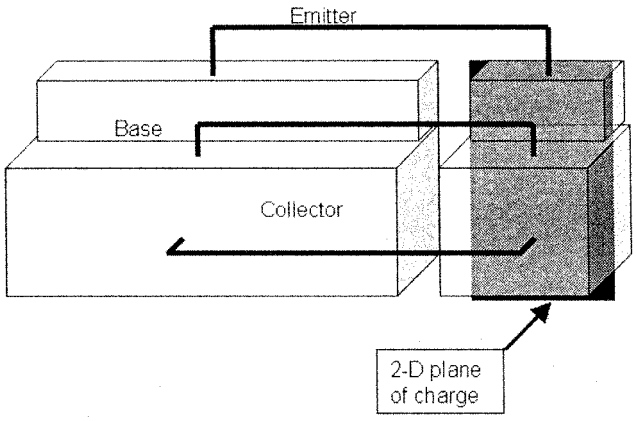

Fig. 3. Illustration of how the SEE ionization is simulated with two parallel 2-D structures.

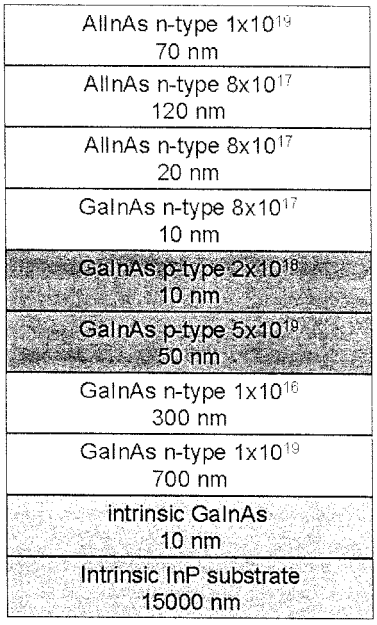

Fig. 4. Modeled structure from (a) emitter to (b) substrate. Not to scale.

modified to match current densities in the E-B junction. The geometry modeled had 15-μm (y) depth and 3-μm width (x) (half of the device width). The two-dimensional results were normalized to be equivalent to a 20-μm^2 emitter area of the actual device.

The single-event induced in the HBT is modeled with two structures in parallel tied to common contacts. The purpose of modeling two structures in parallel was to prevent the effect of a single plane of ionized charge from altering the fields along the HBT's complete length. Utilizing one short-width 2-D simulation (1 μm wide) for a heavy ion event, with a second 2-D larger width (9 μm) tied in parallel, allows one-tenth of the device to be ionized. The disadvantage [being short of a full three-dimensional (3-D) simulation] is that transport is prevented directly between the two "parallel" device structures. The contact boundary conditions for both structures are identical. This technique has been used previously to examine 2-D GaAs MESFET simulations for comparison to 3-D [12]. Fig. 3 illustrates the use of two parallel 2-D simulations. With this technique, we could examine the effect of a single 1-μm (z-direction) plane of charge where the other 9-μm device's electric fields are only influenced by the contact potentials from the perturbed "1 μm" device. We could hypothesize that E_Y would be more dominant than E_Z in the HBT supporting this approach; further work comparing this technique to a 3-D simulation could clarify this issue. The dc and ac characteristics of the "1 μm + 9 μm" device are identical to a device with 10 μm width modeled as a single HBT.

The layers of material modeled are shown in Fig. 4, where the top AlInAs layers are the emitter, p-type InGaAs layers are the base, and n-type InGaAs layers are the collector and subcollector and an InP substrate. Mobility, bandgap, lifetimes, band alignment, and velocity parameters were obtained from various references for the HRL HBT process [10], [11]. The ATLAS model included Shockley–Read–Hall, optical, and Auger recombination. Summation of all device currents was less than 3 nA (0.5 ppm of SEE current) to confirm that numerical error was minimal. Individual device simulations of the HBT were compared to I_C versus I_B, I_C versus V_{BE} and h_{FE} measured data.

B. Circuit Characterization

The circuit modeled was an ECL inverter identical to the circuit utilized in previous work [1]. The complete circuit is

a divide-by-two, composed of an input buffer, 2-bit counter, and output stages. For this study, the first inverter in the input stage was modeled. The ECL circuit is biased at $V_{cc} = 0$, $V_{ee} = -5$ V.

C. Combined SEE Device and Circuit Analysis

The analysis investigated the effect of charge ionization on one of the two differential pair transistors.

For this work, the effective ionization track volume was $0.2 \times 1 \times 15$ μm^3. The optical beam command in ATLAS was used to implement the ionization. The vertical ionization track occurs between 0.6 and 0.8 μm on the x-axis, just to the right of the emitter contact. The energy in the pulse was 3.6 pJ with an optical pulse width of 1 ps deposited over 15 μm with 1.46 eV/e-h pair to estimate an equivalent LET of 9.65 MeV/mg/cm^2. A conversion factor of 17 fC/μm equivalent to an LET $= 1$ MeV/mg/cm^2 for InP was chosen.

In previous laser photoconductive probe experiments, the most sensitive effects were observed between the input clock phase of 180–270°, where the transistor is in the process of turning off [9]. The simulation examined a single event occurring at a phase angle of 250° (170 ps into the simulation). Ten periods of the 1-GHz clock signal were analyzed. The event is introduced in the second period to allow charge densities to reach equilibrium equivalent to normal operation.

III. Results

The various SEE simulations performed were as follows.

1) LET $= 10$ (3.6 pJ, 1.46 eV) introduced at 170 ps in z $=$ 1 μm device with a z $= 9$ μm device in parallel. Unmodified InP substrate.
2) LET $= 10$ (3.6 pJ, 1.03 eV) introduced at 170 ps in z $=$ 1 μm device with a z $= 9$ μm device in parallel. Unmodified InP substrate.
3) LET $= 100$ (36 pJ) introduced at 170 ps in z $= 1$ μm device with a z $= 9$ μm device in parallel. InP short lifetime buffer in the substrate.
4) LET $= 10$ (3.6 pJ) introduced at 170 ps in z $= 1$ μm device with a z $= 9$ μm device in parallel. InGaAs short lifetime buffer in the subcollector.

In all cases, the right-side HBT in Fig. 1 (ahbt2) was the single-event ionized device.

A. SEE of Unhardened HBT

The effect of the 3.6-pJ pulse created qualitative behavior similar to experiments in that the collector potential dropped and recovered over several clock cycles. The collector node of the perturbed HBT drops approximately 100 mV negative and then recovers to the initial dc level. Node 2 (ahbt's collector voltage) is shown in Fig. 5.

The substrate during a normal operating condition simulation has very low hole concentrations in the substrate and collector regions. Following the single event, holes are generated in the substrate and migrate toward the base–emitter junction. Fig. 6 shows a plot of hole concentration at 430 ps (260 ps after the SEE event). Holes remain in the InP substrate and the InGaAs subcollector. A closer examination of the base region shows an

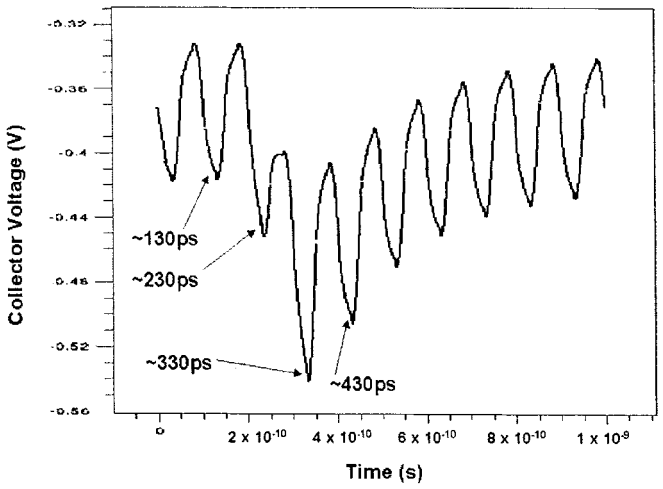

Fig. 5. Voltage transient of the collector node of ahbt2.

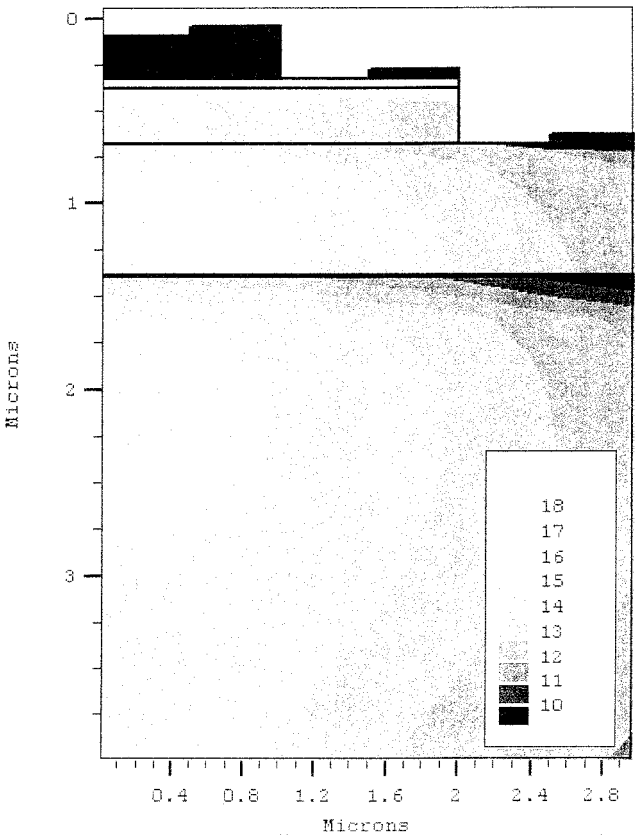

Fig. 6. Hole concentration at 430 ps in the simulation (260 ps after the SEE event). Contour units are in $\log_{10}$ (holes)/cm^3.

increase in holes increasing in the base. Figs. 7 and 8 show plots of hole concentration at 230 ps (60 ps after event) and 430 ps (260 ps after the SEE event). Due to the wide bandgap emitter at the emitter–base junction, holes are impeded from entering the emitter. Holes exit the base region by recombination or by exiting the base contact. Fig. 9 shows a plot of emitter, base, and collector currents. The three currents add to zero, which satisfies current conservation. The majority of base contact current is hole current. Fig. 10 shows the difference in electron and hole quasi-Fermi levels between time periods of identical phase

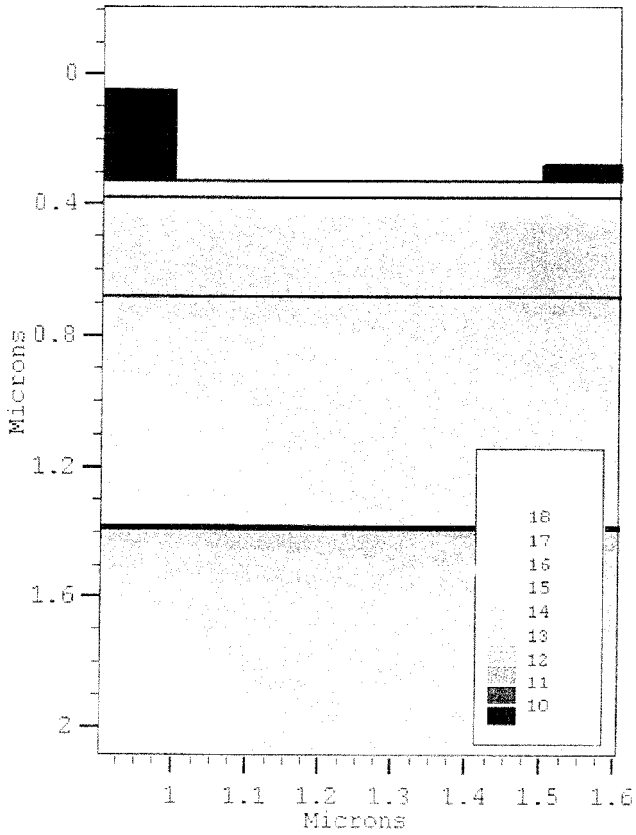

Fig. 7. Closeup view of hole concentration in the base region at 230 ps. Contour units are in $\log_{10}$ (holes)/cm^3.

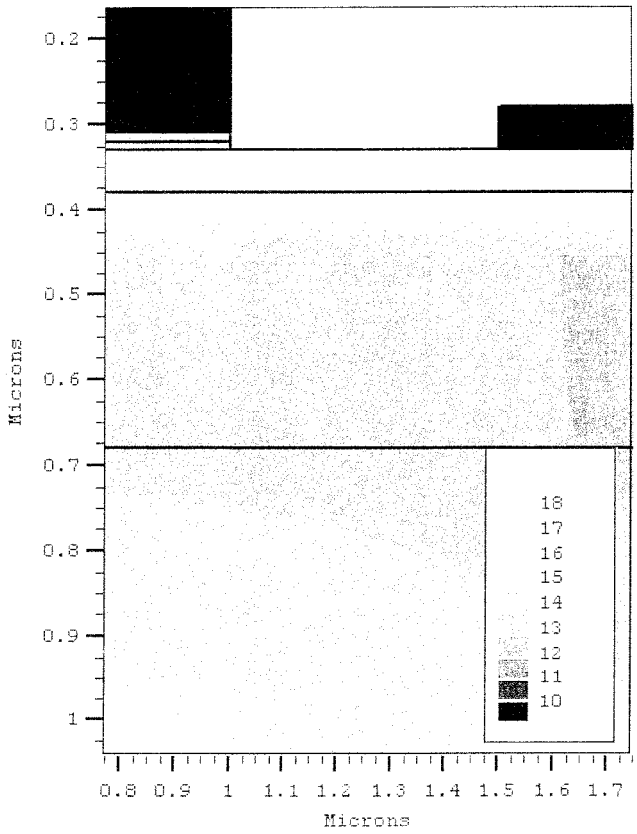

Fig. 8. Close up view of hole concentration in the base region at 430 ps. Contour units are in $\log_{10}$ (holes)/cm^3.

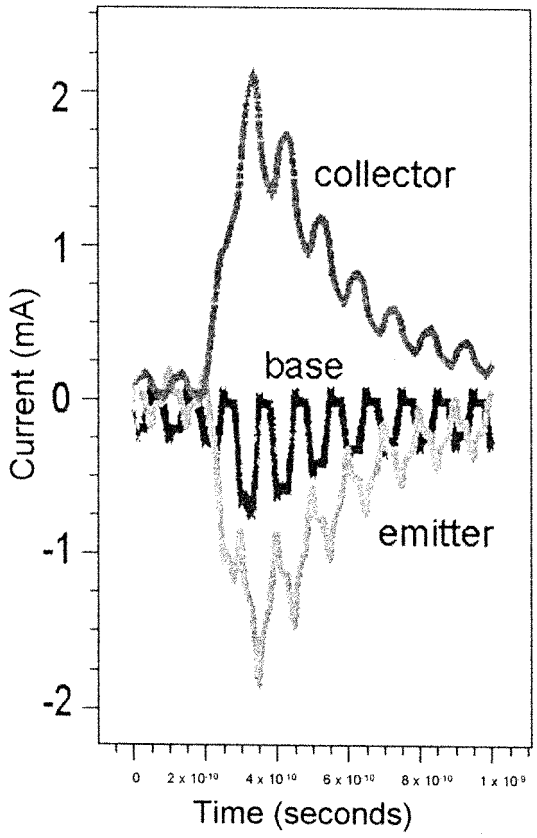

Fig. 9. Currents of emitter, base, and collector of ahbt2.

in the 10-GHz waveform. In an ideal situation, the plot should show a zero difference throughout. Fig. 10 clearly shows that a positive net charge is located throughout the device. The largest differences occur in the substrate, subcollector, and collector and less in the base and emitter. Holes are attracted toward the negative emitter, while electrons collect at the collector. To further investigate, ionization was limited to the InGaAs regions by reducing the beam statement photon energy to below the InP bandgap but above the InGaAs bandgap.

B. SEE of HBT With 1.03-eV Photons

A simulation with photons of 1.2 μm was performed. Charge is ionized in the base, collector, and subcollector in the InGaAs, the smaller bandgap material. No ionization occurs in the wide bandgap emitter or substrate. No perturbation was observed in the voltage transients. The ionization of carriers in the InGaAs and not the InP regions has no observable effect on the circuit.

C. SEE of HBT With Short Lifetime InP Buffer

From the results obtained from the 1.2-μm photon simulation, the effect of utilizing a short lifetime buffer (1 ps) in the InP material to absorb excess charge migrating out of the substrate was examined. Fig. 11 shows the cross section of the device modeled with a short lifetime InP buffer layer. Results of the simulation are shown in Fig. 12. The negative shift of the collector waveform was reduced from 80 to 20 mV, a factor of four.

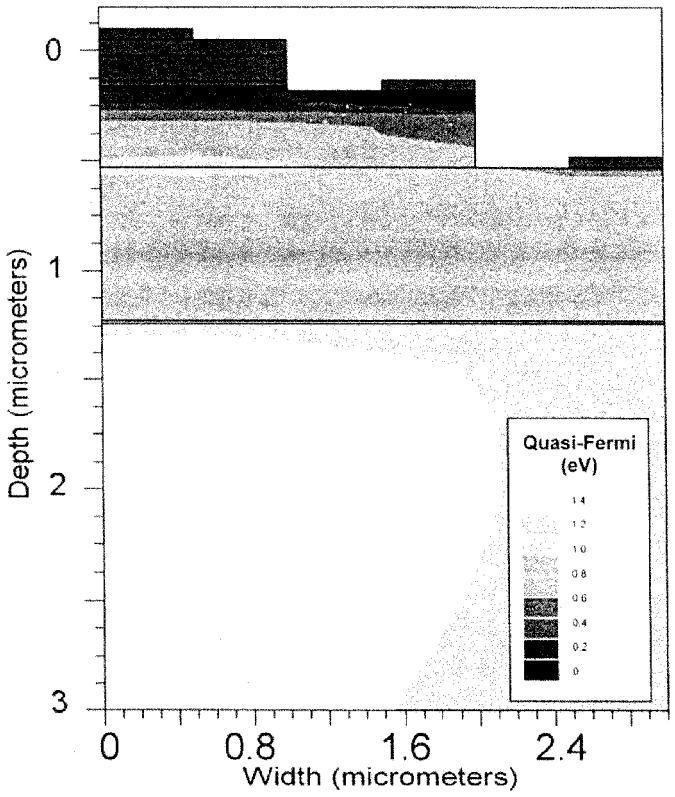

Fig. 10. Quasi-Fermi comparison between normal conditions and SEE event at 260 ps after the SEE event. Difference is taken at same phase to input clock signal.

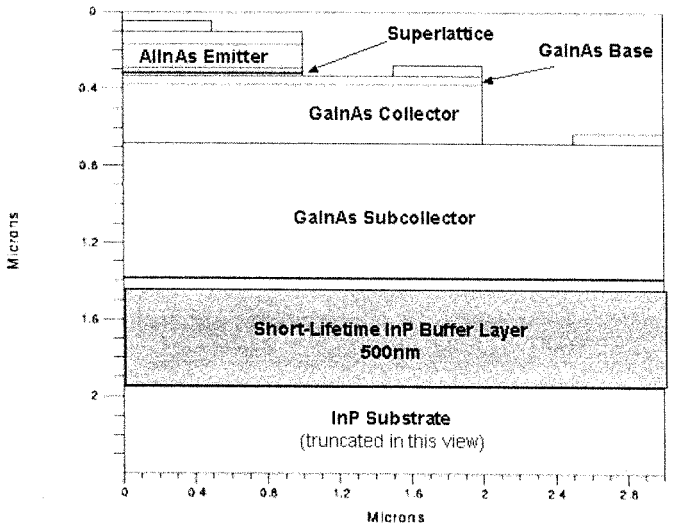

Fig. 11. HBT modeled with InP buffer in substrate location. Note GaInAs is equivalent to InGaAs.

D. SEE of HBT With Short Lifetime InGaAs Buffer

Moving the short lifetime buffer into the bottom of the InGaAs subcollector yielded much improved results. Fig. 13 shows the location of the short lifetime InGaAs buffer. With an increase of an order of magnitude of ionized charge, no perturbation was observed in the collector waveform. Fig. 14 shows a comparison of the hole concentration between the original LET $=$ 10 and the LET $=$ 100 InGaAs buffer simulation at

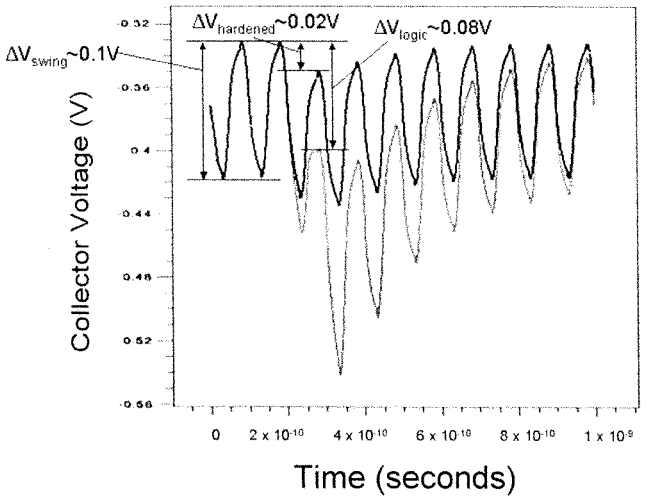

Fig. 12. Voltage transients of collector for unhardened and InP buffer case.

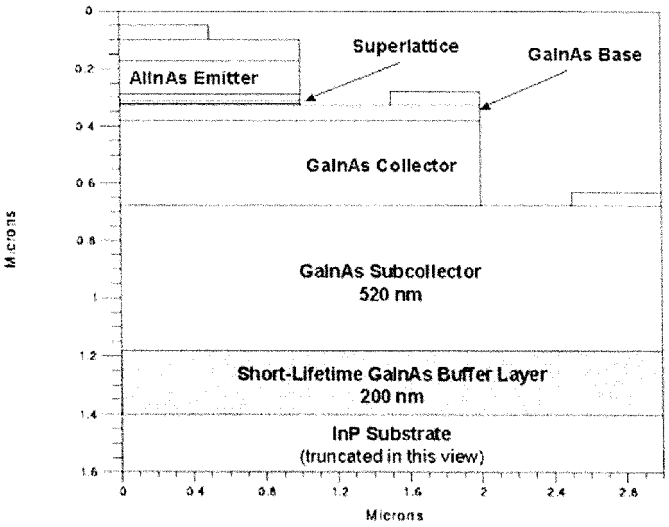

Fig. 13. HBT modeled with InGaAs buffer located below subcollector. Note GaInAs is equivalent to InGaAs.

430 ps. Essentially holes are eliminated in the collector and subcollector.

IV. Discussion

A. Mechanisms Effecting Circuit Waveforms

Operation of the ECL circuit relies on the switching of current between each side of the differential pair. Current is directed to either of the collector load resistors, and the resistor load voltage is transferred from the differential pair collectors by an emitter follower. In this study, the charge collection on the side (ahbt2) of the differential pair that is turning off was examined. This was the device most sensitive to SEE from observing previous voltage transient measurements [9].

For the n-p-n HBT to switch off, the HBT relies on minority carriers (electrons) recombining quickly in the p-type base. Holes reaching the base region keep the B–E junction forward biased, injecting electrons into the collector. If the n-p-n HBT cannot switch off, current continues to flow through the collector load resistor, causing the collector voltage to be more

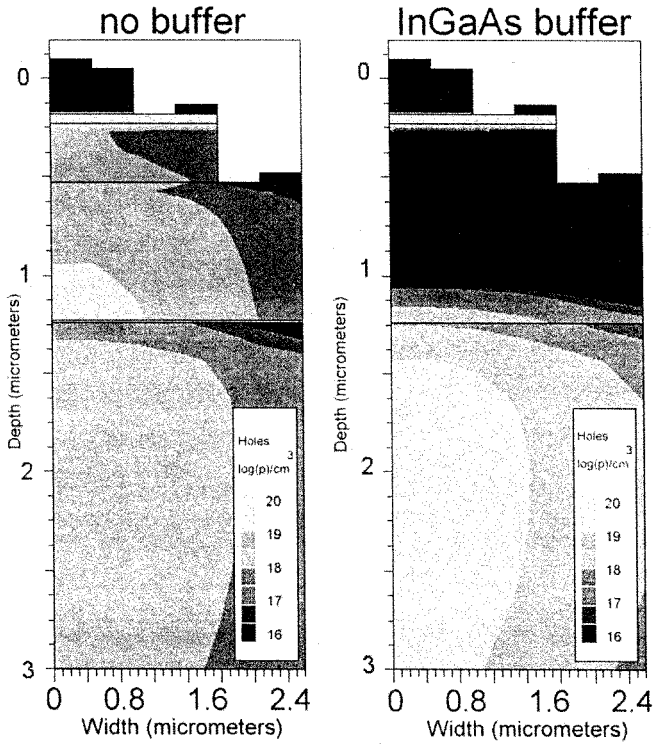

Fig. 14. Hole concentration of (a) unhardened and (b) InGaAs buffer structure at 430 ps. Contour units are in $\log_{10}$ (holes)/cm^3.

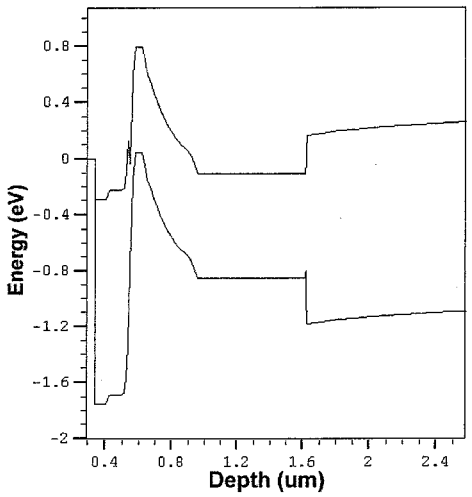

Fig. 15. Band diagram of original HBT structure.

negative than required (Fig. 5). The carriers that provide this excess current are a combination of ionized electrons attracted to the positive collector and emitter electrons induced from the ionized holes that charge the base potential. No displacement currents were observed in any of the terminal currents, concluding that carrier conduction is the main current mechanism.

Eliminating stored holes in the base should cut off the emitter current. The source of the holes is from ionized holes in the collector, subcollector, and substrate. In the simulation, these regions account for 97% of the simulated device depth. From Fig. 9, the integral of collector current is approximately 30% of the total ionized charge in the 15-μm-long track. The base current holds at an increased level even after the emitter current reduces, showing that base saturation exists after 830 ps.

To further investigate this theory, a laser simulation (unlike a heavy-ion simulation) lowering the photon energy (1.03 eV) that only ionizes charge in the InGaAs regions (base, collector) showed no perturbation in the collector waveforms. These results point toward the ionized charge in the substrate to be the majority factor in determining SEE response. Examining a band diagram of the structure in Fig. 15 shows that the valence band provides a path for holes to source to the base region. Due to the band bending of the InGaAs subcollector to the InP substrate, a small barrier to holes is present at the substrate interface. This barrier dampens the rate of holes exiting the substrate and thus prolongs the hole substrate current to the base region.

B. Base–Emitter Superlattice Issues

As stated earlier, this simulation did not include a base–emitter superlattice. The purpose of introducing a heterojunction in a bipolar junction transistor is to reduce reverse injection in the emitter from holes in the base. A superlattice HBT further improves emitter electron tunneling into the base. The hole transport rate from base to emitter is essentially unchanged when the superlattice is added to the HBT [13]. Holes in the base can be removed by recombination, injection in the emitter, or the base contact. Examining Fig. 9 may infer that base contact current is probably the most efficient path to remove holes in the base, especially on negative V_{be} inputs. The simulation results shown in this paper clearly shows the source of ionized holes from the collector and substrate to be the primary mechanism for SEE sensitivity. The use of a short lifetime buffer in the collector or subcollector should provide similar results when hardening an HBT incorporating a B–E superlattice.

C. Effect of Short Lifetime Buffers

Short lifetime buffers have been used in GaAs FET technology to eliminate SEE susceptibility [14], [15]. The buffer provides increased recombination to eliminate excess charge from reaching the transistor. Two types of buffers were examined: 1) an InP buffer in the substrate and 2) an InGaAs buffer below the subcollector. Both buffers were modeled with a 1 ps lifetime, and both were chosen to have intrinsic resistivity.

Fig. 16 shows a band diagram of the InP buffer structure. Due to the smaller InGaAs bandgap, charge that is ionized in the collector and subcollector does not reach the substrate but does reach the base region. This approach only eliminates charge in the InP substrate, causing a factor of four in the negative shift of the collector voltage dc level.

Placement of a short-lifetime buffer in the subcollector region allows recombination of charge in the collector regions while also recombining charge exiting the substrate layer. Fig. 17 shows the band diagram of the InGaAs buffer structure. The InGaAs buffer provided complete single-event immunity with an order of magnitude increase of induced charge (36 pJ or approximately an LET of 100 MeV/mg/cm^2).

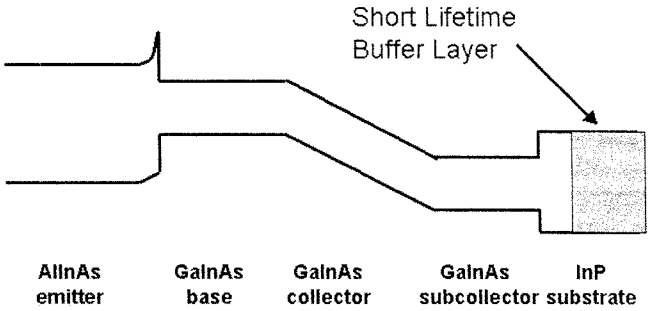

Fig. 16. Band diagram of InP buffer located in substrate.

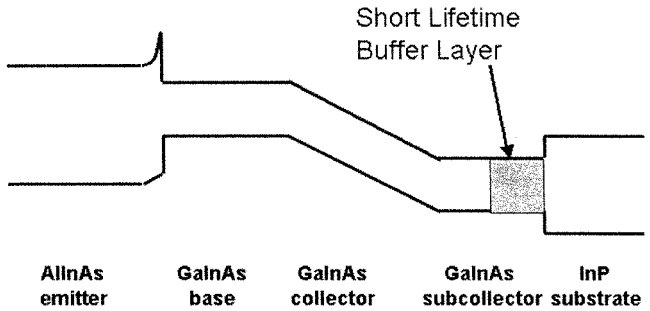

Fig. 17. Band diagram of InGaAs buffer located below subcollector.

D. Implementing a Buffer Solution

The results in this paper show a promising technique that could reduce SEE sensitivity. To implement an InP buffer in the substrate, a high-resistivity material must be used to prevent leakage between devices and the buffer must be lattice matched to the InP substrate. Presently, low-temperature grown InP has shown low resisitivities [16] insufficient to use in a VLSI fabrication process where device isolation is required.

If a buffer is implemented in InGaAs, a low- or high-resistivity buffer would be acceptable. Ballingall *et al.*have demonstrated a picosecond-lifetime low-temperature grown InGaAs with $x = 0.35$ mole fraction [17]. To lattice match the InP substrate, an $In_{0.52}Ga_{0.48}As$ buffer is required. This has not been demonstrated at this time. Even if such a buffer could be demonstrated, the ability to remain stable in a molecular beam epitaxy manufacturing environment would need to be investigated.

V. Conclusion

We are providing the first dynamic device/circuit SEU analysis of InP-based HBTs in an ECL circuit and a technique that may be used to harden the technology to SEEs at gigahertz clock rates. Such a hardening technique using short-lifetime buffer layers would eliminate the possibility of SE effects. These results show that simple HBT structures could be hardened, and the authors suggest that improvement could also be obtained with superlattice HBT processes.

The disadvantage to implementing such a characteristic buffer to harden for SEE is that no performance enhancement would be expected, while process complexity and cost would be increased. Only applications critically degraded by SEE would benefit from short-lifetime buffers below the subcollector.

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