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RADIATION EFFECTS IN HIGH SPEED III-V INTEGRATED CIRCUITS

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The types of applications affected by radiation effects in III-V devices have significantly changed over the last four decades. For most applications III-V ICs have provided sufficient radiation hardness. Some expectations for hardened soft error applications did not materialize until much later. Years of research defined that not only material properties, but device structures, layout practices and circuit design influenced how III-V devices were susceptible to certain radiation effects. The highest performance III-V ICs due to their low power-speed energy products will provide challenges in ionizing radiation environments from sea level to space.

Keywords: Radiation; GaAs, InP, GaN, SiC, compound semiconductors, total dose, displacement damage, single event effects

1. Introduction

The concept of radiation effects in electronics has changed significantly over the last half century. Initially from nuclear weapons and reactor applications to space effects and background terrestrial sources each application requires a special understanding of the radiation source and the delivery spatially and temporally to the target material. Once the incident energy enters the target material it transfers into the electrical circuit (ionizing radiation) or modifies the semiconductor crystal (displacement damage). This review explains how high-speed III-V integrated circuits are affected by radiation. Neither the incident particle types or the basic physics of the particle interaction has changed; only the size, materials and switching energy requirements of our circuits have changed dramatically. Today ICs switch on the order of 1,000s of electrons, instead of tens of millions electrons switched per bit in the 1970's. Due to this continual reduction of switching energy, more background particles can influence device operation. Compound semiconductor ICs has led this reduction of power-speed products (Joules/gate). Low power-speed product circuits are susceptible to more ionizing particles in the environment than with earlier generation electronic technologies.

Compound semiconductors were pursued in Department of Defense research to provide a substantial improvement over silicon-based ICs. In most cases, the first GaAs integrated circuits provided promising rad-hard results that supported the use of III-V devices for the military needs for high performance ICs.[1] The lack of oxides and wider band-gaps led many to believe that all III-V ICs would provide radiation-hardened ICs without substantial modifications. However, the substitution of material alone could not provide radiation-hardened devices at a time when feature sizes, geometries, new structures and circuit topologies contributed to sensitivities to fast local ionization, i.e. single event effects (SEE). The following review of radiation effects in the high-speed compound semiconductors outlines the past history and future directions. Before

investigating the specifics, the cause for some misunderstanding lies in understanding the types of radiation effects. The following provides a brief summary of the most common radiation effects, background in our learning process on radiation effects in III-Vs, specific issues describing the advantages and disadvantages observed in compound semiconductor ICs, and the author's expectations of the future susceptibility of III-V ICs.

1.1. *Radiation effects categories*

Radiation can mean any source of energy that in influences the operation of electronic devices. Light and heat can be considered radiation. However, specifically when the term radiation effects are used this refers to the situation where concentrated energy has influence on electronic devices beyond the normal realm of applied voltage. Semiconductors predominantly interacts with electrons, photons and phonons on the order of a couple of eVs. Any particle more energetic than thermalized electrons could be considered radiation. An example of such particles would be gammas from a couple eV up to GeV heavy ions in space. These various radiation sources can cause reliability problems anywhere from temporary loss of data, circuit degradation, loss of functional operation to destruction of the semiconductor device, either by ionizing carrier densities to very high levels, or creating defects above background levels.

In the field of radiation effects in electronics we must divide the source characteristics and the delivery of these high-energy particles into subsets of effects regardless of the target material. The four most common categories are:

- total dose or total ionizing dose (TID),
- dose rate, gamma dot,
- single event effects (SEE), and
- displacement damage effects

The first three categories generally relate to ionizing radiation, where high-energy particles create electron and holes in pairs. In the last category, higher energy particles can not only ionize electrons but will introduce the atomic displacements in the semiconductor lattice. Such displacement introduces defects that alter the electrical properties of the semiconductor. Therefore depending on the environment, ionizing and displacement damage effects can occur, or only ionizing (charged particles, photons) or only displacement damage by uncharged particles (neutrons).

One common misperception is that the resilience of a technology against one of the several radiation effects implies that the technology is immune to all radiation effects. It is vital that the designers of devices, circuits and systems be aware of the high energy particles available in their operating environment be it, sea level, high altitude avionics, near heavy metals, space or strategic weapon environments. The device must be characterized for each aspect of the radiation environment.

1.1.1. *Total Dose Effects*

The total dose environment refers to the absorbed dose of energy in rads (ergs/g) that the semiconductor material has been exposed to. If the target material is silicon the unit of radiation is referred as Rad(Si). Total dose only accounts for absorbed energy for ionizing electrons. Other names for these effects are gamma, or total ionizing dose. Such environments would include:

- Gammas, electrons, protons in a space environment
- X-rays, gamma radiation from nuclear weapon detonations
- Gammas emitted from radioactive material

The most susceptible transistor materials to total dose effects are insulators. Ionized positive charges in an oxide move relatively slow (possibly years to move microns). Charges trapped in oxide-insulated field effect transistors (FET) shift threshold voltages. Charge trapped in gate or field oxides alters the device characteristics. Due to the lack of oxides in III-V devices compound semiconductor ICs have not shown serious degradation to total dose effects. III-V MESFETs or HEMTs are essentially immune in the harshest total dose environments.

1.1.2. *Dose Rate Effects*

Dose rate effects relate to the rate of absorbed ionizing dose is occurring, independent of the total dose. The effect is only discussed in the design of devices that must operate and/ or survive in the vicinity of a nuclear event. Such rates are described in units of Rad/sec absorbed, i.e. 10^9 Rad/sec. Even though a dose rate of 10^{11} Rad/sec appears high the source of radiation may only exist for several nanoseconds, thus the total absorbed dose is on the order of thousands of Rad(Si). High dose rates during the irradiation period convert a semi-insulating substrate into a highly conductive substrate for nanoseconds. Power and ground buses on the substrate become linked in temporary low impedance paths usually resulting in damage due to high currents. Hardening to dose rate effects requires considerable attention to circuit layout, packaging and power bus design.

Insulating or high resistivity substrates do provide the best protection to dose rate effects. Semiconductors materials with wide band-gaps (i.e. low intrinsic carrier densities) are the most desirable. Wide band-gap compound semiconductor devices produce lower photocurrents than silicon-based ICs.

In recent years the term "dose rate" has also been applied (to the opposite extreme) to testing of total dose effects using Co^{60} gamma sources. When radiation testing oxides the amount of oxide trapped charge is dependent on the experiment's dose rate. The dose rates of total dose experiments are operated from mRad/sec to 100's of Rad/sec much lower and much longer periods than dose rate effects related to nuclear events.

1.1.3. *Single Event Effects*

The two previous ionizing effects relate to absorbed dose over the complete IC. The situation of an individual energetic particle inducing errors or failure to an individual circuit node, or device is categorized as a Single Event Effects (SEE). Unlike Total dose and dose rate effects which have been examined since the 1950's, SEE only became known once electronic devices had miniaturized to require switching energies comparable to energy transferring cosmic rays in the space environment[2] and then alphas from packaging materials in 1978.[3] Wallmark in 1962 had predicted that eventually cosmic ray interaction would become a reliability issue.[4] In 1990's neutrons at aircraft altitudes were recognized to induce SEE.[5] In the late 1980's soft errors from solder emitting alpha particles forced IC manufacturers to obtain low alpha or alpha-free solder.[6] The environments that can induce SEE have and will increase with IC generations that continue to lower power-speed products.

GaAs SRAMs early on showed some susceptibility to SEE, which became its Achilles' heel for radiation applications requiring SEE immunity.[7] Early predictions expected SEE immunity would be based on the larger band-gaps to create less ionization than observed in a Si substrate. The high speed III-V circuits operated on much smaller switching energies due to low voltage swings, low capacitance and additionally had long diffusion lengths in semi-insulating substrates and non-insulating gates that amplified the SEE susceptibility. Today much more is understood about SEE in III-V integrated circuits, and the capabilities of new growth, materials and circuit techniques can provide designs hardened for SEE.

1.1.4. *Displacement Damage Effects*

Displacement damage introduces defects in semiconductors. The electron and proton Van Allen belts, neutrons from nuclear events, or implantation in manufacturing are all environments where displacement damage is observed. Low-doped or intrinsic structures such as solar cells and detectors are sensitive to displacement damage effects. Mid-gap defects increase trapping and recombination processes, analog devices such as bipolar transistors that are highly dependent on base recombination normally degrade due to displacement effects.

The displacement energy transferred to a crystal lattice is referred as non-ionizing energy loss (NIEL), and the electrical defects introduced is related to the binding energies of the atoms, the band structure, and defect transport in the semiconductor. Compound semiconductors like the Group 4 semiconductors can vary their response to displacement damage effects. Intrinsic and low-doped semiconductors are most vulnerable to defects introduced by displacement damage. Depending on the application, one or more of the previously mentioned radiation effects will require characterization. In the next section the chronologically of those applications are discussed.

2. Background

In Table 1 a chronological listing of initial events in the study of III-V radiation effects ICs is shown. Examining Table 1 by the types of studies performed these studies can be divided into three general periods or applications.

- Cold War radiation studies (1960's through 1980's) – Application of III-Vs ICs to military applications, mainly analog amplifiers and photodetectors. Radiation effects related to neutron, total dose and dose rate effects were important to these applications. Most of this work was on discrete devices.

- Space systems use of III-V devices (1980's – 1990's) – The prospect of replacing CMOS/SOS and Si technologies with digital GaAs ICs required radiation characterization in total dose and SEU.

- High-speed communications (1990's- 2000+) – The advent of high speed III-V ICs (GaAs, InP) for Internet and wireless applications require low bit error rates. Applications in both space (cosmic particles) and terrestrial (solder emitting alphas) are susceptible to SEE (i.e. soft errors). These new high speed ICs required understanding of radiation effects at high frequencies.

Future application of compound semiconductors will further require radiation effect studies in,

- High power III-V devices – The future use of GaN and SiC for microwave and low frequency power in military and commercial space applications will require knowledge of displacement damage and ionizing effects.

Table 1 - Timeline of Radiation Effects firsts related to III-V devices

Year	Event
1961	Electron radiation effects on unipolars[8]
1970	Neutron irradiation of GaAs JFETs[9]
1978	Total dose measurements? on GaAs MESFETs[10]
1979	First dose rate study of GaAs FETs[11]
	Dose rate studies on GaAs ICs[12]
1981	Dose rate effects on GaAs photodetectors[13]
1982	Dose rate latchup studies in GaAs ICs[14]
1983	First JFET SRAM SEU proton experiments[7]
	First JFET SRAM heavy ion SEU experiments[15]
1991	First GaAs MESFET SEU data from space experiments[16]
1995	First experiments on dynamic SEU testing of GaAs SEU[17]

Chaffin summarizes early work on radiation damage in GaAs in 1973.[18] A further review of total dose, dose rate and displacement damage (mainly neutrons) has been presented by Simons[1]. Zuleeg presented a chapter on radiation effects in 1985 that reviews the work on weapons effects and emerging space applications.[19] Srour et al provided a review of radiation effects in ICs including a section on GaAs effects.[20] Zuleeg provided an extensive review article in 1989.[21] Zuleeg's work provided a thorough discussion on dose rate and neutron damage effects and later discusses the SEU work on Complementary JFETs.

There was a large amount of open literature up to the mid-1980's investigating total dose and dose rate effects on GaAs. Much of this work showed that GaAs ICs were superior to silicon-based ICs in the weapon environments where dose rate, neutron displacement and total dose effects are important.[21] Most of the devices in these applications were discrete transistors and photodetectors.

In other applications such as space, where memory and logic ICs in satellite systems were required, digital GaAs technologies were just becoming available. Since these ICs were in their infancy in the early 1980's, little data was available on any radiation effect, particular SEE. Additionally the SEE field started in the early 1980s after May et al's work in Si DRAMs.[3] The only III-V ICs available at the time were SRAMs that showed excellent total dose hardness but few results were available in the 1980's on GaAs SEU.[19] Since little concrete SEU data was available and GaAs ICs had shown tolerance to total dose effects the general assumption was the SEU issue would not be important.

Despite some optimistic expectations, the SEE performance of digital circuitry based on compound semiconductors was essentially no better than that of non-hardened silicon CMOS. The CMOS/SOS technologies and CMOS/SOI SRAMs showed superior radiation hardness to the reported GaAs SEU results.[22] From the late 1980's to the mid-1990's investigations utilized circuit modeling similar to Si SEE radiation studies, but the problems required deeper understanding with device simulation in the early 1990's. The 2-D modeling codes were becoming available in the early 1990's that allowed researchers to study the SEE phenomena.[23] Additionally the experimental data into charge collection mechanisms was available by the early 1990's.[24] The reasons for the SEE sensitivity were several fold, small power speed products,[16] long diffusion lengths in semi-insulating substrate, backgating and parasitic bipolar transistor effects in the charge collection process and material ionization rates.[25] In 1995 McMorrow et al presented a review of these GaAs SEE mechanisms.[26] The advantage of GaAs's e-h pair ionization energy (4.8eV) over Si (3.6eV) was not sufficient to outweigh the other disadvantages. In the mean time the size of VLSI Si and CMOS/SOI far outpaced the performance of GaAs SRAMs and microprocessors in gate count and performance/cost ratio.

By 1995 solutions were available to make GaAs ICs immune to SEE[27], and for a short time Motorola was ramping up capability to manufacture rad-hard large high-speed GaAs ICs for the Celestri satellite constellation.[28] However market pressures eliminated Celestri, and Motorola joined with Teledesic, thus dropping the digital GaAs effort. During this time the Motorola's rad-hard digital GaAs technology was incorporated into a few satellite systems.

Today many high-speed communications circuits are being transitioned to other III-V technologies (i.e. InP-based) from GaAs FET ICs. Many of these applications require optoelectronic capability and high-speed requirements that for the most part are only available with direct-bandgap III-V ICs. A small subset of these applications is used in military and commercial space applications. But instead of SRAMs and microprocessors, which were the focus in the 1980's, researchers have investigated these new types of III-V ICs in such applications as crosspoint switches and Application Specific ICs (ASICs).

SEE is still the critical radiation effect for the majority of applications, but testing and studies have migrated to high speed dynamic testing where unlike a decade ago all SEE studies concentrated on soft errors in SRAM storage. Additionally the designs of consumer ICs in terrestrial applications are requiring radiation related reliability studies. The terrestrial sources are atmosphere neutrons; package or solder emitted alpha particles, or cosmic particles at sea level.

Looking ahead, the transfer of GaN and SiC-based devices to high power space applications will also require new studies on displacement damage, destructive SEE effects, and possible passivation issues with total dose effects. The extensive study by DoD laboratories in the 1970's and 1980's is less applicable to the new class of III-V ICs because new compounds, different device structures, geometries and fabrication methods exist today than those used two to three decades ago.

3. Specific Effects in III-V ICs

3.1. *Why are III-V ICs resilient to total dose and displacement damage?*

The absence of oxides in III-V transistors was a major advantage that III-V FETs and HBTs had over the MOSFETs for total dose effects. If Si MESFETs or JFETs were available for circuits, they also would provide higher thresholds to total dose effects over MOSFETs. The III-V substrate material was indirectly responsible for this advantage because gate-insulating oxides were not available. Co^{60} gamma testing provided many exceptional results for GaAs ICs, all above the Mrad(Si) level. MMICs are shown to operate above 10^9 rads before degradation.[29] GaAs JFET SRAMs showed operation to 100Mrad(Si).[30] These levels are magnitudes above those required for the most severe natural environments.

Displacement damage from neutrons showed levels between 10^{14} to 10^{16} n/cm^2.[31] In comparison studies in 1994 of neutron fluence damage on Si JFETs, Si MOSFETs, GaAs MESFETs, the GaAs devices were unaffected to 55Mrads.[32] For both total dose and displacement damage effects devices fabricated on epitaxial material normally performed better than ICs in ion-implanted processes.

The insensitivity of III-V devices to these radiation effects was well known by the early 1980's. Several defense contractors had positioned themselves to provide radhard

GaAs ICs for the DARPA's GaAs initiative, which developed high performance ICs for military systems. Several other factors also came together in the early 1980's. One was the personal computer flourished, increasing the overall demand for cheap ICs (i.e. bulk CMOS), thus increasing commercial demand that eventually attracted IC defense contractors to move into the commercial market. By the end of the 1980's almost all of the initial DoD GaAs foundries had migrated into commercial microwave or ASIC products. Second, the soft error phenomena (i.e. SEE) became important in the radiation effects field, not solely because of materials, but also due to reduced feature size. The GaAs devices further pressed lithography and lowered power-speed products to obtain the highest performance to keep ahead of Si benchmarks. A third factor to exacerbate the SEE was the semi-insulating substrates. The dose rate effects in GaAs benefited over Si substrates due to the higher resistivity but the high density of the GaAs material provided higher ionization of carriers per unit length than silicon substrates.

3.2. *Why is there a high sensitivity to soft errors in III-V ICs?*

The three factors previously mentioned, small feature size, high resistivity substrates and the higher ionization per unit length turned the III-V FETs and HBTs into efficient detectors. This was not recognized at first. The first SEU results in MESFET and JFET SRAMs did not provide the required soft error rates for space systems.[16] When poor results were observed it was not normally published.[33] By the late 1980's some GaAs IC manufacturers had to provide SEE solutions to continue to attract DoD support. The initial approaches to SEU hardening GaAs ICs examined circuit techniques that were similarly used in Si memories.[34] Resistive and capacitive circuit approaches were attempted on CJFET SRAMs;[22] others utilized redundancy,[35] while other investigated superlattices to isolate the substrate.[36]

To understand the SEE sensitivity we need to look at electron and hole carrier generation in the semiconductor, the carrier transport and how charge collected at the contacts influence the circuit. Photocurrent generation in a semiconductor is related to two parameters, creation energy for an electron-hole pair and the density of the material. The creation energy is proportional to the band-gap of the semiconductor as shown by Klein.[37] The band structure of the semiconductor requires conservation of momentum and energy to absorb the kinetic energy of the incident particles, thus the energy to move a valance electron to the conduction band requires higher energy to conserve energy and momentum with the band structure. The density of the material determines how much matter is available for interaction in a particular volume. Therefore the amount of free carriers released is calculated from,

$$LET\ (ehp/um) = LET\ \frac{(MeV * cm^2)}{mg} \times \varepsilon_i(\frac{ehp}{eV}) \times density\ (\frac{gm}{cm^3}) \tag{1}$$

where LET is the linear energy transfer of a particular incident ion and ε_i is the creation energy for an electron-hole pair. LETs for heavy ions in space range between 1 to 100 MeV/mg/cm^2. Table 2 includes a summary of electron-hole pair ionization and band gap for various compound semiconductors and Table 3 provides the charge ionized per unit length in the semiconductor.[38]

Table 2 - Electron-hole pair ionization energies for various semiconductors.

Semiconductor	E_g (eV)	ε_i (eV)
Ge	0.66	2.60
$In_{0.47}Ga_{0.53}As$	0.75	2.85
$Si_{0.9}Ge_{0.1}$	1.03	3.63
Si	1.12	3.64
InP	1.35	4.53
GaAs	1.43	4.75
$Al_{0.7}Ga_{0.3}As$	2.06	6.52
AlAs	2.17	6.83
SiC	2.86	8.76
GaN	3.4	10.3
AlN	6.1	17.8

Table 3 gives a direct comparison of various semiconductors for the ionization induced by an ion with a LET of 1 MeV/mg/cm^2. The fourth column provides the ionized charge (fC) in the conduction band per micron of material in the penetrating ion's path. Comparing GaAs to Si, if an ion penetrated two equivalent volumes of Si and GaAs, the GaAs material would have 70% more free carriers produced. As can be seen in this table, compound semiconductors with heavy masses such as the In-based materials provide even higher free carrier densities, and in contrast low Z compound semiconductors such as GaN and SiC are expected to produce lower amounts of carrier ionization. Back in the 1980's the incorrect assumption was that the higher band gap of GaAs (compared to Si) alone would provide the radiation hardness, the density was not addressed.

The other two issues for SEE susceptibility were the new feature sizes associated with the new circuit designs and the high resistivity substrates. Due to the nature of the JFET and MESFET logic gates, the power supplies were below 2 volts; the lower gate capacitances and the small area gates provided fairly low power-speed switching energies, a very beneficial aspect for high performance integrated circuits. The reduced switching energy increased SEE susceptibility. In some MESFET SRAM designs with impedance loads the circuit only required 5 fC of charge to induce a bit flip.[39] Figure 1 is a compilation of previous reported data[16] and the author's notes estimating geosynchronous orbit heavy ion soft error rates using the Peterson heavy ion equation. The progression of each technology generation is to move left on the plot to lower energy products. Hardening with substrate techniques reduces soft error rates. This is observed

with both III-V approaches with low temperature grown (LTG) buffers or with insulating buried oxides (CMOS/SOI). Particular with III-V FETs, devices with improved gate isolation (i.e. HFETs) provide lower soft error rates and lower power speed products.

Table 3 - Charge per unit length of LET = 1 MeV/mg/cm^2 in various semiconductors.

Target Semiconductor	eV / eh-pair	Density (gm/cm^3)	fC/um for an LET=1 MeV/mg/cm^2	Divide LET by X for pC/um collected
Si	3.6	2.32	10.4	97
GaAs	4.8	5.32	17.8	56
InP	4.5	4.81	17.1	58
$In_{0.47}Ga_{0.53}As$	2.9	5.49	30.3	33
SiC	8.7	3.21	5.9	169
GaN	10.3	6.11	9.5	105

The additional issue was the high resistivity semi-insulating substrate. The semi-insulating substrate is ideal for isolation between transistors, and also eliminated additional steps for isolation. When carriers are ionized the region in the substrate acts

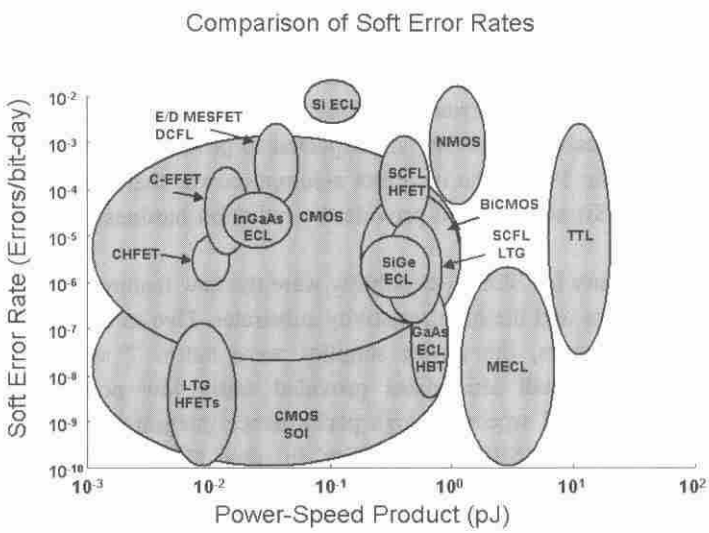

Fig. 1 - Geosynchronous orbit soft error comparisons for various IC technologies.

like a depleted intrinsic detector due to the undoped or low-doped substrate. Carriers ionized in the depleted substrate and/or within a diffusion length of critical depletion regions accumulate carriers due to an electric field in the device. In CMOS/SOS or CMOS/SOI technologies that showed excellent SEU immunity, the sapphire or buried oxide region prevented ionized carriers in the substrate to reach the drain/body junctions in CMOS devices.[40] In GaAs no wide band-gap or insulator barrier existed, and the high mobility of the GaAs substrate with the nanosecond carrier lifetime in undoped material provided diffusion lengths on the order of 5 to 10 microns. CMOS technologies on p-doped silicon epitaxy provided more recombination than undoped silicon to carriers migrating from the Si substrate.

Also attributable to the semi-insulating substrate is the floating body for FETs. Most of the GaAs ICs utilized FET structures that were susceptible to backchannel and/or bipolar effects.[25] A similar phenomenon is present in partially depleted SOI transistors today. Holes collected in the floating body of a CMOS/SOI n-MOSFET back gate the transistor adding source electrons to the initial carrier generation.[41] The difference in the GaAs substrate was that the EL2 defect and the floating body were present. Various experiments and device simulation studies examined backgating and bipolar mechanisms that contributed to the SEE susceptibility.[24,25] The non-insulated gate of GaAs FETs also contributed by providing holes to be collected on the gate terminal directly turning on the FET.[40]

3.3. *How can GaAs ICs be made immune to SEE?*

The use of buried oxides in III-Vs was not available in the 1990's to mimic the CMOS/SOI approach to harden SEE. The only insulator available to utilize was superlattices.[37] The superlattice approach was in the right direction; to limit carriers reaching the channel from the substrate but the band structure of the superlattice trapped carriers that assisted in backgating.[23] Additionally DX centers were present in AlGaAs-GaAs superlattices that contributed to trapping carriers. Other than using a potential barrier to block free carriers in the substrate, the only other approach was to kill the lifetime in the substrate. Proton and neutron irradiation had been observed to reduce upset cross sections of GaAs ICs.[27,42] In 1995 the use of defect rich non-stoichiometric low-temperature grown GaAs buffer layers to reduce lifetime was proposed.[43]. Earlier work had shown that the LTG GaAs buffers eliminated backgating in MESFETs.[44] Implementation in several GaAs processes demonstrated excellent SEU immunity in GaAs memories.[27,28,45] In 1995 digital GaAs ICs hardened to the complete coverage of radiation effects were available. Even though the radiation technical issues were solved no demand existed for rad-hard GaAs ICs. The communications market absorbed the digital GaAs IC foundries for consumer wireless and internet communications. Additionally other technologies were replacing the GaAs FET in digital applications, SiGe and CMOS devices were just under the performance curve of GaAs FETs, and InP-based Heterojunction Bipolar Transistor (HBT) technologies were above the curve. High-

speed ECL Si ASICs were known to be SEE sensitive in static tests.[16] SEE studies of III-V ECL HBT technologies at high clock rates were a new issue to be studied for Bit Error Rates (BER) in SEE environments.[27]

The soft errors observed in dynamic switching circuits is referred as Single Event Transient (SET) where the induced photocurrent produce transient signals in the logic producing errors in the bit stream. Various III-V circuits have been investigated for SET in fiber optic link applications under heavy ion tests.[46]

Heavy ion broad beam experiments (as opposed to micro beam experiments) could not easily provide information on which nodes or devices in a VLSI circuit were susceptible. New tools became available in the radiation effects community to investigate individual transistors in a complex circuit. Micro-beam ion beams and lasers were used to locate susceptible devices. Further the laser pulses used to generate carriers in micron-sized locations could be synchronized with the circuit clock to study soft errors in relation to clock phase. Work has progressed to utilize photoconductive sampling probes to measure the SEE induced voltage transients at individual transistors in a design.[47] These experimental tools provided data to provide verification of circuit and device simulations.

3.4. *What was learnt from dynamic testing and analysis?*

Susceptibility for soft errors in clocked III-V ICs was first recognized when incorporating redundancy techniques by performing majority voting.[17] In slower Si-based circuits redundancy was used often, either at the system, or circuit level. However at high speeds, voting becomes a significant portion of the clock period. A compromise between two rates, the scrub rate, i.e. the rate to write the majority vote result back into three locations, and the rate that the probability that 2 of 3 data registers can accumulate soft errors. The overhead of increase voting logic adds to the number of transistors susceptible to SEE. Further knowledge of the photocurrent persistence is important to determine the scrub rate.

To study soft errors in high-speed logic a circuit is tested in a broad beam ion experiment and a bit-error rate is calculated for particular ion fluence.[48] Running the experiment at various clock frequencies give different susceptibilities due to various race conditions in the integrated circuit.[49] Micron-focused laser beams can be used to determine the most susceptible devices; the laser pulse can also be synchronized with the IC's clock to determine which phase of the clock is most susceptible. Photoconductive sampling probes have been used to provide in-situ measurements of voltage transients internal to the IC. Such an approach was used on GaAs MESFET and InP-based HBT technologies.[47] A surprising result to system designers of HBT ECL circuits was the ability at GHz clock frequencies to lose several clock cycles to an SEE, preventing accurate error correction to be applied to streaming data.[50] System or circuit designs to mitigate such long streams of errors require data link resets. The source of the InP-based SEE susceptibility was charge collection from the semi-insulating substrate similar to

early GaAs FET issues. A solution was proposed to using lifetime killing buffer layers to eliminate the SEE susceptibility.[51]

3.5. *What does the future hold for III-V ICs for radiation effects?*

The radiation effects of space and weapons environments will continually require radiation-hardened microelectronics. However the flood of microelectronics into every know application and in such large quantities of low power-speed product transistors overlap many radiation sources in our terrestrial surroundings, alphas from solder or packaging, Borophosphosilicate glass (BPSG),[52] cosmic radiation at sea level, and byproducts of neutrons at avionic altitudes. Baumann provide a good review of these terrestrial issues.[53] The neutron environment at aircraft cruising altitudes has required fly-by-wire control electronics to be SEE hardened.

The introduction of low density III-V compounds such as GaN and SiC-based ICs should be promising to ionizing radiation applications. The capability to engineer the substrate by bandgap, introduce insulators (Gallium-on-Insulator)[54] or utilize non-stoichiometric materials to control soft error susceptibility will further provide additional solutions for III-V ICs in soft error applications.[55] The recent capability to manufacture GaAs on Si may not only provide a more competitive product to Si-based ICs, but may allow non-stoichiometric techniques to provide radiation hardness for space or terrestrial needs. The future looks promising with increasing capabilities to engineer III-V materials and devices to improve radiation hardening of ICs for future applications.

References

1. M. Simons, "Radiation effects in GaAs integrated circuits: A comparison with silicon", *IEEE GaAs IC Symp*, (1983) pp.124-128.
2. D. Binder, E.C. Smith and A.B. Holman, "Satellite anomalies from galactic cosmic rays", *IEEE Trans. on Nucl. Sci.* **NS-22, 6**, (1975) pp. 2675-2680.
3. T.C. May and M.H. Woods, "Alpha-particle-induced soft errors in dynamic memories," *Proceedings of the 1978 IEEE International Reliability Physics Symposium*, (1978).
4. J.T. Wallmark, and S.M.Marcus, "Minimum size and maximum packing density of non-redundent semiconductor devices", *Proc.of the IRE*, **50, 3,** (1962) pp. 286-298.
5. E. Normand, "Single-event effects in avionics", *IEEE Trans. on Nucl. Sci.*,**43, 2**, (1996) pg. 461-474.
6. M.W. Roberson, "Soft error rates in solder bumped packaging", *Proceedings on the 4th International Symposium on Advanced Packaging Materials*, 15-18 March 1998, Braselton, GA, USA.
7. P. Shapiro, A.B. Campbell, J.C. Ritter, R. Zuleeg, and J.K. Notthoff, *1983 IEEE Natural Space Radiation Effects Conference*, Gatlinburg, TN, July 1983.
8. B.A. Kulp et al, "Electron radiation damage in unipolar transistor devices", *Proc. IRE*, 49, (1961) pp.1437-1438.
9. J.L. McNichols and W.S. Ginell, "Predicted effects of neutron irradiation on GaAs junction field effect transistors", *IEEE Trans. on Nucl. Sci.* **NS-17**, (1970) pp. 52-54.

10. J.M. Borrego et al., "Radiation effects on GaAs MESFETs", *IEEE Trans. on Nucl. Sci.* **NS-25** (1978), pp 1436-1443.
11. M. Simons et al, "Transient radiation study of GaAs MESFETs implanted in Cr-doped and undoped substrates", *J. Appl. Phys.*, **52**, (1981), pp.6630-6638.
12. R. Zuleeg and J.K. Notthoff, "Transient response of GaAs ICs to ionizing radiation", *IEEE Trans. on Nucl. Sci.*, **NS-26**, (1979) pp. 4744-4749.
13. J.J.Wiczer, L.R. Dawson and C.E. Barnes, "Transient effects of ionizing radiation in photodiodes", *IEEE Trans. on Nucl. Sci.* **NS-28**, (1981), pp.4397-4402.
14. R. Zuleeg et al, "Latch-up in GaAs ICs during ionizing radiation exposure", *1982 GaAs IC Symposium Digest* (1982), pp.123-126.
15. R. Zuleeg, J.K. Notthoff and D.K. Nichols, "SEU of Complementary GaAs static RAMs due to heavy ions", *IEEE Trans. on Nucl. Sci.* **NS-30**, (1984), pp. 4533-4539.
16. T.R. Weatherford, A.B.Campbell, D. McMorrow, J.B.Langworthy, W.J. Stapor, A.R.Knudson, E.L.Petersen, D. Wilson, and L. Tran, "Can Digital GaAs Be Used in a Space Environment?: A Look at Single Event Upset in GaAs"", *IEEE 1991 GaAs IC Symposium, Technical Digest,* Monterey, California, October 20-23, 1991.
17. R. Schneiderwind, D. Krening, S. Buchner,K. Kang, T.R. Weatherford, "Laser confirmation of SEU experiments in GaAs MESFET combinational logic for space applications", IEEE Trans. on Nucl. Sci. , **NS-39** (1992), pp. 1665 –1670.
18. R.J. Chaffin, "Microwave Semiconductor Fundamentals and Radiation Effects, John Wiley and Sons, New York (1973).
19. R. Zuleeg, "Radiation Effects in GaAs ICs", Chapter 8, VLSI electronics: microstructure science / edited by Norman G. Einspruch, 1985.
20. J.R.Srour and J.M. McGarrity, "Radiation Effects on Microelectronics in Space", *Proceedings of the IEEE* , **76-11**, (1988), pp. 1443-1469.
21. R. Zuleeg, "Radiation effects in GaAs FET devices", *Proceedings of the IEEE*, **77-3**, (1989), pp. 389 –407.
22. R. Zuleeg, J.K. Notthoff, "SEU Hardening of GaAs E-JFET SRAMs", *Journal of Radiation Effects, Research and Engineering*, 6-2, (1988), pp. 136.
23. T.R. Weatherford, D. McMorrow, W.R. Curtice, A.R. Knudson and A.B. Campbell, "Single event induced charge transport modeling in GaAs MESFETs", *IEEE Trans. on Nuclear Science*, **NS-40**, (1993), pp. 1867-1871.
24. D. McMorrow, A.B. Campbell, A.R. Knudson, S. Buchner, T.R. Weatherford," Transient charge collection from ion tracks in semiconductors", *Nuclear Instruments and Methods in Physics Research Section B*, **67** n 1-4 (1992), pp 384.
25. B.W. Hughlock, G.S. LaRue, A.H. Johnston, "Single-event upset in GaAs E/D MESFET logic", *IEEE Trans. on Nucl. Sci.*, **37-6**, (1990), pp. 1894-1901.
26. D. McMorrow, T.R. Weatherford, S. Buchner, A.R. Knudson, J.S. Melinger, L.H. Tran, and A.B. Campbell, "Single-event phenomena in GaAs devices and circuits", *IEEE Trans. on Nucl. Sci.*, **NS-43**, **2**, (1996), pp. 628 –644.
27. P.W. Marshall, C.J. Dale, T.R. Weatherford, M.Carts, D. McMorrow, A.Peczalski, S.Baier, J. Nohava and J. Skogen, " Heavy ion SEU immunity of a GaAs complementary HIGFET circuit fabricated on a low temperature grown buffer layer", *IEEE Trans. on Nuclear Science,* **NS-42**, (1995), pp. 1850-1855.
28. M. LaMacchia, J. Abrokwah, B.Bernhardt, D. Foster, B. Crawforth, B. Mathes, T. McGuire, and T. Weatherford, "Radiation hardened complementary GaAs (CGaAs^{TM})", *IEEE GaAs IC Symposium Technical Digest,* October 1997.
29. A. Meulenberg, H.-L.A. Hung, K.E. Peterson, W.T. Anderson, "Total dose and transient radiation effects on GaAs MMICs", IEEE Trans. on Elec. Dev., **35-12**, (1988) , pp. 2125-2132.
30. R. Zuleeg, K. Lehovec and J.K. Notthoff, "Effects of total dose ionizing radiation on GaAs JFETs and ICs", *IEEE GaAs IC Symposium Digest*, (1981) pp. 14.

31. J.M. Borrego et al., "Radiation Effects on signal and noise characteristics of GaAs MESFET microwave amplifiers", *IEEE Trans. on Nucl. Sci.* **NS-26** (1979), pp 5092-5099.
32. M. Citterio, S. Rescia, and V. Radeka, "Radiation effects at cryogenic temperatures in Si-JFET, GaAs MESFET, and MOSFET devices", *IEEE Tran. On Nucl Sci.* **NS-42**, (1995) pp. 2266-2270.
33. T.R. Weatherford, "Single event upset in GaAs integrated circuits", PhD thesis, North Carolina State University, 1993.
34. J.L.Andrews, J.E. Schroeder, B.L. Gingerich, W.A. Kolasinski, R. Koga and S.E. Diehl, "Single event error immune CMOS SRAM", *IEEE Trans. on Nucl. Sci.* **NS-29** (1982), pp. 2040-2043.
35. J.R. Hauser, "SEU-hardened silicon bipolar and GaAs MESFET SRAM cells using local redundancy techniques", *IEEE Trans. on Nucl. Sci.* **NS-39**, (1992) , pp. 2-6.
36. R.L. Remke et al, "SEU measurements on HFETs and HFET SRAMs", *IEEE Trans. on Nucl. Sci.* **NS-36**, (1989) pp.2362-2366.
37. C.A.Klein, "Bandgap dependance and related features of radiation ionization energies in Semiconductors", *Journal of Applied Physics*, vol. 39, no. 4, pp. 2029-2038 , March 1968.
38. T.R. Weatherford, "From carriers to contacts, A review of SEE charge collection processes", *IEEE 2002 Natural Space Radiation Effect Conference Short Course notes*, July 2002.
39. T.R. Weatherford, J.R. Hauser, and S.E. Diehl, "Comparisons of single event vulnerability of GaAs SRAMs", *IEEE Trans. on Nucl. Sci.*, **NS-33**, (1986), pg. 1121-1127.
40. A.B. Campbell et al, "Charge collection studies in CMOS/SOS structures", *IEEE Trans. on Nucl. Sci.* **NS-32**, (1985) pp 4128-4132.
41. S.E. Kerns, L.W. Massengill, D.V. Kerns Jr., M.L. Alles, T.W. Houston, H. Lu and L.R. Hite, "Model for CMOS/SOI single-event vulnerability", *IEEE Trans. on Nucl.Sci.*, **NS-36**, (1989) pp. 2305-2310.
42. T.R. Weatherford, L. Tran, W.J. Stapor, E.L. Petersen, J.B. Langworthy, D. McMorrow, W.G. Abdel-Kader, and P.J. McNulty, "Proton and heavy ion upsets in GaAs MESFET devices", *IEEE Trans. on Nucl. Sci.*, **NS-38**, (1991), pp. 1450-1456.
43. T.R. Weatherford, D. McMorrow, W.R. Curtice and A.B. Campbell, "Significant reduction in the soft error susceptibility of GaAs field-effect transistors with a low-temperature grown GaAs buffer layer", *Applied Physics Letters , 67,5,* 31 July 1995, pg. 703-705.
44. F. W. Smith, A. R. Calawa, and C. L. Chen, "New MBE buffer used to eliminate backgating in GaAs MESFETs," *IEEE Elec. Dev. Let.*, **9-2**, (1988) pp. 77–80.
45. T.R. Weatherford, P.W. Marshall, C.J. Marshall, D.J. Fouts, B. Mathes and M. LaMacchia, "Effects of low-temperature buffer-layer thickness and growth temperature on the SEE sensitivity of GaAs HIGFET Circuits", *IEEE Trans. on Nucl. Sci.,* **NS-45,** (1997), pp. 2298-2305.
46. C.J. Marshall, P.W. Marshall, M.A. Carts, R. Reed, S.Baier, and K. Label , "Characterization of transient error cross sections in high speed commercial fiber optic data links", *IEEE 2001 Radiation Effects Data Workshop*, pg. 142-145.
47. G. David. T. Yun, M. Crites, J.F. Whitaker, T.R. Weatherford, K. Jobe, S. Meyer, M. Bustamante, W. Goyette, S. Thomas III, and K. Elliott, " Absolute potential measurements inside microwave digital ICs using a micromachined photconductive sampling probe", *IEEE Trans. on Microwave Theory and Techniques,* **46-12**, (1998), pp. 2330 –2337.
48. M. Shoga, K. Jobe, M. Glasgow, M. Bustamante, E. Smith and R. Koga, "Single event upset at gigahertz frequencies", *IEEE Trans. on Nucl. Sci.*, **NS-41**, (1994), pp. 2252 –2258.
49. R.A. Reed, M.A.Carts, P.W.Marshall, C.J. Marshall, S. Buchner, M. La Macchia, B. Mathes, D. McMorrow, "Single event upset cross sections at various data rates", *IEEE Trans. on Nucl. Sci.* **NS-43**, (1996), pp. 2862-2867.
50. T.R.Weatherford, J. Whitaker, K. Jobe, S. Meyer, M. Bustamante, S.Thomas III, and K. Elliott, "Single event induced voltage transients within InP HBT circuits", *Journal of Radiation Effects*, September 2001.

51. T.R.Weatherford and P.K. Schiefelbein, "SEE Analysis of digital InP-Based HBT circuits at gigahertz frequencies", *IEEE Trans. on Nucl. Sci.*, **NS-48**, (2001), pp. 1980-1986.
52. R.C. Baumann, T. Hossain, S. Murata, H. Kitagawa, "Boron compounds as a dominant source of alpha particles in semiconductor devices", *Proceedings of the 33rd Annual IEEE International Reliability Physics Symposium,* (1995), pp. 297-302.
53. R.C. Baumann, "Soft errors in advanced semiconductor devices-part I: the three radiation sources", *IEEE Transactions on Device and Materials Reliability*, **1-1**, (2001) pp. 17-22.
54. P. Parikh, P. Chavarkar, U. Mishra, " First demonstration of GaAs on insulator (GOI) technology", *54th Annual Device Research Conference Digest,* (1996), pp. 134 –135.
55. P.Specht, M.J.Cich, H. Sohn and E.R. Weber, "P-Conductive LT-GaAs: The alternative for device applications?" *2nd Symposium On Non-Stoichiometric III-V Compounds, Physik Mikrostrukturierter Halbleiter 23*, Friedrich-Alexander-Universitat 2000, pg. 7-12.