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Modeling Single-Event Effects in a Complex Digital Device

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***Abstract*—A methodology to quantify the impact of SEEs on complex digital devices has been developed. This methodology is based on the SEE State-Transition Model and was validated by radiation testing of a complex digital device.**

***Index Terms*—Fault modeling, fault propagation, radiation effects, single-event effects, single-event transients, single-event upsets, transient propagation.**

I. Introduction

THE prediction of the performance of an advanced digital device in a radiation environment can be a complex and difficult task. The long development times and high costs of systems for space applications make accurate component performance prediction exceedingly important. In an attempt to improve this process, the authors have undertaken to develop tools and techniques that will improve our ability to predict the performance of complex digital circuits in the presence of radiation. In particular, this paper describes a technique for modeling the impact of single-event effects (SEEs) to predict the tolerance of a device without exhaustive testing.

In a simple circuit (a single memory cell, for example), the probability of a single-event upset (SEU) occurring is the likelihood that an ionized particle, capable of transferring enough energy to cause an upset, strikes the sensitive region of the circuit. Predicting SEU performance is a matter of understanding the sensitivity of the process and predicting the particle flux. In a complex device, the performance is more difficult to predict. The SEE performance is a function of both the probability that an ionized particle strikes the sensitive region of the circuit and the probability that the resulting single event transient (SET) or SEU propagates in such a way that it causes an error to the external system. (Think of an upset in a register in the CPU of a microprocessor. If the processor overwrites the error before the register is read, the upset will not propagate. If, however, the particular program currently running in the processor reads the register, the SEU will propagate in the microprocessor and may cause an error to the external system.) This paper describes a methodology to quantify the likelihood that an SET or SEU occurs in a complex digital device and causes an error to the external system. This methodology is based on the SEE State-Transition Model [1]. Using this model, the SEE tolerance of a complex digital device was predicted. Laser and heavy-ion testing were then performed on the device to validate the model.

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II. Methodology Development

A. SEE State-Transition Model

The purpose of the SEE State-Transition Model is to represent the current fault condition of a complex device with one of five possible fault states. Fig. 1 is a diagram of the model. State S1 (No SETs or SEUs) is the normal or error-free state. From there, an ion strike will cause the system to transition to one of three states. If the strike occurs on a logic gate, with transitional probability $\beta 2$, the state becomes S2 [Logic Gate Transient(s)]. If the strike occurs on a memory cell and changes the contents of that cell, the next state becomes S3 (SEU). This occurs with transitional probability $\beta 1$. If the strike occurs on an output driver, with transitional probability $\beta 3$, the state becomes S4 (Output Driver Transient). From S2, the transient can be latched into a memory element (S3), occurring with transitional probability $\delta 1$. It can also propagate to an output driver (S4) with transitional probability $\delta 2$, or the SET may stop propagating without being latched or propagating to the output, and the state returns to S1, with transitional probability $\alpha 2$. From S3, the SEU may propagate to the output and cause an error to the external system (S5: Failure) with transitional probability $\varepsilon 1$, it may be overwritten (S1) with transitional probability $\alpha 1$, or it may stay in the memory element (S3). From S4, the SET may cause an error to the external system (S5) with transitional probability $\varepsilon 2$. If it does not cause an error, the state returns to S1, with transitional probability $\alpha 3$.

Estimation of the SEE tolerance involves calculating the transitional probabilities of the complex digital device. The predicted overall tolerance of the device is then determined by combining the transitional probabilities to account for all the possible paths from S1 to S5. Table I shows the modeling that is required to determine the transitional probabilities. The transitional probabilities are grouped as follows: βn are SEE generation probabilities, the αn transitional probabilities return the

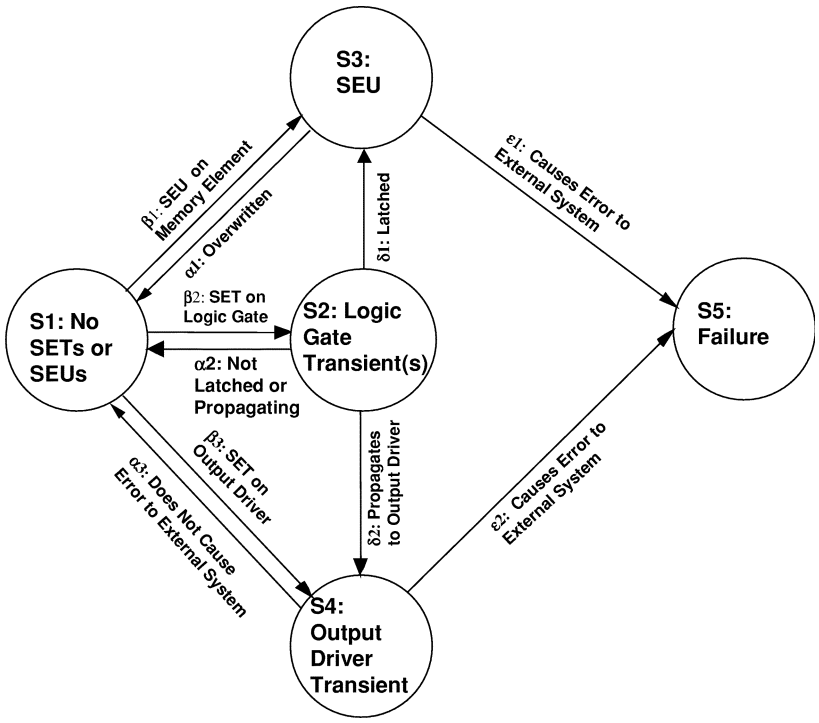

Fig. 1. SEE State-Transition diagram.

TABLE I
MODELING AREAS

Transitional Probabilities	Modeling Areas
$\beta 1$, $\beta 2$, $\beta 3$	SET/SEU Generation
$\delta 1$, $\alpha 1$	SET Analog Propagation, SET Logic Propagation, SET Clock-Edge Effects
$\delta 2$	SET Analog Propagation, SET Logic Propagation
$\varepsilon 1$	SEU Propagation
$\varepsilon 2$, $\alpha 2$, $\alpha 3$	SET Analog Propagation, SET Clock-Edge Effects

state back to S1, δn are SET propagation probabilities, and εn are transitional probabilities to the failure state, S5.

B. SEE Generation Modeling

The objective of SEE generation modeling is to determine how the radiation environment affects the electrical characteristics of the device. For $\beta 1$ (SEU generation on memory element), it is necessary to determine the probability of an incident ion depositing enough energy to cause the contents of the memory element to change. For the SET generation transitional probabilities, $\beta 2$ and $\beta 3$, it is necessary to determine the probability that an incident ion will result in an SET pulse with amplitude equal to a and pulsewidth equal to pw.

Each of these transitional probabilities has probabilistic and deterministic components. The probability that an ion will strike the sensitive volume of a transistor is a function of both energy spectrum of the environment and the effective cross-section of this volume. The energy spectrum is the probabilistic component and is orbit-specific. It is often specified in terms of particle fluence as a function of linear energy transfer (LET). The deterministic components of the transitional probabilities are the effective cross-section of the device and the resulting electrical response of the device to the ion strike. The SEE generation modeling provides an estimate of these deterministic components.

The effective cross-section of a MOSFET in the device is modeled using the following [2]:

$$\begin{aligned}\text{cross}-\text{section length} &: l = l_d + 2W \\ \text{cross}-\text{section width} &: w = w_d + 2W \\ \text{cross}-\text{section} &: \sigma = lw\end{aligned}$$

where l_d and w_d are the physical length and width of the drain of the MOSFET, respectively, and the depletion width, W, is given by [3]

$$W = \left[\left(\frac{2\varepsilon(V_0 - V)}{q}\right)\frac{(N_a + N_d)}{N_a N_d}\right]^{1/2}$$

where ε is the permittivity of silicon, V_0 is the contact potential, V is the applied potential, q is the charge of an electron, N_a is the acceptor concentration, N_d is the donor concentration.

To model the electrical result of the ion strike, a charge injection circuit is used in SPICE. The charge injection circuit simulates the charge collection described in the following [4], [5]:

$$I(t) = \left[\frac{q\mu N(V_{\text{node}} - V_{\text{sub}})}{L_f}\right][e^{-at} - e^{-bt}]$$

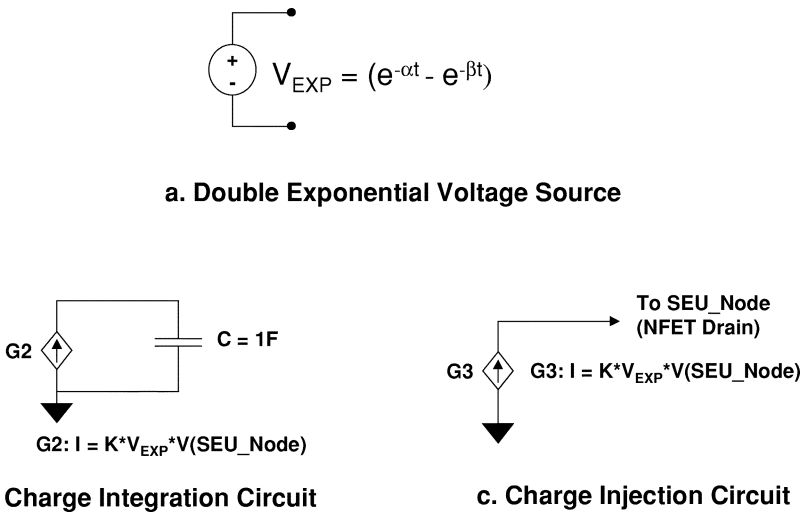

Fig. 2. SET injection circuit.

where μ is the average mobility of the carriers in Si, N is the number of electron-hole pairs generated per unit length, $V_{\rm node}$ is voltage of injection node, $V_{\rm sub}$ is the substrate voltage, L_f is the funnel length, $1/\alpha$ is the collection time constant for the junction, and $1/\beta$ is the time constant for initially establishing the ion track.

Fig. 2 shows the SPICE circuit used to implement charge injection onto the drain of an NFET. The independent voltage source in Fig. 2(a) provides the double-exponential term describing the carrier densities for the voltage-dependent current source, G3. This voltage-dependent current source, shown in Fig. 2(c), is set equal to the product of a constant K, the double-exponential pulse from Fig. 2(a), and the SEU_Node voltage ($V_{\rm sub} = 0$ for an NFET injection). K is constant for a single simulation run. It represents the product of $q\mu N/L_f$. Ions with different LETs are injected from one run to the next by changing K.

After the injection circuit described above has been used to simulate the SET, the charge collected on the 1 F capacitor (shown in Fig. 2(b)) must be converted to LET in units of $\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$. This is accomplished by dividing the total charge collected by the product of the funnel length, L_f, and $10.35\ \mathrm{fC}/\mu\mathrm{m}$ (which is equivalent to $1\ \mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$ in Si [6]).

C. SET Analog Propagation Modeling

The purpose of analog propagation modeling is to determine what happens to the amplitude and pulsewidth of an SET as it propagates through a sensitized combinational logic path. A sensitized combinational logic path is defined as a path in which the propagation of the SET is not blocked by the other inputs to the logic in the path. For example, if an SET has propagated to input A of a 2-input AND gate, and input B is a logic "1," the logic path is sensitized. If input "B" had been a logic "0," the SET could not have passed through regardless of its amplitude and pulsewidth because the logic path was blocked (input B forces the output to logic "0").

To model analog propagation, an SET is injected into a cascade of logic gates in a SPICE simulation. The pulsewidth and amplitude are recorded as it propagates. From these values, a gate attenuation factor is determined in terms of pulsewidth and amplitude. This is similar to determining the transfer function of each gate as described in [7]. If the pulsewidth and amplitude are large enough, the attenuation will be negligible [8]. The minimum pulsewidth and amplitude that will propagate through a logic gate without attenuation is the propagation threshold [1], [9]. This threshold is determined for each logic gate. If the amplitude and pulsewidth of the SET is at or above the propagation threshold for the logic gate, the attenuation factor is set to 1 (i.e., no attenuation).

D. SET Logic Propagation Modeling

The objective of SET logic propagation modeling is to determine the probability that a sensitized combinational logic path, or "critical pipe" [10], [11], exists from the point of the SET generation to the input of the memory element. This probability is denoted as $\mathrm{P}_{\rm scl}$.

The approach used to model this probability is a simplified version of the approach described in [12]. Logic is divided into two types: control logic and datapath logic. Control logic refers to logic that steers the flow of data through the possible datapaths. An example of control logic is a multiplexer that steers the flow of data from the output of the register file to the input of the arithmetic logic unit (ALU). Datapath logic is used in computations, but does not steer the flow of the data. An example is an OR gate used to create a fast adder in the ALU.

For control logic, the probability of logic propagation is assigned based on the how the datapath is steered. This is based on the functional mode of the system. For datapath logic, a random input is assumed. For example, for a 4-input AND gate, the probability that a transient will propagate through input "A" is 1/8. This is the likelihood that the other three inputs (B, C, and D) are equal to a logic "1."

E. SET Clock Edge Effects Modeling

The objective of SET clock-edge effects modeling is to determine the probability that a transient pulse with $\mathrm{amplitude} = a$ and $\mathrm{pulsewidth} = pw$ will be latched into the memory element, or $\mathrm{P}_{\rm latch}(a, pw)$. The modeling focuses on determining

the temporal relationship between the transient's arrival at the memory element and the edge of the control signal that latches it. This involves determining the window of vulnerability, or latching window described in [13], [14]. In previous approaches, determination of this temporal relationship is accomplished using a statistical model of the sample and hold characteristics of the memory element [15], [16], or by modeling transient pulse as a logic pulse in the digital domain [17]. By using SPICE, the modeling approach described stays in the analog domain and accounts for the effect of the amplitude and shape of the transient pulse. The transient is injected one logic cell away from the input of the memory element at various times. Varying the amount of charge deposited controls the amplitude and pulsewidth of the transient. This approach maintains the appropriate transient pulse shape going into the memory element.

The first step of clock edge effects modeling is to determine the latching window. For a specific pulsewidth and amplitude of the transient pulse, this is accomplished by varying the arrival time of the SET to determine the maximum-setup time, $t_{su-\max}$, and the minimum-setup time, $t_{su-\min}$, for this particular pulse. The maximum setup time for a given amplitude and pulsewidth SET is the maximum time the SET can arrive prior to the active edge of the clock signal and still be successfully latched. Similarly, the minimum setup time for a given amplitude and pulsewidth SET is the minimum time the SET can arrive prior to the active edge of the clock signal and still be successfully latched. The latching window is then determined using the following [1]:

$$t_{lw}(a, pw) = t_{su-\max} - t_{su-\min}.$$

The second step is to account for the clock frequency. Because the SET can only be latched once per clock cycle, the probability that the SET is latched is given by [1]

$$P_{\text{latch}}(a, pw) = \frac{t_{lw}(a, pw)}{(\text{clock period})}.$$

F. SEU Propagation Modeling

The purpose of SEU propagation modeling is to determine the probability that an SEU will propagate to the output and cause an output error. This addresses the $\varepsilon 1$ transitional probability on the SET State-Transition Model. This transitional probability is very dependent on the functional mode of the digital device. A key aspect of SEU propagation modeling is the ability to express $\varepsilon 1$ as a mode-conditional probability. There have been two primary approaches to SEU Propagation Modeling. The first approach focuses on breaking the device into functional blocks (e.g., register file, ALU), and determining the cross-sections and duty cycles of these blocks through testing and analysis. The duty cycle and cross-sections are then multiplied to determine the overall device cross-section [18]–[20]. The second approach focuses on simulations using hardware-description languages, such as VHDL. A fault is injected in a hardware description of the device. The effect of this fault on the device operation is determined during the simulation [15], [16], [21]–[23].

The SEU propagation modeling combines aspects of both approaches above. It uses a combination of register-usage analysis (similar to the duty cycle approach) and VHDL simulation. Register-usage analysis is used to reduce the complex digital device to a reasonable number of functional modes. For each possible mode, the registers that are necessary for proper execution within that mode are determined. These registers form the mode-dependent cross-section. For a processor, the complexity reduction is accomplished by considering each assembly language instruction as a unique mode. These instructions specify which registers within the functional blocks of the processor are being used. These instructions can be further broken down into the pipeline stages. For each pipeline stage of each instruction, the number of registers that must not be in error for proper instruction execution is determined. If a register is used, the number of clock cycles since it was last written is recorded. This provides a conditional probability of SEU propagation for each pipeline stage of each instruction.

In some cases, it is not apparent which bits of a register in a functional block add to the mode-dependent cross-section. In this case, fault injection in a VHDL simulation is used to provide additional insight. This is accomplished by injecting an error into each possible bit in the functional block and recording the resulting output errors. These results are then included in the higher level register-usage analysis.

III. Methodology Verification

To verify this methodology, the SEE tolerance of a candidate complex digital device was determined. This device was the KDLX microprocessor, a 16-bit version of the processor described in [24]. It was fabricated through the MOSIS prototyping service, using the Agilent (formerly Hewlett-Packard) 0.5 μm CMOS process and the Tanner Tools Pro SCMOS Standard Cell Library. By using he MOSIS fabrication service together with the Tanner Tools Pro Library, the following data on the design are available: parametric test results from the foundry run, a SPICE transistor-level description of the entire design, and a VHDL description of the processor.

A. SEE Generation Modeling Results

The purpose of the SEE generation modeling is to calculate the deterministic components of the transitional probabilities $\beta 1$, $\beta 2$, and $\beta 3$ (cross-section and electrical response). The cross-section component for each of these transitional probabilities is estimated using the equations described in Section II-B.

For $\beta 1$ (SEU on memory element), the only memory element in the KDLX design is the D-Flip-Flop-with-asynchronous-clear (DFFC) standard cell. Modeling the electric response component for $\beta 1$ requires four input cases to be simulated: $\text{Clk} = 0$, $\text{Data} = 0$; $\text{Clk} = 0$, $\text{Data} = 1$; $\text{Clk} = 1$, $\text{Data} = 0$; $\text{Clk} = 1$, $\text{Data} = 1$. The ClB (active low asynchronous clear) input is set to logic "1" to simulate normal operation. For each input case, the sensitive transistors are determined. For each sensitive transistor, several transients are injected using the injection circuit. The amount of charge deposited from the transients is varied until the minimum charge necessary to cause an SEU has been determined. This minimum

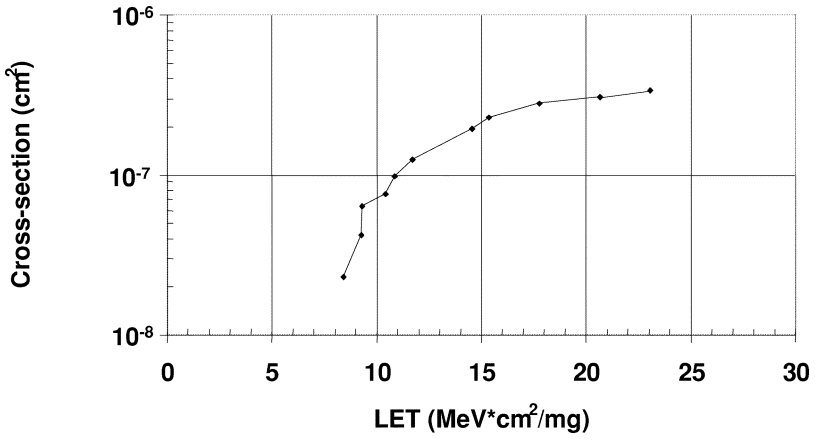

Fig. 3. D-flip-flop cross-section versus LET.

charge is converted to an LET value using an $L_f = 3.9\ \mu\mathrm{m}$. This value was derived from the simulation results in [25], for the simulation case with similar doping levels as the KDLX. Fig. 3 shows the cross-section versus LET curve for a single DFFC standard cell.

To determine the electrical response component of $\beta 2$ (SET on a logic gate), the injection circuit is used to inject an SET into the sensitive regions of each of the standard logic cells. The charge injected is converted to LET, and the output pulsewidth and amplitude are recorded. Fig. 4 shows this resulting voltage for various LETs for the injected pulse. This figure shows that an LET of approximately 13.89 $\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$ is necessary for the SET to make the full voltage swing. As the LET is increased beyond 13.89 $\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$, the pulsewidth of the SET increases.

To determine the electrical response component of $\beta 3$ (SET on output driver), the simulation is similar to modeling the inverter for $\beta 2$, except the output driver is connected to an output pad plus an 8 pF capacitor. The 8 pF capacitor is the input capacitance of a Xilinx XCV300 field programmable gate array (FPGA) [26], which is the device connected to the KDLX in the test system. The results of this modeling indicate that an ion incident upon the PFET requires an LET greater than 347 $\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$ to result in a transient with an amplitude greater than 1.13 V. Similarly, an ion incident upon the NFET requires an LET greater 343 $\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$ to cause a transient with an amplitude greater than 1.27 V. The largest linear energy transfer in silicon from a heavy ion is $\sim 120\,\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$ [27]. Since $343 \gg 120$, $\beta 3$ can be set to 0, and the output drivers of the KDLX are modeled as not susceptible to SETs.

B. SET Analog Propagation Modeling Results

SET analog propagation modeling is necessary to determine if an SET has enough energy to propagate to the input and be latched into a memory element. Fig. 5(a) shows a transient is attenuated significantly as it passes through each inverter: the amplitude is less than 100 mV after it has propagated through four inverters. Fig. 5(b) shows the propagation of a transient that is larger in amplitude and pulsewidth, but is not large enough to propagate without attenuation. In contrast, Fig. 5(c) shows the propagation of a transient that does not attenuate at all as it propagates. The propagation threshold occurs at a point between the size of the transients in Fig. 5(b) and (c).

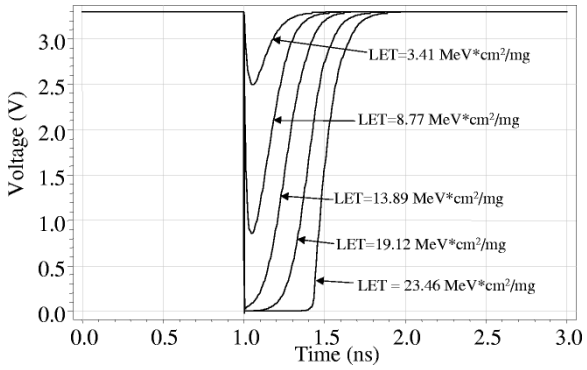

Fig. 4. SET pulse shape versus LET.

To determine this threshold, the simulation is run with multiple SETs injected into the circuit. The amplitude and pulsewidth are measured at each node. Table II shows the results of these simulations. The propagation threshold for a 0–1-0 SET pulse is approximately an amplitude of 3 V and a pulsewidth of 400 picoseconds. The propagation threshold for at 1–0-1 SET pulse is an amplitude of 3.3 V and a pulsewidth of 460 picoseconds.

C. SET Logic Propagation Modeling Results

SET logic propagation modeling determines the probability that an SET will propagate through the logic gate, given that the amplitude and pulsewidth are large enough for analog propagation. Table III shows the probability of logic propagation for each of the standard-cell logic gates used in the KDLX design. For multiple-input logic gates that are not instruction-dependent, the inputs are modeled as random. For the Mux2, the probability is modeled as being instruction-dependent. This is because the Mux2 is used throughout the KDLX to direct the data path as a function of the instruction, whereas the other multiple logic gates have inputs that are not direct functions of the instruction. This is critical because it causes $\delta 1$ to be instruction-dependent (if there is a Mux2 in the datapath). Additionally, the gates that are used in the decoding logic of the pipeline are modeled as instruction-dependent.

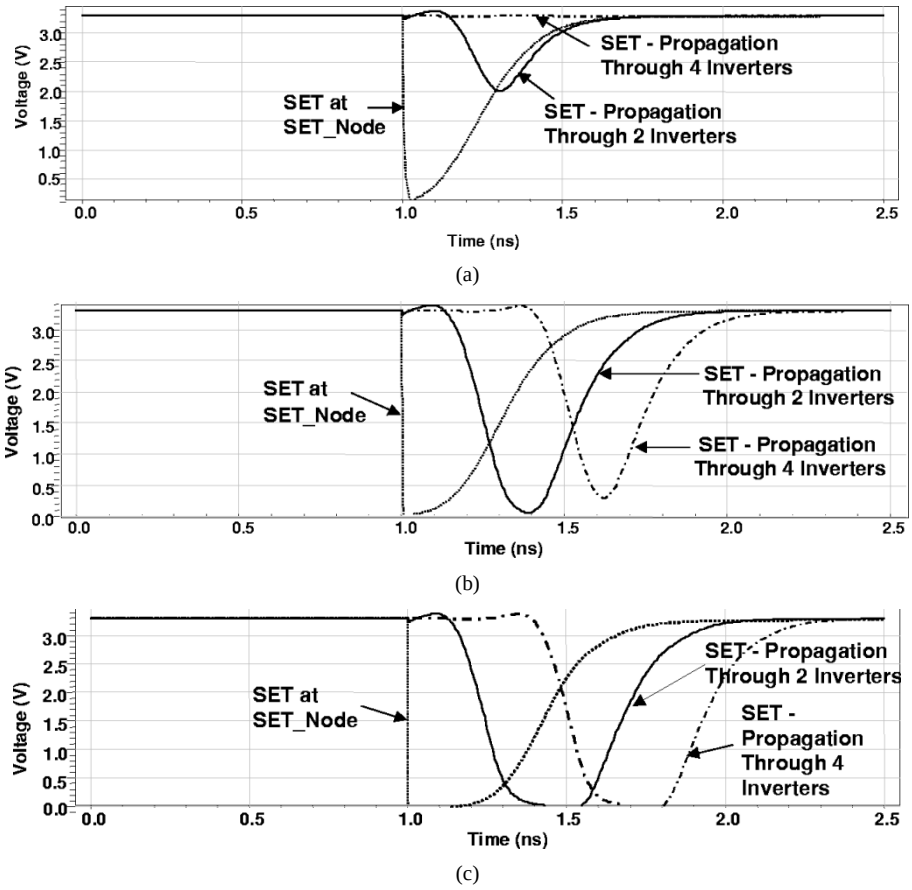

Fig. 5. (a) Transient propagation with significant attenuation. (b) Transient propagation below propagation threshold. (c) Transient propagation above propagation threshold.

TABLE II
ANALOG PROPAGATION MODELING RESULTS

SET Injection Node		1 Inverter Propagation		2 Inverter Propagation		3 Inverter Propagation		4 Inverter Propagation	
Amp (V)	PW (ps)	Amp (V)	PW (ps)	Amp (V)	PW (ps)	Amp (V)	PW (ps)	Amp (V)	PW (ps)
-2.9	240	1.36	200	NA	NA	NA	NA	NA	NA
-3.25	290	2.2	260	-2.58	250	1	140	-.08	180
-3.27	300	2.45	280	-3.11	280	2.16	210	-2.05	220
-3.28	330	2.6	300	-3.26	310	2.59	250	-3.18	270
-3.3	400	2.96	380	-3.3	400	3.06	340	-3.3	390
-3.3	450	3.15	410	-3.3	460	3.22	400	-3.3	460

Amp = Amplitude in Volts (V), PW = pulsewidth in picoseconds (ps)

D. Clock-Edge Effects Modeling Results

Clock-edge effects modeling determines the probability that an SET will be latched into a memory element (P_{latch}). It is a function of the latching window and the clock period. Table IV shows the latching window as a function of the SET amplitude and pulsewidth. If the SET pulse arrives during the latching window and has sufficient energy, it will be latched. Because of the relationship between this probability and the clock frequency, P_{latch} is listed in units of 1/MHz and also as a probability at two specified clock frequencies: 625 KHz and 5 MHz.

Table V shows a comparison between the latching threshold and the propagation threshold. The table shows that the latching threshold is indeed larger than the propagation threshold. A close look at an SET propagating within the flip-flop shows the reason the latching threshold is higher than the propagation threshold. Figs. 6 and 7 show the voltage of the SET pulse at the input of the D-flip-flop, and at Node 4_1, which is the node

TABLE III
PROBABILITY OF LOGIC PROPAGATION

Standard Cell	Probability of Logic Propagation
Inv	1
Buf4	1
Nand2	0.5 (Non-Pipeline) Instruction-Dependent (Pipeline)
Nand3	0.25
Nand4	0.125 (Non-Pipeline) Instruction Dependent (Pipeline)
Nor2	0.5 (Non-Pipeline) Instruction-Dependent (Pipeline)
Nor3	0.25
Nor4	0.125 (Non-Pipeline) Instruction-Dependent (Pipeline)
Xor2	1
Mux2	Instruction-Dependent

TABLE IV
CLOCK-EDGE EFFECTS MODELING RESULTS

SET Amplitude (V)	SET Pulse-width (ps)	Latching Window (ps)	P_{latch} (1/MHz)	P_{latch} @ 625 KHz	P_{latch} @ 5 MHz
-3.3	480	60	6.00×10^{-5}	3.75×10^{-5}	3.00×10^{-4}
-3.3	490	80	8.00×10^{-5}	5.00×10^{-5}	4.00×10^{-4}
-3.3	500	180	1.80×10^{-4}	1.13×10^{-4}	9.00×10^{-4}
-3.3	510	190	1.90×10^{-4}	1.19×10^{-4}	9.50×10^{-4}
-3.3	520	230	2.30×10^{-4}	1.44×10^{-4}	1.15×10^{-3}
-3.3	530	270	2.70×10^{-4}	1.69×10^{-4}	1.35×10^{-3}
-3.3	550	340	3.40×10^{-4}	2.13×10^{-4}	1.70×10^{-3}
-3.3	560	360	3.60×10^{-4}	2.25×10^{-4}	1.80×10^{-3}
3.3	510	70	7.00×10^{-5}	4.38×10^{-5}	3.50×10^{-4}
3.3	520	140	1.40×10^{-4}	8.75×10^{-5}	7.00×10^{-4}
3.3	560	210	2.10×10^{-4}	1.31×10^{-4}	1.05×10^{-3}
3.3	580	240	2.40×10^{-4}	1.50×10^{-4}	1.20×10^{-3}
3.3	600	280	2.80×10^{-4}	1.75×10^{-4}	1.40×10^{-3}
3.3	640	330	3.30×10^{-4}	2.06×10^{-4}	1.65×10^{-3}
3.3	670	370	3.70×10^{-4}	2.31×10^{-4}	1.85×10^{-3}
3.3	690	400	4.00×10^{-4}	2.50×10^{-4}	2.00×10^{-3}

TABLE V
PROPAGATION AND LATCHING THRESHOLDS

Transition	Propagation Threshold		Latching Threshold	
	Amplitude	**Pulsewidth**	**Amplitude**	**Pulsewidth**
1-0-1	**-3.3V**	**460 ps**	**-3.3V**	**480 ps**
0-1-0	**3.0V**	**400 ps**	**3.3V**	**510 ps**

after the input pass-gate of the flip-flop. Fig. 6 shows the voltages for an SET that is slightly above threshold. Fig. 7 shows the voltages for an SET that is slightly below threshold. In both cases, the SET arrives at the DATA input. The transient is attenuated as it passes to Node 4_1. This is because the on-resistance of the pass-gate coupled with the capacitance at Node 4_1 form a low-pass filter that removes the high frequency components of the transients. Transients with wider pulsewidths have more energy at lower frequencies and more energy is passed through the low-pass filter. In Fig. 6, the transient has enough energy after this attenuation to keep the voltage at Node 4_1 at logic "0" when the rising edge of the clock occurs, which results in the SET being latched. In Fig. 7, the transient is able to pass some energy to Node 4_1. However, not enough energy is passed through for the voltage at Node 4_1 to be latched in. Thus, the smaller transient is not latched.

Because the latching threshold is greater than the propagation threshold, the latching threshold defines the minimum amplitude and pulsewidth for an SET in logic to be latched and become an SEU. This simplifies the determination of $\delta 1$, because if the SET meets the latching threshold requirements, the probability of analog propagation is equal to one. If an SET does not meet the latching threshold requirements, $\delta 1$ is set to zero because it will not be latched.

E. Determining the Transitional Probability $\delta 1$

In the SET State-Transition Model, $\delta 1$ is the probability that an SET will propagate from the sensitive region of a logic gate

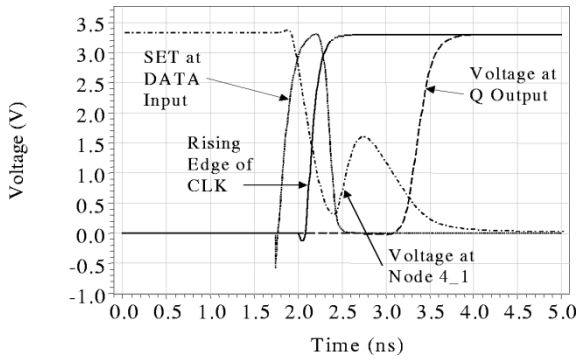

Fig. 6. SET above latching threshold.

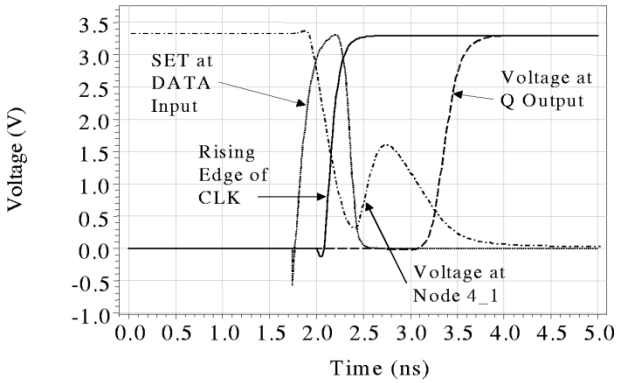

Fig. 7. SET below latching threshold.

where generation occurred to the input of the memory element and be latched in. Thus, $\delta 1$ is the product of the $\mathrm{P_{latcch}}(a, pw) * \mathrm{P_{scl}} * \mathrm{P_{ap}}(a, pw)$, and $\delta 1$ can be multiplied by the cross-section of the logic gate to give the effective cross-section [1]

$$\sigma_{eff} = \sigma \delta l.$$

The total effective cross-section of a logic path is the sum of the effective cross-sections of each of the sensitive regions in the logic path. For a logic path with m sensitive regions [1]

$$\sigma_{eff,\, logic\ path} = \Sigma \sigma_n \delta 1_n,\ n = 1 \text{ to } m.$$

Fig. 8 shows the logic path from the output of registers A and B in the register file to the input of the ALU register for the AND instruction. The importance of modeling the logic propagation of the Mux2 is apparent in this figure. The sensitive regions are determined by the datapath steered by the Mux2s, which are controlled by the instruction being executed. Table VI shows $\delta 1$ and the effective cross-section evaluated at each logic block in the path.

F. SEU Propagation Modeling Results

The SEU propagation modeling uses a combination of instruction-based register-usage analysis and VHDL modeling to determine which internal registers are necessary for the proper execution of an instruction. Proper execution is defined as follows: for each pipeline stage, if all internal registers and external signals that are affected by the instruction are correct at the end of that stage, then proper execution of that stage has occurred. For example, in the register add instruction (ADD Rd, Rs1, Rs2), the contents of source register 1, Rs1, is added to source register 2, Rs2, and stored in the destination register, Rd. Table VII shows the critical registers for each pipeline stage for this instruction. This analysis is performed for all instructions of the KDLX instruction set.

G. System-Level Prediction

The results of the SET propagation simulations and SEU propagation modeling are applied to determine the effective cross-sections of three test programs. The effective cross-section for a given program is the product of the SET transitional probabilities, the SEU transitional probabilities and the cross-sections determined in the SET generation modeling. Test Program #1 is a program that loads all the registers, writes them out immediately, waits for approximately 240 clock cycles, and repeats the process. Test Program #2 is similar, except it loads all registers, waits for 240 clock cycles, and writes them out. Test Program #3 is a functionality test program, similar to the program used for verification of the processor design prior to fabrication. Test Program #3 loads the registers, performs an operation (e.g., ADD, XOR) on the register, and writes the result to the output. All operations are exercised in this manner in Test Program #3. Table VIII shows the average number of sensitive bits per clock cycle for each program. In the table, an access error is defined as an error on the address or data lines during a memory access; a control error is an error on the read or write control signals, and a program address error is an error on the program address bus. Table IX shows the contribution of the memory elements and logic elements to the effective saturated access error cross-sections for Test Program #1 and Test Program #2. The crossover point in the table is the frequency at which the contribution due to logic elements is equal to the contribution due to memory elements. This crossover point is much greater than the operating frequency of the device. The table shows that the effective cross-section due to the logic elements is negligible at 625 kHz and 5 MHz.

IV. Methodology Validation

The validation of this research consisted of both heavy-ion testing and pulsed laser testing. The laser testing validates the specific transitional probabilities. The heavy-ion testing validates the system-level predictions.

A. Laser Testing

The objective of the laser testing is to validate the predicted transitional probabilities $\delta 1$ and $\varepsilon 1$. The laser provides the opportunity to inject an SET or SEU on a specific transistor within the KDLX. Focusing the laser on a transistor of a logic gate allows direct insertion into state S2. This provides for validation of the two critical elements of $\delta 1$: clock-edge effects modeling and the probability of logic propagation. Similarly, focusing the laser on a transistor within a flip-flop provides direct insertion into state S3. This provides for validation of the instruction-based register-usage analysis used to predict $\varepsilon 1$.

The laser tests were performed at the Naval Research Laboratory's Pulsed-Laser Facility for SEEs Investigation [28]. The laser source is a 590 nm wavelength pulsed dye laser. The laser

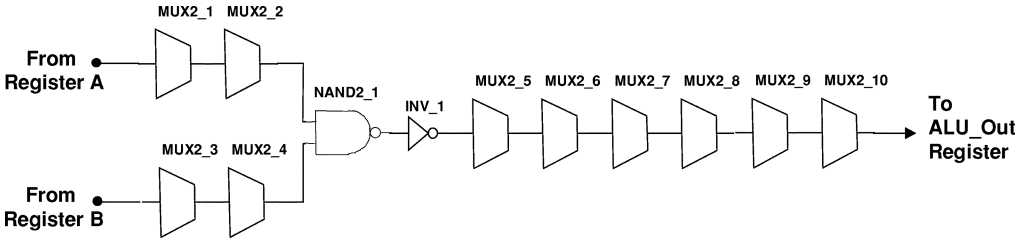

Fig. 8. AND combinational-logic datapath.

TABLE VI
EFFECTIVE CROSS-SECTION OF AND DATAPATH

Logic Block	Cross-section (μm^2)	P_{scl}	P_{ap}	$P_{latched}$ (1/MHz)	$\delta 1$ (1/MHz)	Effective Cross-Section $\sigma*\delta 1$ (μm^2/Mhz)	Effective Cross-Section @ 625 KHz (μm^2)	Effective Cross-Section @ 5 MHz (μm^2)
Mux2_1	131.62	0.5	1	1.50×10^{-4}	7.50×10^{-5}	9.87×10^{-3}	3.29×10^{-3}	2.63×10^{-2}
Mux2_2	131.62	0.5	1	1.50×10^{-4}	7.50×10^{-5}	9.87×10^{-3}	3.29×10^{-3}	2.63×10^{-2}
Mux2_3	131.62	0.5	1	1.50×10^{-4}	7.50×10^{-5}	9.87×10^{-3}	3.29×10^{-3}	2.63×10^{-2}
Mux2_4	131.62	0.5	1	1.50×10^{-4}	7.50×10^{-5}	9.87×10^{-3}	3.29×10^{-3}	2.63×10^{-2}
Nand2_1	41.75	1	1	1.50×10^{-4}	1.50×10^{-4}	6.26×10^{-3}	2.09×10^{-3}	1.67×10^{-2}
Inv_1	35.79	1	1	1.50×10^{-4}	1.50×10^{-4}	5.37×10^{-3}	1.79×10^{-3}	1.43×10^{-2}
Mux2_5	131.62	1	1	1.50×10^{-4}	1.50×10^{-4}	1.97×10^{-2}	6.58×10^{-3}	5.26×10^{-2}
Mux2_6	131.62	1	1	1.50×10^{-4}	1.50×10^{-4}	1.97×10^{-2}	6.58×10^{-3}	5.26×10^{-2}
Mux2_7	131.62	1	1	1.50×10^{-4}	1.50×10^{-4}	1.97×10^{-2}	6.58×10^{-3}	5.26×10^{-2}
Mux2_8	131.62	1	1	1.50×10^{-4}	1.50×10^{-4}	1.97×10^{-2}	6.58×10^{-3}	5.26×10^{-2}
Mux2_9	131.62	1	1	1.50×10^{-4}	1.50×10^{-4}	1.97×10^{-2}	6.58×10^{-3}	5.26×10^{-2}
Total						$\mathbf{1.50 \times 10^{-1}}$	$\mathbf{4.99 \times 10^{-2}}$	$\mathbf{4.00 \times 10^{-1}}$

TABLE VII
CRITICAL BITS AND CLOCK CYCLE FOR ADD RD, RS1, RS2

Pipeline Stage	Critical Registers & Clock Cycles
Fetch	Program_Counter(16 bits): 1 clock cycle
Decode	Decode_Instr_Reg(12 bits): 1 clock cycle
	Rs1(16 bits): n clock cycles since Rs1 was last written
	Rs2(16 bits): m clock cycles since Rs2 was last written
Execute	Execute_Instr_Reg(11 bits): 1 clock cycle
	RA(16 bits): 1 clock cycle
	RB(16 bits): 1 clock cycle
Memory	Memory_Instr_Reg(4 bits): 1 clock cycle
	ALU_Out(16 bits): 1 clock cycle
Writeback	WB_Instr_Reg(6 bits): 1 clock cycle
	Delayed_ALU_Out(16 bits):1 clock cycle

TABLE VIII
AVERAGE NUMBER OF SENSITIVE BITS PER CLOCK CYCLE

Test Program	Access-Errors Sensitive Bits per Clock Cycle:	Control-Errors Sensitive Bits per Clock Cycle:	Program-Address- Errors Sensitive Bits per Clock Cycle:
1	10.7	1.2	15.94
2	231.0	1.2	15.94
3	272.0	7.13	19.24

TABLE IX
COMPARISON OF MEMORY ELEMENT AND LOGIC ELEMENT SATURATED ACCESS ERROR CROSS-SECTIONS.

Test Program	Effective Cross-Section Due to Memory Elements (cm^2/device)	Effective Cross-Section Due to Logic @ 625 kHz (cm^2/device)	Effective Cross-Section Due to Logic @ 5 Mhz (cm^2/device)	Cross-Over Frequency
1	3.59×10^{-6}	9.375×10^{-10}	7.5×10^{-9}	2.393 GHz
2	7.77×10^{-5}	9.375×10^{-10}	7.5×10^{-9}	51.8 GHz

pulses are nominally 1 picosecond in length. Two pulse repetition frequencies were used: 100 Hz and 1 KHz. Optics between the laser source and the device-under-test focus the beam to a spot size of approximately 1.5 μm [29]. This allows the targeting of a single transistor.

1) Laser Test #1: The purpose of Test #1 is to validate the logic propagation modeling. Specifically, it validates the modeling of logic propagation for the Mux2 standard-cell multiplexer. Table III defines this probability as being "Instruction-Dependent." This is a critical concept in the determination of the effective cross-section of a logic path; it says that logic elements that are not in the logic path do not contribute to the effective cross-section. To validate this, the functionality test program, Test Program #3, was executed with the laser beam focused on the combinational-logic elements of the ALU_Logic_Slice module. This module performs the logic operations of the arithmetic logic unit (ALU). Fig. 9 shows its schematic. The shaded circles show the targeted regions. The module consists of an AND gate, an OR gate, an XOR gate, and three multiplexers that determine the output. For logical AND instructions, $\mathrm{Sel0} = 1$ and $\mathrm{Sel1} = 0$, steering the output of the AND gate to the output of the module. Similarly, for logical-OR instructions, $\mathrm{Sel0} = 0$ and $\mathrm{Sel1} = 1$, steering the output of the OR gate to output of the module. The output of the XOR gate is steered to the module output with $\mathrm{Sel0} = 1$ and $\mathrm{Sel1} = 1$ for exclusive-or instructions.

For Test Run #1, the beam was focused on the output of the AND gate. Ten errors were observed at the output: six occurred during the ANDI instruction execution, and four occurred during the execution of the AND instruction. None occurred during the logical-or (OR, ORI) or the exclusive-or (XOR, XORI) instructions

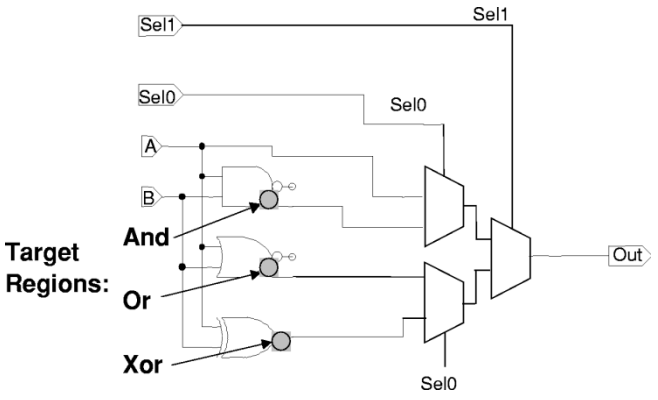

Fig. 9. Laser test #1 targeted regions.

during Test Run #1. In Test Run #2, the beam was focused on the output of the OR gate. Errors occurred only during the execution of the logical-or instructions. Similarly, Test Run #3 focused the beam on the output of the XOR gate. Errors occurred only during the execution of the exclusive-or instructions. The results of these three test runs are summarized in Table X. These results validate the premise that the combinational-logic elements that are not in an instruction's data path do not contribute to the effective cross-section for that instruction.

2) Laser Test #2: The purpose of Test #2 is to validate the clock-edge effects modeling. Specifically, the relationships among the clock frequency, SET pulsewidth, and the probability that an SET is latched (P_{latch}) are validated. This was accomplished by injecting an SET on a transistor in the Full_Adder module of the ALU. In the first group of tests, the output energy detector voltage was 14 mV. In the second group, the laser energy was decreased; the output energy detector voltage was 8 mV. This resulted in a reduced length SET pulse. For each group of tests, the KDLX executed Test Program #2 at four clock frequencies: 625 kHz, 1.25 MHz, 2.5 MHz, and 5 MHz. Table XI shows the results of these tests. Fig. 10 shows a plot of the number of upsets versus the clock frequency. The linear relationship between the clock frequency and the number of upsets is clearly evident, particularly at the higher energy (where the statistics are better). This validates the predicted linear relationship between clock frequency and P_{latch}.

Validation of the absolute quantitative relationship between the length of the SET pulse and P_{latch} requires an accurate measurement of the SET pulsewidth at the injection node. Unfortunately, this is not possible with the KDLX chip. This is because the SET must propagate through multiple logic gates prior to reaching the output; it is shaped and attenuated during this propagation and thus cannot be accurately measured. However, it is clear from the data that for a given clock rate, a longer SET pulse results in a larger P_{latch}.

3) Laser Test #3: The purpose of Test #3 is to validate the predicted transitional probability $\varepsilon 1$. Validation requires injecting an SEU into a register and observing the resulting number of output errors as a function of the program. To accomplish this, the laser beam was focused on the least-significant bit of register R1. This transistor is sensitive only when the clock is high, so the probability of a laser pulse directly causing an SEU is 0.5 (i.e., $\beta 1 = .5$). The pulse repetition frequency of the laser was set at 1 KHz, and Test Program #1 was executed. Each test run lasted two minutes, causing an estimated 60,000 SEUs. This was repeated for Test Program 2, but the laser pulse repetition frequency needed to be reduced to 100 Hz because the test system could not keep up with the error rate. This resulted in an estimated 6000 SEUs. Table XII shows the test results. The measured transitional probability $\varepsilon 1$ for Test Program 1 was 0.003 97. This shows very good agreement with the predicted $\varepsilon 1$: 0.003 91. For Test Program 2 the measured $\varepsilon 1$ was 0.931. This also shows good agreement with the predicted $\varepsilon 1$: 0.922. These results validate the modeling approach for the transitional probability $\varepsilon 1$.

TABLE X
LASER TEST #1 RESULTS

Test Run	Target Cell	Number of Errors	Corresponding Instructions
1	AND Gate	10	ANDI(6) AND(4)
2	OR Gate	11	ORI(5) OR(6)
3	XOR Gate	9	XORI(4) XOR(5)

B. Heavy-Ion Testing Results

The heavy-ion testing provides a measure of the device cross-section as a function of LET. Specifically, this testing validates the combined $\beta 1$ and $\varepsilon 1$ transitional probabilities, because the cross-section due to logic elements is insignificant at the operating frequency of the device as shown in Table IX. By executing the three different test programs used for the system predictions, the program-dependent cross-sections can be validated.

The heavy-ion tests were performed at the Texas A & M University Cyclotron Institute Radiation Effects Facility. Fig. 11 shows a comparison between the predicted access-error cross-sections and the measured access-error cross-sections from the heavy-ion testing. The predicted cross-sections track the measured values well, especially at the higher LETs. At the lower LETs the predicted cross-section overestimates the measured results. This may be due to the first order estimation of collection volume used in this work. Specifically, the collection volume was assumed to be constant over all LETs, with no diffusion length component. The presented data in Fig. 11 fits well at higher LETs without diffusion length consideration. This would suggest that the diffusion length may not be critical. The underestimation of the low LET data may be related to other factors such as the assumption of the shape of the collection volume. Further study with 3-D modeling tools may provide information on better assumptions for this technology. Additionally, using a model that varies the SET pulse shape as a function of LET could also improve the prediction of upset cross sections at lower LETs.

V. REAL-WORLD MODEL APPLICATION

Prior to real-world application of this model, the user must have an understanding of its limitations and strengths. The most significant limitation of this model is its poor prediction of effective device cross-section at low LETs. This is significant

TABLE XI
LASER TEST #2 RESULTS

Clock Speed	Energy Detector Output Voltage (mV)	Number of Upsets	P_{latch}
5 MHz	14	138	1.15×10^{-3}
2.5 MHz	14	78	6.5×10^{-4}
1.25 MHz	14	34.3	2.86×10^{-4}
0.625 MHz	14	17.3	1.44×10^{-4}
5 MHz	8	16	1.33×10^{-4}
2.5 MHz	8	12	1.00×10^{-4}
1.25 MHz	8	4	3.33×10^{-5}
0.625 MHz	8	2	1.67×10^{-5}

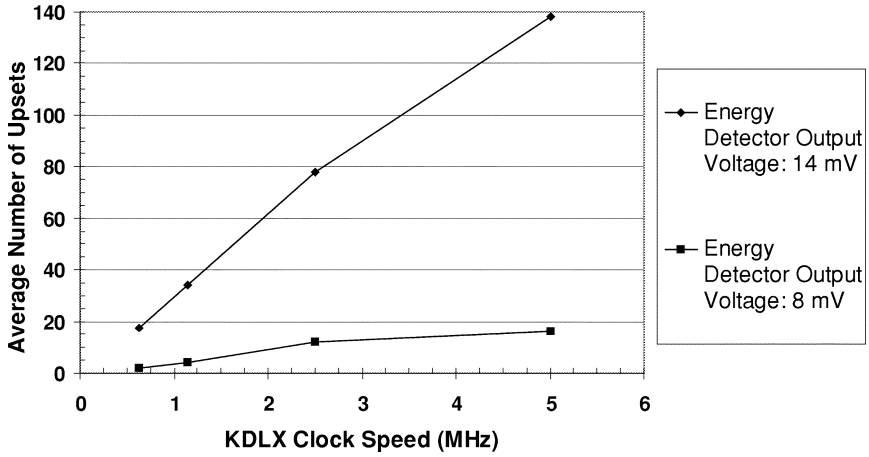

Fig. 10. Laser test #2 results.

TABLE XII
LASER TEST #3 RESULTS

Program	Laser PRF	Number of Pulses	Estimated Number of SEUs	Average Number of Output Errors	Transitional Probability ε1 (Measured)	Transitional Probability ε1 (Predicted)
Test Program 1	1 kHz	120,000	60,000	238.4	0.00397	0.00391
Test Program 2	100 Hz	12,000	6000	5479.8	0.9133	0.922

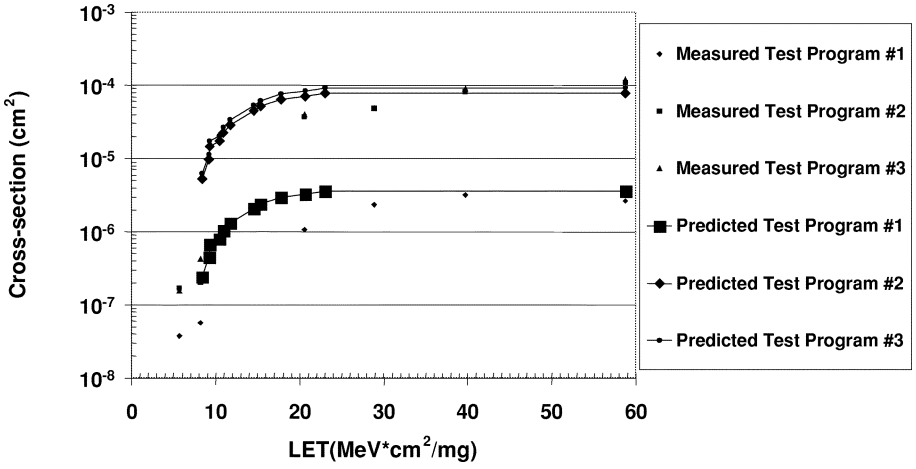

Fig. 11. Measured and predicted access-error cross-section versus LET.

because the natural cosmic ray environment is dominated by lower-LET ions, thus the predicted upset rate will also be dominated by the lower-LET ions (assuming the LET threshold of the device elements is low). Thus, this model will not provide a good prediction of the absolute upset rate on-orbit. Additionally, the accuracy of this model is limited by how accurately the transistor characteristics of the device are known.

The strength of this model is its ability to provide a good prediction of the relative effective cross-sections of a complex device for its various operating modes. This strength is clearly demonstrated in the heavy-ion testing results. Additionally, this model could be used to determine the effective cross-section in a standard-cell design when the cross-sections for the standard cells are known.

VI. Conclusion

The modeling and simulations documented were used to predict the transitional probabilities of the SEE State-Transition Model. These probabilities were combined to predict the test-program-dependent effective cross-section of the KDLX processor. The results of the laser testing validate the modeling of the transitional probabilities $\delta 1$ and $\varepsilon 1$. The results from the heavy-ion testing show very good agreement between the predicted and measured system-level cross-sections at high LETs. This validates the system-level modeling approach described in this paper. Additional research that focuses on modeling the collection volume at lower LETs may improve the overall prediction accuracy of the model.

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