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Multi-finger MOSFET Low Noise Amplifier Performance Analysis

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Engineering

By

XIAOMENG ZHANG

B.S., Dalian Jiaotong University, 2012

2014
WRIGHT STATE UNIVERSITY

WRIGHT STATE UNIVERSITY
GRADUATE SCHOOL

Dec. 29, 2014

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY
SUPERVISION BY Xiaomeng Zhang ENTITLED "Multi-finger MOSFET Low Noise
Amplifier Performance Analysis" BE ACCEPTED IN PARTIAL FULFILLMENT OF
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Abstract

Zhang, Xiaomeng. M.S.Egr, Department of Electrical Engineering, Wright State University, 2014. "MULTI-FINGER MOSFET LOW NOISE AMPLIFIER PERFORMANCE ANALYSIS"

Multi-finger layout technique has been extensively used in Nano-scale CMOS circuit design due to the increased circuit performance compared to a single finger layout. However choosing a finger width (W_f) and number of fingers (N_f) to optimize circuit performance is a challenging problem. In this thesis, the performances of 2.4GHz and 6.0GHz single ended low noise amplifiers (LNA) with fixed total transistor widths in 90nm CMOS technology are analyzed as function of number of fingers, bias voltage (V_{bias}) and channel length (L). The results show that the drain to source current, transconductance and effective gate capacitance increase with increasing number of fingers. The effect of finger numbers, supply voltage and channel length on transistor cutoff frequency, low noise amplifier noise figure, voltage gain, center frequency, and impedance matching is presented. The simulation results show that the finger numbers affect the single ended cascode low noise amplifier slightly due to the inductors used. The bias voltage and channel length are the key parameters for this low noise amplifier design. A 200nm transistor length LNA has better gain and filter quality factor compared with 100nm for 2.4GHz and 6GHz cases in 90nm process. A higher bias voltage can decrease the noise figure, however, the trade-off is the power consumption is increased.

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I. INTRODUCTION

1.1 CMOS Technology

Complementary metal oxide silicon (CMOS) has become a widely used technology in radio frequency application because of its low cost, low power, small size and high integration density features [1].

Channel length is one of the key factors for CMOS technology. As CMOS technology gets more advanced as time goes on, transistor length (feature size) is getting smaller as shown in (Fig. 1.1), while transistor speed becomes faster, integration is bigger, and cost becomes less [2]. However, process variation, voltage variation and temperature variation are getting larger which become the key drawbacks for active components in CMOS nanotechnology. Analog circuit performance like center frequency, gain become more sensitive to process, temperature and voltage variation [3], which result the yield of fabrication down.

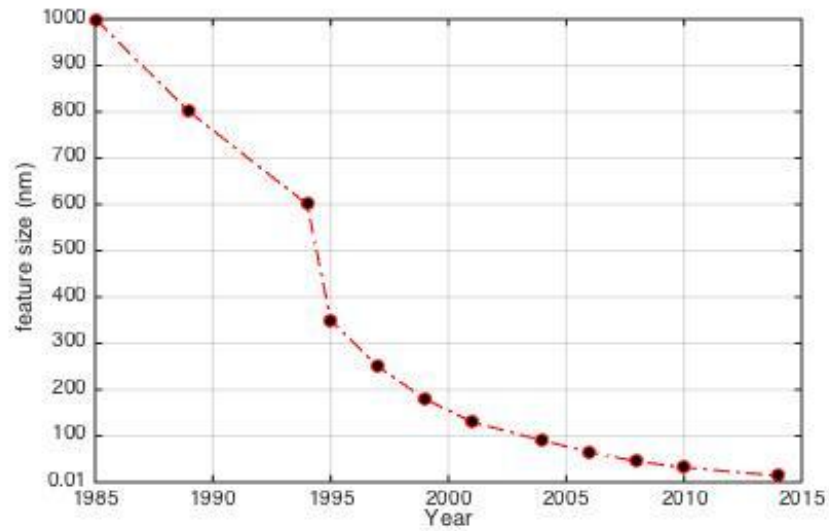


Fig. 1. 1 Feature size versus year plot [2]

1.1.1 Multiple Finger Technology

Multiple finger technique has been proved to have many advantages compared with single finger transistor. It can enhance the transconductance for a single transistor because of the lower gate resistance [4]. [5] It is widely used in industry. Usually, the transistor size in analog circuits is much larger than in digital circuits so it is necessary to divide the transistor into multiple fingers. However, the process variation for each finger is different. If all the fingers have decreasing trends or increasing trends for the transistor width, length, thickness or density, the total error will affect the transistor performance extremely. This is the worst case for a transistor with multi-finger. Most of the times, the random nature of the variations will cause the resulting error to be cancelled by each other [6].

1.2 Process, Voltage and Temperature Variation

PVT stands for the process to create the chip, supply voltage of the circuit and environment temperature of the circuit, which are the three key factors for designing and fabricating a circuit. One of these three factors changes slightly will affect the performance of the whole circuit in microscopic world significantly [5].

1.2.1 Process Variation

Process variations are due to the different environments of manufactory. The slightly difference of temperature, pressure, dopant concentration will changes the performance of the transistors. The condition of the manufactory will change the transistor width, length, diffusion depth, impurity or the concentration density and silicon dioxide thickness [3]. Even in the same wafer, it is still hard to keep all the transistors under the same condition. In this case, it is impossible to keep all the transistors having the same performance, and the process variation exists throughout the entire chip.

1.2.2 Voltage Variation

Voltage variation is due to the variation of the supply voltage. For the transistors, the speed is decided by the current, and the current is decided by the voltage. If the voltages throughout the circuit are different, then the speed will be

affected. When the transistors are working under the saturation region, the current follows the square law. Equation 1.1 [2] shows the relationship between gate voltage and current of the transistors, where V_{gs} and V_{sg} are the gate to source voltage for a NMOS and source to gate for a PMOS transistor, respectively. V_{tn} and V_{tp} are the threshold voltages for the nMOS and pMOS transistors respectively. V_{ds} and V_{sd} are the drain to source voltage for nMOS and source to drain voltage for pMOS respectively. μ_n is electron mobility for NMOS and μ_p is hole mobility for PMOS. C_{ox} is the capacitance per unit area of the gate oxide, which is decided by the permittivity of silicon dioxide and the thickness of the oxide. λ is the channel length modulation. W and L are the width and length for the transistors respectively.

$$\begin{cases} I_{ds} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{gs} - V_{tn})^2 (1 + \lambda V_{ds}) & (nMOS) \\ I_{sd} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right) (V_{sg} - |V_{tp}|)^2 (1 + \lambda V_{sd}) & (pMOS) \end{cases} \quad (1.1)$$

The decrease of the supply voltage will decrease the current exponentially, and increase the propagation delay significantly. In order to keep all the transistors working under the same speed, designers should set up the correct width and length of the transistors, considering the supply voltage. However, it is hard to realize. Firstly, a constant voltage supply is hard to realize. Meanwhile, switching activities across the chip, resistance of the transmission wires and the diversity of the type of logic will lead to the uneven power distribution [5].

1.2.3 Temperature Variation

With the dissipation of power, the temperature changes all the time throughout the chip. The mobility of the holes and electrons depends on the temperature. The mobility is inversely proportional to the temperature above -50°C . Higher temperature will decrease the speed of the semiconductor. Meanwhile, the threshold voltage and the temperature have some relationships. The higher temperature will decrease the threshold voltage. Based on equation 1.1, the decreasing of the threshold voltage will increase the current and speed. In conclusion, it is a competition between the mobility and the threshold voltage. For most of times, the mobility factor wins. The temperature factor changes the performance of the circuit all the time, and it is an unavoidable factor for the every design [3].

1.2.4 Measurements for PVT variations

The process, voltage and temperature variations are unavoidable in every semiconductor designs, which have a significant effect on the performance of the circuit. There is a long way for the designers to find some efficient ways to solve the problems. Corner analysis and Monte Carlo analysis are two ways to analyze process, temperature and voltage variation effects on semiconductors before the fabrication. They can be used to analyze/simulate all different scenarios of the fabrication.

1.3 CMOS Receiver System

Receivers are widely used in electrical devices such as radar, GPS, cell phones etc. Receiver chains are systems that are able to receive any signals from low frequency to high frequency, then convert the received signals to electrical signals by various sensors/detectors, such as heart beating detector, antenna etc. The received signals from sensors are usually weak and noisy, so a low noise amplifier (LNA) and a band pass filter are typically the first two components of a receiver after the sensor as shown in Fig. 1.2. Fig. 1.2 is a block diagram for an antenna receiver chain system [7] [8].

LNA is an electrical amplifier, which amplifies the radio frequency weak signals and provides useful signals to next stage.

The function of a band pass filter (BPF) is to filter out the signals whose frequency below the $f_c - BW/2$ and frequency above $f_c + BW/2$ where BW stands for bandwidth. Therefore, the desired signal can be passed to the next stage circuits, and the filter attenuates most unwanted signals outside the BW [9]. As shown in Fig. 1.2, BPF 1 has the center frequency at radio frequency (f_{RF}) and BPF 2 has the center frequency at intermediate frequency (f_{IF}).

The signals from antenna are usually in radio frequency (RF), which is too high for most signal and image processing. A down converter is used to convert the RF signal to intermediate frequency (IF) signal, which requires a local oscillator (LO) as shown in Fig. 1.2. The IF frequency after BPF 2 with center frequency of f_{IF} is shown in Eq. 1.2.

$$f_{IF} = f_{RF} - f_{LO} \quad (1.2)$$

The following amplifier (AMP) is used to amplify the intermediate frequency signals to the desired strength for further processing.

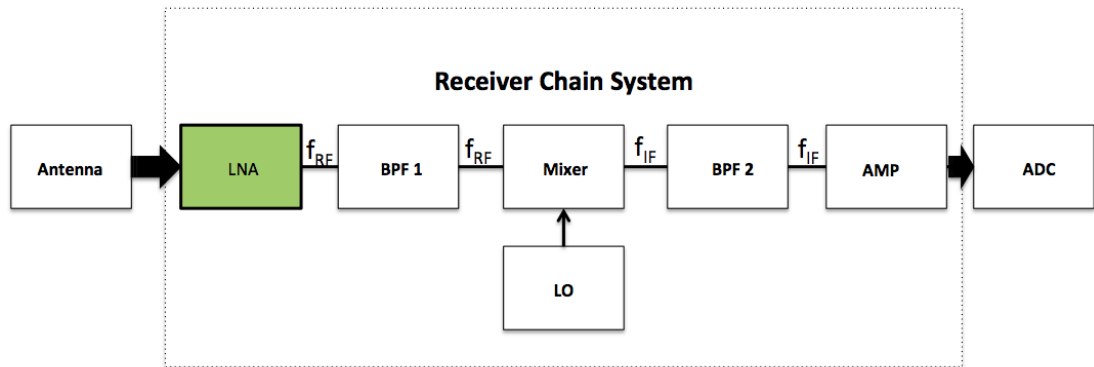


Fig. 1. 2 Receiver chain system [10]

1.4 Low Noise Amplifier

To increase the quality of signals, an LNA is needed to amplify signals at its center frequencies (f_c) with certain bandwidth and less noise. In this case, a high gain, high filter quality factor (Q) and low noise LNA need to be designed to enhance the system performance. The gain (A_V) and Q will affect the quality of the LNA output signals and the property of the entire system. Another key parameter for an LNA is noise figure (NF), which is used to measure how much noise is added by the amplifier to the input noise. [11]. In order to decrease the noise for the whole system, a low noise factor is required for LNA design. Typically, LNA

always be the first stage for a receiver chain system. As the first stage of on-chip component, impedance matching is also very important. A good impedance matching will decrease the signal reflection and increase the signal quality [12] [13].

1.4.1 LNA Architecture

For LNA designs, numerous architectures have been proposed in every year. However, there is no single LNA topology that could satisfy all kinds of applications. In order to get optimum results in certain aspects, other properties must be sacrificed. Fig. 1.3 indicates the trade-offs among different types of LNA architecture [14] [15] [16].

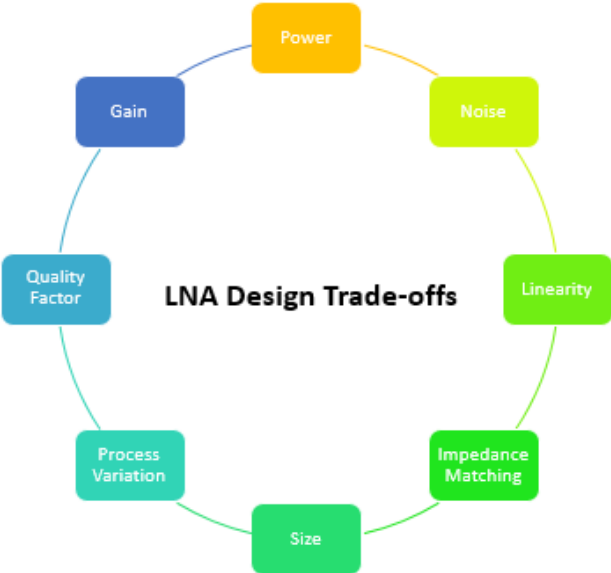


Fig. 1. 3 LNA Design Trade-offs

The architectures can be divided into two classes: single ended LNA and differential output LNA, which are shown in Fig. 1.4 (a) and (b), respectively [17].

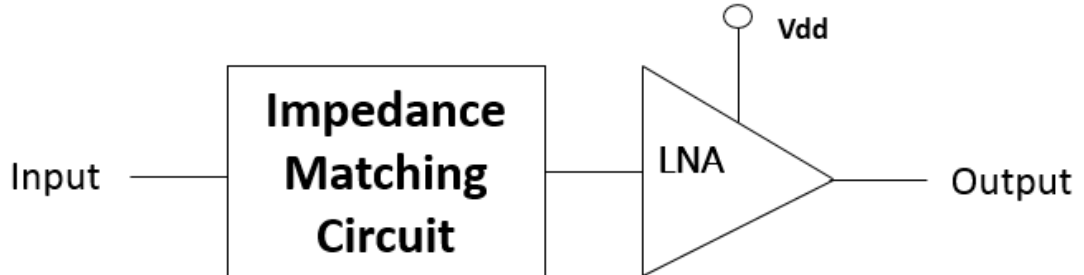


Fig. 1.4(a) Single ended output LNA block diagram

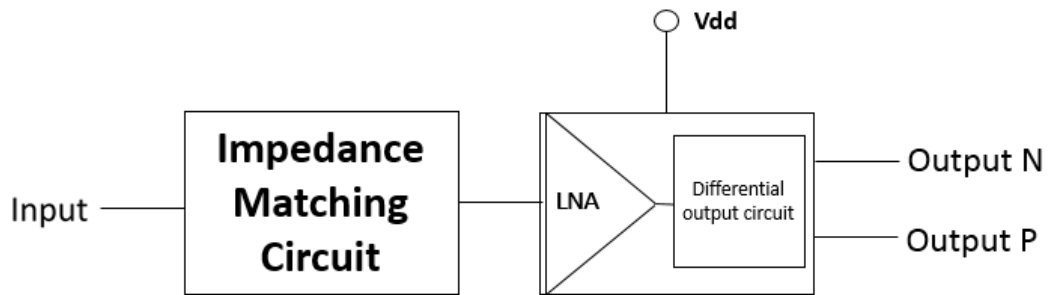


Fig. 1.4 (b) Differential output LNA block diagram

Fig. 1. 4LNA topologies

As the name indicated, single ended LNA has single output and differential has two differential outputs. The differential outputs can be generated by a balun or similar elements from single ended output [18].

Compared with differential output LNA, single ended LNA has the least transistors inside. Single ended LNA is the simplest topology for LNA design. Fig. 1.4 shows five popular input circuits for single ended topologies: resistive common source, shunt series common source, common gate, inductive common source and

cascade inductor source degenerations. All of these input topologies can be used in differential output LNA designs [16] [17].

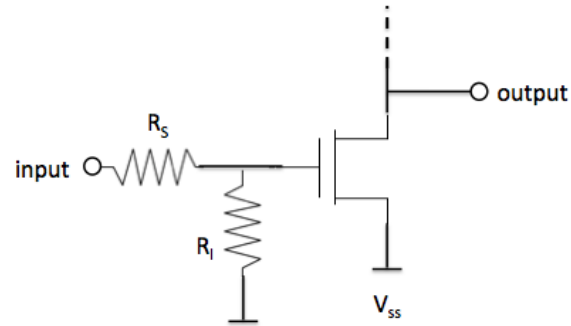


Fig 1. 5(a) Resistive Termination Common Source

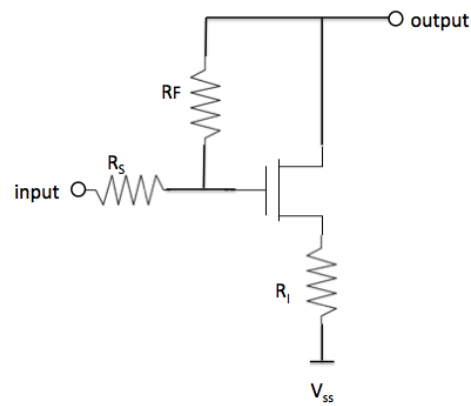


Fig 1. 5(b) Shunt-series Feedback Termination

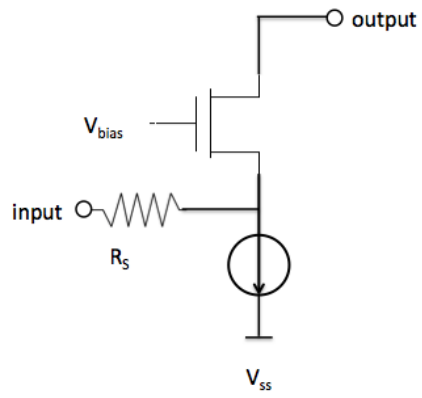


Fig 1. 5(c) Common Gate

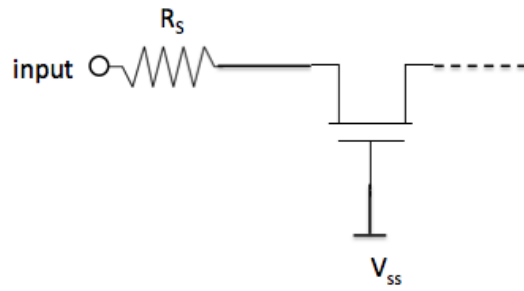


Fig 1. 5(d) $1/g_m$ Termination

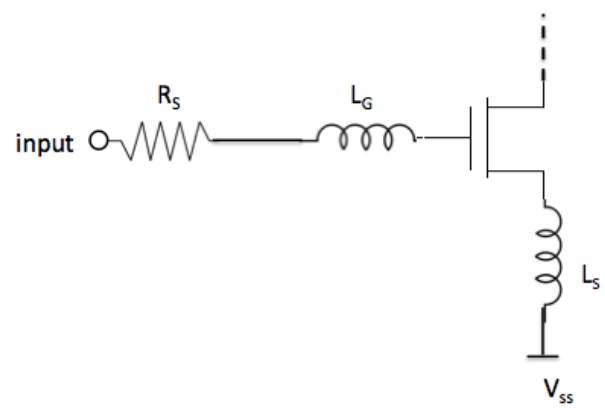


Fig 1. 5(e) Inductive Degeneration

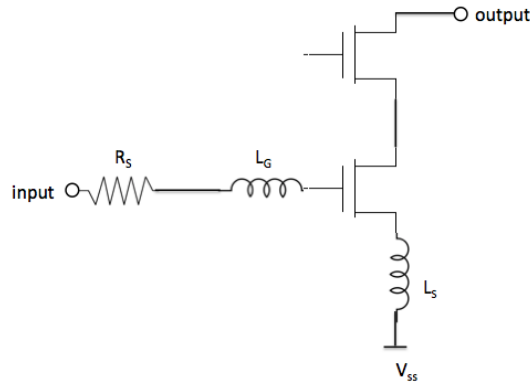


Fig 1. 5 (f) Cascode Inductor Source Degeneration

Fig. 1. 5 Different LNA architectures

Fig 1.4 (a) and (b) are using resistors to generate impedance matching circuit. The resistive components always have negative effects on noise performance. The LNA implemented in some reference paper [19] reported a relative high noise figure (6dB). Common gate circuit shown in Fig 1.4(c) has a much less gain among these designs, which is the trade-off for low power consumption. The disadvantage for $1/g_m$ termination architecture is its noise figure, which can go to around 3 dB or larger theoretically. Fig 1.4(f) is one of the LNA architectures using inductors instead of resistors, which has the best noise performance [16].

Among these five architectures, cascode source degeneration topology has the best performance in input and output isolation, gain and noise factor. The cascode transistor can reduce the Miller Effect for input transistor. The gate and source inductors are used to match off-chip impedance, and the tank circuit consisted by drain inductor and output capacitance will resonate the circuit working at its center

frequency. However, since some off-chip inductors are used in this topology, the drawback of cascade design is the circuit size is much larger than other single ended designs.

1.4.2 Single-Ended Cascode LNA

Single-ended LNA with cascode inductor source degeneration architecture is used for this thesis. The cascode architecture has a good performance in isolation. The transistor connected to gate reduces Miller Effect capacitance connected between input and output. Due to the same transistor widths are used, the transconductances (g_m) for these two transistors are similar, so that the Miller Effect capacitance is reduced because of the lower gain (-1) between the two transistors. Inductors are used instead of resistors because of the good performance for NF. The single ended tuned LNA is one of the popular LNA architectures and has been proved a good noise performance, high gain and high isolation in [13].

1.5 Thesis Objective

For a single ended cascode LNA, there are several parameters that can affect the circuit properties, which are number of fingers, bias voltage and transistor channel length. In order to enhance the receiver chain system performance, a low noise amplifier must be well analyzed and properly chosen. The objective of this thesis is to

1. Investigate the effect of N_f (number of fingers), V_{bias} and L (channel length) to a single transistor with fixed total width;
2. Design a low noise amplifier based on the knowledge on objective 1;
3. Study process variation effect to the LNA;
4. Improve the performance of LNA based on the knowledge on the first three objectives .

The rest of this thesis is organized as following.

- Single transistor performance with considering finger numbers, gate and drain voltage, channel length is discussed in Chapter 2.
- Chapter 3 analyzes a single ended cascode LNA design.
- Chapter 4 demonstrates the LNA simulation results with different input parameters.
- Conclusion and future work are included in chapter 5.

II Multiple Finger MOSFET Transistor Analysis

For an analog circuit such as LNA, a large transistor size is needed to meet the center frequency requirement. Multiple finger technique is the most effective method to build a large size transistor since the lower gate resistance, lower RF noise and higher frequency performance, however, keep reducing the transistor finger width (W_f) or increasing number of fingers (N_f) can result in the penalty of larger gate capacitance [20]. The multi-finger effect on single transistor is analyzed in this thesis.

2.1 Active area and perimeter estimation of multiple finger transistors

Fig. 2.1 indicates the multi-finger technique in a layout design. The example in this layout is an n-type MOSFET with four fingers. The wide width (W) transistor is broken into four shorter transistors with width of $\frac{1}{4} W$ for each single transistor. The four single transistors are combined to a four finger transistor by sharing the source and drain diffusion as shown in Fig. 2.1. The four fingers (in red) are shorted together to form the gate, three source diffusions and two drain diffusions are connected respectively to keep the transistor with four terminals and effective width of W .

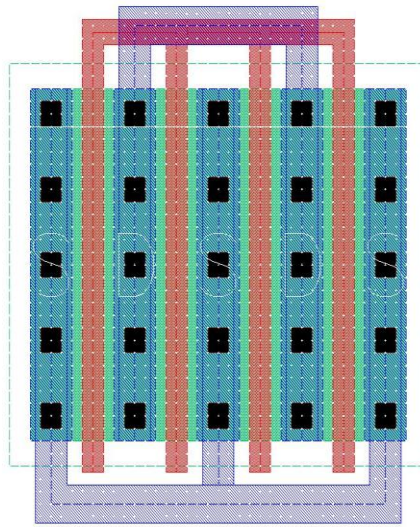


Fig. 2. 1 Multiple finger transistor layout

To analyze the relationship between finger numbers and transistor capacitance, a 3-D transistor diffusion view is show in Fig 2.

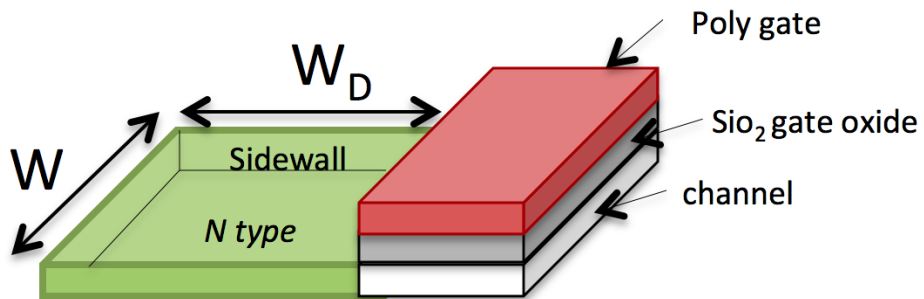


Fig. 2. 2 3-D View of CMOS Transistor Diffusion [21]

W_D is the diffusion width required by the fabrication. W is the width for a transistor. W value decreases with finger number increasing. The value for W can be considered as the finger width for a multi-finger case [21].

Fig. 2.3 (a) is a single transistor with only one finger. Fig. 2.3 (b) and 2.3(c) are single transistors with two fingers and three fingers, which represent even and odd number of fingers, respectively. For a two-finger transistor, each finger width is half of the original width. The area of the drain and source are decreased by increasing the number of fingers.

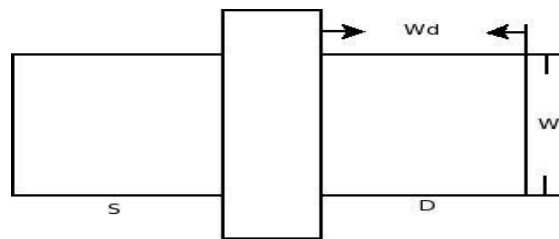


Fig. 2. 3 (a) One-finger single transistor

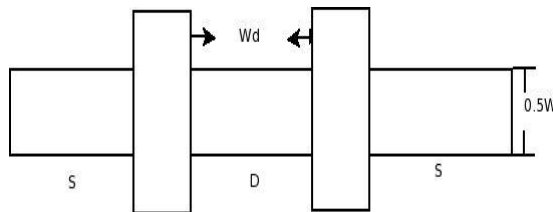


Fig. 2.3(b) Two-finger single transistor

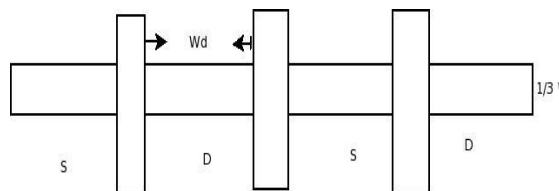


Fig. 2 .3(c) Three-finger single transistor

Fig. 2.3 Single transistor with different N_f

According to Fig2.2 and Fig 2.3(a), the drain (source) area and perimeter for a single finger transistor is developed in Equation 2.1 and 2.2 respectively. For a two-finger single transistor, the areas of drain (A_D) and source (A_S) are estimated in Equation 2.3 and 2.4, and the perimeters of drain (P_D) and source (P_S) in Equation 2.5 and 2.6 [21] [22] [23].

$$A_{D1} = A_{S1} = W \cdot W_D \quad (2.1)$$

$$P_{D1} = P_{S1} = W + 2W_D \quad (2.2)$$

$$A_D = \frac{1}{2}W \cdot W_D \quad (2.3)$$

$$A_S = \frac{1}{2}W \cdot W_D \cdot 2 = W \cdot W_D \quad (2.4)$$

$$P_D = 2 \cdot W_D + W \quad (2.5)$$

$$P_S = 2 \cdot (2W_D + 0.5W) = 4W_D + W \quad (2.6)$$

For a three-finger single transistor, the areas and perimeters of drain and source are estimated in Equation 2.7 to Equation 2.10

$$A_D = 2 \cdot \frac{1}{3}W \cdot W_D = \frac{2}{3}W \cdot W_D \quad (2.7)$$

$$A_S = 2 \cdot \frac{1}{3}W \cdot W_S = \frac{2}{3}W \cdot W_S = A_D \quad (2.8)$$

$$P_D = 2 \cdot 2W_D + \frac{1}{3}W = 4W_D + \frac{1}{3}W \quad (2.9)$$

$$P_S = 2 \cdot 2W_S + \frac{1}{3}W = 4W_S + \frac{1}{3}W = P_D \quad (2.10)$$

Table 2.1 summarizes the derived area and perimeter of drain and source for number of fingers being one, odd numbers and even numbers. Given one finger

transistor drain area as A_{D1} , source area as A_{S1} , and drain perimeter as P_{D1} , source perimeter as P_{S1} .

When N_f is an even number $2K$ (K is an integer), the number of drain diffusion is K , and source diffusions change to be $(K+1)$. Finger width (W_f) decreases to $(W/2K)$. So the total area for drain diffusion can be simplified to $(K \cdot W_f \cdot W_D / (2K))$, which is half A_{D1} ; and the perimeter of drain diffusion is $(2W_D \cdot K)$, which is less than one finger transistor perimeter P_{D1} . The total area for source diffusion is $((K + 1) \cdot W_f \cdot W_D / (2K))$, and $(2(K+1) W_D + 2W_f)$ for source diffusion perimeter.

When the finger number is an odd number, which equal to $(2K+1)$. The transistors are divided into same number of drain and source diffusion, and both of them equal to $(K+1)$. Drain and source diffusions are in same area and perimeter, which is derived to be $((K+1) \cdot W \cdot W_D / (2K + 1))$ and $(2(K+1) W_D + W_f)$ respectively.

Table 2. 1 Drain and source area and perimeter equations.

Finger Number	A_D	A_S	P_D	P_S
1	$A_{D1} = W \cdot W_D$	$A_{S1} = W \cdot W_D$	$P_{D1} = W + 2W_D$	$P_{S1} = W + 2W_D$
2K	$\frac{1}{2} A_{D1}$	$\frac{K+1}{2K} A_{S1}$	$2K \cdot W_D$	$2(K+1) W_D + 2W_f$
2K+1	$\frac{K+1}{2K+1} A_{D1}$	$\frac{K+1}{2K+1} A_{S1}$	$2(K+1) W_D + W_f$	$2(K+1) W_D + W_f$

For a large size single transistor, the multiple finger technology will decrease the drain and source diffusions size extremely. For example, a 100 μm total width transistor with single finger. The areas and perimeters of its diffusion are $100W_D$ and $(100+2W_D)$. For the same transistor, if finger number changed to be 5, then the area will go down to $60W_D$ and perimeter will change to be $(20+6W_D)$. If 20 fingers are used to implement the transistor, then the drain area will become $50W_D$ and source area will go to $55W_D$. The perimeter for drain and source diffusion are $20W_D$ and $(22W_D + 5)$ separately. For 90nm process technology, W_D is about 0.4 μm , which is much smaller than 100 μm .

In conclusion, multiple finger technology can enormously reduce the diffusion area and perimeter.

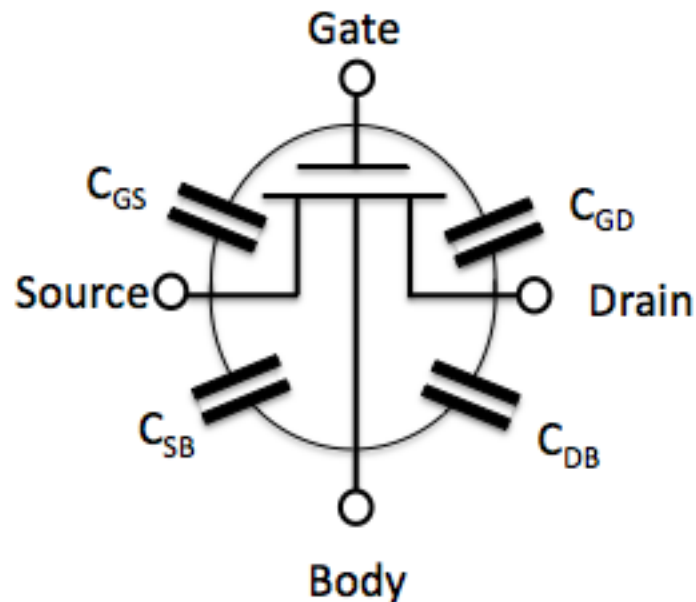


Fig. 2. 4gate to diffusion capacitances and diffusion to body capacitances for a transistor [2]

Parallel plate capacitors can be implemented by two conductors in parallel with insulator between them. For a single transistor, different capacitors exist between different terminals. Fig. 2.4 shows the capacitors between diffusion and gate, and diffusion to body.

The gate to diffusion capacitors (C_{GS} and C_{GD}) are overlap capacitors. They are related to transistor total width. The diffusion capacitors C_{DB} and C_{SB} are parasitic capacitances, which depend on area and perimeter. Parasitic capacitance is decided by two parts, junction capacitance and sidewall capacitance. 2.11 is the equation for junction capacitance, where CJ is the junction capacitance at zero bias, PB is the built-in potential which related to the doping levels, MJ is the junction grading coefficient, V_{db} drain to bulk voltage and A_D is diffusion area [2] [24] [25]. It can be simplified to proportional to area.

$$C_D = CJ \times A_D \times \left(1 + \frac{V_{db}}{PB}\right)^{-MJ} = CJ' \cdot A_D \quad (2.11)$$

Another capacitance is sidewall capacitance (shown in Eq. 2.12). $CJSW$, PHP and $MJSW$ are parameters similar to CJ , PB and $MJSW$, but with different coefficients. The sidewall capacitance can be simplified to be proportional to perimeter. All parameters can be found in the model files.

$$C_S = CJSW \times P_D \times \left(1 + \frac{V_{db}}{PHP}\right)^{-MJSW} = CJSW' \cdot P_D \quad (2.12)$$

For the source diffusion, all the parameters and coefficients are same, only change the drain area and perimeter to source area and perimeter. The diffusion capacitances equation can be simplified in Eq. 2.13 and 2.14:

$$\begin{aligned}
C_{DB} &= CJ \times A_D \times \left(1 + \frac{V_{db}}{PB}\right)^{-MJ} + CJSW \times P_D \times \left(1 + \frac{V_{db}}{PHP}\right)^{-MJSW} \\
&= CJ' \cdot A_D + CJSW' \cdot P_D \quad (2.13)
\end{aligned}$$

$$\begin{aligned}
C_{SB} &= CJ \times A_S \times \left(1 + \frac{V_{sb}}{PB}\right)^{-MJ} + CJSW \times P_S \times \left(1 + \frac{V_{sb}}{PHP}\right)^{-MJSW} \\
&= CJ' \cdot A_{DS} + CJSW' \cdot P_S \quad (2.14)
\end{aligned}$$

Comparing the area and perimeters of $N_f = 1$ case with multiple fingers design cases, the A_D and A_S are nearly reduced by half, and the P_D and P_S are also decreased significantly if the total width is 100um and W_D is about 0.4um. Twenty number of fingers will have a smaller diffusion capacitance than 5-finger number case. Only one finger case will have the largest area and perimeters among these three cases, and its diffusion capacitance will be much larger than others.

2.2 Multiple finger effect on a single transistor

A single transistor with 125um total width and 200nm channel length is tested in this section, and it will be used in the 2.4 GHz LNA design.

Transconductance is one of the important factors for the performance of transistors, which is the ratio of the current variation at the output to the voltage variation at the input as given in Equation 2.15.

$$g_m = \frac{i_{out}}{v_{in}} \quad (2.15)$$

f_T is the cut-off frequency of the transistor, which is related to the transconductance and effective gate capacitance (C_{geff}) as shown in Equation 2.16.

Noise figure is a measurement of degradation of the signal to noise ratio, which introduced in section 1.4. A smaller NF means a better noise performance. Equation 2.17 indicates the relationship between NF and f_T [16].

$$f_T = \frac{g_m}{2\pi C_{geff}} \quad (2.16)$$

$$NF = 1 + 2.4 \left(\frac{\gamma}{\alpha} \right) \left(\frac{f_C}{f_T} \right) \quad (2.17)$$

γ and α are channel thermal noise coefficient, f_C is the center frequency of the circuit. It can be seen that increasing cut-off frequency will bring the benefit of a lower noise figure.

As seen in (2.16) and (2.17), a higher g_m and smaller C_{geff} are two ways to enhance the NF performance. In a single ended tuned LNA, three parameters, V_{GS} , L and N_f , affect the g_m and smaller C_{geff} . The effect by V_{GS} , L and N_f to a single transistor is discussed in section four.

90 nm CMOS technology is used through the entire thesis. Fig. 2.5 shows the transconductance plot for different number of fingers under different V_{GS} , 0.6V fixed V_{DS} and 125um total width.

As seen in Fig. 2.5, the transconductance in narrow width per finger is higher than the transconductance in wider width. Besides, the V_{GS} has a big effect on g_m . With V_{GS} increasing, g_m gets larger until about 0.85V. After 0.85V, the plots become flat for all cases.

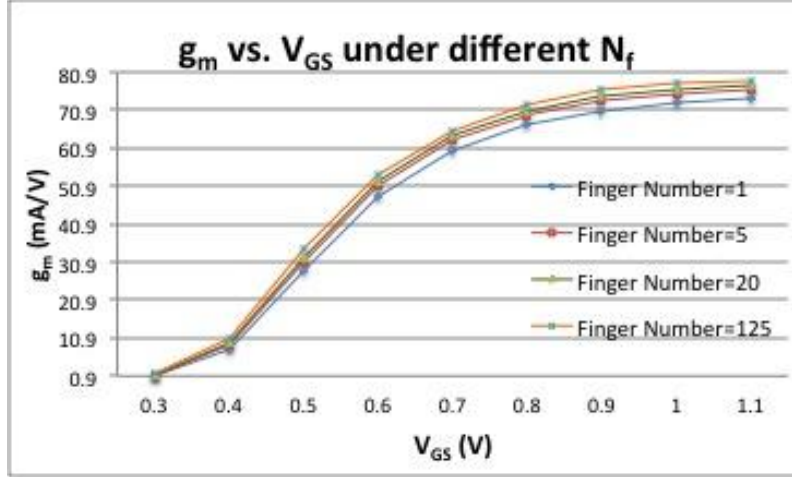


Fig. 2. 5 g_m vs. V_{GS} and N_f plot under 0.6V V_{DS} , 200nm Length and 125um total width

However, keep increasing the finger numbers does not have f_T followed because of the increased gate capacitance. Fig. 2.6 indicates f_T reaches the highest when N_f is 20 compared with 1, 5 and 125. For clarity purpose, only three cases are shown in Fig. 2.6.

From theory [25] [26], the effective gate capacitance is created by the gate sidewall fringing capacitances C_{gDiff} and C_{gCT} , and finger-end fringing capacitance $C_{f(poly-end)}$. The C_{gDiff} and C_{gCT} are linearly proportional to the total width, while the $C_{f(poly-end)}$ is independent of total width but decided by N_f . C_{geff} can be simplified as equation 2.18 .

$$C_{geff} = (C_{ox} \times L + C_{gDiff} + C_{gCT})W_T + C_{f(poly-end)}N_f \quad (2.18)$$

C_{ox} is the capacitance per unit area of the gate oxide, L is the channel length of the gate. $C_{ox} \times L$ is the intrinsic capacitance. $C_{gDiff} + C_{gCT}$ is the extrinsic capacitance. The intrinsic capacitances and extrinsic capacitances are linearly proportional with total width, while the $C_{f(poly-end)}$ is only proportional to N_f . In

this case, the finger numbers should be considered in CMOS design. A larger number of fingers will add the gate capacitance significantly.

The calculated effective gate capacitance by Equation 2.18 is plotted in Fig. 2.7 with respect to N_f . It can be seen C_{geff} increases following number of fingers increasing

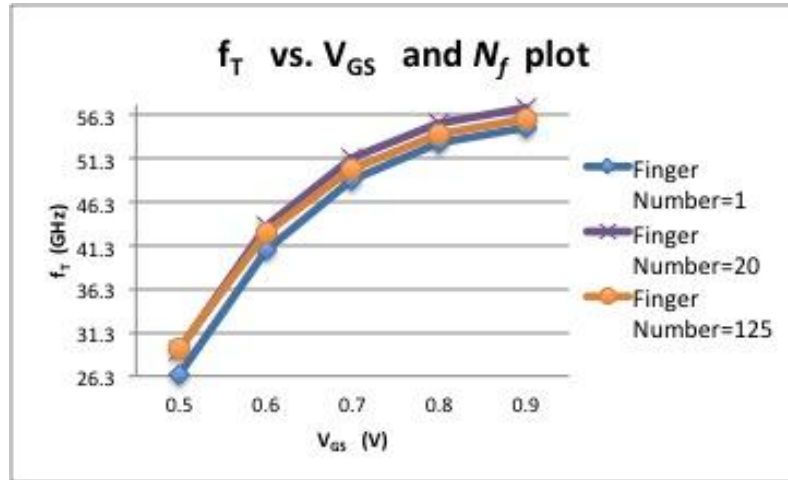


Fig. 2. 6 f_T vs. V_{GS} plot under different N_f , 0.6V V_{DS} and 200nm Length

f_t is low due to 200nm length. May want to discuss a little why 200nm rather than 100nm.

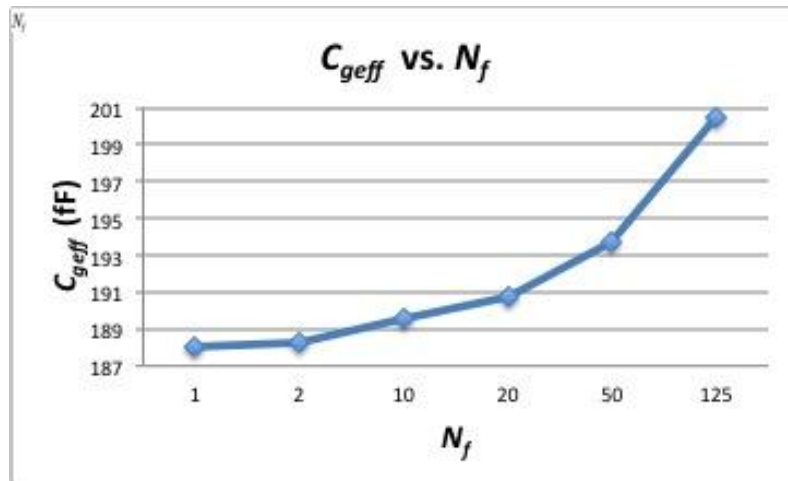


Fig. 2. 7 Calculated C_{geff} vs. N_f plot with 200nm Length

2.3 Other factor effects on a single transistor

V_{DS} and V_{GS} are two voltages that affect the performance of f_T . Fig. 2.8 indicates the relationship between f_T and the two voltages under the same transistor length, width and number of fingers. It can be seen that increasing V_{GS} will increase f_T monotonously if V_{DS} is greater than 0.5V. Also can be seen that f_T plot has the same trend as transconductance versus V_{GS} plot because of proportional relationship between f_T and g_m . Under the same V_{DS} , cut-off frequency goes up between V_{GS} equals to 0.5V to 0.8V, and then changes to be flat. The plot also indicates that the cut-off frequency may go down if keep increasing V_{GS} .

From Fig. 2.8, V_{DS} also affects the cut off frequency, but not as much as V_{GS} . Under same V_{GS} , a higher V_{DS} will increase f_T . In this case, a higher V_{GS} with a higher V_{DS} will enhance the performance of f_T . The performance of LNA with varying bias voltage will be discussed in section 4.

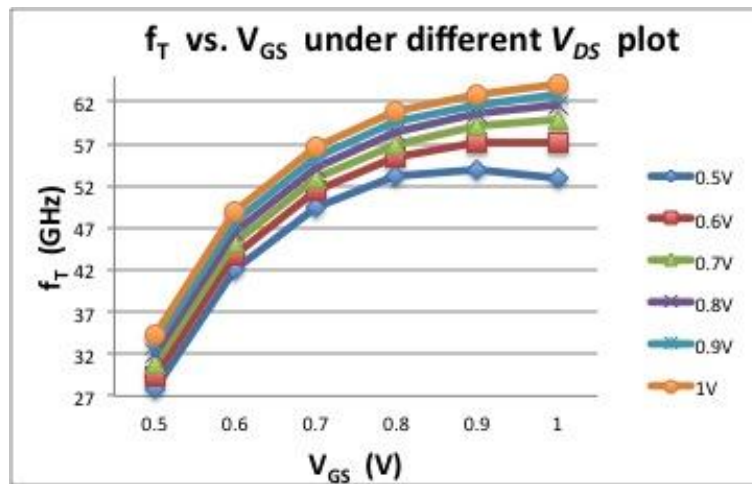


Fig. 2. 8 f_T vs. V_{GS} and V_{DS} plot under fixed width, length and N_f

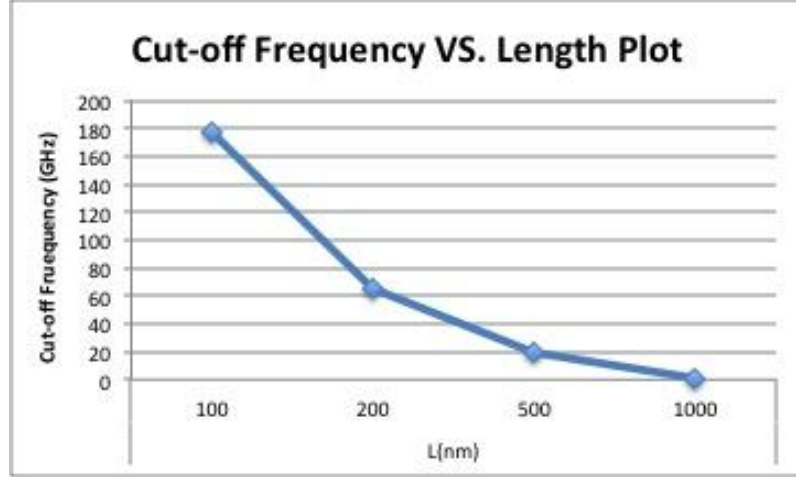


Fig. 2.9 f_T vs. L plot under same voltage, width and N_f

The transistor length has a huge effect on the f_T performance as shown in Fig. 2.9. Smaller channel gives larger cutoff frequency. The testing environment is $V_{DS}=1.2V$ and $V_{GS}=0.75$. From the previous work, a higher voltage of the drain and gate terminals will enhance the f_T performance of the transistor, so the drain and gate voltages are given as a relative high value.

It can be concluded that the narrow length makes the transistor have high cutoff frequency. The cut-off frequency can reach about 160 GHz at 100nm length, while the f_T can only go to several GHz at the 1um length.

Equation 2.19 shows the relationship between transconductance and current:

$$g_m = \sqrt{2\beta I_{DS}(1 + \lambda V_{DS})} \quad (2.19)$$

$$\beta = \mu_n C_{ox} \left(\frac{W}{L} \right) \quad (2.20)$$

β and I_{DS} are inversely proportional to L, so that the g_m is inversely proportional to L. To increase f_T , a higher g_m is needed, which can be implemented by increasing transistor width or decreasing transistor length or doing both.

However, narrow length transistors are more sensitive to PVT variations, which is shown in Fig.2.10. 100nm length and 200nm length NMOS transistors are employed to test the cut-off frequency with Monte Carlo Analysis. For 20 iteration cases and same testing environment for length effect on f_T , 100nm length has a 47.88GHz variation. Comparing the theoretical value for $f_T = 176.57GHz$, it has a -9.9% to 17.21% error. So the total error is 27.12%.

By contrast, the PVT variations performance of a 200nm length transistor is much better. The cut-off frequency varies from 58.51GHz to 70.13GHz, compared with 65.51GHz, which is an 11.62GHz variation. The error percentage range is from -10.69% to 7.05%, and total error is 17.73%. In this case, both the f_T performance and PVT variations should be considered in analog circuit design.

Keep in mind that for analog circuit design, transistor length cannot be too small for ultra-deep submicron CMOS technologies in considering PVT variation effects.

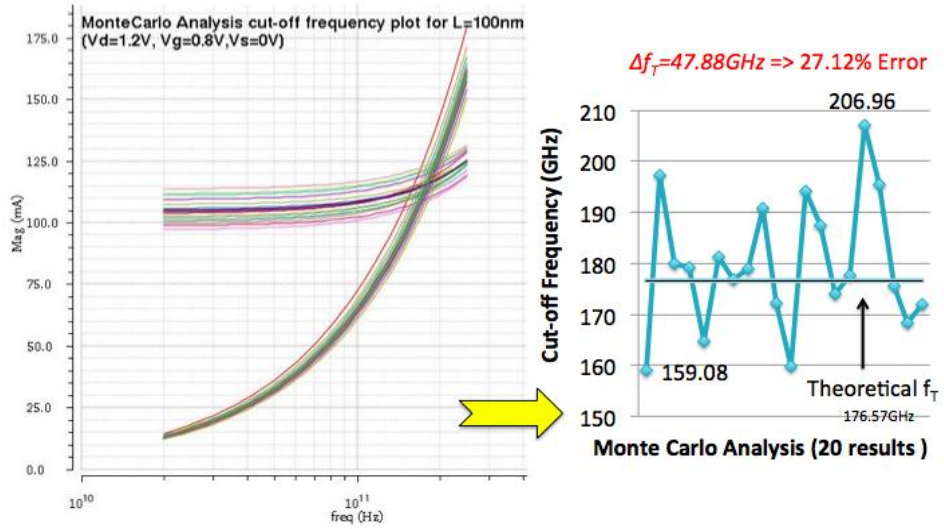


Fig. 2.10(a) Monte Carlo Analysis for 100nm f_T

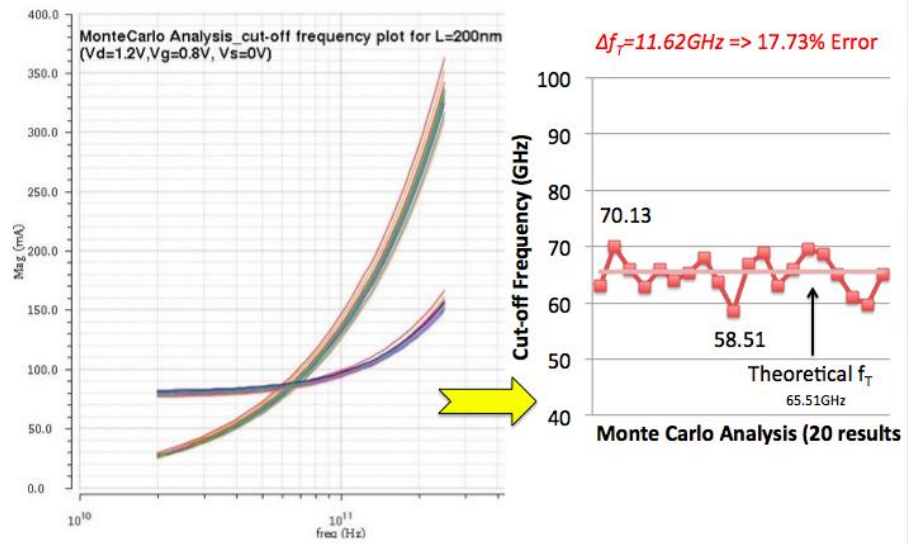


Fig. 2.10(b) Monte Carlo Analysis for 200nm f_T

Fig. 2. 10 100nm and 200nm Transistor f_T Variation

III Low noise amplifier analysis

Based on the discussion in chapter 1, a single ended cascode LNA topology is chosen in this thesis. The purpose for this thesis is to find a combination between transistor length, bias voltage and finger number that can increase the LNA gain, Q and decrease the NF and power consumption.

3.1 Single Ended Cascode Low Noise Amplifier

Because of its high gain and high reserve isolation, Single Ended Cascode LNA is one of the most popular topology in Nano-scale CMOS industry [27] [13]. Fig. 3.1 is the schematic diagram of a cascade inductive degenerated LNA. L_g , L_s and L_d are gate inductor, source inductor and drain inductor respectively [28]. C_b is a big blocking capacitor to prevent DC current flowing into the system. Typically, the output load of this circuit is a band-pass filter or a variable gain amplifier (VGA), which is the next stage of the LNA. The bias voltage (V_{bias}) can be implemented by an active resistor and a resistor as shown in Fig. 3.1. To connect the gate and the drain terminal together, the transistor can generate constant current. The resistance R_{ref} is used to generate the voltage. R_{bias} is a high impedance resistor, which is regarded as open circuit. In this case, there is no current flowing to the gate of M_1 ,

and the voltage generated by the M_3 and R_{ref} can provide M_1 a stable gate voltage. However, the varying sizes of the transistors and active resistors will affect the process variation. For clarity, a DC voltage is directly given to the V_{bias} in Fig. 3.1 in order to test the gate effect and process variation effect on the circuit.

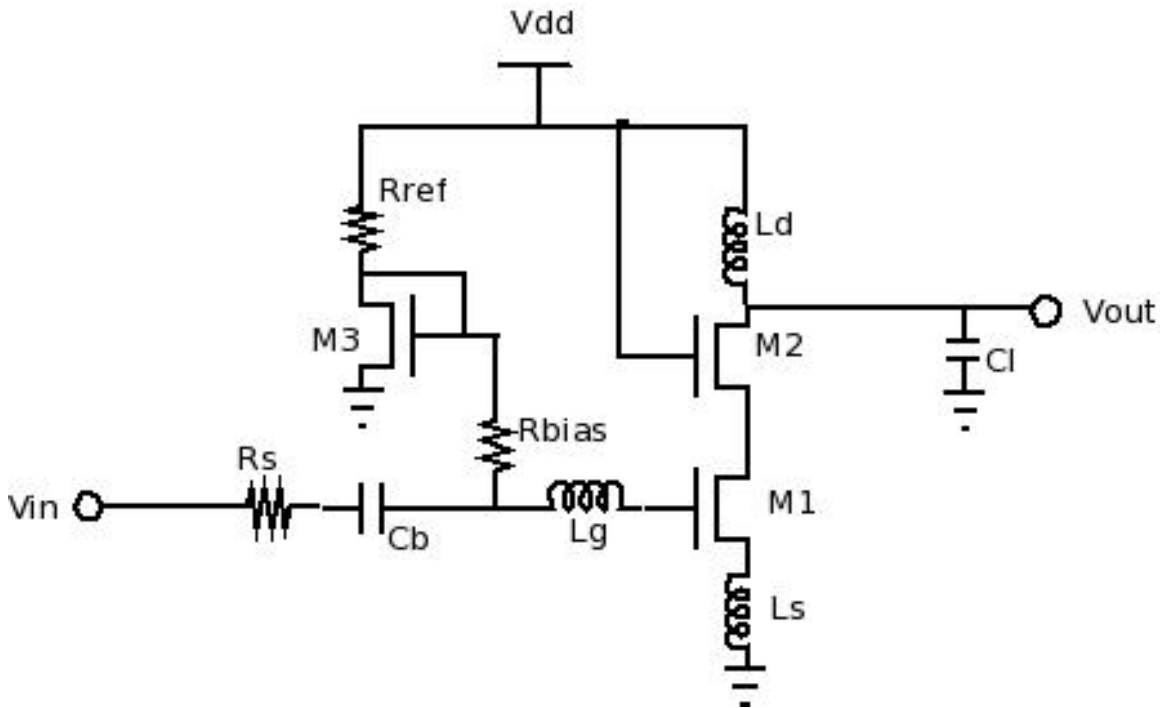


Fig. 3. 1 Single ended tuned low noise amplifier

3.1 Parameters Estimation for LNA

From theory [16] [16], a reasonable transistor width for the LNA in Fig. 3.1 can be set based on center frequency and the process parameters in Equation 3.1 and 3.2.

$$I_{ds1} = I_{ds2} \quad (3.1)$$

$$W_{opt} \approx \frac{1}{[3C_{ox}L + 4.5C_{GS0}]\omega_0 R_S} \quad (3.2)$$

I_{ds1} and I_{ds2} are currents flowing through transistors, W_{opt} is the estimated optimal width for power constraint while keeping the noise figure near the optimal value. For 2.4GHz center frequency, 125um width, 200nm and 100nm length are chosen as the width and length for transistors. For 6GHz center frequency LNA, 90 um total width, 100nm length and 48um total width, 200nm length are used.

Fig. 3.2 is the small signal equivalent circuit for the input part of the LNA in Fig. 3.1 without considering junction capacitance. 50Ω off-chip stable impedance (R_S) is considered as the input source impedance. The maximum power transmission or minimum signal reflection is obtained when the LNA input impedance matches the source impedance. L_g and L_s are the key components for impedance matching of a cascode inductive degenerated LNA. g_{m1} is the transconductance of M_1 . C_b is a big capacitor placed in front of gate. C_{gs} and C_{gd} are gate capacitances. C_{gseq} is the equivalent capacitance of gate total capacitance. The input impedance equation can be given by Equation 3.3 to 3.7:

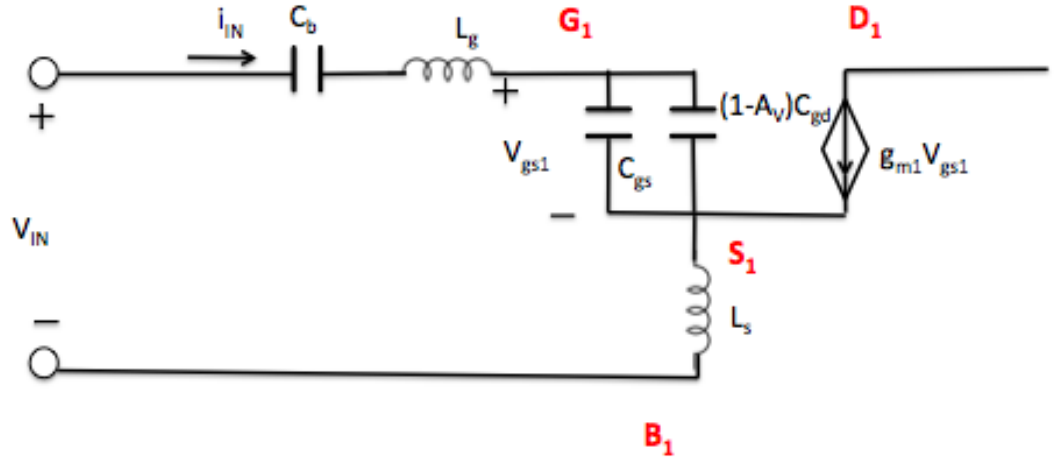


Fig. 3. 2 Small signal equivalent circuit of input circuit

Assuming the gain for M_1 transistor is -1 because it is easy to estimate the equivalent capacitance for the input circuit.

$$C_{gseq} = C_{gs} + (1 - A_V)C_{gd} \approx C_{gs} + 2C_{gd} \quad (3.3)$$

$$v_{IN} = \left[j\omega L_g + \frac{1}{j\omega C_b} + \frac{1}{j\omega C_{gseq}} \right] i_{IN} + j\omega L_s [i_{IN} + g_{m1} V_{gs1}] \quad (3.4)$$

$$V_{gs1} = \frac{i_{IN}}{j\omega C_{gseq}} \quad (3.5)$$

$$\Rightarrow V_{IN} = \left[j\omega L_g + \frac{1}{j\omega C_b} + \frac{1}{j\omega C_{gseq}} \right] i_{IN} + j\omega L_s \left[i_{IN} + g_{m1} \frac{i_{IN}}{j\omega C_{gseq}} \right] \quad (3.6)$$

$$Z_{IN} = \frac{V_{IN}}{i_{IN}} = \left\{ \left[j\omega L_g + \frac{1}{j\omega C_b} + \frac{1}{j\omega C_{gseq}} \right] + j\omega L_s \right\} + \frac{g_{m1} L_s}{C_{gseq}} \quad (3.7)$$

And the impedance matching equation is given by Equation 3.8 to 3.9:

$$R_s = \frac{g_{m1} L_s}{C_{gseq}} = 50\Omega \quad (3.8)$$

$$(L_g + L_s)\omega_0 = \frac{1}{\omega_0 C_b} + \frac{1}{\omega_0 C_{gseq}} \approx \frac{1}{\omega_0 C_{gseq}} \quad (3.9)$$

So the relationship between inductance, capacitance and impedance matching center frequency can be given as Equation 3.10.

$$L_g + L_s = \frac{1}{\omega_0^2 C_{gseq}} \quad (3.10)$$

The gate, source inductors and the capacitors from M_1 transistor affect the impedance matching center frequency together.

Additionally, the tank circuit in Fig 3.3 will resonate the center frequency to the desired value.

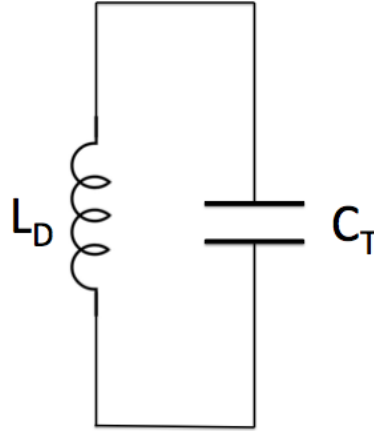


Fig. 3. 3 Tank Circuit in Single Ended LNA

From Fig 3.3, drain inductor has a big effect on f_c . The approximate small signal equivalent circuit of the LNA is given in Fig. 3.4. L_d and the total capacitance of output capacitance C_{db2} and C_L are the key factors affect the tuned center frequency. The f_c can be estimated using Equation 3.11 to 3.12.

$$f_c = \frac{1}{2\pi\sqrt{L_D C_T}} \quad (3.11)$$

$$C_T = C_{db2} + C_L \quad (3.12)$$

It can be found that f_c is proportional to $\frac{1}{\sqrt{L_D}}$ and $\frac{1}{\sqrt{C_T}}$. To meet the high frequency requirement of the f_c , a large size of the transistor width is used in this LNA design, and the finger numbers will affect the performance of the LNA.

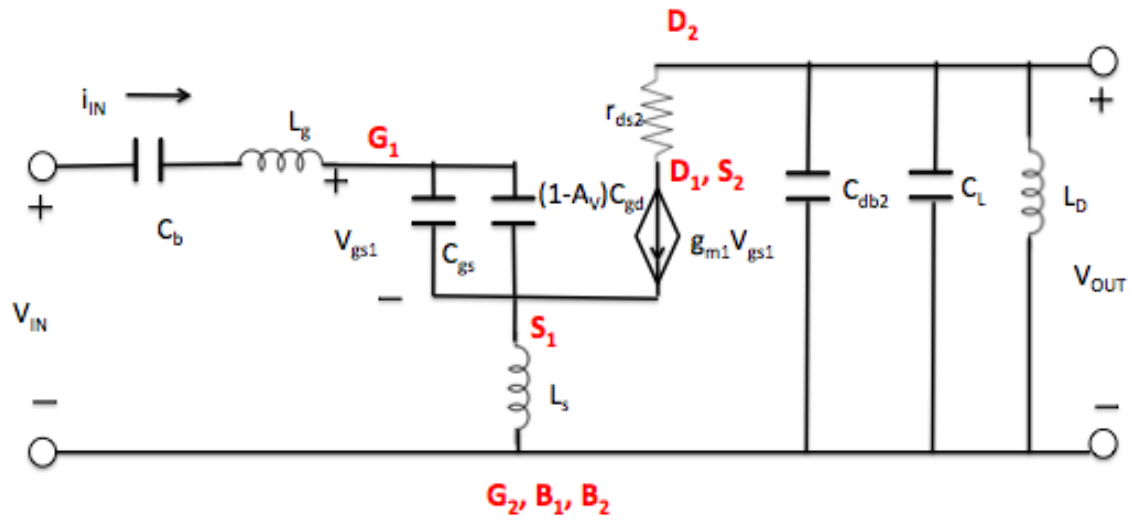


Fig. 3. 4 LNA small signal equivalent circuit

IV Circuit Analysis

The LNA in Fig. 3.1 is implemented in 90nm CMOS technology through Cadence tool. The schematic circuit is shown in Fig 4.1. A typical 1.2V power supply is used for this design. The variables can be classified into three groups: number of fingers, bias voltage and transistor channel length. f_c , voltage gain (A_V), quality factor (Q), impedance matching S-parameter (S_{11}), noise figure (NF), third-order intercept point (IIP3) and 1 dB compression point are tested under different variables.

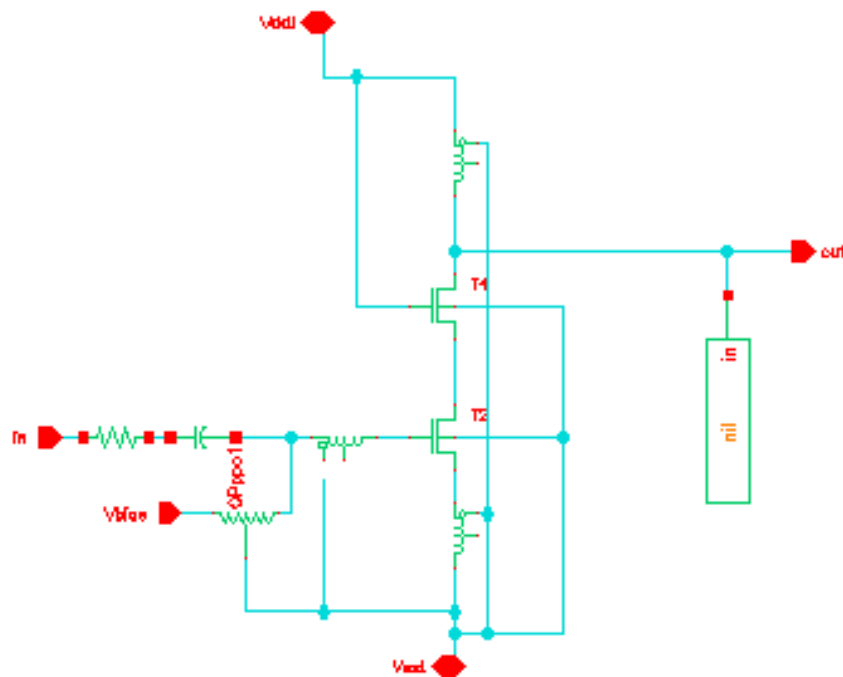


Fig. 4. 1 LNA circuit implemented by Cadence Software

4.1 2.4GHz Low Noise Amplifier

4.1.1 Number of Finger Effects on LNA

To test the performance of multiple fingers, a 0.6V bias voltage and 200nm L are set up as the gate voltage and channel length, respectively. Table 4.1 summarizes the LNA performances under different N_f and W_f with corner analysis.

Table 4. 1 LNA performance with different N_f under 125um total width and 200nm length

N_f	W_f	Corner	f_c	A_v	Q	S_{11}	NF	IIP3	1dB
1	125	tt	2.4	34.6	5.60	-41.02	1.79	-1.95	-11.39
		ss	2.392	34.12	5.73	-33.51	1.81	-2.98	-11.74
		ff	2.408	34.95	5.46	-52.59	1.77	-1.69	-11.05
20	6.25	tt	2.4	34.78	5.45	-46.43	1.78	-1.37	-10.84
		ss	2.392	34.37	5.57	-39.10	1.80	-2.11	-11.22
		ff	2.408	35.08	5.34	-35.41	1.77	-1.12	-10.39
125	1	tt	2.4	34.65	5.42	-44.30	1.77	-1.14	-10.59
		ss	2.4	34.25	5.58	-44.11	1.80	-1.90	-11.14
		ff	2.4	34.92	5.27	-36.81	1.75	-1.06	-10.05
250	0.5	tt	2.4	34.53	5.40	-37.63	1.75	-0.82	-9.99
		ss	2.4	34.15	5.57	-34.29	1.78	-1.42	-10.68
		ff	2.4	34.74	5.23	-35.06	1.73	-1.10	-9.73

As seen in Table 4.1, for the given four different per finger width, the most stable f_c is gotten when W_f are $W_f = 1\mu m$ and $W_f = 0.5\mu m$, but quality factors vary a little bit more. Noise figure, NF, basically are the same because center frequency is too small compared with f_T of four different N_f , based on f_T estimation Equation 2.16. The highest IIP3 is -1.14dBm when $W_f=0.5\mu m$. From the comparison, it

appears that 0.5um per finger width gives the LNA best performance with respect to process variation, noise figure and linearity, but the performance of 6.25um per finger width is almost as good. It has the best gain among these four finger numbers. The data in Table 4.1 shows the process variation does not affect the circuit performance much due to the large passive inductors used.

4.1.2 Bias Voltage Effects on LNA

A 6.25um fixed finger width is used to test the LNA performance at different V_{bias} because of the moderate property in N_f analysis, which can help to detect the dominant factor for a LNA.

From section 2.3, it is concluded that a larger V_{GS} and V_{DS} value can lead to a higher f_T value in a certain range. However, keep increasing the V_{bias} value cannot get a much higher f_T in this circuit because of the decreased drain voltage. The relationship between V_g and V_d is given in Equation 4.1 and 4.2 [2]. The increment of V_{GS1} will break the balance of the two currents flowing through M_1 and M_2 . If the diffusion voltage between two transistors is increased, than the current of M_1 is increasing, while M_2 current will be decreasing, this is not established. The diffusion voltage can only be decreased to keep the balance between these two transistors.

$$\frac{1}{2}\beta(V_{GS1} - V_{T1})^2(1 + \lambda V_{DS1}) = \frac{1}{2}\beta(V_{GS2} - V_{T2})^2(1 + \lambda V_{DS2}) \quad (4.1)$$

$$V_{DS1} + V_{DS2} = 1.2V \quad (4.2)$$

For a 0.6V bias voltage and the drain voltage of M_1 , V_{D1} is set to be 0.6V, then both of the transistors can get a 0.6V drain to source voltage. If increase M1 gate voltage to 0.85V, then drain voltage for M_1 is only 0.4V, which cannot keep M_1 work in saturation region. In this case, the bias voltage can not as high as wanted, there are some range for bias voltage to keep transistor working under saturation region, and 0.6V, 0.65V and 0.75V are chosen as the bias voltage. Table 4.2 summarizes the LNA simulation performance with respect to V_{bias} . Based on noise figure estimation equation (2.17), noise figure will be reduced following V_{bias} increased. But simulation results show little change on the noise figure with bias voltage increasing from 0.6V to 0.75V since drain voltages are keep decreasing.

From the corner analysis in Table 4.2, the variations affect the center frequency and gain less and less by increasing bias voltage. The center frequency has a 0.66% variation for 0.6V bias voltage case, 0.33% for 0.7V V_{bias} and 0% for 0.75V V_{bias} . Considering gain for LNA, it varies 2% for 0.6V gate voltage, 1.27% for 0.65V and 0.12% for 0.75V. All in all, the result of corner analysis is the PVT variations affect the LNA circuit slightly.

As seen in table 4.2, the highest gain and quality factor are at V_{bias} of 0.6V with $L=200\text{nm}$. And the best linearity is when $V_{bias}=0.65\text{V}$. As expected, power consumes more as V_{bias} increases.

Table 4. 2 2.4GHz LNA performance with different Gate Voltage for $W_f=125\mu\text{m}$

L (nm)	W_T (μm)	V_{bias} (V)	Power consumption (mW)	Corner	fc (GHz)	Av (dB)	Q	S11 (dB)	NF (dB)	IIP3 (dBm)	1dB compression (dBm)
200	125	0.6	6.856	tt	2.4	34.78	5.45	-46.43	1.78	-1.367	-10.84
				ss	2.392	34.37	5.57	-39.10	1.80	-2.11	-11.22
				ff	2.408	35.08	5.34	-35.41	1.77	-1.12	-10.39
		0.65	9.225	tt	2.4	34.64	5.26	-46.60	1.77	-0.84	-10.1
				ss	2.4	34.38	5.39	-33.78	1.79	-0.94	-10.57
				ff	2.408	34.82	5.15	-46.57	1.76	-1.12	-9.89
		0.75	14.35	tt	2.4	33.06	4.93	-36.41	1.77	-2.20	-9.29
				ss	2.4	33.03	5.06	-34.65	1.79	-1.79	-9.33
				ff	2.4	33.02	4.79	-36.75	1.76	-2.57	-9.33

If higher gain, higher quality factor and lower power consumption are desired, a smaller bias voltage should be used. If considering process variation, a higher bias voltage is needed with the drawback of the power consumption. This is a trade-off of the LNA circuit design.

Overall, a 0.65V bias voltage can be chosen as good performance of linearity, low power consumption, small NF and process variation.

4.1.3 Channel Length Effects on LNA

Table 4.3 summarizes two cases with 100nm transistor length of LNA design. The first one uses a 200nm length power constrained optimized width in Eq. (3.2), and the second one uses a 100nm length optimization width.

Table 4. 3 LNA performances with 100 nm transistor lengths

V_{bias}	L (nm)	W_T (um)	Power consumption (mW)	Corner	f_c (GHz)	A_v (dB)	Q	S11 (dB)	NF (dB)	IIP3 (dBm)	1dB compression (dBm)
0.75 V	200	125	14.35	tt	2.4	33.06	4.93	-36.41	1.773	-2.20	-9.29
				ss	2.4	33.03	5.06	-34.65	1.786	-1.79	-9.33
				ff	2.4	33.02	4.79	-36.75	1.763	-2.57	-9.33
	100		7.583	tt	2.4	30.39	4.41	-40.62	2.09	-0.27	-9.18
				ss	2.384	30.44	4.6	-39.30	2.11	-0.87	-9.76
				ff	2.416	30.21	4.21	-36.20	2.07	0.61	-8.71
	232	12.65	tt	2.4	27.73	4.22	-40.97	1.72	2.55	-5.22	
			ss	2.392	27.86	4.34	-28.25	1.74	2.20	-5.58	
			ff	2.416	27.49	4.11	-33.98	1.71	2.76	-5.02	

Under the same V_{bias} voltage ($V_{bias} = 0.75V$), the process variation fluctuates a lot comparing with 200nm length design. The NF of the 125um total width is larger than 2dB. The 102GHz high f_T of 100nm cannot help the LNA have a good noise performance because of the mismatch of the width. To get a better NF, a larger transistor size is used, and it has been verified that the NF of 1.72dB is smaller than 1.77dB in 200nm in table 4.2. A_v and Q also are also worse after the 100nm is used. By contrast, the linearity in 100nm length is better than 200nm. The IIP3 even goes to positive value (4.48dBm) compared with -0.84dBm.

Table 4.3 shows that the power consumption is reduced by using a smaller transistor length. A 100nm channel length LNA draws less current than the 200nm channel length LNA. From long channel theory, the current should be increased by reducing channel length. However, the current is decreased because the transistor

switching from long channel to short channel. Process gain, channel length modulation, threshold gate voltage are changed. And with a high V_{GS} , the velocity saturation effect decreases the saturation voltage (V_{DSAT}) for short channel devices, so the 100nm length transistor goes to saturation before the 200nm length transistor [29]. In this case, the current flowing through the long channel transistor is higher than the short channel transistor.

In order to optimize the NF, a larger width is employed in the LNA design. However, the increased total width adds more power to the circuit.

4.2 6GHz Low Noise Amplifier

4.2.3 Number of Finger Effects on 6GHz LNA

A 6 GHz single ended cascode LNA is also designed in 90nm, 1.2V CMOS technology with 0.6V bias voltage. The transistor widths and lengths are 90 μm and 100 nm respectively. Three different number of fingers are tested, which are $N_f=1$ ($W_f = 90\mu\text{m}$), $N_f=20$ ($W_f = 4.5\mu\text{m}$) and $N_f=90$ ($W_f = 1\mu\text{m}$). The simulation results are given in table 4.4.

From table 4.4, it can be seen that 20-finger case has the best performance of process variation, gain and quality factors. The impedance matches well for this case under different corner analysis. By varying the finger width, NF decrease with the number of finger increasing, because of the increased cut-off frequency, however, it still affects the NF performance slightly because of the high center frequency value.

Table 4. 4 6 GHz LNA performances with different N_f under 90um total width and 100nm length

N_f	W_f (um)	Corner Analysis	f_c (GHz)	A_v (dB)	Q	S_{11} (dB)	NF (dB)	1 dB (dBm)
1	90	tt	6.00	26.97	6.97	-21.89	2.34	-2.61
		ff	5.99	29.08	7.60	-26.24	2.15	-5.95
		ss	6.05	24.07	6.17	-15.60	2.67	1.12
20	4.5	tt	6.00	28.19	7.23	-50.81	2.24	-4.12
		ff	6.00	29.89	7.68	-31.56	2.10	-7.00
		ss	6.04	25.71	6.49	-23.43	2.48	-0.69
90	1	tt	6.03	27.88	6.82	-33.22	2.21	-4.35
		ff	6.01	29.55	7.25	-27.37	2.07	-6.85
		ss	6.08	25.39	6.12	-26.58	2.46	-0.98

4.2.4 Bias Voltage Effects on 6GHz LNA

As discussed in the 2.4 GHz LNA designs, bias voltage has a big effect on the LNA performance. A lower gate voltage will increase the gain, quality factor with less power consumption. The 0.6V, 0.65V and 0.75V also used in 6 GHz LNA to test the properties. Table 4.5 shows the simulation results. The testing environment is 1.2V power supply, 90um total transistor width with 20 multiple fingers ($W_f = 4.5um$) and 100nm channel length.

Table 4. 5 6.0 GHz LNA performance with different Gate Voltage

L (nm)	W_T (um)	Vbias (V)	Power consumption (mW)	Corner	f_c (GHz)	A_v (dB)	Q	S_{11} (dB)	NF (dB)	1 dB (dBm)
100	90	0.6	2.15	tt	6.00	28.19	7.23	-50.81	2.24	-4.12
				ff	6.00	29.89	7.68	-31.56	2.10	-7.00
				ss	6.04	25.71	6.49	-23.43	2.48	-0.69
		0.65	2.76	tt	6.01	29.19	7.05	-34.11	2.07	-2.61
				ff	6.02	30.23	7.30	-21.34	2.00	-5.95
				ss	6.02	27.59	6.55	-23.89	2.19	-1.12

		0.7	4.46	tt	6.00	29.82	6.64	-32.47	1.94	-8.37
		5		ff	6.04	30.21	6.81	-19.00	1.92	-7.71
				ss	5.98	29.16	6.39	-18.59	1.98	-8.73

The center frequency slightly changes for each case, and 0.65V case is the most stable one among these three. Voltage gains are increasing with bias voltage increasing. Noise figures are decreasing with the gate voltage going up. It goes down to 2 dB for $V_{bias}=0.75V$. Power consumption is the key factor affected by the bias voltage. For 0.6V and 0.65V bias voltage, the power consumption is nearly the same, however, when gate voltage changes to be 0.75V the power consumption is doubled.

4.2.5 Channel Length Effects on LNA

A 200 nm length and 48 um total width transistor is also used to design the 6 GHz LNA. The simulation results are shown in table 6.6. 1.2V power supply and 0.6V bias voltage are employed in this design. It can be seen that there is no process variation effect in the 200nm length case in corner analysis. The voltage gain has an approximate 20% enhancement compared with 100nm transistor length, and the quality factor goes up as well. The NF and 1 dB compression point have a little bit improvement compared with 100nm transistor width case. The only disadvantage of the 200nm case is the power consumption is higher than the 100nm case. Compared with the other parameters, the performance of the 200nm length is better than the 100nm. Meanwhile, even though the transistor length is doubled, the total widths of the transistors are decreased based on Eq. (3.2). At the same time,

the total area for different designs is very small compared with the inductors. In this case, the changes of the width and length affect the area slightly. The performance is much more important compared with the size.

Table 4. 6 6.0GHz LNA performances with different Length

L (nm)	W_T (um)	N_f	Vbias (V)	Power consumption (mW)	Corner	fc (GHz)	Av (dB)	Q	S11 (dB)	NF (dB)	1dB (dBm)
100	90	20	0.6	2.15	tt	6.00	28.19	7.23	-50.81	2.24	-4.12
					ff	6.00	29.89	7.68	-31.56	2.10	-7.00
					ss	6.04	25.71	6.49	-23.43	2.48	-0.69
200	48		0.6	2.69	tt	6.00	33.69	8	-30.38	2.12	-2.87
					ff	6.00	34.70	8.15	-27.76	2.09	-6.90
					ss	6.00	32.53	7.86	-33.38	2.16	0.76

V Conclusion and Future Work

The focus of this thesis is to study the performance variation caused by transistor number of fingers, bias voltage and channel length, which is detailed as following.

- Using Cadence tool, a single NMOS transistor with fixed total width is employed to evaluate the performance at different finger numbers, gate to source voltage and channel length. In order to obtain the best performance for f_T , g_m , the combination of N_f , V_{bias} and L are analyzed.
- Implement a single ended cascode LNA, which works at 2.4GHz and 6GHz separately. Based on receiver system requirement, the LNA needs low noise, low power, high gain, high Q, good impedance matching and linearity.
- Different N_f , V_{bias} and L are applied for the LNA design in order to test different performances in different situations.
- Find the best combination among N_f , V_{bias} and L that can maintain the circuit performs high gain, low power, low noise when process variation happens.

5.1 Conclusion

6GHz and 2.4GHz LNAs are designed using 90nm CMOS technology with focusing on performance improvement with regarding to finger numbers, bias voltages and channel lengths.

- 200nm channel length can increase the gain and quality factor for an LNA design compared with 100nm length. Meanwhile, the power-optimized width is decreased with increasing the channel length in 90nm process. However, the decreased width does not decrease the power consumption. For the same center frequency LNA design, 200nm length consumes more power than 100nm length under the same bias voltage. Seems the NF is better for 100nm length.
- Process variation affects the single ended LNA slightly due to the three passive inductors used. Passive components have much larger size compared with active component, and they are much more stable than the active transistors. It is hard to point out the variations affected by the finger numbers for this LNA circuit. The finger number effect can be ignored under the same bias voltage and channel length in LNA design. For single transistor analysis, under the same terminal voltages and total width with same N_f , the PVT variations affected by channel length cannot be ignored, 100nm length is more sensitive even though its f_T is much larger than wider channels.
- Bias voltages have a big effect on the power consumptions. When the gate voltage changing from 0.6V to 0.75V, the powers are nearly doubled. Noise figure decreases a little bit due to the enhanced performance of f_T . However, 2.4GHz

and 6GHz are relatively low frequencies compared with 60GHz, the cut-off frequency.

5.2 Future Work

Future work includes:

- 1) Study process variation effects on other blocks of a receiver chain system.
- 2) Explore some other solutions, such as variation detection to mitigate process variation effect
- 3) Finish layout of the studied LNAs and see how process variation affects the layout performance.

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