Fully Monolithically Integrated X-Band Amplifiers with Frequency Selective Feedback

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Stefan Gerlich

geboren am 23.02.1982 in Cottbus (Deutschland)

Gutachter: Prof. Dr.-Ing. Georg Böck (TU Berlin)

Gutachter: Prof. Dr.-Ing. Matthias Rudolph (BTU Cottbus-Senftenberg)

Gutachter: Prof. Dr. techn. Peter Weger (BTU Cottbus-Senftenberg)

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Abstract

The thesis addresses the design of monolithically integrated radio frequency amplifiers for X-band applications. The focus is on low-voltage low-noise amplifiers and efficient power amplifiers with high output power level. The challenge here is to realize stable amplifiers with remarkable performance metrics at low supply voltages. The general approach for stabilization amplifiers in the above frequency range is the use of a cascode topology which, however, requests higher supply voltages then single transistor operation. By using a special passive frequency-selective feedback, the use of the cascode topology could be avoided, and the amplifiers are stabilized over the entire frequency spectrum. Simultaneously, this feedback is used to neutralize the intrinsic feedback of the transistor at operating frequencies. As a result, a frequency dependent performance degeneration of the transistor can be mitigated.

This work describes the influence of the passive frequency-selective feedback. Its usage as well its limitation are explained using the examples of a realized low noise amplifier and different power amplifiers. Further, the design of radio frequency amplifiers at X-band frequencies that employs silicon-germanium heterojunction bipolar transistors is described. All amplifiers were either incorporated in a 0.25 µm SiGe:C BiCMOS technology or in a 0.35 µm SiGe:C bipolar technology.

The main achievements of this work include:

- A 8.7 GHz narrow-band low noise amplifier incorporated in a 0.35 µm SiGe bipolar technology. The noise figure is 2.2 dB and the gain 28 dB at a supply voltage of 3 V [Gerlich 12]. The low noise amplifier was subsequently used for a design of a double-balanced I/Q mixer.

- Two packaged high efficient power amplifiers operating at a center frequency of 12 GHz. They are incorporated in a 0.35 µm SiGe bipolar technology. One amplifier uses a transformer-based output matching network and achieves 30.9 % of power-added efficiency and 23.9 dBm of maximum output power at a supply voltage of 1.8 V. The second amplifier utilizes an LC-balun for impedance matching at the output and a power-added-efficiency of 38 % at 1.8 V is measured. The maximum output power was 23.4 dBm. [Gerlich 13].

- A power amplifier in a 0.35 µm SiGe bipolar technology that uses power

combining techniques to achieve 30 dBm (1 W) and 30 % of power-added efficiency at 10 GHz and 2 V supply voltage.

- Two power amplifiers, incorporated in a 0.25 µm SiGe:C BiCMOS technology, demonstrating the capability of a non-advanced SiGe process to be used for radio frequency power applications. Power combining techniques, the use of the passive frequency-selective feedback and layout optimization enables the realization of power amplifiers which exhibit an output power of 30 dBm and a power-added efficiency of 35 % at supply voltages lower as 2.6 V.

Zusammenfassung

Die Dissertation beschäftigt sich mit der Entwicklung von monolithisch integrierten Hochfrequenzverstärkern für X-Band Anwendungen. Der Schwerpunkt liegt dabei auf rauscharmen Niederspannungs-Verstärkern und effizienten Leistungsverstärkern mit hoher Ausgangsleistung. Die Herausforderung hierbei ist es stabile Verstärker mit markanten Leistungswerten bei niedrigen Versorungsspannungen zu realisieren. Der allgemeine Ansatz zur Stabilisierung von Verstärkern im genannten Frequenzbereich erfolgt über die Verwendung einer Kaskode, welche jedoch höhere Versorungsspannung benötigt als der Einsatz eines einzelnen Einzeltransistor.

Durch den Einsatz einer speziellen passiven frequenzselektiven Rückkopplung konnte die Verwendung einer Kaskoden-Topologie vermieden werden und die Verstärker werden über das gesamte Frequenzspektrum stabilisiert. Gleichzeitig ermöglicht die eingesetzte Rückkopplung eine Neutralisierung der intrinischen Rückkopplung des Transistors. Infolgedessen kann die frequenzbedingte Leistungsverschlechterung des Transistors abgeschwächt werden.

Diese Arbeit beschreibt den Einfluss der passiven frequenzselektiven Rückkopplung. Ihre Verwendung als auch ihre Anwendungsgrenzen werden anhand eines realisierten rauscharmen Verstärkers und verschiedenen Leistungsverstärkern erklärt. Weiterhin wird der Entwurf von Hochfrequenzverstärkern für X-Band Frequenzen erläutert, die Siliciumgermanium Heterostruktur-Bipolartransistor verwenden. Alle Verstärker wurden entweder in einer 0.25 µm SiGe:C BiCMOS-Technologie oder in einer 0.35 µm SiGe:C Bipolar-Technologie realisiert.

Wichtige Ergebnisse, die in dieser Arbeit enthalten sind:

- Ein 8.7 GHz schmalbandiger rauscharmer Verstärker, welcher in einer 0.35 µm SiGe Bipolar-Technologie gefertigt wurde. Die Rauschzahl beträgt 2.2 dB und die maximale Verstärkung 28 dB bei einer Versorgungsspannung von 3 V [Gerlich 12]. Dieser Verstärker wurde im Anschluss für das Design eines doppelt-symmetrischen Mischers verwendet.

- Zwei hoch effiziente und gehäuste Leistungsverstärker, welche bei einer Mittenfrequenz von 12 GHz betrieben werden. Sie wurden in einer 0.35 µm SiGe Bipolar-Technologie realisiert. Ein Leistungsverstärker verwendet als Ausgangsanpassnetzwerk einen Transformator und erreicht einen Leistungswirkungsgrad von 31.5 % und eine Ausgangsleistung von 23.9 dBm bei einer

Versorungsspannung von 1.8 V. Der zweite Verstärker verwendet zur Impedanzanpassung einen LC-Balun am Ausgang und es wurde ein Leistungswirkungsgrad 37.9 % bei 1.8 V gemessen. Die maximale Ausgansleitung betrug 23.4 dBm [Gerlich 13].

- Ein Leistungsverstärker in einer 0.35 µm SiGe Bipolar-Technologie welcher durch Leistungskombinierung eine Ausgangsleistung von 30 dBm (1 W)und einen Leistungswirkungsgrad von 30 % erreicht. Die Versorgungspannung liegt bei 2 V.
- Zwei Leistungsverstärker, gefertigt in einer 0.25 µm SiGe:C BiCMOS-Technologie, demonstrieren die Möglichkeit einen weniger fortschrittlichen SiGe--Prozesses für Hochfrequenz-Leistungsanwendungen zu verwenden. Leistungskombinierung, die Verwendung der passiven frequenzselektiven Rückkopplung und Layoutoptimierung ermöglichten die Realisierung von Leistungsverstärkern mit 30 dBm Ausgangsleistung und einem Leistungswirkungsgrad von 35 % bei Versorgungsspannungen unter 2.6 V.

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
Balun	Balanced-Unbalanced
BJT	Bipolar Junction Transistor
BVCEO	Breakdown Voltage Collector-Emitter with Open base
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DAC	Digital-to-Analog Converter
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HBT	Heterojunction Bipolar Transistor
HF	High Frequency
IoT	Internet of Things
IF	Intermediate Frequency
IM3	Intermodulation Product 3rd Order
IP3	Intermodulation Intercept Point 3rd Order
ISM	Industrial, Scientific and Medical
LNA	Low Noise Amplifier
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integraded Circuit
OFDM	Orthogonal Frequency-Division Multiplexing
PA	Power Amplifier
PAE	Power-Added Efficiency
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PFSF	Passive Frequency-Selective Feedback
QAM	Quadrature Amplitude Modulation
Radar	Radio Detection And Ranging
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SGP	SPICE Gummel-Poon
Si	Silicon
SiGe	Silicon-Germanium
SNR	Signal-to-Noise Ratio
VBIC	Vertical Bipolar Inter-Company
WLAN	Wireless Local Area Network

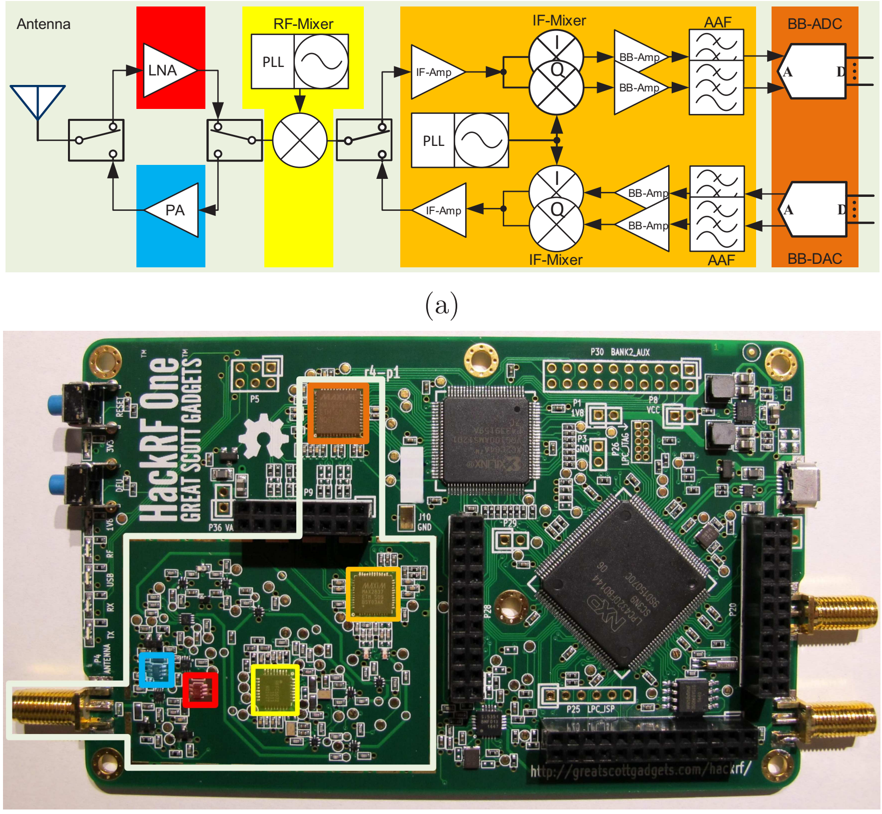
Chapter 1

Introduction

Wireless technologies enable applications nowadays that would have been impossible years ago. Started with simple text messages and ordinary phone calls, the mobile phone is able today to receive information with a peak data rate of 1 Gbit/s. Video calls or online streaming of high definition medias are today everyday features. A similar evolution can be observed for wireless local area networks (WLAN). The first published standard, IEEE 802.11-1997, defined a net data rate of 2 Mbit/s in the industrial, scientific and medical (ISM) frequency band at 2.4 GHz. The latest published standard that is used nowadays commercially, IEEE 802.11ac, provides a data rate of almost 1300 Mbit/s at 5 GHz. Furthermore, the new IEEE 802.11ad WLAN standard for short-range networks uses the 60 GHz band and allows data rates of up to 6930Mbit/s. The presented performance increase of mobile communication and WLAN are only two examples but can be applied to almost every wireless application.

Besides improving existing wireless applications, new applications emerge. Internet of Things (IoT),the predicted great future economic sector, should provide a comprehensive network for almost every conceivable object. Washing machines, dryers, cars, transportation systems, medical systems, even whole buildings, will be able to communicate automatically and share their information by embedded sensors and wireless communication interfaces [Porkodi 14]. Along with this concept is the development of wireless energy harvesting systems, that is to use ambient radio frequency (RF) energy or dedicated wirelessly transmitted RF energy as device power source [Soyata 16]. The charging of device battery or the operating of the device will become spatial independent of a wired power infrastructure. These given examples are only a fraction of today's and future wireless application and could be further expanded by numerous examples in the fields of radio detection and ranging (radar) or millimeter-wave imaging.

Despite all these different applications, almost all wireless RF systems have in general a common transceiver – transmitter and receiver as one component – architecture to operate at radio frequencies. An example for such a transceiver



(a)

(b)

Figure 1.1: State-of-the-art wideband transceiver, (a) – simplified block diagram of a heterodyne transceiver, (b) – Implemented transceiver on a printed circuit board (photograph by wdwd, distributed under a CC-BY-SA 4.0 license)

architecture is given in Fig. 1.1. The block diagram of Fig. 1.1(a) shows a heterodyne transceiver for a state-of-the-art wideband transceiver system. The implementation of the transceiver on a printed circuit board (PCB) is depicted in 1.1(b) and framed by white lines. As seen by the colored areas in 1.1(b) and the corresponding colored subsystems in the transceiver's block diagram, most functions are realized as single chip solution. For example, the intermediate frequency- (IF) mixer incorporates additionally amplifiers, filters and a frequency synthesizer, next to the mixer itself.

The situation is different in the case of the low noise amplifier (LNA) and power amplifier (PA). As seen in the block diagram, the LNA is the first amplifying device in the receiver path, the PA the last amplifying device in the transmitter path. The performance of the devices will be therefore substantially affect the overall performance of the transceiver [Luzzatto 07]. The gain and noise contribution of the LNA will define the receiver's sensitivity. The maximum output power of the PA will have a major influence on the radiated signal strength. Its efficiency will mainly determine the overall system efficiency, as power amplifiers consume most of the system power. Further, power amplifiers require a significant portion of the chip area due to large transistors and matching networks. The result would be higher overall costs because of the larger transceiver chip area.

As consequence of this outstanding status in a transceiver system, low noise amplifiers and power amplifiers need to be designed application-specific and are implemented as individual components in a transceiver. In the example of the wideband transceiver in Fig. 1.1, the general-purpose RF mixer is incorporated in a silicon (SI) complementary metal oxide semiconductor (CMOS) process that is only conditionally suitable for LNAs and PAs operating in a wideband transceiver system. Instead, a individual low noise amplifier and power amplifier based on a gallium arsenide semiconductor technology are used that present a superior performance relative to Si-CMOS based amplifiers.

This example should illustrate that the design of LNAs and PAs has a decisive influence on the performance of transceivers. Although they are only one component of the transceiver, their characteristics determine significantly the overall system.

The thesis focuses on X-band power amplifiers and low noise amplifiers operating in the frequency range between 8 GHz and 18 GHz. Main applications in these frequency bands are phased-array radar systems, e.g. weather radar, air traffic control, missile defense systems, and satellite communication system, as commercial satellite broadcast or military communication systems. All of these applications are operating with long range signals. Therefore, an LNA should provide high gain to amplify weak signals and contribute less noise as possible for a high sensitivity. On the other hand, a PA should deliver a high output power for sufficient signal levels. Further, power amplifiers operating in phased-array radar systems, needs to be very efficient. Since numerous PAs are combined in such radar system, the overall efficiency will be determined by the power amplifiers' efficiency, and thus, determine the operating costs.

1.1 Thesis Motivation

At first glance, wide-bandgap compound semiconductors appear to be the first choice for X-band power amplifiers and low noise amplifiers. Monolithic microwave integrated circuit (MMIC) power amplifiers are reported that deliver output power levels of 41 dBm and more [Resca 14][Kikuchi 14]. The given efficiency reaches values of 50 % and more [Watanabe 13][Schafer 13] at X-band frequencies. Low noise amplifiers with comparable to SiGe LNAs noise performance but superior input robustness [Schuh 13] and linearity [Andrei 12] were demonstrated.

Despite the obvious advantage in the use of compound semiconductor technologies, they are at the moment not economically competitive to SiGe technologies in terms of fabrication costs and yield [Komiak 15]. Another major drawback is the missing possibility to integrate monolithically complete transceivers as MMIC in such technologies. Only transceiver front ends – PA, LNA and switches – were reported [Masuda 12].

By contrast, monolithically integrated X-band transceivers are feasible in silicon germanium technologies [Liu 16]. Furthermore, the integration of a SiGe process into a Si-CMOS technology (BiCMOS) allows to realize mixed-signal MMIC transceivers that incorporate digital interfaces, e.g. analog-digital conversion. Such a MMIC transceiver in a 0.13 µm BiCMOS technology is presented in [Yu 14]. Therefore, the research in the field of SiGe power amplifiers and low noise amplifiers is still reasonable.

One challenge in the design of SiGe PAs and LNAs for X-band applications is the RF performance of a silicon-germanium heterojunction bipolar transistor (SiGe-HBT) in terms of gain. An inevitable trade-off between its breakdown voltage characteristics and high frequency gain is given by the transistor's physical structure. The properties caused by this physical structure is expressed, among other things, in the transit frequency (f_t) and maximum oscillation frequency (f_{max}) of the transistor and is related to the frequency-dependent transistor gain. That is, the higher the frequencies f_t and f_{max}, the higher is the gain at frequencies below. To realize such a so-called high-speed transistor, the transistor's base region should be very thin and the collector should be highly doped. On the other hand, a thin base region and highly doped collector result in low breakdown voltages and limit the maximum collector-emitter operating voltage to low values. For example, the SiGe-HBT of a 0.13 µm BiCMOS technology has a transit frequency of $f_t = 300\,\text{GHz}$ and maximum oscillation frequency of $f_{max} = 500\,\text{GHz}$ [Fischer 13]. The limiting collector-emitter breakdown voltage measured with open base (B_{VEO}) is only 1.7 V.

Power amplifiers at X-band frequencies require high-speed SiGe-HBTs to provide sufficient gain. This also means that the maximum output power is limited by the low usable voltage level. As power is the product of voltage and current, one suitable possibility to increase the output power is to increase the current by an enlarged emitter area.

A similar situation is given for SiGe low noise amplifiers. High-speed SiGe-HBTs are needed to provide high gain at at X-band frequencies but the challenge is not the low breakdown voltages but the high base sheet resistance. As previously mentioned, the characteristic frequencies f_t and f_{max} are also increased by thinning the base region. As a result, the base sheet resistance is increased and as a major source of noise in a transistor, the overall noise performance of the LNA will be thereby degraded. As in the case of the PAs, one solution is to combine numerous transistors in parallel. This will reduce the overall base sheet resistance of the LNA and allows to maintain the bias current of the single transistor at same level of performance.

Despite the simplicity of parallel combining individual transistors, it causes new difficulties in the design of PAs and LNAs. The input and output impedances become smaller, and thus, the requirements on on-chip matching networks are increased. The metal trace width of interconnections must be increased in order to avoid violations of the maximum current density rules of the technology. The result of wider metal traces are increased parasitic capacitances that degrade the overall efficiency of the amplifier.

Another major issue the stability. Considered as one large transistor, parallel connected transistors have the tendency to become unstable. The intrinsic base-collector capacitance of the transistor causes a feedback that enables the transistor to oscillate under certain conditions [Cripps 06].

By usage of the external passive frequency selective feedback, it becomes possible to realize power amplifiers and low noise amplifiers at low supply voltages. Despite numerous parallel combined individual transistors, they are stable of the entire frequency spectrum. Furthermore, the external feedback mitigates the frequency-dependent gain degradation of the transistors by neutralization of the base-collector capacitance at working frequencies. Although the feedback is known from the literature, it was never before used for stabilizing and neutralizing simultaneously.

1.2 State-of-the-Art

The Fig. 1.2 shows the maximum output power and power-added efficiency (PAE) of the most considerable reported X-band SiGe power amplifiers. Power amplifiers that have been contributed by this work are highlighted in red. It is obvious that PAs with high efficiency only demonstrate a moderate output power level. On the other hand, power amplifiers with output power levels near 1 W (30 dBm) have an efficiency lower then 20 %. The challenge of this work was now to develop stable power amplifiers that are more efficient at moderate and high output power levels. Additionally, it should be attempted to achieve a higher output power than previously reported. As shown by the highlighted results in Fig. 1.2, the contributed PAs have leading positions.

An overview of most considerable reported X-band SiGe low noise amplifiers is given in Tab. 1.1. The LNA of this thesis is highlighted in red. Although the performance of some LNAs are better relative to the red marked one, it should be noted that most LNAs are measured on-chip. The low noise amplifier presented in this thesis was bonded onto a substrate, and the performance including all parasitics, e.g. transmission lines or bond wires, was evaluated. Nevertheless, it is apparent from Tab. 1.1 that a high gain could be achieved at low power dissipation compared to other stated amplifiers. Also the value of the noise figure (NF) is comparable to other reported LNAs.

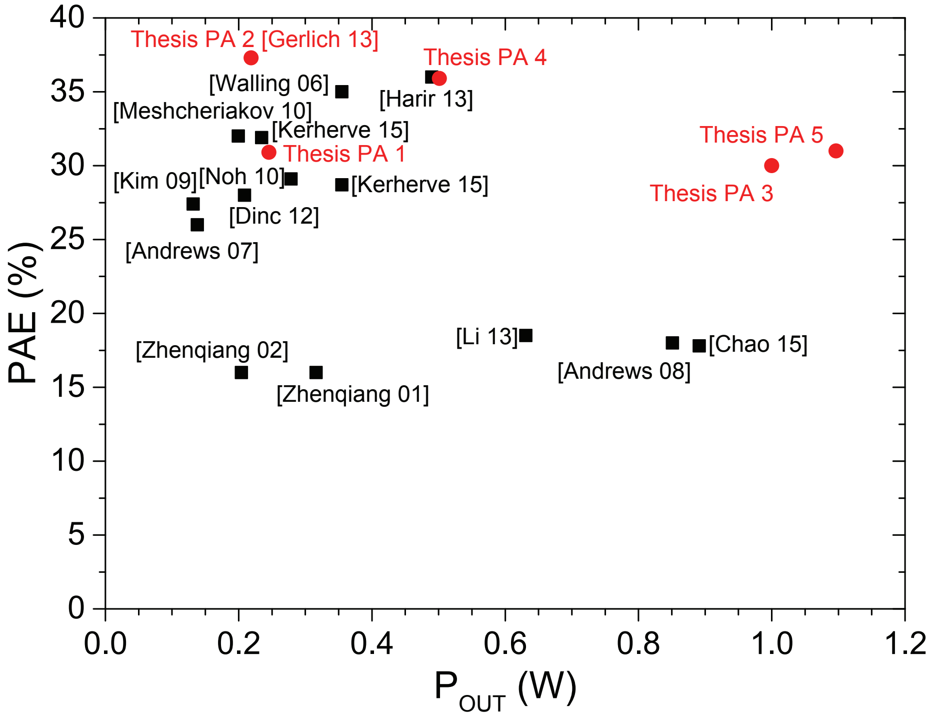


Figure 1.2: Maximum output power as function of efficiency of most considerable X-band SiGe power amplifiers

Table 1.1: Performance of most considerable X-band SiGe low noise amplifiers

Reference	Frequency range (-3dB) (GHz)	Gain$_{max}$ (dB)	NF (dB)	Supply voltage (V)	Power dissipation (mW)	Chip area (mm)^2
[Kuo 06]	8-12	20	1.2	2.5	15	0.73 × 0.72
[Nakajima 07]	8-12	21	4.6	1	3.3	19.1 × 0.63
[Thrivikraman 09]	9.3-11.3 (±0.5 dB)	30	2	5	285	1.6 × 1.1
[Howard 10]	3.4-15.8	21.3	4.2	3.3	116	1.06 × 0.09
[Chartier 10]	1-11	21	2.5	5	70	0.27 × 0.37
[Chartier 10]	1-11	33	2.9	3	78	0.34 × 0.46
[Gerlich 12]	8.43-9.11	28.1	2.2	3	28.5	0.93 × 0.7
[Kalyoncu 12]	8.5-11.5	27	1.6	4	115	1.3 × 0.9
[Poh 12]	8-12	8.5	3.1	0.5	2	0.75 × 0.75
[Dinc 12b]	8-12	21	1.52	2.2	22	0.62 × 0.82
[Schmid 14]	8-12	16.5	1.6	–	19.9	0.8 × 0.9
[Kanar 14]	6.4-11	24.2	1.2	1.8	32.8	0.68 × 0.68
[Davulcu 15]	6.4-11	15	2.7	–	23.1	0.73 × 0.84

1.3 Thesis Organization

The second chapter provides an introduction into preliminary considerations to X-band power amplifiers and low noise amplifiers. Important performance metrics of PAs and LNAs are presented and the most common circuit topologies are presented. The presentation of the two SiGe technologies used to realize the amplifiers of this thesis concludes the second chapter. The basic concept of bandgap engineering is shown and the modeling if SiGe HBTs in both technologies is shown. Furthermore, the selection of a suitable transistor for RF amplifiers is depicted and the passive components models of both technology are shown.

In Chapter 3 the passive frequency-selective feedback is introduced. First, sources of instability in X-band amplifiers are presented. Subsequently, the focus on the intrinsic transistor feedback by the base collector capacitance and its influence of the amplifier's stability is discussed followed by the explanation of the frequency selective feedback and its influence on the circuit performance.

The design of two high efficient and packaged power amplifiers is given in the fourth chapter. As one PA utilize a transformer-based output matching network and the second a LC-Balun, both matching concepts are presented. Subsequently, a power combined PA is presented which is based on packaged transformer PA. The chapter concludes with the presentation of two power amplifiers that incorporated in a non-advanced SiGe technology but demonstrate the capability to use such technologies for the design of RF power amplifiers.

A narrow-band 8.7 GHz low noise amplifier is presented in Chapter 5. The circuit design is shown and the general noise performance of the transistor is shown. The integration of the LNA into a mixer design and the presentation of experimental results conclude the chapter.

Finally, Chapter 6 concludes the thesis with a conclusion and outlook.

Chapter 2

Preliminary Considerations to X-Band Amplifiers

The following chapter provides preliminary considerations to X-band amplifiers. Typical amplifier performance metrics, as power gain or efficiency, are explained. The technology frameworks of two SiGe technologies is presented and the basic idea behind bandgap engineering is depicted in this chapter. Furthermore, the selection of a suitable transistor and different amplifier classes and topologies are given.

2.1 Performance Metrics

The performance evaluation of power amplifiers and low noise amplifiers is done by various performance metrics. They indicate the maximum performance capability and characterize amplifiers under different operating conditions. As some metrics are application specific, only general metrics for the performance evaluation of LNAs and PAs will be presented.

2.1.1 Power Gain and Efficiency

The given power metrics are derived by an simplified block diagram of a general radio frequency amplifier in Fig. 2.1. A source, characterized by the impedance Z_S and AC voltage source V_S, drives the amplifier through an input matching network (IMN), which transform the source impedance to the optimal operating input impedance Z_{IN} of the amplifier. The amplified output signal is delivered to a load, denoted as impedance Z_L. An impedance transformation of the load impedance to the amplifiers output is realized by the output matching network (OMN).

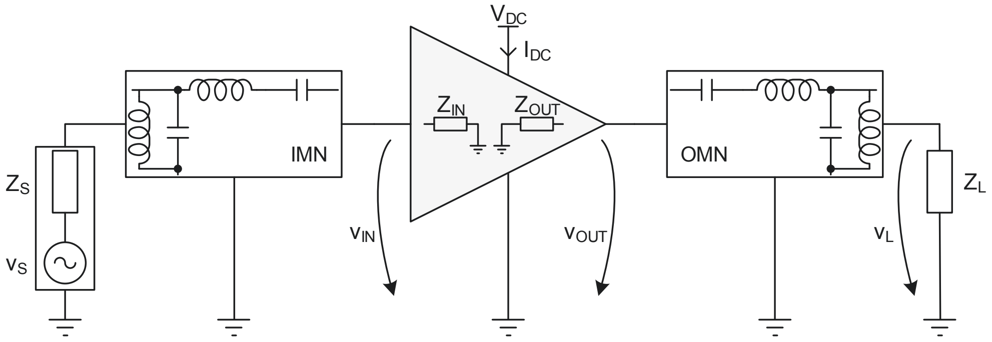


Figure 2.1: Generalized block diagram of a amplifier circuit

Power Gain

For sine wave signals, the relation between an output power and input power of an amplifier circuit can be calculated by three different kinds of gain:

- Operating power gain G_P: The relation between the delivered power to the load impedance P_L and the input power of the amplifier P_{IN} is the operating power gain:

$$G_P = \frac{P_L}{P_{IN}} = \frac{\frac{|v_L|^2}{2\Re\{Z_L\}}}{\frac{|v_{IN}|^2}{2\Re\{Z_{IN}\}}} = \frac{|v_L|^2}{|v_{IN}|^2} \frac{Re\{Z_{IN}\}}{Re\{Z_L\}} \tag{2.1}$$

  The operating power gain is independent of the source impedance. It is therefore useful in the design of bilateral devices, as the design of the output matching network can be realized without a disturbing unmatched input impedance.

- Avaible power gain G_A: The power gain G_A is a function of the output power of the amplifier P_{OUT} to the available source power P_S:

$$G_A = \frac{P_{OUT}}{P_S} = \frac{\frac{|v_{OUT}|^2}{2\Re\{Z_{OUT}\}}}{\frac{|v_S|^2}{8\Re\{Z_S\}}} = 4\frac{|v_{OUT}|^2}{|v_S|^2} \frac{Re\{Z_S\}}{Re\{Z_{OUT}\}} \tag{2.2}$$

  As only the output power of the amplifier is considered and not the power at the load, G_P is suitable for calculations in low noise amplifier design. The optimal noise impedance match at the input of the LNA can be therefore determined by the assumption of a perfectly matched output.

- Transducer power gain G_T: The transducer power gain is defined as the ratio of the output power at the load to the source power.

$$G_T = \frac{P_L}{P_S} = \frac{\frac{|v_L|^2}{2\Re\{Z_L\}}}{\frac{|v_S|^2}{8\Re\{Z_S\}}} = 4\frac{|v_L|^2}{|v_S|^2}\frac{Re\left\{Z_S\right\}}{Re\left\{Z_L\right\}} \tag{2.3}$$

The transducer power gain takes the losses in both matching networks into account. Therefore, the power gain of the complete amplifier circuit is evaluated by G_T.

The power levels and gains of an amplifier can comprises several order of magnitudes. It is therefore useful and common to use a logarithmic scaling and to scale the power to the power of 1 mW:

$$P_{dbm}\left[dBm\right] = 10\log\left(P_{lin}\left[W\right]\cdot 1000\right) \tag{2.4}$$

The logarithmic scaling of power gains is given by the following equations:

$$G_{db}\left[dB\right] = 10\log\left(G_{lin}\right) \tag{2.5}$$

$$G_{db}\left[dB\right] = 10\log\left(\frac{P_{lin,2}}{P_{lin,1}}\right) \tag{2.6}$$

$$G_{db}\left[dB\right] = P_{dbm,2} - P_{dbm,1} \tag{2.7}$$

Efficiency

The efficiency of radio frequency amplifiers is of vital importance. In particular, power amplifiers will consume a large amount of system power in transceiver and transmitters. Thus, their efficiency will primarily determine the overall system efficiency. Further, phased array applications combine numerous power amplifiers to drive the antenna array. It is obvious in this case that low efficient PAs will dissipate a significant amount of heat which is taken away by cooling systems. The other way around, the use of highly efficient power amplifiers enables to lower the requirements on cooling systems, and therefore, save operating costs.

As in the case of power gain, different kinds of definition for the amplifier's efficiency exist:

- Collector efficiency η: The ratio of output power to applied DC power is defined as collector efficiency:

  $$\eta = \frac{P_L}{P_{DC}} = \frac{P_L}{V_{DC}I_{DC}} \tag{2.8}$$

  As the collector efficiency does not take the input power into account, the value of η for amplifiers can be misleading. The output power of low gain amplifiers with high collector efficiencies will be mostly provided by the input power and not by the amplifier itself.

- Power-added efficiency PAE: The power added efficiency takes into account that some amount of output power is not provided by the amplifier itself but from the input power. Therefore, only the amount of output power added by the amplifier is considered to evaluate the efficiency:

  $$PAE = \frac{P_L - P_{in}}{P_{DC}} = \eta \left(1 - \frac{1}{G_P}\right) \tag{2.9}$$

  It is seen from (2.9) that the power-added efficiency of high gain amplifiers is close to the collector efficiency The power-added efficiency is the most common metric for the amplifier efficiency.

- Overall efficiency η_{ov}: Although rarely used in the context of RF amplifiers, the overall efficiency comprises the general physical definition of efficiency as it relates the output power to the overall input power of the amplifier:

  $$\eta_{ov} = \frac{P_L}{P_{DC} + P_{in}} = \frac{P_L}{P_{DC} + \frac{P_L}{G_P}} \tag{2.10}$$

  The definition of PAE in (2.9) is physically not impeccable. Although the gain of amplifiers should be greater than unity, gain values smaller than unity results in a negative power-added efficiency, which has no physical meaning. Only the definition of the overall efficiency results in all circumstances in a meaningful solution.

All given definitions for the efficiency use instantaneous power levels. In the case of complex modulated signals with time-varying amplitudes, it is more suitable to evaluate the efficiency by an average efficiency:

$$\overline{\eta} = \frac{\overline{P_L}}{\overline{P_{DC}}} \tag{2.11}$$

The average output power $\overline{P_L}$ and DC power $\overline{P_{DC}}$ is derived from their probability density functions [Raab 03].

2.1.2 Nonlinearty

Many high frequency applications require linearly amplifying amplifiers because they employ modulation schemes with time-varying envelopes. That means, the output signal of the amplifier needs to be a undistorted replica of the input signal. A distortion of the output signal does not only results in a loss of information but also generates additional frequency components in the output signal spectrum.

The nonlinearity of an amplifier is the results of the exponential transfer function of the transistor. Thus, the transfer function of a memoryless amplifier can be described by a power series, wherein s_{out} denotes the output signal and s_{in} the input signal [Colantonio 09]:

$$s_{out}\left(t\right) = a_1 s_{in}\left(t\right) + a_2 s_{in}\left(t\right)^2 + a_3 s_{in}\left(t\right)^3 + ... + a_N s_{in}\left(t\right)^N = \sum_{1}^{\infty} a_n s_{in}\left(t\right)^n \quad (2.12)$$

Assuming a sinusoidal input signal with the amplitude A:

$$s_{in}\left(t\right) = A\cos\left(\omega t\right) \quad (2.13)$$

and using (2.13) in (2.12), s_{out} is given by using trigonometric transformations, reordering and truncation from the fourth order to:

$$s_{out} = \frac{1}{2}a_2A^2 + \left(a_1 + \frac{3a_3A^3}{4}\right)\cos\left(\omega t\right) + \frac{1}{2}a_2A^2(2\omega t) + \frac{1}{4}a_3A^3(3\omega t) \quad (2.14)$$

Instead of a single frequency component, the output spectrum consists of the fundamental frequency at ω and harmonics at n^{th} multiples of the fundamental. Following conclusions can be made from (2.14):

- For small amplitudes of s_{in}, the harmonics can be neglected and the gain is defined by a_1, the small signal gain. The amplifier is in linear operation.
- An increasing amplitude A leads to variation of the gain at the fundamental by $3a_3A^3/4$. In most cases the value for a_3 is negative, and as consequence, the gain decreases with an increasing input signal strength known as gain compression. The reverse case, gain expansion, is also observable. Especially weakly or non biased transistors show gain expansion before the gain compresses [Zhang 05]. When gain compression or expansion starts to occur, the amplifier goes into saturation.
- The amplitude of the n^{th} harmonic increases by approximately A^n for small input signal strengths.

1 dB Compression Point

The distinction between linear operation and the beginning of amplifier saturation is done at the 1 dB compression point. It is defined as the input power level (IP1dB) at which the gain is dropped by 1 dB, depicted in Fig. 2.2. The related output power (OP1dB) is calculated by the small signal G to:

$$OP1dB\left[dBm\right] = IP1dB\left[dBm\right] + G\left[dB\right] - 1\,\mathrm{dB} \quad (2.15)$$

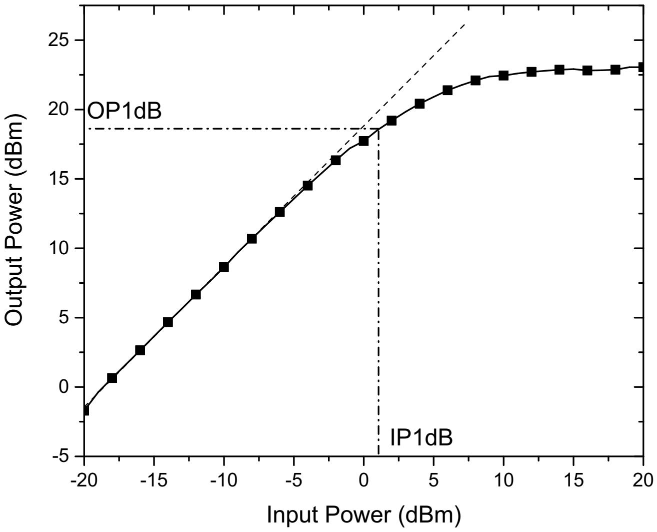


Figure 2.2: Output power as function of the amplifier's input power to determine the input and output 1 dB compression point

Third Order Intercept Point

The presented 1 dB compression point is used to evaluate the linearity of an amplifier with a single tone excitation. This test scenario will not reflect the real case of amplifier applications if they will operate with bandwidth-limited signal instead of a signal at one frequency. Therefore, to consider the linearity of an amplifier with more than one input signal, a two-tone excitation is used.

The measurement setup is shown in Fig. 2.3. Two signals with equal amplitude, $s_{in,1}$ and $s_{in,2}$, are generated by signal sources and combined in a power combiner. The frequency difference between $s_{in,1}$ and $s_{in,2}$ should be much smaller than the signal frequency but large enough to be measured by the spectrum analyzer. To avoid measurement errors through mismatching, attenuators are used to ensure a 50 Ω impedance match between each stage.

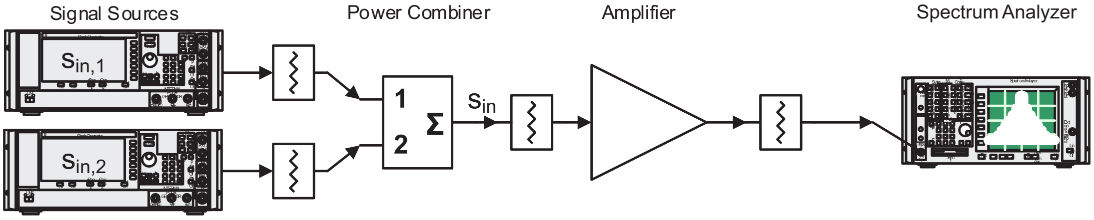


Figure 2.3: Measurement setup for a two-tone excitation of an amplifier to determine the third order intercept point

The output spectrum of a nonlinear system, as the amplifier, will exhibits intermodulation products (IM) under two-tone excitation. These "mixing" products are not harmonics of the input signals but are related to their sum and difference, as will be shown. The input signal s_{in} is given by:

$$s_{in} = s_{in,1} + s_{in,2} = A\cos(\omega_1 t) + A\cos(\omega_2 t), \text{ with } |\omega_1 - \omega_2| << \omega_1, \omega_2 \tag{2.16}$$

The output signal is calculated with the use of (2.12):

$$\begin{aligned} s_{out}(t) &= a_1 (A\cos(\omega_1 t) + A\cos(\omega_2 t)) + a_2 (A\cos(\omega_1 t) + A\cos(\omega_2 t))^2 \\ &\quad + a_3 (A\cos(\omega_1 t) + A\cos(\omega_2 t))^3 + ... \\ &= \sum_1^{\infty} a_n (A\cos(\omega_1 t) + A\cos(\omega_2 t))^n \end{aligned} \tag{2.17}$$

Truncating (2.17) after $n = 3$ and expanding the equation by trigonometric transformations, the spectrum of the output signal will contain following harmonics and intermodulation products :

$$\omega_1, \omega_2 : \left(a_1 A + \frac{9}{4} a_3 A^3\right) (\cos(\omega_1 t) + \cos(\omega_2 t)) \tag{2.18}$$

$$|\omega_1 - \omega_2|, \omega_2 - \omega_1 : (a_2 A^2) (\cos((\omega_1 - \omega_2) t) + \cos((\omega_2 - \omega_1) t)) \tag{2.19}$$

$$2\omega_1, 2\omega_2 : \left(\frac{1}{2} a_2 A^2\right) (\cos(2\omega_1 t) + \cos(2\omega_2 t)) \tag{2.20}$$

$$3\omega_1, 3\omega_2 : \left(\frac{1}{4} a_3 A^3\right) (\cos(3\omega_1 t) + \cos(3\omega_2 t)) \tag{2.21}$$

$$2\omega_1 + \omega_2, \omega_1 + 2\omega_2 : \left(\frac{3}{4} a_3 A^3\right) (\cos((2\omega_1 + \omega_2) t) + \cos((1\omega_1 + 2\omega_2) t)) \tag{2.22}$$

$$2\omega_1 - \omega_2, |\omega_1 - 2\omega_2| : \left(\frac{3}{4} a_3 A^3\right) (\cos((2\omega_1 - \omega_2) t) + \cos((1\omega_1 - 2\omega_2) t)) \tag{2.23}$$

Most of the harmonics and intermodulation products are not of concern because they are located far away from the fundamentals in the spectrum, shown in Fig. 2.4. However, two intermodulation products of third order (IM3) are close to the fundamental frequencies and given by (2.23). When the frequency difference between ω_1 and ω_2 is small enough, $2\omega_1 - \omega_2$ and $|\omega_1 - 2\omega_2|$ will appear in the operating frequency band of the amplifier, and thus, distorting the useful signal.

The metric to evaluate the linearity of the amplifier under two-tone excitation, and derived from the given explanation about IM3, is called "third intercept point" (IP3). Considering the Fig. 2.5 and (2.23), it can be seen that if the amplitude of the fundamental is increased by 1 dB, the amplitude of IM3 increases by 3 dB. The definition of the third intercept point is the point on which the fundamental and third order intermodulation reach the same power level. It should be noted that it is not possible to measure IP3 because of gain compression at higher input power levels. Instead, the power of the fundamental and IM3 is

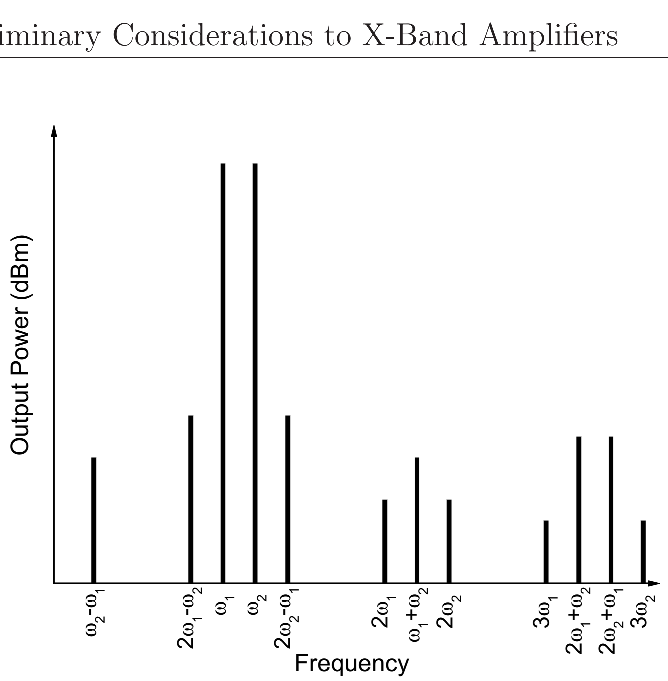


Figure 2.4: Diagram of the amplifier's output spectrum under two-tone excitation

measured at low input signal strengths and the point is extrapolated, as seen in Fig. 2.5. Referring to the output power, the point is stated as "output third order intercept point" (OIP3). In the case that IP3 is read from the input power axis, it is called "‘input third order intercept point"‘ (IIP3).

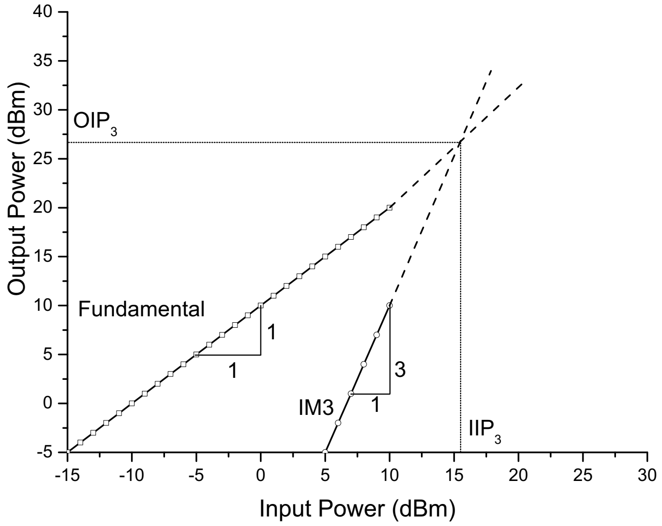


Figure 2.5: Two-tone power transfer characteristic, showing graphical definition of the third-order intercept point

2.1.3 Power Transfer Characteristic and Bandwidth

The power transfer characteristic comprises all presented performance metrics for a single-tone excitation in one diagram. An example of such diagram is given in

Fig. 2.6 and shows the typical power transfer characteristic of a power amplifier.

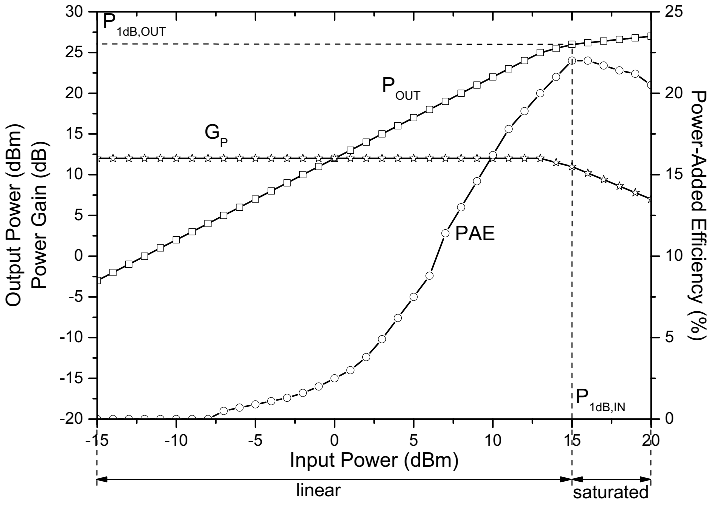


Figure 2.6: Example of a power transfer characteristic of a power amplifier

The diagram depicts the power-added efficiency, output power and power gain as function of the input power. It is possible to read off the maximum output power, power-added efficiency and the small-signal gain of the amplifier, and to distinguish between linear operation and saturation by constructing the 1 dB compression point.

The Fig. 2.7 shows the output power as function of frequency at a specific input power. Depending on the application, several definitions of bandwidth are common.

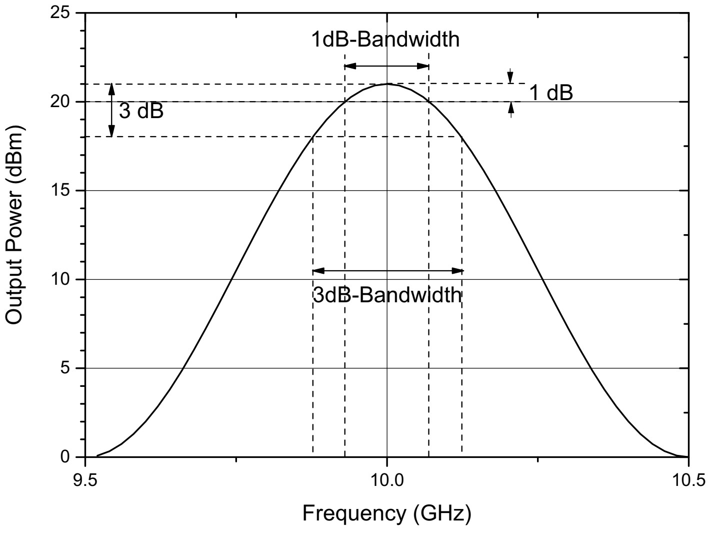


Figure 2.7: 3 dB- and 1 dB-bandwidth definition of amplifiers

The 3 dB-bandwidth defines the frequency range in which the output power varies by 3 dB from the maximum value. Since an output power reduction of 3 dB means that the amplifier can provide only half the maximum power, is the use of a 1 dB-bandwidth more suitable for many applications.

2.1.4 Noise Figure

An important metric for low noise amplifiers is the noise factor (F) or noise figure (NF) and is used to characterize the noise contribution of the amplifier. The definitions of noise factor and figure are given as follow:

$$F = \frac{\text{Signal-to-Noise Ratio at the input}}{\text{Signal-to-Noise Ratio at the output}} = \frac{SNR_{in}}{SNR_{out}} \tag{2.24}$$

$$NF = 10 \log \frac{SNR_{in}}{SNR_{out}} = 10 \log F \tag{2.25}$$

The signal-to-noise ratio is defined as the relation of signal power P_S to noise power P_N:

$$SNR = \frac{P_S}{P_N} \tag{2.26}$$

Using (2.26) in (2.24) and keeping in mind that the available power gain of an amplifier is $G_A = P_{S,out}/P_{S,in}$ results in:

$$\begin{aligned} F =& \frac{P_{S,in}/P_{N,in}}{P_{S,out}/P_{N,out}} = \frac{P_{S,in}/P_{N,in}}{G_A P_{S,in}/(G_A(P_{N,in} + P_{N,add}))} \\ =& \frac{P_{N,in} + P_{N,add}}{P_{N,in}} = 1 + \frac{P_{N,add}}{P_{N,in}} \end{aligned} \tag{2.27}$$

The added noise power of the amplifier at the output is denoted as $P_{N,add}$ in (2.27).

For further solving of (2.27), the simplified noise model of Fig. 2.8 is considered.

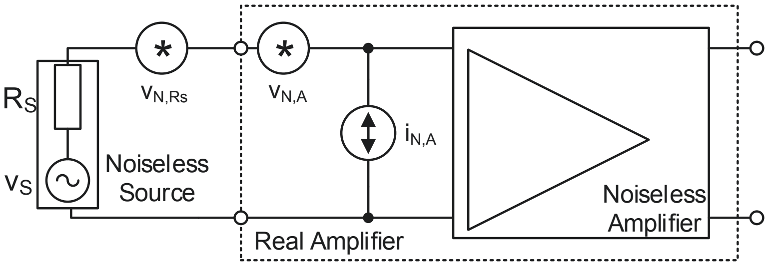


Figure 2.8: Simplified noise model to calculate the noise factor

The amplifier is modeled as ideal, noiseless, amplifier and its noise contribution is taken by the input referred noise voltage source $v_{N,A}$ and current source $i_{N,A}$

into account [Rothe 56]. The source is also noiseless and the source impedance is modeled as resistive impedance R_S, and the noise of the resistor is given by the voltage source $v_{N,Rs}$.

Neglecting any correlation between the noise sources, the added noise power of the amplifier results in:

$$P_{N,add} = \overline{v^2_{N,Rs}} + \overline{v^2_{N,A}} + \overline{i^2_{N,A}} R^2_S \tag{2.28}$$

Consequently, the noise figure is given by:

$$NF = 10 \log \left(\frac{\overline{v^2_{N,Rs}} + \overline{v^2_{N,A}} + \overline{i^2_{N,A}} R^2_S}{\overline{v^2_{N,Rs}}} \right) \tag{2.29}$$

The most common practice to measure the noise performance of an amplifier is to use a noise figure meter which utilizes the Y-factor method [Schiek 06].

2.2 Technology Frameworks

The amplifiers of this thesis are incorporated in two different SiGe technologies. Accordingly, the section describes the basic idea behind the bandgap engineering of Si bipolar transistors and presents the features of the technologies. Furthermore, the basis for the selection of a suitable transistor for the amplifiers is given and the modeling of passive devices in the technologies is depicted.

2.2.1 Silicon Germanium Heterojunction Bipolar Transistor

Silicon germanium heterojunction bipolar transistors are the result of bandgap engineered Si bipolar (homo-)junction transistors. Although the concept of bandgap engineering to improve the transistor's performance was described in 1957 by Kroemer [Kroemer 57], it took about thirty years to realize a first bandgap engineered silicon transistor [Iyer 87].

The general idea behind bandgap engineering is depicted in Fig. 2.9, showing a structure scheme of Si BJT with qualitative doping levels and equivalent band energy diagram. Germanium has a lower bandgap energy (0.67 eV) than pure silicon (1.1 eV), and therefore, an alloy of silicon and a specific small amount n of germanium ($\mathrm{Si_{1\text{-}n}Ge_n}$) will also have lower bandgap energy between the conduction E_C and valence band E_V than silicon. Introduced as base material in a BJT, the consequence would be a by ΔE_g lowered conduction band compared to silicon as base material [Cressler 03]. The difference ΔE_g is given by:

$$\Delta E_g = E_{g,Si} - E_{g,Si_{1-n}Ge_n} \tag{2.30}$$

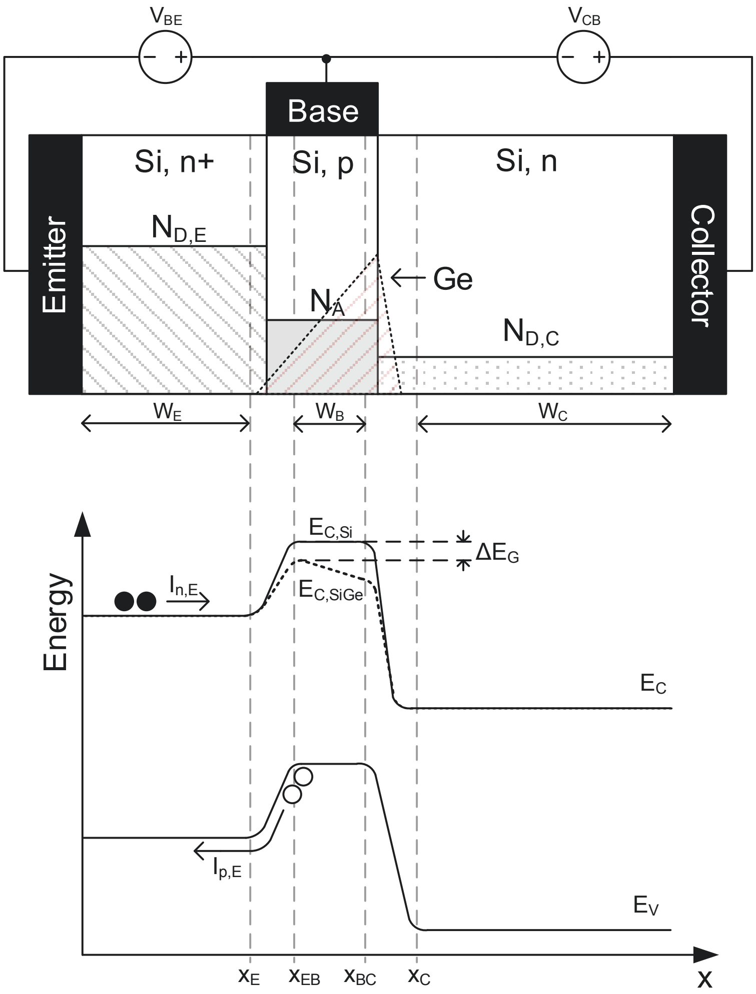


Figure 2.9: Structure scheme of Si BJT and HBT with qualitative doping concentrations and simplified energy band diagram in active mode, base-emitter junction in forward direction and collector-base junction in reverse direction $(V_{BE} < V_{CB})$

The lowered potential barrier for electrons injected into the base increases the emitter base electron current $I_{n,E}$ compared to a BJT for the same base emitter voltage V_{BE}. The energy of the base valence band will not be changed by the SiGe alloy, and therefore, the base emitter hole current $I_{p,E}$ remains unaffected by the bandgap engineering. Neglecting recombination and reverse currents, it is permissible to set $I_{n,E}$ as collector current and $I_{p,E}$ as base current. A subsequent comparison of the static common emitter forward current gain $\beta_{f,DC}$ for Si BJTs and HBTs shows that the increase in $\beta_{f,DC}$ exponentially depends on the bandgap energy difference ΔE_g between Si and $\mathrm{Si_{1\text{-}n}Ge_n}$ [Ashburn 03]:

$$\frac{\beta_{f,DC,Si_{1-n}Ge_n}}{\beta_{f,DC,Si}} \sim e^{\frac{\Delta E_g}{kT}} \tag{2.31}$$

Recalling the approximation of the static current gain of BJTs, shown in (2.32), reveals the impact of the bandgap engineering on transistor design.

$$\beta_{f,DC} = \frac{I_C}{I_B} \approx \frac{I_{n,E}}{I_{p,E}} = \frac{\frac{qD_n}{W_B}\frac{n_{i,B}^2}{N_A}\left(e^{\frac{V_{BE}}{V_T}}-1\right)}{\frac{qD_p}{W_E}\frac{n_{i,E}^2}{N_{D,E}}\left(e^{\frac{V_{BE}}{V_T}}-1\right)} = \frac{D_n W_E n_{i,B}^2 N_{D,E}}{D_p W_B n_{i,E}^2 N_A} \tag{2.32}$$

The current gain of a BJT depends on the ratio of emitter ($N_{D,E}$) and base doping (N_A) and base (W_B) and emitter width (W_E). The emitter of a BJT is already highly doped to decrease the intrinsic emitter resistance and the usage of polycrystalline silicon (poly-Si) as emitter contact material significantly lowers the influence of the emitter width on the current gain. As (2.32) shows, the only possibility to increase $\beta_{f,DC}$ now is to decrease the base doping concentration or thinning the base. Both will have influence on other transistor properties, as the base resistance will be increased by lower doping or base thinning. It is therefore not possible to realize a bipolar junction transistor with high current gain and without degrading significantly other transistor properties, e.g broadband noise caused by the base resistance.

For a HBT with equal doping profile as a BJT, the current gain is exponentially increased by the bandgap engineering. Conversely, this means that the base doping and thickness can be increased to improve other transistor properties by a lowered base resistance.

Furthermore, a graded Ge profile, as shown in Fig. 2.9, will accelerate minority charges in the neutral base by a built-in quasi electric field. The result of the graded Ge profile is a reduced base transit time for electrons in the base. This in turn will further improve the frequency characteristic of the HBT. The quasi electric field is established through the conduction band grading that is given for a linear graded Ge profile by:

$$E_{C,graded}\left(x\right) = \left(E_{C,Si_{1-n}Ge_n}\left(x_{EB}\right) - E_{C,Si_{1-m}Ge_m}\left(x_{BC}\right)\right)\frac{x}{W_B} \tag{2.33}$$

The cross section of a self-aligned double-poly Si HBT is shown in Fig. 2.10. The intrinsic transistor consists only of the n-doped collector, SiGe p-doped base and heavily n-doped monocrystalline silicon emitter. The emitter is connected by a heavily doped poly-Si to its metalized contact. As previously stated, the use of poly-Si decreases the influence of the emitter width on the current gain by decreasing $I_{p,E}$ in (2.32). In the case of the use of poly-Si, a potential barrier at the poly-Si–mono-Si interface reduces the hole current injected from the base [Meister 89]. Moreover, the introduction of poly-Si into the fabrication process allows the formation of a self-aligning base. Base dimensions below lithographic limits became possible and made small transistors with an increased frequency performance feasible [Hashimoto 14]. The poly-Si contact material of the base

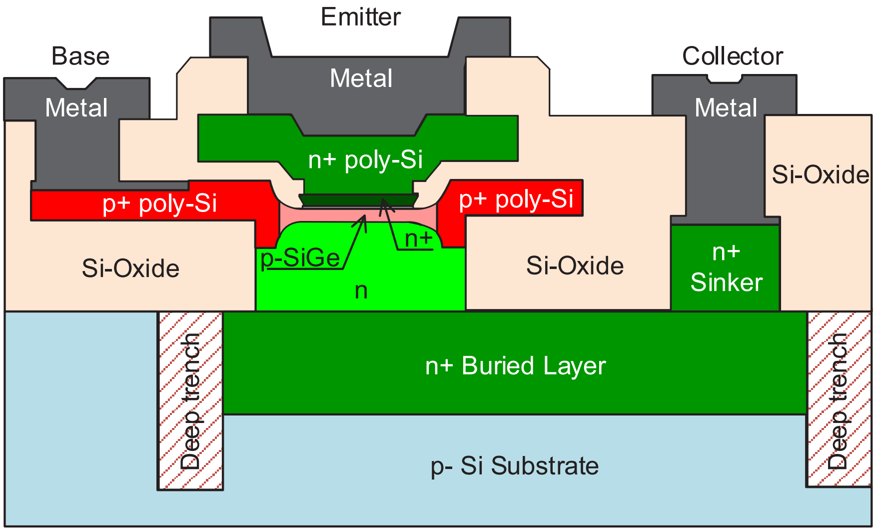


Figure 2.10: Cross section scheme of self-aligned double-poly Si HBT

reduces its sheet resistance. As the collector doping concentration is low, compared to base and emitter doping, the extrinsic collector resistance is reduced by a so-called heavily doped buried layer.

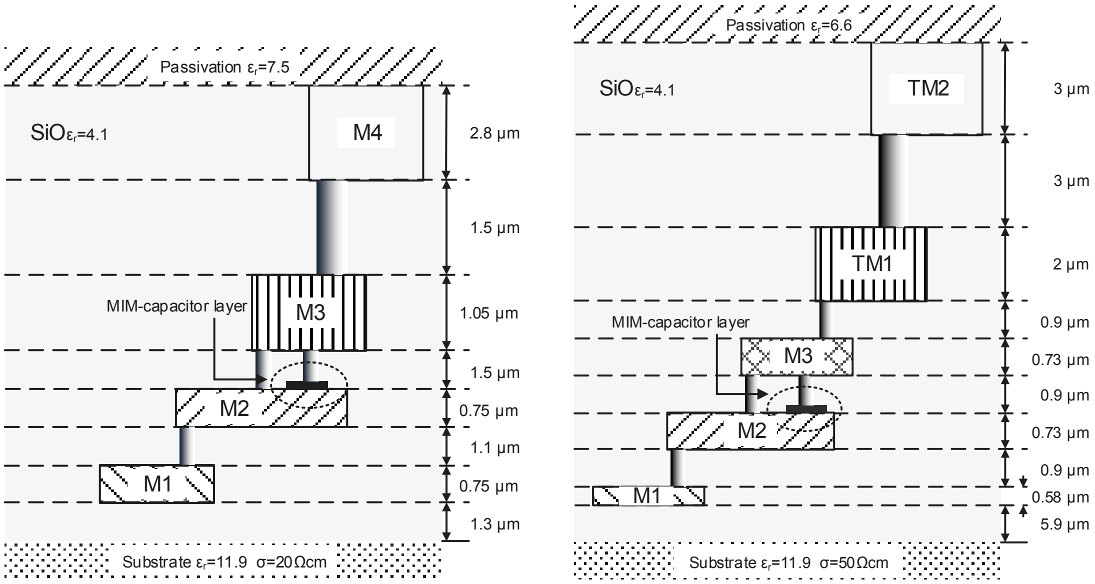
It should be noted that state-of-the-art silicon germanium technologies add a small amount of carbon to the base. Annealing processes at high temperatures enable boron to diffuse out of the base and broaden the base doping profile. When carbon is added, an undersaturation of Si self-interstitials in carbon rich areas occurs by outdiffusing of carbon in these areas. This in turn, suppresses the outdiffusion of boron, and it is demonstrated that the use of carbon in the base improves the static and high-frequency behavior of SiGe:C HBTs [Osten 00].

2.2.2 Features of the Technologies

Two technologies were available to fabricate the power amplifiers and low noise amplifier, IHP Microelectronics's SG25H3 process and Infineon's B7HF200 technology.

B7HF200

The B7HF200 SiGe:C 0.35 µm bipolar technology provides three different vertical npn and on pnp HBTs. The npn transistors differ in their high frequency performance, the fastest device exhibits a transit frequency of 200 GHz and maximum oscillation frequency of 250 GHz. As the transit frequency of the pnp transistor is 3.5 GHz, this transistor is not further considered. Metal-insulator-metal (MIM) capacitors, poly-Si and tantalum nitride (TaN) resistors are available as passive components. The metal stack is depicted in Fig. 2.11(a). The material of the



(a) (b)

Figure 2.11: Metal layer stacks of SiGe technologies, (a) – Infineon B7HF200, (b) – IHP Microelectronics SG25H3

metal layers is copper. A thick top metal layer enables the realization of low-loss inductors and transformers.

SG25H3

In contrast to B7HF200, the IHP SiGe:C HBTs are incorporated in a CMOS technology, SG25H3 is a 0.25 µm SiGe:C BiCMOS technology. Additionally to the HBTs, nMOS and pMOS transistor are available but were not used in the presented designs. Similar to B7HF200, three different npn HBTs are provided with different high frequency performances. The maximum transit frequency of the fastest transistor is 120 GHz with a maximum oscillation frequency of 180 GHz. In contrast to other processes, such as B7HF200, the fast speed transistor has no heavily doped buried collector layer to reduce the collector resistance [Heinemann 06]. Passive components such as poly resistors and MIM capacitors are included. The Fig. 2.11(b) shows the metal layer stack with three metal layer and two thick top metal layers, which can be used to integrate transformers and inductors. The SG25H3 process uses aluminum as metal material.

2.2.3 Transistor Selection for X-band Amplifiers

The selection of a suitable transistor is crucial for the design of RF amplifiers, as its performance mainly defines the overall performance. Both technologies provide three different n-type HBTs that had to be evaluated before an implementation in a design.

The evaluation and subsequent decision was based on the transistor characteristic and performance determined by simulations. It is therefore mandatory that the transistor is accurately modeled. Infineon uses an improved Gummel-Poon model, whereas IHP models the transistor with the Vertical Bipolar Inter-Company model. In the following, and overview on the SPICE Gummel-Poon (SGP) model and the Vertical Bipolar Inter-Company (VBIC) is given. Furthermore, a small-signal model, the hybrid-pi model, for analytic analysis is presented, and the selection of the transistor is illustrated for both technologies.

Spice Gummel-Poon Model

The HBTs of Infineon are modeled by the Gummel-Poon model, implemented in a SPICE simulator called SPICE Gummel-Poon. The circuit model of the HBT is depicted in Fig. 2.12. Although the model was already presented in 1970 [Gummel 70] for BJTs, it was later on adapted for HBTs [Correra 93].

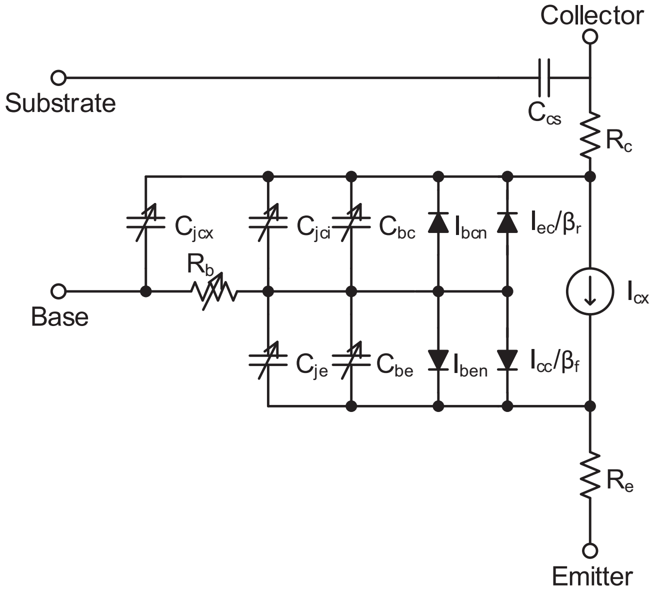


Figure 2.12: Basic Gummel-Poon model used for Infineon's HBTs

Compared to previous models, the novelty of the model is the implementation of the integral charge concept based on the Moll-Ross relation [Moll 56] which allows to consider high-level injection by an increase of the majority charges in the base by a significantly increased minority carrier concentration. The model takes also an additional base recombination current at low-level currents into account.

The collector emitter current I_{cx} in the SGP model is given by:

$$I_{cx} = I_{cc} - I_{ec} = \frac{I_{ss}}{q_b}\left(e^{V_{BE}/n_F V_T} - 1\right) - \frac{I_{ss}}{q_b}\left(e^{V_{BC}/n_R V_T} - 1\right) \tag{2.34}$$

The coefficients n_F and n_R are the forward and reverse emission current coefficients, the thermal voltage V_T is $V_T = kT/q$. In contrast to a constant saturation current I_s for a asymmetrically p-n junction (like in a bipolar transistor)

$$I_S = \frac{qA_j n_i^2 D_n}{W_p N_A}, \text{ with } N_D >> N_A \tag{2.35}$$

the saturation current will change at high-level injection and is therefore defined as:

$$I_S = \frac{I_{ss}}{q_b} \tag{2.36}$$

The saturation current I_{ss} in (2.36) is the saturation current at zero junction bias ($V_{BE} = V_{BC} = 0\,\mathrm{V}$) and it is assumed that the depletion layers are free of mobile charges [Antognetti 89]:

$$I_{ss} = \frac{qD_n n_i^2 A_j}{\int_{\text{neutral base}} N_A(x)\,dx} \tag{2.37}$$

The factor q_b is the relation between majority charges in the base to the base majority charges at zero bias and is splitted into five parts:

$$q_b = \frac{Q_B}{Q_{B0}} = \frac{\int_{\text{neutral base}} qA_j p(x)\,dx}{\int_{\text{neutral base}} qA_j N_A(x)\,dx} \tag{2.38}$$

$$= \frac{1}{Q_{B0}}\left(1 + C_{je}V_{BE} + C_{jc}V_{BC} + \tau_{B,f} I_{cc} + \tau_{B,r} I_{ec}\right) \tag{2.39}$$

It is demonstrated in [Antognetti 89] that by using (2.34) for I_{ec} and I_{cc} in (2.39) q_b can be solved as quadratic equation with the solutions q_1 and q_2:

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{2.40}$$

$$q_1 = 1 + \frac{V_{BE}}{V_B} + \frac{V_{BC}}{V_A} \tag{2.41}$$

$$q_2 = \frac{I_{ss}}{I_{K,f}}\left(e^{V_{BE}/n_F V_T} - 1\right) + \frac{I_{ss}}{I_{K,r}}\left(e^{V_{BC}/n_R V_T} - 1\right) \tag{2.42}$$

The solution of q_1 includes the base width modulation by the parameters V_A (forward Early voltage) and V_B (reverse Early voltage). High-level injection is modeled by q_2. The parameters $I_{K,f}$ and $I_{K,r}$ are the so-called forward and reverse knee currents. It should be mentioned that most SPICE simulators use an approximation for q_b:

$$q_b = \frac{q_1}{2}\left(1 + \sqrt{1 + 4q_2}\right) \tag{2.43}$$

$$q_1 \approx \frac{1}{1 - V_{BE}/V_B - V_{BC}/V_A} \tag{2.44}$$

The low-current effect is modeled by two additional diodes in Fig. 2.12. Consequently, the terminal base current results in:

$$I_B = \frac{I_cC}{\beta_{f,DC}} + \frac{I_eC}{\beta_{r,DC}} + I_{ben} + I_{bcn} \tag{2.45}$$

$$I_{ben} = C_2 I_{ss}\left(e^{V_{BE}/n_{EL}V_T} - 1\right) \tag{2.46}$$

$$I_{bcn} = C_4 I_{ss}\left(e^{V_{BE}/n_{CL}V_T} - 1\right) \tag{2.47}$$

The factors C_2 and C_4 are the forward and reverse low-current nonideal base current coefficients, and n_{EL} and n_{CL} denote low-current base-emitter emission coefficient and low-current base-collector emission coefficient, respectively. The influence and importance of modeling the low-current effect and high-level injection is shown in Fig. 2.13 which depicts the variation of base and collector current. The conclusion of the diagram in Fig. 2.13 is that the use of the SPICE Gummel-Poon model allows to model the variation of the current gain as function of the collector current.

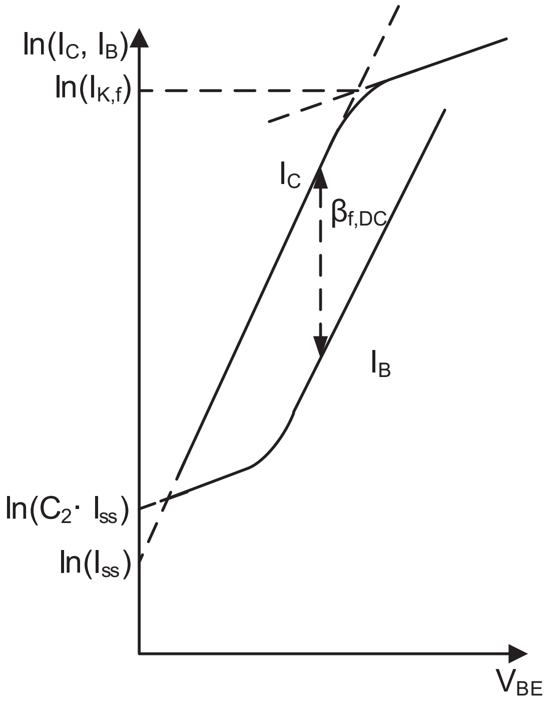


Figure 2.13: Terminal collector current and base current as function of V_{BE} with $V_{BC} = 0$

The base resistance is modeled as a nonconstant resistor because it consists of two resistances. The first resistance is given by the external contact and sheet resistance of the external base. The second part is the resistance of the active base, the region below the emitter in Fig. 2.10. The equation for R_B is [Maas 04]:

$$R_B = r_{bm} + 3\left(r_b - r_{bm}\right)\left(\frac{\tan z - z}{z\tan^2 z}\right) \tag{2.48}$$
$$z = \frac{-1 + sqrt 1 + 144 I_B/\pi^2 I_{rB}}{24/\pi^2 \cdot \sqrt{I_B/I_{rB}}}$$

The minimum base resistance at high current levels is denoted by r_{bm}, r_b is the external contact and base sheet resistance and the current I_{rB} is the current where r_{bm} is twice its value.

The depletion capacitances C_{je}, C_{jci} and $C_{jcx}$are modeled by:

$$C_j(y) = \frac{C_{j0(y)}}{\left(1 - \frac{V_{B(y)}}{V_{j(y)}}\right)^{m_{j(y)}}},\ y = \begin{cases} e, & \text{emitter} \\ c, & \text{collector} \end{cases} \tag{2.49}$$

The capacitance $C_{j0(y)}$ is the depletion capacitance at zero bias, $m_{j(y)}$ represents the grading coefficient and the voltage $V_{j(y)}$ is the built-in voltage of the junction. A problem occurs in (2.49) when the bias voltage $V_{B(y)}$ gets close to the built-in voltage. The capacitance will diverge to infinity. To avoid this issue, $V_{B(y)}$ is limited to:

$$V_{B(y)} < FC \cdot V_{j(y)},\ FC \in [0..1] \tag{2.50}$$

For larger values of $V_{B(y)}$, the capacitance is linearly extrapolated. The depletion capacitance between base and collector is divided into two capacitances to separate between the capacitance at the active base and collector, and an overlapping capacitance between the extrinsic base and collector:

$$C_{jci} = X_{jc} C_{jc},\ X_{jc} \in [0..1] \tag{2.51}$$
$$C_{jcx} = \left(1 - X_{jc}\right) C_{jc} \tag{2.52}$$

The diffusion capacitances C_{bc} and C_{be} are given by:

$$C_{be} = \tau_f \frac{dI_{cc}}{dV_{BE}} = \frac{\tau_f I_{ss}}{q_b n_F V_T} e^{V_{BE}/n_F V_T} \tag{2.53}$$
$$C_{bc} = \tau_r \frac{dI_{ec}}{dV_{BC}} = \frac{\tau_r I_{ss}}{q_b n_R V_T} e^{V_{BC}/n_R V_T} \tag{2.54}$$

It should be noted that the transit time τ_f is not constant in the SPICE Gummel-Poon model but modulated by I_{cc} and V_{BC} [Correra 93].

Similar to depletion capacitances of the base, the collector substrate capacitance

C_{cs} is modeled by:

$$C_{cs} = \frac{C_{cs0}}{\left(1 - \frac{V_{cs}}{V_{jcs}}\right)^{m_{jcs}}},\ V_{cs} < FC \cdot V_{jcs},\ FC \in [0..1] \tag{2.55}$$

Although the given description of the SPICE Gummel-Poon model is not complete, it demonstrates the concept of the model, as subsequent models, like VBIC, are based on the presented concept of integral charge.

Vertical Bipolar Inter-Company Model

IHP Microelectronics uses the VBIC model for the SiGe:C HBTs. The VBIC model was reported in 1996 [McAndrew 96] and was intended to improve the modeling of vertical transistor. The model circuit diagram is depicted in Fig. 2.14. Since VBIC is based on the SPICE Gummel-Poon model, the following explanation focuses on the important distinguishing features.

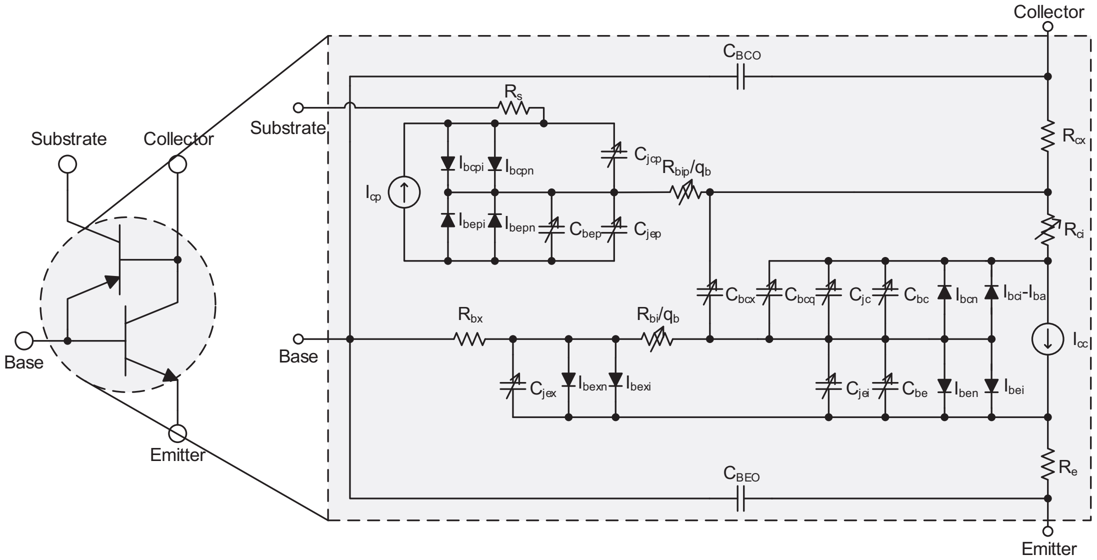


Figure 2.14: Generalized VBIC model to model SG25H3 HBT

Looking again at the cross section of an HBT in Fig.2.10 reveals that next to the npn transistor a parasitic pnp transistor is present. The emitter of the pnp is the base of the HBT, the base is the n-doped collector and the substrate acts as collector. Contrary to the SGP model, this pnp transistor is included in the VBIC model by a partial Gummel-Poon model. Its collector emitter current is modeled by the current source I_{cp} and the base current is modeled by four diodes including diffusion and depletion capacitances, as known from the SGP model.

The most significant difference between VBIC and SGP is the unlink between collector emitter current and base current. Similar to SGP the collector emitter current is given by:

$$I_{cc} = \frac{I_s}{q_b}\left(I_F - I_R\right) = \frac{I_s}{q_b}\left(\left(e^{V_{BE}/n_F V_T} - 1\right) - \left(e^{V_{BC}/n_R V_T} - 1\right)\right) \tag{2.56}$$

Although the notation is slightly different compared to SGP, the components of (2.56) have the same meaning, e.g. I_s of the VBIC model would be I_{ss} in the SGP.

The total base current I_B is presented by:

$$I_{BE} = I_{BEI}\left(e^{V_{BE}/n_{EI} V_T} - 1\right) + I_{BEN}\left(e^{V_{BE}/n_{EN} V_T} - 1\right) \tag{2.57}$$

$$I_B = I_{BE,int} + I_{BE,ext} = W_{BE} I_{BE} + \left(1 - W_{BE}\right) I_{BE},\ W_{BE} \in [0..1] \tag{2.58}$$

As mentioned, the base current I_{BE} is now independent of I_F from (2.56) and is composed of an ideal component by I_{BEI} and a nonideal part denoted by I_{BEI}. Furthermore, the total base current I_B is splitted into two currents, an external (I_{bexn}, (I_{bexi}) and internal (I_{ben}, (I_{bei}), in (2.58) by W_{BE}. It is taken into account that the total base current is affected by the distributed base.

The base collector current is similar to (2.57) modeled by an ideal and nonideal component:

$$I_{BC} = I_{BCI}\left(e^{V_{BC}/n_{CI} V_T} - 1\right) + I_{BCN}\left(e^{V_{BC}/n_{CN} V_T} - 1\right) \tag{2.59}$$

Additionally, I_{BCI} in Fig. 2.14, includes a weak avalanche current I_{ba} to model the avalanche multiplication [Cao 00].

Further improvements are:

- The approximation of the normalized majority base charge q_b in (2.43) is replaced by the exact solution, resulting in an improved Early effect modeling:

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{2.60}$$

- The base emitter depletion capacitance is splitted into an external and internal capacitance by W_B.
- The diffusion capacitance model is extended by the parameter q_1 in the expression for the modulated transit time τ_f
- The formulation of the intrinsic base resistance R_{bi} includes the normalized majority base charge q_b.
- Constant emitter and substrate resistance (R_E, R_S) as well as constant overlap capacitances (C_{BCO}, C_{BEO}) model parasitics capacitances.

- Two additional subcircuits (not shown in Fig. 2.14) model self-heating of the transistor and an excess phase shift due to an additional time delay in the base.
- VBIC includes are variable intrinsic collector resistance R_{ci} which allows to model quasi-saturation, based on the modified Kull model [Kull 85]. That is, high currents in the collector results in an increased voltage drop at the collector resistance which reduces the intrinsic collector voltage. As consequence, the base collector junction could become forward biased despite the fact that the external collector voltage would prevent a forward biasing of the junction. Additionally, two capacitors (C_{bcx}, C_{bcq}) are used to include the effect of a base pushout into the collector.

Although the VBIC model provides an improved accuracy compared to the SGP model, its increased model circuit complexity shows that the modeling process itself becomes more demanding. Even if SGP and VBIC are being further developed and new models with improved high current modeling, as HICUM [Schroter 02] or MEXTRAM [Rijs 96], are provided, they are worthless if the transistors are insufficiently modeled. Convergence problems in simulations or mismatches between simulation and reality are the consequence.

Hybrid-pi Model

The last model that is presented is the small signal model, or hybrid-pi model, as it is used in this thesis. As long as the input signal amplitude is small and low-current effects and high-level injection are neglected, the model of the HBT can be linearized at its operating point, shown in Fig. 2.15

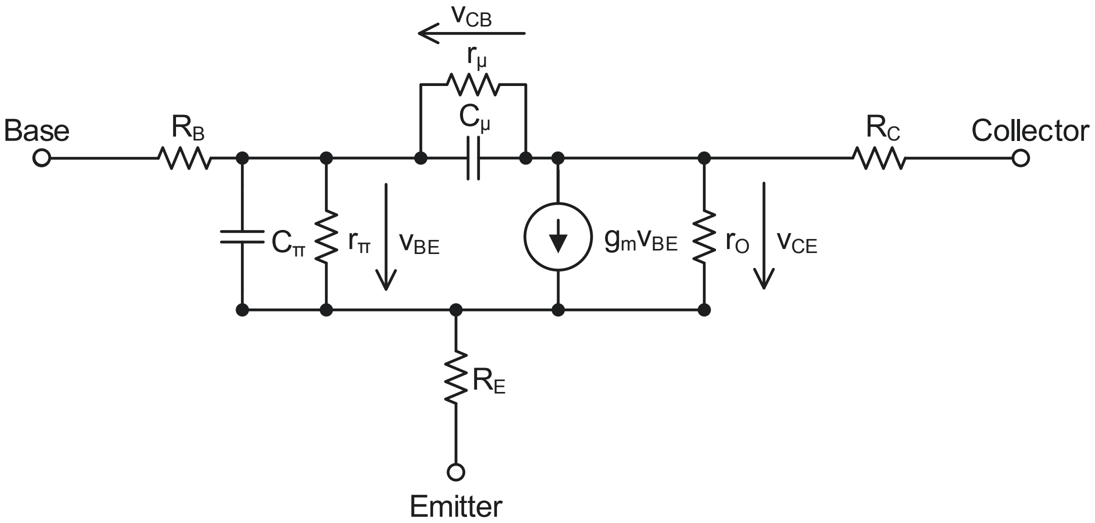


Figure 2.15: Hybrid-pi model for the heterojunction transistor

The description of this model uses following convention for current and voltage signals:

- Capital letters and capital indices denote DC voltages and currents (I_C).
- Small-signal voltages and currents and derived small-signal components are indicated by small letters with small indices (i_c).
- Capital letters with small indices are used for total instantaneous signals ($i_C = I_C + i_c$).

The base, emitter and collector resistance is modeled by constant resistors R_B, R_C and R_E but can be omitted for most analyses and are not further considered. The terminal currents of the base and collector and their relation to each other are given as follow:

$$\beta_{f,DC} = \frac{I_C}{I_B},\ \beta_f = \beta_{f,DC}\left(1 + \frac{v_{CE}}{V_A}\right),\ \text{Early voltage } V_A > 0 \tag{2.61}$$

$$i_C = I_S\left(e^{v_{BE}/V_T} - 1\right)\left(1 + \frac{v_{CE}}{V_A}\right),\ i_B = \frac{I_S}{\beta_{f,DC}}\left(e^{v_{BE}/V_T} - 1\right) \tag{2.62}$$

With the assumption $V_A >> v_{CE}$ and neglecting the second term of the Shockley equation for the currents, the previous expressions can be simplified to:

$$\beta_f = \beta_{f,DC} \tag{2.63}$$

$$i_C = I_S e^{v_{BE}/V_T} \tag{2.64}$$

$$i_B = \frac{I_S}{\beta_{f,DC}} e^{v_{BE}/V_T} \tag{2.65}$$

The components of the circuit diagram in Fig. 2.15 can be now derived as follow:

$$g_m = \frac{di_C}{dv_{BE}} = \frac{I_S}{V_T} e^{v_{BE}/V_T} = \frac{I_C}{V_T} \tag{2.66}$$

$$r_\pi = \left(\frac{di_B}{dv_{BE}}\right)^{-1} = \left(\frac{di_C/\beta_f}{dv_{BE}}\right)^{-1} = \left(\frac{I_S}{\beta_f V_T} e^{v_{BE}/V_T}\right)^{-1} = \frac{\beta_f}{g_m} \tag{2.67}$$

$$r_O = \left(\frac{di_C}{dv_{CE}}\right)^{-1} = \left(\frac{I_C}{V_A}\right)^{-1} \tag{2.68}$$

$$r_\mu = \left(\frac{di_B}{dv_{BC}}\right)^{-1} = \left(\frac{di_C/\beta_r}{dv_{BC}}\right)^{-1} = \frac{\beta_r}{g_{m,r}} \tag{2.69}$$

$$C_\pi = C_{je}\left(v_{BE}\right) + g_m \tau_f \tag{2.70}$$

$$C_\mu = C_{jc}\left(v_{BC}\right) + g_{m,r} \tau_r \tag{2.71}$$

The model can be further simplified by the assumption that the current of the base collector junction is negligibly small, as the base collector junction is assumed to be reversed biased. The resistor r_μ in (2.69) becomes therefore infinity and the capacitor C_μ in (2.71) is only determined by the depletion capacitance.

Transistor Selection

The selection of a suitable transistor was based on the transit or cutoff frequency f_t and maximum oscillation frequency f_{max} of the transistor.

Transit Frequency Transit frequency is the frequency at which the output short circuit current gain $\beta_{AC,SC}$ becomes unity, whereas the transistor is driven by a current source i_b at the input:

$$\lim_{f \to f_t} \beta_{AC,SC}(\omega) \bigg|_{V_{CE}=0\,\mathrm{V}} = \lim_{f \to f_t} \frac{i_c(\omega)}{i_b} \bigg|_{V_{CE}=0\,\mathrm{V}} = 1 \tag{2.72}$$

Based on the hybrid-pi model (Fig. 2.15), the missing current i_c to derive f_t can be calculated as follow:

$$i_c(\omega) = g_m v_{be}(\omega) \tag{2.73}$$

The base emitter voltage $v_b e$ as consequence of the input current is:

$$v_{be}(\omega) = \frac{i_b r_\pi}{1 + r_\pi j\omega (C_\pi + C_\mu)} = \frac{i_b}{\frac{1}{r_\pi} + j\omega (C_\pi + C_\mu)} \tag{2.74}$$

Using (2.74) in (2.73) allows to calculate $\beta_{AC,SC}$:

$$\beta_{AC,SC}(\omega) = \frac{i_c}{i_b} = \frac{g_m v_{be}}{i_b} = \frac{g_m \frac{i_b}{\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)}}{i_b} = \frac{g_m}{\frac{1}{r_\pi} + j\omega (C_\pi + C_\mu)} \tag{2.75}$$

The derivation of the short circuit current gain in (2.75) assumes negligible small collector and base resistances. Furthermore, the small signal resistance r_π can be omitted at high frequencies, as r_π is constant over frequency and the admittance of C_π and C_μ will dominate the denominator with rising frequency, and therefore, $\beta_{AC,SC}$ can be written for high frequencies as:

$$\beta_{AC,SC}(\omega) = \frac{g_m}{j\omega (C_\pi + C_\mu)} \tag{2.76}$$

The definition of the transit frequency in (2.72) can now be used in (2.76) and results in:

$$\beta_{AC,SC}(2\pi f_t) = \frac{g_m}{j\omega (C_\pi + C_\mu)} = 1 \tag{2.77}$$

An rearrangement of (2.77) with respect to ω results in a expression for the transit frequency f_t:

$$f_t = \left| \frac{gm}{2\pi j\left(C_\pi + C_\mu\right)} \right| = \frac{gm}{2\pi\left(C_\pi + C_\mu\right)} \tag{2.78}$$

It is worth to mention that f_t of (2.78) is derived by the small signal model which is a linearized model of the actual transistor. A more physical derivation of f_t can be obtained by the emitter collector transit time delay τ_{ec}:

$$f_t = \frac{1}{2\pi\tau_{ec}} \tag{2.79}$$

The transit time delay τ_{ec} specifies the finite time delay for an electron, in the case of a npn-HBT, crossing the transistor from emitter to collector and is composed of minority carrier storage delays and junction capacitance charging delays. The expression for f_t in 2.79 can be therefore expanded to [Miura 06]:

$$\begin{aligned} f_t =& \frac{1}{2\pi}\frac{1}{\tau_e + \tau_b + \tau_c + \tau_{RC}} && (2.80)\\ =& \frac{1}{2\pi}\left(\frac{V_T}{i_e}\left(C_{je} + C_{jc}\right) + \left(\frac{W_B^2}{2D_{n,B}} + \frac{W_B}{nv_s}\right) + \frac{W_{DC}}{2v_s} + C_{jc}\left(R_E + R_C\right)\right)^{-1} && (2.81) \end{aligned}$$

The base and collector transit time delays are denoted as τ_b and τ_c in (2.80). The additional term W_B/nv_s in (2.81) for τ_b takes the transit time caused by neutral charge storage in the depletion region of base and emitter into account [van den Biesen 86]. The factor n is determined by the base band gap and doping profile, v_s is the saturation velocity, $D_{n,B}$ the diffusion coefficient of electrons in the base and W_B is the width of the neutral base. The depletion region with of the collector is given by W_{DC}. It is further assumed in (2.81) that the transistor has no graded Ge-profile. The junction capacitance charging delays are represented by the RC time constants τ_e and τ_{RC} of the corresponding depletion regions. The term V_T/i_e models the small signal dynamic emitter resistance.

From (2.78) or (2.81), with the approximation of $i_c \approx i_e$, it is obvious that f_t varies with the collector current. A simulation plot of the transit frequency as function of the collector current is shown in Fig. 2.16. At low collector currents the first term of (2.81) will dominate the overall transit time τec. An increase of the collector current results in an increasing transit frequency to the point of highest obtainable transit frequency $f_{t,max}$ at a collector current $I_{C,ft,max}$. Larger collector currents affects the transistor by high-level injection (e.g. base push-out or quasi-saturation) which leads to an increasing transit time, and thus, to a roll-off of f_t.

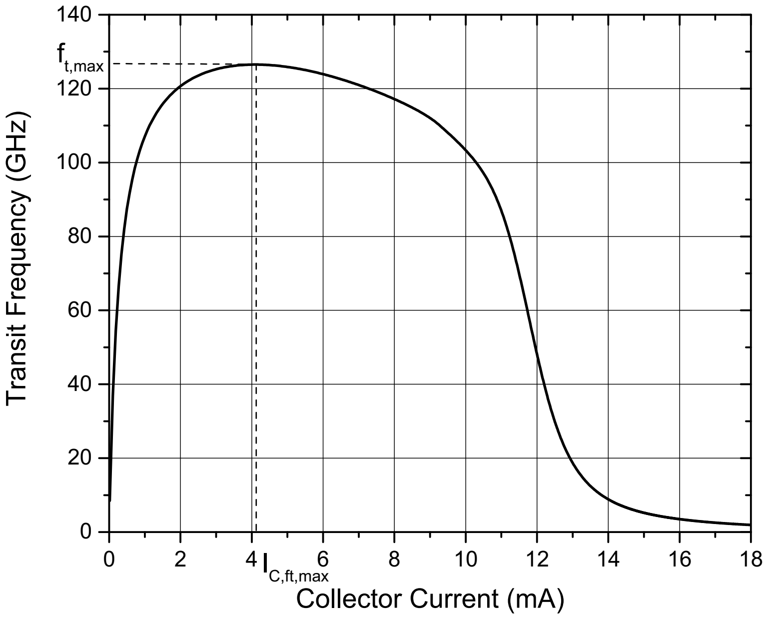


Figure 2.16: The tranit frequency as function of the DC collector current I_C obtained by simulation

The transit frequency is not measured directly but extrapolated from the short circuit current gain versus frequency, as seen in Fig. 2.17.

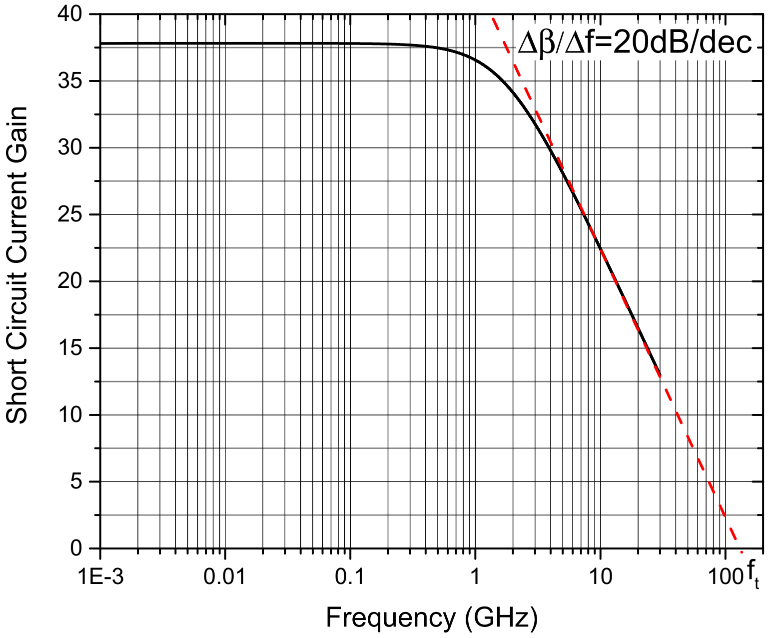


Figure 2.17: Short circuit current gain as function of frequency to extrapolate the transit frequency

Breakdown Voltages An conclusion of the diagram in Fig. 2.16 and (2.81) is that an increase of $f_{t,max}$ can be realized by a thinner base width and/or increased collector current. A larger collector current in turn require a higher collector doping to avoid a base push-out and to reduce the internal collector resistance, and therefore, the internal voltage drop to avoid quasi-saturation. As consequence of a thinner base and more heavily doped collector will be a decrease of the breakdown voltages, BV_{CEO} and BV_{CBO}.

The breakdown voltage BV_{CBO} is defined as the breakdown of the reversely biased collector base junction due to avalanche breakdown caused by high electric field strength. The value of BV_{CBO} depends on the base and collector doping concentrations, and thus, an increased collector doping will lower the value for BV_{CBO} [Ma 02a].

The collector emitter breakdown voltage BV_{CEO} is defined as the upper limit for the collector emitter voltage, measured with an open base. As an ideal current source has an infinite output impedance, it would be also the limit for the case that the base is driven by a current source instead of being left open.

The basic physical principle behind BV_{CEO} is as follows; The leakage current of the reversely biased collector base junction injects holes into the base that contributes to the hole current injected into the emitter because they can not leave the base. As the emitter base current is a multiple of the base hole current, the emitter electron current will rise. This in turn has the consequence of a higher electron-hole generation in the base collector depletion region by impact ionization caused by the high electric field strength. The result is an increased base collector leakage current.

This positive feedback on the collector current ($I_C \approx I_E$) can be expressed by [Veenstra 05]:

$$I_C = I_B \frac{M}{1 + \beta_{f,DC}^{-1} - M} \tag{2.82}$$

The constant M denotes the avalanche multiplication factor:

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^{\eta}}, \ \eta : \text{fitting parameter} \tag{2.83}$$

The breakdown occurs as M reaches the value of $1 + 1/beta_{f,DC}$. Furthermore, BV_{CEO} can be related to BV_{CBO}:

$$BV_{CEO} = V_{BE} + \frac{BV_{CBO}}{\sqrt[\eta]{\beta_{f,DC} + 1}}, \text{ with } V_{CE} = V_{BE} + V_{BC} \tag{2.84}$$

Two conclusion can be made:

- The value of BV_{CEO} is lower than the value of BV_{CBO} because the breakdown defined by BV_{CBO} includes no positive feedback.

- The higher the value of $\beta_{f,DC}$, the lower is the value of BV_{CEO}. Keeping in mind that higher values of f_t can be obtained by thinning the base and that the current gain is proportional to the base width, it becomes obvious why an increase of the transit frequency results in reduction of the breakdown voltages. This trade-off between transit frequency and breakdown voltages is inevitable in the selection of a suitable transistor.

Maximum Oscillation Frequency Based on the definition of the transit frequency, two drawbacks for determining the performance of transistors are recognizable:

- The output load impedance is assumed to be zero, which is obviously not a practical load impedance value.
- The definition of f_t implies only the intrinsic transistor performance, the influence of the base resistance R_B in Fig. 2.15 is neglected, although a certain amount of input power will be dissipated in R_B. Despite the fact that Fig. 2.15 shows the collector and emitter resistance, the value for R_B would be much higher compared to the other resistances and needs to be primarily considered. Furthermore, the time constant due to the base resistance and base collector capacitance is not considered in the definition of f_t.

As consequence for the performance evaluation, a second metric is taken into account, the maximum oscillation frequency which is defined as frequency at which the maximum operating power gain G_{max} becomes unity. The maximum operating power gain is given by the power at the load divided by the power available at the transistor with conjugate matched impedances.

Considering the hybrid model in Fig. 2.15 once more and connecting a conjugate matched source (with Z_S) at the input and a load impedance Z_L at the output. The frequency f$_{max}$ can be derived as follow; The maximum power gain is given by:

$$G_{max} = \frac{P_L}{P_{in}} = \left(\frac{i_c}{i_b}\right)^2 \frac{Z_L}{R_B} \tag{2.85}$$

It is assumed in (2.85) that the output transconductance r_O is negligible large and that most of the input power consumption results from R_B. The output impedance Z_L is given by:

$$Z_L = \frac{v_L}{i_L} = \frac{v_L}{i_c} = \frac{v_L}{g_m v_{be}} \approx \frac{v_L}{g_m v_L \frac{C_\mu}{C_\pi}} = \frac{C_\pi}{g_m C_\mu} \tag{2.86}$$

The derivation of the load impedance is made under following assumptions. The load, and thus, the collector current are equal to $g_m v_{be}$, a current through C_μ is not considered as it is much smaller than i_c. Furthermore, the voltage v_{be} is given by the voltage divider of C_π and C_μ. That is, for very high frequency it is assumed that $|Z_S + R_B| >> |(j\omega C_\pi)^{-1}|$ is valid. The last approximation in (2.86) is that $C_\pi > C_\mu$, and therefore, $v_{be} = (C_\mu/C_\pi)v_L$ is assumed.

The last component in (2.85), the base current is derived by the currents through C_π and C_μ, where again the current through C_μ is neglected:

$$\begin{aligned} i_b &= j\omega\left(C_\pi v_{be} + C_\mu v_{bc}\right) = j\omega\left(C_\pi v_{be} + C_\mu\left(v_{be} - v_{ce}\right)\right) \\ &= j\omega\left(C_\pi v_{be} + C_\mu v_{be} + g_m v_{be} Z_L C_\mu\right) = 2j\omega C_\pi v_{be} \\ &\text{with } v_{ce} = -g_m v_{be} Z_L \end{aligned} \tag{2.87}$$

Substituting (2.87) and (2.86) in (2.85) results in:

$$G_{max}\left(\omega\right) = \frac{g_m v_{vbe}}{2j\omega C_\pi v_{be}} \frac{\frac{C_\pi}{g_m C_\mu}}{R_B} = \frac{g_m}{4\omega^2 R_B C_\pi C_\mu} \tag{2.88}$$

As f_{max} is defined at the frequency $G_{max}\left(2\pi f_{max}\right) = 1$ and with the approximation of $f_t = g_m/(2\pi C_\pi)$, f_{max} is related to f_t by [Cressler 98]:

$$f_{max} = \sqrt{\frac{f_t}{8\pi C_\mu R_B}} \tag{2.89}$$

As seen in (2.89), f_{max} combines the intrinsic transistor performance with parasitics of the transistor, and thus, it is a more realistic performance estimation possible than only with the transit frequency.

Similar to the determination of f_t is the maximum oscillation frequency extrapolated from lower frequency values of the power gain versus frequency with a slope of $-20\,\text{dB}/dec$.

Transistor Selection in both Technologies In the case if IHP transistors, the selection was straightforward based on the performance metrics given in the datasheet (see Tab. 2.1). The transistor with the marking "npnH3PI" was selected as it superior the other two transistors in terms of high frequency performance.

Table 2.1: Performance metrics of IHP transistors

	npnH3PI	npnH3MV	npnH3HV
BV_{CEO} (V)	2.2	5	7
BV_{CBO} (V)	6	15.5	21
f_t (GHz)	110	45	25
f_{max} (GHz)	180	140	80

An interesting fact is that the difference in terms of transit frequency and breakdown voltages between "npnH3MV" and "npnH3HV" is the result only of different collector doping concentrations [Heinemann 06]. Therefore, various transistors with different characteristics can be offered without changing the lithographic mask set.

The parameters of the B7HF200 technology transistors are presented in Tab. 2.2 and the selection of a transistor was similarly carried out as before.

Table 2.2: Performance metrics of Infineon transistors

	npnUHS	npnHS	npnHV
BV_{CEO} (V)	1.5	1.7	4
BV_{CES} (V)	5.8	6.5	14.5
f_t (GHz)	200	170	35
f_{max} (GHz)	250	250	120

Differently to IHP, the device with highest f_t was not chosen. Instead, the transistor "npnHS" was selected for following reasons:

- The current gain difference at 10 GHz is approximately 1.8 dB or increased by a factor of 1.23 for the "npnUHS" compared to the "npnHS". On the other hand, a 30 % larger collector quiescent current is necessary to operate the "npnUHS" at $f_{t,max}$ which potentially will degrade the efficiency.
- The breakdown voltage BV_{CEO} is slighty higher for the "npnHS". Therefore, larger collector voltages are feasible that can enhance the efficiency.
- The parasitics in terms of R_B and C_μ must be similar, as f_{max} is equal for both transistors.

It should be noted that Infineon does not provide values for BV_{CBO} but for BV_{CES} ($BV_{CES} < BV_{CBO}$). The breakdown voltage BV_{CES} is similar to BV_{CEO} with the important difference that the base is shorten to the reference potential. Therefore, BV_{CES} denotes the absolute upper limit for the collector emitter voltage, whereas BV_{CEO} indicates the lowest breakdown voltage for V_{CE}.

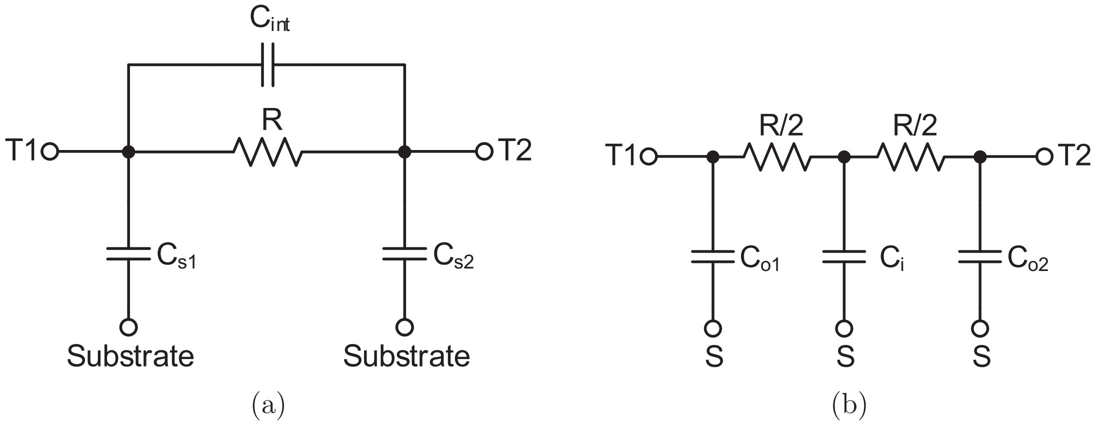
2.2.4 Passive Components

The modeling of passive components is of essential importance as they are used for impedance matching or resonant circuits. Especially, capacitors and inductors have a frequency-dependent characteristics, and it is therefore necessary to take parasitics into account to avoid mismatches between simulation and experimental results.

Resistors

Both technologies provide different types of resistors, as high- and low-doped polysilicon resistors or tantalum nitride (TaN) resistors. The use of different materials and doping concentrations allows to realize resistors with different sheet resistances to optimize the area usage of the resistor in dependence of its intended value. For instance, a high resistor value realized by a low-ohmic sheet resistance, e.g TaN-resistors, results in a long resistor layout which would increase parasitics.

Two scalable models, used in both technologies, are shown in Fig. 2.18. The model depicted in Fig. 2.18(a) is implemented as resistor model in the SG25H3 technology.



(a) (b)

Figure 2.18: Two resistor models to model the frequency-dependent characteristic, (a) – SG25H3 model, (b) – B7HF200 model

The resistor itself is denoted by R. The area dependent substrate coupling is modeled by two capacitors, C_{s1} and C_{s2}. Furthermore, the capacitor C_{int} represents a capacitive leakage between both terminals T_1 and T_2. In contrast, the model of the B7HF200 process in Fig. 2.18(b) splits the resistor R into two equal parts and models the overall resistor area dependent substrate capacitance C_S by C_{o1}, C_{o2} and C_i. The substrate coupling of the resistor body is modeled by C_i which is a part X of the overall substrate capacitance:

$$C_i = XC_S \tag{2.90}$$

The terminal substrate capacitances (C_{o1}, C_{o2}) are given by:

$$C_{o1}, C_{o2} = \frac{(1 - X)\, C_S}{2} \tag{2.91}$$

Capacitors

Bipolar or BiCMOS technologies provide in general two different types of capacitors:

- Junction and MOS capacitors: The depletion capacitance of a reversed bias pn junction can be used as voltage-controlled capacitor. The MOS capacitor utilizes for example the heavily doped emitter region with a oxide on top and a metal layer above the oxide. Furthermore, a MOS transistor itself is applicable as capacitor. The gate-channel capacitance can be used with the gate as top electrode and source/drain as bottom electrode. The main disadvantage is that these type of capacitors have to be biased to exhibit the desired capacitance value. Although these capacitors have a high capacitance density, they suffer from low quality factors and low breakdown voltages [Baker 65]. A further major drawback is the nonlinear dependency of the capacitance value on the bias voltage.
- Metal-Insulator-Metal (MIM): Metal-Insulator-Metal capacitors are realized in general by lateral or vertical close spacing of two metals, separated by an insulator. The simplest form of this type capacitors is the Metal-Oxide-Metal (MOM) capacitor. For instance, two metal layers are placed overlapping for a vertical capacitor structure and are separated by the silicon oxide. As the spacing between metal layers is large and the permittivity of silicon oxide is only about 4, the resulting capacitance density of a MOM capacitor is low but the quality factor and the breakdown voltage would be high relative to junction and MOS capacitors.

The closer definition of Metal-Insulator-Metal capacitors include a separate dielectric and metal layer to form the capacitance. An example is depicted in Fig. 2.19. A top metal is connected through vias to the top metal electrode of the capacitor. A thin dielectric layer (thickness is less than 100 nm) isolates the top electrode from the bottom electrode. The material of the dielectric differs from silicon oxide, materials with a permittivity larger than 4 are used to increase the capacitance density. As in the example of Fig. 2.19, the lower metal layer can be used as bottom electrode.

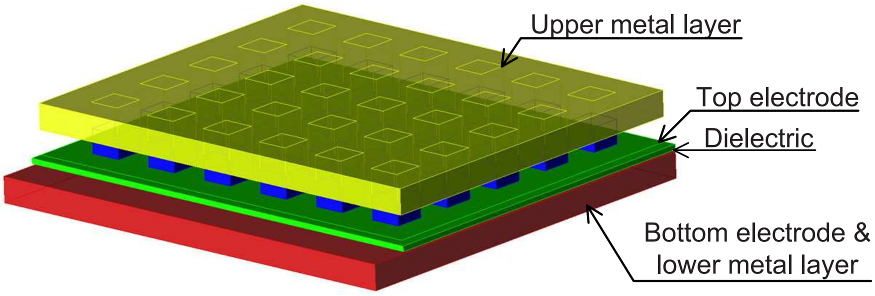


Figure 2.19: 3D view of a Metal-Insulator-Metal capacitor

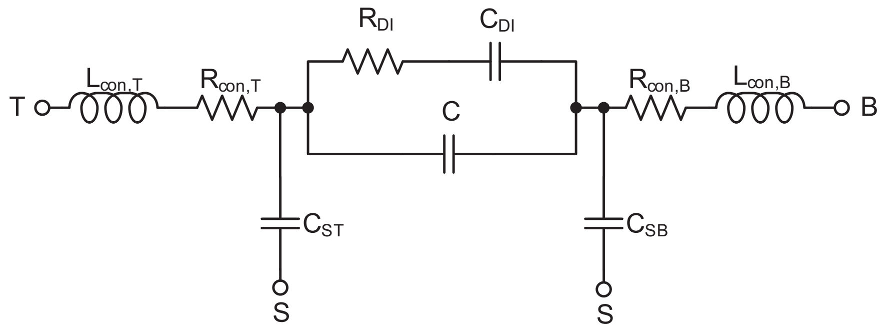


Figure 2.20: Equivalent circuit diagram of a MIM capacitor

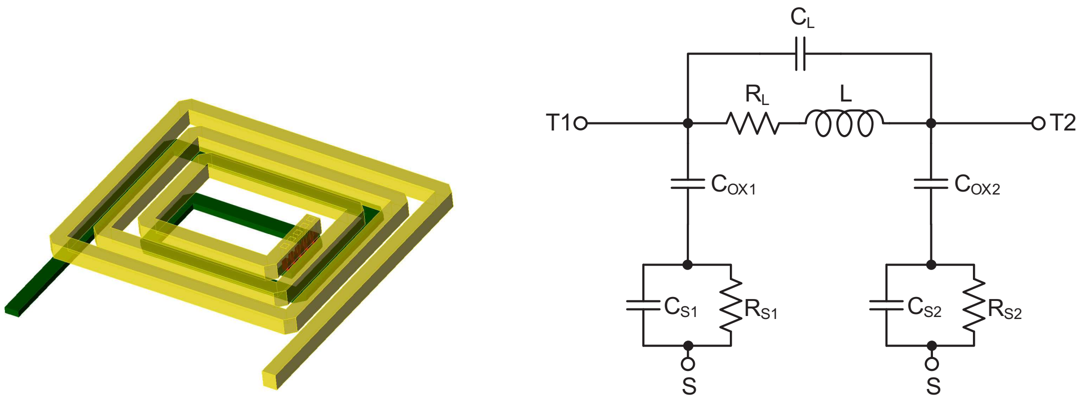
The equivalent circuit diagram of a MIM capacitor which is based on [Gruner 07] is shown in Fig. 2.20. The inductances $L_{con,T}$, $L_{con,B}$ and resitances $R_{con,T}$, $R_{con,B}$ model the parasitics caused by wiring of the capacitor. The value of the MIM capacitor itself is represented by C and losses and the dieletric are included by R_{DI} and C_{DI}. The capacitive substrate coupling is modeled by the capacitors C_{ST} and C_{SB}. It should be noticed that the value of C_{ST} would be much lower than the value of C_{SB} because the top electrode and metal layer are shielded from the substrate by the MIM capacitor, only fringe capacitances contribute to C_{ST}. Therefore, it would be acceptable to omit C_{ST} in the model without losing accuracy.

The MIM capacitor models provided by the foundries are much simpler than the one given in Fig. 2.20. The model of the SG253 includes only the MIM capacitor and a fixed series resistance. Substrate capacitances have to be extracted by RC parasitic extraction procedures and manually included into the design. Infineon includes the bottom substrate capacitance C_{SB} and series resistance for the vias and a resistor for the bottom electrode in the MIM capacitor model. Usually the components $L_{con,T}$, $L_{con,B}$, $R_{con,T}$ and $R_{con,B}$ are not included in a foundry model as the depend on the actual layout of the capacitor.

Inductors

Inductors are a key component in an amplifier design because of their versatile usability. Resonant tanks, DC decoupler and matching networks are examples for the use of inductors. Spatial combined, inductors can be used as magnetically coupled transformers to convert unbalanced to balanced signal and vice versa.

The design of inductors, if they are not provided by the foundry, depends on the requirements. High inductance values can be realized by closely spaced multiple turns. On the other hand, the self-resonance frequency will drop as the interwinding capacitance will be increased. High quality factor inductors are in general designed with thick top metals to reduce winding and losses, and hence, increase the quality factor. As thick top metals tracks have a minimum width and



(a) (b)

Figure 2.21: Inductor example with model, (a) – 3D view of an asymmetrical two layer inductor, (b) – Equivalent lumped circuit

spacing to each other, defined in the technology design rules, the overall inductor potentially needs a significant amount of area which increases the substrate coupling. Detail design procedures are presented in [Burghartz 03].

An example of an asymmetrical inductor which uses two metal layers is shown in Fig. 2.21(a). The equivalent lumped circuit is depicted in Fig. 2.21(b) [Tang 02]. Compared to the model of the resistor or capacitor, the substrate coupling modeling is enhanced by a resistor parallel to the substrate capacitance and an oxide coupling capacitor is included. As inductors are realized with the use of top metal layers, the oxide capacitance above the substrate can not be neglected anymore. Further, to take the conductivity of the substrate into account the resistors R_{s1} and R_{s2} are added. This additional network can also be added to the equivalent lumped circuit models for the resistor and capacitor to enhance the accuracy of the model. The inductance is represented by L and ohmic winding losses are denoted with R_L. The capacitance C_L models capacitive interwinding coupling.

In most cases the values for the components of the equivalent circuit are not derived analytically but with the use of electromagnetic simulations. The result is a model with far more lumped components as seen in the presented basic equivalent circuit model. The other possibility, which offer most electromagnetic simulation software, is to include the frequency-dependent characteristic of the inductor by a set of linear parameters, e.g. s-parameters into the simulation circuit. The advantage is the ease of use of such a model as only a block with input and output is added into the design. However, inadequate set up of the electromagnetic simulation can lead to a faulty set of linear parameters that is more complicate to recognize than non-physical component values in a lumped element model.

2.3 Circuit Topologies

The section covers the most relevant circuit topologies for X-band amplifiers, although the description is not limited to amplifiers in this frequency range. Furthermore, the influence of transistor biasing on output power and efficiency is on the example of the single transistor topology explained.

2.3.1 Single-Ended Amplifier

The simplest topology for an amplifier is the single-ended amplifier. The Fig. 2.22 depicts the basic circuit diagram. As the emitter is the reference for the input and output signal, the transistor configuration is called common emitter configuration. Also the use of a common base or common collector configuration is feasible for an amplifier, the common emitter configuration provides the highest power gain. A common base configuration has a high voltage gain but a current gain less than unity. Reverse in the case of a common collector configuration, the voltage gain is less than unity with a high current gain.

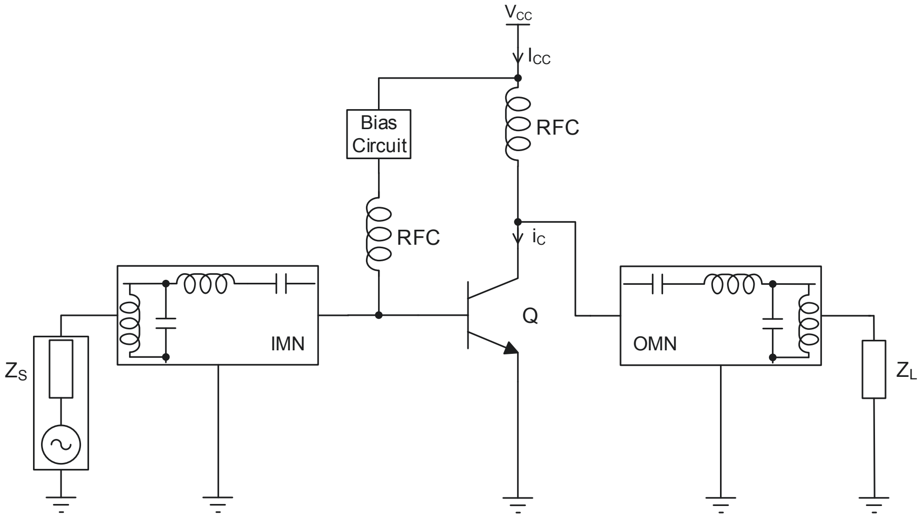


Figure 2.22: Prinicple schematic of a single-ended amplifier

The problem of this single-ended, or unbalanced, common emitter amplifier is the actual realization. As already stated, the emitter is the reference and any impedance Z_E between the transistor's emitter and the system reference will influence or even degrade the transistor performance. For integrated amplifiers, the parasitic emitter impedance can be found in the bond wire. The influence at DC is of minor concern, as the conductivity of the bond wire is high caused by gold or aluminum as bond wire material. Even at high current levels, the influence of the bond wire resistance can be mitigated by numerous bond wires placed in parallel. However, as the operating frequency starts to rise, the inductance of the bond wire leads to an increase of the magnitude of Z_E which will significantly affect the amplifier's performance. Also the benefit of parallel connected bond wires is limited when they are closely spaced to each other. Mutual coupling, as each bond wire carries the same current, confines the minimum overall inductance.

The input and output matching networks (IMN, OMN) enable impedance matching of the source and load impedance to the corresponding transistor impedances. The bias network sets the quiescent collector current.

Based on the value of the quiescent collector current I_C, the literature defines several classes of operation that are subclasses for the class of so-called linear-mode amplifiers. The counterpart is the class of switching-mode amplifiers which use the transistor in general as on/off switch for voltages or currents and is not further considered in this thesis.

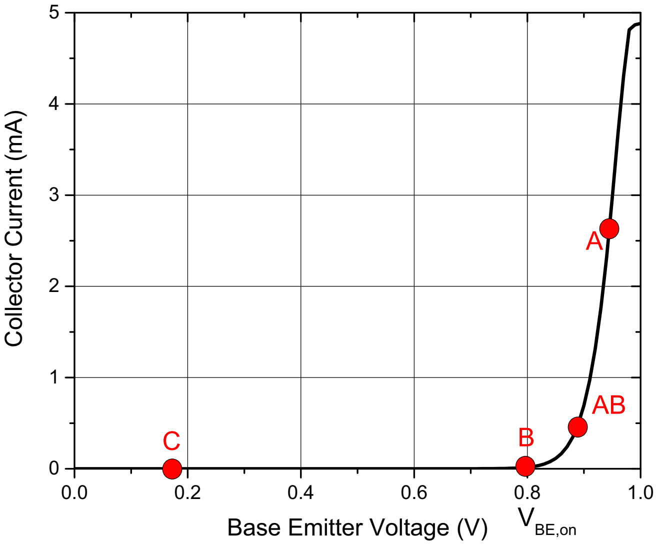


Figure 2.23: Classes assignments of linear-mode amplifiers in dependence of the quiescent collector current I_C

The subdivision of the class of linear-mode amplifiers in dependence of the quiescent collector current I_C is shown by a simulated transfer characteristic of a transistor in Fig. 2.23. Class C amplifiers have no quiescent current and the DC base emitter voltage is below the transistor turn-on voltage $V_{BE,on}$. Also negative values for V_{BE} are possible for this class. The base emitter voltage in class B operation is set near the turn-on voltage. Therefore, a negligible collector current is conducted. The value of the quiescent collector current $I_{C,A}$ for class A amplifier is half of maximum collector current I_{max}. Quiescent currents between class A and B ($I_{C,AB}$) result in class AB operation.

The consequence of different collector quiescent currents and biasing settings can be seen in Fig. 2.24 for all four classes, whereby it is assumed that harmonics

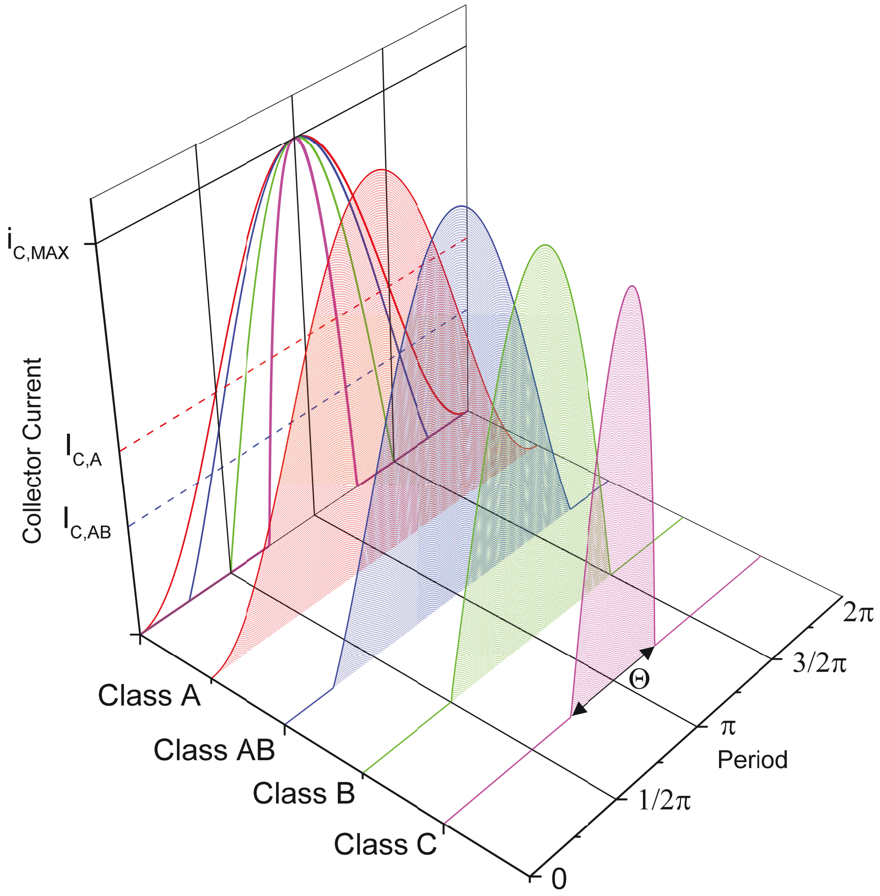


Figure 2.24: Conduction angle of the transistor depending on the biasing. The input signal strength varies with the biasing to maintain a peak current of I_{MAX}.

are shortened to ground and the input signal strength is variable. The period of transistor conduction decreases from class A to C compared to the full input signal cycle. Whereas the conduction period of class A is 2π, it is less than π for class C, as shown in Fig. 2.24. The conduction period of the transistor itself is specified as conduction angle Θ. It is possible to evaluate the performance as function of conduction angle for each class in terms of maximum output power and collector efficiency [Cripps 06]. For this, the collector current is described in the following as:

$$i_C(\theta) = \begin{cases} I_{C,Q} + (i_{C,MAX} - I_{C,Q})\cos\theta, & -\Theta/2 < \theta < \Theta/2 \\ 0, & -\pi < \theta < -\Theta/2, \Theta/2 < \theta < \pi \end{cases} \tag{2.92}$$

The DC current $I_{C,Q}$ is the quiescent current corresponding to the class. Furthermore, the collector current of (2.92) can be rewritten to:

$$i_C(\theta) = \frac{i_{C,MAX}}{1-\cos(\Theta/2)}\left(\cos\theta - \cos(\Theta/2)\right) \tag{2.93}$$

The DC and magnitude of the nth harmonic of the collector current can be obtained by Fourier transformation of (2.93):

$$\begin{aligned} I_C(\Theta) &= \frac{1}{2\pi}\int_{-\Theta/2}^{\Theta/2} i_C(\theta)\,d\theta = \frac{1}{2\pi}\int_{-\Theta/2}^{\Theta/2} \frac{i_{C,MAX}}{1-\cos(\Theta/2)}\left(\cos\theta - \cos(\Theta/2)\right)d\theta \\ &= \frac{i_{C,MAX}}{2\pi}\frac{2\sin(\Theta/2)-\Theta\cos(\Theta/2)}{1-\cos(\Theta/2)} \end{aligned} \tag{2.94}$$

$$\begin{aligned} I_{c,n}(\Theta) &= \frac{1}{2\pi}\int_{-\Theta/2}^{\Theta/2} i_C(\theta)\cos(n\theta)\,d\theta \\ &= \frac{1}{2\pi}\int_{-\Theta/2}^{\Theta/2} \frac{i_{C,MAX}}{1-\cos(\Theta/2)}\left(\cos\theta - \cos(\Theta/2)\right)d\theta \end{aligned} \tag{2.95}$$

From (2.95), the current at the fundamental frequency can be found to:

$$I_{c,1}(\Theta) = \frac{i_{C,MAX}}{2\pi}\frac{\Theta - \cos\Theta}{1-\cos(\Theta/2)} \tag{2.96}$$

Assuming that the voltage amplitude equals V_{CC}, the collector efficiency can be calculated with (2.94) and (2.96) to:

$$\eta(\Theta) = \frac{P_1}{P_{DC}} = \frac{V_{c,1}I_{c,1}(\Theta)}{2V_{CC}I_C(\Theta)} = \frac{I_{c,1}(\Theta)}{2I_C(\Theta)} = \frac{\Theta - \sin\Theta}{2\left(2\sin(\Theta/2) - \cos(\Theta/2)\right)} \tag{2.97}$$

The output power of the fundamental is given by:

$$P_1(\Theta) = v_{c,1}I_{c,1}(\Theta) = \frac{i_{C,MAX}V_{CC}}{2\pi}\frac{\Theta - \cos\Theta}{1-\cos(\Theta/2)} \tag{2.98}$$

The collector efficiency and output power of (2.97) and (2.98) are visualized in the diagram of Fig. 2.25. The maximum output is normalized to the output power of a class A amplifier.

From Fig. 2.25 is apparent that a class C amplifier with a conduction angle $\Theta = 0$ exhibits a collector efficiency of 100 % but provides no output power which is not in accordance with the definition of an amplifier. When the conduction angle is increased, the collector efficiency drops from 100 % to approximately 78.5 % for class B down to 50 % for a class A amplifier. The maximum of output power can be found in class AB operation, and although, class A and B provide the same output power, a class B amplifier would be more efficient relative to class A.

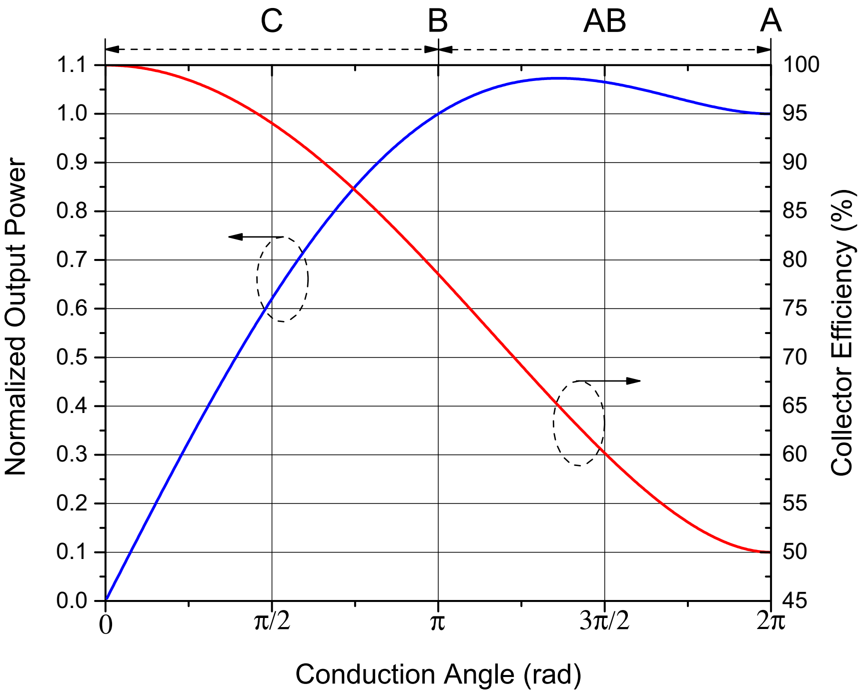


Figure 2.25: Comparison of maximum output power and collector efficiency for linear-mode amplifier subclasses

2.3.2 Cascode Amplifiers

The single-ended topology has the major drawback of low supply voltages that is limited by the breakdown voltage of the transistor. A further problem, as later seen, is the stability of such topology.

Already in the era of vacuum tubes, a topology was used that uses two vacuum tubes stacked on each other, the cascode. Applied on HBTs, the resulting circuit diagram is depicted in Fig. 2.26. A transistor Q_2 in common base configuration is stacked on top of the transistor Q_1 which is in common emitter configuration as in the single-ended topology.

The consequence of this arrangement is the possibility to use higher supply voltages for the circuit as the breakdown voltage of Q_2 adds to the breakdown voltage of Q_1. A further advantage is a reduced influence of the base collector capacitance of Q_1 because the voltage gain of the bottom transistor is decreased by the low input impedance at the emitter of the upper transistor. This circumstance is analyzed in more detail in Chapter 3.

But the cascode has also disadvantages; The supply voltage have to be higher compared to the single-ended design, even it is not necessary or unwanted. That is, to utilize a cascode topology, the supply voltage would be always higher compared to the singled-ended design which potentially will degrade the efficiency. Furhtermore, the connection of the reference potential at the base of Q_2 is critical,

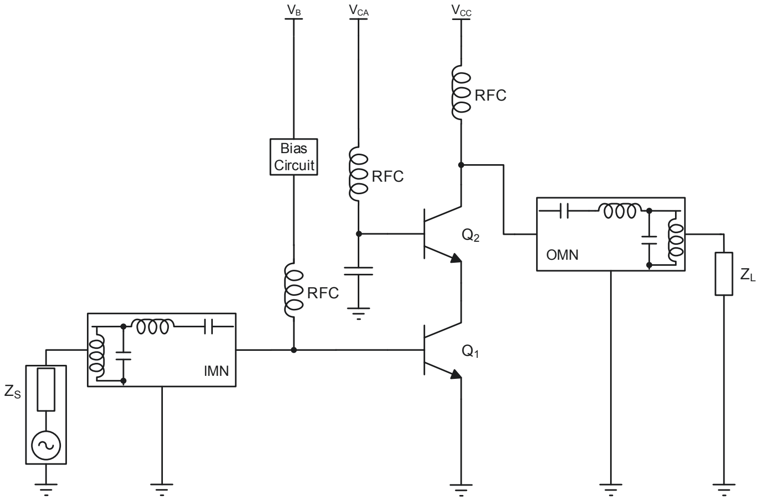


Figure 2.26: Circuit diagram of the cascode topology

any impedance between the base and the reference potential will deteriorate the circuit performance.

Despite of disadvantages, the cascode is one of the most used circuit topologies for LNAs and PAs because of its given advantages. The stacking is not limited to one transistor. And further increase of the output voltage swing can be realized by stacking numerous transistors, as demonstrated in [Liu 15]. The authors use a stack of five transistors.

2.3.3 Push–Pull Amplifiers

As seen on the previous description of the conduction angle, the transistor biased for class AB or B conducts less than a full signal cycle. Therefore, it is common at audio frequencies two use a complementary pair (npn - pnp) of transistors to amplify the signal through its complete period. The issue of pnp transistors at high frequencies is the lower hole mobility compared to the electron mobility which results in slower devices.

Instead of a pnp transistor, a second npn HBT is used and the input signal signal is splitted into two signals that are 180° out of phase, realized by a balun (balanced-to-unbalanced). At the output, both outphased signals are added in the balun to a single-ended, or unbalanced, signal. The concept is shown by the block diagram in Fig. 2.27 and called push–pull topology or differential topology. In most cases the baluns are realized by magnetically coupled transformers or LC-baluns that are presented later.

Compared to a single-ended topology, the push–pull topology allows to realize class AB and B amplifiers that amplify the complete signal but remain the increased efficiency relative to a class A amplifier. Furthermore, a virtual or AC

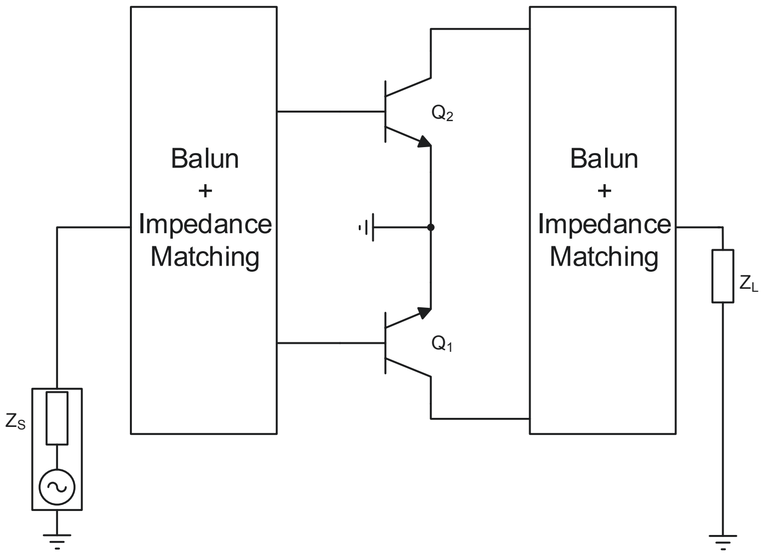


Figure 2.27: Block diagram of the push–pull topology

ground is introduced in the middle of both emitter contacts. The shown reference connection in Fig. 2.27 is only necessary for a DC current. A transformer-based balun has therefore the same virtual ground at the winding center and center taps can be used at the input to bias the transistors and apply the supply voltage at the output balun. Additional feeding inductors are needless. Depending on the type of balun, they can be simultaneously used for impedance matching that would reduce the circuit complexity. The major advantage is the increased output impedance which ease the effort on the impedance matching. Relative to a single-ended topology with equal output power, the output impedance of the push–pull topology is four times higher.

The main drawback of push–pull amplifiers is the balun itself. They increase the circuit complexity in the way that the balun performance significantly influence the circuit performance. Especially the balun at the amplifier's output has a substantial influence on the efficiency of the amplifier. Finally, realized as integrated LC-baluns or transformers, baluns can require a large amount of chip area.

2.3.4 Balanced Amplifiers

The last topology to be presented is the balanced topology, shown in Fig. 2.28. A quadrature coupler, e.g. Lange coupler, splits the the input signal into two with a phase shift of 90°. At the output, both signals are combined into one unbalanced signal.

Although rarely used for amplifiers at X-band frequencies, the topology offers some advantages that make it applicable for certain applications; Assuming both transistors have exactly the same input impedance and the matching networks

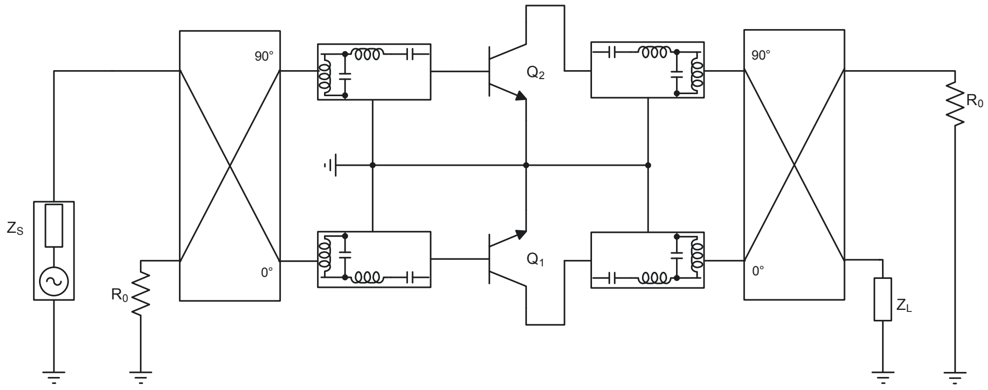


Figure 2.28: Block diagram of the balanced topology

are identical, any mismatch between the source impedance Z_S and the input impedance of the matching networks will be dissipated in the isolation resistor R_0 that has the same value as Z_S. Theoretically, no energy is reflected back to the source impedance due impedance mismatch. The same applies for the output. Therefore, even if the internal circuit is mismatched to the load and source impedance, balanced amplifiers exhibit a very good matching.

The disadvantages of the topology are:

- As the quadrature coupler realizes a 90° phase shift of a signal, it size depends on the wavelength. Therefore, it is more common to use this topology at mm-wave frequencies, not only because of the size but also the losses due long metal traces will be higher at lower frequencies.
- The heat dissipation in the isolation resistor can become significantly high which potentially causes an issue with the overall thermal management of the amplifier. Furthermore, if the resistor is integrated on-chip, it will require chip area.
- The topology has no virtual ground which makes it similar sensitive to parasitic emitter impedance as the single-ended topology.
- Class AB or B amplifiers are hard to realize, as the driving signals are not 180° out of phase.

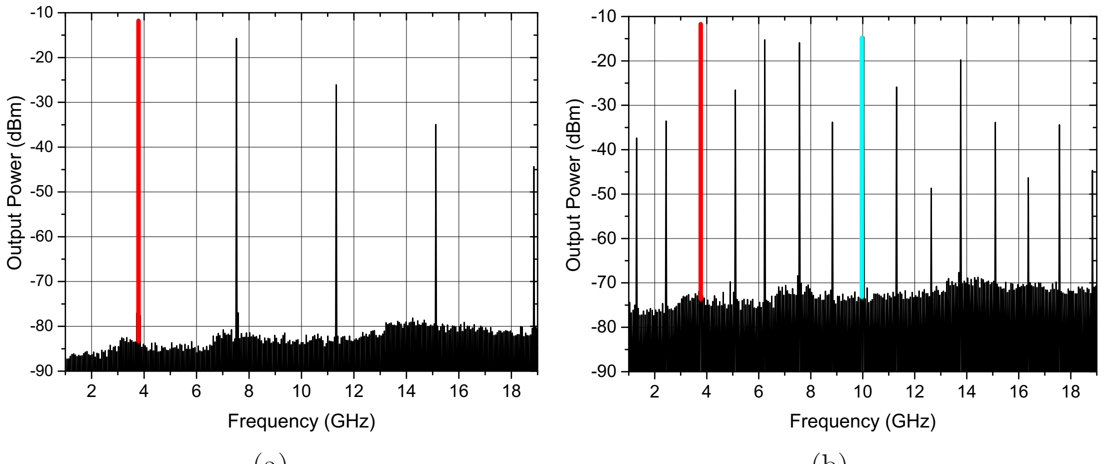
An example of a balanced amplifier with an integrated Lange coupler at X-band frequency is demonstrated in [Le 91].

Chapter 3

Instability and Passive Frequency-Selective Feedback

The stability of an amplifier is of crucial importance. Spurious oscillations, that result from an amplifier instability, not only degrade the performance of an amplifier itself and distort the received or the to be transmitted information but will also interfere with other wireless applications or disturb subsequent stages in the signal processing chain.

A measured example output spectrum of an unstable power amplifier without applied input signal is shown in Fig. 3.1(a). Despite the intended operating frequency of 10 GHz, the fundamental of oscillation can be found at a much lower frequency, red marked in Fig. 3.1(a). Furthermore, the spectrogram depicts harmonics of the oscillation frequency that raise the possibility of an interference with other communication channels.



(a)

(b)

Figure 3.1: Output spectrum of an oscillating amplifier, the oscillation frequency is red marked and the input signal frequency in blue, (a) – Without an input signal, (b) – With an applied 10 GHz input signal

The issue of unwanted emissions becomes even worse with an applied input signal, as seen in the spectrogram of Fig. 3.1(b). Intermodulation between the oscillation frequency, its harmonics and the input signal frequency results in a chaotic output spectrum of the amplifier. In this case, the amplifier is obviously not anymore useful. Therefore, a stability analysis of the amplifier is mandatory in order to predict and counteract instabilities in the design phase.

The first question that needs to be answered by a stability analysis is the origin of the instability, as the characteristics of the active devices and the circuit topology enable different types of oscillation that will be summarized in the next section. Subsequently, the actual circumstances that lead to instability, and therefore to an amplifier oscillation, must be investigated in detail to use suitable countermeasures that are intended to improve the stability of the circuit. Based on this scheme, the amplifier instability caused by the implemented SiGe HBT is analyzed in the following and a stabilization method is introduced which differs from the common stabilization methods for low noise and power amplifiers.

3.1 Oscillation Types of Radio Frequency Amplifiers

The instability sources of radio frequency amplifier can be classified into three main types that are summarized in the following:

Even mode oscillation The most common type is the even mode oscillation which is the result of a feedback path from the output to the input or vice versa in conjunction with an active device. The feedback itself can be caused by an intrinsic transistor feedback or due to an external feedback path by circuit components or structures. A convenient analysis to determine the oscillation tendency of such system – feedback and amplifying device – is provided by a system theory based approach. For this, the block diagram of Fig. 3.2 [Hall 90] is considered.

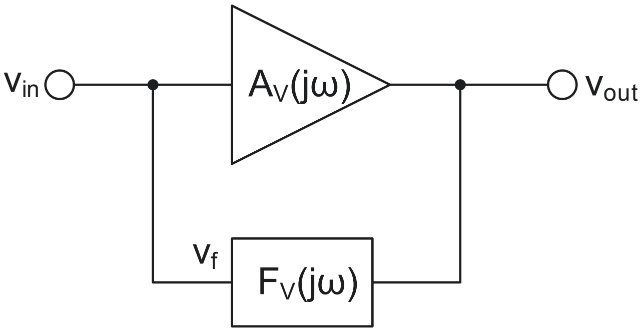


Figure 3.2: Simplified schematic of a feedback amplifier

The transfer function of the voltage amplifier with voltage gain $A_V(j\omega)$ and the feedback with the frequency-dependent transfer function $F_V(j\omega)$ is given as follow:

$$\begin{aligned} S\left(j\omega\right) &= \frac{v_{out}\left(j\omega\right)}{v_{in}\left(j\omega\right)} = \frac{A_V(j\omega)\left(v_{in}\left(j\omega\right)+v_f\left(j\omega\right)\right)}{v_{in}\left(j\omega\right)} \\ &= \frac{A_V(j\omega)\left(v_{in}\left(j\omega\right)+v_{out}\left(j\omega\right)F_V(j\omega)\right)}{v_{in}\left(j\omega\right)} = \frac{A_V(j\omega)}{1-F_V(j\omega)A_V(j\omega)} \end{aligned} \tag{3.1}$$

Decisive for the oscillation behavior of the system is the open-loop transfer function $F_V(j\omega)A_V(j\omega)$ in (3.1). A self-sustaining oscillation without applied input signal can be obtained if the magnitude of the open-loop transfer function equals unity:

$$|F_V(j\omega)A_V(j\omega)| = 1 \tag{3.2}$$

In the absence of an input signal, the start-up oscillation power will be provided by noise. It is obvious that in this case (3.2) will not result in a recognizable oscillation as the noise power is very small and the amplitude will not grow. Therefore, (3.2) needs to be rewritten to provide a start-up condition which allows the oscillation amplitude to grow:

$$|F_V(j\omega)A_V(j\omega)| > 1 \tag{3.3}$$

Furthermore, the amplifier and feedback network will potentially cause a phase shift of the feedback signal which could prevent the oscillation although the condition of (3.2) is satisfied. The necessary phase condition, as second oscillation condition, is derived by splitting (3.2) into its real and imaginary part:

$$\Re\{F_V\left(j\omega\right)A_V(j\omega)\} + \Im\{F_V\left(j\omega\right)A_V(j\omega)\} = 1 \tag{3.4}$$

Both components of (3.4) can be now equated:

$$\Re\{F_V\left(j\omega\right)A_V(j\omega)\} = F_V\left(\omega\right)A_V(\omega) = 1 \Rightarrow A_V(\omega) = \frac{1}{F_V\left(\omega\right)} \tag{3.5}$$

$$\Im\{F_V\left(j\omega\right)A_V(j\omega)\} = F_V\left(\omega\right)A_V(\omega) = 0 \tag{3.6}$$

The consequence of (3.6) is that a stable oscillation require an overall loop phase shift of multiple of 2π for a positive feedback. If both conditions, (3.2) and (3.6) and known as Barkhausen stability criterion, are simultaneously satisfied at a specific frequency ω, the system will exhibit a stable self-sustaining oscillation. However, such circuit conditions are mostly intended and used in the design of oscillators. In contrast, amplifiers are not designed to oscillate, and therefore, will mostly not satisfy (3.2) and (3.6) simultaneously. It is much more probable that the feedback exhibits the necessary phase shift from (3.6) and that the open loop gain is given by (3.3). The result is an oscillation that grows in amplitude which will be then either limited by the level of supply voltage or by a reduction of the active device gain due high level injection.

Instabilities due to even mode oscillations can be easily predicted by the use of simulation software because they do not depend on input signal strengths or specific transistor combining schemes. The system of Fig. 3.2 can be therefore linearized and considered as linear two-port network which is fully describable by means of a frequency-dependent set of linear two-port parameters. It is common in RF amplifier designs to utilize scattering parameters, or S-parameters, as two-port parameters that allow to use predefined stability metrics. Widely used is the Rollet stability factor K which is given by:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_\Delta|^2}{2\,|S_{21}S_{12}|} \tag{3.7}$$

$$S_\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{3.8}$$

By definition, the system is considered as unconditionally stable for arbitrary source and load impedances if the K-factor is larger than unity and an auxiliary condition, for example $|S_\Delta| < 1$, is fulfilled over the entire frequency spectrum [Ohtomo 95]. If the stability factor is less than unity at some frequencies, the system is considered as conditional stable because certain source/load impedance values exists that enable a system's instability. For the sake of completeness, the two necessary stability conditions of Rollet stability factor are reduced to one sufficient condition by the μ-factor [Ohtomo 95]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* S_\Delta| + |S_{21}S_{12}|} \tag{3.9}$$

Similar to the stability criteria of the K-factor, a μ-factor larger than unity characterize an unconditionally stable system, without the necessity to consider auxiliary conditions.

Odd mode oscillation The counterpart of even mode oscillations are odd mode or push–pull oscillations [Penn 15]. They potentially arise between parallel connected transistors (see Fig. 3.3) that have slightly different intrinsic characteristics, by for example process variations, or are loaded by different source or load impedances due unsymmetrical transistor feeder structures with a certain electrical length.

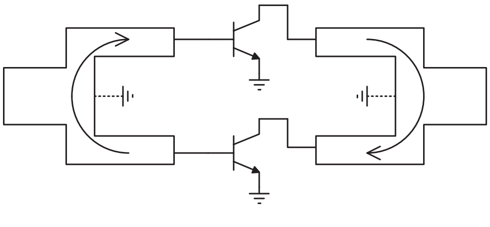


Figure 3.3: Simplified schematic for odd mode oscillation

The result of these asymmetries between the parallel connected transistors are slightly different collector voltages that enable a loop oscillation with 180° outphased signals between both transistors by the nonideal finite isolation between them or by their intrinsic feedbacks.

In contrast to even mode oscillations, odd mode oscillations are not observable from the outside, assuming ideal linear operating transistors. As seen in Fig. 3.3, the nature of the resulting 180° outphased signals between both transistors introduces a virtual ground at the feeding structures. Consequently, the oscillation signal will not be conducted to the input and output of the transistor array. In reality, odd mode oscillations can be observed by the harmonic content of the oscillation. It should be mentioned that SiGe HBT amplifiers presented in this thesis are rarely confronted with the issue of odd mode oscillations, although these amplifiers utilize numerous parallel connected transistors. The spacing between individual transistors is comparably small and complex feeding structures that encourage odd mode oscillations are not used. However, with increasing operating frequency the analysis for odd mode oscillations can no longer be neglected as presented in [Chen 13], and the analysis of odd mode oscillation becomes even more demanding as the number of parallel combined transistors increases, as depicted in Fig. 3.4. Already the combination of four transistors enables one even mode and three different odd mode oscillation possibilities that need to be investigated.

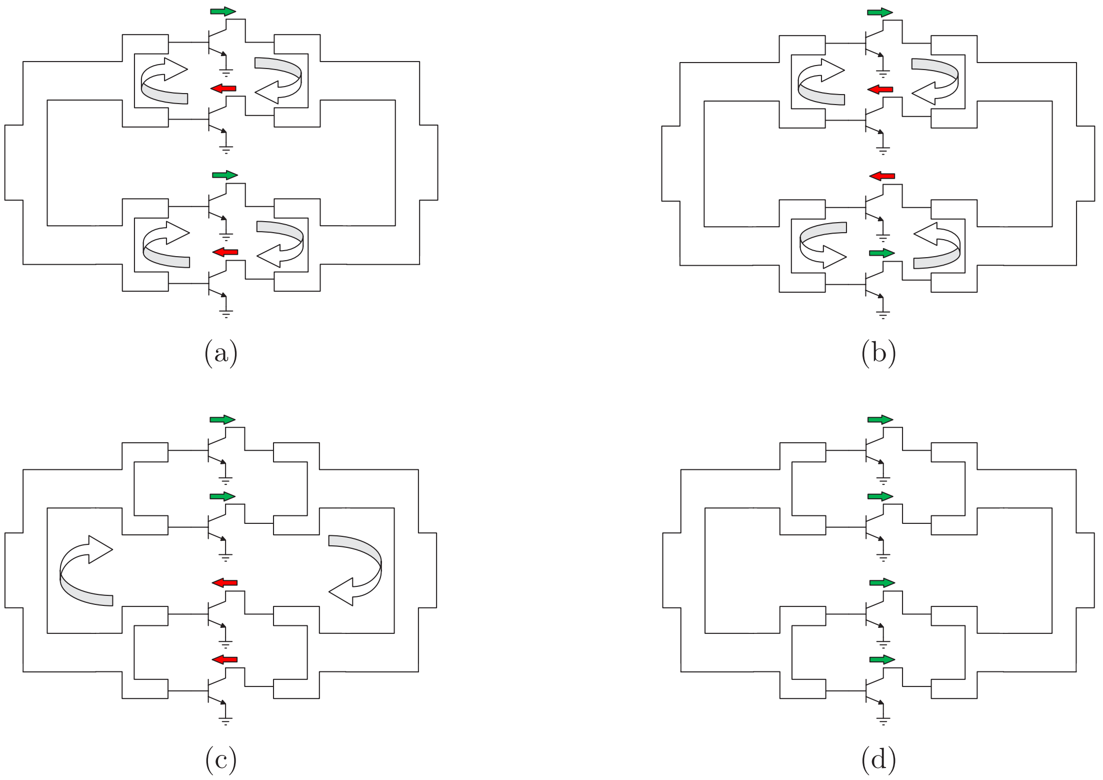

(a) (b) (c) (d)

Figure 3.4: Odd and even oscillation modes of four parallel connected transistors, (a) – Odd mode 1, (b) – Odd mode 2, (c) – Odd mode 3, (d) – Even mode

After even mode oscillations are excluded, the first choice to detect odd mode oscillations would be transient analysis of the circuit but without the knowledge for the reason of odd mode oscillations and increasing circuit complexity, transient simulations could become tremendously time-consuming. A more comfortable analysis is provided by forcing the virtual ground nodes in Fig 3.3 to a real ground and investigate the input reflection coefficient as function of frequency. Values greater than unity with a simultaneous phase shift of 180° [Freitag 88] will indicate frequencies of odd mode oscillation.

Parametric oscillation A further type of oscillation is the parametric oscillation which results in general from a modulation of a nonlinear reactive component in conjunction with a resonant tank by a signal. The tendency of an oscillation behavior depends on the strength of the modulation signal, which is the parameter of this type of oscillation. It is already known from varactor multipliers that certain input signal strengths cause subharmonic oscillations by pumping a nonlinear capacitance [Leeson 66]. In the case of bipolar transistors or HBTs, the nonlinear voltage-dependent characteristic of the base collector capacitance driven by a strong input signal at the base is the cause of such subharmonic oscillations in conjunction with tuned matching networks. A qualitative general analysis of parametric oscillation of bipolar transistors can be found in [Lohrmann 66].

The issue of parametric oscillations in HBTs is that their onset depends on the input signal strength. At small signal strengths, the base collector capacitance exhibits a almost linear dependence on the voltage and parametric oscillation will not occur. It can not be therefore predicted by a small signal analysis. Only time-consuming transient analysis or extended analysis of the circuit transfer function, as demonstrated in [Jugo 01] and [Mons 99], allow to estimate the tendency of circuit for parametric oscillations.

The presented types of oscillation and their causes are the main reasons for unstable RF amplifiers although further types exists, as low frequency oscillation due to the bias network [Gilmore 03] or oscillation enabling feedback loops of the power supply network [Unterweissacher 07].

3.2 Intrinsic Transistor Feedback

The main stability issue of the later presented amplifiers arises from the intrinsic transistor feedback which is the result of the base collector capacitance. It is known from the literature that this feedback causes substantial stability issues with certain source or load impedance values. Although a basic analysis can be found, among others, in [Cripps 06], it is necessary to get a deeper insight to design and implement the passive frequency-selective feedback, presented in the next section.

As the transistor is the amplifying device and the base collector capacitance provides the feedback path, the possible resulting instability is considered to the type of even mode oscillations. Considering the small signal equivalent circuit diagram in Fig. 3.5 it becomes obvious that this instability type can be considered as even mode oscillation. Consequently, the oscillation tendency is independent of input signal strength or amplifier topology, and can be therefore analyzed by the small signal equivalent circuit diagram in Fig. 3.5. The circuit components are equal to the components of the previously present hybrid-pi model and an arbitrary source and load impedance is denoted by Z_S and Z_L.

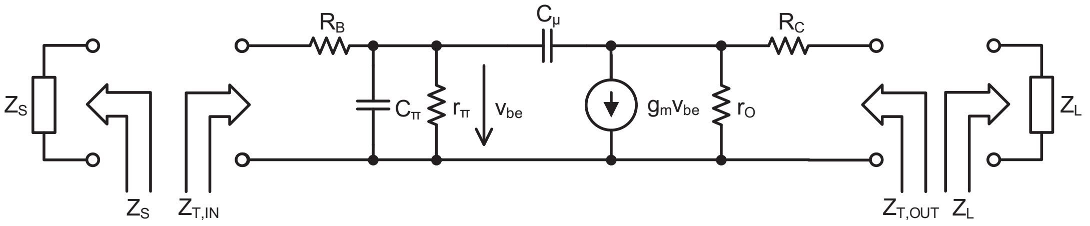


Figure 3.5: Small signal equivalent circuit diagram of a single transistor

The input impedance of the transistor $Z_{T,in}$ can be derived by placing a voltage source at the base and determine the current flowing into the base:

$$Z_{T,in} = \frac{v_{in}}{i_{in}} = R_B + \left(\frac{1}{Z_\pi} + \frac{g_m Z_O + 1}{Z_O + Z_\mu} \right)^{-1} \tag{3.10}$$

The individual impedances in (3.10) are given by:

$$Z_\pi = \left(\frac{1}{r_\pi} + j\omega C_\pi \right)^{-1} \tag{3.11}$$

$$Z_\mu = \frac{1}{j\omega C_\mu} \tag{3.12}$$

$$Z_O = \left(\frac{1}{r_O} + \frac{1}{R_C + Z_L} \right)^{-1} \tag{3.13}$$

Now, instead of using the presented loop analysis approach to analyze the stability, the negative resistance approach is used. For this, Fig. 3.6 shows a scheme of an amplifier terminated with a load impedance Z_L and a signal generator with an impedance Z_S.

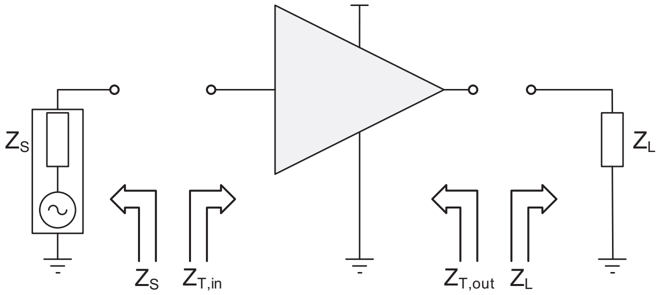


Figure 3.6: Scheme for the stability analysis by negative resistance

If the amplifier and generator impedance satisfy following conditions [Vendelin 05]

$$\Re\{Z_S\} + \Re\{Z_{T,in}\} = 0 \tag{3.14}$$

$$\Im\{Z_S\} + \Im\{Z_{T,in}\} = 0 \tag{3.15}$$

the amplifier will be able to oscillate. However, a start-up of oscillation is not possible by (3.14), it needs to satisfy:

$$\Re\{Z_S\} + \Re\{Z_{T,in}\} < 0 \tag{3.16}$$

Considering the output of the amplifier, the oscillation conditions are provided by

$$\Re\{Z_L\} + \Re\{Z_{T,out}\} = 0 \tag{3.17}$$

$$\Im\{Z_L\} + \Im\{Z_{T,out}\} = 0 \tag{3.18}$$

$$\Re\{Z_L\} + \Re\{Z_{T,out}\} < 0 \tag{3.19}$$

with (3.19) as start-up condition.

The first part of the analysis will be focused on the reactance of source and load impedance and the resulting input and output impedance of the transistor. For this, the equivalent circuit model is simplified by omitting any resistive elements, and therefore, (3.10) simplifies to:

$$Z_{T,in} = \left(j\omega C_\pi + \frac{g_m Z_L + 1}{Z_L - j\left(\omega C_\mu\right)^{-1}} \right)^{-1} \tag{3.20}$$

Considering the three extrema of the load impedance

$$Z_L = \begin{cases} R_L & \text{, resistive} \\ -jX_L & \text{, capacitive} \\ +jX_L & \text{, inductive} \end{cases} \tag{3.21}$$

the real part of (3.20) results into:

$$\Re\{Z_{T,in}\} = \begin{cases} \dfrac{R_L(R_L g_m + 1)}{\Delta_A} & \text{, resistive} \\ \dfrac{X_L g_m}{\left(X_L + (\omega C_\mu)^{-1}\right)} \cdot \dfrac{1}{\Delta_B} & \text{, capacitive} \\ \dfrac{X_L g_m}{\left(X_L - (\omega C_\mu)^{-1}\right)} \cdot \dfrac{1}{\Delta_C} & \text{, inductive} \end{cases} \tag{3.22}$$

$$\Delta_A = \left(R_L(R_L g_m + 1)\right)^2 + \left(R_L + (\omega C_\mu)^{-1}\right)^2 \left(\omega C_\pi + \frac{R_L g_m + 1}{\omega C_\mu \left(R_L + (\omega C_\mu)^{-1}\right)^2}\right)^2$$

$$\Delta_B = \left(\frac{X_L g_m}{-X_L - (\omega C_\mu)^{-1}}\right)^2 + \left(\omega C_\pi - \frac{1}{-X_L - (\omega C_\mu)^{-1}}\right)^2$$

$$\Delta_C = \left(\frac{X_L g_m}{X_L - (\omega C_\mu)^{-1}}\right)^2 + \left(\omega C_\pi - \frac{1}{X_L - (\omega C_\mu)^{-1}}\right)^2$$

It becomes obvious from (3.22) that only an inductive load impedance will result in a negative input resistance of the transistor because a load reactance smaller than the feedback reactance $(\omega C_\mu)^{-1}$ results in a negative denominator. This does not necessarily mean that the amplifier is able to oscillate because the oscillations conditions ((3.14), (3.15) and (3.16)) have to be fulfilled. Replacing X_L with ωL_L and solving the following equation

$$\Re\{Z_{T,in}\} = -R_S,\ 0 < \omega < \frac{1}{\sqrt{L_L C_\mu}} \tag{3.23}$$

results in the frequency value at which the transistor impedance equals the real part of the source impedance R_S for a given inductance L_L:

$$\begin{aligned} \omega_{Rs} = \frac{1}{\sqrt{2}}\frac{1}{C_\pi}\Bigg[& \frac{2C_\pi}{L_L}\left(1 + \frac{C_\pi}{C_\mu}\right) - g_m\left(g_m + \frac{1}{R_S}\right) \\ & + g_m\sqrt{g_m\left(g_m + \frac{2}{R_S}\right) - \frac{4C_\pi}{L_L}\left(1 + \frac{C_\pi}{C_\mu} + \frac{1}{R_S g_m}\right) + \frac{1}{R_S^2}}\ \Bigg]^{1/2} \end{aligned} \tag{3.24}$$

In the case of a non-real solution for (3.24), the value of $\Re\{Z_{T,in}\}$ will not satisfy (3.23), i.e. $|\Re\{Z_{T,in}\}| < R_S$ for $0 < \omega < (\sqrt{L_L C_\mu})^{-1}$. Although the amplifier exhibits a negative input resistance, the amplifier is not able to oscillate for a given R_S. As (3.24) only provides a steady-state solution, the start-up oscillation condition (3.16) will be fulfilled at frequencies smaller than ω_{Rs} if (3.24) results in a real solution.

To complete the analysis at the transistor's input, the condition of the second oscillation criterion from (3.15) has to be determined. If the input transistor reactance satisfies

$$\begin{aligned} X_S &= -\Im\{Z_{T,in}\} = \left(\omega C_\pi - \frac{1}{\omega L_L - (\omega C_\mu)^{-1}}\right)\frac{1}{\Delta_C},\ 0<\omega\leq\omega_{Rs} \\ \Delta_C &= \left(\frac{\omega L_L g_m}{\omega L_L - (\omega C_\mu)^{-1}}\right)^2 + \left(\omega C_\pi - \frac{1}{\omega L_L - (\omega C_\mu)^{-1}}\right)^2 \end{aligned} \tag{3.25}$$

for a given source reactance X_S, the transistor will oscillate at a frequency in the range between zero and ω_{Rs}.

Similar to the analysis at the transistor's input, the oscillation tendency at the output of the transistor in dependence of the source impedance is in the following investigated by means of the criteria from (3.17)–(3.19). The output impedance of the transistor $Z_{T,out}$ of the transistor is given by:

$$Z_{T,out} = \frac{1+\dfrac{C_\pi}{C_\mu}+\dfrac{1}{j\omega C_\mu Z_S}}{g_m + j\omega C_\pi + \dfrac{1}{Z_S}} \tag{3.26}$$

The resulting resistive component of the output impedance for the three source impedance, equal to the load extrema in (3.21), extrema are:

$$\begin{aligned} \Re\{Z_{T,out}\} &= \begin{cases} \dfrac{g_m}{R_S}\left(1+\dfrac{C_\pi}{C_\mu}\right)\dfrac{1}{\Delta_{A,O}} & \text{, resistive} \\ g_m\left(1+\dfrac{1}{C_\mu}\left(C_\pi+\dfrac{1}{\omega X_S}\right)\right)\dfrac{1}{\Delta_{B,O}} & \text{, capacitive} \\ g_m\left(1+\dfrac{1}{C_\mu}\left(C_\pi-\dfrac{1}{\omega X_S}\right)\right)\dfrac{1}{\Delta_{C,O}} & \text{, inductive} \end{cases} \\ \Delta_{A,O} &= \left(gm + R_S^{-1}\right)^2 + (\omega C_\pi)^2 \\ \Delta_{B,O} &= g_m^2 + \left(\omega C_\pi + X_S^{-1}\right)^2 \\ \Delta_{C,O} &= g_m^2 + \left(\omega C_\pi - X_S^{-1}\right)^2 \end{aligned} \tag{3.27}$$

The result of (3.27) is comparable to the result for the input impedance in (3.22), the resistive component of $Z_{T,out}$ becomes negative for an inductive source impedance which is smaller than the reactance of C_π. The frequency at which

$$\Re\{Z_{T,out}\} = -R_L,\, 0 < \omega < \frac{1}{\sqrt{L_L C_\pi}},\, ,\, X_S = \omega L_S \tag{3.28}$$

is fulfilled results to:

$$\begin{aligned}\omega_{Rl} =& \frac{1}{\sqrt{2}} \frac{1}{C_\pi} \sqrt{C_\pi \left(\frac{2}{L_S} - \frac{g_m}{C_\mu R_L} \right) - g_m \left(g_m + \frac{1}{R_L} \right) + g_m \sqrt{-\frac{4C_\pi}{L_S} \left(1 + \frac{1}{R_L g_m} \right)}} \\ & \overline{\overline{+ \frac{C_\pi}{C_\mu R_L^2} \left(\frac{C_\pi}{C_\mu} + \frac{C_\mu}{C_\pi} + 2 \right) + \frac{2g_m}{R_L} \left(\frac{g_m R_L}{2} + \frac{C_\pi}{C_\mu} + 1 \right)}}\end{aligned} \tag{3.29}$$

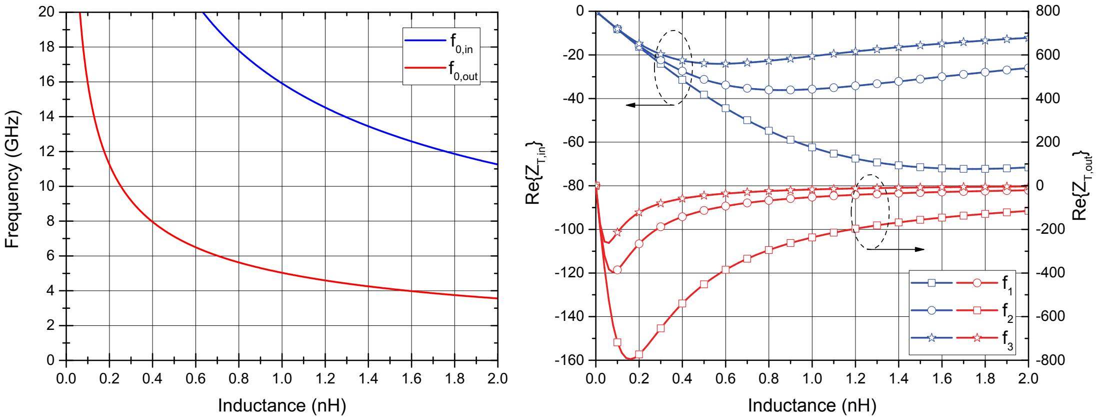
As already stated for the expression (3.24), a non-real value for ω_{Rl} indicates that the absolute value of $\Re\{Z_{T,out}\}$ is smaller than the resistive component of the load impedance, and (3.17) will be not satisfied. In the case of a real solution, the start-up oscillation condition (3.19) is fulfilled at frequencies below ω_{Rl}. The last step is to specify the value of the load reactance X_L by means of (3.18) which enables the oscillation of the transistor:

$$\begin{aligned} X_L = -\Im\{Z_{T,in}\} &= \left(1 + \frac{1}{C_\mu} \left(C_\pi - \frac{1}{\omega^2 L_S} \right) \right) \left(\omega C_\pi - \frac{1}{\omega L_S} \right) \frac{1}{\Delta_{C,O}} \\ 0 < \omega \leq \omega_{Rl},\, \Delta_{C,O} &= g_m^2 + \left(\omega C_\pi - (\omega L_S)^{-1} \right)^2 \end{aligned} \tag{3.30}$$

Two conclusions can be drawn from (3.22) and (3.27) in dependence of a varying inductive load reactance which is represented by an inductance L:

- The upper limit of the frequency range in which a negative resistance exists varies with the value of the inductance. In the case of the input resistance $\Re\{Z_{T,in}\}$, the limit is given by $\sqrt{LC_\mu}^{-1}$, the upper limit for $\Re\{Z_{T,out}\}$ is $\sqrt{LC_\pi}^{-1}$. Considering a transistor in active mode (($V_{BE} < V_{CB}$), C_π will be larger as C_μ because it is composed of the diffusion and junction capacitance, instead of only the junction capacitance in the case of C_μ. Therefore, the upper frequency limit for a negative transistor output resistance will be always lower, as seen in Fig. 3.7(a), where the graph depicts the upper frequency limit for a negative input and output resistance of the transistor.
- The minimum value of $\Re\{Z_{T,in}\}$ and $\Re\{Z_{T,out}\}$ depends on the inductance value and decreases with increasing frequency at which the minimum is observed, as shown in Fig. 3.7(b). A larger inductance results a smaller negative resistance at a lower frequency which results in a greater probability that the start-up oscillation criteria (3.16) and (3.19) become fulfilled.
- A comparison of (3.22) and (3.27) reveals that the oscillation tendency due to a negative output resistance is larger than due to the negative input

resistance because the minimum value for the output resistance is larger, also shown in Fig. 3.7(b).



(a) (b)

Figure 3.7: Upper frequency limit for a negative resistance and negative input/output transistor resistance as function of load/source reactance with the use of the simplified model ($C_\mu = 0.1\,\mathrm{pF}$, $C_\pi = 1\,\mathrm{pF}$, $g_m = 1\,\mathrm{S}$), (a) – Upper frequency limit f_0 for $\Re\{Z_{T,in}\}$ and $\Re\{Z_{T,out}\} \leq 0$, (b) – Value of $\Re\{Z_{T,in}\}$ and $\Re\{Z_{T,out}\}$ at different frequencies, $f_1 < f_2 < f_3 < f_0$

After analyzing the oscillation tendency by a simplified transistor model, two questions need still to be answered; Where does the inductance comes from and how is the oscillation tendency of a real transistor, represented by a more advanced model?

A source or load inductance is mainly the result of parasitic inductances caused by matching networks, e.g transformers, interconnection wirings or bond wires. In the frequency range of the circuit operation they are considered by resonant tanks that significantly reduce their influence in this frequency range. However, with decreasing frequency the inductive characteristic will rise. An example is given by the tee model of a double-tuned lossless transformer, which will be used for instance in X-band PAs, in Fig. 3.8(a). The inductance L_{M12} is the mutual inductance of the transformer primary (L_{pr}) and secondary winding (L_{se}), and the inductances L_1 and L_2 represent leakage inductance due non-ideal coupling. Their values are given by:

$$L_{M12} = k\sqrt{L_{pr}L_{se}},\ k:\ \text{coupling coefficient, } 0 \leq k \leq 1 \tag{3.31}$$
$$L_1 = L_{pr} - L_{M12} \tag{3.32}$$
$$L_2 = L_{se} - L_{M12} \tag{3.33}$$

The leakage inductances are brought into resonance by the capacitors C_1 and C_2 at a frequency in the operating frequency range, for instance at the operating center frequency. Only by considering the tee model it is obvious that at frequencies below the resonance frequency the transformer will behave inductive, and at frequencies above, the capacitors will dominate the transformer's characteristic.

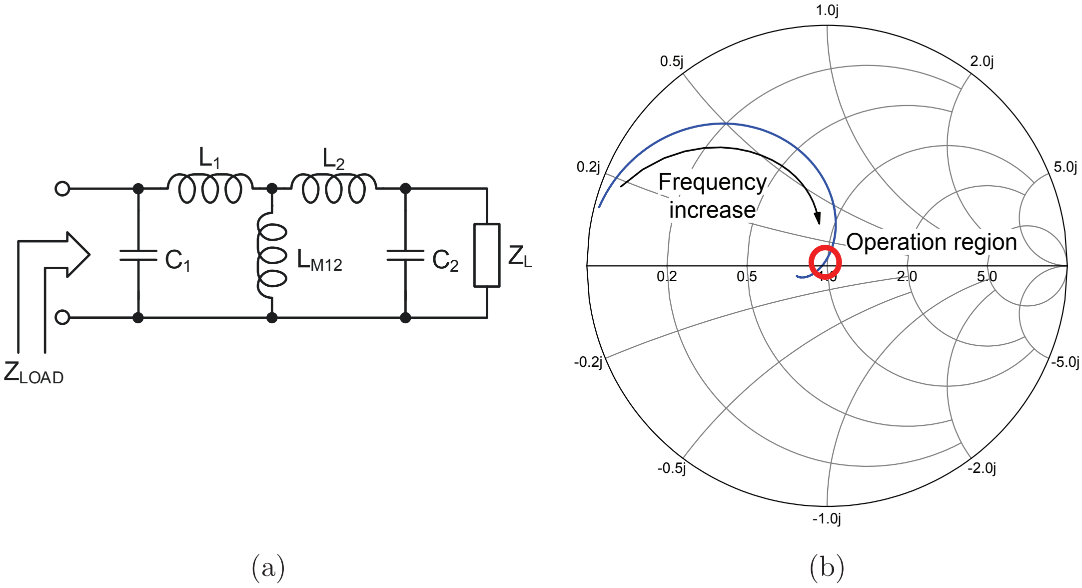


Figure 3.8: Doubled-tuned transformer, (a) – Equivalent tee model, (b) – Impedance Z_{load} versus frequency

The Smith chart in Fig. 3.8(b) confirms the stated frequency dependent characteristic of the transformer. Furthermore, it is shown that at very low frequencies the load impedance Z_L results in a small transformed impedance Z_{Load}. Therefore, the assumption of a pure inductive load/source reactance in the previous analysis is not only a simplification but also applicable to some extend. In the case of bond wires or different matching networks as source of inductance, the analysis will lead to similar results as the presented with the example of a transformer as inductance source.

The second question will be answered by an extended transistor small signal model, shown in Fig. 3.9. The intrinsic transistor model includes now the previously omitted resistive components and wiring capacitances (C_{BE}, C_{CE}, C_{BC})

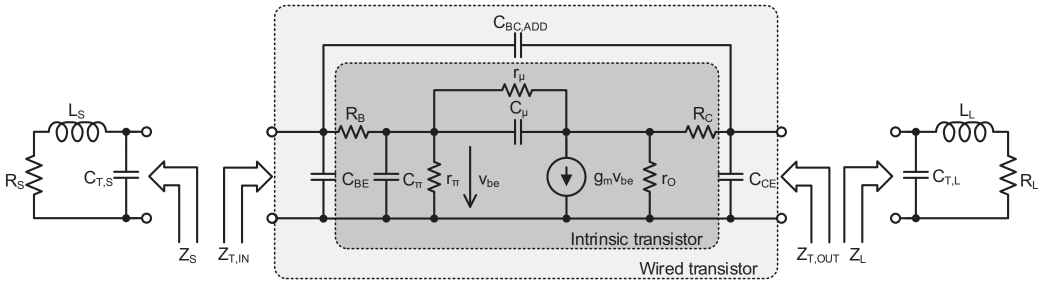


Figure 3.9: Extended small signal equivalent circuit for IHP transistors

are added, as the they will affect the oscillation tendency. The circuit is intended to operate at 10 GHz, and thus, arbitrary parasitic source and load inductances, represented by L_S and L_L, are brought into resonance by $C_{T,S}$ and $C_{T,L}$ at $f_{res} = 10\,\text{GHz}$ by:

$$C_{T,S} = \left(L_S \left(4\left(\pi f_{res}\right)^2 + \left(\frac{R_S}{L_S}\right)^2 \right) \right)^{-1} \tag{3.34}$$

$$C_{T,L} = \left(L_L \left(4\left(\pi f_{res}\right)^2 + \left(\frac{R_L}{L_L}\right)^2 \right) \right)^{-1} \tag{3.35}$$

Furthermore, the transistor is assumed to be matched at the input and output by $R_S = \Re\{Z_{T,in}\}$ and $R_L = \Re\{Z_{T,out}\}$ with $L_S = L_L = 0$. The values of the model components are derived from the IHP transistor "npnH3" operating at a low current density, which is used later in the presented power amplifier designs. The emitter area A_E is $0.185\,\mu\text{m}^2$. The model component values are shown in Tab. 3.1.

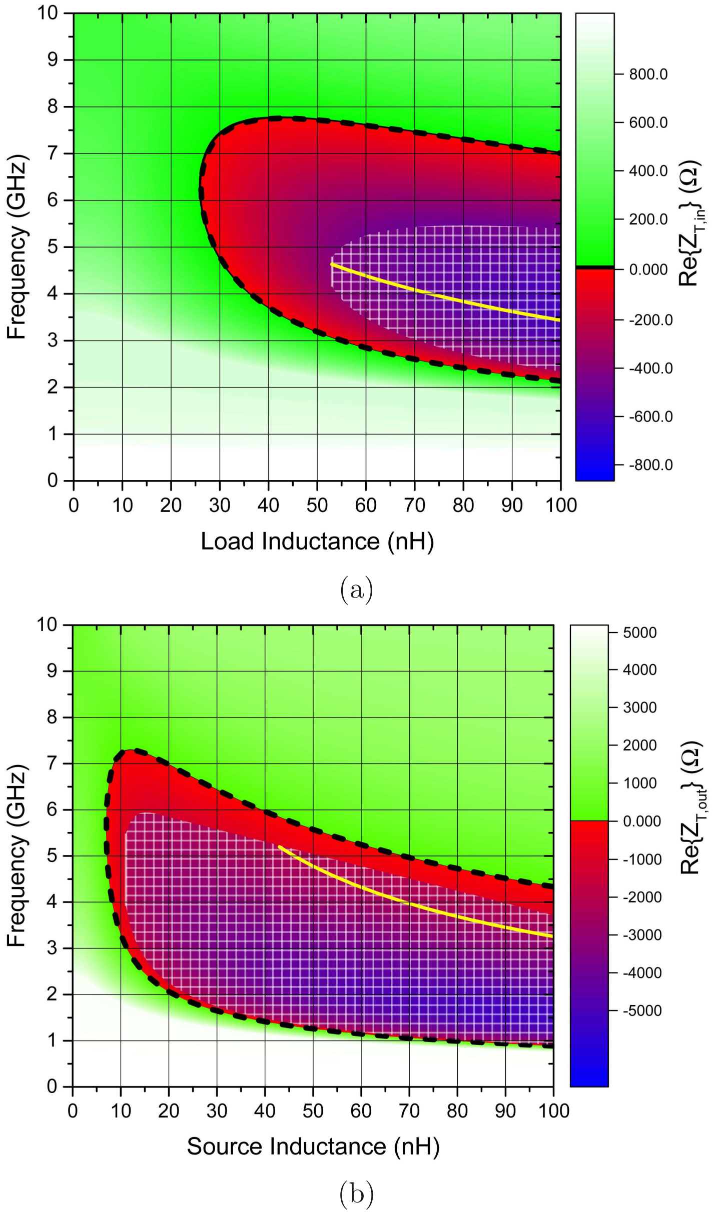
Table 3.1: Components values for the equivalent circuit diagram of Fig. 3.9 at 10 GHz and $A_E = 0.185\,\mu\text{m}^2$.

Component	Value	Component	Value
C_{BE}	1.2 fF	C_{BC}	0.3 fF
R_B	166 Ω	g_m	6.2 mS
r_π	23.1 kΩ	r_O	992 kΩ
C_π	8 fF	R_C	219 Ω
C_μ	0.3 fF	C_{CE}	1.38 fF
r_μ	360.8 kΩ		
R_S	239.8 Ω	R_L	737.9 Ω

For simplicity it is assumed that the parasitic source and load inductances are equal, although they can differ in a real design.

The input and output impedance are derived and solved numerically due to the increased circuit complexity. Two contour plots of the real part of $Z_{T,in}$ and $Z_{T,out}$ are shown in Fig. 3.10(a) and Fig. 3.10(b) as function of frequency and load/source inductance. The frequency range is limited to 10 GHz because of the tuned source and load impedance. Above their resonance frequency, their become capacitive that prevent a negative resistance which was previously presented.

The first conclusion of both plots is that this small transistor will not oscillate under resistive matched condition because the necessary inductance values are far away from realistic assumptions for parasitic inductances. As already seen in the previous analysis, the possibility of an oscillation is larger at the output due to the lower inductance values at which a negative resistance occur.

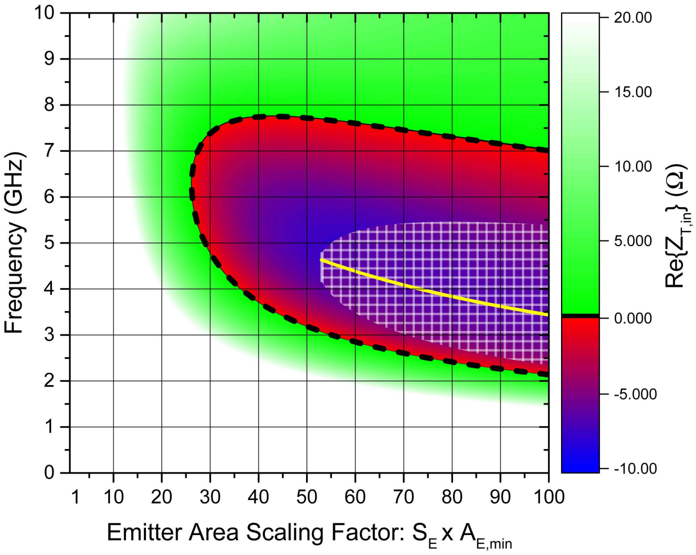


(a)

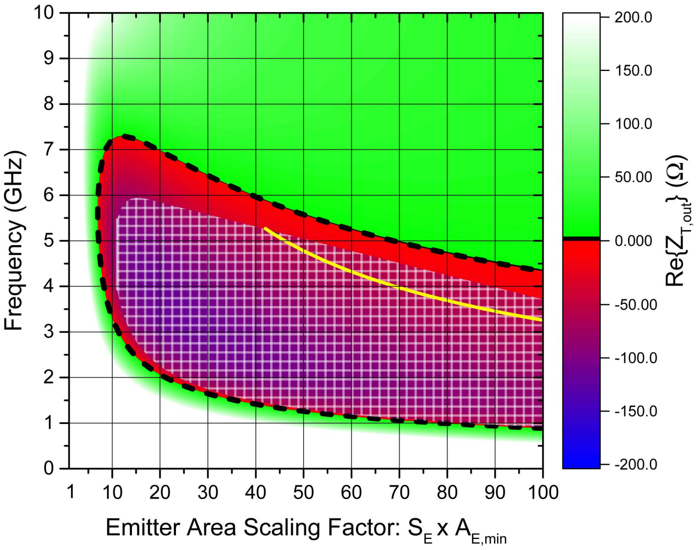
(b)

Figure 3.10: Contour plots of the resistive transistor input and output impedance, the red to blue area indicates a negative resistance, the hatched area inside shows the range of $\Re\{Z_{T,in}\} \leq -R_S$ and $\Re\{Z_{T,out}\} \leq -R_L$, the yellow line depicts the potential oscillation frequency due $\Im\{Z_{T,in}\} = \Im\{Z_S\}$ and $\Im\{Z_{T,out}\} = \Im\{Z_L\}$, (a) – Input resistance $\Re\{Z_{T,in}\}$, (b) – Output resistance $\Re\{Z_{T,out}\}$

A model scaling enables the analysis of the oscillation tendency in dependence of the transistor size at equal current density. For this, each resistive element in Fig. 3.9 is divided by the scaling factor and every capacitor and the current source are multiplied by the factor. It is assumed that the load and source inductance is fixed at a value of 1 nH because it is already known that an increase of the inductance value results in lower potential oscillation frequencies at a given transistor size, as seen by the yellow line in Fig. 3.10(a) and Fig. 3.10(b). The contour plots of $\Re\{Z_{T,in}\}$ and $\Re\{Z_{T,out}\}$ are depicted in Fig. 3.11(a) and Fig. 3.11(b) as function of the emitter scaling factor S_E.



(a)



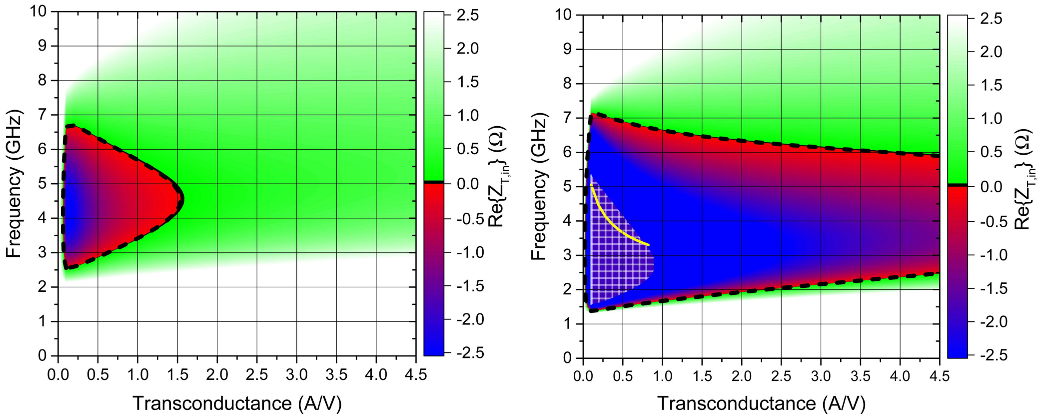
(b)

Figure 3.11: Contour plots of the resistive transistor input and output impedance as function of the emitter area at constant current density, scaled by S_E, (a) – Input resistance $\Re\{Z_{T,in}\}$ at $L_L = 1\,\mathrm{nH}$, (b) – Output resistance $\Re\{Z_{T,out}\}$ $L_S = 1\,\mathrm{nH}$

It can be concluded that from Fig. 3.11(a) with Fig. 3.11(b), although the transistor exhibits a negative input or output resistance at small emitter areas, a minimum emitter area is necessary for the transistor to be able to oscillate at a fixed inductance value. Similar to the previous results, the oscillation potential at the output is larger compared to the input. By comparing Fig. 3.11(a) with Fig. 3.10(a) and Fig. 3.11(b) with Fig. 3.10(b) it can be seen that the oscillation tendency is equal, only the absolute values for $\Re\{Z_{T,in}\}$ and $\Re\{Z_{T,out}\}$ differs. Consequently, the larger the transistor the smaller the inductance which causes an instability. In particular, power amplifiers with their large output stage are therefore prone to become unstable.

The last case to consider is the operating point of the transistor defined by the quiescent collector current. For this, the transistor size and load/source inductance are left constant and the oscillation tendency in dependence of the quiescent collector current and frequency is determined.

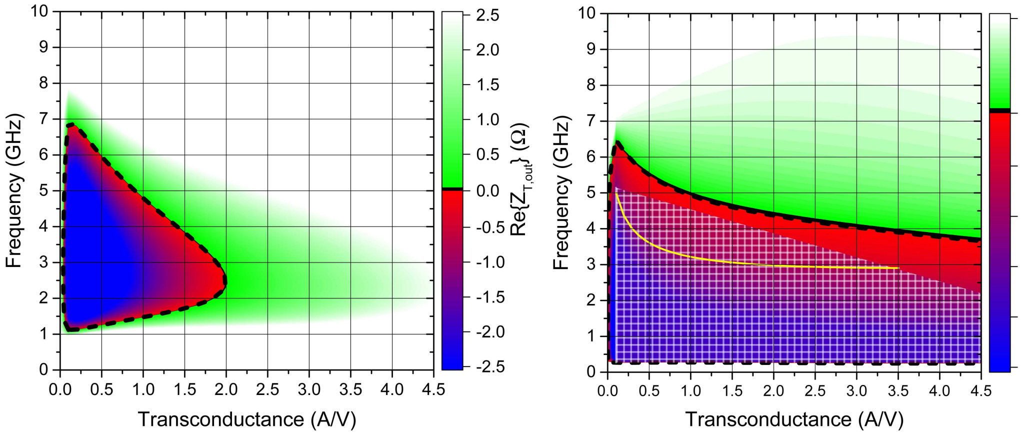
As the transconductance is increased by means of higher collector current density, the resistive intrinsic transistor components in Fig. 3.9 becomes smaller, except r_μ. In contrast, the capacitance C_π will increase due to a higher diffusion capacitance. The base collector capacitance remains unaffected because the model assumes that the base collector capacitance is only given by the depletion base collector capacitance. The extrinsic wiring capacitances will also not change. The numerical result for the resistive input impedance is shown in Fig. 3.12. A negative resistance is observable for low transconductance values with a load inductance of 0.4 nH. However the oscillation criteria are not satisfied seen by the missing hatched area in Fig. 3.12(a). Increasing the load inductance results in a potential oscillation of the transistor, depicted in Fig. 3.12(b). Furthermore, a negative resistance is observable over the complete tuning range of the transconductance.



(a) (b)

Figure 3.12: Contour plots of the resistive transistor input impedance as function of the transconductance, scaling factor $S_E = 50$, (a) – $L_L = 0.4\,\text{nH}$, (b) – $L_L = 0.8\,\text{nH}$

The contour plot of the resistive output impedance is shown in Fig. 3.13. Similar to the input impedance, the the oscillation tendency depends on the transconductance and source inductance. A small source inductance at low collector current densities results in negative output resistances, although the transistor will not oscillate. As the output impedance is more sensitive to the value of the source inductance, a smaller value for L_S was chosen. At larger inductance value the resistive output impedance is negative for all transconductance values and an oscillation would be possible for a wide range of transconductance values.



(a) (b)

Figure 3.13: Contour plots of the resistive transistor output impedance as function of the transconductance, scaling factor $S_E = 50$, (a) – $L_S = 0.1\,\text{nH}$, (b) – $L_S = 0.8\,\text{nH}$

The result of this analysis are:

- The SiGe heterojunction transistor will become unstable if an inductive source or load impedance is present.
- Although a negative resistance at the transistor's input or output is present, it does not necessarily mean that the transistor will oscillate. It should be mentioned that the presented analysis assumed a resistive matched load and source impedance. Any mismatches will result in different load and source impedance, and consequently, cause potentially stability issues despite the transistor was before considered as stable by the analysis.
- The oscillation tendency depends on the transistor's size and operating point. Despite the fact that the tendency also depends on the inductance value itself, the degree of freedom in an amplifier design will be mostly the transistor size and operating point.

The presented analysis is done on the example of the IHP transistor. Although the Infineon transistor differs in its characteristic from the IHP transistor, the similar device structure will lead to comparable results of the analysis performed with the IHP transistor.

3.3 Passive Frequency-Selective Feedback

A passive frequency-selective feedback (PFSF) is introduced between the base and collector to stabilize the transistor in common emitter configuration and mitigate the loss in gain due to the intrinsic transistor feedback. The schematic of the feedback is shown in Fig. 3.14 and consists of inductance L_{FB}, a capacitance C_{FB} and a resistance R_{FB} which includes ohmic losses in the inductance.

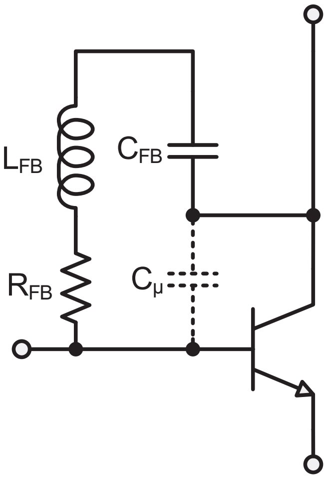


Figure 3.14: Scheme of the passive frequency-selective feedback

The concept of such feedback to either stabilize the transistor or neutralize the effect of the base collector capacitance is reported in the literature. Omitting the feedback inductance results in the well-known RC feedback which is used to stabilize the transistor. The impact of the feedback on the stability can be explained by the oscillation criteria from system theory which stated that the minimum loop gain must be unity for a sustained oscillation. A strong negative feedback, realized by R_{FB} and C_{FB}, will significantly lower the gain, and hence, impede a potential oscillation, as presented for example in [Qiong 11] and [Yu 12]. The counterpart, a RL feedback in conjunction with the base collector capacitance, is implemented to form a resonant tank which enables to cancel the intrinsic feedback path. Although most designs add a capacitor to the extrinsic feedback, the function of this capacitor is only to decouple the base and collector DC current. An example of the usage of this RL feedback is presented in [Gonzalez 96].

The idea is now to realize both separate feedback functions, to stabilize and neutralize, by one feedback simultaneously. That means the feedback must provide a sufficient negative feedback in one frequency range, the region of instability, and resonant out the base collector capacitance or rather mitigate the influence of C_μ in the working frequency range.

The feedback topology presented in Fig. 3.14 in conjunction with C_μ is suitable for this task because the formed resonant tank exhibits two resonances, a series and a parallel resonance. It is known that at series resonance the overall feedback impedance reaches it minimum value, whereas at parallel resonance the impedance is maximum, as depicted by the impedance magnitude plot in Fig. 3.15 with a series resonance frequency below the parallel resonance frequency.

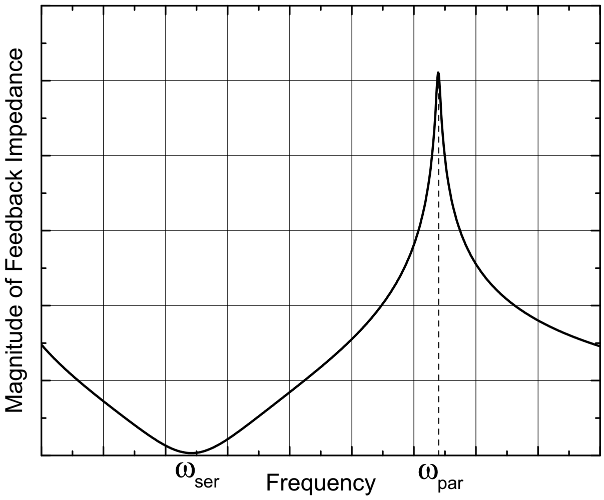


Figure 3.15: Magnitude of feedback impedance as function of frequency

Consequently, the feedback's series resonance is used to stabilize the transistor and the parallel resonance neutralize the transistor. The associated resonance frequencies ω_{ser} and ω_{par}, at series and parallel resonance respectively, will depend on the component values and are given as follow; Assuming ideal components and that the value of the feedback resistor is zero the resonance frequencies are straightforward derived to:

$$\omega_{ser} = \frac{1}{\sqrt{L_{FB} C_{FB}}} \tag{3.36}$$

$$\omega_{par} = \frac{1}{\sqrt{L_{FB} \dfrac{C_{FB} C_\mu}{C_{FB} + C_\mu}}} \tag{3.37}$$

The series resonance frequency is only determined by the extrinsic feedback inductance and capacitance, whereas the parallel resonance frequency is defined by the inductance and the series connection of the capacitors. The overall feedback at series resonance would be zero and at parallel resonance infinity.

By introducing the resistor the frequency response of the resonant tank is broadened, as depicted in Fig. 3.16. An increasing value of R_{FB} results in a larger bandwidth at the expense of a decreasing feedback impedance magnitude at parallel resonance and an increasing impedance at series resonance. Although a larger value of R_{FB} degrades the influence of the feedback, the broadened frequency response allows a desensitization of the feedback on process variations.

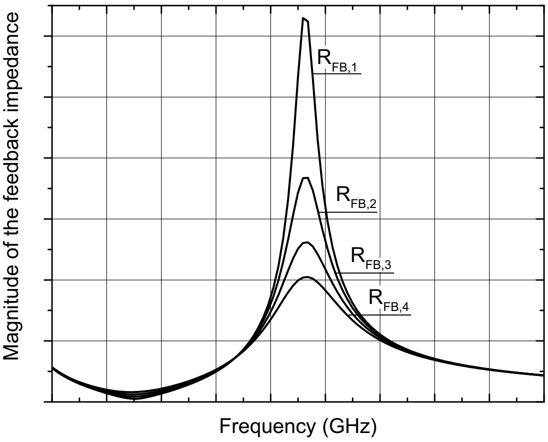


Figure 3.16: Frequency response of the resonant tank as function of R_{FB}, $R_{FB,1} < R_{FB,4}$

As long as the quality factor $Q = \omega L_{FB}/R_{FB}$ is much larger than unity the resulting impedances at series and parallel resonance can be approximated to:

$$Z_{ser} \approx R_{FB} \tag{3.38}$$

$$Z_{par} \approx \frac{L_{FB}}{R_{FB}C_\mu}\frac{C_{FB}}{C_{FB}+C_\mu} \tag{3.39}$$

Therefore, the purely resistive impedance at resonance frequency is almost equal to R_{FB}, and the parallel resonance impedance is defined by the quality factor of the inductance and resistor in conjunction with C_μ and the capacitive voltage divider originated through C_{FB} and C_μ.

If R_{FB} is further increased, and consequently, the quality factor decreases, a more accurate solution is provided by the following derivation of ω_{ser} and ω_{par}; The overall feedback impedance is given by:

$$Z_{FB} = \frac{1}{Z_E^{-1}+Z_I^{-1}} = \frac{1}{\left(R_{FB}+j\left(\omega L_{FB}-\frac{1}{\omega C_{FB}}\right)\right)^{-1}+\left(-j\frac{1}{\omega C_\mu}\right)^{-1}} \tag{3.40}$$

At resonance, the reactance become zero and in the case of the feedback topology the equation to be solved is:

$$0 = \Im\left\{\frac{1}{Z_E}\right\} + \Im\left\{\frac{1}{Z_I}\right\} = -\frac{\omega L_{FB} - \dfrac{1}{\omega C_{FB}}}{R_{FB}^2 + \left(\omega L_{FB} - \dfrac{1}{\omega C_{FB}}\right)^2} + \omega C_\mu \tag{3.41}$$

Reordering (3.41) results to:

$$\omega^5 + \frac{\omega^3}{L_{FB}}\left(\frac{R_{FB}}{L_{FB}} - \frac{2}{C_{FB}} - \frac{1}{C_\mu}\right) + \frac{\omega}{L_{FB}^2}\left(\frac{1}{C_{FB}C_\mu} + \frac{1}{C_{FB}^2}\right) = 0 \tag{3.42}$$

Although (3.42) is an equation of the fifth degree, its type allows to be solved for ω by factorization and subsequent substitution of ω. Altough the equation provides five solutions, only two of them are used because the other three solution are either zero or have a no-physical meaning. The remaining two solutions of ω are the series and parallel resonance frequency and are given with the assumption that the series resonance frequency is below the parallel resonance by:

$$\omega_{ser} = \frac{1}{\sqrt{2}}\frac{1}{L_{FB}}\sqrt{L_{FB}\left(\frac{1}{C_\mu} + \frac{2}{C_{FB}}\right) - R_{FB}^2 - \Delta_{FB}} \tag{3.43}$$

$$\omega_{par} = \frac{1}{\sqrt{2}}\frac{1}{L_{FB}}\sqrt{L_{FB}\left(\frac{1}{C_\mu} + \frac{2}{C_{FB}}\right) - R_{FB}^2 + \Delta_{FB}} \tag{3.44}$$

$$\Delta_{FB} = \sqrt{R^4 + \frac{L_{FB}^2}{C_\mu^2} - 2L_{FB}R_{FB}^2\left(\frac{1}{C_\mu} + \frac{2}{C_{FB}}\right)}$$

If the parallel resonance frequency will be below the series resonance frequency, the expressions for ω_{ser} and ω_{par} have to be exchanged. Substituting ω in (3.40) now with ω_{ser} and ω_{par} from (3.43) and (3.44), respectively, results in exact expressions for the purely resistive feedback impedance at series and parallel resonance:

$$Z_{FB,ser} = \frac{2R_{FB}L_{FB}}{C_\mu\left(R^2 + \Delta_{FB}\right) + L_{FB}} \tag{3.45}$$

$$Z_{FB,par} = \frac{2R_{FB}L_{FB}}{C_\mu\left(R^2 - \Delta_{FB}\right) + L_{FB}} \tag{3.46}$$

It has to be stated that this derivation is only valid for a quality factor larger or equal unity.

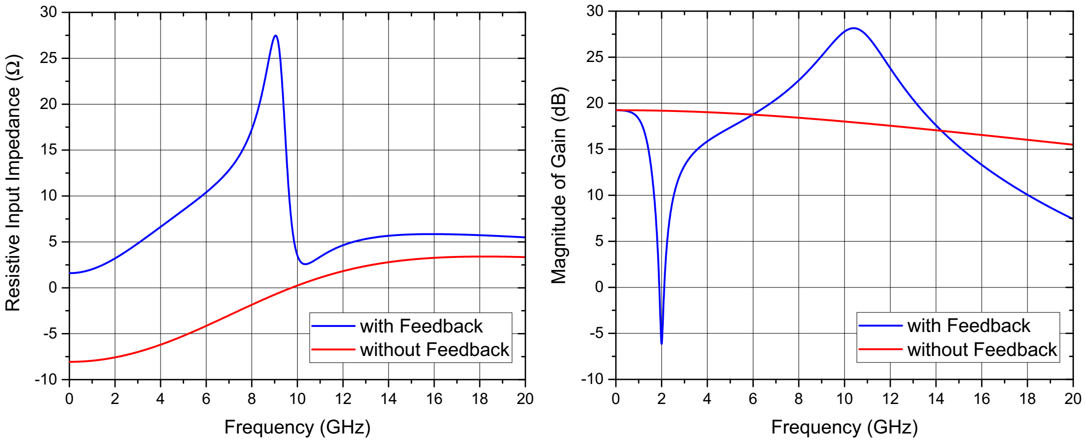
The implementation of the extrinsic feedback is as follow; As soon as the transistor is implemented in the actual circuit, the most likely oscillation frequency can be determined by investigating the transistor's input and output impedance as function of frequency, as done in the previous section. Subsequently the operating frequency is known and the base collector capacitance in conjunction with the base collector wiring capacitance can be determined by simulation, the feedback inductance and capacitance can be derived for example by solving (3.36) and (3.37). The corresponding values L_{FB} and C_{FB} results to:

$$L_{FB} = \frac{1}{C_\mu \left(\omega_{par}^2 - \omega_{ser}^2\right)} \tag{3.47}$$

$$C_{FB} = \frac{C_\mu \left(\omega_{par}^2 - \omega_{ser}^2\right)}{\omega_{ser}} \tag{3.48}$$

The feedback resistor can subsequently be included into the feedback and tuned to achieve a minor sensitivity without deteriorating the feedback influence on the transistor's stability.

Using the simplified transistor model without resistive components, the influence of the feedback on the transistor input impedance is shown in Fig. 3.17(a). The input impedance without feedback is negative at lower gigahertz frequencies but results into positive values with applied extrinsic feedback. The influence on the gain of the transistor is shown in Fig. 3.17(b). The series resonance is clearly observed as notch in the gain at lower frequencies, whereas at the operating frequency of 10 GHz the gain exhibits a peak due to the parallel feedback resonance.



(a) (b)

Figure 3.17: Transistor characteristic with and without feedback, (a) – Transistor resistive input impedance with and without extrinsic feedback, (b) – Transistor gain with and without extrinsic feedback

Chapter 4

X-Band Power Amplifiers Utilizing the Extrinsic Feedback

4.1 Packaged High Efficient Power Amplifiers

Two power amplifiers that utilize two different output matching networks are presented in this section. The first PA ("Thesis PA 1") uses an on-chip transformer as output matching network and the output matching of the second power amplifier ("Thesis PA 2") is realized with an on-chip LC-balun [Gerlich 13]. Furthermore, the chips were intended to be mounted on a $7 \times 7\,\mu\text{m}^2$ ceramic VQFN (Very Thin Quad Flat No Leads) package. As specified by the application requirements the maximum output power in saturation should reach 23 dBm at high efficiency levels. The intended center frequency of both PAs was predefined to 12 GHz.

4.1.1 Design Overview

The design concept of both power amplifiers is equal, except the output matching networks. The schematic is shown in Fig. 4.1. The amplifiers are implemented as two-stage push–pull amplifiers. The use of two stages gives the advantage of driving the output stage with sufficient signal strengths and relax the requirements on the matching networks for the output stage, as the first stage is used as intermediate matching circuit. As previously mentioned, the push-pull topology allows further to reduce the impedance matching ratio by a factor of four compared to single ended design with equal output power. The introduced virtual ground of this topology mitigate the influence of the common node impedance. Both amplifiers are fully on-chip biased by low-ohmic reference networks.

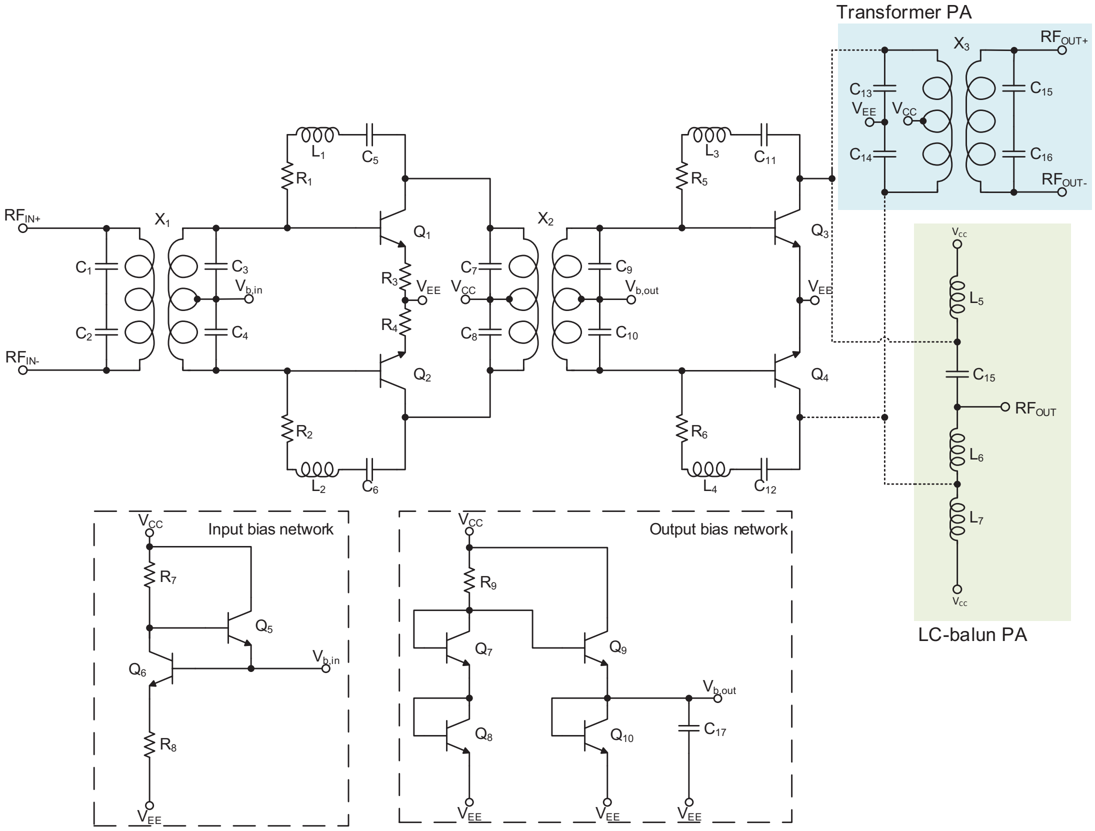


Figure 4.1: Schematic of the packed power amplifiers, the first power amplifier utilizes a transformer, the second PA uses a LC-balun for the output impedance matching

The input transformer X_1 with a turn ratio of 3 : 2 is shown in Fig. 4.2. The value of the primary inductance is 700 pH and the secondary one is 393 pH. The coupling coefficient k at 12 GHz is 0.75. Tuning capacitors (C_1–C_4) enable resonance operation of the transformer at 12 GHz, which are also depicted in Fig. 4.2. The overall area of the transformer is $94 \times 155\,\mu\text{m}^2$.

The input stage, consisting of Q_1 and Q_2, has a overall emitter area of $A_E = 66\,\mu\text{m}^2$. Emitter degeneration resistors (R_3, R_4) are used to improve the linearity of the input stage at the expense of gain, as the emitter resistor provide a negative feedback. The required base collector feedback was realized by a 1.27 nH inductor L_1 and a capacitor C_5 with a value of 750 fF. The resistor value of R_1 was chosen to be $30\,\Omega$. The feedback on the other branch of the input stage is provided by R_2, L_2 and C_6. The DC quiescent current of the input stage is set by Q_5 and Q_6 at a collector current density of $J_C = 1.7\,\text{mA}/\mu\text{m}^2$. Due to the virtual ground of the push–pull topology, the center tap of the input transformer is used as supply connection for the base quiescent current from the emitter follower Q_6. The low output impedance of the emitter follow enables the usage of collector emitter voltages higher than given by BV_{CEO}.

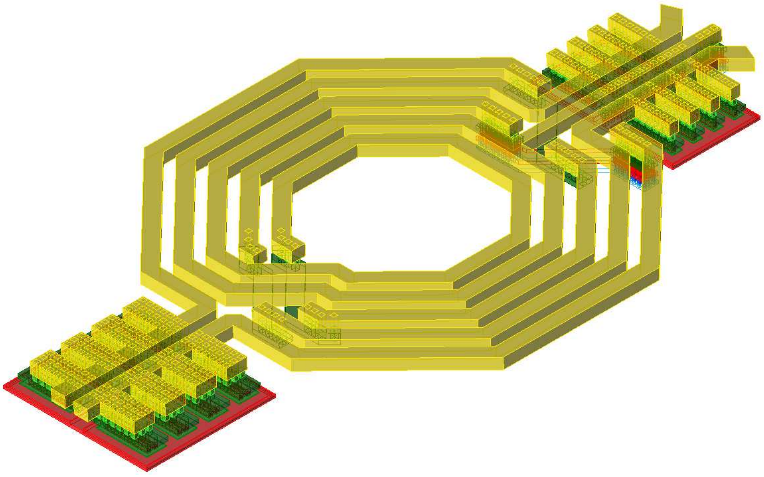


Figure 4.2: Input transformer with turn ratio of 3 : 2

As seen in the discussion about the breakdown voltages of SiGe HBTs, the lower limit of the collector emitter voltage is given by BV_{CEO} that implies an open base or a high-ohmic base contact. As further was stated, the upmost level of the collector emitter voltage is given by BV_{CES}, where the base is shorten to reference potential. That means that the impedance of the bias network at the base determines the maximum possible collector emitter voltage. This circumstance can be straightforwardly simulated by the transistor output characteristic with a voltage source at the base and a sweepable base resistor. As the breakdown behavior of the transistor is not included in the model, the output characteristic as function of the base resistor of a different transistor is plotted in Fig. 4.3.

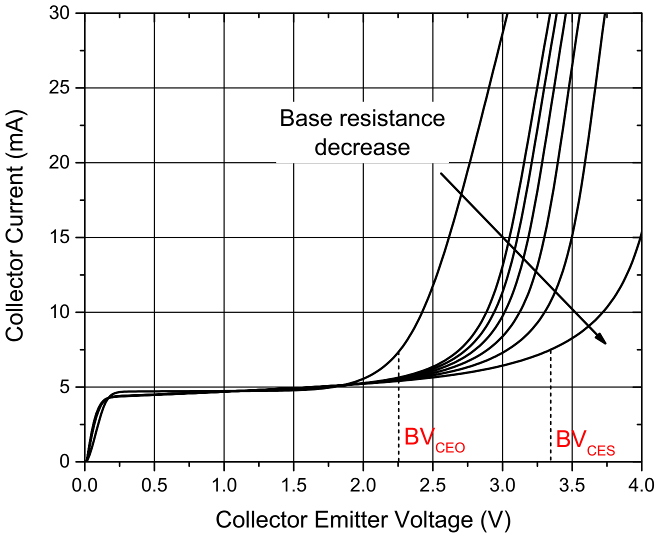


Figure 4.3: Transistor output characteristic as function of the base resistor

For this, the base resistor was swept from 0 Ω to 100 kΩ. As seen by the graph, the lowering of the base resistor results in a delayed onset of the breakdown, and therefore, to a shift of the collector emitter breakdown voltage to higher levels, limited by the two extrema of BV_{CEO} and BV_{CES}.

The impedance transformation between the input stage and output stage also realized by a double-tuned interstage transformer X_2, depicted in Fig. 4.4. The center taps of 2 : 1 transformer are used for the supply voltage of the input stage and the base bias current of the output stage. As the secondary winding has only one turn, the center tap is on the opposite side of the winding. It was therefore necessary to use lowest metal layers to minimize the influence of the magnetic field by the transformer on the bias feeding trace. The green traces in Fig. 4.4 are the connection traces for the supply voltage. The primary inductance of the transformer is 625 pH while the secondary winding inductance is 189 pH. As only one winding is used for the secondary coil, the magnetically coupling factor is only 0.69. Primary and secondary winding tuning capacitors (C_7–C_{10}) facilitate resonant transformer operation. The resonance of the interstage transformer is in particular important. Due to the low input impedance of the output stage and the quality factor of the transformer determined by the capacitors and ohmic losses, it is demonstrated that the current transfer ratio is increased compared to a untuned transformer [Bakalski 04]. As both transformer windings are in resonance, the quality factor can be determined by the capacitors and the ohmic losses. The total area of X_2 is $138 \times 200\,\mu m^2$.

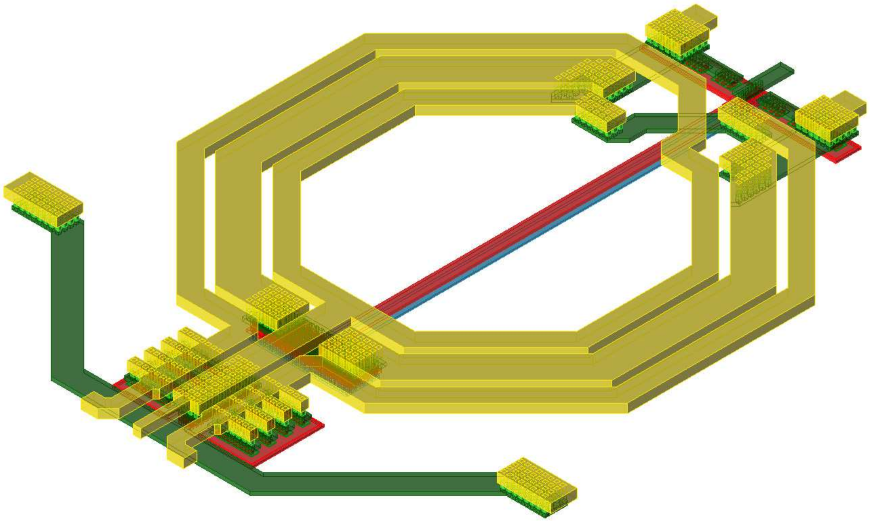


Figure 4.4: Double-tuned interstage transformer with turn ratio of 2 : 1

The output stage of both amplifiers were realized by transistors Q_3 and Q_4 with a total emitter of $A_E = 99\,\mu m^2$ for each transistor. The resistor (R_5, R_6) of the feedback is $5\,\Omega$, and the values for the feedback capacitor (C_{11}, C_{12}) and inductor (L_3, L_4) are 3 pF and 0.64 nH, respectively. Similar to the input stage, a low-ohmic reference network (Q_7–Q_{10}) was used that sets the collector quiescent current density to $J_C = 0.18\,\mathrm{mA/\mu m^2}$.

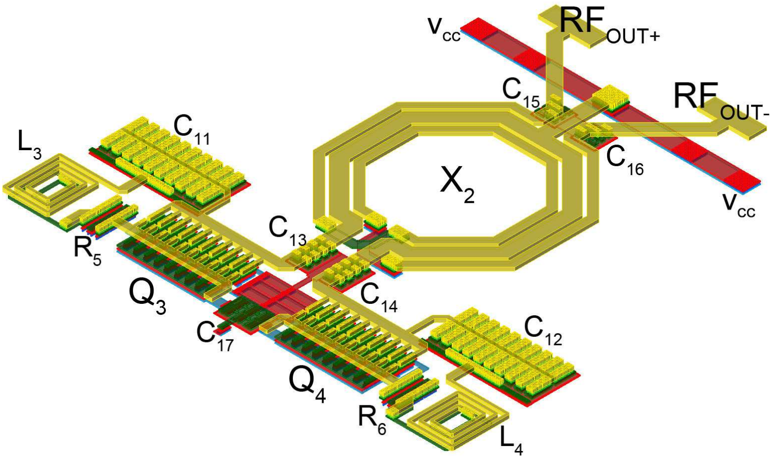


Figure 4.5: Output stage of the packed power amplifier with on-chip transformer as output matching network

The Fig. 4.5 shows the complete output stage, including the feedback and the transformer as output matching networks that are considered in the next section. The transformer X_3 has a total area of $168 \times 234\,\mathrm{\mu m^2}$ with a turn ratio of $1:2$. The primary inductance is 273 pH and the tuning capacitors C_{13} and C_{14} have a capacitance of 300 fF. The coupling coefficient is 0.68 and the value of the secondary inductance is 915 pH with 200 fF tuning capacitors C_{15} and C_{16}.

As the LC-balun is described in the next section, only the values are presented; The inductance L_5 in the green shaded area of Fig. 4.1 is 0.125 nH, L_6 is 0.339 nH and the inductor L_7 is 0.255 nH. The capacitance of the LC-balun, C_{15}, is 540 fF. The layout is shown in Fig. 4.6. The additional inductance between C_1, L_6 and RF_{OUT} was used to match the parasitic package capacitance.

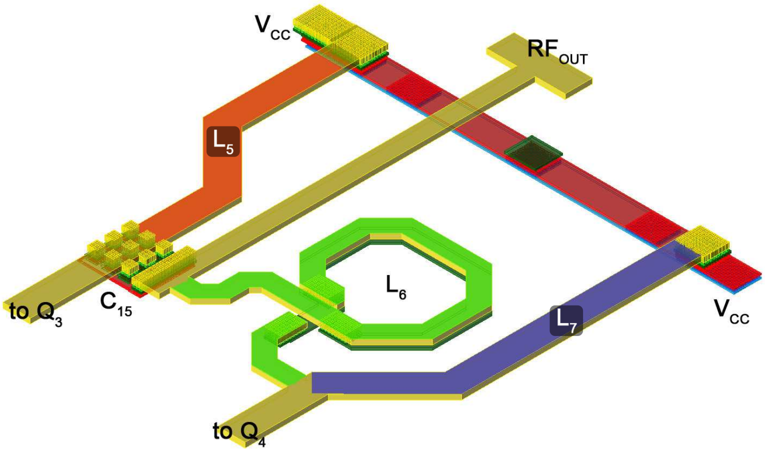


Figure 4.6: Output stage of the packed power amplifier with an LC-balun at the output, the individual inductors are marked in red, green and blue

As the chips were intended to be mounted in a package, the package parasitics had to be taken into account. A simple lumped element model of two parallel package connections is shown in Fig. 4.7. The pad capacitance is modeled by C_{SUB} and takes the finite substrate conductivity by means of R_{SUB} into account. The non-ideal bond wire and lead inductance is given by L_{Bond}, R_{Bond} and L_{Lead}, R_{Lead}. A mutual coupling between the bond wires and leads is denoted by M_{Bond} and M_{Lead}, respectively. The capacitive coupling is represented by C_{coup}, and capacitive coupling of the lead to the reference potential is given by C_{Lead}.

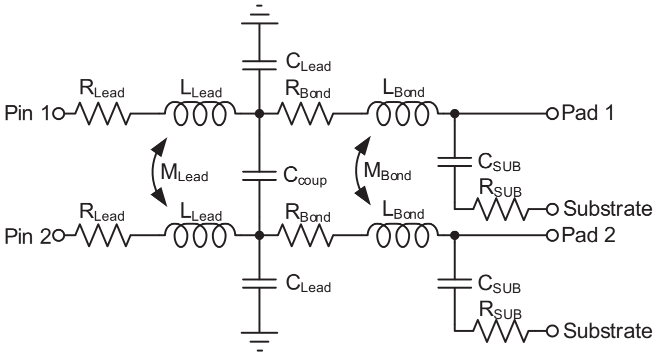


Figure 4.7: Lumped element model of a package

The chip size, position in the package and connection scheme was application specific predefined and shown in Fig. 4.8.

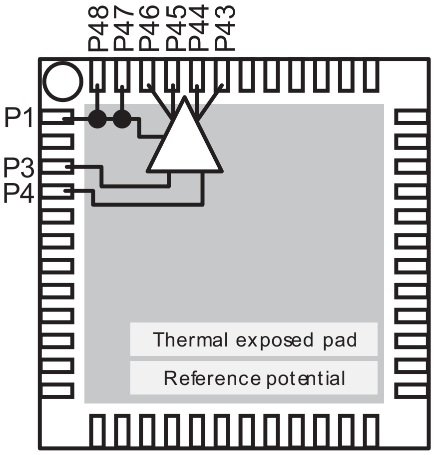


Figure 4.8: Simplified package floorplan for the power amplifiers

The pins P1, P47 and P48 are reserved for the supply voltage, the differential input is on pin P3 and P4 and the differential output is on pin P43 to P46. In the case of the single-ended output of the LC-balun based PA, pins P45 and P46 are connected in parallel. Instead of the use of the model, the results of package electromagnetic simulations were provided by the foundry and are included into the design. The characteristic impedance of the package leads were close to 50 Ω. Only additional capacitance of the package pads had to be taken into account for the matching networks.

The layouts of both power amplifiers are shown in Fig. 4.9 and Fig. 4.10. The chip size is 1066 µm × 1628 µm. The free chip area was filled with decoupling capacitors and unspecified bond pads were used as ground pads. Microstrip transmission lines with a characteristic impedance of 50 Ω were used to connected the input bond pads with the input transformer.

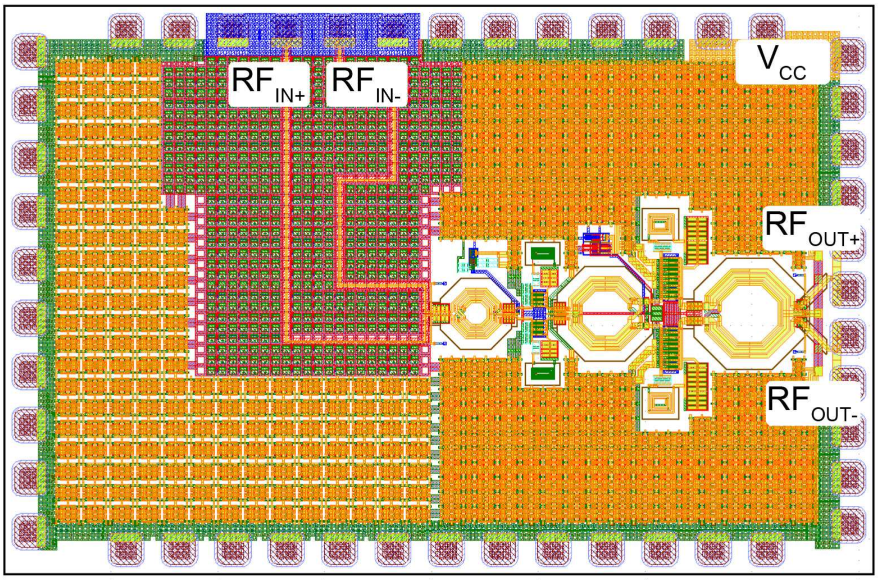


Figure 4.9: Layout of transformer based power amplifier

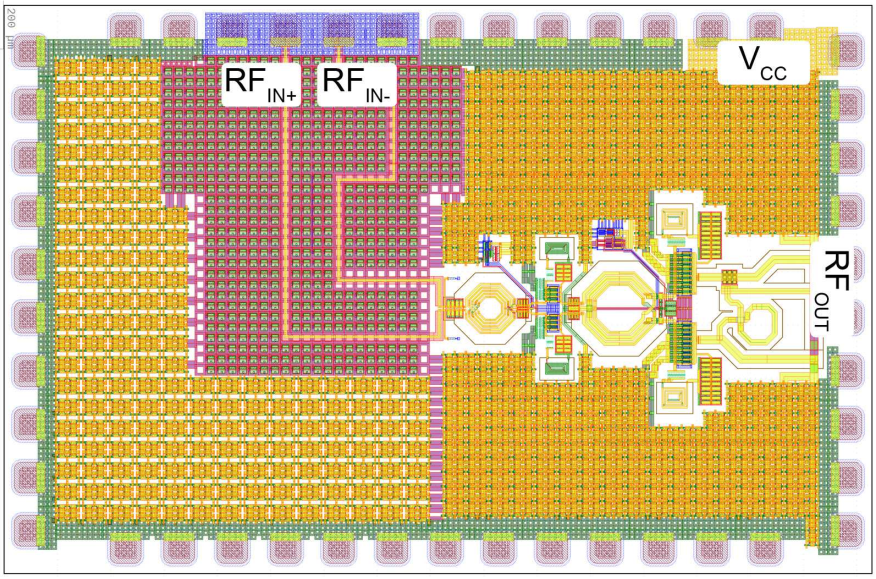


Figure 4.10: Layout of LC-balun based power amplifier

4.1.2 Output Matching Network Designs

The general matching procedure for all power amplifiers was based on load- and source-pull simulation techniques. This technique allows a graphical representation of metrics, as power-added efficiency, output power and gain, as function of the load and source impedance in dependence of quiescent current, input power and device size. The basic concept of source- and load pull simulation is depicted in Fig. 4.11.

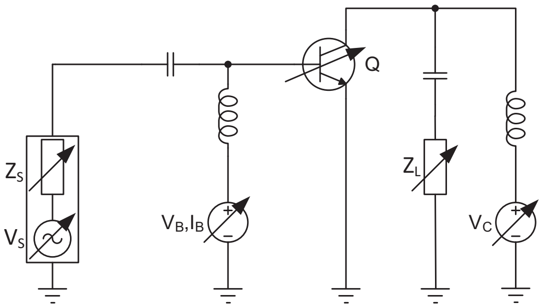
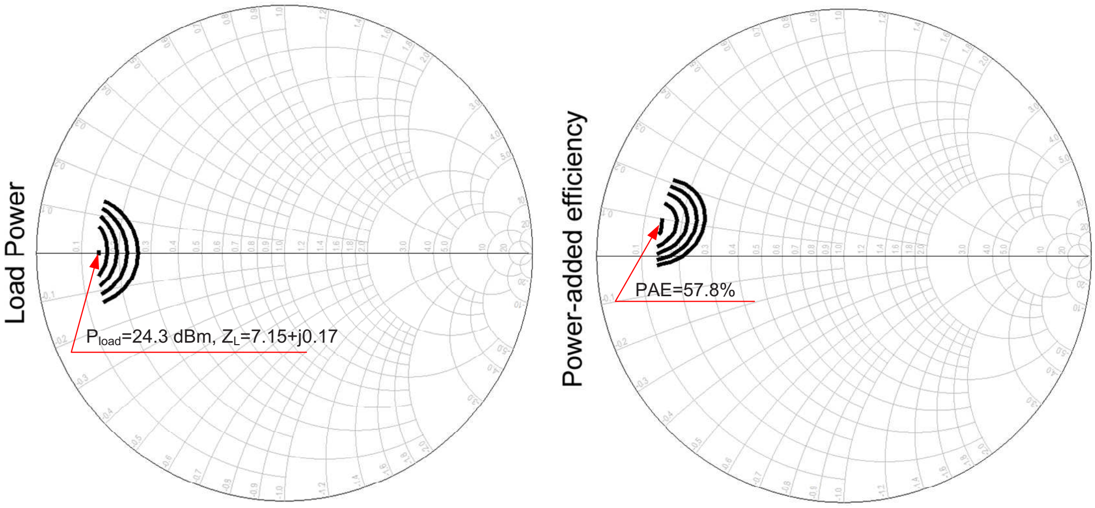


Figure 4.11: Basic setup for source- and load-pull simulation

Quite common is to plot the results of the source- and load pull simulation into the Smith chart. An example is given in Fig. 4.12, the contour plot shows the output power and power-added efficiency of the output stage transistor as function of the load impedance at 12 GHz.



(a) (b)

Figure 4.12: Load pull contour of the Infineon transistor, $A_E = 99\,\mu m^2$, $J_C = 0.18\,mA/\mu m^2$, $V_{CE} = 1.7\,V$ (a) – Load output power contour, (b) – Power-added efficiency contour

The maximum output power is expected to be 24.3 dBm with a load impedance of $Z_L = (7.15 + j0.17)$. Larger load impedances will results in smaller output powers. Similar for the power-added efficiency, the highest efficiency is obtained at a real load impedance of 7.1 Ω. The load reactance value may vary between 3 Ω and 4.8 Ω without changing the efficiency of the amplifier. Furthermore, the load pull simulation of the output stage indicates that the transistor size is suitable for the required output power of 23 dBm.

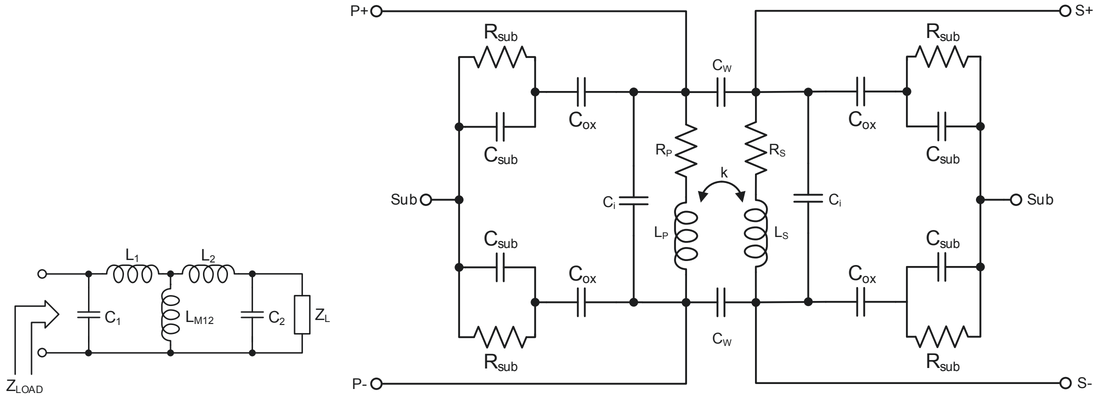
The source and load impedance of transistors will be in most cases smaller than the system impedance. Especially, the output impedance of power amplifiers with their large output stages need to be well matched to the system impedance to deliver efficiently the output power they are designed for. Two common matching networks that are able to provide such impedance transformation requirements are presented in the following.

Transformer

On-chip transformer are widely used in radio frequency circuits because of three major advantages:

- Their inherent DC blocking capability allows to omit components for protecting against electrostatic discharges. These components are for example diodes that are placed between the supply rail, the input or output connection and the reference potential in a reversed direction. Diodes operating in reverse mode act as capacitance by their depletion capacitance, and with increasing frequency the capacitance will negatively influence the circuit performance.
- Transformer can be used as balun. Single-ended signals can be transformed into differential signal and vice versa. Low noise amplifiers or power amplifiers that receive from or transmit power to antenna have in mostly a single-ended input or output, respectively. However, a differential circuit topology is in most cases preferable, as its advantage are already presented.
- By changing the ratio between both inductances of a transformer, the transformer is suitable as impedance transformer. In combination with the foregoing advantages, the magnetically transformer can be used as versatile impedance matching circuit.

Examples of the layout of transformer are already presented in the previous section, only a simple sketch of a transformer with a turn ratio of 2 : 2 is shown in Fig. 4.13(a). The lumped equivalent circuit model can be rather complex and depends on the application of the transformer. A lumped element model for narrow-band application is depicted in Fig. 4.13(b) [El-Gharniti 04]. The model consists of following components:



(a) (b)

Figure 4.13: Narrow-band lumped element model for a transformer(a) – Sketch of a transformer, (b) – Lumped element model

- R_{sub}, C_{sub} and C_{ox} represents substrate and oxide coupling and losses.
- The capacitances C_w and C_i models the capacitive coupling between primary and secondary winding, and interwindings, respectively.
- The inductances of the primary and secondary winding are modeled as ideal inductances L_P and L_S that are not ideally magnetically coupled, denoted by the coupling coefficient k. The value range of k is from zero, for non coupled inductances, to unity, which is the value for ideally coupled inductances. Losses are considered by the resistances R_P and R_S.

The model components can be calculated from the physical layout of the transformer with use of simulation programs that utilize FastHenry algorithms [Kamon 94]. Another approach to characterize the transformer is by the use of electromagnetic simulations. Instead of lumped element model, the result of an electromagnetic simulation is a matrix set of s-parameters which describes the frequency dependent transformer characteristic. The most important metrics of the transformer can be derived by converting the s-parameters into z-parameters:

$$L_P = \frac{\Im\{Z_{11}\}}{\omega} \tag{4.1}$$

$$L_S = \frac{\Im\{Z_{22}\}}{\omega} \tag{4.2}$$

$$R_P = \Re\{Z_{11}\} \tag{4.3}$$

$$R_S = \Re\{Z_{22}\} \tag{4.4}$$

$$k = M_{SP}/\sqrt{L_P L_S} = \frac{\Im\{Z_{12}\}}{\Im\{Z_{11}\}\Im\{Z_{22}\}}, \text{ with } M_{SP} = \frac{\Im\{Z_{12}\}}{\omega} \tag{4.5}$$

The quality factor, as transformer performance metric, of both inductances lies between the quality factor of the inductance with the counterpart open and the quality factor with the counter winding shorten:

$$Q_{P,short} \leq Q_P \leq Q_{P,open} = \frac{\Im\{Y_{11}^{-1}\}}{\Re\{Y_{11}^{-1}\}} \leq Q_P \leq \frac{\Im\{Z_{11}\}}{\Re\{Z_{11}\}} \tag{4.6}$$

$$Q_{S,short} \leq Q_S \leq Q_{S,open} = \frac{\Im\{Y_{22}^{-1}\}}{\Re\{Y_{22}^{-1}\}} \leq Q_S \leq \frac{\Im\{Z_{22}\}}{\Re\{Z_{22}\}} \tag{4.7}$$

As seen in the previous given design description, the transformers are tuned by capacitances into resonance to mitigate power losses. The tuning of the secondary winding is simply realized by placing a capacitor in parallel to the winding, resulting in a resonance frequency of $\omega_r = 1/\sqrt{L_{SEC}C_{SEC}}$. The primary winding tuning is a more demanding because wiring capacitances of the output stage needs to be taken into account. The design procedure is explained on a simplified transformer model, illustrated in Fig. 4.14.

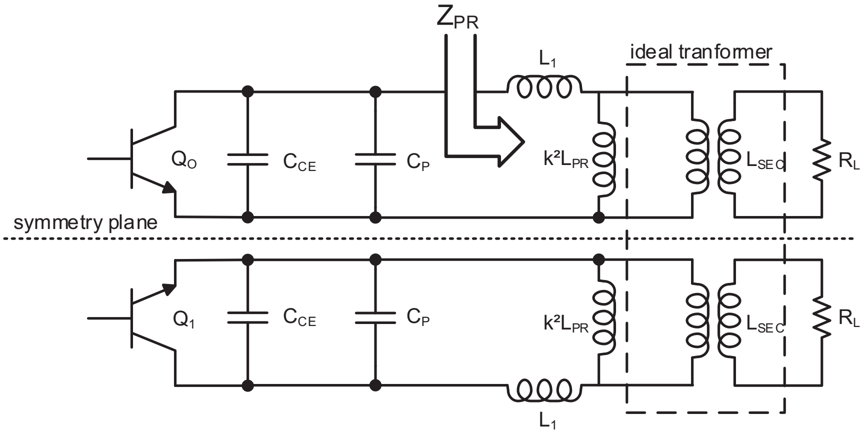


Figure 4.14: Schematic for tuning the output transformer

Considering one half of an output stage, cutted at the symmetry plane due to the virtual ground, and assuming further that the secondary winding is already in resonance ω_r, the inductance k^2L_{PR} in Fig. 4.14 can be omitted. The ideal transformer with a transformation ratio of

$$n = k\sqrt{\frac{L_{PR}}{L_{SEC}}} \tag{4.8}$$

will transform a purely resistive load impedance R_L to the primary side:

$$R_{L,PR} = n^2 R_L \tag{4.9}$$

Therefore, the transformer primary inductance results to

$$Z_{PR}|_{\omega r} = n^2 R_L + j\omega_r (1-k^2) L_{PR} \tag{4.10}$$

with a leakage inductance value of $(1-k^2)L_{PR}$ due to nonideal coupling. The inductance reactance of Z_{PR} can be canceled by a shunt capacitance C_P. However, as seen in the schematic of Fig. 4.14, the collector emitter wiring capacitance will be in parallel to C_P and needs to be taken into account. Therefore, the value for the capacitance C_P is given by:

$$C_P = -\frac{\Im\{Z_{PR}^{-1}\}}{\omega r} - C_{CE} = \frac{\omega_r (1-k^2) L_{PR}}{(n^2 R_L)^2 + (\omega_r (1-k^2) L_{PR})^2} - C_{CE} \tag{4.11}$$

LC-Balun

Another matching possibility is provided by the implementation of an LC-balun as output matching network. The LC-balun is also known as the Lattice-type balun. The general concept is shown in Fig. 4.15. The LC-balun consists of the inductances L_1, L_2 and of the capacitances C_1, C_2. A radio frequency choke coil (RFC) provides a DC current path for the transistor Q_1 and a DC blocking capacitor (DCB) isolates the load from DC current flowing into the load. The impedance R'_L is the characteristic balun impedance which should be twice the desired load impedance of the transistors.

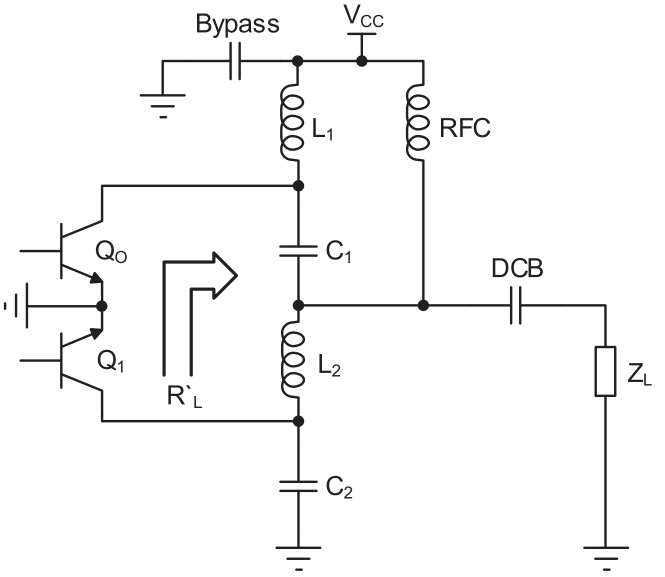


Figure 4.15: General schematic of the LC-balun as matching network for the output stage

Assuming a resistive load impedance Z_L, the values for the LC-balun components at the operation frequency w_{OP} are given as follows:

$$L_1 = L_2 = \frac{\sqrt{R'_L Z_L}}{\omega_{OP}} \tag{4.12}$$

$$C_1 = C_2 = \frac{1}{\omega_{OP}\sqrt{R'_L Z_L}} \tag{4.13}$$

Similar to the case of impedance matching with a transformer, the collector emitter wiring capacitance should be taken into account to load the transistors with a pure ohmic resistance by bringing the capacitances into resonance by shunt inductors L_A at ω_{OP}, shown in the schematic of Fig. 4.16. Obviously, the inductances L_A are in parallel to the balun components L_1 and C_2 and can be therefore substituted by equivalent impedances.

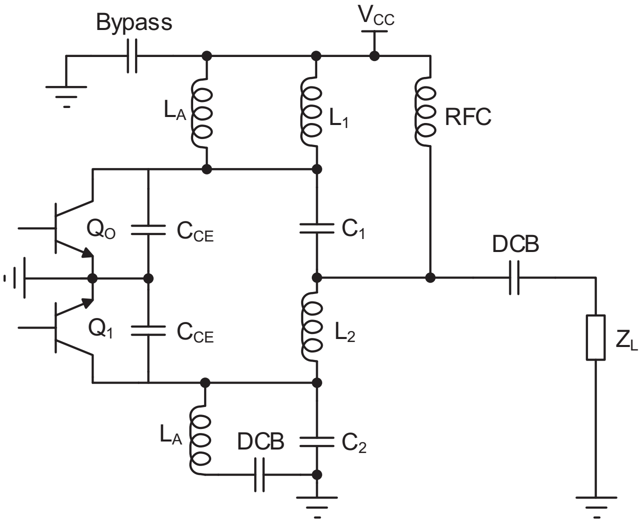


Figure 4.16: Schematic of the LC-balun with collector emitter wiring capacitances of the output stage

The substitution of L_A and L_1 is straightforwardly given by:

$$L_{S,1} = \frac{L_A L_1}{L_A + L_1} \tag{4.14}$$

The second substitution of L_A and C_2 results in equivalent susceptance B_S of:

$$B_S = -\frac{1}{\omega L_A} + \omega C_2 = \frac{-1 + \omega^2 L_A C_2}{\omega L_A} \tag{4.15}$$

Depending on the sign of B_S, L_A and C_2 can be replaced either by a capacitor or inductor:

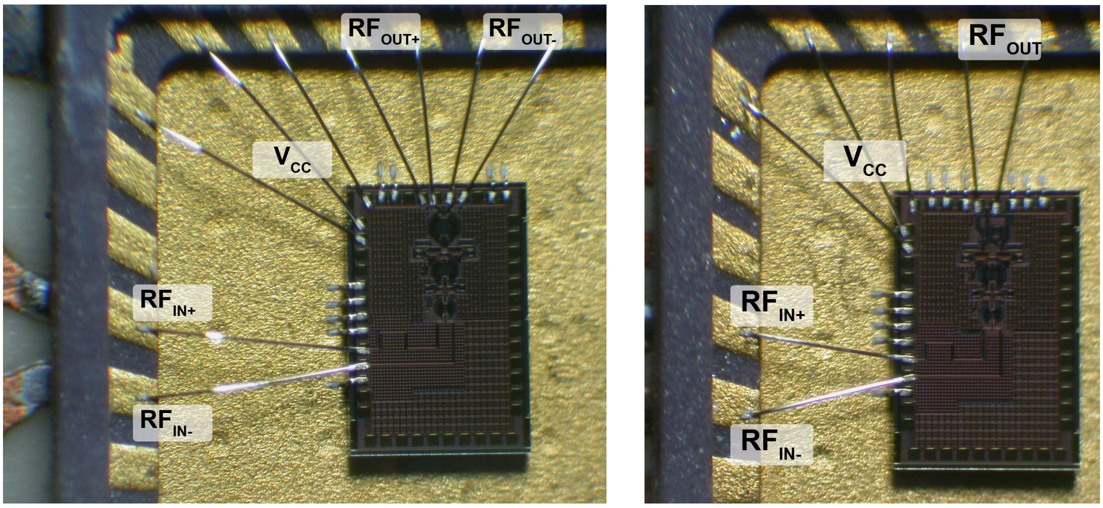
$$-B_S \Rightarrow L_{S,2} = -\frac{1}{\omega B_S} \tag{4.16}$$

$$+B_S \Rightarrow C_{S,2} = \frac{B_S}{\omega} \tag{4.17}$$

In the case of an inductor as substitution component, the RF choke could be omitted, and instead to ground the substituted inductor would be connected to supply voltage, which means that one inductor in the LC-balun design can be omitted.

4.1.3 Experimental Results

Measurement Setup The chips were glued onto the thermal exposed metal pad of the VQFN package, shown in Fig. 4.17 and Fig. 4.17(a). The distance difference of chip and package pads between both amplifiers is simply due to the placement of the chips by hand. Subsequently, the package was closed by a cover which was glued to the package for measurements.



(a) (b)

Figure 4.17: Chips glued onto a VQFN package (a) – Transformer based PA, (b) – LC-balun based PA

The measurement setup is depicted in Fig. 4.18. Both chip packages were mounted on 0.508 mm Rogers 4003 substrate ($\epsilon_r = 3.38$) and 50 Ω microstrip transmission lines were used at the input and output. The transformer based power amplifier is denoted as PA A and in the LC-balun as PA B in Fig. 4.18.

The supply voltage for measurements was 1.8 V in continuous mode and no additional power supplies were necessary, as the power amplifiers are fully on-chip

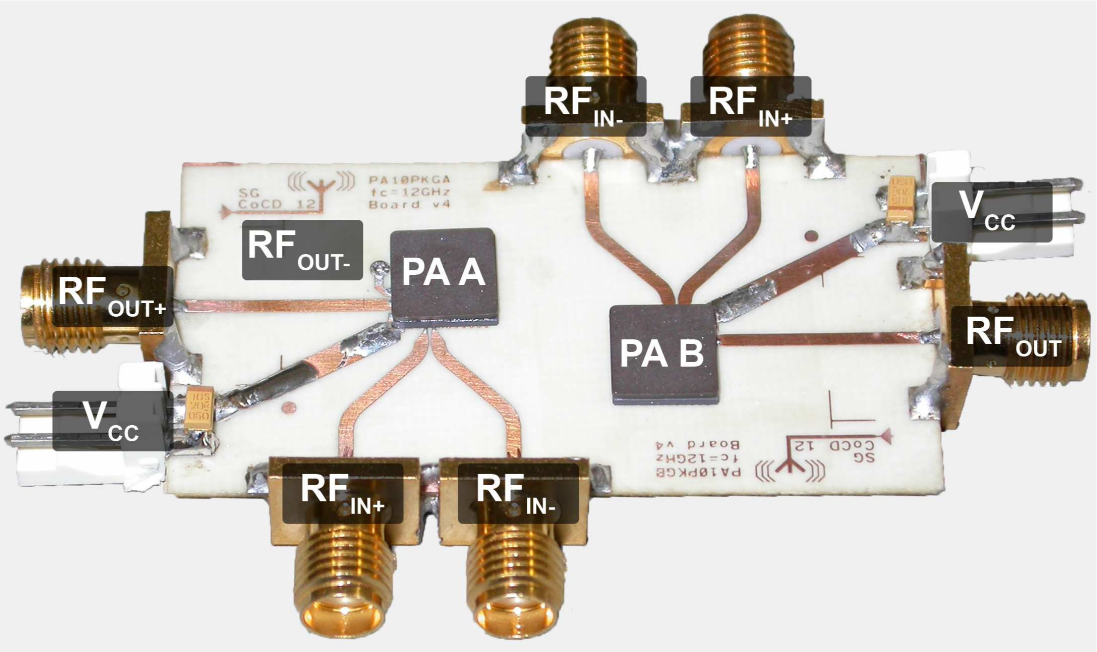


Figure 4.18: Measurement printed circuit board with PA A and PA B

biased.

Results of Power Amplifier A The measured large signal frequency characteristic of the power amplifier is shown in Fig. 4.19 which depicts the maximum output power in saturation and maximum power-added-efficiency as function of the frequency. The dotted lines represents the simulation results.

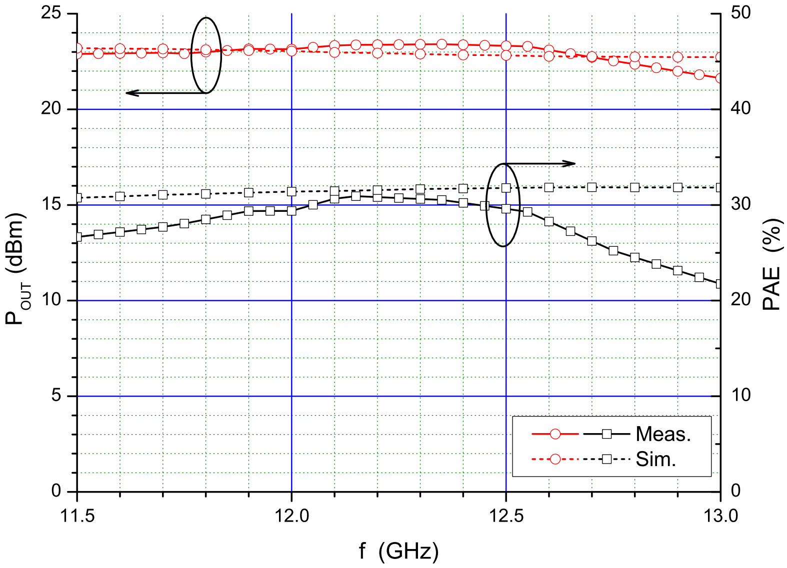


Figure 4.19: Large signal frequency characteristic of PA A

The mismatch in terms of the maximum output power in saturation between measurement and simulation is comparable small. Also the frequency dependence on this characteristic is similar to the results obtained by simulations. The frequency characteristic of the power-added efficiency is between 12 GHz and 12.5 GHz close to the simulation results. The difference for higher frequency results from a output impedance mismatch. As seen in Fig. 4.18, one terminal of the output transformer is connected to a grounded stub. The influence of this stub was taken into account by a simple lumped element model, which is obviously not accurate enough at higher frequencies.

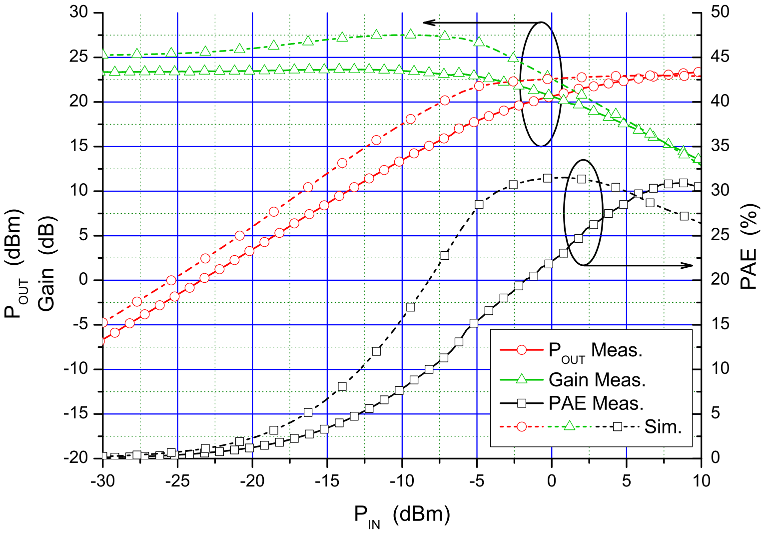


Figure 4.20: Power transfer characteristic at 12.15 GHz

The power transfer characteristics, shown in Fig. 4.20, were measured at an input frequency of 12.15 GHz, the frequency where the highest power-added efficiency of the PA is obtained. Although the measured characteristics look quite different from the simulation results, the only difference is the quiescent current of the PA. The collector quiescent current in the simulation is lower than in measurement, as seen on the gain expansion of the simulated gain. Therefore, the curves of the measurement are shifted to the right because the measured gain is lower. In contrast, the absolute values matches well.

Similar to the power transfer characteristic, the difference in the small gain frequency response of Fig. 4.21 results from different quiescent currents. As the bias of the amplifier is fixed and only depends on the supply voltage, a subsequent change in the bias setting is not possible.

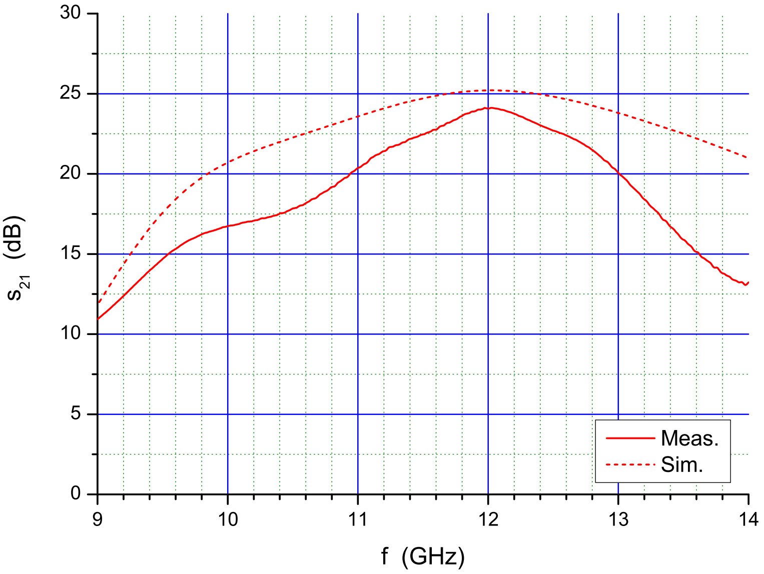


Figure 4.21: Small signal gain frequency response

Results of Power Amplifier B The power amplifiers large signal frequency characteristic is shown in Fig. 4.22. Similar to the previous PA, the maximum output power in saturation and maximum power-added-efficiency as function of the frequency. The dotted lines represents the simulation results which are in good agreement with the measurement results.

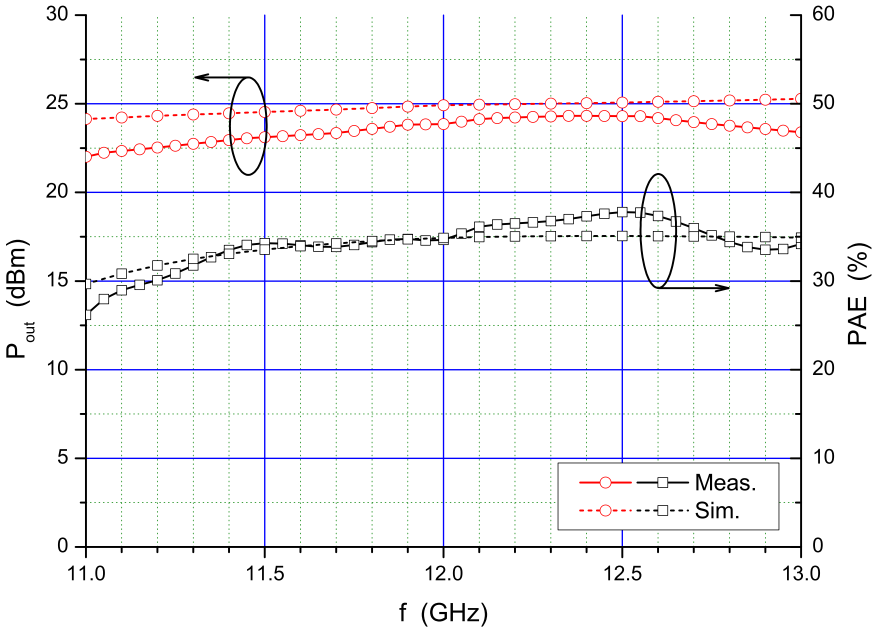


Figure 4.22: Large signal frequency characteristic of PA B

The mismatch in terms of the maximum output power in saturation between measurement and simulation is comparable small. Also the frequency dependence on this characteristic is similar to the results obtained by simulations. The frequency characteristics of the power-added efficiency are between 12 GHz and 12.5 GHz close to the simulation results. The difference for higher frequency results from an output impedance mismatch.

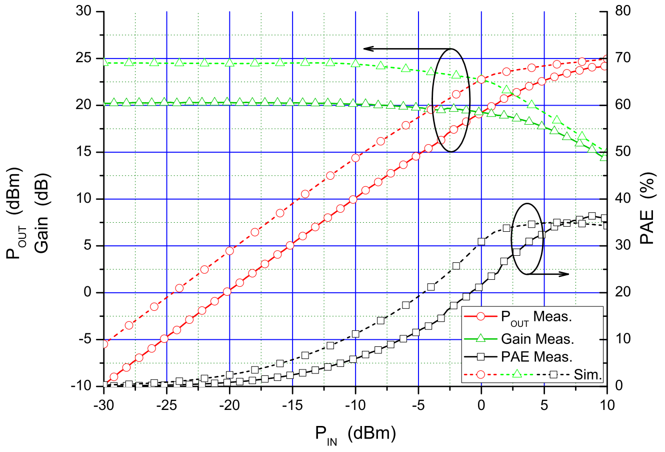


Figure 4.23: Power transfer characteristic at 12.55 GHz

The power transfer characteristic, shown in Fig. 4.23, was measured at an input frequency of 12.55 GHz, the frequency at highest power-added efficiency of the PA. Similar to PA A, the absolute values of output power and PAE matches well, only the gain is shifted to a lower due to different biasing. Therefore, the curves of output power and PAE are shifted to the left.

The frequency dependent small signal gain characteristic is in good agreement to the simulation result, as shown in Fig. 4.24. Only the absolute values are shifted due to a different biasing between simulation and measurement.

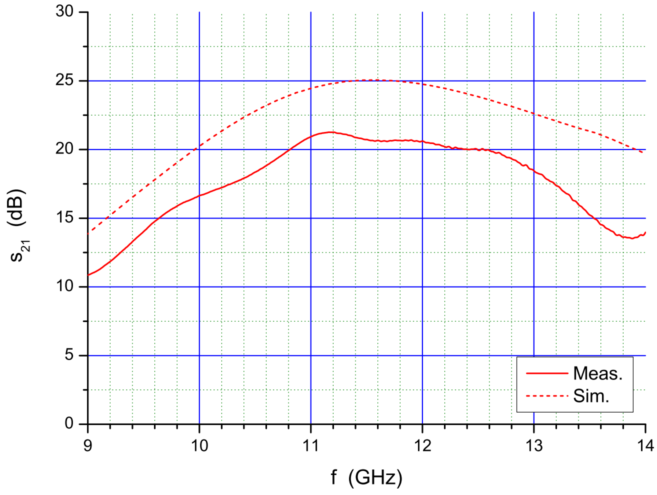


Figure 4.24: Small signal gain frequency response

4.2 A Series-Parallel Power Combined Power Amplifier

The output power capability of a PA can be either increased by an enlargement of the output stage or by combining single power amplifier circuits to one circuit. An enlargement of the output stage will be mostly limited by the matching networks because excessive transformation ratios lead to a significant power dissipation in the matching networks which degrades the overall efficiency [Reynaert 07]. The other opportunity is to combine the power amplifiers by power combiners. In the following, a power amplifier is presented, "Thesis PA 3", which utilizes series and parallel power combining to increase the maximum output power.

4.2.1 Power Amplifier Design

The single power amplifier circuit is based on the previously presented packaged PA with a transformer for output matching. The schematic is shown in Fig. 4.25 which depicts the schematic of two power amplifiers that are series connected by the input and output transformer. The main differences to the packaged PA are:

- As one design goal was to reach 30 dBm of maximum output power and high efficiency, the emitter resistances were omitted to improve the overall efficiency at the expense of linearity, although their influence is small. Nevertheless, even this small influence needs to be eliminated to reach high efficiency levels.

- As consequence of the later presented input transformer structure, the common node of the tuning capacitors on the secondary side of the input transformer are tied to V_{EE} instead to the bias supply.

- Due to the changed transformer structure at the input and output, the leakage inductance seen at the transistor's input and output is increased, although the impedance transformation ratio was kept constant. Therefore, the values of the tuning capacitors at the secondary side of the input transformer and at the primary side of the output transformer were increased to 700 fF at the input and 540 fF at the output. A further consequence of the increased leakage inductances is that the feedback of the input and output stage must be retuned to ensure stable operation. The feedback inductances were not changed, only the resistor of the input stage was reduced to $10\,\Omega$ and the capacitor was increased to 2 pF. The resistor of the output stage feedback was increased to $15\,\Omega$ and the capacitor was reduced to 1.5 pF.

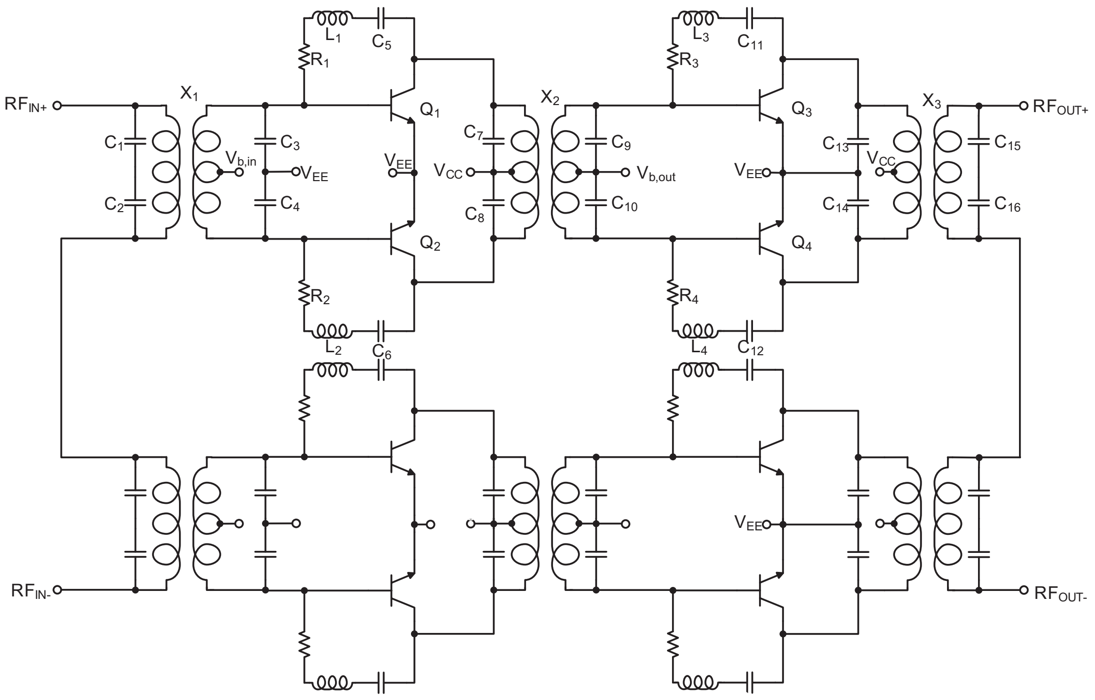


Figure 4.25: Schematic of one half of the power combined power amplifier

The layout of the power amplifier is shown in Fig. 4.26. The full predefined chip size is 1866 × 1428 μm^2. The supply rails are splitted in this layout to avoid unattended feedback loops due to the supply rails between the input and output stages of the individual PA cores and between both combined PAs. Furthermore, the bias of the input and output stage is externally adjustable, for both PA cores simultaneously and separately for both PAs. The layout of the input and output transformer were designed with multiple runs of electromagnetic simulation to provide a similar impedance transformation ratio as in the case of packaged PA and to determine the center tap of the unsymmetrical structure. Both implemented power amplifiers are not combined on-chip but have separate input and output bond pads that allows to measure the performance of a single PA in the case that the power combining of both PAs could not be realized and ends up with a nonfunctional power amplifier.

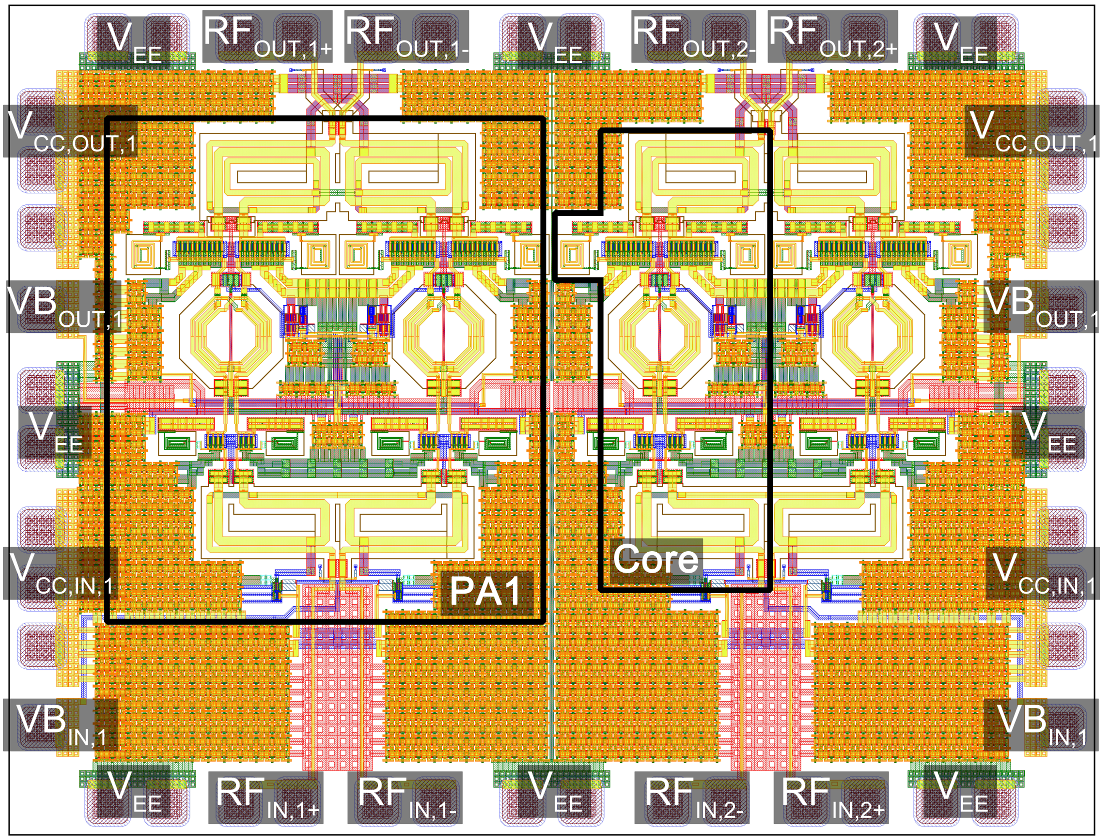
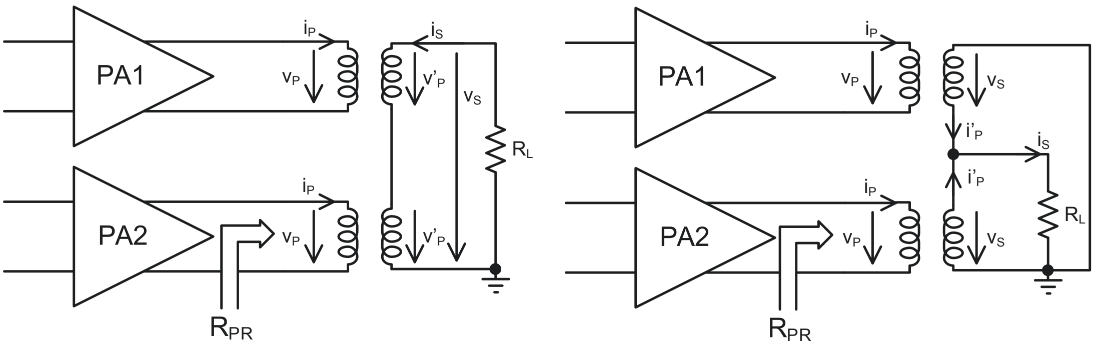


Figure 4.26: Layout of the full power combined power amplifier

4.2.2 Series-Parallel Transformer-based Power Combining

Power combining is widely used in RF power amplifier designs to increase the output power. Two basic variants are common, the series power combining and the parallel power combining. Power amplifiers operating at the X-band are for both variants. Series power combining utilizing transformers is demonstrated in [Comeau 11] although this PA is implemented in a CMOS technology. A PA utilizing one form of parallel power combining is shown in [Andrews 08]. Instead of an on-chip combining, the PA is realized as open-collector PA and combined on a substrate.

The basic idea behind both methods is shown in Fig. 4.27 at the example of two combined power amplifiers. In the case of a series combining, the individually transformed output voltages v_2 are summed up at the load, whereas the power combining of the second variant in Fig. 4.27(b) is realized through the addition of both output currents i_2. The major advantage of a series combining is the relaxed requirements concerning the impedance transformation ratio. Assuming an ideal transformer and a



(a) (b)

Figure 4.27: Basic power combining schemes, (a) – Series power combining, (b) – Parallel power combining

purely ohmic load, the impedance at the transformer's primary side R_{PR} results to:

$$R_{PR} = \frac{1}{2} n^2 R_L, \text{ with } n = \sqrt{\frac{L_{PR}}{L_{SEC}}} \tag{4.18}$$

On the other hand, the impedance on the primary transformer side in the case of parallel combining is:

$$R_{PR} = 2n^2 R_L \tag{4.19}$$

That means that the output matching network needs a transformation ratio that is four times larger compared to a series combining at equal output power level. The answer on the question which combining scheme is more suitable depends on the actual circuit. Series power combining has the advantage of a low impedance transformation ratio. On the other hand, this low transformation ratio results in a low turn ratio of the transformer and this in turn could result in a low efficiency of the transformer.

To calculate the efficiency for series and parallel combining, the transformer has to be lossy, otherwise the efficiency would be always unity. For this, the ohmic losses of the primary winding are represented by a resistance $R_{P,L}$ and the ohmic losses of the secondary winding are taken by into account $R_{S,L}$. The efficiency, as ratio of power on the secondary winding to power on the primary, for the series combining is given by:

$$\eta_S = \frac{P_S}{P_P} = \frac{v_S i_S}{2 v_P i_P} = \frac{i_S^2 R_L}{2 i_P^2 \grave{R}_{PR}} = \frac{n^2 I_P^2 R_L}{2 i_P^2 \grave{R}_{PR}} = \frac{n^2 R_L}{2 \grave{R}_{PR}} \tag{4.20}$$

$$\text{with: } \grave{R}_{PR} = R_{P,L} + \frac{n^2}{2}(R_{S,L} + R_L)$$

$$\eta_S = \frac{n^2 R_L}{2R_{P,L} + n^2(R_{S,L} + R_L)} = \frac{1}{\frac{1}{R_L}\left(\frac{2R_{P,L}}{n^2} + R_{S,L}\right) + 1} \tag{4.21}$$

The transformer efficiency in the case of parallel combining is as follow:

$$\eta_S = \frac{P_S}{P_P} = \frac{v_S i_S}{v_P 2 i_P} = \frac{i_S^2 R_L}{2 i_P^2 \grave{R}_{PR}} = \frac{4n^2 I_P^2 R_L}{2 i_P^2 \grave{R}_{PR}} = \frac{2n^2 R_L}{\grave{R}_{PR}} \tag{4.22}$$

$$\text{with: } \grave{R}_{PR} = R_{P,L} + 2n^2(R_{S,L} + R_L)$$

$$\eta_S = \frac{2n^2 R_L}{R_{P,L} + 2n^2(R_{S,L} + R_L)} = \frac{1}{\frac{1}{R_L}\left(\frac{R_{P,L}}{2n^2} + R_{S,L}\right) + 1} \tag{4.23}$$

Comparing both efficiencies reveals that with increasing turn ratio n the efficiency in the case of a parallel combining scheme is larger relative to series combining. Although this analysis provides a first order estimation for a suitable combining scheme, any further losses, e.g. substrate coupling or interwinding capacitances, are neglected that will significantly influence the transformer's efficiency, especially for transformer with large turn ratios, and need to be considered for a final decision.

As already stated, power amplifiers using one of these two scheme were already reported. The presented power amplifier uses both schemes simultaneously. Two PAs are combined in series, and these two PAs are combined in parallel with another series combined pair. The series combination uses for the input and output transformer are structure which differs from the common symmetrical layout because any leakage inductance due to interconnections should be minimized. A 3D view of the input transformer is shown in Fig. 4.28.

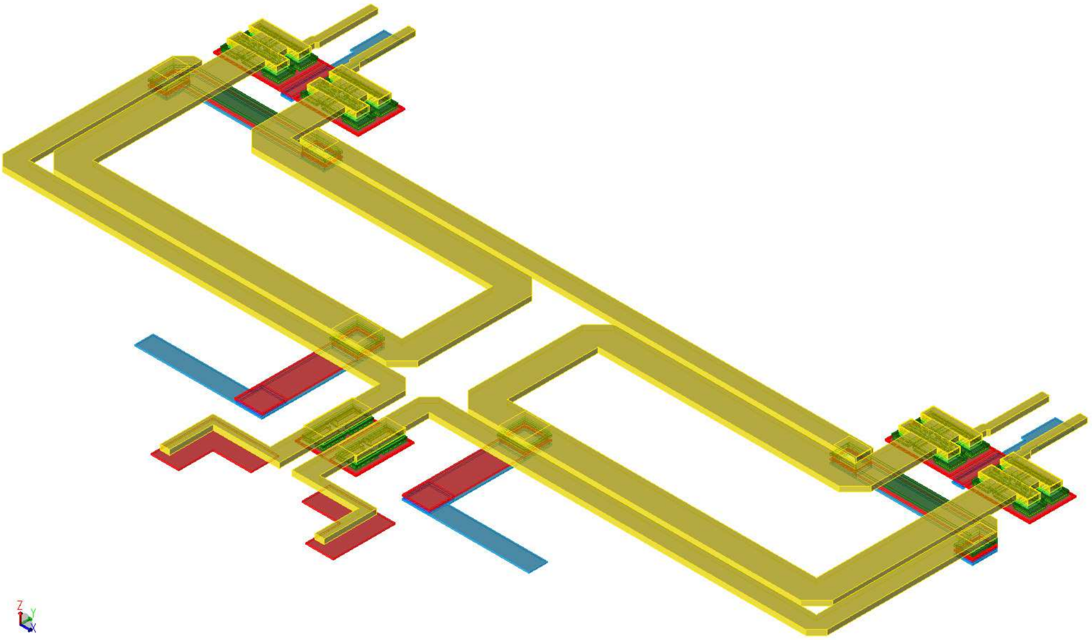


Figure 4.28: Input transformer for series combining

The full structure has an area of 456 × 250 µm^2 and was optimized by the use of electromagnetic simulation. The output combiner is shown in Fig. 4.29. Its area usage is 456 × 285 µm^2.

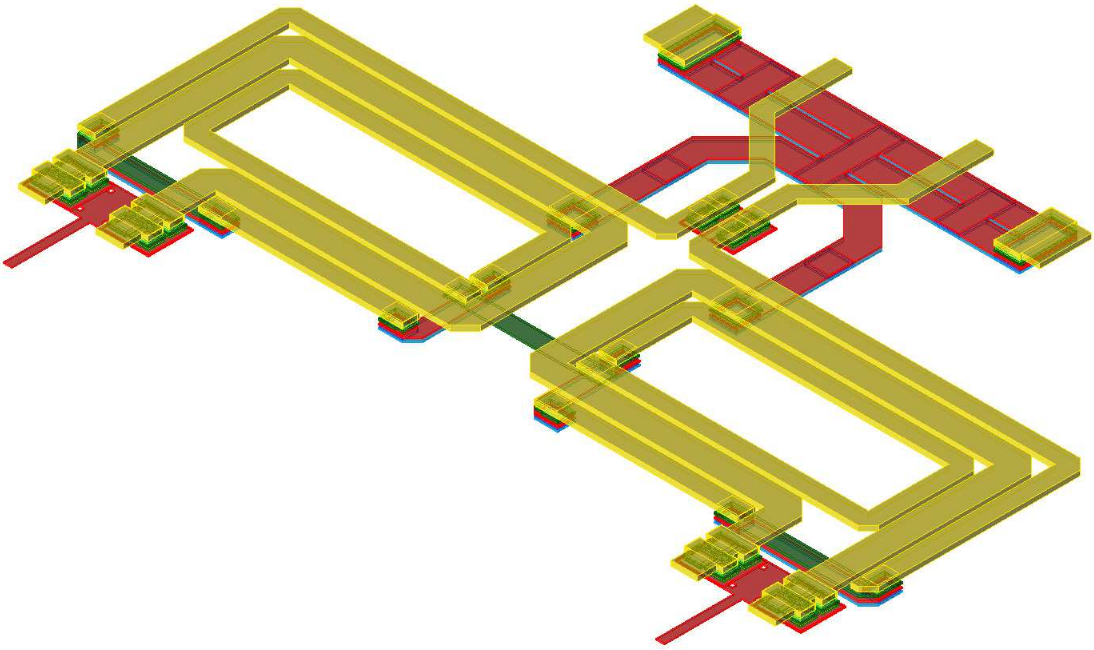
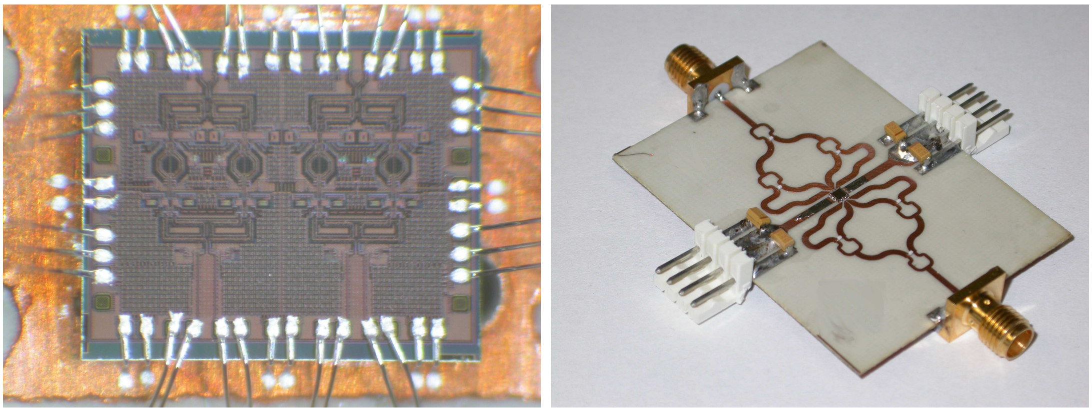


Figure 4.29: Output transformer for series combining

A major problem of this structure are different impedances seen by the transistors if the power amplifier is driven and loaded by a single-ended impedance. Unavoidable interwinding parasitic capacitances diminish the transformer performance in terms of an unbalanced-balanced converter by an additional impedance transformation of the source and load impedance. A second problem which results from this circumstance is the fact that each transistor will be driven and loaded by a different impedance which will influence the feedback performance, and hence, the stability. Therefore, it was decided to operate the amplifier differentially.

4.2.3 Experimental Results

The bonded chip and the PCB for measurements are shown in Fig. 4.30.



(a) (b)

Figure 4.30: Measurement setup for power combined PA, (a) – Mounted chip of the combined PA, (b) – Printed circuit board

A double-stacked Wilkinson combiner is used to connected the power amplifier to the source and load. Furthermore, the Wilkinson combiner is used to provide a differential signal at the PA input and combine the differential signal at the output by means of increasing the transmission line length near the PA on one side by an electrical length of $\lambda/2$. The small signal characteristic, measured with a supply voltage of 2 V in continuous mode, is depicted in Fig. 4.31.

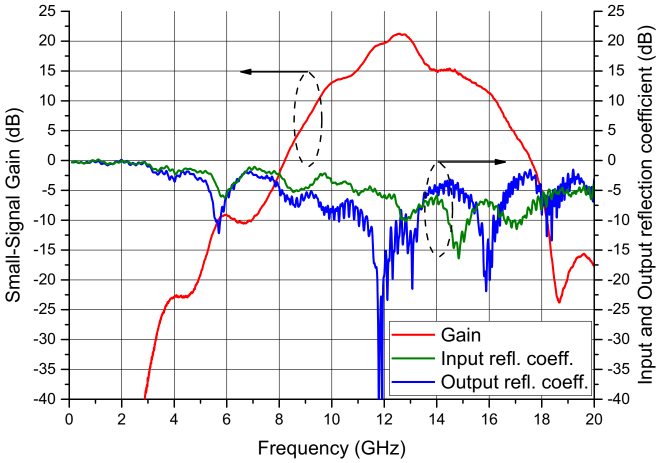


Figure 4.31: Small signal characteristic of the power amplifier

A maximum gain of 20 dB is observed at 12.6 GHz. The maximum output power and power-added efficiency as function of frequency is shown in Fig. 4.32.

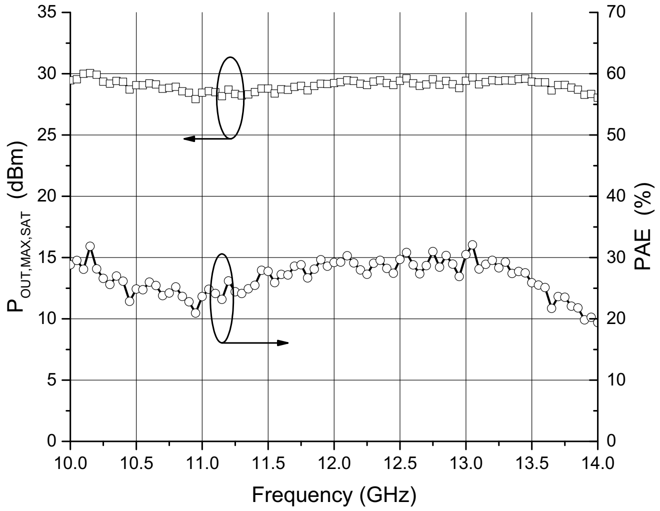


Figure 4.32: Maximum output power and PAE of the power amplifier

The maximum output power of 30.1 dBm is reached at 10.15 GHz, whereas the maximum value for PAE (32.1 %) is at 13.1 GHz.

4.3 Power Amplifiers in a 0.25 µm SiGe:C BiCMOS Technology

The transistors of IHP 0.25 µm SiGe:C BiCMOS technology are less performant compared to Infineon HBTs. However, it will be demonstrated that a power amplifier ("Thesis PA 4") incorporated in this technology achieves similar performance results. Furthermore, a second power amplifier ("Thesis PA 5") which utilizes parallel power combining exhibits a maximum output power of 30 dBm, driven and loaded single-ended.

4.3.1 Circuit Description

The amplifier's topology is similiar to the previous presented PAs. On-chip transformers were used for impedance matching and the extrinsic feedback stabilizes and neutralizes the transistors. The schematic is shown in Fig. 4.33.

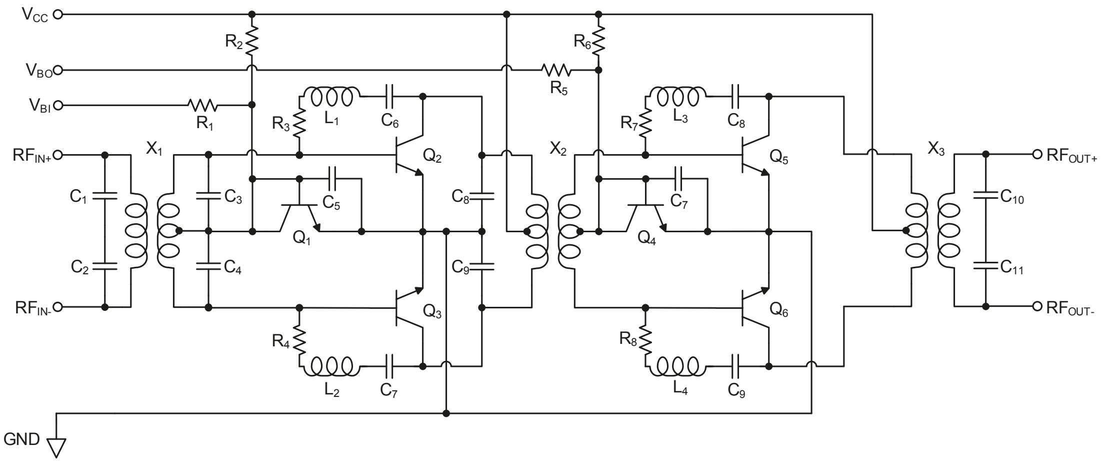
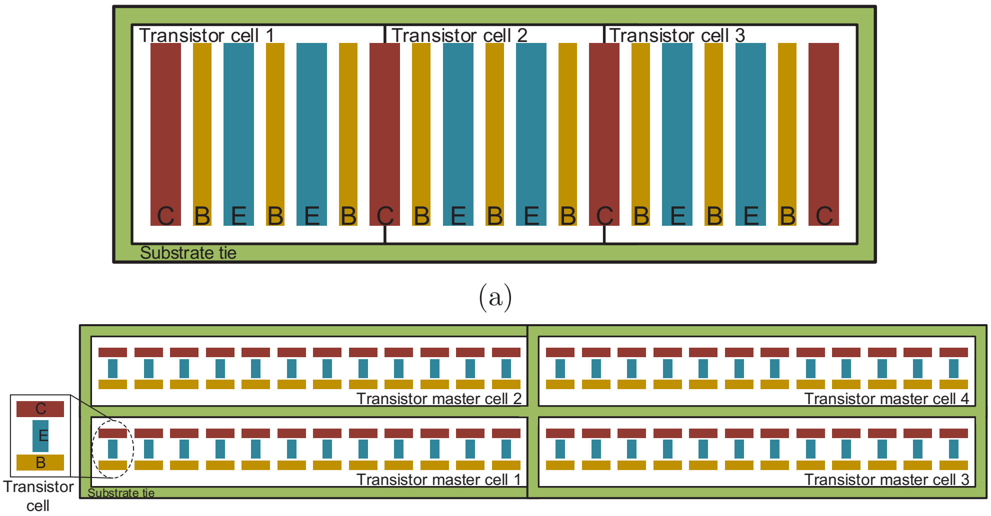


Figure 4.33: Schematic of the single power amplifier

One challenge in the design of efficient PAs in this technology is the layout of the predefined transistor layout cell which should be now considered in more detail. Wiring parasitic introduced through resistances, inductances and metal-metal capacitances of interconnections between parallel-connected transistors introduce additional losses that degrade the efficiency. In particular, wiring parasitics of large transistor arrays in the output stage degrade the performance significantly of the power amplifier. Moreover, not only losses are introduced but also the intrinsic characteristic of a transistor array will be changed by the parasitics, which must be considered in the design.

Advanced SiGe technologies, as the Infineon process, allow a straightforward parallel connection by modifying the connection scheme of the transistor and placing multiple layout cells in a row, as shown in Fig. 4.34(a). Furthermore, some foundries provide parametric layout cells with variable emitter length, and thus, the number of transistors to be combined can be reduced. In contrast to advanced SiGe technologies, the transistor cell of IHP transistors has a small fixed emitter area and is limited to a single base, emitter and collector contact. Up to twelve cells can be combined to one master cell, resulting in an emitter area A_E of 2.2 µm^2. Further enlargements of the array can only be realized by vertical and horizontal stacking of several master cells, as depicted in Fig. 4.34(b). However, design rules stipulate a minimum spacing between each master cell. This in turn increases the metal area for interconnections, and thus, increasing wiring parasitics.



(a)

(b)

Figure 4.34: Example sketches for parallel-connected single transistor cells, (a) – Sketch of an advanced technology with scalable emitter length and variable connection scheme. (b) – Technology used with transistor master cells and horizontal and vertical stacking.

In agreement with the foundry, new transistor layout cells were designed to optimize the area usage. For this, the predefined layout cell with twelve single transistors was broken up, and instead of only twelve transistors, 24, 48, 96 and 120 HBTs can be now placed inside the new master cell, shown in Fig. 4.35.

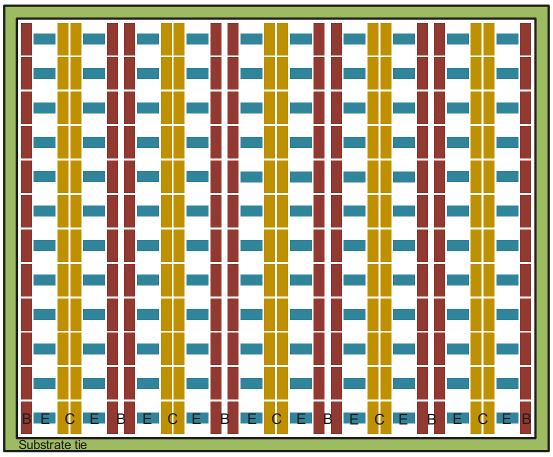


Figure 4.35: Sketch of the modified transistor layout with an emitter area of 22 µm^2

The maximum number of individual transistors results in an overall emitter area of 22 µm^2. The crucial advantage is a total reduction in area of about 40 % for 120 combined HBTs relative to a conventional layout. The difference in area usage of both layouts is shown in Fig. 4.36.

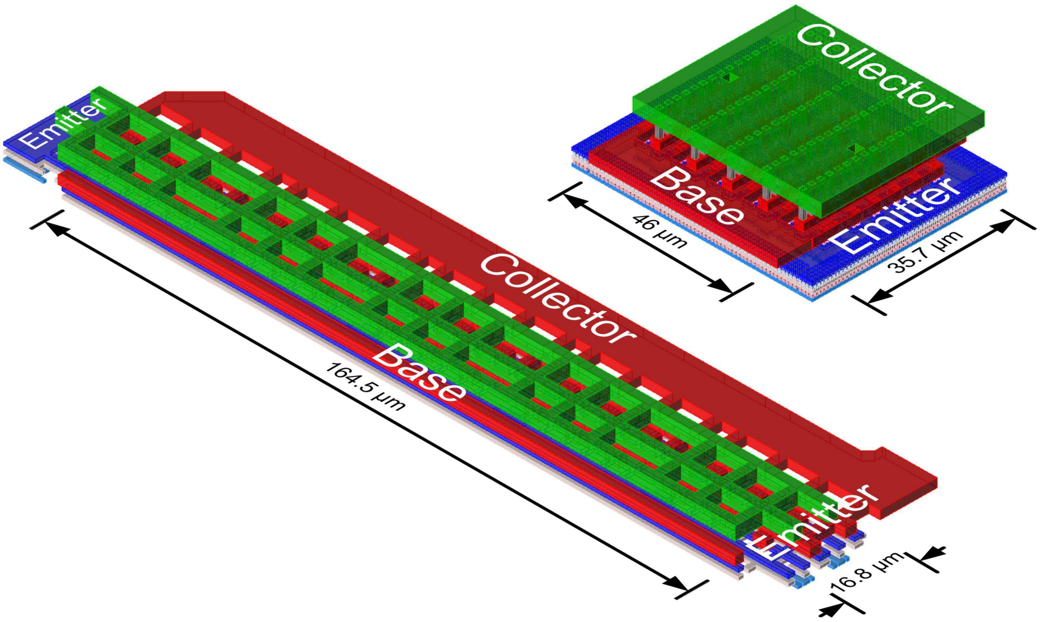


Figure 4.36: 3D view of two transistor layouts with an emitter area of 22 µm^2, the lower layout is designed with predefined layout cells, the upper layout is an improved layout variant, the scaling is equal to each other.

To demonstrate the performance improvement of the revised layout, both interconnection wiring layouts were extracted and characterized through electromagnetic simulation. The results have been included in the transistor model. Subsequently, load-pull simulations with different array sizes were used to determine the maximum output power and efficiency dependent on the transistor array layouts. The results are shown in Fig. 4.37. All values are normalized to values for ideal combined transistors, that is, without wiring parasitics.

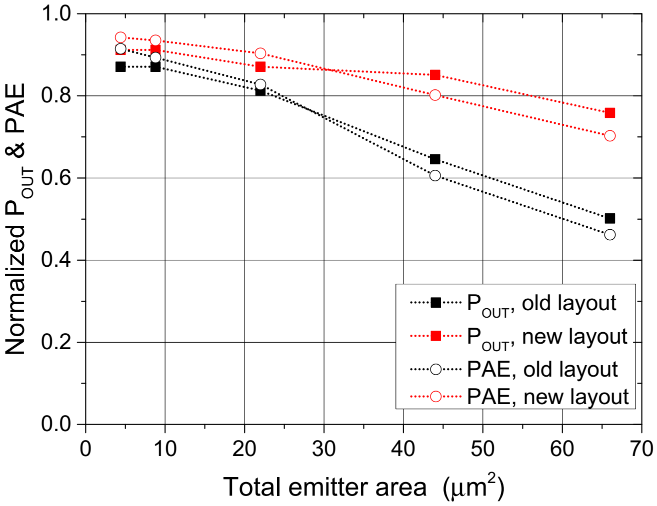


Figure 4.37: Normalized maximum output power and power-added efficiency of the conventional and improved layout concept.

It is immediately apparent from Fig. 4.37 that the revised layout will improve the performance of a PA. It becomes even more significant with an increase in array size. For example, the maximum output power and power-added efficiency will drop by almost 50 % for a conventional layout with A_E=66 µm^2 relative to lossless connected transistors. By contrast, the performance loss of the revised layout is only about 25 %. Furthermore, the diagram reveals that an excessive increase of the transistor array leads to an unequal increase in output power. Although a higher output power is provided by the array, the overall efficiency is, however, already significantly limited.

The output stage (Q_5–Q_6) has a total emitter area of 88 µm^2. That is, two modified transistor layout cells with A_E = 22 µm^2 were used for each branch. The collector quiescent current density was set to 1.1 mA/µm^2 which is much lower than the previously given value at maximum transit frequency. It had to be taken into account that the quiescent current of weakly biased silicon bipolar transistors, i.e. Class B or weak Class AB operation, depends strongly on the input signal strength [McRory 96]. This self-bias effect affects the efficiency and the gain characteristics as a function of input signal level and needs to be considered. The emitter area of the input stage (Q_2–Q_3) is 17.6 µm^2 with a quiescent current density of 1.9 mA/µm^2. The current density has been increased in comparison to the output stage to improve its linearity.

The turn ratio of the output transformer X_3 is 1 : 2, and its size is $188 \times 188\,\mu\text{m}^2$. Metal-insulator-metal (MIM) capacitors on the secondary coil of X_3 were used for resonance tuning. Discrete tuning capacitors on the primary coil of X_3 were omitted because the extracted values of the wiring capacitances from Q_5 and Q_6 indicate that no discrete tuning capacitors were necessary for resonant operation. The area of the interstage transformer X_2 is $120 \times 120\,\mu\text{m}^2$ with a turn ratio of 2 : 1. Tuning capacitors were only used on the primary coil, the secondary coil is already in resonance by the wiring capacitances of the output stage. The input transformer X_1 has a turn ratio of 2 : 1 and an area of $110 \times 110\,\mu\text{m}^2$. Discrete tuning capacitors on both coils were necessary for transformer's resonance at the working frequency due to the smaller transistor size of the input stage, and hence, smaller wiring capacitances.

The quiescent currents of the input and output stage are set by low ohmic reference networks (Q_1, Q_4). Consequently, the collector operating voltage is not limited to the collector-emitter breakdown voltage BV_{CEO}, as previously presented. Both reference networks are adjustable from outside.

The extrinsic feedback of the input stage is realized by an inductance value of 1.2 nH and the value of the capacitor is 2.35 pF. The feedback resistor was chosen to 10 Ω. The inductance of the output stage feedback is reduced to 0.55 nH. The feedback capacitor and resistor values are 3 pF and 3 Ω, respectively. The layout of the chip is depicted in Fig. 4.38. The overall chip size is $1.3 \times 1.1\,\text{mm}^2$.

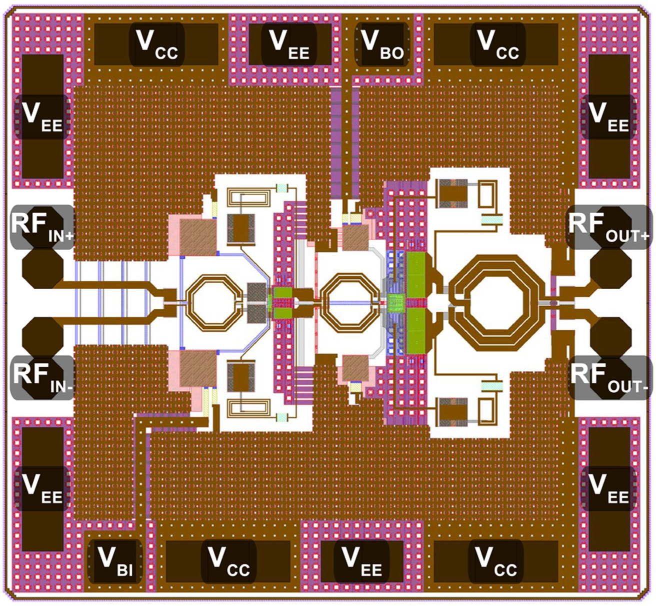


Figure 4.38: Layout of the single IHP power amplifier

4.3.2 Parallel Power Combining

The intention was to combine two PAs to increase the output power by a single transmission line on a printed circuit board off-chip but to take the impedance alteration at the input and output by the on-chip matching networks into account. For this, two individual power amplifiers, which are based on the single PA, are placed with separate input and outputs, as shown in the layout of Fig. 4.39. The power amplifiers themselves do not differ from the presented single power amplifier, only the input and output transformer was changed.

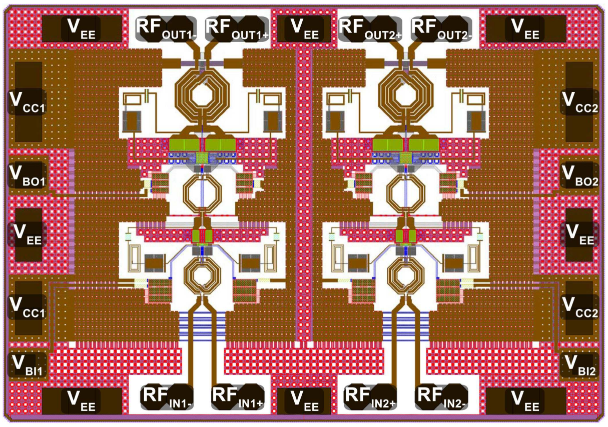


Figure 4.39: Layout of the parallel power combined PA

As the impedance transformation ratio is increased due to the parallel combining, and consequently, will result in low efficient matching networks, it was decided to decrease the transformation ratio at the output by utilizing a microstrip transmission line impedance transformer. The system load impedance of 50 Ω is transformed to 35 Ω at the output of the power amplifier. Furthermore, the opposite sides of the transformer are not simply connected to system ground but to a specific impedance. This allows an additional degree of freedom for a post-design impedance matching. The general concept of this power combining is shown in Fig. 4.40.

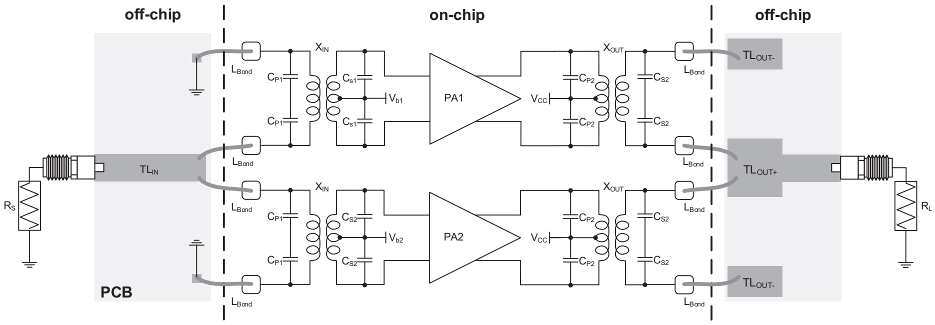


Figure 4.40: Scheme of the parallel power combining

4.3.3 Experimental Results

Both power amplifiers were bonded onto 20 × 20 mm^2 copper blocks. The copper blocks were mounted underneath a 508 µm Rogers 4003 substrate and bond wires connect the chips with PCB traces. The bonded chips of the single and power combined PA are shown in Fig. 4.42(a) and Fig. 4.42(b), respectively. The PCBs for measurements are depicted in Fig. 4.42(c) and Fig. 4.42(d).

The single power amplifier was operated from a single dc supply voltage V_{CC}=2.3 V in continuous mode. An external adjustment of the internal amplifier's biasing circuit was not necessary for the measurements. That is, the connectors V_{BO} and V_{BI} in Fig. 4.42(b) were left open during measurements. The characteristic impedance of the input and output transmission lines are 50 Ω with an electrical length l=λ at 10 GHz.

The small-signal characteristics of the single PA are shown in Fig. 4.41.

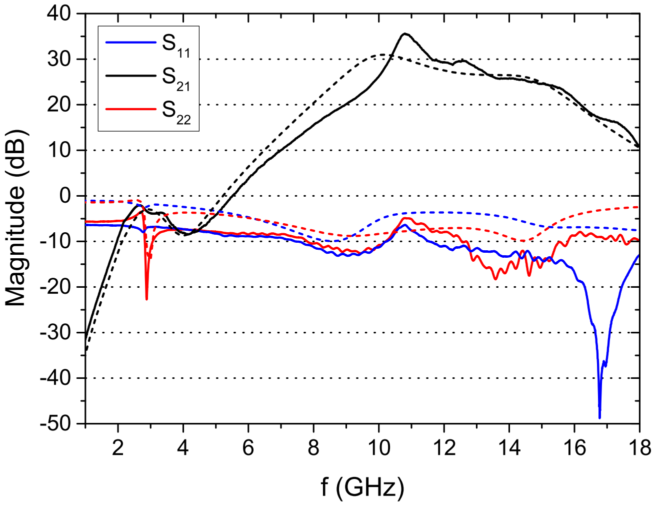
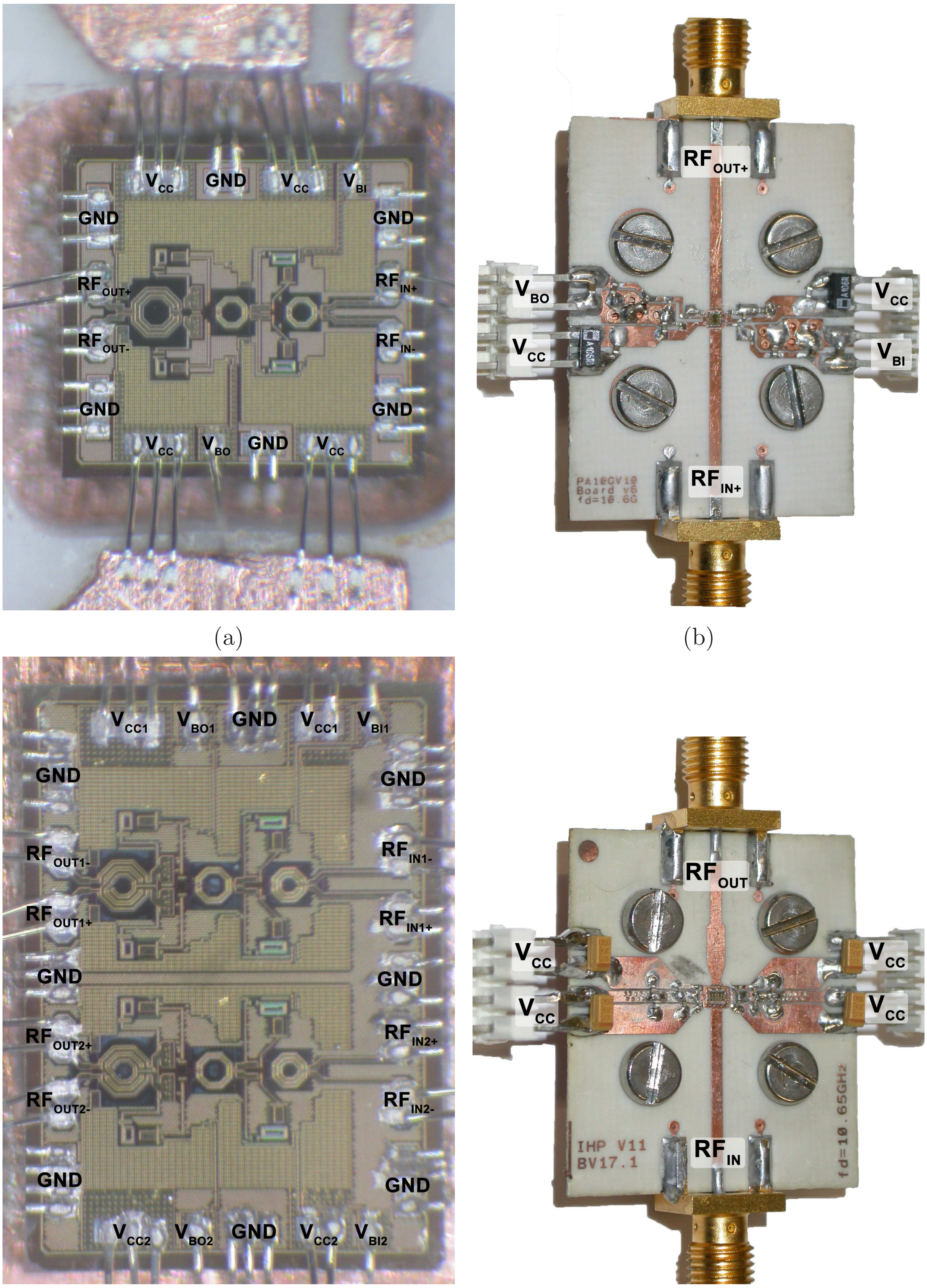


Figure 4.41: S-parameters of the single amplifier, measurement (solid lines) and simulation results (dashed lines)

The small-signal characteristics show a measured maximum gain of 35.5 dB at 10.7 GHz. Except the protrude gain peak, the measurement results are in good agreement with the simulation results. It should be noted that the printed circuit board is fabricated by hand and the power amplifier is bonded manually. Therefore, the assumption of the load and source impedance including bond wires and transmission lines in the simulation will differ from the real design. Consequently, the impedances seen by the transistors will differ and result, in conjunction with the extrinsic feedback, in for example such gain characteristic.

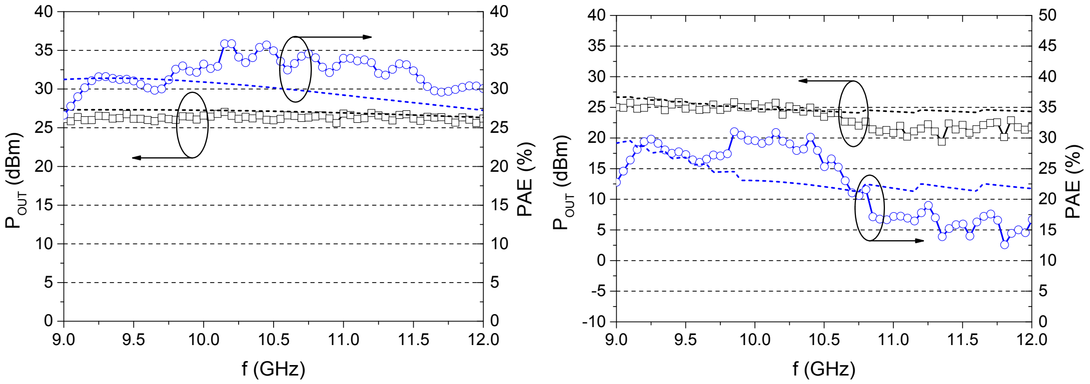
Fig. 4.43(a) shows the maximum output in saturation and maximum efficiency versus the frequency.



(a) (b)

(c) (d)

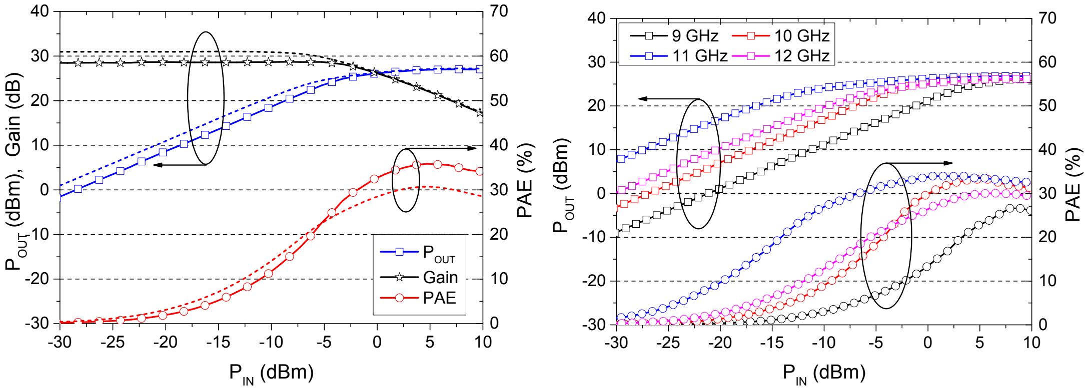
Figure 4.42: Measurement setup for IHP PAs, (a) – Single PA chip, (b) – PCB for single PA, (c) – Combined PA chip, (d) PCB of the combined PA



(a) (b)

Figure 4.43: Large signal characteristic, (a) – Maximum output power and PAE in saturation. (b) – Maximum output power and PAE at the 1dB-compression point

The maximum output power is 27 dBm at 10.15 GHz and the maximum power-added efficiency is 35.9 %. Additionally, the output 1-dB compression point with the corresponding power added efficiencies is depicted in Fig. 4.43(b). Furthermore, the figures 4.44(a) and 4.44(a) show the power transfer characteristic at 10.15 GHz and four power transfer characteristics at different frequencies, respectively.



(a) (b)

Figure 4.44: Large signal characteristic, (a) – Maximum output power and PAE in saturation. (b) – Maximum output power and PAE at the 1dB-compression point

The simulation and measurement results for the power combined PA are obtained at a higher supply voltage. V_{CC} was increased to 2.5 V to achieve a maximum output power of 30 dBm. Furthermore, to obtain the same operating point of transistors, the biasing was decreased by externally bonding the V_{BO} and V_{BI} connections to ground. The input transmission line has a characteristic impedance of 50 Ω with an electrical length of 360°. The necessary impedance transformation at the output is realized by a $\lambda/4$-transmission line transformer. The impedance transformer was optimized with the use of electromagnetic simulations because a tapered structure was necessary to avoid long bond wires. Furthermore, the second ports of the output transformer are not connected to ground but are bonded to small open transmission lines which exhibit a capacitive characteristic.

The S-parameter are shown in Fig. 4.45. A measured maximum gain of 28.1 dB at 10 GHz was achieved with good agreement to the simulation results.

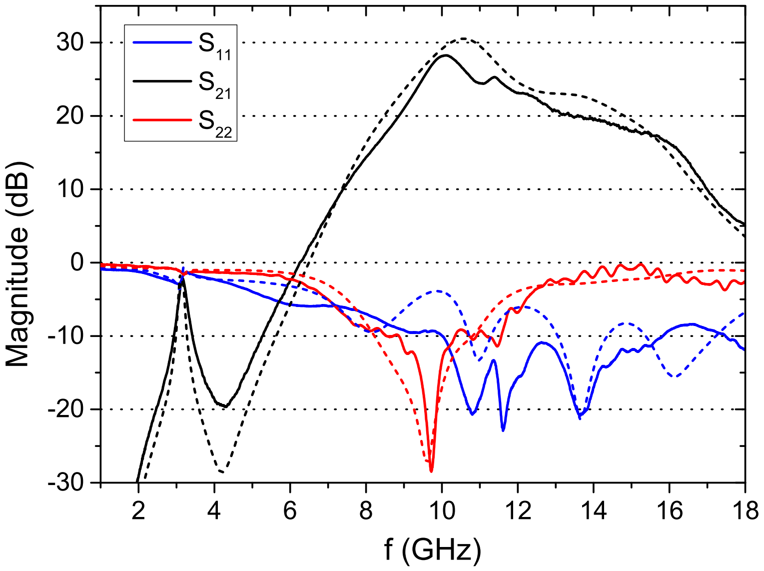


Figure 4.45: S-parameters of the power combined amplifier, measurement (solid lines) and simulation results (dashed lines).

Fig 4.46 shows the maximum output power in saturation and efficiency as a function of frequency. Because of the microstrip load impedance transformer, the bandwidth for large signal characterization is now decreased to 9–10.5 GHz. The maximum output power is 30.4 dBm at 10.15 GHz and the maximum power-added efficiency is 31.3 % at 9.45 GHz. To determine the linearity of the power amplifier, the output 1-dB compression point with the corresponding power added efficiencies is depicted in Fig. 4.47. Furthermore, the figures 4.48 and 4.49 show the power transfer characteristic at 9.45 GHz and four power transfer characteristics at different frequencies, respectively.

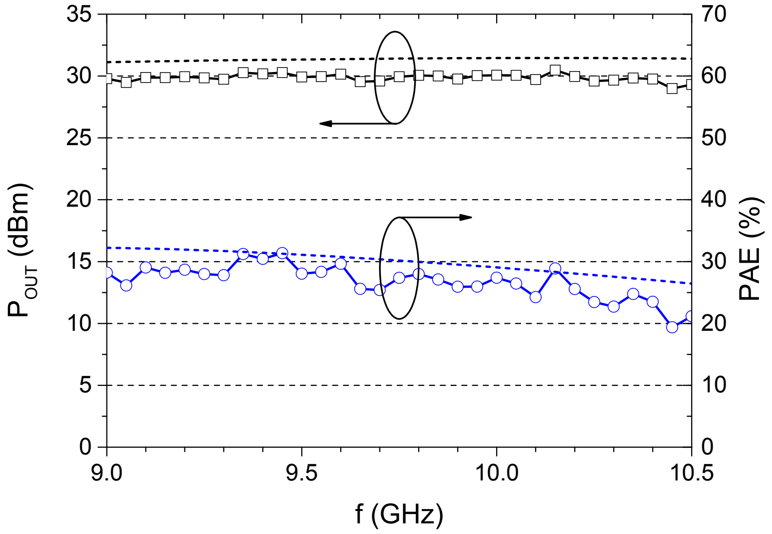


Figure 4.46: Maximum output in saturation and maximum efficiency as function of frequency, measurement (solid lines) and simulation results (dashed lines).

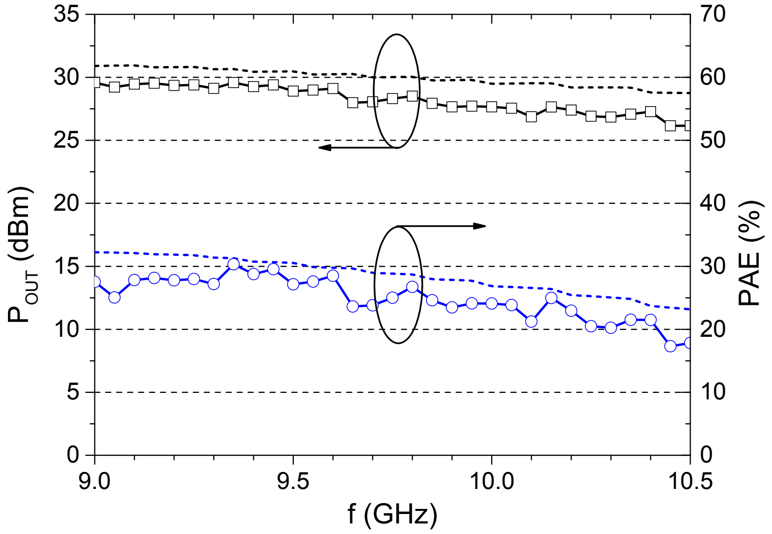


Figure 4.47: Output at 1-dB compression point and corresponding PAE as function of frequency, measurement (solid lines) and simulation results (dashed lines).

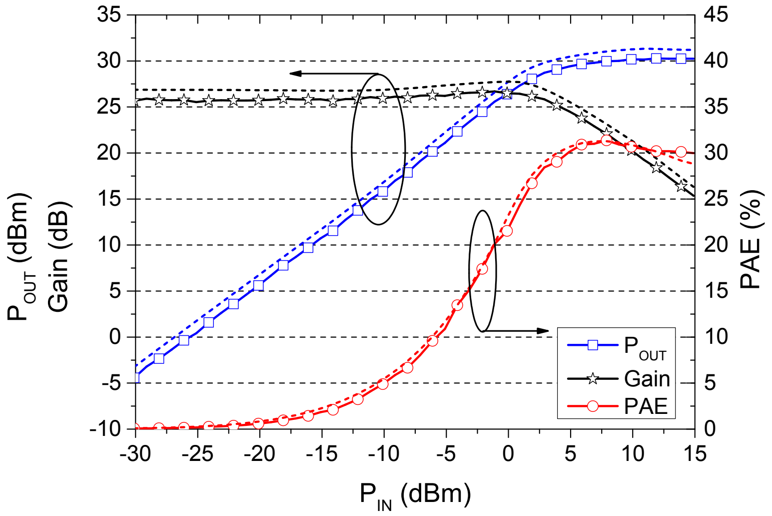


Figure 4.48: Power transfer characteristic at 9.45 GHz, measurement (solid lines) and simulation results (dashed lines).

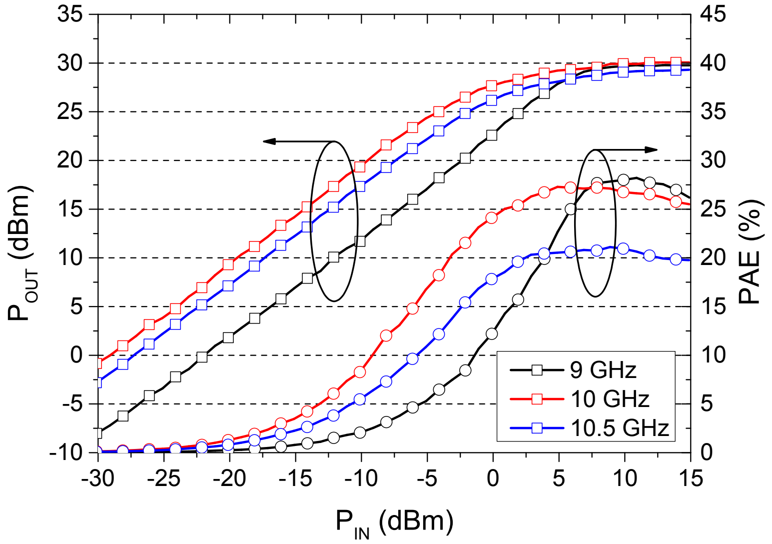


Figure 4.49: Measured power transfer characteristics at different frequencies.

Chapter 5

A Narrow-Band 8.7 GHz Low Noise Amplifier

The performance of low noise amplifiers are of crucial importance in the receiver chain because their noise contribution will mainly determine the the overall receiver noise figure. The outstanding role of LNAs can be best captured by the Friis formula which enables the calculation of the overall noise figure of a cascaded system, shown in Fig. 5.1.

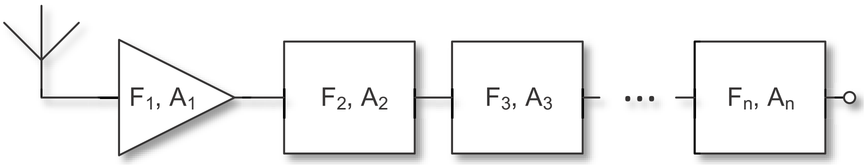


Figure 5.1: Calculation of the system noise figure

The expression for the overall noise factor F, and consequently for the noise figure NF, of a cascaded n-stage system is:

$$F_{sys} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + ... + \frac{F_n - 1}{A_1 \cdot ... \cdot A_{n-1}} = F_1 + \sum_{i=2}^{n} \frac{F_i - 1}{\prod_{k=1}^{i-1} A_k} \quad (5.1)$$

$$NF_{sys} = 10 \log F_{sys} \quad (5.2)$$

From (5.1) it is evident that the noise contribution of the first block will mainly determine the overall noise performance of the system, subsequent building blocks will have a minor influence on the system noise factor. Therefore, the first stage should be low noise as possible. Furthermore, (5.1) reveals that the gain value of the first stage affects the noise contribution of the following stages, and hence should be high.

The low noise amplifier presented in the following was intended as proof-of-concept for the passive frequency-selective feedback because it was used before only in power amplifier designs. As the use of the feedback was successful in the LNA design, the low noise amplifier utilizing the extrinsic feedback was implemented in a mixer design which is subsequently presented.

5.1 Circuit Design

The low noise amplifier was incorporated in Infineon's B7HF200 technology and was intended to exhibit high gain and low noise at stable operations, although the circuit is not based on the widely used cascode topology [Gerlich 12]. Further, the LNA should be narrow-band to ease the design of the LNA core and operate at a center frequency of 8.7 GHz, which is the lower frequency limit of upcoming mixer design.

The schematic of the LNA is shown in Fig. 5.2, which can be subdivided into three parts: At first, the low noise and high gain input stage is realized by Q_1. A cathodyne phase inverter, as second stage, is used to split the gained input signal into two signals that are 180° out of phase to each other. A fully differential amplifier (Q_3–Q_4) is used as third stage and is utilized as buffer for measurement purposes. The components ESD1–ESD4 protects the LNA against electrostatic discharge.

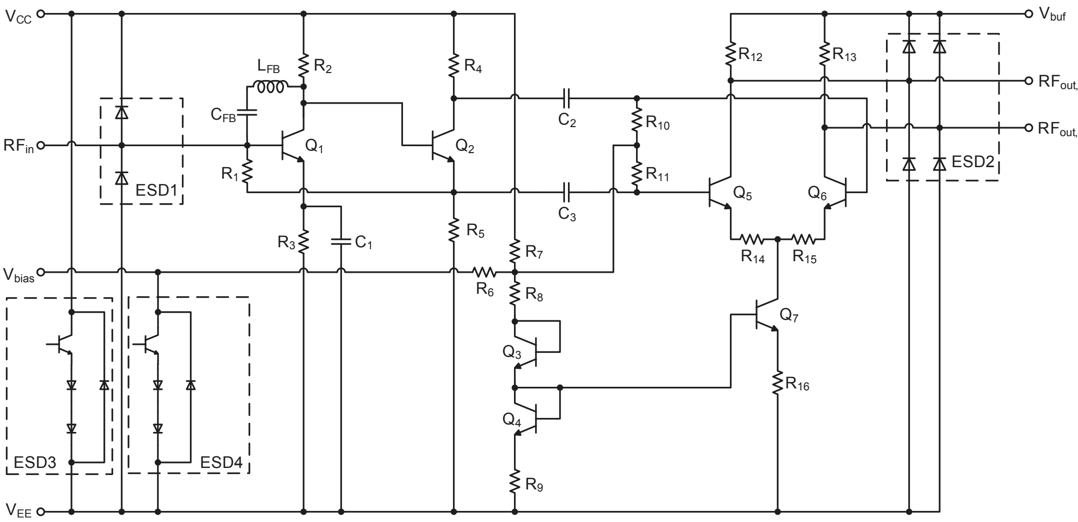


Figure 5.2: Schematic of the 8.7 GHz narrow-band low noise amplifier

Except in the feedback, the design was realized without inductances for biasing, matching networks or resonant tanks to allow a compact design.

Input stage Similar to the previous consideration of the noise figure of cascaded systems, the same principal can be applied to the three-stage amplifier with the consequence that the first stage of the LNA should provide high gain and a low noise contribution. Next to the intention to implement the extrinisic feedback, Q_1 is used in a common emitter configuration instead a common base configuration for the following reasons:

- The gain of a common emitter configuration is higher compared to common base because the a common base amplifier only provides a voltage gain, whereas the common emitter configuration provides both, voltage and current gain. As the gain is one critical criteria in this design, the common emitter configuration is preferred.
- The minimum noise figure of a common base transistor is higher if the noise from the transistor load is taken into account because the load noise will be transferred from the output to the input.
- The advantage of a wide-bandwidth frequency response, as offered by a common base topology, is not necessary in this design because the LNA should be narrow-banded.

The common design procedure for the size and operating point of Q_1 can be derived from the linear noise two-port theory [Gao 15]. In general, the noise factor in terms of y-parameters, that describe the linearized two-port transistor model, is given as:

$$F = F_{min} + \frac{R_N}{\Re\{Y_S\}} \left|Y_S - Y_{opt}\right|^2 \tag{5.3}$$

The admittances Y_S and Y_{opt} are the source and optimum noise transistor admittance, respectively, and R_N is the noise resistance. The minimum noise contribution of the transistor is represented by the minimum noise factor F_{min}. Straightforward from (5.3) is the fact that a optimal noise match is realized by $Y_S - Y_{opt}$ which results in $F = F_{min}$. The noise factor F_{min} depends on the actual transistor and operating point. To derive F_{min}, R_N and Y_{opt} the most important noise sources in a HBT are depicted in Fig. 5.3.

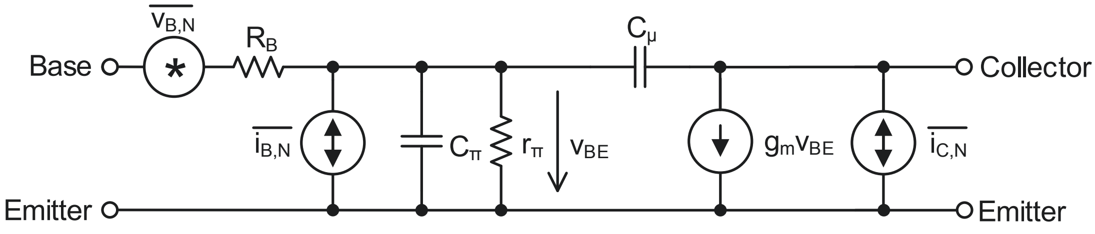


Figure 5.3: Simplified noise model of SiGe heterojunction bipolar transistor

The current noise sources $\overline{i_{B,N}}$ and $\overline{i_{C,N}}$ represent the mean square values for the shot noises, which are the result of carrier fluctuation due the potential barrier in pn-junctions:

$$\overline{i_{B,N}}^2 = 2qI_B\Delta f \tag{5.4}$$

$$\overline{i_{C,N}}^2 = 2qI_C\Delta f \tag{5.5}$$

It should be noted that although $\overline{i_{C,N}}$ is stated to the collector current, the origin of the shot noise is found in the electron current injected from the emitter into the base, passing the potential barrier of emitter base depletion region. The thermal noise contribution by the base resistance is given by:

$$\overline{v_{B,N}}^2 = 4kTR_B\Delta f \tag{5.6}$$

The factor Δf in (5.4)–(5.6) takes the measurement bandwidth into account.

The linear circuit noise theory enables now to represent the transistor as noiseless device and to transfer the intrinsic noise sources to the transistor's input where they are taken by one voltage and one noise source, which are also correlated to each other, into account, depicted in Fig. 5.4.

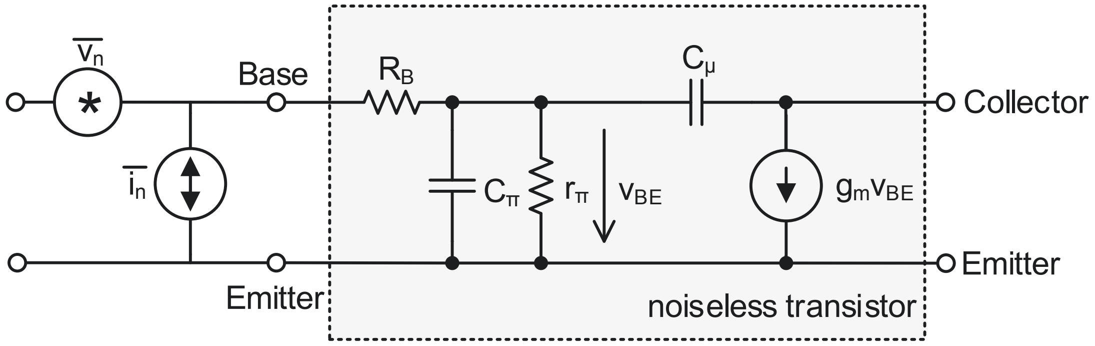


Figure 5.4: Input-referred noise model with two noise sources at the input and a noiseless transistor model

The mean square values of the voltage and current noise source and their correlation function are now replaced by their power spectral density [Niu 05]:

$$S_{v_N} = 4kTR_B + \frac{2qI_C}{|y_{21}|^2} \tag{5.7}$$

$$S_{i_N} = 2qI_B + \frac{2qI_C}{\left|y_{21}y_{11}^{-1}\right|^2} = \frac{2qI_C}{\beta} + \frac{2qI_C}{\left|y_{21}y_{11}^{-1}\right|^2} \tag{5.8}$$

$$S_{i_N v_N^*} = 2qI_C\frac{y_{11}}{|y_{21}|^2} \tag{5.9}$$

The y-parameters in the given expressions of the linearly approximated transistor are given by:

$$y_{11} = \frac{1}{r_\pi} + j\omega\left(C_\pi + C_\mu\right) = \frac{g_m}{\beta} + j\omega\left(C_\pi + C_\mu\right) \tag{5.10}$$

$$y_{12} = -j\omega C_\mu \tag{5.11}$$

$$y_{21} = g_m - j\omega C_\mu, \text{ with } g_m >> j\omega C_\mu \Rightarrow y_{21} \approx g_m \tag{5.12}$$

$$y_{22} = j\omega C_\mu \tag{5.13}$$

Substituting the y-parameters in (5.7)–(5.9) with the expressions of (5.10)–(5.13) results in transistor specific input referred noise sources:

$$S_{v_N} = 4kTR_B + \frac{2qI_C}{g_m^2} = 4kTR_B + \frac{2qkTg_m}{qg_m^2} = 4kT\left(R_B + \frac{1}{2g_m}\right) \tag{5.14}$$

$$\begin{aligned} S_{i_N} &= 2qI_C\left(\frac{1}{\beta} + \frac{g_m\beta^{-1} + j\omega\left(C_\pi + C_\mu\right)}{g_m}\right) \\ &= 2qI_C\left(\frac{1}{\beta} + \left(\frac{g_m}{\beta g_m}\right)^2 + \left(\frac{j\omega\left(C_\pi + C_\mu\right)}{g_m}\right)^2\right) \\ &\approx 2qI_C\left(\frac{1}{\beta} + \left(\frac{j\omega\left(C_\pi + C_\mu\right)}{g_m}\right)^2\right), \text{ with } \frac{1}{\beta} >> \frac{1}{\beta^2} \end{aligned} \tag{5.15}$$

$$S_{i_N v_N^*} = 2qI_C\left(g_m\beta^{-1} + j\omega\left(C_\pi + C_\mu\right)\right)\frac{1}{g_m^2} = 2kT\left(\frac{1}{\beta} + \frac{j\omega\left(C_\pi + C_\mu\right)}{g_m}\right) \tag{5.16}$$

The expressions (5.14)–(5.14) can be now used to derive the necessary component in (5.3). The noise resistance R_N is the equivalent noise resistance of the voltage noise source S_{v_N}:

$$S_{v_N} = 4kTR_N \Rightarrow R_N = \frac{S_{v_N}}{4kT} = R_B + \frac{1}{2g_m} \tag{5.17}$$

The optimum noise impedance at the source Y_{opt} can be derived to [Haus 60]:

$$Y_{opt} = G_{opt} + B_{opt} = \sqrt{\frac{S_{i_N}}{S_{v_N}} - \left(\frac{\Im\{S_{i_N v_N^*}\}}{S_{v_N}}\right)^2} - \frac{\Im\{S_{i_N v_N^*}\}}{S_{v_N}} \tag{5.18}$$

$$= \sqrt{\frac{g_m}{2R_N}\frac{1}{\beta} + \frac{\left(\omega(C_\pi + C_\mu)\right)^2}{2g_mR_N}\left(1 - \frac{1}{2g_mR_N}\right)} - j\frac{\omega(C_\pi + C_\mu)}{2g_mR_N} \tag{5.19}$$

The last parameter, the minimum noise factor, can be calculated by substituting $\Re\{Y_{opt}\}$ from (5.19), (5.7) and (5.9) into

$$F_{min} = 1 + 2R_N\left(\Re\{Y_{opt}\} + \frac{\Re\{S_{i_N v_N^*}\}}{S_{v_N}}\right) \tag{5.20}$$

and results to:

$$F_{min} = 1 + 2R_N \left(\sqrt{\frac{g_m}{2R_N}\frac{1}{\beta} + \frac{(\omega(C_\pi + C_\mu))^2}{2g_m R_N}\left(1 - \frac{1}{2g_m R_N}\right)} + \frac{1}{2R_N}\frac{1}{\beta} \right) \quad (5.21)$$

It is demonstrated in [Niu 05] that (5.21) can be simplified by the realistic assumption of $g_m R_B >> 0.5$ to:

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m R_B}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_t}\right)^2}, \text{ with } \left(\frac{f}{f_t}\right)^2 = \left(f\frac{C_\pi + C_\mu}{g_m}\right) \quad (5.22)$$

The first conclusion of the expression in (5.22) is that the minimum noise figure of a transistor will depend on its collector current density due g_m and f_t. Secondly, as R_B scales with the emitter width, the minimum noise figure will also depend on the emitter width W_E. The Fig. 5.5 shows the simulated minimum noise figure NF_{min} (noise factor in decibel dimension) at 8.7 GHz as function of the quiescent collector current density J_C and of the emitter width, which is selectable between 0.35 µm and 0.55 µm, of the chosen B7HF200 "npn1s" transistor.

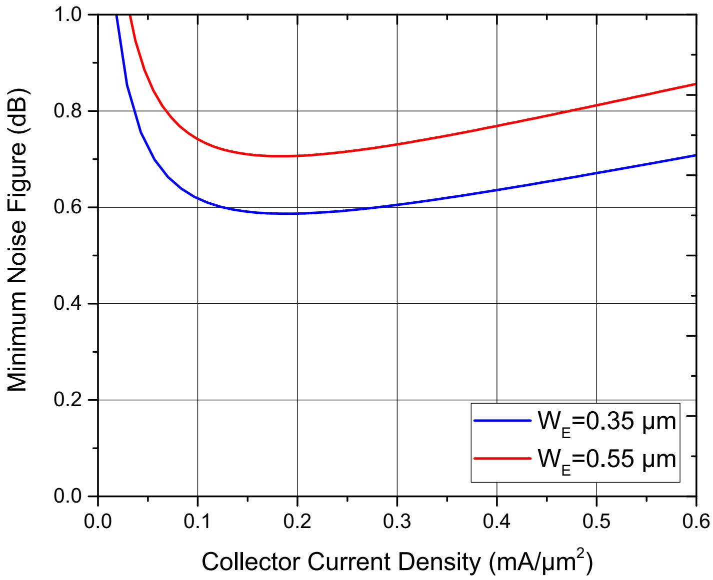


Figure 5.5: Simulated minimum noise figure NF_{min} of B7HF200 SiGe HBT "npn1s" as function of collector current density and emitter width at 8.7 GHz

It is visible that the larger emitter width of 0.55 µm increases NF_{min} because of the larger base resistance in the active transistor area and an emitter width of 0.35 µm was chosen. The dependence on the collector current can be straightforwardly explained by referring back to (5.7)–(5.8); At low collector current, the transconductance g_m ($\approx y_{21}$) is small, and consequently, the noise contribution will be dominated by the base resistance thermal noise. With increasing quiescent current, g_m will rise, and hence, the contribution of the input-refereed collector shot noise becomes smaller, the noise figure drops to a minimum value. Although a further increase in collector current leads to a further increase in g_m, the shot noise contribution of the base and collector will also rise, in particular the base shoot noise, and increase again the noise figure. For the implemented transistor, the optimal noise quiescent current was found to be 0.17 mA/µm^2. A variation in the emitter length will have a negligible influence on the transistor's noise performance at a given collector current density. Although it would reduce the base resistance, the transconductance will be increase g_m in (5.22) by the same amount of scaling, which can be investigated by considering $\sqrt{2(g_m \cdot S)(R_B \cdot S^{-1})}$ with S as emitter length scaling factor.

However, the emitter length will influence the optimum noise admittance and linearity of the transistor. The optimum noise admittance of a transistor with an emitter area A_E of 3.5 µm^2, as used in the simulation of NF_{min}, is $Y_{opt} = (1.5{+}j2)\mathrm{m}\Omega$, or as optimum noise impedance $Z_{opt} = (235.1{+}j321.6)\Omega$. A required matching network at the input for such admittance would significantly diminish the transistor's noise performance. The emitter length was therefore increased to an overall length of 60.7 µm and realized by four parallel connected transistors that utilize instead of a single base-emitter-collector (BEC) connection scheme a CBEBEBC connection scheme. In contrast to the BEC scheme, the noise figure is slightly reduced by a third base contact between the two transistors in this scheme (CBE-B-EBC). Furthermore, the advanced connection scheme allows a compact layout of the transistor, as seen in Fig. 5.6, which reduces wiring capacitances.

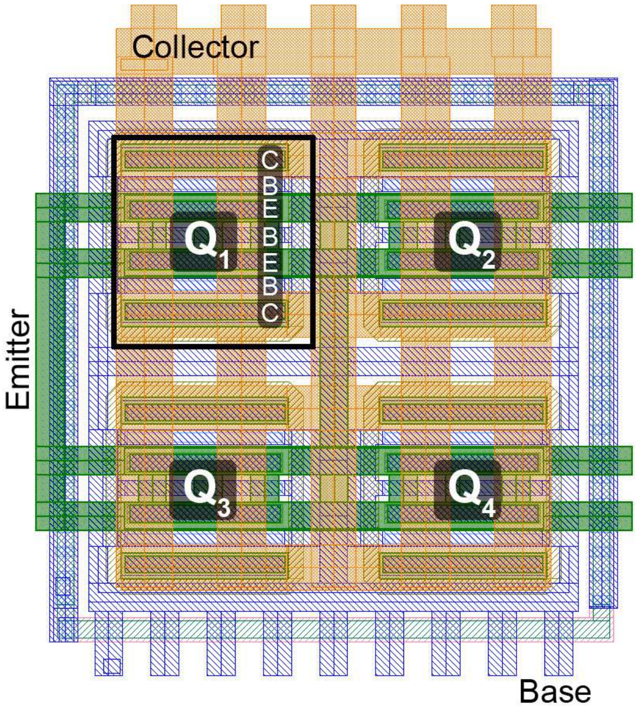


Figure 5.6: Layout of the input stage transistor with $A_E = 21.2\,\mu\mathrm{m}^2$

The overall area of the layout cell is $30 \times 30\,\mu\text{m}^2$. The resulting optimum noise impedance is reduced to $(31.8 + j50.1)\Omega$ at a collector current of 3.5 mA.

As seen in the schematic, Q_1 is biased by the subsequent stage through the resistor R_1. The value of R_1 was chosen to be high enough that it is only used for biasing and not to provide a feedback. Moreover, the large value results only in a small influence on the noise factor of Q_1. The collector resistor (R_2) is $350\,\Omega$ and the gain at lower frequencies is decreased by the emitter resistor R_3 which is bypassed at the working frequency by C_1 ($R_3 = 150\,\Omega$, $C_1 = 6\,\text{pF}$).

Similar to the power amplifier designs, the feedback mitigate the gain drop at the working frequency due to the base collector capacitance and stabilize the transistor additionally to the emitter resistor at lower gigahertz frequencies. Considering the simulated small-signal gain by means of s_{21} and the noise figure of the actual input stage without a feedback in Fig. 5.7, it is seen that the gain decreases monotonically with increasing frequency and the noise figure increases to higher frequencies.

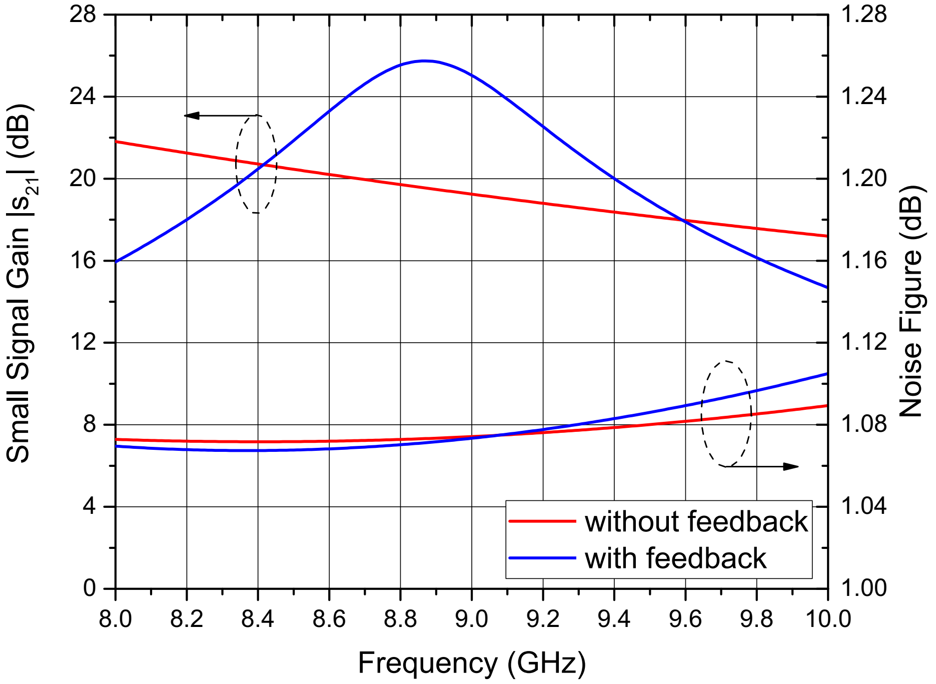


Figure 5.7: Simulated gain and noise figure of the input stage without and with applied feedback

By implementing the extrinisc base collector feedback with an inductance value of $L_{FB} = 2.3\,\text{nH}$ and a capacitance C_{FB} with a value of 3.2 pF, a decrease in gain is avoided, and moreover, the gain value at the operating frequency was increased, depicted in Fig. 5.7. The resulting noise figure is slightly reduced but exhibits a higher slope for higher frequencies due to the faster gain decrease above the resonance frequency between the feedback and the base collector capacitance. Since the LNA should be narrow-band the feedback does not use a discrete resistor to broaden the frequency response. Only the series resistance of the inductance L_{FB} was taken into account which was extracted from the inductance model obtained by electromagnetic simulation.

Phase inverter and buffer The conversion from a unbalanced to a balanced signal is realized by Q_2, which is implemented as cathodyne phase inverter that is known from the era of vacuum tubes. The signal at the collector is the inverted signal of the input, whereas the emitter signal is in phase with the input signal. Both signals are shown in Fig 5.8. The power gain of Q_2 at the collector and emitter is approximately unity.

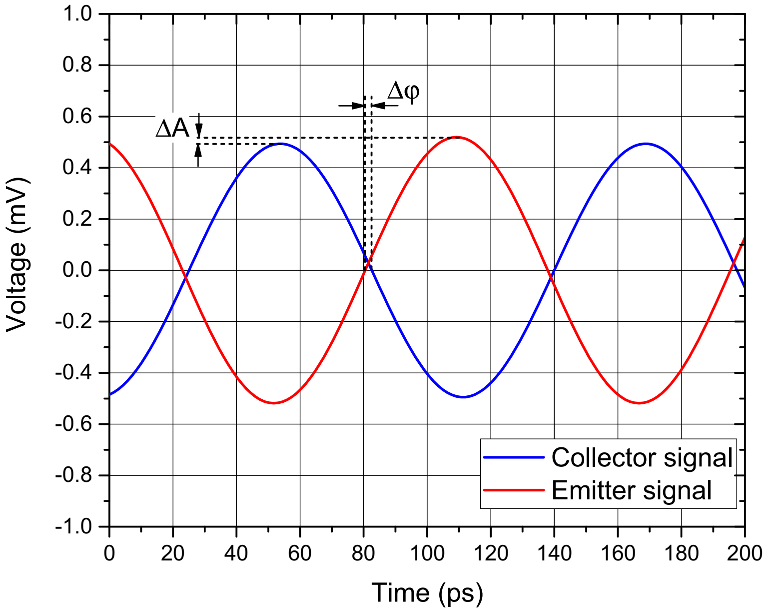


Figure 5.8: Output signals of the cathodyne phase inverter at 8.7 GHz

To reduce an amplitude and phase mismatch (ΔA, $\Delta\phi$), the phase inverter is loaded by the differential buffer $Q5$–$Q6$ which results in equal load impedances at the collector and emitter of Q_2. The tail current source $Q7$ is biased by Q_3 and $Q4$. The same network provides the base quiescent current for the differential buffer. Furthermore, the reference current through Q_3 and Q_4 is changeable externally. The supply voltage was separated from the LNA core supply voltage to deactivated the buffer by $V_{BUF} = 0\,\mathrm{V}$ and conduct the phase inverter signals through the base collector diodes of $Q5$–$Q6$ to the output.

The layout of the low noise amplifier is shown in Fig. 5.9. The full chip size is $0.93 \times 0.7\,\mathrm{mm}^2$. The free space of the chip was filled with decoupling capacitors between V_{CC} and V_{EE}, and V_{BUF} and V_{EE}.

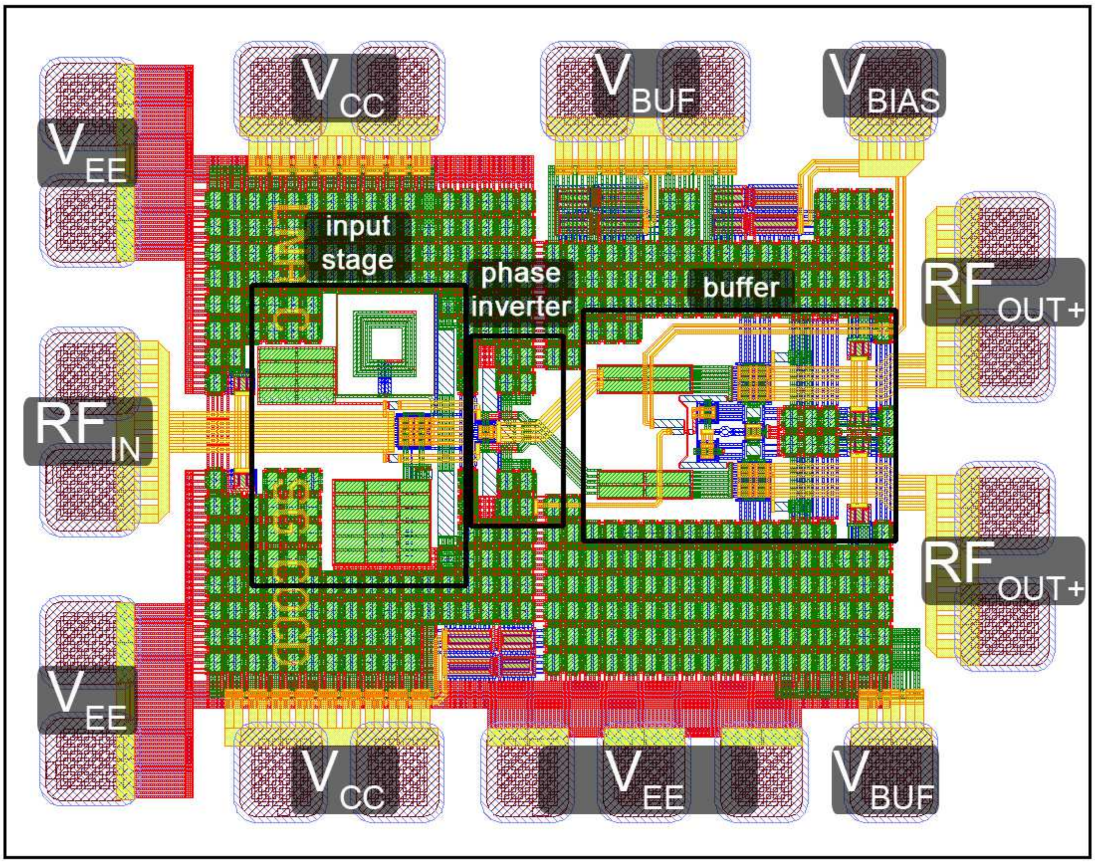


Figure 5.9: Layout of the narrow-band low noise amplifier

Following the completion of the layout, post-layout simulations with the use of electromagnetic simulation were run to optimize the LNA input stage and to take wiring parasitics into account. In particular, the input feeding lines between the RF_{in} bonding pad and Q_1 were optimized in terms of width to provide a sufficient inductance to match the transistor's impedance in conjunction with bond wire inductance and bonding pad capacitance.

5.2 Experimental Results

Instead of measuring the performance on-chip, the bare die was glued on Rogers 4003 substrate to evaluate the LNA performance, shown in Fig. 5.10. The external buffer bias connection was not bonded because a change in the buffer's bias setting will have a marginal influence on the LNA core performance. At the input was the intention to use two bond wires in parallel, and therefore, two bond pads have been placed in the layout. During the chip fabrication, further simulation runs predicted a better performance of the LNA if, instead of two bond wires, three bond wires will be placed in parallel with two bond pads. Therefore, the manual bonding process was optimized to place three bond wires on two bond pads.

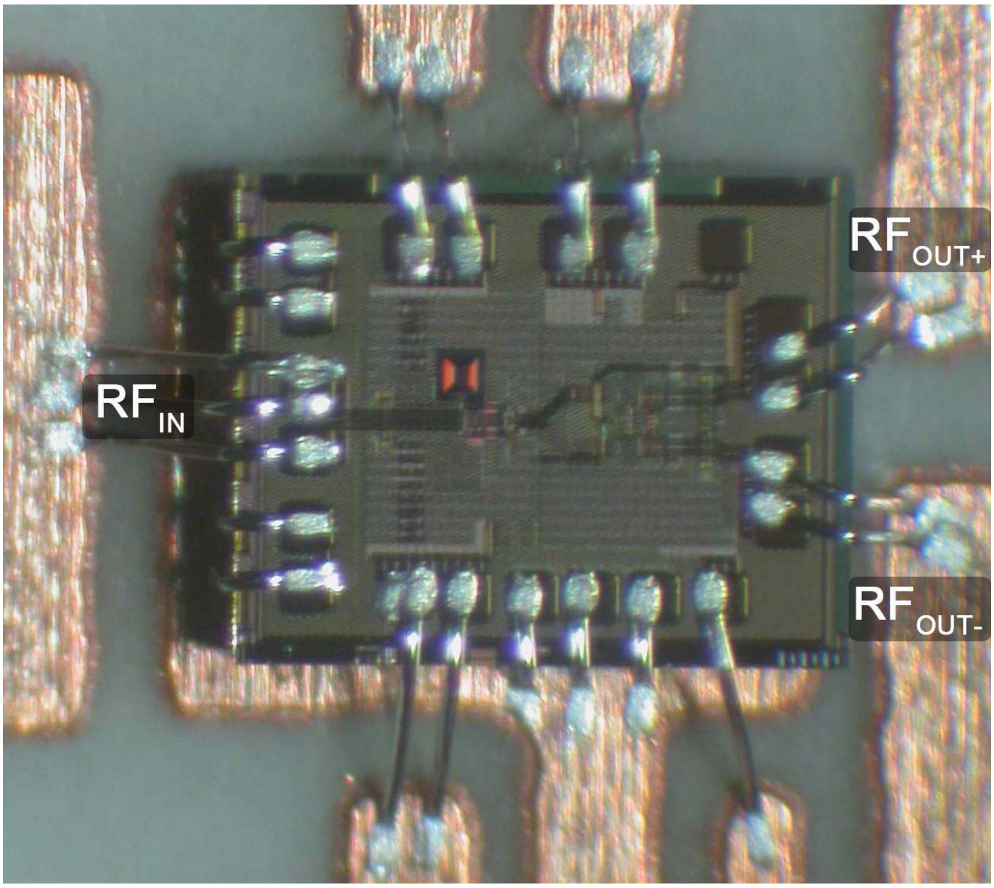
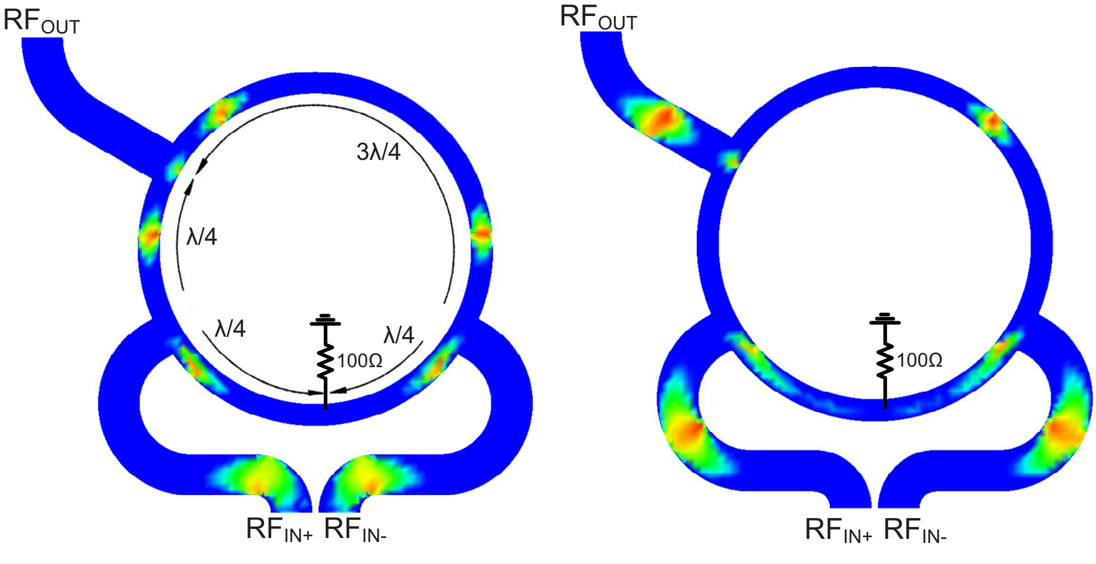


Figure 5.10: Chip photograph of the LNA of the bonded LNA

The differential output of the LNA was converted into a single-ended signal for measurements by the use of a rat-race coupler. The advantage of the rat-race coupler is its compact and simple design as is depicted in Fig. 5.11. A further advantage is that discrete components are not necessary except a resistor at the common node to dissipate the energy resulting from mismatches. The concept of the rat-race coupler is based on the λ-quarter transmission line impedance transformer which transforms a impedance Z_A to its input Z_I by:

$$Z_I = \frac{Z_O^2}{Z_A} \tag{5.23}$$

The impedance Z_0 is the characteristic transmission line impedance of the transformer, and the transmission line length must be a odd multiple of one quarter of the wavelength. As (5.23) is only applicable for one frequency, the bandwidth of the coupler is limited. However, the frequency response of the LNA was designed to be narrow-band, and thus, the limited bandwidth of the coupler is not of concern and the design frequency of the rat-race coupler was 8.7 GHz.



(a) (b)

Figure 5.11: Simulated rat-race coupler, the colored spots indicate high levels of a positive current density at a specific signal period T that allow to "follow" the waves in the coupler, (a) – $T = T_1$, (b) – $T = T_1 + \Delta T$

The complete measurement board is shown in Fig. 5.12. The input transmission line has a characteristic impedance of $50\,\Omega$ and an electrical length of $\lambda/2$. Discrete capacitors are used as decoupling capacitors.

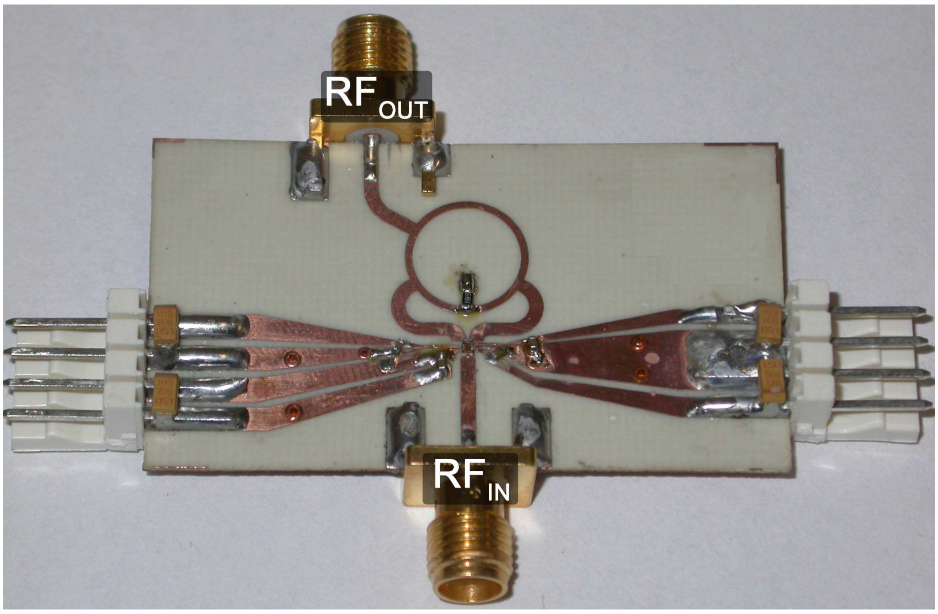
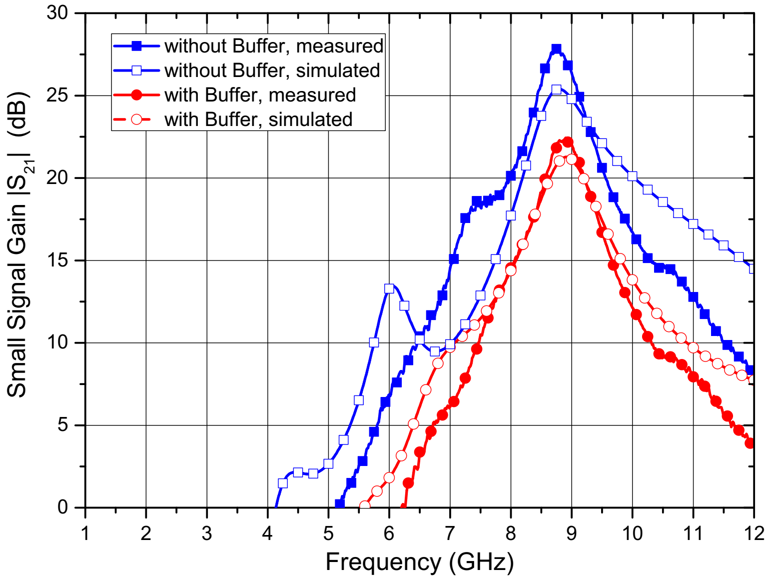


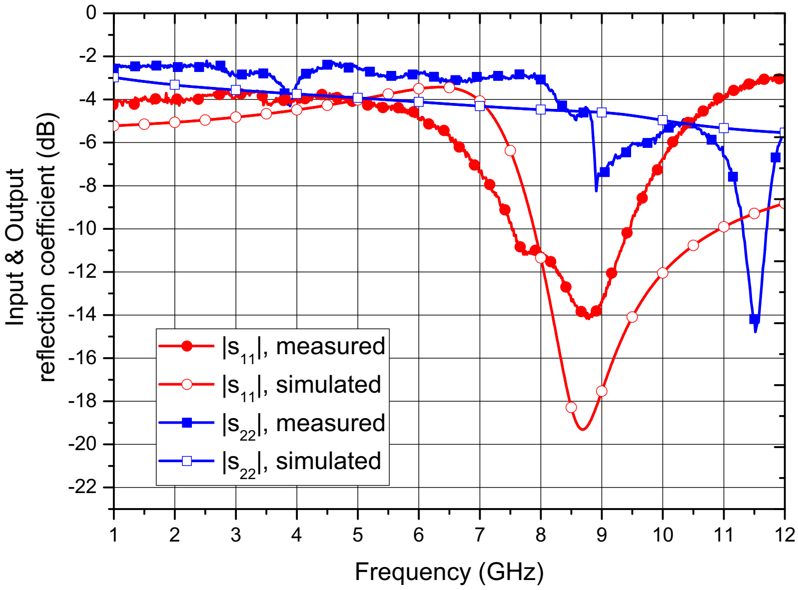
Figure 5.12: Measurement board for the LNA

The supply voltage of the buffer and LNA core was set to 3 V. The DC current drawn from the source was measured to 13.4 mA, which is approximately the value obtained by simulation (13.8 mA). In the case of $V_{BUF} = 0$ V, the dc current consumption is reduced to 9.5 mA that matches with the simulation result of 9.6 mA.

The measurement result of the small signal gain, input and output reflection coefficients are shown in Fig. 5.13(a) and Fig. 5.13(b), respectively.



(a)



(b)

Figure 5.13: Measured small signal characteristic of the LNA, (a) – Small signal gain, (b) – input and output reflection coefficients measured without buffer

A comparison between the simulated and measured small signal gain shows no frequency shift of the gain peak. The measured peak gain without buffer is 28.1 dB and with buffer 22.6 dB. The simulation results are 25.4 dB with and 21.3 dB without the usage of the buffer. The difference of roughly 2.5 dB between measured and simulated gain without buffer results from a different impedance seen by the phase inverter at deactivated buffer which was insufficiently modeled in the simulation. The input and output reflection coefficients in Fig. 5.13(b) matches well in the vicinity of 8.7 GHz, although the simulated input reflection coefficient predicts a better input matching. The simulation of the input reflection coefficients was simplified by a simple bond wire inductance model and transition mismatches between bond wires and transmission line as well as the transition between SMA connector and transmission line were neglected.

The noise figure of the low noise amplifier was measured with the use of a noise source and a spectrum analyzer that utilizes the Y-factor method to determine the system noise figure. The result is shown in Fig. 5.14

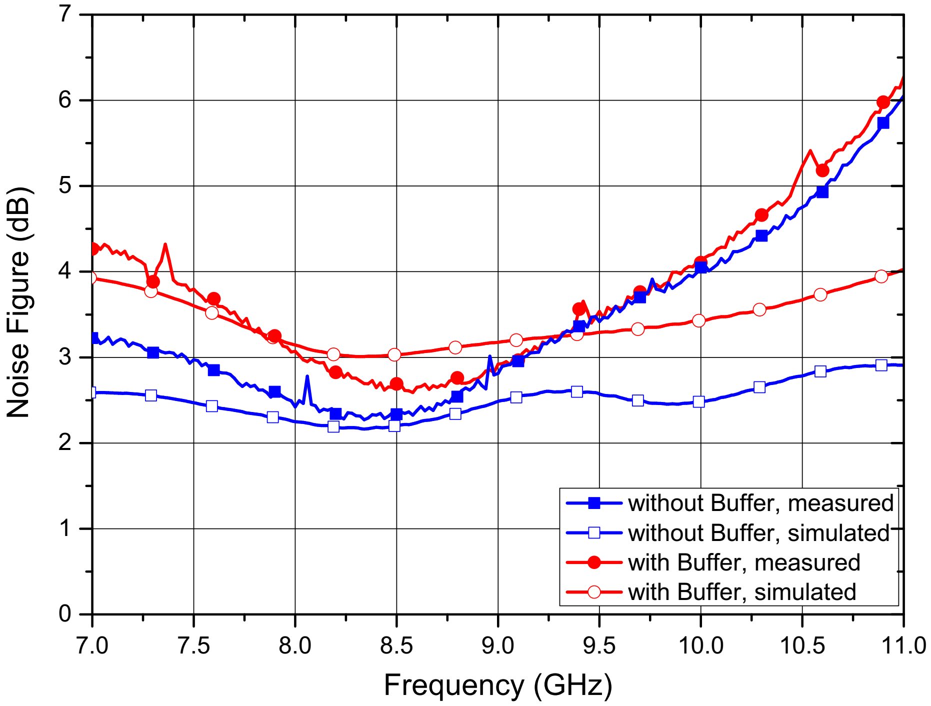
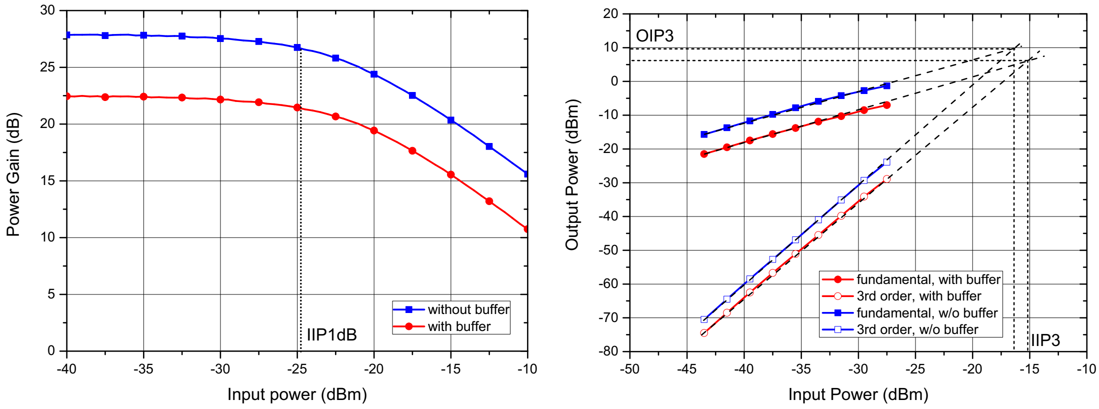


Figure 5.14: Measurement noise figure of the LNA

The minimum measured noise figure is 2.2 dB at 8.5 GHz without active buffer and 2.6 dB with working buffer. A mismatch between simulation and measurement results is comparable small. The issue with the noise figure measured without buffer is the fact that although the buffer is deactivated, its reference network contributes noise because it draws current from the LNA core voltage supply and can not be deactivated. That is clearly a mistake in the design concept and results in a higher noise figure for the LNA core, despite its high gain.

The large signal characterization in terms of 1-dB compression point IIP3 is shown in Fig. 5.15(a) and 5.15(b).



(a) (b)

Figure 5.15: Large signal characterization of the LNA, (a) – 1-dB compression point, (b) – third-order intermodulation

The input-referred 1-dB compression point, measured with and without buffer, is -25 dBm and -25.4 dBm, respectively. The limiting factor in the design is not the LNA or the buffer. The transistor size of Q_2, which is the phase inverter, was chosen too small. This is also afterwards confirmed by the simulation which stated an input 1-dB compression point -23.1 dBm for the LNA without buffer and -22.6 dBm with buffer. The specific linearity of the LNA was not of concern during the design phase because the design was focused on the implementation of the feedback. The input third-order intercept point was measured to -15.2 dBm with buffer and -16.2 dBm without buffer. The simulation results are nearly the same, -15 dBm with buffer and -15.7 dBm without buffer.

5.3 Mixer Integration

Although the design of mixers is not of scope in this thesis, it should be demonstrated in brief that the presented LNA topology is suitable to be integrated in a mixer design. The architecture of the mixer is a double-balanced I/Q mixer with local oscillator (LO) signal conditioning. The operating frequency range for the RF and LO input was predefined from 8.7 GHz to 10.7 GHz and the mixer should be supplied by a single voltage supply. The intermediate frequency range is specified from DC to 500 kHz. Additionally, the bias settings of the mixer, LNA buffer and intermediate frequency buffer should be externally adjustable. Similar to the design of the LNA, ESD protection circuits have to be used at the signal input/outputs and at the supply voltage rails. The general block diagram is depicted in Fig. 5.16.

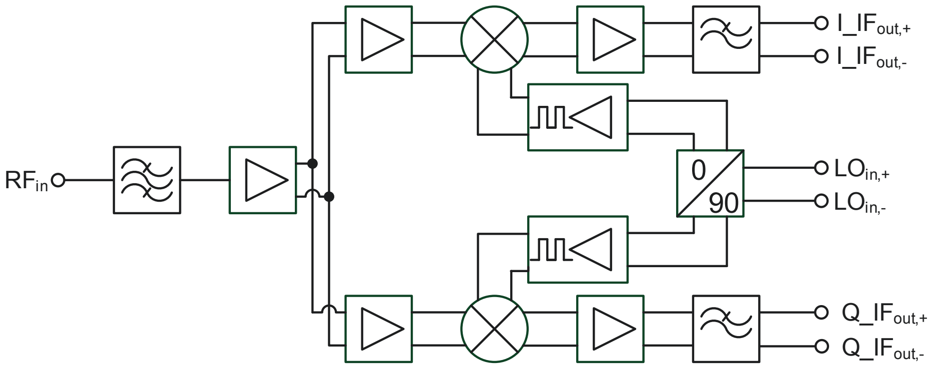


Figure 5.16: Block diagram of the down-converter

The input circuit of the down-converter is the LNA with a filter at its input, which is also used for impedance matching. The LNA core topology is almost identical to the previously presented one, except an additional feedback resistor is used to broaden the frequency response. The circuit diagram is shown in Fig. 5.17.

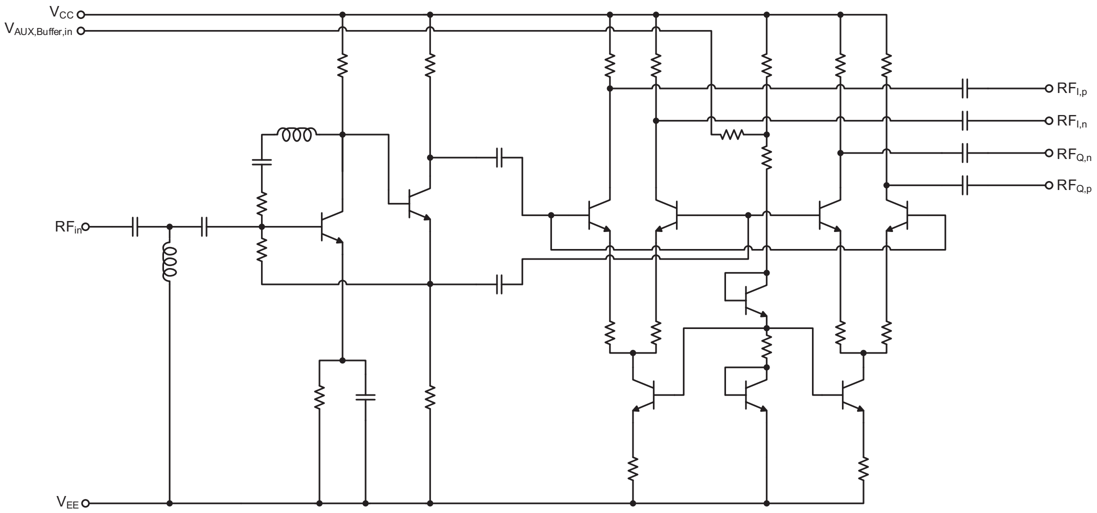


Figure 5.17: Schematic of the mixer input with input filter, LNA core and buffers

As the transistor size of the phase inverter in the previous design limited the linearity, the transistor was enlarged. Furthermore, instead of one buffer, two buffers are loading the phase inverter because the converted differential input signal is used twice in the I/Q mixer topology. The local oscillator signal conditioner (LOSC) splits the differential LO input signal in two quadrature differential signals by use of a third order polyphase quadrature filter (PPF). As the local oscillator signal is assumed to be sinusoidal, a three stage buffer converts the sinusoidal signal into a rectangular signal because the noise performance of the Gilbert cell mixer depends on the signal shape of the LO signal. A hard switching of multiplier stage will improve the noise performance. The circuit diagram of the LO conditioner is shown in Fig. 5.18. The three stage buffer is only shown for one mixer, the second mixer is fed by the same buffer topology.

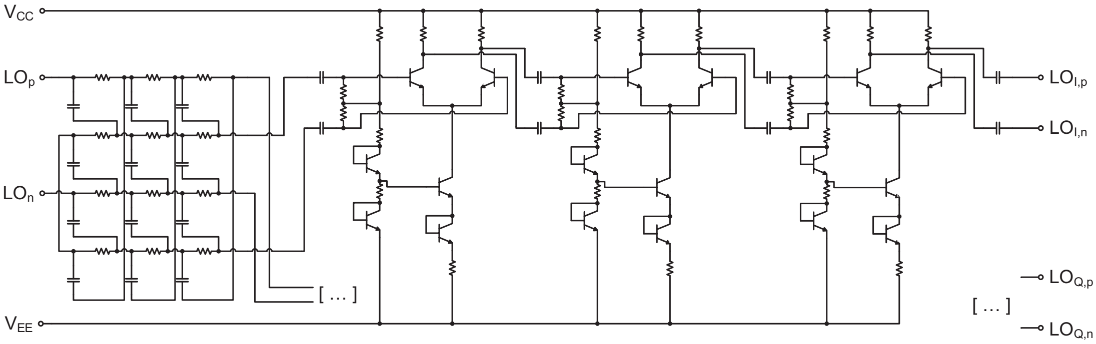


Figure 5.18: Schematic of the local oscillator signal conditioner

As previously mentioned, the mixer core is based on Gilbert cell mixer, with a gaining stage for the differential RF input signal at the bottom and a multiplier stage at the top which is controlled by the differential LO signal. The Fig. 5.19 depicts the schematic of the mixer core.

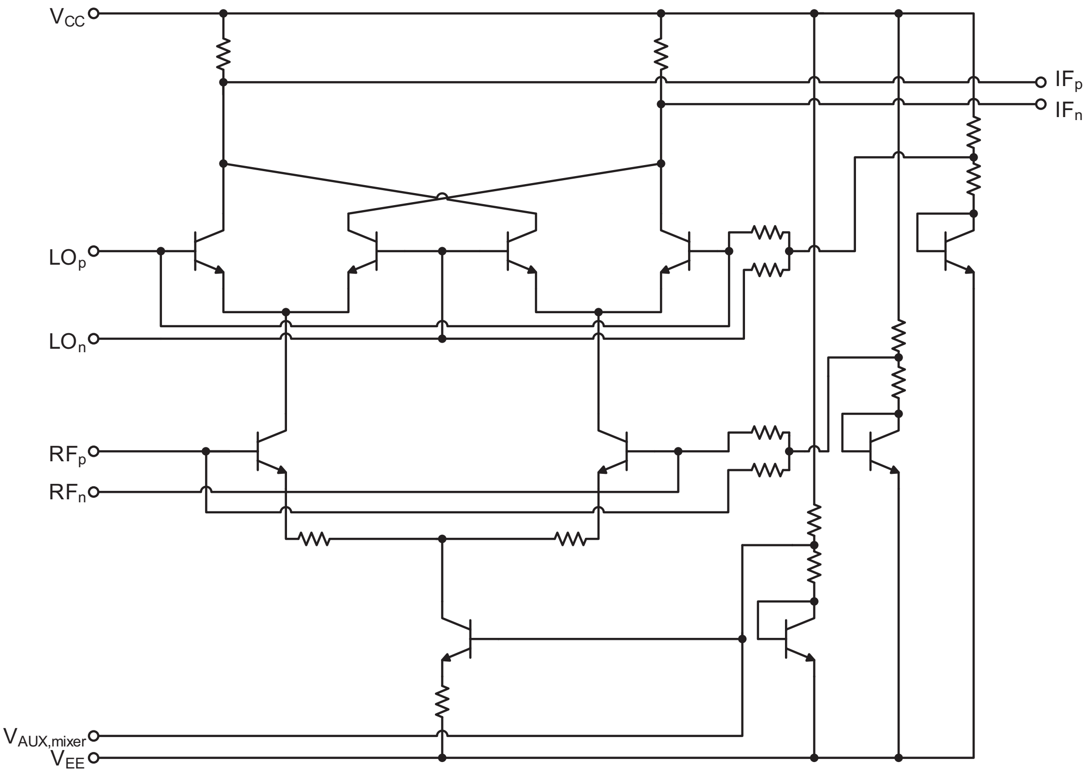


Figure 5.19: Schematic of the mixer core, based on a conventional Gilbert cell mixer

The last component in this design is the intermediate frequency differential output buffer which is also used as low-pass filter by large base capacitors. The schematic of the buffer is given in Fig. 5.20.

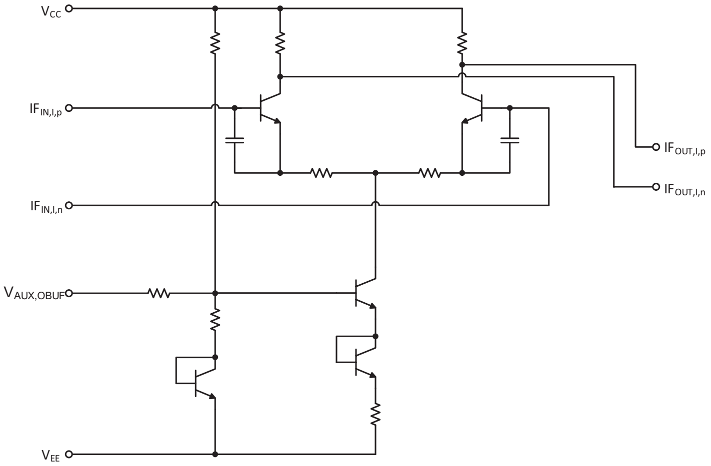


Figure 5.20: Schematic of the intermediate frequency output buffer

The full chip layout is depicted in Fig. 5.21. The size of the chip is 1.75 × 1.85 mm^2.

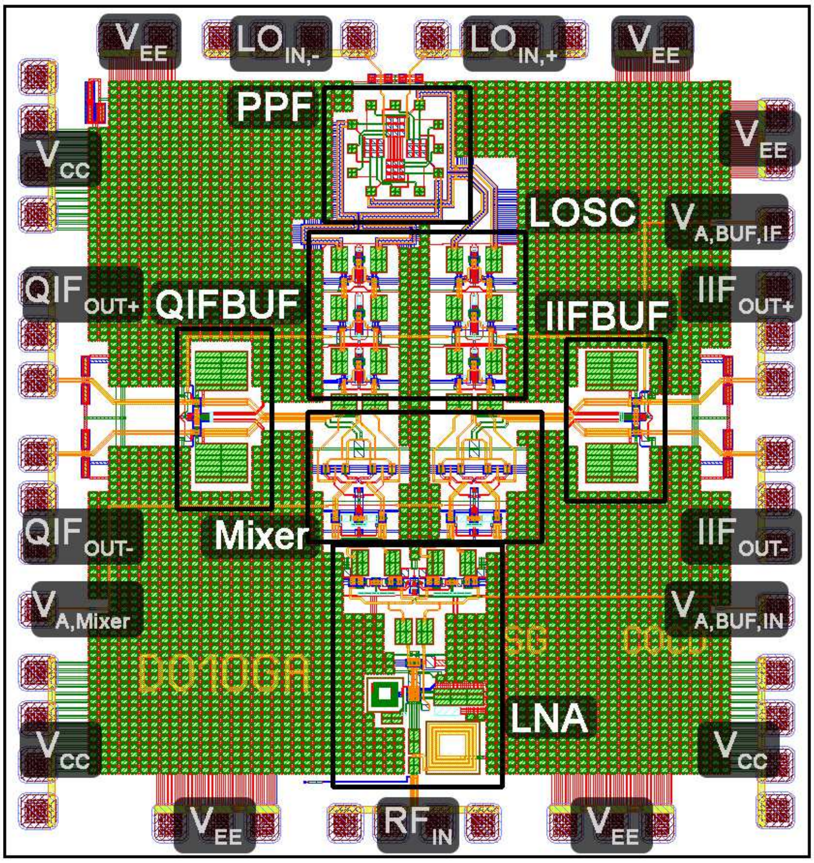
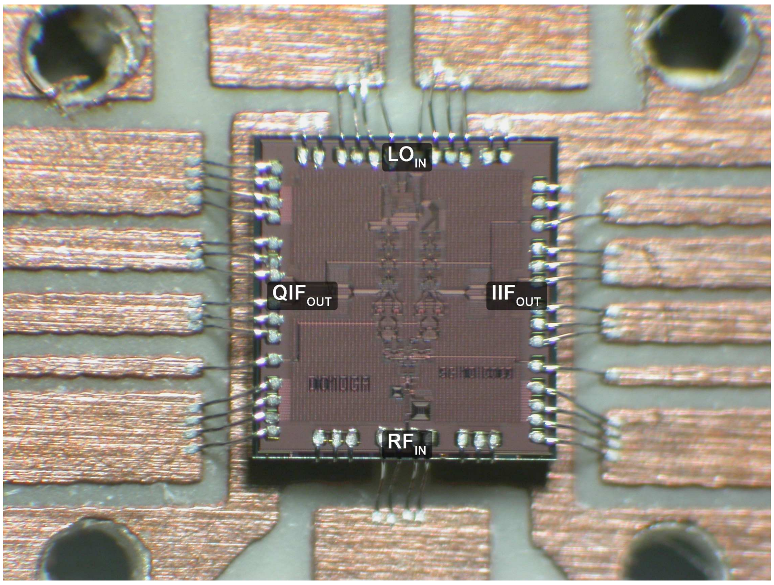


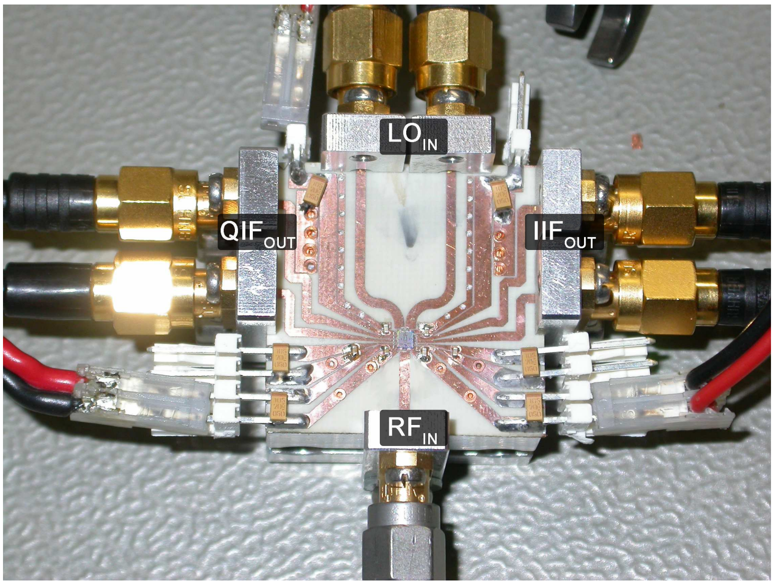
Figure 5.21: Schematic of the intermediate frequency output buffer

As in the case of the LNA, interconnection wirings are taken into account by electromagnetic simulations. Especially, the interconnections in the polyphase filter between stages and branches must be accurately modeled because a resulting phase shift from mismatches between the differential signals or between the quadrature signals will degrade the overall performance of the down-converter.

The bonded chip and the measurement PCB are shown in Fig. 5.22(a) and 5.22(a), respectively.



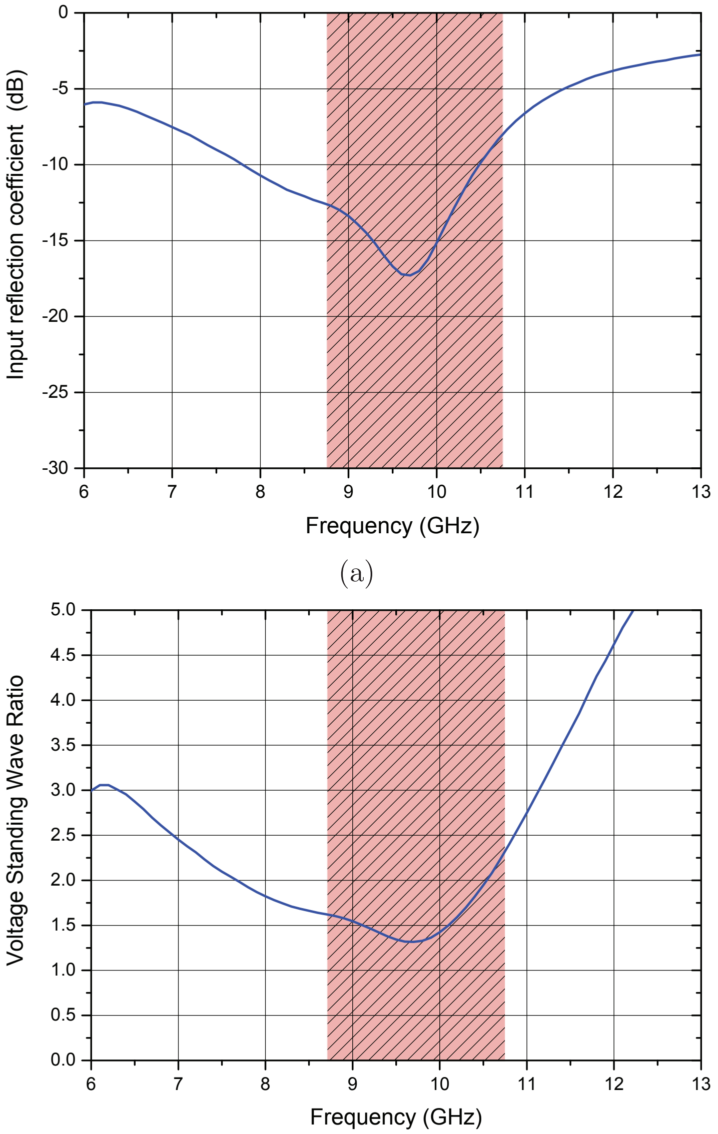
(a)



(b)

Figure 5.22: Measurement setup, (a) – bonded chip, (b) – measurement PCB

The down-converter was operated from a single supply voltage with an output voltage of 4.5 V. The power consumption was measured to be 675 mW. The measured input reflection coefficient and the voltage standing wave ratio are shown in Fig. 5.23.



(a)

(b)

Figure 5.23: Measured small-signal input characteristic with the shaded area as frequency range of interest, (a) – input reflection coefficient, (b) – voltage standing wave ratio

The input reflection coefficient demonstrates a good matching in the frequency range of interest. This circumstance is confirmed by the voltage standing wave ratio with a minimum value of 1:1.3 at 9.6 GHz, which is almost the center frequency of the down-converter. A measured transient intermediate frequency signal at 128 kHz is shown in Fig. 5.24. The LO frequency was set 9.7 GHz and the RF input frequency was therefore 9.699 872 GHz.

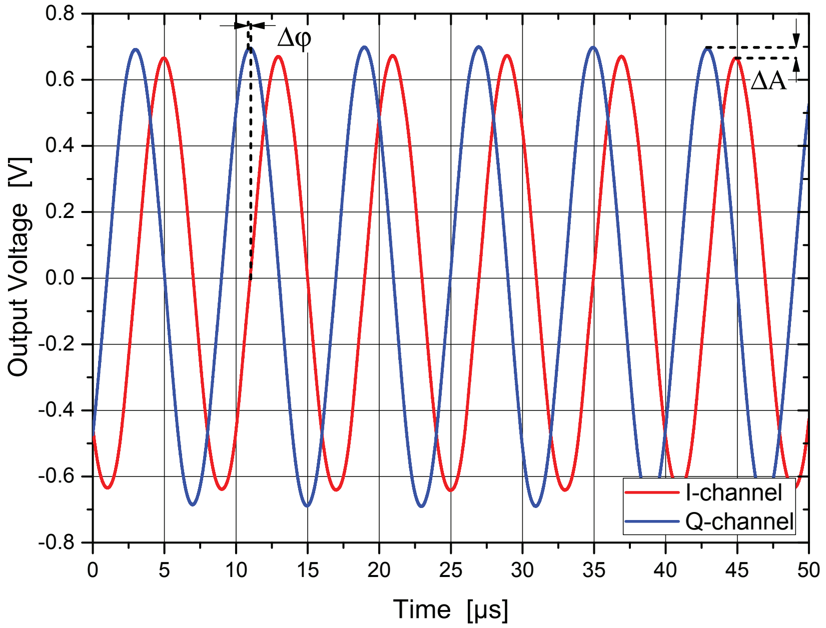


Figure 5.24: Transient IF signal at 128 kHz

The phase imbalance $\Delta\phi$ is 0.7° and the amplitude mismatch ΔA is 0.32 dB between the I- and Q-channel. As the input signal voltage level was 12.57 mV, the resulting voltage conversion gain was determined to approximately 35 dB. Further measurements of the down-converter were not possible due limited measurement capabilities. The noise figure was measured by Infineon and a minimum double sideband noise figure of 6.1 dB were reported.

Although the down-converter was not fully characterized, it is demonstrated in short that the proposed LNA topology with the extrinsic feedback is suitable for an implementation in mixer or down-converter designs.

Chapter 6

Conclusion and Outlook

Within this thesis silicon germanium technology based amplifiers are presented that utilize a passive frequency selective feedback. One major problem of SiGe amplifiers is their stability, as they tend to oscillate at lower gigahertz frequencies. Especially, power amplifiers with their large output stage are prone to oscillations. It is shown that this instability behavior results from inductive source or load impedance in conjunction with the intrinsic transistor feedback due to the base collector capacitance.

The introduction of an external base collector feedback, which is passive and frequency-selective, allows to stabilize the amplifiers. Although they are considered as conditionally stable, they exhibit no oscillation tendency under normal circuit operation. This stabilization method is already presented in the literature but not in conjunction with the second function of the introduced feedback, the neutralization of the transistor at working frequencies. Next to the instability issue of the intrinsic transistor feedback, the base collector capacitance also provides a negative feedback which is frequency dependent and deteriorates the transistor gain with increasing frequency. A second resonance of the external feedback with base collector capacitance neutralizes this negative feedback and prevent the transistor from a gain drop at working frequency.

Based on this knowledge, one low noise amplifier and three power amplifiers were realized in two SiGe technologies and the experimental results of these stable amplifiers are presented in this thesis:

- A 8.7 GHz narrow-band low noise amplifier incorporated in a 0.35 µm SiGe bipolar technology. The noise figure is 2.2 dB and the gain 28 dB at a supply voltage of 3 V [Gerlich 12]. The low noise amplifier was subsequently used for a design of a double-balanced I/Q mixer.
- Two packaged high efficient power amplifiers operating at the Ku-band. They are incorporated in a 0.35 µm SiGe bipolar technology. One amplifier uses a transformer-based output matching network and achieves 30.9 % of

power-added efficiency and 23.9 dBm of maximum output power at a supply voltage of 1.8 V. The second amplifier utilizes an LC-balun for impedance matching at the output and a power-added-efficiency of 38 % at 1.8 V is measured. The maximum output power was 23.4 dBm. [Gerlich 13].

- A power amplifier in a 0.35 µm SiGe bipolar technology that uses power combining techniques to achieve 30 dBm (1 W) and 30 % of power-added efficiency at 10 GHz and 2 V supply voltage.
- Two power amplifiers, incorporated in a 0.25 µm SiGe:C BiCMOS technology, demonstrating the capability of a non advanced SiGe process to be used for radio frequency power applications. Power combining techniques, the use of the passive frequency-selective feedback and layout optimization enables the realization of power amplifiers which exhibit an output power of 30 dBm and a power-added efficiency of 35 % at supply voltages lower as 2.6 V.

For the future, as long as III-V semiconductor technologies are not economically competitive to SiGe technologies, the research will be ongoing in the field of silicon germanium amplifiers. Even if the operating frequencies increases the base collector capacitance will still have its degrading influence on the transistor performance.

The external passive frequency-selective feedback was implemented in amplifiers that operate at X- and Ku-band frequencies. It would be advantageous to be able to use this feedback also at higher frequencies, as the performance degradation due to the intrinsic feedback is even more significant with increasing operating frequencies.

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