Modular Multilevel Converter with Thyristor DC-Link Switch for Full-Torque Variable-Speed Drives

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***Abstract*—The modular multilevel converter (MMC) is a promising topology for medium-voltage drive applications due to its high-quality output waveforms, low device switching frequency and voltage rating. However, the large cell capacitor voltage ripple is a severe challenge faced by MMC at low motor speeds. Recently, a hybrid MMC (HMMC) topology is proven to be a competitive solution because of its lower cell capacitor voltage ripple and no common-mode voltage (CMV) problem compared with other methods. However, the dc-link switch with IGBT limits HMMC to be applied for high-voltage applications. This paper uses the thyristor instead of IGBT as the dc-link switch. To ensure the thyristor can be softly turned on and safely turned off, a new control scheme is proposed. When using this proposed scheme, HMMC can also tolerate the failure of thyristor's turning-off without shutting down the system, improving the reliability effectively. The cell capacitor voltage ripple analysis is presented considering the effects of the thyristor switching process. In addition, a decoupled energy balancing control is utilized to suppress the fluctuation of dc current. Experimental results obtained from a 380 V/7.5 kW downscaled prototype validate the effectiveness of starting up a motor from the standby mode to rated speed with full-torque.**

***Index Terms*—Capacitor voltage ripple, dc/ac power conversion, dc-link switch, modular multilevel convert (MMC), thyristor, variable-speed drives.**

I. Introduction

Multilevel converters have been widely applied in drive applications, such as the modern electric ship medium-voltage direct current (MVDC) system, due to their features of high-quality output waveforms, low device switching frequency and voltage rating [1]-[4]. Among several multilevel converter candidates, the cascaded H-bridge (CHB) and the modular multilevel converter (MMC) are suitable for medium-voltage (MV) to high-voltage (HV) applications, since both of them can easily reach HV level by increasing the number of the cascaded cells. However, the CHB requires a multi-winding phase-shifting transformer to supply power for each cell independently. This transformer is complicated, bulky and costly. Differing from the CHB, MMCs not only don't need such phase-shifting transformers but also have the advantages of modularity and scalability.

Despite their salient features, the main issue of MMCs applied in variable-speed drives is that the cell capacitor voltage contains a fundamental frequency component which is proportional to the magnitude of output current and inversely proportional to the output frequency. This means the cell may suffer excessive ripples of the capacitor voltage in case of the low-speed and high-torque scenarios [5]. Large cell capacitance can be used to limit the capacitor voltage ripples, which in turn increases the cost and volume of the MMC.

One common approach to address this issue is to use the high-frequency components injection (HFCI), which injects high-frequency circulating current in each MMC arm while superposes the same frequency common-mode voltage (CMV) at the ac side of the MMC. In this case, the high-frequency power exchange is established to compensate the energy variations between the upper and lower arm cell capacitors, and therefore, reduces the capacitor voltage ripple [6]-[10]. However, the injected circulating current significantly increases the current stress in each arm, which results in high power losses and overrating risk of the devices. Apart from this, the injected CMV is harmful to the bearings and insulation of the motor [11].

To overcome the above drawbacks, some research has been carried out to improve the circuit design of MMCs. In [12]-[14], additional branches formed by cascaded cells are constructed. These branches provide extra paths for the high-frequency circulating current and CMV introduced by HFCI, which avoids the problems of high current stress and CMV. References [15] and [16] utilize dual active-bridge (DAB) converters to connect the capacitors of three cells from the three phases. Since the currents flowing through the cell capacitors are three-phase symmetrical, the cell capacitor voltage ripple is greatly reduced thanks to the DABs. By adding two switching devices in each cell, the MMC in [17] allows parallel connection within and across arms. Then, the energy variations of cell capacitors are canceled and therefore, effectively suppress the capacitor voltage ripple. In [18] and [19], two MMCs with full-bridge cells in back-to-back connection are proposed, which are able to damp the cell capacitor voltage ripple by decreasing the dc-link voltage. However, all the above modified MMCs involve additional components and consequently increase the cost and power losses.

A hybrid modular multilevel converter (HMMC) with a controllable switch at its dc-link has been proposed in [20],

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which inherently exhibits low cell capacitor voltage ripples without involving CMV nor increasing the arm current stress. However, the dc-link switch used in [20] is IGBT which has high conduction losses and low reliability. More importantly, in medium or higher voltage applications, IGBTs need to be connected in series to withstand the whole dc-link voltage (which is usually tens of kilovolts), which will face the challenges of static and dynamic voltage balancing techniques [21]. This will severely restrict the application of HMMC to higher voltage levels and power ratings.

This paper aims to use thyristor as the dc-link switch to enhance the HMMC. The advantages of thyristor include high efficiency, low cost, high reliability, ease of series connection, and strong anti-surge capability, etc. To ensure the thyristor can be softly turned on and completely turned off, this paper proposes a control scheme using sawtooth wave PWM. Moreover, the proposed scheme enables the HMMC to achieve a tolerant operation in case of a failure of turning off the thyristor, which effectively improves its reliability. The cell capacitor voltage ripple analysis is also conducted with the consideration of the thyristor switching process, which is more accurate compared to the conventional analysis approaches. In addition, a decoupled HMMC arm energy balancing control attempting to minimize the dc-link current stress is added to the proposed control scheme. Experimental results obtained from a 380V/7.5kW downscaled prototype validate the effectiveness of starting up a motor from the standby state to rated speed with full-torque.

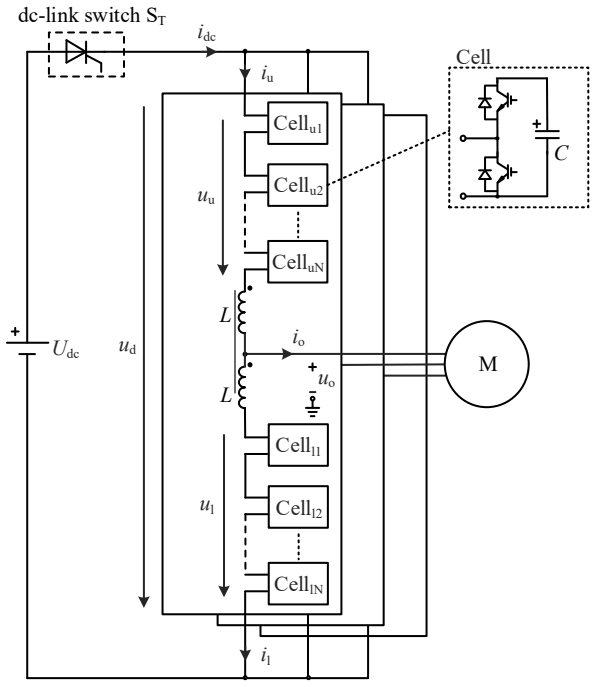

Fig. 1. Circuit configuration of HMMC with the thyristor dc-link switch.

II. Operation Principle of HMMC with Thyristor DC-Link Switch

A. Basics of HMMC

Fig. 1 illustrates the circuit configuration of HMMC which consists of a dc-link switch (thyristor) S_T and a three-phase MMC. Herein, the turn-off of S_T can be realized by controlling the voltage difference between the dc input voltage U_{dc} and HMMC's dc terminal voltage u_d. The MMC has N cascaded cells in each arm. Two arms (upper and lower) are connected in series in each phase via a coupled inductor. This configuration brings a smaller size and lighter weight than using two non-coupled inductors [22]. Each cell consists of a capacitor C and two IGBTs, which is the so-called "half-bridge cell".

Taking one phase as an example. The output voltage u_o and current i_o at MMC's ac terminal are expressed as follows:

$$u_o = U_{OM}\cos(\omega t), \tag{1}$$

$$i_o = I_{OM}\cos(\omega t - \varphi), \tag{2}$$

where U_{OM} and I_{OM} are the magnitudes of output voltage and current, ω is the output angular frequency, and φ is the phase lag angle. I_{OM} will be constant and rated of the motor stator current when the MMC drives a full-load-torque motor:

$$I_{OM} \equiv I_{OM(rated)}. \tag{3}$$

The upper and lower arm voltages (u_u and u_l) of HMMC are

$$\begin{cases} u_u = u_{com} - u_o + \dfrac{1}{2}\Delta u_{cc} \\ u_l = u_{com} + u_o + \dfrac{1}{2}\Delta u_{cc} \end{cases}, \tag{4}$$

where u_{com} is the dc component of the arm voltage, Δu_{cc} is the voltage for driving the dc-link current.

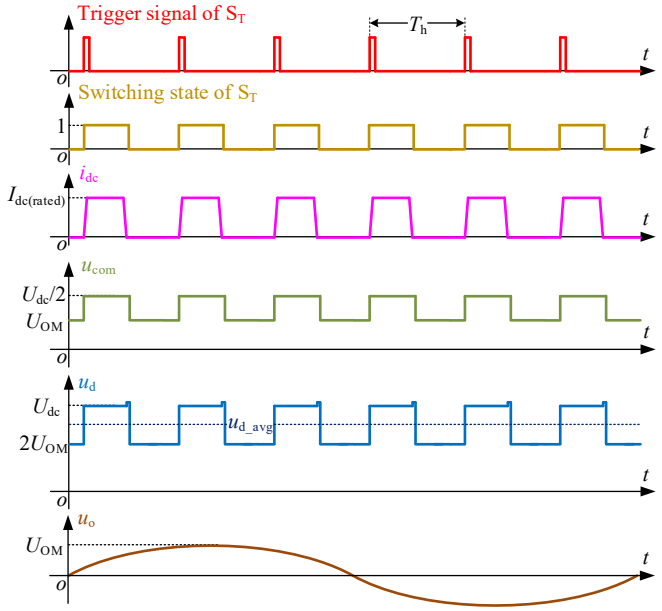

Fig. 2. Operating principle of HMMC.

The most distinctive feature of HMMC is that it can regulate the dc component of arm voltage according to the switching state of the dc-link switch, aiming to suppress the cell capacitor voltage ripple. As shown in Fig. 2, the dc-link switch S_T operates at the frequency of f_h ($f_h = 1/T_h$). When S_T is turned on ($S_T = 1$), u_{com} will equal to $U_{dc}/2$ in each arm. When S_T is turned off ($S_T = 0$), u_{com} will decrease to the required minimum voltage U_{OM} to drive the motor. In variable-speed motor drives, due to the constant Volt/Hertz ratio characteristics, U_{OM} will become

lower when ω decreases. As a result, the average dc terminal voltage u_{d_avg} of the HMMC will be significantly reduced at low speeds, which results in a small cell capacitor voltage ripple [20].

The dc current i_{dc} can be controlled into a trapezoidal wave with the help of the dc-link switch, as shown in Fig. 2. The magnitude of i_{dc} is constant and equals to the rated MMC dc current:

$$I_{dc} \equiv I_{dc(rated)} = \frac{3U_{OM(rated)} I_{OM} \cos\varphi_{rated}}{2U_{dc}}, \tag{5}$$

where $U_{OM(rated)}$ and φ_{rated} are output voltage magnitude and phase lag angle at rated motor speed. When HMMC drives the motor at different speeds, the duty cycle D_i of i_{dc} is adjustable to ensure the power balance between the dc input and ac output. D_i can be calculated as

$$D_i = \frac{3U_{OM} I_{OM} \cos\varphi}{2U_{dc} I_{dc(rated)}}. \tag{6}$$

The arm currents of HMMC are expressed as

$$\begin{cases} i_u = \frac{1}{3} i_{dc} + \frac{1}{2} i_o \\ i_l = \frac{1}{3} i_{dc} - \frac{1}{2} i_o \end{cases}. \tag{7}$$

According to (3) and (5), the magnitudes of i_o and i_{dc} are constant. Thus, the arm current stress of HMMC can remain constant within the whole speed range, which is of its rated value ($I_{dc(rated)}/3 + I_{OM(rated)}/2$). In contrast to HFCI methods, the lower current stress of HMMC benefits to select low rating devices.

B. Switching Process of Thyristor DC-Link Switch

Reliable turn-on and turn-off of the dc-link switch is of great importance to the stable operation of HMMC. Fig. 3 illustrates the turn-off processes of the dc-link switch of IGBT and thyristor using the control scheme in [20]. For the case of IGBT in Fig. 3(a), the dc current i_{dc} has been controlled to almost zero before the dc component of arm voltage u_{com} decreases (at t_0). Since IGBT is a fully controllable semiconductor device, it is able to cut off the residual i_{dc} and then u_{com} will decrease to U_{OM}. In contrast, the thyristor cannot cut off the current. Therefore, the thyristor cannot be turned off at t_0 even if i_{dc} has been quite small, as shown in Fig. 3(b). If u_{com} decreases to U_{OM} after t_0, a huge voltage (U_{dc}-2U_{OM}) will be immediately applied to the coupled inductor of each phase, which will lead to the overrating of i_{dc}. The rising rate of i_{dc} can be derived as

$$\frac{di_{dc}}{dt} = \frac{3U_{dc} - 6U_{OM}}{2L}. \tag{8}$$

Therefore, the conventional control method of IGBT in [20] will no longer apply to the case of using thyristor. To ensure the thyristor can be completely turned off, this section will further analyze its switching process.

Fig. 4 shows the equivalent circuit of the HMMC's dc-side circuit when the thyristor S_T is turned on. According to Kirchhoff's voltage law, it has

$$\Delta u_{cc} = -\frac{2}{3} L \frac{di_{dc}}{dt}, \tag{9}$$

in which $2L/3$ is the equivalent dc inductance of the HMMC. It is observed that Δu_{cc} can be used to drive the dc current and therefore, to turn off S_T.

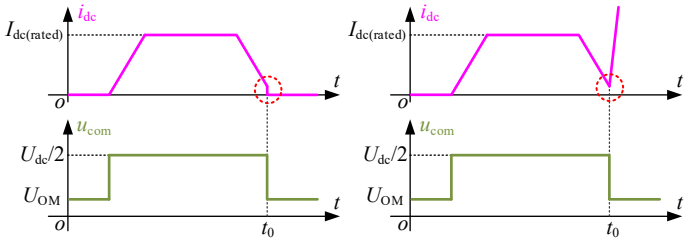

Fig. 3. Turn-off processes of the HMMC dc-link switch by applying the control method in [20]. (a) IGBT dc-link switch; (b) thyristor dc-link switch.

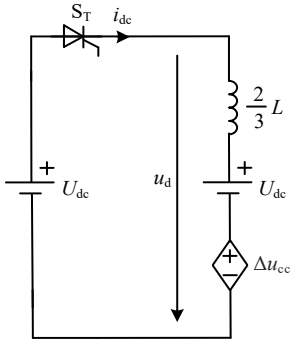

Fig. 4. Equivalent circuit of the dc-side circuit.

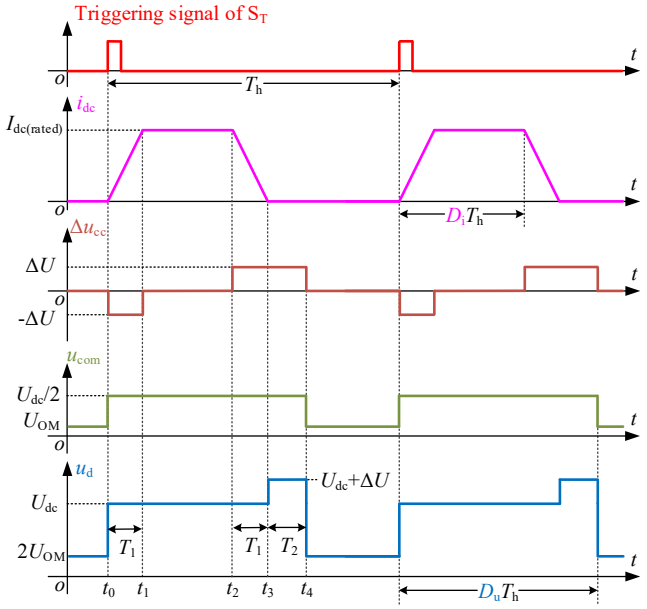

Fig. 5. Schematic waveforms of the thyristor switching process.

Fig. 5 gives the switching process of S_T. u_d starts to increase to U_{dc} and S_T is turned on under zero voltage when S_T is triggered at t_0. Then, Δu_{cc} steps from zero to negative with a magnitude of ΔU. Therefore, a voltage $+\Delta U$ with an opposite polarity to Δu_{cc} is generated across the equivalent dc inductor. This voltage makes i_{dc} increase linearly. Δu_{cc} steps to zero and then i_{dc} remains constant once i_{dc} reaches its rated value $I_{dc(rated)}$ at t_1. Before S_T is turned off at t_2, Δu_{cc} steps from zero to ΔU. Similarly, a negative voltage -ΔU can be generated across to the equivalent dc inductor making i_{dc} decrease linearly. Once i_{dc} becomes zero at t_3, Δu_{cc} will be maintained for a period (T_2).

This makes u_d slightly higher than U_{dc} and therefore, ensures S_T can be turned off completely. Then u_d decreases to $2U_{OM}$. T_2 is mainly determined by the circuit commutated turn-off time of the thyristor, which is usually around 200μs to 430μs according to the technical manual provided by the manufacturer. Based on (9), the rising or falling time $T_1$of dc current can be derived

$$T_1 = \frac{2LI_{dc(rated)}}{3\Delta U}. \tag{10}$$

It is worth to note that, due to the periods of T_1 and T_2, there is a difference between the duty cycle D_i of i_{dc} and the duty cycle D_u of u_d, as shown in Fig. 4. D_i and D_u satisfy the following relationship:

$$D_u = D_i + \frac{T_1 + T_2}{T_h}. \tag{11}$$

C. Switching Frequency and Voltage Requirements of Thyristor DC-Link Switch

Switching frequency of the thyristor affects the operating performance of HMMC. There are mainly two considerations limiting the switching frequency of thyristors: 1) rate of rise of on-sate current during turn-on (di/dt_{crit}, which is usually several hundred A/μs); 2) turn-off time (which is usually around 200μs to 430μs as mentioned before). Therefore 300Hz switching is usually feasible for the thyristors. Considering a certain margin, here the authors limit the switching frequency of thyristor as 250Hz. In order to achieve satisfactory waveforms, switching frequency of the dc-link switch is usually set as 8~10 times the output ac frequency of HMMC. Hence switching of the thyristors can be effective when the output ac frequency is below 25Hz. While for higher output frequency, the capacitor voltage ripple itself is already small and the thyristor can be constantly turned on to operate HMMC as a traditional MMC (which will be verified by experiment results in Section V).

On the other hand, to meet the medium and high voltage requirements, the thyristors need series connection, which calls for the technology of static and dynamic voltage equalization. This technology is very mature in practice and has been widely used, such as Thyristor switched capacitor (TSC) application [23]. Based on the above considerations, the authors think the thyristor is a competitive solution to dc-link switch of HMMC, as it is very robust and cost effective.

III. Analysis of Cell Capacitor Voltage Ripple

As aforementioned, the turn-off duration of the thyristor leads to a difference between D_i and D_u. However, this difference is ignored in [20], which leads to the inaccurate calculation of cell capacitor voltage ripple. In this section, the analysis of cell capacitor voltage considering this difference is presented. Neglecting the voltage drops on the coupled inductor, the insertion indexes of the upper and lower arms can be expressed as

$$\begin{cases} n_u = u_u/U_{dc} \approx (u_{com} - u_o)/U_{dc} \\ n_l = u_l/U_{dc} \approx (u_{com} + u_o)/U_{dc} \end{cases}. \tag{12}$$

The current flowing through the capacitor of each cell can be obtained

$$\begin{cases} i_{Cu} = n_u i_u = \dfrac{1}{U_{dc}}\left(\dfrac{1}{3}u_{com}i_{dc} - \dfrac{1}{2}u_o i_o - \dfrac{1}{3}u_o i_{dc} + \dfrac{1}{2}u_{com}i_o\right) \\ i_{Cl} = n_l i_l = \dfrac{1}{U_{dc}}\left(\dfrac{1}{3}u_{com}i_{dc} - \dfrac{1}{2}u_o i_o + \dfrac{1}{3}u_o i_{dc} - \dfrac{1}{2}u_{com}i_o\right) \end{cases}. \tag{13}$$

Considering that both u_{com} and i_{dc} are almost square waves, the following switching functions are adopted to describe them:

$$i_{dc} = I_{dc(rated)} s_i(t), \tag{14}$$

$$u_{com} = 0.5U_{dc}s_u(t) + (U_{OM} + \delta)[1 - s_u(t)], \tag{15}$$

where $s_i(t)$ and $s_u(t)$ are switching functions with different duty cycles:

$$s_i(t) = \begin{cases} 1, & 0 \le t < D_i T_h \\ 0, & D_i T_h \le t < T_h \end{cases}, \tag{16}$$

$$s_u(t) = \begin{cases} 1, & 0 \le t < D_u T_h \\ 0, & D_u T_h \le t < T_h \end{cases}. \tag{17}$$

It can be seen from (15) that u_{com} will be higher than U_{OM} with a margin voltage δ when S_T is turned off ($s_u(t) = 0$). This voltage can be used to accommodate transient processes such as acceleration of the motor speed or sudden change of the load torque.

Taking the cell of the upper arm as an example. i_{Cu} can be further calculated by adding (14) and (15) into (13). Thus,

$$\begin{aligned} i_{Cu} = {} & \frac{1}{6}I_{dc(rated)}s_i(t) - \frac{U_{OM}I_{OM}}{4U_{dc}} \\ & - \frac{U_{OM}I_{OM}}{4U_{dc}}\cos(2\omega t - \varphi) - \frac{U_{OM}I_{dc(rated)}s_i(t)}{3U_{dc}}\cos(\omega t) \\ & + \frac{I_{OM}}{4}\left\{s_u(t) + \frac{2(U_{OM} + \delta)}{U_{dc}}[1 - s_u(t)]\right\}\cos(\omega t - \varphi). \end{aligned} \tag{18}$$

As the frequencies of $s_i(t)$ and $s_u(t)$ are much higher than HMMC's output frequency (generally f_h is at least ten times higher than f, where f=ω/(2π)). In steady-state, it is reasonable to approximate $s_i(t)$ and $s_u(t)$ based on their average values D_i and D_u. Therefore, based on (6), (18) becomes

$$\begin{aligned} i_{Cu} = {} & -\frac{U_{OM}I_{OM}}{4U_{dc}}\cos(2\omega t - \varphi) - \frac{U_{OM}^2 I_{OM}\cos\varphi}{2U_{dc}^2}\cos(\omega t) \\ & + \frac{I_{OM}}{4}\left[D_u + \frac{2(U_{OM} + \delta)}{U_{dc}}(1 - D_u)\right]\cos(\omega t - \varphi). \end{aligned} \tag{19}$$

The cell capacitor voltage ripple of the upper arm can be obtained by integration of i_{Cu}, which is

$$\begin{aligned} \Delta u_{Cu} = {} & -\frac{U_{OM}I_{OM}}{8U_{dc}\omega C}\sin(2\omega t - \varphi) - \frac{U_{OM}^2 I_{OM}\cos\varphi}{2U_{dc}^2\omega C}\sin(\omega t) \\ & + \frac{I_{OM}}{4\omega C}\left[D_u + \frac{2(U_{OM} + \delta)}{U_{dc}}(1 - D_u)\right]\sin(\omega t - \varphi) \end{aligned}, \tag{20}$$

where C is the cell capacitance.

The cell capacitor voltage ripple of the lower arm can be calculated in the same way:

$$\begin{aligned} \Delta u_{Cl} = {} & -\frac{U_{OM}I_{OM}}{8U_{dc}\omega C}\sin(2\omega t - \varphi) + \frac{U_{OM}^2 I_{OM}\cos\varphi}{2U_{dc}^2\omega C}\sin(\omega t) \\ & - \frac{I_{OM}}{4\omega C}\left[D_u + \frac{2(U_{OM} + \delta)}{U_{dc}}(1 - D_u)\right]\sin(\omega t - \varphi). \end{aligned} \tag{21}$$

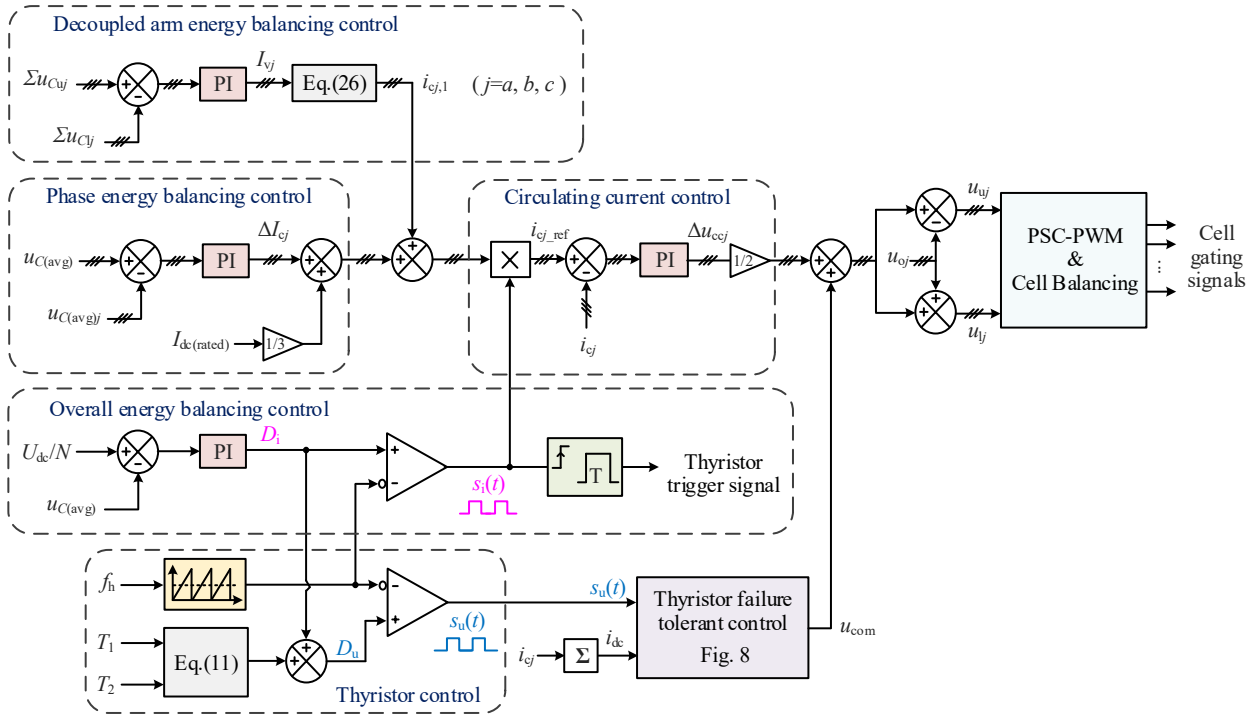

Fig. 6. Proposed control scheme for HMMC with the thyristor dc-link switch.

In (20) and (21), U_{dc}, I_{OM}, and C are constant for full-torque variable-speed drives. Because of the constant Volt/Hertz ratio characteristics of the motor, when ω decreases, U_{OM}/ω will be constant while U_{OM}^2/ω will decrease. Hence, when the motor speed decreases:

1) the first term of (20) and (21) will remain constant;
2) the second term of (20) and (21) will decrease.

Therefore, the first and second terms can be neglected at low speeds. As for the third term, its magnitude will be further affected by δ and D_u. When HMMC works in a steady state, the motor speed and load torque will remain constant. Thus, the voltage δ for accommodating transient processes can be ignored. D_u is the sum of D_i and $(T_1+T_2)/T_h$, as shown in (11). If the motor speed is low, the required power from HMMC's dc input will be small, making D_i close to zero. Moreover, $(T_1+T_2)/T_h$ decreases when the speed decreases. T_h is proportional to ω. (T_1+T_2) is constant. Thus, D_u will be very small at low speed. Based on the above analysis, the third term of (20) and (21) can be approximated as (22) at very low motor speed, by ignoring δ and D_u:

$$\frac{I_{OM}}{4\omega C}\left[D_u+\frac{2(U_{OM}+\delta)}{U_{dc}}(1-D_u)\right]\sin(\omega t-\varphi) \approx \frac{I_{OM}U_{OM}}{2\omega C U_{dc}}\sin(\omega t-\varphi)\,. \quad (22)$$

Due to the constant U_{OM}/ω, the magnitude of the third term will be limited during the low motor speeds. Therefore, the cell capacitor voltage ripple can be well suppressed by HMMC. Similarly, when the motor speed is high, the third term of (20) and (21) can be approximated as (23) by ignoring δ and replacing D_u with 1:

$$\frac{I_{OM}}{4\omega C}\left[D_u+\frac{2(U_{OM}+\delta)}{U_{dc}}(1-D_u)\right]\sin(\omega t-\varphi) \approx \frac{I_{OM}}{4\omega C}\sin(\omega t-\varphi)\,. \quad (23)$$

It shows that the voltage ripple will decrease with the rise of ω. Therefore, when the motor speed is higher, the converter will no longer suffer voltage ripple. HMMC can be switched to the conventional MMC operation mode with the constant on-state thyristor. Compared with IGBT, the thyristor performs much better in affecting the converter efficiency thanks to its lower conduction losses.

IV. Proposed Control Scheme of HMMC with Thyristor DC-Link Switch

This section proposes the control scheme of HMMC with thyristor dc-link switch. Fig. 6 shows an overview of the control scheme. It contains overall energy balancing control, thyristor control, phase energy balancing control, circulating current control and decoupled arm energy balancing control.

A. The Overall and Phase Energy Balancing Control

The overall energy balancing control aims to balance the power between the HMMC dc input and ac output. This control regulates the measured average voltage $u_{C(avg)}$ of all cell capacitors to follow the reference U_{dc}/N, which is achieved by adjusting D_i.

The phase energy balancing control is used to equalize the energy distribution of three phases. This control regulates the average cell capacitor voltage $u_{C(avg)j}$ in phase j (j = a, b, c) to follow $u_{C(avg)j}$ through adding a dc current adjusting component ΔI_{cj} into the circulating current [7].

B. The Thyristor Control

In the thyristor control, the durations T_1 and T_2 are used to produce the reference of D_u. Then a sawtooth wave PWM is utilized, as shown in Fig. 7. D_i and D_u are compared with the same sawtooth wave to generate $s_i(t)$ and $s_u(t)$. Then the thyristor is triggered at every rising edge of $s_i(t)$. $s_u(t)$ is used to generate the dc component of arm voltage u_{com} base on (15). It is noted that in practical applications, some non-ideal factors, such as voltage fluctuation of dc source and noise interference in the controller, may affect the normal turn-off of the dc-link thyristor and cause the problem of overcurrent like that in Fig. 3(b). Hence, a failure tolerant control is proposed to ensure HMMC can still work even if the thyristor fails to be turned off. The flow chart of the failure tolerant control is shown in Fig. 8. Every time when $s_u(t)$ is equal to zero, which means the thyristor should be turned off and u_{com} should be decreased, the measured dc current i_{dc} will be compared with a threshold current I_{pro}. If $i_{dc} > I_{pro}$, which indicates the thyristor has failed to turn off and i_{dc} is rising rapidly, u_{com} is ordered to increase to $U_{dc}/2$. Otherwise, u_{com} will be calculated by (15).

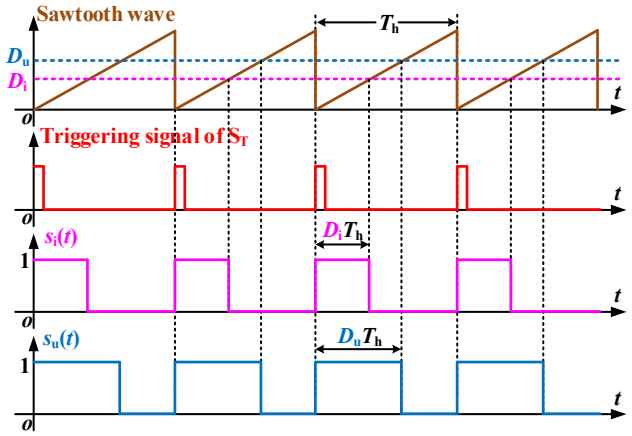

Fig. 7. Sawtooth wave PWM for the thyristor control.

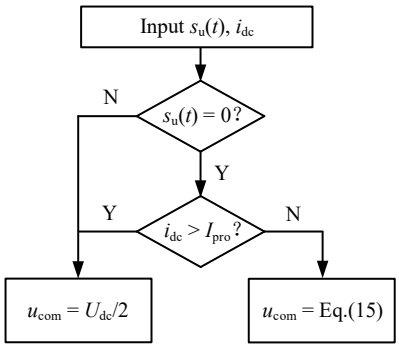

Fig. 8. Failure tolerant control in the proposed control scheme.

C. The Circulating Current Control

Subsequently, the current references produced by overall and phase energy balancing controls are sent to circulating current control to generate the reference i_{cj_ref} of each phase, where $i_{cj\_ref} = s_i(t)(I_{dc(rated)}/3 + \Delta I_{cj})$. A PI controller is used to force the measured circulating current i_{cj} to follow i_{cj_ref} by generating a voltage of Δu_{ccj} in each phase.

Finally, the references of arm voltages u_{uj} and u_{lj} are obtained according to (4) and are sent to the phase-shift carrier PWM (PSC-PWM) to generate cell gating signals. In addition, a cell energy balancing control [22] is adopted to balance the cell capacitor voltages within each arm.

D. The Decoupled Arm Energy Balancing Control

Additionally, to ensure the energy of each phase is evenly distributed in the upper and lower arms, an arm energy balancing control is needed. The conventional method is to add a fundamental-frequency component $i_{cj,1}$ into the circulating current of each phase [20]. Then $i_{cj\_ref} = s_i(t)(I_{dc(rated)}/3 + \Delta I_{cj} + i_{cj,1})$. The reference of $i_{cj,1}$ is

$$\begin{cases} i_{ca,1} = I_{Va}\cos(\omega t) \\ i_{cb,1} = I_{Vb}\cos(\omega t - 2\pi/3) \\ i_{cc,1} = I_{Vc}\cos(\omega t + 2\pi/3) \end{cases}. \tag{24}$$

However, the energy differences between the upper and lower arms in the three phases are different because the three-phase circuit parameters cannot be completely the same. This means $I_{Va} \neq I_{Vb} \neq I_{Vc}$, which leads to

$$\sum_{j=a,b,c} i_{cj,1} \neq 0. \tag{25}$$

Equations (24) and (25) show that there will be a fundamental frequency current on the dc-link, which increases the current stress of the dc-link switch.

To deal with this problem, a decoupled arm energy balancing control is adopted. As shown in Fig. 6, the reference of $i_{cj,1}$ is improved to

$$\begin{bmatrix} i_{ca,1} \\ i_{cb,1} \\ i_{cc,1} \end{bmatrix} = \frac{\sqrt{3}}{3} \begin{bmatrix} \sqrt{3}\cos(\omega t) & -\sin(\omega t) & \sin(\omega t) \\ \sin(\omega t - 2\pi/3) & \sqrt{3}\cos(\omega t - 2\pi/3) & -\sin(\omega t - 2\pi/3) \\ -\sin(\omega t + 2\pi/3) & \sin(\omega t + 2\pi/3) & \sqrt{3}\cos(\omega t + 2\pi/3) \end{bmatrix} \begin{bmatrix} I_{Va} \\ I_{Vb} \\ I_{Vc} \end{bmatrix}. \tag{26}$$

where I_{Vj} is adjusted by a PI controller, aiming to control the average cell capacitor voltage of the upper arm Σu_{Cuj} to follow that of the lower arm Σu_{Clj}. (26) has two characteristics: first, the sum of $i_{cj,1}$ is always equal to zero, which is

$$\sum_{j=a,b,c} i_{cj,1} \equiv 0. \tag{27}$$

Therefore, the fundamental frequency current on the dc-link is eliminated. Second, I_{Vj} of one phase does not affect the arm energy balancing of the other two phases. For example, I_{Va}, which is the output of the PI controller of phase a, is used to produce a fundamental frequency current $I_{Va}\cos(\omega t)$ in $i_{ca,1}$. This current is in phase with the output voltage u_{oa} (where $u_{oa} = U_{OM}\cos(\omega t)$) and draws active power to balance the arm energy of phase a. At the same time, I_{Va} also produces a fundamental frequency current $(I_{Va}/\sqrt{3})\sin(\omega t - 2\pi/3)$ in $i_{cb,1}$. Since this current is orthogonal to u_{ob} (where $u_{ob} = U_{OM}\cos(\omega t - 2\pi/3)$), no active power will be generated among the arms of phase b. Thus, I_{Va} will not affect the arm energy balancing of phases b and c.

Especially, when HMMC needs to switch to conventional MMC operation mode at a high speed, the control scheme is the same as that in Fig. 6 except for the following cases:

1) The reference of i_{cj_ref} switches to $D_iI_{dc(rated)}/3 + \Delta I_{cj} + i_{cj,1}$;
2) The reference of u_{com} switches to $U_{dc}/2$;
3) The thyristor S_T is always triggered and turned on constantly.

V. Experimental Results

A. Experimental Setup

The experimental validation of the aforementioned topology and control methods is performed on a 380 V/7.5 kW scaled-down HMMC motor drive platform as shown in Fig. 9. There are two induction motors (IMs) (Siemens 1LE0001-1CB23-3AA4) connected together by bearings. One is driven by the HMMC. The other is driven by a four-quadrant drive (ABB ASC800-11-0016-3) to simulate a constant torque load. A dc power supply (Chroma 62150H-1000) is used to provide 750 V for the dc source of HMMC. An Infineon-TT120N16SOF thyristor is selected as the dc-link switch S_T with a circuit commutated turn-off time of 0.2 ms. There are 3 cells in each arm of HMMC. The switching frequency of each cell is 3kHz, which ensures satisfactory MMC operation waveforms with the equivalent switching frequency equal to 9kHz. The rated cell capacitor voltage is 250 V. The rated dc current $I_{dc(rated)}$ is 10A. The maximum voltage used for circulating current control is ±10% of the dc source voltage (ΔU=75 V). The switching frequency of S_T is ten times of the HMMC output frequency. Table I gives the parameters of the experimental platform.

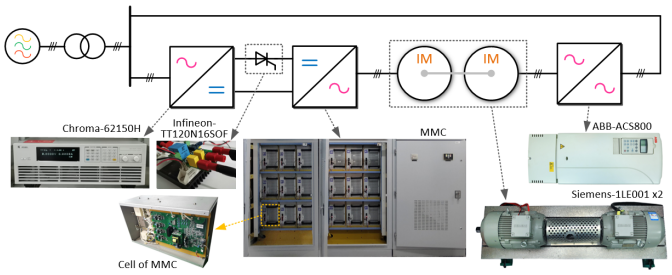

Fig. 9. View of the experimental HMMC motor drive platform.

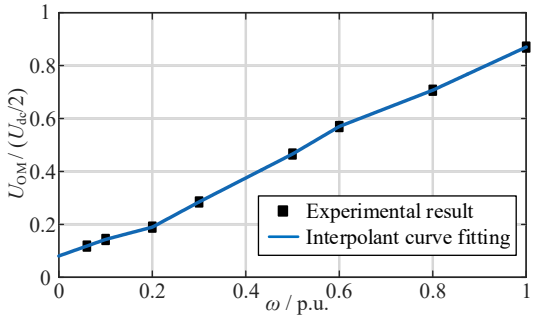

Fig. 10. Experimental results of IM stator voltage U_{OM} under full-torque within the whole speed range.

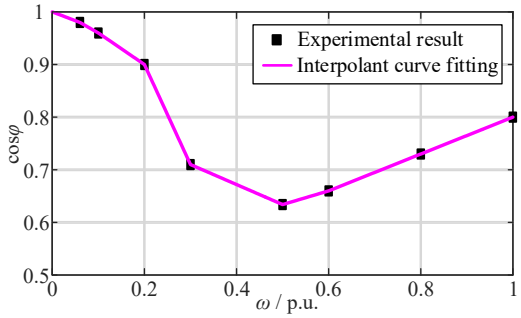

Fig. 11. Experimental results of IM power factor cosφ under full-torque within the whole speed range.

Table II shows the parameters of the IMs. With the full torque of 49 Nm, the magnitude of IM stator current is constant within the whole speed range and is of 22A in each phase. Considering the motor will experience some special characteristics when it runs at low speeds, such as nonlinear Volt/Hertz ratio characteristics and variation of power factor. Figs. 10 and 11 show the IM stator voltage U_{OM} and power factor cosφ within the whole speed range. Then, the cell capacitor voltage ripple of the experimental results can be estimated by (19) and (20).

TABLE I
EXPERIMENTAL PARAMETERS OF HMMC

Number of cells per arm	N=3
dc source voltage	U_{dc}=750V
Voltage for circulating current control	ΔU=75V(=10%U_{dc})
Margin voltage	δ=56V(=7.5%U_{dc})
SM capacitance	C=1.86mF
Arm inductance	L=6mH
Rated output frequency	f_{rated}=50Hz
Rated phase current magnitude	$I_{OM(rated)}$=22A
Rated dc current	$I_{dc(rated)}$=10A
S_T switching frequency	f_h=10×f

TABLE II
EXPERIMENTAL PARAMETERS OF IM

Rated power	S=7.5kw
Number of poles	pp=2
Rated speed	n_r=1460rpm
Stator line-line rated rms voltage	U_l=380V
Stator line-line rated rms current	I_l=15.7A
Rated torque	T_L=49Nm

B. Steady-state Performance

To verify the steady-state performance of HMMC with the thyristor at low frequencies and full torque. Fig. 12 illustrates the experimental results at 3Hz, 10Hz and 25Hz. When running at a very low frequency of 3Hz, as shown in Fig. 12(a), HMMC can smoothly output the full load current i_{oa} with magnitude of 22 A. The dc current i_{dc} is controlled into a trapezoidal wave with its magnitude approximately equal to the rated value 10 A. The peak-to-peak value of cell capacitor voltage (u_{Cua} or u_{Cla}) is 145 V, which is almost consistent with the estimated value 143 V. When the output frequency increases in Figs. 12(b) and (c), the magnitudes of i_{dc} and i_{oa} still remain unchanged. The duty cycle of i_{dc} increases with the rise of the output frequency to produce enough active power for ac output. The peak-to-peak value of the cell capacitor voltage decreases to 58 V at 10 Hz in Fig. 12(b) and 32 V at 25 Hz in Fig. 10(c), which agrees with the estimated value (57 V at 10 Hz and 34 V at 25 Hz). Therefore, the proposed cell capacitor voltage ripple analysis can effectively estimate the ripple.

Fig. 13 shows the waveforms of HMMC with thyristor at high frequencies (30 Hz, 40 Hz and 50 Hz) and full torque. During the high-frequency region [25 Hz, 50 Hz], the thyristor S_T is constantly on and HMMC switches into the conventional MMC operation mode. The cell capacitor voltage ripple decreases when the output frequency rises. In Fig. 13(c), HMMC reaches rated operating conditions and the dc current i_{dc} increases to the rated value 10 A.

To examine the switching process of thyristor, Fig. 14 further gives the zoomed-in waveforms of i_{dc} and dc terminal voltage u_d at 10 Hz from Fig. 10(b). Before S_T is turned on, u_d steps to

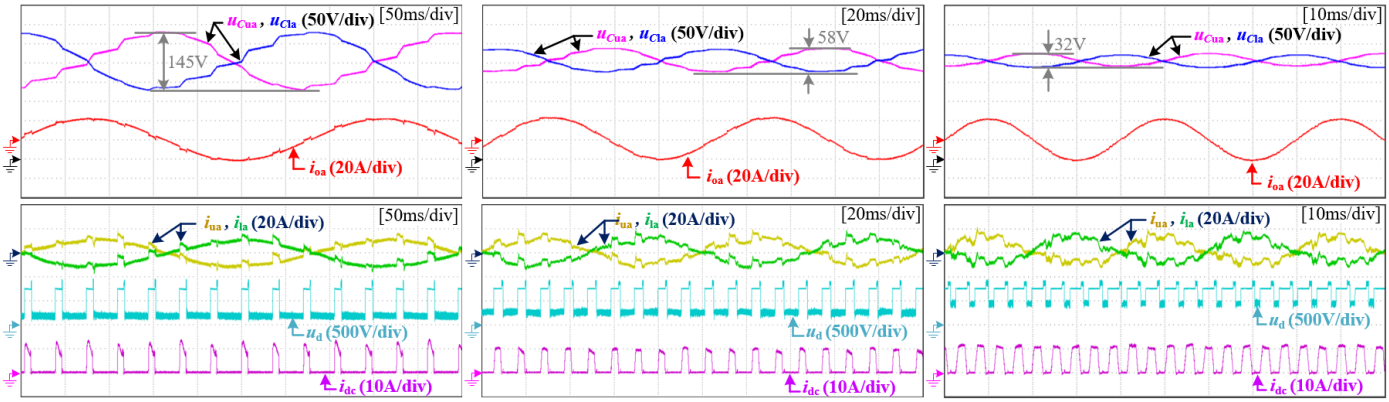

Fig. 12. Experimental results of the HMMC at different output frequencies under full-torque. (a) 3 Hz; (b) 10 Hz; (c) 25 Hz.

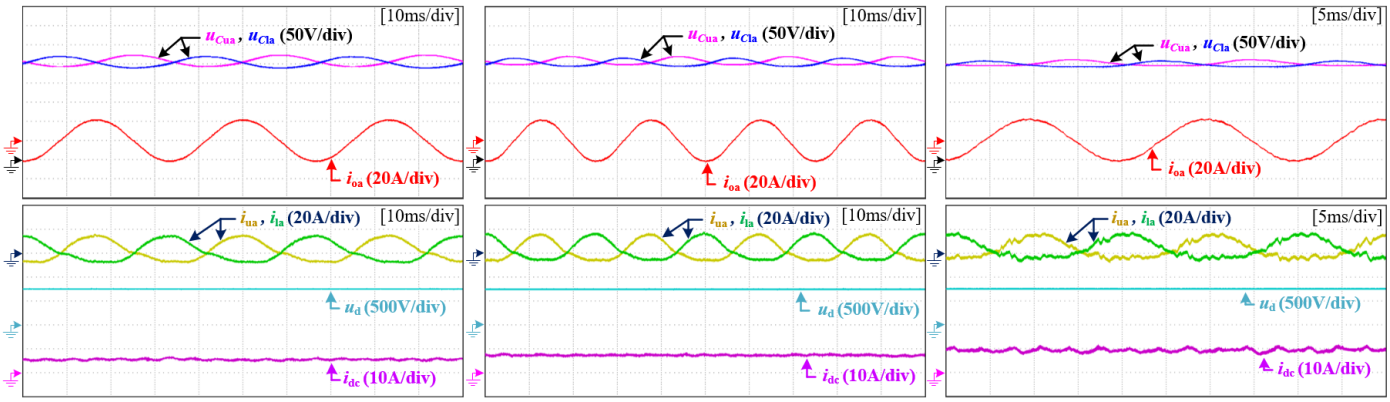

Fig. 13. Experimental results of HMMC (under MMC-operation) at different output frequencies under full-torque. (a) 30 Hz; (b) 40 Hz; (c) 50 Hz.

U_{dc} (750 V), so that S_T can be turned on softly and i_{dc} increases linearly without any overshoot. In the switching-off process, i_{dc} decreases linearly to zero, then u_d steps to be higher than U_{dc} and lasts 0.58 ms (T_2). This time is higher than the circuit commutated turn-off time of the thyristor (0.2 ms). Therefore, S_T can be turned off completely. The rising time T_1 of dc current is 0.51 ms, which closes to the theoretical value (0.53 ms) from (9). Therefore, with the proposed control scheme, the thyristor can be softly turned on and reliably turned off.

Fig. 15 and 16 show the effectiveness of the proposed failure tolerant control. In Fig. 15(a), a case of a 10 Hz HMMC operation without the proposed control is presented for comparison. It can be seen that the thyristor is turned off when the period of (T_1+T_2) reaches 1.1 ms, which is consistent with Fig. 14. Then (T_1+T_2) is reduced to 0.4 ms so that i_{dc} cannot decrease to zero before u_{com} drops. Therefore, when u_{com} drops, the thyristor fails to be turned off and i_{dc} experiences overrating, which leads to the shutdown of the HMMC. This matches well with the analysis from Fig. 3(b). Fig. 15(b) gives the case with the proposed failure tolerant control. When (T_1+T_2) is reduced from 1.1 ms to 0.4 ms, the thyristor fails to be turned off and i_{dc} rises rapidly. But when i_{dc} reaches to the threshold current I_{pro} (I_{pro} = 7A in this case), HMMC recognizes the thyristor fails to be turned off and orders u_{com} to rise to U_{dc}/2. Then i_{dc} dropped gradually. When the thyristor needs to act for the next time, (T_1+T_2) will be reset to 1.1 ms and the HMMC will return to normal operation. Fig. 16 shows the comparison of the experimental results when the thyristor is triggered accidentally.

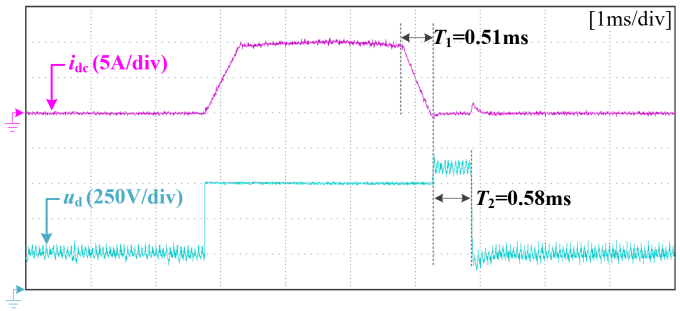

Fig. 14. Experimental waveforms of i_{dc} and u_d at 10 Hz under full-torque.

In Fig. 16(a), HMMC operates with traditional control strategy. A false triggering signal is generated deliberately in $s_i(t)$ after the thyristor turns off. Then the thyristor is turned on and i_{dc} experiences significant overshoot. This current spike would cause the shutdown of HMMC. On the contrary, with the proposed strategy, i_{dc} is limited to the threshold current I_{pro} (I_{pro} = 7A) when the thyristor is triggered unexpectedly, as shown in Fig. 16(b). As a consequence, the proposed method achieves the failure tolerant operation of thyristor without shutting down the HMMC.

Fig. 17 shows the effectiveness of the decoupled arm energy balancing control, considering a case of a 10 Hz output frequency. The conventional arm energy balancing control is used for comparison in Fig. 17(a). It can be seen that the fundamental frequency components $i_{cj,1}$ of circulating currents is asymmetric in three phases. Thus, the sum of the fundamental frequency components $\Sigma i_{cj,1}$ is also in the fundamental

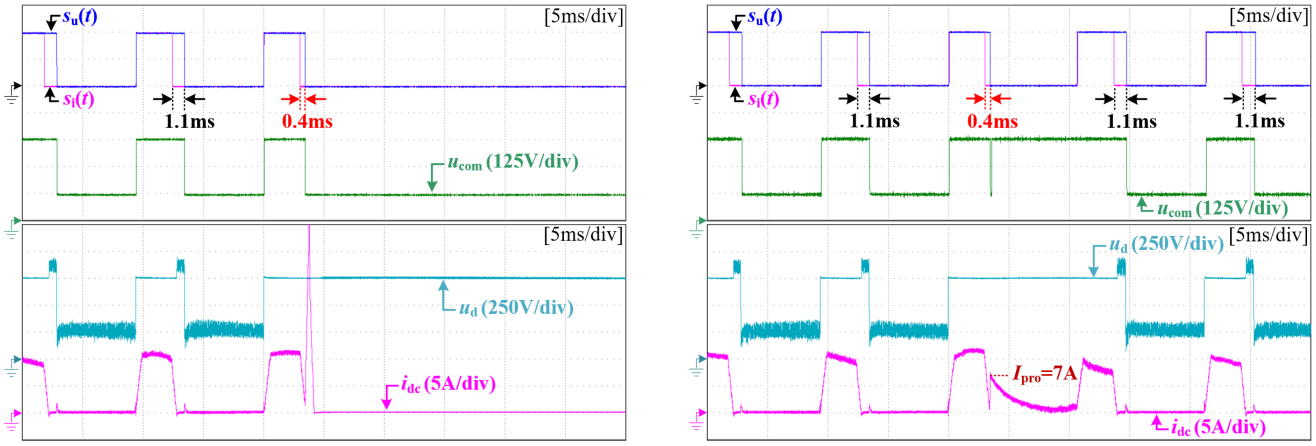

Fig. 15. Experimental results when the thyristor fails to be turned off: (a) without the failure tolerant control; (b) with the proposed failure tolerant control.

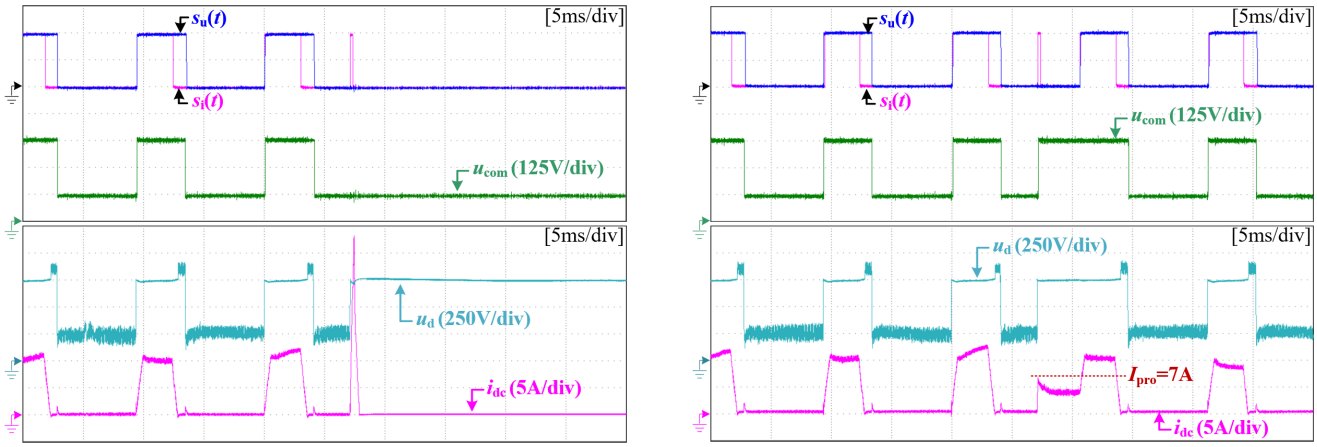

Fig. 16. Experimental results when the thyristor is triggered by mistake: (a) without the failure tolerant control; (b) with the proposed failure tolerant control.

frequency with a magnitude about 1 A. This current flows into the dc-link and exacerbates the fluctuation of i_{dc}. The maximum peak-to-peak value of i_{dc} is 2.8 A, leading to an increase of dc current stress. However, when using the decoupled arm energy balancing control, as shown in Fig. 17(b), $\Sigma i_{cj,1}$ is always zero. Thus the fluctuation of i_{dc} is significantly suppressed with its maximum peak-to-peak value of 1.2 A.

C. Discussion about Cell Capacitor Voltage Ripple

Fig. 18 gives an estimation of the experimental results with different cell capacitor voltage ripple calculation methods at low frequencies. Compared with the method proposed in [20], which is

$$\Delta u_{Cu(pp)} = \frac{I_{OM}}{2\omega C}\left[D_i + \frac{2U_{OM}}{U_{dc}}(1-D_i)\right], \tag{28}$$

the method proposed in this paper [Eq.(20)] can more accurately estimate the cell capacitor voltage ripple. Moreover, the results obtained from both (20) and (28) are like polylines rather than smooth curves. This is because "U_{OM}" and "φ" involved in (20) and (28) are obtained from the polylines in Figs. 10 and 11.

It is worth to note that the proposed failure tolerant control may cause a slight increase in the cell capacitor voltage ripple. As shown in Fig. 15(b), the voltage u_{com} will be forced up to U_{dc} when the thyristor fails to turn off. Thus the duty cycle D_u goes up, which leading to the increase of the cell capacitor voltage

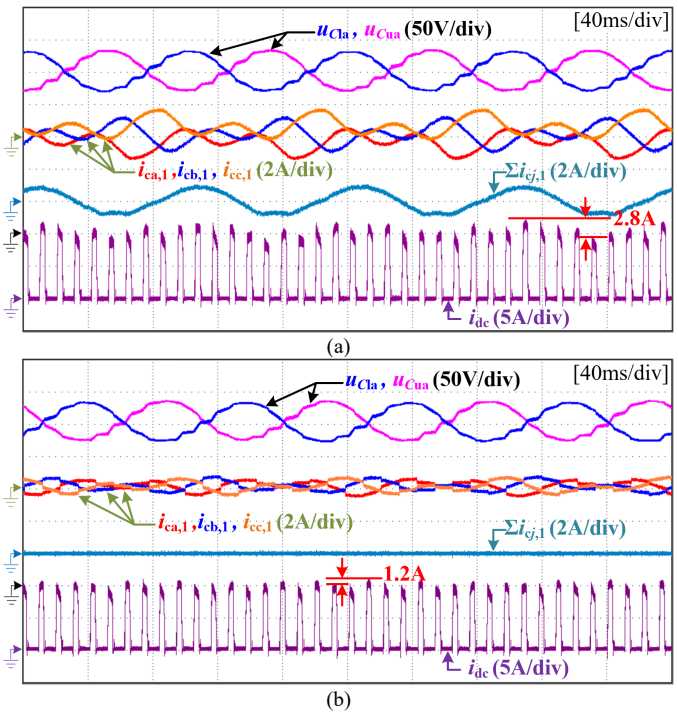

Fig. 17. Comparison the conventional arm energy balancing control and the decoupled arm energy balancing control at 10 Hz with full-torque. (a) Conventional method; (b) decoupled arm energy balancing control.

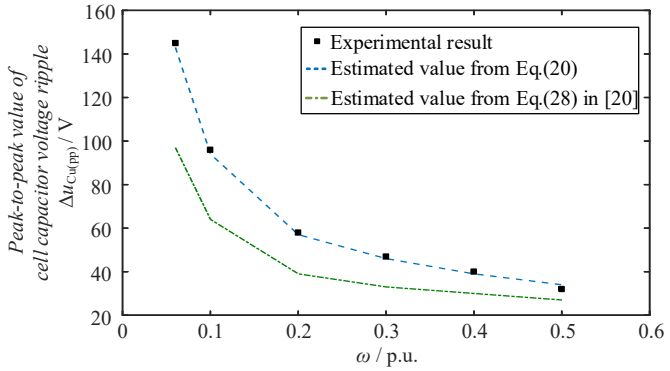

Fig. 18. Comparison of capacitor voltage ripple estimated values from (20) and (28).

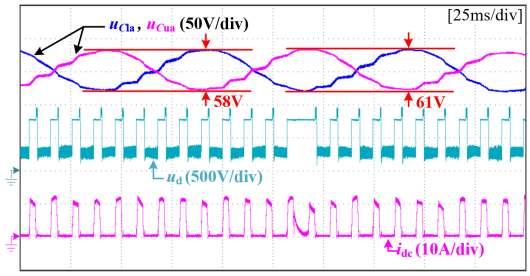

Fig. 19. The cell capacitor voltage waveforms of Fig. 15(b).

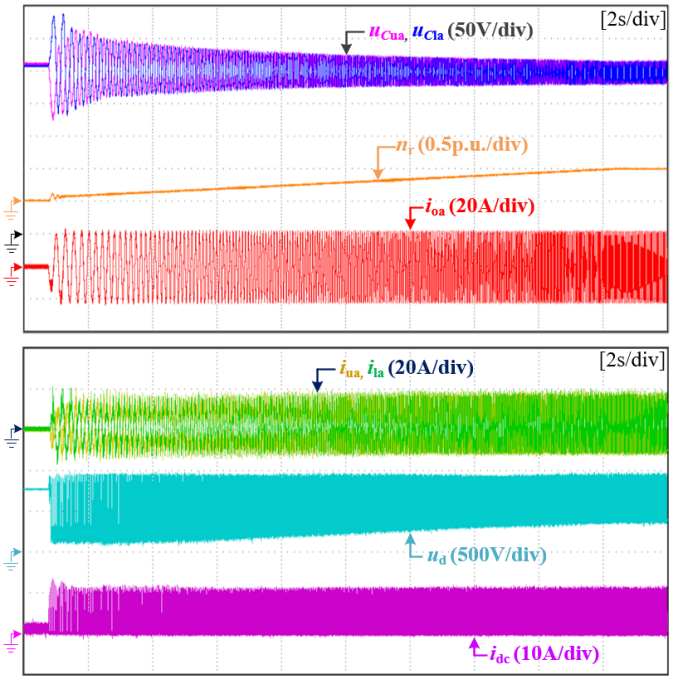

Fig. 20. Start-up process of the IM driven by HMMC from zero to 730 rpm with full-torque.

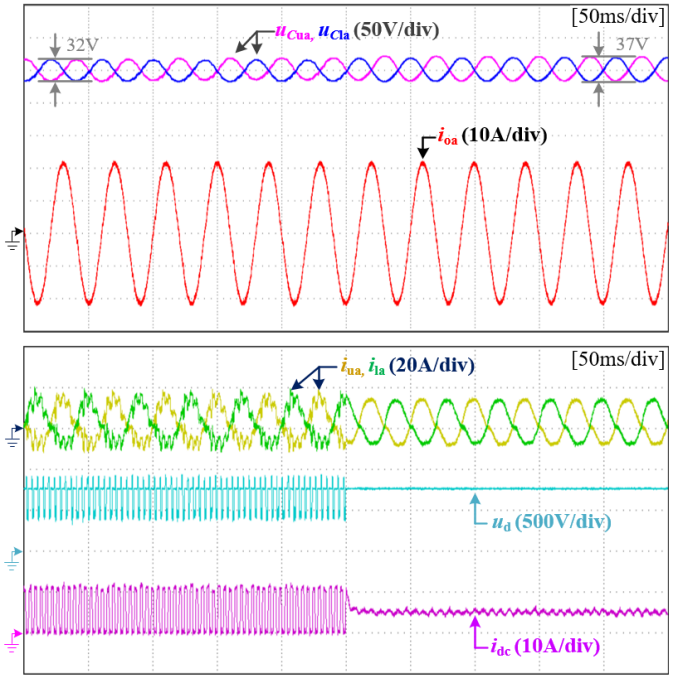

Fig. 21. Dynamic process of switching from the HMMC operation mode to the MMC operation mode at 730 rpm with full-torque.

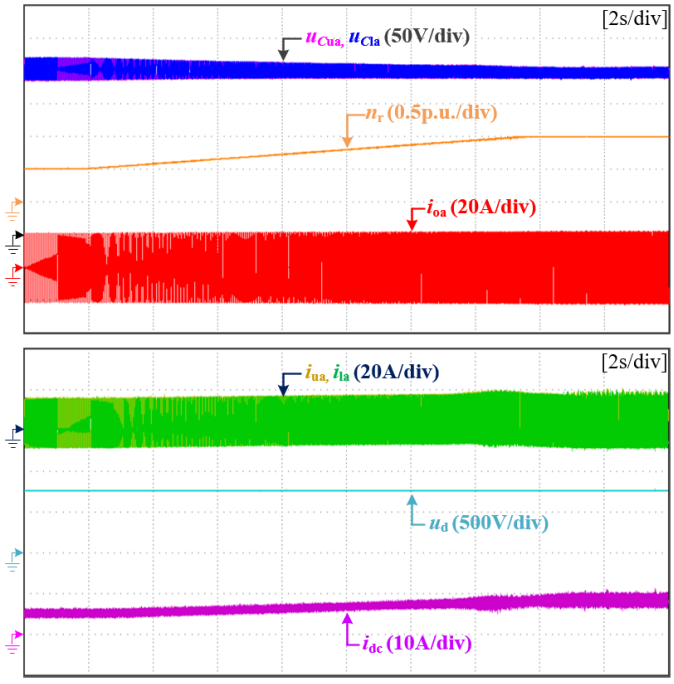

Fig. 22. Acceleration process of the IM driven by HMMC (under MMC operation mode) from 730 rpm to 1460 rpm with full-torque.

ripple according to (20). Actually, in the practical operation of HMMC, the odds of the thyristor failing to turn off is very limited. So the increase of the cell capacitor voltage ripple is slight and negligible. For example, Fig. 19 gives the cell capacitor voltage waveforms of Fig. 15(b). The peak-to-peak value of the cell capacitor voltage slightly increases from 58V to 61V.

D. Start-up Performance

The start-up procedure of the motor is divided into two steps. In the first step, the converter operates as HMMC during the low motor speed region [0, 730 rpm] to suppress the cell capacitor voltage ripple. The second step involves that the converter switches to the MMC mode with S_T constantly turned on during the high-speed region [730 rpm, 1460 rpm].

Fig. 20 shows the start-up process of the IM driven by HMMC during the lower speed region with full-torque. The rotor speed of motor n_r rises smoothly from zero to 730 rpm (0.5 p.u.). The maximum peak-to-peak cell capacitor voltage is suppressed below 150 V. The peak values of the arm currents i_{ua} and i_{la} are maintained around 20 A and no overcurrent appears in the whole process.

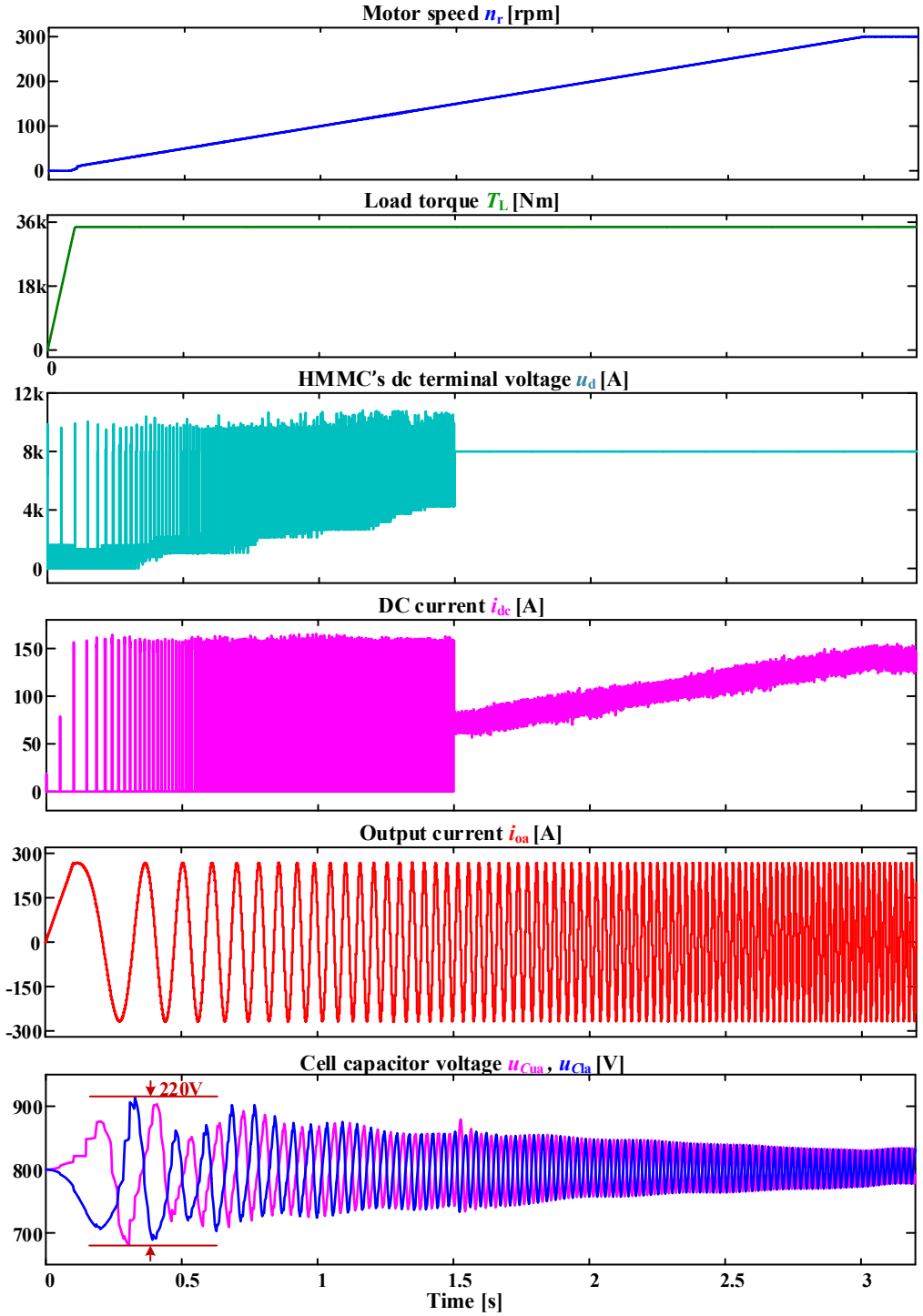

Fig. 23. The startup process of PMSM driven by HMMC with thyristor dc-link switch from standstill to rated speed.

Fig. 21 presents the dynamic process of the converter switching from HMMC to MMC at 730 rpm with full-torque. When S_T is constantly turned on, i_{dc} changes from a trapezoidal wave to a linear wave, and so does the u_d. During the whole dynamic process, the output current i_{oa} remains smooth without overshoot.

Fig. 22 further gives the acceleration process of the IM driven by HMMC from 730 rpm to 1460 rpm with full-torque. The waveforms are the same as the conventional MMC. When n_r reaches the rated speed of 1460 rpm (1 p.u.), the peak value of the arm currents i_{ua} and i_{la} is about 20 A, which is the same level as that during the low-frequency region shown in Fig. 20. This means the cell IGBTs do not need to be oversized compared with the HFCI methods.

Therefore, the HMMC with thyristor can drive the motor with full-torque during the whole speed region [0, 1460 rpm].

VI. Simulation Results

In order to test the performance of the proposed method in higher voltage application, a 1.2-MW/8-kV HMMC drive

system is simulated. The detailed parameters are shown in Table III and IV. As shown in Fig. 23, a permanent magnetic synchronous machine (PMSM) driven by HMMC starts up from standstill to rated speed 300rpm with constant torque. When the PMSM reaches 150rpm (0.5p.u.) at 1.5s, the thyristor is turned on constantly and HMMC switches to the MMC mode. During the whole transition process, the waveforms of motor speed n_r and ac output current i_{oa} are smooth and stable. Within the whole speed range, the cell capacitor voltage ripples are suppressed effectively with the maximum peak-to-peak value equal to 220V.

TABLE III
SIMULATION PARAMETERS OF HMMC

Number of cells per arm	N=10
dc source voltage	U_{dc}=8kV
Voltage for circulating current control	ΔU=800V(=10%U_{dc})
Margin voltage	δ=320V(=4%U_{dc})
SM capacitance	C=4mF
Arm inductance	L=1mH
Rising or falling time of dc current	T_1=125μs
Turn off time of the thyristor	T_2=225μs
Rated output frequency	f_{rated}=50Hz
Rated phase current magnitudes	$I_{OM(rated)}$=250A
Rated dc current	$I_{dc(rated)}$=150A
Cell switching frequency	f_{cell}=900Hz
S_T switching frequency	f_h=10×f

TABLE IV
SIMULATION PARAMETERS OF PMSM

Rated power	S=1.2MW
Number of poles	pp=10
Rated speed	n_r=300rpm
Stator line-line rated rms voltage	U_l=4kV
Rated torque	T_L=34kNm

VII. Conclusion

The dc-link switch is a challenging obstacle restricting the application of HMMC for high-voltage drive systems. This paper uses the thyristor instead of IGBT as the dc-link switch. The contributions of this paper include the following four aspects: 1) A control scheme aiming to make the thyristor softly turned on and reliably turned off is proposed. More importantly, when using the proposed scheme, HMMC can tolerate the turn-off failure of the thyristor without shutting down the converter, which effectively improves the reliability. 2) A decoupled energy balancing control is added to the proposed control scheme aiming to suppress the fluctuation of the dc current. 3) The cell capacitor ripple analysis which considers the effects of the thyristor switching process is presented. Then, a more accurate cell capacitor voltage ripple calculation method than that of [20] is obtained. 4) A 380 V/7.5 kW scaled-down IM prototype is utilized to examine the performance of HMMC with the thyristor dc-link switch. Experimental results validate the effectiveness of starting up a motor from standby mode to rated speed with full-torque.

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