

# **HIGH-EFFICIENCY AND BROADBAND PA DESIGN CONSIDERING THE IMPACT OF DEVICE KNEE VOLTAGE**

A thesis submitted to Cardiff University

in candidature for the degree of

**Doctor of Philosophy**

By

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# Abstract

The new 5G communications system requires the power amplifier (PA) circuits to be operated with high efficiency at both peak and back-off power within a broad RF and video bandwidth. The new 5G signal has an increased complexity for the modulation scheme, resulting into a high signal peak-to-average ratio (PAPR). In consequence, the performances of the PA are limited. This thesis addresses the design analysis for high efficiency and broadband PAs based on harmonic tuned continuous class-F (CCF) mode by including the I-V knee interaction. Most PA modes and waveform engineering techniques to elevate PA performances are ignoring the practical knee voltage. This thesis addresses the new performances of the CCF mode when the I-V knee interaction from the waveforms is considered. The current waveforms are a function of voltage waveforms, that clipped and generates harmonics when voltage waveform is expanded into knee region, as the device is operated with compression. The new performances of the CCF mode does not follow the ideal theoretical performances, instead, changes along the phase of 2<sup>nd</sup> harmonic impedance termination.

The interaction of the current and voltage (I-V) knee on the waveforms of CCF mode allowing load-pull emulation to be calculated, where the  $\alpha$  in CCF mode is the function of 2<sup>nd</sup> harmonic impedances termination in the actual device's load-pull technique. In this research, the load-pull emulation is performed only through mathematical calculation in MATLAB by manipulating the equation of drain current and voltage waveforms. Output power and efficiency contours are generated from load-pull emulation for CCF mode, that have almost identical behaviour with the actual device model and measurement, when the non-linear I-V knee interaction is considered. This emulation also investigates the efficiency of the device at the output power back-off (OPBO) range, with the sweep of the  $\alpha$  parameter. The investigation of the new CCF mode with I-V knee interaction is used as guide for a PA design with restriction of the phase of 2<sup>nd</sup> harmonic impedances termination to keep the efficiency high across wide bandwidth.

The video-bandwidth (VBW) performances for the PA can be extended using a baseband termination circuit at the device's output to shift the resonance frequency coming from the bias network and the device's output parasitic capacitance. The VBW enhancement is crucial in the 5G communication system where it is expected to operate up to 800 MHz, or even beyond this frequency, for the instantaneous bandwidth. Analyses are made on the components used in the baseband termination circuit in this thesis, where the VBW can be further extended by having the highest value of the shunt capacitor that is placed close to the device, with the lowest equivalent series inductance. This configuration shifted the resonance frequency and reduced the impedances seen by the device output on the matching and bias network. All the methods described in this thesis are adapted to design and investigate the performances of compact PA with integrated matching and baseband termination network. This PA is aimed to operate with high efficiency at the 50  $\Omega$  load impedances and at load modulated output power back-off across a wide-bandwidth. A CW simulation tests are used to evaluate the performances of the PA at peak power, while 2 tones signal with sweep frequency spacing is used to evaluate the VBW performances.



# List of Publications

## First author:

S. M. H. Syed Anera, T. Hussein, S. Alsahali, J. J. Bell, R. Quaglia, M. Kermalli, P. J. Tasker and J. Benedikt, “High-efficiency broadband PA design based on continuous class-F mode with compression,” in *IEEE International Microwave Symposium*, Boston, USA, June 2-7, 2019.

## Co-author:

T. Hussein, A. Al-Rawachy, S. Syed Anera, J. Bell, P. Tasker and J. Benedikt, “On the effective modeling of the test-set non-linearity,” in *91st ARFTG Microwave Measurement Conference (ARFTG)*, Philadelphia, USA, 2018.

S. Alsahali, D. Gecan, A. Alt, G. Wang, S. M. H. Syed Anera, P. Chen, S. Woodington, A. Sheikh, P. Tasker, and J. Lees, “A novel modulated rapid load pull system with digital pre-distortion capabilities,” in *93<sup>rd</sup> ARFTG Microwave Measurement Conference (ARFTG)*, Boston, USA, July 7, 2019.

# List of Abbreviations

**1G** – First Generation

**2G** – Second Generation

**3G** – Third Generation

**4G** – Fourth Generation

**5G** – Fifth Generation

**ACLR** – Adjacent Channel Leakage Ratio

**ADS** – Advanced Design System

**AM/AM** – Amplitude to Amplitude Modulation

**AM/PM** – Amplitude to Phase Modulation

**CCF** – Continuous Class-F

**CGP** – Current Generator Plane

**CW** – Continuous Waves

**DC** – Direct Current

**DE** – Drain Efficiency

**DUT** – Device Under Test

**eMBB** – Enhanced Mobile Broadband

**ESL** – Equivalent Series Inductance

**ESR** – Equivalent Series Resistance

**FET** – Field Effect Transistor

**FFT** – Fast Fourier Transform

**GaAs** – Gallium Arsenide

**GaN** – Gallium Nitride

**HEMT** – High Electron Mobility Transistor

**IoT** – Internet-of-Things

**IMD** – Intermodulation Distortion

**IMD3** – Third Order Intermodulation Distortion

**IMN** – Input Matching Network

**JFET** – Junction-Field Effect Transistor

**LDMOS** – Laterally Diffused Metal-Oxide-Semiconductor

**LNA** – Low Noise Amplifier

**LTE** – Long Tern Evolution

**MIMO** – Multiple-Input Multiple-Output

**MMIC** – Monolithic Microwave Integrated Circuit

**MOSFET** – Metal-Oxide-Semiconductor Field Effect Transistor

**OMN** – Output Matching Network

**OPBO** – Output Power Back-Off

**PA** – Power Amplifier

**PAE** – Power-Added Efficiency

**PAPR** – Peak to Average Power Ratio

**PEP** – Peak Envelope Power

**Pout** – Output Power

**RF** – Radio Frequency

**SiC** – Silicon Carbide

**SMD** – Surface-Mount Device

**VBW** – Video-Bandwidth

**WiMAX** – Worldwide Interoperability for Microwave Access

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# Chapter 1

## Introduction

### 1.1 Research Motivations

Wireless communications have been growing and evolving ever since the first successful transmission in 1896 by Guglielmo Marconi [1]. Wireless telecommunications standards have been introduced, initially from 1G, and now, at the time this thesis is being written, 5G has just been launched in several major cities in the world [2]. The difference between these wireless communication standards is the technologies that are introduced in their systems. 1G standard is an analogue based signal, while 2G is based on digital signal [3]. The complexity of the wireless standards increases over time as the demand for the data transfer increases. The 3G standards was introduced to support mobile broadband, where the users can have internet access through their mobile phones [4]. The easy access for the mobile internet has open a new way of communications where users can access the internet to watch TV, streaming videos and video call wirelessly. While the 3G system can support mobile broadband network, this system is not good enough to support higher demand of data over multiple users at higher speed. 4G system is introduced in 2006, where the data transfer rates are aiming up to 1 Gb/s [5]. Several technologies within 4G were introduced such as Worldwide Interoperability for



Microwave Access (WiMAX) and Long-Term Evolution (LTE) to meet the 4G requirements. Within this network, users can access much faster internet speed wirelessly, allowing for example, the streaming of high definition contents without the need for buffering.

The 5G communication which is now under development and partly being introduced since 2<sup>nd</sup> quarter of 2019, is the most anticipated technology in the next decade, and is expected to fully roll out from 2020. The 5G will replace 4G standards such that it will improve significantly on the data rates, with higher connectivity and lower latency [2]. 5G is expected to connect to a much larger network, with increased number of Internet-of-Things (IoT). The major technologies expected in 5G communications are the massive multiple-input and multiple-output (MIMO), and millimetre waves. These technologies allow the 5G communication expected to deliver up to 10 Gb/s to the users [6]. Figure 1.1 illustrates the comparison between 4G and 5G communication demands [6], indicating an increased demands for the new network.

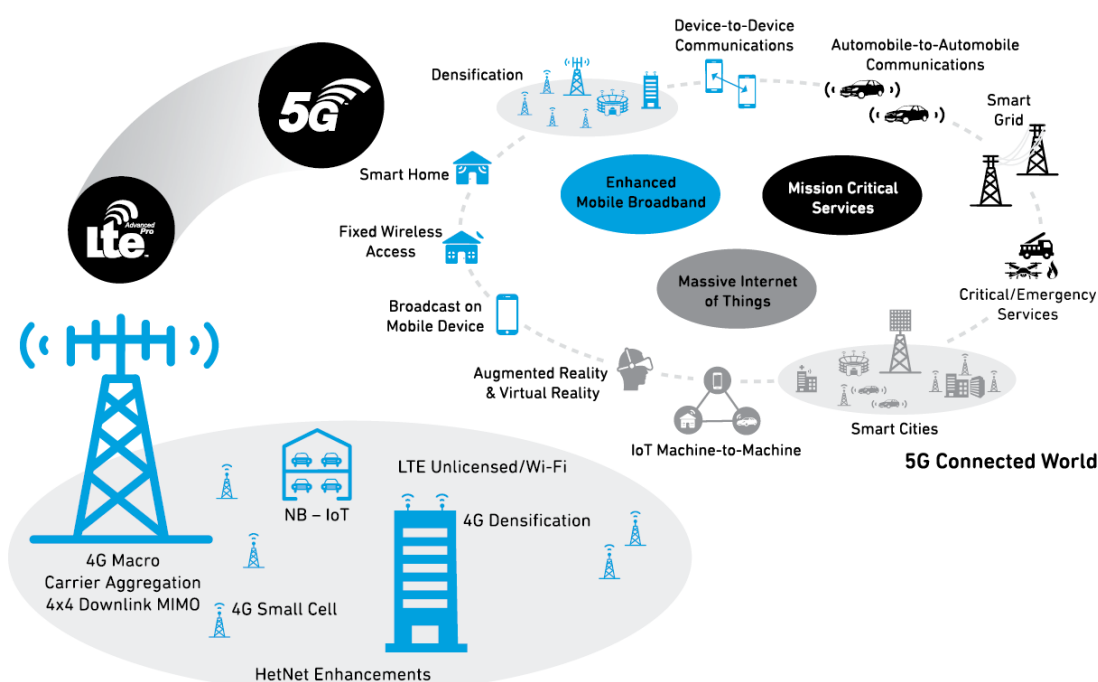


Figure 1.1. Comparison of communication demands between 5G and 4G LTE [6].

## 1.2 RF Power Amplifier Devices

The power amplifier (PA) is the main energy-consumer in the RF communications systems. The digital signal which is carrying the information for transmission has to be amplified, in the RF analogue forms, using PAs. A very basic explanation for PA operation is, the RF input signal is amplified using one or more transistors, by converting the DC power feeding into the device to amplify the small input signal into a large output signal. Transistors are used in PA circuits, with the first transistor was invented in the Bell's Laboratories in 1947. Prior to this invention, vacuum tubes were largely used, however they were bulky and experience heating issues.

Different types of transistors are available in the market, such as BJT, FET, JFET, MOSFET and etc. RF transistor technologies have evolved from the widely used GaAs and LDMOS devices to currently most advanced GaN devices [7]. LDMOS transistor are the most rugged, that can achieve more than 1000 W for a single transistor and operates with high efficiencies. They have been used for the PAs in the base-stations, military applications as well as RF heating for cooking. Despite having an outstanding performance, the LDMOS device can only operates up to a few GHz, recently reported up to 12 GHz [8], where the performances drop and becoming obsolete at millimetre wave frequencies.

On the other hand, GaAs devices have been used in most RF applications, ranging from PA, LNA, switches and attenuators. In the PA application, the GaAs devices emerged primarily for the development of MMIC. It has been used mostly in low power PA and LNA especially in mobile phones applications. GaAs devices can operate at higher frequencies than LDMOS, at millimetre waves frequencies.

More recently, GaN technologies emerged in the market, and have been widely involved in PA research. There are many advantages of this new device technology, such as excellent efficiency and the device operates at very high frequencies beyond 100 GHz towards THz [9]. GaN devices can operate with high breakdown voltage and can also withstand high temperature in comparison to other device technologies [10]. GaN devices have high power density, allowing them to deliver higher power due to high bandgap of 3 eV. Several processes of GaN are available, mostly on SiC, but it also available on diamond [11]. The major drawbacks of GaN technologies are due to its production cost and the market prices.

## 1.3 Classical Power Amplifier Modes

The typical power amplifier operation is classified based on their biasing points [12, 13, 14, 15]. The biasing indicates the PA modes, dividing it into different classes of operation. Considering the transistor as a current source, the biasing points determine the output current drawn into the device, where such behaviour is illustrated in Figure 1.2. This figure shows the transfer characteristic of the device, in this case, using an example of 10 W GaN HEMT device (CGH40010F) [16] is simulated, with a constant drain bias of 28 V.

### 1.3.1 Class-A

Class-A amplifier is the most linear among the other PA modes, where the device is biased at half of the maximum current,  $I_{max}$ , that the transistor can generate. The good linearity performances from this PA mode comes from the full 360 ° conduction angle of the output current and resulting harmonic-free voltage waveform, although non-linearities can still be generated, especially if the device is operated with compression. Despite being

the most linear PA among other classes and producing a high gain, this PA can theoretically operate only at a maximum of 50 % efficiency at the peak power. The class-A amplifier is typically used in a linear PA application such as driver amplifiers for highly input-sensitive RF equipment.

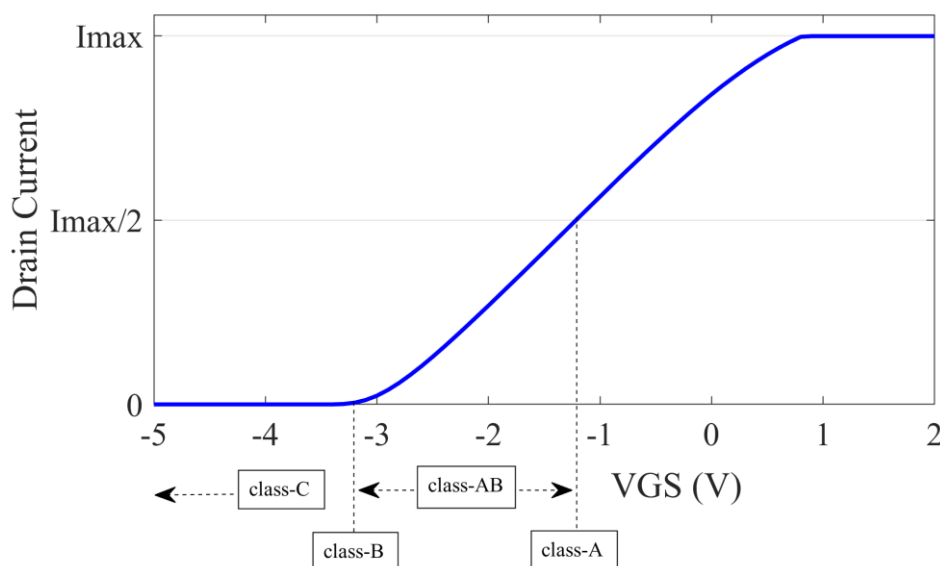


Figure 1.2. PA modes based on the device's gate biasing.

### 1.3.2 Class-B

Class-B mode PA is achieved when biasing the transistor device right at the pinch-off voltage, where the quiescent current drawn by the transistor drain reduced to zero, as shown in Figure 1.2. The conduction angle is  $180^\circ$ , producing half-rectified sinusoidal current waveform, as the device is operated with compression. The harmonics contents in the current waveforms is greater in this mode, due to its truncated shape, while, the harmonics in the voltage waveform have to be short-circuited to maintain a sinusoidal waveform. The harmonics generated by the device output in this mode result into some non-linearity issues, despite efficiency boost of up to 78.5 % theoretically. The operation of the PA in this mode is based on self-biasing, which means that at the low RF input

signal, the device is turns off, drawing very little or no current, which can affect the small signal gain.

### 1.3.3 Class-AB

Class-AB amplifier can be achieved by biasing the device between class-B and class-A, drawing very small amount of current and up to half of the  $I_{max}$ . Thus, the conduction angle varied between  $180^\circ$  to  $360^\circ$ . The PA is less linear than the class-A amplifier, however, it can provide better linearity than the class-B mode. The theoretical efficiency obtained from this mode ranges between 50 % to 78.5 %, depending on the biasing point. Typically, in RF PA application, a deep class-AB mode is chosen, drawing a very small quiescent current from the biasing just above the pinch-off voltage, allowing the PA to operate at high efficiencies, while also provides high gain and good linearity. Class-AB has been in favour in many RF PA design because it provides the trade-off between power, efficiency and linearity.

### 1.3.4 Class-C

Class-C mode amplifier is similar to the class-B amplifier, where it is biased to draw zero quiescent current at the device output. However, the gate bias voltage is lower than the pinch-off voltage, as indicated in Figure 1.2, thus the conduction angle for this amplifier mode is less than  $180^\circ$ . Class-C amplifier is theoretically more efficient than the class-B amplifier, ranging between 78.5 % to 100 %. However, the output of the amplifier generates higher order harmonics, giving it worst linearity performances as compared to the previous mentioned PA modes.

## 1.4 Research Objectives

The overall aim for this research is to improve the efficiency performances of the power amplifier, which is operating over a wide frequency band, mainly focusing between 1.8 GHz to 2.7 GHz. This research aiming to improve the efficiency at 8dB output power back-off (OPBO), targeting for outphasing PA application, as per Huawei's requirement. The specific aims for this research are as follows:

- To develop understanding through mathematical waveform theory, for the efficiency performances of CCF mode, when considering the device's knee voltage.
- To emulate the waveforms and performances of CCF mode when the device is operating under compression.
- To verify the mathematical reformulation of CCF mode with the knee interaction using load-pull simulation and measurement of a GaN device.
- To design, fabricate and measure a hybrid and broadband GaN PA with high efficiency, gain and output power in S-band frequencies based on the reformulated CCF mode operated with compression.
- To develop understanding through mathematical waveform theory, the separation between power and efficiency impedance optima for the CCF mode by considering the device's knee voltage. Understanding the separation between the two optima is crucial to improve the peak DE at output power back-off.
- To develop mathematical analysis for extending video-bandwidth (VBW) in power amplifier design using a practical baseband termination circuit.
- To design a single-stage broadband and compact PA using the integrated matching elements with high efficiency across S-band frequencies and enhanced video-bandwidth.

## 1.5 Research Flows

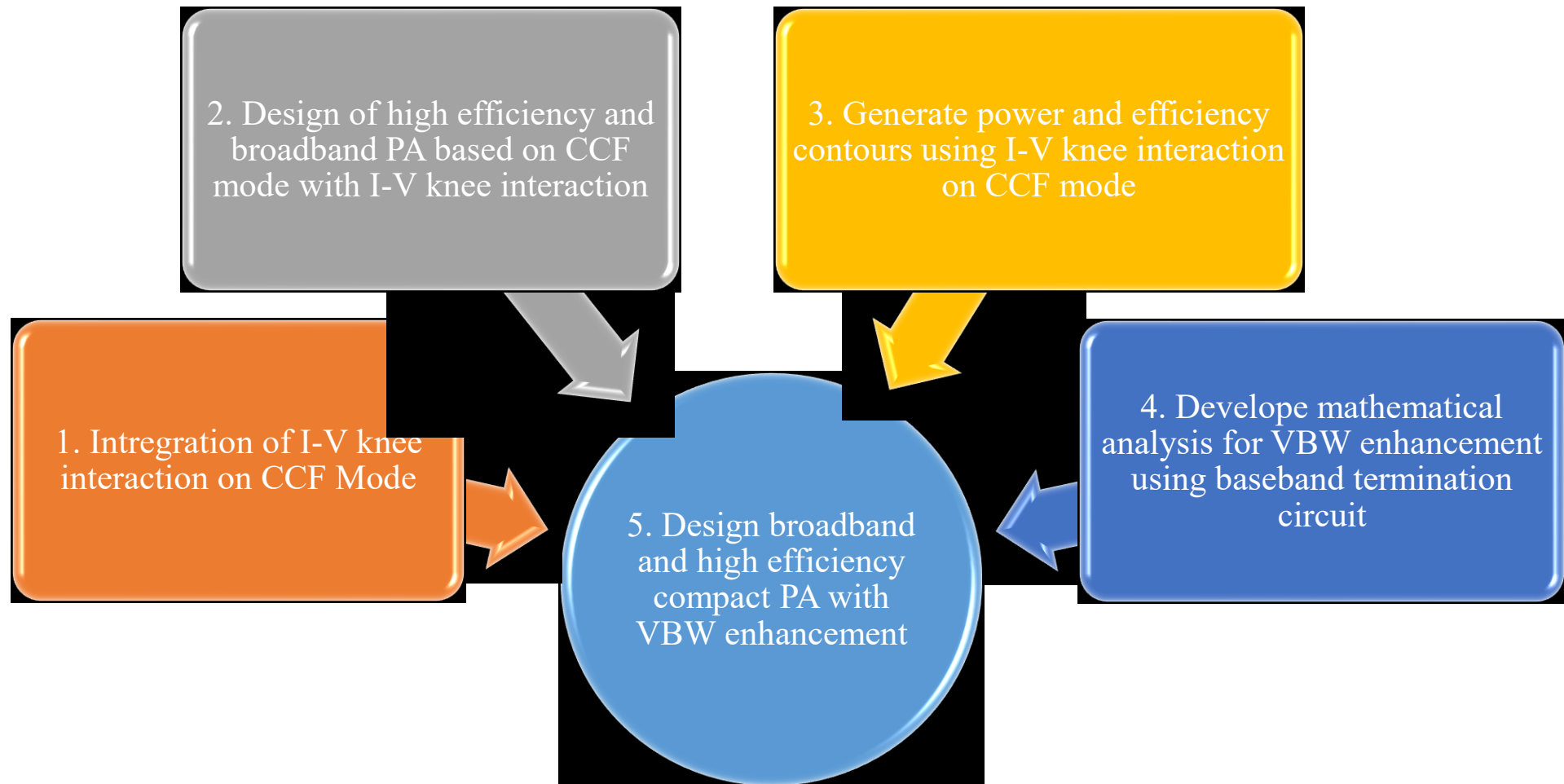


Figure 1.3. Summary of the research flows.

## 1.6 Thesis Organisation

This thesis consists of 8 chapters in total. The first chapter here, consists of the research motivations, aims, and the basic power amplifier classes of operation. The remaining chapters are summarised as follows:

**Chapter 2:** This chapter mainly describes the efficiency enhancement techniques for the power amplifier designs that are mostly adapted by PA designers. Different classes of PA modes are described, that are based on harmonic tuning. From class-F mode to the more recent continuous class-F mode, these PA modes have been the main aspiration for this work. The ideal CCF mode is described, showing its classical performance, where the knee voltage is ignored. Following this, other efficiency enhancement PA architectures, that focus on improving efficiency at power back-off are described. These architectures include Doherty, outphasing and envelope tracking PAs. These PAs represent the hottest topics being discussed as they are likely to be the most suitable PA candidates to be used in the 5G communication systems.

**Chapter 3:** This chapter describes the behaviour of CCF mode when the device is operated with compression. Ideal CCF mode is used as a starting point, whereby the definition of waveforms are reformulated to include the effect of I-V knee interaction. This I-V knee interaction emulates the waveforms behaviour within the knee boundary region, which is observed through mathematical calculation in MATLAB. The new performance of the CCF mode, by including the non-linearities coming from knee interaction are analysed. The mathematical emulation is verified using 10 W GaN device through load-pull simulation and active load-pull measurement.

**Chapter 4:** The main objective for the work in this chapter is to utilise the new mathematical reformulation of CCF mode from Chapter 3, to design a broadband RF PA



with high performances, especially for the drain efficiency, targeted at least 65 % across the wide S-band frequencies (1.7 GHz to 2.8 GHz). A 10 W GaN packaged transistor device is used for the RF PA design, that was designed and simulated using ADS software. The fabricated RF PA is measured, using small signal, large CW signal and modulated signal, to verify its performances.

**Chapter 5:** The work in this chapter extends the mathematical reformulation of CCF mode from Chapter 3, to emulate load-pull based on the waveform's theory, by including the I-V knee interaction on the CCF mode waveforms. The main objective for this work is to generate power and drain efficiency contours of CCF mode, through the mathematical emulation, to investigate the separation between optimum output power and drain efficiency impedances. The first investigation is performed using Pedro's linear load-line analysis [17]. This analysis is extended by including the non-linear I-V knee interaction into the mathematical emulations to give a much more accurate prediction of the actual device behaviour. This theory is supported by the load-pull simulation and measurement of the GaN device, where fundamental load-pull is performed, with a sweep of the 2<sup>nd</sup> harmonic impedances along the edge of the Smith chart. The maximum Pout, DE and peak DE at 8 dB OPBO are compared between the mathematical emulations, device's simulations and measurements.

**Chapter 6:** This chapter provides mathematical calculation and analyses for extending the video-bandwidth of a broadband PA using a baseband termination circuit. First, the analysis is based on the widely used baseband termination circuit by placing a shorted high value capacitor close to the device through a series of a low value inductor. The analysis is based on an ideal circuit, which is then extended for a more realistic approach, by including the equivalent circuit from the ideal components. The novelty in this chapter, is discussed through the analysis of each components within the circuit that is varied, to

improve the VBW performance.

**Chapter 7:** The final work in this thesis is presented in this chapter. The main objective for this work is to combine all the theories and analyses from the previous chapters, into a single PA design. The PA is also required to have a wide video-bandwidth. All these performance objectives are achieved through a compact PA design using an integrated matching network.

**Chapter 8:** This chapter provides the final conclusions for this thesis, by relating the aims and objectives initially set to the research with the overall work achievement. Here, the future works are underlined to describe any improvements that can be carried out from this research, as well as potential further work that can be investigated.

# Chapter 2

## High-Efficiency RF Power Amplifiers Designs

### 2.1 Introduction

The demand for power amplifiers operating with high efficiency has increased over the years, especially with the introduction of the new 5G standards. Mobile equipment that depends on a limited power availability, such as satellites and mobile phones, require high efficiency PAs to be able to operate much longer. In order to deliver bigger and faster data rates, the new communications standards require complex modulated signals, resulting into a high peak-to-average power ratio (PAPR) signals. For example, the LTE signal has 7.6 dB PAPR, which further reduce the overall efficiency performance of PAs when operated under this signal. Several design techniques have been presented, to improve the efficiency of the PA at the peak and back-off power, compared to classical PA modes and architectures.

## 2.2 High Efficiency PA Modes through Harmonic Tuning

The most common efficiency enhancement techniques for a single stage PA is achieved through harmonic tuning. The harmonic impedances presented to the device are tuned to shape the output waveforms for better efficiency performance [13, 14, 18, 19, 20]. Using the waveform engineering techniques, the desired waveforms that yield high performances are stipulated, making it possible to estimate optimum impedances at fundamental and harmonic frequencies. Several publications have optimised their PA performance by selectively tuning the harmonic impedances to enhance efficiency as well as increasing the frequency bandwidth. Here, the termination for the 2<sup>nd</sup> harmonics impedances is considered in [21, 22, 23, 24].

### 2.2.1 Class-F and Inverse Class F

The class-F mode PA can be achieved by shaping the output waveforms of the transistor, such that the drain voltage waveform is a square wave-shape, while the drain current waveform is a half-rectified sinusoidal wave-shape [13, 18, 19, 25]. The conduction angle between the 2 waveforms where the current and voltage alternately turn on is 180 °, as shown in Figure 2.1. Theoretically, these output waveforms are achieved by terminating the even and odd harmonics to short and open circuits respectively, giving a 100 % efficiency. However, infinite numbers of harmonics are needed to achieve this theoretical value, which is not possible for a practical RF PA design. The drain voltage and current waveforms in class-F mode equation is defined in (2.1) and (2.2) [25].

$$V_{ds}(\theta) = V_{dc} * \left( 1 + \frac{231}{200} \sin(\theta) + \frac{77}{400} \cos(3\theta) \right) \quad (2.1)$$

$$I_{ds}(\theta) = \frac{I_{max}}{2} * \left( \frac{2}{\pi} + \sin(\theta) - \frac{4}{\pi} * \sum_{r=1}^n \frac{\cos(2r\theta)}{(2r)^2 - 1} \right) \quad (2.2)$$

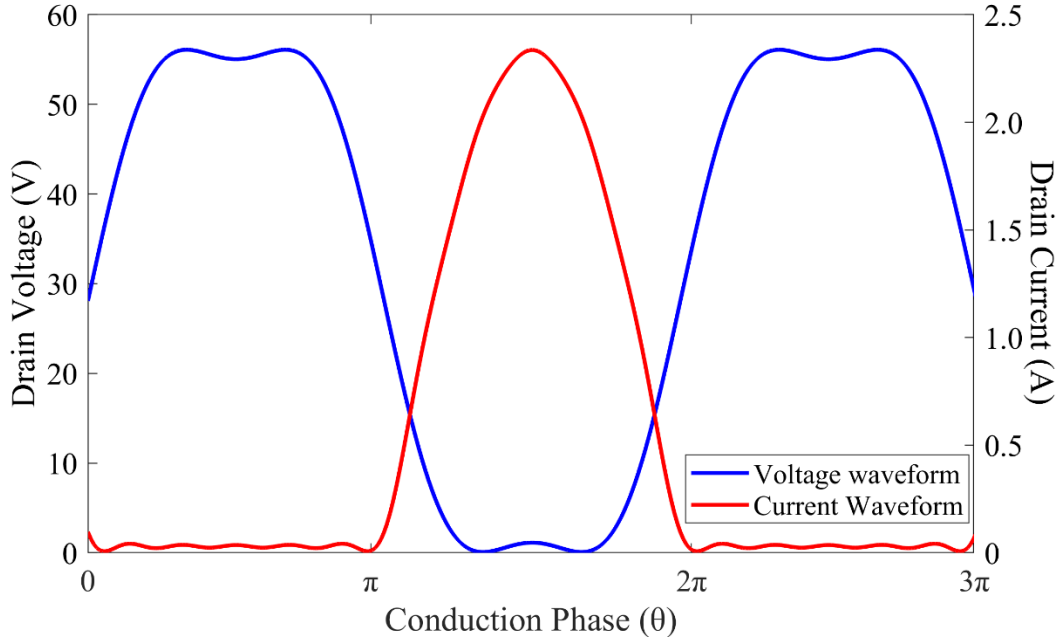


Figure 2.1. Ideal class-F mode waveforms considering up to three harmonics for voltage waveform and up to ten harmonics for current waveforms.

The square voltage waveforms can be expressed in different ways for different wave-shapes. The definition in (2.1) is for a square waveform expressed up to 3<sup>rd</sup> harmonic only, with a minimum ‘bounce’ or ripple on the wave-shape.  $V_{dc}$  is the DC bias voltage on the device’s output drain terminal. Other square waveform definitions as in [26] have more pronounce ‘bounce’ in the minimum and maximum of the wave-shape, while [13, 25] introduced maximally flat square waveform. The different definition of the square waveform shapes has only a minor effect on the shape of the load-lines. However, the current waveform defined in (2.2) consist of the general Fourier expansion for the half-rectified sinusoidal wave-shape, where  $I_{max}$  is the maximum output current the transistor can generate, and  $n$  is the number of even-order harmonics to define the waveform. Figure 2.1 shows the class-F mode waveforms, where the drain current is

defined up to the 10<sup>th</sup> harmonic. A value of 28 V and 2.5 A is used for the  $V_{dc}$  and  $I_{max}$  respectively which is taken from the DCIV characteristic of a typical packaged 10 W GaN device [16]. These waveforms are considered as ideal because the knee voltage of the transistor is ignored. Figure 2.2 shows the ideal load-line for this mode, indicating that the device is turn-on, producing high output current, even though the voltage is at 0 V.

The ideal analysis is used to analyse the performances for the PA under this mode. The output power obtained from the waveform is 18.6 W or 42 dBm. The efficiency is 86.9 %, which is reduced from the maximum theoretical value, due to only small number of harmonics considered. However, this value is higher than the maximum theoretical efficiency in class-B and class-AB. The optimum fundamental impedance for the waveforms in Figure 2.1 is  $28 + j 0 \Omega$ . Figure 2.3 shows the optimum fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonic impedances, normalised to the optimum fundamental impedance, plotted on the Smith chart. The single solution for the optimum impedances for this mode indicates that it can only be useful to design a narrowband PA [27]. A higher efficiency performance for class-F PA can be obtained by considering higher harmonic terminations of the harmonic impedances, as investigated in [28, 29].

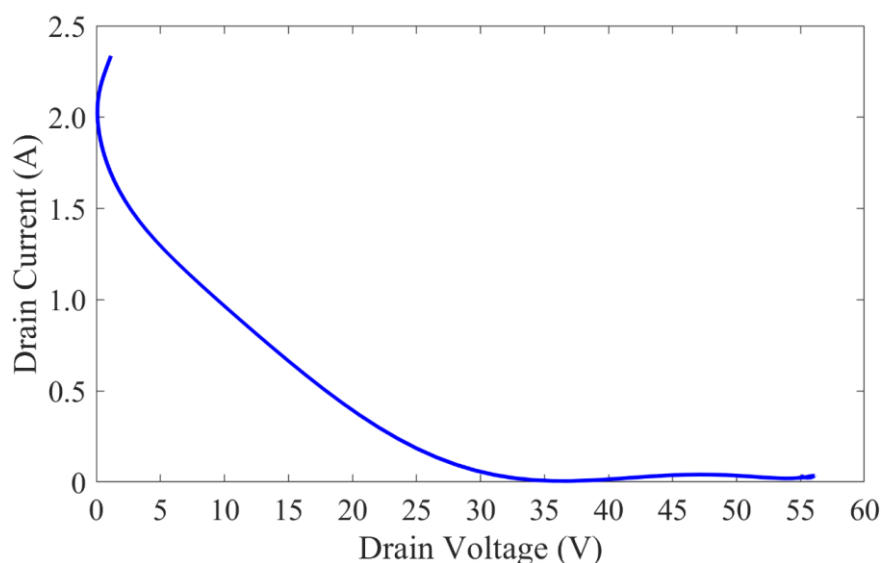


Figure 2.2. Ideal class-F mode load-line.

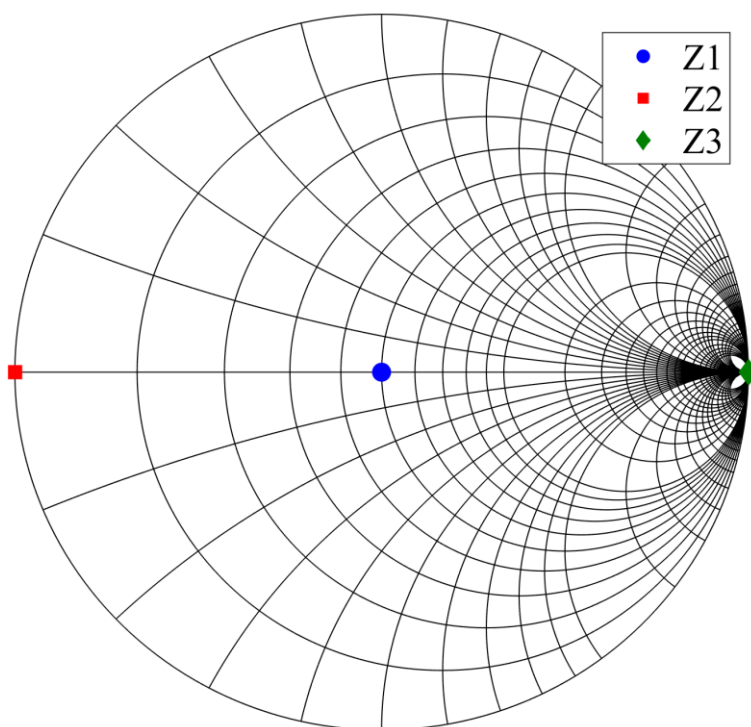


Figure 2.3. Optimum fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonic impedances for ideal class-F mode.

In inverse class-F mode, the definition for the voltage and current waveforms are the dual to the original class-F mode. The current waveform for inverse class-F mode is a square wave-shape while the voltage waveform is a half-rectified sinusoidal wave-shape. This mode can be achieved by terminating the even harmonics to the open circuit and the odd harmonics to a short circuit. Similar to the class-F mode, the ideal inverse class-F mode with an infinite number of harmonics terminated to the device will theoretically give 100 % efficiency. Figure 2.4 illustrates the output waveforms for this mode, by considering up to three harmonics to define both waveforms, which gives 79.5 % efficiency. Figure 2.5 shows the optimum fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonics impedances normalised to the optimum fundamental impedance, for ideal inverse class-F mode.

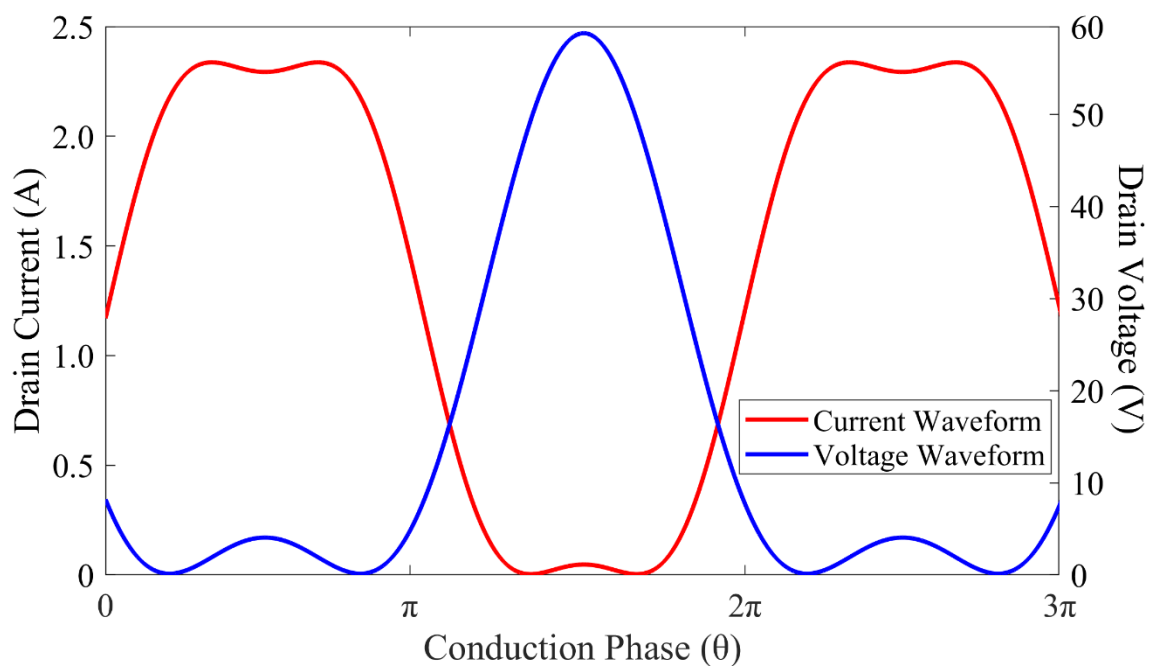


Figure 2.4. Ideal inverse class-F mode waveforms considering up to three harmonics.

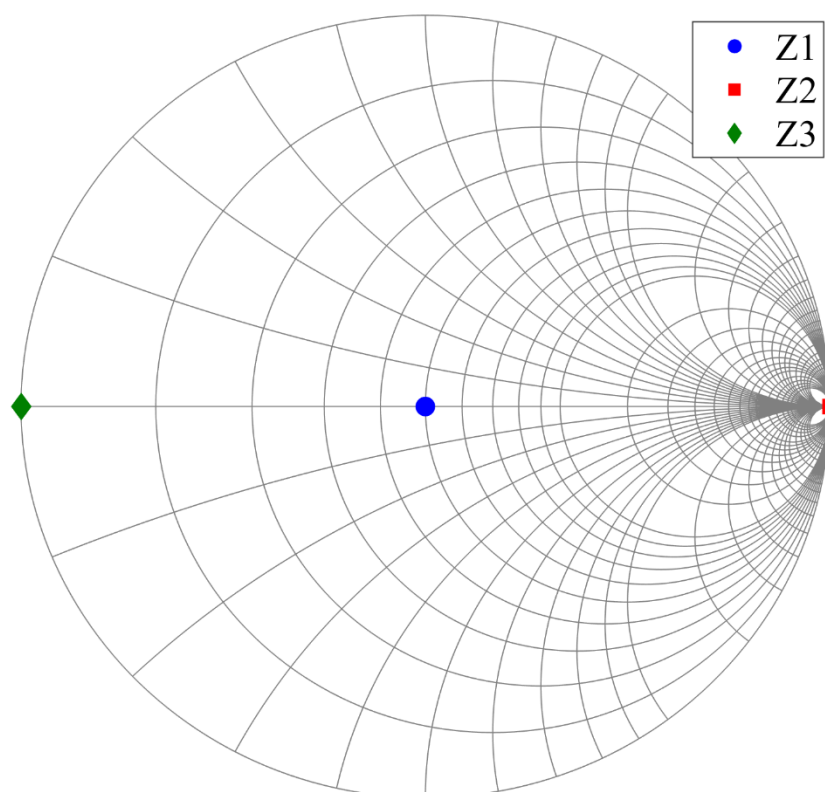


Figure 2.5. Optimum fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonic impedances for ideal inverse class-F mode.



### 2.2.2 Continuous Class-F

The continuous class-F (CCF) mode has been introduced through waveform engineering, based on the class-F mode, by extending the voltage waveforms definition when multiply with continuous operator,  $1 - \alpha \cos(x)$  [30, 31, 32, 33, 34, 26]. The derivation of the voltage waveform equation for CCF mode is shown in (2.3) where the definition of the Fourier expansion is up to the 4<sup>th</sup> harmonics. The current waveform for this mode remains as the half-rectified sinusoidal wave-shape with 180 ° conduction angle. The  $\alpha$  parameter changes the voltage waveform shape, as shown in Figure 2.6, peaking at more than 3 times the drain DC bias. The value of  $\alpha$  can only exist between -1 to +1 to abide with the device's physics, otherwise, beyond this value, the voltage waveforms starts to expand below 0 V. In this analysis, the definition of  $V_{dc}$  is 28 V and the current waveform is similar to the current waveform of the class-F mode shown from Figure 2.1. When the  $\alpha$  parameter increases or decreases to  $\pm 1$  value, even harmonics components appear in the voltage waveform, resulting in inductive and capacitive fundamental and 2<sup>nd</sup> harmonic impedances, as shown in Figure 2.7. The 3<sup>rd</sup> harmonic impedance remains at open circuit because the current waveforms defined from (2.2) do not contain any odd harmonics, which give infinite 3<sup>rd</sup> harmonic impedance when dividing the voltage by current waveform.

$$V_{ds}(\theta) = \left[ V_{dc} * \left( 1 + \frac{231}{200} \sin(\theta) + \frac{77}{400} \cos(3\theta) \right) \right] * (1 - \alpha \cos(\theta)) \quad (2.3a)$$

$$\begin{aligned} V_{ds}(\theta) = V_{dc} * & \left( 1 - \alpha \cos(\theta) + \frac{231}{200} \sin(\theta) - \frac{539}{800} \alpha \sin(2\theta) \right. \\ & \left. + \frac{77}{400} \cos(3\theta) - \frac{77}{800} \alpha \sin(4\theta) \right) \end{aligned} \quad (2.3b)$$

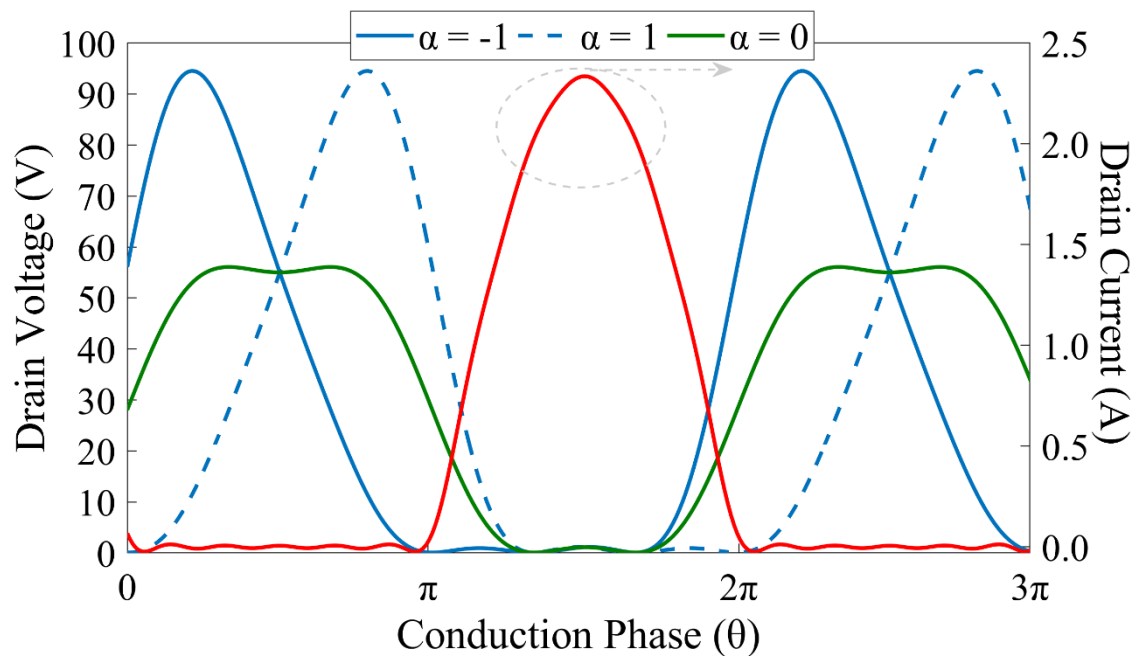
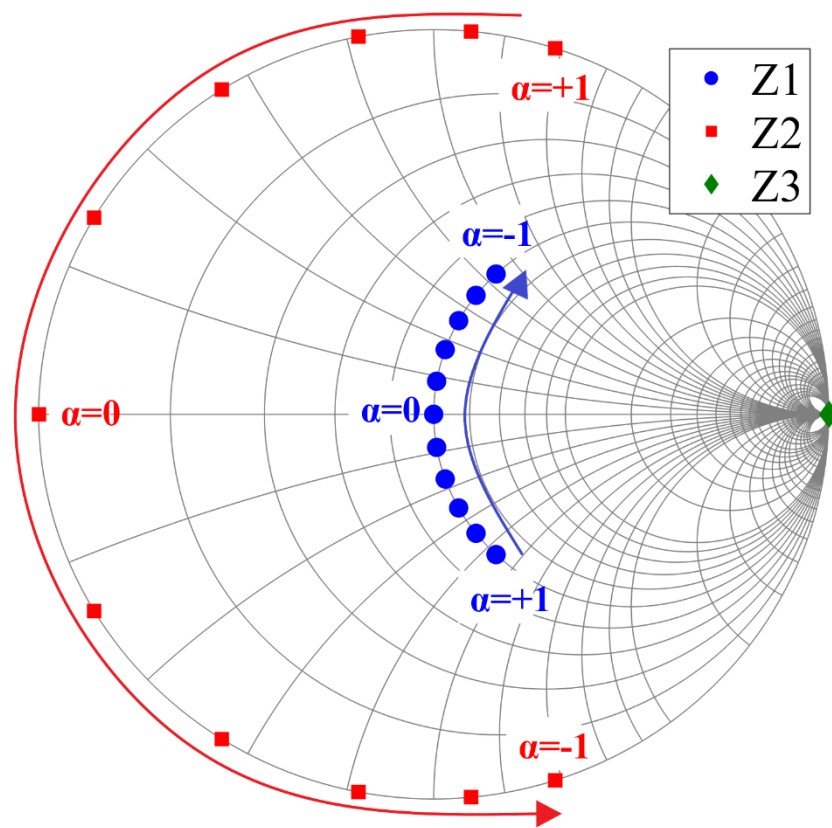


Figure 2.6. Ideal CCF mode waveforms.

Figure 2.7. Ideal CCF mode optimum fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonics impedances.

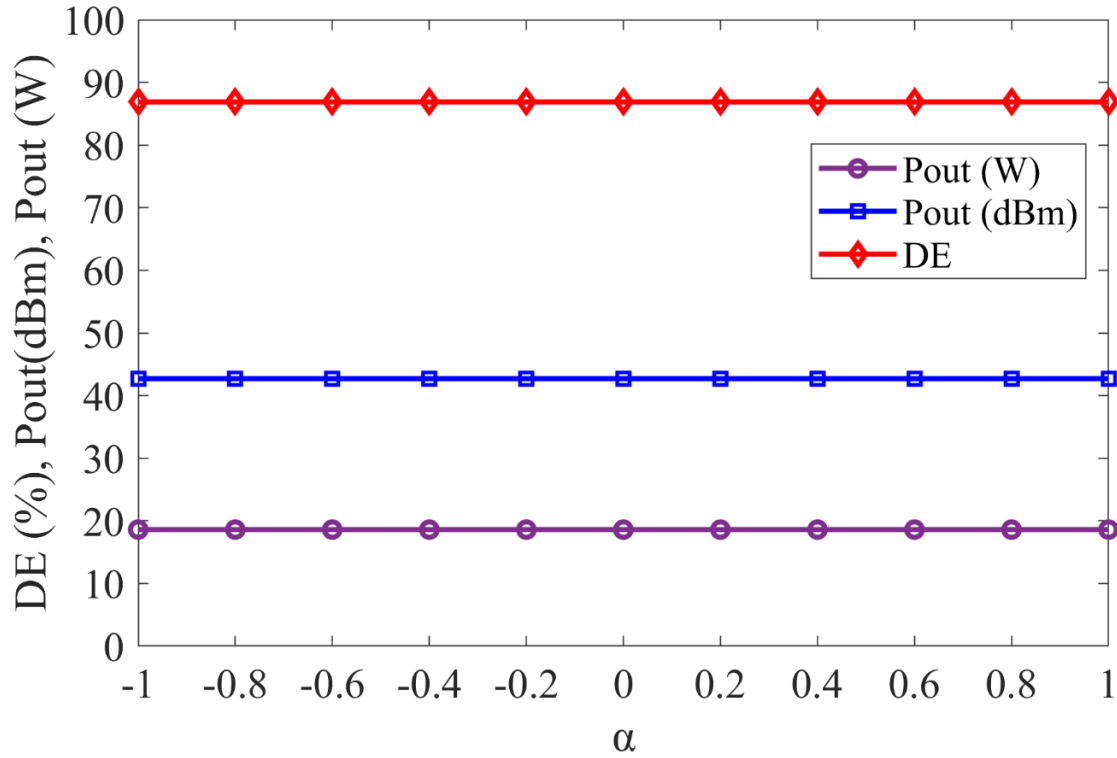


Figure 2.8. Ideal CCF mode performances.

The  $\alpha$  parameters rotates the optimum fundamental and 2<sup>nd</sup> harmonic impedances as shown in Figure 2.7. The  $\alpha$  rotations can be translated into the frequency dependences of PA operation, which can be used as the design space for a broadband PA. The ideal CCF mode provides a constant high efficiency and output power, equal to the performances of class-F mode, but is extended for the whole range of  $\alpha$ . Figure 2.8 shows the DE and Pout values that are constant at 86.9 % and 42 dBm across entire range of  $\alpha$  values. The DE value depends on the number of harmonics contained in the definition of voltage and current waveforms, whilst the Pout value depends on the value of  $V_{dc}$  and  $I_{max}$  from the current and voltage waveform initialisation. The full calculations to obtain the performances for the ideal CCF mode using MATLAB is shown in the Appendix 1.

## 2.3 Efficiency Enhancement Techniques Over Dynamic Range

Although the harmonic tuned PA modes such as the class-F and CCF can improve the efficiency performance, referring back to the waveform theory, high efficiency can only be achieved at the peak power level, where these waveforms are initially defined. The efficiency drops when the input and output power to the PA is backed-off, because the load-line is contracted. Figure 2.9 shows the typical class-AB PA performances over normalised output power level, reaching as low as 30 % at 8 dB power back-off. This value is relatively small when compared to the peak performances. Considering when the actual LTE signal is applied to the PA, the average output power will be at -7.6 dB from the peak, reaching down to -12 dB, resulting into a very low efficiency PA. Moreover, the PAPR for a 5G signal can be expected to be up to -15 dB. Several efficiency enhancement techniques have been introduced to enhance the PA efficiency, not only at the peak, but also at the back-off power level.

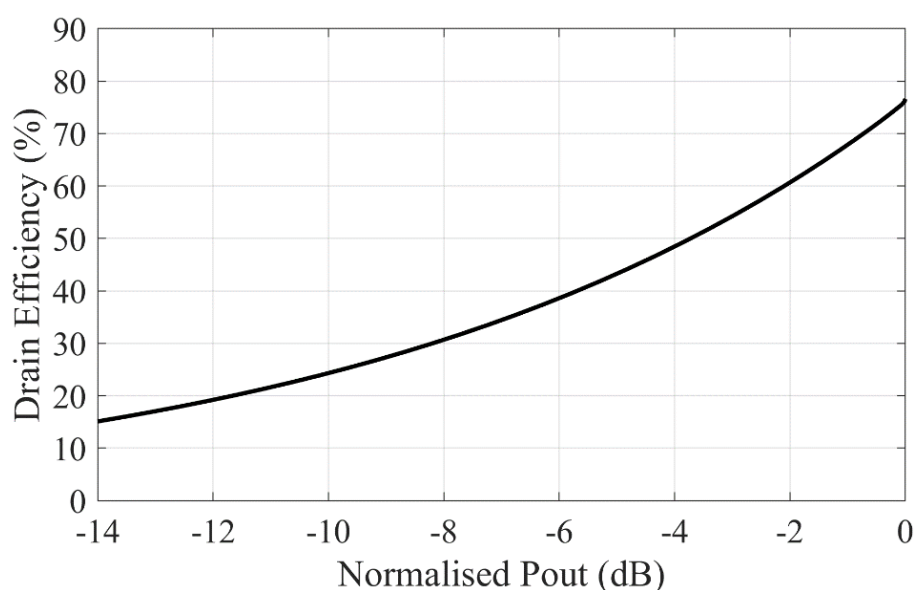


Figure 2.9. Typical DE vs normalised Pout for class-AB PA.

### 2.3.1 Doherty Power Amplifier

The Doherty power amplifier was introduced by W. H. Doherty at the Bell Telephone Laboratories, dating back to 1936 [35], to improve the efficiency of very high-power broadcasting transmitters using vacuum tubes. The classical Doherty PA architecture consists of 2 parallel and identical PAs, that are the main/carrier PA and the peaking/auxiliary PA [12, 18, 35], as illustrated in Figure 2.10. The operations for this symmetrical Doherty PA are as follows. The input signal is split into each PA, where a  $\lambda/4$  line shifts the phase of the input signal to the peaking PA by  $90^\circ$ . Power divider such as Wilkinson or hybrid type is usually used for the signal splitter. The main PA is biased typically at class-AB mode, meaning it is always turned on, producing a small signal gain. The peaking PA is biased in class-C mode, that is depends on a large RF signal for it to turn on. At low input power level, the peaking PA is turned off, producing zero current, while the main PA remains active. During this low input signal operation, the peaking PA has high impedance (presenting open circuit), while the main PA has impedances of  $2 \cdot R_{opt}$  due to the added  $\lambda/4$  line. The total output power is -6 dB from the maximum. At large input signal, the self-biasing on the peaking PA turns it on, reducing the optimal impedance seen by the main PA to  $R_{opt}$ . This operation creates a load-modulation seen by the main PA, in which at both states, the main amplifier is saturated. The maximum voltage of the main amplifier is constant at its peak between 0 dB to -6 dB total output power. The operation of the peaking PA actively load-pulling the main PA, through the  $\lambda/4$  line. Practically, delay lines are added at both the devices' input and output in order to balance the phase delay between the  $\lambda/4$  inverter line. Another  $\lambda/4$  line with  $Z_o/2$  characteristic impedance is added to restore the impedance back to  $50 \Omega$  load impedances.



maximum value of DE again at -6 dB back-off. The DE gradually decreases after this point. To compare, the DE can be greatly improved at the output power back-off from Doherty PA compared to the classical class-AB mode.

Over the years, the Doherty PAs have been a popular choices of the PA designer due to its good efficiency performance over output back-off ranges. The single-input and single-output configuration for this PA makes it preferable for use in RF front-end system. The efficiency performances of the Doherty PA over output back-off range can be extended with multiple stage configuration [18, 36, 37]. In the three stages Doherty PA, 2 peaking PAs are used, with 1 main PA, which reduces the dip of efficiency between maximum power and -6 dB output back-off as seen from classical symmetrical Doherty configuration. An asymmetrical Doherty PA is designed such that the output power of the peaking PA is much higher than the main PA [18, 38, 39]. The benefit of using asymmetrical Doherty PA is that the efficiency performances can be extended beyond the -6 dB output power back-off range, depending on the ratio of the main-to-peak PA power level.

More recently, the Doherty PA has been reconfigured such that the single input signal is not split to the main and peaking PA, instead each PA is driven separately and individually using a digital control [40, 41]. The advantage of using digitally control Doherty PA is that it removes the usual 3 dB losses of the power splitter, hence the gain of the overall Doherty PA can be increased. The phase shift between the input signal to the main and peaking PA can be controlled digitally, which is also beneficial to improve the overall bandwidth performances of the Doherty PA [40]. However, the complexity for this PA configuration could be a drawback for the cost of operation [41]. Additional controlled signal has to be in placed which also added another power consumption and increases the size of the overall circuit.

### 2.3.2 Chireix Outphasing Power Amplifier

Another efficiency enhancement technique was proposed by Chireix in 1935 using an outphasing PA configuration [42]. The term outphasing in this PA meaning 2 non-isolating RF input that are feeding into equally non-linear operating PAs with equal amplitudes but opposite phases [43].

At a specific outphasing angle introduced to the PA's inputs, the reactive element of the load impedances can be cancelled using the shunt reactive elements as shown in Figure 2.12. The operation of sweeping the outphasing angle from the input signal introduces load modulation seen by both PAs, as illustrated in Figure 2.13. The modulated load impedances varies between the optimum  $P_{out}$  impedance to the optimum DE impedance. Strategically, the compensation and the combiner network are designed such that, they will present load modulated impedances to each device, in track with the optimum output power and efficiency of each PA, when the outphasing angle of the RF input is swept [44, 45]. Due to the separation between the optimum power and efficiency of the transistor device, the peak efficiency is obtained at the load impedances where the output power is backed-off (OPBO points).

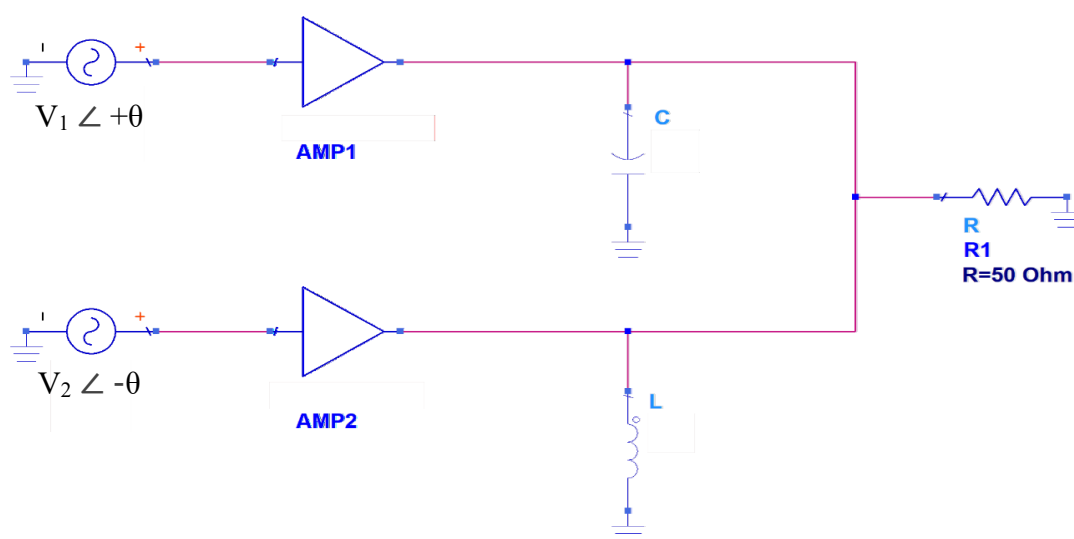


Figure 2.12. Chireix outphasing PA configuration with compensation network.



A packaged integrated Chireix outphasing PA is designed in [46, 47], with reduced size of the overall PA, where the combiner network is designed using transformers that is implemented using bondwires. A compensation network using offset transmission lines, such as in used Doherty PA, is included in the outphasing PA designs in [48, 49] to replace the ideal compensation network using a shunt capacitor and inductor. A combination of Doherty and Outphasing in a single PA, or also called DOPA, extended the operational bandwidth of a typical narrowband Doherty PA and outphasing PA [40, 50]. The PA works in outphasing mode at back-off power, while switching to Doherty mode at the peak power. A self outphasing Chireix PA is designed in [51], where only single input is required for the outphasing PA, that reduces the complexity for the PA operations.

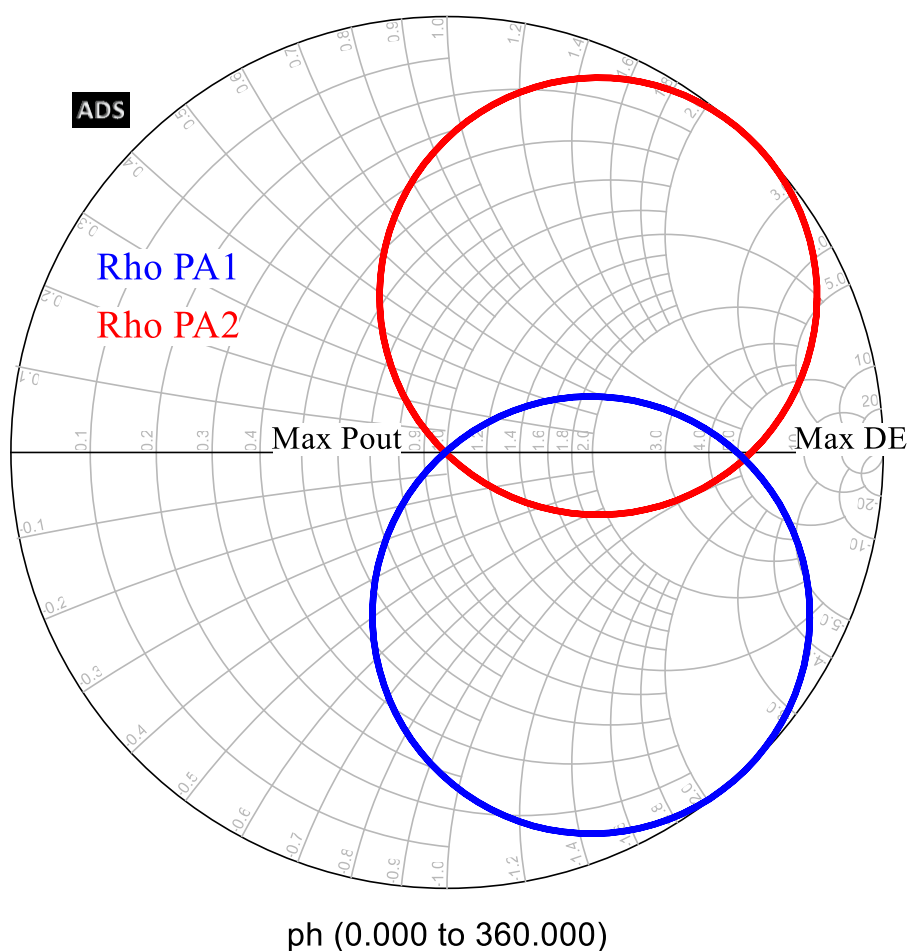


Figure 2.13. Impedances seen by each outphasing PA with compensation network as a function of outphasing angle.

### 2.3.3 Envelope Tracking

Typically PAs are operated with a fixed supply voltage. The envelope tracking power amplifier operates on the basis of shifting the load-line when the drain bias of the transistor device is reduced, with the same slope [12, 18, 52]. The output power is reduced, however, when the device is operated with compression, the efficiency is maintained high. Figure 2.14 shows the movement of the load-line when the drain bias voltage is reduced. The envelope tracking PA can be used to improve the efficiency at the back-off power by modulating the DC supply voltage to track the envelope of the input modulated signal. A DC modulator is used to detect the envelope of input or output modulated signal, which is then used to vary the drain DC voltage supply. In return, the DC bias is reduced for low output power, while keeping the device operated at saturation, which increases the overall efficiency.

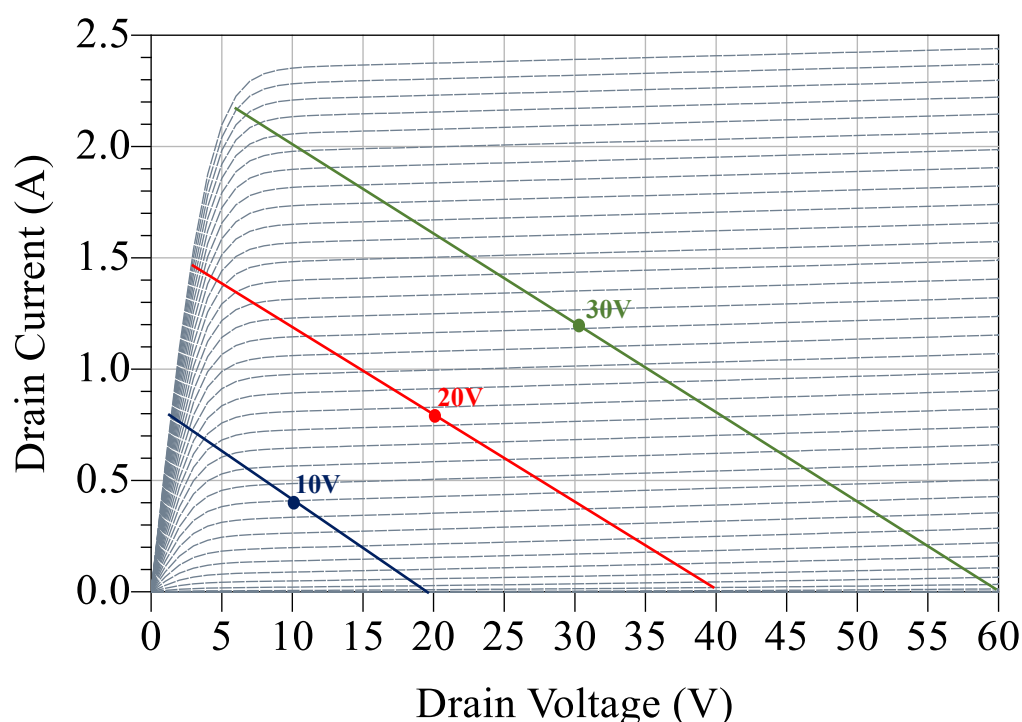


Figure 2.14. Load-line when changing the drain bias voltage.

## 2.4 Chapter Summary

This chapter has described the efficiency enhancement technique for PA design which is the crucial aspect that has driven the overall research within the PA community in recent years. The PA efficiency at the peak power can be improved through harmonic tuning such as in the class-F, inverse class-F and continuous class-F mode. In fact, the fundamental and harmonic impedances have to be carefully chosen to obtain the optimum efficiency performances at the peak power. Other continuous modes that are worth mentioning is the continuous class-B/J and the duality of CCF mode; the continuous inverse class-F mode [53, 54, 55]. PA designs using these modes improves the overall performances across wide bandwidth. Moreover, the input harmonics can also be tuned to improve the drain efficiency and improve the linearity of the PA [56]. The most common techniques used by PA designers for harmonic tuning PAs is to evaluate the transistor performances using load-pull, where the load impedances presented to the device are varied systematically. Active load-pull measurement have been introduced [57, 58, 59] to control fundamental and harmonic impedances presented to the device for the device measurement. More recently, a fast active load-pull measurement [60, 61, 62] improved the time taken for the necessary measurement to only few seconds, giving the PA designer the advantage of being able to evaluate transistor performances more accurately and more quickly.

Over the years, the complexity of the modulated signal used in communication systems has increased, which affects the overall efficiency performance of the PAs used. Several efficiency enhancement techniques have been introduced, dating back to the 1930s, where the Doherty PA and the outphasing PA are introduced. Recently, these PAs together with and the envelope tracking PA, have been widely investigated, because they are considering to be deployed in the 5G communications system. These PAs improve

efficiency at the output power back-off ranges, compared to for example, a typical single stage class-AB PA. More recently, a load-modulated balanced amplifier, or LMBA has been introduced, that is based on a balanced amplifier concept, with an additional controlled injection signal combined at the output through a hybrid couple, to actively load-modulate the PA for higher efficiency at back-off power [63, 64] and which operates over wide bandwidth.

# Chapter 3

## CCF Mode with I-V Knee Interaction

### 3.1 Introduction

To model a realistic transistor operation using the output waveforms, the knee clipping region should not be ignored. The knee region affects the device's load-line from the interaction between current and voltage waveform [12, 65]. Several recent publications have addressed the impact of integrating the operational knee voltage on PA design [66, 67]. The optimum impedance for the main PA in Doherty amplifier at the back-off changes due to non-zero knee voltage, affecting the Doherty performances if it not taken into account [68]. The soft turn-on knee characteristic of the transistor device is used to obtain separated power and efficiency contours of transistor device, to give a better understanding of its load-modulation characteristic [69, 17, 70]. In waveform theory, the realistic approach of modelling the transistor drain waveforms is to include the knee voltage [12], whereby the drain current waveform is now a function of the drain voltage waveform and the knee voltage, simplified in (3.1). In equation (3.1),  $V_{ds}(\theta)$  and  $I_{ds}(\theta)$  refers to the drain voltage and current waveform respectively. This I-V knee

relationship is used to model a realistic operation of transistor within the gain compression region, when the load-line is expanded into the non-linear knee region.

$$I_{ds,knee}(\theta) = \left(1 - e^{-\left(\frac{V_{ds}(\theta)}{V_{knee}}\right)}\right) * I_{ds}(\theta) \quad (3.1)$$

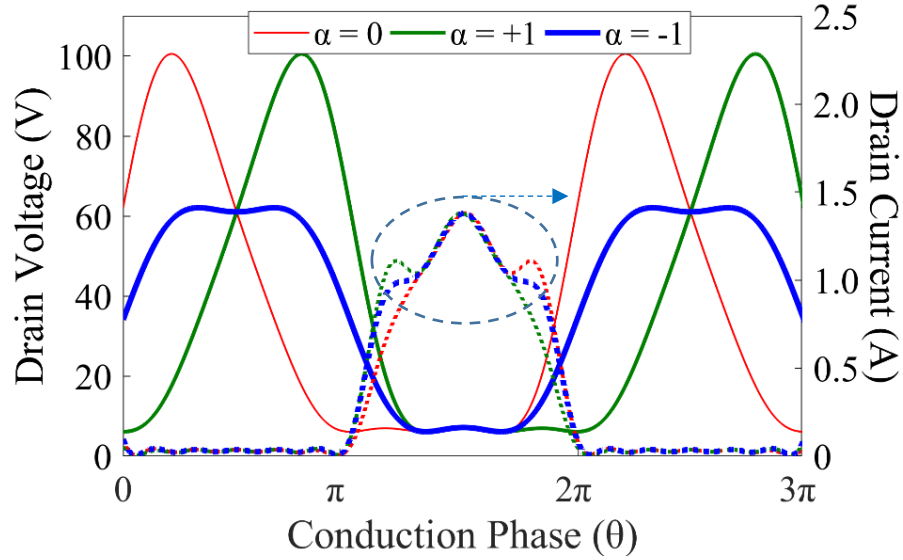


Figure 3.1. CCF mode waveforms with original I-V knee interaction.

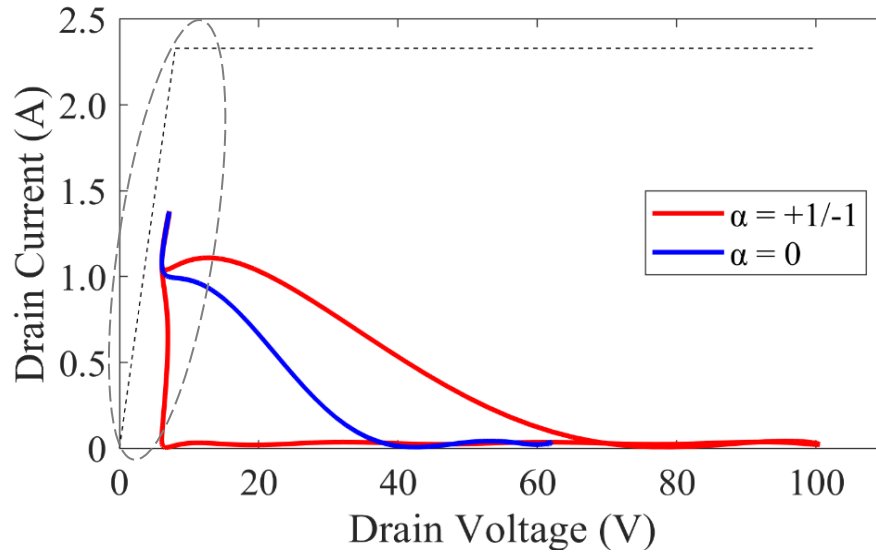


Figure 3.2. CCF mode load-lines with original I-V knee interaction.

An example for class-F waveforms operated with I-V knee scaling are as follows.

First, the drain voltage waveforms are scaled to be within the knee boundary by adding

voltage offset so that the minimum voltage is above zero but less than the knee voltage. The knee voltage is 8 V, taken from 10 W GaN HEMT Wolfspeed device. Using eq. (3.1) above and the resulting waveforms are shown in Figure 3.1, where the current waveforms are now clipped and truncated by the drain voltage waveform and the knee voltage. Figure 3.2 shows the load-lines plotted relative to the DCIV curve for the device, which are not in-line with the knee-boundary and have limited maximum current,  $I_{max}$ .

This chapter addresses this issue by reformulating the I-V knee scaling in (3.1) for compressed CCF mode waveforms. The new performances for the CCF mode by including the knee interaction are obtained through this new emulation and supported by the device verification in simulation and measurement. Passive load-pull simulation is performed in Keysight's ADS by presenting a load tuner at the device's output that defines the fundamental and harmonics impedances. Load-pull measurements are performed on the device using an active load-pull system. In the active load-pull system, fundamental and harmonic signals are injected into the device at the load, to control the impedances presented to the device respectively [57, 58, 59]. This chapter expands upon the first half of the published conference paper accepted in the International Microwave Symposium 2019 [71].

## 3.2 Reformulation of CCF Mode with I-V Knee

Modifications are introduced to both voltage and current waveforms to accurately represent these waveforms in a compressed CCF mode through the load-line analysis. In (3.2),  $\kappa$  is introduced to scale the magnitude of fundamental and harmonic components of the voltage waveform to emulate the compression of the device outputs. The default value of  $\kappa$  is 1 and it is valid only for  $1 \leq \kappa \leq 4/3$  to keep the voltage waveform above zero to

abide the device's physic as limitation. At the default value  $\kappa = 1$ , the device is in the linear region, and the minimum of the voltage waveform is equal to the knee voltage of the device, defined here at the drain voltage value (8 V) at the maximum drain current,  $I_{max}$ . As  $\kappa$  increases, the device is further compressed, and it enters the non-linear knee region.

$$V_{ds,new}(\theta) = \left( V_{dc} - \frac{V_{knee}}{2} \right) * \left( 1 + \kappa * \left( -\alpha \cos\theta + \frac{231}{200} \sin\theta - \frac{539}{800} \alpha \sin 2\theta + \frac{77}{400} \sin 3\theta - \frac{77}{800} \alpha \sin 4\theta \right) \right) + V_{knee} \quad (3.2)$$

$$I_{ds,new}(\theta) = \left( 1 - e^{-\left( \frac{V_{ds,new}(\theta)}{\gamma} \right)} \right) * I_{ds}(\theta) \quad (3.3a)$$

$$\gamma = \begin{cases} |V_{min} - V_{knee}|; & \text{if } V_{min} < V_{knee} \\ 0.01; & \text{if } V_{min} \geq V_{knee} \end{cases} \quad (3.3b)$$

In [12],  $V_{knee}$  has a constant value, whereas [69, 17, 70] suggested a varying  $V_{knee}$  that leads to separation of power and efficiency optimum impedances. The current waveform equation is modified, shown in (3.3). In (3.3a), the knee voltage scaling is a function of the minimum from the voltage waveform ( $V_{ds,new}$ ),  $V_{min}$ , that can be represented by a Piecewise function, detailed in (3.3b). This Piecewise function is introduced, as a simple solution to keep the load-lines in track within the knee boundary. Figure 3.3 and Figure 3.4 show the waveforms of the modified CCF mode for  $\alpha = 0$  and  $\alpha = 1$ , respectively. These waveforms are based on the minimum of the voltage waveforms that are set to 2 V, 4 V, 6 V and 8 V respectively, by varying the  $\kappa$  parameter. The voltage waveforms expanded, reaching a minimum value towards 0, as  $\kappa$  is increases. Consequently, the current waveforms interact with the voltage waveforms movement within the knee boundary, resulting into current waveforms clipping. The movement of



these load-lines is now tracking with the knee boundary region of the device (shown on the grey dotted lines), as shown in Figure 3.5.

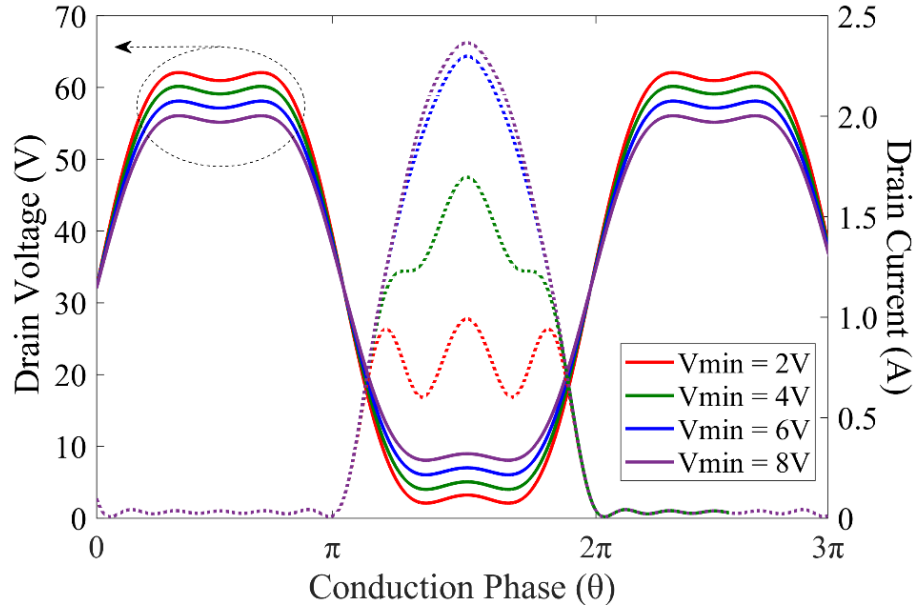


Figure 3.3. Emulated CCF waveforms ( $\alpha = 0$ ) using modification of I-V knee scaling with compression, by varying the  $\kappa$  parameter to change the minimum of the voltage waveform,  $V_{min}$ , to be within the knee boundary.

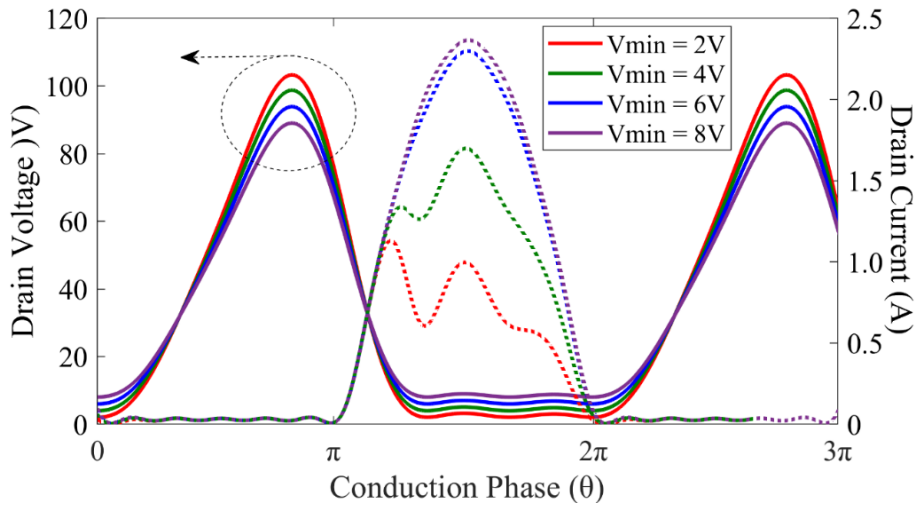


Figure 3.4. Emulated CCF waveforms ( $\alpha = 1$ ) using modification of I-V knee scaling with compression.

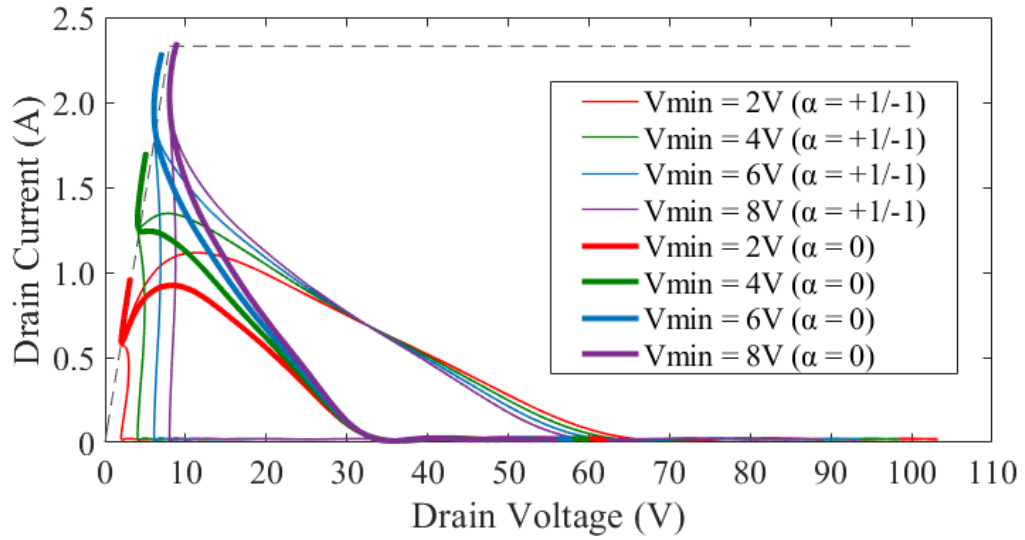


Figure 3.5. Emulated CCF load-lines using modification of I-V knee scaling with compression.

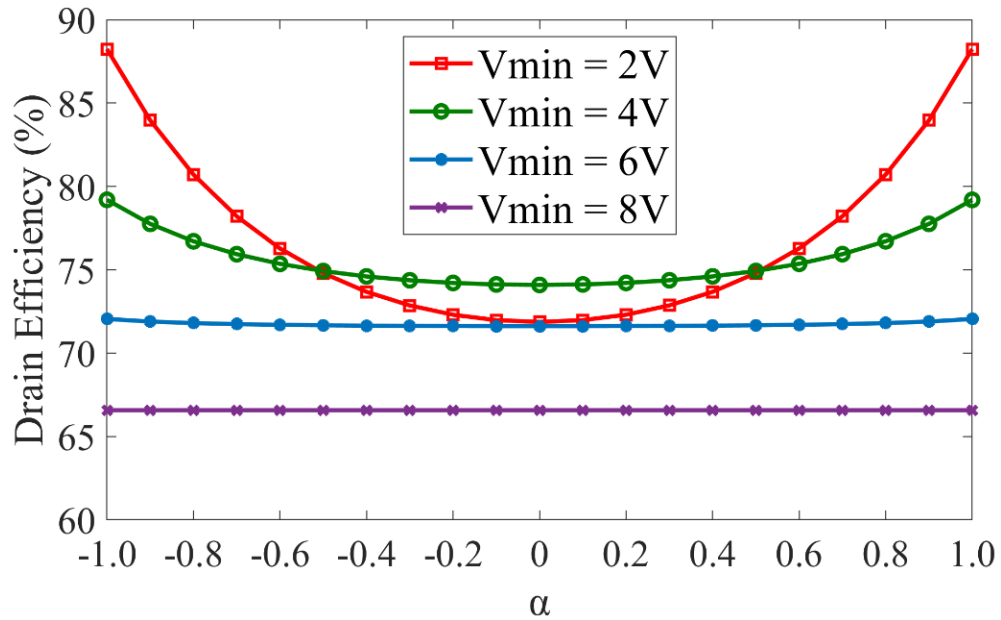


Figure 3.6. Emulated CCF mode drain efficiency at different level of compression within  $\alpha$  spaces.

Figure 3.6 shows the new emulated drain efficiency of the CCF mode with compression from the generated waveforms in Figure 3.3 and Figure 3.4. This efficiency calculation was also extended to cover the entire range of the  $\alpha$  space. The drain efficiency is constant across  $\alpha$  space when the minimum of the voltage waveform is just at the knee

voltage, 8 V, similar to the ideal CCF behaviour in [31, 33, 26]. However, the value of the DE is relatively low, due to a big difference between voltage and current waveforms. The DE increases as the load-lines moves further into knee region, reaching its peak when  $\alpha = -1/+1$ . The drain efficiency is at minimum when  $\alpha = 0$ , as in Class-F mode. Essentially, the new peak drain efficiency changes when the knee voltage is accounted and the device is compressed, showing a symmetrical behaviour around  $\alpha = 0$ . The full calculations for the CCF mode operated with I-V knee interaction through MATLAB is shown in the Appendix 2.

### 3.3 Simulation of CCF Mode with Compression on 10 W GaN Device

A 10 W GaN HEMT packaged device from Wolfspeed (CGH40010F) is used to test the new CCF theory in the previous section. ADS load-pull simulation is performed on the device's non-linear model and the device is de-embedded at the output plane so that the fundamental and harmonics load impedances are presented at the device's intrinsic drain plane. The device is de-embedded using a static de-embedding file which is used in the ADS simulation. To simulate CCF mode on the 10W device, the fundamental load impedances are swept across the entire region of the Smith chart while the 2<sup>nd</sup> harmonic load impedances are swept from 80° to 280° around the edge of Smith chart. The variation of 2<sup>nd</sup> harmonic impedances equals the  $\alpha$  space of CCF mode, which for this device, 80°, 180° and 280° is equal to  $\alpha = +1$ ,  $\alpha = 0$  and  $\alpha = -1$  respectively. The 3<sup>rd</sup> harmonic impedances are kept constant at an open circuit for all simulation points. The device is biased at 28 V and -3.2 V at drain and gate respectively ( $I_{dq}=13$  mA) through ideal DC feed and ideal DC blocks are used at both device's input and output to contain the DC in the PA circuit only. The transistor is driven into compression by an RF input of 2.0 GHz with 50  $\Omega$  source impedances and  $P_{in} = 25, 26, 27$  and 28 dBm. Figure 3.7 depicts the schematic of the passive load-pull simulation performed in ADS. The load tuner shown on the right-side in this figure consists of several sets of equations, that set the matrices of fundamental impedances across the entire Smith chart, 2<sup>nd</sup> harmonic impedances swept across the edge of the Smith chart and 3<sup>rd</sup> harmonic impedance set to open circuit.

Figure 3.8 shows the maximum output power exceeds 10 W (40 dBm) for all swept input powers and phases of 2<sup>nd</sup> harmonic impedances within the  $\alpha$  space (approximately between 80° to 280°). The device achieved its saturated output power (>15 W) at about 4

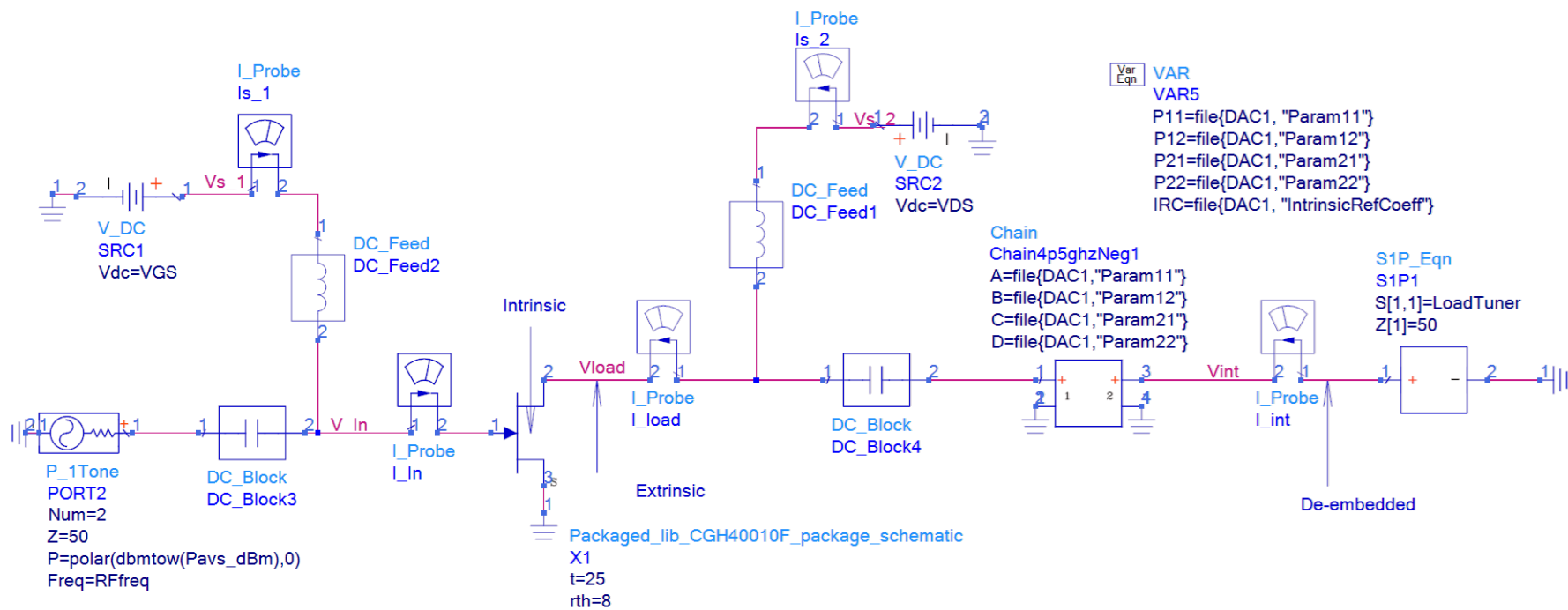


Figure 3.7. Schematic of ADS passive load-pull simulation.

dB gain compression for a source input power of 28 dBm. The changes of maximum output power with phase of 2<sup>nd</sup> harmonic impedances are minimum when the device is compressed and has reached its saturation point. The maximum DE shows symmetrical changes with the phase of the 2<sup>nd</sup> harmonic impedances around 180 °. Within the  $\alpha$  space, DE is highest at the boundaries and lowest for in the middle ( $\alpha = 0$ ) of the  $\alpha$  space. The overall variation of DE approaches 20 % and is in good agreement with the emulated data in Figure 3.6. Although maximum DE continue to increase outside the restricted  $\alpha$  spaces, the maximum Pout shows a steep drop indicating a restriction for 2nd harmonics impedances that can be utilised for the CCF mode.

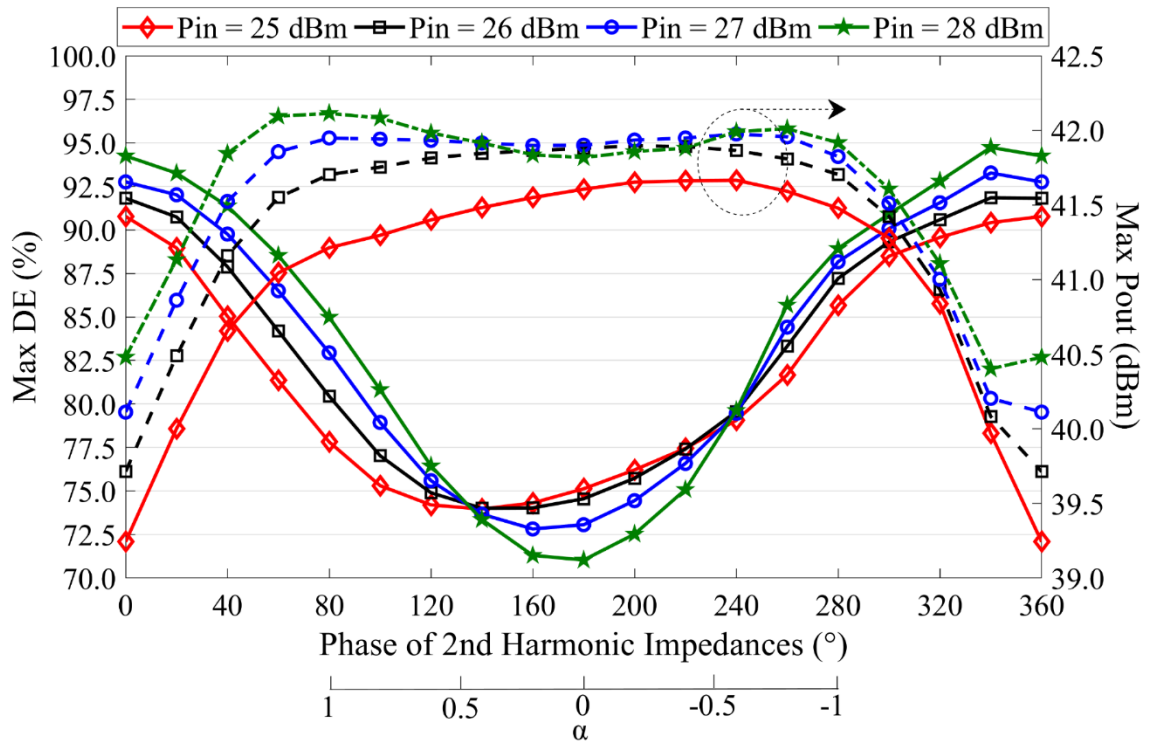


Figure 3.8. Peak DE and Pout from load-pull simulation on 10 W GaN device at CGP by varying phase of 2<sup>nd</sup> harmonic impedance along the edge of Smith chart.

### 3.4 Measurement of CCF Mode with Compression on 10 W GaN Device

The device is measured in a test fixture with an active load-pull system to confirm with the previous ADS simulation. The device is biased with 28 V and -2.85 V at the drain and gate respectively ( $I_{dq} = 13$  mA) through bias tees. CW signal from a signal generator with 50  $\Omega$  characteristic impedance at 2.0 GHz is connected to the device's input through a driver amplifier. The magnitude of the signal generator is varied from 9 dBm to 11 dBm. Two signal generators are connected to the device output through two separate driver amplifiers, to control the fundamental and 2<sup>nd</sup> harmonic impedances presented to the device package plane. Fundamental impedances are swept throughout the Smith chart while the 2<sup>nd</sup> harmonic impedances are controlled at the edge of Smith chart with different phases. Meanwhile the 3<sup>rd</sup> harmonic impedances are not controlled due to their small impact on the device performances [72]. All these impedances are presented and measured at the device's package plane within the test fixture using short, open, line and thru (SOLT) calibration [73]. Figure 3.9 shows the set-up for this active load-pull measurement.

Due to the package's parasitic effect on the transistor, the phases of 2<sup>nd</sup> harmonic impedances from the edge of the Smith chart that have to be presented at the package plane are shifted from the phases presented at the device's current generator plane, which were used in the previous simulation. These phases rotation representing  $\alpha$  space (-1, 0 and +1) at the device's current generator plane from the package plane are: 100 °, 200 ° and 165 ° respectively at 2.0 GHz, as depicted in Figure 3.10.

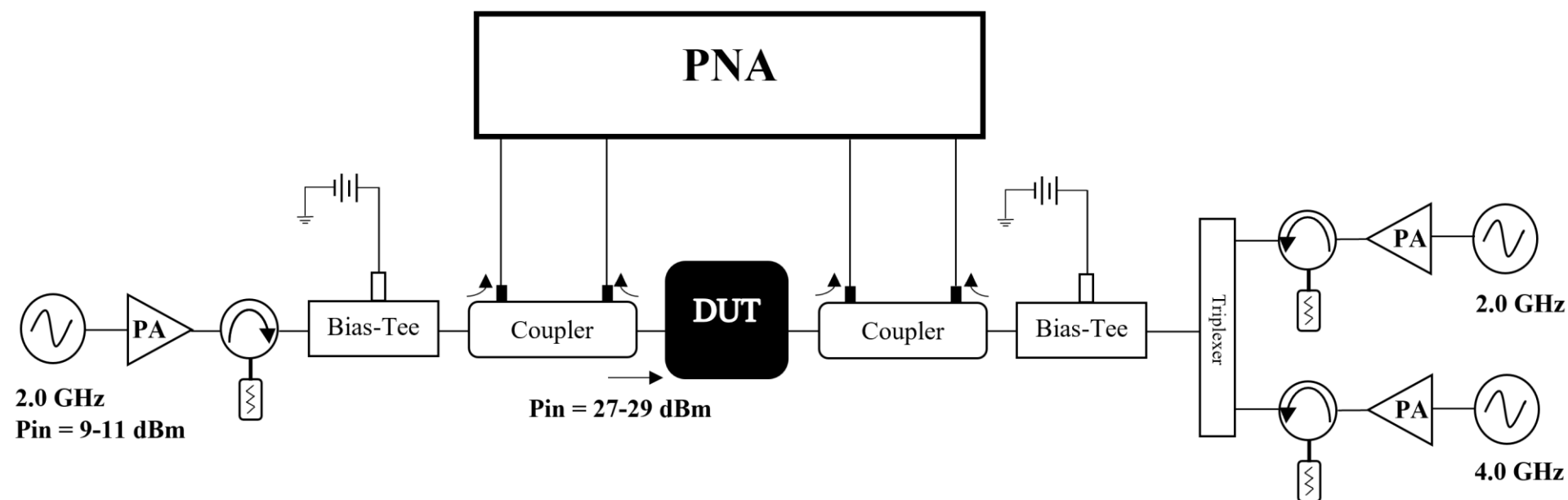


Figure 3.9. Schematic for active load-pull measurement set-up.



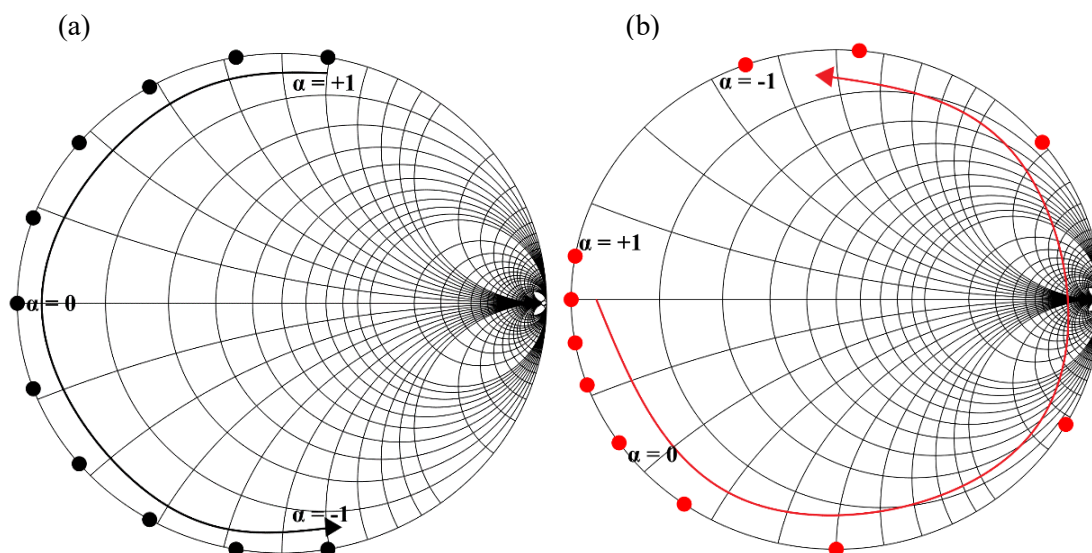


Figure 3.10. Simulated 2<sup>nd</sup> harmonic impedances presented at (a) the CGP and shifted to (b) package plane due to packaged parasitic effects.

Figure 3.11 shows the maximum DE obtained from each fundamental load-pull with 7 different phases of 2<sup>nd</sup> harmonic impedances chosen that are normalised to the  $\alpha$  space at 3 input drive levels. Maximum Pin = 11 dBm from signal generator provides up to 29 dBm to the device input after been amplified by the driver amplifier. Minimum DE are measured at  $\alpha$  close to 0 for all 3 input drives which varies from 57 % to 63.7 % with different input setting. The peak DE are measured at both ends of the  $\alpha$  range. The difference between max DE obtained at  $\alpha = -1$  and  $\alpha = 0$  for Pin=11 dBm is 23 %, which is slightly larger than the emulated and simulated data. Especially for  $\alpha = 0$  case, this difference between the measured peak DE and the simulated DE could be due to the lack of 3<sup>rd</sup> harmonic impedance control. Nevertheless, the variation of peak DE across  $\alpha$  is well match with the emulated results.

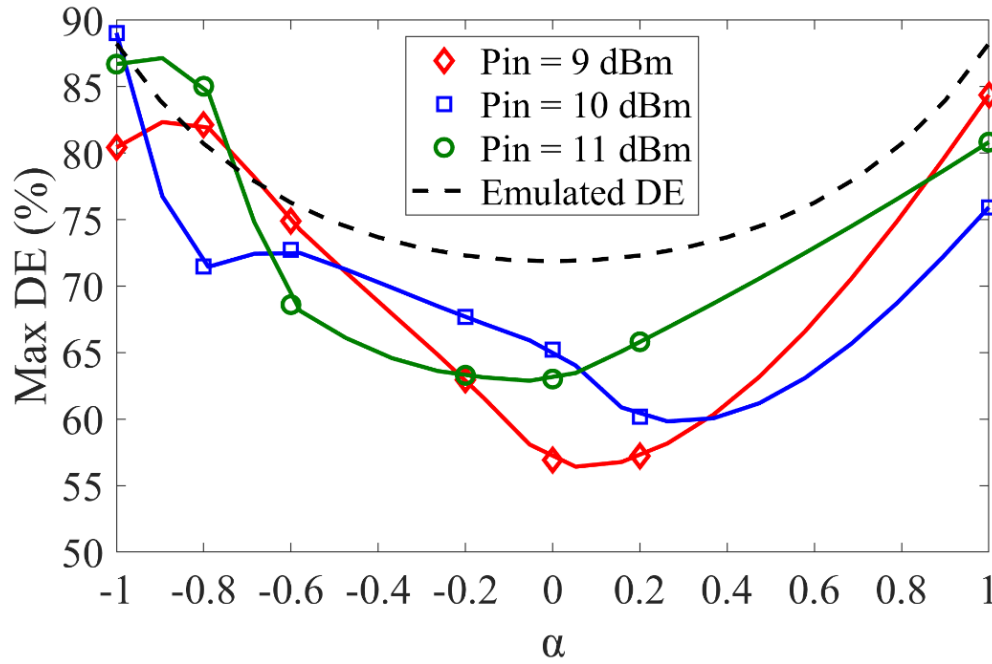


Figure 3.11. Measured and emulated peak DE from fundamental load-pull of 10 W packaged device with respect to  $\alpha$  space and  $P_{in}$  from signal generator.

### 3.5 Chapter Summary

This chapter has concluded, for the first time, the new performances of the CCF mode by including the I-V knee interaction on its waveforms. This new theoretical analysis has reformulated the ideal CCF mode waveforms to include the non-linearities from the knee boundary region, that result in drain current waveforms clipped by both voltage waveform and the knee voltage. When the device is operated with gain compression, the drain efficiencies are no longer constant across the  $\alpha$  space, instead, the peak efficiencies are reached at  $\alpha = -1/+1$ . This new CCF behaviour has been successfully simulated and measured through fundamental load-pull while varying the phase of 2<sup>nd</sup> harmonic impedance across the edge of Smith chart, showing a good agreement with the theoretical prediction. The difference of the peak DE measured at  $\alpha$  close to 0 from Figure 3.11 can be improved by additional 3<sup>rd</sup> harmonic control on the active load-pull measurement by presenting open circuit to the CGP.

# Chapter 4

## Broadband 10 W GaN PA Design Based on CCF Mode with Compression

### 4.1 Introduction

Chapter 3 introduced a reformulation of the CCF mode by introducing additional non-linear I-V knee interaction into the waveform theory. As the device is operated with compression, the knee interaction between the waveforms is unavoidable and must be taken into consideration. The drain efficiency is at the peak, only at the  $\alpha = \pm 1$ , and drops to the lowest value when  $\alpha = 0$ . Several publications have demonstrated the practicality of designing broadband PA using CCF mode by utilising the entire  $\alpha$  space for their broadband PA design [34, 74, 75, 76, 77, 78, 79, 80]. These broadband PAs, including other continuous PA modes in [81, 82, 83, 84, 85] are all measured at compression level, when the device is tested under CW excitation, meaning that the drain waveforms are operating within the knee boundary. The ideal performances of the CCF mode are no longer useful to evaluate the PA performances, when the realistic operation of the device is considered.

In this chapter, a broadband 10 W GaN PA is designed based on the CCF mode for broadband and high efficiency performance, by considering the symmetrical DE performances across the  $\alpha$  space described in the previous Chapter 3. Here, the phase rotation of 2<sup>nd</sup> harmonic impedances is restricted to lie along the edge of Smith chart within close range to  $\alpha = -1$  in order to keep the drain efficiency at the maximum. This chapter summarises as follows. Load-pull simulations with sweep 2<sup>nd</sup> harmonic impedances are performed on the 10 W GaN device model in ADS to obtain the  $\alpha$  design space, across the bandwidth. The PA is designed and fabricated with an optimised matching network that tracks with the fundamental and 2<sup>nd</sup> harmonics impedances optima across the targeted bandwidth (1.8 GHz to 2.7 GHz). The fabricated PA is tested with CW excitation and modulated signal to verify its performances. This chapter describes the final half of the published conference paper in International Microwave Symposium 2019 [71].

## 4.2 Load-pull Simulation

Fundamental load-pull simulation with swept phase of the 2<sup>nd</sup> harmonic impedances is performed at the package plane of 2<sup>nd</sup> generation 10 W device from Wolfspeed (CG2H40010) [86] using the available non-linear behaviour device model, to determine the optimum impedance throughout the design bandwidth for the PA. In this simulation, the 2<sup>nd</sup> harmonic impedance is fixed at a point at the edge of Smith chart, while fundamental impedances is swept across the entire Smith chart. This simulation is repeated by changing the phase of the 2<sup>nd</sup> harmonic impedance to cover along all the region of the edge of the Smith chart. The impedance matching network is always rotating in a clockwise direction with increasing frequency, as the Smith chart. This rotation has

to be taken into consideration when designing the broadband output matching network to keep the  $\alpha$  rotation close to -1 only across the bandwidth, between 1.8 GHz to 2.7 GHz. Figure 4.1 shows the peak DE and Pout obtained from fundamental load-pull while varying phase of the 2<sup>nd</sup> harmonic impedance across the edge of Smith chart at lower and upper design frequency, 1.8 GHz and 2.7 GHz. The variation of peak Pout and DE with phase of the 2<sup>nd</sup> harmonic impedance indicates the  $\alpha$  space at the device's package plane. The  $\alpha$  space (-1, 0 and 1) for 1.8 GHz and 2.7 GHz is approximately 120 °, 200 ° and 165 °, and 170 °, 240 ° and 210 ° respectively at the package plane.

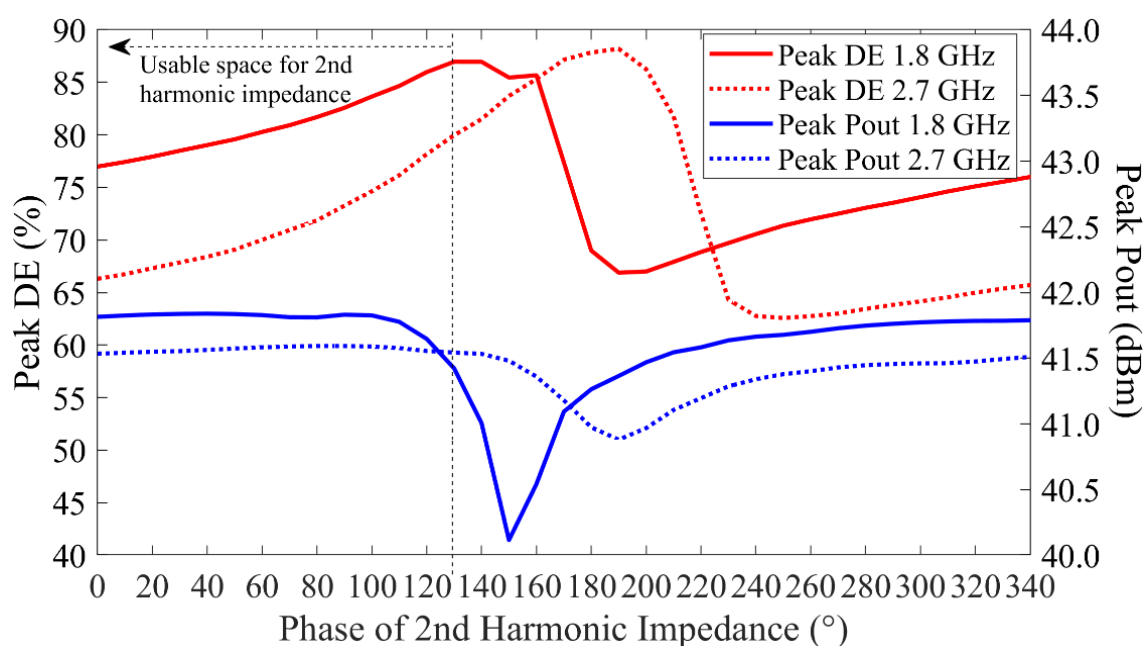


Figure 4.1. Peak Pout and DE from load-pull simulation of 10 W GaN device with sweep phase of 2nd harmonic impedance.

The results shown in Figure 4.1 indicates that the phase of 2<sup>nd</sup> harmonic for  $\alpha = -1$  rotates counter-clockwise on the Smith chart when the frequency increases from 1.8 GHz to 2.7 GHz (from 130 ° to 170 °). Therefore, the design space for the optimum phase of 2<sup>nd</sup> harmonic impedance for  $\alpha = -1$  has to start at 120 °, at 1.8GHz and it will rotate clockwise for higher frequency. Next, fundamental load-pull simulation is performed with fixed termination of 2<sup>nd</sup> harmonic impedance at selected frequency within the bandwidth: 1.8 GHz = 1  $\angle$  130 °, 2.2 GHz = 1  $\angle$  105 ° and 2.7 GHz = 1  $\angle$  80 °. The 3<sup>rd</sup> harmonic impedances are kept constant at open circuit across all frequencies. All these impedances are presented to the device's package plane during the load-pull simulation. Figure 4.2 shows the movements of Pout and DE contours (Pout = 40 dBm and DE = 70 %) across the 3 different frequencies. The Pout and DE contour show a larger area at 1.8 GHz because the setting for the 2<sup>nd</sup> harmonic impedance is at the optimum of  $\alpha = -1$ . On the other hand, the DE contours area becoming much smaller at higher frequencies because the 2<sup>nd</sup> harmonic impedance is not located at the optimum  $\alpha = -1$  region, as shown in Figure 4.1. This indicates the compromise that has to be considered when designing a broadband PA circuit. The area of Pout contour is reduced at 2.7 GHz because the peak Pout at this frequency dropped at the same gain compression shown in Figure 4.1. This is a well-known behaviour of a power transistor that has unstable performance over frequency [13, 18].

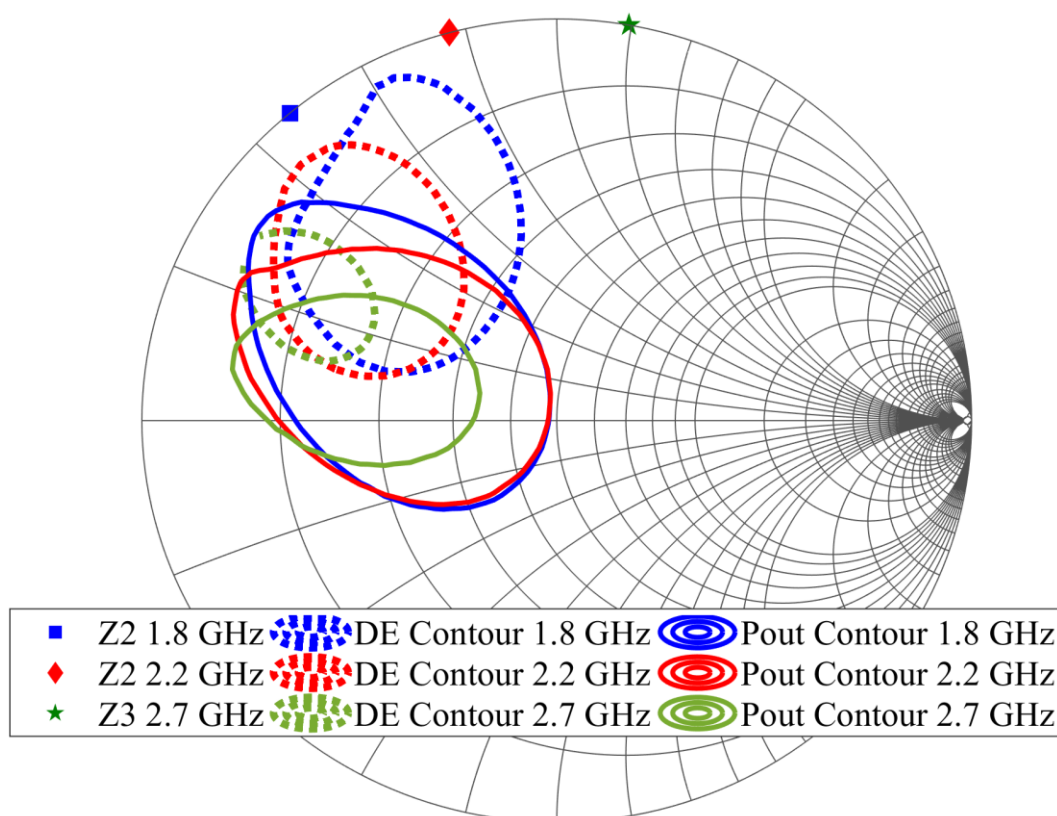


Figure 4.2. Simulated Pout contours (> 40 dBm) and DE contours (> 70 %) for different 2<sup>nd</sup> harmonic load impedances at 1.8 GHz, 2.2 GHz and 2.7 GHz.

### 4.3 Broadband Matching Network

The input matching network, IMN is designed as a bandpass filter to provide high gain for the PA across wide operating bandwidth. The IMN is designed, such that the fundamental impedances presented to the device's gate is the conjugate of the optimum impedances of the device input. The input 2<sup>nd</sup> harmonic impedances is not controlled for the design of IMN. A parallel RC circuit is placed in series between RF input to the device's gate to provide unconditional stability to the device [12, 18]. A high value resistor (10 k $\Omega$ ) is placed in series with the bias network to provide additional stability by preventing any significant current drawn by the device's gate. Figure 4.3 shows the circuit layout for the IMN, designed in ADS. Certain circuit components, such as DC

blocking capacitors and DC bypass capacitors are replaced with the available component model, provided by the manufacturer, to accurately simulate the circuit. These capacitors have their actual series resistance and inductance, that usually degrade the capacitor's performances over frequency.

The output matching network, OMN is designed by controlling the fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's package plane, to be close to a = -1. The OMN consists a series of different width and length microstrip lines, with additional open circuited stubs. A bias line is added with  $\lambda/4$  properties of the centre frequency of the design bandwidth to provide RF isolation to the DC bias. The 3<sup>rd</sup> harmonic impedances are not controlled by the OMN. Figure 4.4 shows the circuit layout of the OMN designed in ADS. All the components in the OMN is tuned and optimised so that the phase of the 2<sup>nd</sup> harmonic impedances presented to the device's package plane is between 120 ° - 80 ° (clockwise rotation) at 1.8 GHz to 2.7 GHz, while the fundamental impedances offer a trade-off between Pout and DE optima across the design bandwidth, as depicted in Figure 4.5.



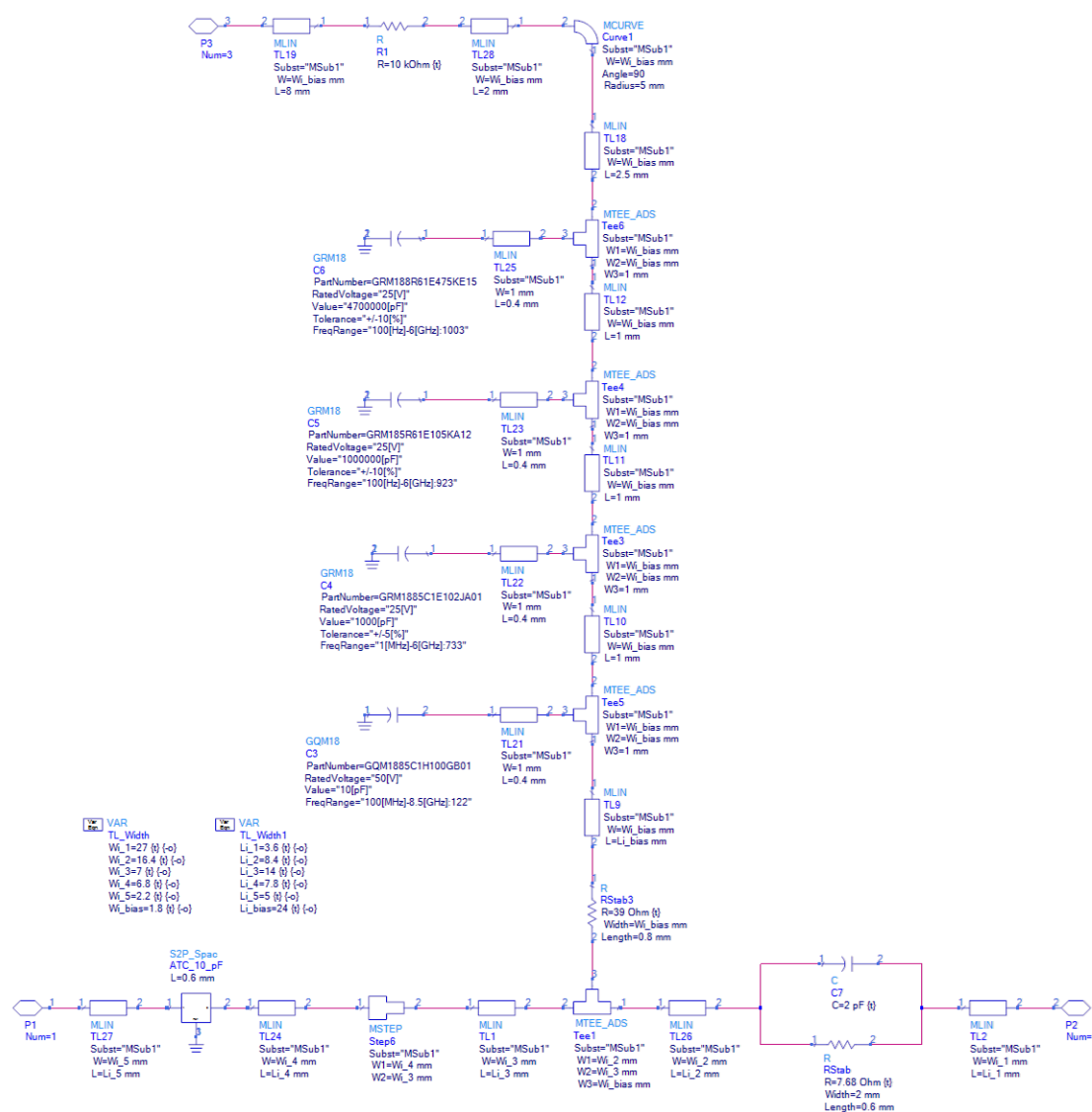


Figure 4.3. ADS circuit layout for the IMN.

The circuit layout is drawn in ADS's Momentum for full 2.5D EM simulation, enabling the computation for the magnetic coupling between the transmission lines. Figure 4.6 shows the entire circuit drawn in Momentum. Several input and output ports are defined, to create multiple ports S-parameter file from the EM simulation. The file is imported back into ADS circuit simulation, where the ports are connected to active and passive components for full RF PA circuit simulation. Due to the EM coupling between the circuit layout, several iterations are made in the circuit layout during the ADS EM simulation to ensure that the impedances of the circuit are almost the same as the initial circuit simulation.

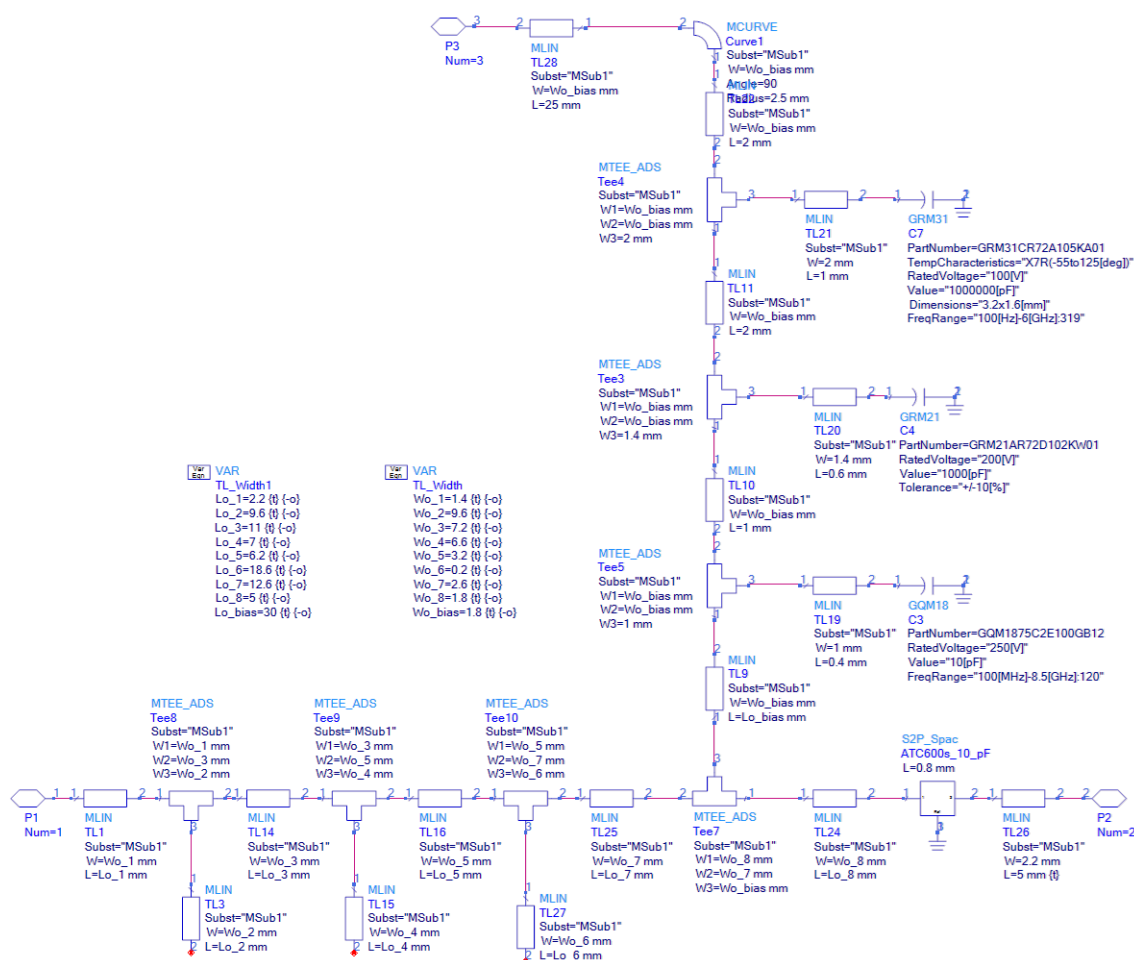


Figure 4.4. ADS circuit layout for the OMN.

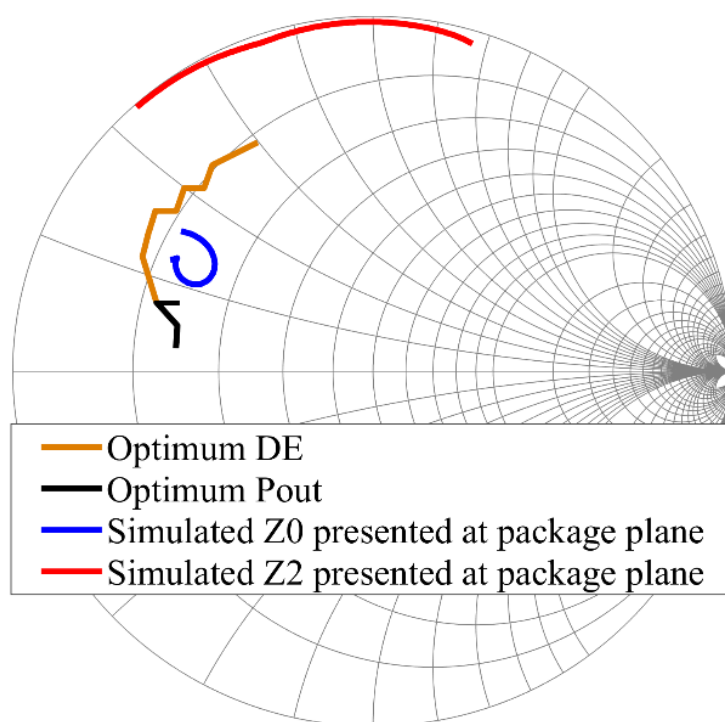


Figure 4.5. Simulated impedances presented to device's package plane.

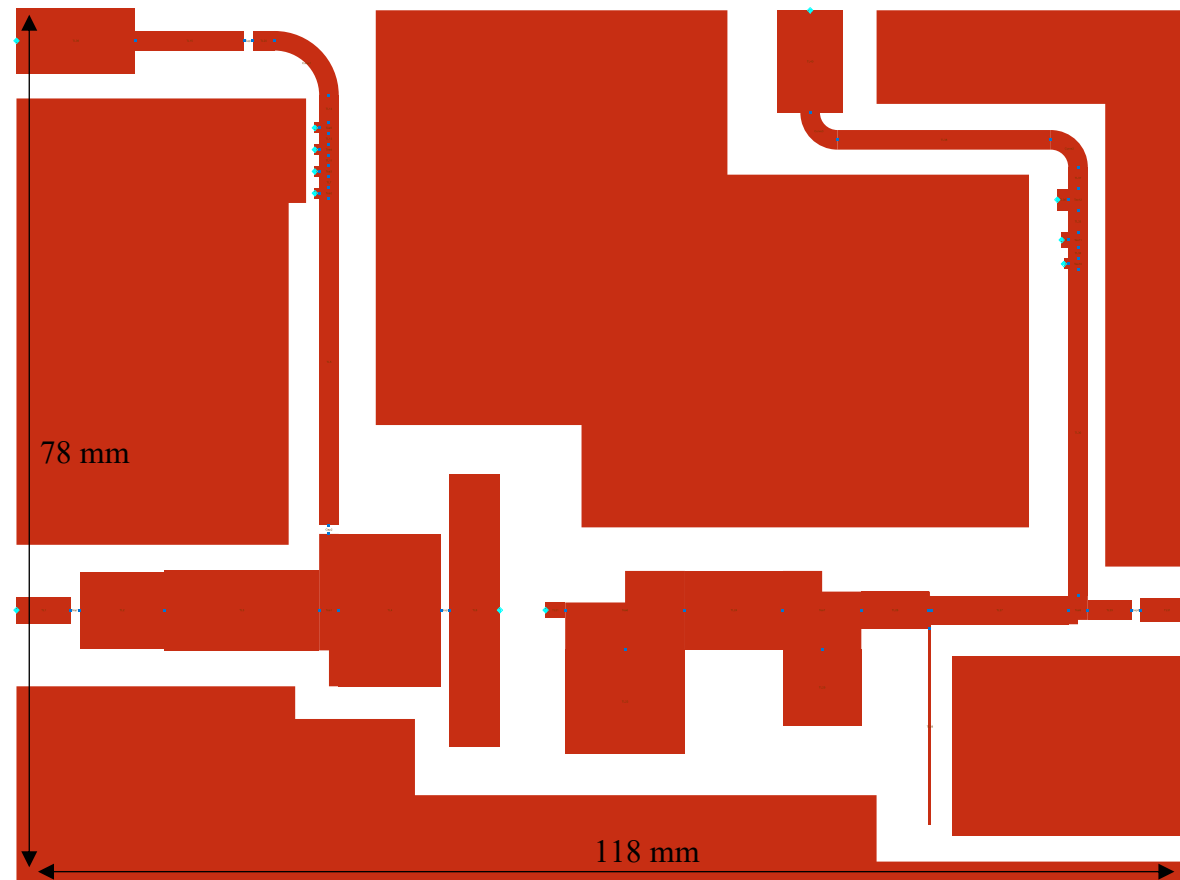


Figure 4.6. Final circuit layout in ADS Momentum.

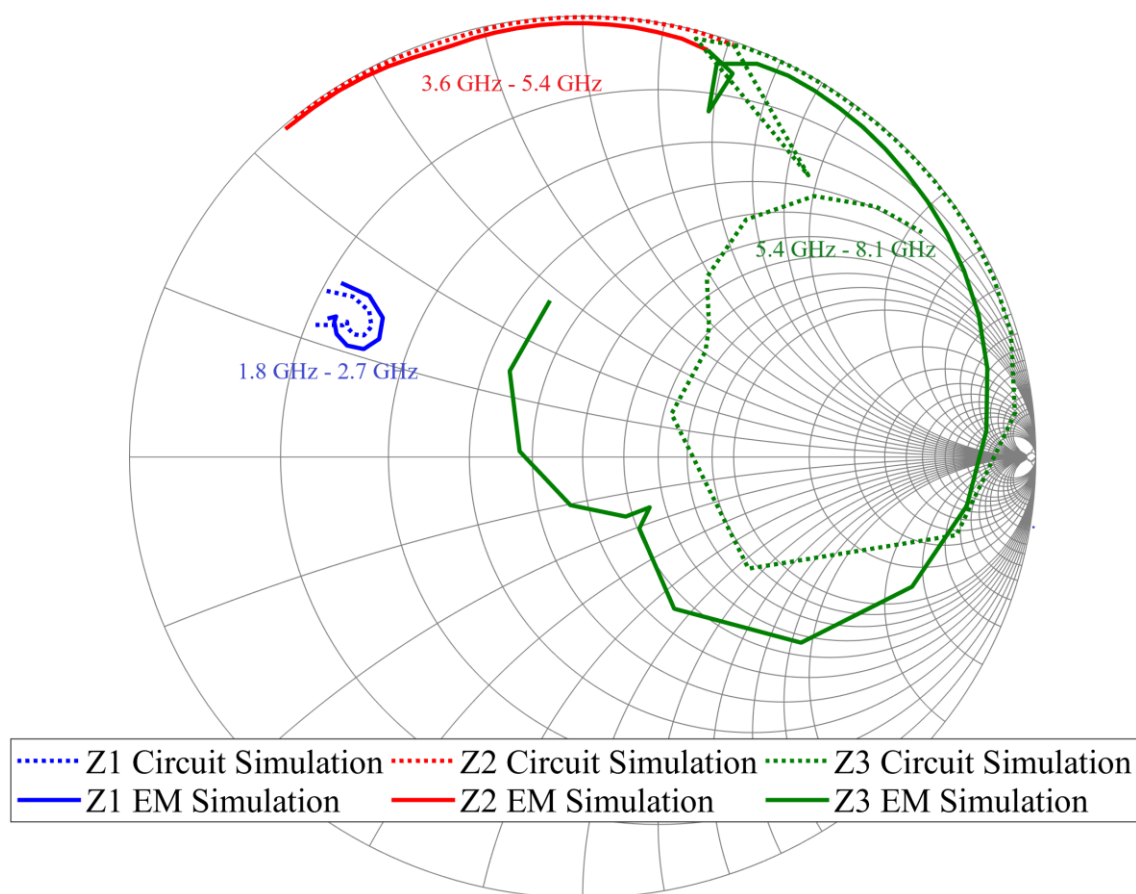


Figure 4.7. Simulated comparison of OMN impedances presented to the device's plane between ideal ADS circuit simulation and 2D Momentum.

Figure 4.7 shows the comparison of impedances presented to the device's output between the ADS circuit and EM Momentum simulations. The fundamental and 2<sup>nd</sup> harmonic impedances are well matched between the circuit and EM simulation. However, the 3<sup>rd</sup> harmonics impedances shows bigger resonance especially at the higher frequencies.

Figure 4.8 shows the fabricated of the prototype broadband 10 W GaN PA. The microstrip line is fabricated from RT/Duroids 5870 laminates, with dielectric constant of 2.33, and 0.79 mm thickness. The dielectric has dual copper cladding, with 30um thickness on each side. The circuit board is mounted on aluminium board for grounding and heat sinking and is fixed with m2.5 screws. A cut out was made on both aluminium

and circuit board for the 10W packaged transistor fixtures. During the measurement, the PA unit was mounted on a heat sink with a fan attached for cooling purpose.

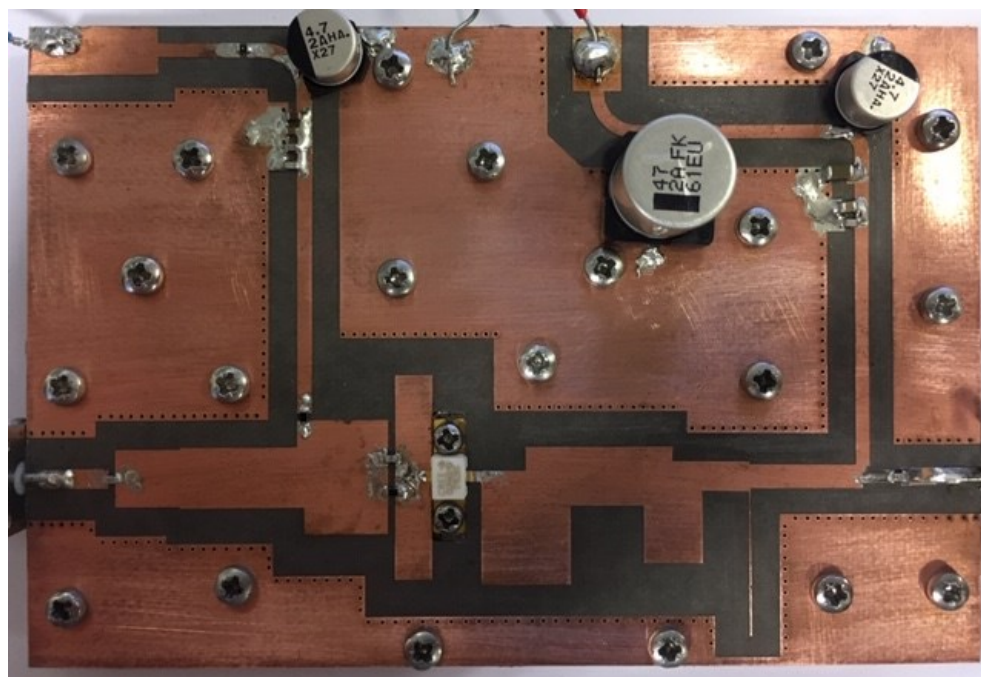


Figure 4.8. Fabricated broadband 10 W GaN PA.

## 4.4 CW Measurement

Prior to large signal CW test, the PA is tested for the small signal gain across bandwidth. This measurement is also significant to determine the stability for the PA. Here, the PA is biased with 28 V and -3.05 V at the drain and gate respectively, drawing 10mA current. An Agilent Fieldfox N9912 instrument is used for the small signal measurement of the RF PA. The input and output SMA ports of the PA is calibrated using a short, open, load and thru (SOLT) calibrations procedures. The first small signal measurement from the initial design indicates that the small signal gain is significantly lower than the expected simulation result, as shown in Figure 4.9. There's also a stability issue accompanied when biasing the device, where the quiescent current drawn by the device is fluctuated. The 2 pF capacitor from the parallel RC circuit of the IMN in Figure 4.3 is tuned and replaced with 5pF capacitor which eventually brings up the small signal

gain as expected. However, the measured new small signal gain is not flat across the bandwidth, with 23 % increases at the lower end frequency. Nevertheless, a simple tuning on the IMN was able to recover the lower gain, as shown in Figure 4.9, and finally provides unconditional stability to the PA. The quiescent current drawn by the PA is stable.

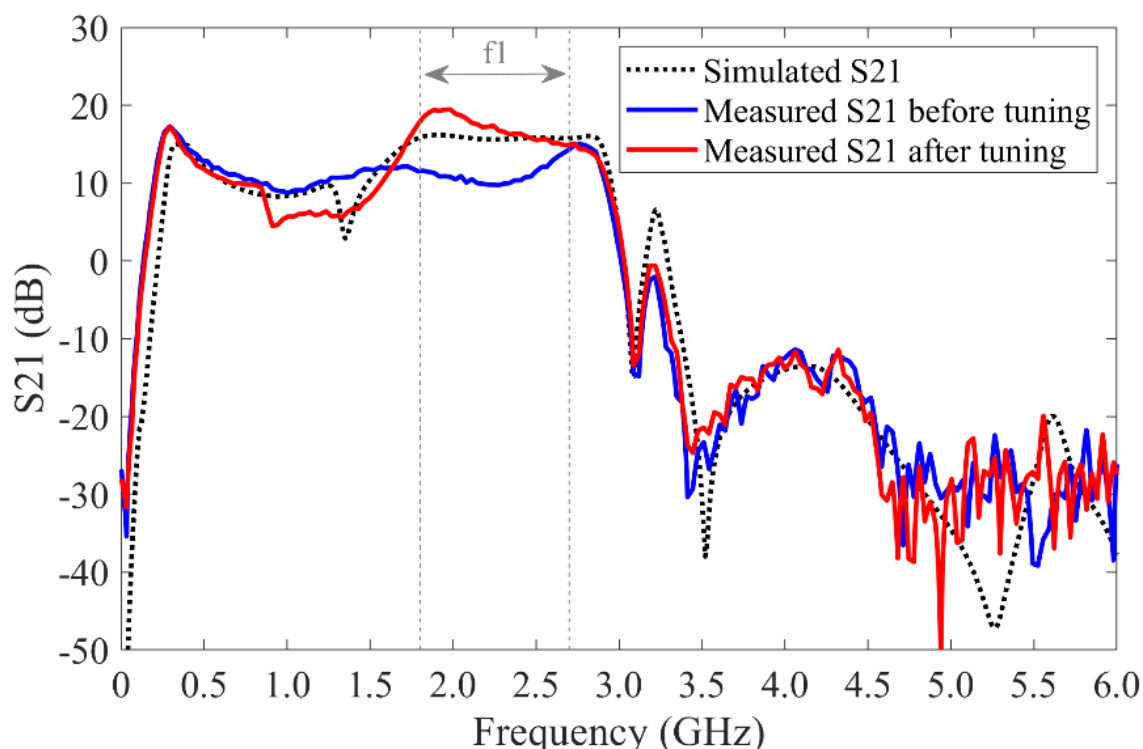


Figure 4.9. Simulated and measured gain (S21).

Next, a large signal CW measurement is performed on the 10 W PA with similar bias setting. Figure 4.10 shows the measured peak performances obtained between 1.7 GHz to 2.8 GHz (48.9 % bandwidth), contrasting with simulated data, for a maximum of 3dB output gain compression. In this measurement, further 200 MHz bandwidth was extended from the original target frequency of the PA design in ADS. A minimum of 8.3 W was measured at 2.8 GHz, peaking at 18.3 W at 1.8 GHz. The DE ranges between 64.3 % (2.8 GHz) to 83.4 % (1.8 GHz). The gain, however, drops from 18 dB to 10.4 dB as

the frequency increases, due to the uneven small signal gain measured previously. In general, the average DE, Pout and gain is 72.1 %, 14.1 W and 14.5 dB, respectively, measured between 1.7 GHz to 2.7 GHz (45.45 % bandwidth) as reported in [71].

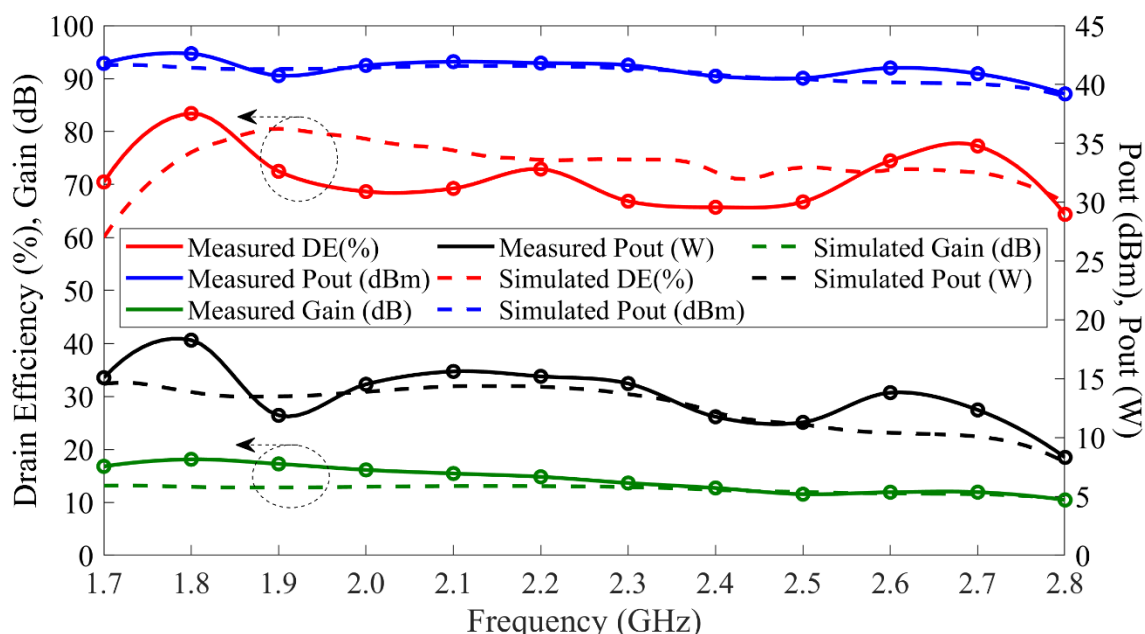


Figure 4.10. Measured and simulated performances of broadband 10 W PA with CW signal.

Figure 4.11 shows the DE vs Pout relationship when a sweep input CW signal is measured on the RF PA between 1.8 GHz to 2.8 GHz, at interval of 0.2 GHz. Due to gain and Pout drop of the PA, the DE reaches it saturation at lower Pout. At 1.8 GHz measurement, the DE is 33.2 % at -8 dB output back-off.

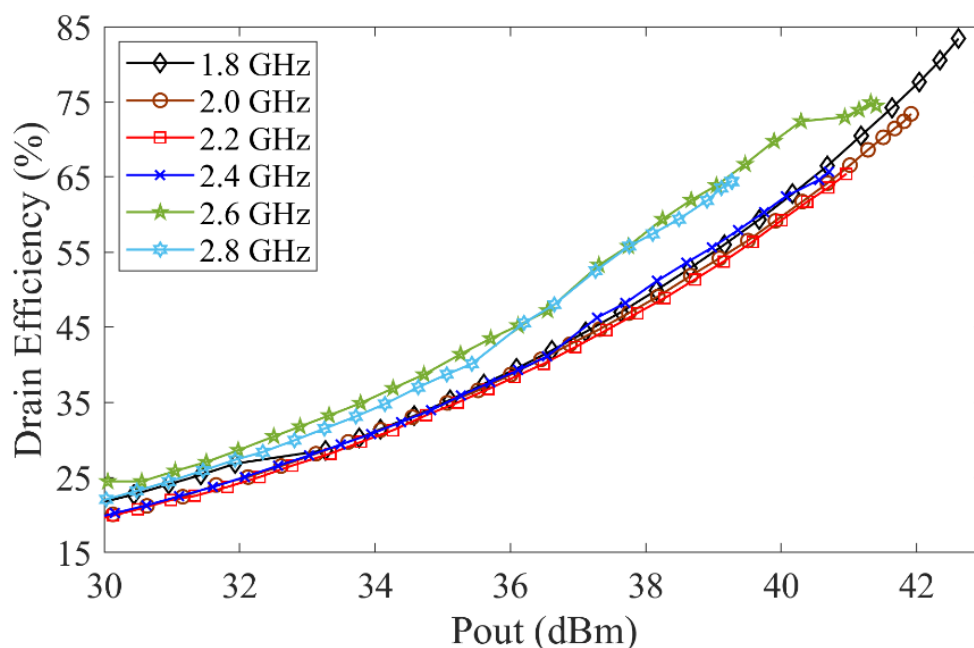


Figure 4.11. Measured DE vs Pout across bandwidth.

To verify the operational modes for this PA, the load-line and impedances presented to the device's current generator plane (CGP) are simulated using the available device model which has internal current and voltage nodes. Figure 4.12 shows the fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's CGP, in which both impedances are within the  $\alpha = -1$  space between 1.8 GHz to 2.7 GHz. The fundamental impedances rotate on the inductive region of the Smith chart, that is in between the optimum Pout and DE impedances, while the 2<sup>nd</sup> harmonic impedances have a strict rotation, cover between  $-53^\circ$  to  $131^\circ$  (clockwise) at the edge of Smith chart across the bandwidth. The intrinsic load-lines at CGP are shown in Figure 4.13, where the load-line for 1.8 GHz is closely similar to load-line of CCF mode for  $\alpha = -1$ . The peak drain voltage reduces as the frequency increases due to  $\alpha$  rotation approaching 0. The load-lines also show that it operated in-line with the knee-boundary from the DCIV characteristic of the device.



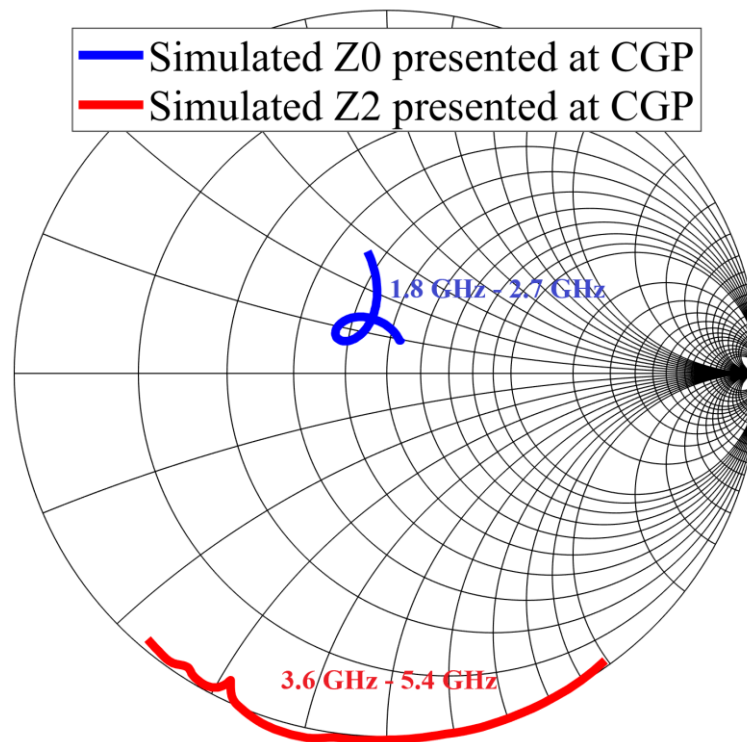


Figure 4.12. Simulated fundamental and 2nd harmonic impedances presented to the device's CGP.

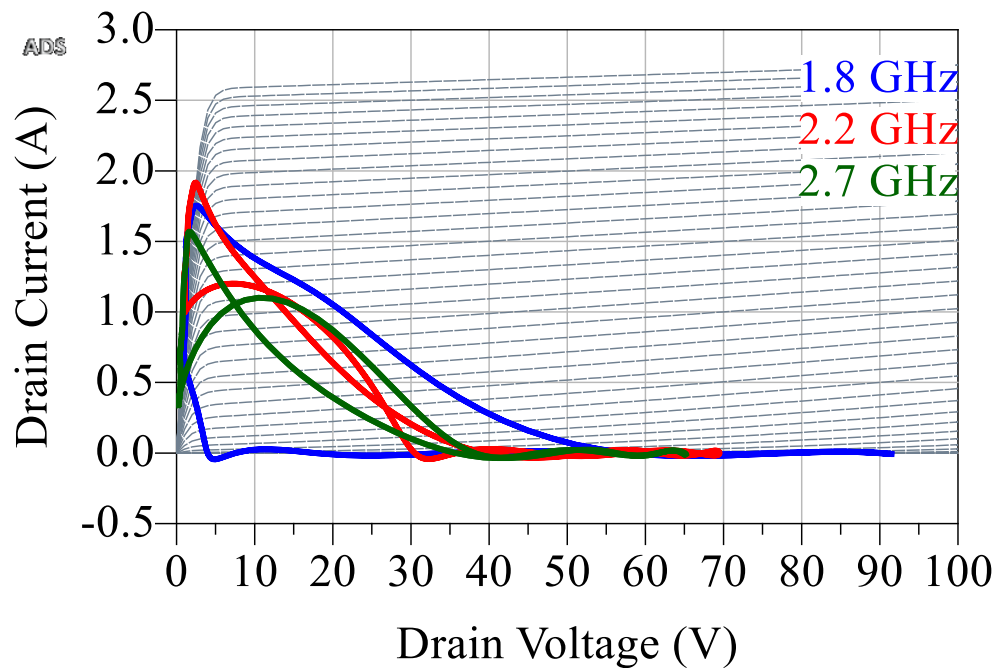


Figure 4.13. Simulated load-lines from 10 W PA at 1.8 GHz, 2.2 GHz and 2.7 GHz.

## 4.5 Modulated Signal Test

Next, the applicability of the PA in communication system is tested by applying single channel, 10 MHz LTE signal with 7.6 dB as peak-to-average-ratio (PAPR). The linearity of the PA is tested across the design bandwidth by applying the LTE signal, centred at 2.0 GHz, 2.5 GHz and 2.7 GHz. A DPD system is used to test linearisability and improve the linearity of the PA. The memory based DPD system is applied from National Instrument (NI) PXi based characterisation system [87]. Figure 4.14 shows the normalised output spectra of the PA, before and after DPD linearisation. The peak  $P_{out}$  obtained from the output spectra is above 10 W, with average between 32.3 dBm to 33.8 dBm, for all frequencies after DPD is applied. The ACLR before DPD is applied ranges between -33.5 dBc to -40.4 dBc, indicating that the PA still exhibit good raw linearity even when it is drive up to 10 W at the peak. The ACLR has reduced to between -52.2 dBc to -55.8 dBc after DPD for all 3 frequencies. Table 4.1 summarises the performances for this PA from the modulated signals measurements. Figure 4.15 and Figure 4.16 show the AM/AM and AM/PM responses before and after DPD is applied, measured at 2.0 GHz and 2.7 GHz centre frequency respectively. Both figures indicate that the DPD system able to correct the gain and phase variations when the PA is drive to compression.

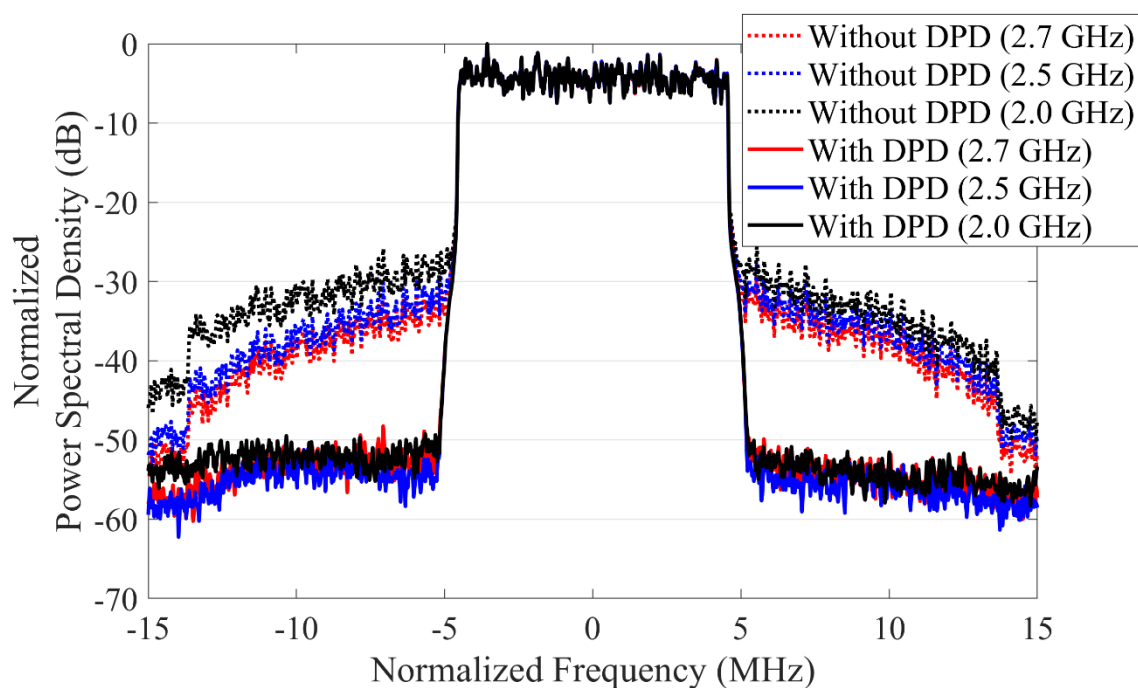


Figure 4.14. Measured output spectra of the PA tested under 10 MHz LTE signal, before and after DPD.

Table 4.1. PA performances under modulated signal before and after DPD is applied.

Centre Frequency	2.0 GHz	2.5 GHz	2.7 GHz
ACLR (L/H) before DPD, dBc	-33.5/-35.8	-38.6/-38.1	-40.4/-39.5
ACLR (L/H) after DPD, dBc	-52.2/-54.1	-54.8/-55.8	-53.6/-54.5
Average Power after DPD, dBm	32.3	32.5	33.8
Peak Power after DPD, dBm	39.9	40.1	41.2

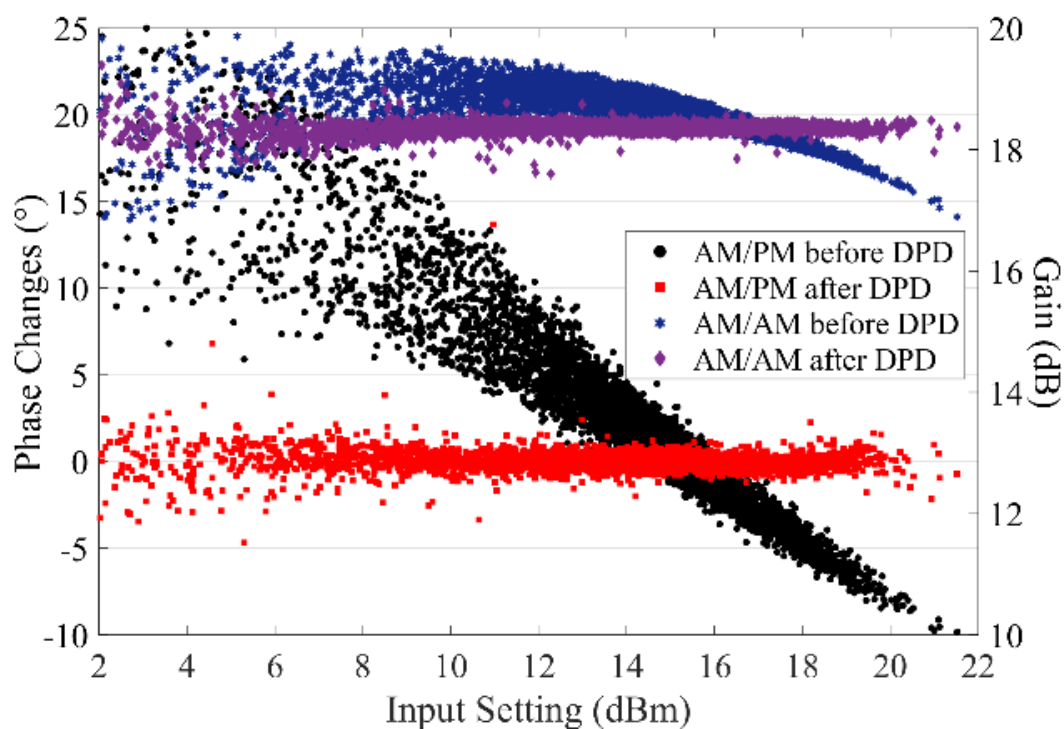


Figure 4.15. AM/AM and AM/PM measured with 10 MHz LTE signal with centre frequency at 2.0 GHz.

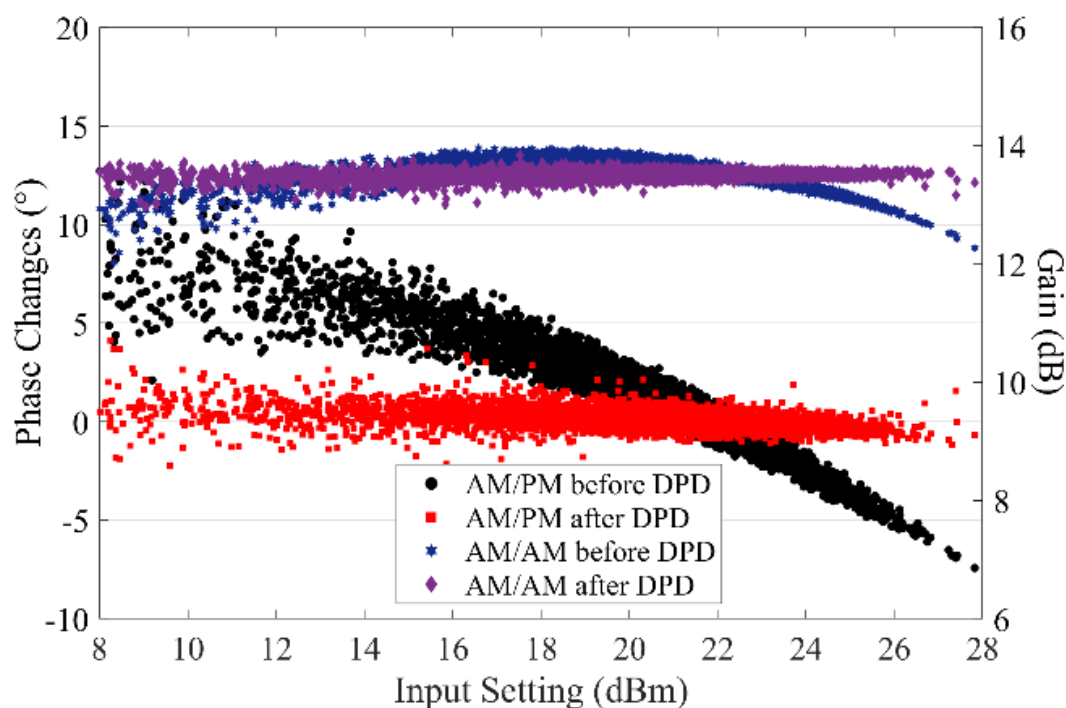


Figure 4.16. AM/AM and AM/PM measured with 10 MHz LTE signal with centre frequency at 2.7 GHz.

## 4.6 Chapter Summary

A broadband 10 W GaN PA has been realised by restricting the phase of 2<sup>nd</sup> harmonic rotation around  $\alpha = -1$  across bandwidth to keep the efficiency high. Up to 83.4 % DE is measured from the PA with average of 71.7 % while the output power ranges between 11.3 W to 18.4 W across 1.7 GHz to 2.7 GHz under CW measurements. A CW measurement was also performed at 2.8 GHz, showing relatively good DE of 64.3 %, although the output power is at the lowest across the bandwidth (8.4 W). The PAs designed in [74, 75, 76, 81], shows the prior art of broadband designs that have similar restricted 2<sup>nd</sup> harmonic phase rotation, however, there are no explanation to particular restriction. Similar design strategy has been implemented through optimisation process rather than appropriate fundamental waveform theory. The gain compression for the PA in this paper is kept at 3 dB maximum, whereas no information is available in all of the references in Table 4.2 regarding the gain compression of the PAs for their CW measurements. The linearity of this PA has been measured using 7.6 dB PAPR, 10 MHz LTE signal and the ACPR has been reduced between -52.2 dBc to -55.8 dBc for carrier frequency of 2.0 GHz, 2.5 GHz and 2.7 GHz. The realised PA exhibits relatively high raw linearity of around -40dBc at 2.7 GHz. Therefore, the utilised DPD system was able to improve it only by about -14 dB to -54.6 dBc. For all these frequencies, the maximum Pout ranges between 39.9 dBm to 41.2 dBm.

Table 4.2. State-of-art comparison for continuous PA modes.

<b>Ref</b>	<b>Bandwidth (GHz)</b>	<b>Pout (W)</b>	<b>DE (%)</b>	<b>Gain (dB)</b>	<b>Gain Comp.</b>	<b>RFPA Class</b>
[34]	0.55 - 1.1 (66.7%)	8.5 - 13.2	65-80	9.5 - 12	NA	CCF
[74]	1.45 - 2.45 (51.3%)	11 - 16.8	70-81	10 -12.6	NA	CCF
[75]	1.3 - 3.3 (86.9%)	10 - 11	60-83	10 - 13	NA	CCF/ CCF <sup>-1</sup>
[76]	1.6 - 2.7 (51%)	10.2 - 17.8	70.3-81.9	11.9 - 15.2	NA	CCF
[81]	1.3 - 2.4 (59.5%)	10.2 - 13.2	62.3-72	11.4 - 14.3	NA	Cont. Class - B/J
<b>This work [71]</b>	<b>1.7 - 2.7 (45.5%)</b>	<b>11.3 - 18.4</b>	<b>65.7-83.4</b>	<b>11.5 - 18.1</b>	<b>3dB max</b>	<b>CCF</b>

# Chapter 5

## Generating Power and Efficiency Contours for CCF Mode with Non-linear I-V Knee

### 5.1 Introduction

The previous work in chapter 3 has introduced a more realistic I-V knee scaling for the CCF mode by integrating the soft turn-on knee region into the waveform theory, giving a better understanding and prediction of the device behaviour when it is operated under compression. This chapter extends this by accounting for the realistic interaction between the knee region of the device and the output waveforms to generate both  $P_{out}$  and DE contours and, subsequently, to predict the efficiency at OPBO impedances for CCF mode. The contours are generated through load-pull emulation, that is entirely based on the MATLAB calculation. The optimum fundamental impedances for CCF mode, based on the ideal waveforms, can only be predicted at single impedances for unique  $\alpha$  values [32, 33, 88]. In recent publications, it has been shown that the transistor

operated in different modes has 2 optima; power and efficiency [17, 70, 89]. The separation between Pout and DE contours is beneficial for load-modulated PA architectures such as the outphasing PA [44, 45, 90, 91]. The original load pull prediction was proposed using Cripps load-line theory in [12, 92]. A dynamic load-line theory is used to predict power contours in this theory, however, due to the constant knee voltage used, this theory provides poor prediction for efficiency contours [17].

This chapter follows the original load-pull emulation for generating power and efficiency contours from [17, 70] that were used for class-B and class-B/J, by extending for CCF mode, for the first time. This method is analysed as linear load-line model. Due to poor prediction of optimum DE performances across the  $\alpha$  range obtained through this method compared to the performances predicted in Chapter 3, a further modification is made in the emulation by also incorporating the non-linear scaling of the current waveform as introduced in the previous Chapter 3. This new method is analysed as non-linear load-line model. A comparison is made between these two load-pull emulation approaches by comparing the peak Pout, DE and DE at 8 dB OPBO across  $\alpha$  range of the CCF mode. The verifications for this theory are performed through a 10 W GaN HEMT load-pull simulation and measurement. Finally, a load-pull measurement is performed on the PA fabricated from the previous Chapter 4 to verify the practicality of the theory with an actual PA circuit.



## 5.2 Linear Load-line Model on CCF Mode

An evaluation based on Pedro's load-line method [17, 70] is expanded here to generate power and efficiency contours for a CCF mode, for the first time. This method includes the soft turn-on knee region of the device to extend the original load-pull method proposed using Cripps load-line theory [12, 92], that predicts the optimum output power impedance but provides poor estimation of the optimum efficiency impedance. Instead of zero knee voltage in the original ideal CCF mode definition, the drain voltage waveform equation (5.1) is modified to estimate the drain voltage behaviour within the knee region. For plotting the current and voltage waveforms, typical quiescent bias values of a 10 W GaN Wolfspeed packaged device, CGH40010F [16], are utilised with the  $V_{dc}$  and  $I_{max}$  values of 28 V and 2.33 A, respectively. The knee voltage from the device is approximately 8V for  $V_{gs} = 0$  V and  $V_{ds} = 28$  V, which is used in this evaluation. The minimum value of drain voltage waveform in (5.1) is equal to  $V_{knee}$  when all the known values are inserted into the equation.

$$V_{ds,new}(\theta) = \left( V_{dc} - \frac{V_{knee}}{2} \right) * \left( 1 - \alpha \cos\theta + \frac{231}{200} \sin\theta - \frac{539}{800} \alpha \sin 2\theta + \frac{77}{400} \sin 3\theta - \frac{77}{800} \alpha \sin 4\theta \right) + V_{knee} \quad (5.1)$$

To generate power and efficiency contours using this linear I-V knee model, fundamental load-pull emulation is performed in MATLAB by choosing one value of  $\alpha$  within its range and varying the magnitude and phase of the fundamental component of the voltage waveform in (5.1). The fundamental component of the voltage waveform is extracted through a fast Fourier transform (FFT) and its magnitude and phase is manipulated. The new fundamental components are inserted back into the remaining DC and harmonic components of the voltage waveform, creating arrays of voltage

waveforms. These new voltage waveforms have different shapes due to variation of fundamental component. For each of the voltage waveforms generated, the half rectified sinusoidal drain current waveform is calculated with respect to the minimum of the drain voltage waveforms. These changes apply to the maximum current,  $I_{max}$ , that depends on the minimum of voltage waveforms,  $V_{min}$ , as defined in (5.2). These procedures generate current waveforms with respect to the fundamentally perturbed voltage waveforms.

$$I_{ds,new}(\theta) = \frac{I_{max,new}}{2} * \left( \frac{2}{\pi} \pm \sin\theta - \frac{4}{\pi} * \sum_{r=1}^{11} \frac{\cos(2r\theta)}{(2r)^2 - 1} \right) + Idq \quad (5.2a)$$

$$I_{max,new} = \begin{cases} \frac{I_{max}}{V_{knee}} * V_{min}; & \text{if } V_{min} \leq V_{knee} \\ I_{max}; & \text{if } V_{min} > V_{knee} \end{cases} \quad (5.2b)$$

Fundamental impedances, Pout and DE are calculated by performing FFT on each new voltage waveform and its subsequent current waveform, enabling the generation of Pout and DE contours. These procedures are repeated again for different value of  $\alpha$  from the voltage waveform in (5.1). Figure 5.1 and Figure 5.2 show the resulting Pout and DE contours from the load-pull emulation on CCF mode for  $\alpha = 0$  and  $\alpha = +1/-1$  respectively. The Pout contours are in 2 dBm steps while the DE contours are in 10 % steps. Two separate optima are obtained for peak Pout and peak DE. The evaluated peak Pout reaches 42 dBm while peak DE is up to 74 % for all  $\alpha$  cases. Interestingly, the achieved separation between the two optimum impedances are relatively constant for different  $\alpha$  values which does not match well with the load-pull data of the actual device.

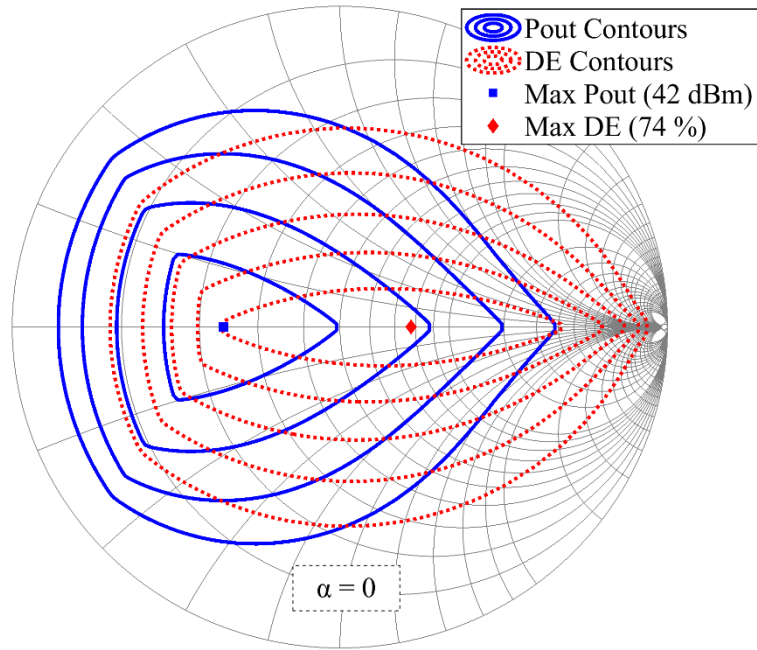


Figure 5.1. Emulated Pout and DE contours from linear knee model of CCF mode for  $\alpha = 0$ .

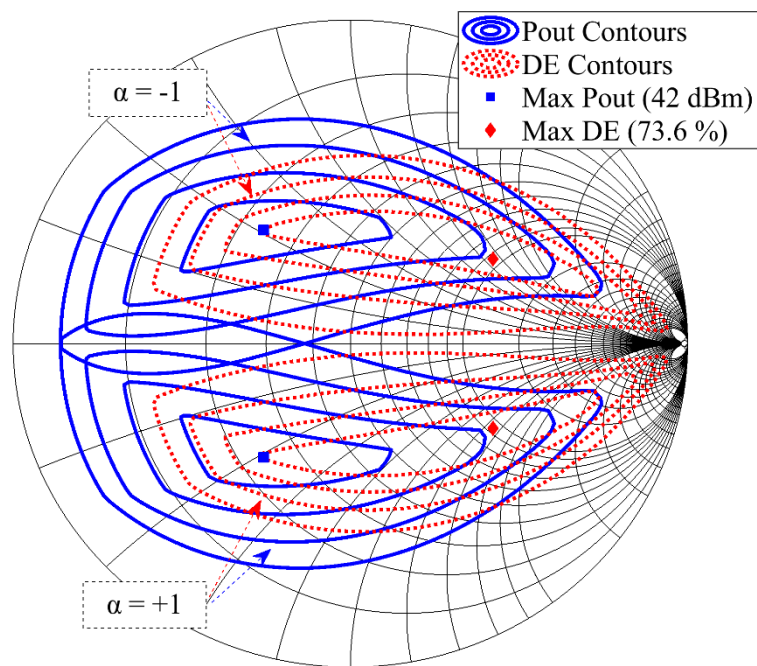


Figure 5.2. Emulated Pout and DE contours from linear knee model of CCF mode for  $\alpha = -1$  and  $\alpha = +1$ .

Figure 5.3 shows all the drain current and voltage waveforms generated from the load-pull emulation for  $\alpha = 0$ . The magnitude of current waveforms reduces as the voltage waveform expands into the knee region. However, the shape of the current waveform

remains to be a perfect half-rectified sinusoidal. The optimum Pout and DE waveforms from the load-pull emulation for  $\alpha = 0$  from the real impedance axis are highlighted in Figure 5.3. At optimum Pout impedance, the drain voltage waveform has a minimum value equal to the knee voltage, while the drain current waveform is at the maximum swing. Meanwhile, the voltage waveform is expanded into the knee region and the magnitude of the current waveform reduced less than half from its maximum swing at optimum DE impedance. The load-lines for waveforms in Figure 5.3 are shown in Figure 5.4, showing it's dynamic movement along the knee boundary.

The efficiency at output power back-off, OPBO, is predicted by plotting DE vs Pout for each  $\alpha$  case. Figure 5.5 shows the trajectory of the interpolated maximum DE across Pout normalised to its maximum value. For this research, 8dB OPBO is chosen with respect to the high PAPR for the most current modulated signal used in communication system. Peak DE at 8dB OPBO for  $\alpha = 0$  is predicted at 65 %.

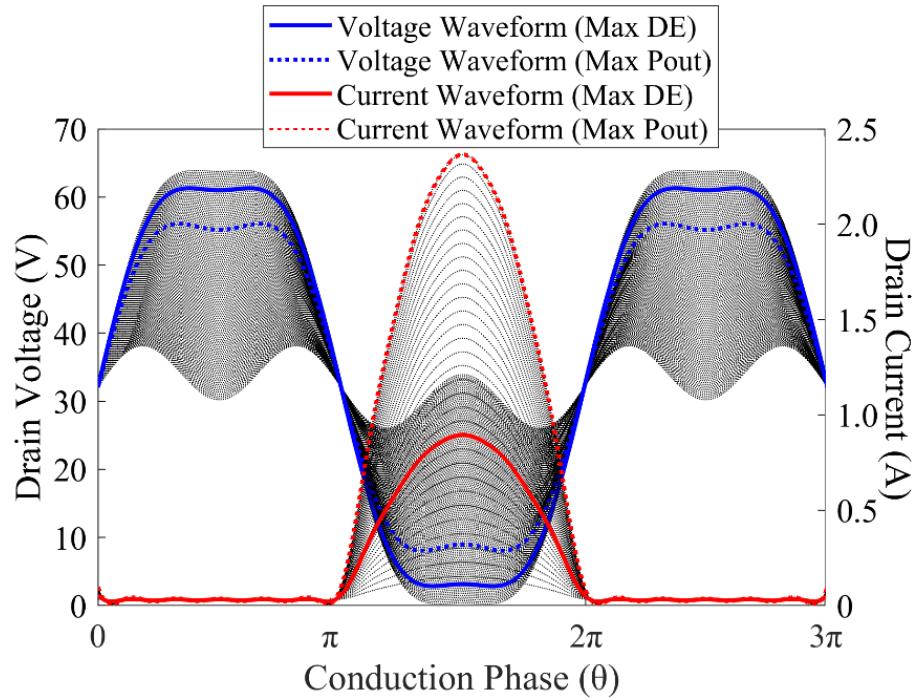


Figure 5.3. Drain current and voltage waveforms from load-pull emulation of linear knee model of CCF mode for  $\alpha = 0$ .

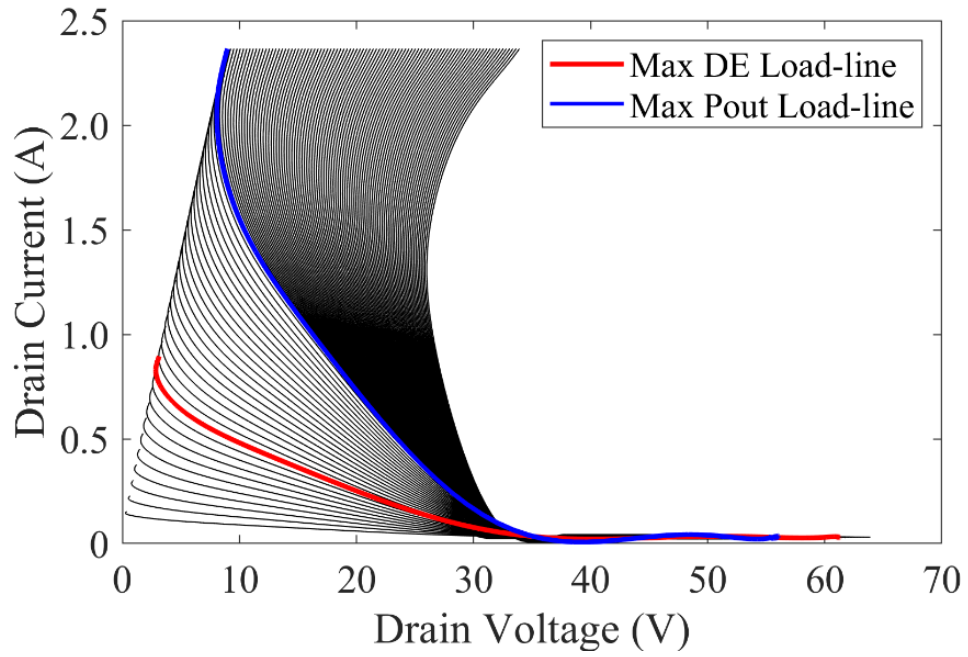


Figure 5.4. Load-lines for optimum DE and Pout from load-pull emulation of CCF model for  $\alpha = 0$ .

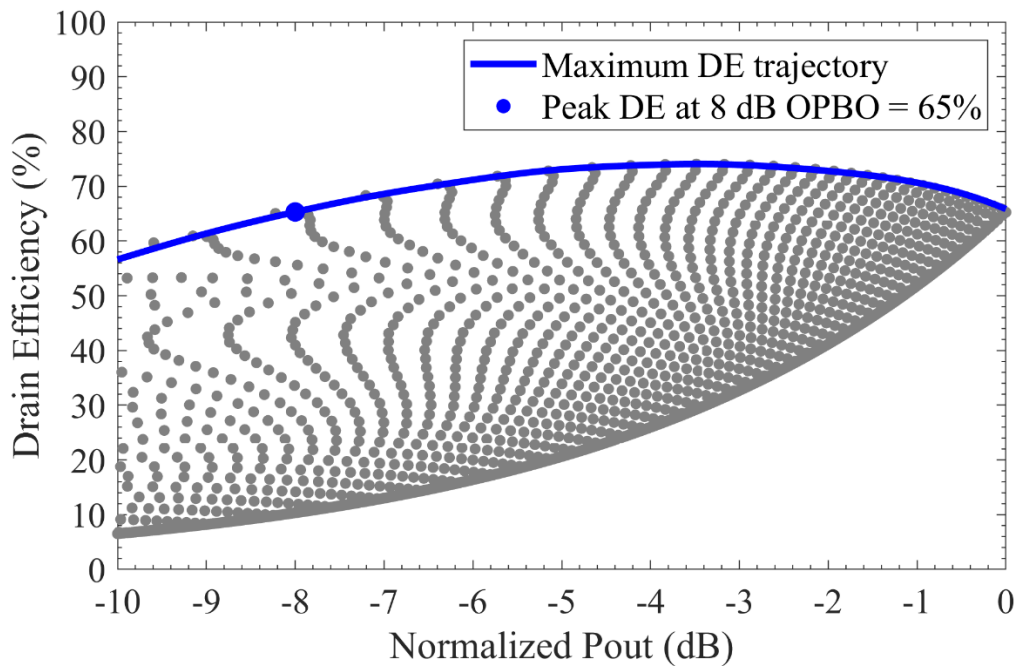


Figure 5.5. DE vs Pout fundamental load-pull using linear knee model for  $\alpha = 0$ .

Following the initial results, the load-pull emulations were expanded to include the entire  $\alpha$  tuning range in more detail. The emulated optimum Pout, optimum DE and peak DE at 8dB OPBO impedances are shown in Figure 5.6. These results provide a constant maximum Pout and DE performance over the entire  $\alpha$  tuning range and are somewhat in strong contrast to RFPA measurements in Chapter 3 and [71]. In addition, a constant performance characteristic is predicted for the 8dB OPBO impedances. As shown in Figure 5.7, max DE and peak DE at 8 dB OPBO exhibit only small variations over entire  $\alpha$  range.

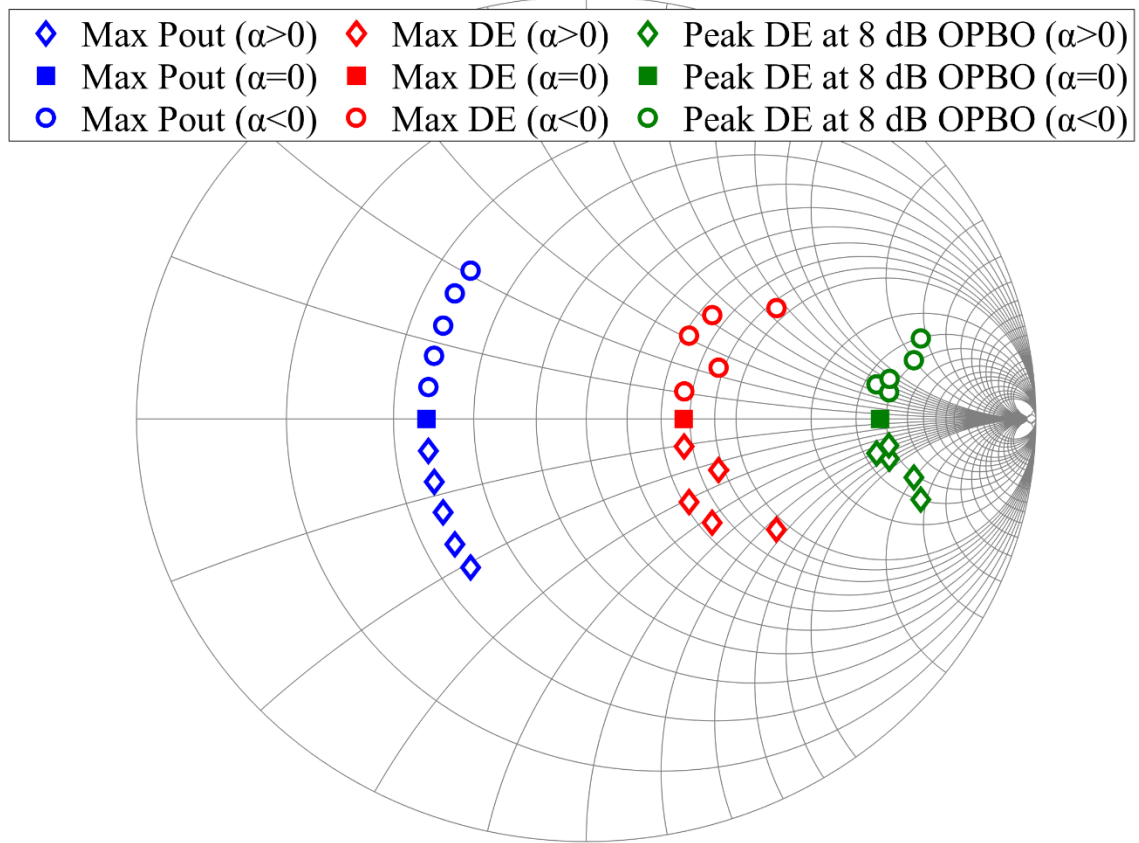


Figure 5.6. Emulated optimum Pout, optimum DE and peak DE at 8 dB OPBO impedances from load-pull of CCF mode using linear knee model for  $-1 \leq \alpha \leq +1$ .

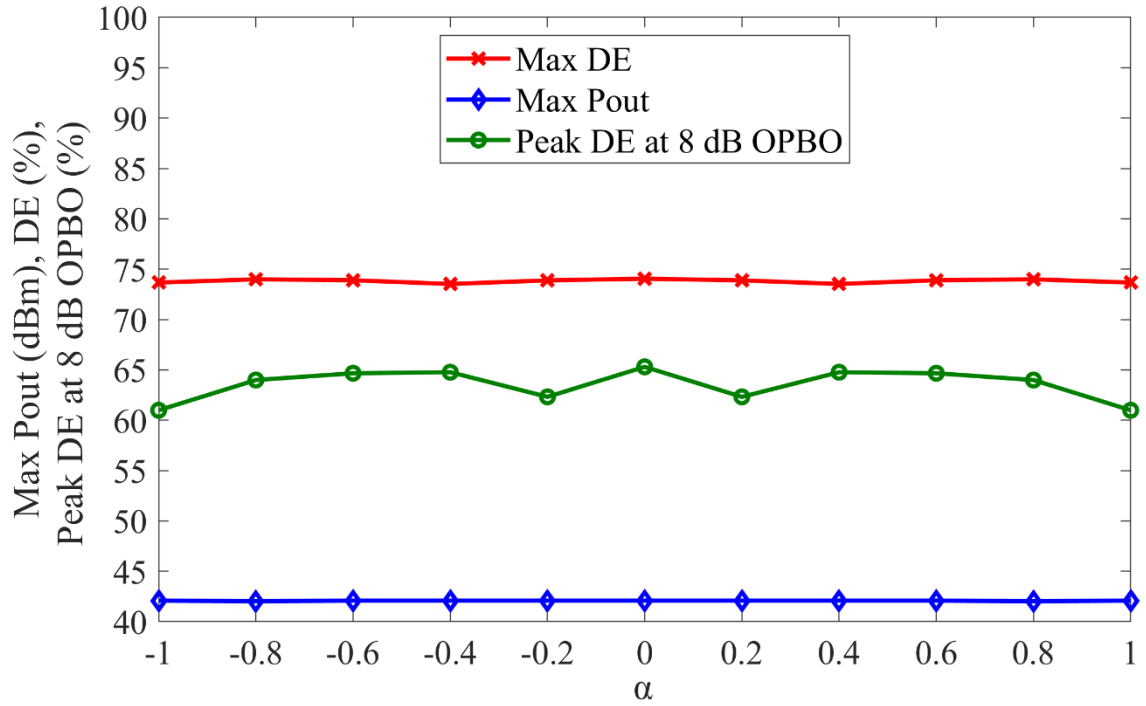


Figure 5.7. Max Pout, max DE and DE at 8 dB OPBO from load-pull emulation of CCF mode using linear knee model.

### 5.3 Non-linear Load-line Knee Model on CCF Mode

For a more accurate prediction of the RFPA performance, a non-linear scaling of the current waveform is introduced to account for the clipping from the drain voltage waveform and varying knee voltages [12]. The general non-linear I-V knee scaling on the drain current waveform, as defined in (5.3) [12], is expanded for load-pull emulations by inserting the drain voltage waveform equation (5.1) into (5.4a). The constant  $V_{knee}$  in (5.2b) and (5.3) is also modified so that it forms a function of minimum value from voltage waveforms as shown in (5.4b). The load-pull emulation is performed in MATLAB similar to the steps mentioned in previous section 5.2. The summary for the MATLAB emulation is shown in Figure 5.8, and the full MATLAB code for this emulation are described in the Appendix 3.

$$I_{ds,knee}(\theta) = \left(1 - e^{-\left(\frac{V_{ds}(\theta)}{V_{knee}}\right)}\right) * I_{ds}(\theta) \quad (5.3)$$

$$I_{ds,New}(\theta) = \left(1 - e^{-\left(\frac{V_{ds,new}(\theta)}{\gamma}\right)}\right) * I_{ds,new}(\theta) \quad (5.4a)$$

$$\gamma = \begin{cases} |V_{min} - V_{knee}|; & \text{if } V_{min} < V_{knee} \\ 0.01; & \text{if } V_{min} \geq V_{knee} \end{cases} \quad (5.4b)$$

The contours generated from the load pull emulation of CCF mode using this non-linear knee model are shown in Figure 5.9 and Figure 5.10. The optimum Pout and DE for  $\alpha = 0$  in Figure 5.9 show a reduced separation between these optima when compared to Figure 5.1. In contrast, the separation between optimum Pout and DE impedances for  $\alpha = \pm 1$  in Figure 5.10 are larger than the  $\alpha = 0$  case in Figure 5.9 indicating higher back-off efficiencies. This difference is quantified in Figure 5.11 when DE is plotted against normalised Pout for each  $\alpha$  case. The maximum efficiency trajectories are interpolated for  $\alpha = 0$  and  $\alpha = \pm 1$  respectively. The peak DE at 8 dB OPBO are 20% higher for  $\alpha = \pm 1$  when compared to the  $\alpha = 0$  case.



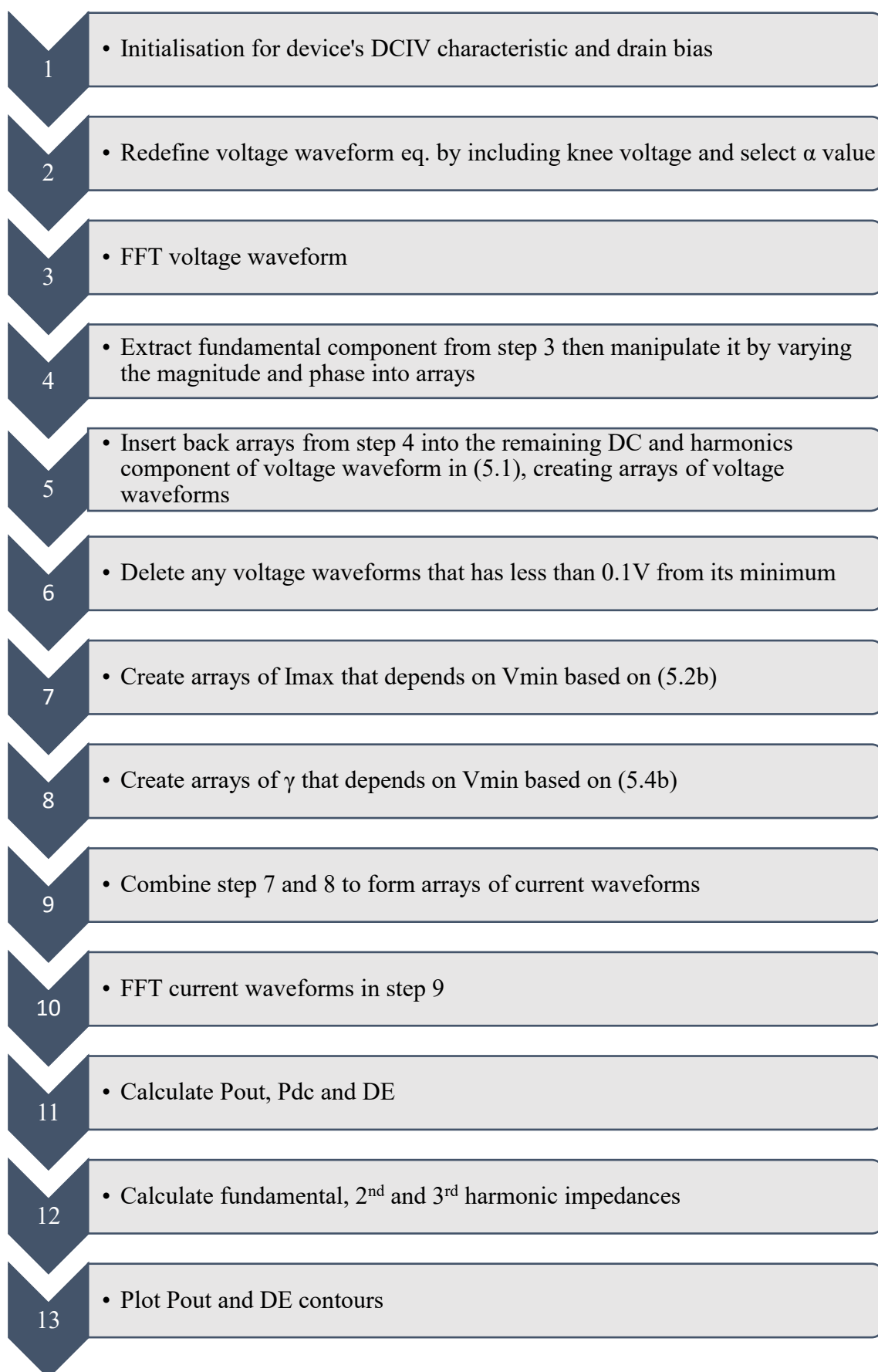


Figure 5.8. Flowchart for the emulation steps in MATLAB to generate load-pull contours for CCF mode with non-linear I-V knee model.

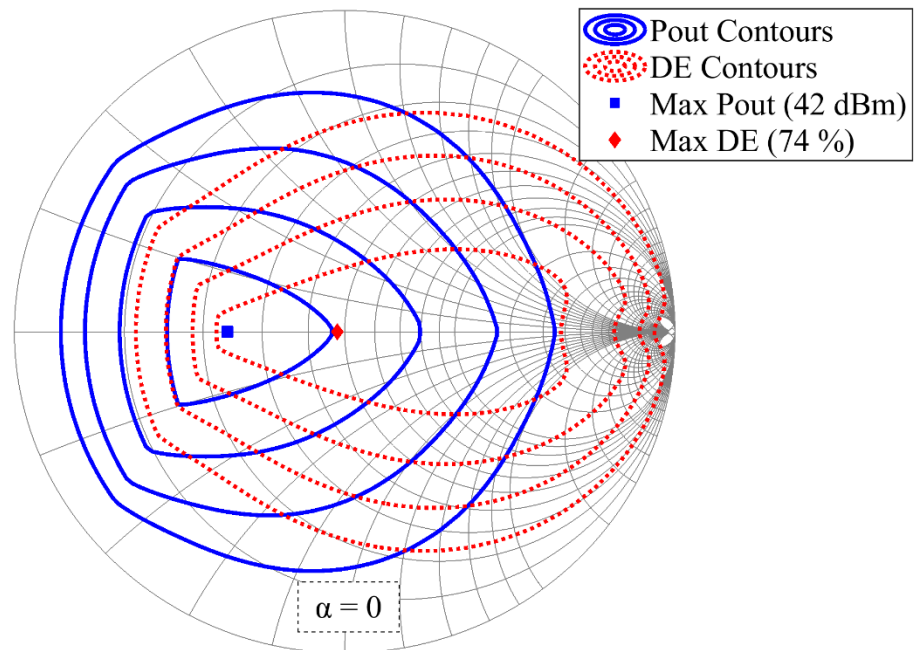


Figure 5.9. Emulated Pout and DE contours from non-linear knee model of CCF mode for  $\alpha = 0$ .

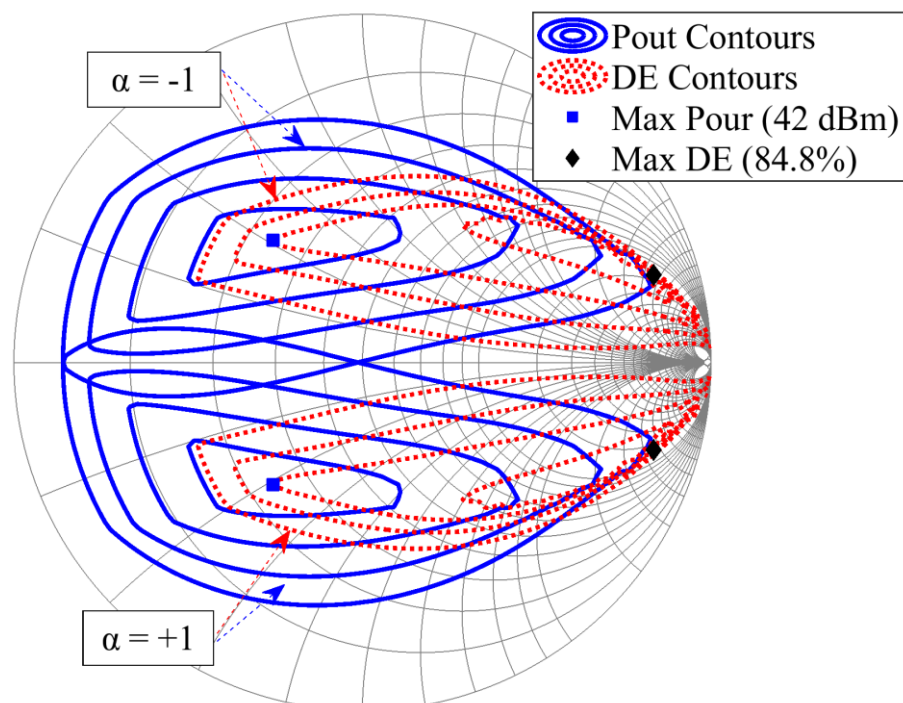


Figure 5.10. Emulated Pout and DE contours from non-linear knee model of CCF mode for  $\alpha = -1$  and  $\alpha = +1$ .

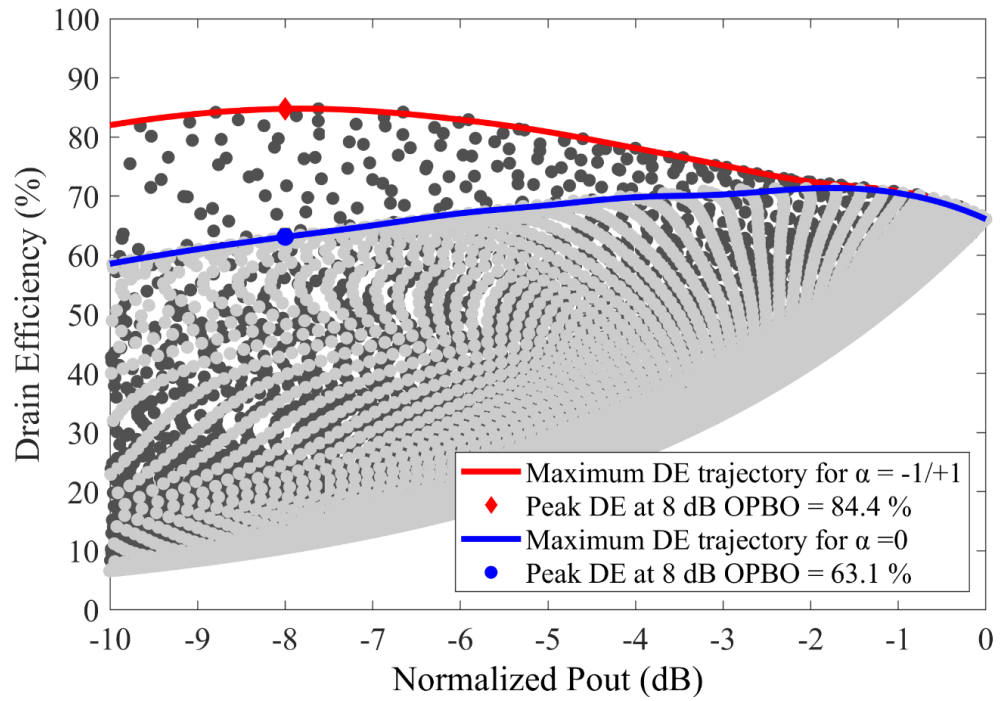


Figure 5.11. DE vs Pout from fundamental load-pull using non-linear knee model for  $\alpha=0$  and  $\alpha=-1/+1$ . Higher DE at 8 dB OPBO is obtained for  $\alpha=-1/+1$ .

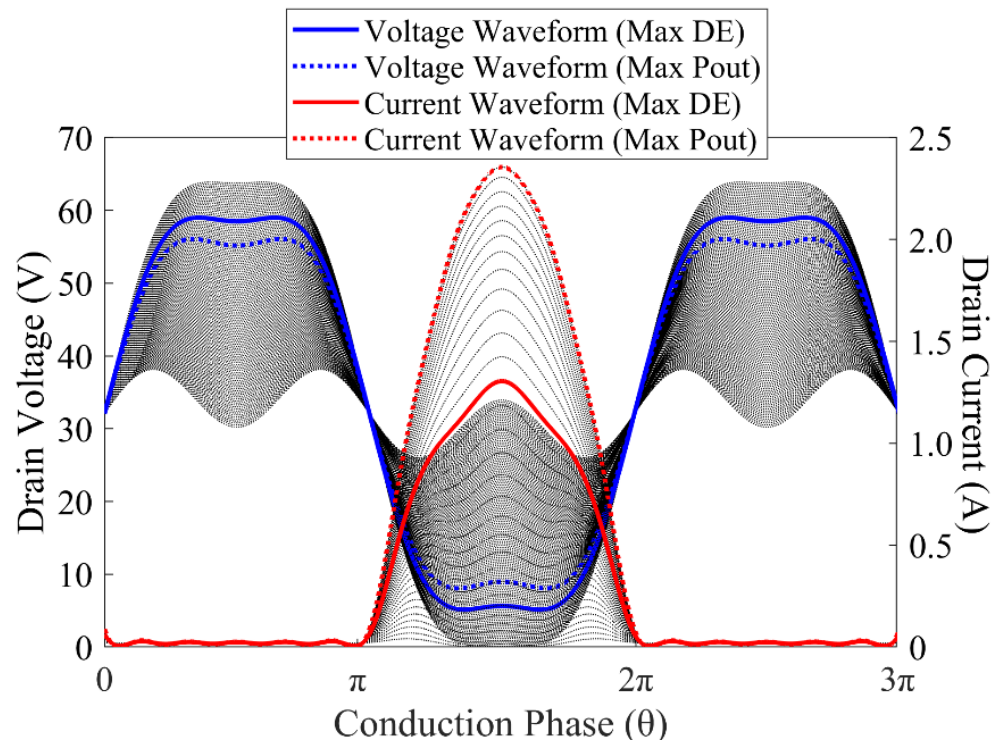


Figure 5.12. Drain current and voltage waveforms from load-pull emulation of non-linear knee model of CCF mode for  $\alpha = 0$ .

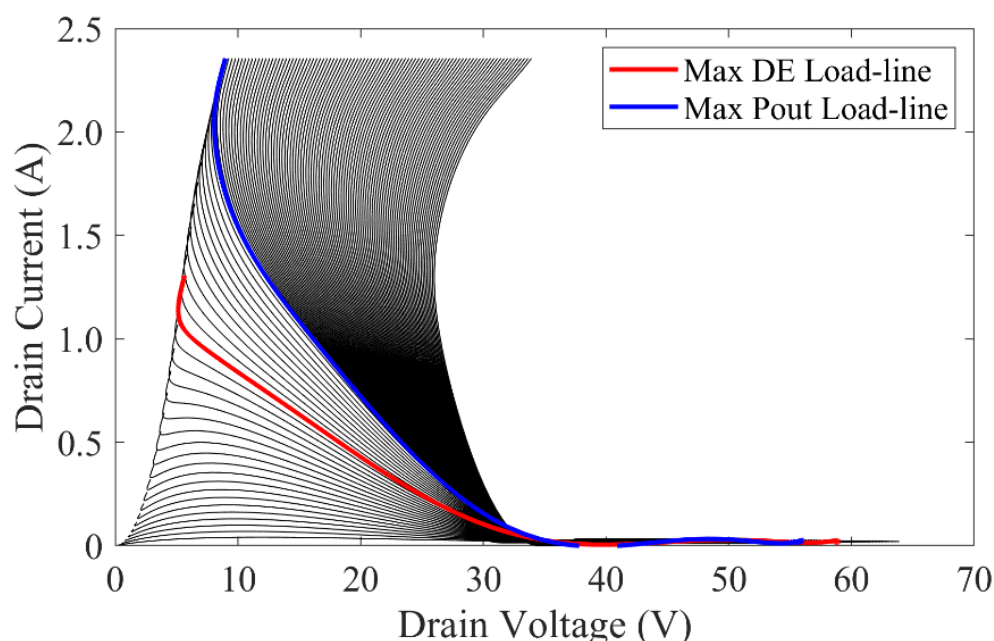


Figure 5.13. Load-lines for optimum DE and Pout from non-linear knee model load-pull emulation of CCF model for  $\alpha = 0$ .

Figure 5.12 shows all the drain current and voltage waveforms generated from the load-pull emulation for  $\alpha = 0$ , showing the waveforms when the load impedances are at the real axis. The highlighted waveforms shows the optimum Pout and DE, where the current waveform at optimum DE is clipped due to the I-V knee interaction. The load-lines for these waveforms are shown in Figure 5.13, showing that they are in-tracking with the knee-boundary. The peak current at optimum DE is higher than the previous emulation in Figure 5.4, indicating that, at the optimum DE impedance, the Pout value is higher than the emulation with linear knee model.

The relatively constant DE performance over OPBO impedances can be explained from the emulated impedances converging for increasing  $\alpha$  onto the same region in the Smith chart, as shown in Figure 5.14. Here, DE and Pout optima are relatively close for  $\alpha = 0$  and it move further apart when  $\alpha$  increases to  $\pm 1$ , where peak DE and DE optima at 8 dB OPBO converge onto the same impedance space. Figure 5.15 contrasts peak Pout, peak DE and DE at 8 dB OPBO from load-pull emulations of CCF mode comparing the

linear and non-linear knee emulations. Utilising the non-linear knee model as introduced in [71], the generated maximum DE and DE at 8 dB OPBO show symmetrical behaviour around  $\alpha = 0$ , where a clear minimum is located. Here, the lowest values for peak DE decreases to 71.3 % for  $\alpha = 0$  and raises to 84.8 % at  $\alpha = \pm 1$ . The variation in DE increases significantly for OPBO impedances with the lowest value decreasing to 63.1 % at 8 dB back-off for  $\alpha = 0$ . Both maximum DE and DE at 8 dB OPBO are reaching a similar value as  $\alpha$  values approaching unity. Meanwhile, the maximum Pout remains constant at 42 dBm for all  $\alpha$  ranges, which is the same for both emulated methods.

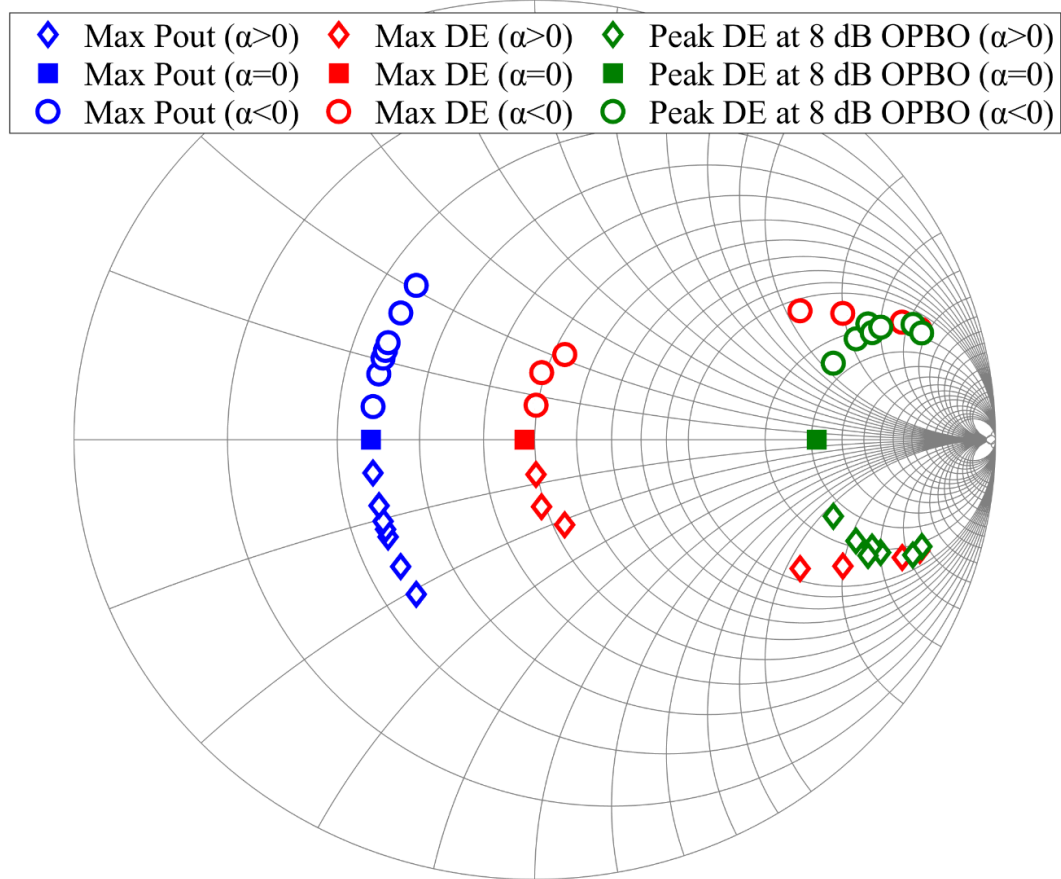


Figure 5.14. Optimum Pout, optimum DE and peak DE at 8 dB OPBO impedances from load-pull emulation of CCF mode using non-linear knee model for  $-1 \leq \alpha \leq +1$ .

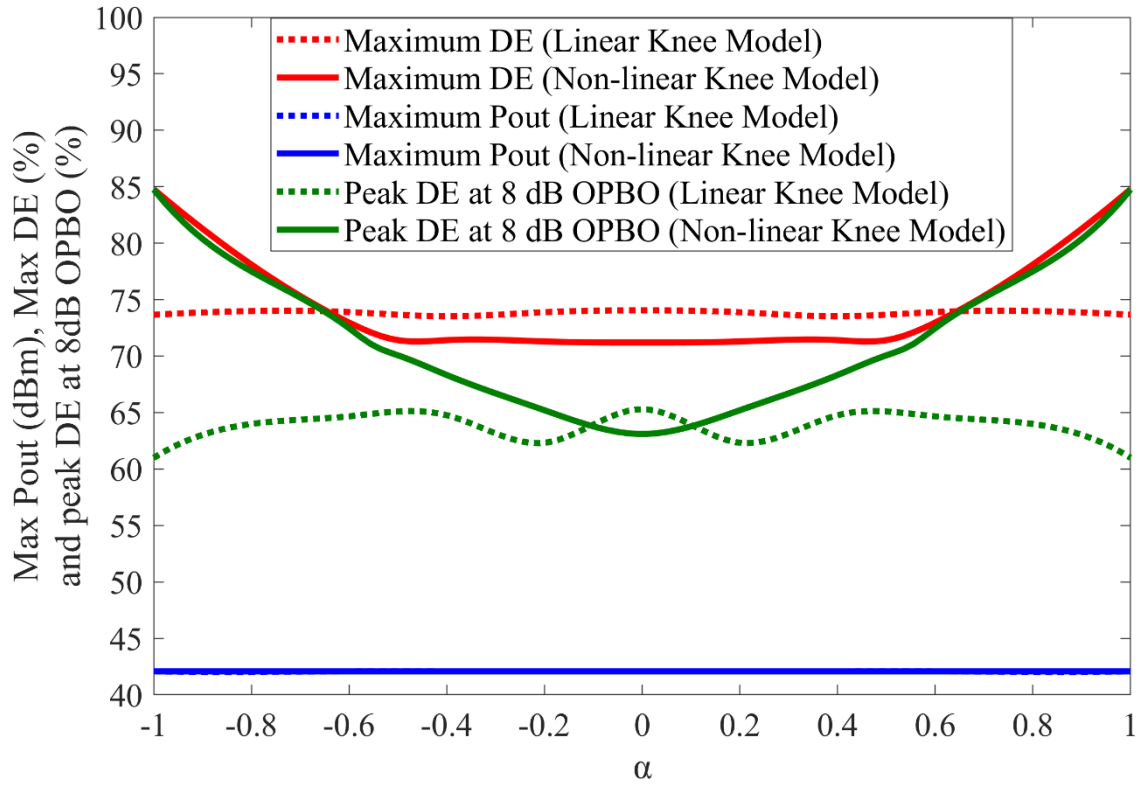


Figure 5.15. Comparisons for maximum Pout, maximum DE and peak DE at 8 dB OPBO from load-pull emulation of CCF mode using linear knee (dotted lines) and non-linear knee (solid lines) model.

## 5.4 Verification from Fundamental Load-pull with Sweep Phase of 2<sup>nd</sup> Harmonic Impedance

### 5.4.1 Load-pull Simulation

The new reformulation of CCF mode theory presented in the previous section 5.3 is verified through 10 W GaN HEMT device (CGH40010) simulations, using the available non-linear device model from Wolfspeed. The simulation is set up as follows: the device's drain is biased with 28 V, the gate is in deep Class-AB (10 mA), and the frequency of operation is 915 MHz. A load impedance tuner terminates the device's current generator plane (CGP) as the device's output parasitic network is de-embedded. Fundamental load-pull is performed while sweeping the phase of 2<sup>nd</sup> harmonic

impedances along the edge of the Smith chart. The input power from the signal generator with a  $50\ \Omega$  characteristic impedance is set to 26 dBm.

Figure 5.16 shows the optimum Pout, optimum DE and peak DE at 8 dB OPBO impedances from fundamental load-pull simulations with varying 2<sup>nd</sup> harmonic impedances. Both Pout and DE optima are close to the real axis of the Smith chart with a minimum separation between them for the 2<sup>nd</sup> harmonic impedance located at the short corresponding to  $\alpha = 0$ . This separation increases as the phase of the 2<sup>nd</sup> harmonic is moved further from short to open circuit, either through the inductive or capacitive region. The load-lines when the 2<sup>nd</sup> harmonic impedance is terminated to the short circuit (class-F) are shown in Figure 5.17. These load-lines are obtained at optimum Pout and DE impedances, which provides the same behaviour as in the emulation from Figure 5.13. Other load-lines are shown in Figure 5.18, when the phase of 2<sup>nd</sup> harmonic is terminated to  $300^\circ$ , that is approximately for  $\alpha = -1$  region. It can be seen that, at optimum DE, the load-lines has a reduced *I*<sub>max</sub> while it is expanded into the knee region, and keeping in-track with the knee boundary, similar to the prediction in the previous emulation.

The previous emulation, as shown in Figure 5.14, indicated a relatively similar position between optima, albeit with a reduced amount of changes. Especially, for  $\alpha = 0$  value, the emulated DE optima have a larger impedance when compared to simulation results. This difference is shown in Figure 5.19 comparing Pout and DE contours for  $\alpha = 0$ . The emulated Pout contours fit well with the simulation results; however, the simulated DE contours are constrained more towards lower impedances. Therefore, the 8 dB Pout contour moves far beyond the DE optimum, indicating larger drop of peak DE at OPBO in comparison to the 20 % drop that was predicted by the load-pull emulation. The reason for the differences between emulation and simulation contours in Figure 5.19 are not yet



entirely understood. Nevertheless, the emulation results are deemed to be sufficient to guide the RFPA design process.

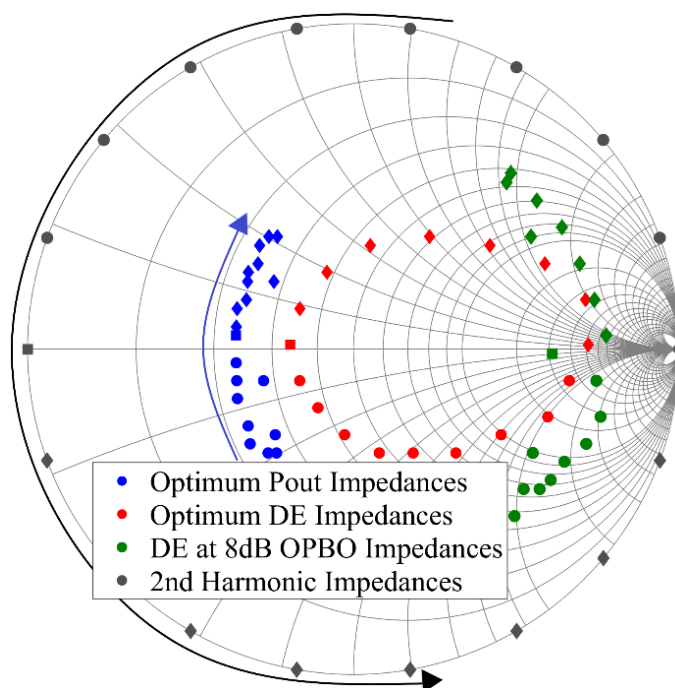


Figure 5.16. Simulated optimum DE, optimum Pout and peak DE at 8 dB OPBO impedances from fundamental load-pull with sweep phase of 2nd harmonic impedances presented on device's CGP.

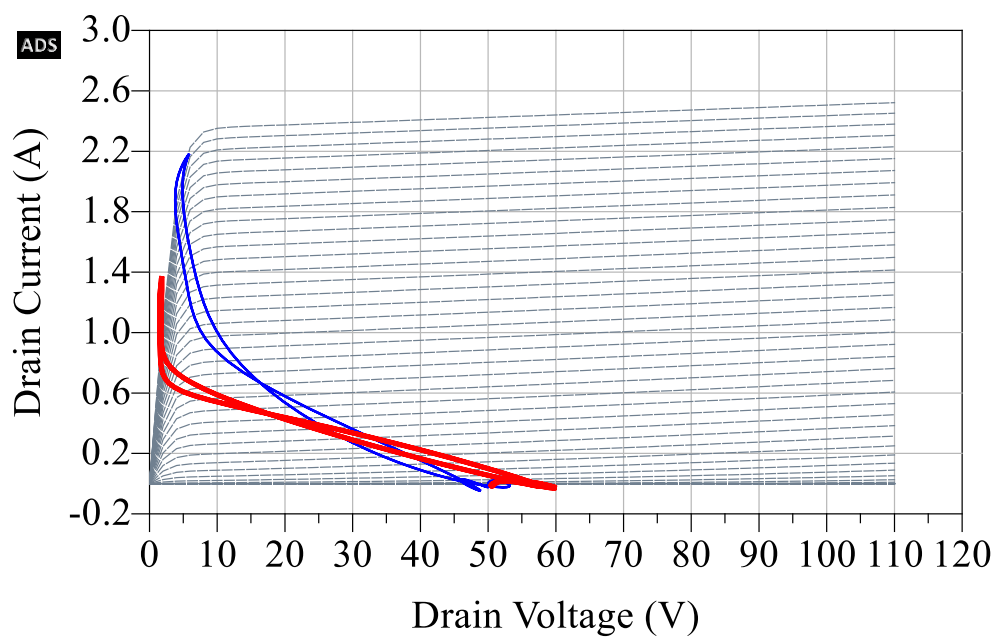


Figure 5.17. Simulated load-lines between optimum Pout (blue line) and optimum DE (red line) in class-F mode (2<sup>nd</sup> harmonic impedances is shorted)



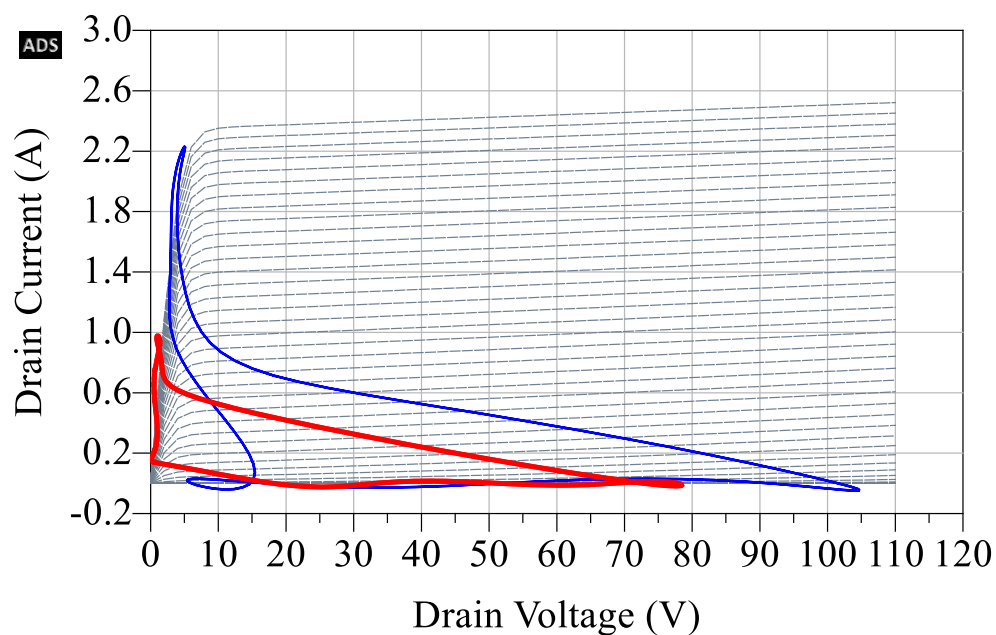


Figure 5.18. Simulated load-lines between optimum Pout (blue line) and optimum DE (red line) in CCF mode when  $\alpha = -1$  (phase of 2<sup>nd</sup> harmonic impedance is 300°)

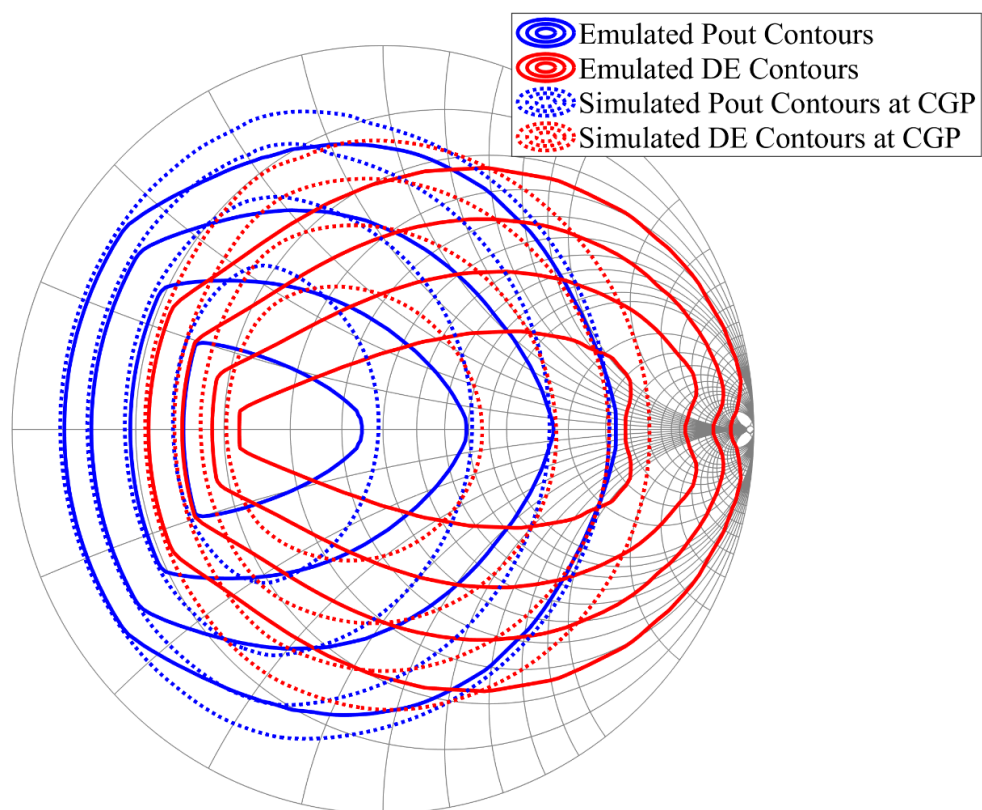


Figure 5.19. Simulated and emulated Pout and DE contour at CGP for  $\alpha = 0$ . The Pout contours stepping down by 2 dB while DE contours decrease in steps of 10 %.

Figure 5.20 shows the performances obtained from the load-pull simulation of the 10W device for a full range of 2<sup>nd</sup> harmonic impedances rotated around the Smith chart. Both optimum DE and peak DE at 8 dB OPBO vary symmetrically around 180 ° with the lowest value obtained when the 2<sup>nd</sup> harmonic is terminated to short circuit and confirming the previous emulation results for  $\alpha = 0$ . Peak DE optima vary symmetrically from 74.5 % to 89.1 % while peak DE at 8 dB OPBO vary symmetrically from 44.7 % to 89 % at different phases of the 2<sup>nd</sup> harmonic impedance setting. As expected, the simulated back-off efficiency is lower for the  $\alpha = 0$  case showing an even larger drop in DE by a further 20 %. These values increase symmetrically around 180 ° when the 2<sup>nd</sup> harmonic impedance is moved closer to an open circuit, almost reaching the peak DE values. The peak Pout stays relatively constant above 40.6 dBm across all phases of the 2<sup>nd</sup> harmonic impedances.

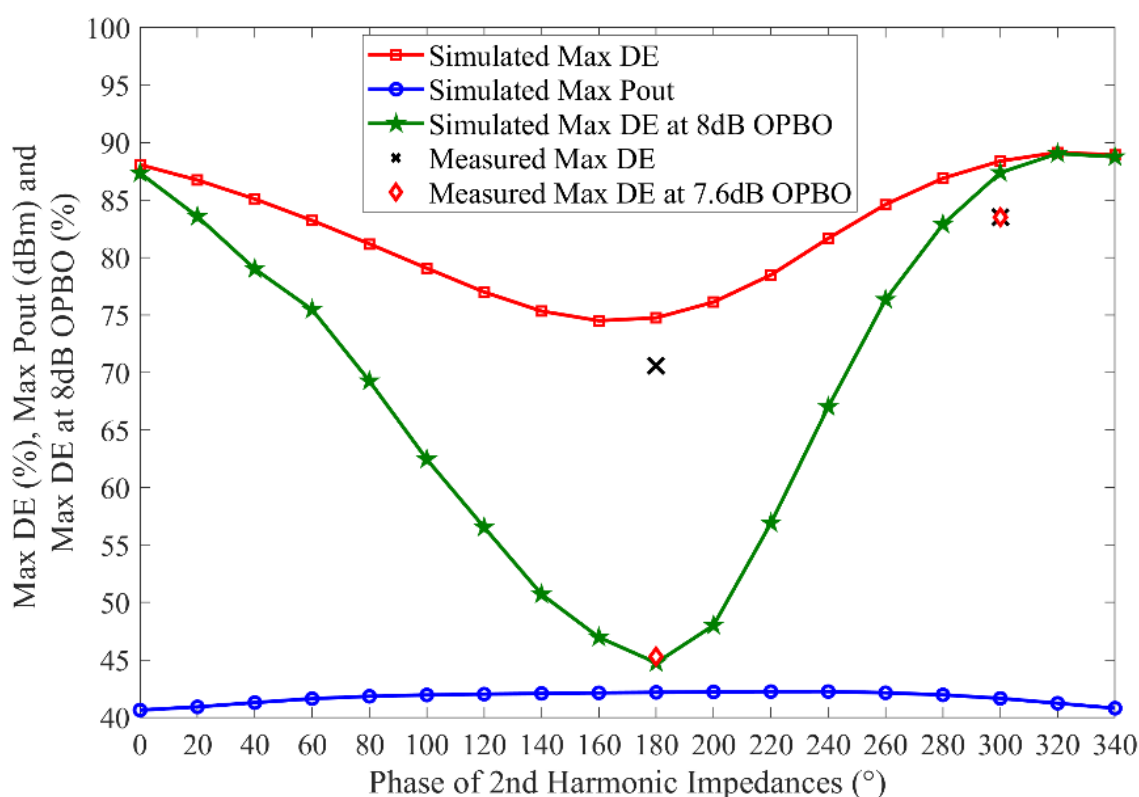


Figure 5.20. Simulated and measured optimum DE, optimum Pout and peak DE at 8 dB OPBO from fundamental load-pull with different phase of 2nd harmonic impedances termination on device's CGP.

## 5.4.2 Active Load-pull Measurement

The 10 W GaN HEMT device mounted on a test fixture is measured using an open-loop active load-pull system with the same bias and frequency of operation. Two signal generators are used at the device's output to control the fundamental and 2<sup>nd</sup> harmonic impedances respectively. The 3<sup>rd</sup> harmonic impedances are not controlled in this measurement setup. Another signal generator is used as a source signal that is connected through a driver amplifier into the device's input to generate a constant input power available to the device (25.5 dBm) to drive the device up to 3 dB compression at optimum  $P_{out}$  impedance. Bias tees are used for both input and output of the device to provide isolation for the RF signal and the DC supply. Two couplers are used at both input and output ports to measure the respective port's impedances and power levels using a PNA. The test-set and test-fixture are de-embedded to present the fundamental and load impedances at the device's package plane. The measurement is performed at the device's package plane due to issue with the de-embedding file for the load-pull measurement set up.

As this measurement is not de-embedded to the device's current generator plane, the required phase of 2<sup>nd</sup> harmonic impedances differ from the previous simulation. By using the available device's model, it is found that the phase of 2<sup>nd</sup> harmonic impedances needed to present  $\alpha=0$  at the device's package plane is 200 °, which is equal to presenting a short circuit at the CGP. Meanwhile, the phase of the 2<sup>nd</sup> harmonic impedance needed for  $\alpha = -1$  at the device's package plane is 40 ° that is equal to presenting 300 ° at the CGP. Fundamental load-pull measurements are performed on the device by setting the magnitude of the 2<sup>nd</sup> harmonic impedance to 0.98 while the phases are set to the aforementioned values.

Figure 5.21 and Figure 5.23 shows the load-pull measurements comparing Pout and DE contours with simulation results for the 2 cases of  $\alpha$  values. Again, optimum Pout and DE impedances in Figure 5.21 are much closer for  $\alpha = 0$ , while they are largely separated for  $\alpha = -1$  in Figure 5.23, hence indicating a lower DE performance at back-off for  $\alpha = 0$ . The 40 % drop between peak DE at 8 dB OPBO from  $\alpha = -1$  to  $\alpha = 0$  has been confirmed in the load-pull measurement as shown in both Figure 5.22 and Figure 5.24.

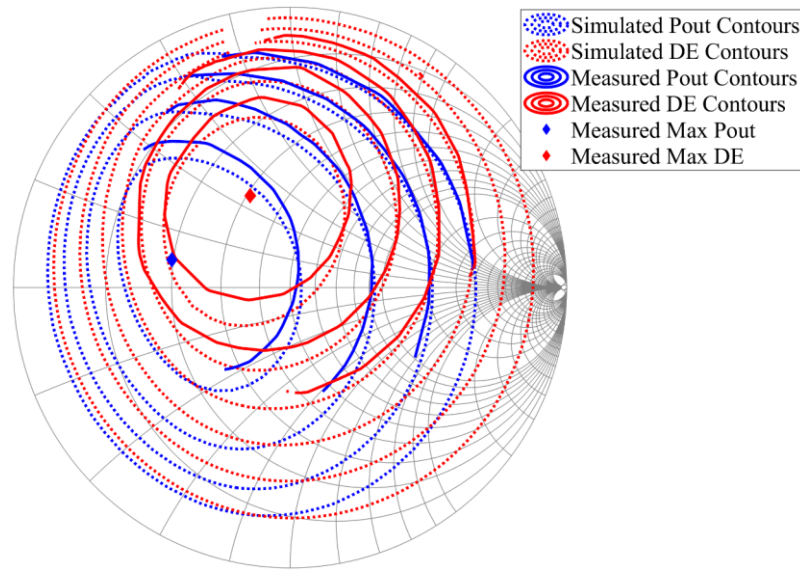


Figure 5.21. Simulated and measured Pout and DE contours at device's package plane for  $\alpha = 0$ .

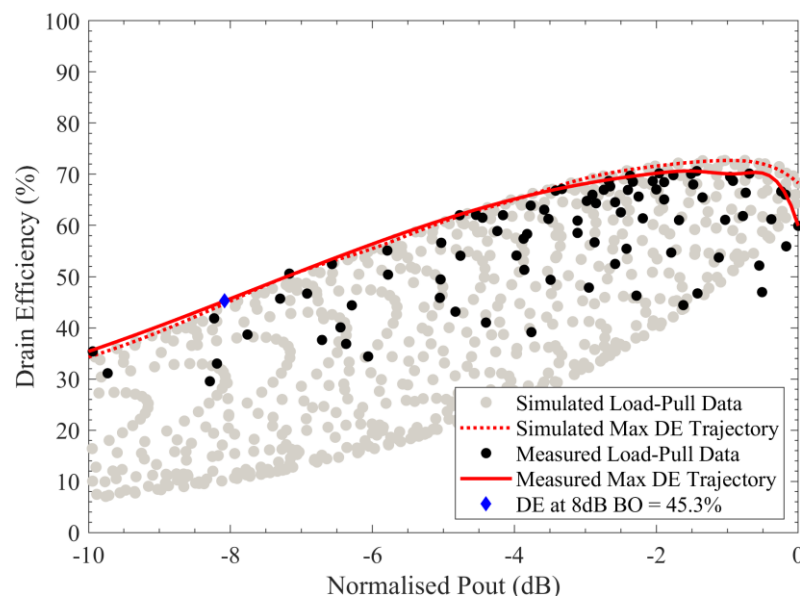


Figure 5.22. Simulated and measured peak DE trajectory from load-pull for  $\alpha = 0$ .

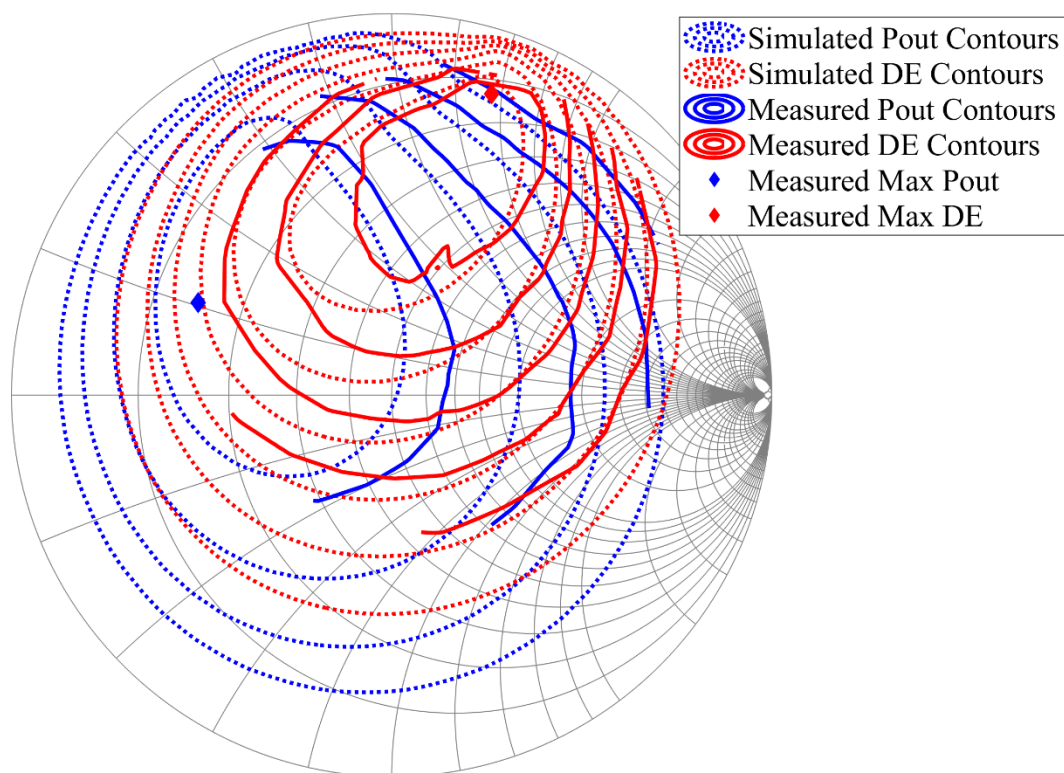


Figure 5.23. Simulated and measured Pout and DE contours at device's package plane for  $\alpha = -1$ .

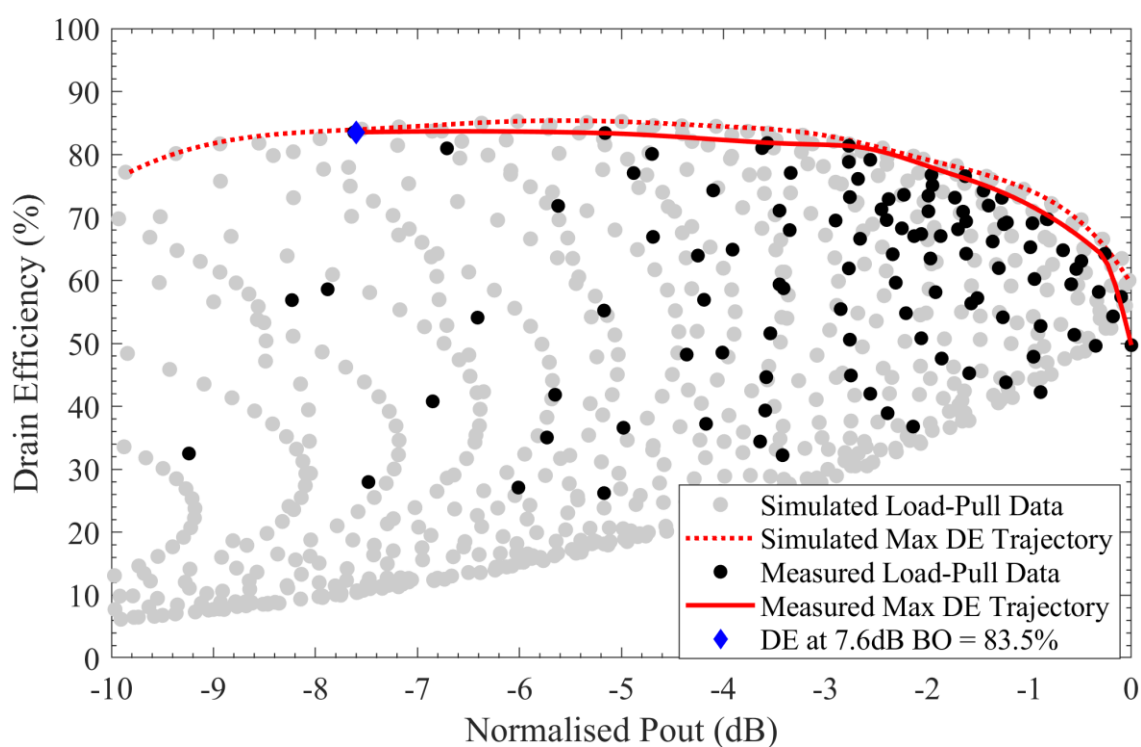


Figure 5.24. Simulated and measured peak DE trajectory from load-pull for  $\alpha = -1$ .

Figure 5.25 shows the peak DE trajectories that was interpolated from measured load-pull data for the two  $\alpha$  cases when plotting DE against normalised Pout. The peak DE trajectories at  $\alpha = -1$  is only measured up to 7.6 dB OPBO because only a small number of impedance points were available during the measurement. The equivalent DE simulation results for  $\alpha = -1$  are added to confirm whether the interpolation is correct. Peak DE measured for  $\alpha = 0$  is up to 70.6 % and drops continuously for an increasing output back-off, while for  $\alpha = -1$ , the DE performance increases by 13 % to 83.5 %. Maximum DE at 8 dB OPBO measured for  $\alpha = 0$  is 45.3 % representing almost a 40 % drop against the achievable performance for  $\alpha = -1$  at 7.6 dB OPBO. As previously mentioned, the emulated back-off performance for  $\alpha = 0$  is overestimating DE by about 20 %. Nevertheless, the results demonstrate that the relatively simple emulations predict quite well the overall performance trade-offs of a PA design at peak and OPBO impedances.

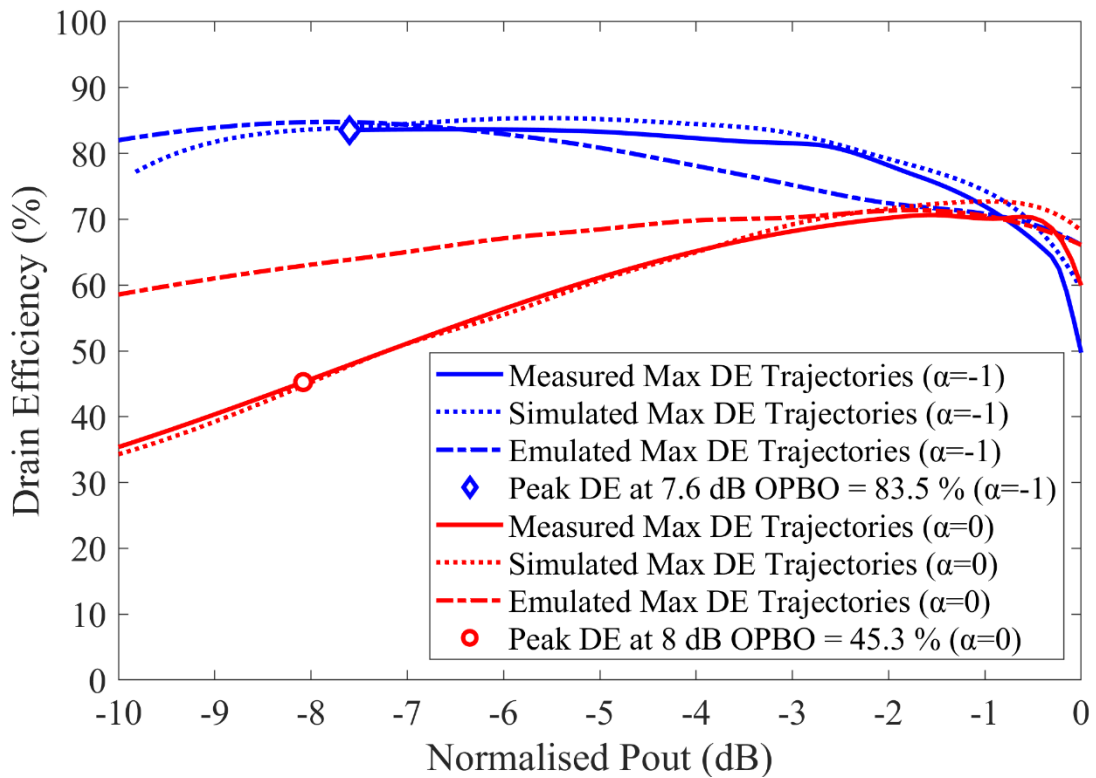


Figure 5.25. Measured, simulated and emulated max DE trajectory for  $\alpha = 0$  and  $\alpha = -1$ .

## 5.5 Load-pull measurement from 10 W GaN PA circuit.

New theoretical and experimental analysis of the CCF mode in the previous section shows that the optimum DE and peak DE at OPBO are reached for  $\alpha = \pm 1$ . Therefore, limiting the  $\alpha$  space to maintain the high efficiencies at Peak Pout and OPBO is an attractive design approach. Conveniently, a previously reported RFPA with a 2<sup>nd</sup> generation Wolfspeed 10 W GaN device (CG2H40010F) [14], which exploits the CCF mode with a restricted 2<sup>nd</sup> harmonic impedance rotation to keep the peak efficiencies high, is employed here to investigate its OPBO performance. The RFPA circuit design focuses on controlling the fundamental and 2<sup>nd</sup> harmonic impedances to be close to the optimum ( $\alpha = -1$ ) throughout the bandwidth to keep the efficiency high. Figure 4.8 depicts the fabricated 10 W GaN RFPA [14]. As already reported, due to instability, the input matching network had to be adjusted, causing a change of the device input impedances at the fundamental and harmonic frequencies, hence reducing peak Pout and DE.

The simulated fundamental impedances at the CGP shown in Figure 5.26 are close to  $\alpha = -1$  across the design bandwidth (1.8 GHz to 2.7 GHz). The phase rotation of 2<sup>nd</sup> harmonic impedances were restricted for a broadband RFPA design ranging from  $-53^\circ$  to  $-131^\circ$  at the edge of the Smith chart. At 2 GHz, the termination of 2<sup>nd</sup> harmonic output impedance at 2 GHz has a phase of  $-87^\circ$  and therefore close to the  $\alpha = -1$  region and the reason for choosing this for load-pull measurements on the PA. The PA is biased with 28 V at the drain and -3.05 V at the gate, drawing 10 mA current. A CW measurement with swept input power is performed on the PA at 2.0 GHz through the 50  $\Omega$  load. Figure 5.27 shows the measured DE and gain plotted against Pout. The output power and DE obtained at 3 dB gain compression is 15.6 W and 73.4% respectively. Next, a load-pull



measurement is performed on the PA circuit with the same input setting at the 3 dB gain compression, using a fast active load-pull system.

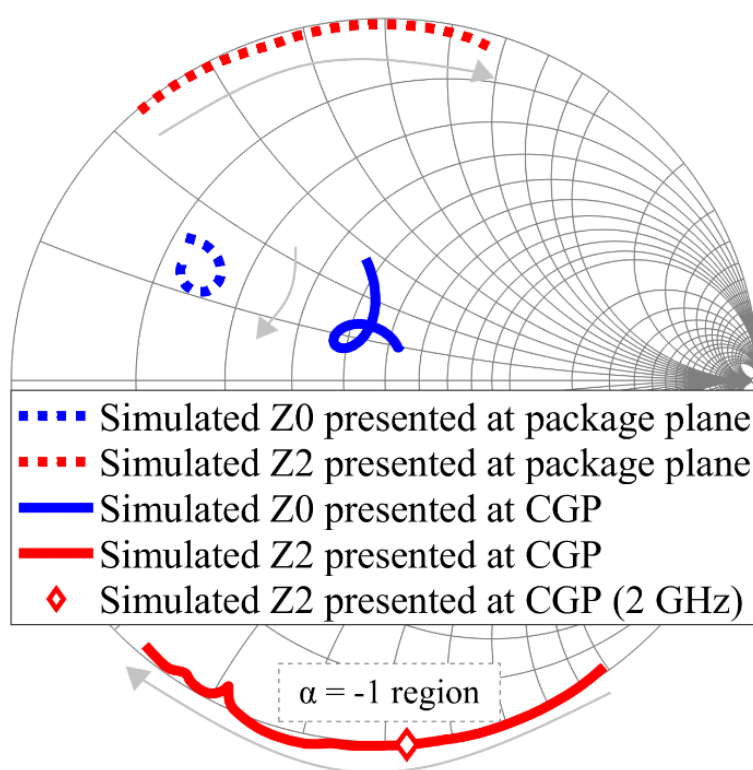


Figure 5.26. Simulated fundamental and 2nd harmonic impedances presented to the device's package plane and CGP. The phase of 2nd harmonic impedance presented at CGP is  $-87^\circ$  at 2.0 GHz that is close to  $\alpha = -1$  region.

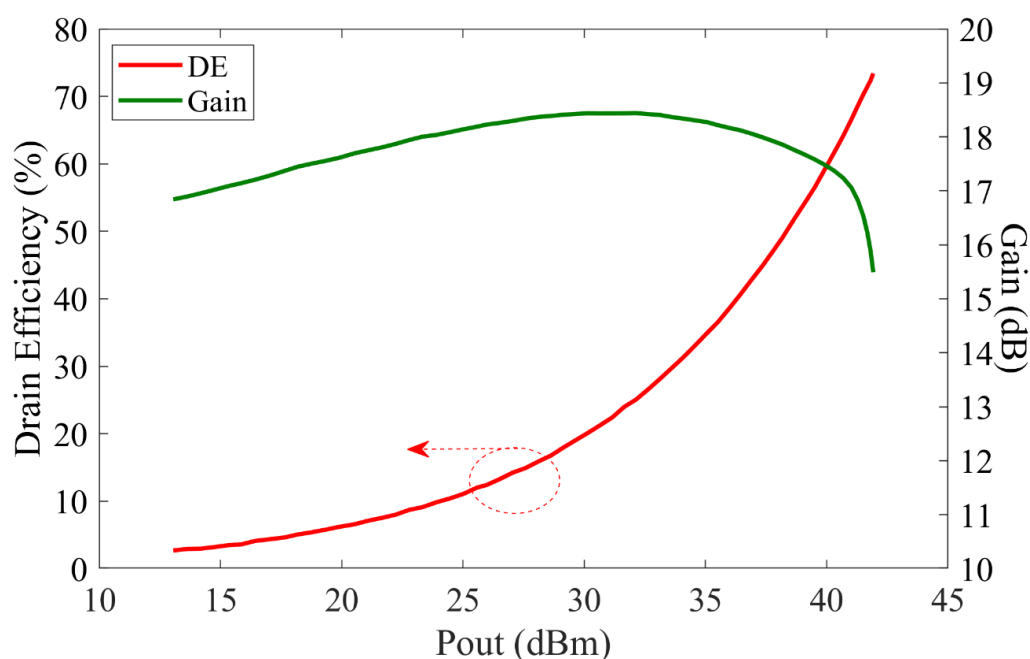


Figure 5.27. Measured DE and Gain vs  $P_{out}$  at 2.0 GHz.



Figure 5.28 shows the Pout and DE contours obtained from the load-pull measurement on the PA circuit in contrast to simulated data. The Pout contours are in step of 2 dBm and the DE contours are in the step of 10 %. To verify the predicted OPBO performance, the measured and simulated peak DE are plotted against normalised Pout in Figure 5.29. Both, the simulated PA performances before and after the tuning of the input network are shown. The initial PA simulation has a 70.3 % DE at 8dB OPBO and in line with emulations and measurements of the device. The 10 % difference from the device's measurement is due to losses within the PA circuit, i.e. matching and bias networks. The simulation results accounting for the input network changes show a very good agreement with the PA measurements meaning that a further DE loss of 10 % due to stabilisation measures that had to be carried out.

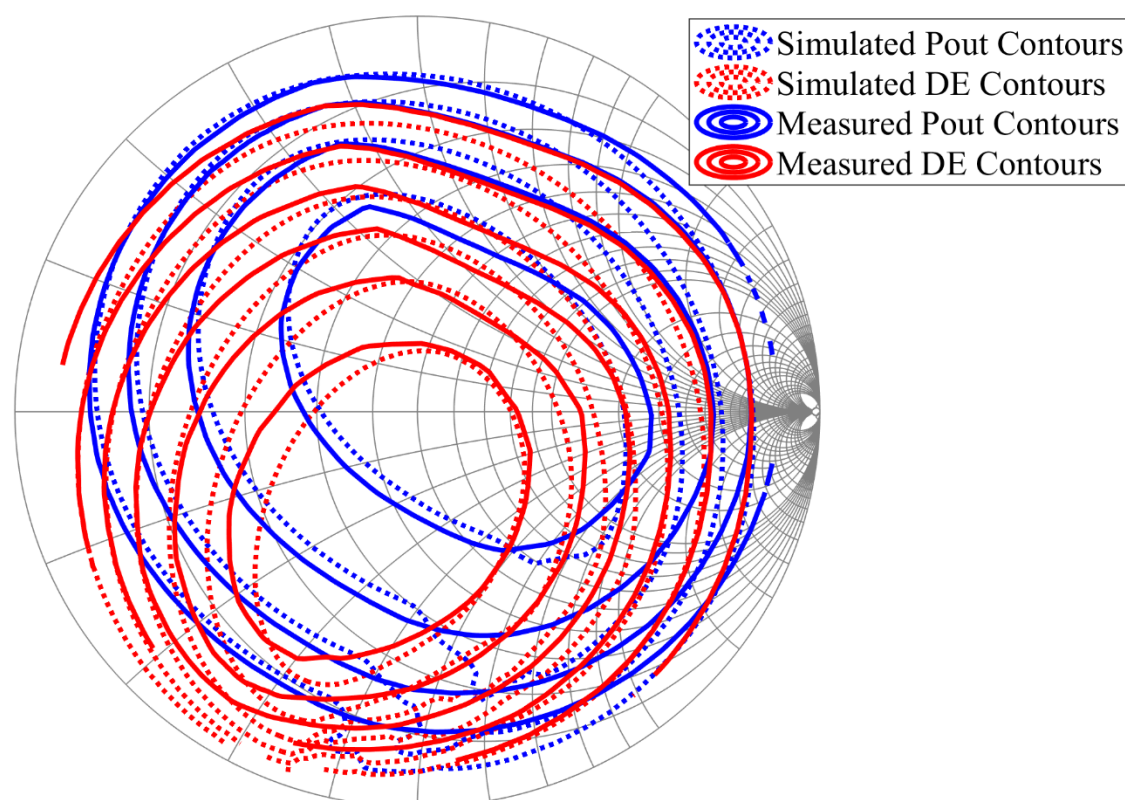


Figure 5.28. Simulated and measured Pout and DE contours from load-pulling 10 W GaN RFPA at 2.0 GHz.

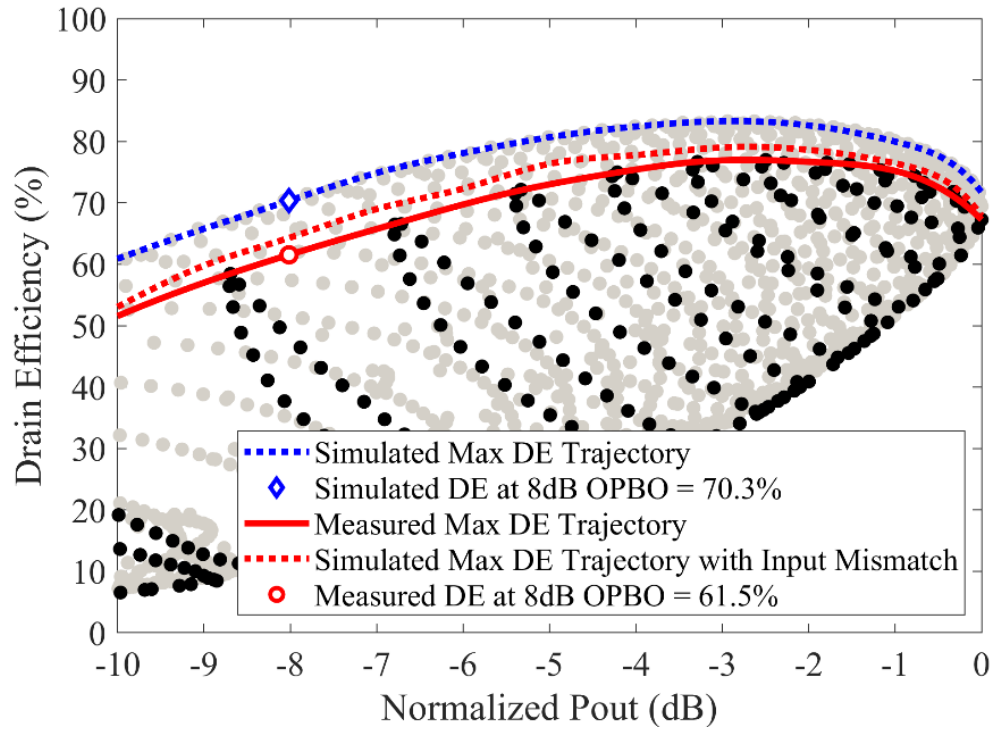


Figure 5.29. Simulated and measured max DE trajectory from load-pulling fabricated 10 W GaN RFPA at 2.0 GHz.

## 5.6 Chapter Summary

This chapter has introduced a new method to generate power and efficiency contours for RF device that operates in CCF mode, only by using waveform theory and calculation in MATLAB. The additional non-linear I-V knee interaction between current and voltage waveforms are included in the emulation enabling the load-lines generated from the emulation to be in-line with the knee boundary of the transistor device. The  $\alpha$  parameter in the CCF mode allows to control the 2<sup>nd</sup> harmonic load impedances to the device. The emulated power and efficiency contours move apart from each other as the  $\alpha$  parameter changes from 0 to  $\pm 1$ . Consequently, the maximum efficiency and peak DE at 8 dB OPBO varies symmetrically across  $\alpha = 0$ , peaking at  $\alpha \pm 1$ . The load-pull emulations is verified through load-pull simulations and measurements using a 10 W GaN packaged transistor, in which the  $\alpha$  parameter from the emulation is translated as the rotation of 2<sup>nd</sup>

harmonic load impedances. As expected, the difference between maximum DE for  $\alpha = 0$  and  $\alpha = -1$  setting from device's load-pull measurement is almost 20 %. Also, the peak DE at 8 dB OPBO varies by 40 % between the two  $\alpha$  parameter setting. In conclusion, the device will have different optimum Pout and DE separation, depending on the 2<sup>nd</sup> harmonic load termination.

The importance of terminating the 2<sup>nd</sup> harmonic load impedances correctly within the  $\alpha$  space is investigated on the 10 W RFPA circuit. This PA has a 2<sup>nd</sup> harmonic impedances presented to the device's CGP close to  $\alpha = -1$  at 2.0 GHz. The measurement result from load-pulling this PA when it is operating at 3 dB gain compression, shows more than 60 % DE at 8 dB OPBO, considering the actual losses and mismatch within fabricated circuit. The circuit losses can be minimised if the 2<sup>nd</sup> harmonic load termination of the device is done inside the package of the transistor. The integrated packaged transistor device can minimise the size of the PA circuits, hence, reducing power losses.

# Chapter 6

## Theoretical Video-bandwidth Extension

### 6.1 Introduction

The previous chapters have demonstrated the theory and practicality of designing high power, broadband and highly efficient power amplifier circuits. These circuit performance parameters are crucial for the next generation of the 5G communications system. According to enhanced Mobile Broadband (eMBB) specification [6], the 5G network operating at sub-6 GHz requires up to 100 MHz channel bandwidth (instantaneous bandwidth) which is 5 times wider than the initial 4G network (20 MHz). Above 6 GHz, the instantaneous bandwidth requirements increase to 400 MHz [6] or even up to 800 MHz [93]. These new operating bandwidth requirements bring new design challenges for PA design, not only for operation over broad bandwidth at high frequency, but also to cover a wide range of instantaneous bandwidth.

PA performance degrades over a wide instantaneous bandwidth due to the memory effects [12, 94, 95]. The instantaneous bandwidth, or also refers to the video bandwidth (VBW) is defined as the maximum amount of spectrum over which the PA can operate,

with a constant intermodulation product. The VBW specifications can vary between one company to another. For instance, *Maxim Integrated* defined VBW as the frequency separation between 2-tones CW signal tested on PA that causes the difference between IMD3 low and high to be no more than 3 dB [94]. This definition is well adopted in several publications addressing VBW improvements in their PA circuits [96, 97, 98]. The IMD3 arises due to the device non-linearity especially when the PAs are operated with compression. The memory effects arises from the modulation in the bias network of RF PA [18], where a finite impedances from the bias network [99] introduce a resonant to the device. These ‘electrical’ memory effects also cause distortion in the AM/AM and AM/PM PA characteristic behaviour. Other memory effects also coming from the thermal effect of the transistor [12, 95], which will not be discussed in this thesis.

Memory effects in RF PA circuits affecting the IMD3 or ACLR asymmetry and low frequency resonant. especially when a modulated signal with wide instantaneous bandwidth is applied. The IMD3 asymmetry complicates the DPD linearisation, in which, a memoryless DPD system will not be able to cancel this asymmetric IMD [94, 95]. Several publications have introduced baseband termination circuit in the output matching network of their PAs, either to suppress the low frequency resonances coming between the device and the bias network, or to reduce the baseband impedances [96, 97, 98, 100, 101]. A baseband termination circuit is introduced to improve the VBW, that consists of shorted high value capacitor connected close to the device’s output (and input) through a small value inductor (transmission lines or bondwires). This additional circuit not only suppresses the output resonance that usually exist at the low baseband frequencies, but also lowers the baseband impedance.

In this chapter, theoretical calculations are performed to investigate the effect of baseband termination circuit on the output resonances and baseband impedances. The

ideal circuit components are replaced with equivalent circuit to accurately model the output resonance within the circuit. Finally, sensitivity analyses are performed on each component within the equivalent circuit from the baseband termination circuit for further improvement of video-bandwidth extension.

## 6.2 Extending VBW with Series Low Inductance and High Capacitance Circuit

One of the memory effects in RF PA is raised from the bias network. The bias network is modelled with bias feed inductance (5 nH) and RF decoupling capacitors (up to 1 uF). This network resonates with output drain capacitances from the active device,  $C_{ds}$ , and create finite impedances at the low frequency, thus limiting the VBW. Figure 6.1(a) shows a circuit model of an output bias network with device's parasitic capacitance and the simplified circuit is shown in Figure 6.1(b). Capacitor C1 represents the parasitic capacitor, in this case, obtained from 240 W bare die GaN HEMT device with a value of 10.3 pF at 1.8 GHz. The bias network consists of a feed inductor, L1 with a value of 5 nH and RF decoupling capacitor, C2 with capacitance of 1 uF.

The resonant frequency from circuit in Figure 6.1 (b) is

$$f_r = \frac{1}{2\pi} \frac{\sqrt{C1 + C2}}{\sqrt{C1 * C2 * L1}} = 701.324 \text{ MHz} \quad (6.1)$$

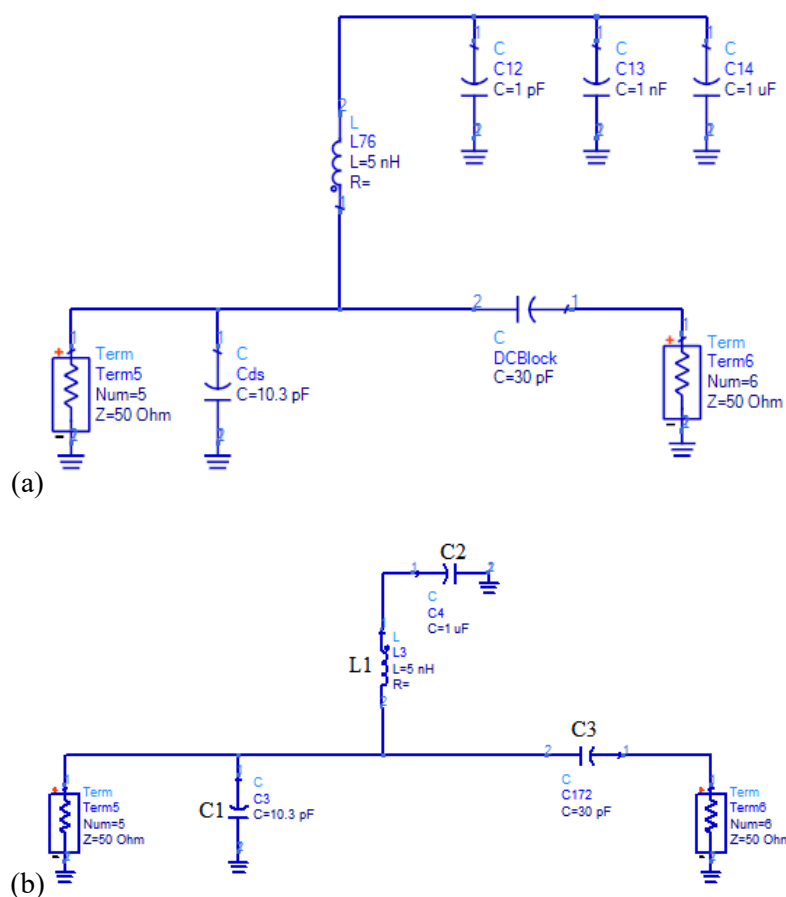


Figure 6.1. LF circuit model (a) consists of bias feed inductor, RF decoupling capacitors, device's parasitic capacitor and DC block capacitor. Equivalent circuit model (b) by considering only the highest value of the RF decoupling capacitor.

The ADS simulation computes resonant frequency of 678 MHz. The result differs with theoretical calculation because the capacitor C3 is excluded in the above equation to simplify the equation. The input impedances looking from the device's internal plane from the circuit in Figure 6.1(b) can be theoretically calculated in (6.2). The input impedances variation up to 2 GHz is shown in Figure 6.2, showing more than  $10\ \Omega$  from 250 MHz. This impedance peaking at 673 MHz, that is close to the circuit's resonance frequency in (6.1), reaching up to  $50\ \Omega$ .

$$Z_{in} = \frac{1}{j\omega C1 + \frac{1}{j\omega L1 + \frac{1}{j\omega C2}} + \frac{1}{\frac{1}{j\omega C3} + 50}}$$

(6.2)

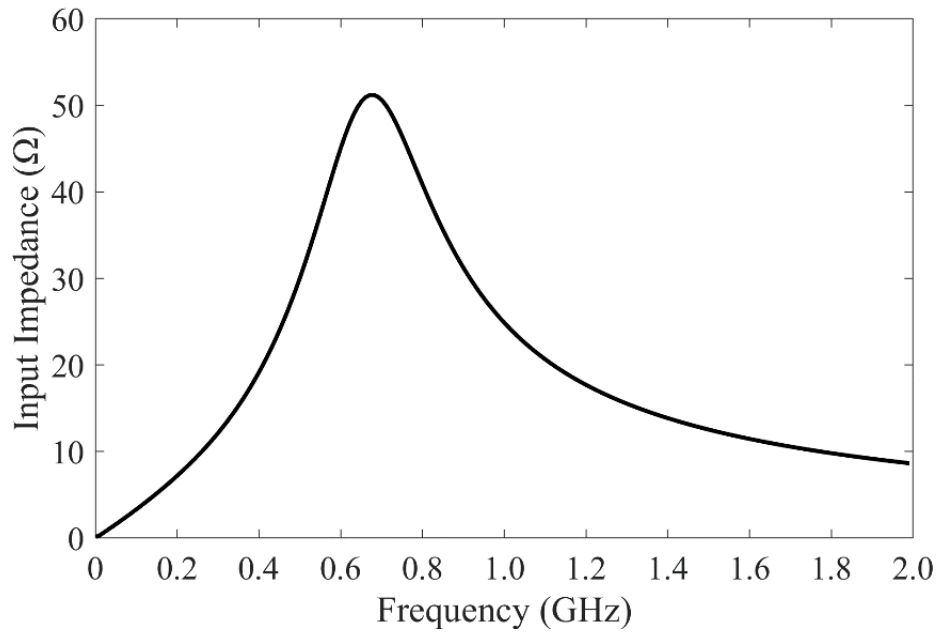


Figure 6.2. Input impedance seen from port 1 on Figure 6.1(b).

The proposed circuit to increase the VBW is shown in Figure 6.3, consisting of the additional series inductor with a low value inductance, L2 (0.1 nH) and a shunt capacitor with a high value capacitance, C3 (1 uF). C1 is the drain parasitic capacitor, C<sub>ds</sub>, and C4 is DC block capacitor. The bias network consists of feed inductor, L1 and largest value of RF decoupling capacitor, C2. Ideally, the additional series LC network has to be as close as possible to the device's drain terminal, which can be achieved by integrating this network inside transistor package. The low value inductor can be replaced with a short bondwires and a ceramic capacitor or single layer capacitor with a high value capacitance can be used for the C3 capacitor.



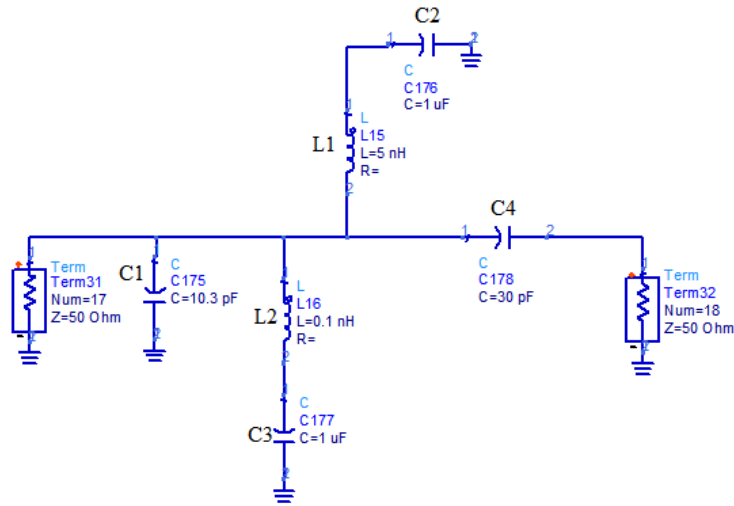


Figure 6.3. Proposed simplified circuit for extending VBW with additional low value inductor, L2 and high value capacitor, C3.

The resonant frequency occurs from the circuit in Figure 6.3 can be theoretically calculated, at which the DC block capacitor C3 are excluded for further simplification without majorly changing the result.

The total impedances of the circuit in Figure 6.3 is:

$$X_T = \frac{1}{j\omega C1 + \frac{1}{j\omega L1 + \frac{1}{j\omega C2}} + \frac{1}{j\omega L2 + \frac{1}{j\omega C3}}} \quad (6.3)$$

If the denominator from (5.3) equals zero, as shown, then

$$j\omega C1 + \frac{1}{j\omega L1 + \frac{1}{j\omega C2}} + \frac{1}{j\omega L2 + \frac{1}{j\omega C3}} == 0 \quad (6.4)$$

a resonance occurs. By solving the equation above, the resonant frequencies for the circuit are:

$$f_r = \frac{1}{2\pi} \sqrt{\frac{\frac{1}{2C1L1} + \frac{1}{2C2L1} + \frac{1}{2C1L2} + \frac{1}{2C3L2} \pm i\sqrt{-4iC1C2(iC1 + iC2 + iC3)C3L1L2 + (-iC1C2L1 - iC2C3L1 - iC1C3L2 - iC2C3L2)^2}}{2C1C2C3L1L2}} \quad (6.5)$$

Two solutions are obtained for the equation above indicating that the circuit in Figure 6.3 has 2 resonant frequencies; 5.008 GHz and 3.151 MHz. The input impedances looking from the device's internal plane can be calculated as below;

$$Z_{in} = \frac{1}{j\omega C1 + \frac{1}{j\omega L1 + \frac{1}{j\omega C2}} + \frac{1}{j\omega L2 + \frac{1}{j\omega C3}} + \frac{1}{\frac{1}{j\omega C4} + 50}} \quad (6.6)$$

By adding the series LC network to the circuit shown in Figure 6.3, the resonant frequency has been increased from 701.324 MHz to 5.008 GHz. However, a low frequency resonant circuit also exists. The input impedances at the low resonant frequency shown in Figure 6.4(b) is high, which can affect the VBW performances. However, the analysis for this circuit only considers ideal circuit components. In reality, circuit components such as the capacitors, exhibits self-resonant properties. In this work, the 1 uF C3 ideal capacitors are replaced with Murata SMD ceramic capacitor, that has an ESL value of approximately 0.8089 nH.

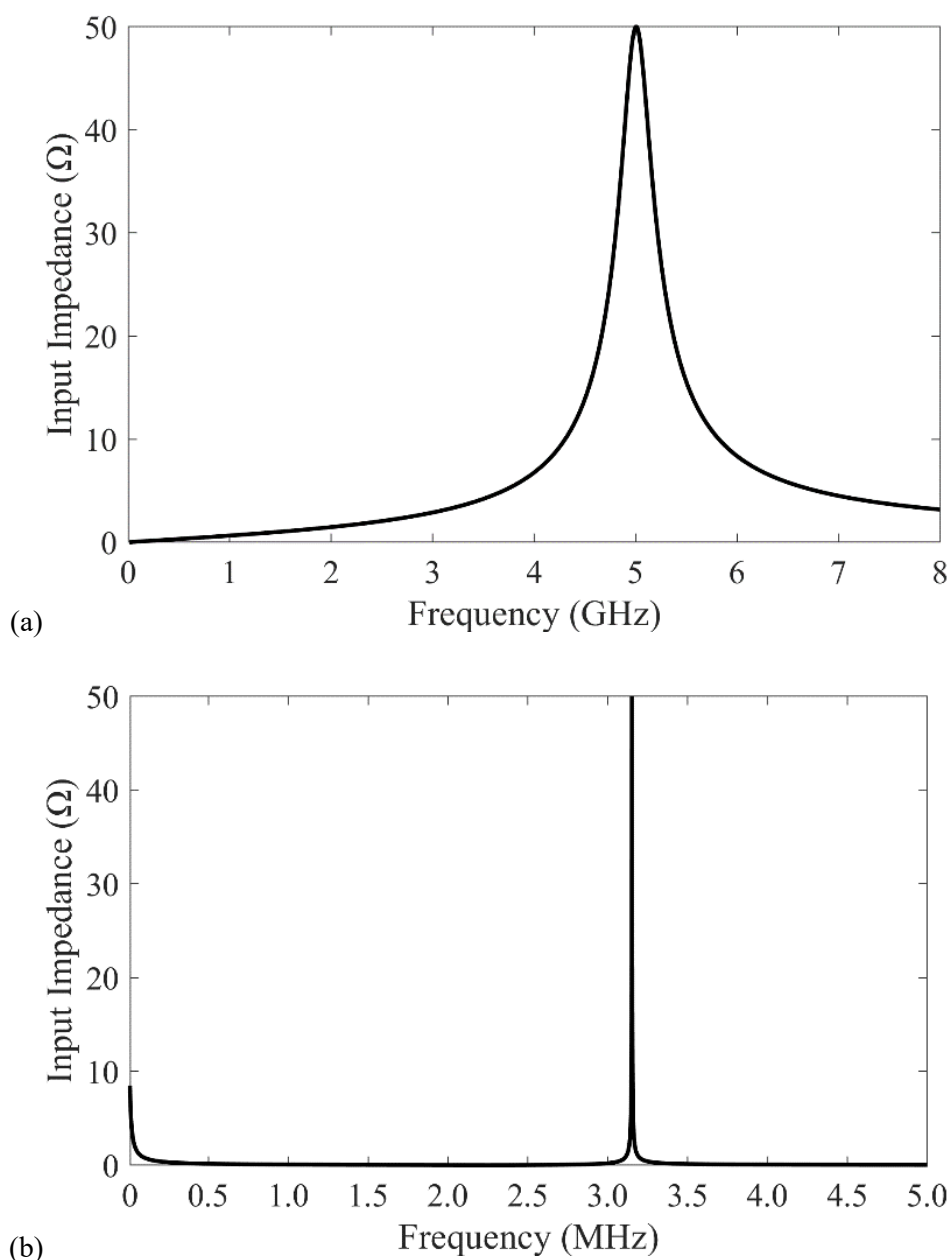


Figure 6.4. Input impedances at the high (a) and low (b) resonant frequencies.

Figure 6.5(a) shows the new circuit by replacing the ideal capacitors at the RF decoupling and the baseband termination circuit with Murata 1  $\mu\text{F}$  ceramic capacitors. In Figure 6.5(b), these capacitors are replaced with its equivalent circuit components consisting of ESR and ESL of 0.01  $\Omega$  and 0.8089 nH respectively. L1 is a bias feed inductor with a value of 5 nH (fixed) while L3 is the low inductance bondwires in the baseband termination circuit with a value of 0.1 nH. C1 represents device's output

parasitic with a value of 10.3 pF while C4 is the DC blocking capacitor with a value of 30 pF.

Total impedances of the circuit in Figure 6.5(b) is

$$X_T = \frac{1}{j\omega C1 + \frac{1}{j\omega L1 + \frac{1}{j\omega C2} + j\omega L2} + \frac{1}{j\omega L3 + \frac{1}{j\omega C2} + j\omega L4}} \quad (6.7)$$

If the denominator of the above equation is equal to zero, the resonant frequencies for the circuit are:

$$f_r = \frac{1}{2\pi} \sqrt{\frac{\frac{C2C3(L1 + L2 + L3 + L4) + C1(C2(L1 + L2) + C3(L3 + L4))}{2C1C2C3(L1 + L2)(L3 + L4)} \pm \sqrt{\frac{4C1C2C3(C1 + C2 + C3)(L1 + L2)(L3 + L4) - (C2C3(L1 + L2 + L3 + L4) + C1(C2(L1 + L2) + C3(L3 + L4)))^2}{2C1C2C3(L1 + L2)(L3 + L4)}}} \quad (6.8)$$

By inserting the values of the components in Figure 6.5(b) into (6.8), the resonant frequencies are 1.769 GHz and 2.746 MHz. The input impedances from the circuit are calculated in (5.9). Although the high resonant frequency is lowered to 1.769 GHz, however, the low resonant frequency shown in Figure 6.6(b) has a small value of input impedances ( $\approx 0.1 \Omega$ ) at low resonant frequency.



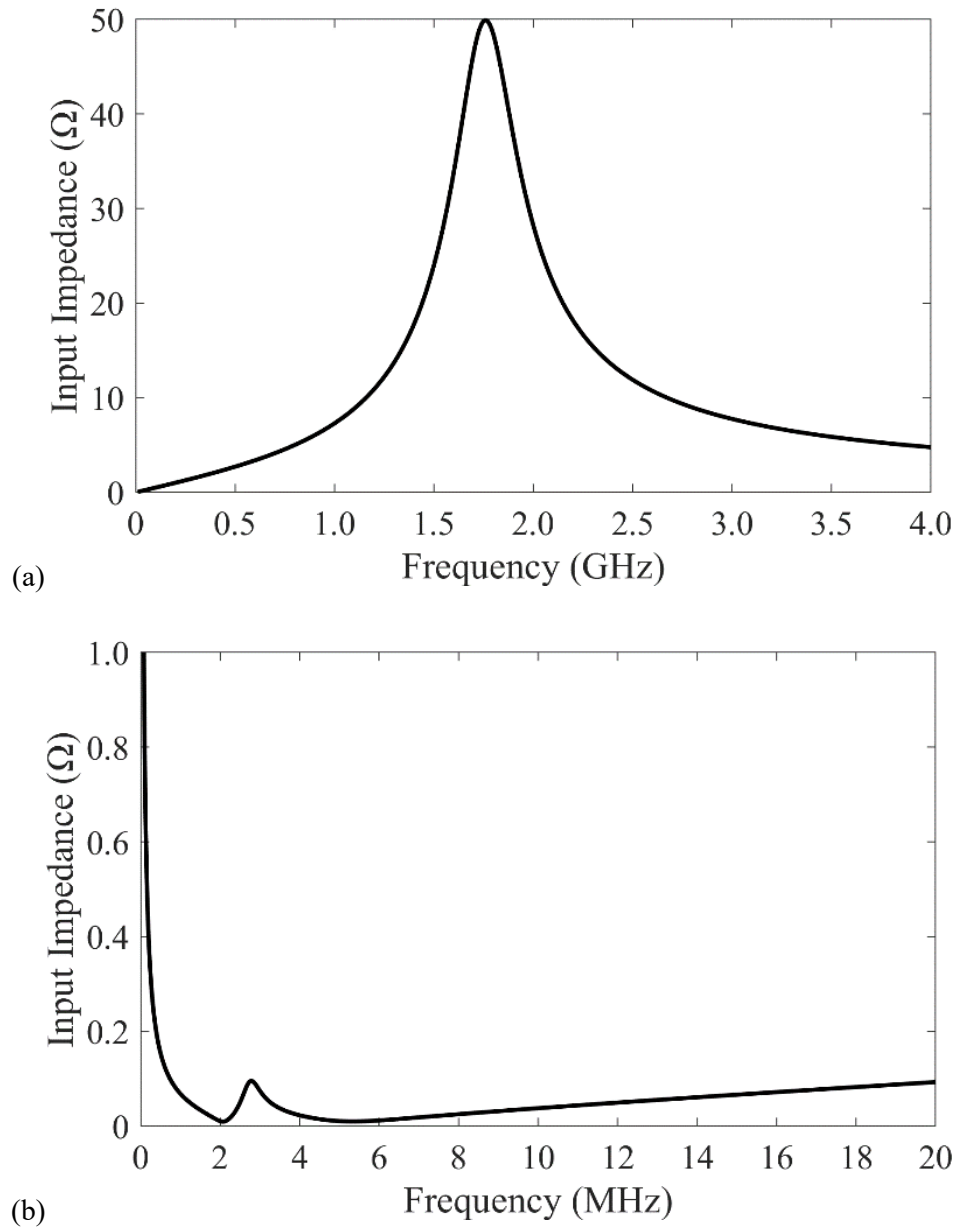


Figure 6.6. Input impedances for network in Figure 6.5 at (a) GHz frequencies, showing the high resonant frequency and (b) scaled down to MHz frequencies, showing the low resonant frequency.

The proposed additional series LC network to the device's output indicates that it can increase the VBW by shifting the resonance to a higher frequency, and also reduce the input impedances of the low frequency input. This network has 2 resonances, at low and high resonant frequencies. Due to self-resonant properties of capacitors, the low

frequency resonance does not affect the LF impedances compared to the analysis made on the ideal components. These analyses are summarised in Table 6.1.

Table 6.1. Comparisons between different analysis of normal bias network, and with additional VBW enhancement circuit.

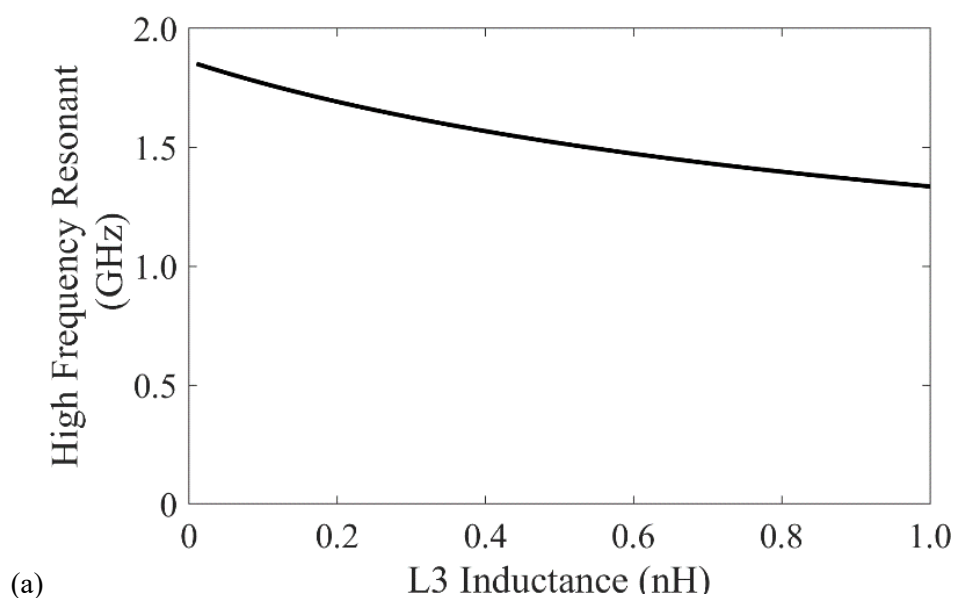
<b>Circuit configuration</b>	<b>Normal output parasitic capacitance and bias circuit</b>	<b>Additional series low inductance and high capacitance for extending VBW</b>	<b>Additional series low inductance and high capacitance for extending VBW  (Ideal capacitor is replaced with equivalent circuit)</b>
<b>Resonant frequency</b>	678 MHz	High = 5.005 GHz Low = 3.152 MHz	High = 1.76 GHz Low = 2.783 MHz
<b>Input impedance at resonance</b>	$\approx 50 \Omega$	High = $50 \Omega$ Low = $\rightarrow \infty$	High = $50 \Omega$ Low = $0.1 \Omega$

### 6.3 High Value Capacitor with Low ESL for Further Extending VBW Performances

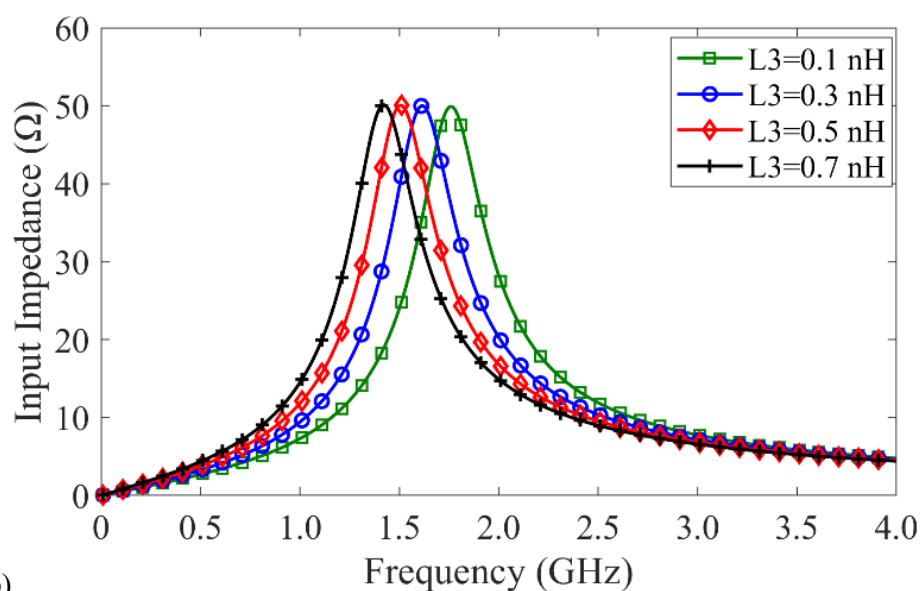
The proposed baseband circuit to increase the VBW performances in broadband RF PA are explored in the previous section. The baseband termination circuit consists of series low value inductance and high value capacitance that can be implemented inside the transistor package. The low value inductor can be replaced with short bondwires while the high value capacitor may be implemented using ceramic capacitors or single layer capacitor. The initial investigations in previous section only quantify for a single fixed value for these components, in which, 0.1 nH inductor is used in series with 1uF ceramic capacitor from Murata with a high breakdown voltage. Sensitivity analysis are carried out in this section, to quantify the effect of using different values of these components on the resonant frequencies and the input impedances.

The first analysis is carried out on the low value inductor, L3 from Figure 6.5(b) which will be assembled using bondwires. By increasing the value of this inductor, the resonance at the high frequency shown in Figure 6.7(a) decreases. Although the peak input impedance is constant with these changes, however, the instantaneous input impedances at each interval frequency increase when the value of the inductor is increased. For instance, the input impedance for the circuit at 1 GHz is almost 10  $\Omega$  when the value of the low value inductor, L3 is set to 0.7 nH, compared to L3 = 0.1 nH. In this case, careful choice should be made so that the bondwires' inductance has a low value as possible by keeping it short. On the other hand, the low resonant frequency in Figure 6.8 is almost constant when the inductor L3 is varied. Also, the peak value of the input impedances at these resonant frequencies are maintained low, even though the inductance values are increased.





(a)



(b)

Figure 6.7. Impact of varying the low value inductor from the additional VBW enhancement circuit on (a) high resonant frequency and (b) its input impedances.

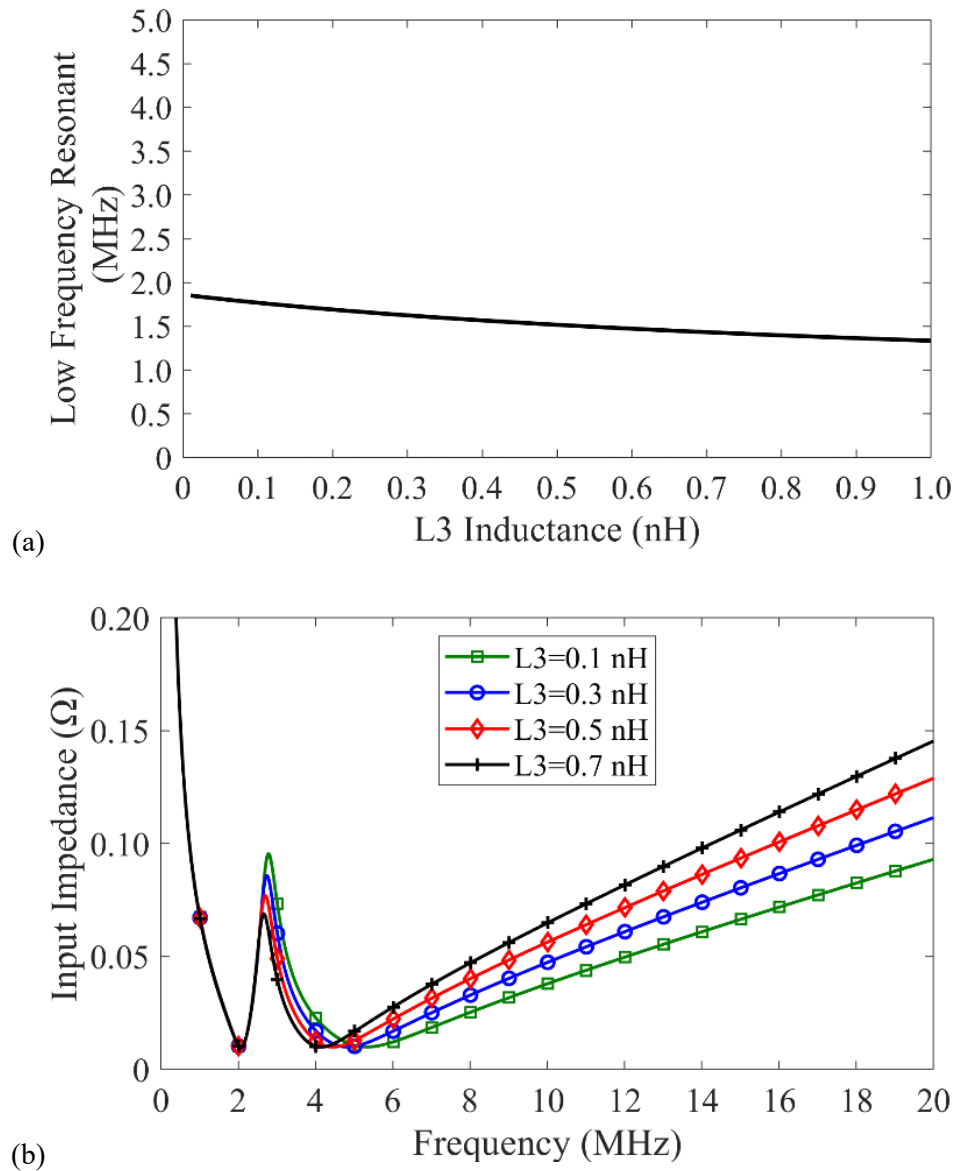


Figure 6.8. Impact of varying the low value inductor from the additional VBW enhancement circuit on (a) low resonant frequency and (b) its input impedances.

Next, the value of capacitor,  $C_3$  from Figure 6.5(b) is varied up to 2  $\mu\text{F}$  while keeping its self-resonant properties constant ( $\text{ESL}=0.8089 \text{ nH}$ ). The high frequency resonant and its input impedances remains unchanged when the capacitor's value are increased to 2  $\mu\text{F}$ . However, the changes for the low frequency resonant and the input impedances of the circuits are more visible when this capacitor's value is varied. The low frequency resonant is high, above 200 MHz when the capacitor  $C_3$  has a low capacitance value, below 100 pF. The low frequency resonant decreases to several MHz as the

capacitance of  $C_3$  increases to 2  $\mu\text{F}$ , as shown in Figure 6.9. Meanwhile, the input impedances of the circuit when the capacitor,  $C_3$  is varied between 0.05  $\mu\text{F}$  to 2  $\mu\text{F}$  are shown in Figure 6.10. It became a problem to extend the VBW of the RF PA circuit if the capacitor used in the series LC network is lower than 0.1  $\mu\text{F}$ , because, it will lead to a higher impedance at low resonant frequency. The input impedances at the resonant frequency reduces when the value of capacitance,  $C_3$  increases to 2  $\mu\text{F}$ .

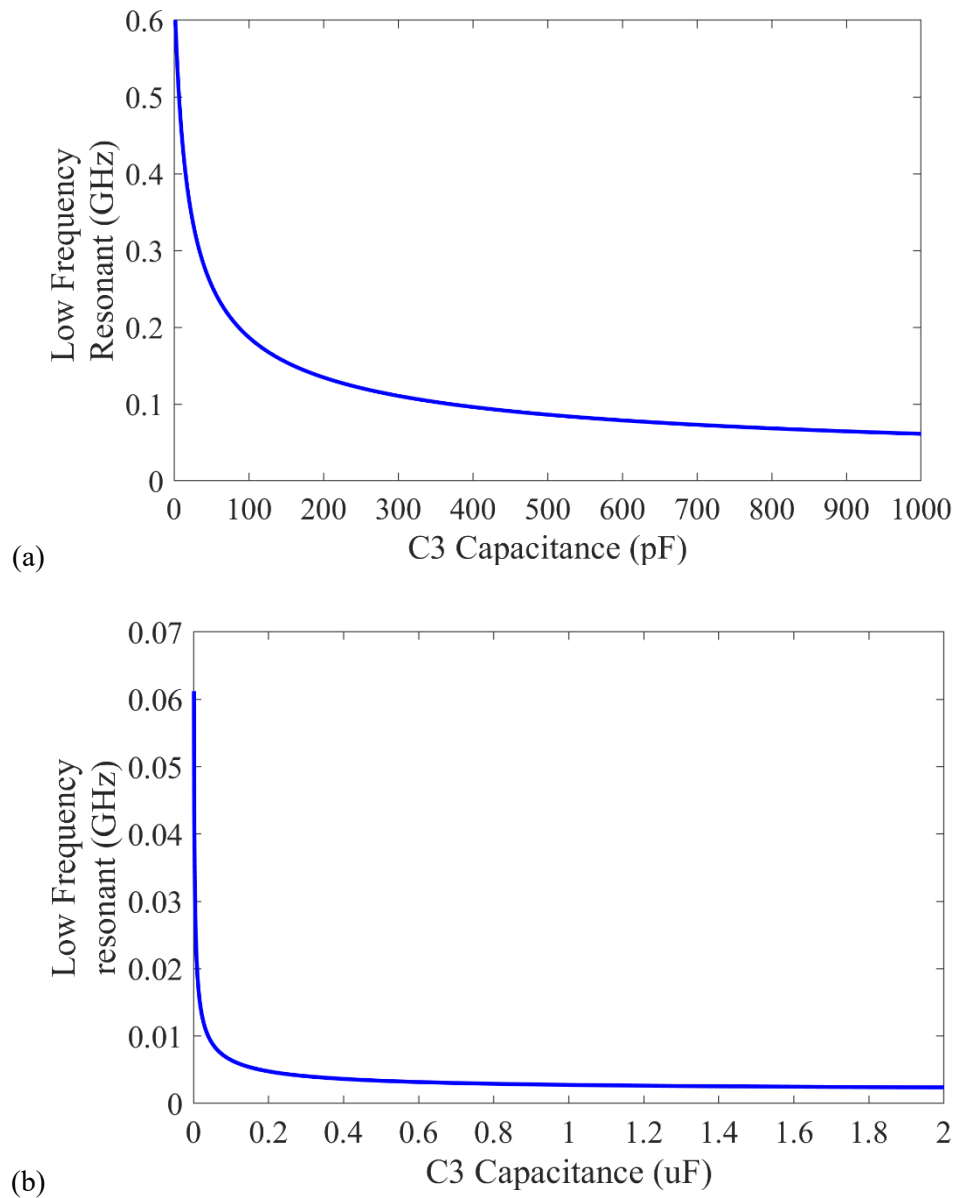


Figure 6.9. Impact of varying the values of high value capacitor,  $C_3$  from the additional VBW enhancement circuit on the low resonant frequencies. (a) up to 1000 pF and (b) up to 2  $\mu\text{F}$ .

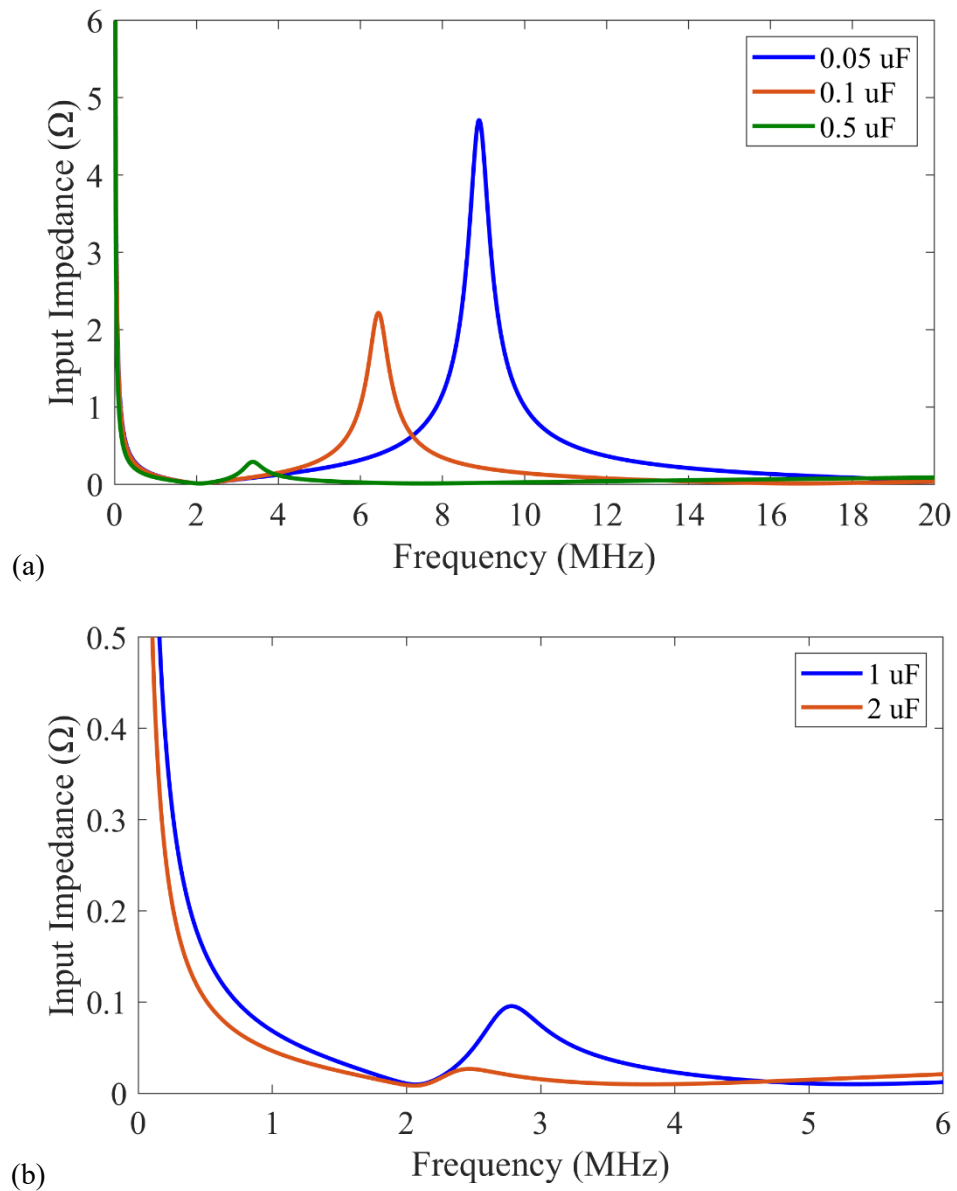


Figure 6.10. Impact of varying the high value shorted capacitor, C3 from the additional VBW enhancement circuit on the input impedances.

The next important investigation on this sensitivity analysis is observed when the self-inductance value,  $L_4$  from the capacitor in Figure 6.5(b) is varied. In this analysis, shown in Figure 6.11, the value of the self-inductance from the capacitor is varied while the capacitance of C3 is maintained at 1 uF. The high resonant frequency decreases while the input impedance increases when the self-inductance of the capacitor is increases. On the other hand, the low resonant frequencies are barely unchanged when the self-inductance values are varied, which is shown in Figure 6.12. Therefore, the VBW can be

greatly increases if the high value capacitor has a low value of self-inductance. Table 6.2 summarises the resonant frequency and the input impedances for the circuit from the sensitivity test of the additional LC network.

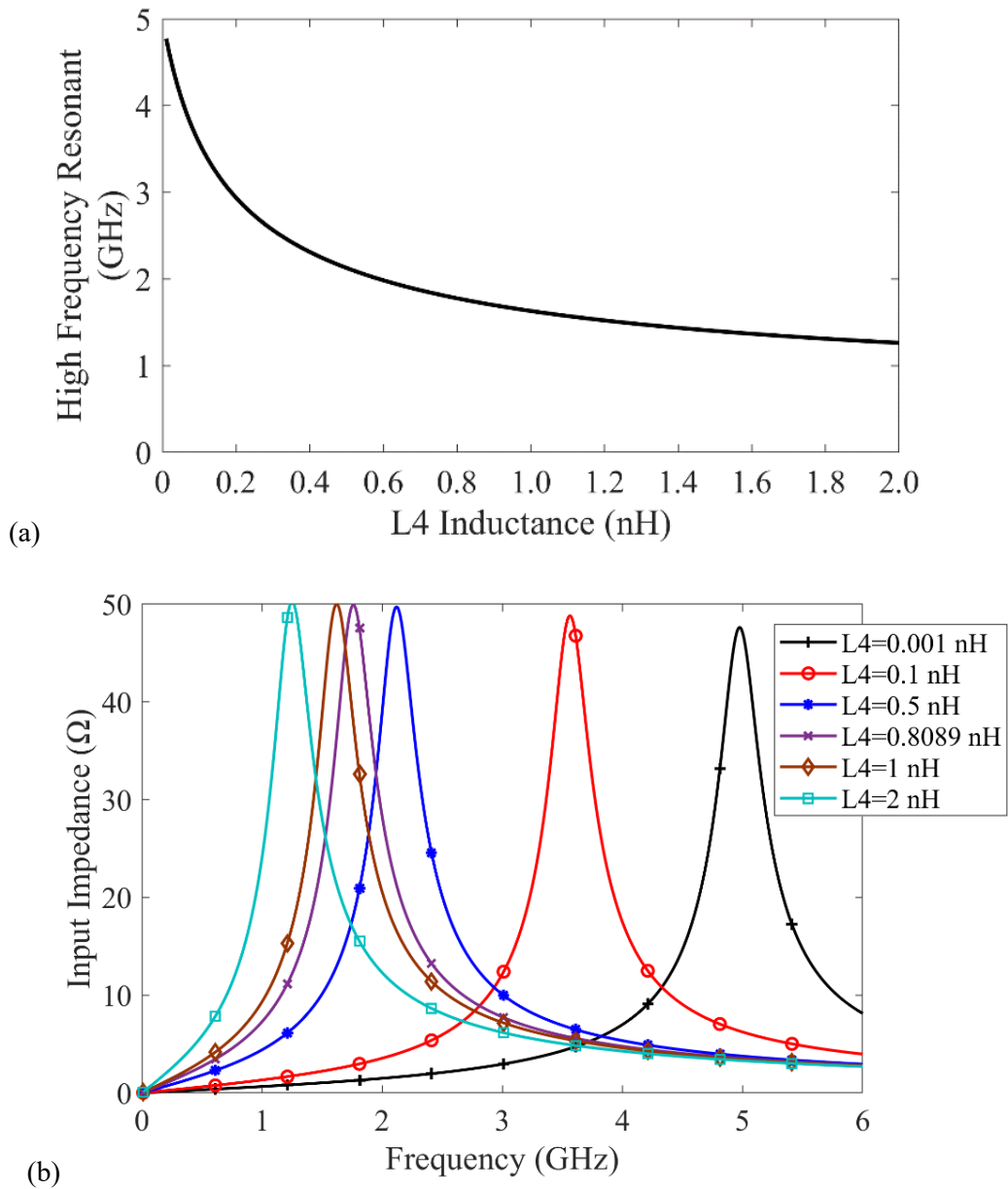


Figure 6.11. Impact of varying the self-inductance value of the shorted capacitor from the additional VBW enhancement circuit on (a) high resonant frequency and (b) its input impedances.

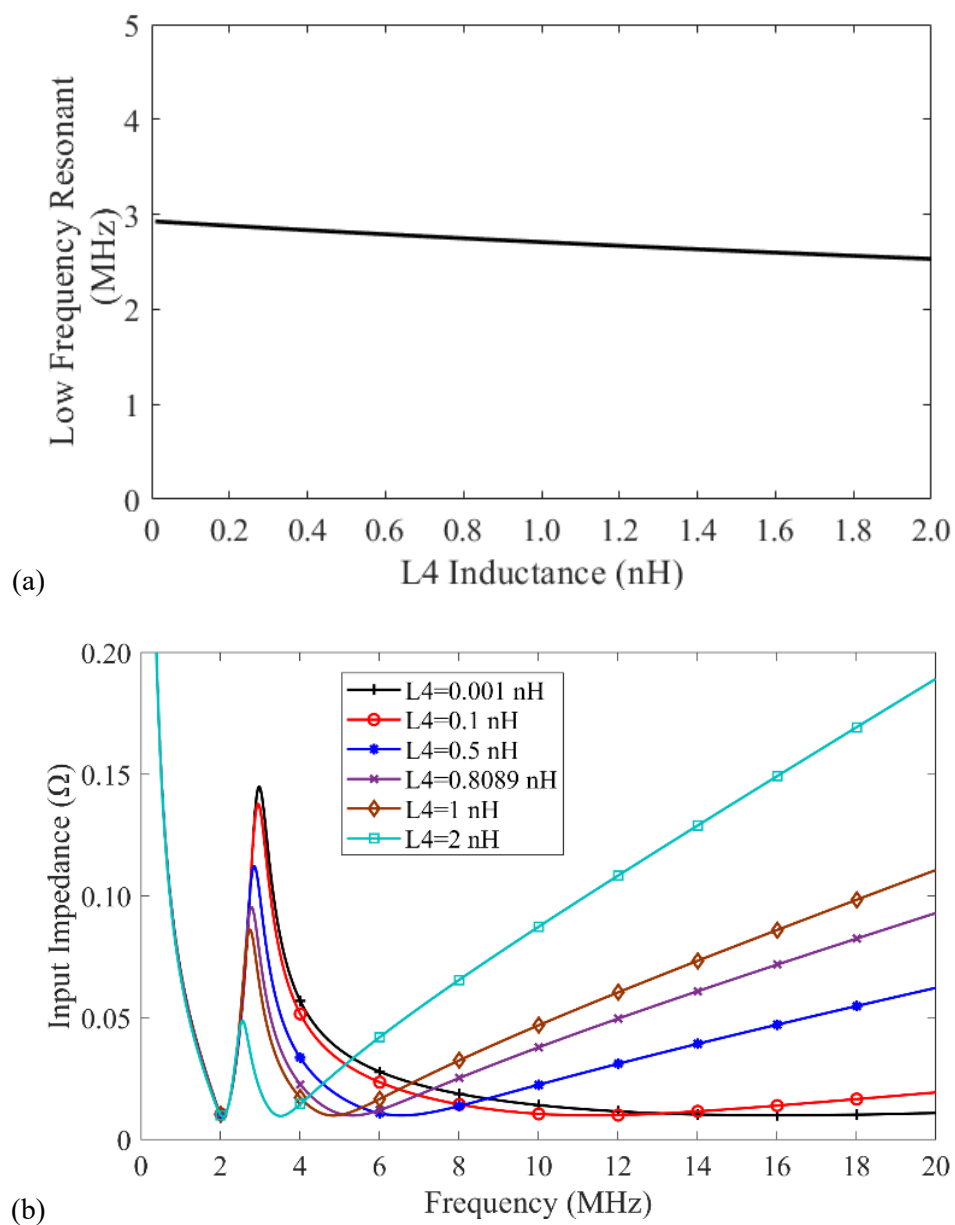


Figure 6.12. Impact of varying the self-inductance value of the shorted capacitor from the additional VBW enhancement circuit on (a) low resonant frequency and (b) its input impedance.

Table 6.2. Summary for sensitivity analysis of circuit in Figure 6.5(b) by varying the value of components in the added LC network for VBW enhancement on the resonant frequencies and input impedances.

	High resonance		Low resonance	
	Resonant frequency	Input Impedance	Resonant frequency	Input Impedance
Inductor, L3	Decreases with increasing value L3	Slightly increases with increasing value L3	Almost constant	Maintained low
Capacitor, C3	Maintained high, by lowering the capacitance value	Constant	Increases with decreasing capacitance value	Increases with decreasing capacitance value  Severely affect VBW performance for C3 value below 0.1 $\mu\text{F}$
Capacitor's self-inductance, L4	Decreases with increases value L4	Increases with increases value L4  VBW can be increases with low value L4	Almost constant	Maintained low for L4 value between 0.1 nH to 2 nH

## 6.4 Chapter Summary

This chapter has provided the analyses of circuit configurations with baseband termination circuit on the PA's resonances and the input impedances on the output of the circuit. The baseband termination circuit consisting of shunted high value capacitors connected close to the device using a small value inductor for connection. Using the equivalent circuit for the high value capacitor, it was found that the resonant frequencies shifted above 1 GHz, when comparing to a classical circuit without baseband termination circuit. However, a lower resonant frequency arose due to the integration of this baseband termination circuit. A sensitivity analyses are performed on the circuit components within the baseband termination circuit. It was found that the inductor to connect between the device and the shunt capacitor has to have lowest value of inductance to increase the high resonant frequency. The capacitance value of for the shunted capacitor has to be as high as possible, ideally above 1  $\mu\text{F}$ , to keep the input impedance of the circuit as low as possible at the lower resonant frequency. Finally, the equivalent series self-inductance associated with the high value capacitor has to have an inductance value as low as possible, to shift the high resonant frequency further from 1 GHz.



# Chapter 7

## Compact Broadband PA with Integrated Matching and VBW Extension

### 7.1 Introduction

Most of available packaged transistors consist of a transistor die attached with bondwires to the transistor package's gate and drain tabs. The bondwires provide finite inductances associating with parasitic capacitance due to the physical contacts between the bondwires and the landing pads [18, 52]. The integrated matching transistor, or pre-matched packaged transistor is becoming more popular at GHz frequencies as it provides excellent performances within the design bandwidth [18]. The matching networks inside an integrated PA typically consist of bondwires and single layer capacitors, that are all arranged as a stack LC network to provide fundamental and/or harmonic matching to the device. Harmonic tuning is usually employed in integrated matched PAs, boosting the efficiencies and overall performance over broad frequency bands [22, 82, 83, 102, 103, 104, 105]. The packaged PA in [22] for example is harmonically tuned to boost the packaged transistor performance. The integrated matched PAs in [82, 83] contain of

internal input and output harmonic matching, whereas the fundamental and biasing circuit are implemented using microstrip lines. A pre-matched packaged PA is designed in [106], in which the PA only operates at 3.5 GHz. In [102], the input and output matching networks are fully designed using bondwires and single layer capacitors, thus reducing the total size of the PA.

Additional baseband termination circuits, such as described in Chapter 6 have been integrated in compact PA designs [96, 97, 98, 101], where these PAs are realised using integrated matching circuit, consisting of bondwires and single layer capacitors. These PAs are designed such that the bondwires connection between the transistor die and high value capacitors are made as close as possible. Further advanced PA design techniques utilising the integrated PA matching include the packaged-integrated outphasing PA [46, 47].

This chapter will combine the design theories described in all the previous chapters to design a compact PA with high efficiencies and enhanced VBW performances over a broad frequency band, using integrated matching networks. A 15 W GaN (CGH60015D) die from Wolfspeed [107] is used to design the PA. The PA is designed such that the OMN presents fundamental and 2<sup>nd</sup> harmonic impedances close to the  $\alpha = -1$  region, to the device's CGP across a wide bandwidth, to achieve the highest efficiencies and have a wide separation between device's power and efficiency contours. Integrated matching networks are used to partially match the input of the PA while fully matching the fundamental and 2<sup>nd</sup> harmonic frequencies at the device's output. The PA is designed on an open board, without any enclosed package to remove any packaging-size limitation to prove the design theories. The VBW extension circuit is embedded in the design using the available high value and wire bondable capacitor from Knowles Capacitors [108].

This capacitor has a capacitance value of 10 nF, and working up to 40 GHz with high 100 V breakdown voltage, enabling it to be integrated with a GaN device.

The PA is designed and simulated in 3D EM software, EMPro, enabling the computation of additional mutual inductances and magnetic coupling between the components inside the circuit. The simulated S-parameter files from the 3D EM solver are imported back into ADS to compute the circuit performances. A set of simulations are performed on the PA using CW, 2-tones signal and modulated signals to evaluate its broadband and VBW performances. Finally, a narrowband outphasing PA is designed and simulated using a Chireix combiner to combine the outputs of the two similar PAs.

## 7.2 15 W GaN Bare Die Device Characterisation in CCF Mode

### 7.2.1 C<sub>ds</sub> Parasitic Drain Capacitance Extraction

A bare die discrete transistor has fewer output parasitics associated with it because this device does not contain internal bondwires, compared to commercially available packaged transistors. This means that, such package parasitic components, consisting of internal bondwires,  $L_p$  and package capacitance,  $C_p$  can be taken out from the parasitics component for the transistor physical modelling. The transistor die's output parasitics can be modelled by an output drain capacitance,  $C_{ds}$  only. The value of  $C_{ds}$  is extracted from the  $S(2,2)$  coefficient from the s-parameter, obtained through the device's simulation. This  $C_{ds}$  value depends on the drain bias and frequency of operation. The  $C_{ds}$  value is approximately 1.3 pF at 28 V drain bias and at frequency operation of 2.0 GHz. Figure 7.1 shows the extracted values of  $C_{ds}$  that shows an exponential increment up to 10 GHz.

According to [109, 110], the device's resonance can be measured using S21 probe between device's drain and the bias network. Figure 7.2 show the simulation performed on the device's model with the S21 probe to obtain the device's resonance. The device is biased with 28 V at the drain through a 10 nH inductance to provide isolation for the RF signal into DC supply. The gate and the source of the device is terminated to the ground. A DC blocking capacitor and 50  $\Omega$  load termination is connected to the device output. The S21 probe is connected in between the device's extrinsic plane and the bias network. Similarly, the device can be modelled with only drain parasitic capacitance,  $C_{ds}$  as shown in Figure 7.3. Here, the drain DC voltage supply is removed from the circuit simulation.

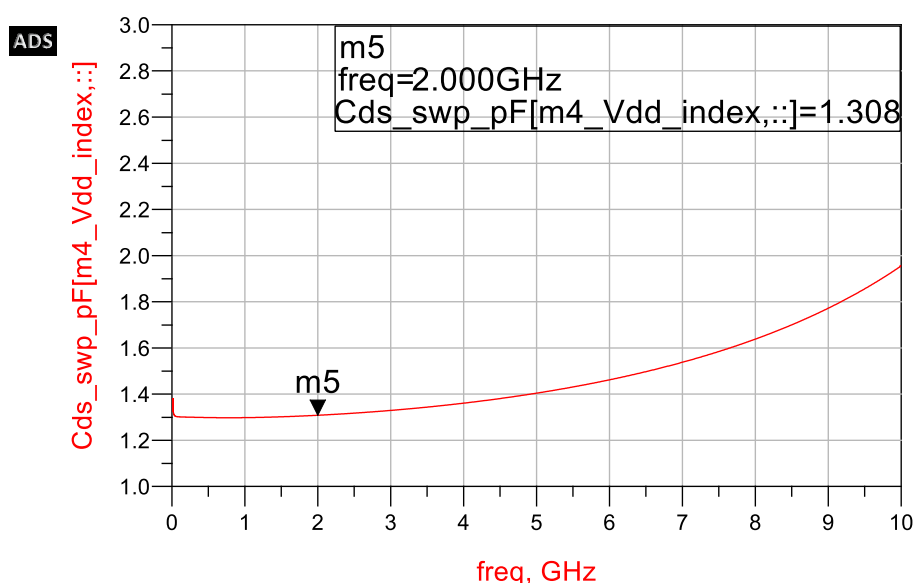


Figure 7.1. Parasitic drain capacitance,  $C_{ds}$  extracted from 15W bare die transistor bias with 28V at the drain.

The comparisons of S21 resonance between the 2 circuits in Figure 7.3 are shown in Figure 7.4. The resonant frequency obtained from simulation using device's model is 540 MHz with a few offsets of resonant frequencies obtained using device's  $C_{ds}$  only, that is 580 MHz. The magnitude difference between the two modelling approaches is only 1.1 dB. Another resonance is observed when actual device's model is used, at frequencies

higher than 1 GHz, which indicates the non-linear behaviour of the device that cannot be simply modelled with the equivalent circuit in Figure 7.3(b). However, at the lower frequency below 1 GHz, the resonances obtained between the two modelling approaches are fit almost perfectly well. Also, the input impedances seen from the device in Figure 7.5, shows a similar projection in the Smith chart for both simulation techniques at frequencies below 1 GHz. As a conclusion for this section, the bare die GaN device can be simply modelled with output parasitic capacitances,  $C_{ds}$  only.

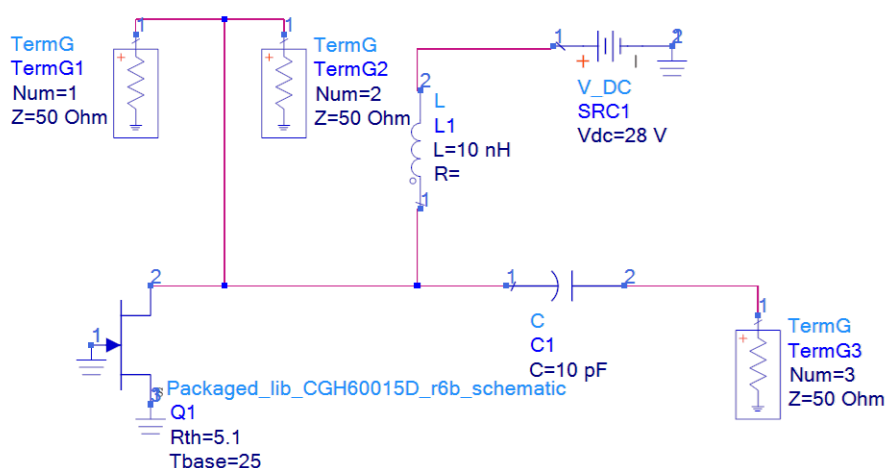


Figure 7.2. Simulation using S21 probe (using termination 1 and 2) to determine resonant between transistor's drain output and the bias network using the device's model.

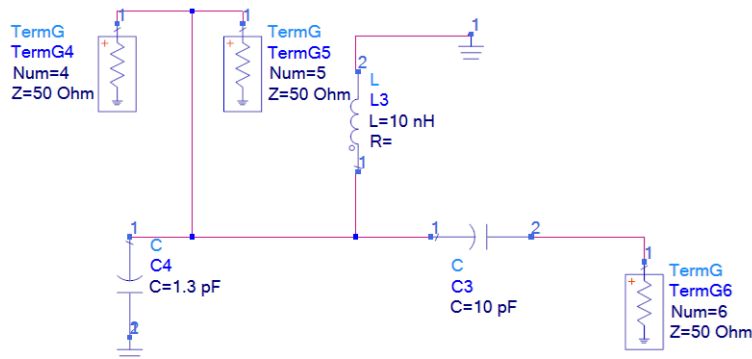


Figure 7.3. Simulation using S21 probe (using termination 4 and 5) to determine resonant between transistor's drain output and the bias network using the device's drain parasitic capacitance,  $C_{ds}$ .

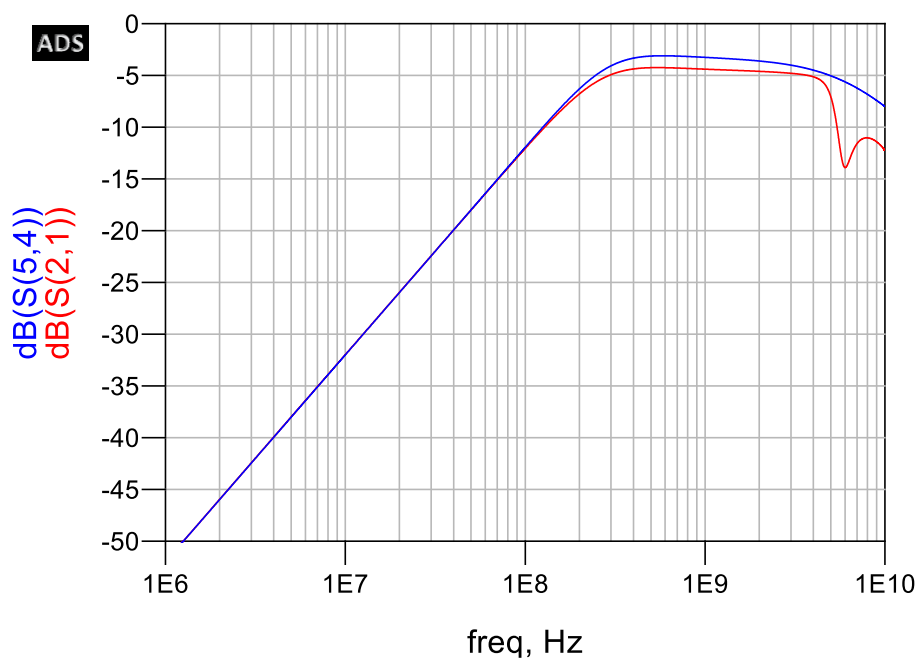


Figure 7.4. Output resonant between transistor and bias network simulated through device's model (S2,1) and  $C_{ds}$  S(5,4).

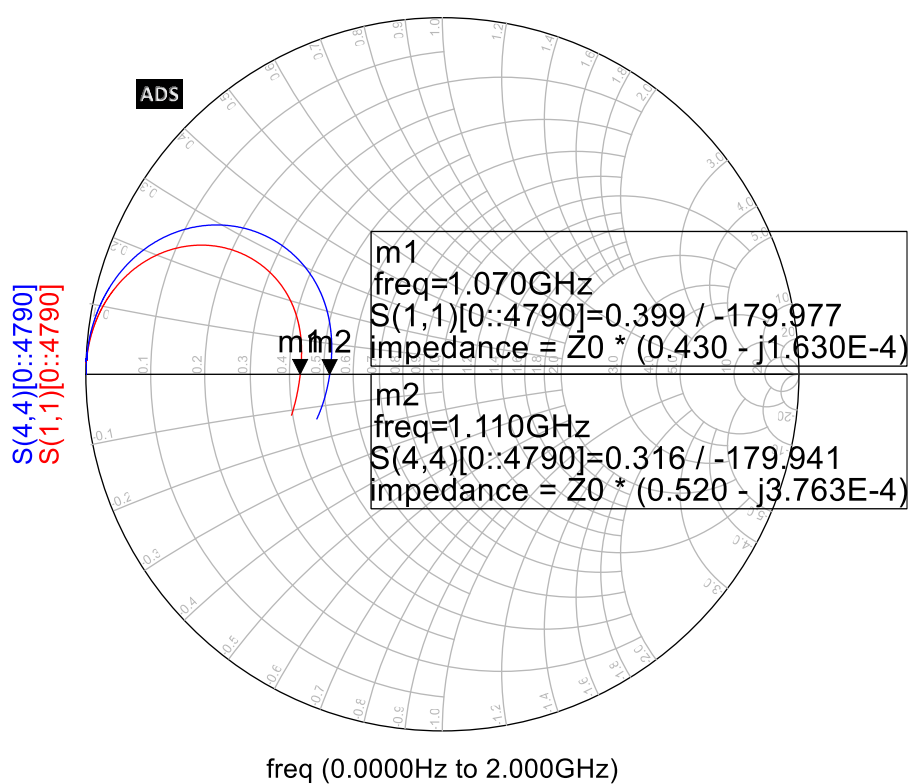


Figure 7.5. Impedances seen from the device simulated through device's model S(1,1) and  $C_{ds}$  S(4,4).

## 7.2.2 CCF Mode - Finding Optimum Impedances

Load-pull simulation is performed on the 15 W GaN device by varying the fundamental impedances across entire Smith chart while sweeping the phase of 2<sup>nd</sup> harmonic impedances across the edge of Smith chart. Meanwhile, the 3<sup>rd</sup> harmonic impedance is kept at open circuit. The device is biased at 28 V at the drain and -3 V at the gate, drawing a current of 69 mA. To simulate the CCF mode on this device, all these impedances are presented to the device's current generator plane, by a simple solution of only using negative value of the parasitic drain capacitance,  $C_{ds}$ , with a value of -1.3 pF that was obtained in Section 7.2.1. The optimum peak Pout and DE impedances with respect to the 2<sup>nd</sup> harmonic impedances obtained from this simulation are shown in Figure 7.6.

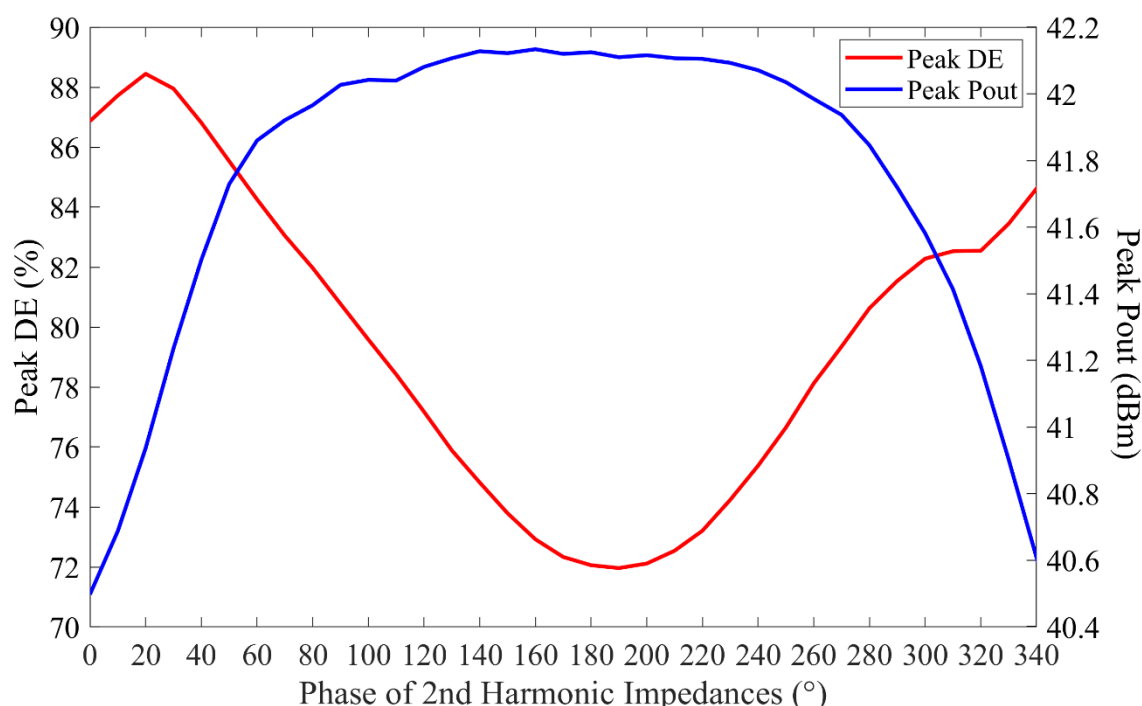


Figure 7.6. Optimum peak DE and Pout from fundamental load-pull 15 W GaN die with sweep phase of 2<sup>nd</sup> harmonic impedances at CGP (1.8 GHz).

It can be seen that the peak DE is at the minimum when the 2<sup>nd</sup> harmonic impedances presented to the CGP is at the short circuit (phase = 180 °). The DE

performances is almost symmetrical at this phase, reaching the peaks when the phase of 2<sup>nd</sup> harmonic impedances is moved towards open circuit, either through inductive or capacitive region. The CCF mode exist approximately when the phase of 2<sup>nd</sup> harmonic impedances are between 80 ° to 280 °, where at these states, the peak output power is over 15 W. Beyond this region, the peak output power drops lower than 15 W, although the peak drain efficiency continue to rise.

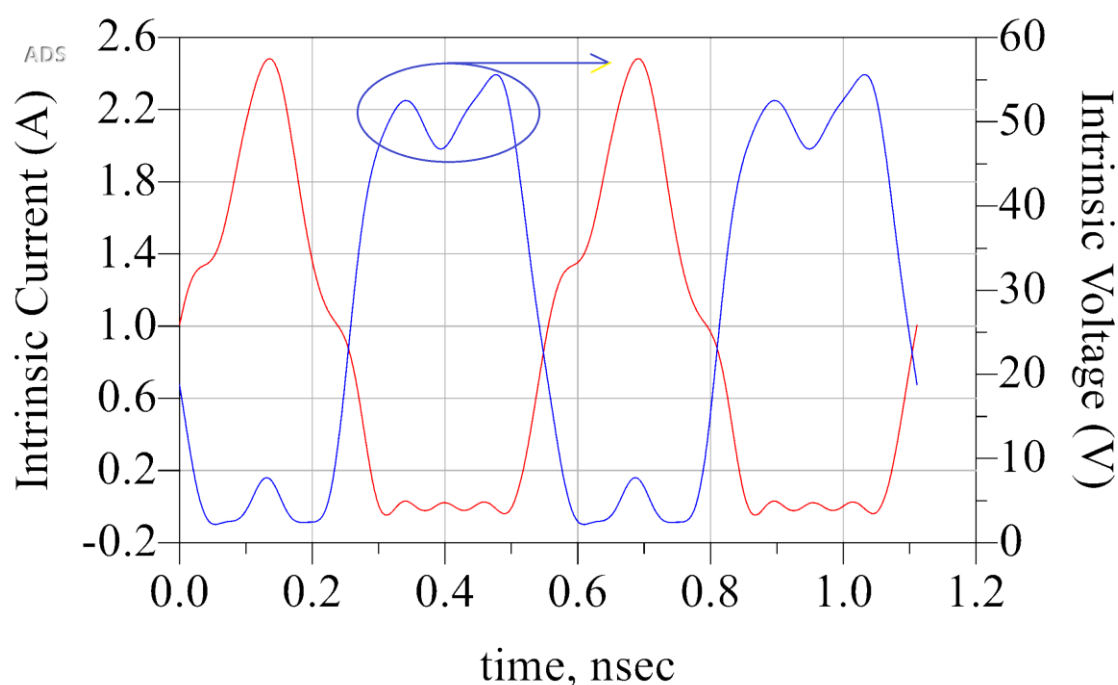


Figure 7.7. Waveforms of class-F mode from de-embedded load-pull simulation.

To verify the waveforms at the CGP plane from the -Cds de-embedding, the class-F mode waveforms are presented in Figure 7.7. Here, the waveforms are obtained when the 2<sup>nd</sup> harmonic impedance is presenting short circuit at the device's CGP and the fundamental impedance is at the optimum Pout impedance,  $23 + j0 \Omega$ . The drain voltage waveform is square wave-shape while the drain current waveform is a half-rectified sinusoidal wave-shape with a knee clipping. The load-line for this waveform is shown in



Figure 7.8, overlapping with the simulated DCIV characteristics. Due to small current drawn by the device as the device is biased in class-AB mode, the conduction angle for the current waveform is larger than  $180^\circ$ , changing the load-line shape slightly from the ideal class-F mode load-line. However, this biasing is chosen to have a trade-off between gain, efficiency and linearity for the PA.

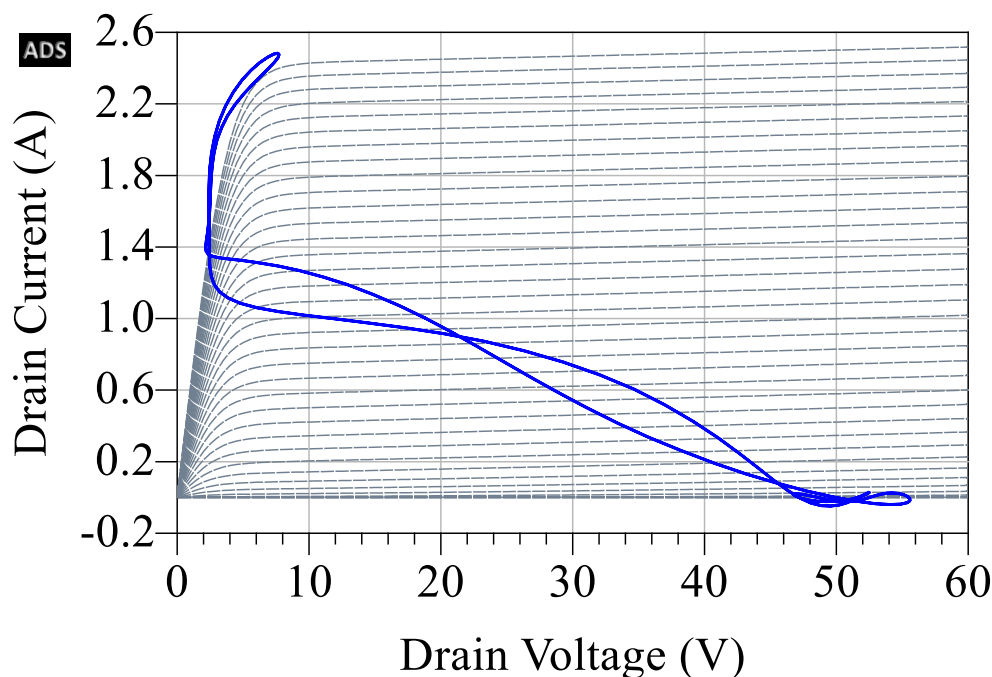


Figure 7.8. Load-line of class-F mode from de-embedded load-pull simulation.

Next, similar load-pull simulations are performed at the device's plane at the lower and higher end frequency for the PA. These simulations are performed so that it is easier to define the target impedances that are required for the design of the broadband output matching network. Also, the design space for targeting the  $\alpha = -1$  region across the bandwidth can be determined. Figure 7.9 shows the fundamental load-pull simulation with swept 2<sup>nd</sup> harmonic impedances performed at the device plane at 1.8 GHz and 2.7 GHz. At 1.8 GHz, the  $\alpha$  space across the device's plane exists when the phase of 2<sup>nd</sup> harmonic impedances are swept approximately between  $95^\circ$  to  $140^\circ$  (clockwise rotation), where the dip of the peak DE at  $150^\circ$  indicates the operation of lower efficiency

of class-F mode. Meanwhile, the  $\alpha$  space for 2.7 GHz exists for the phase of 2<sup>nd</sup> harmonic impedances swept between 130 ° to 150 °. To design a broadband PA operating between these 2 frequencies within  $\alpha = -1$  region, the ideal rotation of the phase of 2<sup>nd</sup> harmonic impedances has to be in between the 90 ° to 0 ° (clockwise rotation). This will keep the efficiency high, not only at the peak power and 50  $\Omega$  load impedances, but also at the load modulated OPBO.

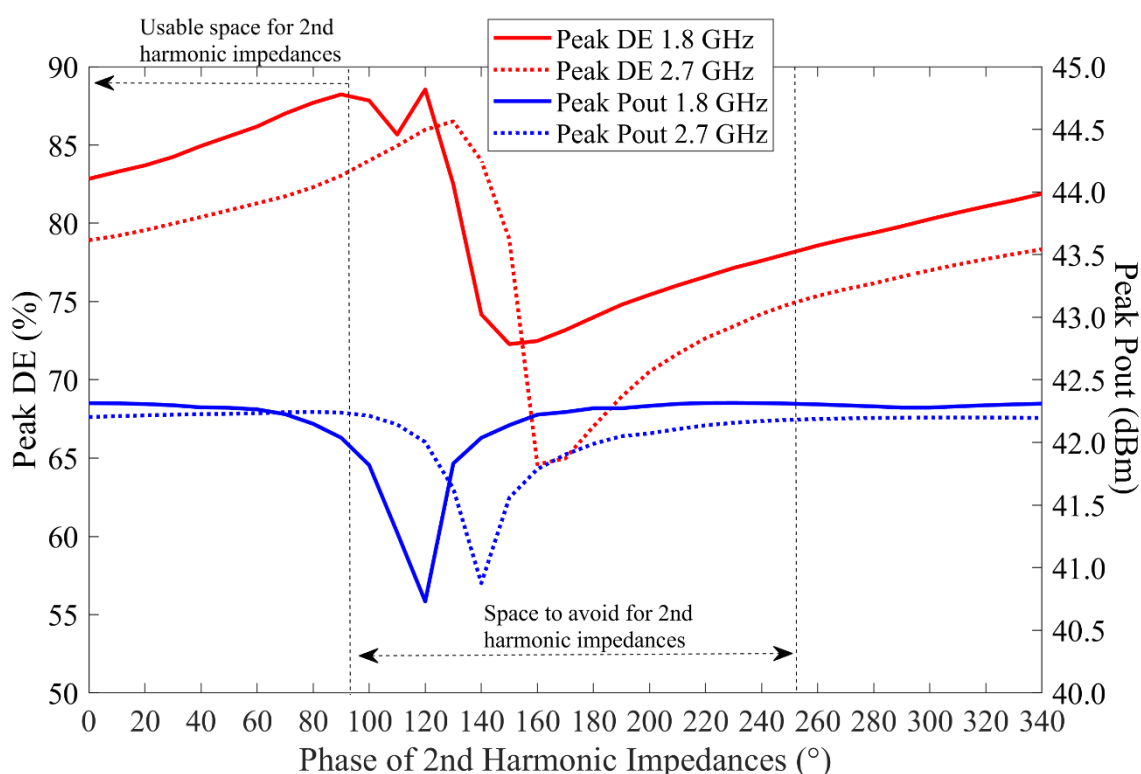


Figure 7.9. Optimum peak DE and Pout from fundamental load-pull of 15 W GaN die with sweep phase of 2<sup>nd</sup> harmonic impedance at the device's plane.

Next, the optimum impedances across the design frequencies are investigated by targeting the 2nd harmonic impedances. To further improve the efficiency at peak and OPBO, the phase of 2nd harmonic impedance at 1.8 GHz, 2.2 GHz and 2.7 GHz are chosen to be at 100 °, 95 ° and 80 °. Fundamental load-pull simulation is performed at the device's extrinsic plane across these frequencies and the setting of the 2nd harmonic impedances. Figure 7.10 shows the rotation of the Pout and DE contours for the 3 frequencies with respect to its 2<sup>nd</sup> harmonic impedances terminations. The Pout and DE

contours are showing for  $>41.5$  dBm and  $>70$  % respectively. It can be seen that the Pout contours for 1.8 GHz is smaller than the other frequencies, because the targeted 2<sup>nd</sup> harmonic impedance is  $10^\circ$  higher than the maximum of ideal 2<sup>nd</sup> harmonic impedance range investigated in Figure 7.9. Nevertheless, the chosen target of 2<sup>nd</sup> harmonic impedance at the 1.8 GHz resulted into a larger separation between Pout and DE contours (shown in blue lines). Meanwhile, the contour separation is much closer at 2.7 GHz, due to 2<sup>nd</sup> harmonic impedances termination moving further from  $\alpha = -1$  region. This is the limitation to designing a broadband PA with large separation between Pout and DE contours across the bandwidth, and the necessity to limit the movement of the 2<sup>nd</sup> harmonic impedance in the matching network.

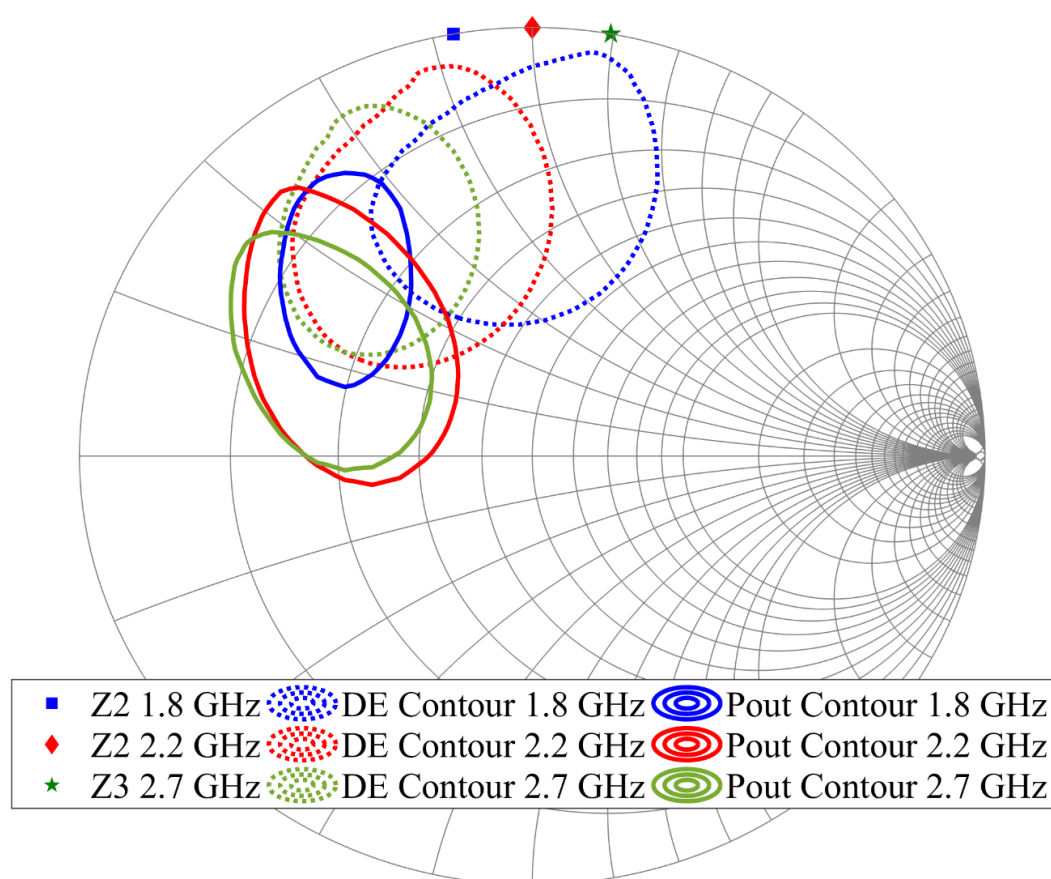


Figure 7.10. Simulated Pout contours ( $> 41.5$  dBm) and DE contours ( $> 70$  %) for different 2<sup>nd</sup> harmonic load impedances at 1.8 GHz, 2.2 GHz and 2.7 GHz from load-pull at the device's plane.

## 7.3 Matching Network Design using Ideal Components

It is easier to start designing the matching network for the PA using ideal components in ADS before converting and simulating it in 3D structures to take accounts of the coupling effects and other parasitics coming from the active and passive components within the actual circuit. Here, the integrated matching network is used for both input and output matching network to terminate fundamental and harmonic impedances to the device. Stacked LC networks are implemented in this design as they can provide both fundamental and harmonic matching and simplified the circuit layout [18]. Rogers RT/Duroids 5870 laminate is used for the microstrip circuit to provide termination and easy access for the RF input and output ports as well as the DC biasing terminals.

### 7.3.1 Ideal Input Matching Network

The ideal input matching network (IMN) designed for the PA is shown in Figure 7.11. Two stacked LC networks are used for the internal matching that provide partially fundamental matching to the device's input. The value of the capacitors is chosen to be within the available ATC's single layer capacitors custom design kit [111]. An additional small value inductor from the 2<sup>nd</sup> shunted capacitor from the device's gate is connected to the bias network that is implemented using  $\lambda/4$  microstrips line. A parallel LC component is used on the microstrip lines to provide stability for the device. An additional 150  $\Omega$  resistor is connected in series within the bias network to inhibit any current drawn into device's input, thus providing further stability and protection to the device. The fundamental matching network on the IMN has to be separated between integrated matching and microstrips line, because only the SMD resistors are considered for this design. Otherwise, the resistor could also be replaced with bondable resistor, that could further reduce the complexity and size for the IMN.

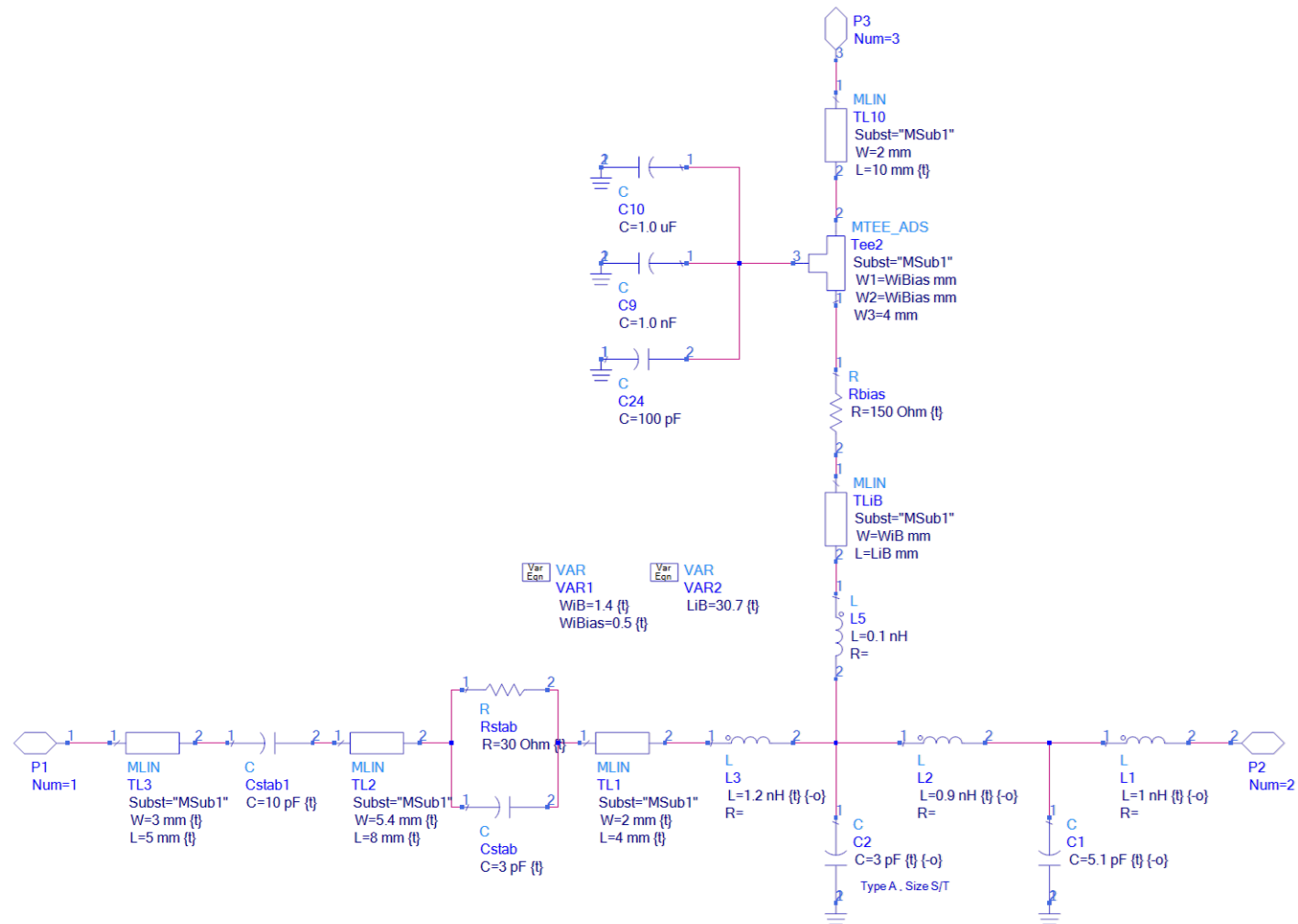


Figure 7.11. Ideal input matching network.

### 7.3.2 Ideal Output Matching Network

The ideal output matching network (OMN) in Figure 7.12 is designed by fully terminating the fundamental and 2<sup>nd</sup> harmonic impedances to the device using the stacked LC network. In order to fully match the fundamental impedances, 3 stacked LC networks are needed. In this design, the size of the OMN is further reduced by connecting the 3<sup>rd</sup> shunt capacitor from the device's drain to a 50  $\Omega$  microstrip line, through a single layer DC blocking capacitor. The use of a single layer capacitor for the DC blocking replaces the traditional bulky SMD capacitor. Similar to the IMN design approach, the value of the single layer capacitors in the OMN are chosen to be within the range available in [111]. The VBW extension network is integrated in the OMN by placing the Knowles 10 nF single layer capacitor [108] to the first matching capacitor from the drain tab, through a connection of bondwires. These bondwires have a high value of 2.5 nH, to block RF signal into the high value capacitor as it tends to be lossy within the RF frequency. An s2p file is provided by Knowles to model the 10 nF capacitor that can be simulated up to 40 GHz. This file gives accurate prediction for the performances of the capacitor when accounting the high frequency signal. The DC bias network is implemented using microstrip lines by connecting the 1<sup>st</sup> shunt capacitor to the  $\lambda/4$  line using bondwires that has a small inductance value.

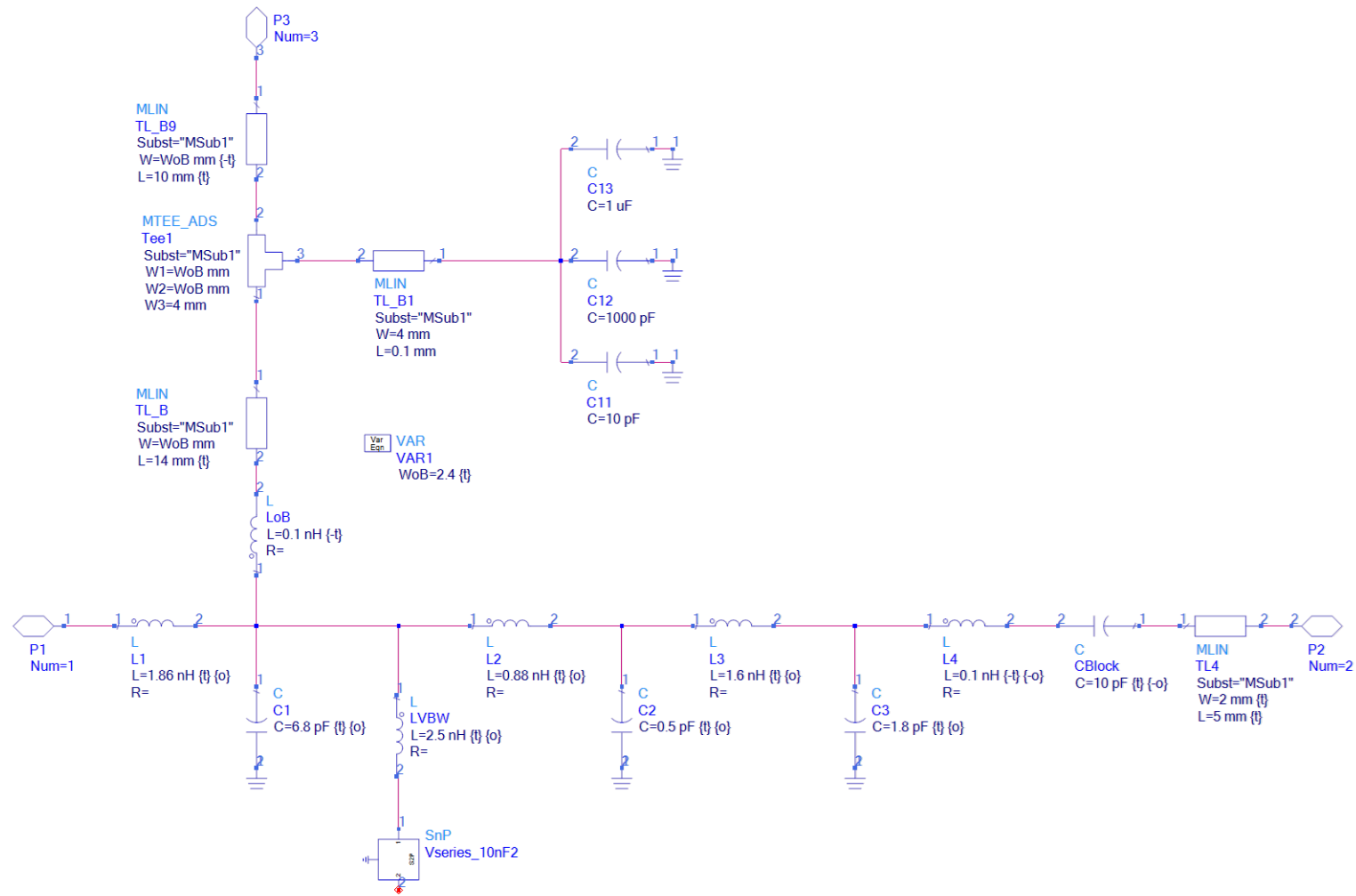


Figure 7.12. Ideal output matching network.

## 7.4 3D PA Model Implementation in EMPro

The IMN, OMN and the device are drawn in 3D EM simulator, EMPro. The 15 W GaN die device is drawn based on datasheet provided [107]. Two gold pads on the die are drawn for the gate and drain connectivity. The values of the single layer capacitors are selected based on the availability in ATC's single layer capacitor custom design kits [111], that has a similar or close values to the ideal design components. All of these capacitors are double plated with thin gold material between the dielectric material, which is suitable for both grounding and bondwires connection. The single layer capacitors also have a high breakdown voltage, ranging from 50 V to 100 V, which is suitable for the high voltage operation of GaN devices. The bondwire has a diameter of 2 mil (0.0508 mm). Copper plate is used to provide grounding for the transistor, single layer capacitors and the microstrip lines. The 3D PA with VBW extension design in EMPro is depicted in Figure 7.13. The PA has a total dimension of 40.4 mm x 28.0 mm x 6.0 mm. The ground copper plate is depicted as the golden metal block which holds all the active and passive devices. The green coloured block placed on top of the copper base is the dielectric of the laminate which has a dual copper cladding. The bottom copper cladding from the dielectric is attached to the copper base, while the top copper cladding is designed as the microstrip lines for the output, input and bias network connections. Full 3D S-parameter simulation is performed in EMPro on all 14 ports defined on the active device, the inputs and outputs connections, as well as for the additional SMD components that are not modelled in the drawing. Figure 7.14 shows the details of the integrated matching network including the bare die device, placed on the copper plate. This simulation assumed a perfect bonding between each of the passive and active devices with the grounding plate. Figure 7.15 summarises the design flow for this PA.



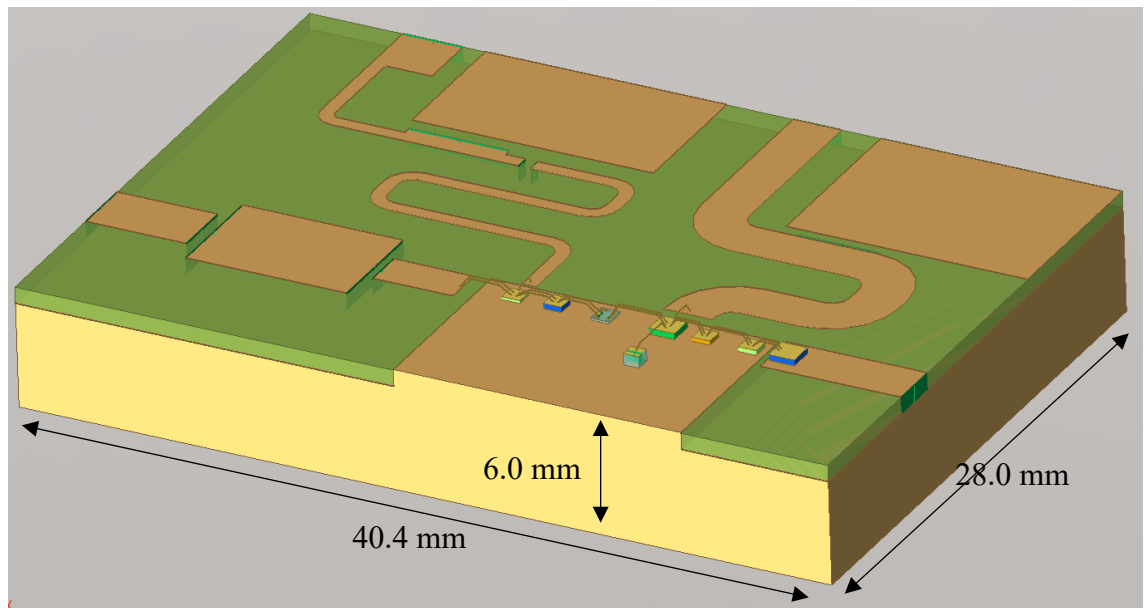


Figure 7.13. 3D PA with VBW enhancement modelled and simulated in EMPro.

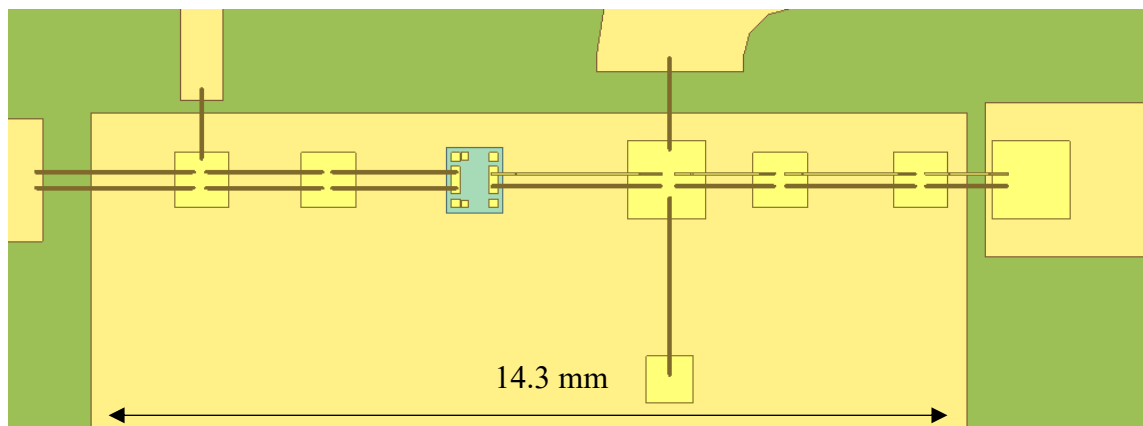


Figure 7.14. Integrated matching network for PA with VBW enhancement.

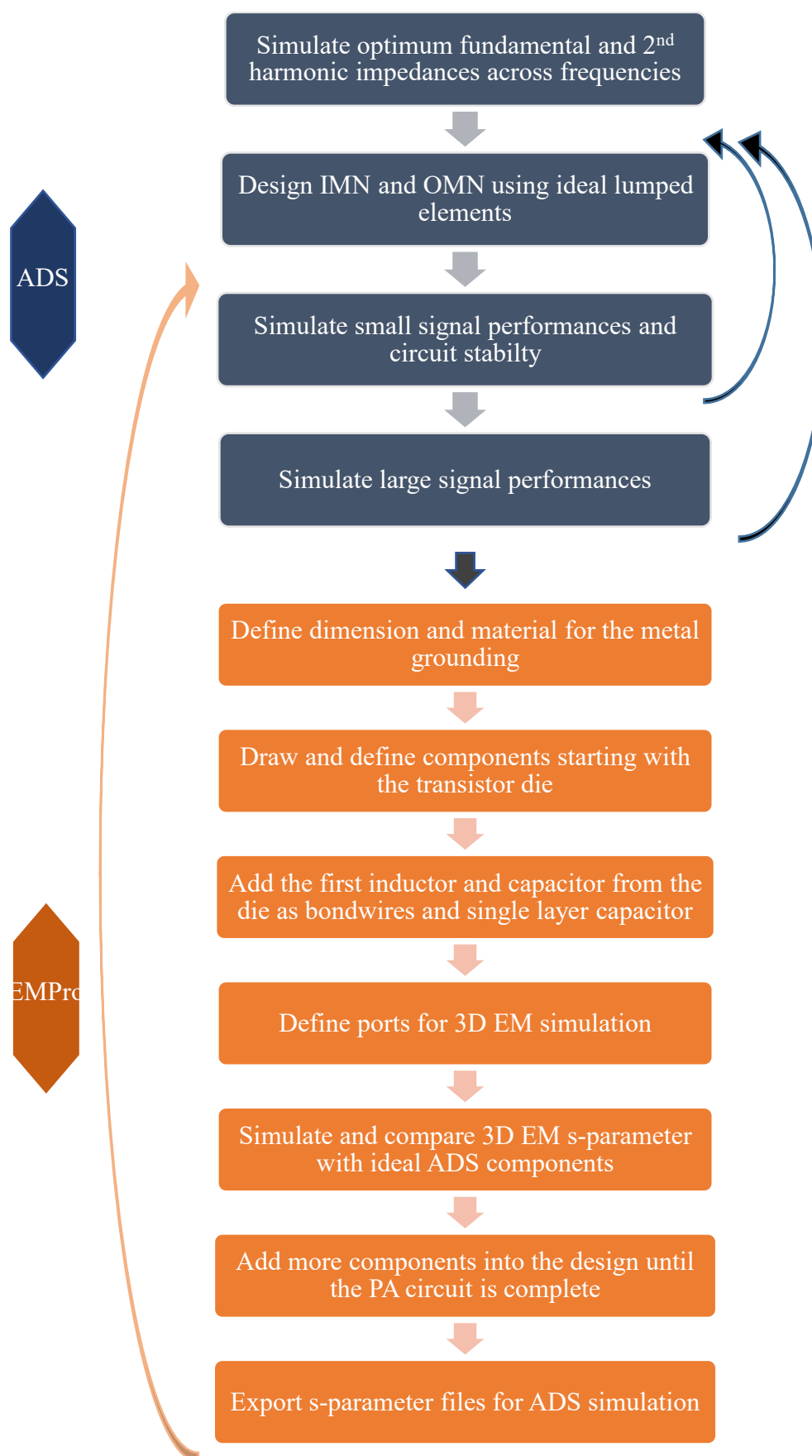


Figure 7.15. Flowchart for integrated matching PA design in ADS and EMPro.

### 7.4.1 S-Parameters Comparison between Ideal and 3D PA Simulation

The verification between the ideal and 3D implementation for the PA is performed in ADS, where the generated S-parameter file from EMPro is compared with the ideal circuit. Here, the other SMD components which are left out from the EMPro simulation is attached to the ports created from the EMPro design. Figure 7.16 shows the comparison of fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's input between the ideal components from Figure 7.11 and the 3D EM simulated circuit from Figure 7.13. There's a minor movement for the fundamental impedances seen by device's input between the ideal ADS and 3D EM simulation, which only affect the gain of the PA. The variation of the 2<sup>nd</sup> harmonic impedances rotates much bigger for the 3D EM simulated circuit, especially at the higher harmonic frequencies. However, the effect of input 2<sup>nd</sup> harmonic impedances is not discussed in this thesis. Figure 7.17 shows the comparison of fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's drain between ideal components and the 3D EM simulated circuits. The fundamental impedances of the 3D EM circuits are closely following with the ideal circuits. The trends are similar for the 2<sup>nd</sup> harmonic impedances, except at high frequencies, where the 3D EM simulated circuits start showing a resonance.

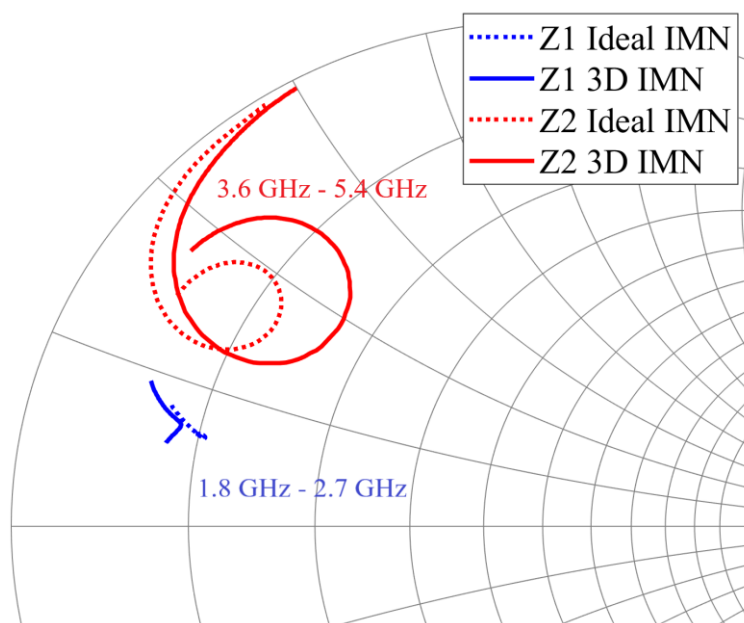


Figure 7.16. Comparison of fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's gate between ADS ideal simulation and EMPro 3D EM simulation.

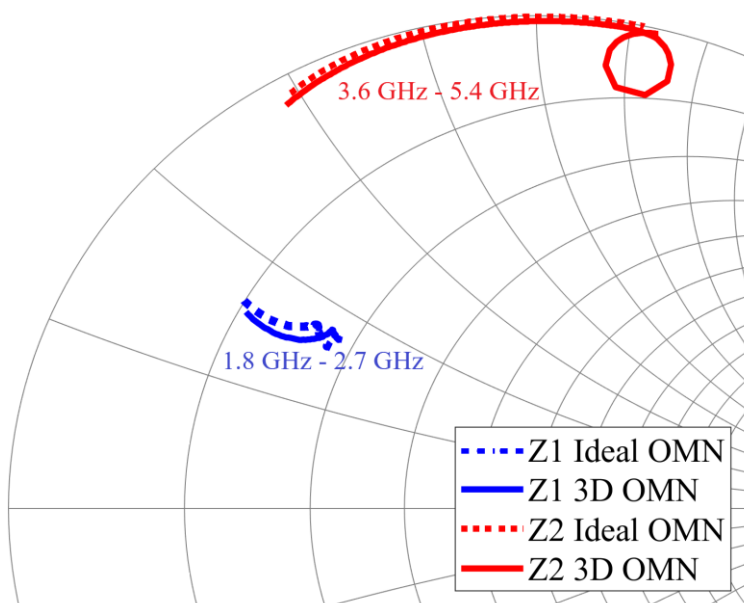


Figure 7.17. Comparison of fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's drain between ADS ideal simulation and EMPro 3D EM simulation.

### 7.4.2 PA without VBW Enhancement

Another PA is designed with exclusion of the VBW enhancement circuit to compare the VBW performances with the previous PA circuit. The approach taken to design this PA is similar to the previous PA, in which, the optimum fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's output plane are within the same location on the Smith chart across design bandwidth. The configuration of the output matching network has to be changed because of the exclusion of baseband termination circuit. The IMN for this circuit is similar to the PA with VBW enhancement.

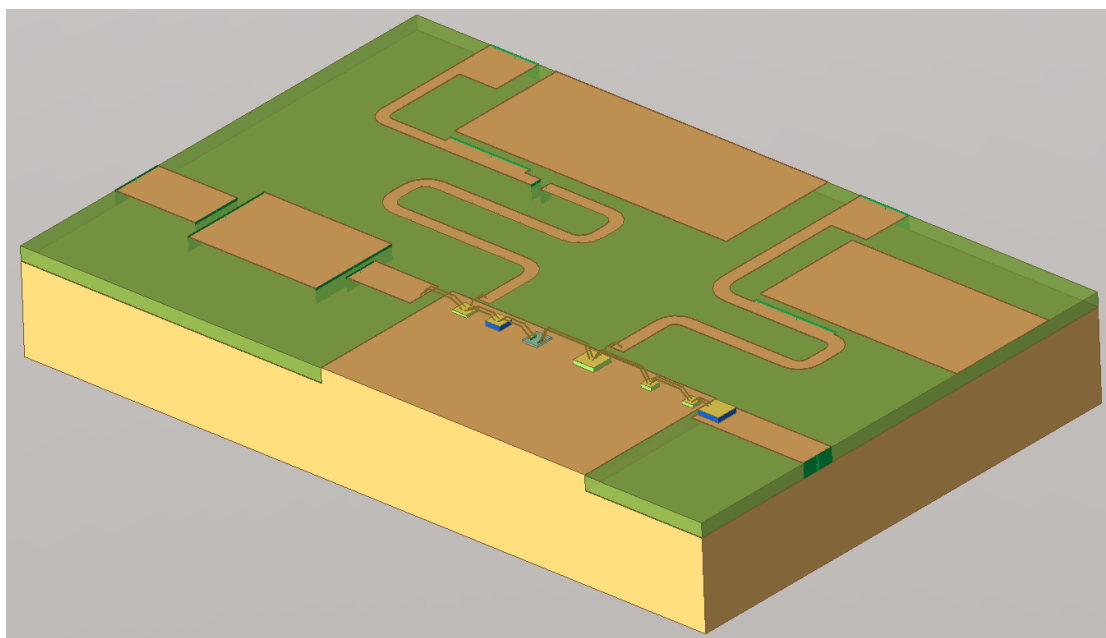


Figure 7.18. 3D PA without VBW enhancement modelled and simulated in EMPro.

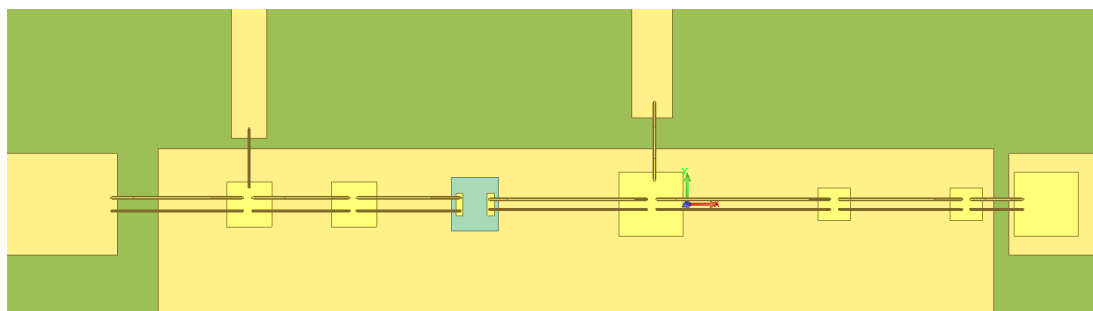


Figure 7.19. Integrated matching network for PA without VBW enhancement.

## 7.5 PA Simulations

The verification for the PA's performances is tested using ADS simulation. The PA was not fabricated at the time of writing this thesis, due to financial and resources limitations. The accuracy for the tests relies on the 3D EM simulation on the PA which accounting the magnetic couplings and parasitic capacitances between the active and passive components within the circuit. In all simulations performed here, the PA is biased with 28 V and -3 V at the drain and gate respectively, drawing 69 mA current.

### 7.5.1 S21 Output Resonant

Figure 7.20 shows the resonances between device's drain and bias network simulated through S21 probe, that is placed at the device's drain terminal as proposed in [109, 110] comparing the PA circuit with and without VBW enhancement. The resonance that has magnitude above -20 dB has been successfully shifted from 400 MHz to above 1 GHz when baseband termination circuit is integrated in the PA design. The lower resonance that has magnitude below -20 dB are both measured between 2-3 MHz on both circuits, however, due to the low magnitude, this small resonance will not affect the VBW performances for the circuit. Figure 7.21 shows the comparison of impedances seen by the device drain towards the output matching circuit, showing small spikes of increased impedance at the lower resonant frequencies. The impedances continue to rise as the frequency increases, peaking at the higher resonant frequency for PA without VBW enhancement. In contrast, the impedances seen by device drain is greatly reduced for PA with VBW enhancement, from 44  $\Omega$  to 12  $\Omega$  at 550 MHz.

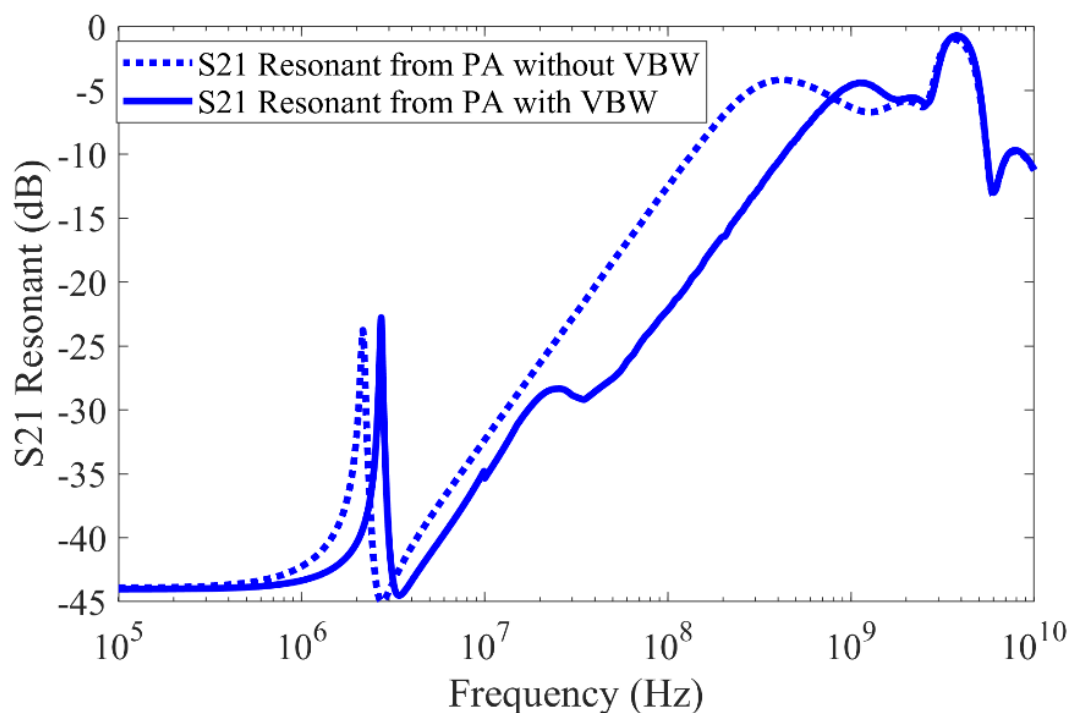


Figure 7.20. Output S21 resonant for PA with and without VBW enhancement.

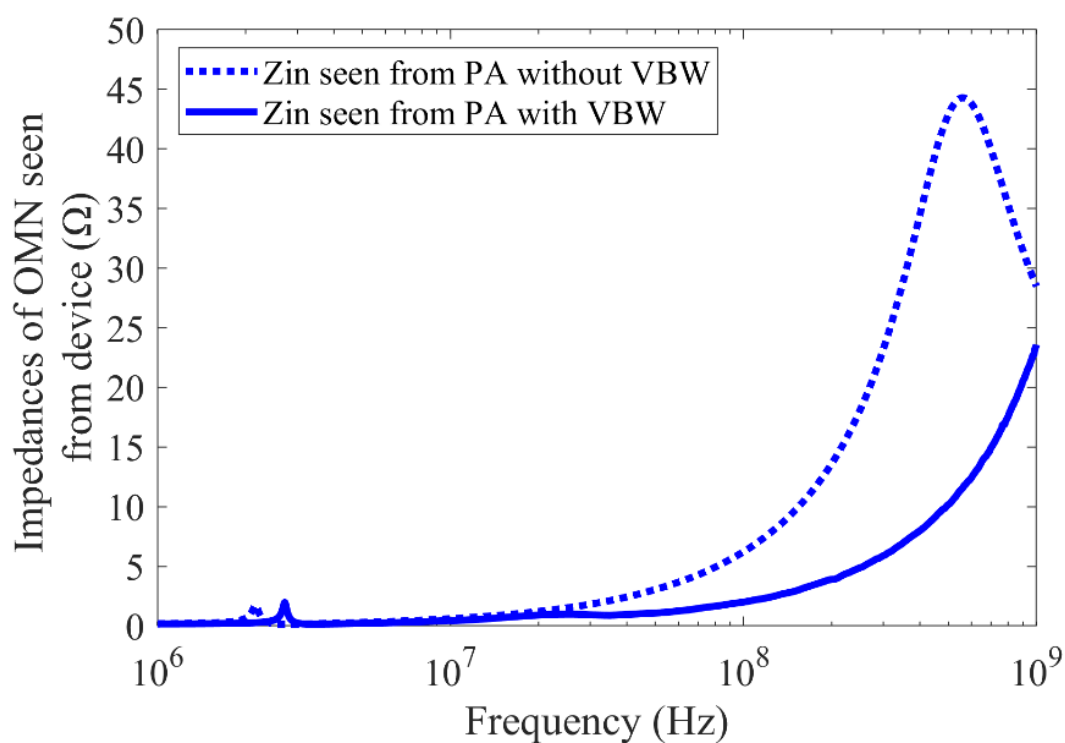


Figure 7.21. Input impedance seen from the device's drain for PA with and without VBW enhancement.

## 7.5.2 Small Signal Test

Next, a small signal test is performed on the PA with the VBW enhancement. Figure 7.22 shows the small signal gain for this PA, that reaches up to 16.7 dB at 2.0 GHz. The small signal gain is above 15 dB between 1.5 GHz to 2.7 GHz. Both input and output return losses are considered good across the broad design frequencies. The small signal test also allows the measure of stability for the PA. The stability criteria used in the simulation are based on the stability factor,  $k$  and  $\mu$ , which has been described in [112]. Figure 7.23 shows that the stability factor,  $k$  and  $\mu$  are above 1 across all frequency ranges, indicating that the PA is unconditionally stable.

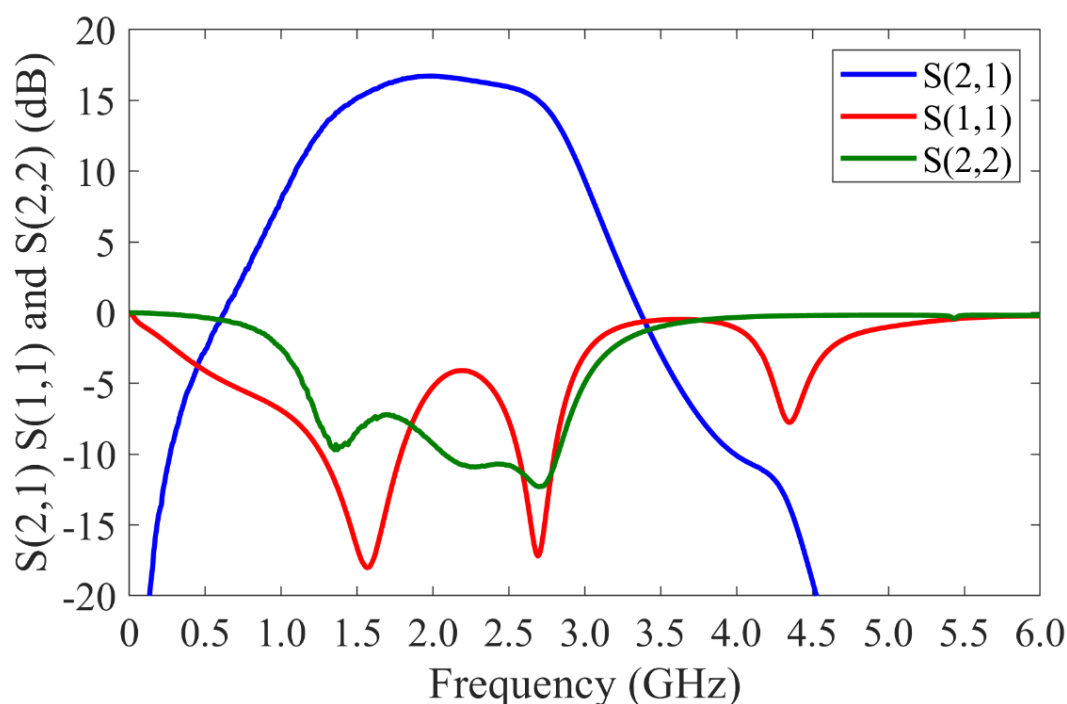


Figure 7.22. Small signal S-parameter simulation showing the gain, input and output return losses.



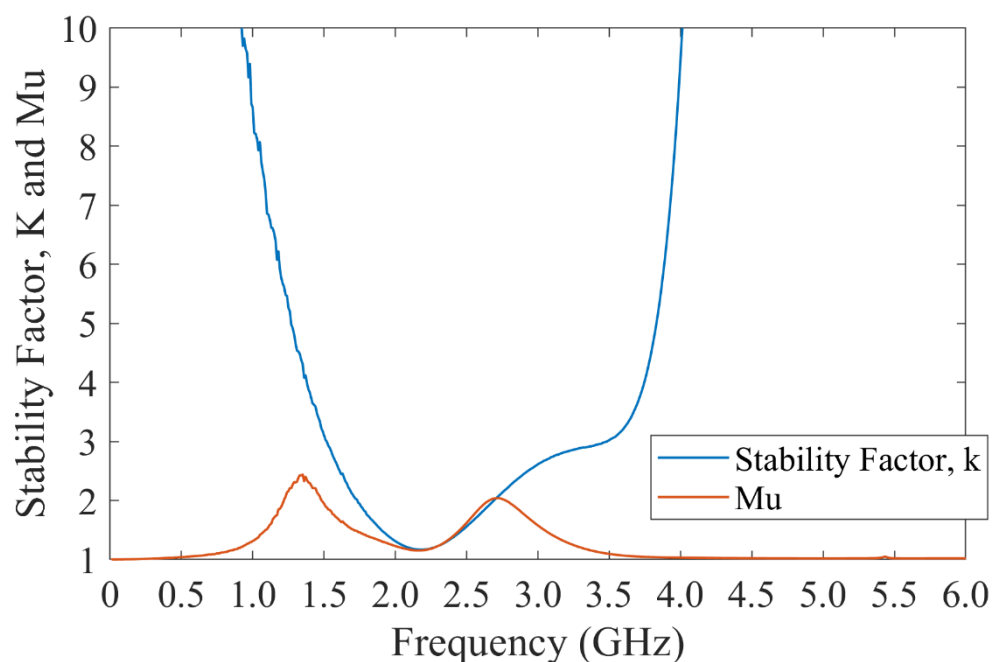


Figure 7.23. Small signal simulation for stability test.

### 7.5.3 CW Signal Test

Figure 7.24 shows the comparison of the PAs performances at  $50\ \Omega$  termination under CW signal. Both PA are driven with equal input CW signal across bandwidth up to 4 dB gain compression; with a constant  $P_{in} = 30.5\ \text{dBm}$  for PA with VBW enhancement and  $P_{in} = 30\ \text{dBm}$  for PA without VBW enhancement. The output power and drain efficiency are all above 15 W and 62.7 % across bandwidth for PA with VBW enhancement. However, the CW performances are much better for the PA without VBW enhancement; DE above 69.5 % across bandwidth. The transducer gain for PA with VBW enhancement is almost flat across bandwidth, which is at 11.5 dB, and it is 0.5 dB less than PA without VBW enhancement. This is due to higher input power required to drive the PA into 4 dB gain compression. Overall, both PAs achieved high output power and DE from 1.8 GHz to 2.7 GHz. Table 7.1 summarises the performances of the PA with VBW enhancement under the CW test across the bandwidth.

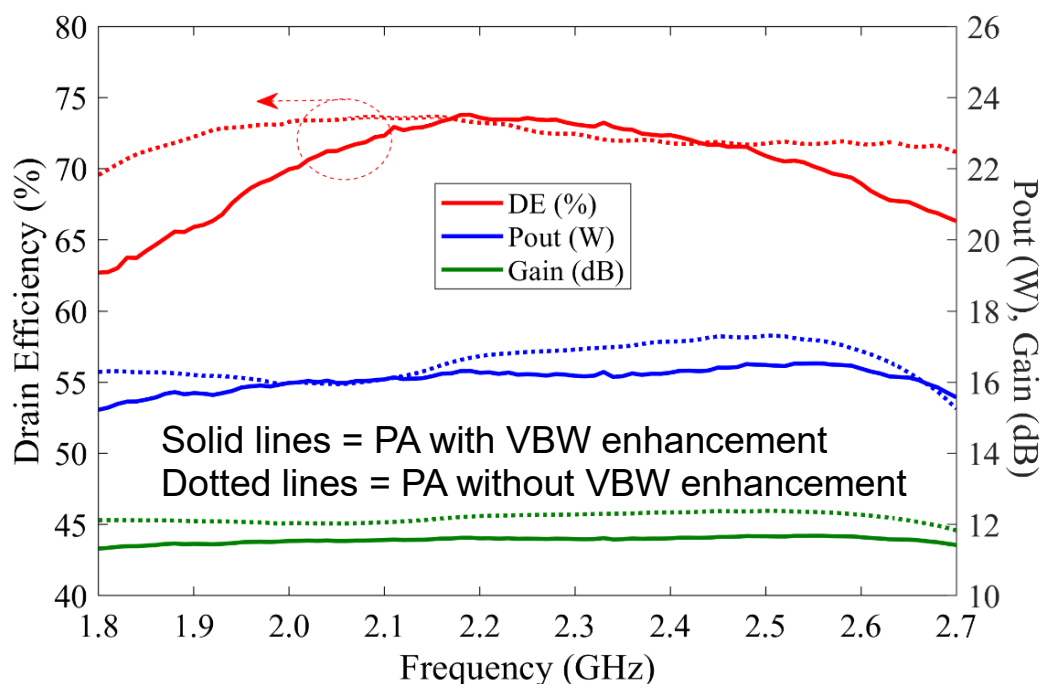


Figure 7.24. Simulated PA performances using CW signal.

The major difference for the performances of the PA designed with and without VBW is the drain efficiency across frequency ranges. The PA without VBW enhancement has almost flat DE across bandwidth. Meanwhile, DE for the PA with VBW enhancement is at lowest at both end of the operating frequencies and is at maximum at 2.2 GHz. The average output power for PA without VBW is 0.4 W higher than PA with VBW. The reason for different performances between these 2 PAs is due to different impedances that are presented to the device's plane. Also, the baseband circuit has minor impact of the RF performances, which explains the necessity to have bigger bondwires inductance connected to the baseband circuit's 10 nF capacitor to prevent RF leakage to DC power supply.

Figure 7.25 shows the fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's extrinsic plane between the 2 PAs. Although both 3D OMN for each PA are designed to be almost identical to its respective ideal network, however, these 3D OMN are not presenting the same impedances to the device's extrinsic plane. This is due to the

additional VBW capacitor that shifted the total impedances (fundamental and harmonics), therefore, the OMN for PA with VBW has to be re-tuned to get the best performances. This also explained the difference in component values within the internal matching network for both designs.

Table 7.1. Summary of simulated PA with VBW performances under CW.

Frequency (GHz)	Pout (dBm)	Pout (W)	DE (%)	Gain (dB)
1.80	41.83	15.22	62.70	11.33
1.90	41.96	15.69	65.91	11.46
2.00	42.04	15.98	69.96	11.54
2.10	42.06	16.08	72.33	11.56
2.20	42.24	16.26	73.59	11.61
2.30	42.28	16.18	73.12	11.59
2.40	42.34	16.27	72.36	11.61
2.50	42.38	16.48	70.90	11.67
2.60	42.27	16.38	68.96	11.64
2.70	41.84	15.58	66.32	11.42

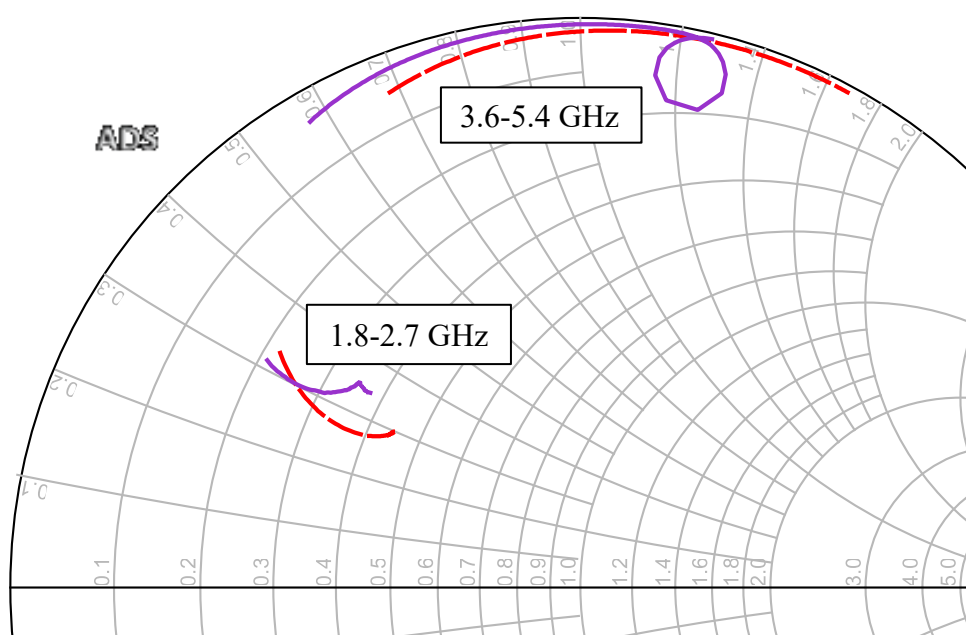


Figure 7.25. Comparison impedances presented to the device plane between 3D PA with (solid purple lines) and without (dotted red lines) VBW.

In harmonic balance simulation of the RF PA circuit, the impedances of the OMN presented to the CGP of the device is shown in Figure 7.26. These impedances are obtained due to the presence of internal current and voltage of provided in the device's model. The fundamental impedances across the bandwidth are located in the inductive region of the Smith chart, which is close to the  $\alpha = -1$  region of the CCF mode. On the other hand, the 2<sup>nd</sup> harmonic impedances rotate from the open circuit to the  $\alpha = -1$  region across the bandwidth.

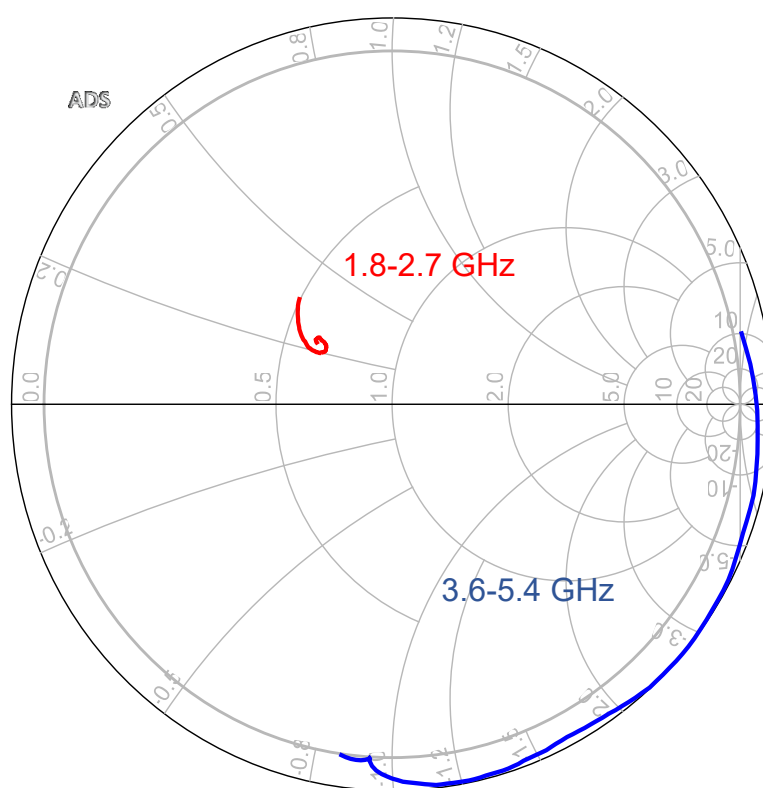


Figure 7.26. Simulated fundamental (red line) and 2<sup>nd</sup> harmonic (blue line) impedances presented at device's CGP.

A load-pull simulation is performed at the PA's 50  $\Omega$  load termination, using the same input power (30.5 dBm), to obtain its OPBO performances. Here, a comparison is made between the ideal and 3D EM simulated circuit, to evaluate the power losses within the actual circuit. Figure 7.27 and Figure 7.28 show the maximum Pout and DE obtained from the load-pull simulation between ideal and 3D circuit for the PA with VBW

enhancement across 1.7 GHz to 2.8 GHz frequency. Both figures show that the performances drop between ideal and 3D circuit simulation. On average, the output power and DE losses between ideal and 3D circuit simulation is 0.92 W and 5.8 % across bandwidth respectively. Overall, the max Pout is above 15mW for frequency between 1.8 GHz to 2.7 GHz while the max DE is above 70 % across this bandwidth. In another comparison, a fundamental load-pull simulation with the same 2<sup>nd</sup> harmonic termination as the PA circuit is performed, where the maximum Pout and DE across the frequencies are shown in both Figure 7.27 and Figure 7.28. This comparison is made to show the maximum performances that the device can deliver, without the matching network.

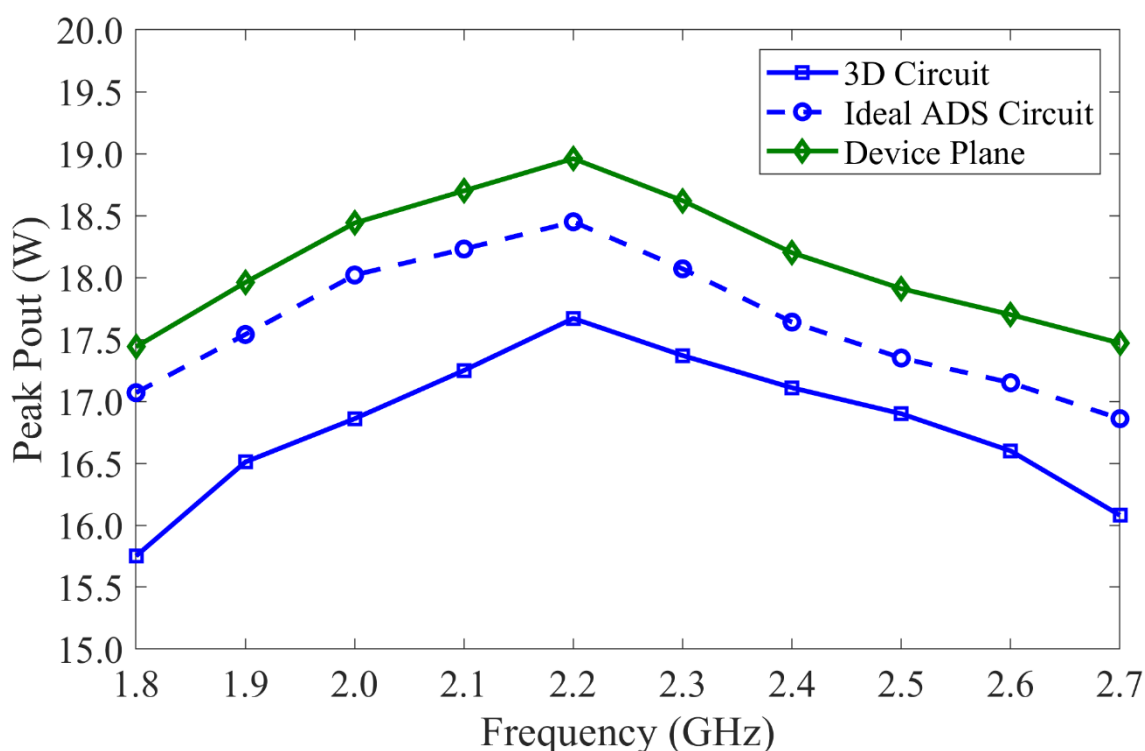


Figure 7.27. Comparison of peak Pout from fundamental load-pull simulation on PA with VBW enhancement between ideal and 3D circuit.

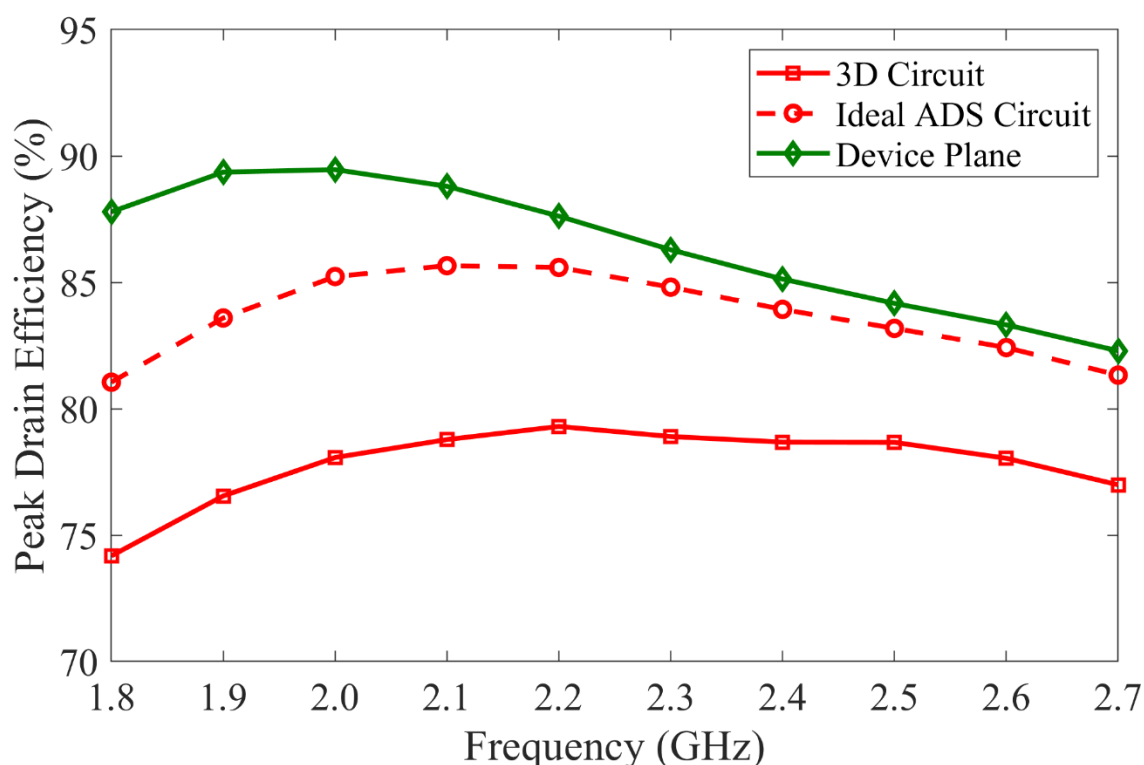


Figure 7.28. Comparison of peak DE from fundamental load-pull simulation on PA with VBW enhancement between ideal and 3D circuit.

Meanwhile peak DE at the 8 dB and 6 dB OPBO are shown in Figure 7.29. Similar to the max Pout and DE performances in previous figures, the peak DE at OPBO drops between the load-pull simulation of the ideal and 3D circuit. On average, 12.3 % DE drops at 8dB back-off between 2 circuits, with maximum loss of 17 % drops at 1.8 GHz. Meanwhile, average of 10.2 % DE drops at 6 dB OPBO, with maximum loss of 12.5 % across bandwidth. Overall, at least 55 % DE is achievable at 8 dB OPBO for frequency bandwidth between 1.8 GHz to 2.7 GHz while at least 65 % DE is achievable at 6dB OPBO for the same bandwidth. In addition, a minimum of 60 % and 70 % DE at 8 dB and 6dB OPBO is achievable for frequency bandwidth between 2.0 GHz to 2.7 GHz.

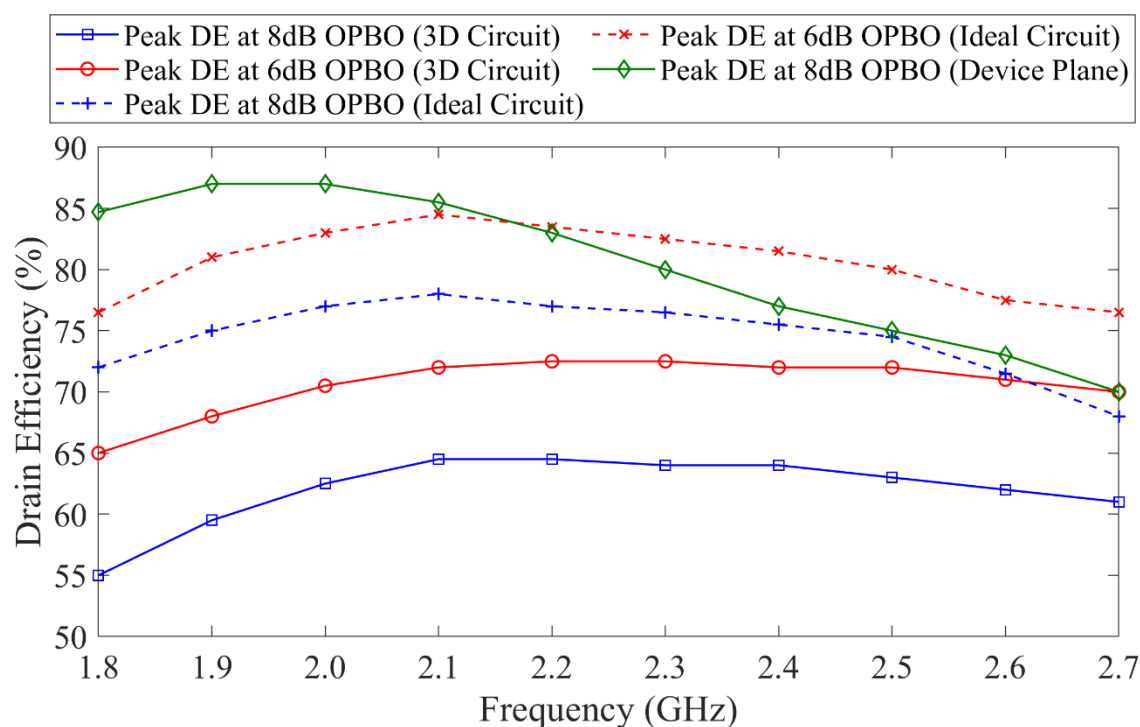


Figure 7.29. Comparison of peak DE at 8 dB and 6 dB OPBO from fundamental load-pull simulation on PA with VBW enhancement between ideal and 3D circuit.

### 7.5.4 PA Linearity under Modulated Signal Test

The PA with VBW enhancement is tested with 20 MHz LTE downlink input signal with 8.8 dB PAPR. The input power for the LTE signal is scaled so that the peak output power of the PA reaches at least 15 W across the bandwidth. Figure 7.30 shows the input LTE signal tested on the PA and the output spectrum at the load. At 2.2 GHz, an average of -30.3 dBc of ACPR is achieved for maximum of 16 W output power. A maximum of 73.5 % DE is obtained at this peak power while the mean DE is 41.4 %. Figure 7.31 shows the AM/AM and AM/PM responses of the PA from the modulated signal test. Figure 7.32 shows the DE plotted against  $P_{out}$ .

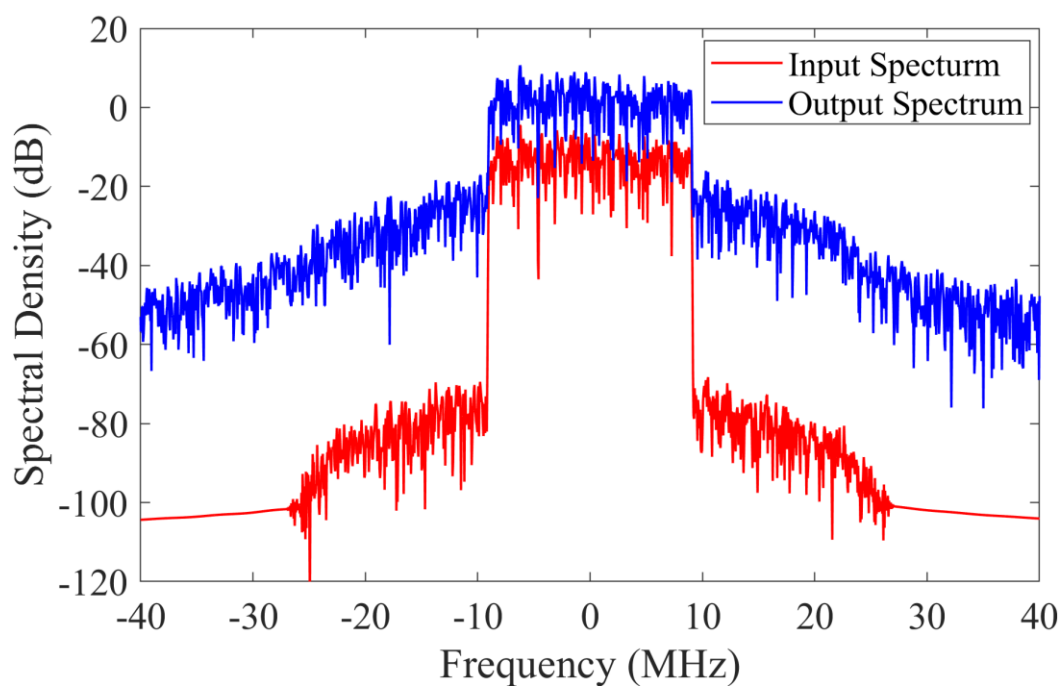


Figure 7.30. Input and output spectrum of the PA with VBW enhancement tested with 20 MHz LTE signal at 2.2 GHz carrier frequency.

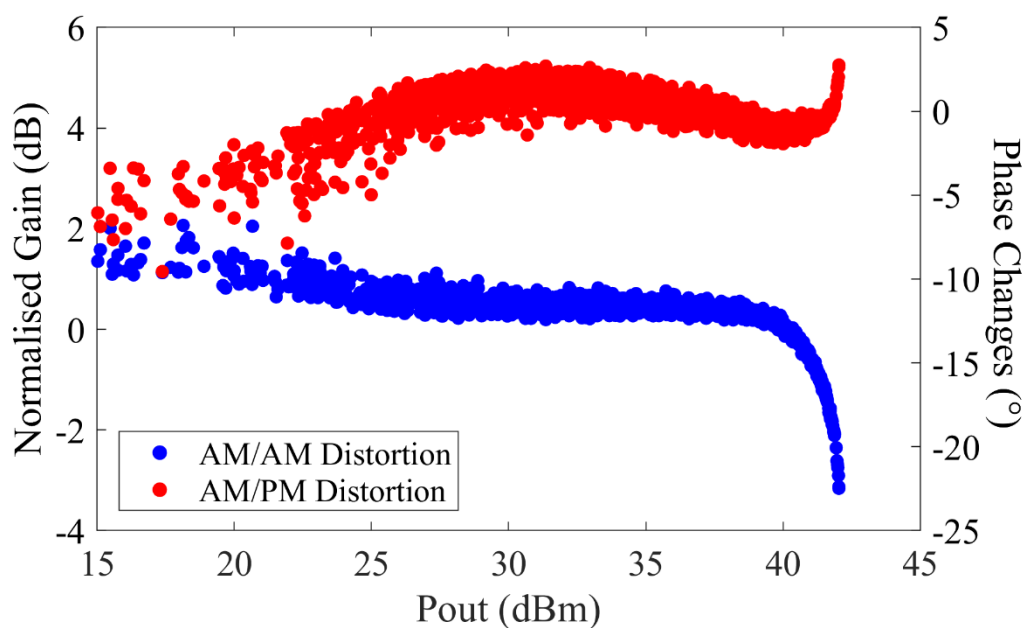


Figure 7.31. AM/AM and AM/PM responses of the PA with VBW enhancement using 20 MHz LTE signal at 2.2 GHz.



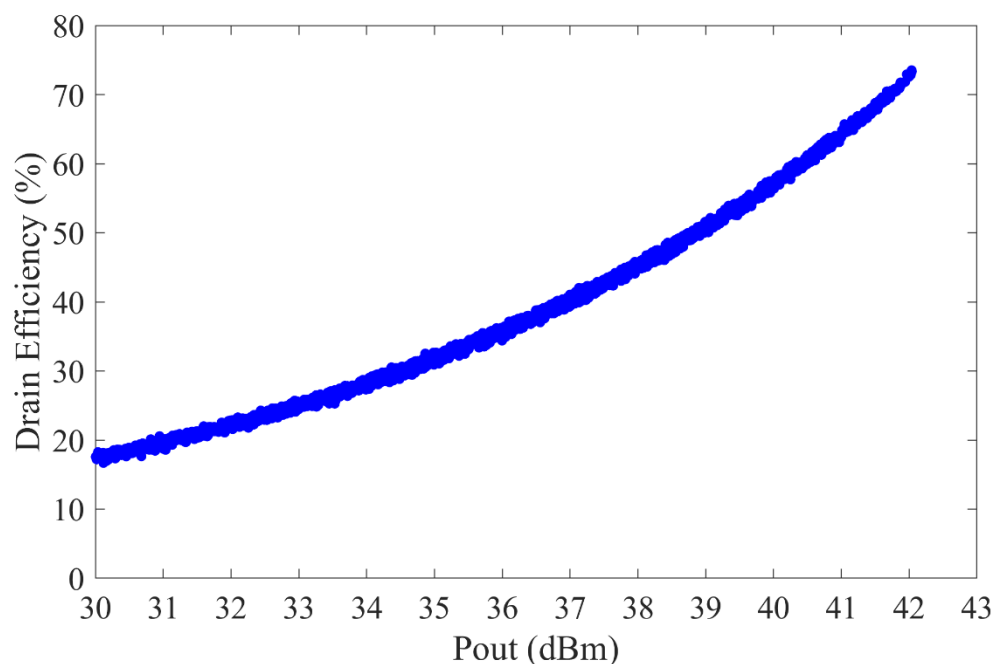


Figure 7.32. DE vs Pout of the PA with VBW enhancement tested using 20 MHz LTE signal at 2.2 GHz.

Figure 7.33 shows the overall performances of the PA with VBW enhancement tested under various carrier frequency of the 20 MHz LTE signal. At minimum Pout of 15 W across all frequency, the peak DE is above 60 %, while mean DE reaching up to 41.4 %. The ACPR maintained below -30 dBc for all 1.8 GHz to 2.6 GHz.

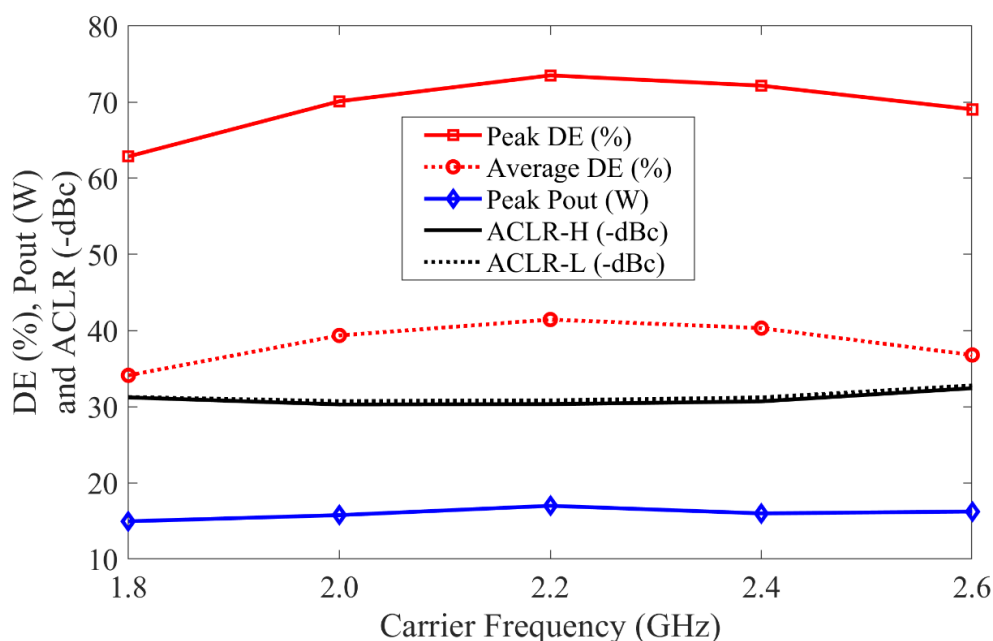


Figure 7.33. Performances of the PA with VBW enhancement with various carrier frequency of 20 MHz LTE signal.

### 7.5.5 VBW Performances

Next, 2-tones simulations are performed on both 3D RF PA circuits with and without VBW enhancement to obtain its VBW performances. In the first 2-tone simulation, the centre frequency,  $f_c$  is set to 2.25 GHz while the carrier's frequency,  $f_1$  and  $f_2$  are set to  $f_{1,2} = f_c \pm (f_{\text{spacing}}/2)$ . The spacing frequency,  $f_{\text{spacing}}$  is swept from 1 MHz to 800 MHz with 1 MHz frequency step. The input power for both PA is set to be equal for all frequency spacing sweep, so that the peak envelope power, PEP is above 15 W. Figure 7.34 shows the PEP and DE performances for both PAs across the frequency spacings. The dotted lines which represent the 2-tone performances for the PA without VBW enhancement; showing both PEP and DE drops from 15 W to 11.5 W at 350 MHz, which is almost close to the resonance simulated on the output of the PA (400 MHz), before gaining its performances back up. On the other hand, constant DE and PEP are obtained for PA with VBW enhancement without any dips. However, the DE and PEP drop when the frequency spacings are increased, due to broadband responses of the PA that was shown from Figure 7.24. The Pout and DE are at the maximum at the centre frequency of the bandwidth (2.2 GHz) and drop at both lower and upper frequency ends. The IMD3 stays below -20 dBc for PA with VBW enhancement, while the IMD3 resonant occurs at 350 MHz for PA without VBW enhancement, in which the magnitude reaches above -15 dBc at this resonant. Figure 7.35 shows the difference between IMD3 low and high for the PA with VBW enhancement, showing > 3 dB separation at 400 MHz. There is no clear relationship of the IMD crossover at 260 MHz for PA with VBW and the S21 resonance from the OMN and the device.

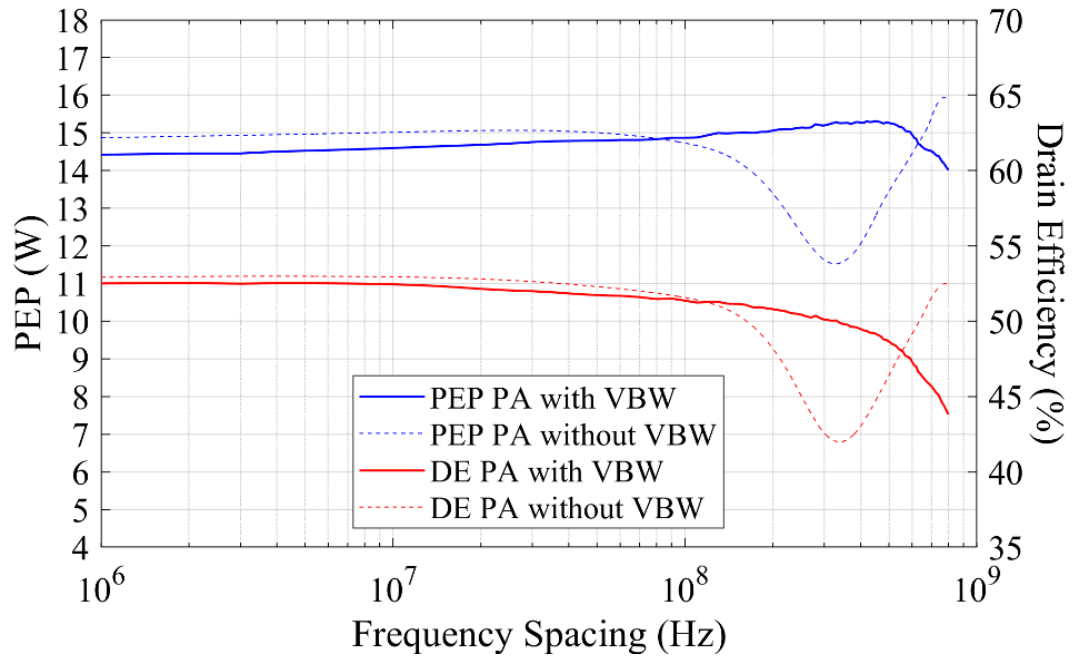


Figure 7.34. PEP and DE from 2-tone simulation on 3D PA with (solid lines) and without (dotted lines) VBW enhancement. ( $f_1 = 2.25 \text{ GHz} - f_{\text{spacing}}$ ,  $f_2 = 2.25 \text{ GHz} + f_{\text{spacing}}$ ).

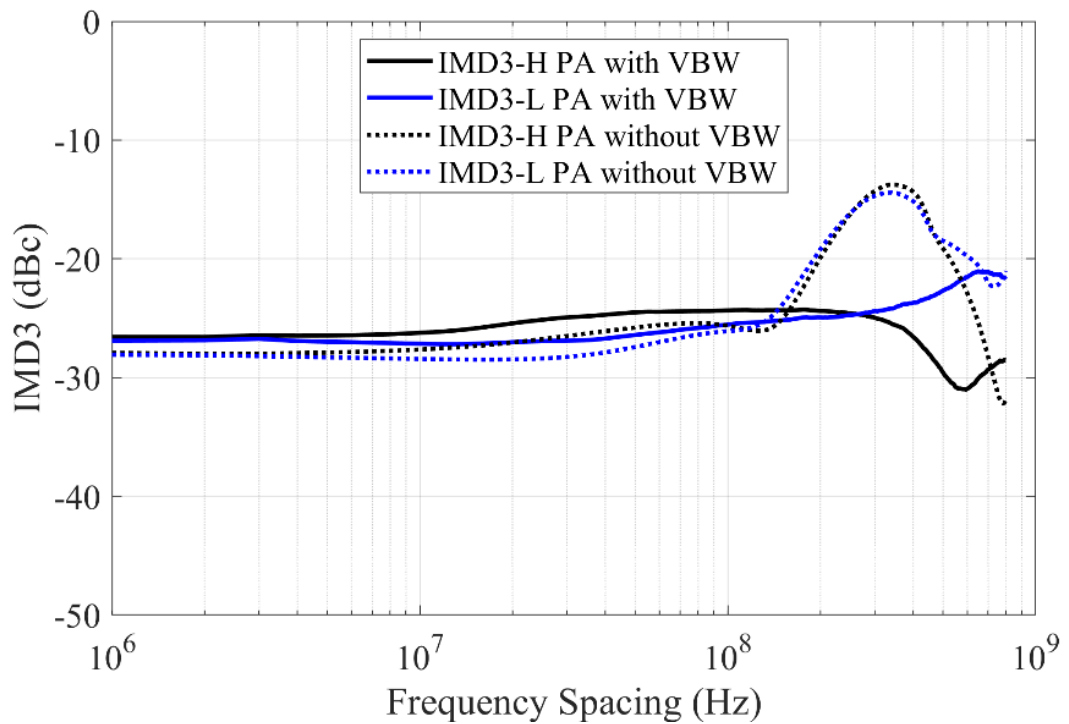


Figure 7.35. IMD3 high and low from 2-tone simulation on 3D PA with (solid lines) and without (dotted lines) VBW enhancement.

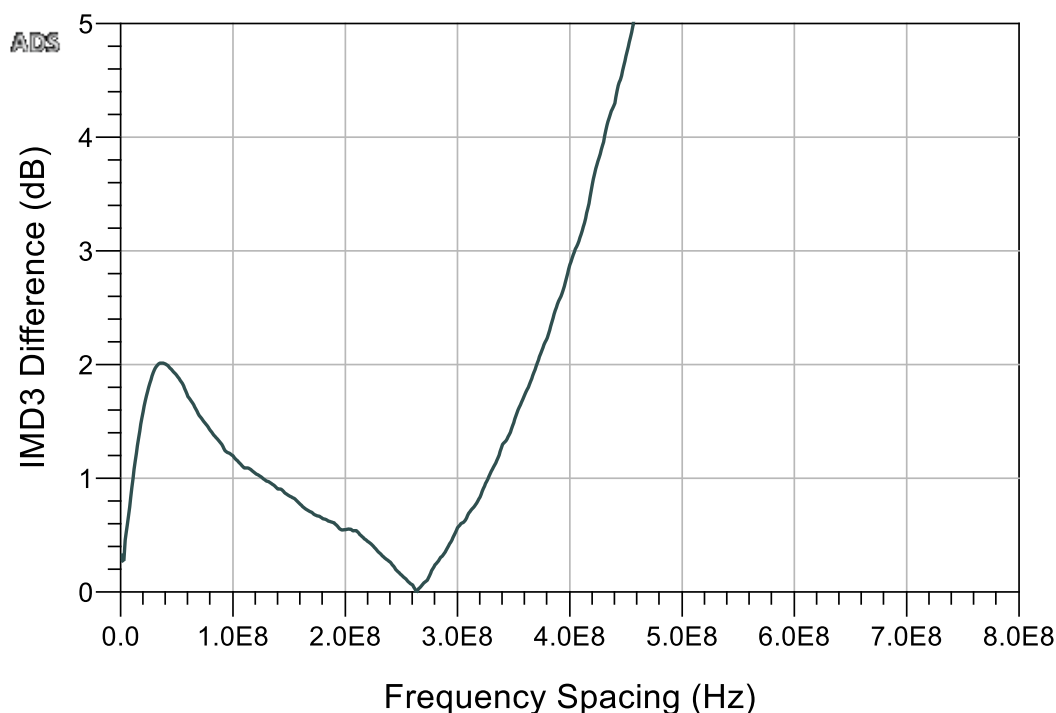


Figure 7.36. IMD3 low and high difference for PA with VBW enhancement.

Another 2-tone simulation is performed on the PA with VBW enhancement, in which the first tone,  $f_1$  is set constant at 1.8 GHz while the second tone,  $f_2$  is swept along the increment of frequency spacing. Figure 7.37 shows that the PEP and DE increases with frequency spacing similar to the broadband CW performances of the PA. This extended VBW performance is achieved through the additional VBW circuit, that shifted the output resonance and reduced the input impedances seen by the transistor drain. The 2-tone simulation shows a stable performance when the frequency spacing between the tones is increased up to 900 MHz, however, the magnitude of DE and PEP also depends on the broadband responses of the PA with CW signal. In contrast, a clear performances drops are observed for PA without VBW enhancement, as shown in Figure 7.34, due to resonances on the PA's OMN in Figure 7.20.

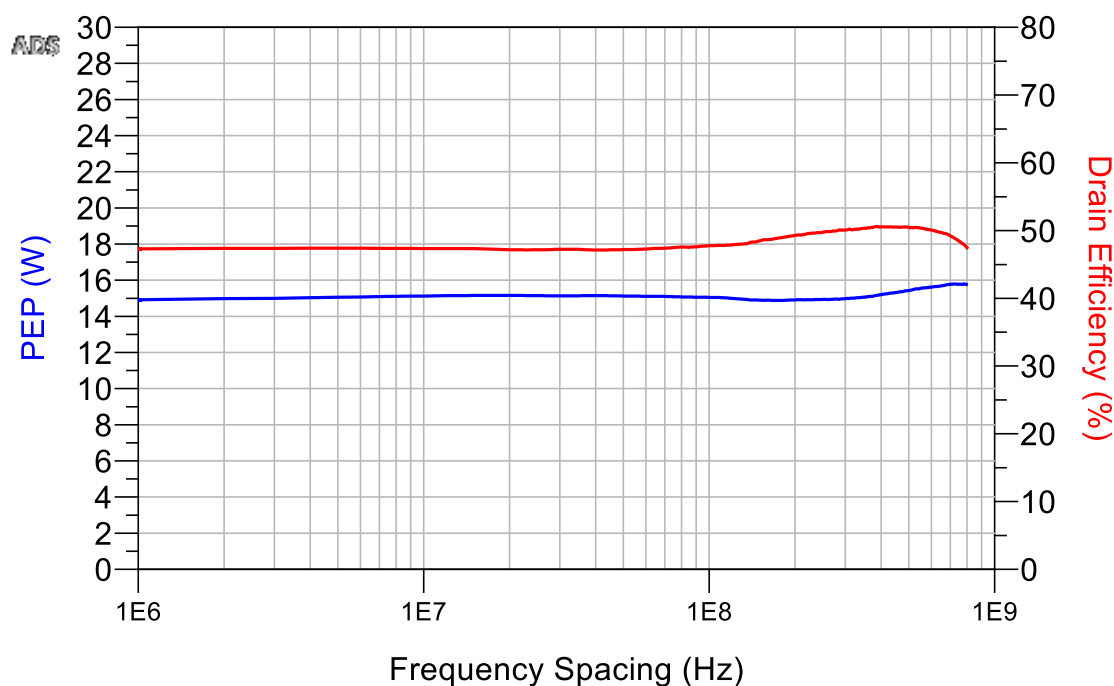


Figure 7.37. PEP and DE from 2-tone simulation of PA with VBW enhancement ( $f_1=1.8$  GHz,  $f_2 = f_1 + f_{\text{spacing}}$ ).

Finally, both PAs are tested with 2 x 20 MHz LTE signal. One of the LTE signal is centred at 1.8 GHz while the other is varied from 1.85 GHz to 2.7 GHz. Similar to the previous 2-tone simulation, the performances drop between 300 MHz to 400 MHz for PA without VBW enhancement. Meanwhile, the PEP stays above 15 W for PA with VBW enhancement. The maximum DE stays above 47 %, peaking at 52.2 % when the 2 LTE signals are separated by. The efficiency is higher for PA without VBW at 50 MHz frequency separation due to higher broadband responses of this PA at lower frequency, as shown in Figure 7.24.

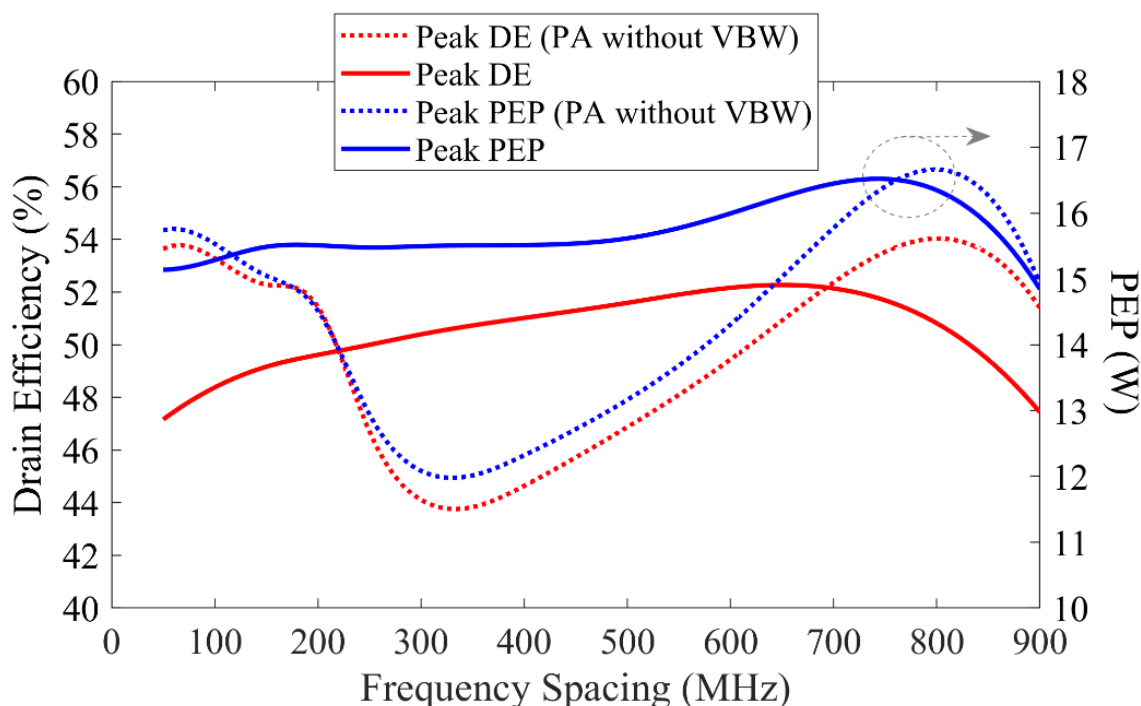


Figure 7.38. PEP and max DE for PA with and without VBW enhancement obtained from 2 x LTE signal with various frequency separation.

## 7.6 Narrowband Outphasing PA Application

The application from the compact PA that was designed in this chapter is extended for a narrowband outphasing PA, by taking advantage of the 2<sup>nd</sup> harmonic impedances termination close to  $\alpha = -1$  region at this frequency. In Chapter 5, the efficiency at OPBO is predicted to be at the peak when the transistor is operated in CCF mode and the  $\alpha = -1$ . In Section 7.5.3, the 3D simulated PA is load-pulled at the 50  $\Omega$  termination, showing 70 % and 60 % DE at -6.8 dB and -9.1 dB OPBO at 2.2 GHz. The feasibility of this PA for outphasing PA is investigated here. Figure 7.39 shows the schematic of outphasing PA operating at 2.2 GHz. The two PAs are operated with the same bias, frequency and input power and are combined using an asymmetric combiner from each of the 50  $\Omega$  termination. The combiner is designed such the impedances seen from the PAs are in track with the Pout and DE contours from each PA during the outphasing operation.

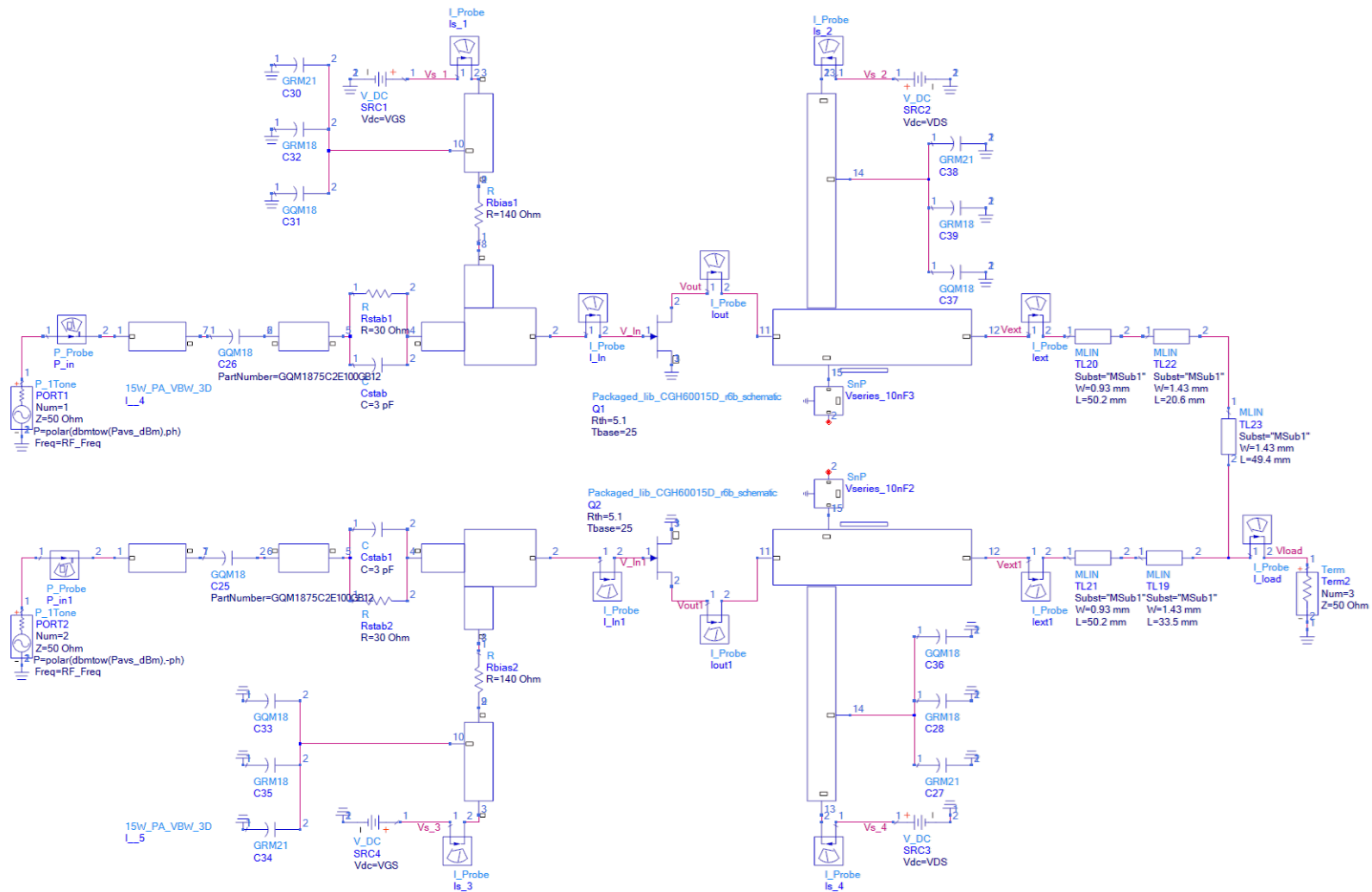


Figure 7.39. Schematic of narrowband outphasing PA consisting of 2 x 3D emulated PA with VBW enhancement and a combiner circuit.

The input power for each PA is set to 30.5 dBm, equal to the input power used in the CW simulation for the single PA, that resulted up to 4 dB output gain compression at 2.2 GHz. The input power for each PA is out-phase between each other, with the phase values swept from  $0^\circ$  to  $90^\circ$ . Figure 7.40 shows the trajectories of impedances seen from each PA into the combiner, along the outphasing operations, which overlap between optimum  $P_{out}$  and DE from load-pull contours of the PA at  $50\ \Omega$  termination for 2.2 GHz. However, the trajectories of the outphasing operation overshooting the optimum DE impedance so that the drain efficiency performances for the outphasing PA can be extended at higher OPBO range. Figure 7.41 shows the performances for the narrowband outphasing PA by plotting the drain efficiency against output power, between 2.18 GHz to 2.22 GHz. At 2.2 GHz, the peak  $P_{out}$  and DE obtained from the simulation is 34.7 W and 71.4 % respectively. The efficiency stays above 60 % and 50 % at -6 dB and -8 dB

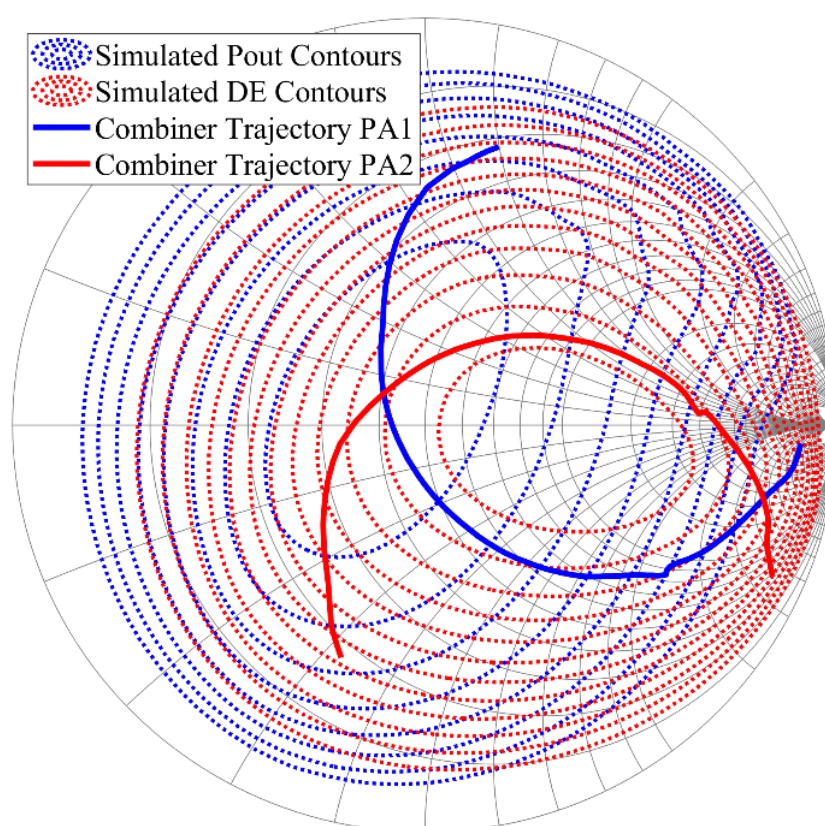


Figure 7.40. Impedances trajectories seen from each PA into the combiner network from the outphasing angles plotted on the fundamental load-pull contours from the PA  $50\ \Omega$  load operated at 2.2 GHz.



OPBO respectively across all frequencies. Table 7.2 summarises the performances obtained from the narrowband outphasing PA. The performances at 2.2 GHz shows the best trade-off between peak Pout, peak DE and DE at OPBO range.

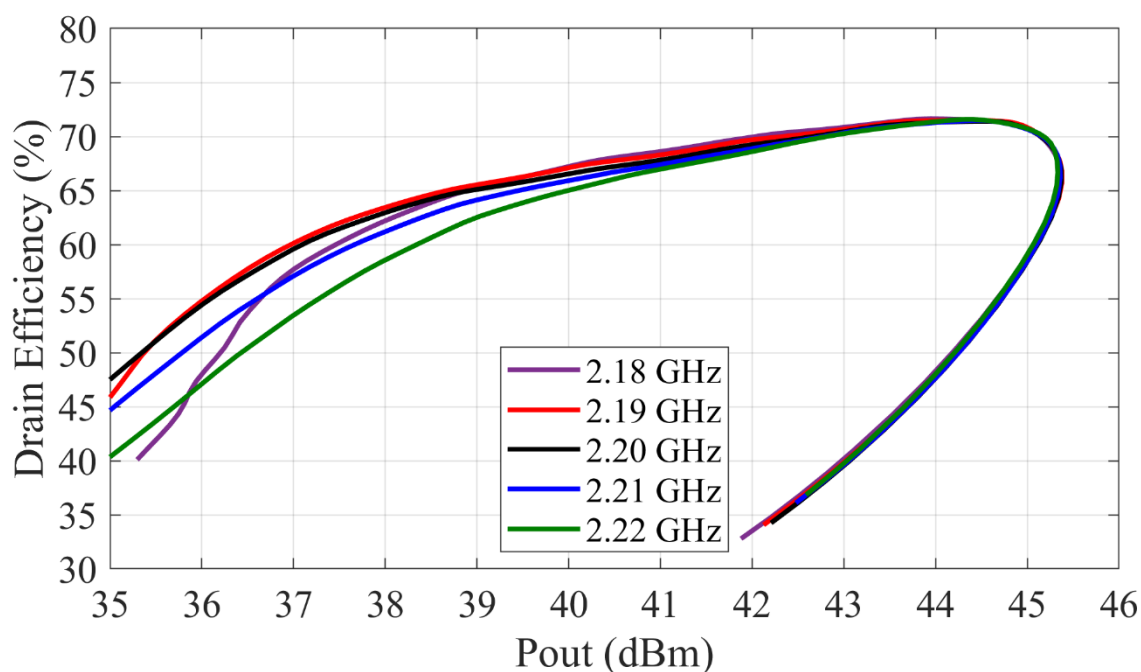


Figure 7.41. Simulated performances of the narrowband outphasing PA centred at 2.2 GHz.

Table 7.2. Summary of narrowband outphasing PA performances.

Frequency (GHz)	Peak Pout (dBm)	Peak Pout (W)	Peak DE (%)	DE -6 dB OPBO (%)	DE -8 dB OPBO (%)	DE -10 dB OPBO (%)
2.18	45.4	34.7	71.6	66.0	59.3	41.2
2.19	45.4	34.7	71.5	66.1	61.7	50.0
2.20	45.4	34.7	71.4	66.0	61.1	50.5
2.21	45.4	34.7	71.5	64.8	58.8	46.8
2.22	45.3	33.9	71.6	63.6	55.5	42.0

Table 7.3 below shows the state-of-art comparison for narrowband outphasing PAs with this work. The drain efficiency achieved in this work is the highest at the peak power and OPBO within relatively similar frequency of operation. Meanwhile, the performances obtained in [44] is better, with almost 15 % higher efficiency at 6 dB OPBO, due to lower than 1 GHz operational frequency. The transistor has higher output power and efficiency at lower frequency, and gradually decreases up to the cut-off frequency, where the performance steeply reduces [12, 13].

Table 7.3. State-of-art comparison for narrowband outphasing PAs.

<b>Ref</b>	<b>Frequency (GHz)</b>	<b>Peak Pout (dBm)</b>	<b>Peak DE (%)</b>	<b>DE at 6 dB OPBO (%)</b>	<b>DE at 8 dB OPBO (%)</b>
[44]	0.9	44.5	83	81	65
[46]	2.3	48.5	70	59	57
[49]	1.95	44.5	68	62	53
[51]	2.15 – 2.18	52.6	Up to 59.6	40 - 46	Up to 30
This work	2.18 – 2.22	45.3	71.4	63.6 – 66.1	55.5 – 61.7

## 7.7 Chapter Summary

This chapter has presented a complete design of broadband compact PA using integrated matching network based on all the theories and investigation that have been discussed from all previous chapters. In order to obtain high efficiency broadband PA at peak power and at load modulated OPBO, the PA is designed to have limited rotation of fundamental and 2<sup>nd</sup> harmonic impedances presented to the device's output across  $\alpha = -1$  region. The integrated matching networks are implemented using bondwires and single layer capacitors, which reduces the overall size of the PA. The implementation of integrated matching network also allowing the baseband termination circuit to be integrated into the design, to improve the VBW performances.

The design of compact (40.4 x 28.0 x 6.0 mm) 15 W GaN PA with VBW enhancement circuit is presented. This PA operates between 1.8 GHz to 2.7 GHz, with peak power ranging between 15.2 W to 16.5 W when simulated at up to 4 dB gain compression. The drain efficiency at the peak power level varied between 62.7 % to 73.6 % across the bandwidth. This PA is simulated with overall  $11.5 \pm 0.15$  dB gain across the bandwidth. The linearity of this PA is simulated with 10 MHz LTE signal, centred across the design bandwidth. On average, the ACLR from the output spectra is below -30 dBc when the PA is operated with compression. The average efficiency ranges between 34 % to 41.5 %.

The output resonance from this PA has been shifted above 1 GHz, with impedance looking from the device's output plane reduces to 12  $\Omega$  at 550 MHz. The VBW performances of this PA is tested using 2-tone signals by sweeping the frequency spacing between the two tones. No significant drop of PEP and DE at up to 900 MHz frequency separation for the PA with VBW enhancement, while major drop in the performances are

simulated at the same resonant frequency for the PA without VBW enhancement. The frequency spacing where the difference between IMD3 above 3 dB has been extended to 400 MHz, further proving the VBW enhancement for this PA.

Finally, the same PA is used to construct a narrowband outphasing amplifier. A Chireix combiner is designed to combine 2 PAs with VBW enhancement, to operate at centre frequency of 2.2 GHz. This frequency is chosen due to the highest DE at OPBO it can produce. The outphasing PA is simulated to have peak DE of more than 60 % at 6dB OPBO between frequency range of 2.18 GHz to 2.22 GHz. The peak DE at 10 dB OPBO reach above 55 % at 2.20 GHz.

# Chapter 8

## Conclusions and Future Work

### 8.1 Conclusions

A new reformulation of the CCF modes has been successfully attempted by combining the ideal waveforms formulation with the non-linear I-V knee interaction. The PA mode has different performances between the original ideal theory with the additional knee interaction. The device's knee voltage and the knee boundary are heavily considered in this thesis, due to the fact that the PA always operates with compression at peak power, where the load-lines always interacts with the knee, resulting into the non-linearities seen on the PA's output. The design of a single stage PA utilising CCF mode can be maximised when considering the  $\alpha = -1/+1$  regions only, because these region gives the highest efficiency across the entire  $\alpha$  space. In this thesis, a broadband PA is designed by carefully choosing the rotation of fundamental and 2<sup>nd</sup> harmonic impedances within  $\alpha = -1$  space, resulting in the highest efficiencies across the bandwidth. The measured broadband 10 W GaN RF PA achieved higher than 10 W peak output at 3 dB gain compression between 1.7 GHz to 2.7 GHz, reaching up to 18.4 W at 1.8 GHz. The DE measured at the peak

power is above 64.3 %, reaching up to 83.4 %. The PA is tested with modulated LTE signal, and the DPD system is able to correct the output signal to have ACLR below -55 dBc when the PA is operated at saturation. This measured performances from the PA shows the best performance trade-off between bandwidth, gain and efficiency among other PAs that has been published.

The separation between Pout and DE contours from the device is determined by the termination of the 2<sup>nd</sup> harmonic impedances. In this thesis, it has been proven through mathematical emulation, device simulations and measurements, that this separation is at the maximum when the 2<sup>nd</sup> harmonic impedances are terminated at the  $\alpha = \pm 1$ , from the CCF mode design space. A larger separation between these optima indicates the high peak efficiency that can be obtained at higher OPBO, which is beneficial for outphasing PA application. The practical separation between Pout and DE contours can be predicted in mathematical load-pull emulation, by incorporating non-linear I-V knee interaction between the drain waveforms. This load-pull contours prediction is much better than the classical load-pull calculation, when considering the optimum Pout, optimum DE and peak DE at OPBO.

A compact, high-efficiency and broadband PA is designed using integrated matching network, to reduce the overall size of the PA, as well as to integrate the PA with the easy access of baseband termination circuit to enhance the VBW. The baseband termination circuit consisting of high value single layer shunt capacitor, that is placed in close proximity to the device's output. By controlling the fundamental and 2<sup>nd</sup> harmonic impedances termination to the device within the  $\alpha = -1$  space across the bandwidth, the efficiency at peak power and 50  $\Omega$  load impedances is maximise. The peak efficiency is between 62.7 % to 73.6 % simulated at 50  $\Omega$  load across 1.8 GHz to 2.7 GHz. At load modulated OPBO, the efficiency is above 70 % and 60 % at -6dB and -8 dB OPBO

respectively. The VBW performances is extended up to 900 MHz, where no significant drop of DE and Pout when 2 modulated LTE signal with varied frequency spacing are tested.

## 8.2 Future Work

There are several potential works that can be further investigated, either to improve the works in this thesis, or to provide a new research investigation. Based on Chapter 3, the investigations of I-V knee interaction are only made to the CCF mode. The same waveform engineering technique can be applied to other PA modes, or even other PA architectures such as Doherty PA and outphasing PA, to include the non-linearity coming from the knee voltage.

Based on Chapter 5, the power and efficiency contours from load-pull emulation of CCF mode when  $\alpha = 0$  can be improved by controlling the 3<sup>rd</sup> harmonic of the voltage waveform. When the 3<sup>rd</sup> harmonic component of the waveform is increases, the waveform will be bouncy at the minimum, which will potentially be resulting into closer separation between optimum Pout and DE impedances, hence, lower peak DE at OPBO. The measurement of the device to verify the separation between Pout and DE contours across different 2<sup>nd</sup> harmonic tuning range could be increases to cover whole range across the edge of Smith chart. This will provide more data points to validate with the device's simulation. In fact, since the reformulation theory is based on the load-lines of the waveforms moving within the knee region, the load-pull measurement can be extended to measure the device at the CGP. This will allow the measurement of the drain current and voltage waveforms at optimum Pout and DE impedances, to validate with the predicted theoretical calculations.

The work in Chapter 6 focuses on the analyses of the baseband termination circuit on the output of the device. The analysis can be extended to reduce the baseband impedance and resonance at the device's input. It is crucial to reduce the resonance and impedances coming from the device's output as it will be affecting the performances at the device's output. For example, the 2<sup>nd</sup> harmonic on the device's input will have a great effect on the output's non-linearities, as well as the IMD3 separation. The effect of adding resistors on the bias network could also be investigated to reduce to magnitude of the low frequency resonant.

The work in Chapter 7 provides excellent simulation results for the compact PA design with integrated matching network and VBW enhancement. However, this PA has not yet been fabricated. It would be beneficial to verify the simulation results by fabricating this PA. The limitation to fabricate this PA is due to the financial resources, because the cost to operate the bondwires machine is high. Nevertheless, it is important to investigate several effects from the actual fabricated circuit. The bondwires connection in the 3D EM simulator assumed a perfect landing connection, whilst in reality, ball bonding or wedge bond add different topology to the actual bondwires shape. This could potential change the actual properties of the bondwires. The bondwires machine also have variation in their accuracy, depending on the machine and the person who is operating it. A sensitivity test can be done in the ideal circuit analysis to evaluate which structures of the bondwires that are sensitive for any small change. The connection between the active and passive components also assumed a perfect landing to the ground base. In reality, a conductive epoxy is usually used to attach the components to the metal ground base, which would change the parasitic capacitance between the components.



The analyses from the design of the broadband and compact PA with VBW enhancement in Chapter 7 have found that there's a major drop in the output power and efficiency between the device plane and the  $50\ \Omega$  termination, due to the integrated matching network. The integrated matching network has resulted into up to 12 % efficiency losses, when comparing the ideal circuit and the 3D EM simulated circuit performances. The losses along the passive components in the matching network such as the single layer capacitors and the bondwires can be reduced if the RF PA is designed to terminate 2<sup>nd</sup> harmonic impedances only. This will reduce the overall size of the integrated matching elements, where the fundamental impedances can be designed using a microstrip lines. In fact, in the outphasing PA applications, the 2<sup>nd</sup> harmonic impedances can be terminated as a single stage LC network using integrated matching network, to control the 2<sup>nd</sup> harmonic impedances rotations of the device, so that the optimum  $P_{out}$  and DE impedances have a large separation. The Chireix combiner network can be designed using microstrip lines, that also acts as the fundamental matching network and the delay lines.

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# MATLAB Code for Ideal CCF Mode

```
% import Smith Char from Excel
Xsmith = xlsread('Smith_Chart_Excel.xlsx','C2:C14801');
Ysmith = xlsread('Smith_Chart_Excel.xlsx','D2:D14801');

% fft sampling initialisation

fs=10000;
t=0:1/fs:2.0-1/fs;
f=50;
x=2*pi*f*t;

% 10W GaN initialisation

Vdc=28;
Imax=2.3;
Vknee=8;

% Set alpha range
alpha=transpose(-1:0.2:1);

% Ideal CCF Voltage Waveform equation

VgenCCFIdeal= (Vdc*(1 + 0.003 - (alpha*cos(x)) - (0.0003*alpha*cos(x)) +
(231/200*sin(x)) - (539/800*alpha*sin(2*x)) + (77/400*sin(3*x)) -
(77/800*alpha*sin(4*x))));

% Ideal Current Waveform

IgenIdeal= (Imax/2) * ((2/pi) - sin(x) - ((4/pi)*(1/3*cos(2*x) + 1/15*cos(4*x) +
1/35*cos(6*x) + 1/63*cos(8*x) + 1/99*cos(10*x))))+0.03;

% Waveform Plots
figure
yyaxis left
plot(x,VgenCCFIdeal(1,:))
hold on
plot(x,VgenCCFIdeal(11,:))
hold on
plot(x,VgenCCFIdeal(6,:))
axis([0 10 0 100])
xlabel('t')
ylabel('Drain Voltage (V)')
hold on
yyaxis right
plot(x,IgenIdeal)
```

```

hold off
axis([0 10 0 2.5])
ylabel('Drain Current (A)')
legend({'Voltage waveform a = -1','Voltage waveform a = 0','voltage waveform a = +1','Current Waveform'})

```

**% Load-lines with different alpha**

```

figure
plot(VgenCCFIdeal,IgenIdeal)
ylabel('Drain Current (A)')
xlabel('Drain Voltage (V)')
legend({'a=-1','a=-0.8','a=-0.6','a=-0.4','a=-0.2','a=0','a=0.2','a=0.4','a=0.6','a=0.8','a=1'})

```

**% FFT Ideal Current Waveform**

```

FFTIgenIdeal = fft(IgenIdeal)/10000;
IgenIdeal_f0 = FFTIgenIdeal(1)/2;
IgenIdeal_f1 = FFTIgenIdeal(101);
IgenIdeal_f2 = FFTIgenIdeal(201);
IgenIdeal_f3 = FFTIgenIdeal(301);

```

**% FFT Ideal CCF Voltage Waveform**

```

FFTVgenCCFIdeal = fft(VgenCCFIdeal,[],2)/10000;
VgenCCFIdeal_f0 = FFTVgenCCFIdeal(:,1)/2;
VgenCCFIdeal_f1 = FFTVgenCCFIdeal(:,101);
VgenCCFIdeal_f2 = FFTVgenCCFIdeal(:,201);
VgenCCFIdeal_f3 = FFTVgenCCFIdeal(:,301);

```

**% Performances Ideal CCF Mode**

```

PoutCCFIdeal = real(IgenIdeal_f1 * VgenCCFIdeal_f1)/2;
PoutCCFIdeal_dBm = real((10*log10(PoutCCFIdeal))+30);
PdcCCFIdeal = real(IgenIdeal_f0 * VgenCCFIdeal_f0);
EfficiencyCCFIdeal = PoutCCFIdeal ./ PdcCCFIdeal * 100;

```

**% Plot Pout and Efficiency against alpha**

```

figure
plot(alpha,PoutCCFIdeal)
hold on
plot(alpha,PoutCCFIdeal_dBm)
hold on
plot(alpha,EfficiencyCCFIdeal)
hold off
xlabel('a')
ylabel('DE (%), Pout(dBm), Pout (W)')
legend({'Pout (W)','Pout (dBm)','DE'})

```

% Impedances for Ideal CCF

```
Z_CCFIdeal_f1 = -(VgenCCFIdeal_f1/IgenIdeal_f1);  
Z_CCFIdeal_f2 = -(VgenCCFIdeal_f2/IgenIdeal_f2);  
Z_CCFIdeal_f3 = -(VgenCCFIdeal_f1/IgenIdeal_f3);
```

%Reference Impedance to fundamental impedance at alpha = 0

```
Zref=Z_CCFIdeal_f1(6);
```

%Convert Impedances to magnitude and phase for polar plot

```
Mag_CCFIdeal_f1 = abs((Z_CCFIdeal_f1-Zref)./(Z_CCFIdeal_f1+Zref));  
Phase_CCFIdeal_f1 = angle((Z_CCFIdeal_f1-Zref)./(Z_CCFIdeal_f1+Zref));
```

```
Mag_CCFIdeal_f2 = abs((Z_CCFIdeal_f2-Zref)./(Z_CCFIdeal_f2+Zref));  
Phase_CCFIdeal_f2 = angle((Z_CCFIdeal_f2-Zref)./(Z_CCFIdeal_f2+Zref));
```

```
Mag_CCFIdeal_f3 = abs((Z_CCFIdeal_f3-Zref)./(Z_CCFIdeal_f3+Zref));  
Phase_CCFIdeal_f3 = angle((Z_CCFIdeal_f3-Zref)./(Z_CCFIdeal_f3+Zref));
```

% Convert to cartesian

```
XCCFIdeal_f1=Mag_CCFIdeal_f1.*cos(Phase_CCFIdeal_f1);  
YCCFIdeal_f1=Mag_CCFIdeal_f1.*sin(Phase_CCFIdeal_f1);
```

```
XCCFIdeal_f2=Mag_CCFIdeal_f2.*cos(Phase_CCFIdeal_f2);  
YCCFIdeal_f2=Mag_CCFIdeal_f2.*sin(Phase_CCFIdeal_f2);
```

```
XCCFIdeal_f3=Mag_CCFIdeal_f3.*cos(Phase_CCFIdeal_f3);  
YCCFIdeal_f3=Mag_CCFIdeal_f3.*sin(Phase_CCFIdeal_f3);
```

% Impedances of CCF on Smith Chart

```
figure  
plot(Xsmith,Ysmith,'k','HandleVisibility','off')  
hold on  
scatter(XCCFIdeal_f1,YCCFIdeal_f1,'b','filled','SizeData',70)  
hold on  
scatter(XCCFIdeal_f2,YCCFIdeal_f2,'rs','filled','SizeData',70)  
hold on  
scatter(XCCFIdeal_f3,YCCFIdeal_f3,'gd','filled','SizeData',70)  
hold off  
legend({'Z1','Z2','Z3'})
```

# MATLAB Code for Emulating CCF Mode with Compression using I-V Knee Interaction

% fft sampling initialisation

```
fs=10000;  
t=0:1/fs:2.0-1/fs;  
f=50;  
x=2*pi*f*t;
```

% 10W GaN initialisation

```
Vdc=28;  
Imax=2.33;  
Vknee=8;
```

% Set alpha range

```
alpha=[-1;-0.8;-0.6;-0.4;-0.2;0;0.2;0.4;0.6;0.8;1];
```

% Set kappa, K range for voltage waveform scaling

```
K1=1;  
K2=1.085;  
K3=1.17;  
K4=1.25;  
K5=1.25;  
K6=1.25;
```

% Ideal Current Waveform

```
IgenIdeal= (Imax/2) * ((2/pi) - sin(x) - ((4/pi)*(1/3*cos(2*x) + 1/15*cos(4*x) +  
1/35*cos(6*x) + 1/63*cos(8*x) + 1/99*cos(10*x))))+0.03;
```

% New CCF Voltage Waveform with different K values

```
VgenCCF_K1=(Vdc-(Vknee/2))*(1+(K1*(0.003 - (alpha*cos(x)) -  
(0.0003*alpha*cos(x)) + (231/200*sin(x)) - (539/800*alpha*sin(2*x)) +  
(77/400*sin(3*x)) - (77/800*alpha*sin(4*x)))))+Vknee;
```

```
VgenCCF_K2=(Vdc-(Vknee/2))*(1+(K2*(0.003 - (alpha*cos(x)) -  
(0.0003*alpha*cos(x)) + (231/200*sin(x)) - (539/800*alpha*sin(2*x)) +  
(77/400*sin(3*x)) - (77/800*alpha*sin(4*x)))))+Vknee;
```



VgenCCF\_K3=(Vdc-(Vknee/2))\*(1+(K3\*(0.003 - (alpha\*cos(x)) - (0.0003\*alpha\*cos(x)) + (231/200\*sin(x)) - (539/800\*alpha\*sin(2\*x)) + (77/400\*sin(3\*x)) - (77/800\*alpha\*sin(4\*x)))))+Vknee;

VgenCCF\_K4=(Vdc-(Vknee/2))\*(1+(K4\*(0.003 - (alpha\*cos(x)) - (0.0003\*alpha\*cos(x)) + (231/200\*sin(x)) - (539/800\*alpha\*sin(2\*x)) + (77/400\*sin(3\*x)) - (77/800\*alpha\*sin(4\*x)))))+Vknee;

VgenCCF\_K5=(Vdc-(Vknee/2))\*(1+(K5\*(0.003 - (alpha\*cos(x)) - (0.0003\*alpha\*cos(x)) + (231/200\*sin(x)) - (539/800\*alpha\*sin(2\*x)) + (77/400\*sin(3\*x)) - (77/800\*alpha\*sin(4\*x)))))+Vknee;

VgenCCF\_K6=(Vdc-(Vknee/2))\*(1+(K6\*(0.003 - (alpha\*cos(x)) - (0.0003\*alpha\*cos(x)) + (231/200\*sin(x)) - (539/800\*alpha\*sin(2\*x)) + (77/400\*sin(3\*x)) - (77/800\*alpha\*sin(4\*x)))))+Vknee;

% Find minimum value from each voltage waveform

minVgenCCF\_K1=min(VgenCCF\_K1,[],2);  
minVgenCCF\_K2=min(VgenCCF\_K2,[],2);  
minVgenCCF\_K3=min(VgenCCF\_K3,[],2);  
minVgenCCF\_K4=min(VgenCCF\_K4,[],2);  
minVgenCCF\_K5=min(VgenCCF\_K5,[],2);  
minVgenCCF\_K6=min(VgenCCF\_K6,[],2);

% Convert to scaling for current waveform

Igenscale\_K1(1,:)=(minVgenCCF\_K1<Vknee) .\* (abs(minVgenCCF\_K1-Vknee)) + (minVgenCCF\_K1>=Vknee) .\* (0.01);  
Igenscale\_K2(1,:)=(minVgenCCF\_K2<Vknee) .\* (abs(minVgenCCF\_K2-Vknee)) + (minVgenCCF\_K2>=Vknee) .\* (0.01);  
Igenscale\_K3(1,:)=(minVgenCCF\_K3<Vknee) .\* (abs(minVgenCCF\_K3-Vknee)) + (minVgenCCF\_K3>=Vknee) .\* (0.01);  
Igenscale\_K4(1,:)=(minVgenCCF\_K4<Vknee) .\* (abs(minVgenCCF\_K4-Vknee)) + (minVgenCCF\_K4>=Vknee) .\* (0.01);  
Igenscale\_K5(1,:)=(minVgenCCF\_K5<Vknee) .\* (abs(minVgenCCF\_K5-Vknee)) + (minVgenCCF\_K5>=Vknee) .\* (0.01);  
Igenscale\_K6(1,:)=(minVgenCCF\_K6<Vknee) .\* (abs(minVgenCCF\_K6-Vknee)) + (minVgenCCF\_K6>=Vknee) .\* (0.01);

% New current waveform

IgenCCF\_K1=((1-exp(-VgenCCF\_K1 ./ Igenscale\_K1.')) .\* IgenIdeal);  
IgenCCF\_K2=((1-exp(-VgenCCF\_K2 ./ Igenscale\_K2.')) .\* IgenIdeal);  
IgenCCF\_K3=((1-exp(-VgenCCF\_K3 ./ Igenscale\_K3.')) .\* IgenIdeal);  
IgenCCF\_K4=((1-exp(-VgenCCF\_K4 ./ Igenscale\_K4.')) .\* IgenIdeal);  
IgenCCF\_K5=((1-exp(-VgenCCF\_K5 ./ Igenscale\_K5.')) .\* IgenIdeal);  
IgenCCF\_K6=((1-exp(-VgenCCF\_K6 ./ Igenscale\_K6.')) .\* IgenIdeal);

### % FFT CCF Voltage Waveform

```
FFTVgenCCF_K1 = fft(VgenCCF_K1,[],2)/10000;  
VgenCCF_K1_mag = abs(FFTVgenCCF_K1);  
VgenCCF_K1_f0 = FFTVgenCCF_K1(:,1)/2;  
VgenCCF_K1_f1 = FFTVgenCCF_K1(:,101);  
VgenCCF_K1_f2 = FFTVgenCCF_K1(:,201);  
VgenCCF_K1_f3 = FFTVgenCCF_K1(:,301);
```

```
FFTVgenCCF_K2 = fft(VgenCCF_K2,[],2)/10000;  
VgenCCF_K2_mag = abs(FFTVgenCCF_K2);  
VgenCCF_K2_f0 = FFTVgenCCF_K2(:,1)/2;  
VgenCCF_K2_f1 = FFTVgenCCF_K2(:,101);  
VgenCCF_K2_f2 = FFTVgenCCF_K2(:,201);  
VgenCCF_K2_f3 = FFTVgenCCF_K2(:,301);
```

```
FFTVgenCCF_K3 = fft(VgenCCF_K3,[],2)/10000;  
VgenCCF_K3_mag = abs(FFTVgenCCF_K3);  
VgenCCF_K3_f0 = FFTVgenCCF_K3(:,1)/2;  
VgenCCF_K3_f1 = FFTVgenCCF_K3(:,101);  
VgenCCF_K3_f2 = FFTVgenCCF_K3(:,201);  
VgenCCF_K3_f3 = FFTVgenCCF_K3(:,301);
```

```
FFTVgenCCF_K4 = fft(VgenCCF_K4,[],2)/10000;  
VgenCCF_K4_mag = abs(FFTVgenCCF_K4);  
VgenCCF_K4_f0 = FFTVgenCCF_K4(:,1)/2;  
VgenCCF_K4_f1 = FFTVgenCCF_K4(:,101);  
VgenCCF_K4_f2 = FFTVgenCCF_K4(:,201);  
VgenCCF_K4_f3 = FFTVgenCCF_K4(:,301);
```

```
FFTVgenCCF_K5 = fft(VgenCCF_K5,[],2)/10000;  
VgenCCF_K5_mag = abs(FFTVgenCCF_K5);  
VgenCCF_K5_f0 = FFTVgenCCF_K5(:,1)/2;  
VgenCCF_K5_f1 = FFTVgenCCF_K5(:,101);  
VgenCCF_K5_f2 = FFTVgenCCF_K5(:,201);  
VgenCCF_K5_f3 = FFTVgenCCF_K5(:,301);
```

```
FFTVgenCCF_K6 = fft(VgenCCF_K6,[],2)/10000;  
VgenCCF_K6_mag = abs(FFTVgenCCF_K6);  
VgenCCF_K6_f0 = FFTVgenCCF_K6(:,1)/2;  
VgenCCF_K6_f1 = FFTVgenCCF_K6(:,101);  
VgenCCF_K6_f2 = FFTVgenCCF_K6(:,201);  
VgenCCF_K6_f3 = FFTVgenCCF_K6(:,301);
```

## % FFT CCF Current Waveform

```
FFTIGenCCF_K1 = fft(IgenCCF_K1,[],2)/10000;  
IgenCCF_K1_mag = abs(FFTIGenCCF_K1);  
IgenCCF_K1_f0 = FFTIGenCCF_K1(:,1)/2;  
IgenCCF_K1_f1 = FFTIGenCCF_K1(:,101);  
IgenCCF_K1_f2 = FFTIGenCCF_K1(:,201);  
IgenCCF_K1_f3 = FFTIGenCCF_K1(:,301);
```

```
FFTIGenCCF_K2 = fft(IgenCCF_K2,[],2)/10000;  
IgenCCF_K2_mag = abs(FFTIGenCCF_K2);  
IgenCCF_K2_f0 = FFTIGenCCF_K2(:,1)/2;  
IgenCCF_K2_f1 = FFTIGenCCF_K2(:,101);  
IgenCCF_K2_f2 = FFTIGenCCF_K2(:,201);  
IgenCCF_K2_f3 = FFTIGenCCF_K2(:,301);
```

```
FFTIGenCCF_K3 = fft(IgenCCF_K3,[],2)/10000;  
IgenCCF_K3_mag = abs(FFTIGenCCF_K3);  
IgenCCF_K3_f0 = FFTIGenCCF_K3(:,1)/2;  
IgenCCF_K3_f1 = FFTIGenCCF_K3(:,101);  
IgenCCF_K3_f2 = FFTIGenCCF_K3(:,201);  
IgenCCF_K3_f3 = FFTIGenCCF_K3(:,301);
```

```
FFTIGenCCF_K4 = fft(IgenCCF_K4,[],2)/10000;  
IgenCCF_K4_mag = abs(FFTIGenCCF_K4);  
IgenCCF_K4_f0 = FFTIGenCCF_K4(:,1)/2;  
IgenCCF_K4_f1 = FFTIGenCCF_K4(:,101);  
IgenCCF_K4_f2 = FFTIGenCCF_K4(:,201);  
IgenCCF_K4_f3 = FFTIGenCCF_K4(:,301);
```

```
FFTIGenCCF_K5 = fft(IgenCCF_K5,[],2)/10000;  
IgenCCF_K5_mag = abs(FFTIGenCCF_K5);  
IgenCCF_K5_f0 = FFTIGenCCF_K5(:,1)/2;  
IgenCCF_K5_f1 = FFTIGenCCF_K5(:,101);  
IgenCCF_K5_f2 = FFTIGenCCF_K5(:,201);  
IgenCCF_K5_f3 = FFTIGenCCF_K5(:,301);
```

```
FFTIGenCCF_K6 = fft(IgenCCF_K6,[],2)/10000;  
IgenCCF_K6_mag = abs(FFTIGenCCF_K6);  
IgenCCF_K6_f0 = FFTIGenCCF_K6(:,1)/2;  
IgenCCF_K6_f1 = FFTIGenCCF_K6(:,101);  
IgenCCF_K6_f2 = FFTIGenCCF_K6(:,201);  
IgenCCF_K6_f3 = FFTIGenCCF_K6(:,301);
```

### % Performances CCF Mode with Compression

```
PoutCCF_K1 = real(IgenCCF_K1_f1 .* VgenCCF_K1_f1)/2;  
PdcCCF_K1 = real(IgenCCF_K1_f0 .* VgenCCF_K1_f0);  
EfficiencyCCF_K1 = PoutCCF_K1 ./ PdcCCF_K1 * 100;
```

```
PoutCCF_K2 = real(IgenCCF_K2_f1 .* VgenCCF_K2_f1)/2;  
PdcCCF_K2 = real(IgenCCF_K2_f0 .* VgenCCF_K2_f0);  
EfficiencyCCF_K2 = PoutCCF_K2 ./ PdcCCF_K2 * 100;
```

```
PoutCCF_K3 = real(IgenCCF_K3_f1 .* VgenCCF_K3_f1)/2;  
PdcCCF_K3 = real(IgenCCF_K3_f0 .* VgenCCF_K3_f0);  
EfficiencyCCF_K3 = PoutCCF_K3 ./ PdcCCF_K3 * 100;
```

```
PoutCCF_K4 = real(IgenCCF_K4_f1 .* VgenCCF_K4_f1)/2;  
PdcCCF_K4 = real(IgenCCF_K4_f0 .* VgenCCF_K4_f0);  
EfficiencyCCF_K4 = PoutCCF_K4 ./ PdcCCF_K4 * 100;
```

```
PoutCCF_K5 = real(IgenCCF_K5_f1 .* VgenCCF_K5_f1)/2;  
PdcCCF_K5 = real(IgenCCF_K5_f0 .* VgenCCF_K5_f0);  
EfficiencyCCF_K5 = PoutCCF_K5 ./ PdcCCF_K5 * 100;
```

```
PoutCCF_K6 = real(IgenCCF_K6_f1 .* VgenCCF_K6_f1)/2;  
PdcCCF_K6 = real(IgenCCF_K6_f0 .* VgenCCF_K6_f0);  
EfficiencyCCF_K6 = PoutCCF_K6 ./ PdcCCF_K6 * 100;
```

### % Plot Load-line at each alpha

#### % alpha = 0

figure

```
plot(VgenCCF_K1(6,:),IgenCCF_K1(6,:),VgenCCF_K2(6,:),IgenCCF_K2(6,:),VgenC  
CF_K3(6,:),IgenCCF_K3(6,:),VgenCCF_K4(6,:),IgenCCF_K4(6,:),VgenCCF_K5(6,:),I  
genCCF_K5(6,:),VgenCCF_K6(6,:),IgenCCF_K6(6,:))
```

#### % alpha = 0.6/-0.6

figure

```
plot(VgenCCF_K1(3,:),IgenCCF_K1(3,:),VgenCCF_K2(3,:),IgenCCF_K2(3,:),VgenC  
CF_K3(3,:),IgenCCF_K3(3,:),VgenCCF_K4(3,:),IgenCCF_K4(3,:),VgenCCF_K5(3,:),I  
genCCF_K5(3,:),VgenCCF_K6(3,:),IgenCCF_K6(3,:))
```

#### % alpha = 1/-1

figure

```
plot(VgenCCF_K1(1,:),IgenCCF_K1(1,:),VgenCCF_K2(1,:),IgenCCF_K2(1,:),VgenC  
CF_K3(1,:),IgenCCF_K3(1,:),VgenCCF_K4(1,:),IgenCCF_K4(1,:),VgenCCF_K5(1,:),I  
genCCF_K5(1,:),VgenCCF_K6(1,:),IgenCCF_K6(1,:))
```

```
% Plot Pout at different K against alpha
```

```
figure
```

```
plot(alpha,PoutCCF_K1,alpha,PoutCCF_K2,alpha,PoutCCF_K3,alpha,PoutCCF_K4,alpha,PoutCCF_K5)
```

```
% Plot Efficiency at different K against alpha
```

```
figure
```

```
plot(alpha,EfficiencyCCF_K1,alpha,EfficiencyCCF_K2,alpha,EfficiencyCCF_K3,alpha,EfficiencyCCF_K4,alpha,EfficiencyCCF_K5)
```

```
%plot waveform for a=0
```

```
figure
```

```
yyaxis left
```

```
plot(x,VgenCCF_K4(6,:))
```

```
hold on
```

```
plot(x,VgenCCF_K3(6,:))
```

```
hold on
```

```
plot(x,VgenCCF_K2(6,:))
```

```
hold on
```

```
plot(x,VgenCCF_K1(6,:))
```

```
hold on
```

```
axis([0 10 0 70])
```

```
yyaxis right
```

```
plot(x,IgenCCF_K4(6:),'HandleVisibility','off')
```

```
hold on
```

```
plot(x,IgenCCF_K3(6:),'HandleVisibility','off')
```

```
hold on
```

```
plot(x,IgenCCF_K2(6:),'HandleVisibility','off')
```

```
hold on
```

```
plot(x,IgenCCF_K1(6:),'HandleVisibility','off')
```

```
hold off
```

```
axis([0 10 0 2.5])
```

```
legend({'Vmin = 2V','Vmin = 4V','Vmin = 6V','Vmin = 8V'})
```

```

%plot waveform for a=1
figure
yyaxis left
plot(x,VgenCCF_K4(11,:))
hold on
plot(x,VgenCCF_K3(11,:))
hold on
plot(x,VgenCCF_K2(11,:))
hold on
plot(x,VgenCCF_K1(11,:))
hold on
axis([0 10 0 110])
yyaxis right
plot(x,IgenCCF_K4(11,:), 'HandleVisibility','off')
hold on
plot(x,IgenCCF_K3(11,:), 'HandleVisibility','off')
hold on
plot(x,IgenCCF_K2(11,:), 'HandleVisibility','off')
hold on
plot(x,IgenCCF_K1(11,:), 'HandleVisibility','off')
hold off
axis([0 10 0 2.5])
legend({'Vmin = 2V', 'Vmin = 4V', 'Vmin = 6V', 'Vmin = 8V'})

```

# MATLAB Code for Generating Contour Plots of CCF Mode with Non-linear I-V Knee Interaction

```
% import Smith Chart from Excel
Xsmith = xlsread('Smith_Chart_Excel.xlsx','C2:C14801');
Ysmith = xlsread('Smith_Chart_Excel.xlsx','D2:D14801');

% fft sampling initialisation
fs=10000;
t=0:1/fs:2.0-1/fs;
f=50;
x=2*pi*f*t;

% 10W GaN initialisation
Vdc=28;
Imax=2.33;
Vknee=8;
Idq = 0.02; %add small current from Class-AB bias to avoid >100% DE

%Set alpha value (-1 to +1 range)
alpha=0;

% Ideal current waveform
IgenIdeal= (Imax/2) * ((2/pi) - sin(x) - ((4/pi)*(1/3*cos(2*x) + 1/15*cos(4*x) + 1/35*cos(6*x) + 1/63*cos(8*x) + 1/99*cos(10*x)))) + Idq ;

% New voltage waveform with knee voltage
VgenCCF_K1_a0=(Vdc-(Vknee/2))*(1+(0.003 - (alpha*cos(x)) - (0.0003*alpha*cos(x)) + (231/200*sin(x)) - (539/800*alpha*sin(2*x)) + (77/400*sin(3*x)) - (77/800*alpha*sin(4*x))))+Vknee;

%FFT voltage waveform
FFTVgenCCF_K1_a0 = fft(VgenCCF_K1_a0,[],2)/10000;
VgenCCF_K1_f1 = FFTVgenCCF_K1_a0(:,101);

%set dV
dV=(0.1:0.05:1.6).'; %0.1:0.01:1.6`

% set dtheta
dtheta=(-84:4:84); %

%Manipulate fundamental component
NewCCF_F1=((abs(VgenCCF_K1_f1))*dV) .* exp(1i*(angle(VgenCCF_K1_f1)+(dtheta/180*pi)));
```

% flatten matrices above

```
NewCCF_f1=reshape(NewCCF_F1,[],1);
```

%Put fundamental component back into full waveform equation

```
NewVgenCCF_K1_a0= (real(NewCCF_f1)*cos(x)-imag(NewCCF_f1)*sin(x))+(Vdc-  
(Vknee/2))*(1+(0.003 - (539/800*alpha*sin(2*x)) + (77/400*sin(3*x)) -  
(77/800*alpha*sin(4*x))))+Vknee;
```

%take only positive voltage waveform above 0.2V

```
NewVgenCCF_K1_a0(any(NewVgenCCF_K1_a0<=0.2,2),:)=[];
```

%Obtain the minimum of the voltage waveforms

```
minNewVgenCCF_K1_a0=min(NewVgenCCF_K1_a0,[],2);
```

%Imax scale

```
ImaxScale(1,:)= (minNewVgenCCF_K1_a0<=Vknee) .*  
(((Imax)/Vknee)*minNewVgenCCF_K1_a0)) + (minNewVgenCCF_K1_a0>=Vknee)  
.* (Imax) ;
```

% scaling for Imax of current waveforms

```
Igenscale_K1_a0(1,:)=(minNewVgenCCF_K1_a0<Vknee) .*  
(abs(minNewVgenCCF_K1_a0-Vknee)) + (minNewVgenCCF_K1_a0>=Vknee) .*  
(0.01);
```

% New current waveforms

```
NewIgenCCF_K1_a0=((1-exp(-NewVgenCCF_K1_a0 ./ Igenscale_K1_a0.')) .*  
((ImaxScale./2) * ((2/pi) - sin(x) - ((4/pi)*(1/3*cos(2*x) + 1/15*cos(4*x) +  
1/35*cos(6*x) + 1/63*cos(8*x) + 1/99*cos(10*x)))) + Idq ));
```

% FFT Voltage waveforms

```
FFTNewVgenCCF_K1_a0 = fft(NewVgenCCF_K1_a0,[],2)/10000;  
NewVgenCCF_K1_a0_f0 = FFTNewVgenCCF_K1_a0(:,1)/2;  
NewVgenCCF_K1_a0_f1 = FFTNewVgenCCF_K1_a0(:,101);  
NewVgenCCF_K1_a0_f2 = FFTNewVgenCCF_K1_a0(:,201);  
NewVgenCCF_K1_a0_f3 = FFTNewVgenCCF_K1_a0(:,301);
```

% FFT Current Waveforms

```
FFTNewIgenCCF_K1_a0 = fft(NewIgenCCF_K1_a0,[],2)/10000;  
NewIgenCCF_K1_a0_f0 = FFTNewIgenCCF_K1_a0(:,1)/2;  
NewIgenCCF_K1_a0_f1 = FFTNewIgenCCF_K1_a0(:,101);  
NewIgenCCF_K1_a0_f2 = FFTNewIgenCCF_K1_a0(:,201);  
NewIgenCCF_K1_a0_f3 = FFTNewIgenCCF_K1_a0(:,301);
```



**% Calculate performances**

```
PoutCCF_K1_a0_W = real(NewIgenCCF_K1_a0_f1 .* NewVgenCCF_K1_a0_f1)/2;  
PoutCCF_K1_a0_dBm = real((10*log10(PoutCCF_K1_a0_W))+30);  
PdcCCF_K1_a0 = real(NewIgenCCF_K1_a0_f0 .* NewVgenCCF_K1_a0_f0);  
EfficiencyCCF_K1_a0 = PoutCCF_K1_a0_W ./ PdcCCF_K1_a0 * 100;
```

**% Set reference impedance**

```
Zref=50;
```

**%Calculate fundamental impedances**

```
ZNewCCF_K1_a0_f1 = -(NewVgenCCF_K1_a0_f1./NewIgenCCF_K1_a0_f1);  
Mag_NewCCF_K1_a0_f1 = abs((ZNewCCF_K1_a0_f1 -  
Zref)/(ZNewCCF_K1_a0_f1+Zref));  
Phase_Mag_NewCCF_K1_a0_f1 = angle((ZNewCCF_K1_a0_f1 -  
Zref)/(ZNewCCF_K1_a0_f1+Zref));
```

**%Calculate 2nd harmonic impedances**

```
ZNewCCF_K1_a0_f2 = -(NewVgenCCF_K1_a0_f2./NewIgenCCF_K1_a0_f2);  
Mag_NewCCF_K1_a0_f2 = abs((ZNewCCF_K1_a0_f2 -  
Zref)/(ZNewCCF_K1_a0_f2+Zref));  
Phase_Mag_NewCCF_K1_a0_f2 = angle((ZNewCCF_K1_a0_f2 -  
Zref)/(ZNewCCF_K1_a0_f2+Zref));
```

**%Calculate 3rd harmonic impedances**

```
ZNewCCF_K1_a0_f3 = -(NewVgenCCF_K1_a0_f3./NewIgenCCF_K1_a0_f3);  
Mag_NewCCF_K1_a0_f3 = abs((ZNewCCF_K1_a0_f3 -  
Zref)/(ZNewCCF_K1_a0_f3+Zref));  
Phase_Mag_NewCCF_K1_a0_f3 = angle((ZNewCCF_K1_a0_f3 -  
Zref)/(ZNewCCF_K1_a0_f3+Zref));
```

**% Convert polar form impedances to cartesian form**

```
XNewCCF_K1_a0_f1=Mag_NewCCF_K1_a0_f1.*cos(Phase_Mag_NewCCF_K1_a0_f1  
);  
YNewCCF_K1_a0_f1=Mag_NewCCF_K1_a0_f1.*sin(Phase_Mag_NewCCF_K1_a0_f1  
);  
XNewCCF_K1_a0_f2=Mag_NewCCF_K1_a0_f2.*cos(Phase_Mag_NewCCF_K1_a0_f2  
);  
YNewCCF_K1_a0_f2=Mag_NewCCF_K1_a0_f2.*sin(Phase_Mag_NewCCF_K1_a0_f2  
);  
XNewCCF_K1_a0_f3=Mag_NewCCF_K1_a0_f3.*cos(Phase_Mag_NewCCF_K1_a0_f3  
);  
YNewCCF_K1_a0_f3=Mag_NewCCF_K1_a0_f3.*sin(Phase_Mag_NewCCF_K1_a0_f3  
);
```

```

% Creating grids for contour function
[xi, yi] =
meshgrid(linspace(min(XNewCCF_K1_a0_f1),max(XNewCCF_K1_a0_f1)),linspace(mi
n(YNewCCF_K1_a0_f1),max(YNewCCF_K1_a0_f1)));
PoutContour_W =
griddata(XNewCCF_K1_a0_f1,YNewCCF_K1_a0_f1,PoutCCF_K1_a0_W,xi,yi);
PoutContour_dBm =
griddata(XNewCCF_K1_a0_f1,YNewCCF_K1_a0_f1,PoutCCF_K1_a0_dBm,xi,yi);
EfficiencyContour =
griddata(XNewCCF_K1_a0_f1,YNewCCF_K1_a0_f1,EfficiencyCCF_K1_a0,xi,yi);

% Plotting Pout and DE contours on Smith Chart
figure
plot(Xsmith,Ysmith,'k')
hold on
[C,h]=contour(xi,yi,PoutContour_dBm,max(PoutCCF_K1_a0_dBm)-
10:1:max(PoutCCF_K1_a0_dBm),'blue','ShowText','on');
clabel(C,h,'FontSize',10,'Color','blue','LabelSpacing',300)
hold on
[C,h]=contour(xi,yi,EfficiencyContour,max(EfficiencyCCF_K1_a0)-
80:4:max(EfficiencyCCF_K1_a0),'red','ShowText','on');
clabel(C,h,'FontSize',10,'Color','red','LabelSpacing',300)
hold off
title('Pout and DE Contours')

```

# **Publication 1**

## **Title:**

High-Efficiency Broadband PA Design Based on Continuous Class-F Mode with Compression

## **Authors:**

**S. M. H. Syed Anera**, T. Hussein, S. Alsahali, J. J. Bell, R. Quaglia, M. Kermalli, P. J. Tasker and J. Benedikt

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# High-Efficiency Broadband PA Design Based on Continuous Class-F Mode with Compression

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**Abstract**— The paper presents a novel reformulation of the Continuous Class-F (CCF) mode by including an I-V knee scaling equation in the drain current waveform. The device's knee region scales down the waveform and distorts the ideal flat performances especially when the device is in compression. The output power and drain efficiency are no longer constant across  $\alpha$  variation in the CCF mode. Instead, symmetrical performances across  $\alpha$  space are simulated and measured showing drain efficiency is at peak when  $\alpha$  is at its extreme: +1 or -1. 10W GaN HEMT broadband PA (1.7 GHz to 2.7 GHz) is designed by restricting phase rotation of 2<sup>nd</sup> harmonic impedances within  $\alpha=1$  ranges across bandwidth. The manufactured PA achieved 11.3W-18.4W Pout and 65.7%-83.4% DE. When operated with 10MHz LTE signal with 7.6dB PAPR at 2.7 GHz, the PA achieved ACPR levels of -53.6/-54.6 dBc after DPD.

**Keywords**—Broadband, continuous modes, power amplifiers, high efficiency, digital predistortion (DPD).

## I. INTRODUCTION

The CCF mode is an extension of Class-F mode in which the original square waveform is multiplied with the continuous operator,  $1 - \alpha \cos(\theta)$ , giving a set of drain voltage waveforms, expanded in (1) [1]. The range of  $\alpha$  values are only valid between -1 and +1. On the other hand, the drain current waveform is a half-rectified sinusoidal shape shown in (2). Both (1) and (2) represent the ideal CCF mode, which does not include the practical transistor non-linearity coming from the knee region. For plotting the current and voltage waveforms, values of a 10W Wolfspeed packaged device, CGH40010F, are utilized with the Vdc and I<sub>max</sub> values of 28V and 2.33A, respectively.

$$V_{ds}(\theta) = V_{dc} * \left( 1 - \alpha \cos\theta + \frac{231}{200} \sin\theta - \frac{539}{800} \alpha \sin 2\theta + \frac{77}{400} \sin 3\theta - \frac{77}{800} \alpha \sin 4\theta \right) + V_{dc} \text{Offset} \quad (1)$$

$$I_{ds}(\theta) = \frac{I_{max}}{2} * \left( \frac{2}{\pi} \pm \sin\theta - \frac{4}{\pi} * \sum_{r=1}^{11} \frac{\cos(2r\theta)}{(2r)^2 - 1} \right) + I_{dc} \text{Offset} \quad (2)$$

Both ideal drain voltage and current waveforms for CCF mode are shown in Fig. 1. The voltage waveform changes with  $\alpha$  ranges while the current waveform is maintained the same. Constant output power and efficiency is theoretically achieved as reported in [1], which depends on the number of harmonics in the waveforms. Harmonics tuning has been discussed in [2]-

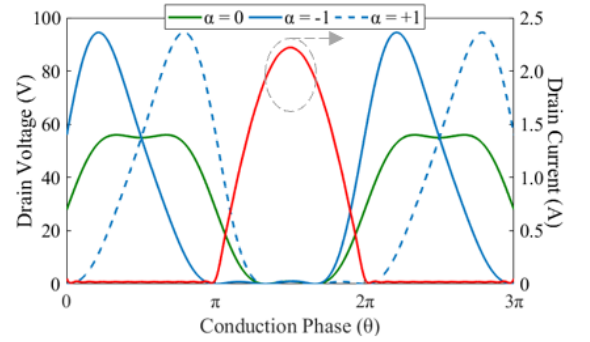


Fig. 1 Intrinsic drain current and voltage waveforms for the classic ideal CCF mode for  $-1 \leq \alpha \leq +1$  plotted using (1) and (2).

[3], leading to an improvement of power amplifier efficiency through waveshaping.

## II. I-V KNEE EFFECT ON CCF MODE

To model a realistic transistor operation, the knee clipping region should not be ignored. The knee region affects the performance of the transistor by introducing a relation between current and voltage waveform [2] and [4]. In (3), the drain voltage waveform and the knee voltage scale the drain current waveform. This property gives a concept of I-V knee relationship for a realistic operation of transistor within the gain compression region.

$$I_{ds,knee}(\theta) = \left( 1 - e^{-\left( \frac{V_{ds}(\theta)}{V_{knee}} \right)} \right) * I_{ds}(\theta) \quad (3)$$

This paper introduced a modification on both voltage and current waveforms to accurately represent these waveforms in a compressed CCF mode through load-line analysis. In (4),  $\kappa$  is introduced to scale the magnitude of fundamental and harmonic components of the voltage waveform to emulate the compression of the device outputs. The default value of  $\kappa$  is 1 and it is valid when  $1 \leq \kappa \leq 4/3$  to keep the voltage waveform above 0 to abide the device's physics. At this default value, the device is in the linear region, and the minimum of the voltage waveform is equal to the knee voltage of the device, defined here at the drain voltage value (8V) at the maximum drain current I<sub>max</sub>. As  $\kappa$  increases, the device is further compressed, and it enters the non-linear knee region.

$$V_{ds,new}(\theta) = \left( V_{dc} - \frac{V_{knee}}{2} \right) * \left( 1 + \kappa \left( -\alpha \cos\theta + \frac{231}{200} \sin\theta - \frac{539}{800} \alpha \sin 2\theta + \frac{77}{400} \sin 3\theta - \frac{77}{800} \alpha \sin 4\theta \right) + V_{knee} \right) \quad (4)$$

$$I_{ds,new}(\theta) = \left( 1 - e^{-\left( \frac{V_{ds,new}(\theta)}{\gamma} \right)} \right) * I_{ds}(\theta) \quad (5a)$$

$$\gamma = \begin{cases} \min(V_{ds,new}(\theta)) - V_{knee} & \text{if } \min(V_{ds,new}(\theta)) < V_{knee} \\ 0.01 & \text{if } \min(V_{ds,new}(\theta)) \geq V_{knee} \end{cases} \quad (5b)$$

In [2],  $V_{knee}$  has a constant value, whereas [5] suggested a varying  $V_{knee}$  that leads to separation of power and efficiency optimum impedances. The current waveform equation is modified, shown in (5). In (5a), the knee voltage scaling is a function of the minimum from the voltage waveform that can be represented by a piecewise function, detailed in (5b). Fig. 2 shows the load-lines of the modified CCF mode for  $\alpha=0$  (thick lines) and  $\alpha=-1/+1$  (thin lines) and  $\kappa$  is varied so that the minimum of the voltage waveforms is set to 2V, 4V, 6V and 8V respectively. The movement of these load-lines is tracking with the knee boundary region of the device (shown on the grey dotted lines).

Fig. 3 shows the new emulated efficiency performances of CCF mode with compression from the generated load-lines in Fig. 2. The drain efficiency increases as the load-lines moves further into knee region and peaks when  $\alpha = -1/+1$ . The drain efficiency is at minimum when  $\alpha = 0$ , as in Class-F mode.

### III. CCF MODE SIMULATION FOR 10W GAN DEVICE WITH COMPRESSION

10W GaN HEMT packaged device from Wolfspeed (CGH40010F) is used to test the new CCF theory in previous

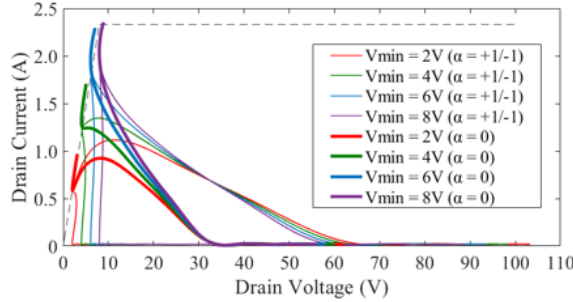


Fig. 2. Load-lines of intrinsic drain waveform for CCF mode using modification of I-V knee scaling with compression.

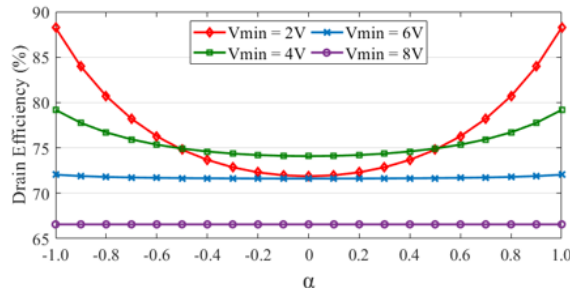


Fig. 3. Emulated drain efficiency of CCF mode at different level of compression within  $\alpha$  spaces.

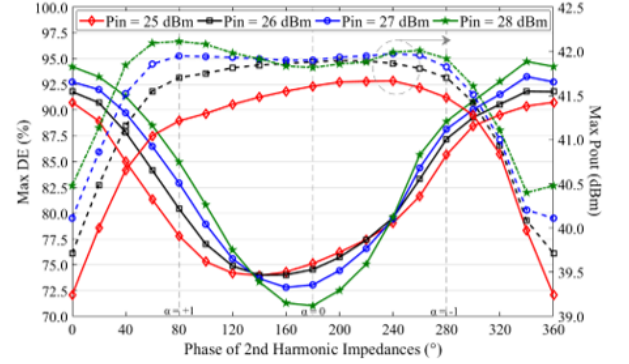


Fig. 4. Max DE and Pout obtained from simulated fundamental load-pull of 10W packaged device at different phase of 2<sup>nd</sup> harmonic impedances and Pin.

section. ADS load-pull simulation are performed on the device's non-linear model and the device is de-embedded at the output plane so that the fundamental and harmonics load impedances are presented at the device's intrinsic drain plane. To simulate CCF mode on the 10W device, the fundamental load impedances are swept across the entire region of the Smith Chart while the 2<sup>nd</sup> harmonic load impedances are swept from 80° to 280° around the edge of Smith Chart. The variation of 2<sup>nd</sup> harmonic impedances equals the  $\alpha$  space of CCF mode, which for this device, 80°, 180° and 280° is equal to  $\alpha = +1$ ,  $\alpha = 0$  and  $\alpha = -1$  respectively. The 3<sup>rd</sup> harmonic impedances are kept constant at an open circuit for all simulation points. The device is biased at 28 V and -3.2 V at drain and gate respectively ( $I_{dq}=13\text{mA}$ ) and driven into compression by an RF input of 2.0 GHz with 50 $\Omega$  source impedances and Pin = 25, 26, 27 and 28 dBm.

Fig. 4 shows the maximum output power exceeds 10W (40 dBm) for all swept input powers and phases of 2<sup>nd</sup> harmonic impedances within the  $\alpha$  space (approximately 80° to 280°). The device achieved its saturated output power (>15W) at about 4 dB gain compression for a source input power of 28 dBm. The changes of maximum output power with phase of 2<sup>nd</sup> harmonic impedances are minimum when the device is compressed and has reached its saturation point. The maximum DE shows symmetrical changes with the phase of the 2<sup>nd</sup> harmonic impedances. Within the  $\alpha$  space, DE is highest at the boundaries and lowest for in the middle ( $\alpha=0$ ) of the  $\alpha$  space. The overall variation of DE approaches 20% and is in good agreement with the emulated data in Fig. 3. Although maximum DE continuous to increase outside the restricted  $\alpha$  spaces, the maximum Pout shows a steep drop indicating a restriction for 2nd harmonics impedances that can be utilized for the CCF mode.

### IV. CCF MODE MEASUREMENT FOR 10W GAN DEVICE WITH COMPRESSION

The device is measured on a test fixture with an active load-pull system to confirm with the previous ADS simulation. The device is biased with 28V and -2.85V at the drain and gate respectively ( $I_{dq} = 13\text{mA}$ ) through bias tees. CW signal from a signal generator with 50 $\Omega$  characteristic impedance at 2.0 GHz is connected to the device's input through a driver amplifier. The magnitude of the signal generator is varied from 9 dBm to 11 dBm. Two signal generators are connected to the device output through two separate driver amplifiers, to control



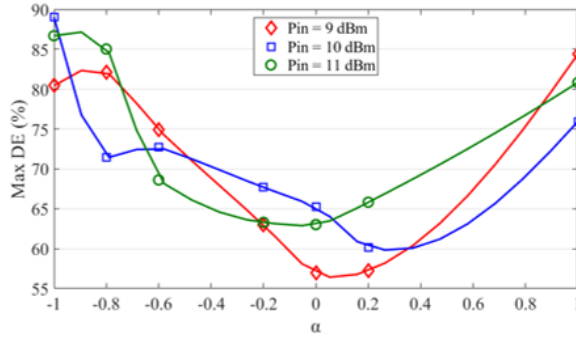


Fig. 5. Max DE obtained from measured fundamental load-pull of 10W packaged device with respect to  $\alpha$  space and Pin from signal generator.

the fundamental and 2<sup>nd</sup> harmonic impedances presented to the device package plane.

Fundamental impedances are swept throughout the Smith Chart while the 2<sup>nd</sup> harmonic impedances are controlled at the edge of Smith Chart with different phases. Meanwhile the 3<sup>rd</sup> harmonic impedances are not controlled due to their small impact on the device performances [6]. All these impedances are presented and measured at the device's package plane within the test fixture. Due to the package's parasitic effect, the phases of 2<sup>nd</sup> harmonic impedances that need to be presented at the package plane are shifted from the phases presented at the device's current generator plane, which were used in the previous section. The phases representing  $\alpha$  space (-1, 0 and +1) at the device's current generator plane from the package plane are: 100°, 200° and 165° respectively at 2.0 GHz.

Fig. 5 shows the maximum DE obtained from each fundamental load-pull with 7 different phases of 2<sup>nd</sup> harmonic impedances chosen within the  $\alpha$  space at 3 input drive levels. Maximum Pin = 11 dBm from signal generator provides up to 29 dBm to the device input after been amplified by the driver amplifier. Minimum DE measured at  $\alpha$  close to 0 for all 3 input drives and increases from 57% to 63.7% as Pin increases. The maximum DE are measured at both ends of the  $\alpha$  range. The difference between max DE obtained at  $\alpha = -1$  and  $\alpha = 0$  for Pin = 11 dBm is 23%, which is slightly larger than the emulated and simulated data

#### V. DESIGN OF BROADBAND 10W GAN PA BY RESTRICTING PHASE ROTATION OF 2<sup>ND</sup> HARMONIC IMPEDANCES

New theoretical analysis of CCF mode in previous sections shows that the peak efficiencies are reached for  $\alpha = -1/+1$  when it is operated in the non-linear knee region. As most of modern RF GaN devices are operated at similar compression values at the peak powers, limiting the  $\alpha$  space to maintain the high efficiencies is an attractive design approach. A similar 10W GaN device (CG2H40010F) is used to a design broadband PA by exploiting the CCF mode with a restricted 2<sup>nd</sup> harmonic impedance rotation to keep the efficiency high. Fig. 6 shows the fabricated PA circuit layout. The design of this circuit focuses on controlling the fundamental and 2<sup>nd</sup> harmonic impedances to be on the optimum  $\alpha = -1$  throughout the bandwidth. Fig. 7 shows the simulated fundamental (1.7-2.7 GHz) and 2<sup>nd</sup> harmonic impedances (3.4-5.4 GHz) presented at the package and current generator plane of the

device. The impedances at current generator plane are obtained from available voltage and current nodes at the intrinsic plane provided by the device's model.

Fig. 8 shows the comparison of simulated and measured CW performances of the fabricated PA at 3 dB output gain compression. A maximum of 83.4% DE is obtained at 1.8 GHz while the DE stays above 65.7% across bandwidth with average of 71.7%. The output power varies between 11.3W to 18.4W across bandwidth with average of 14.4W. The transducer gain is 15 dB  $\pm$  3.4 dB. The measured gain at lower frequencies are significantly higher than the values obtained in the simulation due to the mismatch in the input matching network, leading to lower input power needed to drive the PA into 3dB gain compression. Solid green line in Fig. 7 shows the actual mismatched Z<sub>in</sub> which moves further away into the device's optimum source impedance for the lower frequency from to the ideal simulated Z<sub>in</sub> (dotted green line). Meanwhile the simulated fundamental impedances presented at the package plane in Fig. 7 represent a trade-off between the optimum P<sub>out</sub> and DE impedances, which were obtained from load-pull simulation on the device across the bandwidth.

The applicability of the PA in communication system is tested by applying a 10 MHz LTE signal (centered at 2.0 GHz, 2.5 GHz and 2.7 GHz) and DPD system is used to improve the linearity of the PA. The LTE signal has peak to average ratio (PAPR) of 7.6 dB. Fig. 9 shows the normalized output spectra of the PA before and after DPD linearization. The ACPR before DPD is applied ranges between -33.5 dBc to -40.4 dBc and has

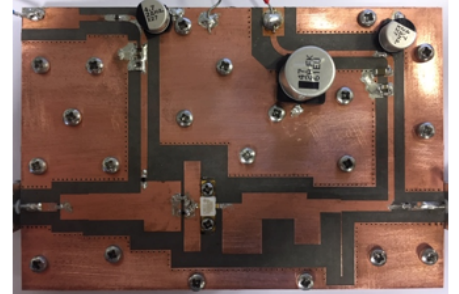


Fig. 6. Fabricated 10W Broadband GaN (CG2H40010) PA circuit.

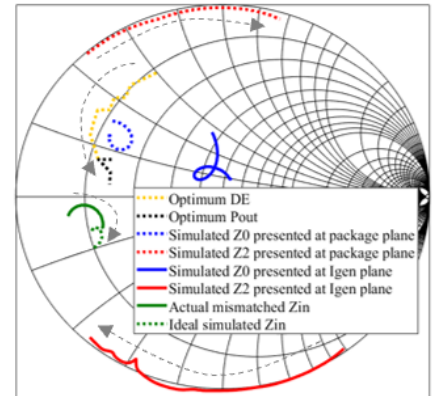


Fig. 7. Simulated impedances presented at the device across bandwidth.

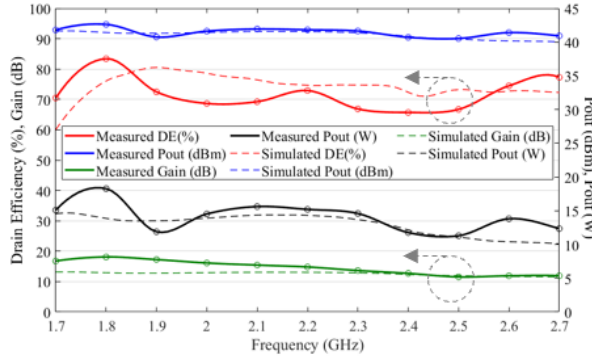


Fig. 8. Measured and simulated performances of 10W PA.

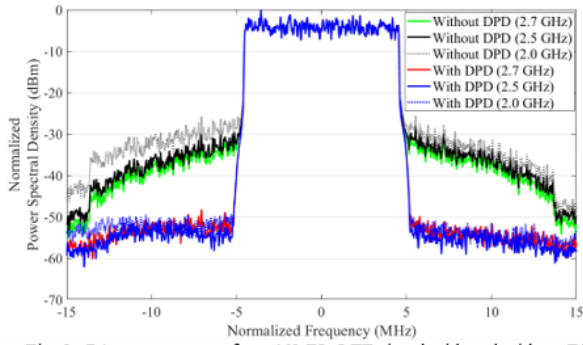


Fig. 9. PA output spectra from 10MHz LTE signal with and without DPD.

reduced between -52.2 dBc to -55.8 dBc after DPD for all 3 frequencies. The maximum Pout obtained is between 39.9 dBm to 41.2 dBm. The measured PAE at 2.7 GHz is 29%.

## VI. CONCLUSION

New theoretical analysis of the CCF mode, operated in the non-linear knee region of the transistor, was presented. Through waveform engineering, the ideal CCF mode output waveforms are reformulated by considering the device's I-V knee interaction. When the device is operated at gain compression, the drain efficiencies are no longer constant across the  $\alpha$  space; the peak efficiencies are reached for  $\alpha = -1/+1$ , due to the I-V knee effect. This new CCF behavior has been successfully modelled, simulated and measured in this paper for the first time. A broadband 10W PA has been realized by restricting the phase of 2<sup>nd</sup> harmonic rotation around  $\alpha = -1$  across bandwidth to keep the efficiency high. Up to 83.4% DE is measured from the PA with average of 71.7% while the output power ranges between 11.3W to 18.4W across bandwidth under CW measurements. The PAs designed in [8]-[11] shows prior arts of broadband design that has similar restricted 2<sup>nd</sup> harmonic phase rotation, however, there are no explanation to particular restriction. Similar design strategy has been implemented through optimization process rather than appropriate fundamental waveform theory. The gain compression for the PA in this paper is kept at 3dB maximum, whereas no information is available in all references in Table 1 regarding the gain compression of the PAs for their CW measurements. The linearity of this PA has been measured using 7.6 dB PAPR, 10 MHz LTE signal and the ACPR has been reduced between -52.2

Table 1. Comparison of the state-of-art PA.

Ref	Bandwidth (GHz)	Pout (W)	DE (%)	Gain (dB)	Gain Comp.	RFPA Class
7	0.55 - 1.1 (66.7%)	8.5 - 13.2	65-80	9.5 - 12	NA	CCF
8	1.45 - 2.45 (51.3%)	11 - 16.8	70-81	10 - 12.6	NA	CCF
9	1.6 - 2.7 (51%)	10.2 - 17.8	70.3-81.9	11.9 - 15.2	NA	CCF
10	1.3 - 2.4 (59.5%)	10.2 - 13.2	62.3-72	11.4 - 14.3	NA	Cont. Class - B/J
11	1.3 - 3.3 (86.9%)	10 - 11	60-83	10 - 13	NA	CCF/CCF <sup>-1</sup>
<b>This work</b>	<b>1.7 - 2.7 (45.5%)</b>	<b>11.3 - 18.4</b>	<b>65.7-83.4</b>	<b>11.5 - 18.1</b>	<b>3dB</b>	<b>CCF</b>

dBc to -55.8 dBc for carrier frequency of 2.0 GHz, 2.5 GHz and 2.7 GHz. The realized PA exhibits relatively high raw linearity of around -40dBc at 2.7 GHz. Therefore, the utilized DPD system was able to improve it only by about -14 dB to -54.6 dBc. For all these frequencies, the maximum Pout ranges between 39.9 dBm to 41.2 dBm.

## ACKNOWLEDGMENT

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