ADVANCED DOHERTY POWER AMPLIFIER DESIGN FOR MODERN COMMUNICATION SYSTEMS

Thesis submitted in fulfilment of the requirements for the degree of

Doctor of Philosophy

By

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September

2018

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ABSTRACT

Mobile communication technologies are becoming increasingly sophisticated and have experienced rapid evolution over the last few decades, and this is especially true for the base station transmitter. In response to the ever increasing demand in communication traffic and data throughput, largely driven by video based social media platforms, both spectral and power efficient device and systems are needed to fulfil the requirements. In terms of energy consumption, the power amplifier is an important component, and although developing efficient technologies for handset equipment is important, it is the base station element of the communications system that poses the greater challenge, having to deal with many channels simultaneously, resulting in the need to linearly and efficiently amplify highly dynamic phase and amplitude modulated signals possessing very large peak-to-average power ratios, at high power levels. This unique set of challenges has led to continuous research to improve the efficiency of amplifiers that can accommodate such signals, and the Doherty architecture has now become the architecture-of-choice.

However, most of the previous research studies demonstrate Doherty performance enhancement through a 'conventional' design approach that uses one input source and a passive power splitter to deliver power to each half of the Doherty structure. They do not emphasize the additional efficiency and other performance improvements that are possible in Doherty amplifiers when using two different, independent and phase coherent input sources, attached to the input path of both *main* and *auxiliary* amplifiers.

The novel research work presented in this thesis introduces an optimised design approach for Doherty amplifier architectures with individual input sources, as well as detailing a measurement architecture that is necessary to characterise such structures, using separate, phase-coherent input sources in a realistic measurement scenario. Finally, following extensive characterisation of a number of promising architectures, investigations around efficiency enhancement are focused around the adaption of gate bias applied to the *auxiliary* amplifier device, and identifying, for the first time, what is possible by generating different shaping functions that relate bias voltage to the magnitude of the input signal.

One completely new area of research and novelty introduced in this work for example shows how choosing the right shaping function can give improved linearity and importantly *linearisability* by producing a flat gain over dynamic range. Note that *linearisability* is important, and is defined here as the term used to describe the ease with which the non-linearities of a device or power amplifier can be corrected. It is often assumed in power amplifier design that efficiency and power are the most important parameters, and that modern digital pre-distortion (DPD) techniques can easily correct any non-linearity that may result. Industry is now finding that this is not the case however, and the type and nature of the non-linearity in terms to AM-AM and AM-PM distortion is very important in determining of the degree of linearization possible.

ACKNOWLEDGEMENTS

Alhamdulillah, to Almighty God for the wisdom, strength and blessings He gave.

First and foremost, it is a genuine pleasure to express my deep sense of gratitude to my supervisor, Dr. Jonathan Lees, Senior Lecturer, School of Engineering, Cardiff University for his continuous support, guidance and encouragement. His dedication and keen interest above all his overwhelming attitude to help his students had been solely and mainly responsible for completing my research study. I appreciate all his contributions of support, ideas and time, as well as his quick feedback and constructive comments were really inspiring and helpful.

I owe everything to my family who encouraged and helped me at every stage of my personal and academic life. My deepest appreciation belongs to my siblings for their patience and understanding. I dedicate this work to my sincere and generous father, Mr. Kamarudin Said, and my loving mother, Mrs. Wan Rokma Wan Ghani. I love you all.

Last but not least, I would like to express gratitude to all the members of Centre for High Frequency Engineering (CHFE), Cardiff University for their friendship, inspiration and fruitful discussions. To all my friends, thank you for your continuous support throughout my PhD journey.

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ABBREVIATIONS

ABD	Adaptive Bias Doherty
BST	Base station transceiver
CAD	Computer-Aided-Design
CD	Classical Doherty
CW	Constant Wave
DPA	Doherty power amplifier
DSO	Digital signal oscilloscope
DSP	Digital Signal Processing
ET	Envelope tracking
FET	Field-effect transistor
GaN	Gallium Nitride
IAD	Input Attenuation Doherty
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LMBA	Load Modulated Balanced Amplifier
LO	Local oscillator
MIMO	Multiple in multiple out
PA	Power Amplifier
PAE	Power added efficiency
PAPR	Peak-to-average power ratio
PEP	Peak Envelope Power
RF	Radio Frequency
SDD	Symbolically defined device
Tanh	hyperbolic tan
WiMAX	WorldWide Interoperability for Microwave Access

CHAPTER 1

INTRODUCTION

1.1 Background and Research Motivation

Over recent decades, modern communication systems have needed to develop rapidly with the dramatic increase of communication applications and users. The demand is data driven, mainly by the desire of younger generations to watch video and the growing number of other mobile subscribers that need faster network access for their business and personal purposes which consumes, and this has contributed to tremendous increase in data traffic. Exceeding the data quota limit means that we need to pay more, or internet speed will decrease.

Over $2 billion per year is spent powering a typical operator's mobile communications network, the majority of which due to the base station terminal (BST) element. According to figures from Vodafone [101], the BST demands 60% of total mobile network power consumption, while the core infrastructure consumes 15% followed by 20% from mobile switching equipment. In terms of efficiency, the IET has reported [101] that a typical 3G BST consumes 500W of RF input power in order to produce 40W of output power, and this poor efficiency is due mainly to the baseband stages. In the United Kingdom (UK) area for example, around 12,000 base stations required by a 3G mobile network, consume more than 50GW energy per year, so it is clear that poor efficiency translates to significant energy being wasted as heat, and is a major problem the industry needs to address.

Therefore, mobile operators have a desperate need to provide more efficient networks by investing in new technology such as 5G and rolling out increasing numbers of cellular base stations. The information rate that can be transmitted over a certain bandwidth plays an important role in ensuring spectrally efficient information transmission. 5G demands however bring new challenges because services and daily needs are done through the internet. Hence, the number of devices and connections across wireless networks will increase, and as a consequence there will be increased demand in the total amount of data and the need to handle many physical connections. Moreover, there is a subscriber expectation for higher capacity without paying more, thus the challenge here is to increase the data capacity of the network without increasing the operating cost. In addition, 5G imposes new requirements in terms of data latency, of high data rate and real-time interaction to allow critical services to respond faster, such as in medical monitoring and rescue [1]–[3].

For the radio frequency power amplifier (RFPA), this will mean significantly increased instantaneous bandwidths and much wider ranges of frequency used. More throughput will require more data capacity, wider bandwidths and higher peak-to-average power ratios (PAPR), but will come at the cost of reduced average efficiency.

1.1.1 Radio Frequency Power Amplifier in Communications System

Generally, the RFPA is a type of electronic amplifier that has an ability to amplify the low-power RF signal into a higher power signal suitable for transmission. A common problem with the RFPA is the inability to maintain the high

power efficiency over wide frequency bandwidths. There is also trade-off between power efficiency and linearity. Various research works have looked at overcoming this problem, which is further reported in Chapter 2.

The different classes of power amplifier are generally categorized in terms of their electrical characteristics, circuit configuration and method of operation. The conduction angle for example represents the fraction of a wavelength of a sinusoidal excitation that causes a device to conduct, over one cycle of operation. RFPAs can be further classified based on the selection of the bias point. The bias point, along with the drive level determines the conduction angle, where the RF cycle is active.

1.1.2 Class-A Power Amplifier

Generically, and most simply, conventional PA classes are classically divided into Class-A, -B, -AB and -C. In a Class-A power amplifier, the transistor is biased at a point in the output characteristic that causes output current to flow for the full-cycle of input signal. In other words, the transistor is biased at the centre of the most linear region of the transfer characteristic, resulting in a conduction angle of 360^{o} and high overall linearity. Apart from that, the class-A amplifier can only achieve a maximum ideal efficiency of 50% at peak envelope power (PEP). Other properties of class-A are a constant DC current and voltage and hence constant DC power, as well as a high gain. Therefore, this type of amplifier is typically used in high linearity and high gain operation applications.

1.1.3 Class-B Power Amplifier

A class-B amplification is characterised by a transistor biased such that only half of the input cycle causes output conduction, hence the conduction angle reaches 180°. This results in a reduced power gain (3dB) and an ideal drain efficiency of class-B is (higher than class-A) of 78.5% at peak envelope power (PEP). Interestingly, the *ideal* class-B amplifier is linear as there is theoretically no change in conduction angle with applied drive level. In reality however, class-B is less linear than class-A due to the typical soft turn-on behaviour of a device, resulting in a distorted voltage waveform and what is traditionally known as cross-over distortion. In this mode, there is therefore a need to minimise harmonic distortion in order to improve the linearity performance to acceptable levels.

1.1.4 Class-AB Power Amplifier

When the transistor is biased between class-A and class-B, the resulting amplifier is known as a class-AB amplifier, where the conduction angle is in a range between 180° and 360°, and where the ideal achievable efficiency is between 50% and 78.5%. The class-AB amplifier relies on a small quiescent current flow (typically 10-20% I_{DSS} for a FET device) to bias the transistor just above the device's pinch-off voltage, resulting in a conduction angle slightly more than the 180 degrees of class-B, but less than the 360 degrees of class-A. Class-AB is often the mode of choice in commercial power amplifier design as it offers the highest fundamental current of any of the classical modes, and as a result, a good compromise between power, linearity and efficiency.

1.1.5 Class-C Power Amplifier

It is important to note that class-C amplification results when the operating bias point of a transistor is reduced to levels that cause conduction angles of less than 180^{o} to exist. This can lead high drain efficiency operation up to 90% but with poor gain and linearity as the output signal introduces severe distortion. Class-A, -B and -AB amplifiers are generally considered as linear amplifiers as the output and input signals show a relatively linear relationship.

Table 1 below shows a summary of conventional amplifiers classes operating characteristics, referring to the loadline plotted in Figure 1.1.

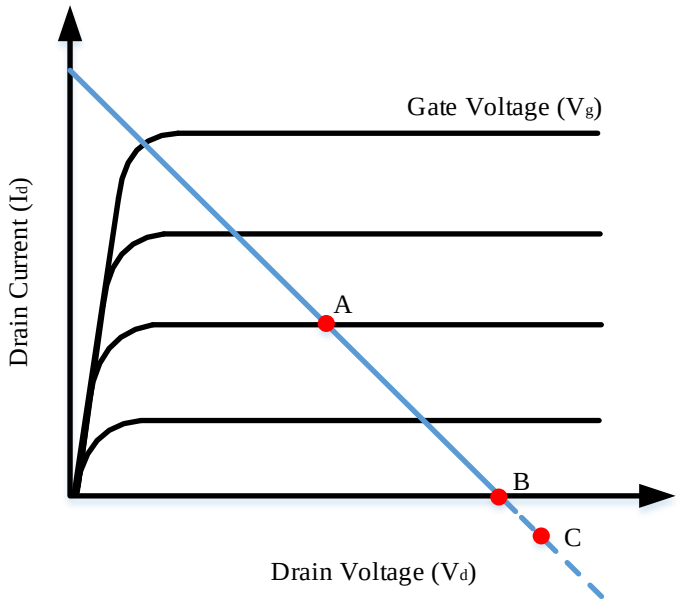


Figure 1.1: DC-IV and loadline graph showing conventional amplifier classes and their bias operating points

Table 1: Characteristic of conventional amplifier classes, note that "θ" represents the conduction angle.

	Class-A	**Class-AB**	**Class-B**	**Class-C**
Q Position	In the centre of IV plane / transfer characteristic	Between the centre of the IV plane and I_d=0	I_d=0	I_d=0
Conduction Angle, θ (rads)	2π	$\pi < \theta < 2\pi$	π	$\theta < \pi$
Ideal drain efficiency (%)	Up to 50	50 - 78.5	Up to 78.5	78.5 - 100

As telecommunication systems continue to evolve, many applications demand high-efficiency devices and circuits; for battery longevity in mobile handsets, reduced power consumption in base station equipment, reducing heat generation and allowing base station amplifiers to be mounted at the top of masts (passive cooling) that in turn reduces costs of feeder cables, leading to a general need for high-efficiency power amplifiers. However, conventional reduced conduction mode classes of amplifier, although offering relatively high efficiency, are not suitable for all applications. In all cases, one key parameter must be sacrificed to maximise another; for example, a class-A amplifier sacrifices efficiency for linearity while class-C amplifier sacrifices linearity and gain for efficiency.

In response to the introduction of early 2G communications systems, where the modulation used resulted in a continuous wave (CW) modulation envelope, a

range of amplifier classes/modes were developed. These are based on fundamental classes, but use harmonic impedance termination and switching techniques to achieve very-high efficiency without the usual sacrifices being made. These classes are generally known as harmonically tuned amplifiers and include class-D, -E, -F and inverse class-F amplifiers.

1.1.6 Class-D Amplifier

Class-D amplifiers are typically used in audio applications because of the efficiency benefit they bring, in comparison to conventional linear amplifiers, but has found some use in RF applications [4], [5]. Class-D has the capability to overcome the problem of power wastage and thermal dissipation through the use of switching mechanisms. The transistor itself acts as a switch that turns on and off alternately, minimising the voltage and current overlap. In the voltage mode configuration shown in Figure 1.2, the series L and C resonates at the operational frequency and tune the output amplifier to produce sinusoidal output current waveform. The main difference between a linear amplifier based on a conventional classes and for example a Class-D amplifier are the achievable efficiency and the high power that can be produced. The class-D amplifier acts as a switch to *steer* the output current through a load, resulting in minimal dissipated power lost within the output of the device. The efficiency of class-D amplifier can be improved up to 90%-95% in practical designs [6].

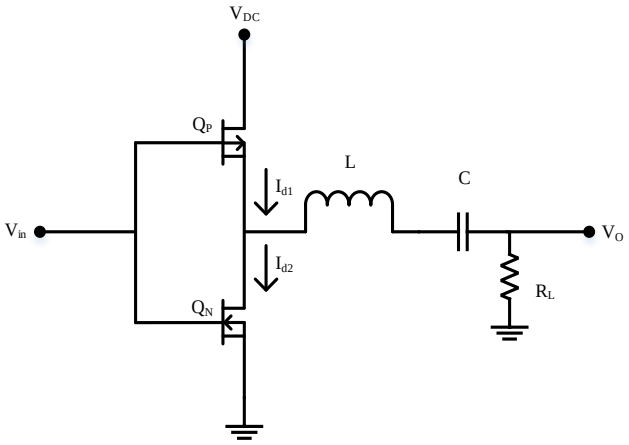


Figure 1.2: Class-D amplifier circuit [7]

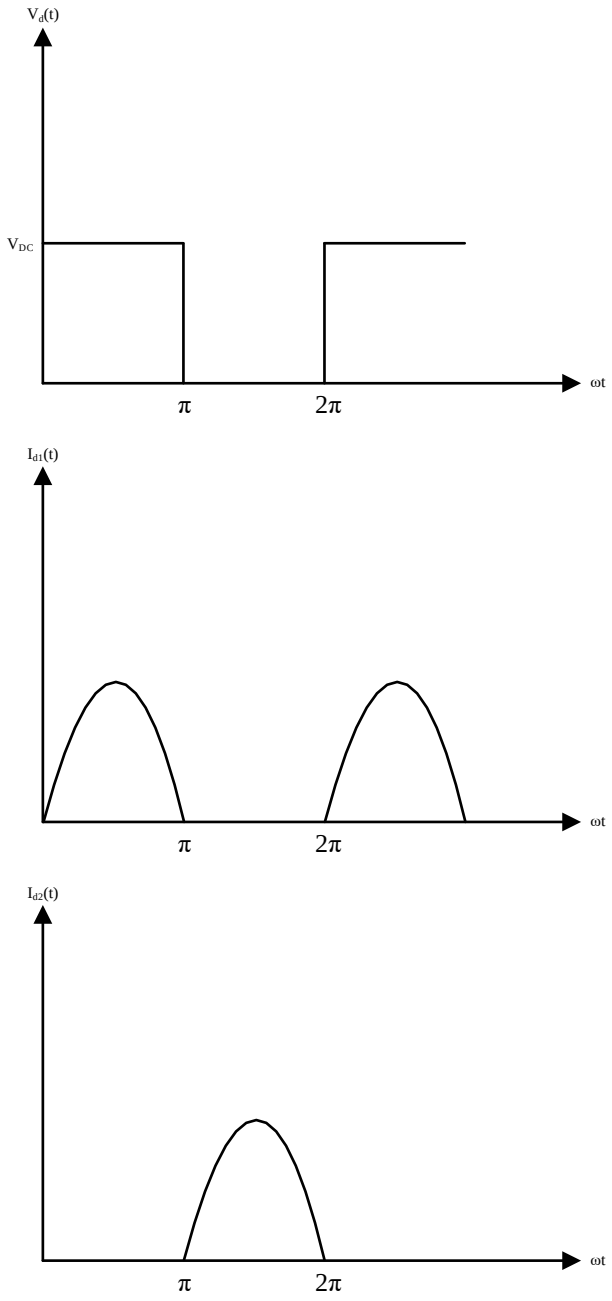


Figure 1.3: Voltage and current waveform of class-D amplifier shown in Figure 1.2.

1.1.7 Class-E Amplifier

Due to component parasitic effects from mainly inductors and capacitors, it is challenging to realise class-D at microwave frequencies. Hence, Class-E amplifiers have been developed, that are based on the same, basic idea, and that make use of the parasitic components in the output harmonic tuning network. When the transistor switch is on, the voltage across the switch is zero, and when the switch is off, the current through switch is zero. Hence, the high Q resonator circuit and lumped components produce a sinusoidal output signal at the output of the amplifier [7]–[9]. The ideal 'toggled' waveforms are shown in Figure 1.5 achieve a result of 100% efficiency due to non-overlapping on and off current changes.

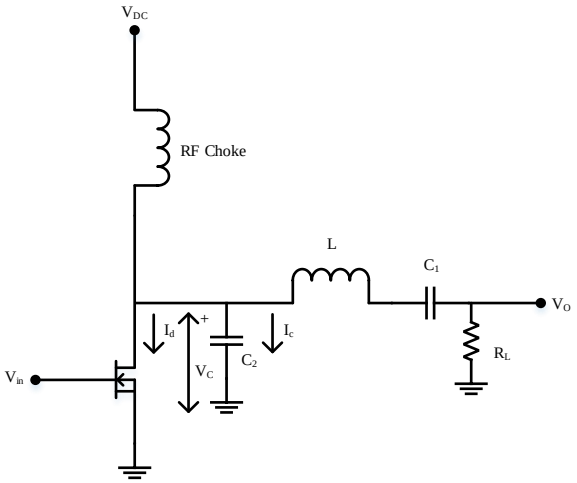


Figure 1.4: Class-E amplifier circuit [7]

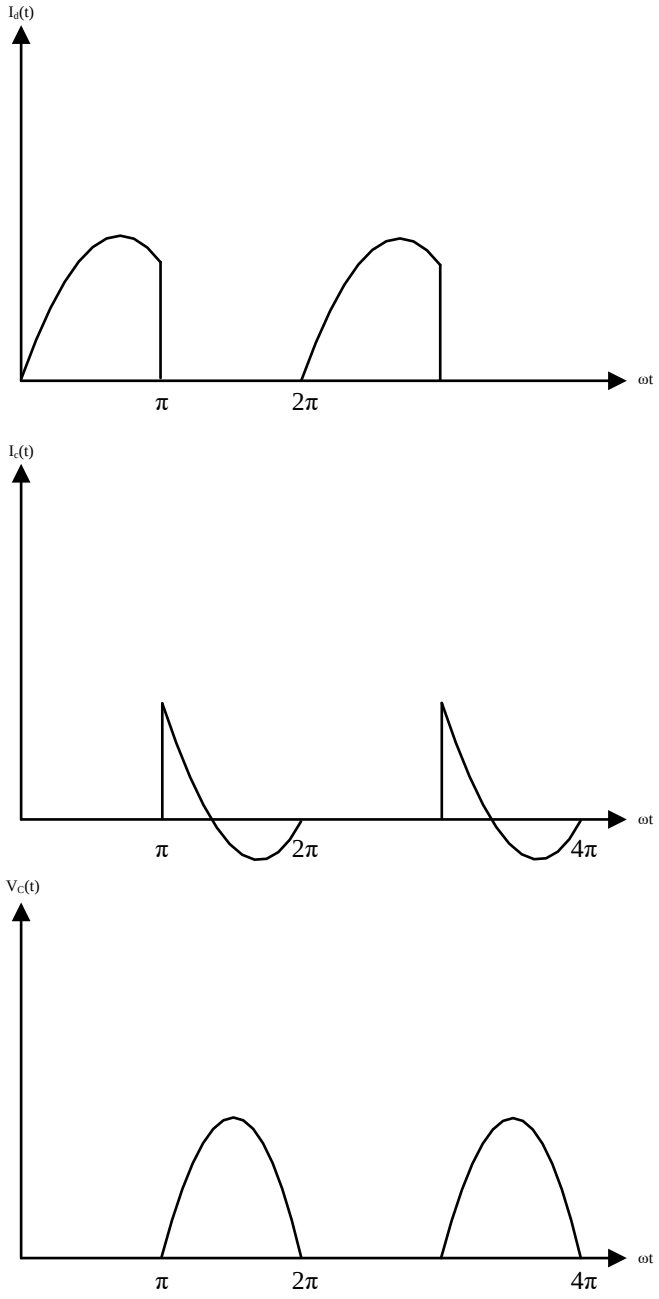


Figure 1.5: Voltage and current waveform of Class-E amplifier

1.1.8 Class-F Amplifier

The class-F amplifier is another amplifier structure that, assuming an infinite number of harmonics to form a square and half-wave sinusoid waveform shapes for voltage and current respectively at the device output [10], can ideally achieve an efficiency of 100%. Generically, this mode achieves high efficiency and high power by adding a harmonic resonator at the output to shape the voltage waveform in the time-domain. This type of amplifier is still capable of achieving high-efficiency with limited or truncated harmonic control, as reported in [11], and typically increases in efficiency of 10% or more compared to class-B and deep class-AB operation are possible. Achieving the inverse-wave shaping relationship (between current and voltage) is known as inverse class-F amplifier and can achieve similar performance improvement. Table 2 below presents the difference between class-F and inverse class-F power amplifiers.

Table 2: Comparison of class-F and inverse class-F amplifier

Class-F	**Inverse Class-F**
Based on Class-B bias.	Based on Class-A bias.
Shorted at even harmonics and open at odd harmonics. Result is an output voltage waveform approximating a square wave.	Shorted at odd harmonics and open at even harmonics. Result is an output voltage waveform approximating a half-rectified wave.
Output current waveform consists of even harmonic and forming half-rectified sine wave.	Output current waveform consists of odd harmonic and forming square waveform.
Only first three harmonics are, while higher harmonics are usually shorted or not considered.	Only considered first three harmonics at both input and output network.

The inverted class-F amplifier is sometimes preferred over class-F if the frequency response of the device is limited. For example, making a class-F using LDMOS is difficult as the output capacitance of the device physically prevents 3rd harmonic exiting the device, whereas 2nd harmonic is available for termination. As inverse class-F involves opening the second and shorting the 3rd, it is more suitable for this type of device. Due to the presence of second harmonic voltage components, the inverse class-F RFPA will generate a higher peak output voltage waveform than class-F. This can cause breakdown problems, for example in silicon devices.

1.1.9 Continuous Mode Amplifier

Continuous mode amplifiers offer a way to achieve high efficiency while operating over potentially very wide bandwidths. Generally, continuous modes provide a mathematical framework [12] to extend the fundamental and harmonic impedance space of conventional PA modes to significantly increase bandwidth over which the power and efficiency can be enhanced. Likewise, we can say that performance is affected by the harmonic manipulation. For example class B/J continuous mode operation is based on a conventional class-B (or 'deep' class-AB) bias, and thus demonstrates similar drain current waveforms to class-B, operating at the same conduction angle. The requirement of a reactive termination of the fundamental load differentiates class-B/J with other amplifier modes. However, class-B/J does not require harmonic resonator circuit to achieve maximum efficiency, giving advantage to obtain high efficiency over wide bandwidth compared to other conventional linear PA. The class-F approach can only fulfil the impedance

requirement over a narrow bandwidth, while the class-B/J continuous mode could cover a much wider bandwidth, as reported in [13]. Moreover, class-B/J power amplifiers have shown that it is possible to achieve high efficiency in a wider bandwidth when controlling just the first two harmonic impedances, as stated in [14].

1.2 Simulator Tools for Simulation

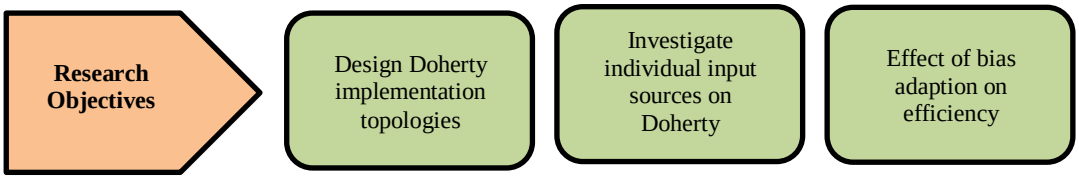
In this work, a number of simulation tools are utilized to carry out the simulation process easily. One of these is Harmonic Balance (HB) simulator, which is a frequency domain approach for simulating analogue RF and microwave problems, especially the distortion in nonlinear circuits and systems. It obtains frequency-domain steady-state spectral content of voltages or current in the circuit. This simulator is also used to perform power amplifier load-pull contour analysis. Other than that, Parameter Sweep and Sweep Plans are used for automatically combining sweeps of several parameters into a hierarchical sweep plan, such as finding the bias voltage that yields the best efficiency.

The input and output matching network as mentioned in Chapter 6 are built using the Smith Chart Tool provided in ADS. At the higher circuit levels, where we need to simulate the circuit in a real environment, Microstrip Substrate (MSUB) plays an important role here to claim all the substrate's parameters, such as substrate thickness, relative dielectric constant, conductor thickness and dielectric loss tangent.

1.3 Aim and Objectives

The aims of this research are to compare the performance in terms of output power, efficiency and linearity of three Doherty power amplifier implementations: Classical Doherty (CD), input attenuation (IAD) and adaptive bias Doherty (ABD). The research focuses on an adaptive bias approach. In order to achieve these aims, three main objectives are set as follows.

- To design and simulate firstly ideal and then realistic versions of all three Doherty implementations in Keysight's Advanced Design System (ADS) environment at an operational frequency of 2GHz. The first design prototype is a Classical Doherty, as this acts as a reference for other design prototypes, allowing meaningful comparison.
- To measure the actual performance of a fabricated Doherty implementation in a bespoke measurement system, critically using two independent but phase coherent input sources, and to optimise this where possible.
- To investigate the effects of the bias adaption approach on the efficiency in Doherty designs.



1.4 Thesis Organization

This thesis is structured into seven chapters, summarized as follows.

Chapter 2 presents a literature review to identify the related works to this PhD research. This chapter begins with an overview of efficient communication system applications. A number of key efficiency enhancing architectures relevant to the research are also discussed. The chapter then goes into further detail of the Doherty architecture, which is the focus of this work. The Doherty literature covers fundamental circuit behaviour, the concept of load modulation and various Doherty implementations.

Chapter 3 provides a detailed discussion around developing ideal design prototypes through simulation in the Advanced Design System (ADS) environment. This chapter is concerned with the development of relatively ideal simulations with the aim of firstly establishing ideal Doherty behaviour in all three implementations. A simple, parasitic-free transistor model is developed using simple trigonometrical equations to represent the trans-conductive and knee-region behaviour of a typical RF device. Later in the chapter, this ideal model is replaced with a realistic non-linear model for a 10W gallium nitride (GaN) device from CREE (now Wolfspeed). Both models are validated to ensure they achieve the acceptable and expected performance the reference case. The chapter then covers the simulation activities of other Doherty PA implementations; the classical Doherty, input attenuation and adaptive bias.

Chapter 4 is devoted to discussing the measurement system that needed to be developed for this research, and that was used to verify the simulation activities of

the Doherty PA implementations. Instead of presenting a traditional, single source approach, this chapter presents three different measurement configurations that critically support independent excitation of *main* and *auxiliary* devices in the Doherty structure. The Doherty is typically characterised as an RF-in RF-out structure with a fixed input phase and magnitude relationship, fixed by an input structure such as a hybrid 90-degree coupler. For the work presented in this thesis, it was a key to achieve independent excitation capability to allow investigation of optimal phase and magnitude relationships between the two devices within the Doherty structure, as well as implement new and interesting implementations, including the input attenuation approach. This involves using different types and configurations of signal generators as input sources. All the setups are shown in block diagram for easier visualization.

Chapter 5 describes the first prototype of a 'generic' Doherty PA design using real device, and includes simulation, fabrication and measurement. The Doherty is a complex structure to design and optimise, yet is typically designed using a 'traditional' PA design methodology, leading to non-optimal results. To investigate the limitations in this design approach, it was decided to start with an initial, 'kick-start' design to provide a vehicle for initial measurement and characterisation. As a result, imperfect performance was expected, with value of this prototype more in allowing observation of defects and non-ideal behaviour that could be noted and used as a learning process to produce an optimised Doherty design later in the research project.

Chapter 6 presents a continuation of activities from the previous chapter with a focus on optimisation of the initial prototype. This chapter specifically discusses and

considers parasitic component effects in a high frequency device in the simulation environment. An optimised design flow needed for correct Doherty design is introduced and discussed further is this chapter, starting from load-pull simulation at the device's intrinsic current generator plane, before moving to the *main* device and then the *auxiliary* device individually. Importantly, this chapter then considers the novel ideas around how the relative input phase between *main* and *auxiliary* devices can affect the overall performance, and how optimisation of gate bias and input attenuation profiles affect the overall Doherty PA performance. This chapter further explores the possibilities presented by the bias adaption technique and specifically, how specific shaping functions that relate input envelope magnitude to the gate bias applied to both *main* and *auxiliary* transistors can be used to obtain improved '*linearisability*' of the Doherty structure.

Chapter 7 is the final chapter, which concludes all the research work and contributions, and highlight the works that can be taken in future.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

The power amplifier is a critical element in any modern wireless communication system. The general challenge has been the same for many years - to minimise the DC energy consumed relative to the RF or microwave energy transmitted. Although this goal appears straight forward, the research challenge, in the context of future communications systems needed for example to enable 5G remains considerable. This is because high performance and efficiency is required whist operating over ever-increasing frequency bandwidths, ever-increasing dynamic range or peak-to-average power ratio (PAPR), at increasing operating frequency ranges (including multi-carrier operation), whilst remaining relatively linear, or at least 'linearisable'[1] and at the same time minimising cost.

As a result, the volume of international PA related research work continues to be significant and has even increased relative to other, traditional microwave areas. It should be remembered that even small increases in efficiency can lead to significant

[1] 'Linearisable' achieving *DPD-friendly* distortion characteristics, with the assumption that a DPD system will always be required in a modern communications system, good *linearisability* will lead to reduced complexity (and hence cost) DPD solutions.

improvements in terms of battery longevity and size in handsets and operational (OPEX) related costs for base stations [15]–[17].

In this chapter, an overview of research around Doherty PA architectures is presented. Firstly, a review of the efficiency enhancement methods in power amplifier design is presented, focusing on the architectures of Chireix outphasing, envelope tracking (ET) and the Doherty amplifier. The study then narrows to focus on the concept of the Doherty amplifier, including its behaviour and load modulation technique applied to this structure. Following this, specific focus is given to the three main Doherty implementations; Classical Doherty, input attenuation and bias adaption. Research relating to bias adaption over efficiency is revised in detail as it is the main focus of this thesis. Finally, the chapter is concluded with a summary of efficiency enhancement with different methods of implementations.

2.2 Efficiency Enhancement Method in Power Amplifier Design

According to the constraints identified in section 2.1, ongoing research has focussed on conceiving and developing relevant techniques that can efficiently convert DC power into RF power at both device level, and architectural level [18]. Generally, in conventional RF PA design, peak efficiency is possible only at maximum output power. As discussed in Chapter 1, for a single ended PA structure, efficiency then drops rapidly as the power is backed-off from the point of maximum output power or peak envelope power (PEP). Hence, a number of architectures have

been identified and utilised to overcome the problem of degraded efficiency with power back-off that involve the use of multiple, interacting devices.

2.2.1 Chireix Outphasing

This architecture was first invented by Henri Chireix in 1935, and was an advanced technique to improve the power efficiency of very high power amplitude modulation (AM) broadcast transmitters [19]. The basic concept of this technique is widely publicised and has been revised to form other techniques, such as Linear amplification using Nonlinear Components (LINC) proposed by D. C. Cox in 1974 for linear amplifier design purposes [20]. In a Chireix configuration, active transistors are exposed to one another through a simple reactance compensating network, and effectively load-pull one another in a collaborative way. Note that unlike Chireix, LINC relies upon a high level of isolation between the two active devices, and as a result, provides no efficiency enhancement.

The Chireix outphasing technique basically combines, using two nonlinear RF PAs, constant wave (CW) signals with different phases. The relative phase of the two CW signals is precisely controlled and through a constructive / destructive interference process, combine at the output to form the required AM modulated envelope. The result is high efficiency and high linearity ‘transmitter’ that utilises constant modulation envelopes [21]–[25]. An outphasing RF signal splitter for a single input Chireix has been developed in [26], which used a linear circuit to exploit the input impedance variation to modify input signal phase. This splitter approach achieved 52.6 dBm peak output power and remained 50% drain efficiency at 5.7 dB

output power back off (PBO) at 2.17GHz. Other work [27] shows that an analog signal component separator (SCS) can be used to control the outphasing angle and amplitude between two signals, resulting in 73% of peak drain efficiency reducing to 60% at 7 dB back off power, with 43 dBm peak output power at 2.11GHz.

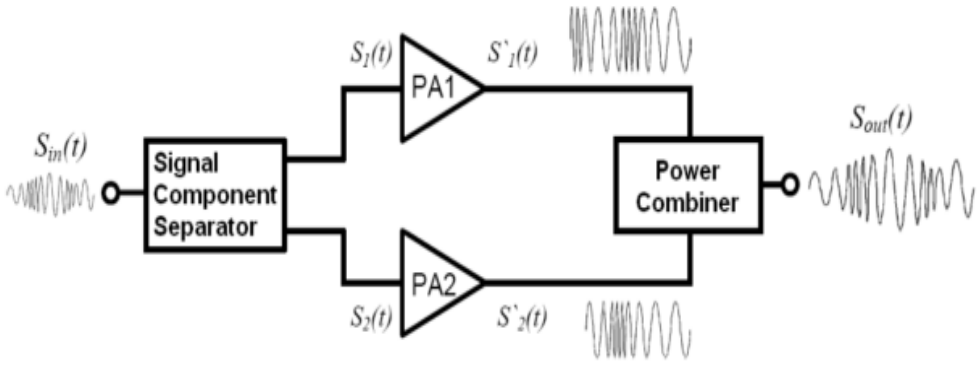


Figure 2.1: Simplified block diagram of the Chireix outphasing architecture [28].

The main limitations of Chireix outphasing include the fact that the two, precisely phased CW input signals need to be synthesised, as well as the fact that it is difficult to optimally combine the two outphased signals once they have been generated. In addition, power can be wasted in the output combiner. In other work [29], a technique is demonstrated where unused out-of-phase signal components are recovered to the power supply, resulting in 63% of overall efficiency at 1.96 GHz.

2.2.2 Envelope Tracking

The envelope tracking (ET) power amplifier is another multiple-device architecture used for efficiency enhancement, involving DC power supply modulation in response to the input envelope magnitude, ensuring the RF device can operate at high efficiency when RF power is backed-off [30]–[33]. A conventional PA relies on a fixed DC power supply and achieves peak efficiency only at peak envelope power, whereas an ET architecture, due to the modulated DC supply, can maintain high-efficiency throughout the PBO region. Hence, the supply voltage can be limited to that is needed to provide the required output power and hence high efficiency can be achieved at all instantaneous power levels.

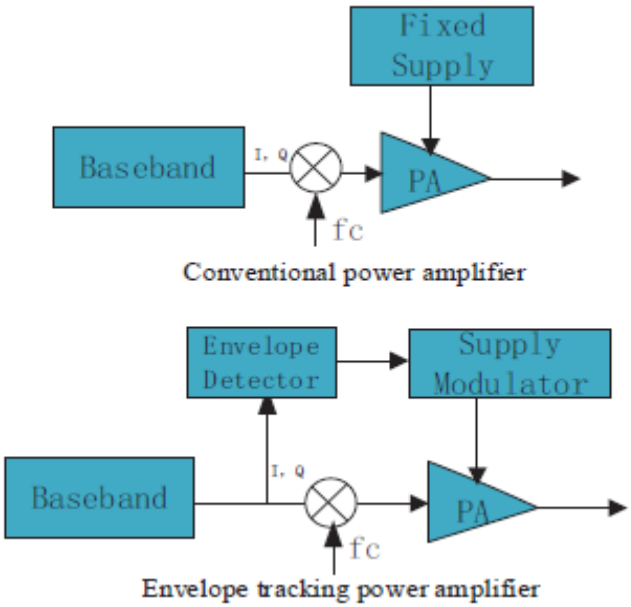


Figure 2.2: Block diagrams of conventional PA and envelope tracking PA [34].

One of the important techniques related to the ET architecture is the use of 'shaping functions' in the closed loop ET path [34]–[38] necessary to relate the dynamic tracking voltage to the instantaneous magnitude of the modulation envelope. Shaping functions take into consideration the transistors limiting DC characteristics and dynamic load presented by the PA to the supply modulator when applying the required voltage. Optimising shaping functions can be especially important in achieving best performance, for example in for LTE application. One of the most critical elements of any PA design is the trade-off between efficiency and linearity. An analytical study has revealed a conceptual theory to balance these two parameter using ET architectures [33].

One significant disadvantage of ET is that it requires very fast and wide bandwidth DC power supply to modulate the required voltage. In addition, this architecture also requires very accurate timing alignment between the modulation envelope and the dynamic ET supply to avoid catastrophic performance degradation during operation.

2.2.3 The Doherty Amplifier

The Doherty PA is a high-efficiency, multiple-device architecture, which is now commonplace in mobile telecommunications infrastructure base station transceiver (BST) equipment. It was first invented by W. H Doherty at the Bell Telephone Laboratories Inc. in 1936 to improve the low efficiency associated with very high power (MW) broadcasting transmitters using vacuum tubes [41]. The main idea at the core of the Doherty PA architecture is using two interacting devices to

maintain a near saturation level and hence a high-efficiency state in one of the devices. When comparing the combined efficiency of both devices, a significant improvement is observed in average efficiency over dynamic range, over an equivalent periphery balanced amplifier (here used as a reference). This 'active load-modulation' concept allows this elegant RF-in – RF-out structure to achieve high efficiency over power back off ranges in the region of 6dB for classical and typically 10 dB for extended dynamic range Doherty amplifiers [42], [43].

The classical Doherty PA structure comprises two symmetrical active devices, typically known as *main* and *auxiliary* devices respectively, connected at their outputs using a $\lambda/4$ transmission line, which acts as an impedance inverter. A complete configuration of this architecture is illustrated in Figure 2.3. The *main* device is usually biased in class-AB, while the *auxiliary* device is biased in some degree of class-C. The phase difference between two input signals is theoretically 90 degrees, however this value varies according to device characteristics, for example, drive dependent S_{11}, and the types of transmission lines used. The conventional Doherty configuration includes a delay line at the input to balance the phase delay introduced by an impedance inverter at the output. The power developed by both devices sums in phase in the load. The Doherty's operation will be discussed in detail in subsection 2.3.

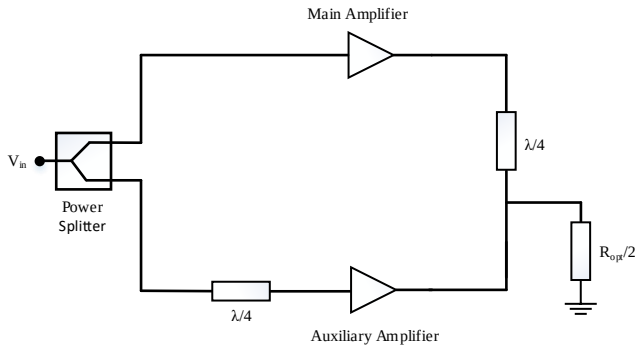


Figure 2.3: Configuration of Doherty PA architecture, which consists of *main* and *auxiliary* devices connected in parallel with an output impedance transformer.

This architecture is widely used in modern communication systems, generally due to its capability of maintaining high efficiency at average and peak power levels, as well as its suitability for signals with high peak-to-average power ratio (PAPR). Another attraction is it is a simple RF-in RF-out architecture when compared to other high-efficiency architectures, especially ET, and this advantage cannot be overstated due to the cost implications for network providers when developing high-efficiency systems.

In terms of wideband applications, Doherty architectures are limited and cannot accommodate wide bandwidths (>20%) due to the limitation imposed by the quarter wavelength impedance transformer. Because of the popularity of the architecture, there is significant ongoing research to develop Doherty architectures that can achieve high efficiency over extended bandwidth [44]–[48], although this remains a challenge. By minimizing the necessary impedance transformation over dynamic range ratio to extend the bandwidth, implementations have been

demonstrated that run between 1.8 GHz and 2.3 GHz and that can maintain efficiency above 50% and 60% at 26 and 34 dBm respectively [49]. At mm-wave, 35% efficiency has been achieved at 21 dBm over a 7 GHz bandwidth (22-29 GHz) [50], using GaAs PHEMT transistor technology.

In a multistage Doherty amplifier, it is possible to have multiple points of peak efficiency because of the multiple different bias points being used for different amplifiers. This technique gives another advantage of Doherty architecture to perform with high efficiency over extended dynamic range. In [51], a 3-stage Doherty amplifier was designed to maintain 47% of efficiency at 46 dBm output power in the range of 9 dB power back off. Other research works using three stages DPA [52] show that dynamic range can be extended up to 12 dB back-off power with 50%–61.8% and 51.9%–66.2% at 6 dB back-off. More research studies have used this approach for extending the range of back-off power [53]–[55].

Choosing an inherently high-efficient and high-power device also helps the architecture to achieve good overall performance. The Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor technology continues to dominate the RF amplifier semiconductor due to its relatively low cost, and has been the device technology of choice for network providers since it was first introduced a few decades ago. Its continued domination is largely due to various and continued generational design innovations which maintain its relevance for current and emerging communication systems. Although LDMOS will continue to be used extensively, it is a fact that its maximum frequency of operation is fundamentally limited to typically 3.5 GHz, and this will prove a limitation in addressing for example, certain 5G frequency bands in the future.

Gallium Nitride High Electron Mobility Transistor (GaN-HEMT) devices have been chosen in this research for several reasons: Firstly, this technology allows for high-power and potentially higher efficiency operation compared to LDMOS. In [47] and [48], it has been shown for example that more than 60% drain efficiency can be achieved using GaN device in amplifier designs. Secondly, GaN technology has a much higher breakdown voltage than that of LDMOS, allowing more adventurous, harmonically tuned designs to be considered if necessary, as well as potentially improved reliability. It is also reported that the device technology has high comparative linearity [58]. Thirdly, the comparatively smaller intrinsic output capacitance of GaN allows for an extended operational frequency range. It therefore presents itself as a likely technology for future 5G communications systems bands that will be out of the range of current LDMOS technologies. The added, and less obvious benefit of smaller output capacitance and extended frequency operation is that the PA designer has access to harmonic current components at the extrinsic device plane that allows the possibility of high-efficiency modes to be engineered through *waveform engineering* [59]–[62] techniques.

2.3 Basic Concept of Doherty PA

2.3.1 Doherty Behaviour

To understand how Doherty architecture achieves efficiency enhancement, it is important to understand, at a circuit level, how it works and the important factors involved, as mentioned in [18], [63]–[65]. Although there are many variations of

Doherty operation, with reference to Figure 2.3 above, so called Classical Doherty behaviour is explained with the assumption that input power is split equally and delivered to *main* and *auxiliary* devices. In terms of normalised dynamic range, the range of input drive level can be divided into two regions; a low-power region (V_{in}<0.5) and a high-power region (V_{in}>0.5). In the low-power region, only the *main* device is active, while *auxiliary* device is biased off, and completely inactive. As the output current of *main* device increases, the output current of *auxiliary* device remains as zero. The *auxiliary* device ideally presents itself as an open circuit, and the load presented to the *main* device is therefore $2R_{opt}$, due to the impedance transforming property of the 90 degree line as shown in equation (1).

$$ZI^2 = Z1 * Z2 \quad (1)$$

The Smith chart in Figure 2.4 below represents the load modulation activity as seen by the *main* device during 'normal' Doherty behaviour. Again, with reference to Figure 2.3, and assuming a value of R_{opt}=50Ω (where R_{opt} is the optimum load for the device that causes maximum power) and a load resistance of R_L=R_{opt} /2. Carefully setting the characteristic impedance of the output λ/4 wave line such that Z_T= R_{opt}=50Ω, causes the load of R_{opt}/2 to be transformed to a impedance of $2R_{opt}$=100 Ω that is then presented to the *main* device.

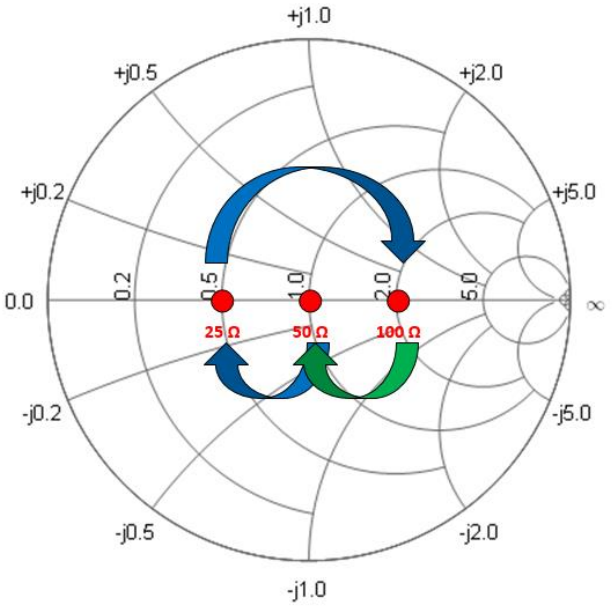


Figure 2.4: Load modulation transformation when only *main* device is active.

In this simple scenario, the load has been 'modulated', and transformed from $R_{opt}/2$ to $2R_{opt}$ and presented to the *main* device. Remembering that the *auxiliary* device is inactive in the low power region, as the input drive level is increased, the *main* device's fundamental output voltage magnitude will increase linearly, until it reaches saturation (and maximum efficiency), at an input drive level that will be referred to as the transition point (V_T). It is important to note that, up to this point, although inactive, the voltage at the output of the *auxiliary* device also increases linearly. From Figure 2.5 and Figure 2.6 below we can see that the voltage and current behaviour up to the transition point is also linear.

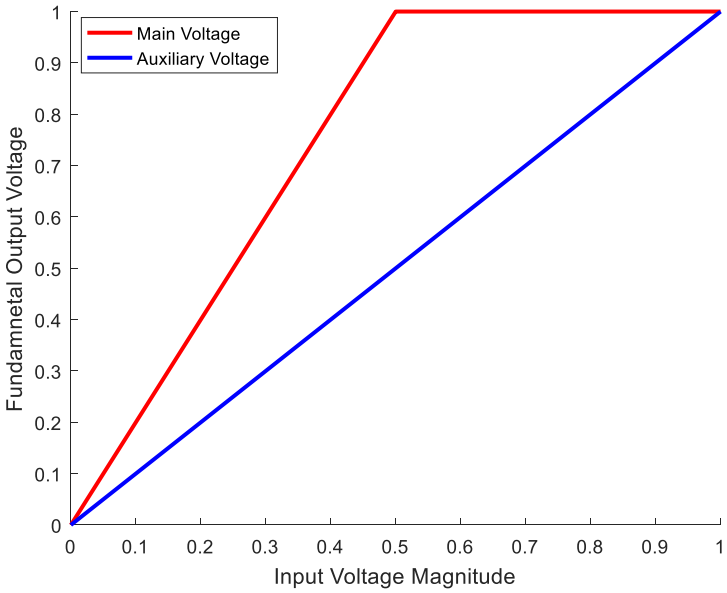


Figure 2.5: Fundamental normalised output voltage magnitude for *main* and *auxiliary* devices over normalised input voltage.

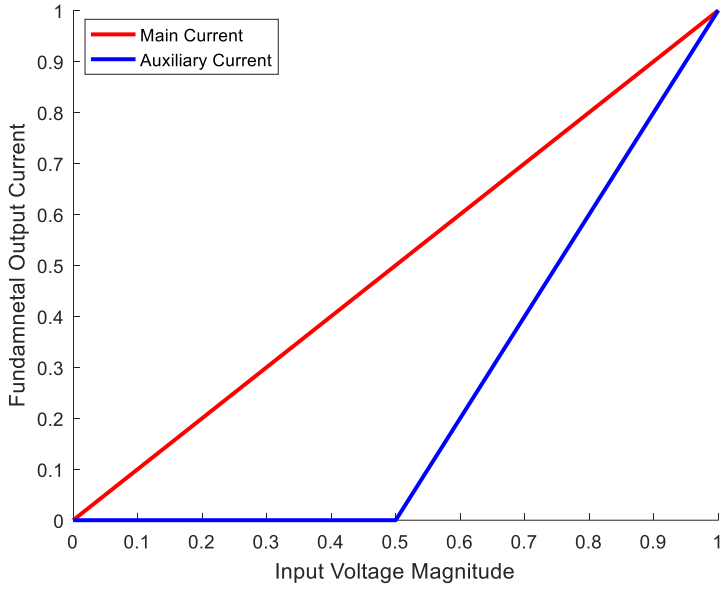


Figure 2.6: Fundamental normalised current magnitude for *main* and *auxiliary* devices over normalised input voltage.

At the transition (V_T) point, where the input voltage magnitude=0.5 normalised, the *auxiliary* device starts to become active and begins to supply current to the load.

At the transition point (V_{in}=0.5), *main* device has already reached its saturation level, and now must be maintained there in order to prevent distortion. In the high power region (V_{in}>0.5), the input drive keeps increasing above transition point, and the *auxiliary* device now generates current. The rate of current increase generated by the *auxiliary* device needs to be higher than that of the *main* device as it needs to achieve a maximum current at PEP, and this is usually achieved through an asymmetrical split at the input of the structure. The combined current contribution from both devices flowing into the load causes the load impedance seen from the *auxiliary* device to increase from $R_{opt}/2$ towards R_{opt}, and from the perspective of the *main* device, $2R_{opt}$ towards R_{opt}.

The Smith chart in Figure 2.7 below represents the load modulation activities for *auxiliary* device when the drive has increased from V_{in}=0.5 to V_{in}=1. At the transition point, the load presented to the *auxiliary* device is infinite as voltage exists without any current contribution. At PEP, the additional current contribution from the *main* device flowing in the load ($I_m+I_p=I_{out}$) causes the load resistance of $R_{opt}/2$ to be modulated to a new value of $R_L=R_{opt}$ **Ω**. Similarly, for the *main* device, the modified load of R_{opt} is transformed through the output λ/4 wave line of $Z_T=R_{opt}$ and appears as R_{opt} at the *main* device. This corresponds to the second peak of efficiency at PEP and a plateau of efficiency between the transition point and PEP.

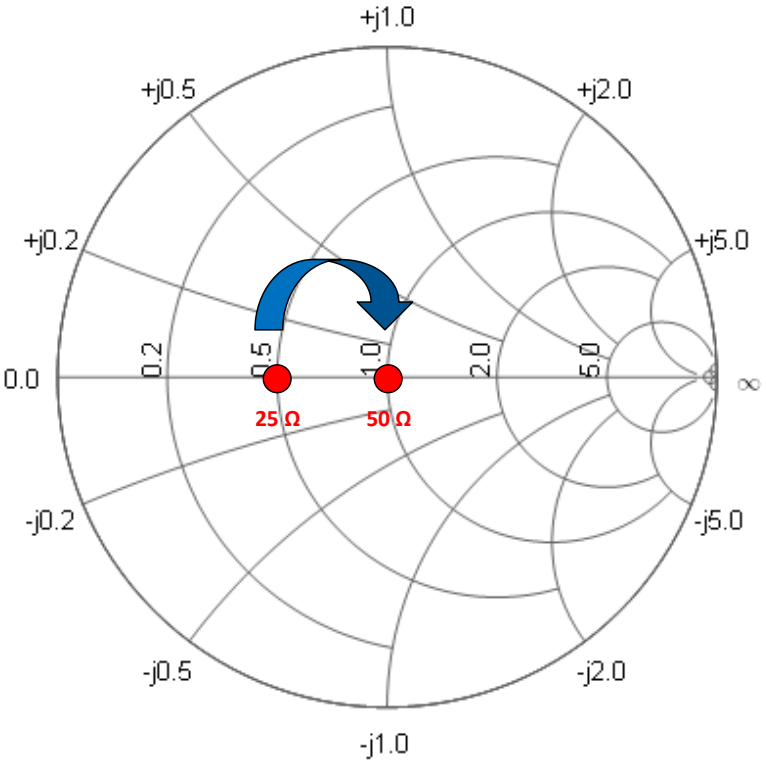


Figure 2.7: Load modulation transformation when *auxiliary* device is active while *main* device in stauration region.

Eventually, at maximum drive and PEP, when both amplifiers are in a near saturated state, the voltage and current contributions of *main* and *auxiliary* amplifiers are the same, meaning that the same output power is contributed by both of the amplifiers into the load.

Finally, both devices reach saturation and see the dynamic impedances shown in Figure 2.8. The changes of impedances for *main* and *auxiliary* devices at the low and high power region are known as load modulation. In reality, the load would be modified at the rate of the modulation envelope frequency, resulting in a significantly increased average efficiency over wide dynamic range.

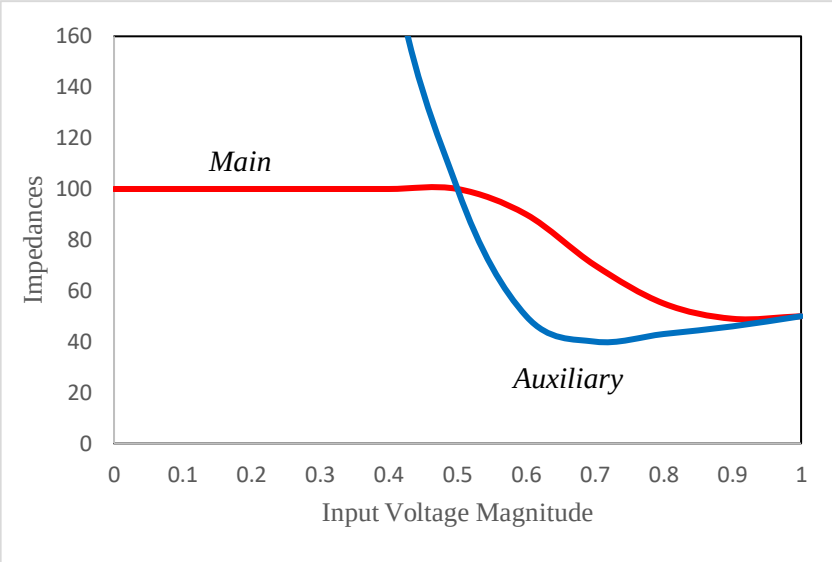


Figure 2.8: Impedance behaviour for both *main* and *auxiliary* devices.

2.3.2 Load Modulation in Doherty

Referring to Doherty behaviour discussed in the previous section, we can say that Doherty PA falls into the class of load modulation architecture which involves the dynamic modification of load impedance to capture high efficiency. Most research studies of Doherty PA design are described in terms of an active load modulation technique [66]–[69]. In [70] Chen et al. presented a technique to modify the load using shunt quarter wavelength short stubs. This Doherty PA operated from 2.0 to 2.6 GHz, and achieved an average 40% of drain efficiency over 8 dB dynamic range.

Modifying the load can also contribute to wideband Doherty design. The Load Modulated Balanced Amplifier (LMBA), although not strictly a Doherty amplifier, is one implementation of a load modulation architecture for wideband

applications, that uses a 3 dB hybrid coupler to create a third port for coherent signal injection and active load modulation. This method has been shown to achieve 70% of efficiency over an octave band [71]. Another approach in the wideband application space is termed *dynamic load modulation* [72]. This technique involves modulation of the load impedance using a 90V breakdown voltage silicon diode varactor. It is capable to attain the efficiency up to 79% from 1 to 1.9 GHz operating frequency at 10 dB PBO using GaN HEMT device technology and covers octave bandwidth.

Whilst in [73], an inverse class-F PA run at 1 GHz frequency could reach 60% of efficiency at 41.6 dBm maximum output power by changing the load modulation using tunable capacitors placed in the output resonator instead of fixed capacitor. However, this method only covers 5 dB of output power back-off.

N. Ryu et al. in [74] controlled the *auxiliary* amplifier's gate bias voltage using Variable Balun Transformer (VBT) impedance inverter to modulate the load, as well as eliminating the phase delay at the input path of *auxiliary* amplifier and reducing the overall size of the Doherty PA. This work has been demonstrated on 0.13-μm CMOS technology fabrication PA. The measured PAE was 51% at 1 dB compression of 31.9 dBm output power.

2.4 Doherty Implementations

The Doherty implementations discussed in the following sections are specifically the different approaches used to control the conduction behaviour of the *auxiliary* device, in order to achieve equal maximum current contribution for both

devices at PEP. Specifically, these techniques are i) Classical Doherty, ii) Bias Adaption and iii) Input Attenuation.

2.4.1 Classical Doherty

The Classical Doherty power amplifier (DPA) arrangement relies on a static bias approach to control the conduction of the *auxiliary* device and an asymmetrical power splitter arrangement at the structure's input in order to achieve the same maximum current for both *main* and *auxiliary* amplifiers at PEP. The classical DPA is the 'usual' or preferred implementation due to its simplicity and ease of implementation.

Another advantage highlighted by the classical Doherty is the eventual waveform tends to naturally resemble class-F waveforms. This means that the harmonics being generated by both devices are important. The class-F amplifier is based on a class-B bias arrangement, and can operate in a less saturated region to form a half sinewave current waveform and almost square voltage waveform. This is an interesting area for Doherty research, and taking into consideration harmonic tuning in Doherty architecture, class-F has been used in a number of implementations as a replacement to the usual class-AB for the *main* amplifier part [75], [76], which was known as F-DPA. However, these works only presented Computer-Aided-Design (CAD) optimization instead of theoretical and practical demonstration.

In [77], all the output current of harmonic components is short-circuited to form the sinusoidal waveforms characteristic of the class-F amplifier. However, the *auxiliary* amplifier was biased in class-C.

2.4.2 Input Attenuation

The basic idea of the input attenuation (IA) Doherty approach is to control the relative conduction of the *auxiliary* and *main* devices using the magnitude of the applied input signals rather than offsetting input bias [78]. Conceptually, the magnitude modification can be simply achieved by placing a symmetrical power splitter and a variable attenuator at the input path of the *auxiliary* amplifier. Another method is to use independent, phase coherent sources, one for the *main* and one for the *auxiliary* devices, and to adjusting the relative input phase of the signal applied to the *auxiliary* amplifier to achieve the required result [79].

A number of researchers have developed this basic idea to enhance efficiency, as shown in [79], where applying a dual input power arrangement to drive *main* and *auxiliary* devices, phase was aligned digitally to overcome the performance degradation due to dynamic phase misalignment. The PAE that resulted was above 50% over 8 dB of output power back off, which was 10% improvement in comparison to conventional analog Doherty PA architecture. In other work [80], the technique of adaptive input power distribution is proposed. An extended-resonance divider was designed to allow more power to be injected to both amplifiers. The input power was efficiently driven to both amplifiers which resulted in a 2%-3% improvement in PAE compared to a conventional Doherty PA design. This approach was verified in [81], showing that the input impedance can considerably affect the input drive for GaAs Heterojunction Bipolar Transistors (HBTs). The advantage of this approach is to avoid non-complexity of circuit design and a more compact design.

In other work, exploiting the input power and phase alignment mechanism digitally using DSP to produce dual input channel at the input was a good choice to avoid wasted input drive at PBO and correct the dynamic phase alignment between *main* and *auxiliary* amplifier [82]. This technique achieved 54% of average efficiency, which was 8% improvement compared to conventional Doherty PA.

As addressed in [83], an adaptive input power mechanism was attached to the *main* amplifier input to remove the gate leakage current presence when the input drive level increases. This work involves three stages DPA and consists of 10W, 15W and 35W of GaN HEMT devices represented *main*, first *auxiliary* and second *auxiliary* amplifier respectively. They were fabricated and tested at 3.5 GHz. This technique could achieve the drain efficiency up to 37.3% at 9.5 dB and 45.6% at 4.3 dB at power back off when applying CW signal, whilst achieved 39.5% at 8 dB PBO for WiMAX signal.

However, the overall input attenuation approach requires input magnitude detection to be placed at the *auxiliary* amplifier path, which inevitably increases design complexity and ultimately cost in comparison to classical Doherty implementations. On the other hand, the idea that in modern transmitter implementations, the availability of an additional RF path is not unreasonable, so the additional cost may be lower than first anticipated.

2.4.3 Bias Adaption

Due to the soft turn-on behaviour of transistor devices, fixed class-C biasing of the peaking PA in classical Doherty means that the current contribution following

the transition point is gradual rather than instantaneous. This causes problems that must be accommodated in Doherty design, and that ultimately results in reduced efficiency around the transition point. It is clear that precise control of the gate bias to allow the required conduction as and when required would be a good thing, and that would allow both the correct turn-on behaviour and the maximum current of *peaking* amplifier could be reached. The adaptive bias (AB) Doherty is one method to improve efficiency by controlling the gate voltage of *auxiliary* amplifier in response to input signal envelope, and can also involve gate voltage control of the *main* amplifier, to achieve optimal Doherty behaviour [84]–[86]. In comparison to IA Doherty, controlling bias at modulation frequencies is arguably easier (and lower cost) than controlling RF amplitude.

In the AB Doherty, in the low power region, the *main* amplifier is biased in class-B while *auxiliary* amplifier is some degree of class-C. The gate voltage of *auxiliary* amplifier must then be adjusted appropriately to give the desired output current for any input power in high power region from the transition point onward. Figure 2.9 clearly shows that there is a gradual transition from class-C to class-B of *auxiliary* amplifier, reaching equal gate voltage at maximum input drive level (PEP). The *main* amplifier bias voltage remains constant in this approach. Advantages include same-sized devices to be used and the bias profile may be adapted or shaped to achieve optimal performance.

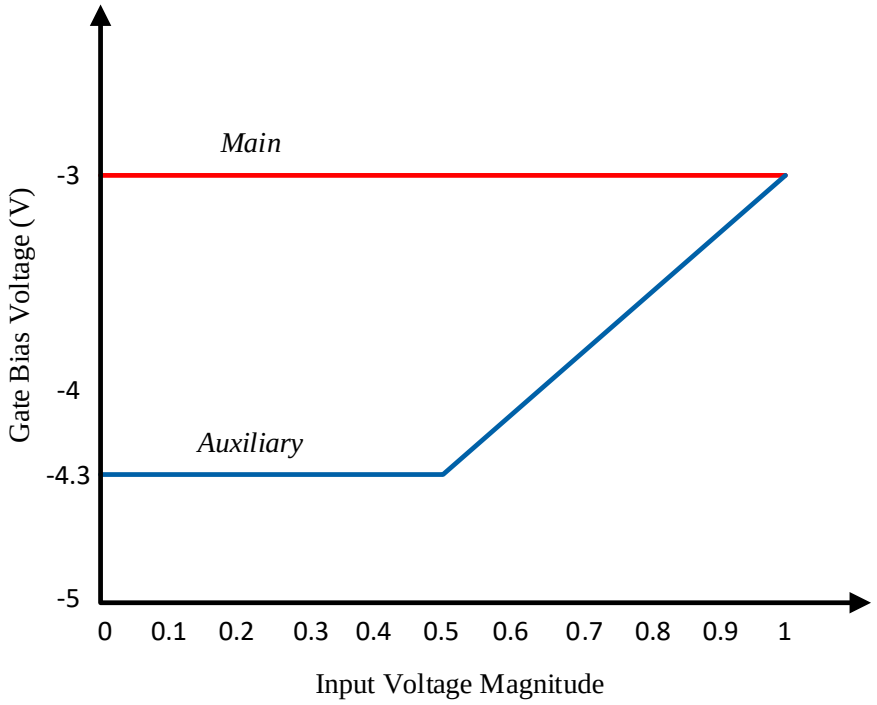


Figure 2.9: Gate bias profile corresponding to input voltage magnitude.

In [87], S. Chen and Q. Xue used an adaptive bias system controller to manage the gate voltage. Manually controlling however involves time constrains, so a simple network controller was proposed to use a forward bias diode and other lumped components to achieve the necessary control.

Supplying asymmetrical drain voltage at both *main* and *auxiliary* devices to improve efficiency at 8 dB power back off has been achieved in [88]. The drain voltage varies in the range of 30V to 50V. This method achieved 50% and 48% of efficiency at 55 dBm saturation power and back off power, respectively.

There has been effort to optimize the gate bias applied to *main* and *auxiliary* devices to supply higher output power. The main idea of this approach is to overcome the knee voltage effect that affects the performance of the Doherty efficiency as well as overall output power. Implementing this method results in 60.5% of drain efficiency at 44.35 dBm of average output power [89].

In [90], an adaptive bias circuit was attached to the *auxiliary* device using a lumped Lange quadrature coupler as a power divider for small cell base station applications. The wasted signal from the coupler's isolated port was used as an input signal for the adaptive circuit, giving an overall PAE of 45.8% at 38.6 dBm output power and 31.2% at 7 dB back off power, respectively.

Bias adaption approaches not only involve changing gate bias, but can also apply to modifying the device supply voltage. Several research studies have been conducted to produce high efficiency by manipulating the supply voltage. [91], [92]. This approach can achieve 40-50% of PAE in the range of 25-29 dBm output power when the supply voltages were set up from 1.5V to 4V.

2.5 Conclusion

Based on the literature studies above, it is clear that many methods exist and have been investigated to improve and maintain high efficiency performance over power back off, as well as other important parameters such as maintaining output power, bandwidth and linearity. The synthesis of accurately controlled relative phase drive signals enables the Chireix outphasing architecture to obtain high efficiency

over dynamic range, similar to that of a Doherty. As for ET systems, although promising to offer a wide bandwidth solution, the space required for the DC supply modulator and the bandwidth the modulator can realistically achieve are limiting factors. The Doherty architecture is the clearly a simple structure and the fact that it is an easily-linearised RF-in RF-out architecture continues to be attractive to industry, even though it is inherently band limited due to its use of quarter wave transformers, and makes this architecture the one of choice for base station application.

The classical Doherty PA has the capability of achieving high efficiency over 6 dB of power back off. The Input attenuation approach gives the opportunity to control relative phase between *main* and *auxiliary* inputs and can easily provide phase compensation, which is important for certain device technologies, although it does increase circuit complexity. The fundamental current and turn-on behaviour of the *auxiliary* amplifier can be most effectively managed using the bias adaption technique. This avoids early, or delayed turn-on of the *auxiliary* amplifier when *main* amplifier is not saturated or over compressed respectively.

Most of the adaptive bias techniques do not relate to gate bias modification of *auxiliary* amplifier, and are limited to the *main* amplifier, or involve the control of the DC supply, similar to ET. For this reason, the gate controlled adaptive bias Doherty architecture is consider as a priority in this PhD research.

In terms of measurement, it was important that all of the above Doherty implementations are able to use independent sources for achieving better measurement result. A bespoke measurement system needed to be conceived and implemented. This kind of measurement setup is discussed in Chapter 4.

CHAPTER 3

DEVELOPING IDEAL DESIGN PROTOTYPES THROUGH SIMULATION

3.1 Overview

Previously, in Chapter 2, a number of well-known architectures that have been used to enhance the efficiency are discussed. In addition, the basic concept and behavior of Doherty PA is highlighted as one of the most promising efficiency improvement methods. In addition to the classical Doherty, a number of advanced Doherty implementations are introduced namely input attenuation and bias adaption.

The main objective of this chapter is to discuss the development of a device modeling strategy which uses both ideal transconductive, and realistic manufacturer-supplied models used at low frequency operation to remove effects of reactive parasitic elements. The discussion goes further and addresses model validation to ensure that they are able to be used in Doherty PA design. Moreover, this chapter will also present the simulation activities of Doherty implementations and aims to identify the key differences between these techniques, taking the Classical Doherty PA as reference.

The chapter starts by introducing the ideal device model generated using a Keysight ADS symbolically defined device (SDD) and a realistic device model from

Wolfspeed, followed by both model's validation. Later, the chapter will describe the simulation results of three Doherty PA implementations. Finally, the findings from all Doherty approaches using validated device model will be compared and summarized.

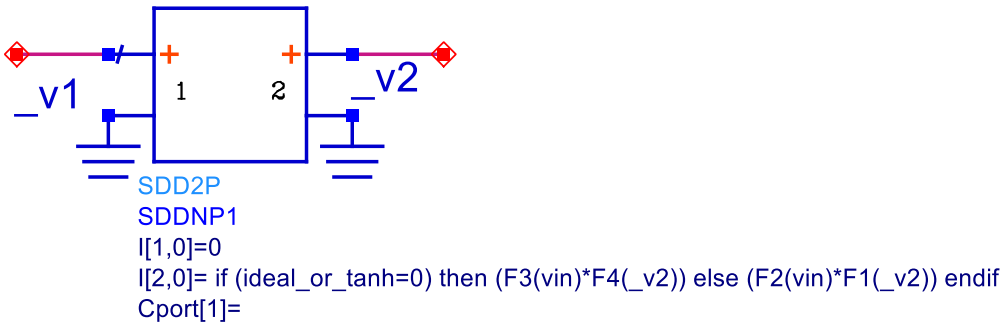
3.2 Development of an Idealized Device Model Approach

3.2.1 Ideal Model using a Symbolically Defined Device (SDD)

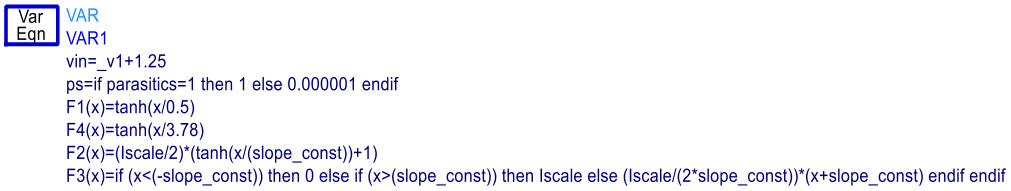
In any PA design, it is highly advantageous to establish a relatively ideal, reference design prior to a real circuit design activity, so that fundamental circuit operation can be confirmed, and the design is built within desired specifications. For an amplifier design, this normally begins by establishing a basic ideal model. For this aspect of the research, a very basic ideal model was needed for use within the Keysight ADS simulation environment that represented the relatively ideal trans-conductive nature of a typical RF device, but without any of the complexity introduced by reactive parasitic elements such as non-linear input and output capacitance. ADS offers an ideal component for this purpose in the form of a symbolically defined device (SDD), as represented in Figure 3.1 (a). This component can easily relate port voltage stimuli to a current response, through simple implicit (or explicit) equations, as shown in Figure 3.1 (b). Once the equations are established, all that needs to be done is to make the key parameters in the equations controllable to achieve the desired device characteristics. In this case, a series of hyperbolic tan (*tanh)* functions

are used to create this model, and specifically to represent the transconductance and knee-region behaviour of the device.

We first need to choose option *ideal_or_tanh*=0 to implement an "ideal environment" for the SDD symbol, without parasitic effects. Referring to equations in Figure 3.1 (a) and (b), decreasing the *slope_const* parameter leads to greater pinch-off value of transconductance plot with greater slope. Reducing the value of the parameter *Iscale* reduces the saturation current of transconductance characteristic. By adjusting the constant (currently 3.78) in function F4(x), a variety of knee characteristics, ideal to very 'soft' can be obtained.



(a) Ideal GaN transistor model built from an SDD component. By adjusting key parameters, essential device characteristic can be easily modelled



(b) Ideal GaN transistor model built from an SDD component. By adjusting key parameters, essential device characteristic can be easily modelled

Figure 3.1: Ideal GaN transistor model built from an SDD component (a), drive from a set of equation (b). By adjusting key parameters, essential device characteristic can be easily modelled.

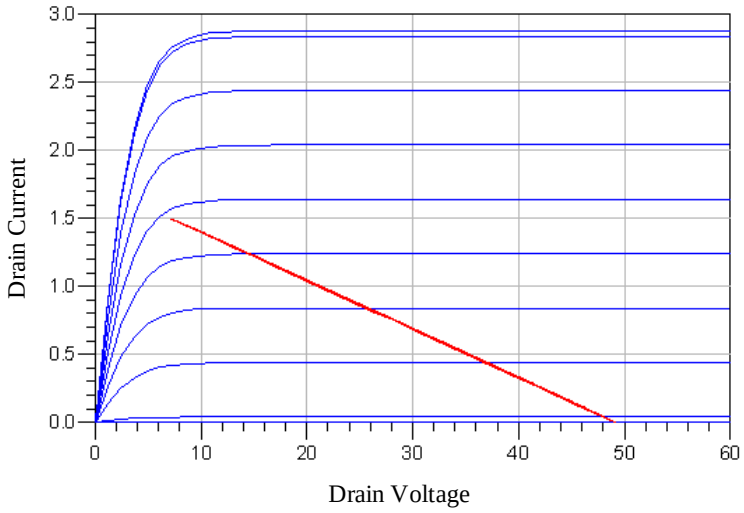


Figure 3.2: DC-IV plot generated by the SDD model, input biased at -2.1V, prooving that this model works as expected in a Class-A amplifier configuration

3.2.2 Realistic Model from Wolfspeed

Once fundamental circuit operation has been established, the ideal model discussed in subchapter 3.2.1 can be replaced with a much more representative, 'full' non-linear manufacturer-provided device model to allow simulation of the device in a realistic environment. For this work, a 10W gallium nitride (GaN) high electron mobility transistor (HEMT) device from Wolfspeed were to be used. The most recent models provided by Wolfspeed, are particularly suitable for this work as they provide access to both the intrinsic current generator plane and external package plane waveforms. Visibility of the fully de-embedded intrinsic device RF waveform behavior relative to the intrinsic DC extracted I-V curve functionality is valuable for design as allows the dynamic load line to be revealed by plotting the time domain

current versus voltage waveforms. This can then be plotted relative to the static DC-IV characteristic to allow 'traditional' load-line based PA design to continue, and dynamic interaction of the load line with the transistors IV boundary conditions, for example the knee voltage, to be explored. This is particularly important in Doherty design as using the Doherty's *auxiliary* device to 'control' the *main* device load line behavior, and to prevent knee interaction is key in achieving optimal Doherty behavior, is only possible using fully deembeded waveforms, and is a focus area of this research.

In comparison to silicon, GaN devices can tolerate high electric fields, and hence have higher breakdown characteristics. They also possess a higher current density and lower intrinsic input and output capacitance in comparison to competitor technologies, such as Laterally Diffused MOSFET (LDMOS), Gallium Arsenide (GaAs) and Gallium Nitride on Silicon (GaN-on-Si), which in turn provides an advantage of, allowing smaller devices with higher input and output impedance, providing wider bandwidth matching and a better choice for compact design. Details about this device can be found in Datasheet attached in Appendix A.

3.2.3 Model Validation

Both device models need to be validated to ensure that they are suitable to be used in design. The ideal and real device models must firstly be comparable to each other in terms of general performance, because they will be used in higher amplifier design later in this thesis. Hence, a simulation that involves comparison between SDD and Wolfspeed device model is included here for that purpose.

Firstly, the fundamental controlling parameters of the ideal device model discussed in section 3.2.1 above are adjusted to achieve a good DC agreement between the SDD and Wolfspeed models. Remembering that the non-ideal effects due to a device's reactive parasitic elements can be significantly reduced by simply reducing the operational frequency, this step ensures the Wolfspeed model can be presented as a relatively "ideal" model with no parasitic effects, in addition to using SDD ideal model. The idea here is that this provides an intermediate step, between highly ideal, and realistic behavior and will allow improved design.

The first comparison involves using the schematic shown in Figure 3.3 and an AC simulation at a reduced 100MHz operating frequency, to avoid parasitic effects in the Wolfspeed model. A low frequency, such as 100MHz is chosen because it does not excite the parasitic elements within the device model, therefore simplifying the model behavior, providing clarity and aiding understanding. In a DC circuit, an inductor has minimal resistance and the current flows through the inductor directly. As the frequency increases, the behavior of magnetic fields will cause the inductor to exhibit increasing impedance. Similarly, a capacitor acts as an open circuit to DC and once the AC current injected, the capacitor will exhibit lower and lower impedance as the frequency increases. The parasitic elements effect is discussed in further details in subchapter 6.2. DC blocks are used in the schematic in to prevent DC current into the source and load, and to pass only AC signals, while an ideal DC feed is used to allow DC current flow whilst blocking the RF signal from entering or 'seeing' the DC bias supplies. The voltage for gate and drain are set to -2.1V and 28V respectively, whilst input voltage is swept in the range of optimized value 0.1V to 1V throughout simulation. The output *term* component is used to represent the ideal real load for this device of 28 Ohms.

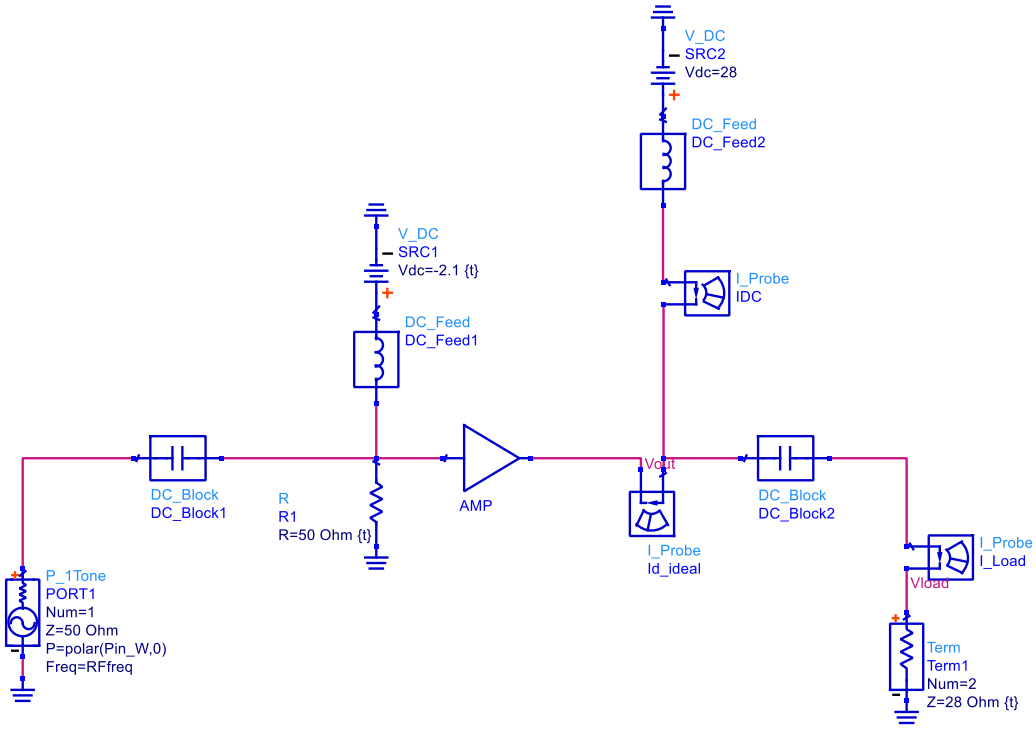
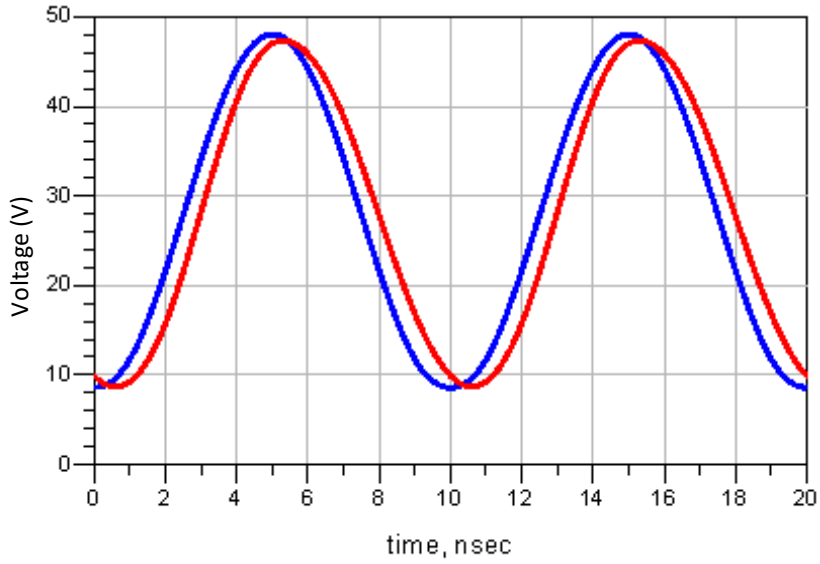
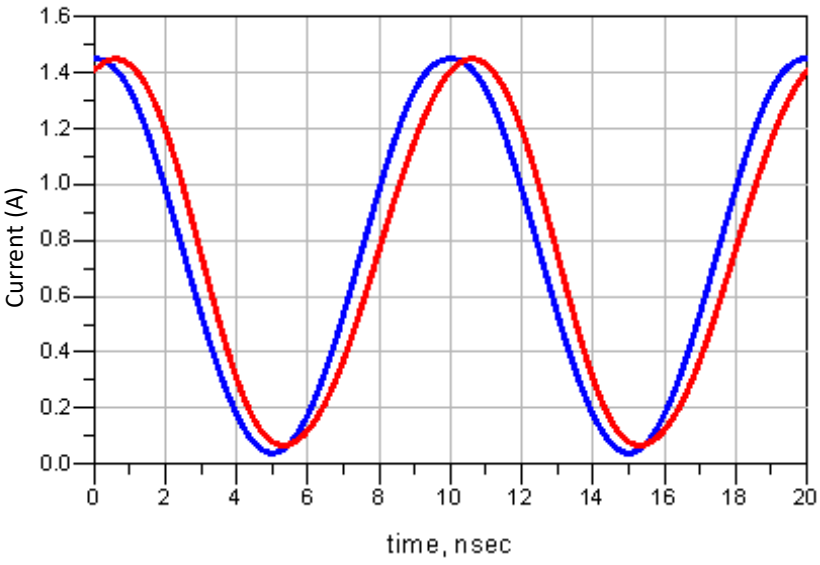


Figure 3.3: Schematic of simple AC simulation for both SDD and Wolfspeed model at low frequency

Overall performance in terms of gain and efficiency is shown for both device models in Figure 3.6. The gain is similar at typically 30 dB while the efficiency reaches the maximum of 40% over output power range used and shows a good agreement. The plot in Figure 3.4 depicts a 40V peak-to-peak voltage waveform for both models, with a small phase shift introduced by the Wolfspeed device model. The phase delay is evident in current waveforms as well, with a peak current of 1.5A observed. The small difference in phase is noted, but considered an acceptable difference at this stage, and is an internal effect of GaN transistor itself.



(a) Voltage plot for SDD and Wolfspeed devices (blue: voltage for SDD device; red: voltage for Wolfspeed device)



(b) Current plot for SDD and Wolfspeed devices (blue: voltage for SDD device; red: current for Wolfspeed device)

Figure 3.4: Voltage and current waveforms for SDD and Wolfspeed device models at P1 dB

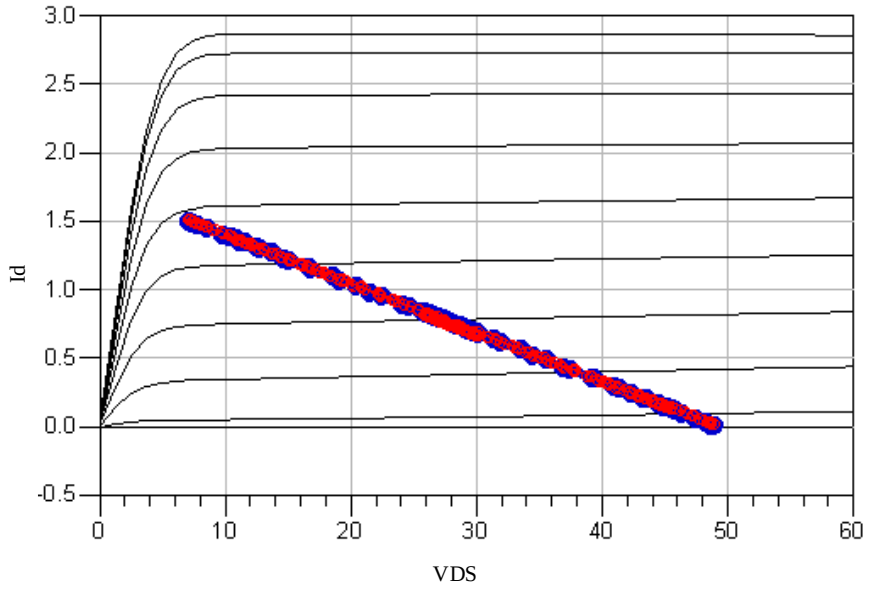


Figure 3.5: Plots of laodline for both SDD (in blue) and Wolfspeed (in red) device model at P1 dB. The loadlines are captured for a class-A amplifier, which generated approximately 1.5A of drain current and 49V maximum drain-to-source voltage

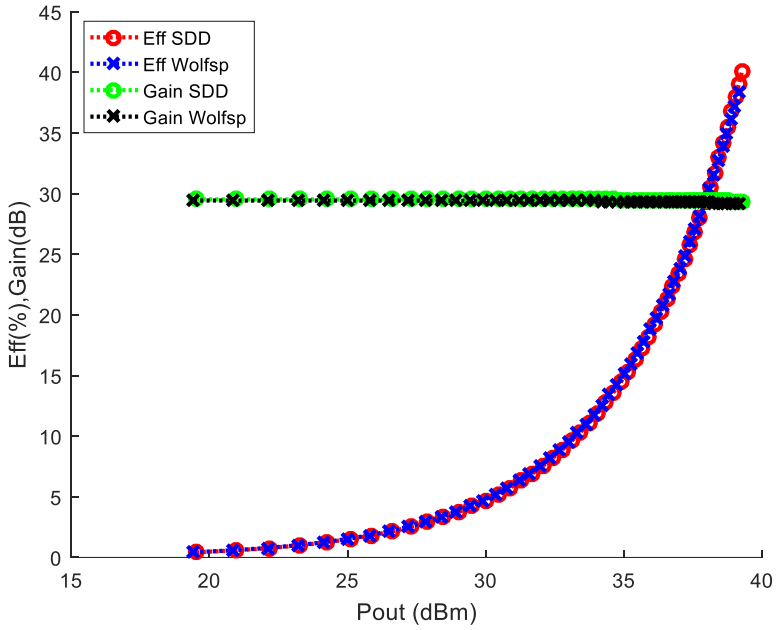


Figure 3.6: Plots of efficiency and gain for both ideal SDD and Wolfspeed device model

3.3 Simulating DPA Implementations

3.3.1 Classical DPA Simulation

Having shown that the SDD-based and Wolfspeed models agree, the investigation then proceeded to build a classical Doherty PA architecture that involves *main* and *auxiliary* devices connected at their outputs with an impedance transformer presented as a λ/4 transmission line. The *main* and *auxiliary* devices are biased in class-B and class-C for *main* and *auxiliary* amplifiers respectively.

Figure 3.7 below shows the schematic of a basic classical Doherty PA architecture, where it can be seen that no output matching other than the λ/4 transformer is necessary because operation is at low frequency (100 MHz). The amplifier symbol is generated from simple schematic shown in Figure 3.8. The R1 resistor is placed before the device to control the impedance and overall stability of the circuit itself.

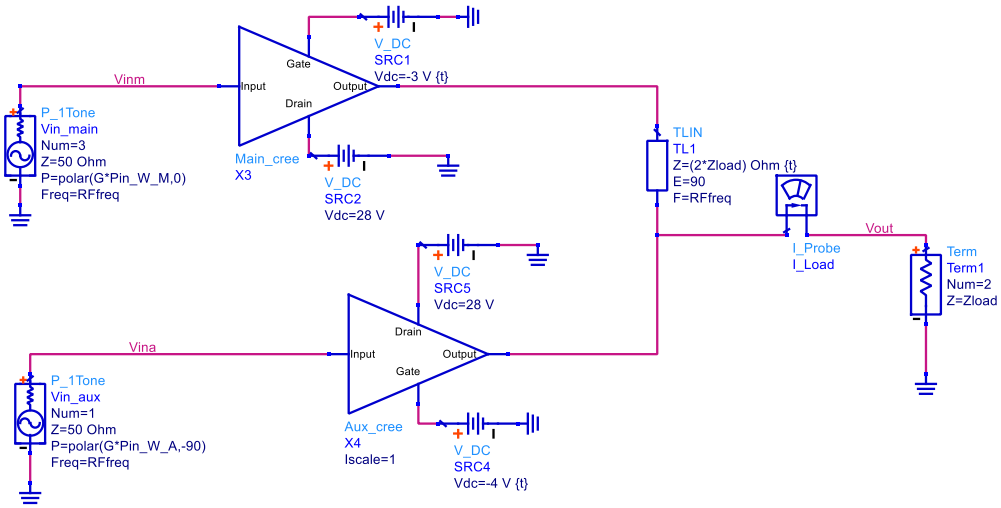


Figure 3.7: A Classical Doherty PA schematic built from realistic Wolfspeed device models at low frequency allowing parasitic effects to be ignored

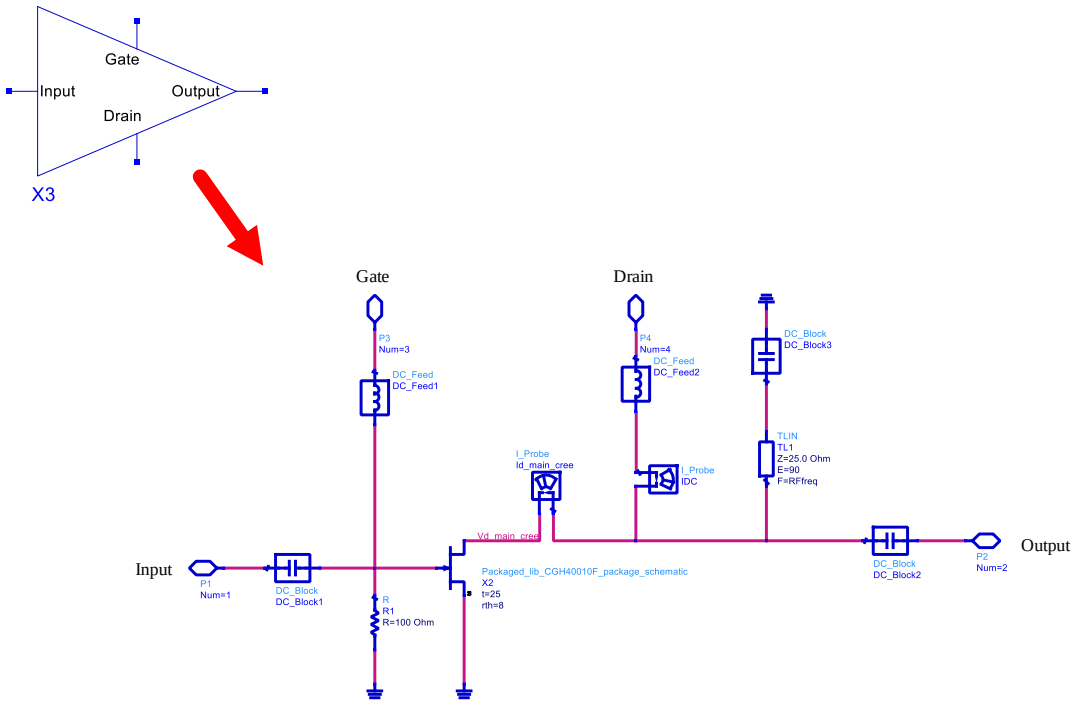


Figure 3.8: The circuit that exists within each amplifier symbol, showing the presence of ideal DC blocking and feed components, current meters, voltage nodes and an even-order harmonic trap in the form of a shorted λ/4 wave line.

This design is built with asymmetrical drive *main* and *auxiliary* amplifiers. Two input sources are connected to the classical Doherty architecture, labelled as Pin_{WM} and Pin_{WA}, which represent the input power for *main* and *auxiliary* amplifiers respectively, in response to the input voltage. Input voltage for *main* amplifier is normalised from 0.1 to 1 and it is swept in harmonic balance simulation. Vin_{aux} is built from an equation (5) to represent the behaviour of *auxiliary* amplifier. The current remains zero when Vin_{main} is not yet reached half of maximum voltage, and will further increase with some factor, and vice versa. The relative input phase at the

input of *auxiliary* amplifier is set to -90 degree to compensate the phase delay line introduced by λ/4 inverting transformer.

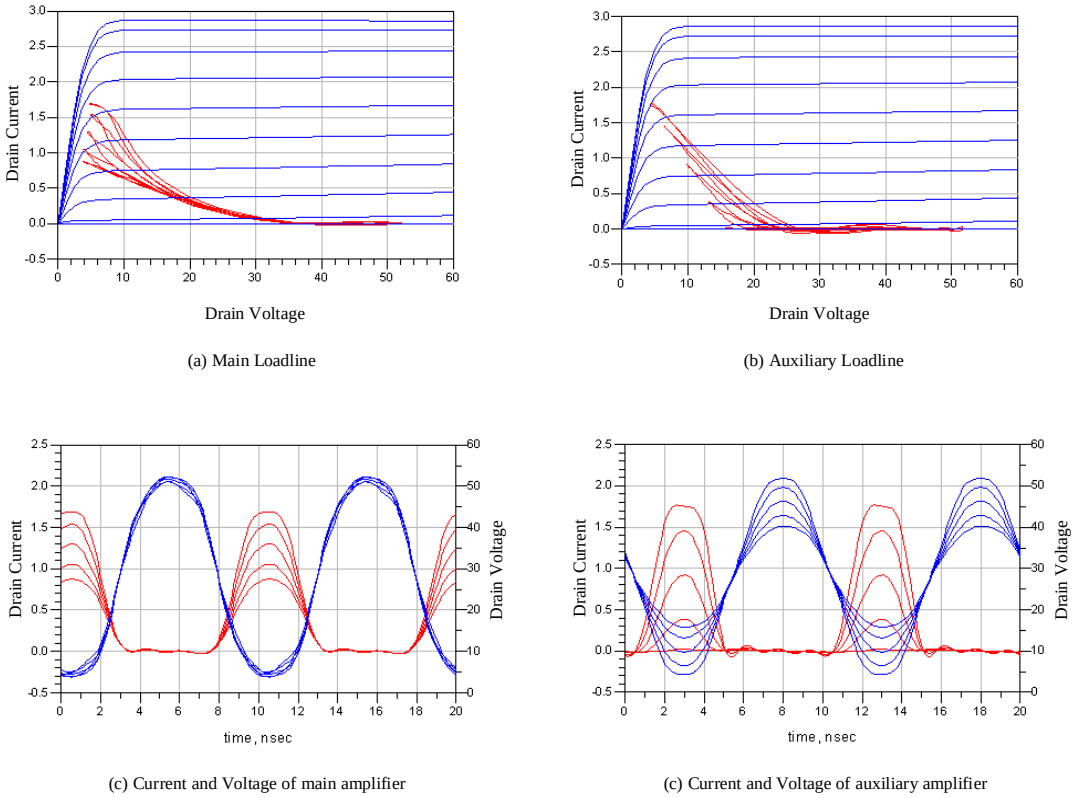
$$Pin_{W_M} = \frac{Vin_{main}{}^2}{R} \quad (2)$$

$$Pin_{W_A} = \frac{Vin_{aux}{}^2}{R} \quad (3)$$

$$Vin_{main} = from\ 0.1\ to\ 1\ (nomalised) \quad (4)$$

$$Vin_{aux} = if\left(Vin_{main} < \frac{Vin_{max}}{2}\right) then\ 0\ else\ (\left(Vin_{main} - \frac{Vin_{max}}{2}\right) * factor) endif$$

(5)



(a) Main Loadline

(b) Auxiliary Loadline

(c) Current and Voltage of main amplifier

(c) Current and Voltage of auxiliary amplifier

Figure 3.9: *Main* and *auxiliary* amplifier behaviour for Classical DPA simulation at high power region, *main* amplifier biased in Class-B while *auxiliary* amplifier biased in Class-C. Referring to (c) and (d), the red plot represent drain current while the blue plot represent drain voltage.

Figure 3.10 described the amplitude of fundamental current and voltage for *main* and *auxiliary* device in response to increasing input voltage. In the low power region below the transition point (Vin=0.65V), we can see that the *main* voltage linearly increases until it reaches saturation, whilst the *main* current also increases linearly, in agreement with theory, to reach a current of approximately 0.5 I_{max} of 0.45A. From the transition point voltage onward, the high power region begins and the fundamental current supplied by the *auxiliary* device rises from zero until it

reaches almost the same maximum current as *main* device, whilst the voltage remains relatively linear. Note that some expansion is observed due to the compression of *main* amplifier when the input voltage keeps increasing and the non-ideal behavior of realistic Wolfspeed device.

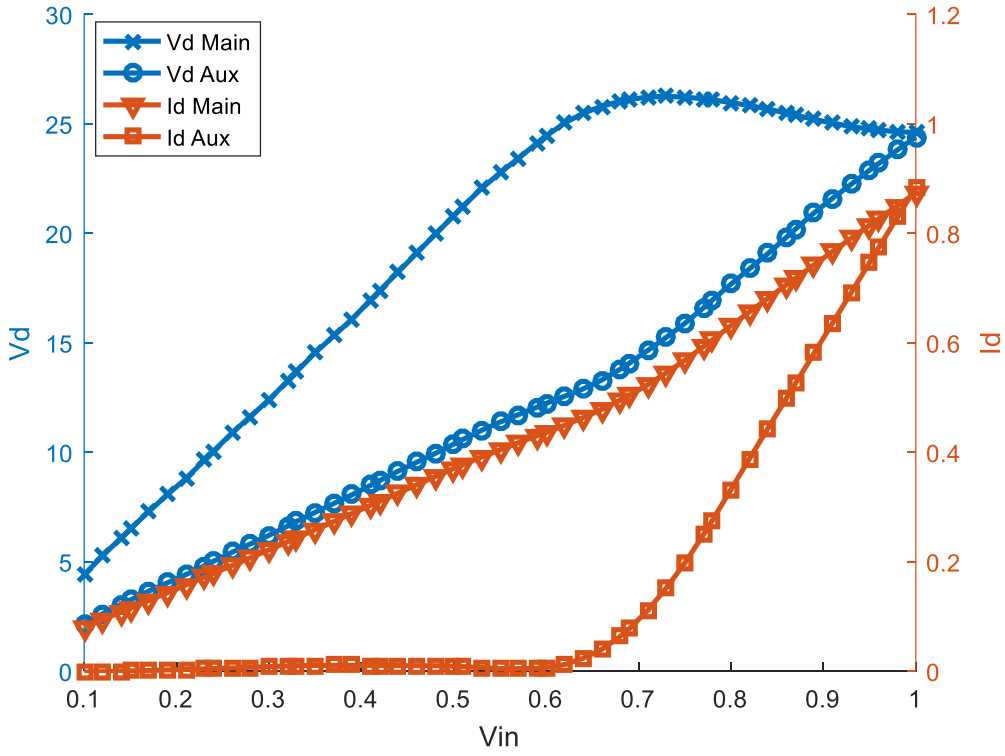


Figure 3.10: Drain current and drain voltage behavior of Classical Doherty PA in response to input voltage

The first peak of efficiency takes place at the transition point when *main* device voltage reaches saturation and the *auxiliary* device current begins to increase. It is worth remembering that the plotted efficiency refers to Drain Efficiency (DE). Power-Added Efficiency (PAE) is not considered in the analysis due to very high gain of the device an that fact that under these conditions, PAE will be very similar to DE. The efficiency plateau occurs as the *main* device voltage is held constant and the *auxiliary* current increases. Both peak efficiencies could reach 70% of overall performance at 6dB back-off power, whilst the total gain gives an average value of 35dB overall, however this slightly increases at the point when *auxiliary* device operated, due to the non-ideal GaN device behaviour.

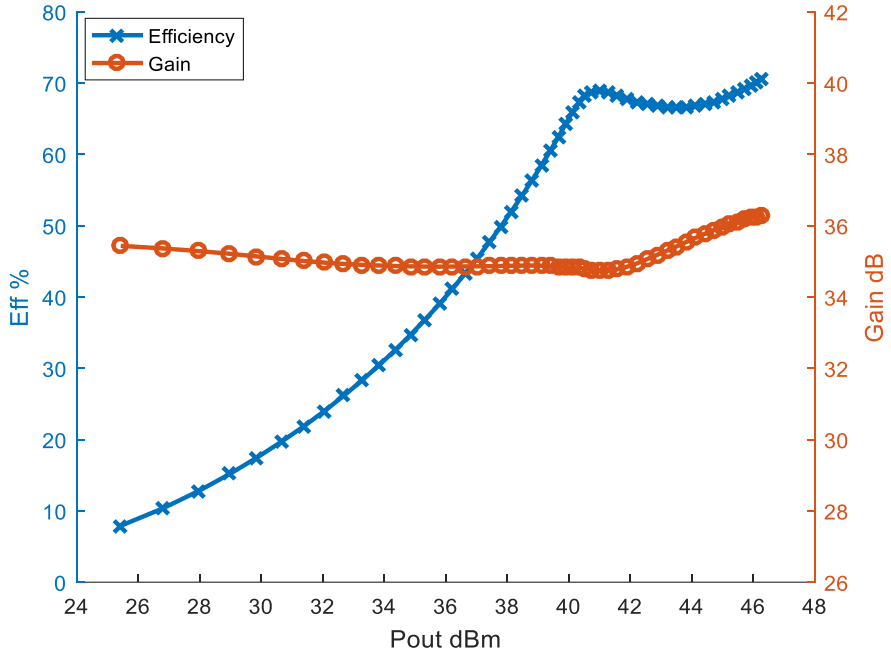


Figure 3.11: Efficiency and gain of Classical Doherty PA in response to output power

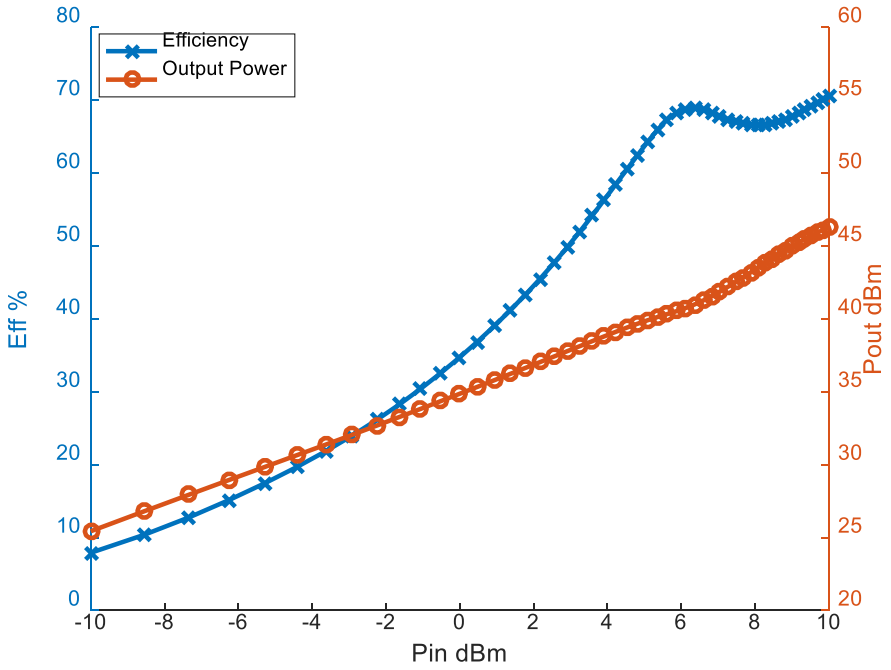


Figure 3.12: Efficiency and output power performance of Classical Doherty PA in correspond to input power

3.3.2 Input Attenuation Simulation

As discussed in earlier chapters, input attenuation is another approach to achieve Doherty action, and improve the efficiency through conduction behavior of *auxiliary* device control. In this approach, the magnitude of *auxiliary* device excitation needs to be modified dynamically in response to magnitude of *main* device excitation. This approach uses the same structure as Classical Doherty PA, the difference is that the same biasing point, class-B condition can now be applied to both *main* and *auxiliary* devices. Adjustments are made to the value of input phase and input drive to ensure the relative input phase and magnitude differences are well aligned. The input voltage sweep is set to the optimum, between 0.1V and 1.0V to make the analysis easier. The input power delivered to the *auxiliary* device is modified according to the desired fundamental output current profile, and ensures the *auxiliary* device is able to start delivering current to the load when the fundamental current of *main* device reaches corresponds to the transition point. The graph in Figure 3.13 shows that current of the *main* device increases linearly throughout, and the *auxiliary* device increases linearly from the transition point until the PEP (Vin=1) is reached, where both devices contribute exactly the same fundamental current to the load. The behavior of fundamental currents and voltages during throughout the amplifier dynamic range are well illustrated in Figure 3.13.

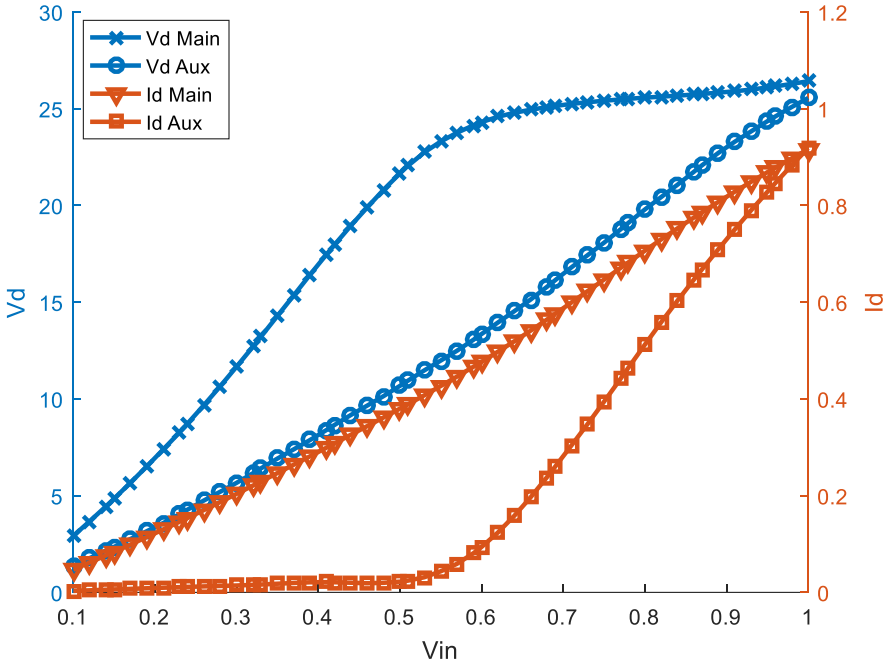


Figure 3.13: Drain current and drain voltage behavior of input attenuation approach in response to input voltage

Throughout the power sweep, and with reference to Figure 3.14 and Figure 3.15, the combined fundamental power can be seen to linearly increase without any obvious sign of compression. The average efficiency is 65% over the high-power region, whereas below transition point it reduces to 30%. The peak efficiency occurs at PEP, and is 73%, which is 3% higher compared to Classical DPA as discussed in subchapter 3.3.1. This is due to the fact that in the input attenuation Doherty, both *main* and *auxiliary* devices are biased in class-B at PEP, whereas in classical Doherty, the *auxiliary* device remains in class-C, and therefore contributes less fundamental current due to its reduced conduction angle mode of operation [63].

It should also be noted that the efficiency at the transition point is suppressed compared to classical Doherty. This is again because of the class-B bias, and the fact that there is a small quiescent current flowing in the shallow class-B bias point used, which reduces efficiency slightly as the *auxiliary* device begins to contribute current.

In summary, it is observed from these simple simulations that the input attenuation Doherty can offers improved performance in comparison to the classical approach, in terms of its linearity, although the transition point efficiency is degraded due to the class-B bias of the *auxiliary* device.

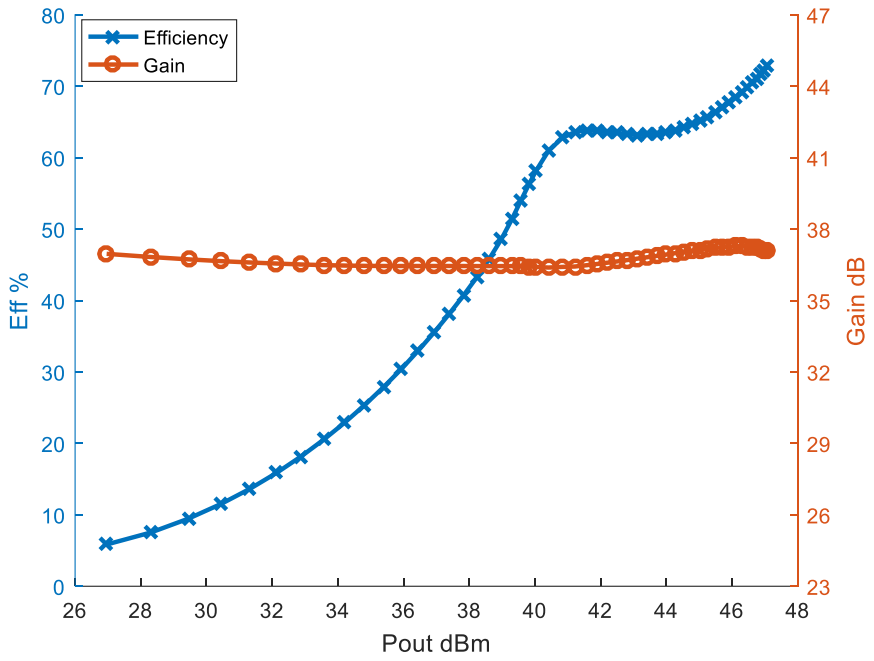


Figure 3.14: Efficiency and gain of input attenuation approach in response to output power

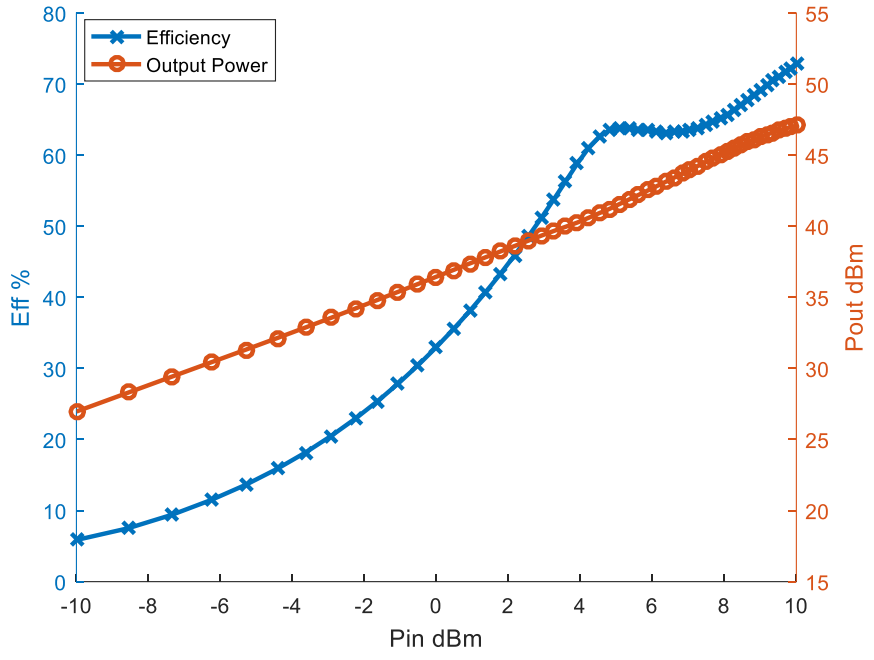


Figure 3.15: Efficiency and output power performance of input attenuation in correspond to input power

3.3.3 Adaptive Bias Simulation

Another way of fulfilling the requirement of *auxiliary* fundamental current is by dynamically controlling the conduction angle of *auxiliary* device. This approach can be done by modifying the gate bias voltage applied to the *auxiliary* device itself in response to the magnitude of the applied input signal, according to a defined profile or 'shaping function'. One advantage of this approach is an ability to set the bias voltage of *auxiliary* device such that it is completely 'off' throughout the entire low power region, right upon to the transition point, while *main* device remain active, thus reducing quiescent current and recovering efficiency around the transition point. Additionally, this approach can correct for the soft turn-on behavior of the *auxiliary* device around the transition point. This is important as an abrupt *auxiliary* turn-on allows the *main* device voltage to expand to its maximum value, before being limited by the current of the *main* device. In comparison, *auxiliary* bias in the classical Doherty needs to be adjusted such that the *auxiliary* device starts conducting before the transition point, again, degrading efficiency around this area.

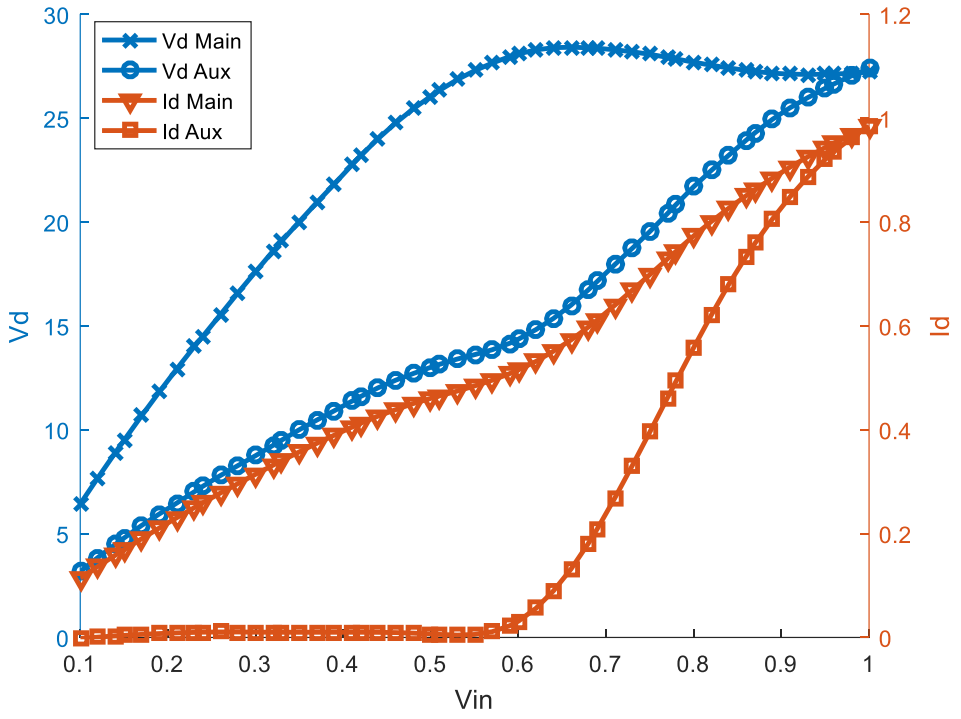


Figure 3.16: Drain current and drain voltage behavior of adaptive bias approach in response to input voltage

Referring to Figure 3.17 and Figure 3.18 below, the gain shows a small amount of compression throughout the low-power region when only the *main* device is active, which is typical of this type of GaN device in this bias condition, and later shows expansion as the *auxiliary* device becomes active. The same condition affected to the output power which is generating non-linearity at the transition point area indirectly. This is due to knee voltage effect when the gate voltage is hardly applied. However, this condition gives 1dB greater of dynamic range at back off power compares to previous approach and same peak of efficiency at both *main* and *auxiliary* device operation region. The performance comparison for all Doherty implementations can be referred in Figure 3.19.

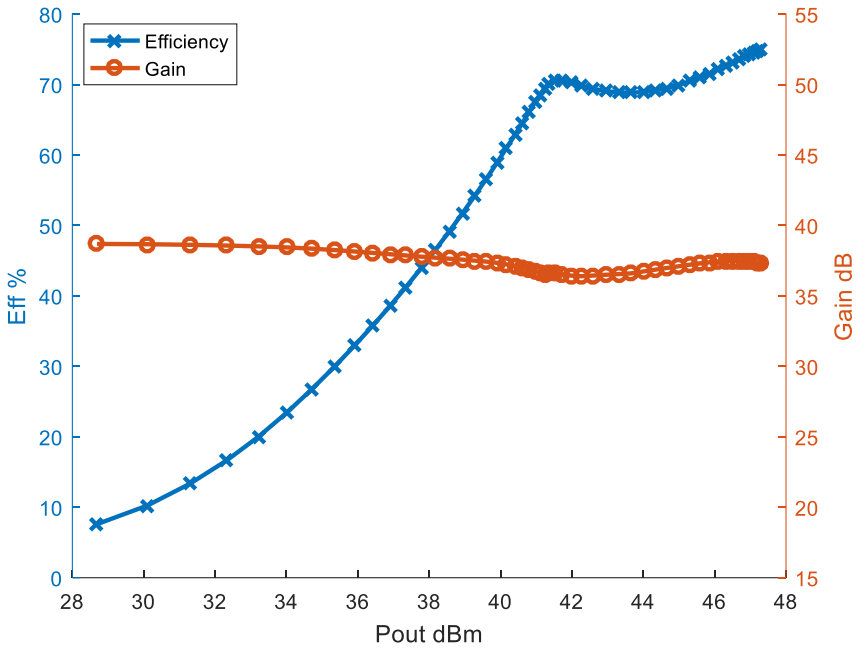


Figure 3.17: Efficiency and gain of adaptive bias approach plotted verses output power

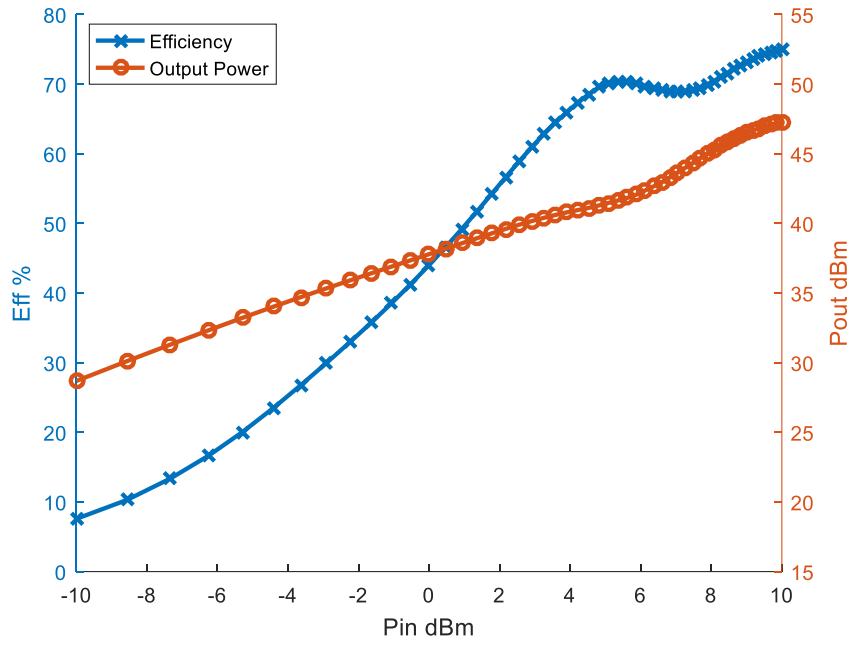


Figure 3.18: Efficiency and output power performance of adaptive bias approach plotted verses input power

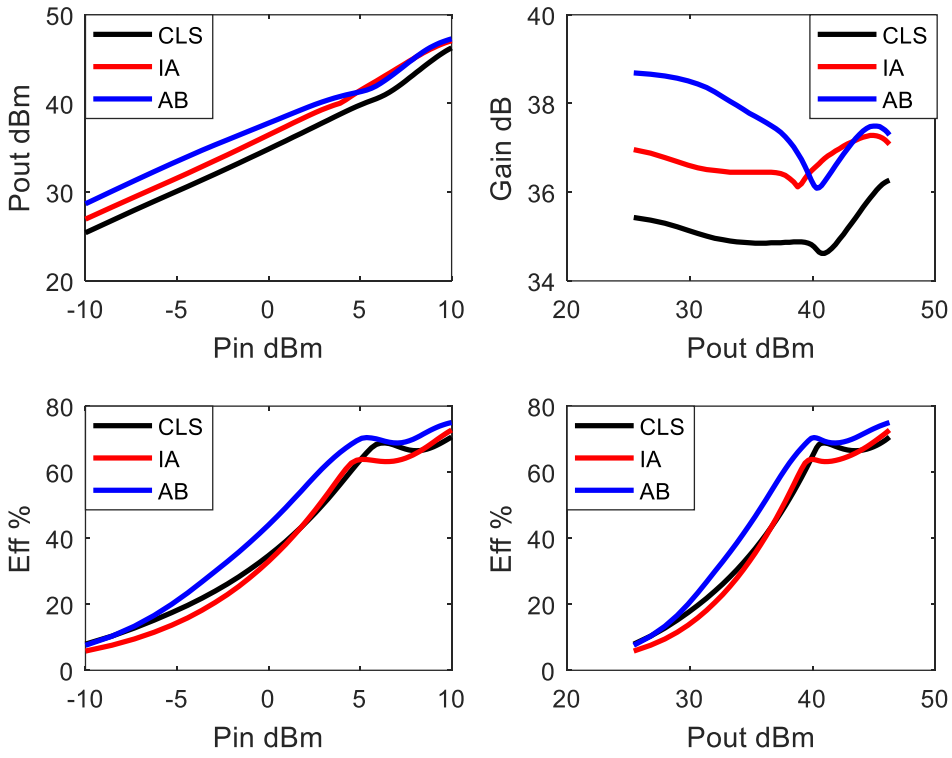


Figure 3.19: Comparison of overall performances for all Doherty implementations; note that CLS = Classical Doherty, IA = Input Attenuation Doherty, AB = Adaptive Bias Doherty

For each Doherty implementations, the amplitude-to-amplitude modulation (AM-AM) and amplitude-to phase modulation (AM-PM) distortion outputs are captured in Figure 3.20 respectively when the shaping function is applied, as the results of pre-distortion. How does the shaping function and its inverse function work to improve the overall AM-AM and AM-PM performance is further discussed in subchapter 6.7.2.

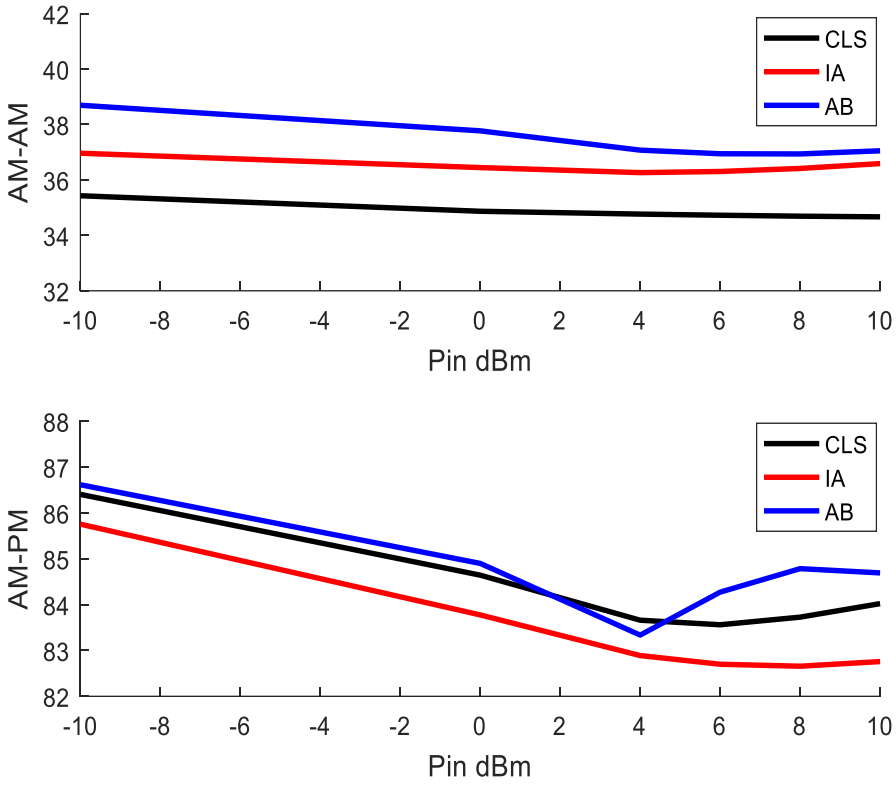


Figure 3.20: Comparison of AM-AM and AM-PM for ideal Classical (black line), input attenuation (red line) and adaptive bias (blue line) Doherty

In order to overcome the soft turn-on effect of the *auxiliary* device associated with classical Doherty behavior, some analysis needs to be firstly done to find the ideal function that relates bias voltage required to the input power, to cause an abrupt turn-on and then linear fundamental current increase. This was done empirically and manually, by defining a suitable profile, and then fitting a polynomial, as illustrated in Figure 3.21. The gate voltage is first set to -6V to ensure it is totally off at all levels in the low power region, before applying a suitable voltage to cause immediate turn-on at the transition point. This function can then be used to implement the required dynamic *auxiliary* gate voltage as the input magnitude varies. In a real environment, this function could simply be achieved using a diode varactor to generate the baseband signal, and a Field-programmable Gate Array (FPGA) board to control the bias voltage.

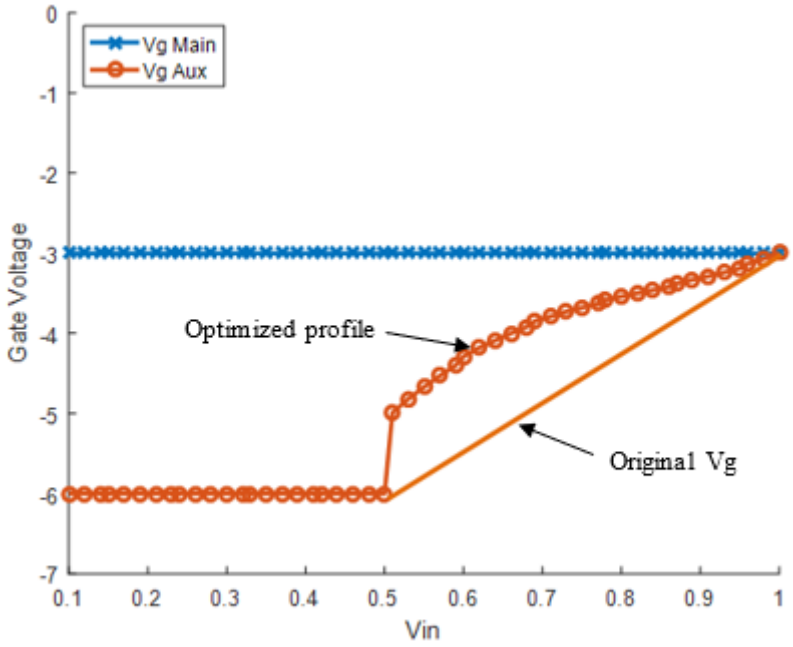


Figure 3.21: Adaptive bias profile for *main* and *auxiliary* device

The faint dotted line in Figure 3.22 shows the original fundamental current response to the applied gate voltage, and the resultant, linearized response to the new gate bias profile. We can see that the transition point of optimised *auxiliary* drain current is started early as compared to the original line with response to the slightly increase of maximum current.

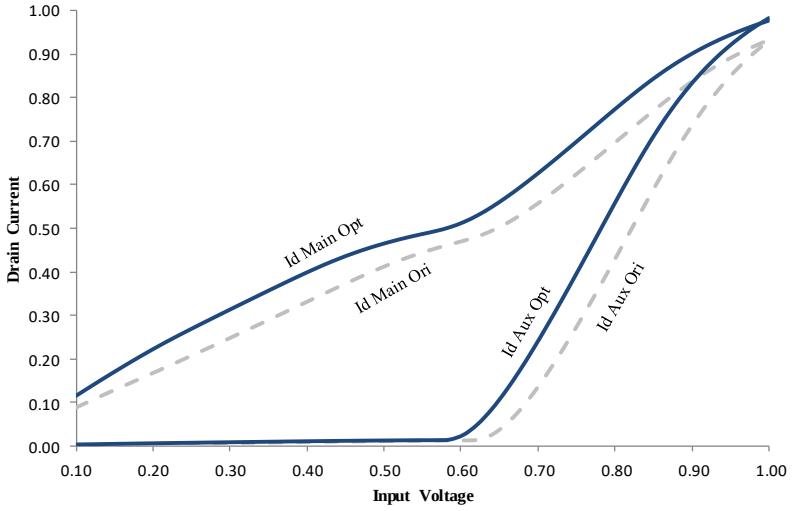


Figure 3.22: The fundamental current for *main* and *auxiliary* device at original and optimised bias profile.

3.4 Conclusion

Based on the simulation results, Doherty behavior was observed in different implementations using both device models discussed; a relatively ideal SDD component and a realistic Wolfspeed model running at low frequency, within the ADS simulation environment. A GaN technology was chosen as it offers many advantages over for example Si LDMOS in that it has higher power density, less parasitic output capacitance, reduced physical size and is more easily matched.

The three approaches of classical Doherty, input attenuation and adaptive bias were compared as approaches to improve efficiency over dynamic range. From the simulation results, it can be seen that the three approaches offer different advantages

and disadvantages; the overall efficiency performance in response to output power was highest for the adaptive bias approach, whilst for the input attenuation approach, linearity was better, and peak efficiency was higher in comparison to Classical Doherty PA, but lower at the transition point due to *auxiliary* device quiescent conduction. In term of input power sweep response, input attenuation approach is almost linear compares to adaptive bias. The simulations of all approaches prove that they can all be utilized to enhance the overall efficiency performance. In this work, we will focus on adaptive bias approach because it indicates very good efficiency at both transition and peak power, as comparison to other approaches.

CHAPTER 4

INDEPENDENT-SOURCE MEASUREMENT SYSTEM

4.1 Overview

In the previous chapter, a number of ideal designs were discussed in detail. Before progressing with the design of the real prototype, which will be discussed in detail in Chapters 5 and 6, it is important to be familiar with the measurement system that will be used to characterise these. The first objective of this chapter is to identify the measurement need and the possible measurement approaches to that can be adopted to prove the simulation activities of each Doherty PA implementation.

The second objective is to recognize the limitations of each measurement approach, and potential solutions to achieving phase coherence between the independent sources, and involves a number of measurement arrangements using different instruments. An independent, dual-input measurement system is found to be the best solution available, and is discussed in detail.

Following the identification of instrument limitations, three options are identified as the most likely measurement solutions to fulfil the test requirement.

4.2 Measurement System Approach

4.2.1 Dual-input Doherty: An Ideal Measurement Approach

The measurement system shown in Figure 4.1 is able to test the dual-input Doherty power amplifier [81]-[82], and is in fact very similar to the transmitter architecture that would be used in a real system using this type of dual input Doherty PA. A similar measurement approach is typically used to characterize Multiple In Multiple Out (MIMO) systems [94]. The measurement system consists of a Digital Signal Processing (DSP) board that generates two baseband signals, X_{BBM} and X_{BBA} for *main* and *auxiliary* inputs, respectively, at a clock frequency that is identical for the two signals, and with a time alignment that is ideally perfect. Both signals are up-converted by using a common Local Oscillator (LO), thus guaranteeing frequency and phase coherence, except for the phase noise added by the up-converters. The modulated RF signals are then amplified by driver PAs before being fed to the Doherty PA fixture. The modulated RF input signals are called X_{RFM} and X_{RFA}, and their phase and amplitude can be fully and accurately controlled by acting on the baseband I and Q signals at DSP level. In other words, the splitting function f_{SPLIT} between *main* and *auxiliary* can be implemented in amplitude (A_{SPLIT}) and phase (θ_{SPLIT}) at baseband:

$$X_{BBA} = X_{BBM} e^{j\theta_{split}} \tag{6}$$

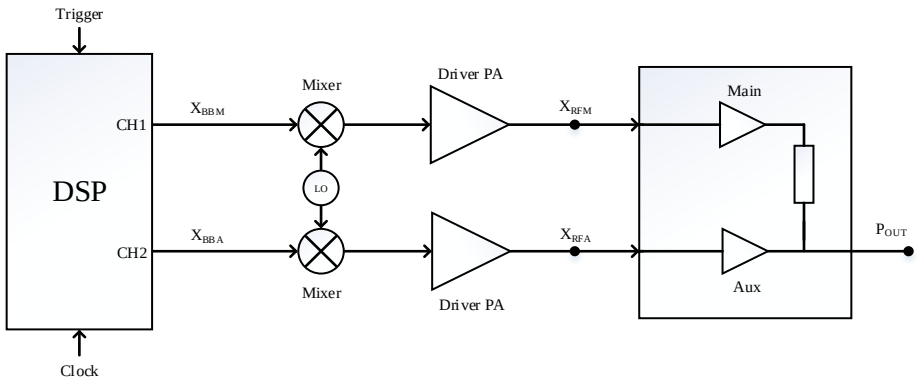


Figure 4.1: Ideal measurement system for Dual-Input Doherty

Unfortunately, a dual IQ output DSP board was unavailable for these experiments, so another measurement approach needed to be identified.

4.2.2 Independent Signal Generator Excitation

An alternative solution to the previously described system is to use two independent benchtop vector signal generators (i.e., RF generators with internal IQ modulators) and to somehow synchronise them in order to achieve frequency and phase coherency of the RF carriers, and clock and time alignment of the modulated signals. Figure 4.2 shows two independent RF vector arbitrary wave generators, considering in particular the Keysight solution, as Economy Signal Generator (ESG), Performance Signal Generator (PSG), or Manufacturing X-series Generator (MXG) models. In general, these instruments have internal DSP functionality that can store waveform ‘symbol’ data (a sequence of IQ samples) loaded from a computer, that

can then be ‘played’ at a sample rate imposed by a local clock. Sequences of symbols are usually repeated indefinitely once the signal generator receives a trigger command, that can be internal or externally generated. The baseband signal is then up-converted using a local LO.

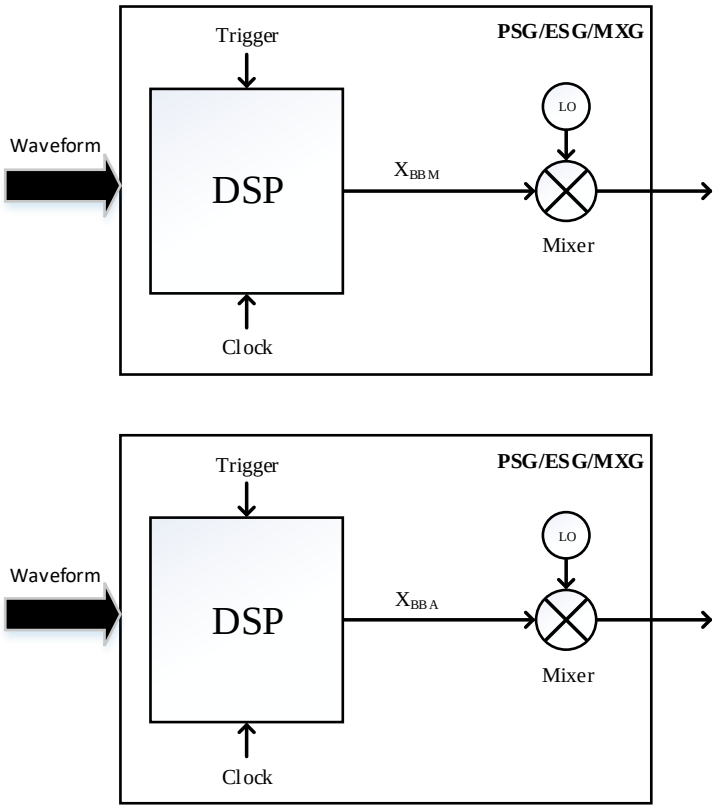


Figure 4.2: The block requirement of two independent input drives to replace conventional measurement setup

4.3 Using ESG Signal Generator as Input Drivers

Taking the block diagram in Figure 4.2 as a reference, a complete independent-source measurement system can be constructed to perform the same operation as mentioned in subsection 4.2.1. There are few approaches that can be considered to perform this solution; the first uses two identical ESG signal generators, for *main* and *auxiliary* input signal injection. A block diagram of this approach is shown in Figure 4.3 below. A 10 MHz reference signal is used to link the 'master' instrument together with its 'slave'. This synchronisation serves to align the local clocks and the local oscillators through the instruments internal phased-lock-loops. The RF output signals generated from signal generators are X_1 and X_2 for *main* and *auxiliary* devices respectively.

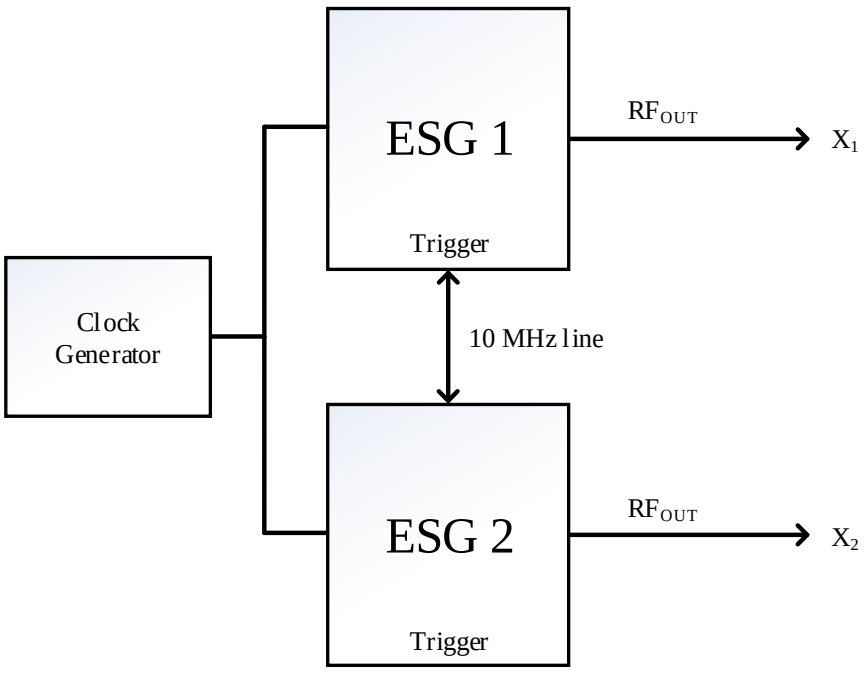


Figure 4.3: Using ESG with external 10MHz reference line

Although this approach is effective in locking frequency and hence relative phase, the solution faces the problem of potentially large phase drift, in the sense that the phase difference between X_1 and X_2 can change slowly over time. If the first measurement records a phase difference $\Delta\emptyset_a$ between the two generators, the same setting will give a phase difference$\Delta\emptyset_b$, as presented in Figure 4.4 below. The difference $\Delta\emptyset_b - \Delta\emptyset_a$ is somewhat instrument and frequency dependent, but is typically in the range of several degrees in a minute, meaning that reasonable phase stability is only achieved for 10s of seconds. This is particularly problematic for the measurements planned here, since it is necessary to firstly establish an optimum relative phase in an initial calibration phase, and then perform a large number of measurements, varying other parameters such as bias, input drive levels, etc, as well as potentially the relative phase itself, either side of this point.

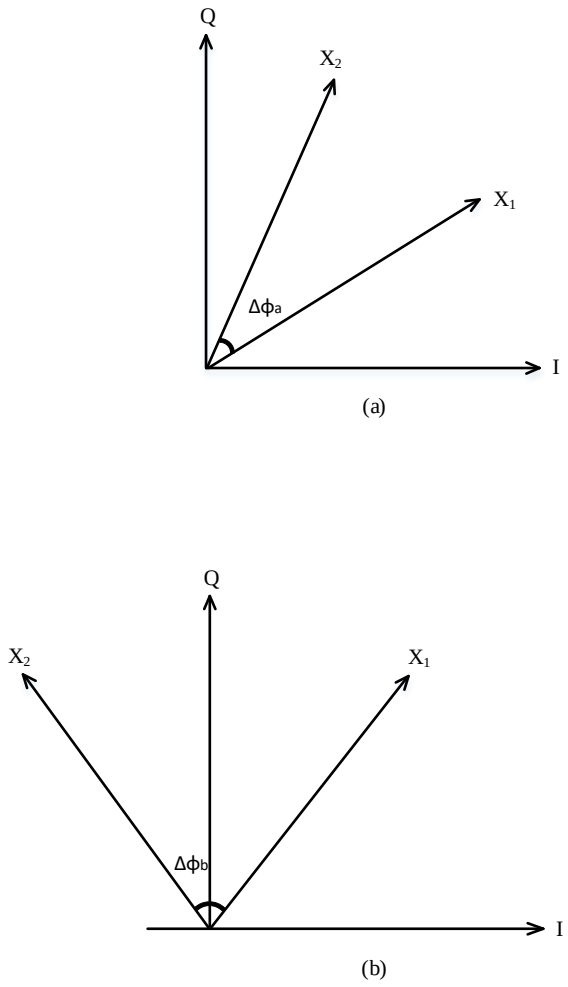


Figure 4.4: Changing of phase over time, resulting in different delta value recorded for several measurements taken

4.4 Using PSG Signal Generators as Input Drivers

The second approach is to use two PSG signal generators to drive *main* and *auxiliary* device inputs. The PSG signal generators used have a special option; UNX (Ultra Low Phase Noise) with an additional reference oscillator bandwidth setting

that can improve phase noise and phase drift. Figure 4.5 depicts the measurement system used in this approach. The PSG signal generators used are also fitted with another special option; HCC and trigger functions. The HCC Option allows the RF phase generated by two instruments to be coherently locked by sharing a common local oscillator (LO), typically using a dedicated LO distribution box. As the same LO is used by both instruments, this approach produced zero relative phase drift over time. There is also a need to share a clock generator and a trigger signal link between both PSGs. The individual reference phases captured by PSG can be checked by connecting both to a Digital Signal Oscilloscope (DSO).

This setup gives very good results for continuous waveform (CW) measurements, while it still raises issues for modulated signal measurements. The reason is related to the way the instruments trigger an oversampled baseband waveform, which means the trigger event will cause the waveform to replay in one of four possible starting quadrants. As a result, the baseband signal may be well aligned, or it may not, in an unpredictable way. One way to overcome this issue is to connect a multi-channel digital oscilloscope to probe the baseband output from each generator and checking for alignment, forcing a re-trigger. Only when the alignment is satisfactory will the measurement be considered as valid. This control must be done using identical cables on both paths, and it also slows down the measurement of a factor that is not predictable a priori.

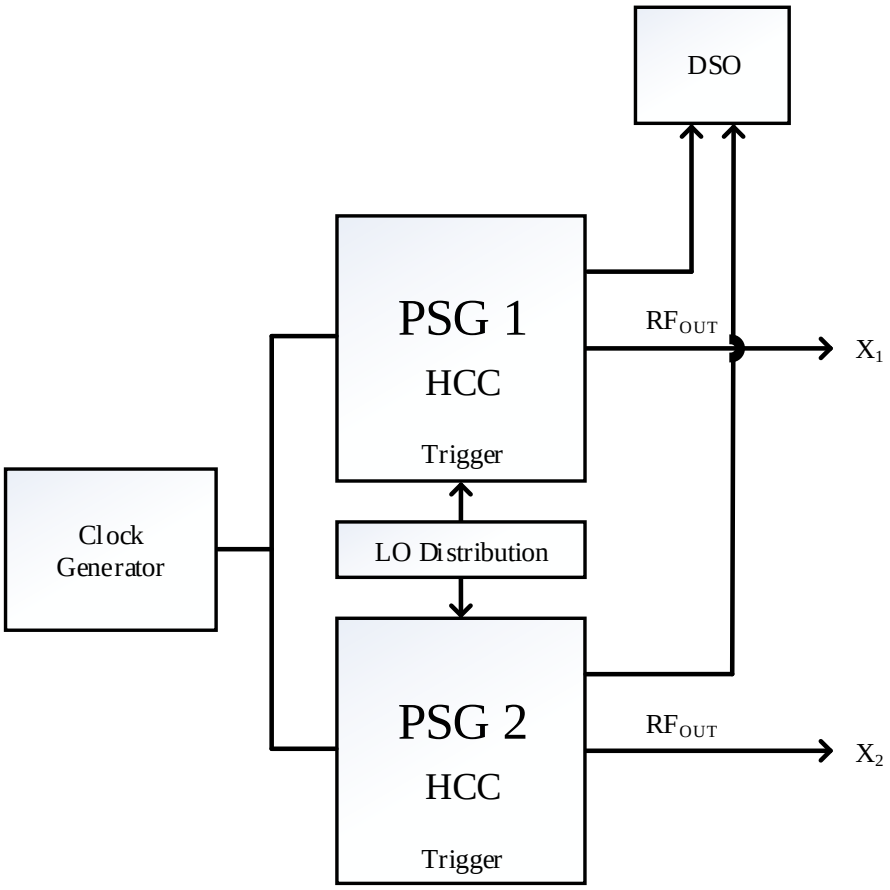


Figure 4.5: Using PSG with HCC function and external LO distribution box

4.5 Using MXG Signal Generators as Input Drivers

The best solution for precise co-phased modulated signal alignment relies on the MXG generators as shown in Figure 4.6. The LO sharing options permits a single LO to be split and fed to both up-converters. This guarantees the phase and frequency coherency. Regarding the baseband trigger, by connecting the EVENT TRIG OUT output of the *main* generator to the BB TRG IN input of the *auxiliary*

generator with a 30 cm coaxial cable (the length that suggested by Keysight to guarantee time alignment), the two generators will automatically align their triggers.

MXG generators are not available at the moment at the CHFE laboratories, but can be loaned from Keysight. For this reason, the PSG setup will be used to test the prototype in CW condition, and when all the measurements and corrections to the hardware are complete, the MXG setup will be loaned to perform modulated signal measurements.

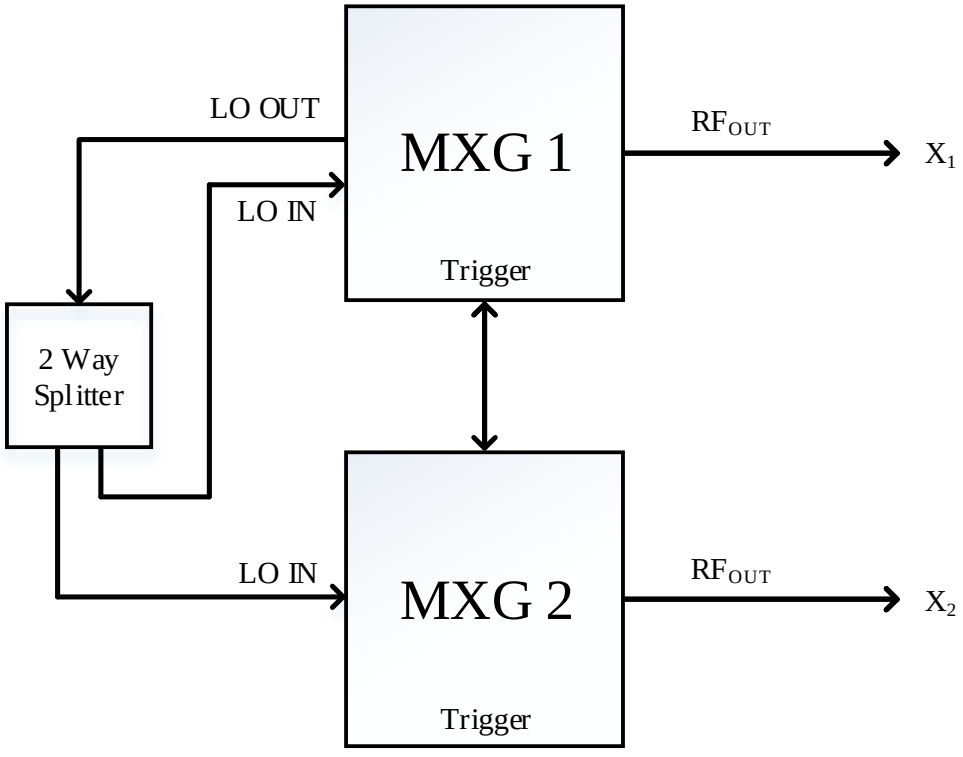


Figure 4.6: Using MXG with two-way splitter

4.6 Conclusion

This chapter reported the measurement system that could be ideally used to test the Doherty PA performance with independent input drives. Three solutions were identified; the first one was using ESG signal generators with a 10MHz reference. This solution has limitations in terms of unacceptable phase drift over the measurement time frame.

The second solution uses more advanced PSG signal generators, linked through an external LO distribution box and a shared baseband clock. This solution gives good frequency and phase stability, so it can be used for CW measurements, but it has poor baseband time alignment and so is unsuitable for modulated measurements. The third solution uses more modern MXG signal generators with a shared LO capability and internal baseband re-alignment functionality, giving good RF and baseband alignment. However, this setup will be considered in the future work due to the current unavailability of the MXG instruments.

CHAPTER 5

DOHERTY PROROTYPE 1: DESIGN, SIMULATION, BUILD AND TEST

5.1 Overview

In the previous chapter, the possible measurement approaches to test a dual, independent input Doherty PA were discussed. An independent input approach was chosen over a conventional passive power splitting arrangement typically used in Doherty structures, due to the ability to correct any dynamic phase misalignment that can exist between *main* and *auxiliary* devices. Individual instrument constraints also contribute as a strong factor in the choice of this approach.

The first objective of this chapter is to discuss an initial, first-pass design of a prototype Doherty PA. This documents the first attempt to become familiar with Doherty PA, and to conduct a design in a conventional way. The exposure to Applied Wave Research Microwave Office (AWR-MWO) software for the simulation activities and generating layout is also part of the early learning process. The second objective of this chapter is to discuss Doherty PA measurement using the dual input drive approach previously described in Chapter 4.

This chapter is organised by firstly discussing the Doherty PA schematic design, which involves the design steps including the choice of lumped components

used. Following this, further discussion on generating the layout to develop a suitable and reliable design with a fabricated fixture is done presented. Later, this chapter covers the measurement activities of Doherty PA to confirm desired performance. Finally, in the conclusion section, the ability of this prototype to function as Doherty PA architecture is clarified, as well as discussion of the factors involved.

5.2 Design Simulation in AWR Environment

The first design prototype used a 6-port model of a 10W transistor made by CREE Inc. (now Wolfspeed), with simulation activities conducted in the AWR MWO environment. The basic schematic of the DPA design can be found in Figure 5.1. The prototype is designed part by part, beginning with *main* PA section. The matching network is designed to match the device at 2 GHz, and is added to the schematic before whole *main* device schematic is copied to build the *auxiliary* PA part, followed by adding transformer transmission line as the impedance inverter and then final output matching network at the end to transform a load of 50 Ohms to the required Doherty output impedance. The series inductor and capacitor are a part of matching network as well.

In this design, large capacitance (1nF) DC blocks are placed at both inputs to prevent input bias passing back to the sources, whilst offering low impedance to RF signals. RF chokes are placed between the DC bias power supplies and the biasing sections to create a condition of low impedance for DC and high impedance path for

RF, and prevent RF signals within the circuit being influenced by the low impedance of DC supplies.

Meanwhile, impedance matching networks are needed to transform source impedances to the conjugates of the devices input impedance, and the load impedance to that required for Doherty action and for maximum power transfer. It should be noted that, although a concern in a commercial realisation, in this design, matching for wide bandwidth is not the aim.

Following an initial design, components that make significant changes to the performance of total efficiency, output power, current and voltage are identified, and tuned accordingly to get the desired result.

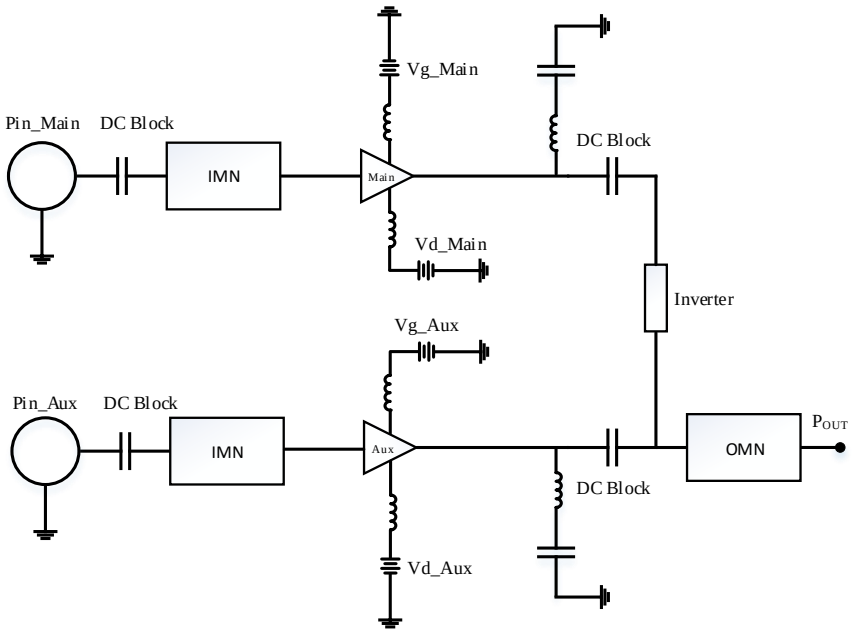


Figure 5.1: Schematic block diagram of first DPA prototype, simulated in AWR Microwave Office environment

The *main* amplifier is first simulated, followed by the *auxiliary* amplifier. Later the impedance inverter is added to complete Doherty PA architecture. The overall simulated performance of first DPA prototype can be seen in Figure 5.2 which presents the efficiency and output power achieved as a function of input power, and at a carrier frequency of 2 GHz. As part of the design process, the input power applied to the *main* and *auxiliary* devices is varied from their nominal values and any changes in performance.

The first step in the analysis involved simply observing how the *main* device behaves with the *auxiliary* device completely off throughout the complete input power sweep range, thus establishing that the Doherty is working as expected in the low-power region of operation. Setting the gate voltage to -2.7V and the *auxiliary* device biased completely off, resulting 52% of maximum efficiency. During the power sweep, the gain reaches a maximum of 15 dB and a maximum output power of 40 dBm is achieved. The amplifier begins to saturate however at an input power approximately -3 dBm, marking the transition point. Notice that the efficiency continues to increase beyond this point, but this is expected as the amplifier compresses.

The investigation continued by 'switching-ON' the *auxiliary* device by applying a gate voltage of to -3.2V, and maintaining the same drain voltage as *main* device 28V over the same input power sweep, resulting the same behaviour as *main* amplifier. At this point, it was concluded that by following a classical PA design approach, the presence of *auxiliary* device did not bring about obvious Doherty behaviour in this architecture. After some time experimenting within the simulation

environment to establish why this would be, it was decided to proceed with the fabrication of a prototype to try and provide empirical data.

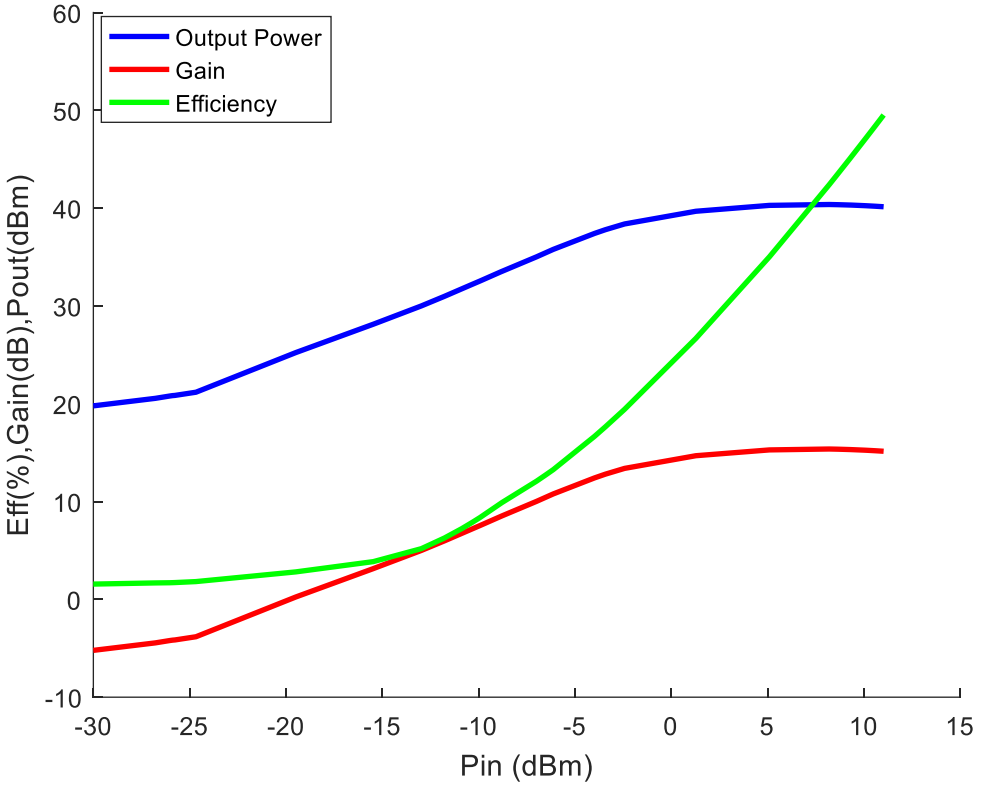


Figure 5.2: Efficiency, output power and gain in corresponding to input power

5.3 Layout and Fabrication

The design flow continued with the final simulation stage, which is transferring the schematic design into a layout for fabrication. Generating a correct layout is critical as it will influence the fabrication process and final fixture. Thus, a number of factors are taken into consideration when generating the layout:

- The size of the device itself must conform to the actual size of the physical transistor. Details of the size can be found in datasheet, Appendix A. The device's size is not merely length and width, but also its depth to fit it in the slot. The device should not sit too deeply from the fixture's surface because it will cause bending up on the package leads, or sit too high as this will cause bending down of the package leads and a poor launch.
- The size of the components used is identified, and in this case, size 0603 capacitors and inductors are used. Therefore, a fitted gap is created in the layout - larger gaps cause difficulties during soldering process, whilst smaller gap will overlap the original transmission line of the design.
- Providing good grounding around the transmission lines. Since the design has two independent inputs, thus good isolation is important to prevent mixed signals, so grounding structures between the two input paths are important.
- Providing some flexibility to tune the component placement - a component's position in schematic, layout and fabricated fixture can be expected to change.
- Providing enough space to place wires for connecting the biasing supply with power supply.

- Including real component's physical model in the layout simulation to ensure the correct dimension size and performance.

Figure 5.3 presents the final layout design after considering the points mentioned above, which has been manually generated from original schematic. Some re-arrangement is done to make this design neat and for ease of components placement later during fabrication.

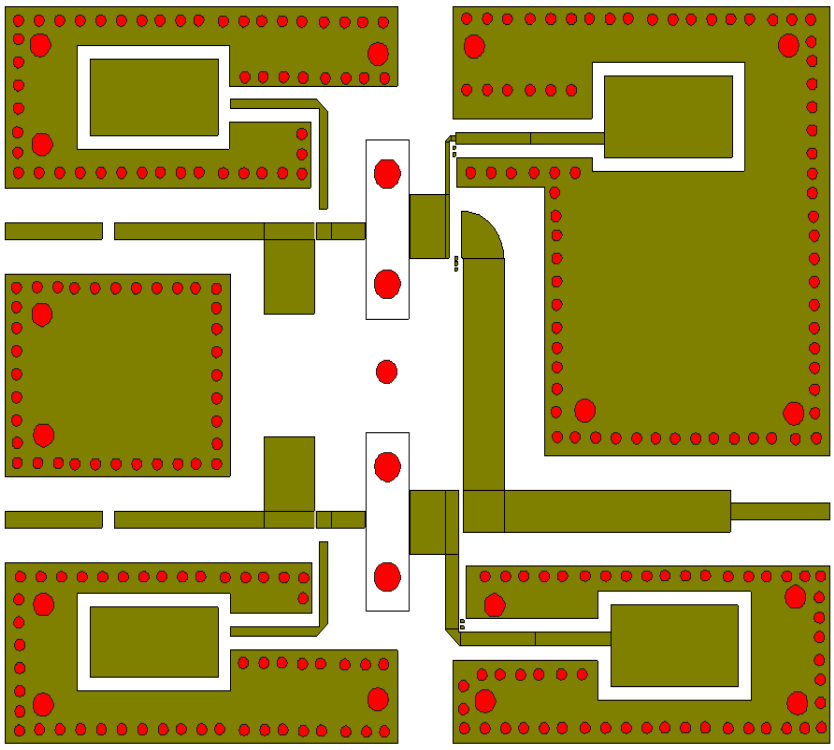


Figure 5.3: Layout of first prototype, green colour represent copper coated while round shape in red portray the via and fixing holes

The fabrication process uses RT/Duroid 5880 laminate from Rogers Corporation with 100 X 75mm size, and the board is mounted on a copper plate using screws for proper grounding as shown in Figure 5.4. The SMA connector is embedded at the edge of copper plate to connect both RF and DC instruments through appropriate cables. TL1 and TL2 represent the λ/4 line to allow the impedance transformation to happen.

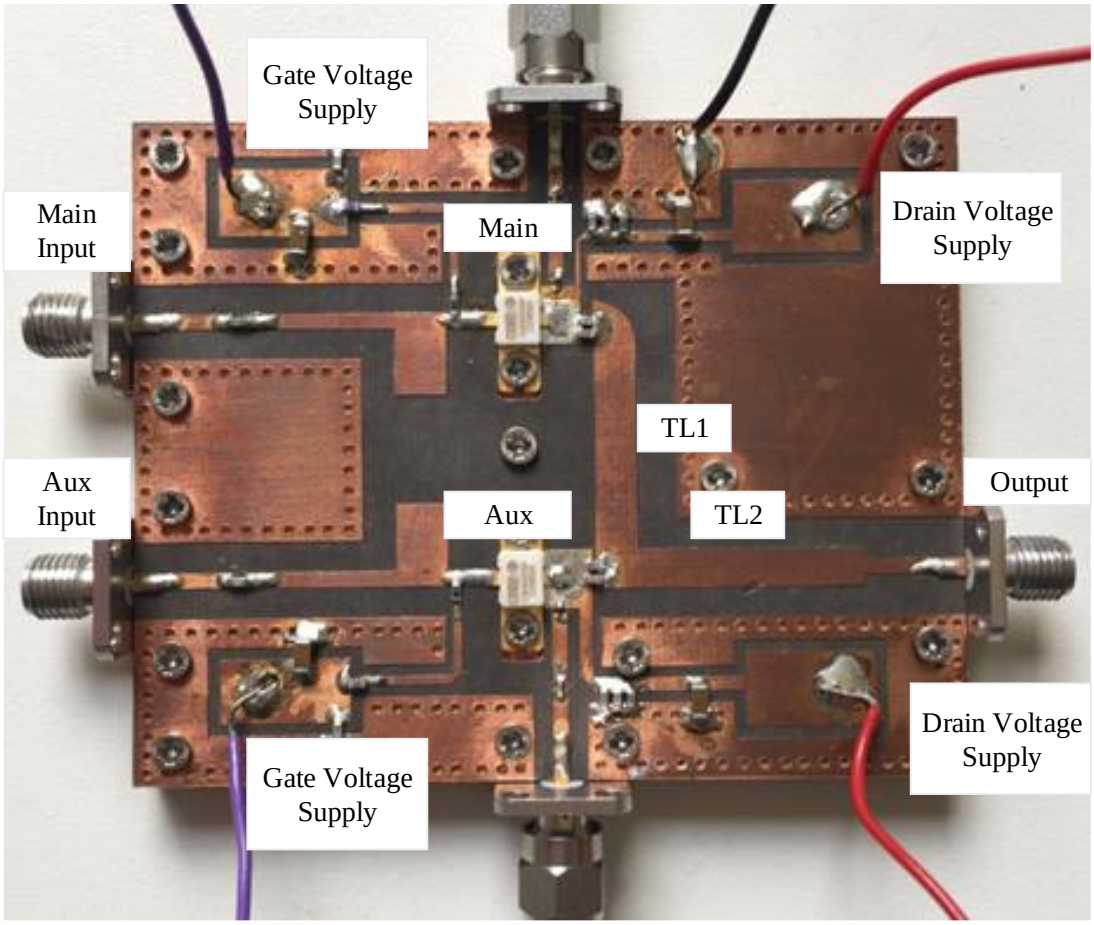


Figure 5.4: Fixture of first prototype which fabricated on RT/Duroid 5880 laminate and mounted on copper plate

5.4 Measurement Results and Discussion

5.4.1 Measurement Setup Diagram

As discussed detail in Chapter 4, the ability to control phase coherency is the main reason why an independent input source approach is selected to measure the Doherty PA. Figure 5.5 below shows the measurement system setup for that purpose. Two signal generators (model E8267D and E4421B) are used to inject the signals for *main* and *auxiliary* device respectively. The signal generators are then connected to drive amplifiers and linked to attenuator before passing to the devices. A dual channel power supply is used for gate biasing of *main* and *auxiliary* devices. It is important to use the supply that has the capability to changing the voltage precisely as achieving the correct I_{dq} is necessary for the overall Doherty PA performance. In this system, the drain voltage is fixed to 28V for both devices. The output power is then recorded using a power meter.

The presence of input and output attenuators, which are not included in the Figure 5.5, act as a protection to equipment, as well as to the devices themselves. It is important to take such precautions because of the cost involved to build the whole setup. For that matter, the maximum power that can be tolerated by each piece of equipment device used needs to be noted before deciding upon suitable values of attenuator to be used.

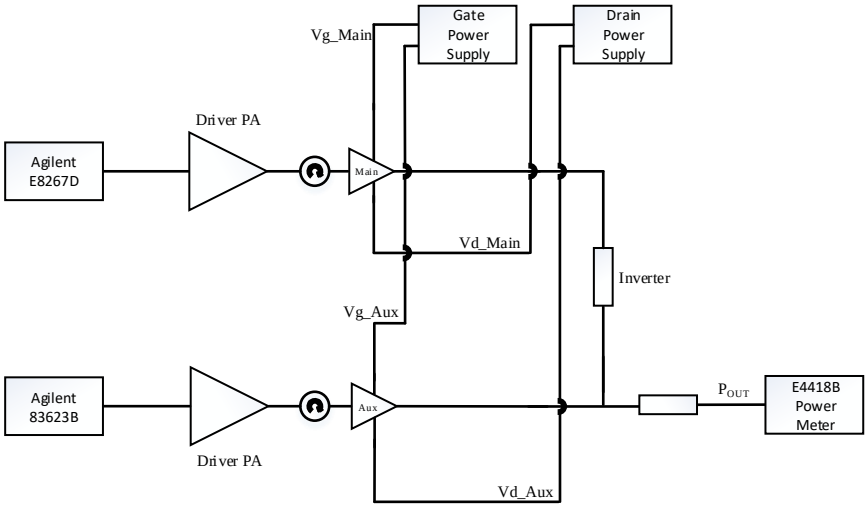


Figure 5.5: Independent sources measurement setup diagram

5.4.2 Power Calibration

The measurement process begins with power calibration to ensure the existing measurement system is able to produce accurate results. It is also to ensure that the drive power is sufficient and doesn't compress. Figure 5.6 depicts the setup of this activity, which consists of signal generators linked to driver amplifiers, which are then connected via a 3 ports isolator to the device. The reflected port of the isolator is terminated to 50Ω load, so any power reflected from the device will be safely dissipated. The output port of the isolators are then connected the Device Under Test (DUT), which in this case is the *main* and *auxiliary* devices of the prototype DPA. The power is calibrated at the input plane of the DUT, by attaching this point of the system to a calibrated and suitably attenuated power meter, and then running a power sweep, and recording the values, as shown in Figure 5.7.

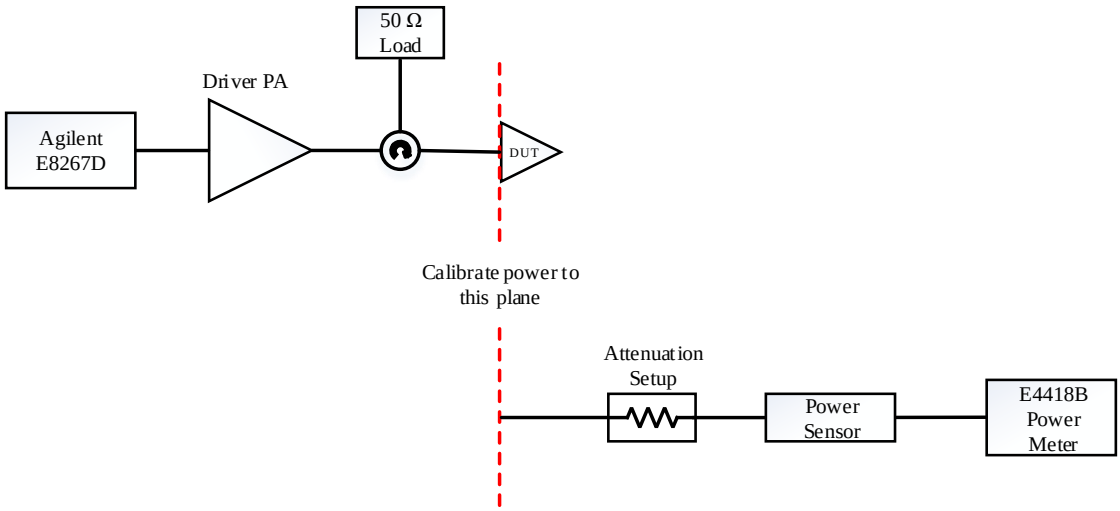


Figure 5.6: Setup of power measurement calibration to reference plane

The actual power at calibration plane can be calculated by adding the attenuation setup value to the measured power sensor value. The linear result shown in Figure 5.7 represents the output power captured by output power meter is in agreement with the input power from signal generator.

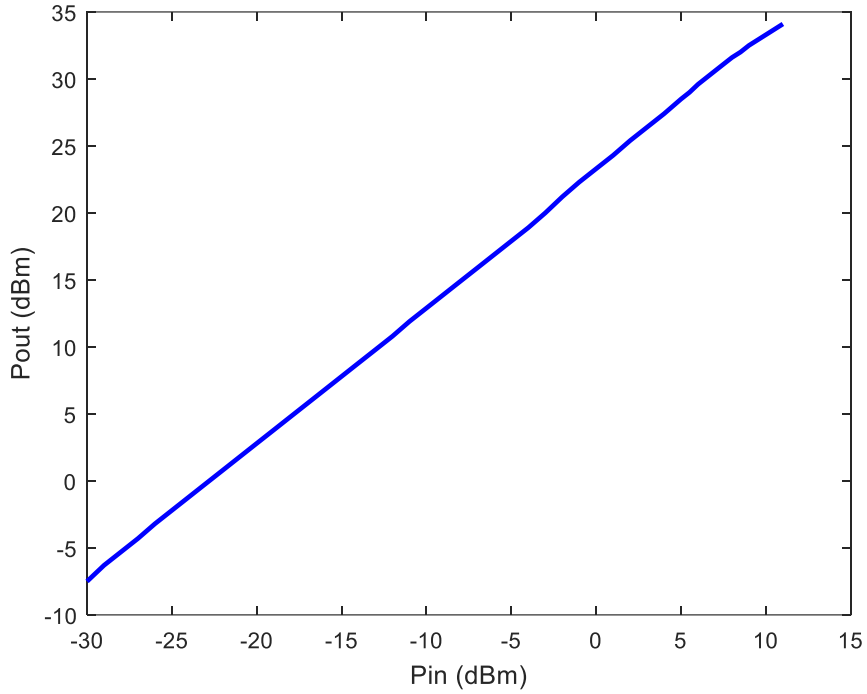


Figure 5.7: The linearity of power taken from power meter, shows that output power is corresponding to the input power with a 20 dB offset established by the power attenuator attached to the power meter

5.4.3 Manual Test of Relative Input Phase

The relative input phase between *main* and *auxiliary* excitations is a critical parameter as it ensures the correct Doherty action and summation of power at the output of the structure. Inaccurate results influenced by non-coherent relative input phase can easily result if this parameter is not considered carefully. Before measurements, a relative input phase test is done manually to ensure the phases of

two signal generators are i) completely locked and stable over time and ii) controllable.

Both *main* and *auxiliary* devices are biased, and the input power is fixed at 3dBm, where the interaction is maximum. Later, the phase of *auxiliary* device excitation is varied from 0 degree to 360 degrees while readings of the DPA output power is taken. The plot in Figure 5.8 below shows clearly the phase that results in maximum output power. Thus, the phase of 200 degrees is taken as relative input phase required for this prototype and measurement arrangement, and this was set in the *auxiliary* signal generator. To establish the phase coherence was stable over time, the arrangement was left for 1 hour.

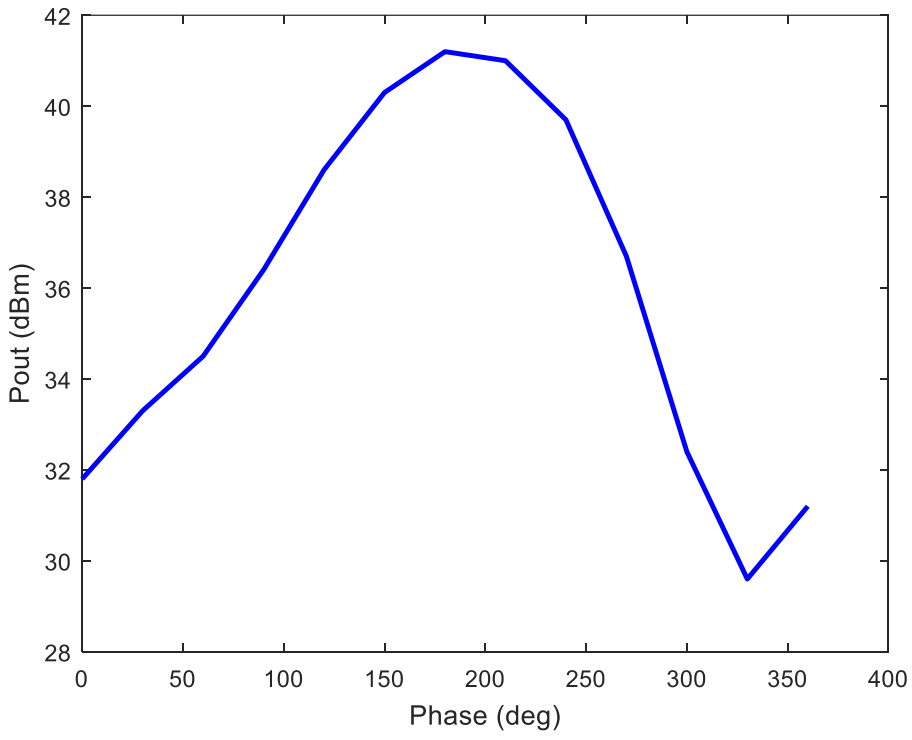


Figure 5.8: Maximum output power can be seen to occur clearly at the optimum relative phase point.

5.4.4 *Main* and *Auxiliary* Device Test

Biasing voltages were first established prior to any RF measurement. This is important to ensure the correct quiescent current is achieved for each device, according to simulations. Some issues where found where the pinch-off value shown in datasheet was different to that observed in real measurement. In this case, a gate voltage of -2.77V was needed to bias the *main* transistor to class-B, and -3.4V was required to pinch it off. However, these values may vary slightly for different transistors used. A fixed value of 28V was supplied to both *main* and *auxiliary* transistors as drain supply voltage. The operating frequency was set to 2 GHz for the whole measurement activity.

This first Doherty PA prototype was measured manually. It began with the *main* PA measurement part, where the *auxiliary* amplifier is biased completely-off, as in initial simulation. The performance of the *main* part of the DPA in Figure 5.9 shows good performance, and generally in good agreement with initial simulation, with efficiency increasing to a maximum of approximately 45% at P_{in} = +4dBm, where there is clear saturation. The gain shows a classical expansion followed by compression associated with class-AB bias, and is on average 13 dB across the dynamic range, peaking at +14 dBm at P_{in} = -14dBm, before decreasing with ongoing saturation. The power linearity is linear up to P_{in} = -14dBm, where there is an inflection related to the onset of compression. The measured DC current is also revealing and shows an initial reduction with a minimum at P_{in}=-14dBm, followed by an expansion as the device compresses. This is also symptomatic of a class-B bias condition as the clipping of the lower part of the sinusoidal current waveform causes the average current (DC) to decrease. As the input is driven further, the top part of

the current waveform compresses, and this raises the average current again increases. As drive continues, the current waveform becomes symmetrically compressed, and the average current tends towards a class-A quiescent bias condition.

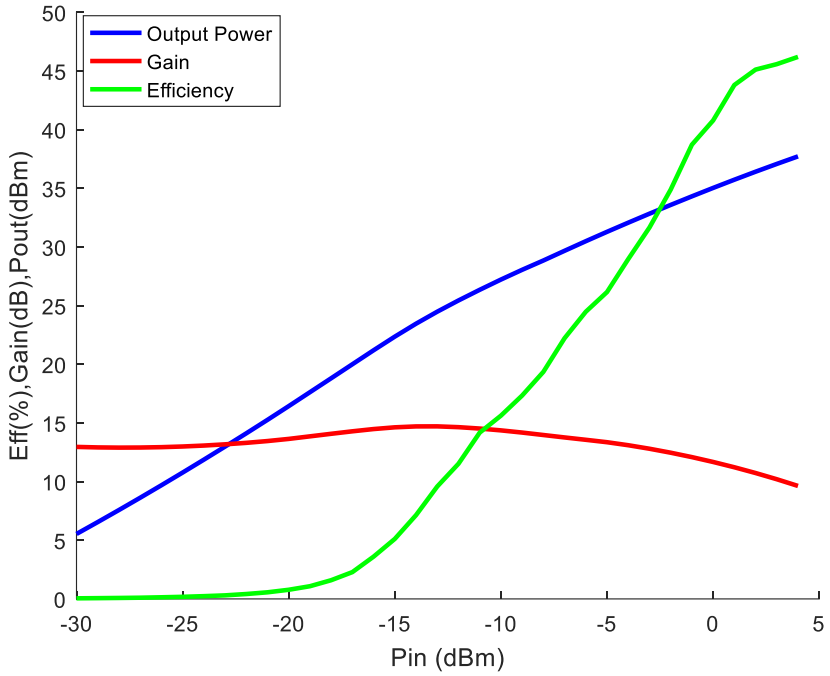


Figure 5.9: Efficiency, output power and gain in corresponding to input power for *main* amplifier.

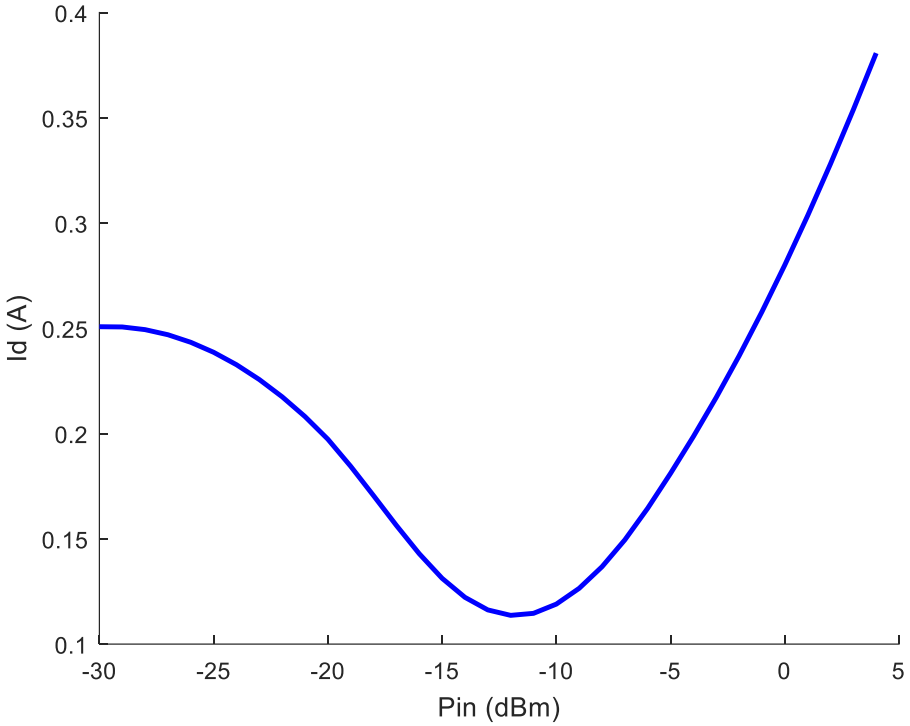


Figure 5.10: Current behaviour in corresponding to input voltage, expected to be linear when *auxiliary* amplifier is off.

The measurements continued with testing the *main* PA at other frequencies to check for changes in output performances. In addition to 2 GHz, two additional operating frequencies were chosen for this experiment - 1.8 GHz and 1.9 GHz, and the results can be seen in Figure 5.11 below. From the results presented, it is clear that the *main* amplifier's overall performance in terms of efficiency and gain is better at 2 GHz. Although the peak power is better at 1.9 GHz, the efficiency is significantly degraded at this frequency.

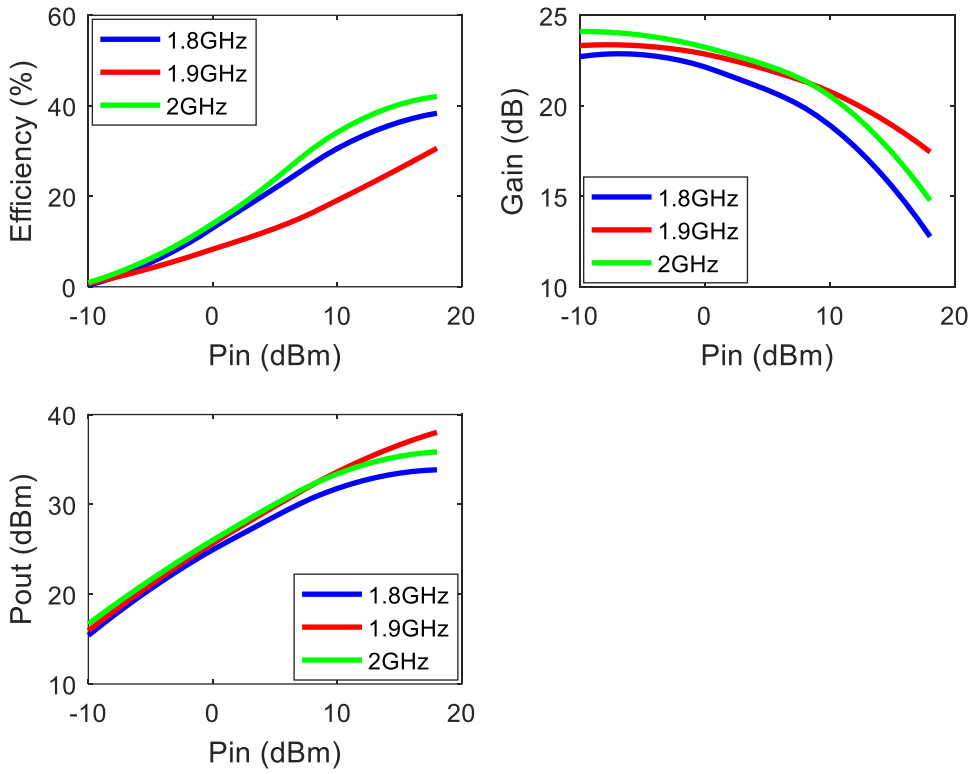


Figure 5.11: Overall performance comparison of the *main* amplifier at different frequencies – 1.8, 1.9 and 2 GHz, sweeping the input power from -10 dBm to +20 dBm in separate measurement session.

The measurement is then continued with the *auxiliary* amplifier active, while maintaining the *main* device to be active for the whole measurement. The gate bias of the *auxiliary* device is set to -2.82V and the relative phase to 200 degree (as established from earlier measurements). As this is a classical arrangement, the input drive powers for both devices are set to be same. The efficiency plateau indicates 25% of average efficiency which is 9% higher than the peak efficiency. Whilst gain is 30 dB which is a bit higher as expected, and the presence of non-linearity power in

this device leads to these abnormalities as well. The gain should be flat to meet the Doherty behaviour. The output power at the transition point (Pin=-14 dBm) in Figure 5.9 is ~22dBm, but it is more like ~30 dBm in Figure 5.12, means that the *auxiliary* device is contributing more power at the transition point, eventhough the *auxiliary* device is completely off. The collapse in efficiency, power and gain after the transition point is symptomatic of the wrong phase being used. It is admitted that the optimum phase sometimes drifted during the measurement.

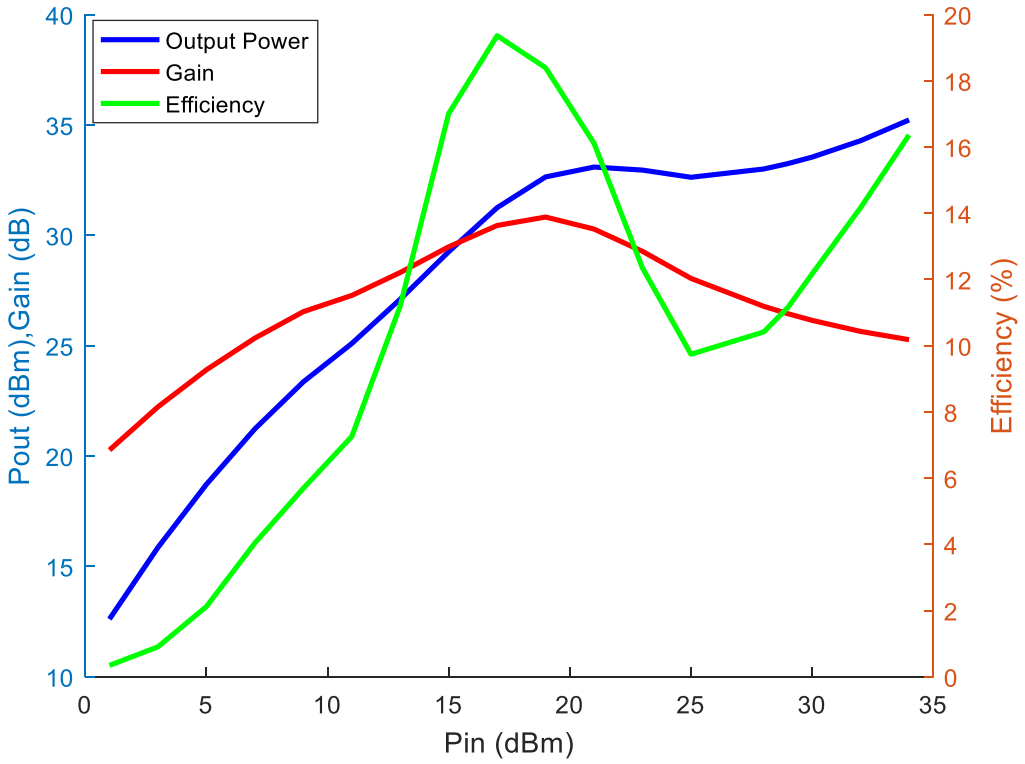


Figure 5.12: Overall efficiency, output power and gain in corresponding to input power

Currents generated from both devices are drawn in Figure 5.13. The *auxiliary* current started to operate at 15 dBm. Whilst *main* current is exponentially increased, meeting the same maximum current of 0.32A.

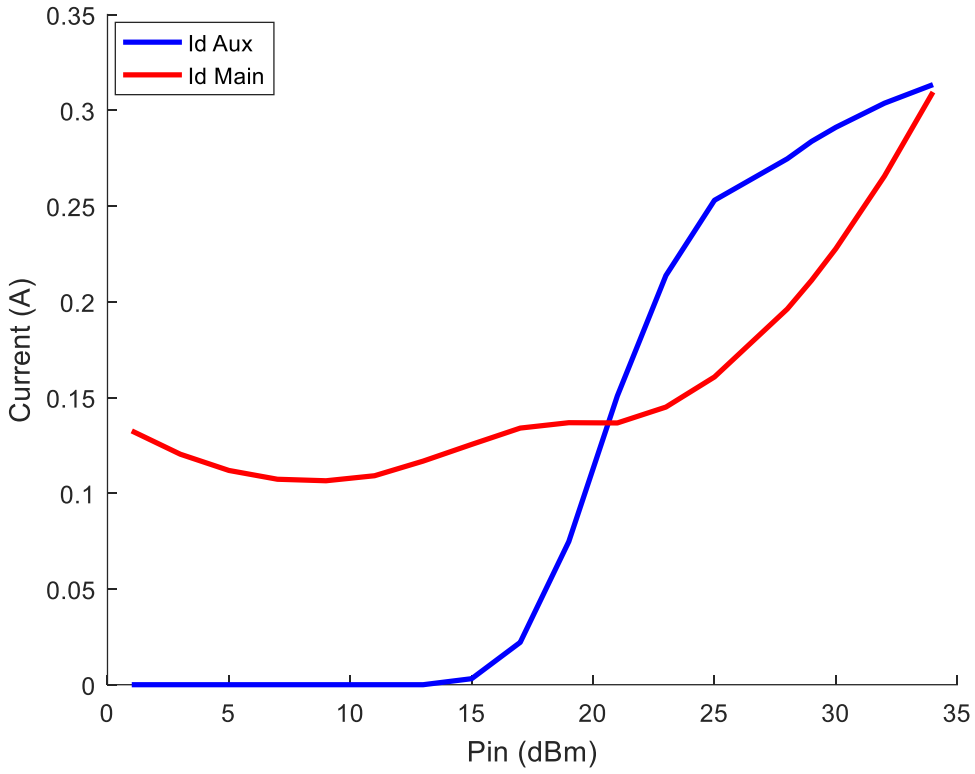


Figure 5.13: Drain current for *main* and *auxiliary* devices in corresponding to optimised input power.

The inconsistency input power axes in Figure 5.9 and Figure 5.12 is because of the two input drive used in this measurement, therefore they are optimised manually to meet both device requirements. For every point of input drive recorded, the points where they're similar are taken to represent input power.

5.5 Conclusion

Based on the results discussed above, it is clear that this first prototype did not behave as Doherty PA architecture. It is thought that one of the main factors that led to this poor performance was that the prototype design followed a traditional PA design approach, and did not follow a logical waveform-engineered design flow. In the latter, the design should start with investigation of the GaN device itself to ensure the device's characteristics and performance agree with the model used. Thus, it is important to know the limitations of the device before taking further steps to form Doherty PA architecture.

The second factor identified was the likelihood of incoherent phase between two signal generators, which affected the whole measurement activity. When the same test was done repeatedly, the phase recorded was inconsistent. During investigative measurements, the relative phase was observed to drift by up to 50 degrees. Thus, it is thought that inaccurate input phase alignment during measurements has had a high impact to the measured Doherty performance. As a result, the measurement setup does not guarantee a consistent relative phase relationship during measurements, even though it was indicated that the phase was locked.

Even though the prototype did not function as hoped, the design, simulation, fabrication and measurement activities associated with this prototype were a valuable learning activity before producing a second, optimised prototype through a more robust design approach, as discussed in the next chapter.

CHAPTER 6

DOHERTY POWER AMPLIFIER SIMULATION AND LINEARISABILITY INVESTIGATION

6.1 Overview

The first Doherty amplifier design prototype developed in the AWR Microwave Office environment is discussed in Chapter 5. Although the results achieved were not as expected, the process formed a very important stage in the early introductory process of Doherty amplifier design, and the realisation that Doherty design was not a simple task, and actually needs careful thought and an optimised design approach. Several factors that caused the poor performance were clearly identified at the end of the last chapter.

This chapter will discuss the second attempt to design a Doherty, taking into consideration all of the failure related factors identified in the first design. The other difference is that this new work is designed and simulated in the Keysight ADS environment, but using the same device model. The design flow is discussed in detail in this chapter, from device characterization through to producing a complete Doherty architecture. In addition to this, the effect of adaptive bias and input attenuation methods of controlling the *auxiliary* device conduction, and their impact on efficiency performance is also further discussed in this chapter. It was important to revisit these two implementations as it was necessary to identify the key

parameters involved in developing these techniques further. Later, this chapter will cover the *linearisability* of a Doherty amplifier, and how this can be improved using this type of function.

This chapter is organised as follows; firstly, a discussion of effects that a device's parasitic components have on high frequency design are presented, as this is a key factor in achieving good Doherty operation. Secondly, a more detailed Doherty design-flow is presented, which includes load modulation, as well as individual analysis of *main* and *auxiliary* amplifiers, and how they are then combined to form a complete Doherty PA. As identified in earlier chapters, the relative input phase between *main* and *auxiliary* device excitation is a critical parameter that needs serious consideration, so is also included. Finally, the bias adaption and input attenuation approaches are discussed, as well as a new and novel approach to engineer *linearisability* through bias adaption, before a conclusion at the end of the chapter.

6.2 Parasitic Component Effects on High Frequency Device

Although it is acknowledged that some device parasitic effects, such as input and output capacitance are dynamic in nature, and related for example to terminal voltages, these effects, for this work are considered to be small, and so the discussions around device parasitic components in this subchapter include static, passive component only.

In high frequency design, the frequency-dependent behaviour of passive components is very important. Generically, we know that the lumped components are often used in amplifier design, which includes resistors, inductors and capacitors which are reactive, and as a consequence, have impedance that changes in response to changing frequency. The reactance can be simply calculated using equation (7) and (8) for capacitor and inductor respectively.

$$X_C = \frac{1}{2\pi f C} \tag{7}$$

$$X_L = 2\pi f L \tag{8}$$

Component parasitics are not only related to the electronic component value itself, but can also be the component's size, shape, non-ideal material used to construct the component or electromagnetic coupling between parts of the component that are in proximity to each other

When a transistor model is operated at low frequencies (<100 MHz for example), the intrinsic parasitic reactive components have a much reduced impact on results, and the 'core', transconductive behaviour of the model will be revealed. Reactive parasitic will only begin to have an effect when the operational frequency increases, when the transistor departs from its "ideal" transconductive behaviour. However, the development of an ideal device model in Chapter 3 ignores the parasitic existence because it is used to develop a design at low frequency [95], [96].

Although reducing frequency of operation to progress a design and, in this case, to identify fundamental Doherty behaviour is a valid and valuable approach, it

is also a fact that in a realistic design, the presence of parasitic capacitance and inductance at the input and output of a device needs to be accommodated at RF frequencies, otherwise these will cause mismatch and stability issues at high frequency.

6.2.1 Parasitic Components in FET

Figure 6.1 shows a schematic of a generic FET that consists of current generator (I_{ds}) surrounded by various parasitic elements. At low frequencies, the reactive components can be ignored, however, the resistive components remain and are frequency independent. The parasitic components are not ignored when the DC simulation is run. When we reduce the impact of the reactive elements (as detail discussed in 6.2), their influence decrease as their reactance changes with frequency. For DC, all of the inductors have an impedance of 0Ω while the capacitors have very high impedance, thus we can ignore them at low frequency. The reactance presented by the intrinsic capacitances C_{ds}, C_{gs} and C_{gd} vary with frequency and affect the whole performance of an amplifier when the frequency increases.

The de-embedding network typically used to observe intrinsic current generator plane waveforms inside the Wolfspeed device is given in Figure 6.2 and shows the positive-valued significant intrinsic components of the GaN device (before the central current probe) followed by a mirror-image negative-valued de-embedding components (after the current probe). Importantly, this positive-negative network exploits the ability to have negative capacitance, resistance and inductance in the simulation environment, and provides a way to access current generator voltage and

current whilst having no net impact on the model behaviour at elevated frequencies, which is exploited when running load-pull simulations which are discussed in 6.3.1. Table 3 shows the value of each component in the network. Remember that Figure 6.1 represents the generic FET transistor package cited from literature [97], hence it does not specifically portray the FET shown in Figure 6.2, that we used in this research work. For a simple mapping of these two networks, we can refer to the mirror-image negative-valued (after the current probe) of Figure 6.1. The C_{ds} in specific network represent the C_{ds} in generic network, Lbond and Rbond refers to Ld and Rd, C_{pad1} represent C_{padi}, C_{pad2} represent C_{pda}, while L_{pad1}, R_{pad1}, L_{pad2}, R_{pad2} refer to inductor, resistor and capacitor at the tab side of transistor itself.

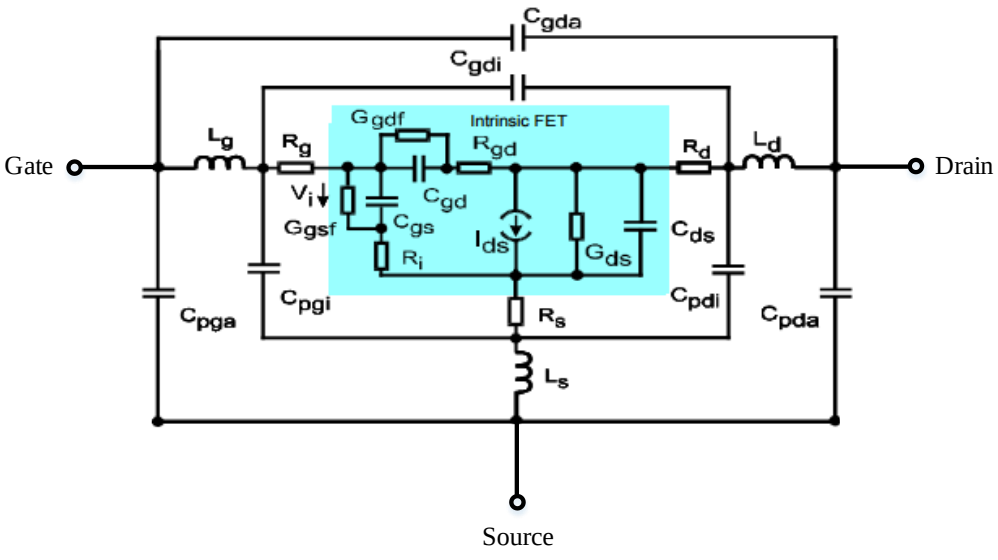


Figure 6.1: Generic FET transistor package [97]

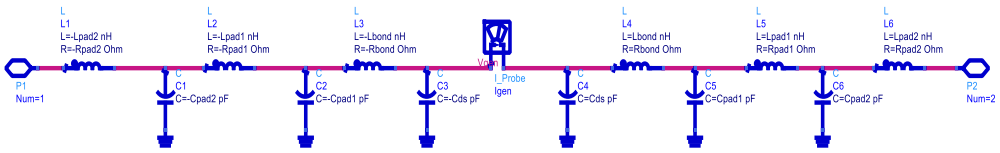


Figure 6.2: De-embedding network of Wolfspeed device used in the whole simulations.

Table 3: Value of each component in de-embedding network

Variables	**Value**
L_{pad1}	0.03nH
L_{pad2}	0.32nH
R_{pad1}	1.055Ω
R_{pad2}	0.11Ω
C_{pad1}	0.48pF
C_{pad2}	0.48pF

6.3 An Improved Design Flow Chart

Doherty amplifier design should firstly begin with load-pull simulation using, in this case, a modified built-in load-pull template within the ADS simulation environment. The importance of load-pull simulation is to identify a device's true response to the different load impedances it may experience in an actual amplifier environment. Importantly, in this design the load-pull template offers the ability to fully de-embed parasitic effects and to shift the measurement reference plane to the intrinsic current generator plane (CGP) reference, instead of the package plane. This is critical as it allows design to happen at the same plane that DC-IV data is measured, and hence RF voltage and current waveforms can be used and plotted against each other to define dynamic load-lines, that, when overlaid on DC-IV data, show meaningful device boundary interaction, for example interaction with the knee, pinch-off and saturation regions of the IV plane.

Following load-pull simulations, an individual *main* amplifier design continues using class-AB biased device followed by a similar individual *auxiliary* amplifier design in class-C bias. Later, the combining output impedance transformer is connected to enable load modulation and efficiency enhancement. A delay line is also added in the *auxiliary* path to compensate the phase generated from *main* amplifier path through the inverting transformer. A complete flow chart of design activities is shown in Figure 6.3 below. Each stage of the design mentioned above is discussed in detail below. This prototype is designed using the same GaN Wolfspeed 10W Field Effect Transistor (FET) model, CGH40010F.

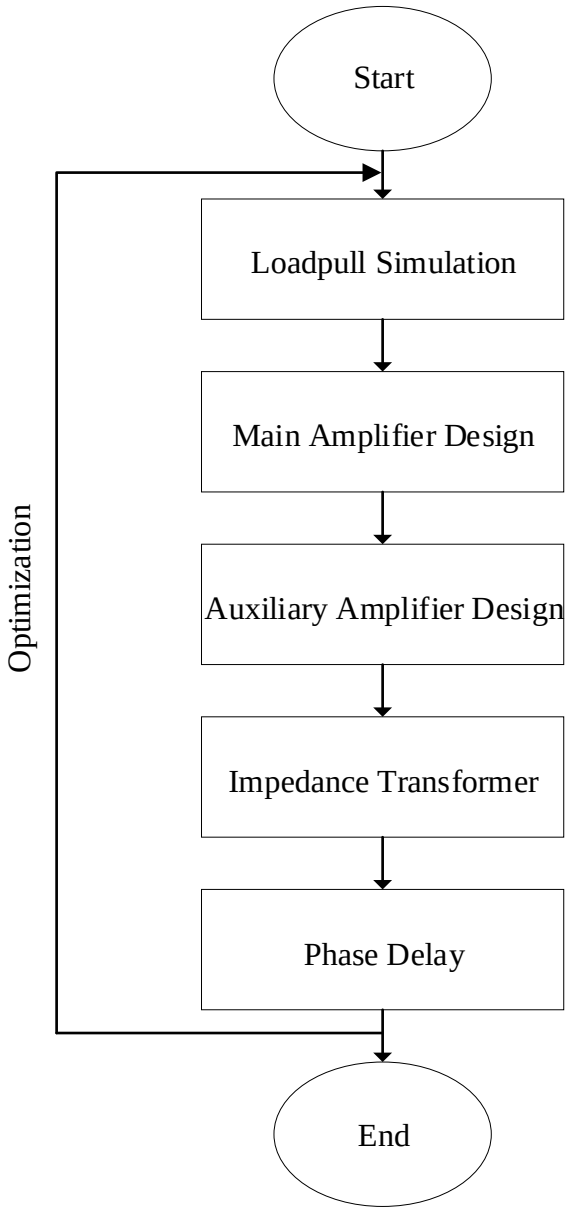


Figure 6.3: Complete Doherty amplifier design flow chart

6.3.1 Load pull Simulation

Generally, load pull simulation is used to determine the maximum output power, gain or efficiency at given load impedance, which are plotted on a set of contours in the smith chart. That impedance will be the actual impedance seen by a device in amplifier design. In this work, the load pull simulation is done using built in Load-pull Instrument in the ADS environment, as shown in Figure 6.4. The Load-pull instrument contains a load-pull tuner that sweeps the load reflection coefficient while the available source power of a single tone is held constant. This tool is connected to the device and the addition of a de-embedding network for this device which allows characterization at both the current generator (CGP) and package plane. The CGP here refers to the intrinsic plane within the transistor itself, while package plane behaviour will include the transistor and its parasitic components. The load tuner in the load pull will vary the load impedance presented to the device. It is based on harmonic balance simulation.

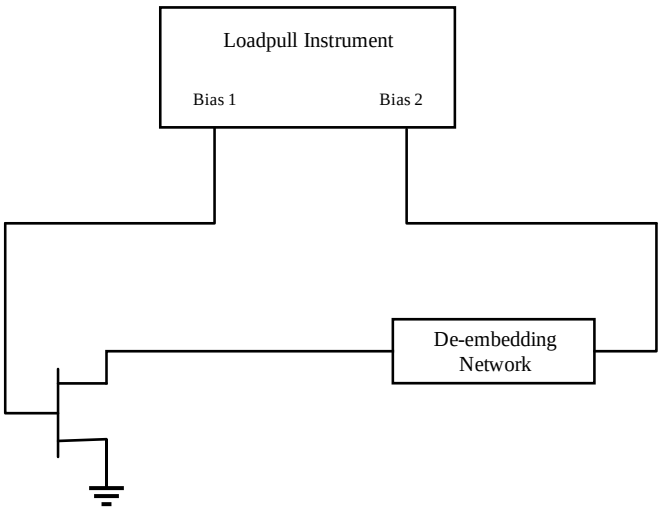


Figure 6.4: Loadpull system configuration, the Loadpull Instrument is a ready tool that can be found in ADS software.

The Wolfspeed device model used has the advantage of having built-in de-embedding functionality that gives access to current and voltage waveforms at the transistor's CGP, directly from load-pull simulation. However, as this is a relatively new feature in this model, it was decided to include the traditional de-embedding network approach in Figure 6.2 in the analysis and to compare the results of both. Figure 6.5 and Figure 6.6 below show the dynamic load-lines and voltage and current waveforms that form them respectively, for a class-B bias, for the two de-embedding approaches. Encouragingly, it can be seen that current and voltage behaviour is very similar for both approaches. The difference lies in the off-state part of the waveforms, where there is visibly more displacement current due to the dynamic nature of the output capacitance not being fully de-embedded by the simple static de-embedding approach.

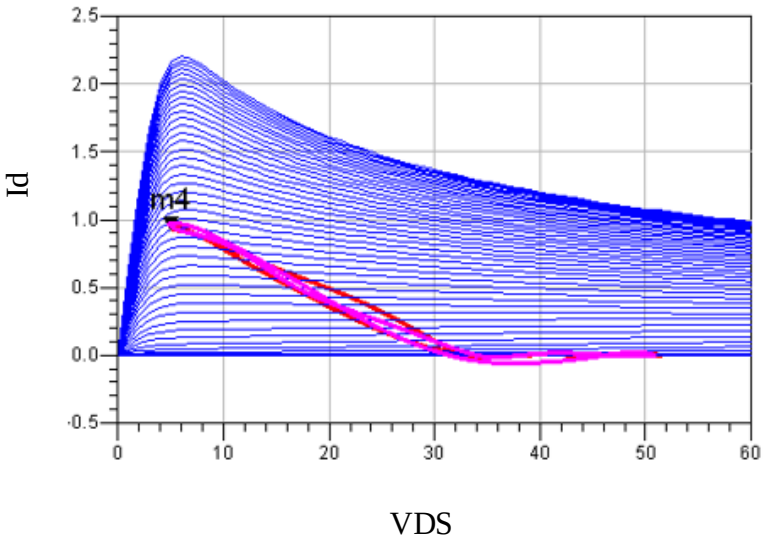
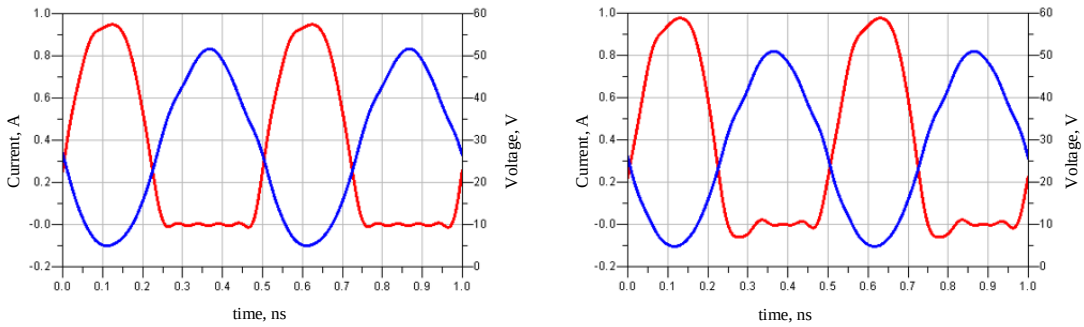


Figure 6.5: The pink loadline is captured from static de-embedding network, while red loadline is from the devices built-in loadpull function.



(a) Current and voltage for built-in function

(b) Current and voltage for de-embedding network

Figure 6.6: Current (red line) and voltage (blue line) waveforms captured from built-in model and static network approaches to de-embedding.

In this simulation, the Load-pull Instrument uses a harmonic balance simulation controller running at 2 GHz, with input power set to +16 dBm, gate bias to -3.5V for class B and drain bias to 28V. The captured drain efficiency is 60.4% with 21.6 dB of gain. This has been achieved by using the access to the current generator plane to force specific class-B impedances, specifically, an optimum fundamental resistance and a short circuit for second and third harmonics

Figure 6.7 illustrates these impedance conditions have been achieved at the current generator plane, and also illustrates the fact that there are a different set of required impedances at the package plane, due to the presence of parasitic capacitance and inductance, which of course is where matching design needs to take place. The fundamental, unnormalised optimum impedance at current generator plane is found to be 43.8-j0.75 Ohms, whilst the second and third harmonic impedances are pointed at the 0 Ohms. However, the corresponding fundamental impedance recorded at package plane is 27.1+j14.1 Ohms, with second and third harmonic impedances rotated to the capacitive side of the Smith chart.

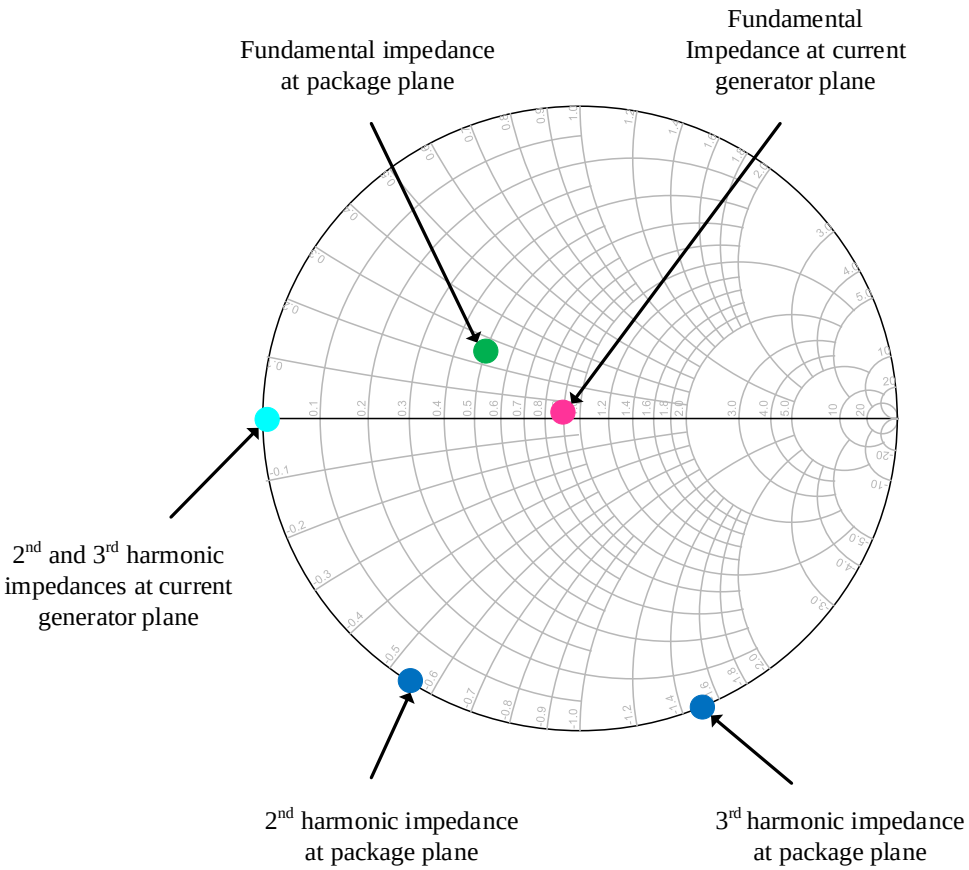
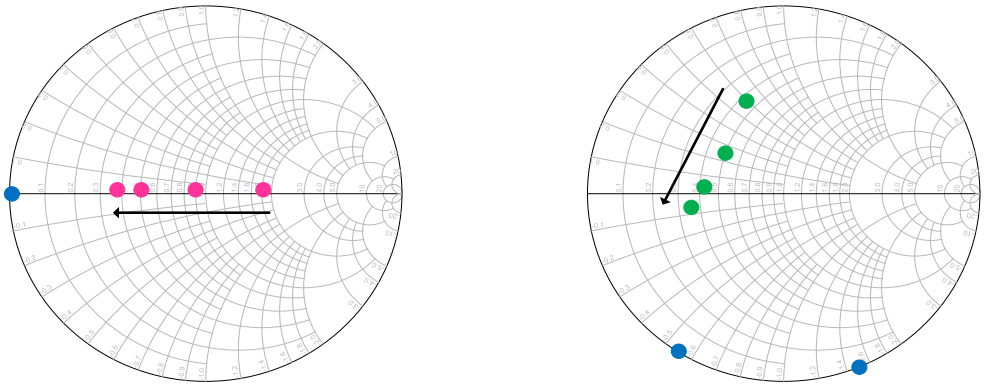


Figure 6.7: Fundamental and harmonic impendaces seen by the device at CGP and package plane.

The next phase of analysis involved exploring a novel aspect of this work, which was an investigation into using waveform engineering to optimise Doherty operation. Specifically, this involves using the harmonic load-pull template described above to engineer the specific impedance environment necessary for the *main* device to behave optimally. This involves engineering the dynamic load-line (itself constructed from time domain current and voltage waveforms), such that it 'tracks' up the IV plane, its slope increasing, remaining close to the knee region, with increasing drive. This is, of course, what would ideally happen to the *main* device in an optimised Doherty amplifier, and would yield a linearly increasing fundamental current component alongside a constant sinusoidal voltage waveform - ideal Doherty behaviour.

With this in mind, Figure 6.8 (a) shows this fundamental impedance change as the input drive level is increased, for input power levels of 13.3 dBm, 16 dBm, 18.7dBm and 21.7dBm. As input power increases, the fundamental impedance at CGP moves from ~100 Ohm towards ~25 Ohm, and the harmonics remain at short circuits. Figure 6.8 (b) shows how this CGP impedance are modified at the package plane and reveal the required design impedances for the matching network.

The corresponding set of CGP dynamic loadlines presented in Figure 6.9 show how when the input power increases, the load-line moves vertically, tracking the knee region and maintaining a constant fundamental voltage and hence constant *main* device efficiency.



(a) Fundamental impedances (pink dot), 2nd and 3rd harmonic impedances (blue dot) at current generator plane.

(b) Fundamental impedances (green dot), 2nd and 3rd harmonic impedances (blue dot) at package plane.

Figure 6.8: Impedances captured at current generator plane (a) and package plane (b) for drive levels of 13.3 dBm, 16 dBm, 18.7 dBm and 21.7 dBm.

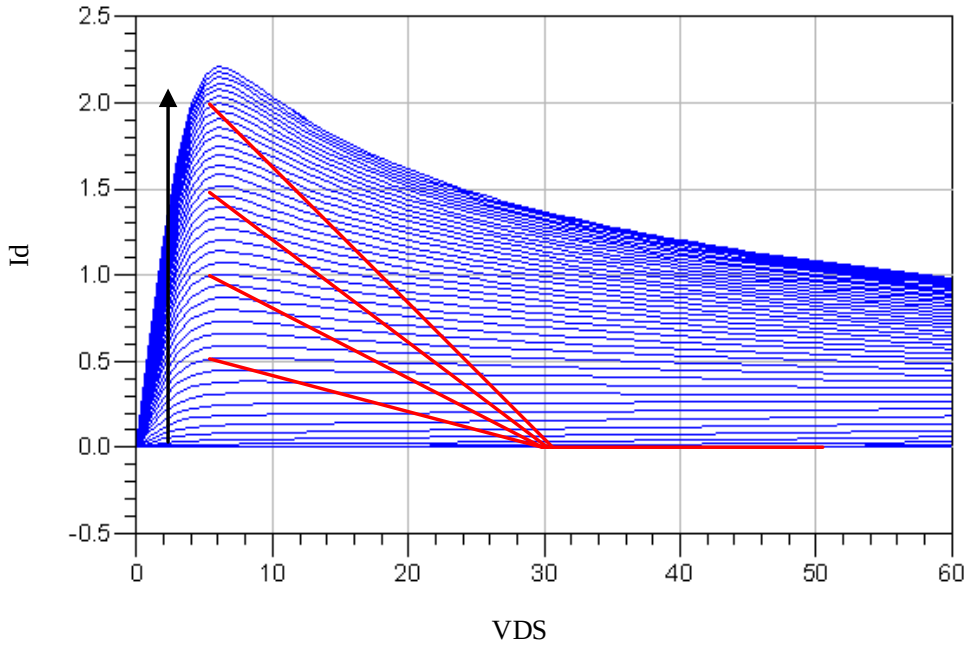


Figure 6.9: Waveform engineered, simplified ideal CGP Loadline of the *main* device in response to linearly increasing input power level and reducing fundamental load.

6.3.2 Design of the *Main* Device

The *main* amplifier is designed as a single class-AB structure, starting with the input matching network. The required input impedance seen looking into the device is determined from the earlier load-pull simulations, and then used within a Smith chart matching tool within the ADS software to design an appropriate matching network. The bias network is also incorporated into the matching network in an attempt to avoid unnecessary complication when combining the whole schematic later in the design.

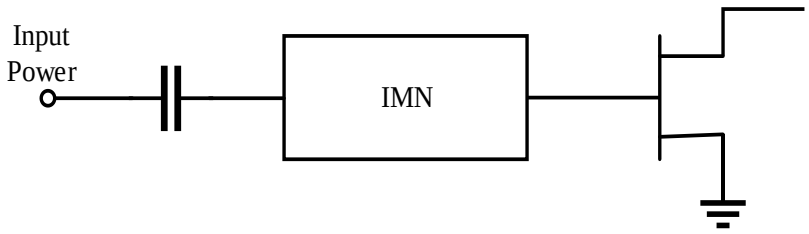


Figure 6.10: Input matching network for single class AB amplifier, including DC block to avoid the DC current flows to the input

The necessary Doherty impedance required to be seen by the *main* amplifier, for output matching purposes is also taken from load-pull simulation at CGP as mentioned in subchapter 6.3.1 and shown in Figure 6.8 (a). Later in the design, a length of transmission line is added with the required characteristic impedance (35.3Ω), to transform this impedance at the CGP from R_{opt} to $2R_{opt}$, as calculated in equation (1) in subchapter 2.3.1.

During tuning, the *main* amplifier will ideally see the *auxiliary* amplifier as high impedance, which is represent here in the schematic, by an open-ended transmission line, as illustrated in the first part of Figure 6.11. The second part of Figure 6.11 shows how this is then connected to the traditional impedance inverting network, with additional ports for the *auxiliary* device (∞) and the load (Z_L). The additional length of compensating transmission line is necessary, along with the output matching network (OMN) to rotate the real, low-power region load impedance of 2_{Ropt} to the corresponding package plane impedance on the inductive side of the Smith chart. The Smith chart in Figure 6.12 below indicates the two extremes of the impedance transformation range that results as the Doherty transits the high-power region of dynamic range, in the presence of this compensating line, with points corresponding to R_{opt} in blue and $2R_{opt}$ in red.

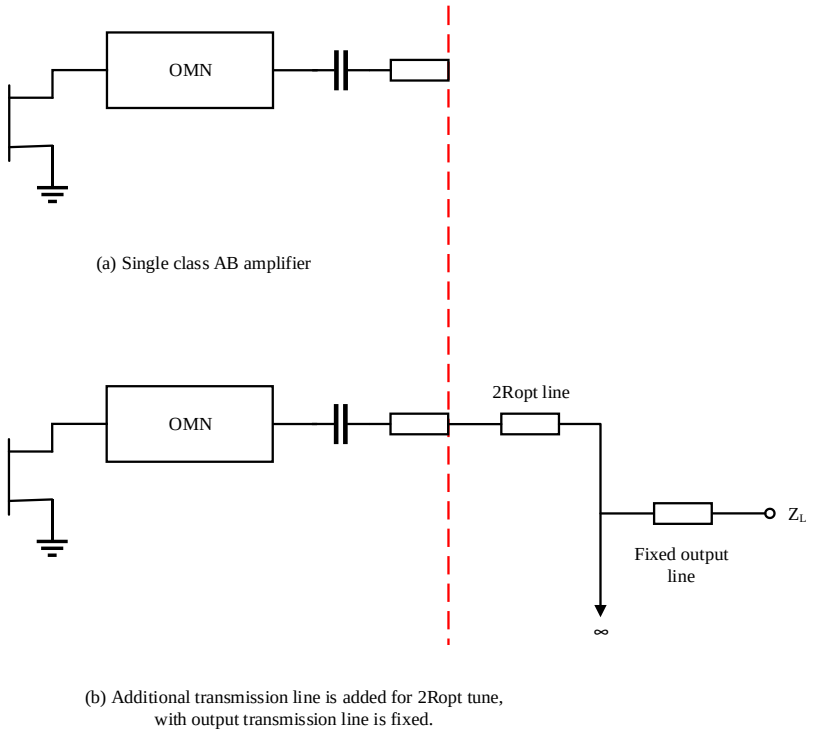


Figure 6.11: The *main* amplifier design steps; a) designing single amplifier first, then adding an additional compensating transmission line to tranform $2R_{opt}$ to the necessary impedance, and b) attacjing to the full output matching network.

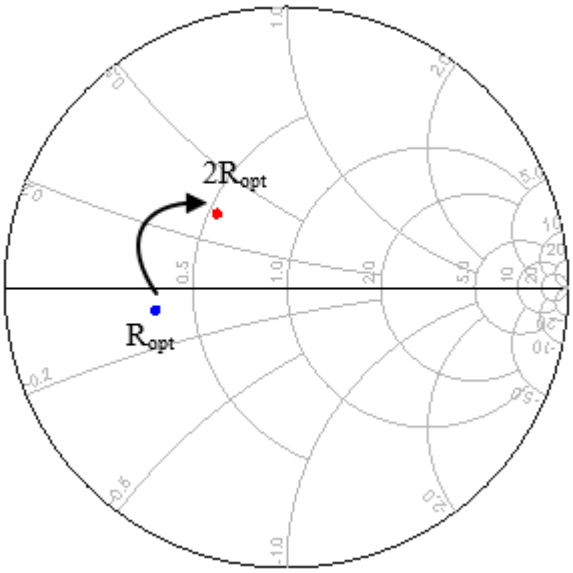


Figure 6.12: Impedance transformation from Ropt to 2Ropt, at the package plane, presented on smith chart.

6.3.3 Design of the *Auxiliary* Device

Moving to the next stage of the design involves developing a class-C biased *auxiliary* amplifier. This work is limited to a symmetrical Doherty amplifier design, which means that both *main* and *auxiliary* amplifiers need to use the same physical 10W device. Therefore, in this work, the input side for the *auxiliary* device is copied from that used in *main* amplifier design. A further 'offset' transmission line is added after DC block at the output path, and provides a compensating delay, tuned to compensate for the phase offset introduced by the *main* device compensating line, as shown in Figure 6.13. The offset line is also necessary to rotate the off-state output impedance presented by the *auxiliary* device towards an open circuit, such that it does not influence the *main* device behaviour in the low-power state. The value of

offset line has to be carefully chosen aligned with the required relative input phase of *main* and *auxiliary* inputs.

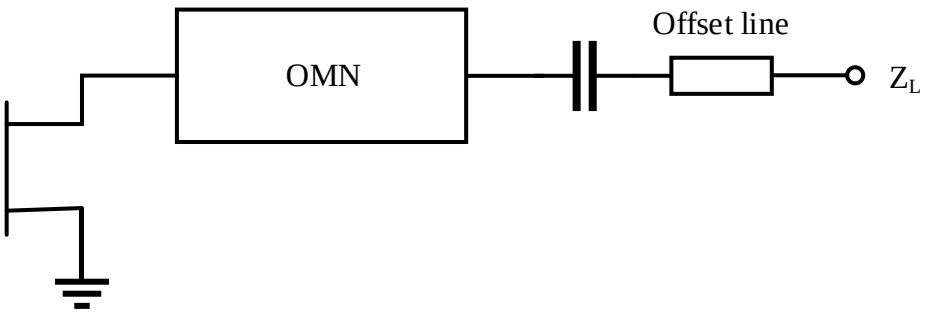


Figure 6.13: Offset line added at the end of *auxiliary* amplifier path to compensate the phase delay of *main* amplifier.

6.3.4 Full Doherty Design

As discussed in 6.3.2 and 6.3.3, the component parts of the Doherty amplifier are constructed separately for *main* and *auxiliary* amplifiers. They are finally combined to form a complete Doherty architecture, as shown in

Figure 6.14 below. Different input sources are also applied to this prototype for precisely controlling the relative input phase as well as the input power.

The Doherty schematic is initially built using ideal transmission line (TLIN) components to ensure the architecture is initially well behaved. Characteristic impedance and electrical length of the line are defined at an operating frequency of 2

GHz. Once correct simulated behaviour is established, TLIN components are then converting into physical microstrip line (MLIN) components defined in terms of physical width, length and substrate, and provide simulation in a more realistic environment. The substrate characteristics are defined in the simulation schematic, which is the same substrate as was used in prototype 1, in Chapter 5.

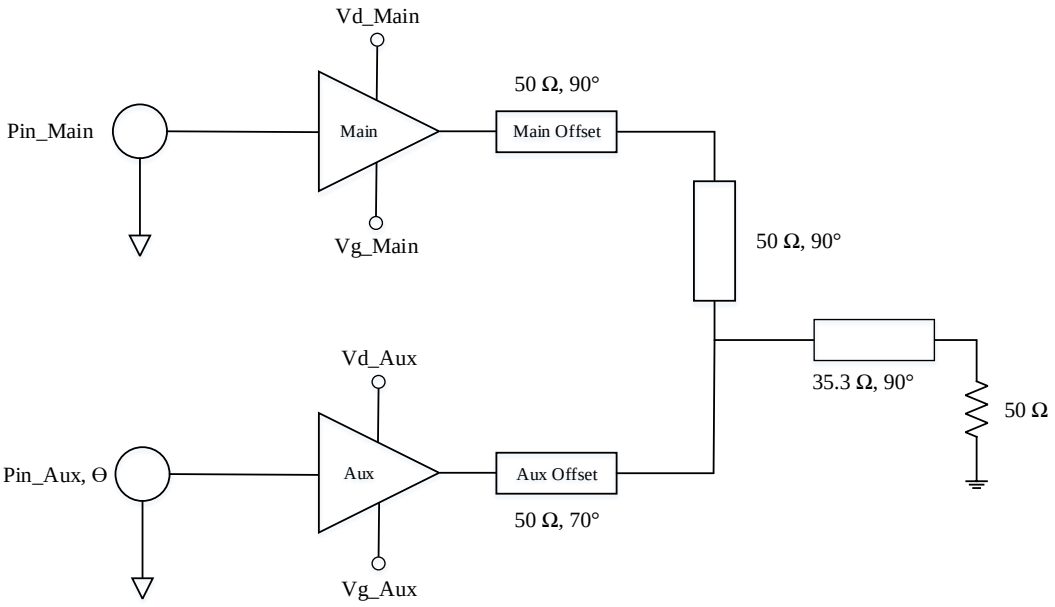


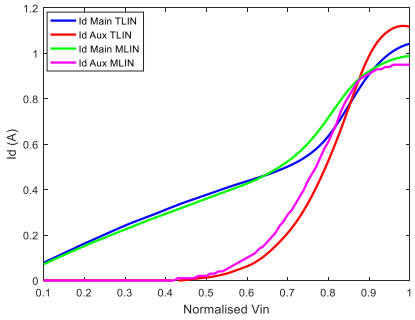
Figure 6.14: Full schematic of Doherty amplifier design, which is a combination of *main* and *auxiliary* parts. The IMN and OMN are included in the amplifier symbols.

Figure 6.15 below show the comparison result of TLIN and MLIN structures, for a complete Doherty simulation. The magnitude of fundamental current after optimization behaved as expected in a Doherty, with the transition point at 0.55V

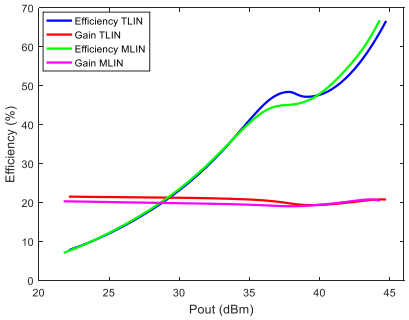
along a normalised input voltage range between 0 and 1V. This makes sense as in an ideal classical Doherty, the transition point occurs at Vin_max/2.

From the transition point, the *auxiliary* current then increases linearly until reaching the same maximum current as *main* amplifier. The maximum fundamental current achieved by both amplifiers is 1A for MLIN and 1.15A for TLIN implementations. It can be seen that the overall efficiency is 50% and 70% at transition point and PEP point respectively, at ~6 dB power back off. Moreover, the gain is relatively constant at 20 dB and slightly drops at the transition point as the *main* device compresses, and then expands slightly as the *auxiliary* begins to contribute.

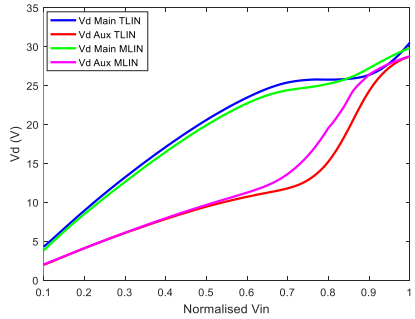
The transformation of impedances pattern for *main* and *auxiliary* amplifiers is illustrated in Figure 6.16. Referring to the impedance of *main* amplifier, it can be seen to be constant at 55Ω throughout the low-power region, whilst at V_{in} = 0.55V of transition point it begins to drop, as expected, and reaches the same impedance as *auxiliary* of 30Ω at PEP. However, this is still acceptable as Doherty architecture because it meets the requirement of Doherty behaviour with load modulation clearly being applied and efficiency enhanced in the high power region.



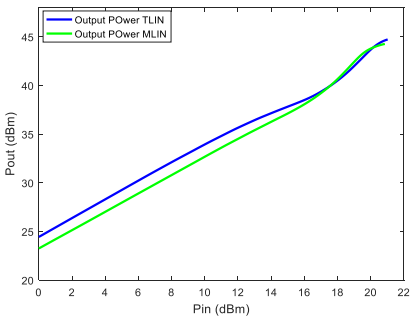
(a) Fundamental current



(a) Efficiency and gain



(a) Fundamental voltage



(a) Output power

Figure 6.15: Results of overall performance of Doherty amplifier, comparing transmission line with microstrip line implementations, using a real device model at 2 GHz.

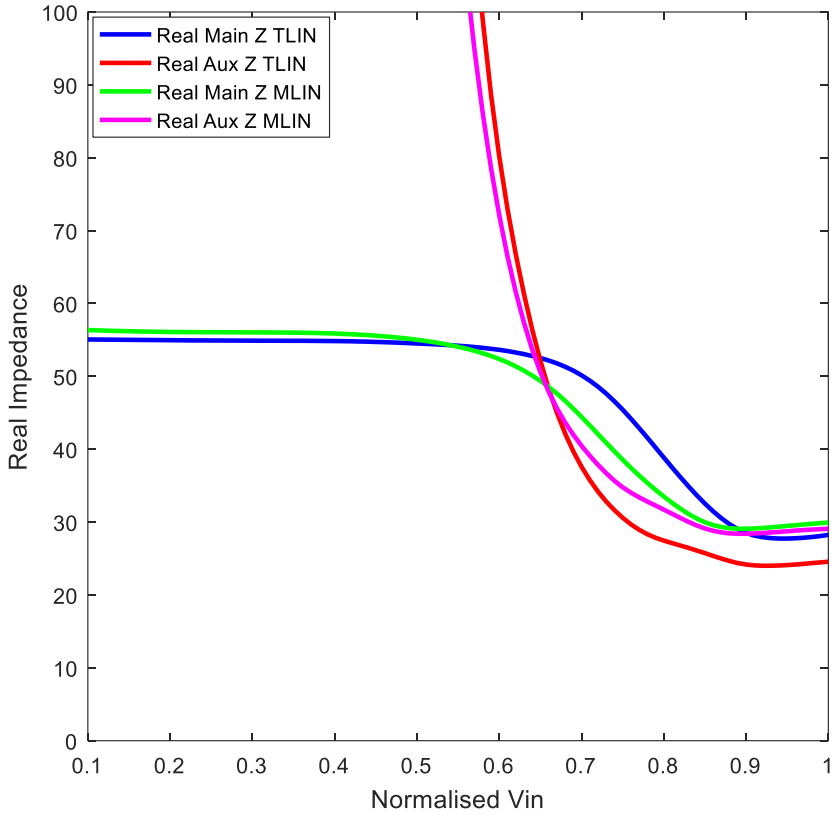


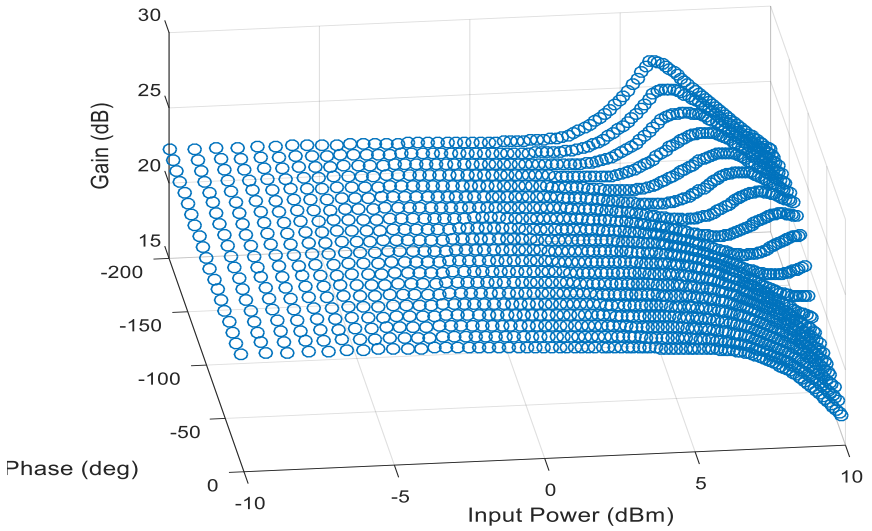
Figure 6.16: Impedance seen by *main* and *auxiliary* ampifiers over entire dynamic range.

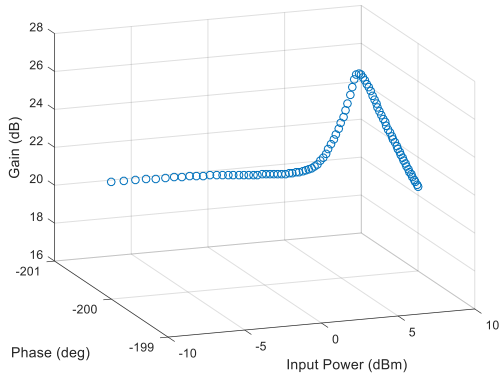
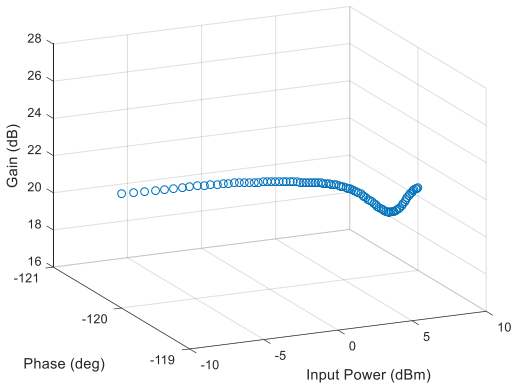
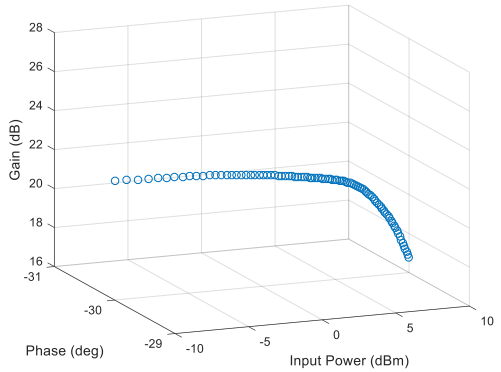
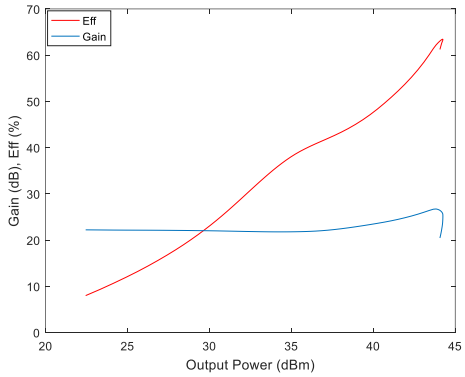
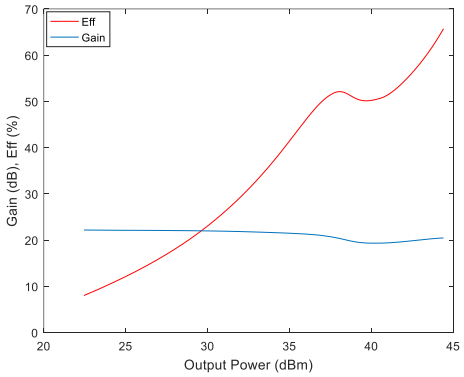
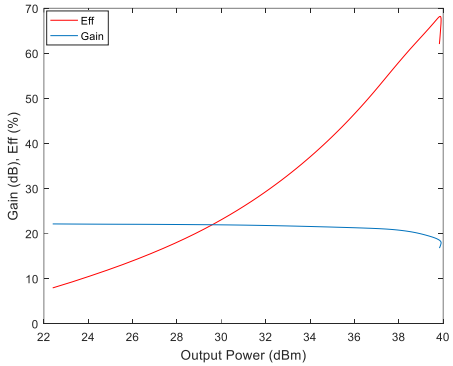
6.4 Relative Input Phase Analysis at a Selected Gain

Relative input phase is recognised as critical parameters in the design of this prototype, and needs to be chosen wisely to ensure good overall performance. One major concern in doing this is that by optimizing one parameter, there may be significant impact to other performance parameters. In this design, three different values of relative phase are used to explore how the structure responds in terms of efficiency and output power. Table 4 below depicts the performance of classical

Doherty at relative input phase values of -200, -120 and – 30 degrees. These phases are randomly plotted, based on the gain profile chosen (referring to overall scatter plot). From these results, it is possible to decide which phase gives then most beneficial response, in terms of gain profile and other parameters. It is noted that, for this arrangement, -120 degrees of relative phase results in the best overall performance.

Table 4: Relative Input Phase Analysis

Scatter plot of overall gain, input phase and input power	

	-200 degree	**-120 degree**	**-30 degree**
Scatter plot of gain at selected input phase			
Efficiency at selected gain and input phase, in respond to output power			

6.5 Input Attenuation Doherty-Effects on Efficiency

The input attenuation Doherty implementation, as described in the literature review in Chapter 2, aims to ensure the optimal conduction behaviour of the *auxiliary* amplifier in response to the magnitude of the input applied to the *main* amplifier. To achieve this, different sources are used to drive independent inputs of the Doherty structure. To realize this approach, the input power supplied to the *auxiliary* amplifier is altered according to a pre-defined function, and the relative input phase is also controlled accordingly. For a commercial realisation using this approach, a separate RF channel would be required, increasing complexity and expense.

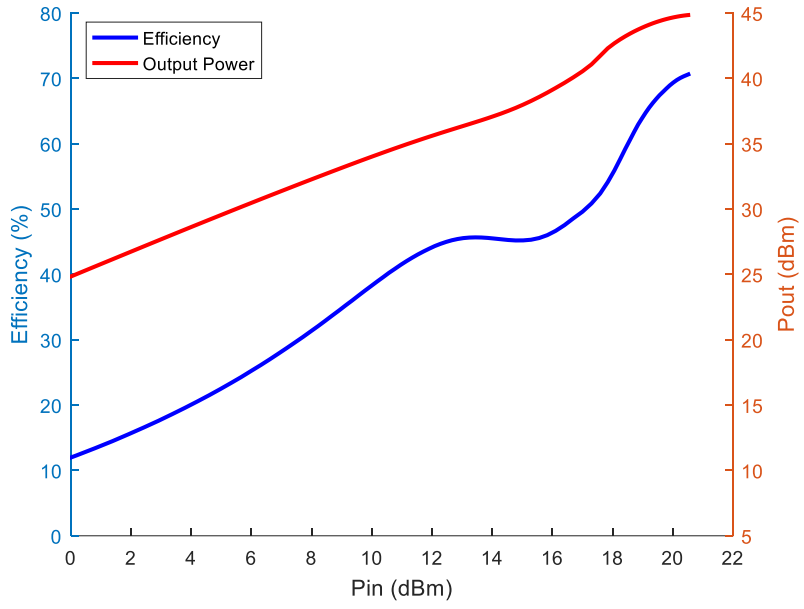
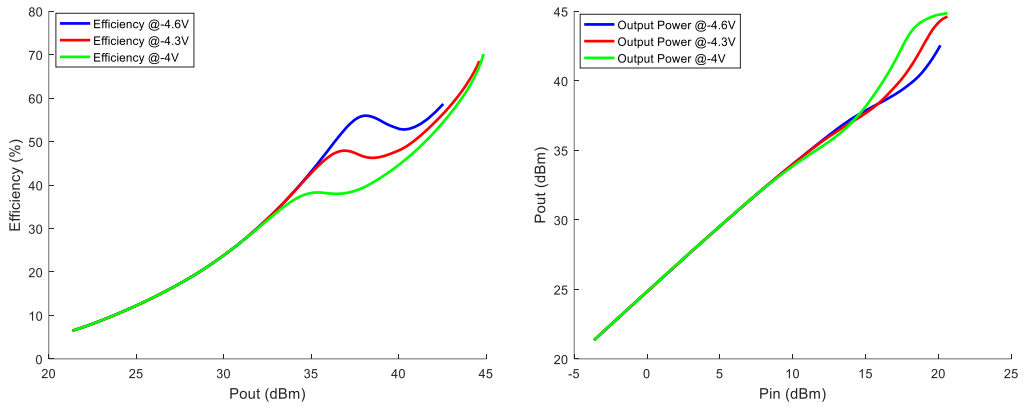


Figure 6.17 Simulation of output power and efficiency for the input attenuation approach

6.6 *Auxiliary* Bias Effects on Performance

As discussed in the adaptive bias subchapter 2.4.3, either changes in gate or drain bias of *main* and a*uxiliary* amplifier can be used to affect the overall performance of the Doherty amplifier. In order to see the impact of bias adaption on efficiency, a classical Doherty PA architecture is used. In this analysis, there are two approaches used; in the first, the gate bias of *auxiliary* amplifier is considered at three class-C bias points around the nominal classical bias point; -4.6V, -4.3V and -4V, while the gate voltage of *main* amplifier is set to a static -3V. The drain voltage of both amplifiers is set to 28V. Graphs in Figure 6.18 below shows how the transition point varies with bias, and what happens when the *auxiliary* device begins to conduct too early in the dynamic range, causing lower average efficiency. The dynamic range is also increased.



(a) Efficiency

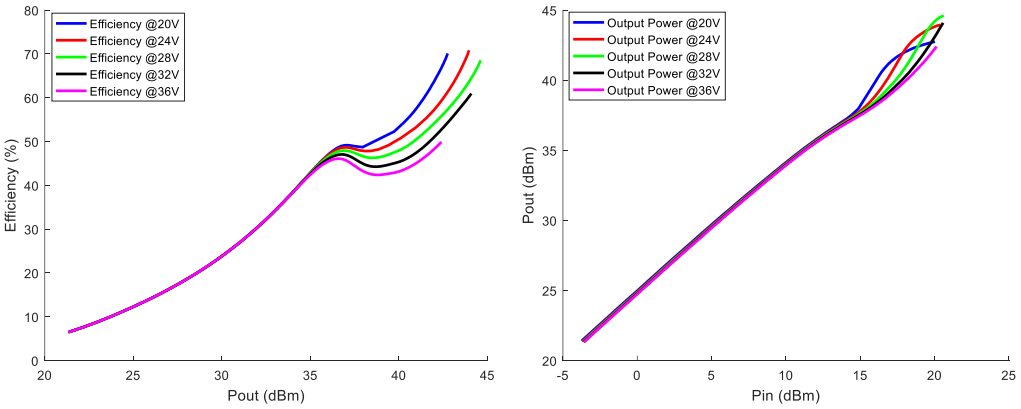
(a) Output power in response to input power

Figure 6.18 The overall performance when gate voltage of *auxiliary* amplifier is varied, whilst other volatages are fixed.

In the second experiment, the drain voltage of *auxiliary* amplifier is varied; 20V, 24V, 28V, 32V and 36V, with constant 28V supplied to *main* amplifier. As we can see in Figure 6.19, when the voltage supply is increased, the peak efficiency gets closer to the efficiency at the transition point. Unfortunately however, the dynamic range is decreased due to knee walk-out effects associated with GaN device technology. The transition point efficiency is not affected because the *auxiliary* currents start to operate at same point for all drain voltage variations. Figure 6.20 (a) shows the expected efficiency performance (red dot) as a results from Table 5, constructed from linearized output power (brown line) shown in Figure 6.20 (b). The bias adaption results presented in both conditions offer an initial analysis to identify patterns in Doherty performance, so that further, more advanced approaches can be targeted for more significant improvements, which will be discuss in detail in the next section.

Table 5: Look up table for initially generating the desired gain shape and function.

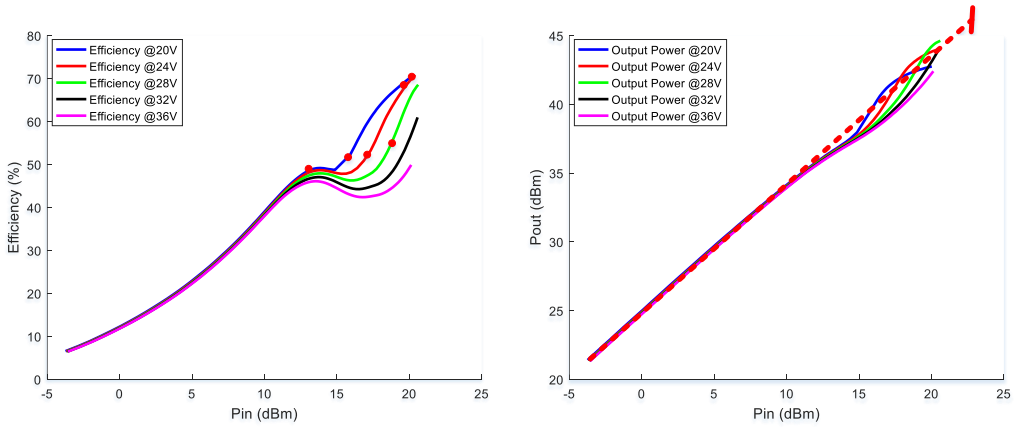
Input Power (dBm)	***Auxiliary* Drain Voltage (V)**
13	20
15.5	20
17	24
18.5	28
19.5	20
20	24



(a) Efficiency

(a) Output power in response to input power

Figure 6.19 The overall performance when drain voltage of *auxiliary* amplifier is varied, whilst other voltages are fixed.



(a) Efficiency in response to input power

(b) Output power in response to input power

Figure 6.20: Expected efficiency (a) as resulted from linearized output power (b).

6.7 *Linearisability* using Adaptive Bias Approach

6.7.1 Generating an *auxiliary* gate bias shaping function

It has been seen that the *auxiliary* behaviour strongly affects the overall efficiency, power and linearity performance of the overall Doherty. The *auxiliary* amplifier can be controlled, for example, to immediately switch on at the transition point, when the *main* amplifier reaches its saturation state, as discussed earlier in Chapter 2. This section discusses the theoretical idea of implementing a linearising method through an adaptive bias function applied to the *auxiliary* gate bias. The relationship between this profile and the magnitude of the input voltage is described by a function that we shall call the shaping function, for easier understanding. It means that when we apply this function to the gate of the *auxiliary* device, better overall performance can be achieved. To explore the benefits of a shaping function, firstly the gate voltage of *auxiliary* amplifier is swept to -3.7V, 4V, 4.3V and 4.6V. Each point resulted in a variation of gain, which later can be manipulated, as shown in Figure 6.21, to form a desired shape of gain. For example, the final gain graph achieved through an optimised shaping function is shown here as a blue line.

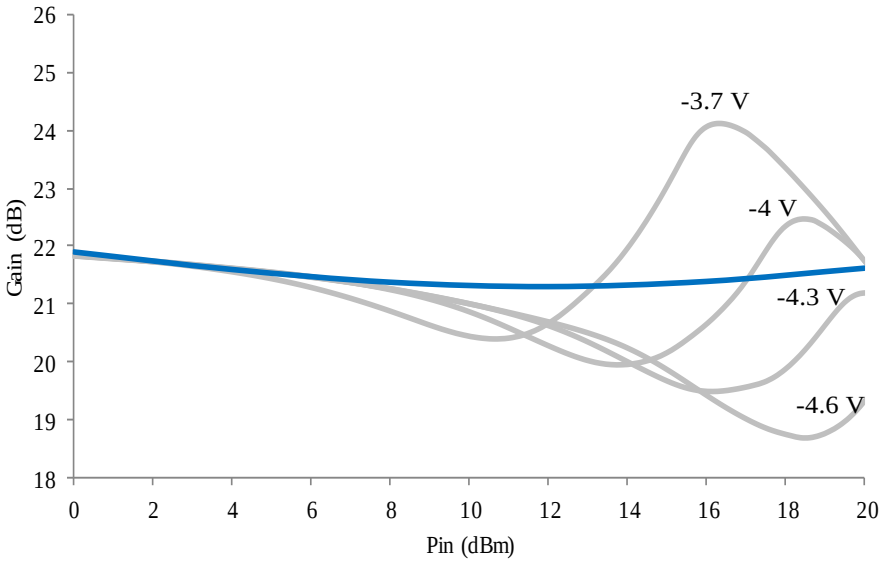


Figure 6.21: Gain variation in the range of -3.7V to 4.6V in 0.3V step.

Table 6 shows a look-up table used for this purpose. For each point of input power and gate voltage, a gain value is shown from a function of equation (9). The equation used a *sine* function with relation to maximum and minimum *auxiliary* gate voltage, labelled as V_{gmax} and V_{gmin} respectively, whilst A = 2, B = 2, C = 0.04, D = 21.9. With this value, we can predict the performance of Doherty PA, for example efficiency as presented in red dot in Figure 6.22.

Table 6: Look up table for initially generating the desired gain shape and function.

Input Power (dBm)	***Auxiliary* Gate Voltage (V)**
7	-4.0
13	-3.70
17	-4.0
20	-4.0

$$Gain\ Function = \frac{A.(Vgmax - Vgmin)}{B.\sin(Pin/C)} + D \quad (9)$$

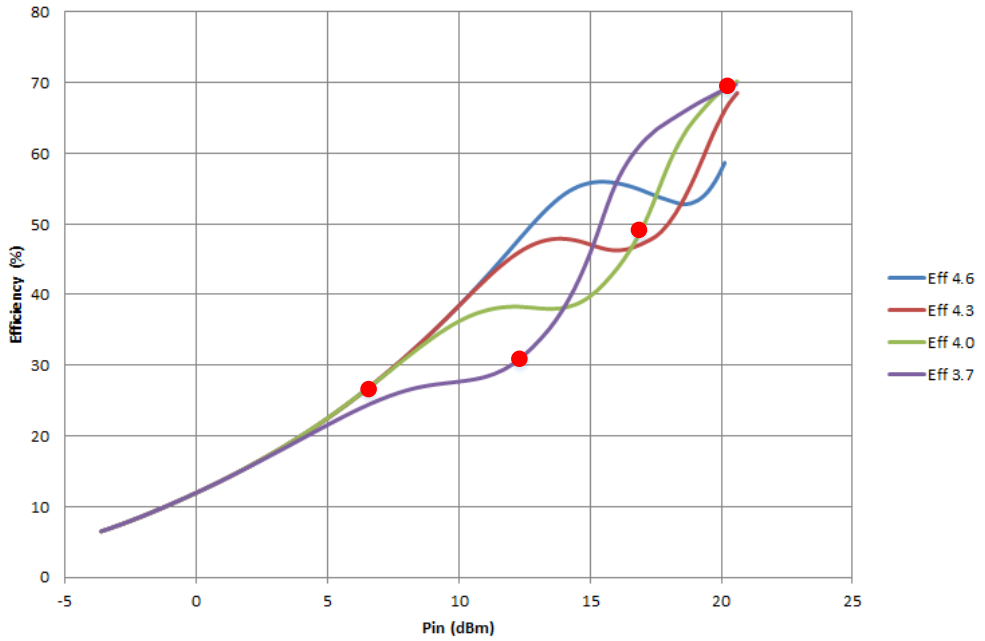


Figure 6.22: Expected efficiency in correspond to shaping function shown in Figure 6.21.

6.7.2 *Linearisability* of Amplifier

The *linearisablity* of an amplifier, in this work, refers to the suitability of an amplifiers, or the ease with which its AM-AM and AM-PM distortion characteristics can be corrected through traditional linearization approaches. An approach is introduced that involve the creation and application of shaping functions, created for example in 6.7.1 to produce a flat gain. We can assume that the shaping function as part of the pre-distortion used, a method by which one first stimulates a non-linear PA, and then observes the results of that stimulus at the output of the PA to estimate the AM-AM and AM-PM effects. These estimated distortions are then removed from the PA by pre-distorting the input stimulus with their inverse equivalents.

Theoretically, if an inverse function can be extracted from the original distortion function, they can be combined to cancel each other out, and to present a flat gain. The function graph in Figure 6.21 is addressed closely and illustrates in Figure 6.23 below where red line is the original shaping function while blue line is the inverse version of the original function. Cancellation out between these two will produce a flat gain. In real environment, the shaping function can be placed at the *auxiliary* gate through a support network while the inverse function can be located at the input source. Furthermore, it can also be implemented at the other part such as drain supply voltage. Using the function, the percentage to get the best result is higher rather than manipulating the bias manually, because we take the points that fall into gain's range to create the function in certain boundary.

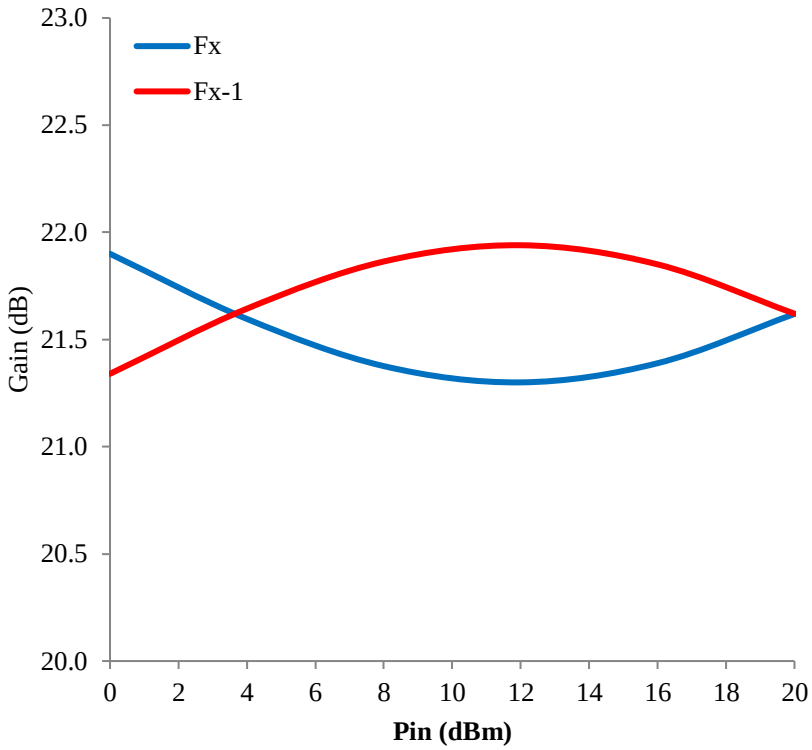


Figure 6.23: Shaping function (blue line) generated from equation and its inverse function (red line)

Referring to Figure 6.24, we can see clearly how the gate voltage of the *auxiliary* amplifier changes as a function of input power, when the shaping function is applied. The *auxiliary* gate voltage causes the device to be completely off in the lower power region until it reaches the transition point at Pin = 8dBm, and becomes active in the high power region, to fulfil the requirement of Doherty PA. The bias function is set in the range of -4.6V to -3.7V with 0.3V steps, to ensure that the device operates in its specification's boundary. Whilst the input power is swept from 0 dBm to 20dBm, and maintaining the drain voltage for both devices at 28V as well

as supplying -3V gate bias to the *main* amplifier consistently - all conditions necessary for achieving maximum efficiency at maximum power.

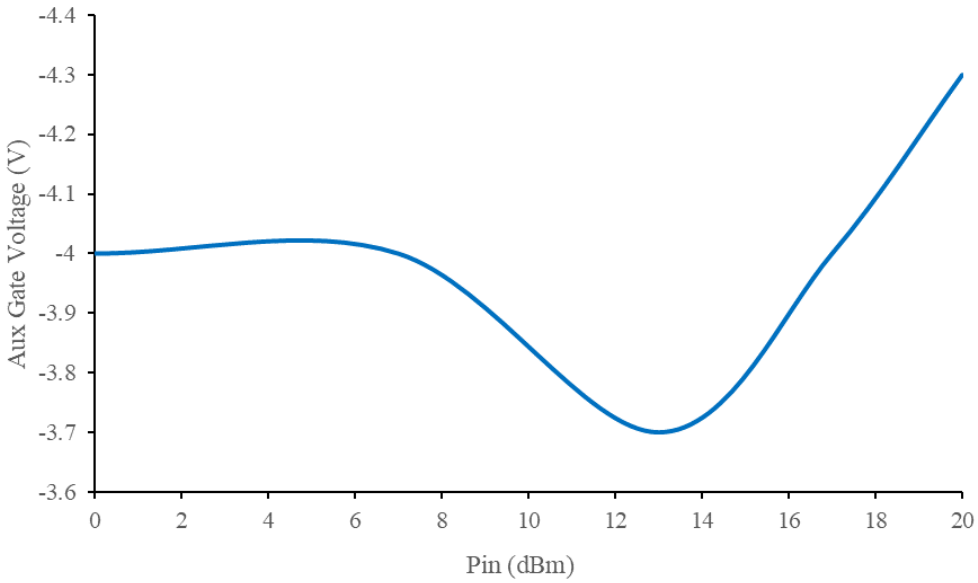


Figure 6.24: Changes of a*uxiliary* gate voltage as a function of input power

The resulting flat AM-AM gain characteristic is shown as a solid blue line in Figure 6.25. In comparison to the original adaptive bias Doherty, the gain-drop and expansion at high power region, shown in dotted blue, is corrected through the applied shaping function, which produces a corresponding linear gain and output power plot.

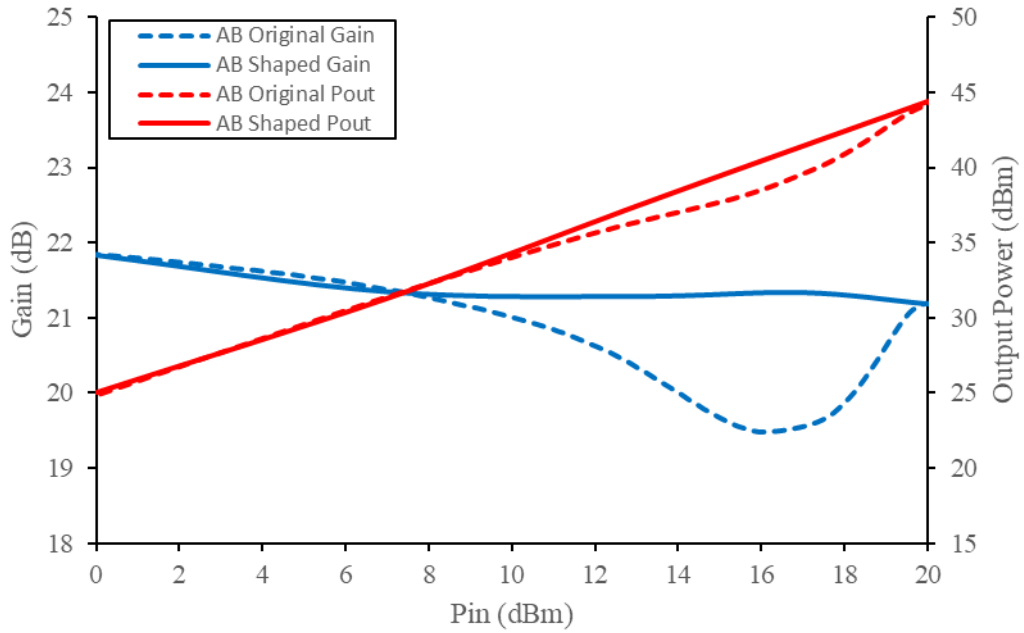


Figure 6.25: AM-AM result in response to input power sweep when the shaping function applied to *auxiliary* amplifier

The gain-phase or AM-PM represents the phase difference between *main* or *auxiliary* inputs and the combined output in degrees. Using firstly the input voltage applied to the *auxiliary* device as a reference, the gain-phase can be seen to change significantly as we 'flatten' the gain using the adaptive bias approach discussed earlier, as shown in Figure 6.26. Then, using instead the input to the *main* device as a reference, the gain-phase plot is also shown, this time as the red line in the same Figure 6.26. The behaviour of these two plots is interesting and due to the combination of two AM-PM characteristics.

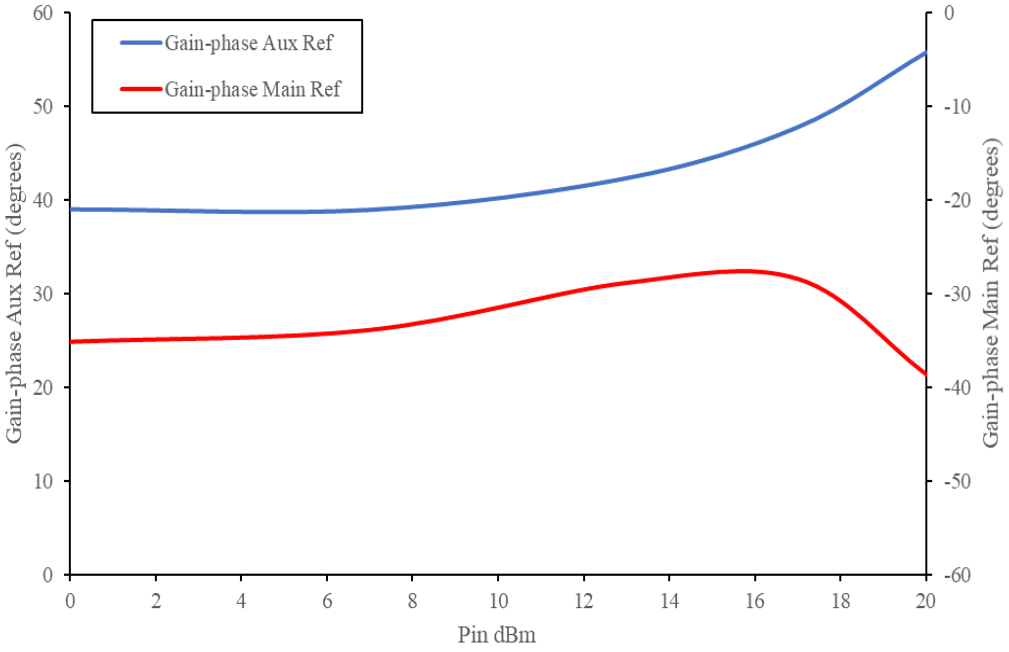


Figure 6.26: AM-PM result as a function of input power sweep when the shaping function is applied at *auxilairy* amplifier (blue line) and *main* amplfiier (red line)

6.8 Conclusion

In this chapter, a new, improved Doherty architecture is designed and presented, that operates at high frequency (2 GHz), and where the frequency-dependent behaviour of passive parasitic elements that influence the design and achievable performance are taken into account.

A systematic approach to Doherty amplifier design is explained in this chapter with proper design flow outlined, developing schematic from an ideal and microstrip transmission lines. It is important to know the properties of the device

itself before proceeding to the next design level. Other than drain voltage supply and gate bias voltage, the impedance seen by the device is also critical point that needed to be taken into serious consideration.

With regard to the problem with *auxiliary* amplifier not turning-on at the right time, adaptive bias and input attenuation approach are implemented, with the support from analysis involving the change of drain (supply) and gate bias voltage. With these new findings, the adaptive bias approach is further explored and refined by introducing an equation-driven shaping functions that are shown to improve linearity by flattening the gain and improve other performance, whilst showing the trade-off between AM-AM and AM-PM distortion in the Doherty structure.

CHAPTER 7

CONCLUSION AND FUTURE WORKS

7.1 Conclusion

Maintaining high efficiency over dynamic range, when the input power varies is one of the main issues that need to be addressed in power amplifier design, and the symmetrical Doherty amplifier is one of the architecture that can provide high efficiency over power back-off. It is chosen for the focus of this research because the architecture is simple in concept and relatively straight forward in its design, and as a result, is widely used in base station transmitters for cellular communication systems. Although previous works have discussed methods to improve Doherty efficiency, the adaptive bias approach with separate phase coherent input sources has not yet been specifically demonstrated. The objective of this work was therefore to design an adaptive bias Doherty structure and to demonstrate its implementation using individual input sources, to fill this gap in research. This chapter discusses and summarizes the three objectives listed in Chapter 1.

The first objective was to design a conventional Doherty architecture with two input sources. Two prototypes are demonstrated, the first prototype is realised in the AWR Microwave Office simulation environment, and this is the first attempt to learn the basics of Doherty amplifier design. The results obtained were generally poor, and not as expected, and the factors contributing to this non-ideal operation are

highlighted in detail in Chapter 5. It was however considered important to include this ‘poorly performing’ prototype and to use it as a vehicle to highlight typical design flaws that can occur in a traditional PA design flow applied to a Doherty deign.

The second prototype is designed in the Keysight ADS simulation and design environment. Taking all the root-causes of the earlier-identified poor performance fully into consideration, the new design begins with a device load-impedance analysis at the de-embedded, intrinsic current generator plane. The conventional Doherty amplifier achieved 50% and 70% of average and peak drain efficiency respectively with 20 dB gain overall.

The third objective is to measure Doherty performance in a real measurement environment with two independent input sources attached to *main* and *auxiliary* amplifiers. In this configuration, it is easier to precisely control adjust the relative input power and phase, and this is important because these are crucial parameters to get-right to achieve good Doherty performance. The measurement approach is implemented for the first prototype design, where the technique as well as need and approach for equipment calibration are explained and clarified. Unfortunately, for this first prototype, simulation results do not meet the Doherty behaviour expectations, and the measurement findings are consistent with this poor performance. However, the development of an independent input sources approach is shown to be applicable, effective and suitable to be used in further measurements.

The main emphasis of the research work is showing how bias adaption can enhance Doherty efficiency and performance, and this is demonstrated with a focus on gate voltage adaption, specifically to avoid the soft turn on behaviour of the

auxiliary amplifier. A shaping function approach is introduced for that purposes based on the idea explained in Chapter 6. Applying bias adaption through the use of shaping functions provides the possibility for improved *linearisability* of a Doherty power amplifier that promises better efficiency.

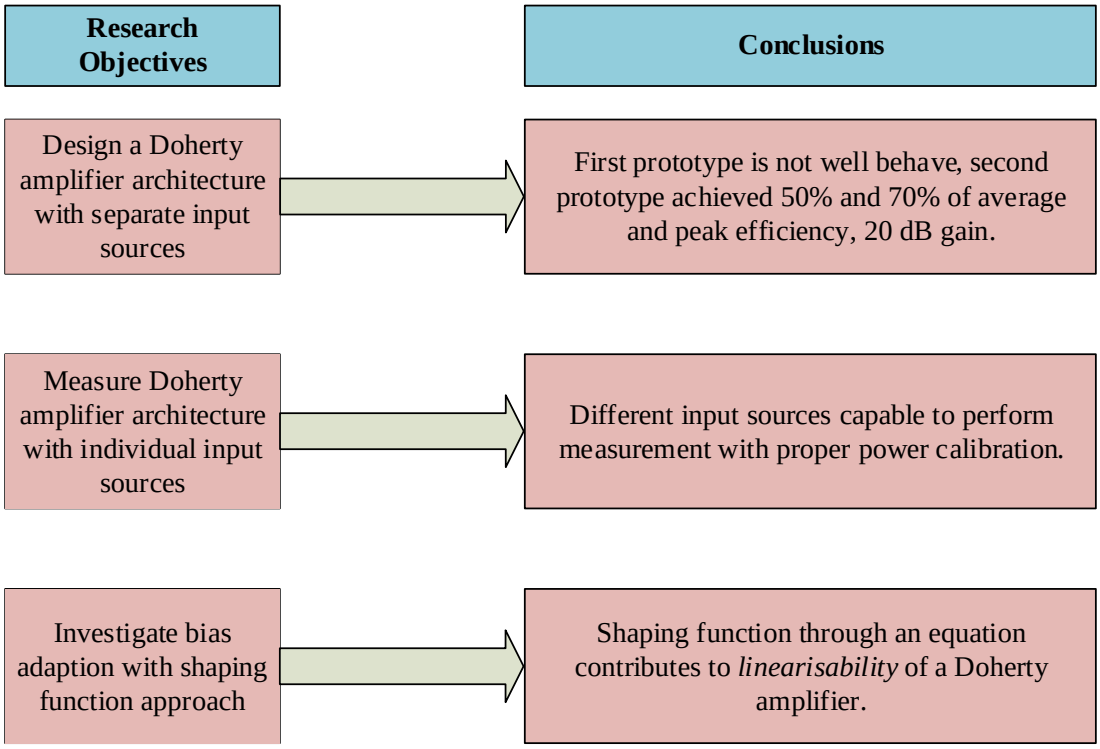


Figure 7.1: Summary of research objectives and conclusion.

7.2 Future Works

This research work shows that bias adaption can be successfully applied in the Doherty amplifier architecture. However, there are still limitations that can be addressed for better overall performance in future research studies.

- The advantages of designing and using two separate input drives for the Doherty PA design is presented in this work, and this provides the opportunity for these input signals to be pre-distorted individually with less complex networks, and improved linearity – this needs to be explored further.
- The shaping functions mentioned in Chapter 6 can be implemented in both ADS simulation and static measurement. Nevertheless, a proper network / approach that is able to apply the shaping function automatically, in response to continuous modulation is needed.
- In addition to *auxiliary* gate bias, it is also possible to apply a shaping function to the gate bias of *main* amplifier to engineer good levels of performance and *linearisability,* until good Doherty performance has achieved.
- This work is limited to using symmetrical Doherty PA architectures, and it is worth investigating the implementation of the shaping function approach to asymmetrical Doherty PA structures that using a bigger *auxiliary* device and achieves extended dynamic range, as well as designing a multistage Doherty architecture, for wider bandwidth.
- Although this work has considered only one approach at a time, it is worth investigating combining both input attenuation and adaptive bias approaches

simultaneously, to understand if a better overall performance can be achieved.

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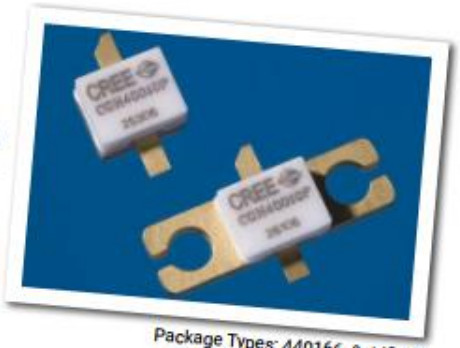
APPENDIX A

CREE

CGH40010

10 W, DC - 6 GHz, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.



Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

FEATURES

- Up to 6 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical P_{SAT}
- 65 % Efficiency at P_{SAT}
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Large Signal Models Available for ADS and MWO

Rev 4.0 – May 2015

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	84	Volts	25°C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25°C
Storage Temperature	T_{STG}	-65, +150	°C	
Operating Junction Temperature	T_J	225	°C	
Maximum Forward Gate Current	I_{GMAX}	4.0	mA	25°C
Maximum Drain Current[1]	I_{DMAX}	1.5	A	25°C
Soldering Temperature[2]	T_S	245	°C	
Screw Torque	τ	60	in-oz	
Thermal Resistance, Junction to Case[3]	$R_{\theta JC}$	8.0	°C/W	85°C
Case Operating Temperature[3,4]	T_C	-40, +150	°C	

Note:
[1] Current limit for long term, reliable operation
[2] Refer to the Application Note on soldering at www.cree.com/RF/Document-Library
[3] Measured for the CGH40010F at P_{DISS} = 14 W.
[4] See also, the Power Dissipation De-rating Curve on Page 6.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–	V_{DC}	V_{DS} = 28 V, I_D = 200 mA
Saturated Drain Current	I_{DS}	2.9	3.5	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	120	–	–	V_{DC}	V_{GS} = -8 V, I_D = 3.6 mA
RF Characteristics[2] (T_C = 25°C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12.5	14.5	–	dB	V_{DD} = 28 V, I_{DQ} = 200 mA
Power Output[3]	P_{SAT}	10	12.5	–	W	V_{DD} = 28 V, I_{DQ} = 200 mA
Drain Efficiency[4]	η	55	65	–	%	V_{DD} = 28 V, I_{DQ} = 200 mA, P_{SAT}
Output Mismatch Stress	VSWR	–	–	10 : 1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 200 mA, P_{OUT} = 10 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	4.5	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.3	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.2	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40010-AMP.
[3] P_{SAT} is defined as I_G = 0.36 mA.
[4] Drain Efficiency = P_{OUT} / P_{DC}

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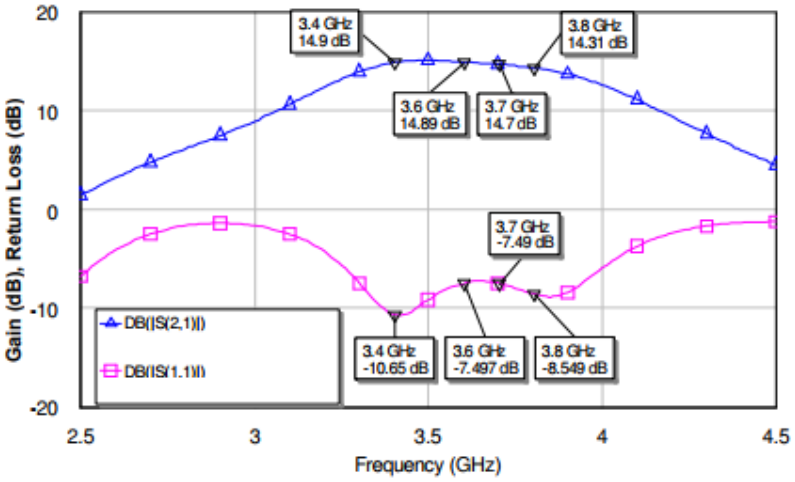
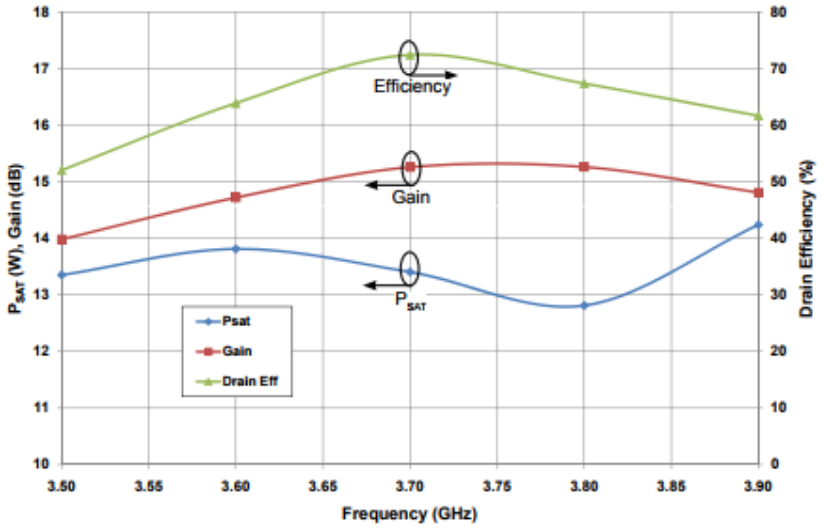
Typical Performance

Small Signal Gain and Return Loss vs Frequency of the CGH40010 in the CGH40010-AMP



P_{SAT}, Gain, and Drain Efficiency vs Frequency of the CGH40010F in the CGH40010-AMP
V_{DD} = 28 V, I_{DQ} = 200 mA



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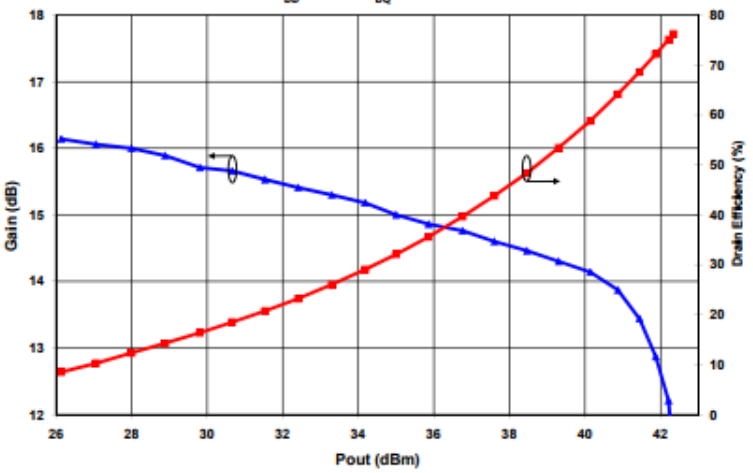
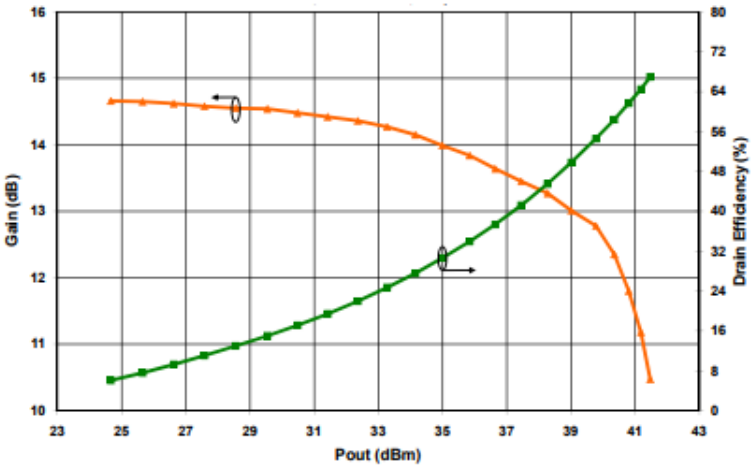
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 2.0 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



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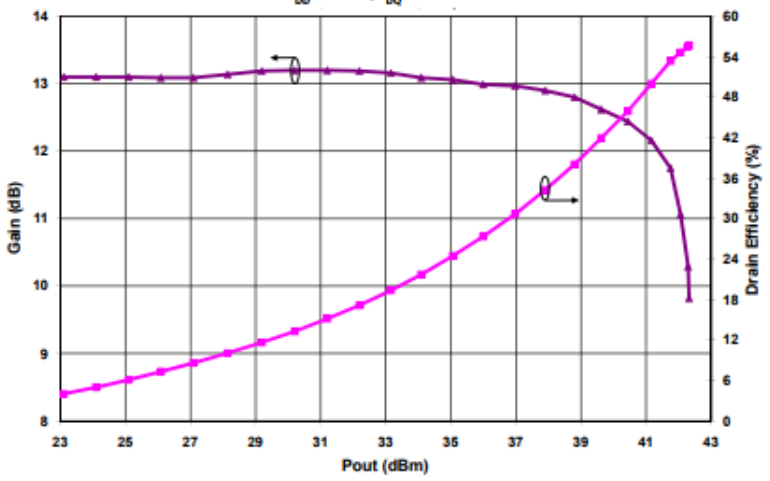
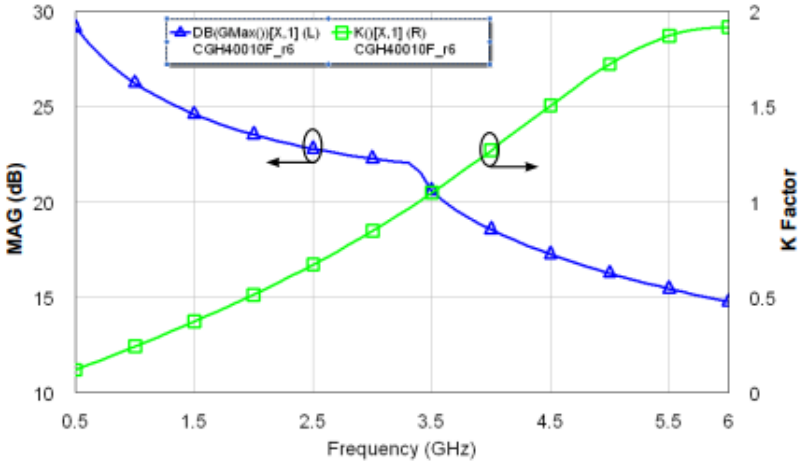
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



Simulated Maximum Available Gain and K Factor of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 200 mA



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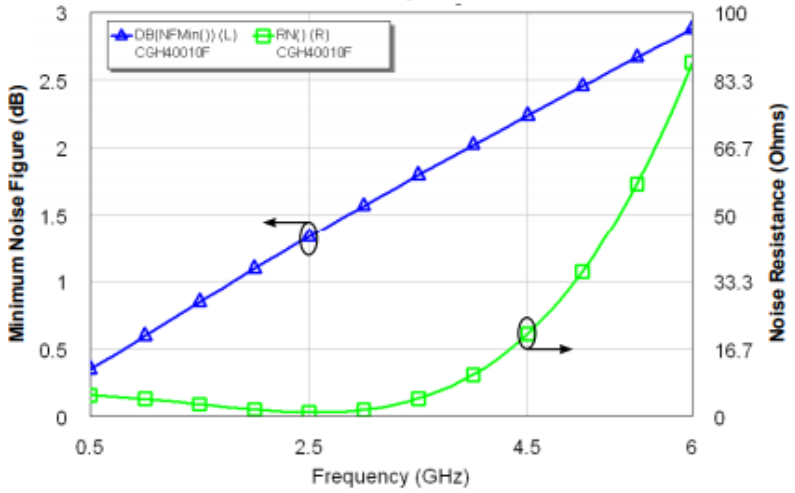
Typical Noise Performance

Simulated Minimum Noise Figure and Noise Resistance vs Frequency of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 100 mA



Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Test Methodology
Human Body Model	HBM	1A > 250 V	JEDEC JESD22 A114-D
Charge Device Model	CDM	1 < 200 V	JEDEC JESD22 C101-C

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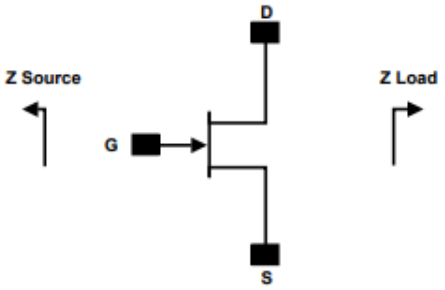
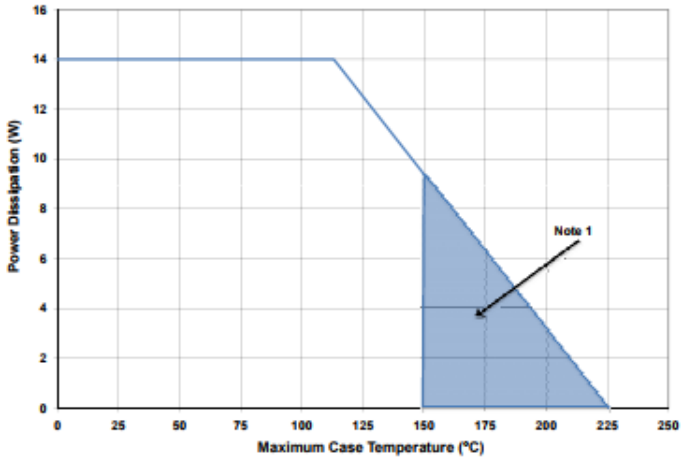
Source and Load Impedances



Frequency (MHz)	Z Source	Z Load
500	20.2 + j16.18	51.7 + j15.2
1000	8.38 + j9.46	41.4 + j28.5
1500	7.37 + j0	28.15 + j29
2500	3.19 - j4.76	19 + j9.2
3500	3.18 - j13.3	14.6 + j7.46

Note 1. V_{DD} = 28V, I_{DQ} = 200mA in the 440166 package.
Note 2. Optimized for power, gain, P_{SAT} and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

CGH40010 Power Dissipation De-rating Curve



Note 1. Area exceeds Maximum Case Operating Temperature (See Page 2).

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CGH40010-AMP Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1,R2	RES,1/16W,0603,1%,0 OHMS	1
R3	RES,1/16W,0603,1%,47 OHMS	1
R4	RES,1/16W,0603,1%,100 OHMS	1
C6	CAP, 470PF, 5%,100V, 0603	1
C17	CAP, 33 UF, 20%, G CASE	1
C16	CAP, 1.0UF, 100V, 10%, X7R, 1210	1
C8	CAP 10UF 16V TANTALUM	1
C14	CAP, 100.0pF, +/-5%, 0603	1
C1	CAP, 0.5pF, +/-0.05pF, 0603	1
C2	CAP, 0.7pF, +/-0.1pF, 0603	1
C10,C11	CAP, 1.0pF, +/-0.1pF, 0603	2
C4,C12	CAP, 10.0pF,+/-5%, 0603	2
C5,C13	CAP, 39pF, +/-5%, 0603	2
C7,C15	CAP,33000PF, 0805,100V, X7R	2
J3,J4	CONN SMA STR PANEL JACK RECP	1
J2	HEADER RT>PLZ.1CEN LK 2 POS	1
J1	HEADER RT>PLZ .1CEN LK 5POS	1
-	PCB, RO4350B, Er = 3.48, h = 20 mil	1
Q1	CGH40010F or CGH40010P	1

CGH40010-AMP Demonstration Amplifier Circuit

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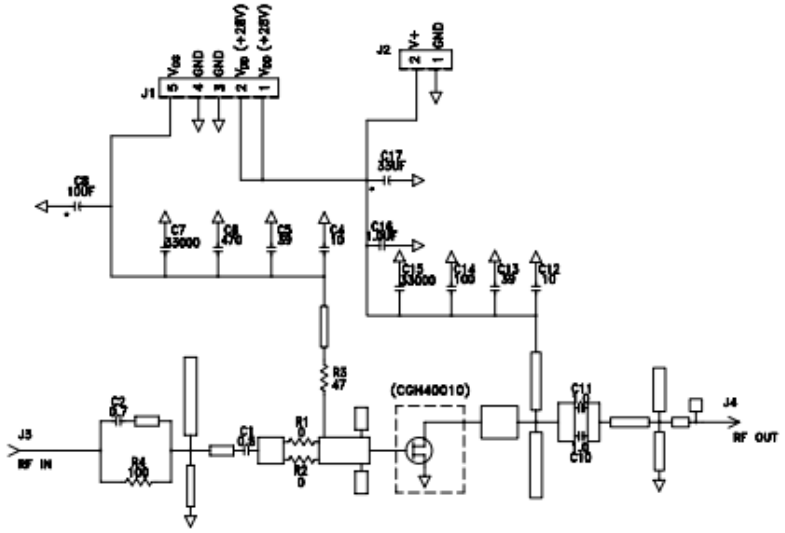
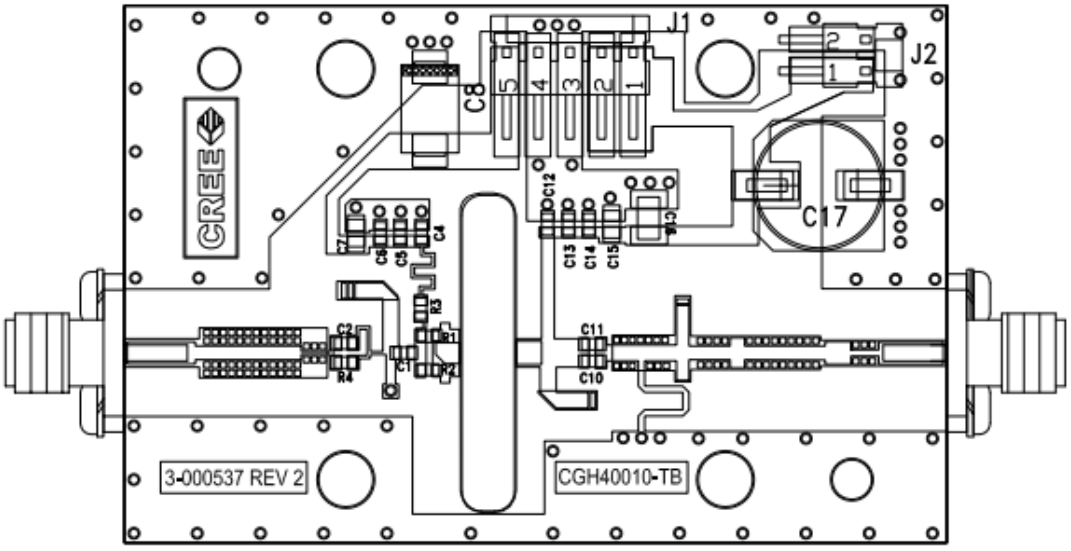
CGH40010-AMP Demonstration Amplifier Circuit Schematic



CGH40010-AMP Demonstration Amplifier Circuit Outline



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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 100 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.909	-123.34	17.19	108.22	0.027	21.36	0.343	-90.81
600 MHz	0.902	-133.06	14.86	101.82	0.028	15.60	0.329	-98.65
700 MHz	0.897	-140.73	13.04	96.45	0.028	10.87	0.321	-104.84
800 MHz	0.894	-146.96	11.58	91.78	0.029	6.84	0.317	-109.84
900 MHz	0.891	-152.16	10.41	87.61	0.029	3.33	0.316	-113.95
1.0 GHz	0.890	-156.60	9.43	83.82	0.029	0.19	0.318	-117.42
1.1 GHz	0.889	-160.47	8.62	80.31	0.029	-2.66	0.321	-120.40
1.2 GHz	0.888	-163.90	7.93	77.02	0.029	-5.28	0.326	-123.02
1.3 GHz	0.887	-166.99	7.34	73.90	0.029	-7.72	0.332	-125.36
1.4 GHz	0.887	-169.80	6.82	70.92	0.029	-10.01	0.338	-127.51
1.5 GHz	0.887	-172.39	6.38	68.05	0.029	-12.18	0.345	-129.50
1.6 GHz	0.887	-174.80	5.98	65.28	0.028	-14.24	0.353	-131.37
1.7 GHz	0.887	-177.07	5.63	62.59	0.028	-16.21	0.360	-133.15
1.8 GHz	0.887	-179.22	5.32	59.97	0.028	-18.09	0.369	-134.87
1.9 GHz	0.887	178.73	5.04	57.41	0.028	-19.91	0.377	-136.54
2.0 GHz	0.888	176.76	4.78	54.89	0.027	-21.66	0.385	-138.17
2.1 GHz	0.888	174.86	4.55	52.42	0.027	-23.35	0.393	-139.77
2.2 GHz	0.888	173.02	4.34	49.99	0.027	-24.98	0.402	-141.34
2.3 GHz	0.888	171.23	4.15	47.60	0.026	-26.56	0.410	-142.90
2.4 GHz	0.889	169.48	3.97	45.24	0.026	-28.08	0.418	-144.45
2.5 GHz	0.889	167.76	3.81	42.90	0.026	-29.55	0.426	-145.99
2.6 GHz	0.890	166.07	3.66	40.59	0.025	-30.98	0.434	-147.53
2.7 GHz	0.890	164.39	3.53	38.30	0.025	-32.36	0.442	-149.06
2.8 GHz	0.890	162.74	3.40	36.03	0.025	-33.69	0.450	-150.59
2.9 GHz	0.891	161.10	3.28	33.78	0.024	-34.97	0.458	-152.12
3.0 GHz	0.891	159.46	3.17	31.55	0.024	-36.20	0.465	-153.65
3.2 GHz	0.892	156.21	2.97	27.12	0.023	-38.51	0.479	-156.72
3.4 GHz	0.893	152.96	2.79	22.73	0.022	-40.63	0.493	-159.80
3.6 GHz	0.893	149.69	2.64	18.38	0.022	-42.52	0.505	-162.90
3.8 GHz	0.894	146.38	2.50	14.05	0.021	-44.17	0.517	-166.03
4.0 GHz	0.894	143.03	2.38	9.72	0.020	-45.56	0.527	-169.19
4.2 GHz	0.894	139.61	2.28	5.40	0.019	-46.67	0.537	-172.39
4.4 GHz	0.895	136.11	2.18	1.07	0.019	-47.46	0.546	-175.64
4.6 GHz	0.895	132.53	2.09	-3.29	0.018	-47.90	0.554	-178.95
4.8 GHz	0.895	128.85	2.01	-7.68	0.017	-47.96	0.561	177.69
5.0 GHz	0.895	125.06	1.94	-12.10	0.017	-47.61	0.568	174.25
5.2 GHz	0.895	121.15	1.88	-16.58	0.016	-46.84	0.573	170.72
5.4 GHz	0.895	117.11	1.82	-21.12	0.016	-45.67	0.578	167.10
5.6 GHz	0.895	112.94	1.77	-25.73	0.015	-44.12	0.582	163.38
5.8 GHz	0.895	108.62	1.72	-30.42	0.015	-42.30	0.586	159.54
6.0 GHz	0.895	104.15	1.68	-35.20	0.015	-40.33	0.589	155.56

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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 200 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.911	-130.62	18.41	105.41	0.022	19.44	0.303	-112.24
600 MHz	0.906	-139.65	15.80	99.47	0.023	14.31	0.299	-119.83
700 MHz	0.902	-146.70	13.80	94.50	0.023	10.17	0.298	-125.50
800 MHz	0.899	-152.41	12.22	90.19	0.023	6.68	0.299	-129.85
900 MHz	0.898	-157.17	10.96	86.34	0.024	3.67	0.302	-133.28
1.0 GHz	0.896	-161.24	9.92	82.82	0.024	0.99	0.305	-136.05
1.1 GHz	0.896	-164.79	9.06	79.56	0.024	-1.41	0.309	-138.34
1.2 GHz	0.895	-167.95	8.33	76.49	0.024	-3.62	0.314	-140.30
1.3 GHz	0.895	-170.80	7.70	73.57	0.023	-5.66	0.320	-142.01
1.4 GHz	0.894	-173.41	7.17	70.78	0.023	-7.56	0.326	-143.54
1.5 GHz	0.894	-175.82	6.70	68.08	0.023	-9.35	0.332	-144.94
1.6 GHz	0.894	-178.09	6.28	65.47	0.023	-11.05	0.338	-146.24
1.7 GHz	0.894	179.78	5.92	62.92	0.023	-12.66	0.345	-147.48
1.8 GHz	0.894	177.75	5.59	60.43	0.023	-14.19	0.352	-148.68
1.9 GHz	0.894	175.81	5.30	57.99	0.023	-15.65	0.358	-149.84
2.0 GHz	0.894	173.94	5.04	55.59	0.022	-17.05	0.365	-150.99
2.1 GHz	0.894	172.13	4.80	53.23	0.022	-18.39	0.372	-152.12
2.2 GHz	0.894	170.37	4.58	50.91	0.022	-19.67	0.379	-153.26
2.3 GHz	0.895	168.65	4.38	48.61	0.022	-20.90	0.386	-154.39
2.4 GHz	0.895	166.96	4.20	46.33	0.021	-22.08	0.393	-155.54
2.5 GHz	0.895	165.30	4.03	44.08	0.021	-23.20	0.400	-156.69
2.6 GHz	0.895	163.66	3.88	41.84	0.021	-24.27	0.407	-157.85
2.7 GHz	0.895	162.04	3.74	39.63	0.021	-25.28	0.414	-159.03
2.8 GHz	0.895	160.43	3.60	37.43	0.020	-26.25	0.420	-160.22
2.9 GHz	0.896	158.83	3.48	35.24	0.020	-27.16	0.427	-161.42
3.0 GHz	0.896	157.24	3.37	33.06	0.020	-28.02	0.433	-162.64
3.2 GHz	0.896	154.06	3.16	28.74	0.019	-29.57	0.446	-165.13
3.4 GHz	0.896	150.87	2.98	24.44	0.019	-30.88	0.457	-167.69
3.6 GHz	0.896	147.66	2.82	20.16	0.018	-31.95	0.468	-170.31
3.8 GHz	0.897	144.41	2.68	15.89	0.018	-32.76	0.478	-173.00
4.0 GHz	0.897	141.10	2.56	11.61	0.017	-33.30	0.488	-175.77
4.2 GHz	0.897	137.72	2.45	7.33	0.017	-33.55	0.497	-178.61
4.4 GHz	0.897	134.26	2.35	3.03	0.017	-33.50	0.505	178.47
4.6 GHz	0.897	130.71	2.26	-1.31	0.016	-33.18	0.512	175.46
4.8 GHz	0.896	127.06	2.17	-5.68	0.016	-32.58	0.518	172.36
5.0 GHz	0.896	123.30	2.10	-10.09	0.016	-31.74	0.524	169.16
5.2 GHz	0.896	119.42	2.04	-14.57	0.016	-30.72	0.529	165.86
5.4 GHz	0.896	115.41	1.98	-19.10	0.016	-29.60	0.534	162.44
5.6 GHz	0.896	111.26	1.92	-23.71	0.016	-28.46	0.537	158.89
5.8 GHz	0.895	106.97	1.87	-28.40	0.017	-27.41	0.540	155.20
6.0 GHz	0.895	102.53	1.82	-33.19	0.017	-26.54	0.543	151.36

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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 500 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.914	-135.02	18.58	103.70	0.020	18.36	0.300	-126.80
600 MHz	0.909	-143.57	15.88	98.05	0.020	13.67	0.302	-133.51
700 MHz	0.906	-150.23	13.83	93.33	0.021	9.90	0.304	-138.40
800 MHz	0.904	-155.61	12.23	89.23	0.021	6.77	0.307	-142.08
900 MHz	0.903	-160.09	10.95	85.56	0.021	4.08	0.311	-144.94
1.0 GHz	0.902	-163.93	9.91	82.21	0.021	1.71	0.314	-147.23
1.1 GHz	0.901	-167.29	9.04	79.09	0.021	-0.41	0.319	-149.10
1.2 GHz	0.901	-170.29	8.31	76.15	0.021	-2.35	0.323	-150.69
1.3 GHz	0.900	-173.00	7.69	73.35	0.021	-4.12	0.328	-152.07
1.4 GHz	0.900	-175.50	7.15	70.66	0.021	-5.78	0.333	-153.29
1.5 GHz	0.900	-177.81	6.69	68.07	0.021	-7.32	0.338	-154.41
1.6 GHz	0.900	-179.98	6.27	65.54	0.021	-8.77	0.344	-155.44
1.7 GHz	0.900	177.96	5.91	63.08	0.020	-10.15	0.349	-156.43
1.8 GHz	0.899	176.00	5.59	60.67	0.020	-11.45	0.355	-157.38
1.9 GHz	0.899	174.12	5.30	58.30	0.020	-12.68	0.361	-158.30
2.0 GHz	0.899	172.31	5.04	55.97	0.020	-13.85	0.366	-159.22
2.1 GHz	0.899	170.54	4.80	53.67	0.020	-14.96	0.372	-160.14
2.2 GHz	0.900	168.83	4.58	51.40	0.020	-16.01	0.378	-161.06
2.3 GHz	0.900	167.15	4.39	49.16	0.019	-17.01	0.384	-161.99
2.4 GHz	0.900	165.49	4.21	46.94	0.019	-17.95	0.390	-162.93
2.5 GHz	0.900	163.87	4.04	44.73	0.019	-18.85	0.396	-163.88
2.6 GHz	0.900	162.26	3.89	42.54	0.019	-19.69	0.402	-164.86
2.7 GHz	0.900	160.66	3.75	40.37	0.019	-20.48	0.407	-165.85
2.8 GHz	0.900	159.08	3.62	38.21	0.019	-21.21	0.413	-166.86
2.9 GHz	0.900	157.51	3.50	36.05	0.018	-21.89	0.418	-167.89
3.0 GHz	0.900	155.93	3.39	33.91	0.018	-22.52	0.424	-168.95
3.2 GHz	0.900	152.79	3.18	29.65	0.018	-23.61	0.435	-171.12
3.4 GHz	0.900	149.64	3.00	25.40	0.017	-24.48	0.445	-173.38
3.6 GHz	0.900	146.45	2.85	21.17	0.017	-25.11	0.454	-175.73
3.8 GHz	0.900	143.23	2.71	16.93	0.017	-25.51	0.463	-178.17
4.0 GHz	0.900	139.94	2.58	12.69	0.017	-25.67	0.471	179.30
4.2 GHz	0.900	136.58	2.47	8.43	0.016	-25.60	0.479	176.67
4.4 GHz	0.899	133.14	2.38	4.15	0.016	-25.32	0.486	173.94
4.6 GHz	0.899	129.61	2.29	-0.17	0.016	-24.85	0.492	171.12
4.8 GHz	0.899	125.97	2.21	-4.53	0.016	-24.24	0.498	168.18
5.0 GHz	0.898	122.23	2.13	-8.94	0.016	-23.54	0.503	165.13
5.2 GHz	0.898	118.36	2.07	-13.41	0.016	-22.80	0.507	161.96
5.4 GHz	0.898	114.36	2.01	-17.95	0.017	-22.11	0.511	158.66
5.6 GHz	0.897	110.22	1.95	-22.56	0.017	-21.54	0.514	155.22
5.8 GHz	0.897	105.94	1.90	-27.26	0.018	-21.16	0.517	151.63
6.0 GHz	0.897	101.51	1.86	-32.04	0.019	-21.04	0.519	147.87

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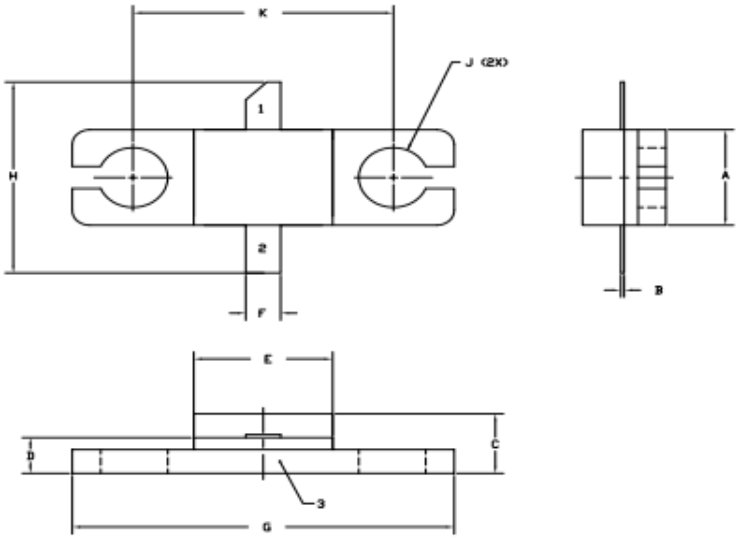
Product Dimensions CGH40010F (Package Type — 440166)

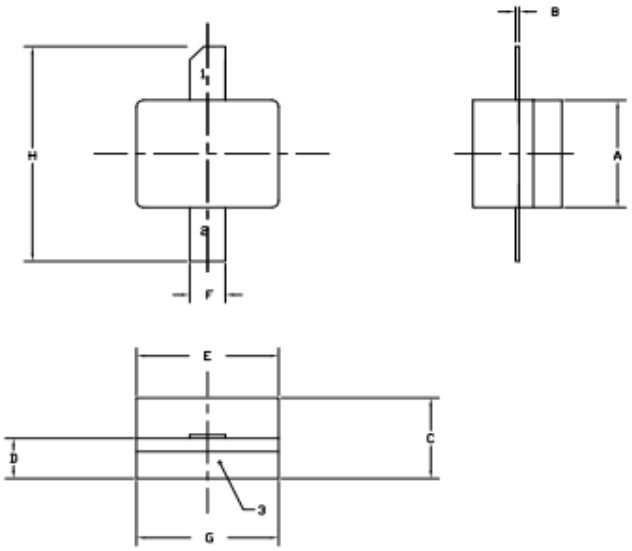


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.004	0.006	0.10	0.15
C	0.115	0.135	2.92	3.43
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.545	0.555	13.84	14.09
H	0.280	0.360	7.11	9.14
J	ø .100		2.54	
K	0.375		9.53	

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Product Dimensions CGH40010P (Package Type — 440196)



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.003	0.006	0.10	0.15
C	0.115	0.135	2.92	3.17
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.195	0.205	4.95	5.21
H	0.280	0.360	7.11	9.14

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

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Product Ordering Information

Order Number	Description	Unit of Measure	Image
CGH40010F	GaN HEMT	Each	
CGH40010P	GaN HEMT	Each	
CGH40010F-TB	Test board without GaN HEMT	Each	
CGH40010F-AMP	Test board with GaN HEMT installed	Each	

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