DC Grid Discriminating Protection

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To my loving parents, António and Benvinda,
for their encouraging words and hard work
which supported my education in multiple ways.

Abstract

High-voltage direct current (HVDC) has been proven an affordable and technically capable solution to bring vast amounts of power over long distances, though overhead lines, underground or undersea cables. As a result, a large number of point-to-point HVDC links appeared in several locations over the last decades. The technological step currently going on is the connection of point-to-point links to form a multi-terminal dc (MTDC) grid, a configuration that would bring several advantages. The construction of MTDC grids faces a few technical challenges, where the most notorious one might be dc grid protection.

This thesis presents protection strategies for MTDC grids equipped with different dc fault clearance and isolation devices. These include ac circuit breakers (ACCBs), converters with fault blocking (FB) capability, dc circuit breakers (DCCBs) and fast dc disconnectors (only for isolation purposes). Each of these strategies in presented in a chapter, where the steps of the protection strategy are described and overvoltage suppression methods are proposed. The protection strategies include dc fault detection and dc fault discrimination algorithms. In literature, extensive research is available regarding dc fault discrimination, potentially the "hottest" topic in dc protection. In this thesis, discrimination algorithms are proposed being those based on analysis of local currents and voltages. Thus, link communication channels are not required, which reduces the overall decision-making time.

The performance of the developed protection strategies is tested in PSCAD/EMTDC environment. DC faults are applied on two MTDC grids, including a 4-terminal meshed grid and the CIGRE 11-terminal dc grid. The main outcomes of this thesis include the discriminative fault criteria and the tailored protection strategies for dc grids equipped with either ACCBs, FB converters or DCCBs as main fault current clearance devices.

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The development of this piece of work was only possible thanks to the support of extraordinary people.

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"Rhaid i ni ddysgu i fyw gyda'n gilydd fel brodyr, neu farw gyda'n gilydd fel ffyliaid."

"We must learn to live together as brothers or perish together as fools."

"我们必须学会像弟兄一样一起生活，否则我们将如愚人一般一同灭亡."

"Devemos aprender a viver juntos como irmãos ou perecer juntos como tolos."

"අපි සහෝදරයෝ ලෙස එකට ජීවත් වීමට හෝ මෝඩයෝ ලෙස එකට මිය යාමට ඉගෙන ගත යුතුය."

"Ya kardeş gibi birlikte yaşayacağız ya da aptallar gibi birlikte Yok olacağız." [1]

Martin Luther King Jr.

[1] Order of languages: Welsh, English, Chinese, Portuguese, Sinhala and Turkish.

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List of abbreviations

AC	Alternating Current
ACCB	AC Circuit Breaker
CIGRE	Conseil International des Grands Réseaux Électriques (International Council on Large Electric Systems)
CRCC	Comparison of Rate of Change of Current
DEM	Detailed Equivalent Model
DC	Direct Current
DCCB	DC Circuit Breaker
FB	Fault Blocking (Converter)
FD	Fast DC Disconnector
HB	Half-bridge (Converter)
HVDC	High-voltage DC
IGBT	Insulated Gate Bipolar Transistor
IRENA	International Renewable Energy Agency
MMC	Modular Multi-level Converter
MTDC	Multi-terminal DC (Grid)
OHL	Overhead Line
P2Gnd	Pole-to-ground
P2P	Pole-to-pole
PPS	Progressive Protection Strategy
PSCAD/EMTDC	Power System Computer Aided Design/Electromagnetic Transients including DC
VSC	Voltage Source Converter
XLPE	Cross-linked Polyethylene

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Chapter 1

Introduction

1.1 Background and Motivation

In April 24, 2017, world population reached 7 500 million people [1]. This number is expected to increase (from 5 278 million in 1990) to 9 700 million people by 2050 [2]. This impressive demographic growth brings numerous social and technological challenges to society including suitability of urban population, food supply, energy demand, among others.

Demographic and industrial growth lead today's society to be very dependent on electric energy. This can be obtained from various more or less environment friendly sources. Civil society is relatively well educated and aware of their ecological footprint, impacts of fossil resources and of renewable generation. This lead to organisation of numerous initiatives around the world to demand for environment friendly energy policies. As one of the results, an historical mark was achieved by November 4th, 2016, where representatives of 195 countries signed the "Paris Climate Agreement". This is a worldwide deal to mitigate global warming effects in the years to come. The deal includes energy policies to reduce greenhouse gas emissions such as reduction of fossil based energy while increasing the renewable energy generation mix.

Fig. 1.1 illustrates growth of renewable energy capacity worldwide. As observed, the year 2016 transgressed for the first time the 2 000 GW installed capacity. Notwithstanding, a continuous investment in renewable sources of energy is well expected as the way forward.

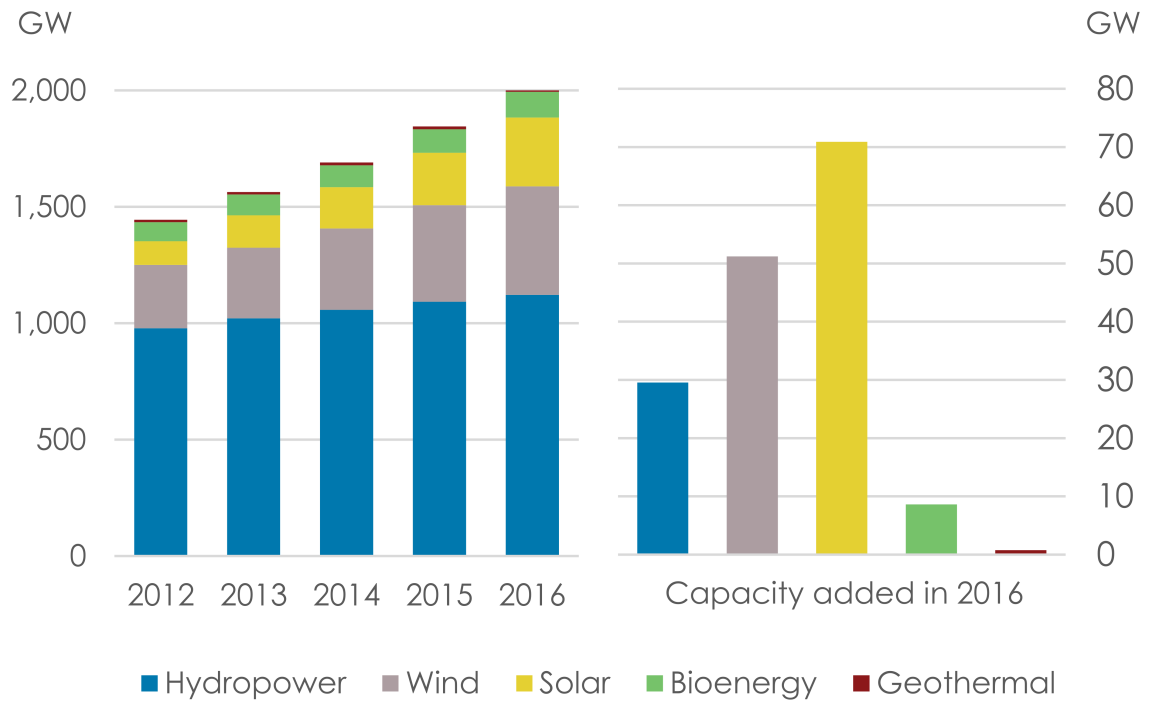

Fig. 1.1 Global renewable capacity growth by 2016. Courtesy of IRENA [3].

Even renewable energy faces a challenge nowadays: which locations have the most favourable renewable energy potential? Over the last decades, deserts have gathered attention due to the immense solar energy potential. "Within 6 hours, deserts receive more energy from the sun than humankind consumes within a year", quoting [4]. The North Africa desert is particularly of interest as it could fuel Europe with large amounts of renewable energy. The development of such a project is dependent of efficiency of solar cells and transmission network, but mostly of political initiative. A long-term agreement between countries around the Mediterranean Sea would be necessary to provide a sustainable operation strategy, economic compensation, investments costs and maintenance costs.

An area with an immense potential renewable generation of 100 GWh [5] is the North Sea. This offshore energy potential has lead in 2010 to the creation of the North Seas Countries' Off-shore Grid Initiative, a joint initiate from the energy authorities of the ten countries of the North Sea region. Their mission is to find out the best way to connect the large amounts of available offshore wind energy to mainland Europe. The main goal is to encourage the development of an offshore grid infrastructure with a focus on multi-terminal,

multi-vendor, high-voltage direct current (HVDC) transmission system [6]. In addition, European Union has been sponsoring major research projects on the area of offshore grid technologies and HVDC transmission. Examples include the TWENTIES, MEDOW, and PROMOTioN projects [7].

At the present time, a number of point-to-point HVDC links have been built. Fig. 1.2 shows inland and offshore high-voltage links in several countries at the North of Europe. Offshore HVDC links (in purple) are placed in several locations including the North Sea, English Channel, Baltic Sea and Irish Sea.

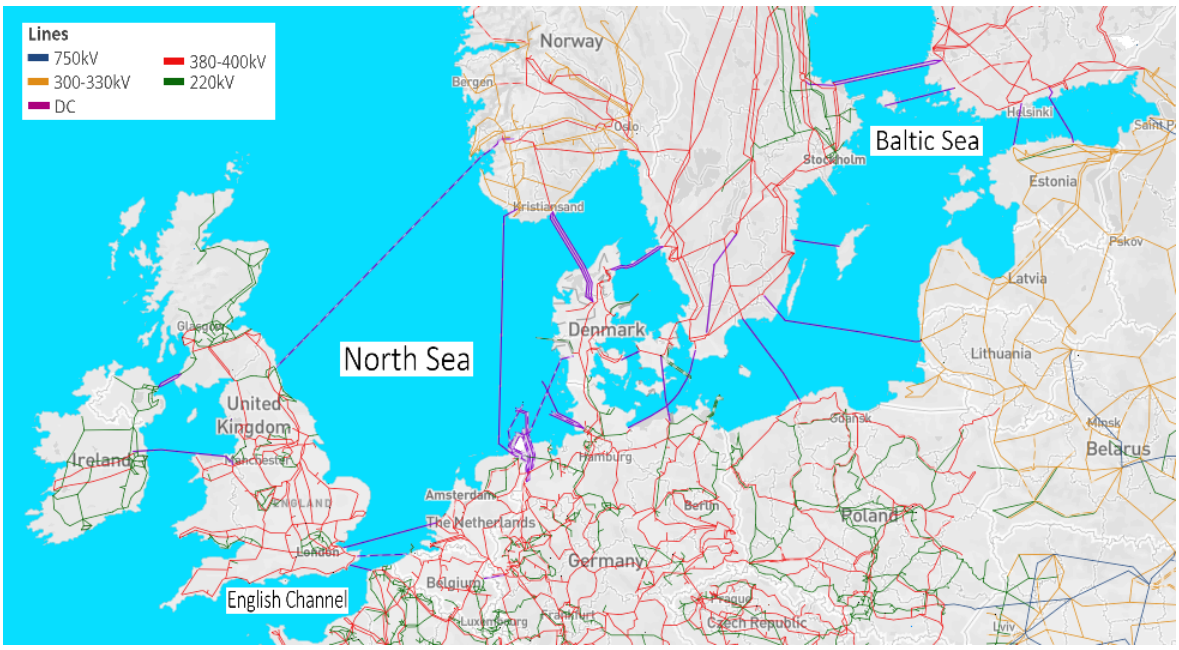

Fig. 1.2 Map of existing or under-construction high-voltage links around the North Sea and the Baltic Sea regions. Notice that most of the offshore links are in HVDC transmission. Adapted from [8].

There are several economic, technical and social reasons to use dc transmission instead of traditional ac transmission. The break-even distance, occurring when dc transmission becomes economically more attractive than ac transmission, is typically considered to be ∼60-100 km for cables and up to ∼800 km for overhead lines (OHLs) [9–11]. In terms of technical advantages, dc links feature fewer power losses and a higher power transmission capacity with the same conductor in comparison with ac transmission. The voltage drop in dc systems is almost negligible and therefore, there is no need of reactive power compensation. Additionally, dc links are ideally free of skin effect and of time varying magnetic field;

thus, dc systems may be used nearby sensitive communication systems. The use of cables is particularly encouraged due to political and environmental constraints on consenting and building new OHLs. Such a consideration led to the construction of the first onshore European HVDC cable, where the construction of new OHLs had social acceptance issues [10].

HVDC transmission systems are classified as back-to-back, point-to-point and multi-terminal dc (MTDC) grids. Back-to-back systems have an inverter and a rectifier stations at the same building (or geographically close). They are used to connect ac grids with different operating frequencies or areas that may be asynchronous. Point-to-point systems are used to transmit large amounts of power from a generation point over long distances to a load point. These constitute currently the most used configuration of HVDC systems. In fact, a number of point-tot-point links has proliferated in several locations around the world. Fig. 1.3 shows the installed capacity of HVDC systems in the world, which has an exponential behaviour.

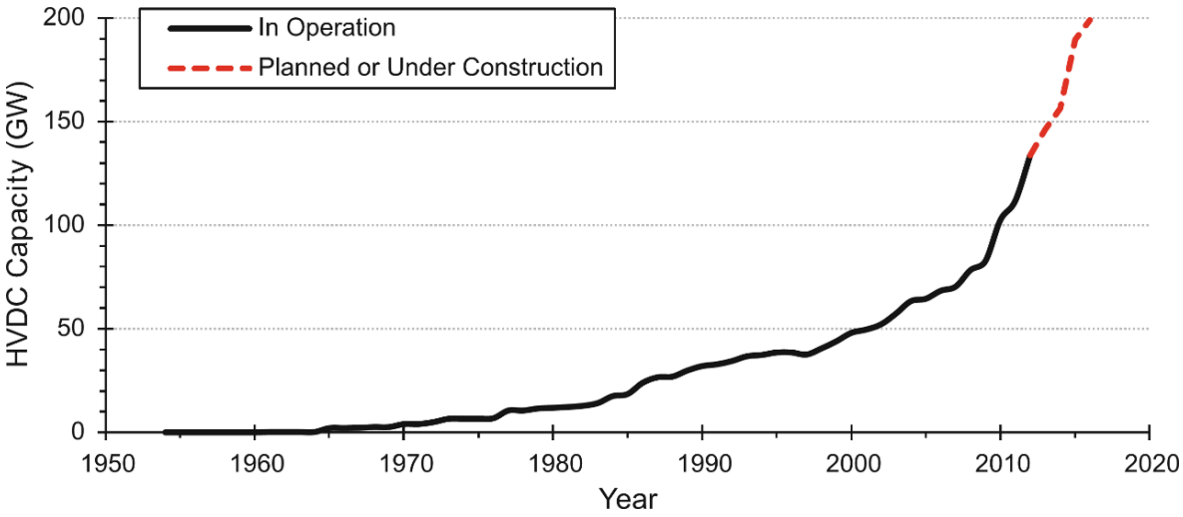

Fig. 1.3 Evolution of the installed HVDC capacity worldwide [12].

The development of MTDC grids comprise the next technical step. These are formed by connecting more than two converters, resulting in a radial or meshed MTDC grid. This grid is seen as a reliable solution for the next generation of power systems transmission [13, 5, 11]. For instance, it has been recognized that an MTDC grid in the North Sea may bring several benefits, including the exchange of reserves between Great Britain, Norway and Continental European grids, supply of energy to offshore platforms such as gas stations, access to wider power market areas, and an increased security of supply [13]. In spite of

the great advantages, few MTDC grid projects have been developed so far due to technical challenges, political and economic drivers.

1.2 Research Objectives

The feasibility of dc networks is currently being driven by industrial competition. Areas with substantial research development include HVDC converters, operation and control, power electronic devices, HVDC cables, dc power flow controllers, dc circuit breakers (DCCBs), dc protection strategies, dc-dc transformers and standardisation issues [5, 14–17]. Among these, dc fault protection is recognised as potentially the last major technical barrier to developing reliable MTDC grids.

DC protection can be divided into two categories: dc protection devices and dc protection strategies [5]. Devices that can be used for dc grid protection include DCCBs, converters with current fault blocking (FB) capability and ac circuit breakers (ACCBs) [18, 19], see Fig. 1.4.

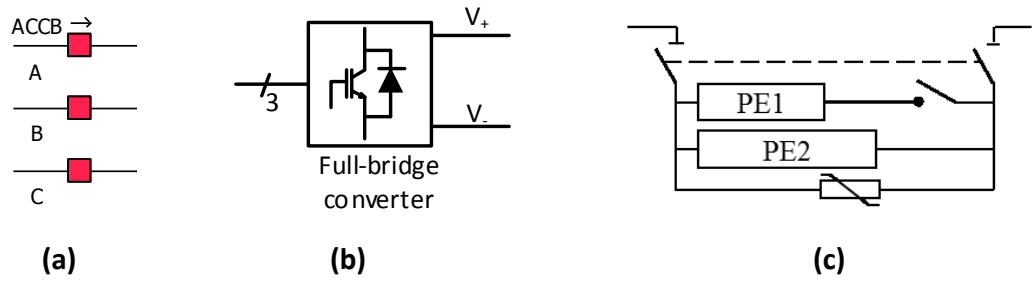

Fig. 1.4 Devices that lead to dc fault clearance include (a) ACCBs, (b) converters with FB capability and (c) DCCBs.

Although high-voltage DCCBs have been thoroughly investigated over the last years, the technology is still commercially unavailable[20]. Even when DCCBs become technically feasible, their integration to HVDC projects may be prohibitive in the short term due to economic constraints. Therefore, alternatives such as ACCBs and converters with fault current blocking capability are under consideration on several dc protection studies.

Ideally, only the faulty link should be isolated from the non-faulty network. However, this approach is only possible if DCCBs are used. In addition,faulty link discrimination comprises a great challenge as well. Discrimination should be based only on local dc currents and voltages and it should be achieved in a period of a few milliseconds only. This is a requirement due to dc fault current rate of change of potentially several kA/ms.

Investigation of protection algorithms for dc grids is being carried out in several directions including adaptability of ac protection methods for dc systems, communication based methods and current or voltage derivative methods. The aim of these algorithms is to quickly detect and discriminate a dc fault. The development of innovative algorithms for dc grid discriminating protection will enhance the feasibility of MTDC grids. This is the main challenge addressed in this thesis where the research objectives are as follows:

1. To develop a fundamental understanding of pole-to-pole (P2P) and pole-to-ground (P2Gnd) fault behaviour, dc protection requirements and modelling of MTDC grids;

2. To propose dc fault discriminating algorithms:

   (a) independent of link communication;

   (b) robust to link type (cable, OHL, and both cable and OHL in the same link), MTDC grid operation (monopole, bipole) and configuration (radial, meshed).

3. Protection strategies should be developed for grid equipped with:

   (a) ACCBs:
   all the ACCBs need to open in order to clear dc fault currents. A protection strategy should minimise the negative effects of dc grid outage.

   (b) Converters with FB capability:
   all the converters are required to block in order to clear dc fault currents. A protection strategy should minimise the negative effects of dc grid outage.

   (c) DCCBs:
   only the DCCBs placed at the faulty link should open. Hence, a protection strategy should identify the faulty link in a quick and accurate manner.

4. Lastly, the strategies with ACCBs, FB converters and DCCBs should include methods to suppress overvoltage events resultant from P2Gnd faults in symmetrical monopole networks.

1.3 Thesis Structure

This thesis is divided in eight chapters, being those organised as follows:

Chapter 1 introduces the topic of research and the work's motivation. The objectives of the thesis are stated and the publications are given.

Chapter 2 focus on the reviewing the literature on protection for HVDC grids. The challenges and requirements of dc protection are highlighted. Protection algorithms are grouped, described and critically reviewed. Devices that could provide dc fault isolation or clearance are described. Then, a number of protection strategies is given and grouped according to the used fault clearance devices and protection philosophies. The chapter ends with a discussion and prospective research trends in dc protection.

Chapter 3 presents the modelling of MTDC grids, which was performed with PSCAD/EMTDC. Two dc grids are modelled, including a 4-terminal and the CIGRE 11-terminal grid. The pre-fault current and voltage values are given for each grid. Equipment modelling is given in detail, including HVDC converters, dc links, protection devices and logic protection units.

Chapter 4 describes the fault detection and fault discrimination algorithms. The proposed algorithms analyse only local dc current and voltage since communication channels represent a technical restriction for a fast dc protection. In this chapter, two algorithms are given to discriminate only the faulty link. A third algorithm is presented to reclose fast dc disconnectors (FDs) of DCCBs, if necessary.

Chapter 5 describes a protection strategy for dc grids equipped with ACCBs. The strategy includes the fault detection and fault discrimination algorithms from Chapter 4. A non-minimum opening philosophy is proposed while a progressive recovery of non-faulty parts of the network is achieved. Overvoltage suppression is performed with discharging circuits. Simulation results are given in detail for a P2P and for a P2Gnd fault case.

Chapter 6 describes a protection strategy for dc grids equipped with converters with FB capability. The strategy includes the fault detection and fault discrimination algorithms from

Chapter 4. A minimum opening philosophy is proposed. An overvoltage suppression method is proposed and takes advantage of the converter configuration. Hence, additional hardware such as link discharging circuits are not necessary. Simulation results are given in detail for a P2P and for a P2Gnd fault case.

Fig. 1.5 illustrates the chapters' content and connections between chapters.

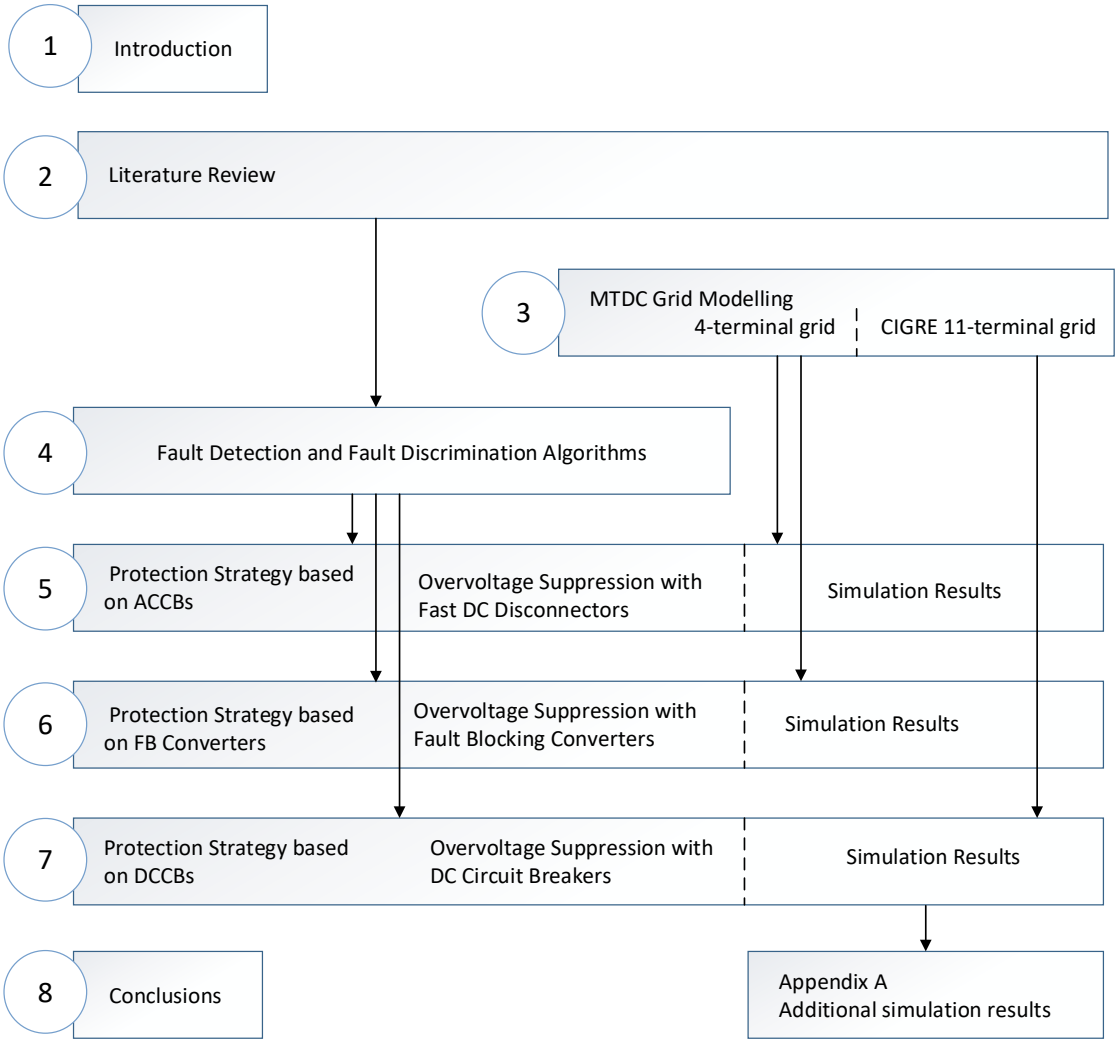

Fig. 1.5 Thesis structure per chapter.

Chapter 7 describes a protection strategy for dc grids equipped with DCCBs. The strategy includes the fault detection and fault discrimination algorithms from Chapter 4. A minimum opening philosophy is proposed, hence only the DCCBs discriminated as internal the fault

link are opened. Simulation results are given in detail for a P2P and for a P2Gnd fault case. These faults are applied at the CIGRE 11-terminal dc grid.

The thesis ends with Chapter 8. Conclusions of the thesis are discussed in several categories and a recommendations for future work are suggested.

1.4 List of Publications

During the doctorate study, three document have been written for publication. These resulted from a collaboration between Cardiff University and the industrial sponsor GE's Grid Solutions (former Alstom Grid UK Ltd). The publications are given below:

1. Rui Dantas, Jun Liang, Carlos E. Ugalde-Loo, Andrzej Adamczyk, Carl Barker, Robert Whitehouse, "Progressive Fault Isolation and Grid Restoration Strategy for MTDC Networks" IEEE Transactions on Power Delivery, (Accepted)
2. Rui Dantas, Jun Liang, Carlos E. Ugalde-Loo, Andrzej Adamczyk, Carl Barker, Robert Whitehouse, "Protection Strategy for Multi-terminal DC Networks with Fault Current Blocking Capability of Converters" in 13th IET International Conference on AC and DC Power Transmission (ACDC 2017), pp. 1–7, Manchester, 2017.
3. Rui Dantas, Jun Liang, Carlos E. Ugalde-Loo, Andrzej Adamczyk, Carl Barker, Robert Whitehouse "DC Grid Protection: Review and Research Trends", Electric Power Systems Research (Under Review)

1.5 List of Contributions

The work developed during this doctorate brings new contribution to the research field of dc grid protection. The main contributions are listed below followed by a brief description.

1. Protection algorithm of comparison of rate of change of dc current (CRCC).

   In the literatures, fault discrimination based on travelling waves typically consists on capturing the time period between consecutive waves, which represents a certain distance. The CRCC algorithm differs from existing literature in the way that fault

discrimination is achieved thanks to a magnitude comparison of travelling waves and not due to the time period between travelling waves.

2. Protection strategy for MTDC grids based on ACCBs.

   In the literatures, a method that uses ACCBs to clear faults in dc grids is able to isolate the faulty link and restore the network in 500 ms (described at Section 2.5.1). In this thesis, a progressive strategy is proposed which is able to reduce the grid outage time and offers back-up protection. These methods are compared in section 5.4.2.

3. Protection strategy for MTDC grids based on FB converters.

   In literature, not much attention is paid to converters with fault blocking capability (reviewed at Section 2.5.2). In this thesis, a protection strategy is developed to clear and isolate a dc fault, thanks to the operation of FB converters and dc link disconnectors.

4. Protection strategy for MTDC grids based on DCCBs.

   There are several algorithms in the literature that consider DCCBs for dc fault protection and a few protection philosophies might be possible (as detailed at Sections 2.5.3 and 2.5.4). In this thesis, DCCBs are operated according to the proposed discrimination algorithms (as the CRCC) while the MTDC grid model is of high complexity (11 terminal CIGRE dc network as seen at Section 7.3).

5. Overvoltage suppression methods with FB converters.

   In literatures, overvoltage suppression is typically based on switches that connect a link pole to the ground. In this thesis, these devices are not required for grids equipped with FB converters as these are able to provide the overvoltage suppression function.

6. Publication of an IEEE paper and presentation in an IET conference.

   Dissemination of the findings has been made through a publication in a international recognised journal and presentation in a internationally recognised conference. At the time of writing, these is a still other journal publication waiting for decision. In addition, all the research finding were shared with the industrial sponsor.

1.6 Project Participation

The doctorate thesis was funded by the project "DC Grid Discriminating Protection", delivered by GE's Grid Solutions (former Alstom Grid UK Ltd) to School of Engineering, Cardiff University, UK. The project had a three years duration and ran from 01/04/2014 until 31/03/2017.

The working tasks include investigation of fault detection and discrimination strategies for a simple 4-terminal dc grid and for the CIGRE 11-terminal dc grid.

Chapter 2

Literature Review

2.1 Introduction

In recent years, projects with large power generation capabilities harvesting energy from renewable sources have appeared. Examples include the 6.4 GW Xiangjiaba hydro power plant in China [21] and offshore wind farms in the North Sea [13]. Other technically challenging ideas that have been considered include a mainland European Supergrid [22] transmitting large amounts of wind and hydro power from the North and solar power from the South to a number of European countries [9]. These projects share a common geographical constraint: power generation is available in remote locations which are far from cities and main load centres. Although the construction of such environmentally friendly energy projects requires political cooperation between countries, the technical issues may be overcome by adopting HVDC power transmission [14].

Substantial research has been carried out into dc grids, particularly for open sea areas, in terms of topologies and control [23]. However, offshore wind farm configurations are greatly dependent on the cost of laying cables and of the adopted protection devices, which in turn have a direct influence on the selection of a dc protection strategy in terms of the maximum power loss allowed following a fault.

Protection is currently one of the main technical impediments for the construction of a MTDC grid. ACCBs can adequately protect point-to-point HVDC connections, but the same protection concept might not be easily acceptable for an MTDC grid as the de-energization of the entire system is required [24]. Converters with FB capability are able to interrupt

the ac infeed current to the dc side, and hence, clear dc faults currents [25]. This option is faster than using traditional ACCBs but comes at a cost. DC circuit breakers (DCCBs) are a potential solution to selectively isolate a faulty link [26, 27]. However, two major aspects have to be considered regarding the hardware and software of future protection units. Firstly, DCCBs may have limited current breaking capabilities [11]. Secondly, dc protection algorithms are not established yet and represent a technology still underdeveloped [5]. It is agreed though that methods leading to a logical decision of opening (or not) a DCCB based on local measurements should ensure discrimination in a fast and reliable manner.

This Chapter carries out an in-depth critique review of dc fault discrimination methods and covers the protection methodologies and devices available in the open literature. In addition, improvements to existing dc protection strategies are suggested and trends for the next generation of protection strategies are discussed.

2.2 Challenges of DC Protection

DC fault clearing is very challenging as both the breaking operation and time requirements are more demanding than those for ac fault clearing. Firstly, in dc systems there is no natural zero-crossing point, meaning that dc currents have to be driven to zero and the fault energy has to be dissipated by the interrupting device. Secondly, dc fault currents should be interrupted within a few milliseconds to limit the prospective fault current magnitude. In [16] a period of less than 2 ms is recommended for fault clearance, which is a much shorter time in comparison to ac protection. This is due to the low link impedance and the fast current increasing behaviour, which can be of tens of kA/ms [28]. The recommended time period is a challenging target that may become feasible if fast dc current clearance devices such as fast DCCBs or FB converters are employed.

Fault current breaking devices and discriminative protection strategies are a major research topic in HVDC. In this context, the DCCB has been identified as a key component, although it is not yet commercially available. However, the use of other fault interruption devices such as FB converters may justify the avoidance of DCCBs in dc grids. In addition, the use of traditional ACCBs might be feasible for a dc network of limited size. Hence, dc protection comprises a wide area of research with a number of potential research directions.

2.2.1 Requirements for Protection

The main protection requirements for ac or dc networks are listed below [14, 16]:

(a) Sensitivity: detection of a faulty link only if a fault is present (not in normal operation);

(b) Discrimination (or selectivity): correct identification of faulty and non-faulty links;

(c) Speed: the maximum combined fault detection time and protection operation time must be short enough to prevent equipment damage and system instability;

(d) Reliability: the protection scheme performs correctly by considering main and backup criteria;

(e) Seamlessness: after the fault clearance, the remaining part of the system continues to operate in a secure state;

(f) Robustness: detection of faults in normal or degraded mode and discrimination from any operational events.

2.2.2 Grid Behavior Under a DC Fault

A number of factors contribute to the severity of a dc fault. The current and voltage behaviour is influenced by fault resistance, equivalent capacitance of links and converters, fault location, short circuit ratio of the ac network and current rate limiting devices, if applicable [26]. If current rate limiting dc reactors are used at the dc link ends, an extra time of a few milliseconds is allowed for protection decision-making and operation. The current rising rate limit is given by

$$\frac{di}{dt} = \frac{\Delta V_{max}}{L} \tag{2.1}$$

where ΔV_{max} is the maximum P2Gnd voltage. The design of dc reactor L should comply with the maximum breaking capabilities and decision time of the protection scheme. For example, for a 320 kV dc grid with 10% maximum overvoltage, a reactor of 100 mH is recommended to limit the current rise to 3.5 kA/ms [27].

In order to illustrate the voltage and current profile during a dc fault, a 4-terminal dc grid has been modelled (see Fig. 2.1). The dc network operates with a dc voltage of $\pm$ 200

kV and has half-bridge (HB) modular multi-level converters (MMCs). These converters are chosen as are a research preference of the industrial sponsor.

The dc cables are represented as frequency dependent (phase) models. Links 12, 14 and 24 have a length of 200 km while link 23 has a length of 50 km. A 50 mH current rate limiting device is considered at each link end. A grounding point is placed between each ACCB and converter station. This is composed of a star inductance with a high impedance earthing arrangement [29].

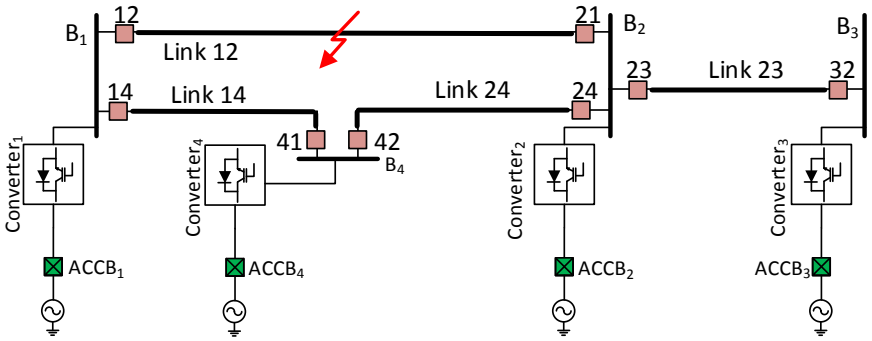

Fig. 2.1 Four-terminal dc network.

A fault is modelled as a time controlled switch in series with a resistance. These are placed between the positive pole and the negative pole; and between the positive pole and ground. The development of a fault with an arcing period and its potential effects, such as modification of travelling wave fronts, are not analysed in this thesis and are recommended for future research.

P2Gnd and P2P faults are described in this Section. Fig. 2.2 illustrates generic profiles for dc current and dc voltage. These are based on a positive-P2Gnd and a P2P fault occurring at 2 ms in the middle of link 12 (see Fig. 2.1) while current and voltage profiles are captured on dc relay 12.

P2Gnd faults in symmetrical monopole topologies lead to a voltage shift: the voltage of the faulty pole moves towards the ground level, pushing the voltage on the other pole to twice the pre-fault value as seen in Fig. 2.2 (a). This event causes an overvoltage. During this transition, a temporary current oscillation occurs which might not be sensed by overcurrent algorithms (Fig. 2.2 (c)). In practical HVDC schemes, pole insulation is typically protected against overvoltage by surge arresters with a protective level below 1.85 p.u.

P2P faults imply more severe conditions to dc links and the surrounding equipment. An overcurrent might occur in the links of the whole grid, with a rate of rise that could reach tens of kA/ms (Fig. 2.2 (d)) [30]. This occurs with a quick (but not instantaneous) voltage collapse in all dc terminals as seen in Fig. 2.2 (b).

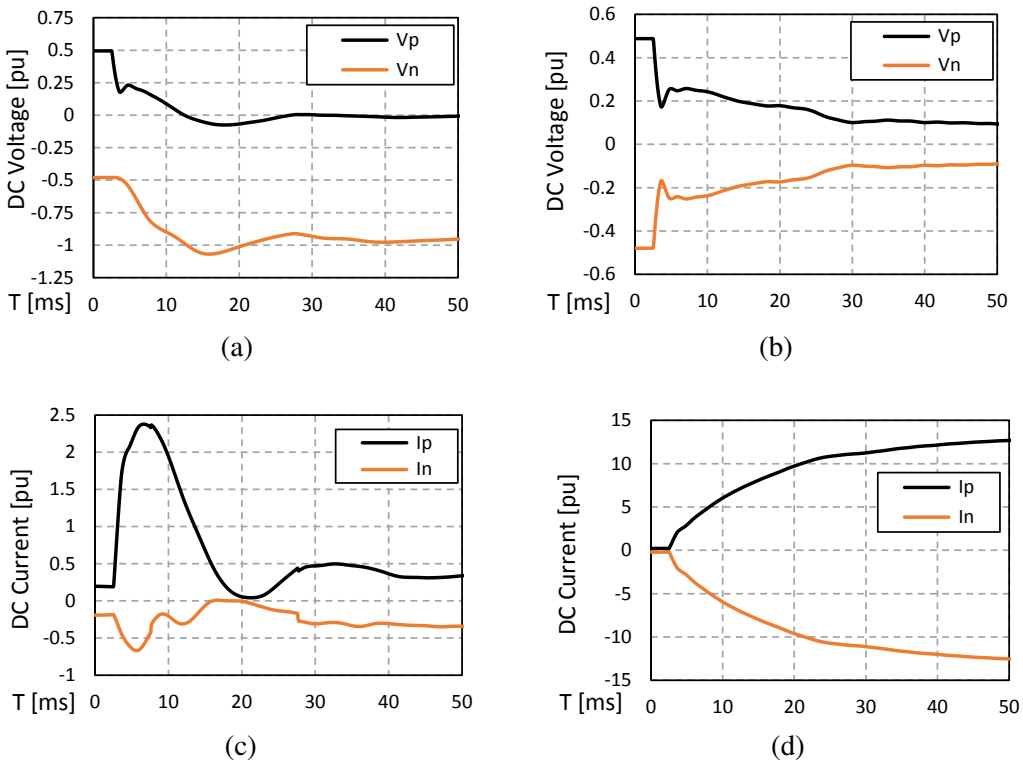

Fig. 2.2 DC voltage profile for (a) a positive-P2Gnd fault in symetric monopole grid and (b) for a P2P fault. DC current profiles for (c) a positive-P2Gnd fault and (d) a P2P fault.

2.3 Fault Detection and Discrimination Methods

The role of a protection strategy for dc links is given Fig. 2.3. Current and voltage sensors are placed at each dc line end. These data are processed by a number of algorithms in a logic unit. Protection algorithms are categorised in three groups. Firstly, fault detection algorithms identify disturbance on a network. Secondly, fault discrimination algorithms identify the faulty link within a network. Lastly, fault location algorithms identify the approximate location of the fault within a known faulty link (*i.e.* fault distance to a link end).

In this Section, attention is paid to fault detection and fault discrimination algorithms while fault location is not treated. It could be argued that fault detection is not problematic

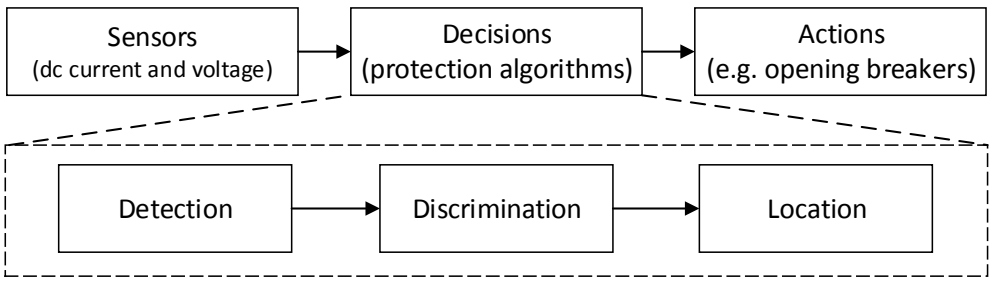

Fig. 2.3 Role of protection systems and stages of a protection strategy.

in MTDC grids since it may be achieved within 1 ms after the arrival of transient waves by using methods based on overcurrent, undervoltage, current derivative or voltage derivative [31]. Fault discrimination has been identified as the most challenging task from dc network protection [20]. Therefore, link discrimination due to dc faults 'is the main scope. Protection of busbars, converter stations, filters and other equipment is out of the scope of this Section.

2.3.1 Current and Voltage Magnitude-Based Methods

Overcurrent and directional overcurrent protection are simple methods to detect a fault either on ac or dc grids. A combination of magnitude, direction and duration criteria may be used to achieve partial discrimination.

The magnitude criterion is determined by either a fixed or a variable threshold corresponding to currents larger than the nominal link rating. The local direction criterion is determined by the current flow change at the initial transient stage of a fault. If current flows from the dc link to a busbar, the fault must be external. However, if the current flows from a busbar to the dc link, the fault can be either internal or external. Hence, only partial discrimination is achieved when the local direction current criterion is employed.

Fig. 2.4 illustrates the dc current profile for a potential internal dc fault (relay 12) and for an external dc fault (relay 23). On the potential internal fault, the dc current experiences an increasing behaviour after the arrival of the transient waves. This occurs at both ends of the faulty link and typically in one end of the non-faulty links. Moreover, if the dc current experiences a decreasing behaviour, this indicates that the fault is flowing from the dc link to the busbar. As a consequence, the fault must be external. The previous scenarios are valid

for a current sensor orientation from the busbar to the dc link. Hence, partial discrimination is easily achieved with the local current direction criterion.

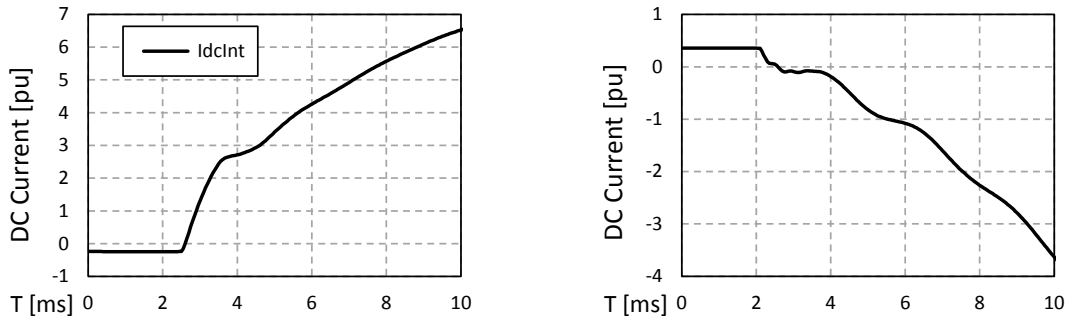

Fig. 2.4 DC current for (a) a potential internal fault and for (b) an external fault.

Voltage-based methods include undervoltage and overvoltage approaches [31]. The positive and negative pole voltages are monitored continuously, making protection decisions in accordance with predefined thresholds. These include a minimum and maximum voltage to detect cases of undervoltage or overvoltage. Fault detection by undervoltage is relatively faster than fault detection by overcurrent due to the transient capacitive discharge of dc links.

Similarly to local current methods, fault detection is easily achieved. However, discrimination may not be accomplished due to the fast voltage collapse in all dc terminals.

2.3.2 Derivative-Based Methods

Current and voltage derivative methods are suitable not only for dc fault detection but also for dc fault discrimination. A dc fault can be detected and/or discriminated by comparing the magnitude of a derivative signal with predefined thresholds [32].

In the case of a dc fault, the dc current and dc voltage change faster in the faulty link than in the non-faulty ones. To make this method practically feasible in dc networks, dc fault current rate limiting devices should be employed at the dc link ends. These devices, also know as link end inductors, perform as a smoothing barrier between the faulty and healthy parts of an MTDC grid [33]. The dc inductors have a negligible influence on the steady-state operation. However, in the case of a disturbance, the dc current rate of rising is limited and the voltage across the device is proportional to $L \times di/dt$. Hence, the thresholds considered by derivative-based methods are highly dependent on the rating of the link end inductors.

Without these, it would be difficult to distinguish an internal fault at the far end of the link from an external fault electrically close to the far end busbar. It should be borne in mind that the design of large dc reactors represents a technical challenge, an increased investment and an increased operational cost.

In [34], a discrimination algorithm employing three criteria is proposed. It includes a dc current rate of change criterion within a predefined time window (thus overcoming the noise disadvantage), a dc voltage derivative criterion and a current leakage criterion. In [32], a fault discrimination algorithm is proposed based on voltage derivative levels in combination with undervoltage and current direction criteria. In [35, 36, 33], the differential voltage magnitude, measured across the current rate limiting device at the transient stage, is used to discriminate a fault as internal or external. The strategy used in [37] considers a voltage derivative function to discriminate the faulty link within an MTDC grid. The strategies in [35, 36, 33, 37] take into account the damping provided by the current rate limiting device. Fault discrimination can be supported by other criteria; *e.g.* current direction of the first transient wave.

The discrimination approaches discussed in the previous references are slightly different among them but have the derivative method as the main core. With well-designed thresholds, this method leads to a correct discrimination of the faulty dc link at an early stage after the start of the fault. However, such a derivative approach has a few drawbacks. These include the sensitivity to noise interference, to fault impedance and to the rating of the current rate limiting device, which must be minimised. In addition, this method has been tested in networks mainly composed of cable links. The presence of overhead lines (OHLs) within the network might require adaptation of pre-set thresholds or of the rating of the current rate limiting device. Hence, this leaves a margin for further validation of the derivative concept on wider grid configurations.

Fig. 2.5 illustrates the current and voltage derivative profiles for a P2P fault at the middle of link 12 as seen by relay 12 (see Fig. 2.1). In Fig. 2.5 (a, c), the dc fault is applied on a cable while in Fig. 2.5 (b, d), dc fault is applied on a OHL (link 12 is replaced by an OHL). The magnitude of the derivative signal is the value compared with pre-set thresholds and that leads to fault discrimination. These values are slightly different between the two cases, which means that the thresholds should be different too. In addition, OHLs have a noticeable

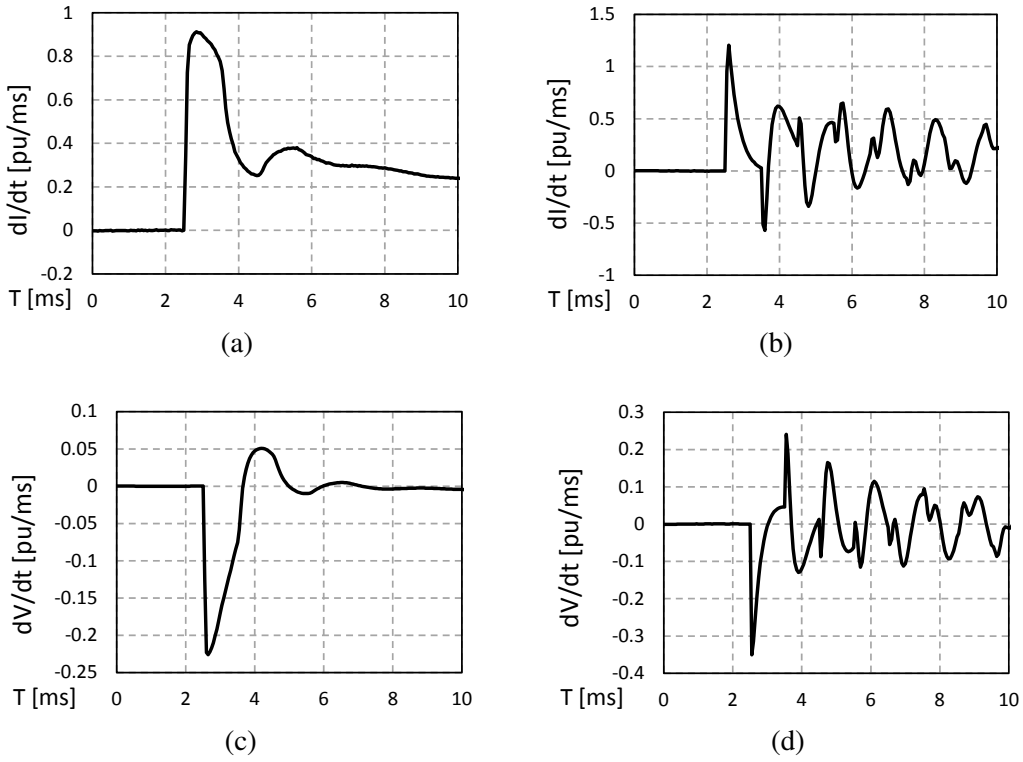

Fig. 2.5 DC current derivative profile (a) in a cable and (b) in an OHL. DC voltage derivative profiles in (c) a faulty cable and (d) in a faulty OHL.

high-frequency component which may affect the accuracy of sensors, causing calculation errors and a potential incorrect discrimination judgement. The discrimination algorithms proposed in this thesis (Section 4.3) minimise the issues aforementioned. The algorithm in Section 4.3.1 uses current derivative functions but does not require pre-set thresholds, which would be hard to calculate due to different link types and grid configurations.

2.3.3 Unit Protection Methods

The knowledge of the input and the output data of a dc link leads to a single equipment protection approach, know as unit protection. A communication channel is therefore required between both link ends. Hence, the link end relays have the ability to exchange information between them, but at the expense of a delay. Correspondingly, if only local data is available, a protection strategy falls in the non-unit protection approach.

Methodologies to achieve fault discrimination within the unit protection approach include the current difference and the current direction schemes (even with high impedance faults)

[38, 29]. The first method is based on the current difference I_{diff} between two sensors placed at the ends of the same dc link. In steady state, I_{diff} is equal to zero (neglecting noise interference and power losses); however, in the case of an internal fault, I_{diff} increases as the infeed current from both ends is different in magnitude. Once I_{diff} transgresses a pre-set threshold, the fault is discriminated as internal to the link. The second method is based on the comparison of the directions of dc current at the same pole and link. Hence, if both directions are positive, the fault must be internal. Conversely, if one current direction is negative, the fault must be external to that link.

Communication between dc relays is possible by adding a channel in parallel with the power dc link connecting both link ends; however, this induces transmission and processing time delays. Dedicated or non-dedicated communication channels for HVDC applications may be based on optical fibre technology. If the channel is dedicated exclusively to protection proposes, a transmission delay of 1 ms per 200 km may be incurred [38]. Although such a small transmission delay value is theoretically possible, in practice a larger delay is expected. Non-dedicated channels exhibit larger delays as the exchanged data packages are used not only for protection but also for other purposes such as control. For these channels, an additional delay may be considered in the case of corrupted data, which may be corrected by re-sending data packages. The processing delay (data concentrating, multiplexing and delay associated with transducers) is an ambiguous quantity and its measurement is not specified in current standards [39].

Time synchronisation is generally required in relays at both link ends for a suitable application of discriminative methods. This implies adding a delay that matches the link propagation constant delay (defined as $\gamma(\omega) = \sqrt{ZY}$, where $Z = R + j\omega L$ is the series impedance and $Y = G + j\omega C$ is the shunt admittance of the link).

Fig. 2.6 illustrates the application of the current difference method for a dc relay internal and a dc relay external to the faulty link. A positive-P2Gnd fault is considered in the middle of link 12. Relay 12 is internal and relay 23 external to the faulty link. Signal *'Iloc'* represents the local current, *'Irem'* the remote current and 'Idiff' the difference between both *'Iloc'* and *'Irem'*. A communication delay of 10 ms is assumed. It can be observed that for the internal relay (Fig. 2.6 (a)), *'Idiff'* initially increases. This occurs due to the initial positive rate of change of current on both ends of the faulty link. As a result, the fault is classified as internal.

Correspondingly, for the external relay (Fig. 2.6 (b)), *'Idiff'* initially decreases. As a result, the fault is classified as external.

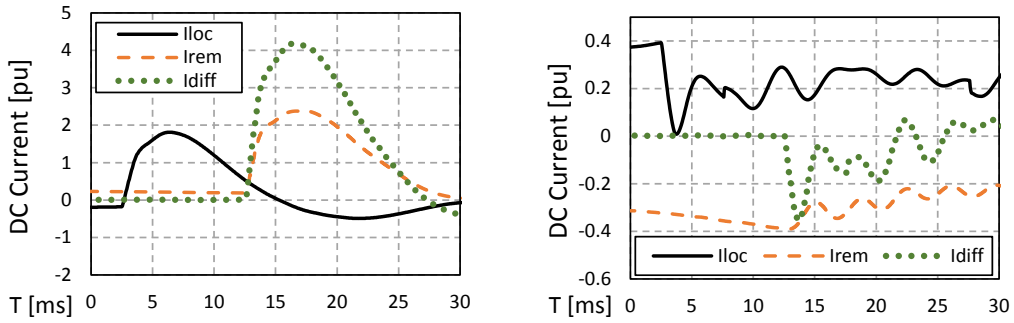

Fig. 2.6 DC current difference for (a) internal and (b) external fault.

It should be emphasised that the previously discussed time constraints may not be suitable for fast dc protection actions –especially considering long dc links. The China Southern Power Grid has HVDC links of nearly 1000 km [40]; these conditions introduce considerable time delays. Therefore, communication-based methods may be used only as backup protection for MTDC grids. Conversely, for short link lengths, these methods may be adapted to the main protection algorithms –as in the case of a number of submarine grids [41]. It should be known that the protection algorithms proposed in this thesis do not require dc link communications. Therefore, associated costs with link communication channels are avoided while fault discrimination is equally ensured.

2.3.4 Signal Processing and Other Methods

Signal processing techniques have been used in HVDC point-to-point configurations to detect the fault location within a known faulty dc link [42]. Adaptation of such techniques for fault location between links in radial or meshed dc grids is currently an expanding research area.

Travelling wave methods are based on the waves resulting from disturbances. These waves propagate along the dc link causing high-frequency oscillations which are continuously attenuated until they disappear. The wavelet analysis can be then used to decompose the characteristics of travelling waves [43]. Wavelets are defined by the wavelet function and a scaling function in the time domain [44].

The application of travelling wave-based methods relies on the accurate detection of arrival times between wave-fronts or on the energy of the travelling waves. These methods require an adequate equipment modelling and sensors with high sampling rate data from a few milliseconds interval –depending on the link propagation delay and link length [45, 46]. Additionally, a few milliseconds should be accounted for processing time [45]. Reference [47] provides practical techniques for detecting transient wave-fronts.

A different discrimination approach includes the distance (or impedance) protection method. This is commonly used in high-voltage ac networks as it achieves a highly successful rate of fault discrimination. It is based on the continuous monitoring of current and voltage, from where impedance Z is calculated and represented over an R-X plane. A number of boundaries or zones of protection are defined in this plane, including at least a primary and one backup protection zone [48]. Fault discrimination is achieved if the impedance seen by the relays falls within a zone during a pre-determined period of time.

The adaptation of the distance method to dc grids has been considered mainly for fault location [49]. Fault discrimination with the distance protection approach is challenging due to the initial transient current and voltage waveforms upon a fault, as these have high change rates which may induce measurement errors. Moreover, the grid frequency changes abruptly during the transient stage and no fundamental frequency can be defined for distance protection calculations.

2.3.5 Comparison and Discussion

Fault detection on dc grids can be based on simple methods such as undervoltage or derivative functions. However, fault discrimination is the main challenge. The local current direction criterion gives partial discrimination and should be considered as part of a primary protection strategy due to its simplicity. Current direction based on unit protection can also achieve discrimination. However, the use of communication-based methods is highly unlikely to be adopted as primary protection scheme, at least in the case of low impedance faults. This is due to the delay introduced by the communication channel and the processing delay which is highly dependent on the technology adopted.

The best-recognized fault discrimination algorithms are based on the current or voltage derivative approach. These are quick since the incident transient wave contains most of the

information required for decision making. These methods rely on the rating of current rate limiting devices which work as a separation between a faulty area and a non-faulty area. The feasibility of this method for dc OHLs and for P2Gnd faults on symmetrical monopole configurations requires more development as less attention is typically paid to these type of links and fault. Hence, the derivative method, although very promising, still has a room for improvement and validation.

Travelling wave-based methods with one terminal data analysis may have good discrimination characteristics but are highly dependent on the grid configuration. For example, these methods should be sensitive to the multiple reflections on meshed dc grids, to the grid configuration change (for example, due to the outage of dc links for maintenance purposes) and to the presence of OHLs and cables.

2.4 Converters, Fault Clearance and Isolation Devices

Protection strategies for MTDC grids are being developed using different converter types and current breaking technologies. This section gives a description of these devices together with combinations of them for protection purposes. Devices that lead to dc fault clearance include ACCBs, DCCBs and converters with FB capability.Devices that lead to dc fault isolation include DCCBs and fast (or ultra-fast) dc disconnectors. Fig. 2.7 shows a number of combinations of devices to protect a network against dc faults.

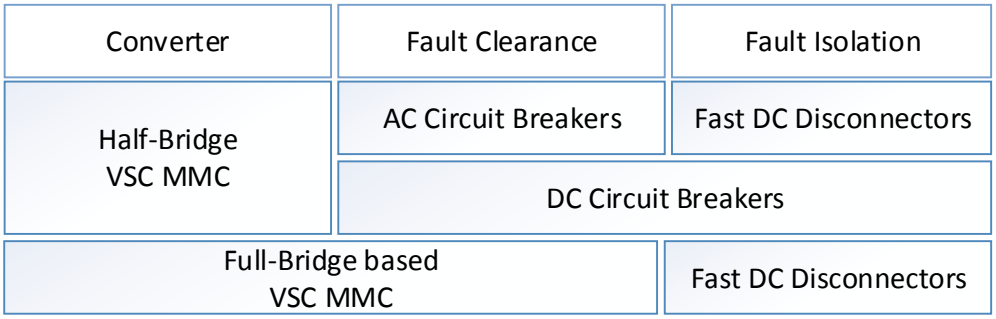

Fig. 2.7 Three combinations of potential protective devices for HVDC grids equipped with MMCs.

2.4.1 Converters for HVDC grids

Several types of converters appeared to serve HVDC transmission. Along the times, converters have evolved accordingly to power electronics technology. The main devices historically used on converters include the hot cathode (1920s-1960s), mercury-arc valve (since the 1930s), thyristor (since 1972), gate turn-off thyristor (GTO) and insulated-gate bipolar transistors (IGBTs), (since 1997) [50]. In terms of converter topology, these are mainly based on:

(a) Line commutated converter (LCC) built with mercury-arc valves (until the 1970s) or with thyristors (until present day) [20];

(b) Voltage source converter (VSC) built with switches with turn-off capability, as GTOs and IGBTs(since 1997) [51, 52]

VSCs appeared following developments in GTOs and IGBTs. These converters have several advantages over LLCs [20, 53]. VSCs do not require reactive power support and power control can be achieved on the four *P*-*Q* quadrants. Power reversal is easily obtained by changing the current direction while keeping the voltage level; thus it allows an easier integration with MTDC grids [14]. For this reason, industrial and academic research studies focus nowadays largely on VSC based converters.

VSCs also evolved along times. The topologies built to manufacture VSCs started with the two-level converter (1997 [54]), moving to the three-level converter (2002 [55]) and later to the promising technology with a MMC (2010, [56]).

MMCs were proposed in 2003 [57] and their first commercial application took place in 2010 [56]. Internally, an MMC is formed by an upper and a lower arm per phase. Each arm contains a smoothing inductance and a number of submodules, each one representing a voltage step. DC voltage rating is achieved in a scalable manner by arranging submodules in series.

Advantage os VSC based MMC technology includes the ability to operate in weak ac grids, black-start capability, fine control or active and reactive components and insignificant level of harmonic generation (hence filters may be not required).

Fig. 2.8 shows the configuration of an MMC. The submodules can be based on HB or full-bridge configurations.

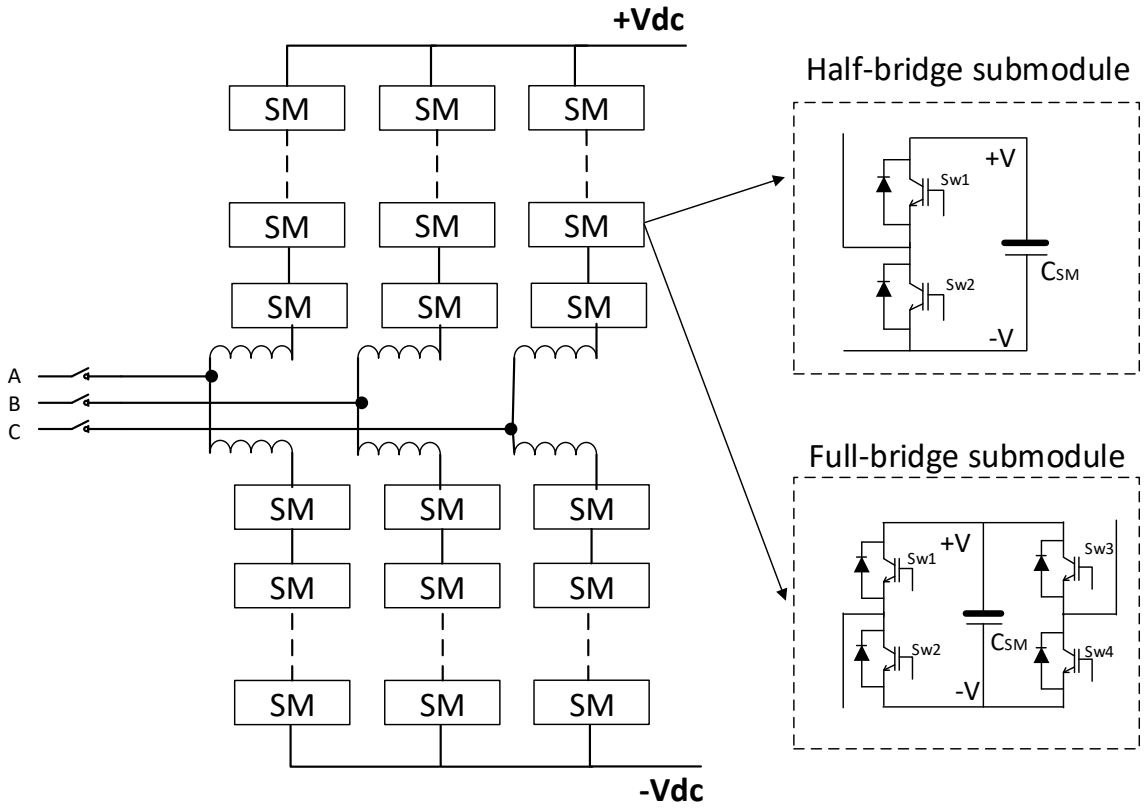

Fig. 2.8 MMC converter topology with submodule based on HB or FB configuration.

Half-Bridge Based Converters

Converters based on HB submodules are widely used in the HVDC market. HB based converters do not have fault clearance capability. During the transient fault, an ac infeed current flows through the uncontrolled free-wheeling diodes from the ac side to the dc fault side.

In order to protect the converter's diodes, a protective bypass switch and/or a thyristor is fired following fault detection. This allows most of the current to flow through the bypass device and not through the diodes [58, 59]. Fig. 2.9 illustrates a more detailed view of an HB submodule that includes a protective thyristor and bypass switch.

Full-Bridge Based Converters

In comparison with HB submodule converters (which have positive and zero voltage as output states), MMCs equipped with FB submodules can have three output states: positive voltage, zero voltage and negative voltage. This functionality gives the converter the possibility to

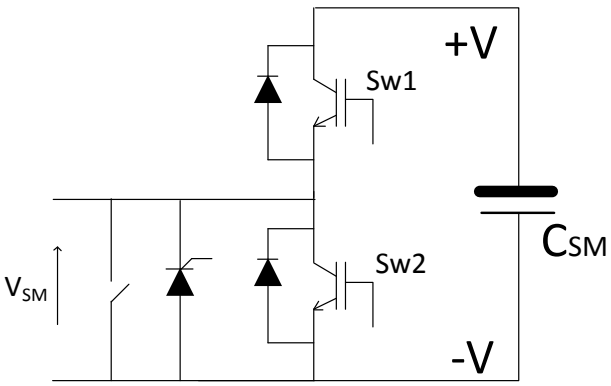

Fig. 2.9 Detailed view of an HB submodule of an MMC converter.

control and/or suppress dc currents. During dc faults, the current interruption can be achieved by removing the gate signals of all IGBTs, where the fault current path is illustrated in Fig. 2.10. The submodule voltage opposes the dc voltage and current flow decays to zero within a few milliseconds. In addition, an FB converter can operate as a static synchronous compensator (STATCOM), even during a dc fault, and support the ac side voltage [19].

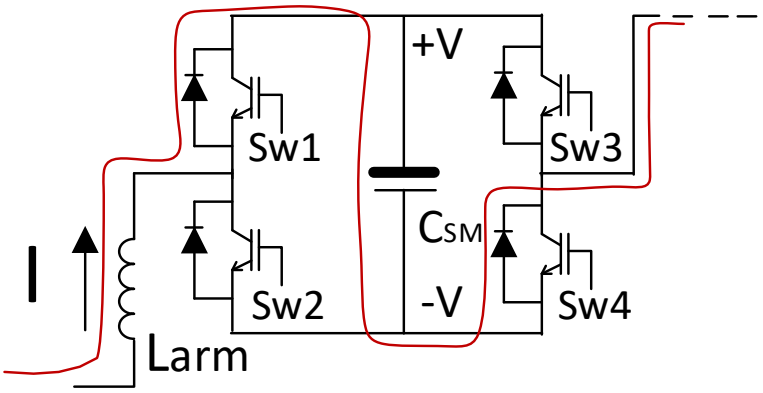

Fig. 2.10 FB MMC with submodule and fault current conduction path while in blocking mode.

FB converters are not limited to the full-bridge technology in each arm submodule, as other configurations might be included within this category. Examples include the alternate arm converter, which has an alternative topology based on FB submodules and director switches in each arm [19]. It aims to reduce investment and operation costs while keeping the benefits of a current interruption capability. In [60] a fault tolerant converter is described with FB cells on the ac side. These designs are also able to interrupt the ac side contribution to a dc side fault.

An MTDC grid equipped with FB converters requires ACCBs or FDs as fault isolation devices at dc links. After fault clearance, the ac side current decays quickly to zero but a dc side component flows on the dc links. This component decays to zero with an oscillation dependent on the natural frequency of the associated cables and/or OHLs. Hence, ACCBs on the dc side make use of the current oscillation to their advantage to isolate the dc fault. Alternatively, if FDs (devices that have no noticeable current breaking capability) are used on the dc side, fault isolation is delayed until the dc component decays to an approximate zero value.

The major drawbacks of the FB MMC are the higher conduction losses and relatively higher investment cost in comparison to converters based on HB MMC. In addition, fault clearance is achieved by blocking all converters associated with a dc network. Hence, the whole network suffers a temporary outage after the event of a dc fault.

2.4.2 DC Circuit Breakers (DCCBs)

DCCBs are able to interrupt dc current within a few milliseconds. The hybrid DCCB has recently emerged as a topology offering a good performance and low power losses in comparison with passive oscillation mechanical and power electronic DCCBs [61]. The design principle of a hybrid DCCB is based on three parallel branches as shown in Fig. 2.11. DC current flows in the primary branch under normal conditions. This branch has a fast mechanical disconnector and a power electronics switch. Once the low voltage electronic switch is turned off, the fault current commutates from the primary branch to the auxiliary commutation branch. Soon after, this facilitates the arc free opening of the mechanical disconnector at the primary branch. The third branch, based on a series of surge arresters, dissipates the energy and drives the current decay to zero. Not only the current magnitude is important but also the amount of energy that the breaker needs to dissipate. This energy not only depends on the fault current amplitude at the breaking instant but also on the system inductance and the driving electromotive force of the power system.

A number of manufacturers are making efforts to develop DCCBs. A few hybrid DCCB concepts have been analyzed in [61–65], a active current injection DCCB in [66], a fast switching DCCB in [67] and a power electronic DCCB in [68]. The DCCB design takes into account the interruption time, current and voltage ratings, nominal power losses and energy

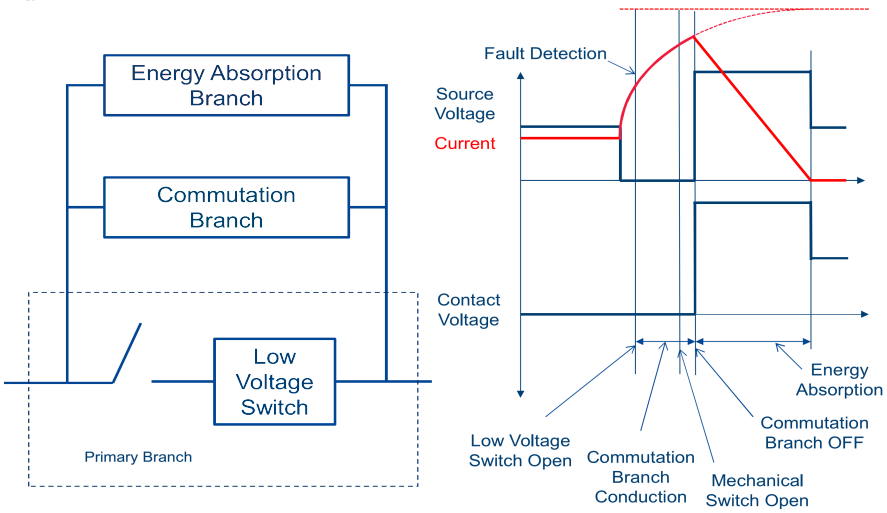

Fig. 2.11 An hybrid DCCB and operational steps for dc current interruption [62].

dissipation requirements. A voltage level of 120 kV and a fault clearance within 5.3 ms for a prospective fault current of 7.5 kA have been achieved with a hybrid DCCB as reported in [61]. Following interruption tests for a rate of current rise of 2.9 kA/ms, the arrester bank was able to dissipate the energy so that the fault current decays to zero. In addition, power losses during DCCB normal operation are exceedingly low [61].

2.4.3 AC Circuit Breakers (ACCBs)

ACCBs are electric switches used for fault clearance. They are economic and already available on the converter ac side. Their operation time is typically of 40-60 ms on opening and on re-closing [69]. The operation of ACCBs is described by a sequence of steps. Once a fault is detected, a trip order is generated and both trip coils are energised. The high voltage electric arc is extinguished at a natural current zero crossing in a sealed chamber typically containing SF_6 gas. Simultaneously, an order to check the breaking failure protection is executed. If the arc is not extinguished, the breaker does not open and another breaking attempt is performed at the next current zero-crossing point [70].

2.4.4 Fast DC Disconnectors (FDs)

A circuit-isolating mechanism that is not rated to interrupt fault current is an isolator, disconnector or sectionalizer. An FD may be a hybrid or a mechanical switch that offers a physical

separation between active parts. Ultra fast disconnectors with an opening time of less than 2 ms are components present in hybrid DCCB prototypes [64].

2.4.5 DC-DC transformers

DC-DC transformers (also knows as dc-dc converters) are expected to play an important role on splitting large MTDC grids into smaller grids with different voltage levels. Converter topologies include a front-to-front approach; *i.e*, a dc-ac-dc conversion. Hence, the ac side can employ ACCBs in order to block fault currents (although with a time constraint). The dc side can be designed with two-level dual active bridges, with a modular approach employing HB or FB submodules or with a combination of both. These and other topologies are reviewed in [71]. DC/DC transformers with FB submodules have the advantage of featuring fault current blocking capability.

DC/DC transformers for HVDC are currently at an early development stage and their protection role in MTDC grids is still unclear. As a reference, a CIGRE working group has proposed an eleven-terminal dc grid benchmark for transient studies [15] which includes two DC/DC transformers. However, these transformers do not feature FB capability, which suggests that DCCBs may be required at their terminals for protection against dc link faults.

2.5 DC Fault Clearance and Isolation Strategies

DC protection strategies should be designed with respect to the available technologies while considering their costs. Even when DCCBs become available in the market, their expected high cost may be initially prohibitive and, therefore, other schemes incorporating different current breaking devices should be considered [62].

2.5.1 Using ACCBs and FDs

A protection strategy based on ACCBs requires fault detection and fault discrimination algorithms where several approaches are possible. However, in terms of dc fault clearance, the opening of all the ACCBs associated to the faulty dc grid is required. The conjunct opening action leads to the interruption of ac infeed currents to the dc side fault. Then, the dc fault current decays towards zero where eventually dies out. Once the dc current

becomes nearly zero, FDs are able to open and isolate the faulty link. After fault clearance and isolation, a protection strategy needs to reclose ACCBs, resume operation of converters and restore dc grid power flow.

In the open literature, a protection method based on ACCBs has received substantial attention. This approach, referred as the 'Handshaking' method, uses ACCBs already placed on the ac side of the converters and FDs to clear and isolate a dc fault in an MTDC grid [72, 24]. This strategy is applicable to dc networks equipped with HB converters. Communication channels are not needed and all decisions are based on local measurements at the dc and ac terminal sides.

Once a dc fault is detected, either by overcurrent, undervoltage or derivative means, converters are blocked to protect internal power electronic devices. Following this, discrimination is achieved locally by selecting potentially faulty dc lines. Such a selection is based on the dc current direction and magnitude at each dc link connected to a node. Fault clearance is finally achieved by opening all ACCBs, which leads to ac infeed current interruption and dc grid de-energization.

The sequential steps in the 'Handshaking' method are summarized as follows:

(a) Detect the dc fault;
(b) Block IGBTs of the VSCs;
(c) Select the potential faulted dc line;
(d) Open the ACCB;
(e) Wait for the voltage and the current of the selected line to decay to zero;
(f) Open the FD of the selected line;
(g) After a waiting time, re-close ACCB and balance positive and negative P2Gnd voltage;

(i) Re-close the FDr when the voltages on both sides of the disconnector reach their pre-set value;
(j) De-block the IGBTs of all converters.

Once the current decays to zero, the FDs of selected dc lines where the fault potentially occurred have to open. After dc voltage balancing operations if required, ACCBs are re-closed. This restores the dc grid voltage on the healthy part of the MTDC grid, leading to

re-closing FDs placed in non-faulty links. At this point, the fault is discriminated and isolated and all converters are unblocked.

The healthy dc grid is restored approximately 500 ms after the P2Gnd fault starts [24]. This long time is due to the substantial operational times of ACCBs and the current decay rate (which would be larger for P2P faults). It should be known that in this thesis, a protection strategy is designed for dc grids based on fault while fault clearance is ensured by ACCBs (Chapter 5). In this chapter, grid outage times much below 500 ms will be achieved thanks to a protection philosophy different from the 'Handshaking' method .

2.5.2 Using Converters with Fault Current Blocking Capability and FDs

MMCs based on FB submodules are able to block dc faults. In order to clear a dc fault within an MTDC network, all converters should have current blocking capabilities. The blocking action will cause a short temporary outage of the whole network. However, an FB configuration does not require ACCBs or DCCBs for fault clearance. Instead, it requires fault isolation devices at each link end (such as FDs).

Fault detection and discrimination criteria for grids equipped with FB converters can follow a similar approach as in the methods discussed in Section 2.3. For instance, it is expected that the protection strategy includes local fault detection and subsequent current blocking actions in all converters. The fault clearance time should be in the order of a few milliseconds [62]. A discriminative algorithm should then ensure a selective operation of the disconnectors. A protection scheme based on the 'Handshaking' method [24] or on communication-based schemes (such as [29]) would guarantee a correct fault isolation a few tens of milliseconds after the start of the fault. The de-blocking operation of the converters is expected to occur after a successful fault isolation. This last action marks the start of the recovery process of the dc network.

An analysis of a protection strategy with FB converters and different communication needs is discussed in [73]. The fault location and grid restoration are analysed in the cases of no communication, minimum communication or full communication (central unit) in a dc network. The give reference concluded that the use of communication channels leads to a coordinated de-blocking sequence and, therefore, to a reduction of the dc grid outage time.

Further studies are expected to be carried out taking into consideration grid constraints. The main challenges to be addressed include fault discrimination algorithms, fast converter de-block coordination strategies and backup protection.

2.5.3 Using DCCBs - Minimum Tripping

The minimum tripping approach is based on the conventional protection philosophy. In this category of algorithms, the number of protective devices acting is the least possible. Ideally, only the breaking devices on the faulty link open. This rationale is typically applied in ac grids, where tripping signals are generated following fault discrimination. For MTDC grids, the principle is only valid if DCCBs are used.

With a minimum tripping approach, the discrimination must be achieved in a single stage, with no orders to open and re-close unnecessary breakers being required. This requirement can be met by the current difference scheme [38].

The use of advanced discrimination algorithms, which might require the use of communication, brings a processing and transmission delay that typically results in a higher dc fault current level at the interruption instant. As a consequence, the current and energy capabilities of the DCCBs should be higher when minimum tripping methods are in place in comparison to non-minimum methods [74].

2.5.4 Using DCCBs - Non-Minimum Tripping

In this approach, breaking devices on non-faulty links may open. The breaker tripping orders may be generated with fault detection or partial fault discrimination signals. An example of this concept is the 'Open Grid' strategy. This is a non-conventional protection scheme employing DCCBs [31], where logic decisions are based on local measurements. By avoiding communication, fault detection is achievable at a very early stage of the dc fault transients.

The aim of the algorithm is to rapidly trip each DCCB capable of detecting a fault. The DCCB tripping process is carried out without discrimination and is entirely based on local measurements. Thereafter, the discrimination criterion is based on the local residual link voltage. The fault is then permanently discriminated by re-closing healthy circuits. In addition, the method can be modified to achieve a partial discrimination within the dc substation.

The methodology takes advantage of the speed of DCCBs to break the fault current at a lower amplitude, considering that the current breaking capability is limited with today's technology. During the initial transient stage of a fault, dc currents rise towards a steady-state value which may be many times the nominal value. DCCBs have a maximum breaking capability, which may be lower than the steady-state maximum fault current. By eliminating the delay required for the initial fault discrimination, the DCCBs can be opened in a minimum time, reducing their individual current and energy duties. Moreover, the non-discriminative opening of multiple DCCBs allows them to share the breaking duty [74]. Such an approach allows a reduction in the component ratings of the DCCBs and thereby the overall protection cost.

In the 'Open Grid' approach, the current reaches zero faster than in other methods as the breaking operation starts from lower fault current values. Therefore, a discrimination process is required afterwards followed by a re-closing operation; these actions might take more time than what was gained from a faster opening. Hence, the overall fault recovery may take more time if the 'Open Grid' method is adopted.

Fig. 2.12 shows a comparison between the devices that might open within the 'Handshaking', FB converter, 'Open Grid' and current difference strategies. The protection devices that receive an opening order are within the area of the protection scheme. The outage zone for DCCB non-minimum tripping methods illustrates the worst case scenario where all DCCBs detect the fault. However, under most circumstances, the initial outage zone will be limited DCCBs being electrically closest to the fault as these devices will stop the further fault propagation.

2.5.5 Mixed Protection Strategies

A mix of methodologies and breaking devices may also lead to more reliable protection strategies. Fault clearance studies have been performed considering different technologies in [29], where P2Gnd and P2P faults are addressed with a combined breaking operation of ACCBs, converters with FB capabilities and DCCBs. A combination of multiple protection devices within an MTDC grid is proposed in [62]. The strategy is based on an initial division of the MTDC network into smaller areas. In the case of a disturbance, DCCBs placed in dc links connecting two areas first open without discrimination. Afterwards, each area deals

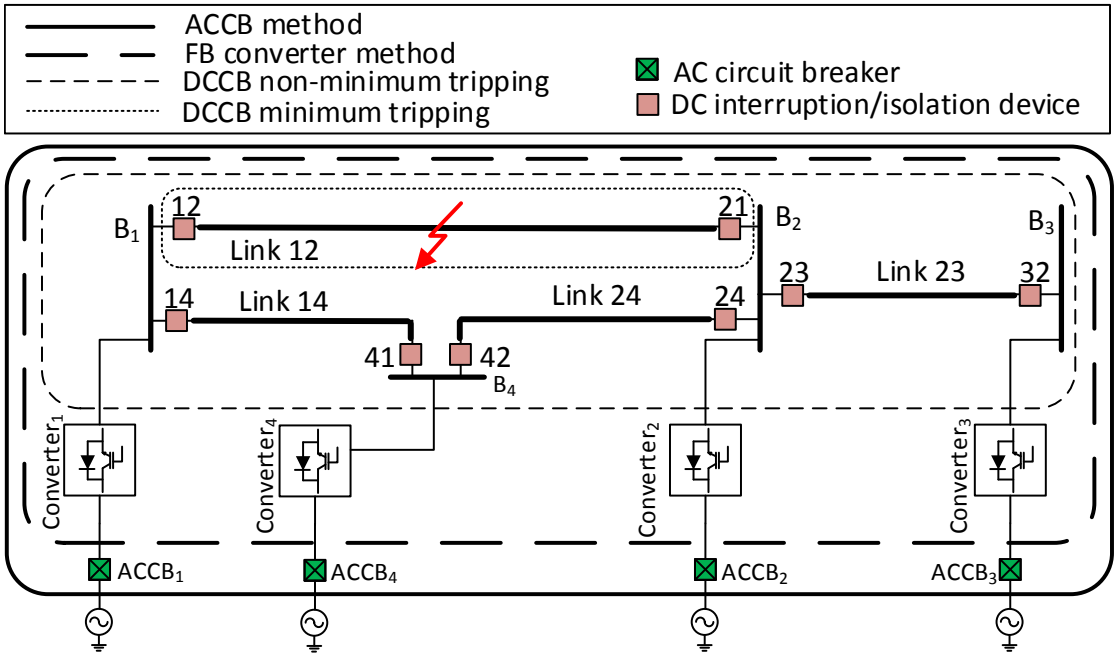

Fig. 2.12 Initial grid outage zones for protection strategies using different dc current breaking devices (hypothetical view).

with its own internal disturbances, enabling a normal operation in healthy areas. This way, protection strategies are applied within the faulty area employing the available breaking devices (*e.g.* ACCBs).

Fig. 2.13 shows a scenario where the different fault current clearance devices co-exist within the same MTDC network. This mixed protection scheme has the practical advantage of employing a limited number of DCCBs. In addition, it might be suitable to temporarily divide large MTDC networks into small areas so that disturbances affect only the faulty area while the security of supply is not affected by the other areas [5].

2.6 Discussion and Research Trends

DC protection is the key area that will facilitate the deployment of a large-scale dc grid. However, a number of challenges have been identified and should be addressed in the near future. New protection strategies must be developed to comply with dc grid feasibility studies [14]. These strategies should be fast and discriminative. They must guarantee that

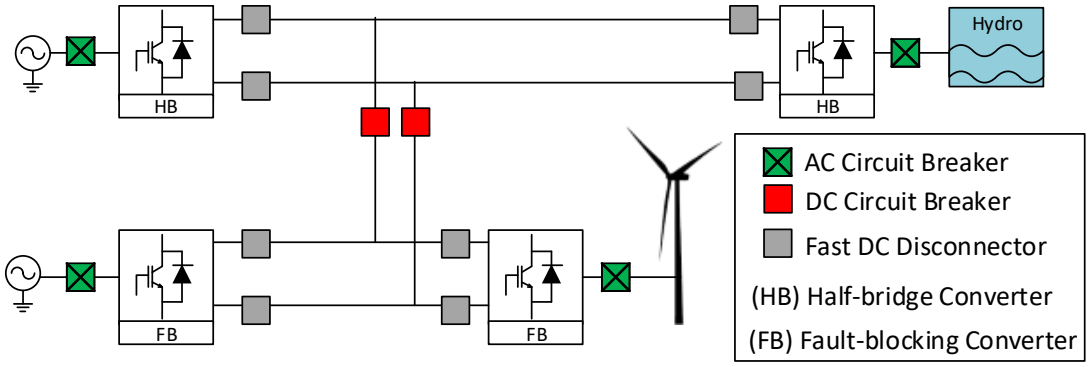

Fig. 2.13 Hypothetical view of a MTDC grid equipped with different fault clearance devices.

the capabilities of the breaking devices are not exceeded and that ac and dc networks do not experience undesired stability issues.

Research activities on current breaking devices remain important for the industry. A number of manufacturers are making substantial efforts to develop their own fast DCCBs while, at the same time, grid operators from different countries and international authorities aim for harvesting more renewable energy in remote areas. Such a discrepancy between the desired technology and the potential market requirements will ensure a sustained growth of research in MTDC grids [9].

Ideally, a protection strategy for dc links protected by DCCBs should be designed to strike a balance between the allowed maximum number of operated breaking devices and the breaking devices current interruption capabilities. Should DCCBs in healthy links open, the re-closing criteria need to be optimised to guarantee a minimum outage time. Having a dc grid out of service for less than 50 ms may be acceptable for the stable operation of ac grids nearby [31]. However, an ac system might not accept a dc grid to be out of operation for 300 ms [62]. A dc grid outage period must not cause the tripping of ac protection and such a duration is not well established currently [5].

Research activities on protection strategies shall consider dc faults on OHLs, which is not a common practice. DC OHLs include a new set of phenomena and operational conditions that are currently not investigated in dc cable networks. These include the possibility of transient faults, conductor galloping, magnetic couple between OHLs sharing the same tower and dc network overlap with ac networks which may lead to possible ac-to-dc faults. In addition, OHL-based dc networks have a small capacitance and a faster propagation delay

due to the lower capacitance-to-inductance ratio. Hence, this research gap is expected to be addressed in future publications.

Reliability is potentially the last major obstacle preventing the large integration of MTDC grids into existing networks [20]. This shall be addressed through the development of dc protection strategies and fault interruption devices able to minimise the disturbance caused by a dc fault. This should be done in such a way that the stability of the ac grid and security of supply is ensured. These issues are being analysed in ongoing pilot projects such as the Nan'ao and Zhoushan MTDC grids in China, where DCCBs are expected to be added in the medium/long term run [75].

2.7 Summary

A reliable operation of MTDC grids will be strongly dependent on dc protection technologies. To this end, this Chapter has reviewed existing protection strategies for dc grids. In general, these have been designed to maximise the capabilities of grid protection devices such as ACCBs, DCCBs, FDs and converters with FB capability.

Link discrimination without the need of communication channels has been identified as a major technical challenge. Protective strategies must be both fast and discriminative. The protection of dc networks is expected to occur using either minimum or non-minimum tripping approaches. The minimum tripping approach relies on fault discrimination and requires tripping orders to the devices around the faulty point only. This approach requires large current rate limiting devices to reduce the fault current magnitude by the time of the fault clearance. The non-minimum tripping approach requires opening more devices than the minimum necessary ones, interrupting the fault at the beginning of its inception, and then re-closing protection devices placed on non-faulty links. Both approaches have advantages and their adoption relies on the accepted period of grid outage and current breaking capabilities of available devices. Notwithstanding, additional protection strategies must be proposed and validated in order to move towards a safe power transmission in MTDC grids.

It is expected that point-to-point dc links evolve to MTDC grid topologies in the near future. For this to happen, different protection devices and philosophies within a larger grid should be incorporated. A coordination between the capabilities of protection devices and algorithms will be fundamental to ensure efficient solutions.

Chapter 3

MTDC Grid Modelling

3.1 Introduction

DC links and converters have a considerable influence on dc fault transients. In order to ensure a accurate representation of dc current and voltage transients for investigating dc protection, special attention is given to modelling. Two MTDC networks are designed for protection studies including a 4-terminal meshed dc network and CIGRE 11-terminal dc network [15].

The used modelling software is PSCAD/EMTDC v4.6 which is a renown tool for electromagnetic simulations recognised by both academia and industry. Computation sampling rate in PSCAD/EMTDC is chosen as 0.2 ms while the visualisation rate is of 0.4 ms. It should be noticed that this short sampling rate is not a restriction on practical applications as protection relays are currently able to operate even with lower sampling rates. For instance, devices with a 1 μs record sampling rate and with a processing sample rate or 0.1 ms are commercially available [76].

Per unit (p.u.) system is used in most of the results in this thesis. The current and voltage base values are given in Table 3.1:

Table 3.1 Per unit system base values.

Voltage base (P2P voltage):	400 kV on monopole network 800 kV on bipole network
Current base:	2 kA

3.2 4-terminal DC Test System

A 4-terminal dc grid is built to represent a generic dc grid for testing of protection strategies where dc fault clearance is achieved either using ACCBs, FB converters or DCCBs. The objective is to have sufficient accuracy while having a small/medium computational simulation time.

3.2.1 DC Network Configuration

The designed 4-terminal dc grid is based on [5] while a link is added in order to have a meshed configuration. The outcome is given in Fig. 3.1.

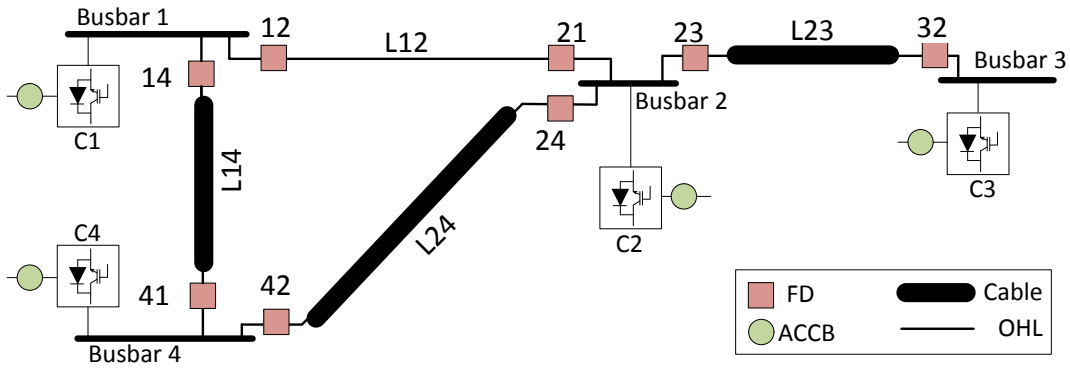

Fig. 3.1 Configuration of a 4-terminal dc network.

The dc grid comprises three cables and one OHL. The chosen lengths of links L12, L23, L14 and L24 are, 200 km, 100 km, 100 km and 150 km, respectively. Each link end is equipped with an FD. Converters are based on MMC VSC technology with HB or FB submodules.

3.2.2 DC Network Operation

The 4-terminal dc grid has a symmetrical monopole topology with a $\pm$ 200 kV P2P voltage. The dc grid control principle is based on a master-slave scheme where converter C2 operates in a dc voltage control mode while converters C1, C3 and C4 employ an active power control mode. A more detailed description of the control schemes is referred in [58]. The control modes and setpoints are given in Table 3.2.

Table 3.2 Converters' operational modes and settings.

Converter	Control mode	Control setpoints
C1	P, Q	-400 MW, 0 Mvar
C2	V_{dc}, Q	400 kV, 0 Mvar
C3	P, Q	-200 MW, 0 Mvar
C4	P, Q	500 MW, 0 Mvar

DC voltages and currents at the pre-fault stage are given in Table 3.3. These values are for one pole. The values are in the p.u system as given in Table 3.1.

Table 3.3 Steady-state dc voltages and dc currents at the 4-terminal dc grid [p.u.].

Converter	DC Voltage	DC Current
C1	0.481	-0.59
C2	0.486	0.515
C3	0.483	-0.395
C4	0.483	0.505

Link	DC Current
L12	-0.269
L23	0.407
L24	-0.175
L14	0.164

3.3 CIGRE 11-terminal B4 DC Test System

The increasing interest in HVDC technologies has lead to a proliferation of dc network models for control and protection studies. As a disadvantage, results from a wide number of network models are harder to be compared on an equal basis. In addition, control and protection algorithms should ideally not be restricted only to a specific topology but rather applicable to large and realistic topologies. Efforts to analyse more suitable topologies for HVDC grid studies and to develop a potential standard dc topology have been put in place by several organisations and universities [23, 77, 78, 15]. The model proposed by CIGRE working group B4 [15] is tested in this thesis. This consists of a complex 11-terminal dc network composed of three sub-systems. These are referred as:

- Sub-system 1: point-to-point link with $\pm$ 200 kV;

- Sub-system 2: monopole radial network with ± 200 kV;
- Sub-system 3: bipole meshed network with ± 400 kV.

Sub-system 1 is connected to sub-system 2 through ac connections. Sub-system 2 is connected to the sub-system 3 through a dc-dc transformer. The sub-systems 1 and 2 also have connections to sub-system 3 through ac links. The sub-system 1, which has no dc connection to the major HVDC network composed of sub-systems 2 and 3, is not considered in the simulations. This assumption is in agreement with [15] which suggests that research studies may be carried out using the whole CIGRE dc grid or only sub-systems of it.

3.3.1 DC Network Configuration

The configuration of CIGRE 11-terminal dc network is shown in Fig. 3.2. This network includes 11 converter terminals, 1 switching terminal (busbar 12), 11 ac relays, 14 dc links and 28 dc relays and 2 dc-dc transformers.

The dc grid is composed of cables, OHLs, two parallel OHLs sharing the same tower and a mixed link composed of a cable and of an OHL. The links lengths and types are given in Table 3.4.

Table 3.4 DC link numeration, length and type.

Link	Length [km]	Type
L12	200	Cable
L112	500	Cable
L14/15	400	Parallel OHLs
L23	300	Cable
L39	200	Cable
L49	200	Cable
L412	200	OHL
L512/L513	300	Parallel OHLs
L67	200	Cable
L78	100 + 100	Cable + OHL
L89	200	Cable

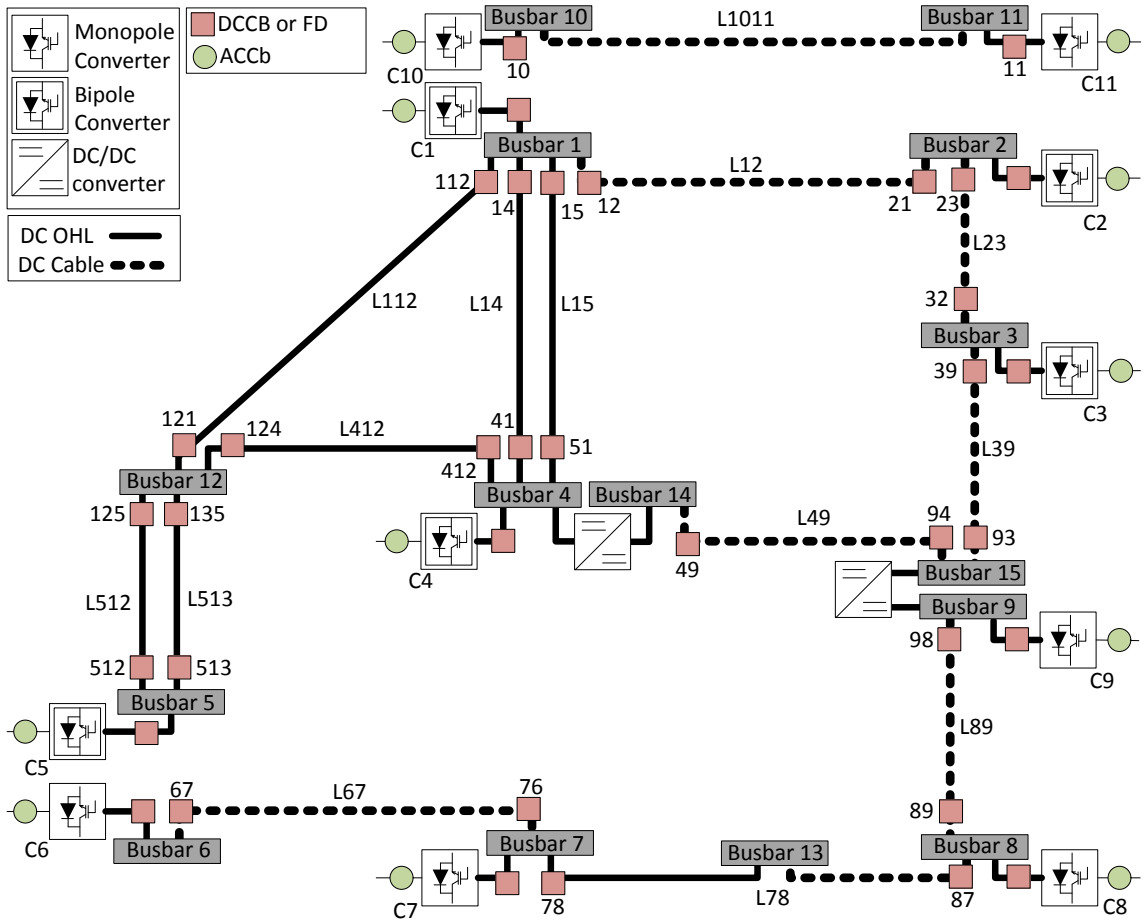

Fig. 3.2 Configuration of CIGRE 11-terminal dc network.

The CIGRE 11-terminal dc grid model in PSCAD/EMTDC was developed by HVDC Manitoba Research Centre Inc and is publicly available (upon request). The version tested during this thesis was released in July 2014.

3.3.2 DC Network Operation

The control modes and setpoints of the converters in sub-systems 2 and 3 are given in Table 3.5.

DC voltages and currents at the pre-fault stage are given in Table 3.6. These values relate to the positive pole which is symmetrical to the negative pole. The values are given in p.u. system.

Table 3.5 Control modes and setpoints of converters.

Converter	Control mode	Operational setpoints
C1 (Bipole)	V_{dc}; V_{ac}	2×404 kV; 1 p.u.
C2 (Bipole)	P; Q	2×300 MW ; 0 Mvar
C3 (Bipole)	P; Q	2×500 MW; 0 Mvar
C4 (Bipole)	PV_{dc} droop; V_{ac}	2×(-750) MW, 400 kV (P/V droop =5); 1 p.u.
C5 (Bipole)	P; V_{ac}	2×(-850) MW; 1 p.u.
C6 (Monopole)	V_{dc}; Q	400 kV; 0 Mvar
C7 (Monopole)	PV_{dc} droop; V_{ac}	-800 MW, 400 kV (P/V droop =5); 1 p.u.
C8 (Monopole)	P; Q	500 MW; 0 Mvar
C9 (Monopole)	V_{dc}; f	400 kV; 50 Hz

Table 3.6 Steady-state dc voltages and dc currents at CIGRE 11-terminal dc grid [p.u.].

Converter	DC Voltage	DC Current
C1	0.489	1.04
C2	0.494	0.36
C3	0.496	0.60
C4	0.484	-0.68
C5	0.475	-1.09
C6	0.494	0.40
C7	0.488	-0.73
C8	0.498	0.60
C9	0.493	-0.13

Link	DC Current
L12	-0.40
L112	0.57
L14, L15	0.43
L23	-0.05
L39	0.57
L49	-0.38
L412	0.55
L512, L513	-0.55
L67	0.40
L78	-0.33
L89	0.27

3.4 Equipment Modelling

3.4.1 Converters

Converter models have been categorised into 7 types from full physics based models to load-flow models [58]. Detailed models have better accuracy in relation to simplified models, although at the expense of increasing simulation time. A comparison between accuracy and computation time for several converter models can be found in [79].

The detailed equivalent model (DEM) is recommended for dc protection studies [58]. This is classified as a type 4 model which is suitable for transient studies where the internal access to submodules is not required. On the converter DEM, the internal IGBTs and diodes are represented by a two-state resistive device. The submodule capacitor is represented by a resistor in series with an equivalent voltage source. Hence, the DEM includes accurate impacts of different capacitors voltages at each module level. Performance results of this model in comparison to more advanced models can be found in [59].

Three types of converters are used in this thesis including HB MMC, FB MMC and dc-dc transformers. The HB and FB MMCs are modelled as type 4 (DEM). The steady-state operation is similar to both the HB and FB converters [52]. In terms of protection, HB based MMC does not block fault currents while FB based MMC interrupts ac infeed currents which leads to dc fault current clearance. DC-DC transformers are modelled as ideal transformers with passive elements that represent power losses. In terms of dc protection, dc-dc transformers do not have fault blocking capability.

3.4.2 DC Links

Generally, there are two approaches to model dc links [80]. The first approach is based on π sections where a system can be characterised by a localised circuit of passive elements. In order to distribute the elements over a number of link sections, multiple π sections could be used. The second approach is based on frequency-dependent parameter models. More importantly, this approach is based on travelling waves theory and the passive elements are frequency-dependent. For example, a voltage disturbance at a certain point of a link will

propagate in both directions and arrive at link' terminals after a propagation delay. This behaviour is not present on links based on π sections [80].

There are two frequency-dependent models available in PSCAD/EMTDC. These are the frequency-dependent mode and frequency-dependent phase models. The first model accurately represents electromagnetic transients in the case of balanced systems such as with ideal transposition of conductors. The second model (the frequency-dependent phase model) is able to represent transients for imbalanced systems. This model is based on universal line model theory [81] and is considered the most accurate modelling approach in the PSCAD/EMTDC environment [80]. Therefore, the frequency-dependent phase model is considered for modelling dc links.

Two types of dc links are considered in the dc network including cables and OHLs. These are designed for the $\pm$ 200 kV and$\pm$ 400 kV voltage levels. The parameters of the underground cable are given in Table 3.7.

Table 3.7 Cable parameters.

Layer	Material	r[mm]	ρ [Ω/m]	ε_r[-]	μ_r[-]
Core	Copper	25.2	1.72e10-8	1	1
Insulation	XPLE	45.2	-	2.3	1
Sheath	Lead	48	2.2e10-7	1	1
Insulation	XPLE	53	-	2.3	1

where r represents the outer radius, ρ is the resistivity, ε_r is the relative permittivity and μ_r is the relative permeability.

Fig. 3.3 illustrates the layout of cables and OHLs towers. The parallel OHL corridors are based on the $\pm$ 400 kV towers (Fig. 3.3 (d)) with a distance of 50 m between towers.

3.4.3 Link end Current Rate Limiter device

A current rate limiter device has the capability to limit the rate of change of a dc current. In the literatures, these devices might be referred as link inductor, limiting dc reactor, current rate of change limiting device or superconducting current limiter [35, 84–86]. In practice,

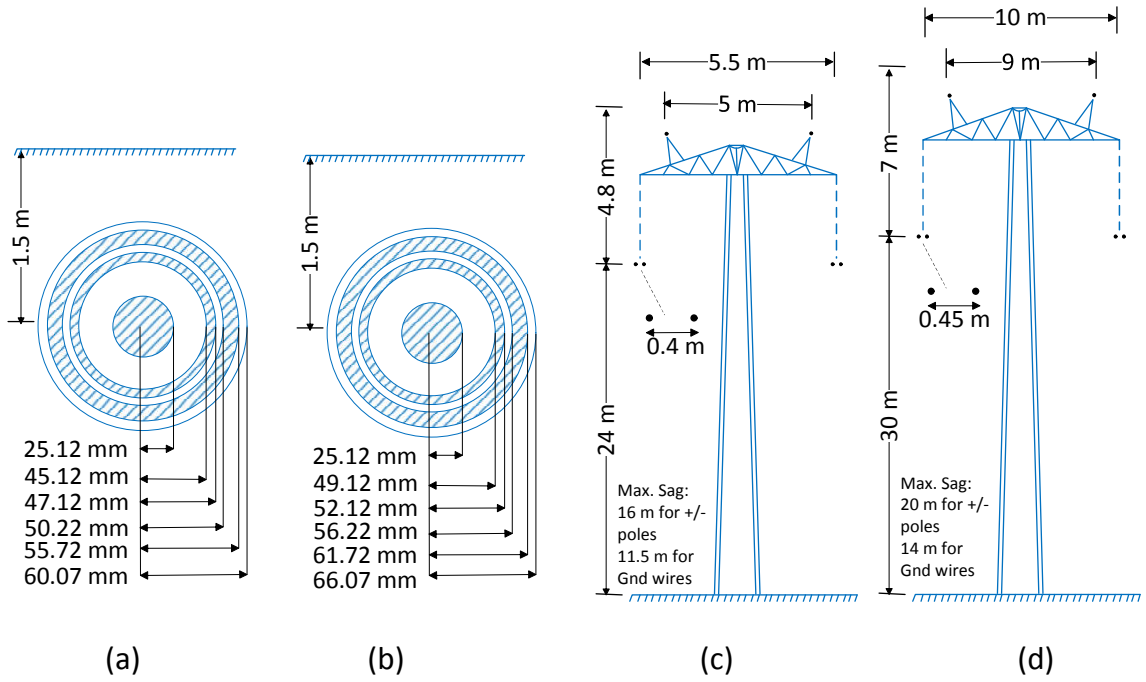

Fig. 3.3 Dimensions of dc cable for voltages of (a) ± 200 kV and (b) ± 400 kV. OHL tower dimensions for voltages of (c) ± 200 kV and (d) ± 400 kV (adapted from [82, 83, 15]).

this device shall be an inductor placed at each end of a dc link and has the function to limit the rate of rising of fault dc current.

The rating of link end inductors is often linked in the literatures with the performance of DCCBs. This approach is based on the reduction of the rate of change of current which in turn allows a protection strategy to have an additional time for fault discrimination and fault clearance. This additional time is typically associated with operation delays of DCCBs. Moreover, the inductor size choice can be driven by current or voltage derivative functions that are associated to fault discrimination. As a consequence, the design of dc link end inductors is not an established process. Therefore, several ratings are found in the open literatures for wide operation conditions (see Table 3.8).

Introducing link end inductors has a number of disadvantages. These will increase the overall losses in the system, increase the fault current interruption time and increase the magnetic energy that needs to be cleared by the DCCBs [88]. A compromise needs to be found when installing these inductors: the lower current rate increase and the additional time that can be gained must be weighed against the size and cost (investment and losses) of

Table 3.8 Link end inductor ratings in the literatures.

Reference	[66]	[63]	[32]	[87]	[18]
Grid voltage	$\pm$ 320 kV	$\pm$ 320 kV	$\pm$ 320 kV	$\pm$ 320 kV	$\pm$ 120kV
DCCB operation	8-10 ms	2 ms	2 ms	2 ms	$\approx$ 5 ms
Inductor rating	300 mH	100 mH	20-40 mH	50 mH	40 mH

the inductors. Adding large inductors will also negatively influence dynamics and transient control responses in dc grids [20].

The rating of link end inductors is chosen with basis on simulations results. In the case of a DCCB based protection strategy, a 50 mH link end inductor is used. This value leads to dc fault current below the DCCB capability at the current breaking instant. In the case of a protection strategy based on FB converters, a 10 mH link end inductor is used which is considered a residual value in HVDC grids. This value leads to a dc fault current below 2 p.u. at the blocking instant of FB converters which has a minimum processing delay of 0.1 ms. In the case of an ACCB based strategy, the fault clearance occurs with several tens of milliseconds (assumed as $\approx$ 50 ms in this thesis). Hence, in order to limit the current magnitude for such a long period, very large inductors would be required. In this case, fault current should be limited through other means as a higher ac side impedance [20]. For simplification, 10 mH inductors are also used in the case of an ACCB based strategy.

Lastly, in this thesis, link end inductors are modelled as a single lumped element. This model offers a ideal behaviour at low frequencies but might be not accurate at higher frequencies [89]. Notwithstanding, the link end inductor rating and model is not optimised in this thesis and should be bespoke for each project.

3.4.4 Fast DC Disconnectors (FDs)

FDs are fault isolation devices without or with limited residual current breaking capability. These are used to isolate dc faulty links in grids where fault clearance is achieved by operation of ACCBs of FB converters. FDs are placed at each link end.

FDs can be designed according to two approaches. Firstly, a mechanical switch (as an ACCB) can be considered. This switch is able to open within a few tens of milliseconds once

the dc current decays to zero. Secondly, a mechanical/hybrid disconnector based on the main conduction branch of DCCB prototypes can be used. In these cases, the operational times might be reduced to 2 ms [61]. In terms of current interruption, a residual breaking capability of a few tens of amperes is expected.

In this thesis, the operation time of an FD is assumed as 10 ms while the residual breaking capability is assumed 30 A. An FD effectively opens when a dc current remains below 30 A for a continuous period of 10 ms. These values are considered practically feasible and conservative.

3.4.5 DC Circuit Breakers(DCCBs)

The DCCB model considered in this thesis is the hybrid breaker [61, 63, 65]. This model is based on the standard single phase breaker available in the PSCAD/EMTDC library. A surge arrester is added in parallel with the breaker in order to represent the energy absorption branch introduced by the hybrid DCCB.

The DCCB interruption time is assumed as 5 ms. This is a practical and conservative approach. With the opening of a DCCB, the dc current magnitude starts to decay while the inductive energy is stored in the surge arrester bank. In the simulated models, the dc current magnitude decays to zero in typically 1-2 ms after the DCCB opening procedure starts. In terms of current breaking capability, a 16 kA value is assumed which will be achievable in upcoming devices [63].

3.4.6 AC Circuit Breakers (ACCBs)

The ACCB is based on the standard three phase breaker in the PSCAD/EMTDC library. The ACCB model has a 40 ms operation delay in order to represent a realistic operation. Then, the fault current is expected to be interrupted at the next zero-crossing intersection. As a result, an ACCB opens typically 50 ms after fault detection. In addition, ACCBs include pre-inserted soft-start resistors which reduce the magnitude of the inrush currents. These resistors are not necessary for the correct operation of the protection strategies but shall be present for high-voltage applications.

Adjacent to ACCBs, grounding points are provided. These are placed between the ACCB and the converter station. A grounding point is composed of a star inductance with a high impedance earthing arrangement [29]. These are required for simulation initiation, as a reference to the converters allows the dc voltage to raise symmetrically at both poles.

3.4.7 DC Relays and Busbar Units

Logic signal processing units are considered as dc relays and busbar units. DC relays are placed at each link end and are associated with current and voltage sensors together with an FD or DCCB. Busbar units are associated with each busbar and are the units that execute the protection strategies. For completeness, current and voltage sensors with a bandwidth of 6 kHz are commercially available [90, 91].

A delay of 2 ms is assumed for signal processing purposes such as data acquisition, coding and decoding analogue-digital signals, data filtering and data transmission. This delay is associated with data transfer delay between a busbar station and nearby dc relays which are geographically close. In the literatures, the processing delay is typically an ambiguous quantity. However, a 2 ms assumed delay leads to a more realistic model and is acknowledged by the industrial partner.

A summary of the MTDC system parameters is given at Table 3.9.

3.5 Summary

The modelling of dc grids is performed prior to the study of protection algorithms and protection strategies. Special attention has been paid to use models that represent with great accuracy the currents and voltage transients generated due to dc faults.

HVDC converters are modelled as detailed equivalent models as recommended by CIGRE [58]. HVDC cables and OHLs are represented using frequency-dependent phase models. These dc link models represent transient for imbalanced systems such as faults in dc systems. As a result, the models represent with good precision the transients originate by dc faults. The ACCB and DCCB models are also based on realistic approaches where a 40 ms and 5 ms operation delays are considered, respectively.

Table 3.9 DC network parameters.

Converter model	DEM, Type 4	[-]
Submodules per arm	200	[-]
Converter arm inductor	100	[mH]
DC grid voltages	$\pm$200; $\pm$400	[kV]
Link model	Frequency dependent phase	[-]
Link end current rate limiter	10; 50	[mH]
ACCB operation time	$>$40	[ms]
FD operation time	10	[ms]
DCCB operation time	5	[ms]
Per Unit base voltage (monopole dc grid)	400	[kV]
Per Unit base voltage (bipole dc grid)	800	[kV]
Per Unit base current	2	[kA]

Two MTDC grids are modelled, *i.e.* a 4-terminal and the CIGRE 11-terminal dc grid. With these, dc faults can be simulated for various studies which include faults at cables, at OHLs, at a bipole grid, at a monopole grid, immediately after a busbar or at the middle of a link, among other fault scenarios.

Chapter 4

Fault Detection and Fault Discrimination Algorithms

4.1 Introduction

To ensure a highly reliable and affordable transmission system is a necessity for grid operators.The negative effects of a dc fault in a dc grid must be minimised by an appropriate protection strategy. Such a strategy must ensure personal safety, equipment safety and minimal service disruption in the event of a fault. To comply with these requirements, a fault needs to be detected, discriminated and isolated timely and accurately. In addition, a protection strategy should consider fault clearance based on the technical and economic limitations of these devices. For instance, several options with distinctive costs and technical capabilities are under consideration to clear dc fault currents. These include ACCBs, converters with fault blocking capability and DCCBs. Hence, the design of a protection strategy represents a trade-off between minimising the negative effects of a disturbance in a system and having a low investment and operational cost.

Each element on an HVDC system requires a protection strategy. Unit protection is used for equipment such as transformers, converters or filters, devices that are geographically at the same location. Moreover, dc links can span over an immense geographical area. This reduces the chances to implement link communication channels due to unacceptable communication delays. Therefore, non-unit link protection is typically preferred over unit

protection for dc links protection. Non-unit protection leads to faster fault detection and discrimination decision-making. Thereupon, fault clearance time and potential high fault current magnitude are correspondingly reduced.

This chapter gives the fault detection and fault discrimination algorithms developed for dc protection. These are described in detail and supported by simulation results, as necessary. Such results are related to a fault case at a simple 3-terminal dc grid (see Fig. 4.1). In this case, a P2P dc fault occurs at the middle of link 12, *i.e.* 100 km from dc relays 12 and 21, and has 5 Ω impedance. The dc links are modelled as frequency-dependent cables and the MMCs are based on HB submodules (described in detail in Section 3.4).

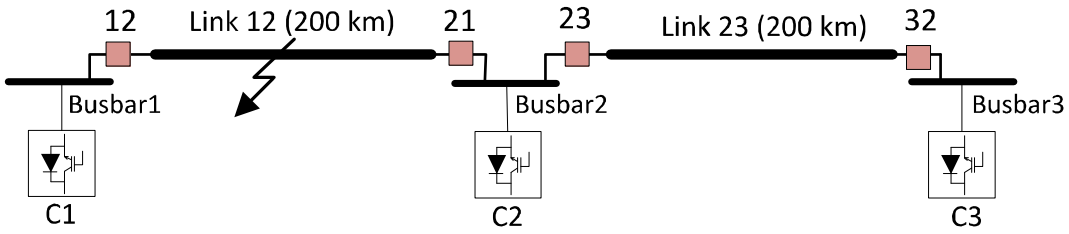

Fig. 4.1 Three terminal dc grid with a low impedance fault at link 12.

4.2 Fault Detection Algorithms

The detection of a dc fault comprises the first step of a protection strategy. The event of fault detection leads to the start of fault discrimination and fault clearance operations. Hence, it is crucial to have an algorithm that detects a fault disturbance in a timely and correctly manner [16]. A quick fault detection algorithm may brings several advantages, including:

(a) low current magnitude at the fault clearance instant;

(b) low rating of current breaking devices;

(c) low rating of fault current rate limiters;

(d) potential low energy absorbed by hybrid DCCBs or FB converters;

(e) quick start of the fault discrimination algorithm and more data for online analysis.

4.2.1 Overcurrent Detection

The most widely used algorithms in power systems are based on a comparison of a signal (such as current or voltage) with a threshold [70]. The overcurrent detection criterion is based on monitoring dc current magnitude and observe a transgression of a pre-defined threshold (Eq. 4.1).

$$I_{DC}(t) > I_{DCthr} \tag{4.1}$$

Threshold I_{DCthr} should be as small as possible in order to have a quicker fault detection. However, it must also be sensitive to operational events such as noise, setpoint changes or potential temporary link overload. Environment temperature can also alter the overcurrent threshold in a number of systems [92, 21]. In this thesis, threshold I_{DCthr} is set as 1.2 p.u. This value is based on an operational deviation of 0.1 p.u. which is an acceptable deviation for a temporary overload [92]. Additionally, a safety margin of 0.1 p.u. is included to consider potential noise and precision errors from sensors. This way, the overcurrent threshold becomes 1.2 p.u.

4.2.2 Undervoltage Detection

The undervoltage criterion consists of comparing dc voltage magnitude against a threshold. If the dc voltage decays below a threshold V_{DCthr}, then a fault is detected within the network. The algorithm follows as:

$$V_{DC}(t) < V_{DCthr} \tag{4.2}$$

Threshold V_{DCthr} is set as 0.85 of the nominal values. Such magnitude takes into account potential operational voltages which in Great Britain can range between 0.9-1.05 p.u. (Annex V of [93]). Additionally, a safety margin of 0.05 p.u. is included to consider potential noise and precision errors from sensors.

4.2.3 Current Derivative

A current derivative algorithm is considered in this thesis. Foremost, overcurrent and undervoltage methods are able to achieve fault detection in a relatively short time, typically below 1 ms after the arrival of transient waves. Subsequently, the fault discrimination algorithms are initiated. However, if the fault detection is not achieved with the first transient wave (incident wave), such a wave is disregarded from analysis by fault discrimination algorithms. In this case, the incident wave is considered as a normal operation transient instead of a disturbance transient. Therefore, the fault discrimination algorithm might perform incorrectly. This issue is avoided by considering a current derivative algorithm, as it typically leads to a faster disturbance detection in comparison to overcurrent or undervotlage algorithms.

In this thesis, a current derivative algorithm is designed to detect dc current disturbances in a very quick manner. This speed requirement comes from the need to initiate the fault discrimination algorithms as soon as a fault transient wave arrive to a dc relay. Hence, a considerable small threshold $dIdt_{thr}$ is chosen in order to have a fast disturbance detection. The algorithm becomes:

$$\frac{dI_{DC}}{dt}(t) > dIdt_{thr} \tag{4.3}$$

Threshold $dIdt_{thr}$ is based on the maximum current derivative in steady-state operation. Each protection relay sets its threshold which is dependent on the accuracy of the current sensor, potential noise and dc current quality. It should be noticed that the sensitivity is not the main requirement of the current derivative algorithm (the main requirement is speed). The current derivative algorithm is designed to detect a disturbance in the grid while dc fault detection is ensured by overcurrent or undervoltage algorithms. Hence, if there is no overcurrent or undervotlage, protective actions (such as opening a DCCB) are not taken.

Fig. 4.2 shows the module of a current derivative of a dc current acquired during steady-state operation (relay 21 of Fig. 4.1). Despite being considered a constant dc current, rates of change are visible in a small scale due to high frequency oscillation. For example, the maximum current derivative magnitude is approximately 0.014 p.u./ms in Fig. 4.2. Hence, $dIdt_{thr}$ would have the value of 0.014 (in this relay) times a safety factor set as 2. As a result,

if the current derivative transgresses the value of 0.028 p.u./ms (from 0.014×2), a fault might be present and the fault discrimination algorithms would be initiated. This is a practical approach to detect quickly a current disturbance with a small threshold.

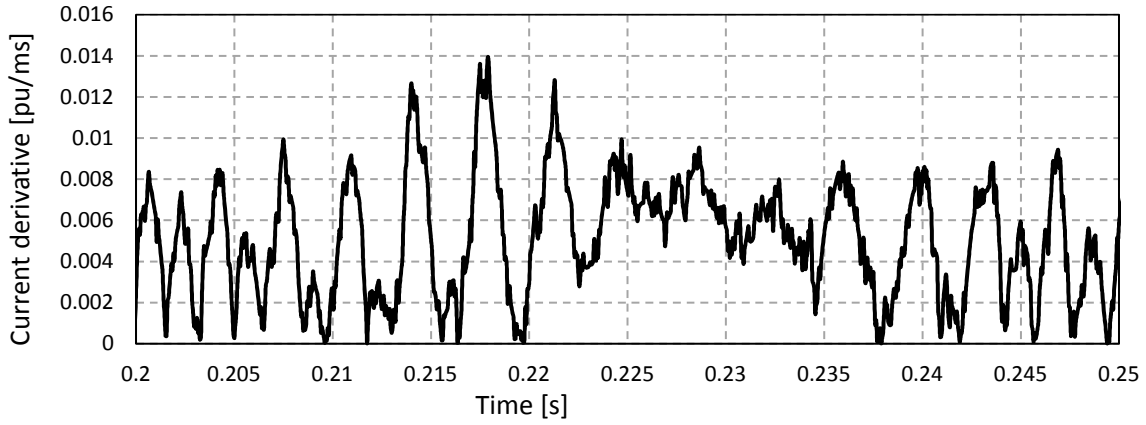

Fig. 4.2 DC current derivative acquired during steady-state operation.

The current derivative algorithm leads to detection of a disturbance just in a few time samples after the arrival of the incident wave, even for dc relays at remote places in relation to the dc fault location. As a result, the fault discrimination algorithms start at an early stage and are able to analyse online the incident and reflected transient waves. The speed of the current derivative algorithm is crucial for a correct start of the decision-making at the fault discrimination algorithms.

4.3 Fault Discrimination Algorithms

The main purpose of discrimination (or selectivity) is to identify the faulty link within a network. This process is achieved by analysing dc current or dc voltage measurements. These data can be based on local measurements (non-unit protection) or remote measurements (unit protection). In the literatures, various algorithms have been proposed for discrimination of dc networks [30]. Among these, communication-based methods (unit protection) achieve good results in terms of selectivity [38] but at the expense of incurring communication delays, potential channel failure and a high system cost. Methods based on local data (non-unit protection) have the advantage of a quick decision-making. Recent work has addressed algorithms based on current or voltage derivatives [32, 35, 37]. The derivative approach is

very sensitive to fault impedance, link type and rating of link end inductors. The derivative methods can achieve a high level of discrimination if accurate thresholds are used. However, the given references consider only DCCBs for dc fault clearance, MTDC configurations composed mostly of cables and link end inductors with considerable large ratings (as 100 mH [37]). For this reason, alternative algorithms shall be investigated to discriminate faults in a different number of scenarios, including grids composed of cables and/or OHLs and dc links without large link end inductors.

In this section, fault discrimination criteria use local dc current and voltage measurements. Three discrimination criteria are given. Two of these (Sections 4.3.1 and 4.3.2) perform decision-making for the opening of FDs or DCCBs. The third criterion (Section 4.3.3) only performs decision-making for the re-closing of FDs or DCCBs which is a necessary action if a device is open on a non-faulty dc link.

4.3.1 Comparison of Rate of Change of Current (CRCC)

The objective of this developed algorithm is to quickly discriminate the faulty dc cable or OHL by analysing the local dc current behaviour. DC current transient waves are generated with a dc fault and propagated along a dc network. Transient waves including the incident wave and reflected waves. The magnitudes of these waves are captured and compared against each other in this discrimination algorithm.

Start of a DC Fault

A voltage drop can be observed when a dc fault occurs on a link. In the worst case scenario, the pre-fault voltage U_0 decays to a lower level. The fault severity is linked to the fault impedance, *i.e.* faults with a low impedance lead to high changes of voltage and current. The voltage change (U_0') is divided over the fault impedance R_f and link impedance Z_c [32]. The voltage at fault location V_f becomes:

$$V_f = \frac{Z_c/2}{R_f + Z_c/2} U_0' \tag{4.4}$$

while the link characteristic impedance Z_c is:

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{4.5}$$

where R, L, G and C are the resistance, inductance, conductance and capacitance per unit Δx of a link, respectively. The voltage and current transients propagate through a network in the form of travelling waves. These waves arrive at the link terminals after a delay where current and voltage sensors are placed.

Propagation of Transient Waves

Transient waves propagate from the disturbance location to the network's terminals. The behaviour of voltage or current at a link with a length Δx are described by the link distributed parameters equations:

$$v(x) - v(x + \Delta x) = (R + jL\omega) i \Delta x \tag{4.6}$$

$$i(x) - i(x + \Delta x) = (G + jC\omega) v \Delta x \tag{4.7}$$

where v and i are the voltage and current measurements and $\omega = 2\pi f$. The derivation of the above equations in order of length x leads to the Telegrapher's equations:

$$\frac{d^2 v}{dx^2} = (R + jL\omega)(G + jC\omega) v \tag{4.8}$$

$$\frac{d^2 i}{dx^2} = (R + jL\omega)(G + jC\omega) i \tag{4.9}$$

The transient waves arrive at the link terminals with a propagation delay γ times the link length l. The voltage and current waves that travel along a link are based on the above equations with a time shift [94]. The propagation velocity *vel* is defined by:

$$vel = \frac{1}{\sqrt{LC}} \tag{4.10}$$

As power links are not lossless, the magnitude of the travelling waves decays while the waves propagate along a link. Several discontinuities in a network distribute the energy and modify the direction of travelling waves. Discontinuities include inductive link termination, fault location or link joints. At a discontinuity, the travelling wave energy propagates to other

links with a transmission coefficient T (Eq. 4.11) while a part of it is reflected backwards with a reflection coefficient Γ. At the fault location, Γ is given by:

$$T = 1 + \Gamma \tag{4.11}$$

$$\Gamma = \frac{1}{1 + 2\frac{R_f}{Zc}} \tag{4.12}$$

Fig. 4.3 illustrates the relation of T and Γ at a link discontinuity due to a fault with resistance R_f.

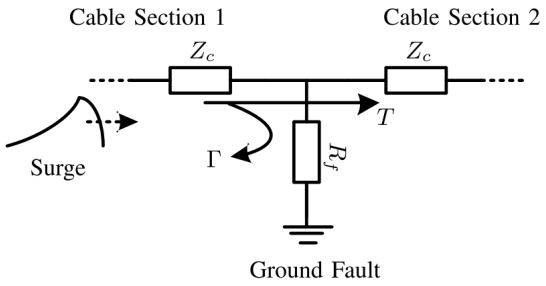

Fig. 4.3 Reflection and transmission of waves at fault location [26].

The first wave that arrives at a terminal is known as the incident wave. The following waves are known as the reflected waves. Both of these travelling waves are transmitted forward and reflected backwards at inductive terminations which are typically present at HVDC link ends.

DC Current Rate Limiter (Link End Inductors)

DC link end inductors can effectively limit the rate of rise of dc current. In turn, the dc fault current magnitude is reduced at the instants of breaker tripping or converter blocking. For instance, the MTDC grid cases in this thesis are equipped with either 10 mH or 50 mH link end inductors. These values are considered as small ratings in the literatures [37, 84].

In steady-state operation, the dc current is constant and the voltage V_{Lle} across the link end inductor L_{le} is zero. In the case of a transient dc current, the voltage V_{Lle} changes proportionally to the inductor's size and current derivative as given by:

$$V_{Lle} = L_{le}\frac{di_{dc}}{dt} \tag{4.13}$$

Fig. 4.4 shows data of relay 21 due to the fault case at the 3-terminal dc grid (in Fig. 4.1). The voltage across the inductor next to relay 21 is illustrated in Fig. 4.4 (b).

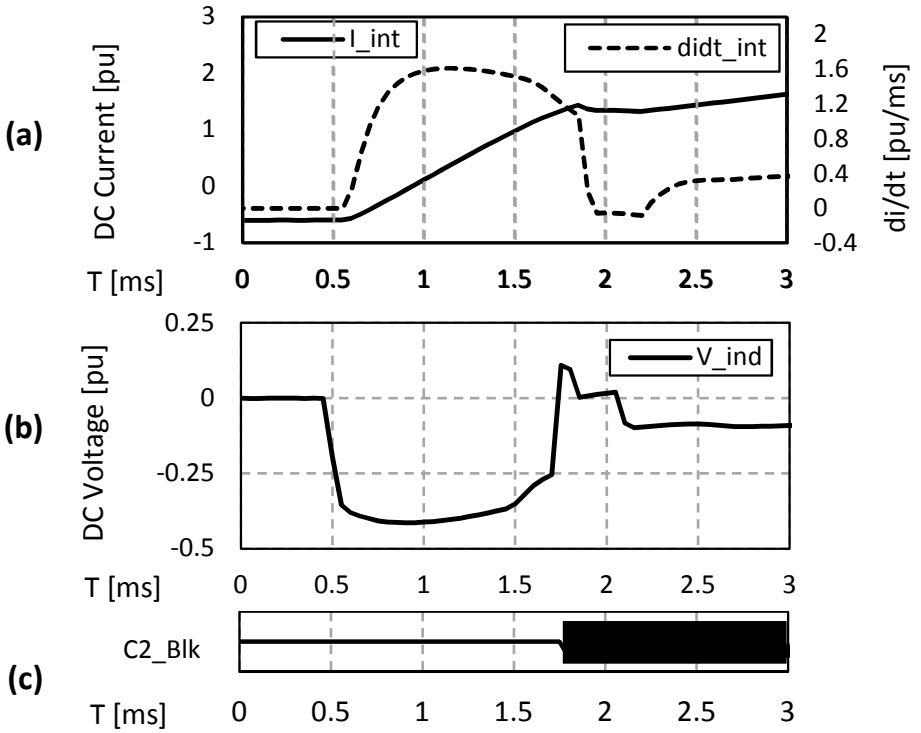

Fig. 4.4 Data associated with relay 21 and converter C2 including (a) current and current derivative, (b) voltage across inductor and (c) converter C2 blocking state.

As observed, the magnitude of the voltage across the inductor increases sharply with the arrival of the transient waves (at ≈ 0.5 ms). Then with converter blocking (at ≈ 1.7 ms), the submodule capacitive discharge is interrupted which leads to a reduction of the current contribution to the fault (Fig. 4.4 (a)). As the current derivative reduces, the voltage across the link end inductor also reduces.

At this point of writing, the propagation delay, the link end inductor and the converter blocking influence current and voltage behaviour. In order to clarify the influence of the converter blocking action, the terminal voltage is analysed prior to and following converter blocking instants.

Converter Blocking

Converter blocking occurs with fault detection at the converter station or with fault detection at a dc relay in the station's proximity. This action does not occur instantaneously after

fault detection but rather with a minimum processing delay of 0.1 ms (assumed in this thesis as the minimum recommended by the industrial sponsor). It should be noticed that the converter blocking action is a required action as it protects sensitive power electronic devices and interrupt capacitive discharge from submodules. In the case of converters with FB submodules, the blocking action also interrupts the ac current infeed.

The busbar dc voltage decays slower in comparison to the faulty link voltage in the period between the start of a fault and the converter blocking. This occurs because of two reasons. Firstly, the voltage decay at the terminal is limited as the voltage across the link end inductor increases. Secondly, converters provide voltage support in case of excessive voltage deviations. The thresholds of such deviations are set as $\pm$ 5% of nominal values which are pre-defined values for all converters in the network.

After converter blocking, the control functions (as dc voltage control) are no longer provided. In turn, this action accelerates the voltage drop which has been initiated previously by the dc fault. Therefore, the dc voltage at a terminal drops with a rate of change following a dc fault and drops with other rate of change following converter blocking. These voltage profiles propagate through the network and are observed at the relays downstream of such a converter. As a result, the dc voltage decay behaviour can be observed as dependent of firstly the dc fault and secondly the converter blocking actions.

Fig. 4.5 illustrates the dc voltage at the positive pole of a converter. As observed, the converter blocking action (at $\approx$ 1.7 ms) leads to a significant voltage drop, in comparison to the voltage drop caused by arrival of dc fault transient waves (at $\approx$ 0.5 ms).

DC voltage support due to the dc fault or the blocking of one converter is supported by the converters which are not blocked. This occurs by injecting more current or reducing the current export. As a result, rates of change of dc current occur with different slopes. These changes of rate are captured for analysis by the discrimination algorithm CRCC.

Capturing Magnitudes of DC Current Transients

The magnitude of transient waves can be analysed with several signal processing tools including fast Fourier transform (FFT), Laplace transform, discrete wavelet transform and derivative functions [94–96]. In recent literature, current or voltage derivatives have been widely used methods to capture transient behaviours [32, 37]. In this thesis, the transient

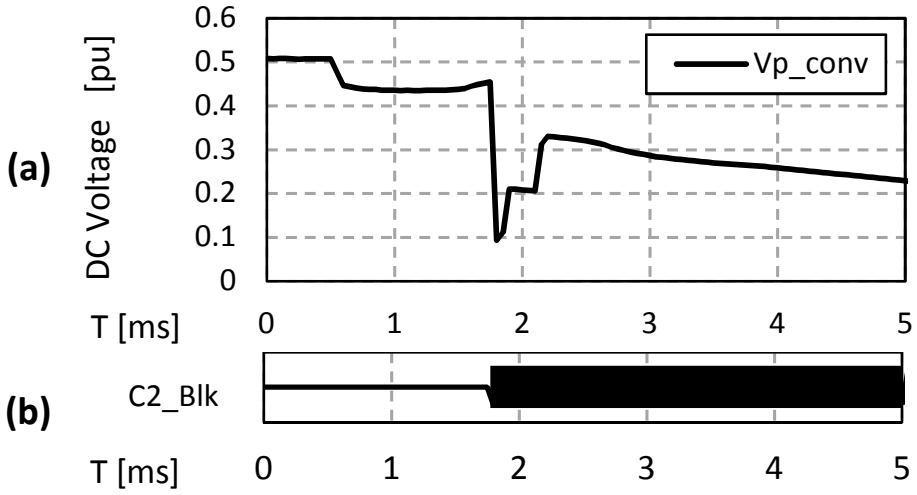

Fig. 4.5 (a) voltage at converter C2 terminal and (b) C2 blocking state.

waves are analysed with the second order current derivative function. A drawback of a derivative function is amplification of error. However, considering the good accuracy of commercial HVDC current sensors ($\pm$ 0.1 % for dc currents up to 600 kA [90, 97]), the second current derivative should be processed with a reduced error.

An alternative to the current derivative function is the analyses of voltage across a link end inductor [35, 33]. In fact, the profile of a voltage change across a link end inductor V_{Lt1} and V_{Lt2} is equal to the second order derivative of dc current:

$$\frac{V_{Lt2} - V_{Lt1}}{\Delta t} = \frac{\Delta V_{Lt}}{\Delta t} = \frac{dv_{Lt}}{dt} = L_t \frac{d^2 i_{DC}}{dt^2} \tag{4.14}$$

Two types of thresholds could be considered in the design of a protection algorithm. These are fixed thresholds or relative (variable) thresholds. In the first case, a fault is discriminated by comparison of *e.g.* current derivative with a pre-defined fixed threshold. Thresholds are calculated with basis on the prospective fault currents that should be known through analytic, simulation or experimental verifications. In the second case, relative thresholds are considered for discrimination purposes. These are compared against each other instead of being compared against a fixed pre-defined threshold. Hence, information about the prospective magnitude of fault currents or voltages is not required. Instead, the current or voltage behaviour (or pattern) should be known. The use of relative thresholds could

bring several benefits including robustness against high fault impedance and adaptability to different dc grid configurations.

Two magnitudes should be acquired in the design of a protection strategy with relative thresholds. Taking into account the dc voltage behaviour (as in Fig. 4.5), two events cause significant voltage drops. These are associated with the arrival of transient waves due to dc fault and due to converter blocking. As a result, these two events lead to the acquisition of the relative thresholds, referred in this thesis as *MaxInc* and *MaxRef*. These are associated with the incident wave and with reflected transient waves as:

Initiation: detection of a dc fault or of a dc disturbance
MaxInc: maximum of the incident wave
MaxRef: maximum of the reflected waves
Termination: blocking of local converter

The values *MaxInc* and *MaxRef* are identified in a period up to 2 ms which comprises the interval between detection of a disturbance and converter blocking. This is a necessary requirement as the blocking of HB or FB converters greatly distorts the local dc current and voltage. In addition, a protective decision achieved at an early stage (recommended as within 2 ms [16]) leads to an earlier fault clearance and to a lower fault current magnitude at the clearance instant.

These maximum values are critical points of the second order current derivative. Fig. 4.6 illustrates the relative thresholds for dc current fault case. The second order derivative is used to capture the thresholds.

The developed protection algorithm CRRC takes advantage of the two relative thresholds maximum of incident wave and global maxim of reflected waves.

Fault Discriminative CRCC criterion

The aim of the CRCC algorithm is to discriminate the faulty link in MTDC grid, independently of the link type. The discrimination criteria are based on maximum incident wave *MaxInc* and global maximum reflected wave *MaxRef*. Firstly, a criterion validates the value of *MaxInc*. This value should be higher than a residual threshold 'MaxIncThr' considered to avoid processing errors that appear when the dc current rate of change is very

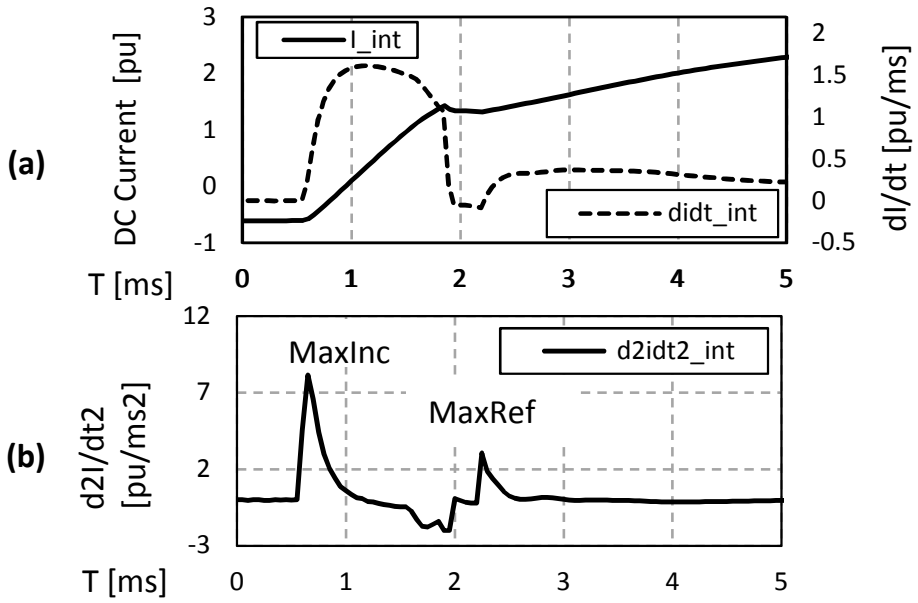

Fig. 4.6 (a) DC current with first derivative together with (b) second derivative. The thresholds *MaxInc* and *MaxRef* are acquired at the second order derivative

small. The threshold 'MaxIncThr' is set as 0.2 p.u./ms2 and is based on observations in PSCAD/EMTDC simulations. This criterion ensures that signal *MaxInc* is obtained at the first (incident) transient wave regardless of its amplitude.

Secondly, a fault is discriminated as internal if *MaxInc* is larger than *MaxRef*. Conversely, a fault is discriminated as external if *MaxInc* is smaller than *MaxRef*. The relation between the magnitudes of *MaxInc* and *MaxRef* is clarified in Fig. 4.7. This flowchart explains generic voltage and current profiles at three locations of a dc grid. The fault occurs in link whose currents and voltages profiles are given in the left-side column of Fig. 4.7. Then, the fault propagates to a nearby terminal (see central column) and after shortly after to non-faulty links (see right-side column).

Following a dc fault, the voltage decays greatly in the faulty link (*e.g.* 80% in 1 ms). This leads to a large magnitude of the incident current wave *MaxInc* (at the left-side column in Fig. 4.7). Shortly after, reflected waves are sensed by the relays at the faulty link. As the waves propagate through a network, these lose energy continuously until die out. This occurs because the dc current tends to reach a new steady-state fault level. For this reason, the reflected waves have small magnitudes in comparison to the incident fault wave. As a result, the *MaxRef* is smaller than *MaxInc* at the faulty link.

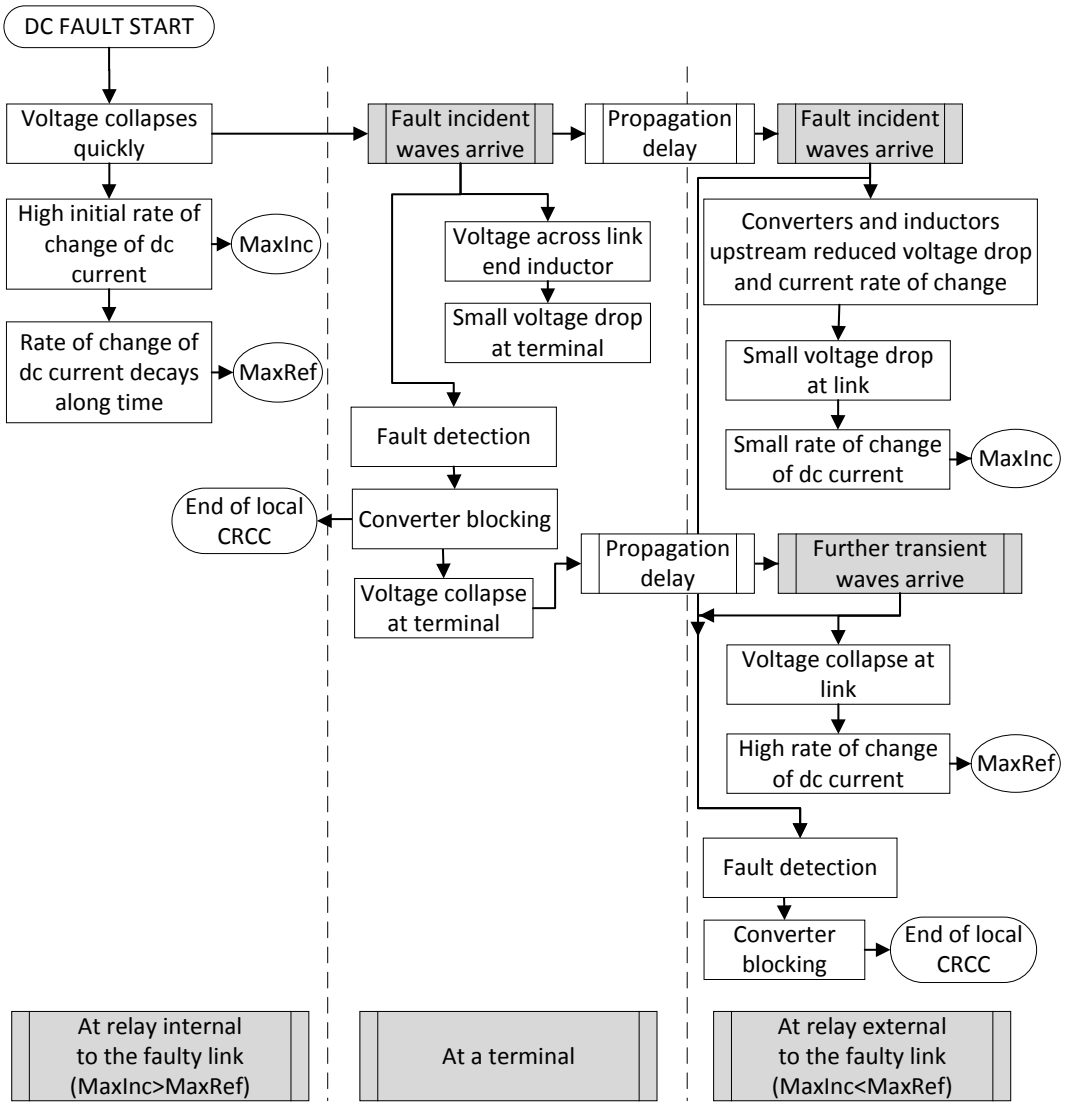

Fig. 4.7 Flowchart with generic magnitudes of currents and voltages at the faulty link, terminal next to the faulty link, and non-faulty link.

Once transient waves arrive to a termination, a voltage appears across the link end inductor. As a result, the voltage drop at the terminal due to the dc fault is relatively small (at the central column in Fig. 4.7). Shortly after, the blocking of a converter leads to the end of the discrimination algorithm at the local busbar unit. With such action the dc voltage collapses towards the voltage level imposed by the dc fault. Therefore, the transient waves caused by converter blocking propagate through the network.

After a propagation delay, fault incident waves arrive at non-faulty links (see right-side column in Fig. 4.7). The magnitude of these waves is relatively small as it is the voltage drop.

Shortly after, transient waves due to converter blocking also arrive at non-faulty links. The voltage collapses to the level imposed by the fault and the dc current experience a large rate of change. For this reason, the reflected waves have larger magnitudes in comparison to the incident fault wave. As a result, the *MaxRef* is typically larger than *MaxInc* at the faulty link.

The thresholds *MaxInc* and *MaxRef* are captured during the transient stage of dc fault currents as illustrated in Fig. 4.7. The generic magnitudes of these thresholds are illustrated in Fig. 4.8. According to the CRCC algorithm, internal dc fault currents have an initial high rate of change (4.8 (a)). Conversely, external dc fault currents experience an initial small rate of change that increases shortly after with the collapse of the network voltage (4.8 (b)).

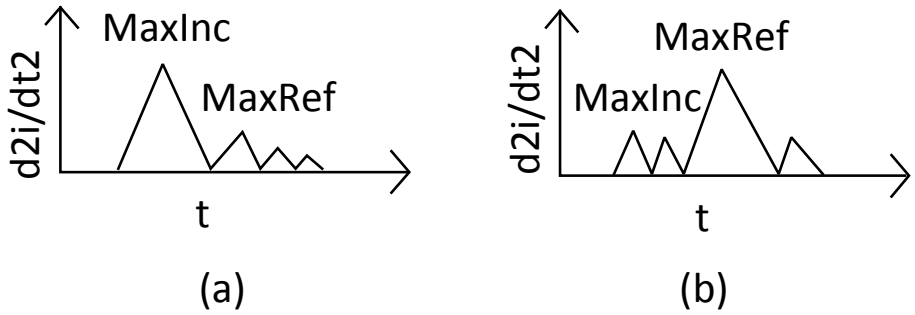

Fig. 4.8 Generic profile of current derivative in (a) a faulty link and in (b) a non-faulty link.

The CRCC algorithm terminated with the blocking of the local converter. At the end, the discrimination CRCC algorithm becomes:

If *MaxInc* > *MaxRef* and *MaxInc* > *MaxInc*Thr
Then the fault is considered internal to the link
Else the fault is considered external to the link

Verification with a 3-terminal DC Grid

Results of the CRCC algorithm's performance in a 3-terminal dc grid are given in this subsection. The fault location and voltages in several points of the radial grid are illustrated in Fig. 4.9. The fault occurs at 100 km from relay B21 and starts at 0 ms. Fig. 4.9 should draw the attention for two aspects. Firstly, the voltages closer to the fault location are much lower in comparison to voltages measured in more remote locations. Secondly, a voltage

appears across the inductor next to relay B21 that temporarily 'separates' the faulty area from the non-faulty area. It should be noticed that at 1 ms, the faulty area has a voltage of nearly 0 p.u. while the non-faulty area has a voltage much higher than 0.25 p.u. The voltage drops in Fig. 4.9 are associated with rates of change of current that are analysed by the CRCC algorithm. These rates of change (referred as *MaxInc* and *MaxRef*) are captured in each dc relay.

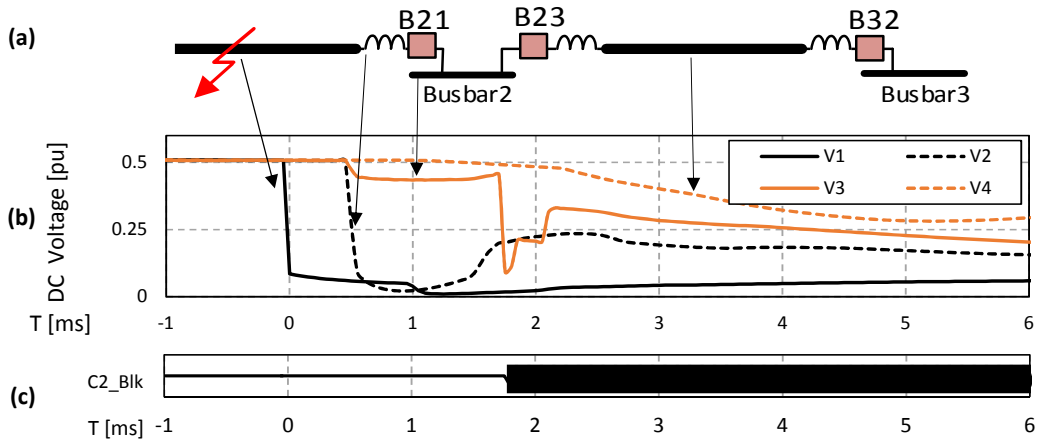

Fig. 4.9 Magnitude of dc voltage following a dc fault event. (a) Radial dc network, (b) dc voltage and (c) blocking of converter at busbar 2.

Fig.4.10 illustrates data for an internal and an external dc relay which correspond to relays B21 and B32 (in Fig. 4.9 (a)), respectively. In Fig. 4.10 (a), the dc current changes markedly with the arrival of transient waves while the dc voltage collapses. The *MaxInc* is associated with the incident transient wave and *MaxRef* is associated with the following reflected waves. By comparing *MaxInc* with *MaxRef*, the profile in Fig. 4.10 (a1) is classified as internal to the faulty link. Converter C2 which is in between the faulty and the non-faulty link, blocks approximately 1 ms after the arrival of the transient waves (see Fig. 4.10 (a3,b3)).

In Fig. 4.10 (b), the arrival of transient waves leads to an increase of the current rate of change together with a voltage drop represented by the negative derivative of dc voltage (see Fig. 4.10 (b2)). The *MaxInc* is captured with the incident wave. From approximately 3 ms, the current rate of change experiences a stepper increasing slope. The same behaviour occurs to the dc voltage which derivative decreases faster in comparison to pre-3 ms instant. This change occurs with to the arrival of transient waves due to blocking of converter C2, marked with the dashed line. The *MaxRef* is captured is the maximum local of the reflected waves

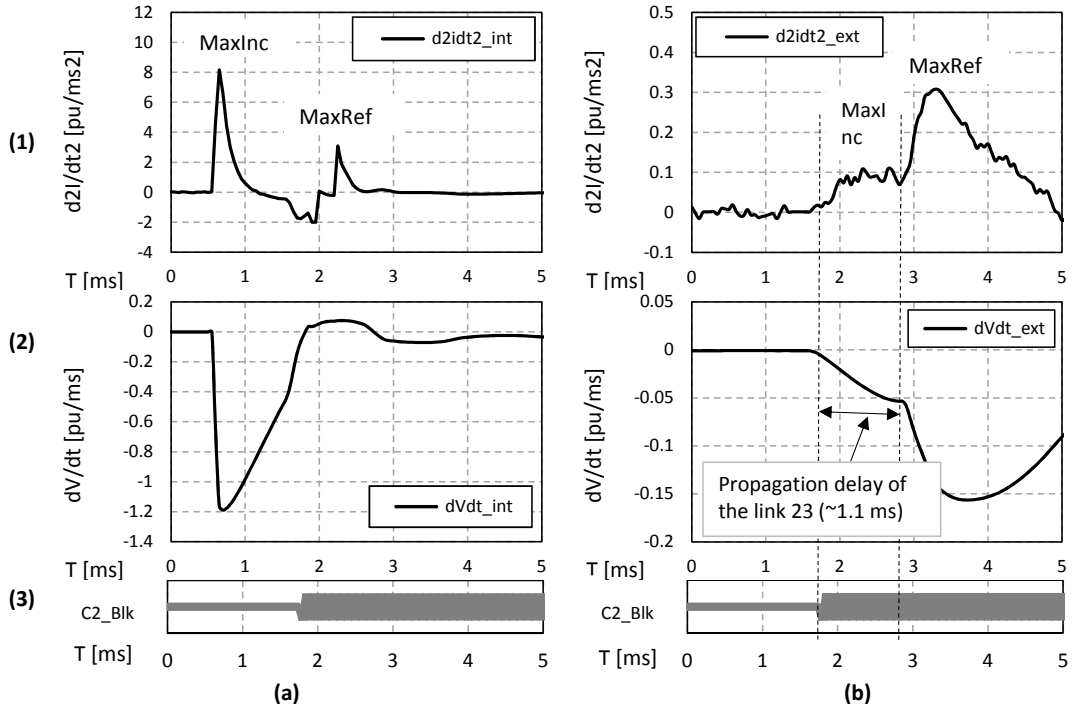

Fig. 4.10 Data analysed by the CRCC algorithm for (a) internal dc relay and (b) an external dc relay. In (a1, b1) dc current second order derivative, (a2, b2) voltage derivative and (a3, b3) converter C2 blocking state.

which is captured after 3 ms. By comparing *MaxInc* with *MaxRef*, the profile in Fig. 4.10 (b) is classified as external to the faulty link.

4.3.2 Sign of Current Derivative

The sign of the current derivative criterion is based on the direction of dc current upon fault detection. This criterion is typically associated with link communications channels [38]. In such a case, fault discrimination can be achieved in every dc relay. In this thesis, communication links are not considered for designing protection algorithms due to communication delays. Therefore, the algorithm of the sign of current derivative is applied locally at the busbar unit level. This approach leads to partial discrimination only. The term "partial discrimination" means that dc relays is classified as potentially internal or as non-potential to a faulty link. In order to achieve full discrimination (only the dc relays at the faulty link are identified), the potentially internal dc relays are discriminated with the CRCC discrimination algorithm (Section 4.3.1).

The orientation of the dc current sensors plays a role in the sign of current derivative algorithm. For clarity, the current sensor orientation adopted is pointing from the busbar to the dc link on the positive pole, and in the opposite direction on the negative pole (as illustrated in Fig. 4.11).

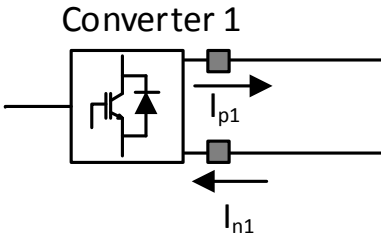

Fig. 4.11 Orientation of the current sensor at the positive and negative pole.

Considering the current sensor orientation in Fig. 4.11, a dc relay is classified as potentially internal to a dc faulty link if the associated dc current sensor experiences a positive rate of change on the positive pole (or opposite sign on the negative pole) as given in Eq. 4.15. This indicates that the dc fault current is flowing in the busbar-to-link direction. A dc relay classified as potentially internal to the faulty link can be either internal or external to the faulty link.

$$\frac{dI_p}{dt}(t) > 0 \tag{4.15}$$

Conversely, a dc relay is classified non-potential to the faulty link if the associated dc current sensor experiences a negative rate of change on the positive pole (or opposite sign on the negative pole) as given in Eq. 4.16. This indicates that the dc fault current is flowing on the link-to-busbar direction. A dc relay classified as non-potential to the faulty link must be external to a faulty link.

$$\frac{dI_p}{dt}(t) < 0 \tag{4.16}$$

Fig. 4.12 shows data related to the fault case of Fig. 4.1. The dc current and current derivative are shown for an internal dc relay (relay 21, Fig. 4.12(a)) and for an external dc relay (relay 32, Fig. 4.12(b)). Both of the dc currents experience initially an increasing

behaviour following the dc fault occurrence at time of 0 ms. Hence, both dc relays are classified as potentially internal to the fault link.

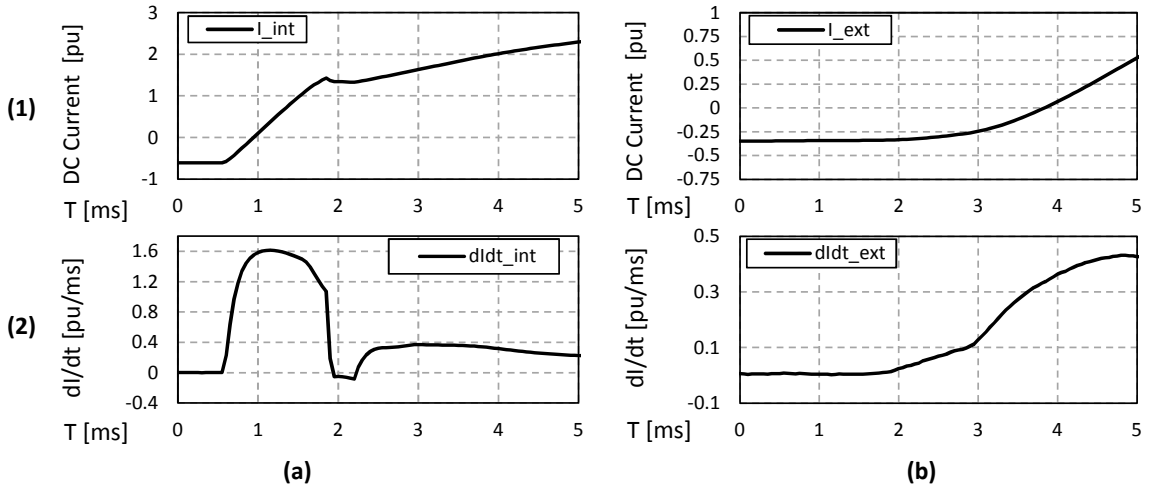

Fig. 4.12 DC current measurement at a dc relay (a1) internal and (b1) external to a faulty link. Similarly, dc current derivative at a dc relay (a2) internal and (b2) external to a faulty link.

In the unlikely event of having more than one dc current (in the same logic busbar unit) with a positive sign of current derivative, an additional criterion is considered to select only one potential dc relay. In such a case, the relay that has the largest dc current change is classified as potentially internal while the others are classified as external.

4.3.3 Voltage Recovery

A discrimination criterion is designed to decide the re-closing of fault isolation devices (either FDs or DCCBs) that are in the opening state at non-faulty links. In other words, the voltage criterion is considered to re-close devices (if required) while the criteria of sign of current derivative and CRCC are considered to selectively open isolation devices.

The voltage discrimination criterion (as the name suggests) is based on dc link voltage recovery. Voltage recovery occurs following fault clearance, fault isolation and converters' resuming operation. The latter action leads to recovery of the nominal dc voltage in a network. The voltage recovery is only observable on non-faulty links as at least one link end isolation device is in the closed state (as in Fig. 4.13). In this figure, B12 is ordered to reclose once dc voltage rises approximately to nominal values, *i.e.* from 0.3 s. It should be noticed that as the

faulty link is isolated from the non-faulty network (FDs or DCCBs at the faulty link are open at both ends), the voltage is not restored in such a link.

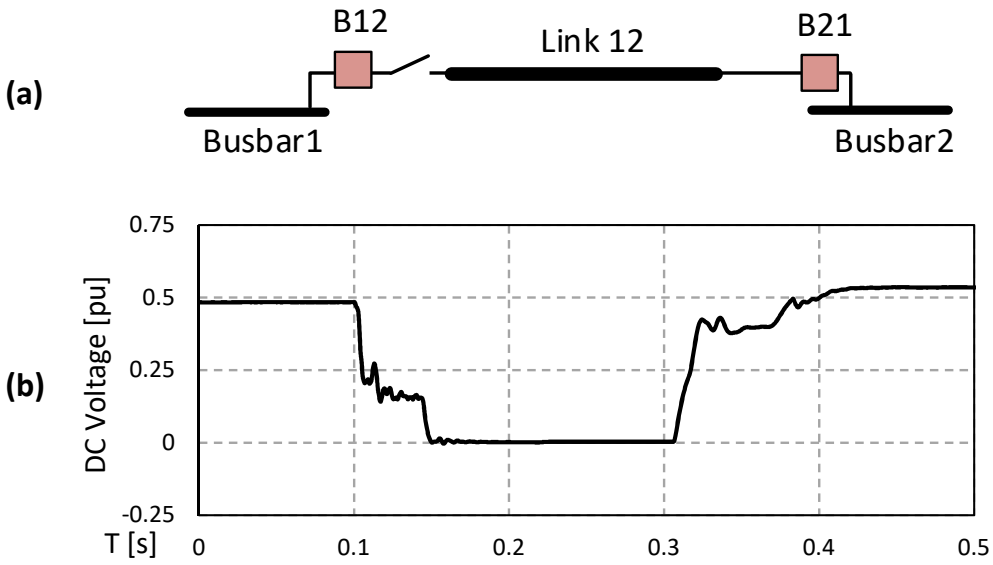

Fig. 4.13 (a) Non-faulty link and (b) voltage collapse and restoration.

The voltage recovery criterion discriminates a fault as external if the P2P and P2Gnd dc voltage recovers to approximately nominal values as given by:

$$V_{pn} > 0.9 \text{ pu} \tag{4.17}$$

$$V_p > 0.3 \text{ pu} \text{ and } V_n < -0.3 \text{ pu} \tag{4.18}$$

The thresholds in (4.17) (4.18) have been defined after analysing the dc voltage recovery following an extensive number of simulations of the test system. These values should be bespoke for each specific MTDC grid project.

4.4 Summary

Adequate fault detection and fault discrimination algorithms are a major requirement for safe operation dc networks. These algorithms should be fast and sensitive. The time to achieve fault detection is typically very short, *e.g.* within 1 ms. The algorithms that lead to the detection of dc disturbances include overcurrent, undervoltage and current derivative.

Three algorithms are given for fault discrimination. The first algorithm (the developed CRCC criterion) leads to fault discrimination in a short period of time (typically < 2 ms). The second algorithm is based on the sign of current direction. The third algorithm is based on voltage recovery. The latter two algorithms are based on the literatures and are simple methods to achieve a certain degree of discrimination. All the algorithms consider only local dc current measurements for decision making.

The fault detection and fault discrimination algorithms are supported with results based on a simple 3-terminal dc grid (given in Fig. 4.1). These algorithms should be integrated in protection strategies as it will be explained in the following chapters.

Chapter 5

Proposed Protection Strategy for MTDC Grids equipped with AC Circuit Breakers

5.1 Introduction

ACCBs have been employed to protect point-to-point dc links [20] and the first MTDC grids [75]. Although they constitute a mature technology, the main disadvantages of using ACCBs are their relatively long operation time and the temporary outage caused to the whole dc network.

The use of ACCBs for the protection of MTDC grids has been examined in the literatures. In the "handshaking" method [24] (described at Section 2.5.1), fault clearance is achieved by the opening of ACCBs and fault isolation is achieved by the opening of FDs when the current becomes zero. MTDC grid restoration occurs with ACCB reclosing actions. A fixed time delay (*e.g.* 100 ms) due to ACCB operation is considered as part of the restoration process. However, if the fault is not isolated within that period, the grid restoration process may re-initiate the dc fault. To avoid this issue, a larger delay would be required at the expense of increasing the outage time of an MTDC grid –which may not be desirable.

In order to reduce the outage time of an MTDC grid protected by ACCBs, a methodology is proposed. The algorithm, referred here as progressive protection strategy (PPS), uses

ACCBs to clear dc faults and FDs to isolate dc links. The PPS exploits the possibility of restoring parts of the network at different times. Hence, power restoration might occur in a part of the grid even if the faulty link is not completely isolated from the dc grid. This way, the power transfer between ac systems connected through dc links occurs faster in comparison to conventional methods. Reduction of the MTDC grid outage time brings additional benefits, including a reduction in the energy not supplied, and a reduced impact on stability and frequency deviations of adjacent ac systems [98, 13, 99].

The application of the PPS in large MTDC grids may not be suitable as it would lead to a power in-feed loss at a scale that might not be acceptable to transmission system operators. However, it represents a viable and economic option to protect smaller sections of a large MTDC grid that is segregated into small zones by DCCB operation [62].

5.2 Progressive Protection Strategy (PPS)

The PPS algorithm, if adopted, should be implemented in every busbar unit of an MTDC grid. Each unit will exchange data with the neighbouring dc relays, converter station and ACCB. A busbar unit receives current and voltage measurements from local dc relays, runs the PPS algorithm and, as necessary, sends opening/closing orders to the associated ACCB and FDs together with blocking/de-blocking orders to the associated converter. In the case of a dc fault, the PPS will detect it, discriminate it and initiate a protection sequence of these units. This process is described in detail in the following subsections.

5.2.1 DC Fault Detection and Clearance

The fault detection criterion is based on link overcurrent or undervoltage (introduced at Section 4.2). The instant of the fault detection t_{det} is determined by the delay of the arrival of transient waves to a dc relay (based on a propagation delay t_{prop}) and a threshold transgression delay t_{tra}, associated to current or voltage measurements, Eq. 5.1.

$$t_{det} = t_{prop} + t_{tra} \tag{5.1}$$

Fault detection is typically achieved within 1 ms after the arrival of the transient waves. Following fault detection at a busbar unit, three actions occur in parallel:

a) Blocking of the associated converter (if in de-blocked mode):

The converter blocking actions protect internal power electronic components while preventing capacitance discharge to the dc fault. This action does not interrupt fault current path as an ac infeed current flows through the uncontrolled diodes in the HB submodules.

In addition, a converter blocks in the case of overcurrent detection in the positive or negative pole, regardless of the orders from the PPS.

b) Opening order of the associated ACCB:

ACCBs receive and opening order as they perform the dc current fault clearance process. The opening order of ACCBs has a time delay of 2 ac cycles. Therefore, in PSCAD/EMTDC simulations, the ACCBs typically open at ≈ 50 ms after the start of the fault.

With the ACCB opening, the ac current infeed is interrupted and the dc current decays towards zero. Once the dc current decays below a residual breaking capability of the FDs, these are able to open and ensure link isolation.

c) Discrimination of 'potential' and 'non-potential' FDs:

The fault discrimination process relies on the identification of 'potential' and 'non-potential' FDs. 'Potential' FDs include those placed in the faulty link and in s number of non-faulty links. This implies that the fault location is partially discriminated at this stage. 'Non-potential' FDs are identified as those placed in non-faulty links. Identification of the 'potential' FDs is based on the sign of current derivative algorithm (see Section 4.3.2).

Each busbar station should have one FD classified as 'potential' which is the FD most likely to be internal to the faulty link. The other FDs associated with the same busbar station are classified as 'non-potential'. In the case of parallel dc links, multiple FDs may be classified as 'potential'.

It should be noticed that the current derivative sign may be positive in more than one link connected to the same busbar. To identify the most suitable 'potential' FD, a current magnitude criterion is used. The FD that exhibits the largest positive current derivative is defined as 'potential'. The remaining FDs associated to the same busbar unit are classified as 'non-potential'.

5.2.2 Fault Isolation

Following ACCBs opening operations, the dc fault current magnitude starts to decay towards zero. The decaying time is dependent on the fault current I_0 at the clearance instant and on the equivalent resistance R and inductance L of the fault discharge path. This can be mathematically expressed as:

$$I_{dc}(t) = I_0 \, e^{-\frac{R}{L}t} \tag{5.2}$$

The time constant (L/R) is larger for a low impedance fault which constitutes the most common fault type [100]. Once the dc line currents decay below the residual breaking capability of the FDs, all of these devices open. This operation is achieved following a period of tens of milliseconds to seconds.

Fig. 5.1 illustrates a typical dc fault current profile where ACCBs are considered for fault clearance. Converter blocking occurs after fault detection while ACCB opening occurs with an approximately 50 ms delay. In this fault case, the dc current decays to nearly zero (at approximately 250 ms after the start of the fault) which enables FD opening operation.

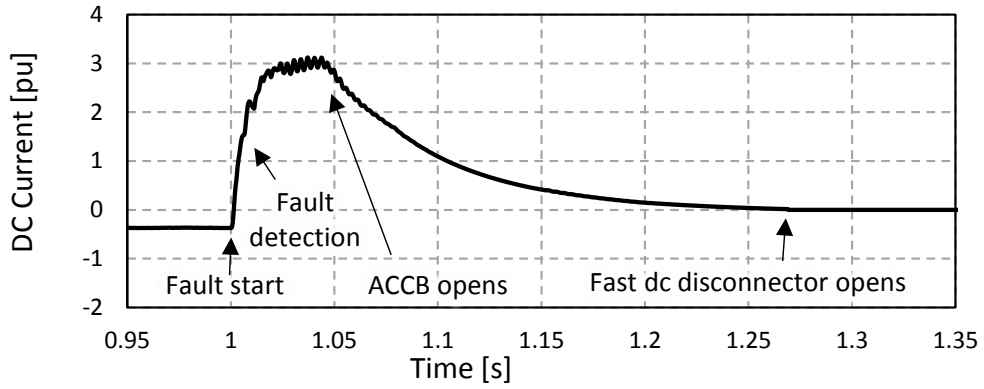

Fig. 5.1 Generic dc fault current behaviour.

The decaying behaviour of the dc fault current delays the isolation actions and, consequently, holds up the grid recovery process. This is a major constraint for MTDC grid equipment relying on ACCBs for protection. However, this shortcoming is partially mitigated by the PPS by reducing the overall network outage time.

The PPS has a non-discriminative FD opening algorithm and a discriminative FD reclosing algorithm. Hence, all the FDs receive an opening order. Once an FD opens, it is required

to remain in open mode for a minimum period of time Δt_{is}. This time lag is considered in order to avoid the reclosing of an FD before the opening of the FD at the other link end. This period of time is assumed as 10 ms in case of P2P faults and as 40 ms for P2Gnd faults. The reason for a larger waiting time in P2Gnd faults is due to an additional overvoltage suppression operation. This action is performed using a resistive discharge circuit whose principles are detailed in Section 5.2.3.

5.2.3 Overvoltage and Voltage Imbalance Suppression in case of P2Gnd fault

A P2Gnd fault in a symmetrical monopole network causes the voltage collapse in the faulty pole while the voltage in the healthy pole moves towards twice the nominal value. The healthy pole overvoltage and voltage imbalance must be suppressed before the re-start up of the dc network. Such overvoltage decays naturally to zero but in a process that can last from hundreds of milliseconds to seconds. In order to accelerate this process, resistive discharge circuits are considered. These have the function to quickly discharge the energy in the overvoltage pole to the ground.

These are based on switches (such as an FD) that connect each pole to the ground through a resistor, as shown in Fig. 5.2. The ground switches (GS_P, GS_N) and a discharging resistor (R_{gs}) are considered at each link end. In practical terms, the mentioned ground switches would operate as fast fault thrower switches with a high current discharge capability (*i.e.* several kA) [101].

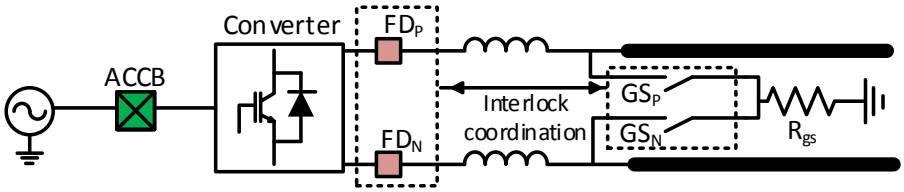

Fig. 5.2 Configuration of a grounding switch.

The ground switches are normally in the open state. These close if a P2Gnd fault is detected and if it is associated to a 'non-potential' disconnector in open mode (in the positive and in the negative poles). The re-open operation occurs once the dc voltage and the dc

current flowing through the discharge resistor decay to a residual value. Once the switch re-opens, the operation of the associated FD is resumed. An interlock coordination signal between the FD and the switch inhibits the closed mode of them at the same instant.

The smaller the size of the resistor R_{gs}, the shorter time it requires to discharge the link energy. Assuming a withstanding current peak of 4 kA, a 50 Ω resistor is considered. This value leads to a link energy discharge within 10-15 ms.

5.2.4 Grid Restoration: Reclosing 'Non-potential' FDs

Once all the FDs associated to a busbar station are opened, the discriminative reclosing process starts. Grid restoration occurs with three actions.

1. Reclosing of the 'non-potential' FDs once the 'potential' FD opens;
2. Reclosing of the ACCB, if associated with a converter in pre-fault rectifier mode, after the reclosing operation of any FD. This action leads to partial dc voltage recovery on non-faulty dc links.

   The reclosing of the ACCB, if connected to a converter in pre-fault inverter mode, occurs with dc link voltage recovery. This action leads to current flow restoration.

   This criterion keeps the power exchange between ac and dc grids with the same direction at both the pre-fault and dc grid recovery periods. An ac grid exporting power at the pre-fault instant will export power during grid recovery by means of a converter in rectifier operation. Conversely, an ac grid importing power at the pre-fault instant will import power during grid recovery by means of a converter in inverter operation.
3. De-blocking of a converter once the following criteria are met:

   a) The ACCB is closed;

   b) The voltage has recovered (as given in Section 4.3.3)

   The converter will be de-blocked after the ACCB reclosing operation is concluded to prevent harmful switching transients. With these requirements, the de-blocking starts typically $\approx$ 10 ms after an ACCB reclosing operation.

The resuming operation of ACCBs and converters allows the nominal voltage re-establishment in the non-faulty part of the network. The power flow initiates at dc links if both link end FDs are in the closed mode.

5.2.5 Grid Restoration: Reclosing 'Potential' FDs

At this instant, part of the dc grid is restored. In order to restore the remaining non-faulty links, a dc voltage criterion is considered. The voltage criterion does not only reclose dc FDs at non-faulty dc links but more importantly, it re-closes them at a safe time when the fault is isolated. This means that dc voltage works as a link communication channel that does not allow reclosing actions without fault isolation. For this reason, discriminative algorithms, such as the proposed CRCC, are not considered in the PPS. Although the CRCC could discriminate the dc relays, it does not recognise the best time to reclose the FDs at non-faulty links which is the purpose of the voltage recovery criterion.

The re-closing of 'potential' FDs placed at non-faulty links occurs if the dc link voltage meets one of two criteria. The first criterion is based on dc link voltage recovery as introduced in Section 4.3.3.

The second criterion is based on detection of an overvoltage suppression action. This action occurs due to the operation of resistive discharging circuits which are performed only in case of a P2Gnd fault (see Section 5.2.3). The discrimination criterion is based on voltage drop to zero at the non-faulty pole which occurs with overvoltage suppression action. This behaviour can be capture with an overvoltage pole detection (given in Eq. 5.3), overvoltage raises/decay towards zero (given in Eq.5.4) and residual voltage measurements (given in Eq. 5.5).

$$V_p > 0.55 \text{ pu} \quad or \quad V_n < 0.55 \text{ pu} \tag{5.3}$$

$$\frac{dV_p}{dt} < 0.01 \text{ pu} \quad or \quad \frac{dV_p}{dt} > 0.01 \text{ pu} \tag{5.4}$$

$$V_p < 0.05 \text{ pu} \quad and \quad |V_n| > 0.05 \text{ pu} \tag{5.5}$$

The thresholds in the equations above are based on extensive observations in PSCAD simulations. The criterion in Eq. 5.3 is only satisfied in P2Gnd faults, as an overvoltage

(assumed as nominal voltage plus a 10% margin) appears in one pole, a behaviour that is not possible in P2P faults as the voltage collapses in both poles. The criterion in Eq. 5.4 is satisfied if the dc link energy is quickly discharged to zero through means of a ground switch. In this case, natural energy discharge though link shunt capacitance would last for a long period of time (varying from seconds to hours) which is considerably below the 0.01 pu/ms threshold. Lastly, grid restoration may start once the overvoltage suppression action terminates, which is given by a residual and symmetrical voltage at both poles (ideally 0.0 pu). Therefore, if the voltage is assumed as below 0.05 pu as in Eq. 5.5, and in combination with criteria in Eq. 5.3 and Eq. 5.4, the dc link is discriminated as external to the fault and is ready to be restored.

Fig. 5.3 illustrates the voltage criteria in a P2Gnd fault case. It should be noticed that the events of overvoltage, overvoltage raise/decay towards zero and residual voltage detection occur in a sequential way at non-faulty dc links. Lastly, in order to avoid misjudgement due to transient voltages, the above criteria must last for a minimum period of time, *e.g.* 0.5 ms.

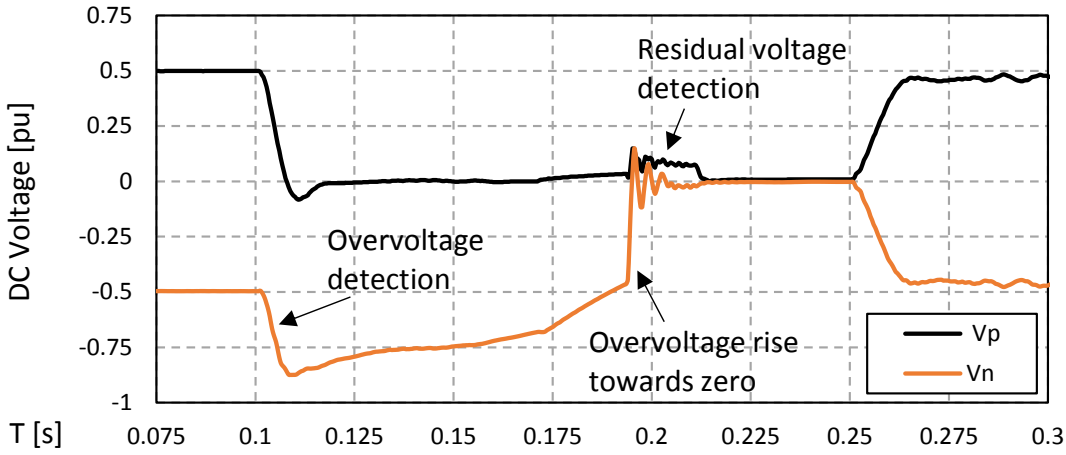

Fig. 5.3 DC voltage behavior following P2Gnd fault and overvoltage suppression events.

Once the 'potential' FDs placed at non-faulty links are identified, these receive a reclosing order. The grid restoration within this step is as follows:

1. Reclosing of the 'potential' FD once one voltage criterion is met;
2. Reclosing of the ACCB (if in open mode). The ACCBs associated with converters in rectifier mode de-block and restore dc voltage. The ACCBs associated with converters in inverter mode de-block only once dc voltage is restored.

3. De-blocking of a converter (if in blocking mode) if:

   i) The ACCB is closed;

   ii) The voltage has recovered (as given in Section 4.3.3)

At this point, all ACCBs have been reclosed, the converters have been de-blocked and the FDs placed at non-faulty links have been reclosed. The faulty link remains isolated by the open mode of the 'potential' FDs placed at each link end.

5.2.6 Summary of the PPS

Fig. 5.4 shows a comprehensive flowchart of the PPS. The sequence of actions is as follows:

1. DC fault detection.
2. Initial protective actions:
   (a) Converter blocking order;
   (b) Identify 'potential' and 'non-potential' FDs;
   (c) ACCB opening order.
3. FDs opening operation.
4. Ground switch operation if overvoltage is detected.
5. Grid restoration I:
   (a) Reclose 'non-potential' FDs;
   (b) Reclose ACCB;
   (c) De-block converter.
6. Evaluate voltage restoration.
7. Grid restoration II:
   (a) Reclose 'potential' FDs;
   (b) Reclose ACCB (if open);
   (c) De-block converter (if blocked).

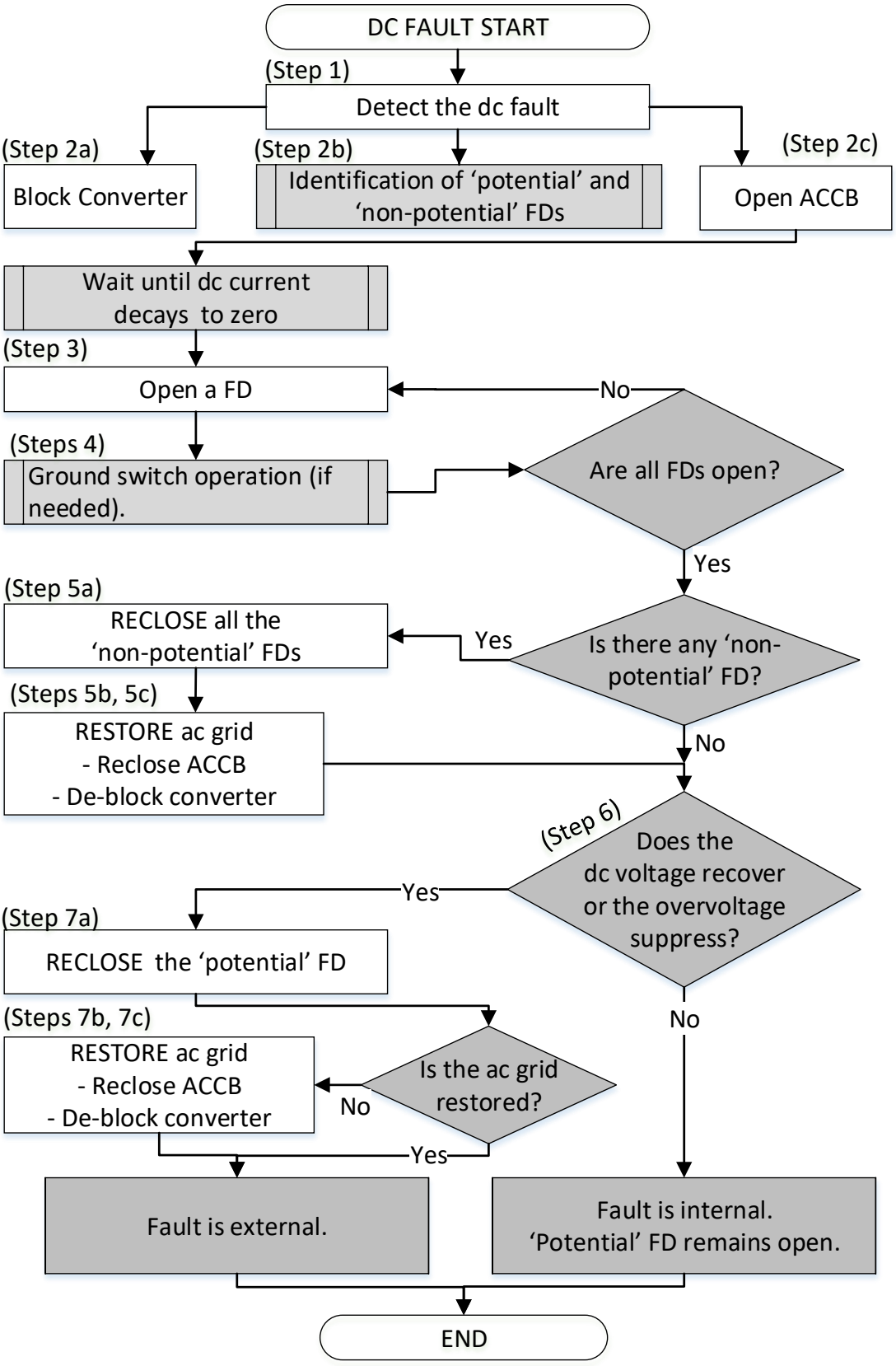

Fig. 5.4 Detailed flowchart of the PPS for an individual busbar station.

5.3 Simulation Results

Two fault cases are used to test the PPS (see Fig. 5.5). In the first case, a P2P fault occurs on link 12, 30 km away from dc Relay 21 with a fault impedance of 0.1 Ω. In the second case, a P2Gnd fault occurs at the middle of link 24 with a fault impedance of 10 Ω.

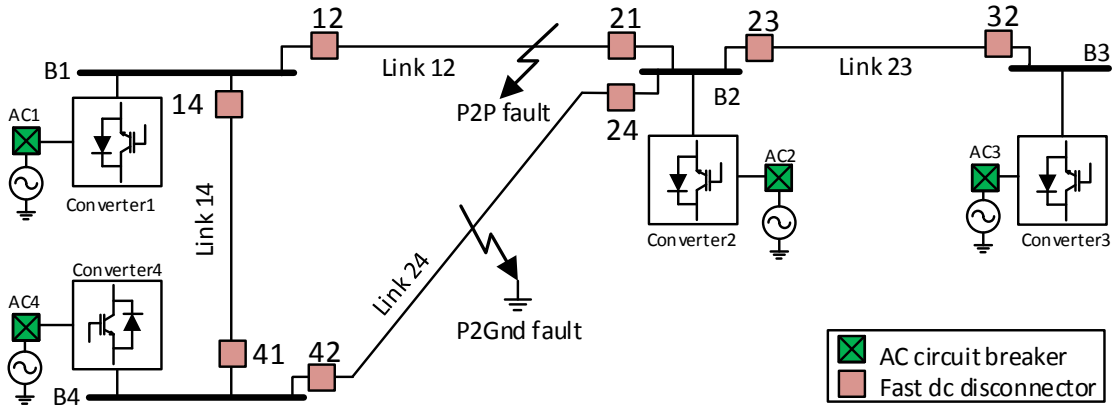

Fig. 5.5 MTDC grid case study with location of the fault scenarios.

The fault location or fault impedance value does not affect the behaviour of the PPS as the algorithm is only sensitive to the fault detection criteria (see Section 4.2) and FD classification based on the sign of current derivative (see Section 4.3.2).

5.3.1 Pole-to-Pole Fault

A P2P fault occurs at 0.1 s and is detected within 1 ms after the arrival of transient waves. Considering that link propagation delay occurs, fault detection is achieved at all dc relays within 3 ms after the start of the fault. This is Step 1 in Fig. 5.4.

Fig. 5.6 illustrates a time window of the whole fault clearance, isolation and grid restoration process. The thick lines represent the blocking of converters, opening of ACCBs and opening of FDs. Fig. 5.7 shows the positive pole dc current and voltage in a number of dc relays and the current output of the converters. As it can be seen in Fig. 5.6 (a), the converters are blocked within a few milliseconds after the start of the fault (Step 2a in Fig. 5.4).

In the discrimination process (Step 2b), each busbar unit classifies the FDs as 'potential' or 'non-potential'. The 'potential' FDs which exhibit a positive sign of current derivative

(see Section 5.2.1) are FDs 12, 21, 32 and 42. In Fig. 5.7 (a), the dc currents that have an increasing behaviour shortly after 0.1 s are associated with 'potential' FDs. Curve 'I14p', associated with FD 14, has a decreasing behaviour which relates to a negative sign of the current derivative. With this criterion, FDs 14, 41, 23 and 24 are classified as 'non-potential'. The opening order of ACCBs occurs after fault detection (Step 2c) but the opening operation occurs only at $\approx$ 50 ms following the dc fault (see Fig. 5.6 (b)). From this instant, the dc current starts to decay to zero at the dc links and converters, as shown in Figs. 5.7 (a) and 5.7 (c).

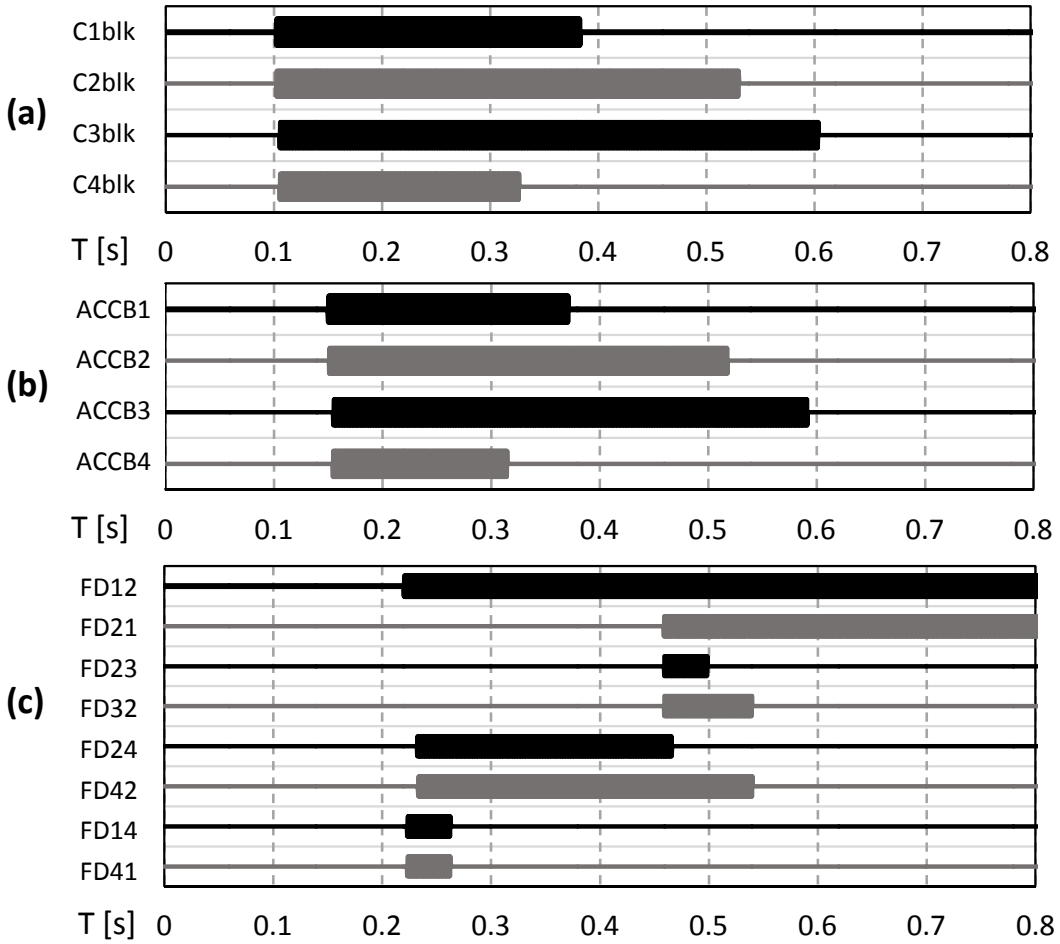

Fig. 5.6 State of (a) the converters, (b) ACCBs and (c) FDs for the P2P fault case.

In Step 3, the opening operation of FDs occurs once the dc fault current decays to nearly zero. The opening and reclosing times are illustrated in Fig. 5.6 (c). For instance, 'FD14' in Fig. 5.6 (c) opens once 'I14p' in Fig. 5.7 (a) reaches a nearly zero magnitude which occurs

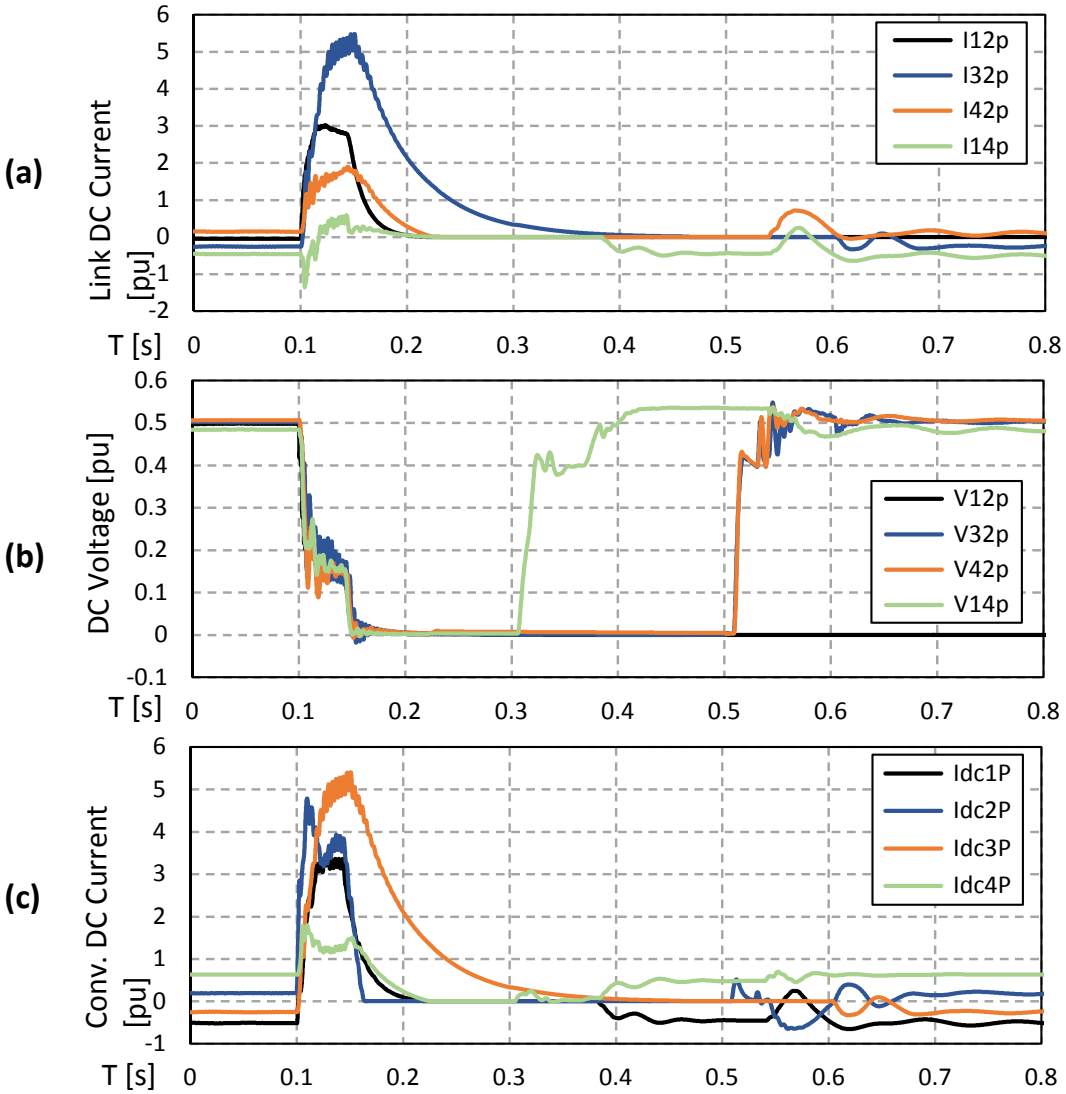

Fig. 5.7 DC (a) link currents, (b) link voltages and (c) converter currents for the P2P fault case.

at ≈ 0.22 s. However, 'FD21', associated with dc current 'I21p', is able to open only at a later stage at ≈ 0.45 s.

Step 4 is not applicable for P2P faults as there is no dc overvoltage. This will be described in the P2Gnd fault case.

All FDs associated with busbar units 1 and 4 (FDs 12, 14, 41 and 42) open at ≈ 0.22 s as shown in Fig. 5.6 (c). As a result, Step 5 starts in these busbars. Firstly, 'non-potential' FDs 14 and 41 receive a reclosing order (Step 5a). This leads to the restoration of link 14. Firstly, in Step 5b, ACCBs 4 (associated to converter C4 which was in rectifier mode) reclose at

≈ 0.31 s (see Fig. 5.6 (b)). ACCBs 1 (associated to converter C1 which was in inverter mode) reclose at ≈ 0.38 s. From the reclosing of ACCBs 1 and 4, a dc current flows through the uncontrolled diodes and raises the dc voltage of link 14 to 'V14p' in Fig. 5.7 (a). In Step 5c, Converters 1 and 4 de-block (see Fig. 5.6 (a)). At this instant (≈ 0.39 s), the power flow on link 14 restores as evidenced by 'I14p' and 'V14p' in Figs. 5.7 (a) and 5.7 (b). Restoration of link 14 occurs before isolation of the faulty link 12 (≈ 0.45 s).

At ≈ 0.45 s, FDs 21, 23 and 32 open (see Fig. 5.6 (c)). As all FDs associated to busbar unit 2 are open, Step 5 starts (this step has already been concluded for busbar units 1 and 4). At busbar unit 2, 'non-potential' FDs 23 and 24 reclose (Step 5a), ACCB 2 recloses (Step 5b), and Converter 2 de-blocks (Step 5c). These actions are represented by the changes of thick to thin lines of 'FD23', 'FD24', 'ACCB2' and 'C2blk' in Fig. 5.6. Such actions lead to voltage restoration at non-faulty links 23 and 24 at ≈ 0.51 s (see Fig. 5.7 (b)). At busbar unit 3, Step 5 is not applicable as there are no 'non-potential' FDs.

Step 6 relates to the discrimination of 'potential' FDs placed at faulty links (FDs 12 and 21) and at non-faulty links (FDs 32 and 42). Voltage restoration occurs next to 'potential' FDs 32 and 42 as seen by 'V32p' and 'V42p' at ≈ 0.51 s in Fig. 5.7 (b)). As result, Step 7 starts at busbar units 3 and 4 (associated to FDs 32 and 42, respectively).

Step 7 relates to grid restoration actions. In Step 7a, 'potential' FDs 32 and 42 reclose (≈ 0.53 s in Fig. 5.6 (c)). These are discriminated in Step 6. At this instant, the protection algorithm terminates in busbar unit 4 as all devices are reclosed and Converter 4 is de-blocked. In busbar unit 3, the ac grid is not yet restored. Hence, in Step 7b ACCB 3 recloses and in Step 7c Converter 3 de-blocks ('ACCB3' and 'C3blk' in Figs. 5.6 (b) and 5.6 (a)). Following these actions, the protection algorithm terminates for busbar unit 3. The voltage does not restore on link 12 and the fault is discriminated as internal to their 'potential' FDs 12 and 21.

By the end, only those FDs placed on the faulty link are in open state. The fault is discriminated and the non-faulty part of the dc grid is recovered in a progressive manner. Link 14 voltage is restored at approximately ≈ 0.31 s while remaining non-faulty links are restored at approximately ≈ 0.51 s.

5.3.2 Pole-to-Ground Fault

The fault starts at 0.1 s. Fault detection is achieved within a few milliseconds after the start of the fault (Step 1 in Fig. 5.4). As a consequence, the converter blocking orders (Step 2a), the identification of 'potential' and 'non-potential' FDs (Step 2b) and the ACCB opening orders (Step 2c) are set.

Fig. 5.8 shows the device operations during the fault clearance, isolation and grid recovery actions. These include the blocking of converters, the opening of ACCBs, opening of FDs and the closing operation of a number of ground switches. Fig. 5.9 shows a number of signals during application of the protection strategy, including current and voltage measurements in a number of dc relays and the dc current output at each converter.

In Step 2b, FDs 14, 24, 32 and 42 are identified as 'potential'. These exhibit a positive sign of current derivative after the start of the fault as seen by the increasing behaviour of dc current (*e.g.* 'I42p' in Fig. 5.9 (a)). FDs 12, 21, 32 and 41 are identified as 'non-potential' since they feature a negative sign of the current derivative as seen by the decreasing behaviour of dc current following the arrival of transient waves (*e.g.* 'I41p' in Fig. 5.9 (a)).

In Step 3, FD opening operations at $\approx$0.17 s are shown in Fig. 5.8 (c). For P2Gnd faults, FDs shall be in open mode for a minimum time period, assumed as 40 ms. During this period, the opening and reclosing operation of grounding switches is performed.

In Step 4, the grounding switches in the non-faulty links are closed as seen in Fig. 5.8 (d). This operation drives the overvoltage at the non-faulty pole to zero as seen at $\approx$0.2 s by, for example, 'V41n' in Fig. 5.9 (c).

Steps 5 and 6 occur in parallel for P2Gnd faults. In Step 5a, 'non-potential' FDs reclose. This is represented by a change from thick to thin line of 'FD12', 'FD21', 'FD32' and 'FD41' in Fig. 5.8 (c). In Step 6, 'potential' FDs 14 and 32 are classified as external to the faulty link due to the criterion of overvoltage suppression, as shown by 'V32n' and 'V41n' in Fig. 5.9 (c). As a consequence, Step 7 starts. Hence, 'potential' FDs 14 and 32 reclose ('FD14' and 'FD32' in Fig. 5.8 (c)).

The reclosing of a dc disconnector (Steps 5a and 7a) leads to an ACCB reclosing order (Steps 5b and 7b), as shown in Fig. 5.8 (b). Firstly, the ACCBs 2 and 4 are reclosed, as these are associated with converters operating in the rectifier mode. Shortly after with voltage restoration, ACCBs 1 and 3 reclose which are associated with converters operating in the

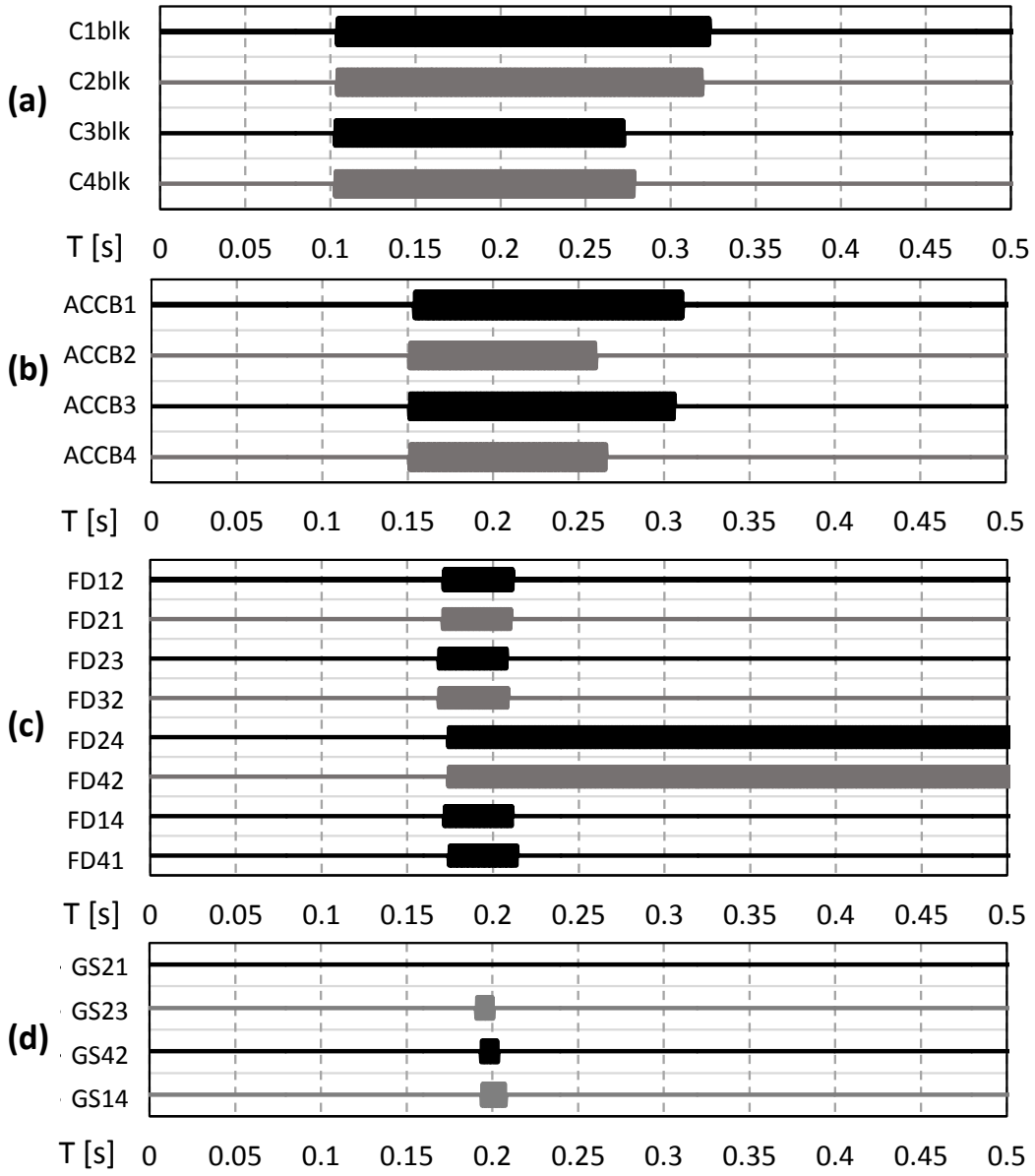

Fig. 5.8 State of (a) the converters, (b) ACCBs, (c) FDs and (d) grounding switches for the P2Gnd fault case.

inverter mode. These actions are followed by dc grid re-energization as observed at ≈0.25 s by 'V32p' and 'V32n' in Figs. 5.9 (b) and 5.9 (c). The next action comprises the converter de-blocking (Steps 5c and 7c) at ≈0.27 s and ≈0.32 s (see Fig. 5.8 (a)).

At this instant (≈0.32 s), the PPS is terminated at all busbar units. The dc voltage on faulty link 24 does not recover or exhibit a quick overvoltage suppression. As a consequence,

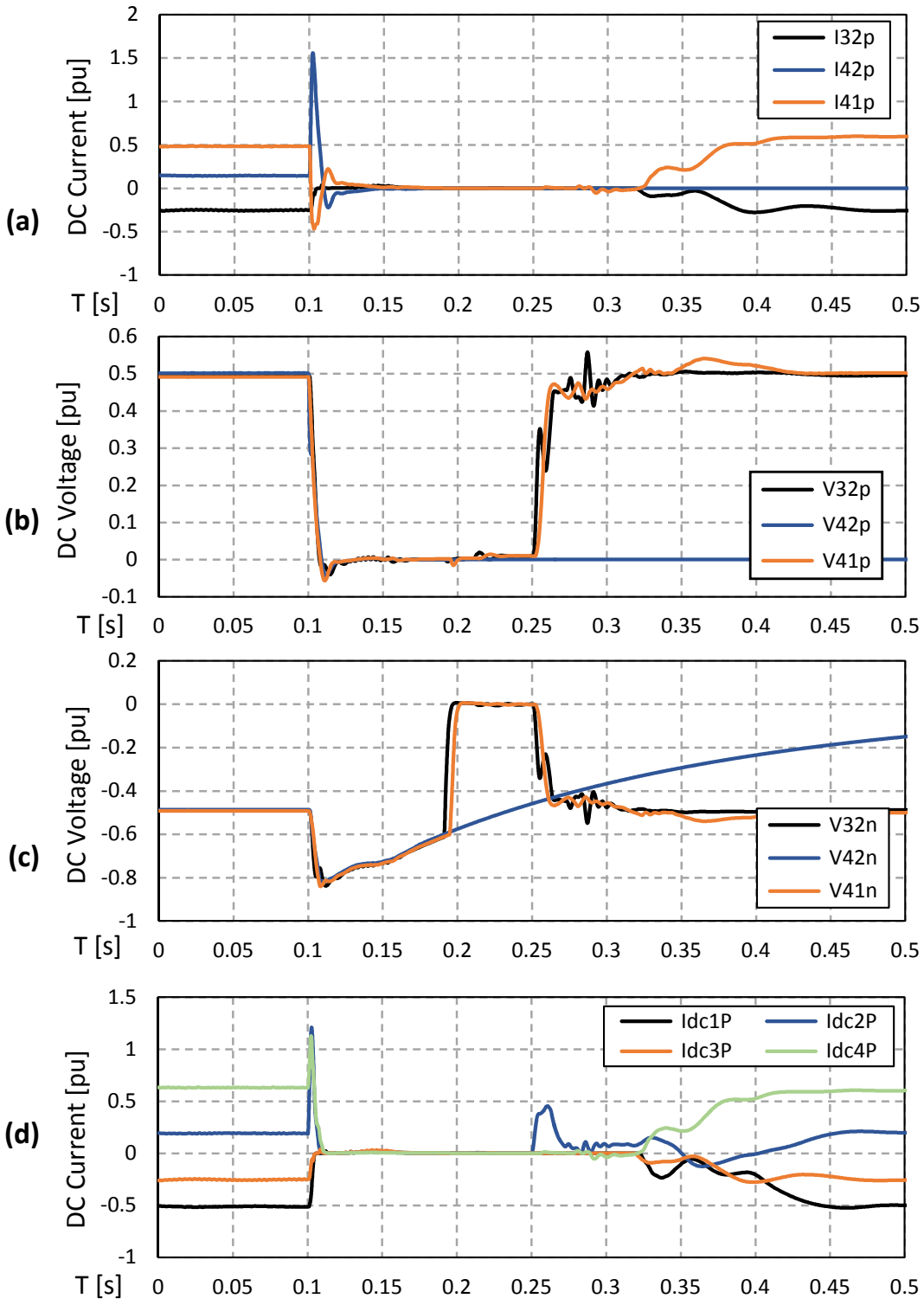

Fig. 5.9 (a) DC link currents, (b) dc voltage on positive pole, (c) dc voltage on negative pole and (d) dc converter current for the P2Gnd fault case.

'potential' FDs 24 and 42 are classified as internal to faulty link 24. Other FDs reclose due to the discrimination criteria achieved in Steps 2b and 6 (shown in Fig. 5.4).

For P2Gnd faults, the recovery of the MTDC network occurs within 300 ms after the start of the fault. The clearance process for these faults is faster than for P2P faults mainly due to two reasons. Firstly, during the voltage shift transient period in symmetrical monopole networks, the dc fault current experiences an oscillation that may not lead to an overcurrent [99]. Secondly, the high grounding impedance at the ac converter side constitutes a part of the fault discharge path and, therefore, increases the current decay rate in comparison to P2P faults [26, 29].

It should be highlighted that due to the slow operation of ACCBs, both P2Gnd and P2P faults require a considerable time to be cleared. This leads the converter current to increase for a few tens of milliseconds. This may not be acceptable in practical applications and, as a result, a compromise must be made between limiting the magnitude of the ac current infeed to reduce the converter rating and the design of converters to withstand high currents. Design considerations that reduce potential high currents include increasing the rating of arm inductors, which reduces the rate of change and the magnitude of current at the interruption instant [102]. To protect the converter's diodes, a protective bypass switch and/or a thyristor is additionally fired during the fault, allowing most of the current to flow through the bypass device and not through the diodes [58]. The short-circuit ratio (SCR) also plays a role on the ac current infeed during a dc fault. A reduced SCR leads to a smaller ac current infeed through the converter's arms [26]. Thus, with a proper design, converters are able to withstand high currents due to a dc fault.

5.4 Discussions

This section discusses back-up protection with the PPS approach and a critical comparison between the PPS and a method found on the literature [24] that also considers ACCBs as dc fault clearance devices.

5.4.1 Back-up Protection

Protection schemes must guarantee safety even in the case of failure of protection devices. Hence, misoperation of a FD is tested with the PPS. The misoperation term means that a FD is ordered to open but fails to execute the opening action.

The opening operation of all the FDs without discrimination guarantees fault isolation even in the case of FD failure. The PPS has an interlock signal that inhibits 'non-potential' FDs to be reclosed if the 'potential' FD does not open. If a 'potential' FD in the faulty dc link fails, the protection of the grid upstream is assured by the opening operation of the FD in the other link end (also a 'potential' FD). In the link end of the FD in failure, the fault is isolated from the network downstream by the 'non-potential' FDs associated with the same busbar station.

Fig. 5.10 illustrates a misoperation case of a FD. In this case, 'FD1' is assumed as 'potential'. However, it fails to open and FDs 'FD2' and 'FD3' must provide backup protection. With the PPS, the 'FD2' and 'FD3' open and remain in open mode until the opening of the potential 'FD1'. As 'FD1' remains in the closed mode, the back-up FDs do not re-close and isolate the fault from the grid downstream.

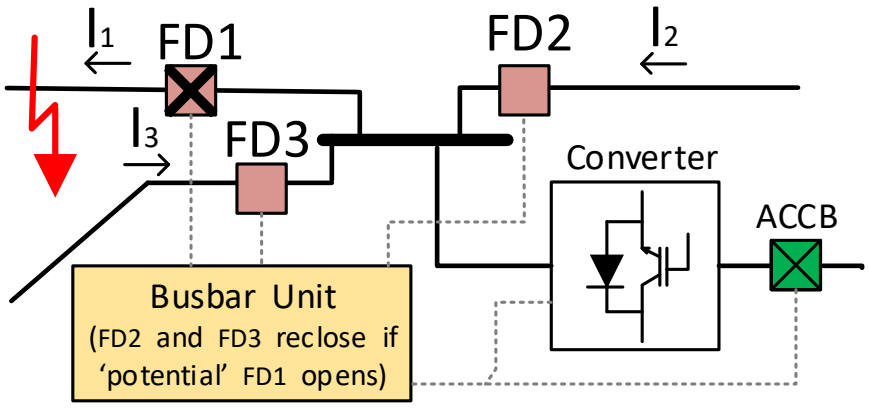

Fig. 5.10 Isolation failure and back-up interlock signal in a busbar station.

The P2P fault case (given in Section 5.3.1) is repeated while FD 12 is ordered to remain in the closed mode, simulating a misoperation. In this case, back-up protection shall be ensured by the opening of FD 14. Fig 5.11 shows the results for this fault case where FD 12 ('FD12') remains in closed mode (thin line) and FD 14 'FD14' is kept in open mode with the

PPS. Hence, the fault is isolated and only the links 12 and 14 are out of operation. The links 23 and 42 have all the FDs re-closed, leading to partial grid restoration.

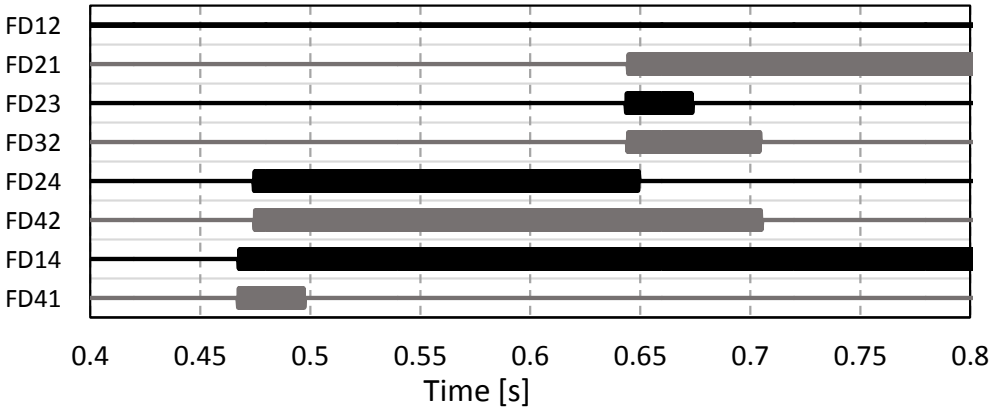

Fig. 5.11 State of FDs considering failure of dc FD 12 (P2P fault case of Section 5.3.1).

The ACCB and converter of the busbar station associated with the FD in failure remain isolated from the network as not all the FDs open. Hence, the PPS ensures backup protection in case of FD failure.

5.4.2 Comparison of Performance of the PPS Against the "Handshaking" Method

The "handshaking" method has been introduced in [24] [72]. In this method, the opening operation occurs in a limited number of FDs. Then, the network restoration occurs with a waiting time after the opening of a disconnector. This time is due to the operation of ACCBs where a delay was assumed as 100 ms (in [24] [72]). This means that the fault must be isolated within 100 ms after opening the first dc FD in the network. If the fault isolation is not ensured, the grid re-energisation might re-initiate the dc fault. This restoration failure event is likely to happen if an FD opens more than 100 ms later than another FD.

Fig. 5.12 shows the dc current and state of FDs with the handshaking method upon a P2P fault on link 12 at 20 km from relay 12. It should be noticed that grid restoration is not simulated. The "handshaking" method would require the opening of 'potential' FDs that, in this fault case, are FDs 12, 21, 32 and 41 (in open state in Fig. 5.12 (b)). Then, ACCB 2 would re-close 100 ms after the opening of 'FD21' which is at ≈ 0.85 s. However, such an operation would re-initiate ac infeed current to the dc side fault. As the current increases, the

FDs opening operation would fail. Hence, a time delay larger than 100 ms, for re-closing ACCB 2 in this case, would be necessary to ensure dc fault isolation.

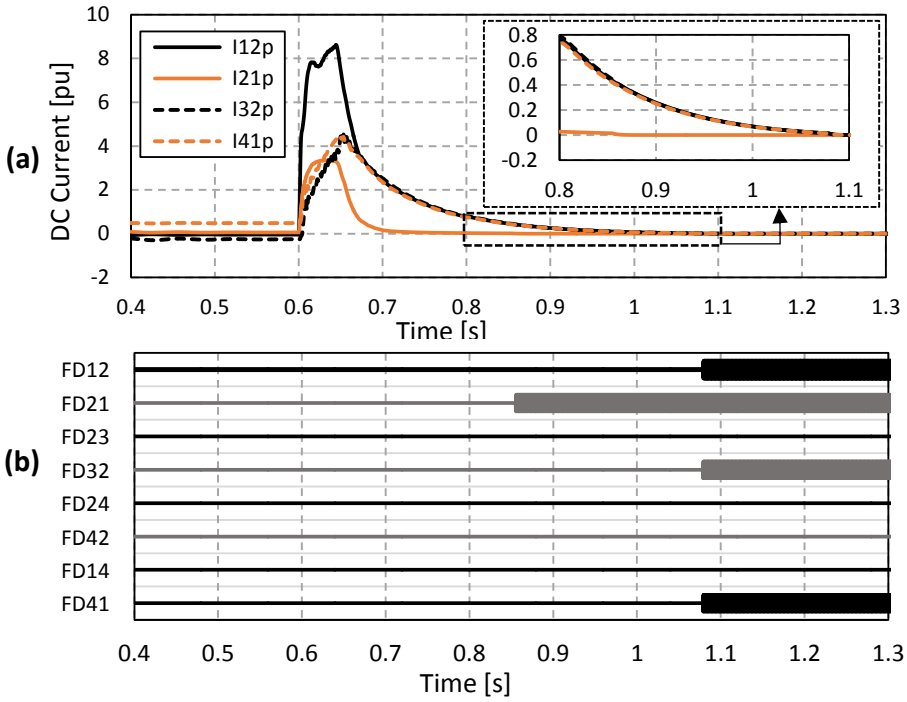

Fig. 5.12 (a) DC link current and (b) FD opening state with the "handshaking" based strategy without ACCB reclosing.

In the PPS approach, the re-closing of ACCB 2 would occur only after the opening of all FDs associated to the busbar station 2, and after the re-closing of one of these disconnectors. For this reason, the grid restoration would not compromise the fault isolation process.

It should be highlighted that while the "handshaking" method was not conceived to deal with the failure of isolation devices, the PPS includes back-up protection (see Section 5.4.1). This capability ensures a higher reliability of the PPS in comparison to the "handshaking" method.

5.5 Summary

When ACCBs are used to clear dc side faults, P2P and P2Gnd faults lead to a temporary outage of the whole dc network. A novel protection strategy has been proposed to reduce the grid outage time through the progressive restoration of the dc grid.

The proposed strategy is able to detect a dc fault, discriminate the faulty link and restore non-faulty links in a progressive manner. Each FD is ordered to reclose in a step-by-step basis. The opening and reclosing operation of ACCBs and FDs is controlled in a busbar unit while link communication is not required. Hence, such unit could be easily adapted to different dc grid configurations, making the PPS a robust and flexible strategy.

Benefits of the PPS include fault clearance with economic ACCBs, avoidance of dc link communication channels, a limited time of power outage in the dc network and a guaranteed back-up protection. Grid restoration is faster in comparison to the "handshaking" method as it does not rely on the faulty link isolation time. The PPS has the ability to restore non-faulty dc links even if the faulty link is not completely isolated from the network. This reduces grid outage time.

Simulation results have illustrated the application of the PPS for two types of faults. For a P2Gnd fault, the dc network can be restored within 300 ms. In the case of a P2P fault, the grid outage ranges from hundreds of milliseconds to seconds as this depends on the dc fault current decay behaviour.

Chapter 6

Proposed Protection Strategy for MTDC Grids equipped with FB Converters

6.1 Introduction

The design of MMC submodules is essentially restricted to HB or FB configurations [103]. HB submodules employ a design with 2 IGBTs, which incur of lower power losses in comparison to FB submodules (4 IGBTs). As a result, MMCs built entirely with HB submodules are more attractive in terms of investment and operational costs. However, the main drawback of HB based converters is the fault current that flows uncontrollably through the free-wheel diodes following a dc fault. Therefore, grids equipped with HB converters must rely on ACCBs or DCCBs to achieve dc fault current clearance.

Converters with FB submodules are able to quickly interrupt the converter fault current contributions [19, 73]. In this case, ACCBs or DCCBs are not required as fault clearance is ensured by the converters. Other advantages of the FB converter include dc voltage controllability and flexibility; *i.e.* possibility of a smooth voltage ramp up, voltage level reduction to mitigate atmospheric conditions, and voltage polarity reversal for fast de-ionisation of the arc [104].

To the knowledge of the author, only one protection strategy for MTDC grids using FB converters has been reported in the open literature [29]. In spite of its potential, dc protection with FB converters constitutes an under-researched topic due to higher investment

and operation cost (in comparison to HB converter) and due to the expected DCCBs, devices that would selectively isolate a dc faulty link. However, FB converters might have advantages that should be carefully analysed. To bridge this research gap, this chapter proposes a protection strategy for MTDC grids equipped with FB converters and link end FDs.

6.2 DC Fault Current Clearance Using FB Converter

DC fault current clearance can be quickly achieved by blocking the FB converters in a dc network. The blocking order consists of the removal of firing pulses to the electronic switches of an MMC (typically are IGBT devices). There are two criteria that trigger the converter blocking order. Firstly, converters are typically protected against overcurrent [5]. In such case, a blocking order is generated with a processing delay assumed as 0.1 ms. Secondly, in the case of fault detection at a dc relay at the neighbourhood of a converter station, a blocking order is generated with a processing delay assumed as 2 ms. These criteria and delays have two main advantages:

1. Ensure converters' safety as fault current flowing through their arms is limited to 1.2 p.u.;
2. Provide up to 2 ms fault related data to discrimination algorithms. It should be notice that converter blocking distorts greatly the current and voltage behaviour. Hence, the fault discrimination algorithms (discussed in Sections 4.3.1 and 4.3.2) should analyse data only until the converter blocking instant.

The dc current clearance principle due to a FB converter blocking action is based on the arm voltage, which opposes the fault current flow [103]. At the pre-blocking event, the dc fault current flows from ac side to dc side towards the fault location. With FB converter blocking, the polarity of arm voltage reverses and opposes to the dc link voltages. As a result, the voltage opposes the current flow, forcing the current to be zero.

Fig. 6.1 illustrates the current path of an FB submodule during converter blocking. It should be noticed that firstly, the current flows through the diodes as the IGBTs are blocked. Secondly, the current flows from the positive to the negative plate of the capacitor (the capacitor is charging). Lastly, considering that the dc side is associated with the positive

pole of a link, the arm voltage delivers a negative voltage. In addition, the voltage sum of all capacitors in an arm is larger in magnitude than the dc side link voltage. Once all FB converters in a network block, all current contributions to the dc fault location are interrupted and faulty link isolation can be achieved.

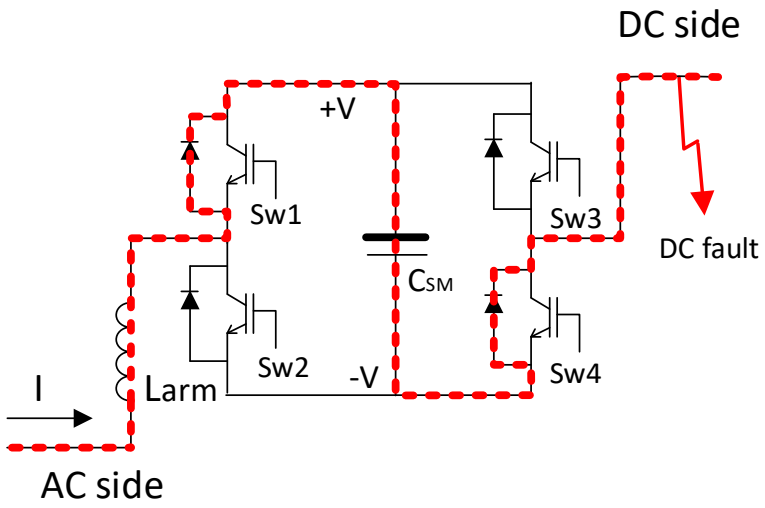

Fig. 6.1 FB submodule with current path during blocking mode.

Following the FB converter blocking order, the current decays to zero while the fault energy is stored in the submodule's capacitors. The dc fault energy E_{dc} absorbed by the arm submodules is defined as:

$$E_{dc} = \frac{1}{2} L_{eq} (I_{pk})^2 \tag{6.1}$$

where the equivalent inductance L_{eq} and the approximate dc current peak at the blocking instant I_{pk} are defined as:

$$L_{eq} = L_{dc} + \frac{2}{3} L_{arm} \tag{6.2}$$

$$I_{pk} = I_0 + \frac{V_{dc} T_{blk}}{L_{eq}} \tag{6.3}$$

where L_{arm} is the converter arm inductance, L_{dc} the equivalent link inductance, I_0 the pre-fault dc current, V_{dc} the P2P dc voltage, and T_{blk} the time from the arrival of a transient fault current until the converter blocking instant.

The FB blocking mode generates a dc voltage equal to $-V_{dc}$. Hence, the approximate time T_{fall0} for the dc current to decay to zero is given by:

$$T_{fall0} = \frac{1}{2} I_{pk} \frac{L_{eq}}{V_{dc}} \tag{6.4}$$

The decay time to zero T_{fall0} depends on T_{blk} and L_{eq}. Hence, having a low value for T_{blk} and L_{eq} results in a faster current interruption time and in a lower energy absorption by the FB submodules' capacitors. T_{blk} should be limited with a fast fault detection time. L_{eq} should be limited by using low rating link end current rate limiting inductors. The rating of these devices is associated with current derivative discrimination methods, fault detection and discrimination delays, and current clearance delay given by devices such as DCCBs [63]. For grids with FB converters, the minimum expected delay until blocking is assumed as 0.1 ms which is quicker than the showcased fast DCCB prototypes [18, 105]. As a result, current rate limiting inductors in grids with FB converters can be of a low rating (or even non-existent) in comparison to grids equipped with DCCBs. As a drawback, fault discrimination algorithms based on the current or voltage derivatives (as given in Section 2.3.2) may not be applicable for grids equipped with low rating current rate limiting inductors.

Fig. 6.2 illustrates a dc current behaviour at the output of an FB converter during a dc fault scenario (current at converter C2 at fault in Section 6.5.1). The dc current starts to increase after 20 ms while converter blocking is achieved before 22 ms. The dc current decays quickly to zero due to the blocking action. For clarification, the negative current profile (between 22 ms and $\approx$ 22.5 ms in Fig 6.2) is not an expected behaviour. This event requires further investigation.

In recent open literatures, a few FB control approaches are proposed to clear dc fault currents [106, 107]. In these approaches, instead of blocking an FB converter upon fault detection, the converter could be switched to a "fault control mode". This "fault control mode" would control dc fault current, dc voltage and/or active/reactive power in order to meet potential requirements. For example, in a dc grid composed of cables, a FB converter could operate with a dc current and dc voltage control. In this case, the dc voltage should be reduced smoothly to zero to avoid potential polarity reversals which could affect the cable insulation layers [104]. Another example includes FB converters near a weak ac system.

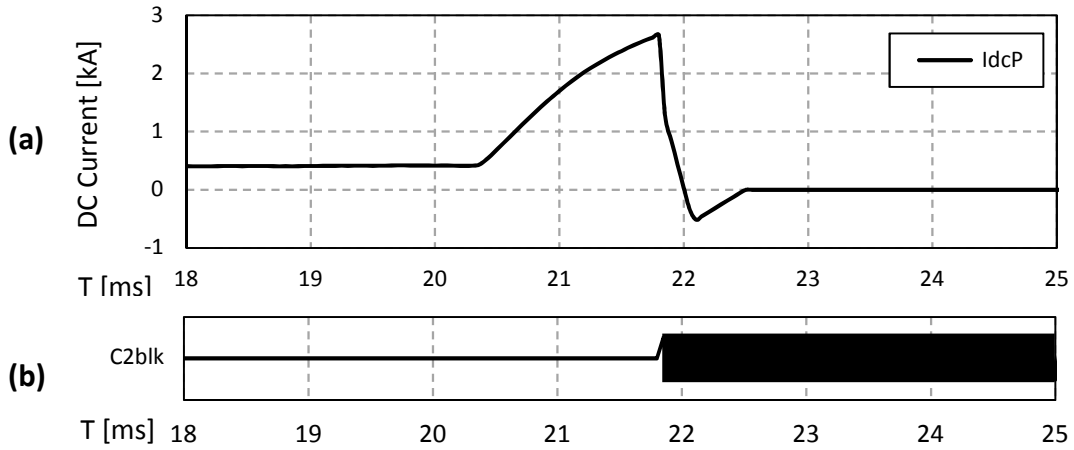

Fig. 6.2 Selection C2 blocking.

In this case, during the "fault control mode", the converter could support the ac voltage by injecting reactive power while reducing the dc side fault current [106].

The FB control approaches in the cited references lead to dc fault clearance in a period of time of a few milliseconds more than the converter blocking action (*i.e.* removing the firing pulses of IGBTs). In this thesis, due to simplicity and to focus on protection, the dc fault clearance is achieved by blocking FB converters. The performance of dc protection strategy should remain identical independently of the FB control principle during a dc fault.

6.3 Overvoltage and Voltage Imbalance Suppression

A P2Gnd fault in a symmetrical monopole dc network causes a shift of the network voltage. This means that the faulty pole voltage moves towards zero while the non-faulty pole voltage moves towards twice the nominal value. In practical applications, surge arresters are used to limit the overvoltage level to typically less than 1.9 p.u.

With converter blocking, the grid voltage is no longer controlled. Then, the overvoltage decays naturally to zero in a process that can last hundreds of milliseconds to hours. This depends on the shunt conductance of the dc link which is particularly residual with cross-linked polyethylene (XLPE) cables [108]. Therefore, in grids composed of XLPE cables, the natural overvoltage decay may last a few hours.

Overvoltage is harmful to dc links as it causes stress on insulation layers. If the overvoltage is repetitive or for long periods of time, it may reduce the expected lifetime of a cable.

Therefore, overvoltage events must be suppressed in a timely and cost-effective manner. In this chapter, an alternative overvoltage suppression method is proposed. This method eliminates the need for additional devices such as dc discharging circuits (as proposed in Section 5.2.3 for a grid with HB converters). Instead, this method takes advantage of the FB converter's capability to suppress overvoltage events.

The overvoltage suppression principle is based on a temporary short circuit between the positive and negative pole prior to fault isolation actions. This consists of by-passing all the converter submodules in one upper and one lower arm which is achieved by re-closing two IGBTs in series in the FB submodules. Considering the submodule block in PSCAD/EMTDC simulations (see Fig. 6.3) IGBTs 2 and 4 are chosen to be by-passed during the overvoltage suppression period.

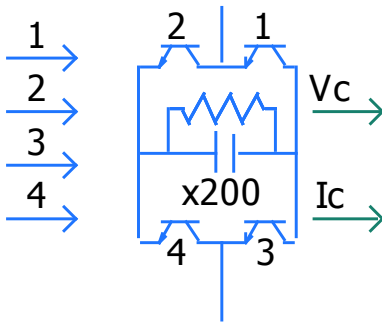

Fig. 6.3 View of FB submodule representation from the converter model in PSCAD/EMTDC.

During the overvoltage suppression period, the positive and negative P2Gnd voltages become equal. Then, these voltages decay to zero together due to the ground reference provided by the fault location. The direct connection of two points with different voltages might cause an inrush current peak. Hence, the arm current is limited during the process and a maximum magnitude can be set as 2 kA in this case (equal to nominal current). This limit is set by a criterion that re-opens the arm IGBTs for 1 ms if dc current raises over 2 kA. The threshold value depends on the dc peak forward current of the adopted IGBTs. For instance, considering an IGBT nominal ampacity of 2 kA, a peak collector current of 4 kA is allowed for periods up to 1 ms [109]. Therefore, a 2 kA threshold ensures a safe operation of IGBT devices.

Fig. 6.4 illustrates the FB converter configuration and an busbar with two dc links. The FB submodule configuration is zoomed in where IGBTs 2 and 4 ('sw2' and 'sw4') remain switched on during the overvoltage suppression action.

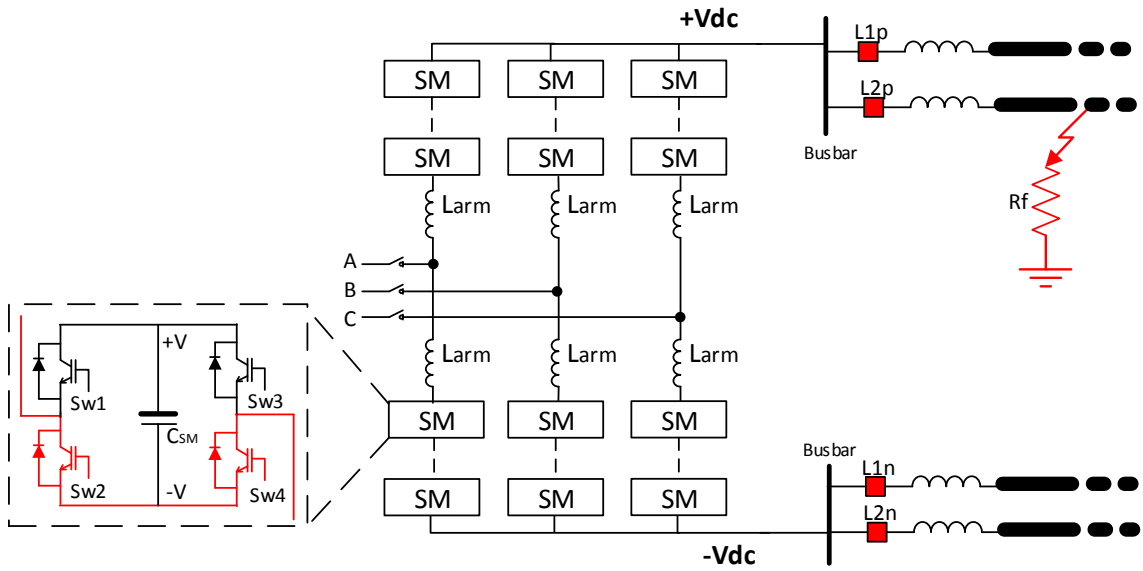

Fig. 6.4 FB converter configuration with submodule operation during the overvoltage suppression operation (IGBTs 2 and 4 in closed mode).

This method should be applied before fault isolation and before the network energisation. Therefore, the whole network remains with an identical voltage level while the P2Gnd fault works as a voltage reference. As a result, a symmetrical low voltage is quickly achieved in the whole network for both the positive and the negative poles.

The control of submodule' IGBTs for the overvoltage suppression action is based on the following criteria:

1. Detection of a P2Gnd fault

   A P2Gnd fault is detected by analysing the voltage profile in the positive and negative poles. Then, at the blocking instant, if a voltage higher the 0.55 p.u. is experienced in one and only one pole, a P2Gnd fault is discriminated. This criterion can be expressed as:

   $$\text{If } V_p > 0.55 \text{ p.u. or } V_n < -0.55 \text{ p.u.,}$$

   Then start of overvoltage suppression action.

2. Overcurrent limit

   If the arm current raises to a value assumed as 2 kA, the IGBTs receive an open order with a duration of 1 ms. The healthy pole discharge is resumed after this. An additional threshold transgression leads to further 1 ms in open mode. The process is repeated until the residual dc voltage operation is achieved. Mathematically the criterion becomes:

   $$\text{If } I_p > 2 \text{ kA or } I_n > 2 \text{ kA},$$
   $$\text{Then suspend the overvoltage suppression action (for 1 ms).}$$

3. Symmetrical and residual dc voltage detection

   The operation terminates once a residual voltage is achieved in the positive and negative poles. If the dc voltages are below a threshold for a 2 ms time period, the operation stops. This criterion can be expressed as:

   $$\text{If } V_p > 0.025 \text{ p.u. and } |V_n| < 0.025 \text{ p.u. for 2 ms},$$
   $$\text{Then end of overvoltage suppression action.}$$

Fig. 6.5 illustrates the behaviour of the dc voltage and the current at phase A of converter C2 in the case of a positive-P2Gnd fault (fault case in Section 6.5.2). The state of IGBTs in an FB submodule (submodule 100 of 200, upper arm of phase A, randomly chosen) is also illustrated (Fig. 6.5(c)).

The fault starts at 20 ms as observed in Fig. 6.5. The dc voltage experiences an undervoltage on the positive pole V_p and an overvoltage on the negative pole V_n. The converter is blocked for approximately 22 ms which is when signals T1_u -T4_u become zero (Fig. 6.5 (c)). At approximately 27 ms, the overvoltage suppression operation starts. The arm current (Fig. 6.5 (b)) increases quickly to 2 kA, which leads to a suspension of the overvoltage suppression algorithm for a one millisecond. It should be noticed that with the increase of arm current (I_{armT} and I_{armB}) the series IGBTs are switched off for a 1 ms period ($T2_u$ and $T4_u$ (see Fig. 6.5 (c))). The overvoltage is suppressed and the voltage arrives in steady-state near zero value at approximately 37 ms. At this instant, the overvoltage suppression action terminates.

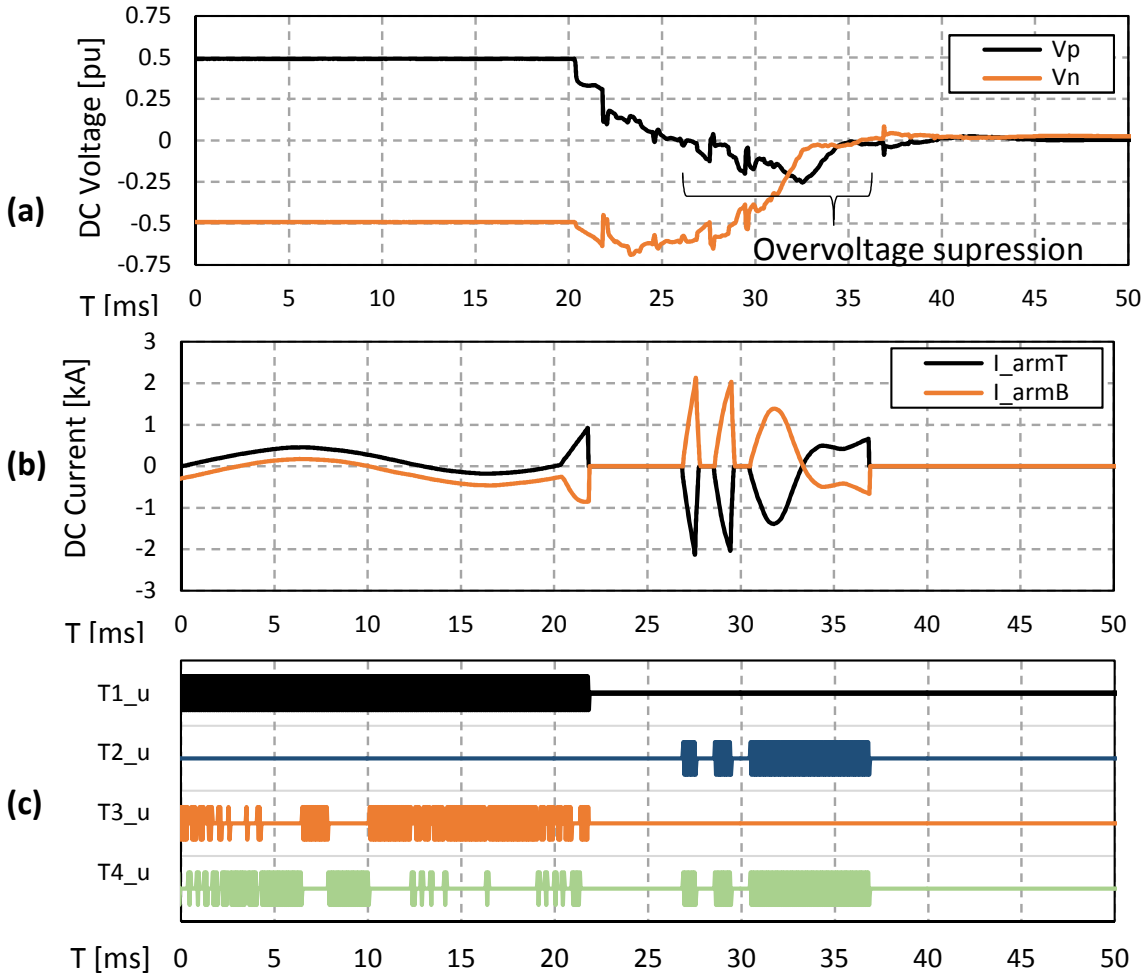

Fig. 6.5 Application of the overvoltage and voltage imbalance suppression method during a P2Gnd fault The (a) positive and negative voltage, (b) arm currents and (c) the firing pulses on the IGBTs in a FB submodule.

6.4 Protection Strategy Description

A protection strategy is designed for MTDC grids equipped with converters with FB capability. Fault isolation is ensured by FDs placed at each link end. In this strategy, all converters at the MTDC grid must have current blocking capability. This is a necessary condition as dc current clearance occurs following ac current infeed interruption at all converter stations. In this way, all sources that could feed the dc fault current are blocked. The protection strategy is described in this section through a sequential number of steps.

6.4.1 DC Fault Detection

The protection strategy is initiated with dc fault detection. It includes overcurrent, undervoltage and current derivative methods, as given in Section 4.2. The first criterion to be met leads to fault detection in a dc relay. A dc fault is typically detected within 1 ms after the arrival of the first transient wave.

6.4.2 FB Converter Blocking

The blocking of a FB converter occurs due to three reasons. Firstly, it protects the submodule's IGBTs from overcurrent events. Secondly, it stops the submodule capacitive discharge to the dc side fault. Lastly, it blocks the converter fault current. The FB converter blocking order is triggered by two criteria if:

1. In a converter station, an overcurrent is detected in the positive or negative pole. The overcurrent threshold is 2.4 kA while the nominal dc current is 2 kA. The blocking order has a delay of 0.1 ms.
2. In a dc relay, a dc fault is detected by overcurrent or undervoltage means. In this case, the blocking order arrives with a 2 ms delay due to processing requirements in the busbar station.

After receiving a blocking order, the firing pulses of converters stop. This leads to a suppression of arm currents within a few milliseconds. This time period (T_{fall0} in Eq. 6.4) is approximately 2 ms in the dc grid model of this thesis.

6.4.3 Discrimination of FDs

Immediately after dc fault detection, the discrimination algorithm starts. This algorithm analyses local data acquired at a dc relay. Then the algorithm classifies an FD, associated with the dc relay nearby, as internal or external to the faulty link.

Fault discrimination methods are detailed in Section 4.3. The FD classification algorithm is composed of two criteria. The first criterion comprises the sign of current derivative algorithm (given in Section 4.3.2). This methodology is able to discriminate at least half of the FDs at non-faulty links. The second criterion comprises the CCRC algorithm (given

in Section 4.3.1). This criterion aim to discriminate faults taking into account the sign and potential variations of the current change rate within a short time period. This period is typically less than 2 ms as it comprises the time between the dc fault detection until the converter blocking instant. Therefore at the converter blocking instant, the discrimination algorithm classifies an FD as internal or external to a faulty dc link.

6.4.4 Overvoltage Suppression

A voltage shift and overvoltage appears in the case of a P2Gnd fault in a symmetrical monopole dc network. The overvoltage must be quickly suppressed in order to prevent harmful conditions to dc equipment. Section 6.3 describes a method to suppress overvoltage and voltage imbalance in dc grids equipped with FB converters.

The method ensures a fast overvoltage decay rate, a low and symmetrical voltage level and no harmful converter arms currents. The duration of the process is typically 10 ms.

6.4.5 Fault Isolation

Fault isolation is ensured by the opening of the FDs placed at the faulty link ends. FDs have an operation delay of 10 ms and open once the dc current decays below the residual current breaking capability (assumed previously as 30 A).

The protection strategy has a minimum opening approach. This means that only the FDs in the faulty link should open. The opening of FDs following a dc fault is dictated by the discrimination algorithm. If an FD is discriminated as internal, the dc link is discriminated as faulty and the FD opens. If the dc link is classified as non-faulty, the FD remains closed.

6.4.6 Grid Restoration

After fault clearance and fault isolation, dc grid restoration is initiated by the de-blocking of FB converters. The converters operating as rectifiers at the pre-fault instants restore the dc voltage. Shortly after, the converters operating as inverters at the pre-fault instants restore the dc power flow. The de-blocking of a rectifier occurs if any of the following conditions are met:

1. Discriminated FD opening operation:
   If the FDs discriminated as internal to the faulty link are open, the fault is isolated. Therefore, the converters are able to de-block and resume operation. The de-blocking order has a practical time delay of 5 ms. This period is considered due to likely opening delay between the discriminated FDs at both ends of the faulty link.

2. Voltage recovery:
   The recovery of link dc voltage at a busbar indicates the grid restoration has started by converters connected to a remote busbar. Therefore, a converter shall be de-blocked if local dc voltage recovers approximately to nominal values. The voltage thresholds given in Section 4.3.3 are considered in this criterion.

3. Maximum time in blocking mode:
   Converters are de-blocked after a maximum time in blocking mode if there are no locally discriminated FD. This maximum time is set as 200 ms which is sufficient to guarantee fault isolation (as it typically occurs in less than 150 ms).

The de-blocking of a converter in inverter mode occurs once the voltage recovery criterion is met. In this way, the power exchange between ac and dc grids keeps the same direction at both the pre-fault and the grid recovery periods. Succinctly, an ac grid exporting power at the pre-fault instant will export power during grid recovery by means of a converter in rectifier operation. Conversely, an ac grid importing power at the pre-fault instant will import power during grid recovery by means of a converter in inverter operation.

In a few cases, an FD might open in a non-faulty dc link. Therefore, grid restoration would be terminated by re-closure of such FDs. The re-closing criterion is based on the voltage recovery algorithm as given in Section 4.3.3.

At the end of the protection strategy, only the FDs placed on the faulty link are in the open state. The FB converters are de-blocked and their control operation is resumed.

6.5 Simulation Results

The 4-terminal dc grid introduced in Section 3.2 is considered for fault simulations in this chapter. The grid includes 4 FB converters for fault current clearance and an FD at each link end for fault isolation.

Two fault scenarios are described in detail in this section, including a P2P and a P2Gnd fault. Fig. 6.6 illustrates the location of the dc faults in the dc network. A P2P fault occurs at 20 ms at link 12, 20 km from relay 12 and 180 km from relay 21, and has an impedance of 0.1 Ω. A P2Gnd fault occurs at 20 ms at the middle of link 24 (*i.e.* 75 km from relay 24 and relay 42) and has an resistance of 10 Ω.

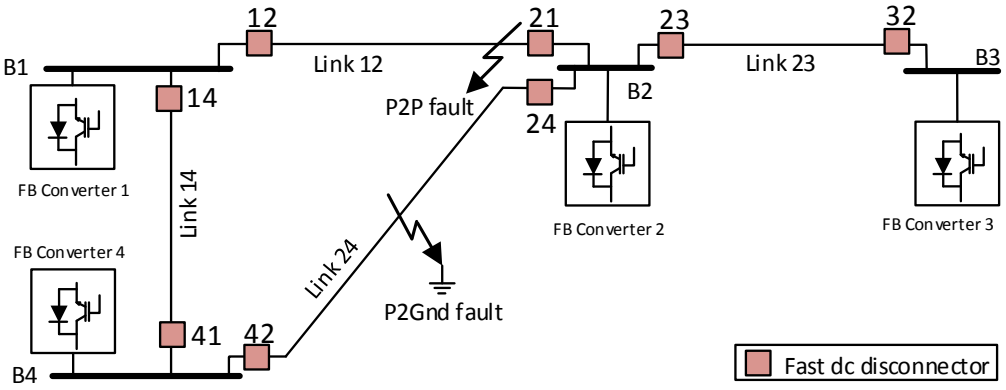

Fig. 6.6 MTDC grid case study with FB converters. The location of the fault scenarios is shown.

6.5.1 Pole-to-Pole Fault

A P2P fault causes a quick voltage collapse over all the network. Due to the significant disturbance caused, dc fault detection is achieved in a few time samples after the arrival of the transient waves at each dc relay .

Converters block following fault detection at a dc relay or at the converter station. Fig. 6.7 illustrates the converter blocking state. As observed, all the converters block shortly after the start of the dc fault.

Fault discrimination algorithms are initiated following fault detection in a dc relay. These algorithms analyse local dc current in order to classify their associated FD as internal or

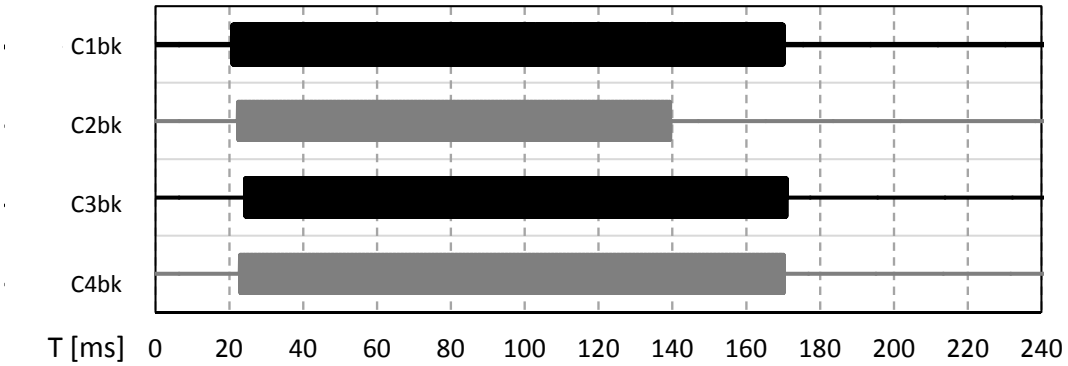

Fig. 6.7 Converter blocking P2P .

external to the faulty link. The CRCC and sign of current derivative algorithms (Section 4.3.1 and 4.3.2) are performed at this stage. DC relays 12, 21, 32, and 41 experience a positive rate of change following the arrival of transient waves. These are potentially internal to the faulty dc link, according to the sign of the current derivative algorithm. At this stage, partial discrimination is achieved. To achieve full discrimination, only the two relays in the faulty link should be discriminated as internal. The CRCC criterion gives that level of discrimination whose performance is described for an internal and for an external relay.

Fig. 6.8 illustrates the behaviour of the CRCC algorithm on dc relay 21 which is internal to the faulty link. Shortly after 20.5 ms, the transient waves arrive at dc relay 21. Fault detection is quickly achieved as marked by 'Fdet2' in Fig. 6.8 (c). At the same instant, the discrimination criterion of sign of current derivative classified this relay as potentially internal to the faulty link, 'Sdidt21' in Fig. 6.8 (c).

The second current derivative is illustrated in Fig. 6.8 (b). It should be noticed that the negative values are omitted for visual clarity. In Fig. 6.8 (b), attention shall be paid to the maximum of the curve. In relay 21, there are two maxima identified, 'MaxInc_{21}' and 'MaxRef_{21}'. The first maximum is associated with the incident transient wave while the second is associated with the first reflected wave. By comparing these values, the magnitude of the first maximum is higher than the magnitude of the second, as marked by 'CRCC_{21}' in Fig. 6.8 (c). The signal 'CRCC_{21}' remains true (thick line) during the fault discrimination period which starts with fault detection and ends with converter blocking 'C2blk'. Therefore with converter blocking, the decision to open or keep closed the local FD is given. For the

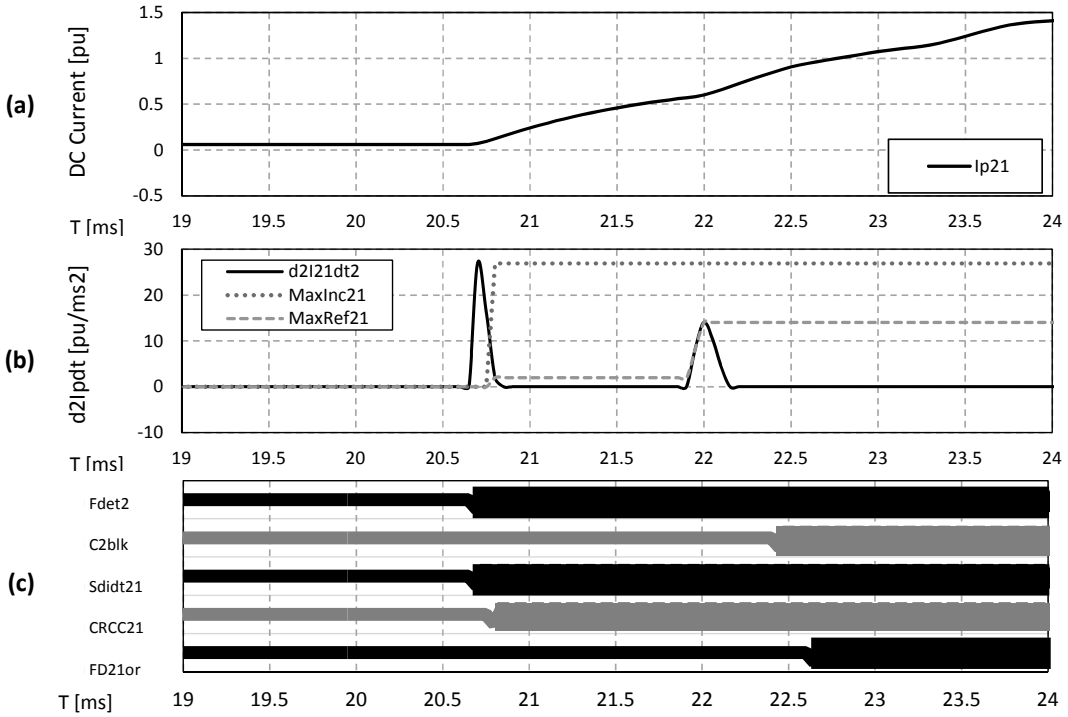

Fig. 6.8 Data analysed by the discrimination algorithms in the internal dc relay 21. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion and (c) protection signals.

internal relay 21, as '$CRCC_{21}$' is true, an order to open the FD 21 is given ('FD21or' in Fig. 6.8 (c)).

Fig. 6.9 illustrates the behaviour of the CRCC algorithm on dc relay 41 which is external to the faulty link. Shortly after 21 ms, the transient waves arrive at dc relay 41. Fault detection based on overcurrent or undervoltage is achieved after 22 ms (see 'Fdet4' in Fig. 6.9 (c)). However, the start of the discrimination algorithm at this instant (of $\approx$ 22 ms) would mean that previously observed transient currents would not be considered for online analysis. Such a fault detection delay could lead to misjudgement of the CRCC criterion as the incident wave appears before the fault detection flag 'Fdet4'. In order to avoid this problem, the discrimination algorithm is initiated with fault detection (overcurrent or undervoltage algorithm) or disturbance detection (current derivative algorithm). In this way, fault discrimination is initiated at $\approx$ 21.5 ms.

In dc relay 41, a dc current disturbance is detected a few time samples after the arrival of the transient waves due to the sensitive current derivative method. This event initiates

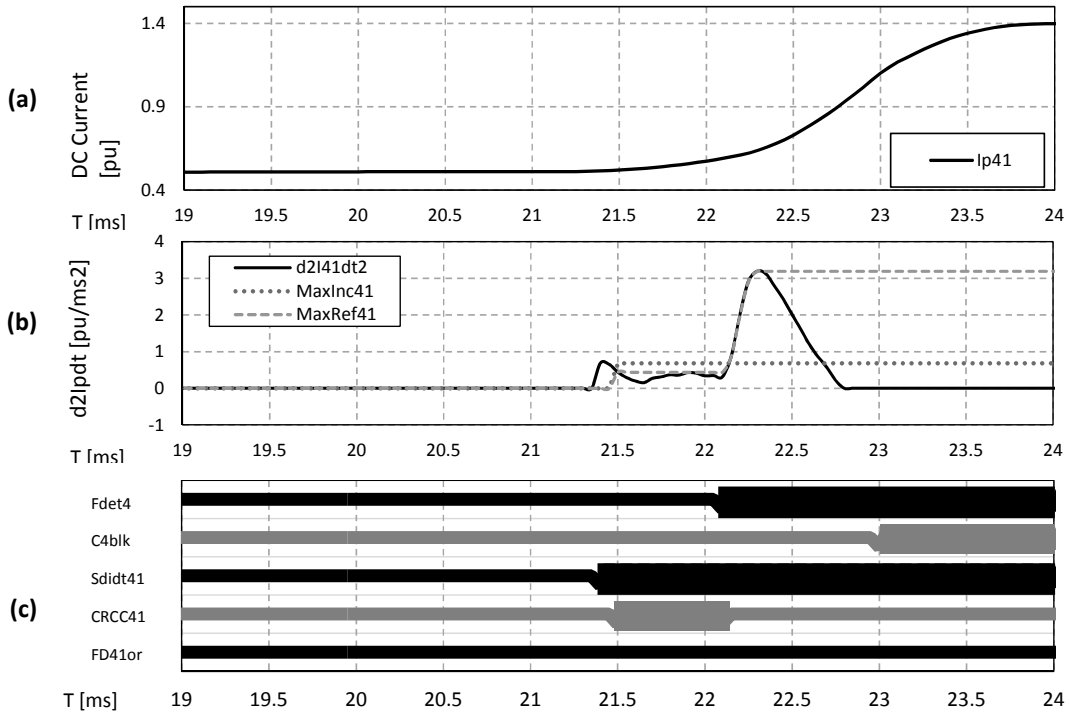

Fig. 6.9 Data analysed by the CRCC discrimination criterion in the external dc relay 41.

the discrimination algorithm. At the same instant, the discrimination criterion of the sign of current derivative classifies this relay as potentially internal to the faulty link (see signal 'Sdidt41' in Fig. 6.9 (c)).

The second current derivative is illustrated in Fig. 6.9 (b). In relay 41, there are two maxima identified, 'MaxInc$_{41}$' and 'MaxRef$_{41}$'. 'MaxInc$_{41}$' is associated with the incident transient wave while 'MaxRef$_{41}$' is associated to the local maximum of the reflected waves. By comparing these values at the converter blocking instant, the magnitude of the first maximum is smaller than the magnitude of the second. With converter blocking ('C4blk' at $\approx$ 23 ms), the decision to open or keep the local FD closed is given. Therefore, at this instant the fault is classified as external to link 14 (where relay 41 is placed). As a consequence, the FD 41 order remains closed (with zero value as shown by 'FD41or' in Fig. 6.9 (c)).

Fig. 6.10 illustrates the state of FDs during the application of the protection strategy. The thin line represents the closing mode while the thick line represents the opening mode. FDs placed at the faulty link include FD 12 and FD 21. With the proposed protection strategy, only the two FDs at the faulty link open.

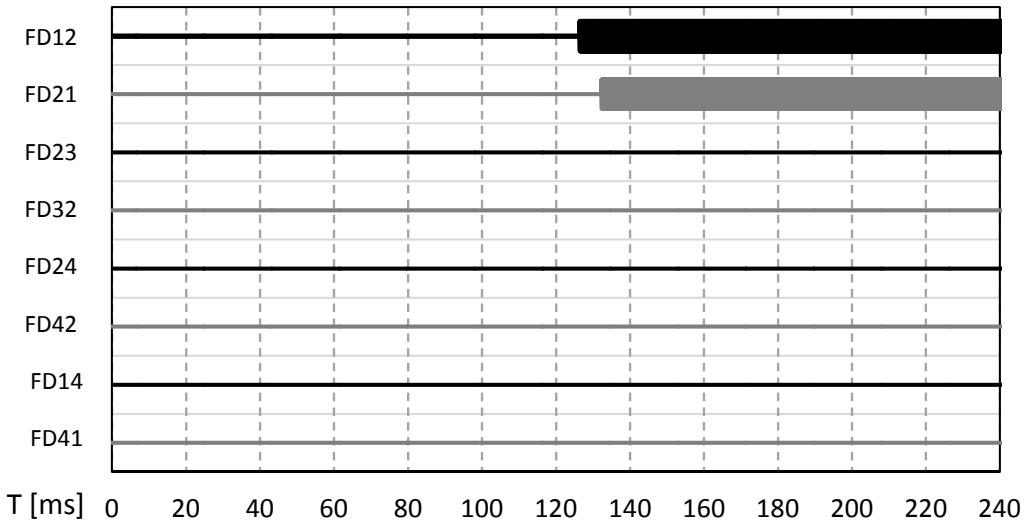

Fig. 6.10 State of FDs following the dc P2P fault.

Fig. 6.11 illustrates dc currents and voltages at the dc grid. The converter dc current is quickly interrupted with blocking actions. As shown previously in Fig. 6.7, converter C2 is the first to de-block. This converter restores smoothly the dc link voltage while current is kept within nominal values. The currents and voltages are not shown as they are identically symmetric to the positive pole values.

6.5.2 Pole-to-Ground Fault

A positive-P2Gnd fault occurs at 20 ms in link 24. This event causes a voltage shift in the monopole networks. Therefore, an overvoltage appears at the non-faulty pole which is suppressed with the methodology presented in Section 6.3.

Fault detection occurs quickly after the arrival of the transient waves. This event leads to blocking of FB converters as illustrated in Fig. 6.12.

The next step of the protection strategy comprises fault discrimination. Considering the discriminative algorithm based upon the sign of current derivative, each busbar unit classifies one FD as potentially internal to the faulty link. The potentially internal FDs are associated with an increasing behaviour of the current derivative at the fault detection instant. In this fault case, FDs 12, 24, 32 and 42 are discriminated as potentially internal to the faulty link. In order to reduce the number of discriminated FDs, the CRCC discrimination criterion is considered.

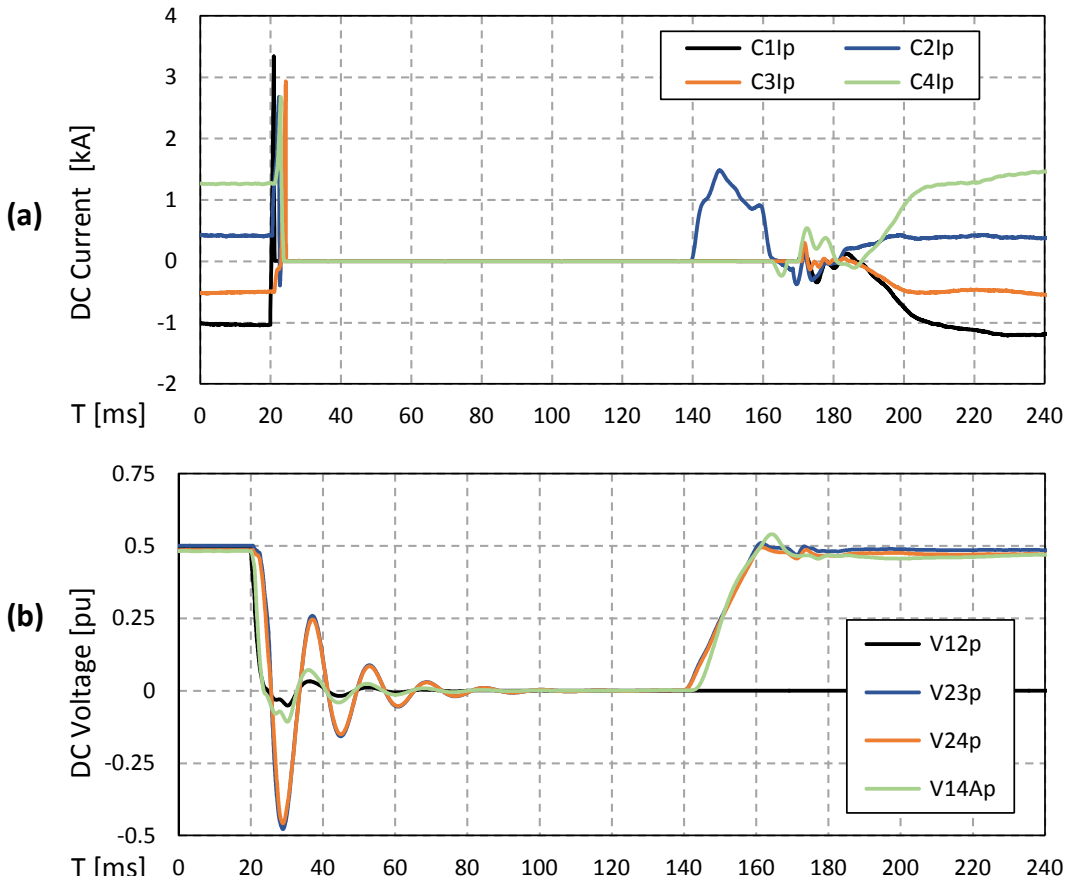

Fig. 6.11 DC currents and voltages at the network.

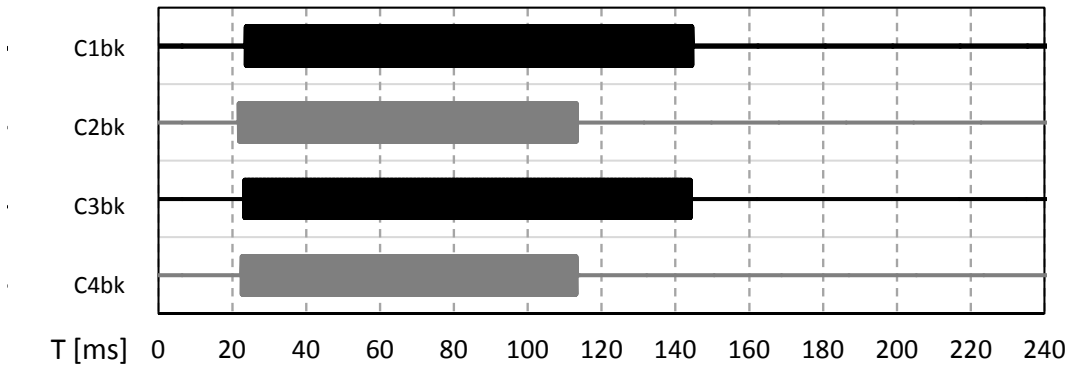

Fig. 6.12 Converter blocking with P2Gnd.

Fig. 6.13 illustrates protection related data of dc relay 24 which is internal to the faulty link. The dc current at relay 24 in Fig. 6.13 (a) has an increasing behaviour at fault detection ($\approx$ 20.5 ms) which meets the sign of current derivative criterion. This results in the flag of the signal 'Sdidt24' as shown in Fig. 6.13 (c).

Fig. 6.13 (b) shows the second order current derivative at relay 24, together with forward transient waves. At the start of the fault, a large rate of change of dc current is noticed due to the capacitive discharge of the faulty link which is a dc cable in this case. Afterwards, the dc fault current keeps increasing until converter blocking ('C2blk' in Fig. 6.13 (b)), but the rate of change diminishes. During the discrimination period, between fault detection and converter blocking, only one forward transient wave is detected which is related to the incident transient wave. The second maximum ('MaxRef_{24}'), is numerically coded to be identified immediately after the achievement of 'MaxInc_{24}'. For this reason, 'MaxRef_{24}' in Fig. 6.13 (b) does not correspond to the maximum local of reflected waves. Nonetheless, the decision making is not altered due to this performance.

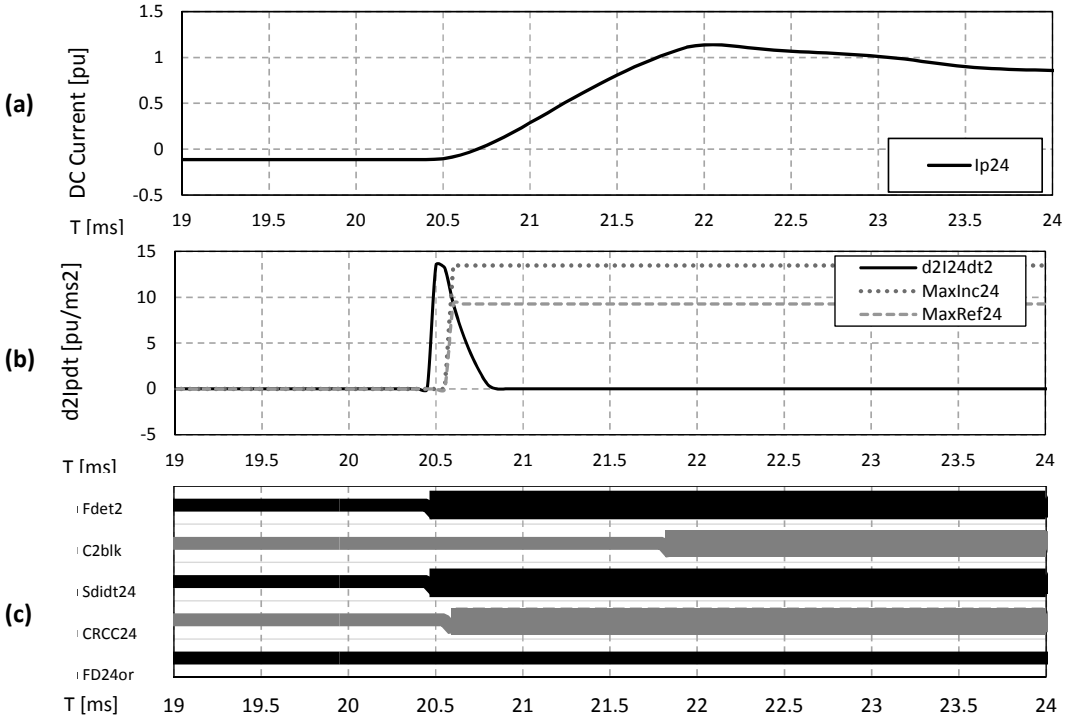

Fig. 6.13 Data analysed by the CRCC discrimination criterion in the internal dc relay 24.

By comparing the magnitudes 'MaxInc_{24}' and 'MaxRef_{24}' (in Fig. 6.13 (b)), the maximum of the incident wave is larger. This leads to discrimination of FD 24 as internal to the faulty link. Correspondingly, the discrimination signal 'CRCC_{24}' remains with value one (thick line). An opening order to the FD 24 is given. However, this order only occurs after overvoltage suppression actions. For this reason, 'FD24or' in Fig. 6.13 (c) remains with a zero value in the visualised period.

Fig. 6.14 illustrates protection related data of dc relay 32, which is external to the faulty link. The dc current at relay 32 (see Fig. 6.14 (a)) has an increasing behaviour at fault detection (after 21 ms), which meets the sign of current derivative criterion. This results in the flag of signal 'Sdidt32' (see Fig. 6.14 (c)).

Fig. 6.14 (b) shows the second order current derivative at relay 32, together with forward transient waves. In this figure, forward incident and reflected waves can be observable. The magnitude of these waves is associated with the signals 'MaxInc_{32}' and 'MaxRef_{32}', used in the CRCC discrimination algorithm . It should be noticed that the reflected wave starts at $\approx$ 22.3 ms (see Fig. 6.14 (b)). This event occurs at $\approx$ 0.55 ms after the blocking of converter C2 which occurs at $\approx$ 21.8 ms ('C2blk' in Fig. 6.13 (c)). The $\approx$ 0.55 ms interval corresponds to the propagation delay of cable 23 which has a length of 100 km . Therefore, the blocking of converters downstream external dc relays (*i.e.* converters placed between an external dc relay and the fault location) cause transient waves that propagate together with reflected transient waves. This reason supports the higher magnitude of reflected waves in comparison to the incident wave at external dc relays. By comparing the magnitudes of 'MaxInc_{32}' and 'MaxRef_{32}' at the decision making instant, *i.e.* at converter C3 blocking ($\approx$ 23.4 ms in Fig. 6.14 (c)), the reflected wave 'MaxRef_{32}' achieved a larger value than the incident wave 'MaxInc_{32}'. As a result, dc relay 32 is discriminated as external to the fault link. Therefore, FD 32 remains closed during the application of the protection strategy.

Fig. 6.15 illustrates the dc voltage on the positive and on the negative poles following the P2Gnd fault in link 24. The voltage is measured at busbar 2. Fig. 6.15 (a) shows the voltage with natural overvoltage decay at the non-faulty (negative) pole. Fig. 6.15 (b) shows the dc voltage with the application of the overvoltage suppression method, described in Section 6.3. As observed, the method based on the bypass of FB converter arms leads to a quick overvoltage suppression at the network.

Once a residual dc voltage is achieved at both poles, the discriminated FDs receive an opening order. In this fault case, these are the FDs 24 and 42. Fig. 6.16 illustrates the state of the FDs in the dc network. As observed, only the FDs placed at the faulty link open.

Fig. 6.17 illustrates dc current and positive and negative pole dc voltages. The dc current increases immediately after the start of the fault. Concurrently, the dc voltage experiences a shift where the non-faulty negative pole enters an overvoltage area. This overvoltage is

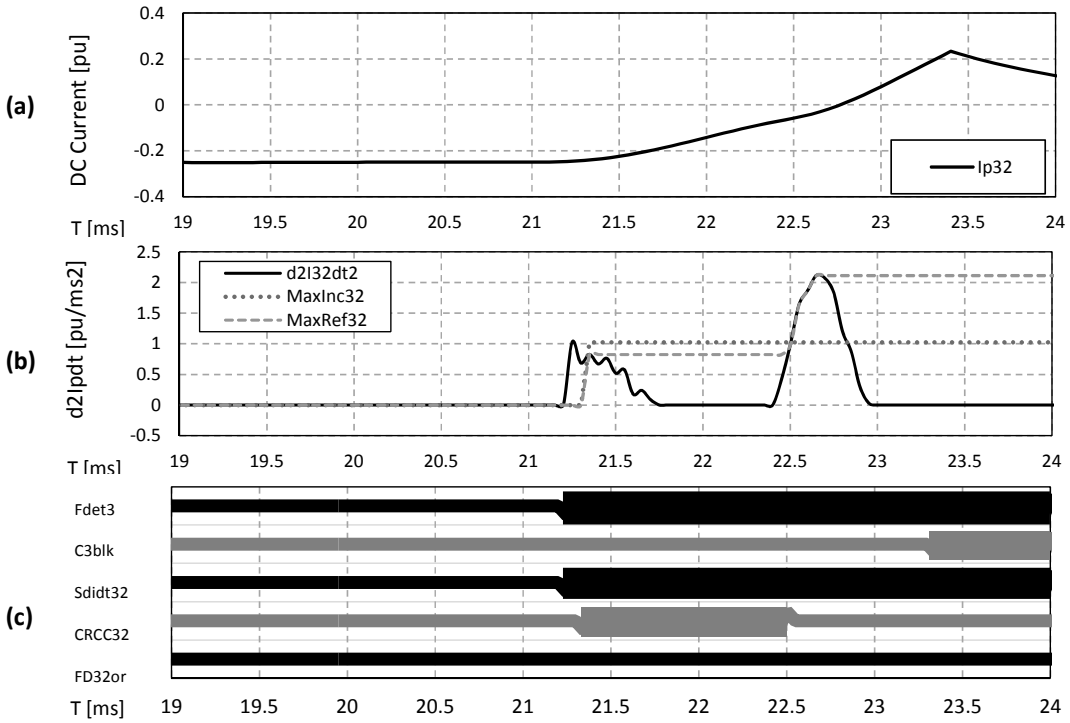

Fig. 6.14 Data analysed by the CRCC discrimination criterion in the external dc relay 32.

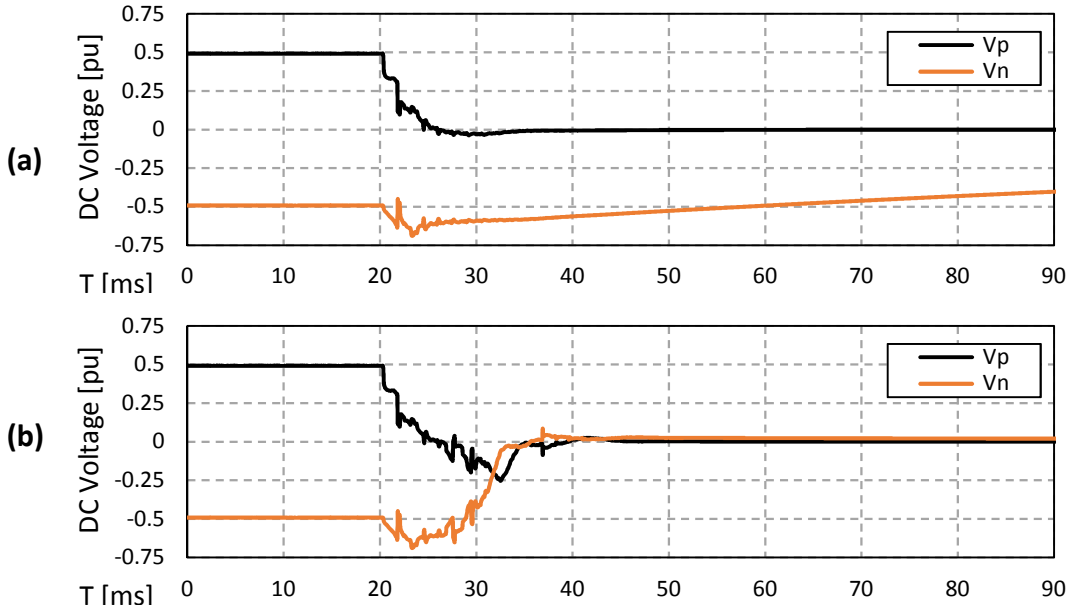

Fig. 6.15 DC voltage profiles at converter C2 following the P2Gnd fault where (a) overvoltage decays naturally and (b) overvoltage is suppressed through FB converter operation.

suppressed shortly after. With overvoltage suppression, currents flow at converters' arms are kept within nominal values, *i.e.* typically below 2 kA (as seen in Fig. 6.17 (a)). More

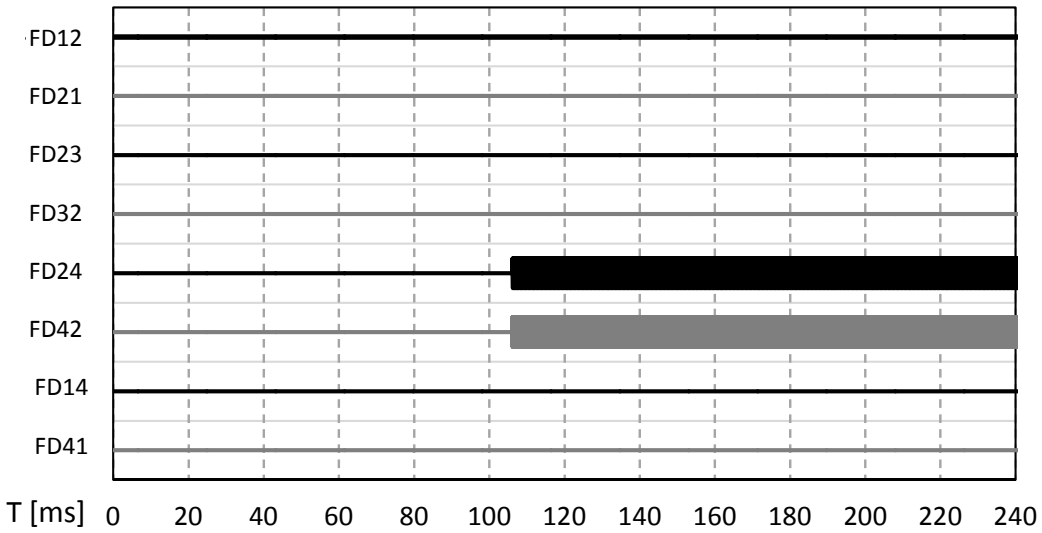

Fig. 6.16 State of FDs following the P2Gnd fault.

importantly, the voltage at the non-faulty pole moves quickly towards zero (see Fig. 6.17 (c)). A few tens of milliseconds after, the converters are de-blocked and dc currents and voltages are re-established in the MTDC network.

6.6 Summary

This chapter described a protection strategy developed for dc grids equipped with converters that possess FB capability. The protection strategy includes the steps for fault detection, fault clearance, fault discrimination, faulty link isolation and grid recovery. Fault detection is ensured by overcurrent and undervoltage criteria. Fault discrimination is ensured by the sign of current derivative, CRCC and voltage recovery criteria. DC fault clearance occurs with the blocking of FB converters while fault isolation occurs with the opening of the discriminated FDs.

The most challenging aspect of the protection strategy comprises the fault discriminating algorithm with local data. In the proposed method, a high successful discrimination rate is achieved thanks to two criteria. These are the sign of the current derivative criterion(adapted from the literature) and CCRC criterion developed during this doctorate. The combination of these methods ensure that the FDs placed in the faulty link receive an opening order. The referred discrimination criteria only consider local dc current measurements to achieve fault

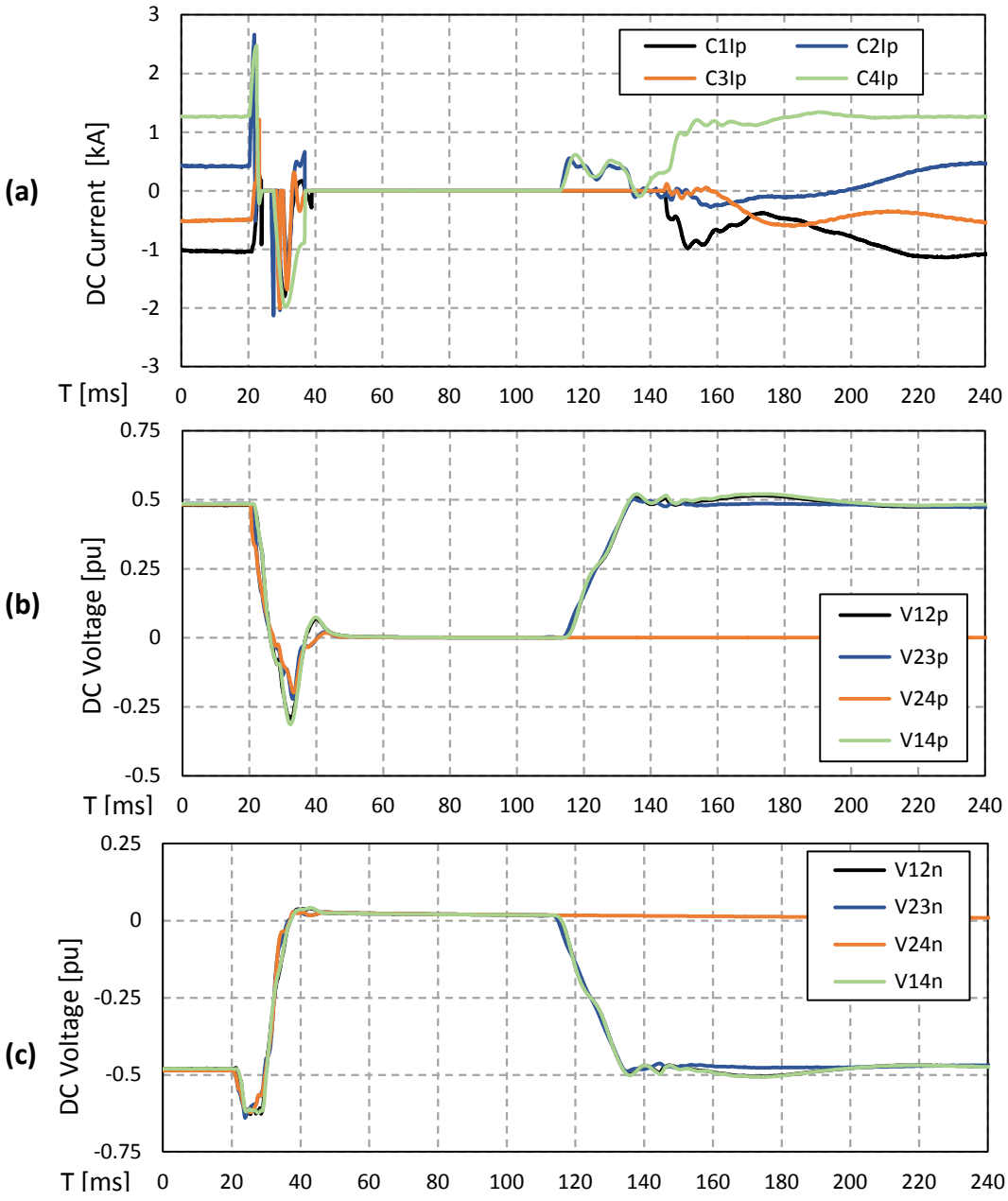

Fig. 6.17 (a) DC converter current together with dc voltage on the (b) positive pole and on the (c) negative pole.

discrimination. Therefore, fault discrimination is typically achieved in less than 2 ms after the arrival of the first fault transient wave.

In the MTDC network under study, P2Gnd faults cause an overvoltage on the non-faulty pole. Therefore, overvoltage events are suppressed thanks to a novel algorithm based on by-passing of FB submodules. This operation drives the dc voltage to a low and symmetrical

value at all the network terminals. With the presented method, dc discharging switches are not necessary and thus reduce investment and operational costs.

Simulation results are given and described for a P2P and a P2Gnd dc fault cases. Results show that the protection strategy correctly detects and discriminates the dc fault within a network. Only the FDs in the faulty link are discriminated as internal. Therefore, only these FDs receive an opening order. These results support the minimum opening philosophy of the protection strategy. Although dc fault clearance occurs quickly due to FB converter operation, fault isolation occurs with several tens of milliseconds of delay. This is due to the lower performance of the FD devices which have a 10 ms operation delay and only open after having a dc current below a residual threshold (assumed as 30 A) for a continuous period of 10 ms. Therefore, a faster operation of FD devices would reduce the outage time of an MTDC grid.

Chapter 7

Proposed Protection Strategy for MTDC Grids equipped with DC Circuit Breakers

7.1 Introduction

DCCBs represent a promising technology for protection of dc networks. Their advantages include selective fault clearance and avoidance of temporary grid outage.

The insertion of DCCBs on dc grids will be dependent on technical and economic restrictions. The main technical challenges include optimisation of operational speed, power losses, current breaking capability and energy absorption requirements. Although many DCCB prototypes have been developed by a number of companies and universities [62, 61, 63–68], these are still in testing stages. To the author's knowledge, there are no commercial DCCBs for HVDC applications at the time of writing.

The most suitable DCCB configuration for HVDC application is referred to as the hybrid DCCB. This configuration provides high current breaking capability, high operational speed and low operational power losses. At the CIGRE meeting 2014 (see [18]), a DCCB prototype was presented where a prospective fault current of 7.5 kA was interrupted in $\approx$ 5 ms for a grid voltage of 120 kV. The $\approx$ 5 ms period included about 2.5 ms of dc current increase until interruption and about 2.5 ms of dc current decrease due to energy absorption by a surge

arrester bank. Later in 2015, a full-bridge based DCCB was presented (see [65]) where a prospective fault current of 15 kA was interrupted within 3 ms for a grid voltage of 200 kV. The latter case represents, at the time of writing, the tested DCCB prototype with highest fault current interruption capability to the knowledge of the author.

In terms of economic restrictions, an HVDC DCCB is expected to be very expensive, as initially occurs with innovative technologies. The cost shall be driven by market demand, which will certainly cause a price drop over the years. In order to reduce investment costs, the introduction of DCCB in dc grids should follow a similar approach to the Zhoushan grid in China [75]. In this 5-terminal dc grid, protection devices and strategies are designed for three different project stages. In the first stage, protection is initially ensured by ACCBs. In the second stage, a number of DCCBs is added in strategic locations of the grid, to improve overall system availability. Lastly, in the third stage, DCCBs will be added to all terminals to significantly reduce network outage in case of a dc fault.

Inevitably, DCCBs are expected to be available for HVDC grids in a medium term. Once they become available, the next technical question would be how to operate them via protection. To address this question, this chapter proposes a protection strategy where fault currents are cleared by DCCBs.

A protection strategy using DCCBs should follow one of two approaches. These include non-minimum or minimum DCCB opening (introduced in Sections 2.5.4 and 2.5.3). In the non-minimum DCCB opening approach, dc fault current clearance is prioritised. In this case, DCCBs placed in non-faulty links could be required to open without discrimination. Alternatively, if a minimum tripping approach is considered, discrimination algorithms should discriminate the faulty link in a timely manner and generate a tripping signal only to the DCCBs placed in the faulty link. Comparing these two approaches, the non-minimum approach has the advantage of opening DCCBs a few milliseconds earlier and the prospective dc fault current at the interruption time would be lower together with DCCB breaking capabilities. However, with the non-minimum approach, the opening of several DCCBs and their reclose might not be accepted by system operators. A reason for this argument could be the philosophy of ac protection which follows a minimum opening approach. Therefore, a dc protection strategy should be better accepted if it follows a minimum opening approach as well.

In this chapter, the DCCB based protection strategy follows a minimum opening approach. The fault detection and fault discrimination methods introduced in Chapter 4 are considered for decision making. Simulation results are based on the CIGRE 11-terminal dc test system [15, 58] described at Section 3.3. This large network comprises a rather complex arrangement that will give the assessment of the robustness of the detection and discrimination algorithms.

7.2 Protection Strategy Description

The DCCB based protection strategy, if adopted, should be implemented in every busbar unit of an MTDC grid. A busbar unit analyses current and voltage measurements from local dc relays and runs the fault detection and fault discrimination algorithms. Then, as necessary, it sends opening/closing orders to the associated DCCB together with blocking/de-blocking orders to the associated converter. This strategy is described in detail in the following subsections.

7.2.1 DC Fault Detection

The protection strategy initiates with detection of a dc fault. The fault detection is achieved with overcurrent and overvoltage algorithms. Typically, a dc fault is detected a few time samples after the arrival of the first transient waves.

7.2.2 Converter Blocking

A converter blocking order is generated to protect sensitive power electronic switches from potential harmful currents. The blocking order is generated following any of the following criteria:

1. In a converter station if an overcurrent is detected. The overcurrent threshold is 2.4 kA while the nominal dc current is 2 kA. The blocking order has a delay of 0.1 ms.
2. In a dc relay if a dc fault is detected by overcurrent or undervoltage means. In this case, the blocking order arrives with a 2 ms delay due to signal processing requirements.

With a blocking order, the firing pulses for converters' IGBTs become zero. In this way, the submodules' capacitors and IGBTs are protected against ac infeed fault currents. These currents keep flowing to the dc side fault during converter blocking, but mainly through the uncontrolled diodes and submodule's thyristor, if existent.

7.2.3 Discrimination of DCCBs

The fault discrimination methods considered in this thesis are provided in Section 4. These algorithms analyse local dc current and voltage measurements in order to classify a dc fault either as internal or external to their associated links. The fault discrimination algorithms fall in two criteria. The first criterion is based on the sign of current derivative. This algorithm is able to discriminate at least half of the dc relays at non-faulty links. The second criterion comprises the CRCC algorithm. This algorithm takes into account potential variations of the current rate of change within a short period of time.

A dc relay (in turn associated with a DCCB) that meets both the current direction and CRCC criteria is discriminated as internal to the faulty link. Conversely, a relay that does not meet the aforementioned criteria is classified as external to the faulty link.

7.2.4 Fault Clearance and Isolation

DCCBs discriminated as internal to a faulty link receive an opening order. These devices have the duty to interrupt the dc fault current and isolate the faulty link. DCCBs operate with a 5 ms delay after receiving the opening order.

Fig. 7.1 illustrates the behaviour of a dc fault current together with a DCCB opening order and DCCB opening state. From the DCCB opening instant, the dc fault current starts to decay towards zero. Then, the fault energy is absorbed by a surge arrester bank (as given in the hybrid DCCB configuration).

7.2.5 Overvoltage and Voltage Imbalance Suppression in P2Gnd Faults

In the case of a P2Gnd fault in a monopole dc link, a voltage shift occurs on the monopole network. The fault impedance changes the voltage symmetry, forcing the faulty pole voltage

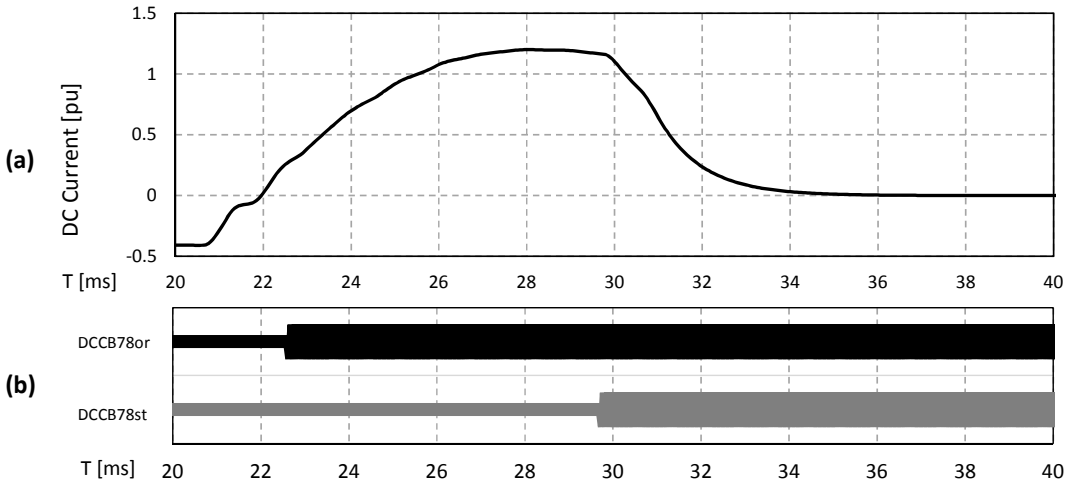

Fig. 7.1 (a) DC fault current profile and (b) DCCB state.

to move towards zero while the non-faulty pole voltage moves towards twice the nominal value. This causes a harmful overvoltage at non-faulty poles of dc links.

In this thesis, two overvoltage suppression strategies have been proposed (see Sections 5.2.3 and 6.3). Regarding a grid with HB based converters, an overvoltage suppression strategy was proposed with basis on a discharging circuit that dissipates the energy in the non-faulty poles (as described in Section 5.2.3). This circuit is composed of a limiting resistor and an FD which is a device with no appreciable current breaking capability. Therefore, the overvoltage is suppressed and reduced to zero, together with the discharging current on the FD.

In this chapter, DCCBs are not a technical restriction. Therefore, the discharging circuit could be composed of a limiting resistor R_{OS} and DCCBs, instead of FDs (as in Section 5.2.3). This arrangement is refereed as discharging DCCB circuit in this thesis. The discharging DCCBs are identical to link DCCBs (modelled in Section 3.4.5) with exception of having a lower current breaking capability. The rating of R_{OS} is based on potential maximum current and voltage on the discharging circuit. Therefore, the adopted approach is to select an high limiting resistor which would lead to a relatively low discharging current together with a low rated discharging DCCB. Accordingly, a R_{OS} with 500 Ω ensures that the discharging current remains below 1 kA for a maximum overvoltage of 440 kV (for a 1.1 p.u. operating voltage as permitted according to [93]). Having a relatively low discharging current leads to a reduced rating of the discharging DCCB. In turn, such a discharging DCCB should be an

economical device. Fig. 7.2 illustrates the discharging circuit with DCCBs and a limiting resistor.

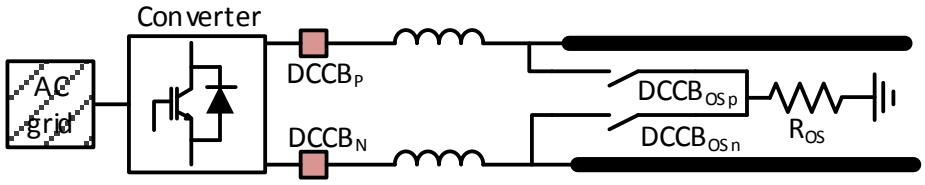

Fig. 7.2 Configuration of the discharging circuit with DCCBs.

The advantage of using a discharging circuit with DCCBs instead of FDs is that overvoltage can be reduced to the nominal voltage instead of being reduced to zero. Thus, with DCCBs the dc voltage restoration after a P2Gnd occurs in a quicker manner. The control of the discharging DCCBs ($DCCB_{OSp}$ or $DCCB_{OSn}$) is based on the following principles:

1. In normal operation:
   Discharging DCCBs remain in open state.
2. In overvoltage suppression mode:
   (a) Close the positive pole discharging DCCB if overvoltage is detected on the positive pole:

$$V_p > 0.55\ p.u. \tag{7.1}$$

   (b) Close the negative pole discharging DCCB if overvoltage is detected on the negative pole:

$$V_n < -0.55\ p.u. \tag{7.2}$$

   (c) Reopen the positive/negative pole discharging DCCB once the dc voltage magnitude on the non-faulty pole approximates to the nominal voltage magnitude of | 0.5 | p.u.;
   (d) only one pole discharging DCCB shall operate.

The discharging DCCB enables the dc voltage to be shifted back to the nominal values of $\pm$ 0.5 p.u. However, this DCCB incurs in an operation delay assumed as 5 ms; thus the DCCB re-opening order must be given with a 5 ms advance period. As a consequence, it becomes hard to re-open the discharge DCCB with an exact dc voltage of $\pm$ 0.5 p.u. In order to simplify the re-opening action, a practical threshold of | 0.55 | p.u. is considered. This

threshold is based on observations of overvoltage suppression simulations. The criteria to re-open the discharging DCCB becomes:

$$\text{If } V_{nf} < |\ 0.55\ | \text{ p.u., then re-open discharging DCCB}$$

where V_{nf} is the voltage at the non-faulty pole.

Fig. 7.3 shows current and voltage profiles resulting from a positive-P2Gnd fault at a monopole dc link and operation of a discharging DCCB. The current on the discharging circuit is illustrated together with voltage and discharging DCCB state. It should be noticed that after the dc voltage experiences a shift at the start of the fault (at 20 ms) where the faulty pole voltage '*Vp*' decays towards zero and the non-faulty pole voltage '*Vn*' moves towards –1 p.u. With closing of the DCCB 'disDCCB' (thin line), the grid voltage moves to nominal values while a current '*Idis*' flows in the discharge circuit. DCCB '*disDCCB*' opens (thick line) when the dc voltage is approximately $\pm$ 0.5 p.u.

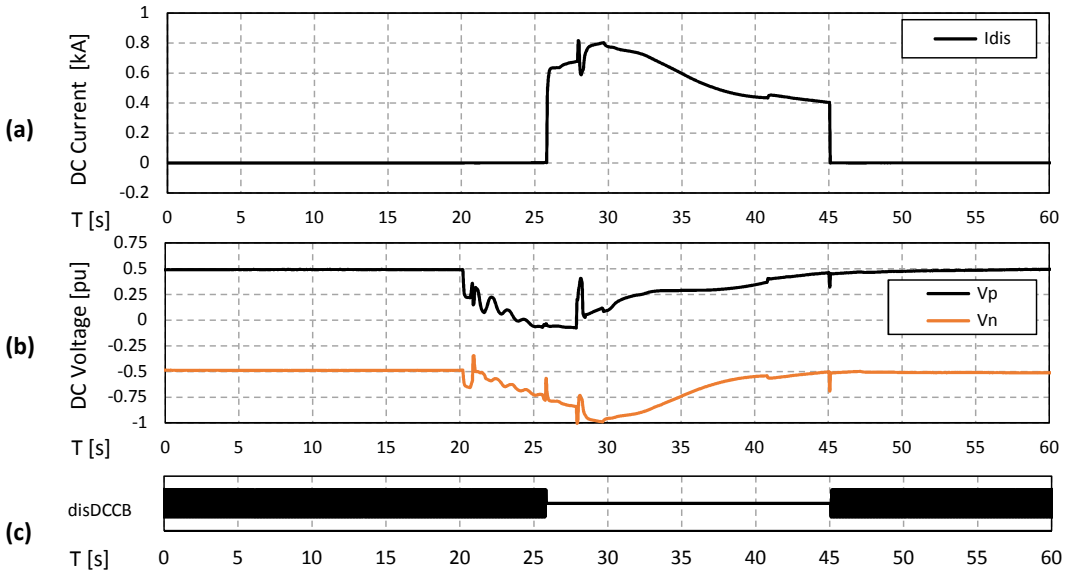

Fig. 7.3 (a) DC fault current on a discharging circuit, (b) dc voltage and (c) discharging DCCB state.

The overvoltage and voltage imbalance suppression method occurs independently of other actions in the protection strategy, including converter blocking and link DCCB opening. Therefore, some transients are expected during overvoltage suppression operation (such at $\approx$ 29 ms in Fig. 7.3 (b)).

In the CIGRE 11-terminal grid, the sub-system that includes converters C6 to C9 has a radial monopole configuration. Therefore, overvoltage events are expected in the case of a

P2Gnd fault at any of the links connecting these converters. The CIGRE 11-terminal system includes a bipole section where overvoltage events due to P2Gnd faults are not achievable.

In the radial monopole of the CIGRE 11-terminal grid, only two discharging circuits are required being those located at the busbar units 7 and 8. These locations ensure overvoltage suppression in case of a P2Gnd fault at any location of the monopole grid (composed of dc links 67, 78 and 89).

7.2.6 Grid Restoration

After fault clearance, dc grid recovery is initiated with the de-blocking operation of converters. The converters operating as rectifiers at the pre-fault instants restore the dc voltage. Shortly after, the converters operating as inverters at the pre-fault instants restore the dc power flow. The de-blocking of a rectifier occurs if any of the following conditions is met:

1. Discriminated DCCB opening operation:
   If a DCCB discriminated as internal to the faulty link is open, the fault is isolated. The de-blocking order has a practical time delay of 5 ms. This period is considered due to likely opening delays between the discriminated DCCBs at both ends of the faulty link.

2. Voltage recovery:
   The recovery of link dc voltage at a busbar indicates that grid restoration has started by a converter connected to a remote busbar. Therefore, converters shall be de-blocked if the local dc voltage recovers approximately to nominal values. The voltage thresholds given in Section 4.3.3 are considered.

3. Maximum time in blocking mode:
   Converters are de-blocked after a maximum time (in blocking mode) if the any criterion at the above is not met. This maximum time is set as 50 ms which is a large value in comparison to typical delays of fault isolation and voltage recovery.

The de-blocking of a converter in inverter mode (at the pre-fault instants) occurs with the criterion of voltage recovery as mentioned above. This way, the power exchange between ac and dc grids keeps the same direction during both the pre-fault and the grid recovery periods.

Succinctly, an ac grid exporting power at the pre-fault instant will export power during grid recovery by means of a converter in rectifier operation. Conversely, an ac grid importing power at the pre-fault instant will continue to import power during grid recovery by means of a converter operating in inverter mode.

In a few fault scenarios, a DCCB might open in a non-faulty dc link. In this case, grid restoration may be terminated by re-closure of such DCCBs. The re-closing criterion is based on the voltage recovery algorithm given in Section 4.3.3.

7.3 Simulation Results

DC fault simulations are performed in the CIGRE 11-terminal network using PSCAD/EMTDC. Two fault cases are described in detailed. These include a P2P fault and a P2Gnd fault. The P2P fault occurs at the middle of link 14 and has an impedance of 10 Ω. The P2Gnd fault occurs at the middle of the cable section of link 78 and has an impedance of 0.1 Ω. Fig. 7.4 illustrates the CIGRE 11-terminal dc grid configuration and the location of the two detailed fault cases.

7.3.1 Pole-to-Pole Fault

A P2P fault starts at OHL 14 at 20 ms. The fault occurs at the middle of link 14, *i.e.* 200 km from relay 14 and 200 km from relay 41. Consequences of the P2P fault include a quick voltage drop in most dc links and an overcurrent is several neighbour links.

Fig. 7.5 illustrates the converter blocking actions, which occurs after fault detection at dc relays or at the converter stations. Regarding the converters at the faulty link terminals, it can be noticed that C1 ('C1$_{blk}$') blocks slightly earlier than C4 ('C4$_{blk}$'), even when they are placed at the same distance from the fault location. The reason for different blocking times is related to the power setpoint of each converter at pre-fault instants: C1 was in rectifier mode (injecting 1 p.u. current into dc grid as given in Table 3.6), while C4 was in inverter mode (taking out $\approx$ 0.72 p.u. current from dc grid). With the dc fault, current from both converters flows to the fault location. Therefore, dc current moves quickly from 1 p.u. to 1.2 p.u. in C1, leading to overcurrent in less than 1 millisecond after the start of the fault. In C4, dc current moves from –0.72 p.u. to 1.2 p.u., which takes slightly a longer time in comparison to the

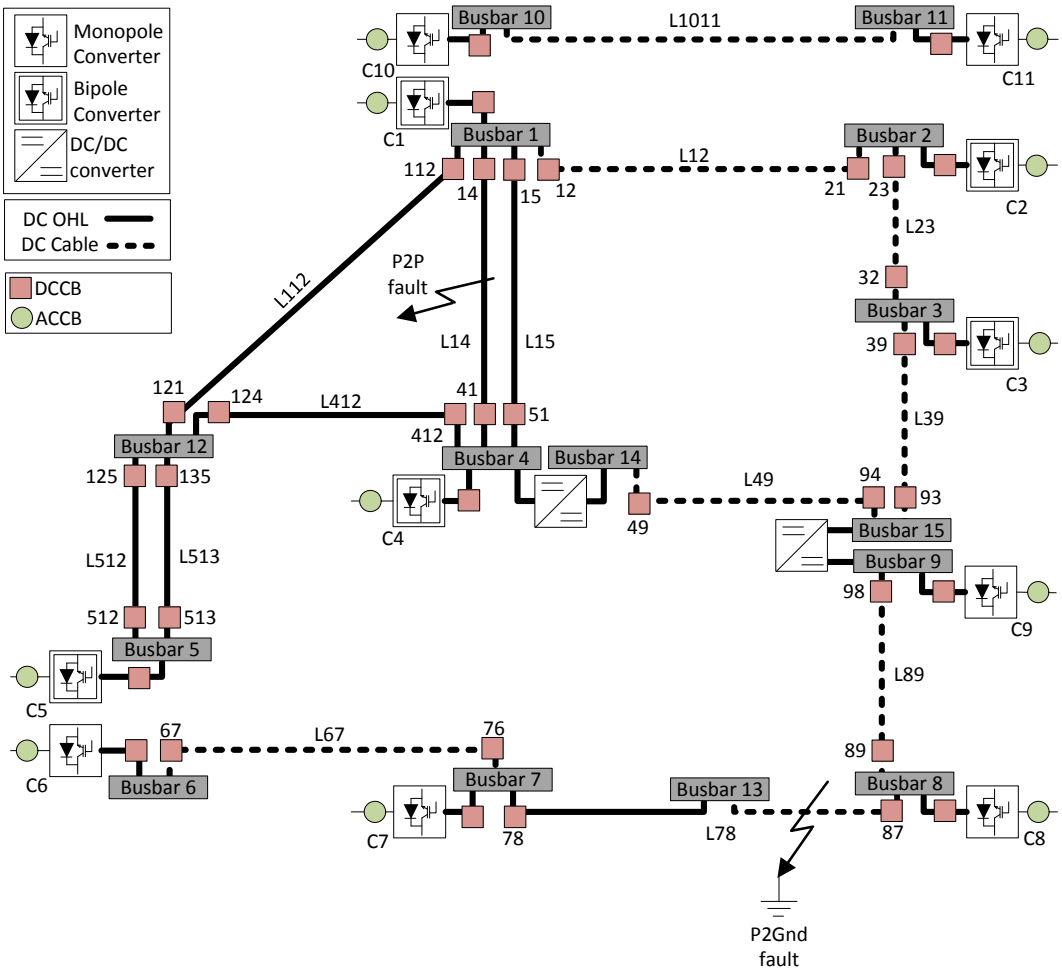

Fig. 7.4 Location of the P2P and P2Gnd faults in the CIGRE 11-terminal dc network.

overcurrent in C1. Converters C2, C3, C5, C7-C9 are also blocked followed fault detection either at a neighbouring dc relay or converter station.

Converter C6 is placed in a remote area (1000 km of dc links separate C6 from the dc fault location) and does not detect the dc fault. Such link lengths represents a challenge for protection systems where sensitive fault detection algorithms are required. Therefore, this area should receive more attention in future research. For completeness, long lines might have dispersion of the travelling waves following faults that occur due to the frequency dependency model of the line [110]. The effect of this phenomenon in the proposed algorithms is recommended for future research.

1. Page 126: In general, there should be more emphasis on the limitations/weaknesses of the proposed algorithms. A specific case could be a limitation due to line lengths. 1000km

lines are extremely long and protecting them is a challenge. This is useful to other researchers and might be included as future work too.

2. Page 126: For long lines, 1000km+, dispersion of the travelling waves following faults will occur due to the frequency dependency. Slower frequencies will trail the faster frequencies. This phenomenon will also depend on the modes of propagation. However, it is likely to have an effect on the CRCC method, so a mention of this phenomenon, with perhaps some reference to the literature, would be recommended for completeness.

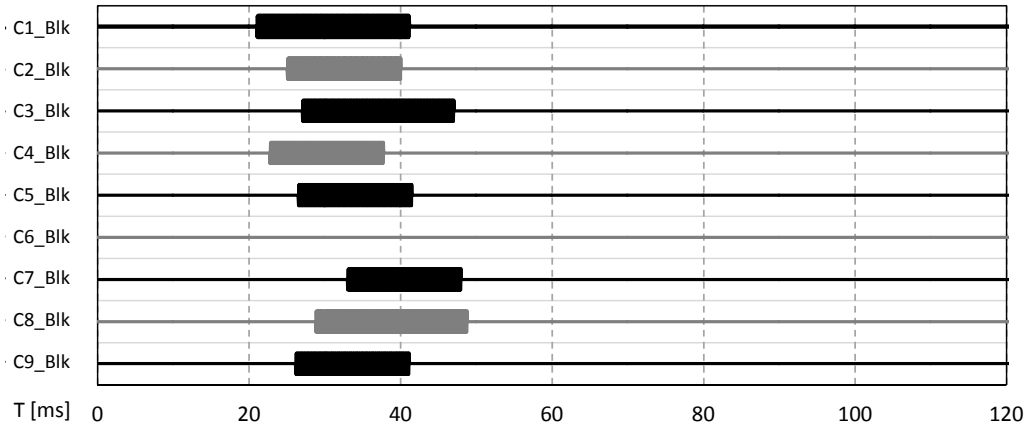

Fig. 7.5 Converter blocking state

The discrimination algorithms are initiated if a disturbance is detected by overcurrent, undervoltage or current derivative means. The discrimination criteria introduced in Section 4.3 are used to support decision making. Considering the criterion of sign of current derivative, a number of DCCBs is selected as potential internal to the faulty location. Then, in order to discriminate only the DCCBs internal to the faulty link, the CRCC criterion is considered.

Fig. 7.6 illustrates data analysed by discrimination algorithms from a relay internal to the faulty link, relay 41. In Fig. 7.6 (a), it is perceptible that dc fault current is increasing over time. This behaviour relates to a positive sign of current derivative. As a result, DCCB 41 is classified as potentially internal to the faulty link (see 'Sdidt41' in 7.6 (c)). In order to verify that DCCB 41 is internal to the faulty link, the second order current derivative is analysed (see 'd2I41dt2' in Fig. 7.6 (b)) with the CRCC criterion. The magnitudes of the transient waves are captured, being those marked as '$\text{MaxInc}_4$1' and '$\text{MaxRef}_4$1' as seen in Fig. 7.6 (b).

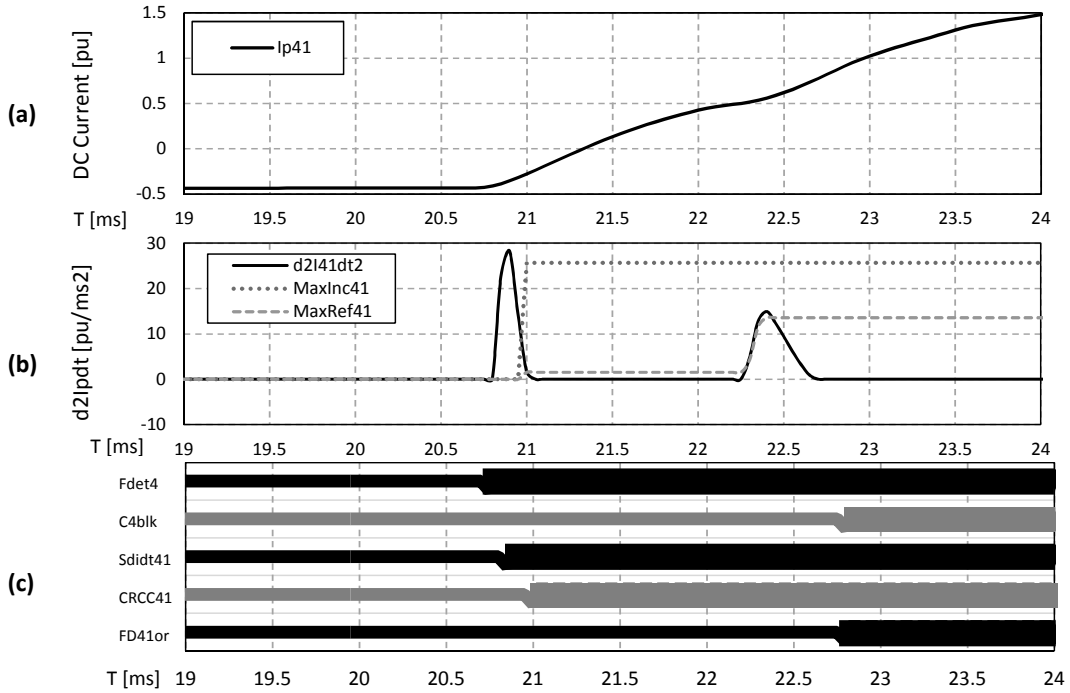

Fig. 7.6 Data analysed by the discrimination algorithms in the internal dc relay 41. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

For an internal fault, the current experiences an initial high rate of change that decays continuously over time. This behaviour is experienced on relay 41. In fact, the initial current change leads to a high value of the incident wave 'MaxInc_{41}', while the following wave, the reflected wave 'MaxRef_{41}', has a much smaller magnitude. By comparing the magnitudes of the 'MaxInc_{41}' and '$\text{MaxRef}_{4}1$', it is concluded that the initial wave has a larger magnitude than the second wave, as marked by the signal 'CRCC_{42}' in Fig. 7.6 (c). The decision to open DCCB 41 ('DCCB41or') is given at the instant of converter blocking 'C4blk'. As the signal 'CRCC_{42}' is true (thick line) during the blocking of converter C4, the DCCB 4 is classified as internal to the faulty link and receives an opening order (thick line of 'DCCB41or').

Fig. 7.7 illustrates data analysed by discrimination algorithms from a relay external to the faulty link (relay 89). This relay is in a remote location in comparison to the fault location (600 km distant).

The discrimination algorithm starts with detection of a disturbance shortly after 24 ms ('Fdet8') due to the current derivative algorithm. A few milliseconds later, fault detection is achieved and leads to converter blocking (2 ms later) at $\approx$ 29 ms. It should be noticed that

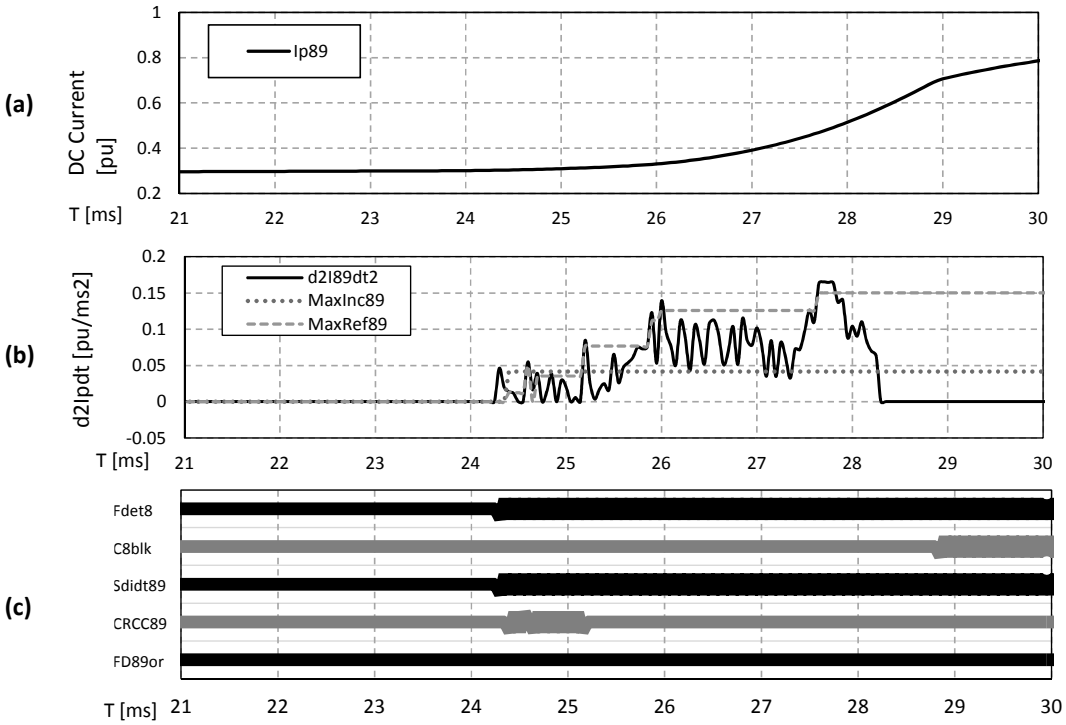

Fig. 7.7 Data analysed by the discrimination algorithms in the external dc relay 89. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

during the time window given in Fig. 7.7, dc current remains below 1 p.u.; hence overcurrent detection is not achieved.

In terms of transient waves, the second order current derivative ('d2I89dt2' in Fig. 7.7 (b)) experiences a number of peaks. They occur due to multiple reflections of transient waves at inductive terminations of several links and even at the OHL-cable joint connection of link 78. Additionally, measurement noise is amplified by the current derivative function which adds up to the transient waves. In 'd2I89dt2', the magnitude in the reflected waves increases over time. This behaviour is opposite to the one seen in the internal dc relay 41. The discrimination judgement at relay 89 is achieved with the blocking of converter C8 ('C8blk') in Fig. 7.7 (c). At this instant, signal '$CRCC_{89}$' is false (thin line). Therefore, relay 89 is classified as external to the faulty link. For this reason, DCCB 89 order ('DCCB89or') remains closed (thin line).

Fig. 7.8 illustrates the outage of links in the CIGRE 11-terminal network. This figure is directly linked with the state of DCCBs. However, instead of illustrating the state of 26

DCCBs, only the outage of the 13 dc links is shown. The link outage is represented by a double thick line which represents the open state of both link end DCCBs. In this fault case, only the DCCBs 14 and 41 are classified as internal to the faulty link. As a result, DCCBs 14 and 41 open resulting in the isolation of the faulty link L14.

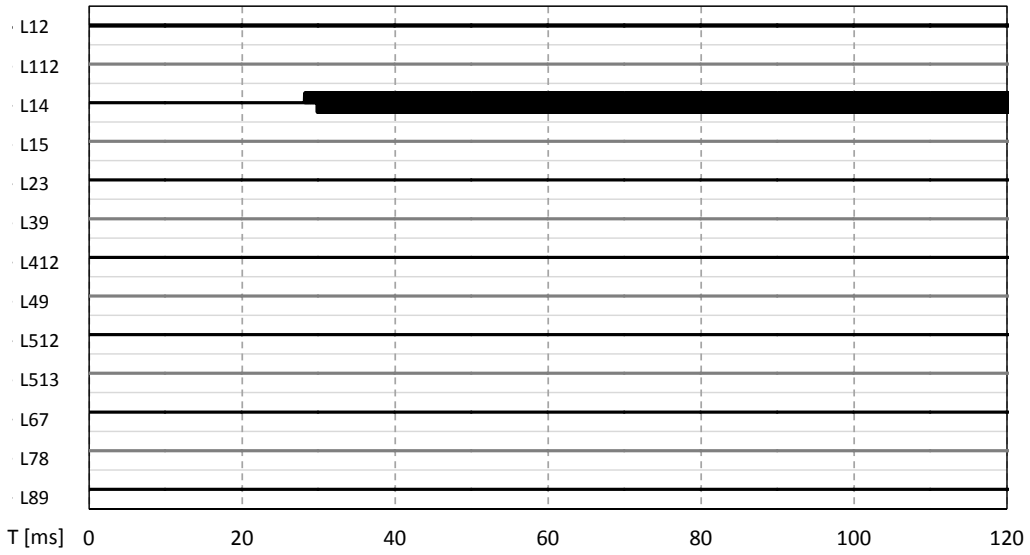

Fig. 7.8 Link outage due to opening of link end DCCBs.

Fig. 7.9 illustrates currents and voltages at a number of converters. For visualisation clarity, only the values related to the positive pole are shown as they are approximately symmetric to the negative pole values. The P2P fault causes overcurrent in some converters and a voltage collapse in most network terminals. However, fault clearance and isolation are provided by fast DCCBs. Therefore, the disturbance lasts only for a few tens of milliseconds. After this period, dc currents and dc voltages return to the pre-fault values with respect to the new grid configuration, where link 14 is out of operation.

7.3.2 Pole-to-Ground Fault

A P2Gnd fault occurs at link 78 which is placed in the monopole part of the dc grid. Link 78 is composed of a 100 km section of OHL and a 100 km section of underground cable. The fault location occurs at the middle of the cable section; *i.e.* 50 km from relay 87. The dc fault starts at 20 ms.

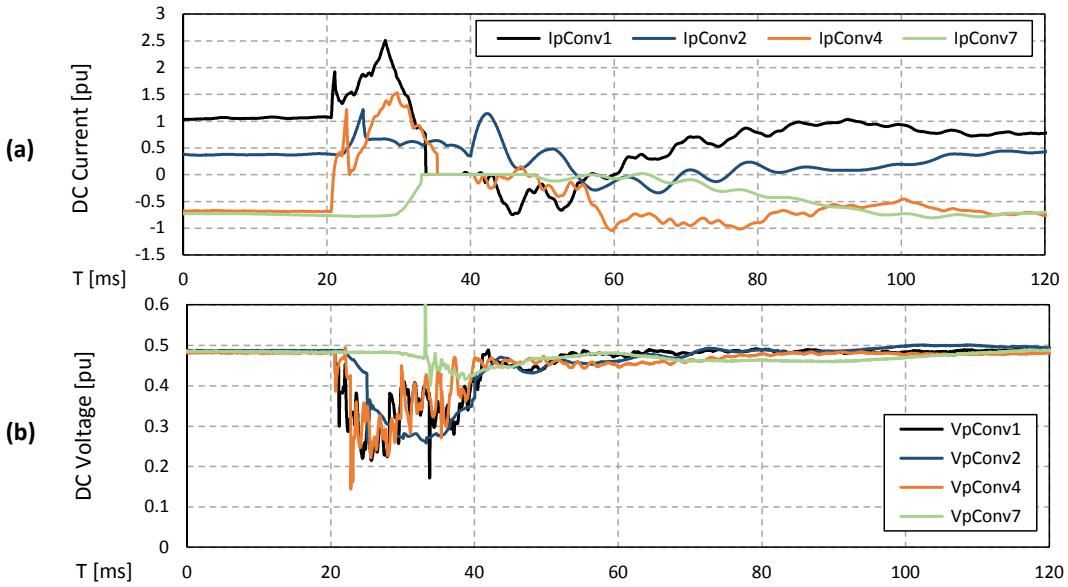

Fig. 7.9 Profile of (a) converter dc currents and (b) positive pole voltages.

The P2Gnd fault causes a voltage shift in the monopole grid composed of links 67, 78 and 89. In this grid, the P2P voltage remains within nominal values as only the voltage reference changes. As a consequence, the voltage at the terminals of the dc-dc transformer between the monopole and bipole grid remains mostly unchanged. Fig. 7.10 shows the voltage at both terminals of the dc-dc transformer, considering that 'Vp89' and 'Vn89' stand for the monopole network while 'Vp94' and 'Vn94' stand for the bipole network.

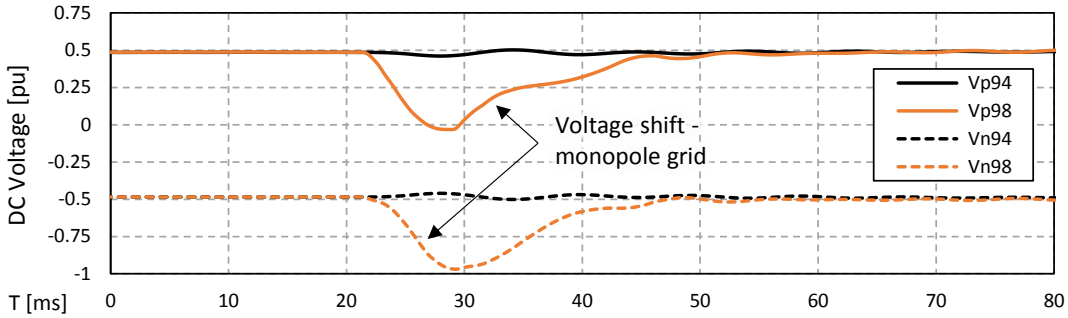

Fig. 7.10 DC voltage at monople and bipole dc links due to a positive-P2Gnd fault.

As observed in Fig. 7.10, undervoltage is not achieved in the bipole grid while dc current also remains within nominal values. As a result, fault detection is not achieved at the bipole network. In the monopole network, fault detection is achieved by means of overcurrent or

undervoltage methods. These events lead to the blocking of converters C6-C9. Fig. 7.11 illustrates the converter blocking state.

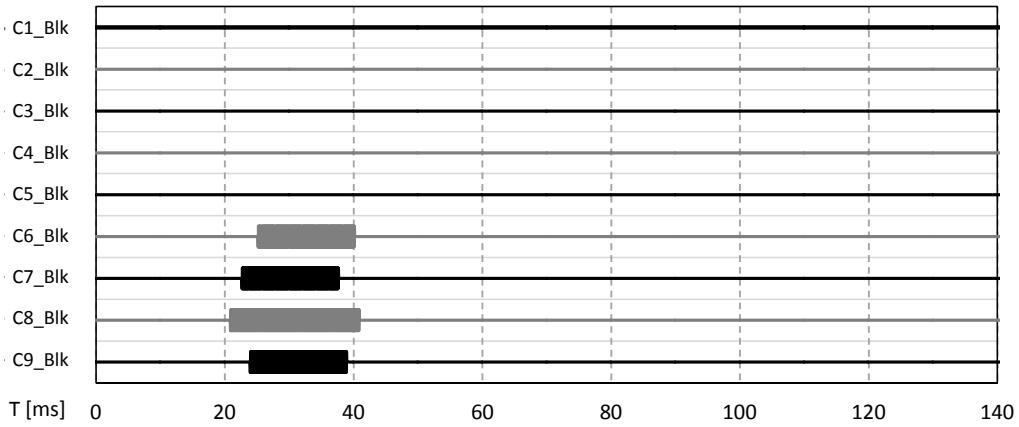

Fig. 7.11 Converter blocking state.

Fault discrimination is initiated with the detection of a disturbance in the system. The sign of current derivative and CRCC discrimination algorithms are executed to classify a relay as internal or external to the faulty link. Then, an order to clear and isolate the dc fault is set to the DCCB classified as internal to the faulty link.

Fig. 7.12 shows protection data that concerns to dc relay 78 which is internal to the faulty link. Regarding the sign of current derivative, fault current 'Ip78' experiences an increasing behaviour from $\approx$ 20.5 ms. This indicates that the fault current flows in the direction of busbar 7 towards link 78 where the fault is located. As a consequence, signal 'Sdidt78' becomes true (see Fig. 7.12 (c)). At this point, the fault is considered potentially internal to link 78. In order to confirm that the fault is within link 78, the CRCC algorithm is performed. The dc current data analysed by the CRCC is given in Fig. 7.12 (b). With the arrival of the incident transient wave, a large change of current is experienced, as captured by the signal 'MaxInc_{78}'. Shortly after, reflected transient waves arrive to relay 78, as captured by signal 'MaxRef_{78}'. In this case, the magnitude of the transient waves is reduced over time. This behaviour leads the 'MaxInc_{78}' to be larger than 'MaxRef_{78}', as reported by the signal 'CRCC_{78}' (see Fig. 7.12 (c)). Considering the value of 'CRCC_{78}' at the decision time (at blocking of converter C7 ('C7blk')), the fault is classified as internal to link 78. Therefore, the DCCB 78 receives an opening order ('DCCB78or').

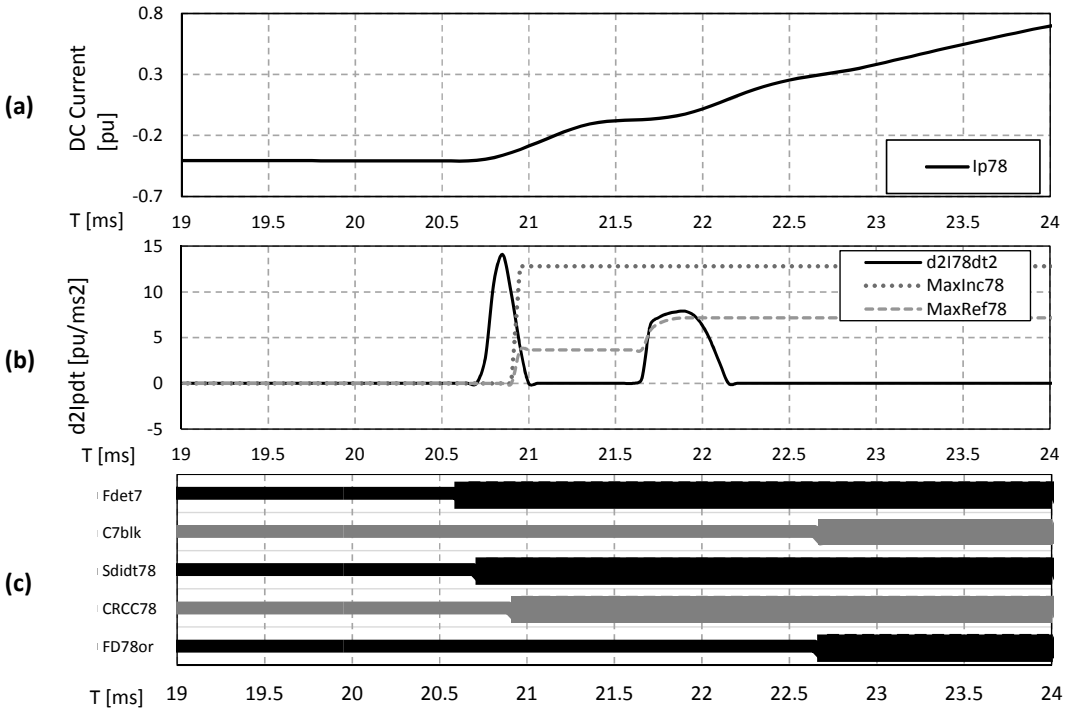

Fig. 7.12 Data analysed by the discrimination algorithms in the internal dc relay 78. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

Fig. 7.13 illustrates protection data associated with relay 98 which is external to the faulty link. Regarding the sign of current derivative, relay 98 is classified as potential internal to the faulty link as the current behaviour in Fig. 7.13 (a) is similar to that shown in Fig. 7.12 (a). Regarding the CRCC algorithm, the curve in Fig. 7.13 (b) presents transient waves with different magnitudes. In this case, the magnitudes are not reduced in time as it occurred in Fig. 7.12 (b). The incident wave's magnitude is captured with signal 'MaxInc$_{98}$' while the maximum magnitude of the reflected wave is captured with 'MaxRef$_{98}$'. By comparing the magnitude of the rates of change of dc current, the fault is classified as external to link 89. This is marked by signal 'CRCC$_{98}$' at the decision instant; *i.e.* at the blocking of converter C9 ('C9blk').

The transients in relay 98 are better explained with help of Fig. 7.14. This figure shows the second derivative of dc current at relay 98 with and without the influence of the dc-dc transformer associated to busbar 9. For instance, 'MaxRef$_{98}$' in the external relay 98 corresponds to the third transient wave 'tw3' which starts at $\approx$ 22.1 ms (see Fig. 7.13 (b)).

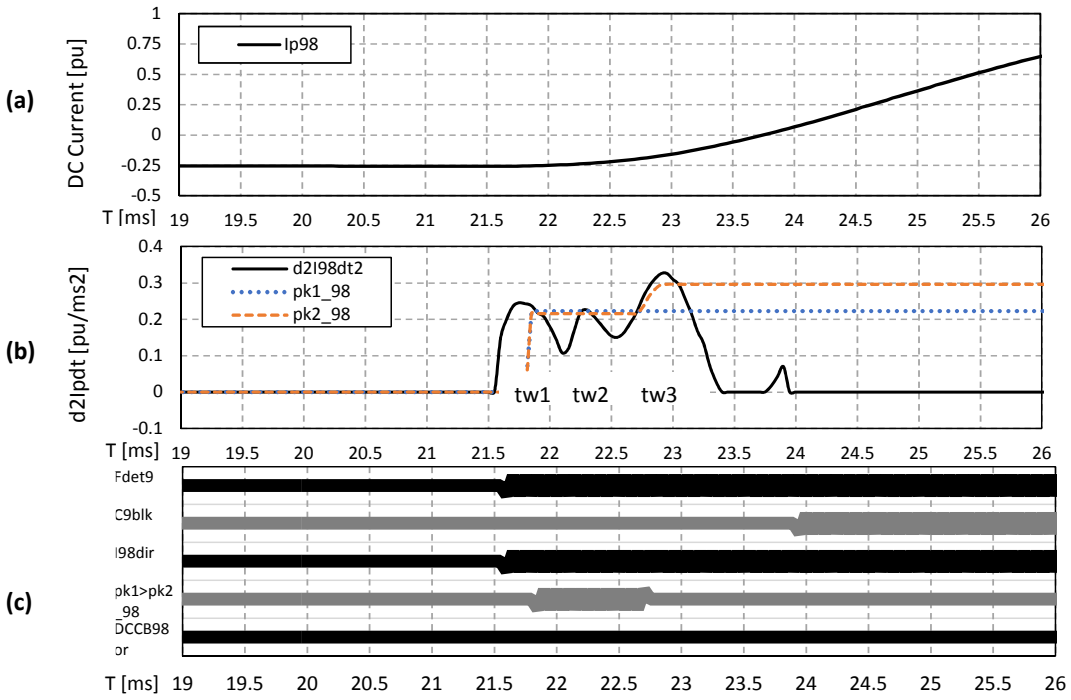

Fig. 7.13 Data analysed by the discrimination algorithms in the external dc relay 98. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

This wave is associated with the disturbance caused by blocking of converter C8 at $\approx$ 20.9 ms. Adding the propagation delay of link 89 (1.2 ms for the 200 km long cable), the transient wave arrives at relay 98 at 22.1 ms. However, in this case, there is a second transient wave 'tw2', that is added to the reflected wave 'tw3' (see Fig. 7.14 (a)). The origin of the wave 'tw2' in Fig. 7.14 (a) is associated with backwards reflections at the dc-dc transformer, that is connected to busbar 9.

It should be noticed that the magnitudes of three transient waves are visible in Fig. 7.14 (a) while in Fig. 7.14 (b) only two magnitudes are visible. This is because the removal of the dc-dc transformer also removes the reflected wave 'tw2' at Fig. 7.14 (a). Notwithstanding, the outcome of the discrimination algorithms is not modified due to the influence of the dc-dc transformer.

Fig. 7.15 illustrates the outage of dc links which is given by the opening state of DCCBs at both ends of a link. DCCBs 78 and 87 have been discriminated as internal to the faulty link. As a consequence, only these receive an open order while the other DCCBs remain in the closed state.

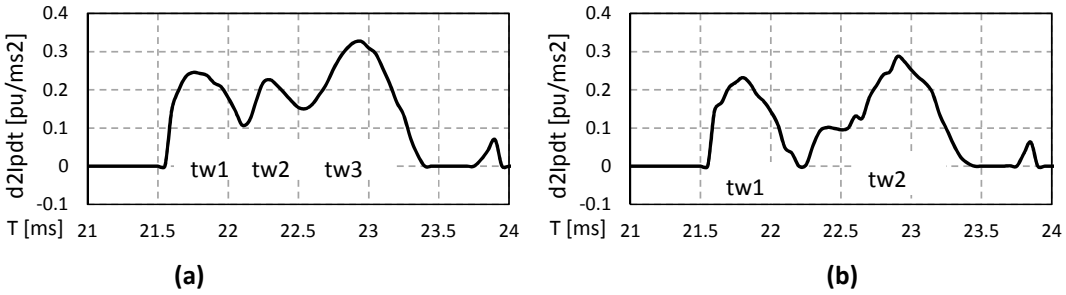

Fig. 7.14 Second derivative of dc current at relay 98 (a) with and (b) without a dc-dc transformer connected at busbar 9.

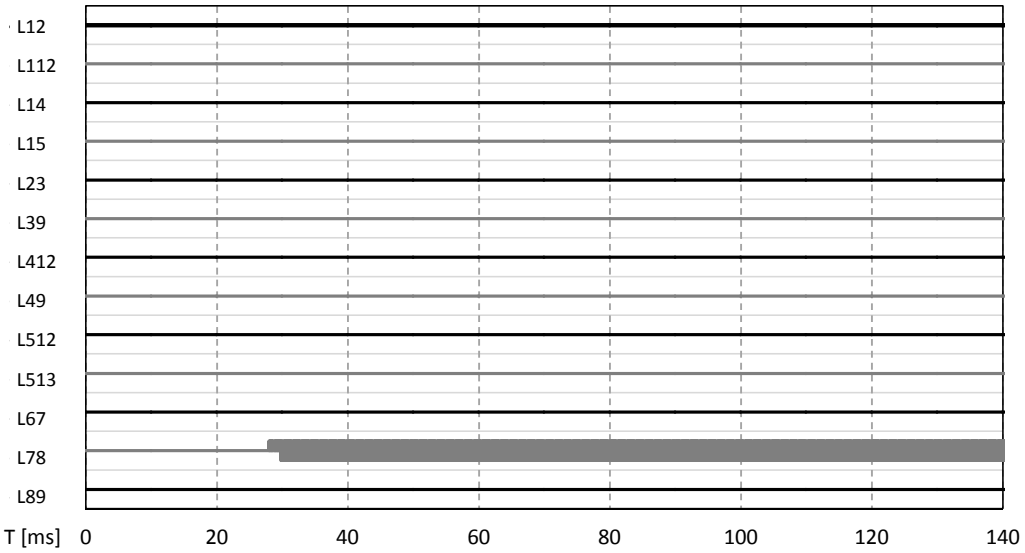

Fig. 7.15 DC link outage due to link end DCCB opening.

Overvoltage and voltage imbalance suppression occurs in parallel with other actions of the protection strategy, including converter blocking and dc fault clearance. The overvoltage and voltage imbalance operation occurs after detection of a P2Gnd fault in the monopole network. Two overvoltage discharging circuits are installed at busbars 7 and 8. Fig. 7.16 illustrates currents, voltages and the state of the DCCBs associated to these discharging circuits. It should be noticed that after fault isolation at $\approx$ 29 ms, the dc voltage at the non-faulty pole starts to increase towards nominal values. The DCCB are re-open once the voltage at non-faulty pole approaches the –0.5 p.u. magnitude.

DC current and voltage profiles are illustrated in Fig. 7.17 for a few converters. It should be noticed that the currents and voltages ('IpConv4','VpConv4','VnConv4') at converter C4 which is in the bipole part of the network, experience minor modifications due to the

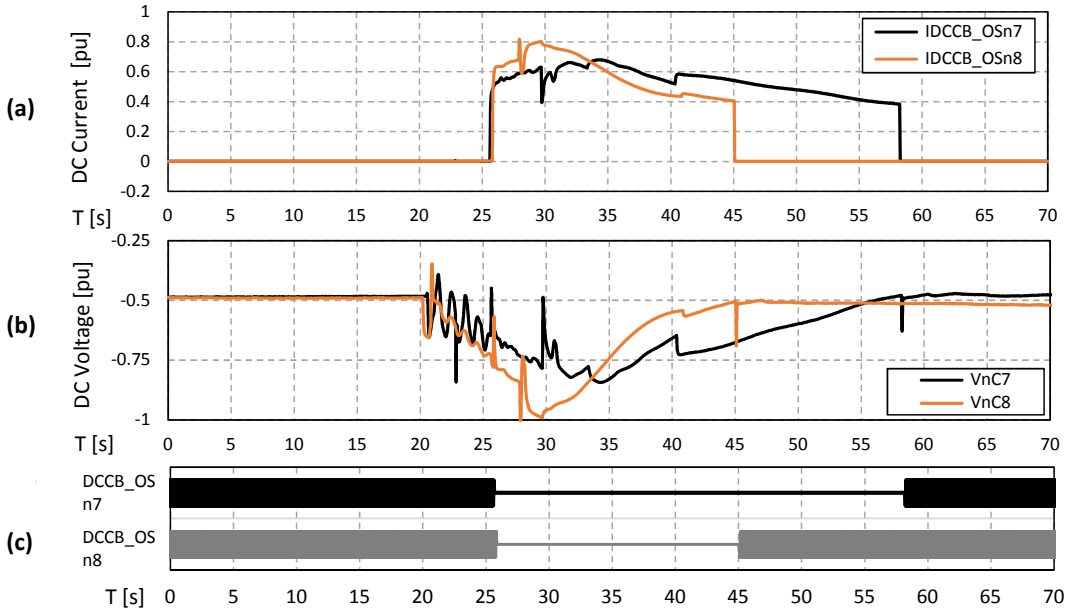

Fig. 7.16 (a) Current on the discharging circuits, dc voltage at the non-faulty pole and (c) state of the discharging DCCBs 7 and 8.

P2Gd fault. Correspondingly, currents and voltages at the monopole network experience overcurrent ('IpConv8'), undervoltage ('VpConv6', 'VpConv7', 'VpConv8') and overvoltage ('VnConv6', 'VnConv7', 'VnConv8') events.

At the end, the dc fault has been correctly discriminated with the sign of current derivative and CRCC algorithms. The faulty link has been isolated from the non-faulty part of the network and the grid operation restored. The currents and voltages return to the pre-fault setpoints with respect to the new grid configuration.

7.3.3 Additional Fault Cases

Two additional fault cases are given at Appendix A. These include a P2P fault on a link connected to the switching busbar 12 (link 412) and a P2Gnd fault on a bipole dc link (link 12). These fault cases lead to new conclusions that are briefly presented in this subsection.

In the P2P fault case, dc relays 512 and 513 incorrectly discriminate the dc fault as internal. DCCBs 512 and 513 receive an opening order due to decision making of the CRCC criterion. Then, these DCCBs receive a reclosing order due to the voltage recovery criterion.

In the P2Gnd fault case at a bipole dc link, an overvoltage shift does not appear on the dc links. Therefore, overvoltage suppression operations are not required. In addition, only the

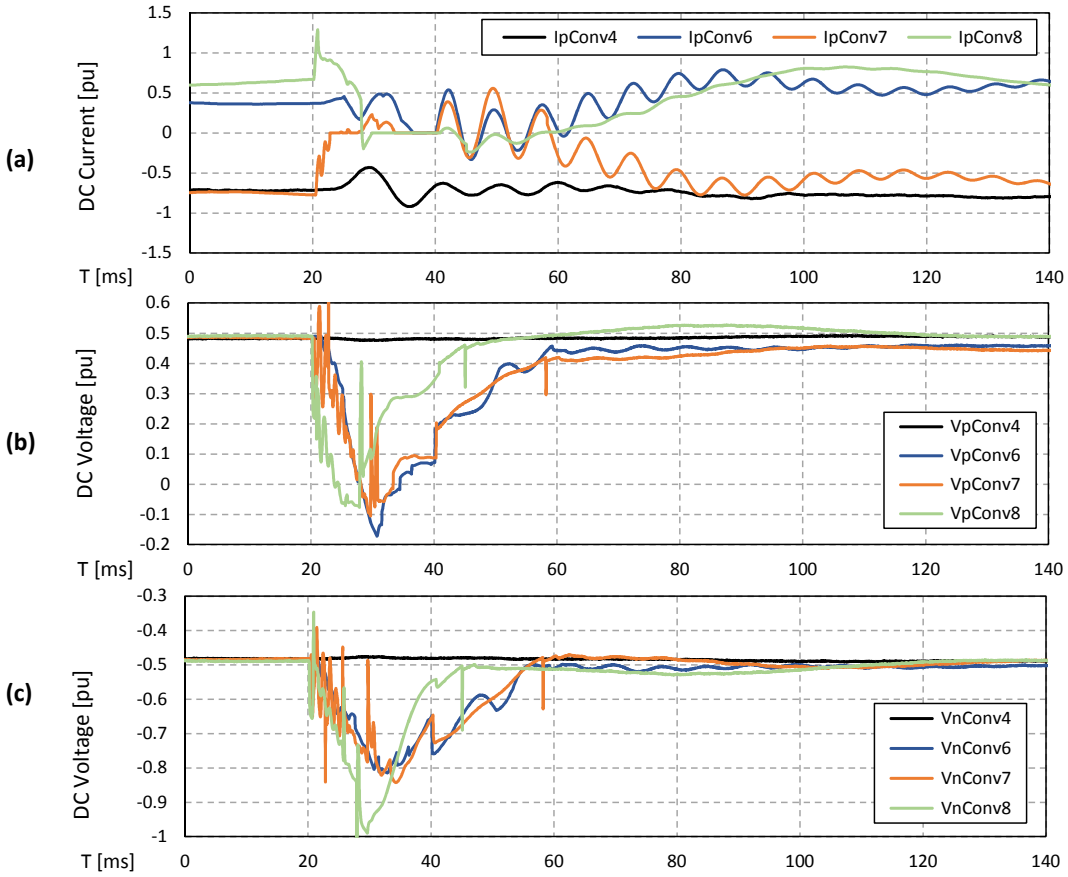

Fig. 7.17 Profile of (a) converter dc currents, (b) positive pole dc voltages and (c) negative pole dc voltages.

faulted pole of the faulted link is isolated. Therefore, the faulty link remains with 50% of transmission capacity available. This constitutes a main advantage of bipole configurations.

7.4 Summary

A protection strategy for MTDC grids equipped with DCCB was proposed in this chapter. The strategy is initiated with fault detection which leads to: (a) converter blocking, (b) fault discrimination, and (c) overvoltage and voltage imbalance operation, if necessary.

Converter blocking is required for self-protection of sensitive power electronics devices such as IGBTs and to interrupt the submodule's capacitive discharge to the dc fault. Fault discrimination leads fault clearance and isolation by appropriately ordering the opening of DCCBs classified as internal to the faulty link. The algorithms that lead to DCCB

classification are based on the sign of current derivative and CRCC criterion (introduced at Section 4.3). The combination of these algorithms supports a minimum-tripping protection strategy where typically only the DCCBs placed in the faulty link open. These algorithms are based on local measurements of dc current only which means that decision making is achieved in a timely manner. Lastly, overvoltage suppression is based on a discharging circuit that employs a limiting resistor and a low rating DCCB. This methodology is applied in the event of a P2Gnd fault on a monopole grid. Such a fault causes a voltage shift and overvoltage in one pole. Thus, the overvoltage should be quickly removed to avoid stress to the insulation of links. The discharge current is up to 1 kA which leads to the design of a low rating discharging DCCB. The overvoltage is suppressed in a few tens of milliseconds. This operation occurs in parallel with fault isolation and power restoration.

Simulation results describe the events for two fault cases that occur in the CIGRE 11-terminal dc system. This is a complex dc network that includes cables, OHLs, links composed of both cable and OHL sections, monopole converters, bipole converters and dc-dc transformers. Results show that typically only the DCCBs in the faulty link receive an opening order. This rate of success meets the requirements of the minimum-tripping protection philosophy. The protection strategy is robust to grid configuration, link type, dc fault type, and impedance (as long fault detection is achieved).

Chapter 8

Conclusions and Future Work

8.1 General Conclusions

DC protection is a major technical challenge in HVDC transmission systems. This thesis investigated protection algorithms and protection strategies for MTDC grids equipped with several fault clearance devices. The main contributions of this thesis include the CRCC fault discrimination algorithm, dc protection strategy for grids equipped with either ACCBs, FB converters or DCCBs, and overvoltage suppression algorithms for grids equipped with either ACCBs, FB converters or DCCBs.

8.1.1 Fault Discrimination Algorithms

This thesis was initiated with the objective to find discrimination algorithms for complex dc grids such as the 4-terminal and the CIGRE 11-terminal dc grid (described in Section 3.2 and 3.3). To meet this objective, a novel approach for the design of dc discrimination algorithms becomes necessary. Accordingly, this work focused on identifying patterns of dc fault currents that could be considered to design discrimination algorithms. The magnitude of the fault current should not be considered as it is very dependent on fault impedance, location and link type. Therefore, the research resulted in the development of the novel fault discrimination algorithm CRCC. This algorithm is based on the profile of transient waves generated after a dc fault and blocking of converters. The CRCC algorithm differs from

algorithms in the open literature in the way that, the magnitude of transient waves, or time difference between consecutive waves is not required.

With the CRCC discrimination algorithm, the faulty link is typically correctly identified within 2 ms. Therefore, the CRCC has an advantage against (a) link communication-based algorithms and (b) algorithms based on current/voltage derivative functions. The algorithms in (a) have an intrinsic link communication delay that might not be accepted for the protection of dc links. The algorithms in (b) are typically suitable for grids composed of dc cables and with large ratings of link end inductors. Therefore, their application is restricted in grids with OHLs and for grids where link end inductors may not be required (such as grids equipped with FB converter). On the other hand, the CRCC algorithm has been tested for a number of faults in cables, OHLs, low ratings of link end inductors, different impedances and locations. As a result, this thesis contributed with a fast dc fault discriminative algorithm that proved to be robust in many fault scenarios.

8.1.2 ACCB, Fault Blocking Converter and DCCB: A Comparison

The design of a protection strategy must take into consideration the technical restrictions of the devices that lead to dc fault current clearance. In this thesis, protection strategies are developed according to the technical limitations of three devices: ACCBs, FB converters and DCCBs. For interest, at the time of writing, ACCBs are in operation for the protection of dc grids, FB converters are commissioned, and DCCBs are in development/testing stage in academia and industry.

The selection of one device for dc protection as favourite in relation to other is dependent on technical and economic drivers for each project. Guidelines for the selection of ACCBs, FB converters or DCCBs to protect a dc grid should be based on acceptable outage time of a network, prospective acceptable dc current, power outage, ac grid disturbance and naturally, overall cost.

The usage of ACCBs for dc protection brings a very economical advantage in relation to other alternatives. The main drawbacks include the long interruption time of ACCBs, a temporary outage of the whole dc grid (hundreds of milliseconds to seconds) and prospective large dc fault currents.

The usage of FB converters for dc protection appears to be the safest solution as the dc fault currents start to be interrupted very quickly. The convert blocking action occurs with very small delays which limits the fault current magnitude to the overcurrent threshold (set as 1.2 p.u. in this thesis). Drawbacks include the operational power losses from the FB submodules which are relatively higher in comparison to HB submodules. The same argument is valid for the cost, as FB submodules will be more expensive than HB submodules. Lastly, temporary grid outage (a few tens of milliseconds) is necessary as all the FB converter must block to interrupt the ac infeed currents. In addition, fault isolation is performed by FDs, devices that have no appreciable current breaking capability and an operation delay assumed as 10 ms. Thus, a performance improvement of FDs could lead to a very small dc grid outage time.

The usage of DCCBs for dc protection should be considered in projects where costs are not a significant restriction. Although, at the moment, the cost of such a device suffers from lack of information in the literature. In terms of technical capabilities for dc protection, DCCBs are superior to ACCBs and to FB converters. DCCBs can selectively isolate the faulty link in a few milliseconds and dissipate fault energy. DCCBs may lead yet to a relatively large dc current magnitude as they are typically slower than the blocking action of FB converters.

The employ of ACCBs or FB converters should be limited to relatively small dc grids or to parts of a larger dc grid if DCCBs are used in tie connections. Therefore, the power outage would be relatively small in a way that the neighbouring ac grids would experience an acceptable power and frequency deviations.

8.1.3 Overvoltage and Voltage Imbalance Suppression Methods

Overvoltage appears with a P2Gnd fault on a monopole dc grid. P2Gnd faults are considered the most common type of fault while the monopole grid should be most used configuration in dc systems. These considerations are based knowing that, firstly P2Gnd faults are particularly incident on dc cables. These employ a metallic screening connected to ground that surrounds each pole, making easier to experience a P2Gnd fault instead of a P2P fault. Secondly, monopole grid configurations use one converter at each end and do not require a ground

return. Therefore, monopole grids are more economic than bipole grids which in turn, shall make the monopole as the favourable configuration in HVDC transmission.

Overvoltage and voltage imbalance suppression can be achieved with discharging circuits. Typically, these circuits are based on a discharging resistor and a switch (such as an FD or a DCCB).

In this thesis, an innovative approach to suppress overvoltage is proposed for grids with FB converters (described in Section 6.3). In this approach, hardware such as discharging resistors and switches are not required. Instead, the proposed algorithm takes advantage of the FB converter configuration to suppress overvoltage and voltage imbalance in a quick and safe manner. This is achieved with a temporary by-passed of FB submodules while the P2Gnd fault provides a voltage reference. There is no overcurrent flowing through FB submodules as these can be blocked to suspend the overvoltage suppression operation.

8.1.4 DC Protection Philosophy Comparison

Protection philosophies investigated in this thesis include the minimum and non-minimum opening approaches. In ac protection, only the ACCBs placed at the faulty link should open (*i.e.* minimum approach). In dc grid protection, the same approach should ideally be used. However, non-minimum approaches have proven to be a better solution for a number of protection strategies.

The dc protection strategy based on ACCB is designed on the non-minimum approach - all the FDs are required to open. This strategy has proven as more efficient than minimum approaches. It allowed a progressive recovery of the dc grid while in certain cases, part of the MTDC grid would be back to normal operation while the fault dc link is not completely isolated yet.

The DCCB based protection strategy is based on minimum approach. This should be a widely accepted approach for system operators or entities familiarised to ac protection. However, protection strategies such as Open Grid (see Section 2.5.4) proved to have practical advantages as it leads to a faster fault clearance, a smaller current magnitude at the interruption instant, and therefore a lower rating of DCCBs.

As a conclusion, there is no recommended philosophy for dc protection. Standardisation of dc protection issues is expected in the future to encourage the minimum tripping approach for dc systems, as in the case with ac systems.

8.2 Future Work

Recommendations for future work include:

1. Experimental validation of the developed discrimination algorithms.
   The application of the algorithms in practical dc relays would benefit if tests are performed with more realistic conditions which would include measurement devices, dc links and advanced converter models.

2. ACCB (or FB converter) based protection strategy with low rating DCCBs instead of FDs.
   Low rated DCCBs (*e.g.* 1 kA breaking capability) could replace FDs, devices with no appreciable current breaking capability. Hence, an hybrid methodology could reduce dc grid outage time, reduce energy not supplied while keeping the investment costs with a relatively small increase.

3. Mixed protection devices within one MTDC grid.
   DCCB in strategic locations of an MTDC grid may prove efficient to reduce costs while having an overall dc grid availability. Such DCCBs could be used to divide a larger MTDC grid into smaller sub-systems. Then, each sub-system would clear the dc fault (if internal) with the available protection devices. These could be ACCBs or FB converters. If the fault is external, a sub-system could continue operation with minimal disturbance. Advantages of mixed protection devices within an MTDC grid include (a) cost reduction as only DCCB is considered instead of a DCCB in each link and (b) increases availability as sub-systems of the dc grid continue their operation while the faulty sub-system clears the dc fault.

4. Optimisation of FB converter blocking action during a dc fault.
   The blocking of FB converter, *i.e.* removing the firing pulses of converters' IGBTs, leads to a quick current suppression. This is a simple approach that benefits a faster

link isolation by opening the FDs. However, during the converter blocking, the dc voltage becomes uncontrollable and experiences polarity oscillations that could cause stress on cable insulation. Therefore, the FB converter blocking operation could be replaced by a current and voltage control approach where both the current and voltage are driven to zero. Such a control is expected to take a longer time to clear dc fault currents although it might be beneficial to control dc fault voltage.

5. Investigation of temporary dc faults.
   HVDC systems with OHLs are subjected to temporary faults. Algorithms to discriminate temporary from permanent dc faults should be developed in order to increase the availability of dc links.

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Appendix A

Additional DC Fault Cases

The protection strategies in this thesis are supported by two fault cases in each chapter: a P2P and a P2Gnd fault case. These results lead to general conclusions about the performance and applicability of the protection strategies. However, the CIGRE 11-terminal dc grid has brought a number of challenges that were not considered with the 4-terminal dc grid. Hence, additional fault cases at specific locations at the CIGRE 11-terminal could bring new results. For this reason, two additional fault cases are given at the CIGRE 11-terminal grid while fault clearance is ensured by DCCBs.

Fig. A.1 illustrates the location of fault cases described in this Appendix. The first fault case is a P2P fault at link 412 which is a link connected to a busbar without a converter station (switching busbar). The fault occurs at the middle of the link 412 (*i.e.* 100 km from relays 412 and 124) and has a 100 Ω impedance. The second fault case is a P2Gnd fault in a bipole dc link. This fault occurs at link 12, immediately after relay 21 and has a 0.1 Ω impedance.

A.1 Fault Case at a Link Connected to a Switching Busbar

A P2P fault starts at link 412 at 20 ms. Consequences of the high impedance fault include voltage drop and overcurrent is a few neighbouring dc links.

Fig. A.2 illustrates the converter blocking actions which occur after fault detection at dc relays or at converter stations. Fault detection does not occur at a number of dc relays as the high impedance fault does not cause severe current or voltage disturbances.

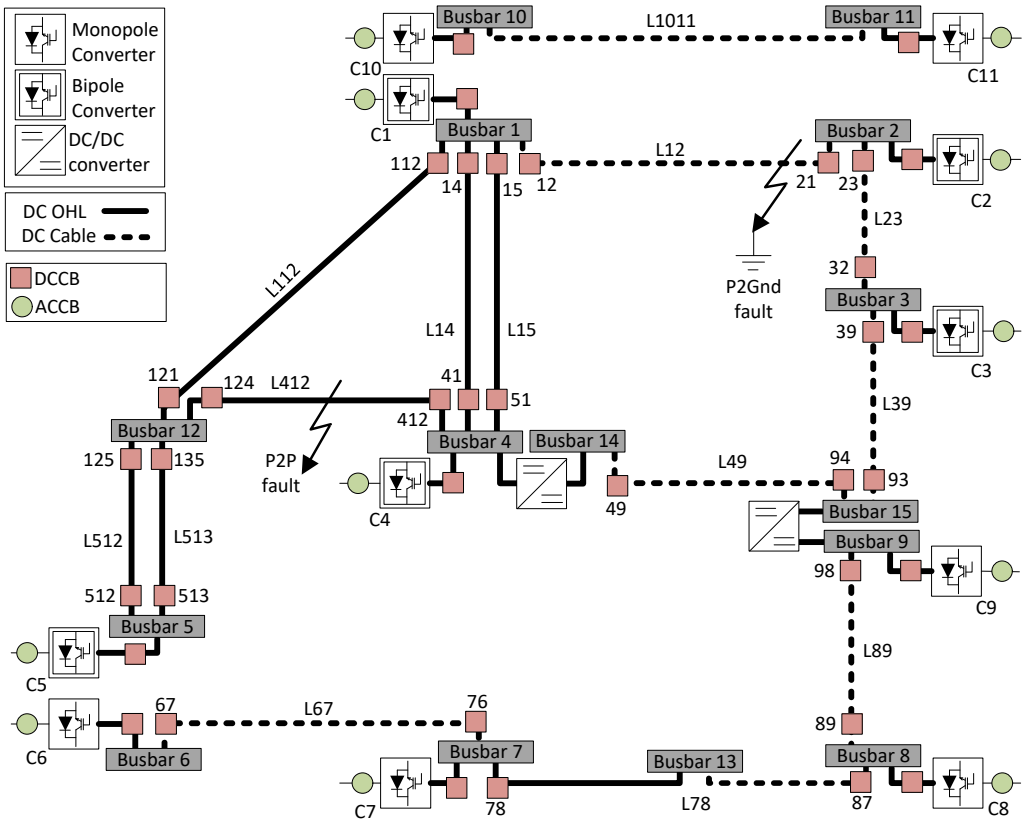

Fig. A.1 Location of the P2P and P2Gnd fault within the CIGRE 11-terminal dc grid.

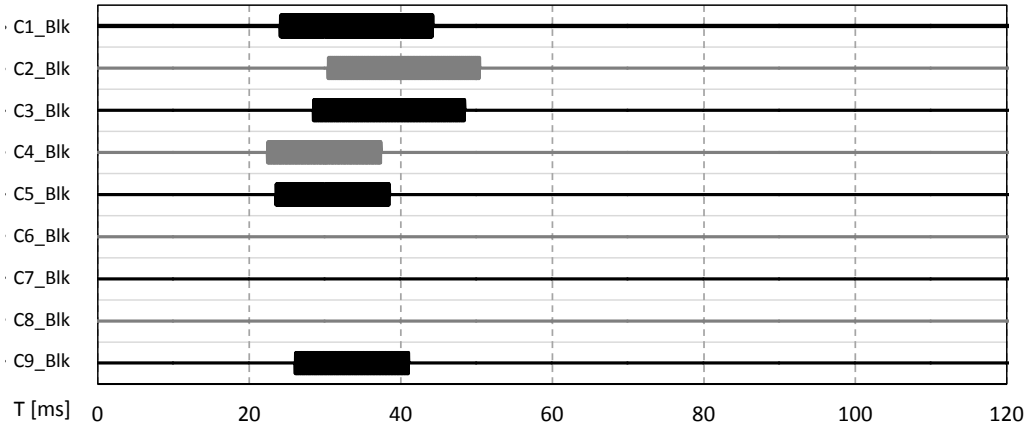

Fig. A.2 Converter blocking state.

The sign of current derivative and CRCC discrimination criteria (introduced in Section 4.3) are used to support DCCB opening decision making. Fig. A.3 illustrates data analysed by discrimination algorithms from a relay internal to the faulty link, relay 124. In Fig. A.3 (a), it is perceptible that dc fault current is increasing over time. This behaviour relates

to a positive sign of current derivative which is marked by signal 'Sdidt124' (in A.3 (c)). The CRCC criterion analyses the magnitudes of transient waves, being those marked as 'MaxInc$_1$24' and 'MaxRef124' (see Fig. A.3 (b)). As the magnitude of the incident wave is larger than the magnitude of the reflected waves, the fault is correctly classified as internal to link 412, as marked by 'CRCC124' (see Fig. A.3 (c)).

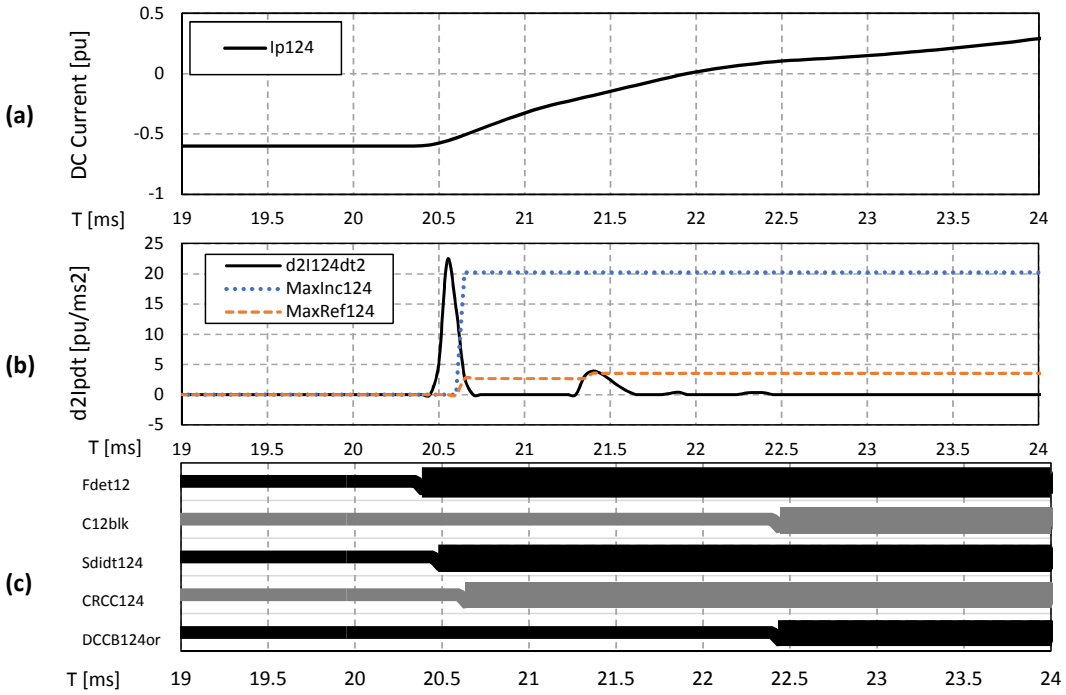

Fig. A.3 Data analysed by the discrimination algorithms in the internal dc relay 124. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

Fig. A.4 illustrates data analysed by discrimination algorithms from a relay 512 which is external to the faulty link. It should be noticed that the profile in Fig. A.4 (b) and Fig. A.3 (b) are very similar. The main difference of this fault case in comparison to the previously described fault cases, is that a dc relay is incorrectly discriminated as internal (relays 512 and 513 in this fault case). The discriminative signals for relay 512 are marked as 'Sdidt512' and 'CRCC512' which leads to opening of DCCB 512 (see 'DCCB512' in Fig. A.3 (c)). The incorrect decision making from the CRCC algorithm is related to the grid configuration and relay 512 location, which is placed downstream of a busbar without a converter station (switching busbar 12). Therefore, the transient waves at Fig.A.4 (b) are due to the dc fault

disturbance while disturbances due to upstream converter blocking (non-existent at busbar 12) are not generated.

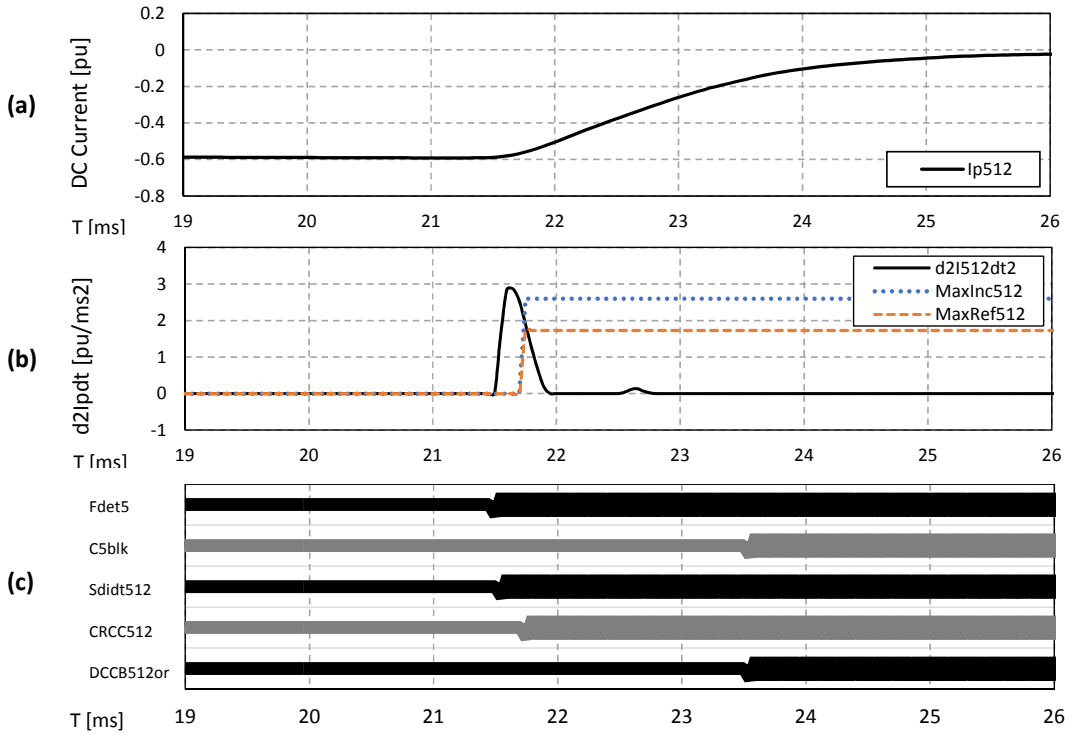

Fig. A.4 Data analysed by the discrimination algorithms in the external dc relay 512. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

Fig. A.5 illustrates the outage of links in CIGRE 11-terminal network. The DCCBs that receive an opening order are placed on the faulty link (DCCBs 412 and 124) and on the non-faulty links 512 and 513 (DCCBs 512 and 513). It should be noticed that the DCCBs in the faulty link are kept open. On the other hand, DCCBs 512 and 513 (placed on a non-faulty link) receive a reclosing order.

The reclosing order of DCCBs 512 and 513 is generated due to the discrimination criterion based on voltage recovery. Fig. A.6 shows the dc voltage at relay 412 (on the faulty link) and at the relay 512 (on a non-faulty link). It should be noticed that with the opening of the DCCBs, the voltage decays to zero on the faulty link as driven by the dc fault. In the non-faulty link, the dc voltage remains next to nominal values as links 512 and 513. This occurs because these links remain connected to the healthy part of the network (DCCBs

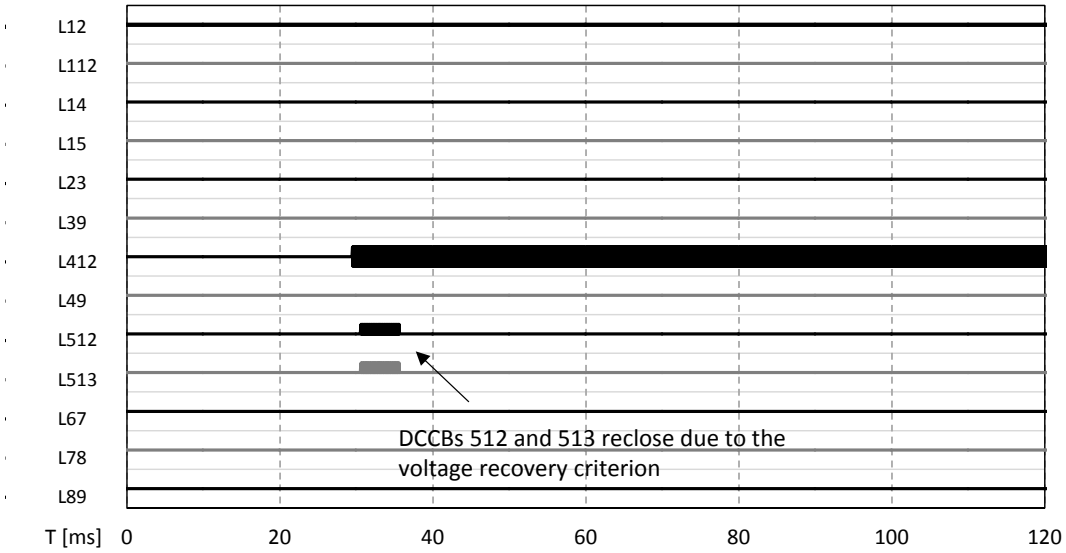

Fig. A.5 Link outage due to opening of link end DCCBs.

125 and 135 remain closed). Therefore, a voltage recovery criterion leads to the reclose of DCCBs 512 and 513. As a result, only the faulty link 412 remains isolated.

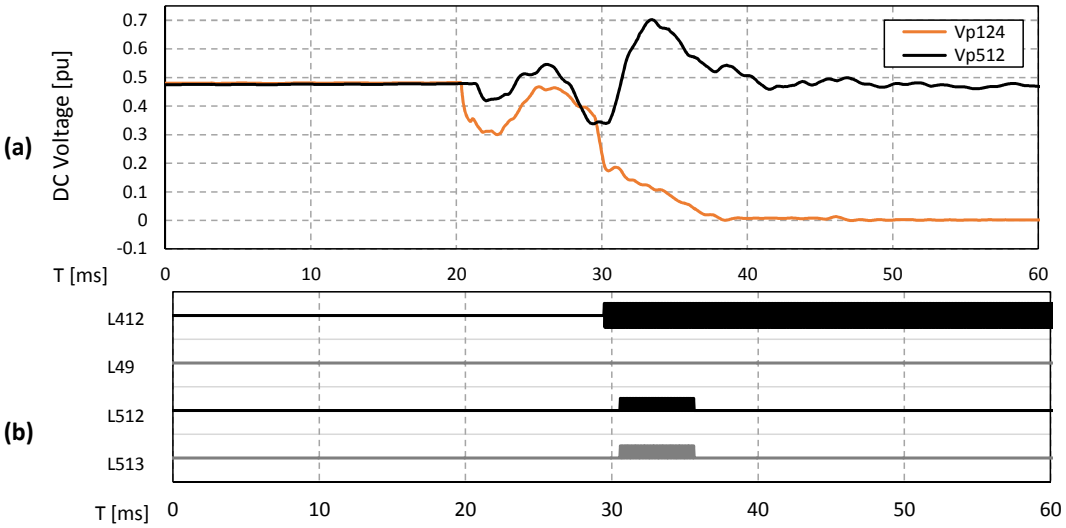

Fig. A.6 (a) DC voltage recovery and (b) outage of a few dc links.

A.2 Pole-to-Ground Fault Case at a Bipole dc Link

In the previous P2Gnd fault cases, faults were placed in monopole dc links (in Sections 5.3.2, 6.5.2, 7.3.2). In these cases, P2Gnd faults caused a voltage shift in the monopole network

and overvoltage. Then, algorithms were considered to suppress overvoltage and voltage imbalance.

In this Section, a P2Gnd fault occurs at a bipole dc link which is link 12 of the CIGRE 11-terminal dc grid. P2Gnd faults on bipole systems result in current and voltage behaviours similar to P2P faults, *i.e.* large currents and a voltage collapse is expected in the faulty pole. Fig. A.7 shows the dc voltage on positive and negative poles following the P2Gnd fault case at bipole link 12. It should be noticed that only the faulty positive pole voltage 'Vp12' collapses.

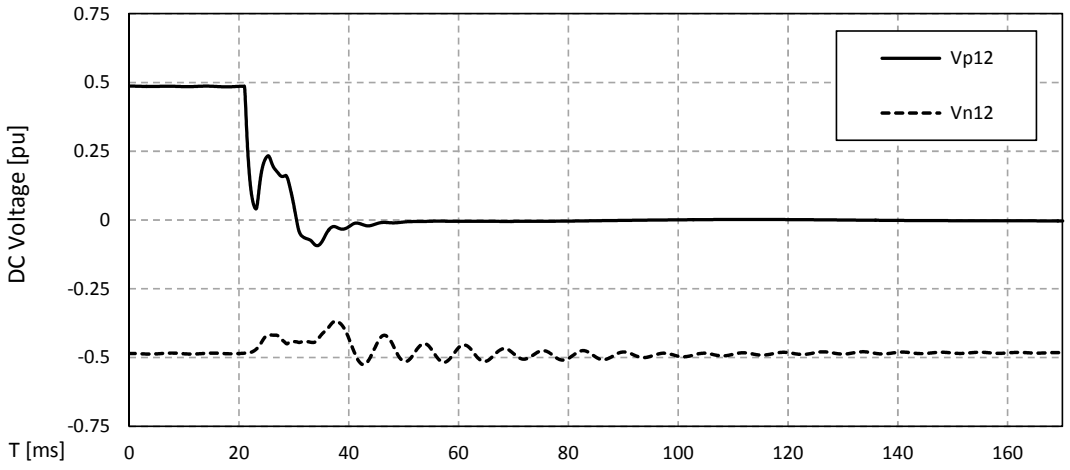

Fig. A.7 Voltage at the faulty bipole dc link.

P2Gnd faults on bipole dc links also lead to a partial outage of the faulty dc link, *i.e.* the faulty pole must be isolated while the non-faulty pole can remain connected to the network. This is one of the main advantages of bipole dc networks where P2Gnd faults cause unavailability of only 50% of the faulty link. Therefore, as the simulated P2Gnd fault occurs at the positive pole of link 12, the DCCBs at the positive pole of link 12 should be opened while the DCCBs at the negative pole of link 12 should be closed.

Fig. A.8 illustrates the blocking of converters at the dc network. These operations occur following fault detection at dc relays or at converter stations.

Fault discrimination is initiated with detection of a disturbance in the system. In this fault case, dc relays 12 and 21 are classified as internal to the faulty link. Hence, these receive opening orders.

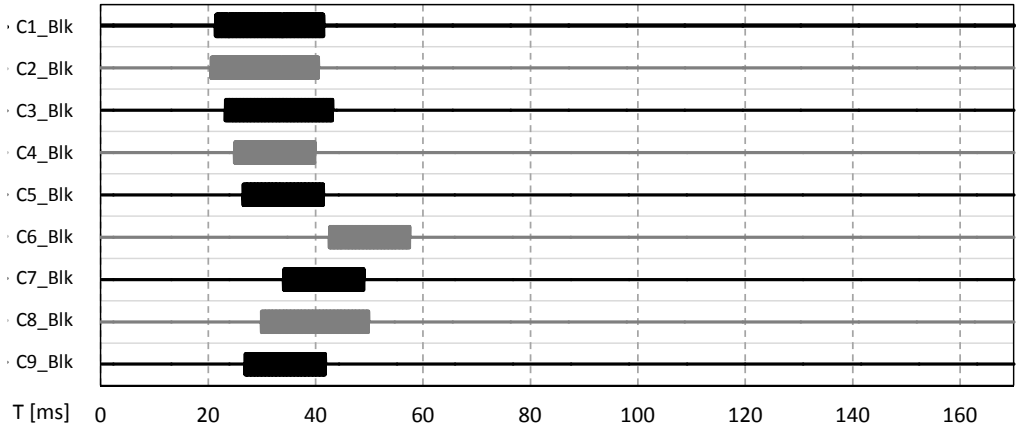

Fig. A.8 Converter blocking state.

Fig. A.9 shows protection data that concerns to dc relay 21 which is internal to the faulty link. It should be noticed that the fault is discriminated as internal 'CRCC21' and DCCB 21 receives an opening order 'DCCB21or'.

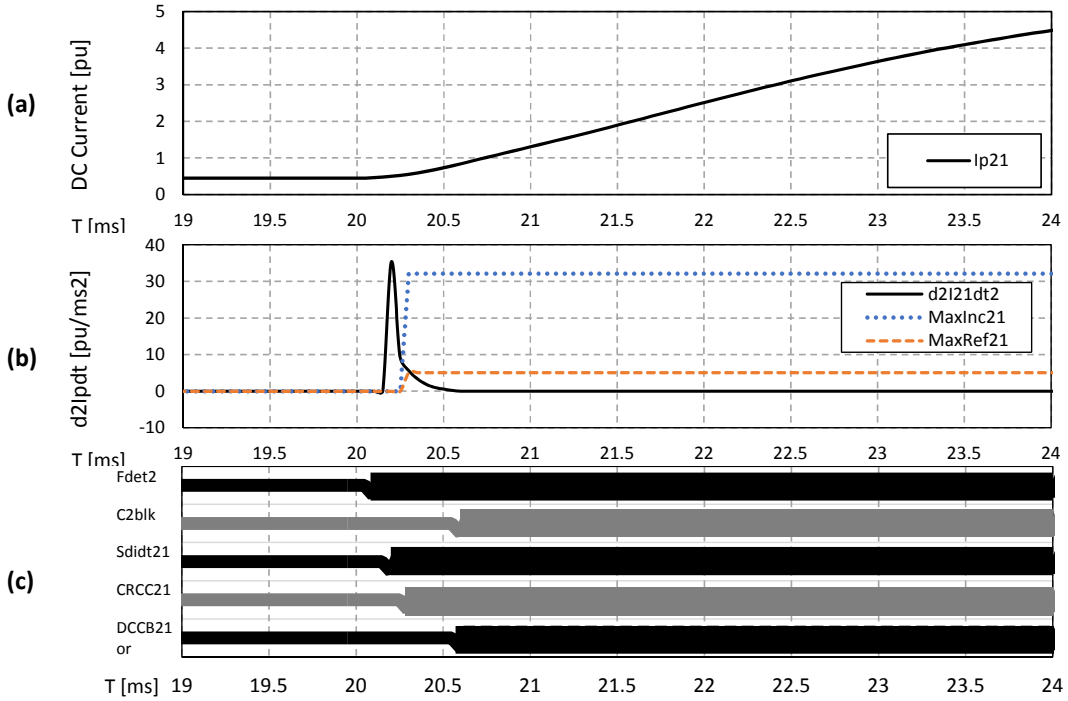

Fig. A.9 Data analysed by the discrimination algorithms in the internal dc relay 21. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

Fig. A.10 illustrates protection data associated with relay 32 which is external to the faulty link. It should be noticed that the fault is discriminated as external 'CRCC32', a

decision that occurs at the blocking of converter C3 ('C3blk'). DCCB 32 is ordered to remain closed, as marked by the thin line of 'DCCB32or'.

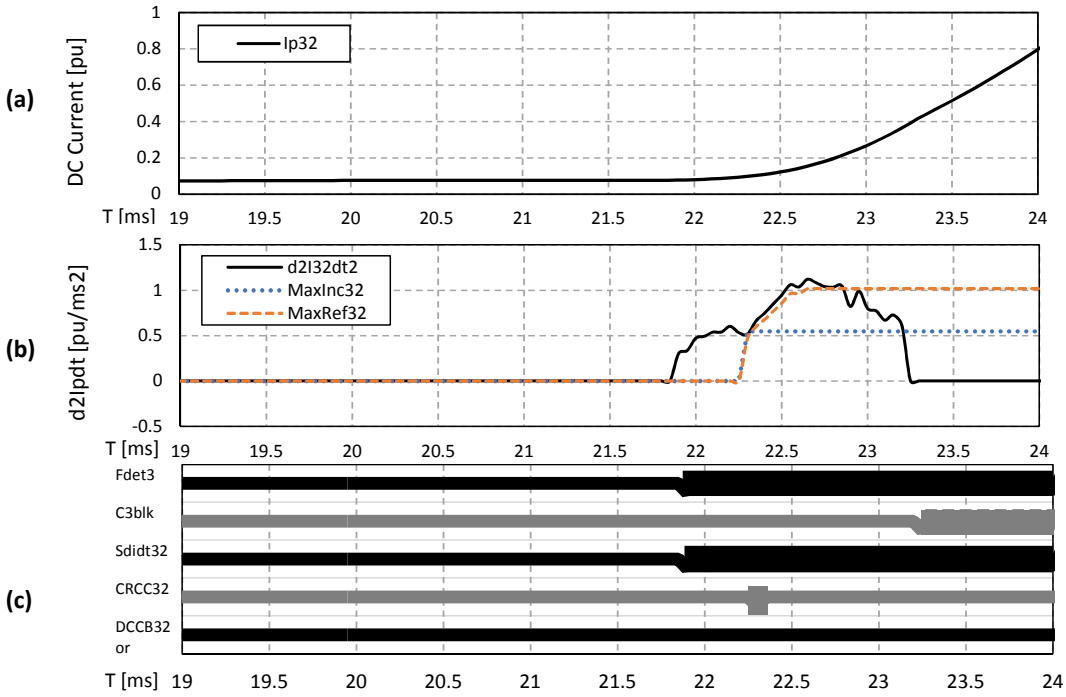

Fig. A.10 Data analysed by the discrimination algorithms in the external dc relay 32. View of (a) dc current, (b) second derivative of dc current together with MaxInc and MaxRef of CRCC criterion, and (c) protection signals.

Fig. A.11 illustrates the outage of dc links which is given by the opening state of DCCBs at both ends of a link. DCCBs 12 and 21 have been discriminated as internal to the faulty link. As a consequence, only these receive an open order while the other DCCBs remain in the closed state. However, as the fault only affects the positive pole, the negative pole should be re-connected to the grid. Consequently, the negative pole DCCBs 12 and 21 receive an reclosing order. The state of DCCBs closed at the positive pole and open at the negative pole is marked by the diagonal strips in 'L12' at Fig. A.11.

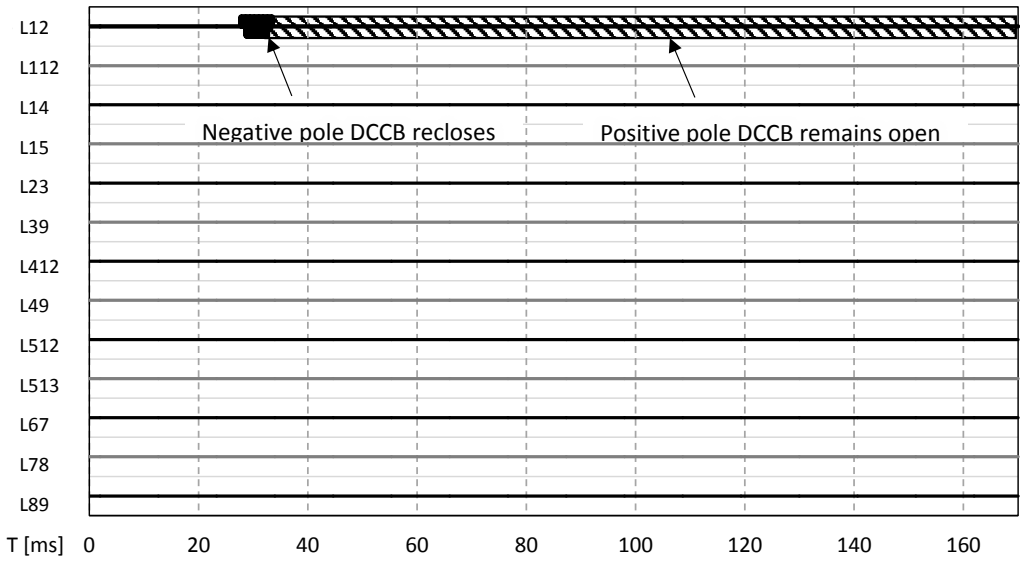

Fig. A.11 DC link outage due to DCCB opening.

DC current and voltage profiles are illustrated in Fig. A.12 for a few dc links. It should be noticed that the positive fault current 'Ip12' (see Fig. A.12 (a)) is zero while the negative pole current 'In12' (see Fig. A.12 (b)) is different from zero. Similarly, the positive pole voltage 'Vp12' (in Fig. A.12 (c)) is zero while the negative pole current 'Vn12' (in Fig. A.12 (d)) is different from zero. These values are due to the open state of positive pole DCCB and close state of negative pole DCCB.

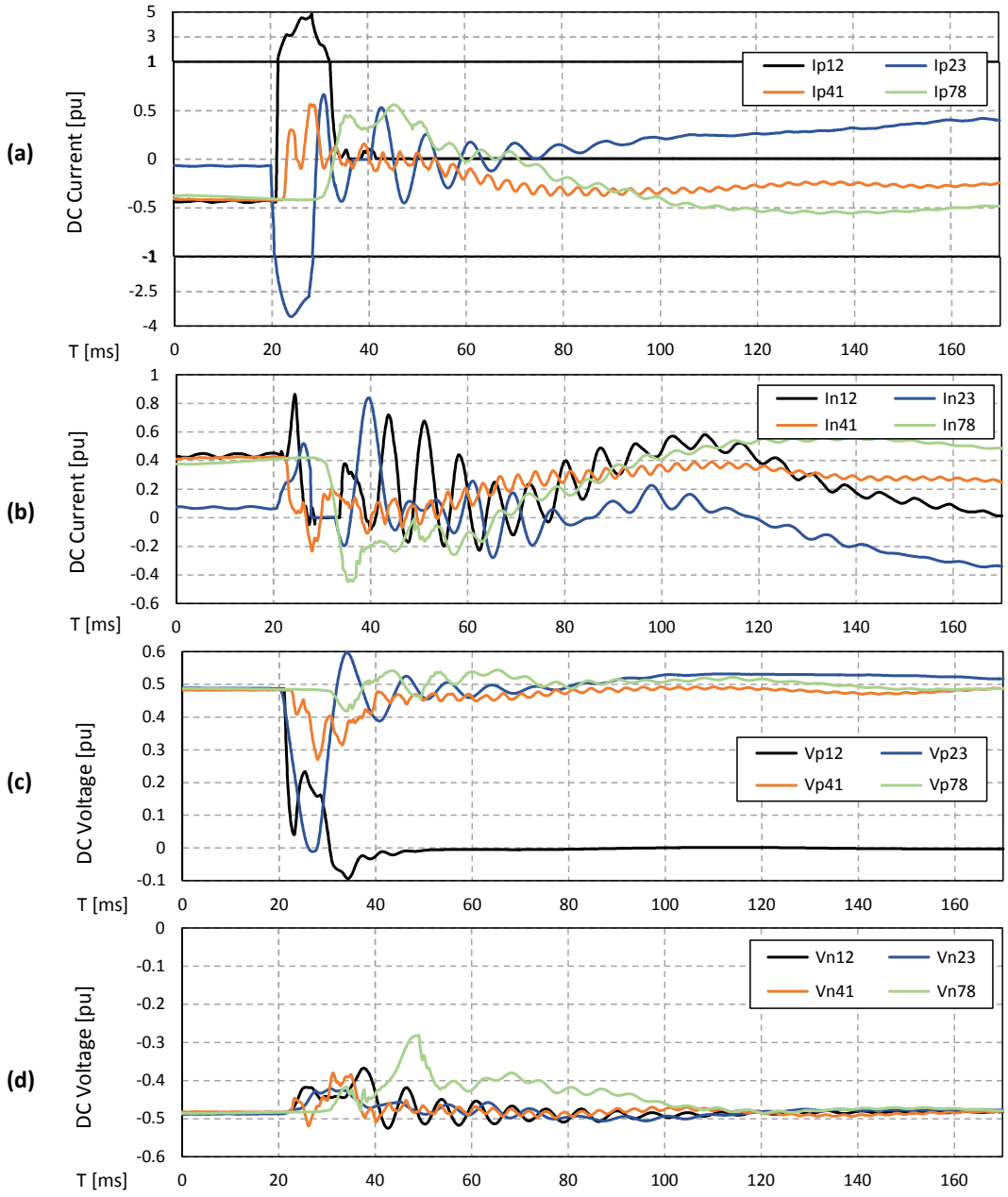

Fig. A.12 Profile of (a) converter dc currents, (b) positive pole dc voltages and (c) negative pole dc voltages.

Ultimately, the dc fault has been correctly discriminated and the faulty pole of the link 12 has been isolated from the non-faulty part of the network. Therefore, the P2Gnd fault at the bipole link 12 caused an outage of 50% capacity of such a link. The currents and voltages return to the pre-fault setpoints, with respect to the new grid configuration.