THE PROTECTION AND INTERCONNECTION OF HVDC GRIDS

Thesis submitted for the Degree of Doctor of Philosophy

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ABSTRACT

It is cost-effective to construct a High Voltage Direct Current (HVDC) grid via interconnecting existing HVDCs. The grid protection and the interconnection between HVDCs are studied in the thesis.

The future HVDC grid will be protected via the hybrid HVDC circuit breakers due to their high interrupting speed and low conduction losses. The hybrid DC circuit breakers have to be installed at each line end to fulfil the requirement of the grid protection. The overall cost of the breakers used in a HVDC grid will be extremely high as each breaker contains a large number of semiconductor switches. The research question in this part is how to reduce the cost of the hybrid DC circuit breakers. The novel interlink hybrid HVDC circuit breakers based on the concept of sharing main breaker branch will be proposed to reduce the size of the main breaker branch. An alternative method through coordination of converters and hybrid HVDC circuits breakers will be proposed to reduce the current rating of the breaker.

Most of the commissioned HVDC projects are point-to-point Line Commutated Converter (LCC) HVDCs. The interconnection of LCC-HVDCs will achieve the benefits of the grid operation, such as highly efficient and flexible power transportation, and high security of power transportation. However, benefits of the interconnection are hindered by the disadvantages of the LCC-HVDC. The first one is that a LCC-HVDC has to reverse its voltage polarity in order to reverse its power. The second one is that a LCC-HVDC is at risk of the commutation failure, which will cause a DC fault when a commutation failure occurs. The research question in this part is how to achieve the interconnection of LCC-HVDCs with the benefits of the grid operation. Interconnection of LCC-HVDCs with the capability of power reversal and commutation failure mitigation will be studied, and the corresponding controls for the interconnection system will be proposes.

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LIST OF ABBREVIATIONS

AC	Alternate Current
AC-CB	AC Circuit Breaker
AFAC	Advancing Fire Angle Control
CF	Commutation Failure
CFII	Commutation Failure Immunity Index
CFMC	Commutation Failure Mitigation Control
CFP	Commutation Failure Prediction
CTL	Cascaded Two-level Converter
CLI	Current limiting inductor
DC	Direct Current
DCCRC	DC Current Reduction Control
DC-CB	DC Circuit Breaker
HCB	Hybrid DC circuit breaker
HB	Half Bridge
HVAC	High Voltage Alternate Current
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-commutated Thyristor
IHCB	Interlink Hybrid DC circuit breaker
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
LCS	Load Commutation Switch
MB	Main Breaker
MDC	DC/AC/DC Converter
MI	Mass Impregnated
MMC	Modular Multi-Level Converter
MOV	Metal Oxide Varistor
MTDC	Multi-terminal High Voltage Direct Current
NLM	Nearest Level Modulation
OHL	Overhead Line
P2P	Point To Point
PI	Proportional Integral

PLL	Phase Locked Loop
PS-PWM	Phase Shift Modulation
PWM	Pulse Width Modulation
RCB	Residual Circuit Breaker
SCR	Short Circuit Ratio
SM	Submodules
STATCOM	Static Synchronous Compensator
TSO	Transmission System Operator
UHVDC	Ultra-high Voltage Direct Current
UFD	Ultrafast Disconnector
VSC	Voltage Source Converter
WF	Wind Farm

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CHAPTER 1 HVDC GRID DEVELOPMENT

The global warming poses a fundamental threat to the environment, species, and humans. One main source causing the global warming is the power plant using fossil fuel. To reduce the carbon emission, the development of renewable energy sources is encouraged to replace the fossil energy sources gradually. Many countries have proposed a roadmap to increase the proportion of the electricity from the renewable energy. Take the EU as an example, at least 40% electricity will be generated from renewable energy source up to 2050 [1]. Rich and continuous renewable energies are normally available in remote locations. In the EU, the rich offshore wind power sources located on the North Sea and Baltic sea. The solar power of east Middle and North Africa can be exported to the EU countries. In China, the renewable energy in the west has great potential to be consumed by eastern and southern countries. In the US, the rich wind power and solar power locating on Great Plain can be developed for the western and eastern load centres. The High voltage direct current (HVDC) technology is considered to be the proper solution for the electricity transportation.

1.1 **Why HVDC technology**

The AC technology has proved very effective in the generation and distribution of electrical energy. However, for the long-distance and bulk-power transmission, HVDC is more efficient and economical.

An HVDC link consists of a converter station, that converts the AC voltage of the conventional power grid into DC voltage, a transmission line, and another converter station on the other end, where the voltage is converted back into AC. The advantages of the HVDC transmission over the AC transmission are shown below:

1.1.1 Lower investment cost

The cost of an HVDC transmission line is lower than an AC transmission line at the same capacity. the cost of the converter should be added to the cost of an HVDC link. For long-distance electricity transmission, the HVDC transmission is still more cost-effective than the AC transmission, the break-event distances in terms of the cable link and the overhead line link are shown in Fig. 1.2.

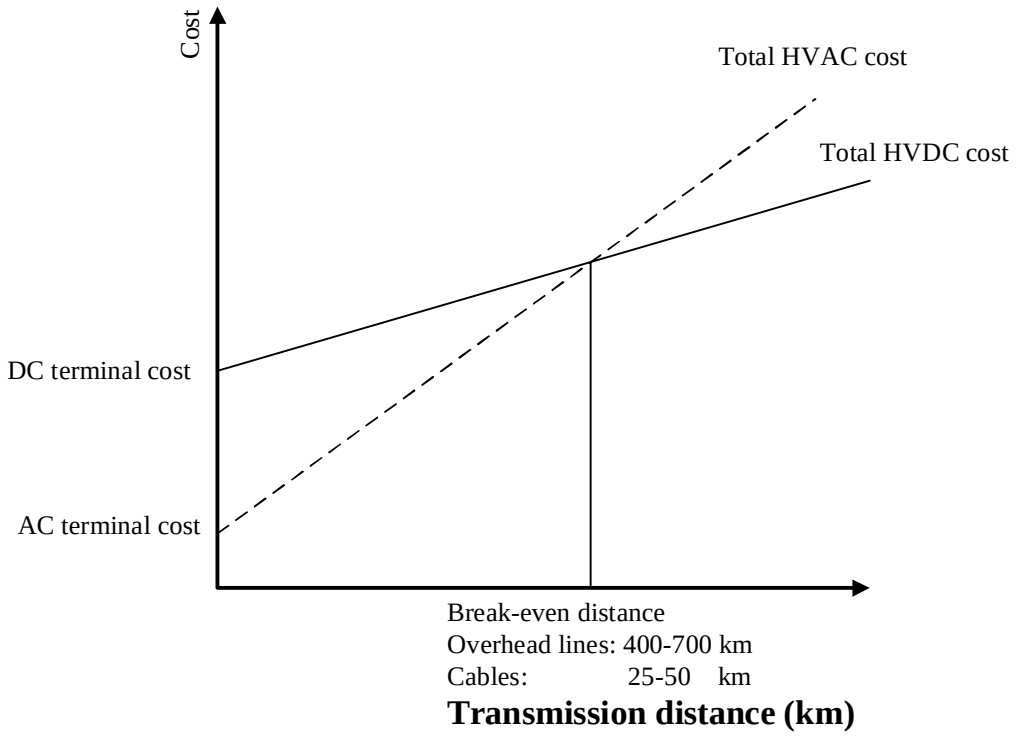


Fig. 1-1 Total cost for an AC and HVDC solution according to the transmission distance [2]

1.1.2 Lower loss

The losses of HVDC transmission lines are lower than AC transmission lines at the same capacity. Adding the converter loss typically is 0.6%-1% depending on the types of the HVDC technology, the total loss of an HVDC link is still lower than the pure AC transmission line when the transmission distance is beyond a certain distance. A side-by-side loss comparison of the AC transmission and the HVDC transmission using overhead lines is shown in Fig. 1-1. The HVDC cable losses are also lower than the AC cables.

1.1.3 Ability of long-distance connection

HVDC is the only option when the cable link is over 80 km. For an AC cable, the reactive power flow due to the large cable capacitance will limit the transmission distance. little AC electricity is delivered when the transmission distance is over 80 km. There are no technical limits to the potential length of an HVDC cable. The long-distance connection ability of the HVDC cable link promotes the development of the offshore wind energy, where the conventional AC transmission cannot reach.

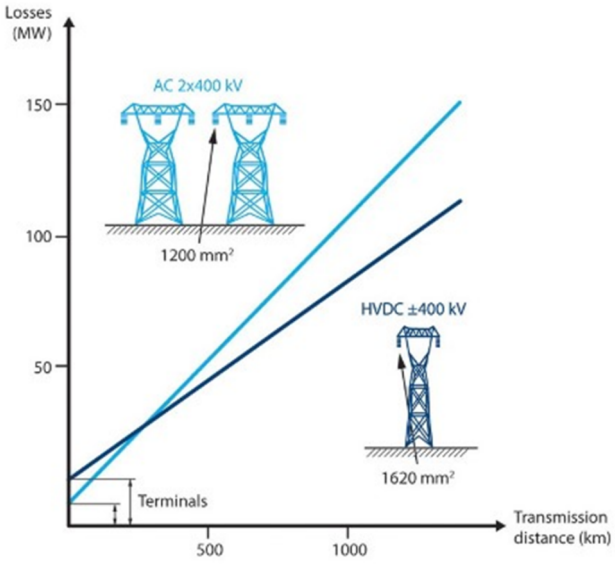


Fig. 1-2 The loss of the AC transmission and HVDC transmission using overhead lines [3]

1.1.4 Reduced right-of-way

Generally, an HVDC link has two poles, and each pole is comparable to an AC three-phase line. Therefore, the HVDC link using overhead lines requires less space and has less environmental impact. An example is shown in Fig. 1-3. Top lines are two 3000MW HVDC bipolar overhead lines at ±500 kV. To transport the same amount of the power, five AC overhead lines are needed at 500 kV.

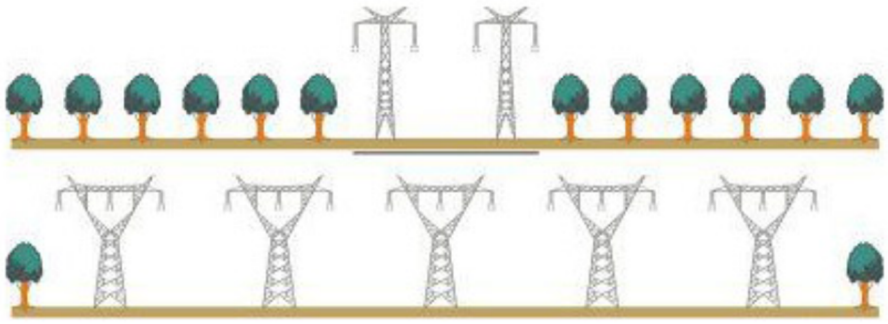


Fig. 1-3 The space requirement of AC and HVDC transmission [4]

1.1.5 Operation support from converter

HVDC converters enable secure and stable asynchronous interconnection of AC systems. The power can be transported in both directions under the control of the converter without disturbing the AC systems. The HVDC link will not contribute to the short-circuit currents of the interconnected AC system, which avoids the possible enhancement of the current ratings of AC protect devices. Normal operation of the AC system is maintained even a fault occurs on the HVDC lines and the other interconnected AC system. In many cases, the converter can improve the performance of AC networks. Additional control functions including the reactive power compensation, constant frequency control etc, can enhance the safe operation of the AC systems.

1.2 **Why HVDC grids**

The substantial growth in renewable energy generation demands an expansion of existing power system. The HVDC will be the backbone of power transmission system over a long distance. An overlayed pan-Europe Supergrid using HVDC technology is undertaking. And finally, the Supergrid will connect the whole of Europe, North African and the Middle East to allow sharing the hydro, wind, and solar resources.

An HVDC grid is a multi-terminal HVDC system to interconnect multiple AC networks together. Multiple power sources and load centres will be integrated into one HVDC grid. The power flow in the HVDC grid is highly flexible and each load can be supported by any sources.

1.2.1 Highly efficient power transmission

Each HVDC link can only interconnect two AC systems. To achieve the power exchange among multiple AC systems, the power conversion between AC and DC is needed many times in HVDC links system. The power losses of the conversion are high. For example, if AC system A is requested to transport the power to AC system C, the power has to be transferred from DC to AC and then back to DC at AC system B, see Fig. 1-4. The power exchange among the AC systems can be achieved via the HVDC grid directly, only two times of AC/DC power conversion are requested and the power losses of the conversion are relatively lower.

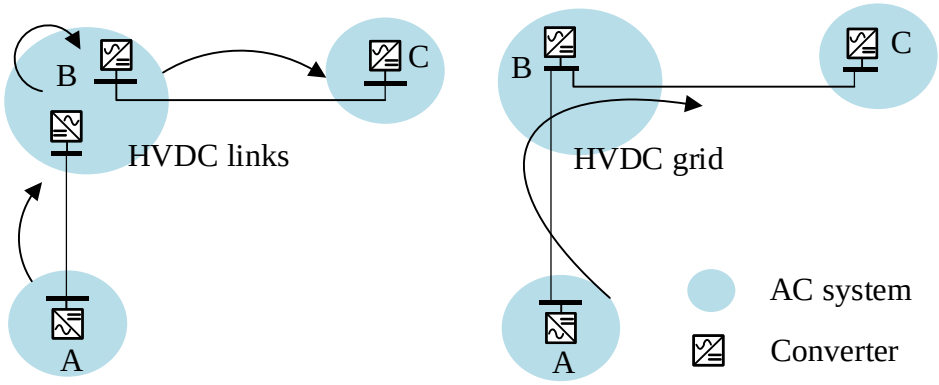


Fig. 1-4 HVDC links and HVDC grid

1.2.2 Less number of converters

Comparing to the individual HVDC links, an HVDC grid interconnecting same number of AC systems may reduce the number of the converters. As shown in Fig. 1-4, The number of converters locating on the same AC system B can be reduced to one by using the HVDC grid.

1.2.3 Smoothing the fluctuation of renewable energy

A generation outputs of some of the renewable energy are variable and unpredictable, which may not track the demand of the load. The HVDC grid allows integrating the controllable power source such hydropower to compensate the fluctuation of the renewable energy. A constant and stable power transportation is maintained for the connected load centres.

1.2.4 Potential for high reliability

The HVDC grid has the potential to contain the high reliability. Additional transmission lines can be added in the HVDC grid to provide an alternative path for power flow. When a line fault occurred, the power can still be transported to the desired AC systems via the alternative transmission line as shown in Fig. 1-5.

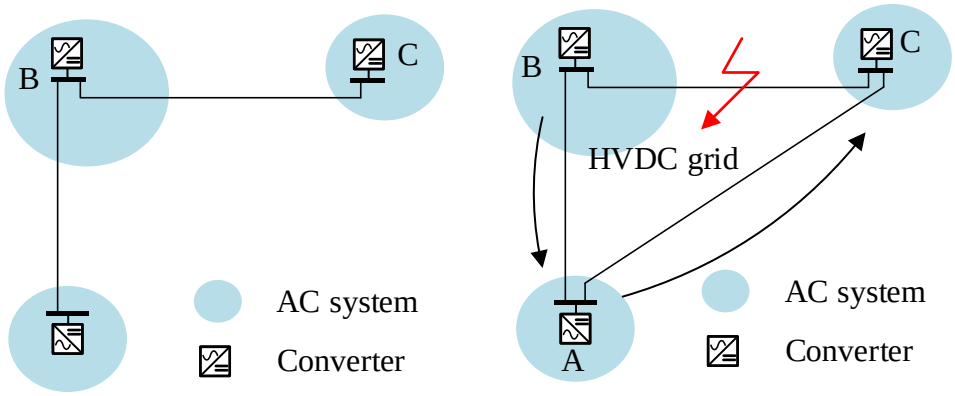


Fig. 1-5 Different topologies of the HVDC grid

1.3 HVDC development

1.3.1 Europe

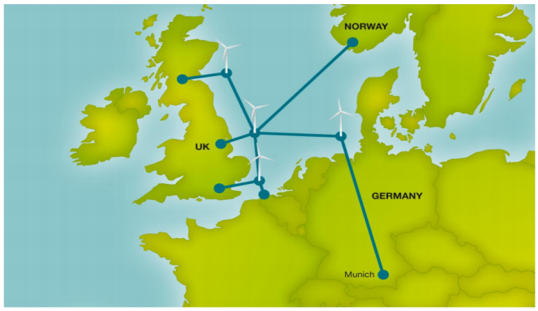
In 2010, an EU roadmap toward a prosperous and low carbon Europe by 2050 [1], adopted by the European Commission, emphasises that the power sector is one of the cornerstones of reaching the 80% greenhouse gas reduction target by 2050 and will be decarbonized at least 95%. The solution is to develop the low/zero carbon generation technologies including fossil fuel with carbon capture and storage, nuclear, and renewable energy sources. The traditional fossil fuel plant will be retired gradually. The proportion of the electricity from the renewable energy sources will be 40% to 80% by 2050 depending on the proposed pathways. The European Wind Energy Association [5] points out that 320 GW of wind energy capacity expects to be installed in the EU in 2030, which will fulfil 24.4% of the EU's electricity demand.

The massive renewable energies are normally in remote locations and distributed unevenly among the European countries, such as wind power in the North Sea and Baltic Sea, the solar power around the Mediterranean Sea. A continental Supergrid will be essential to interconnect the networks locating on individual countries and provide the access for them to renewable energy sources. The renewable energy will be shared among European countries tied on the Supergrid and therefore achieve their specific greenhouse gas reduction targets. The cross-border electricity trading will be enhanced. The Supergrid will promote the presence of one European electricity market. The potential benefits of the Supergrid are shown below:

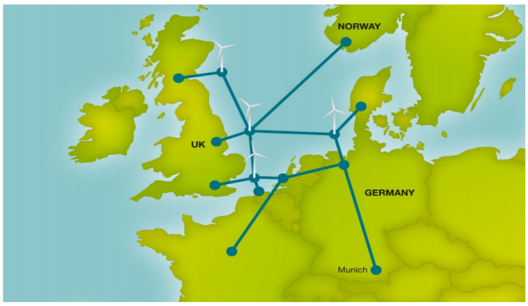
- Connect some remote renewable sources, which cannot be reached by traditional ac systems in an economic way.
- Compensate the fluctuation of renewable energy sources.
- Increase the grid security and security of supply.
- Reduce the congestion in existing power system.

The construction of the Supergrid will wake a long period. It is built from the North Sea and then will be expanded into the whole Europe The Friends of the Supergrid categorizes the whole process of the construction into 3 phases and their brief descriptions are drawn in Fig.1-6. Phase 1 is from 2015 to 2020. During this period, the interconnections will be achieved among the wind generation clusters Firth of Forth, Dogger Bank and Norfolk Bank located on the east coast of the UK, the German and Belgian North Sea clusters, and Norwegian hydropower. The power will be delivered to the existing power systems at the Glasgow, Hull and London of the UK, Zeebrugge of the Belgium, and the south of German. The phase 2 will continue the interconnection process in Phase 1 from 2020 to 2025. The phase will start after 2025, the Supergrid will be expanded to the rest of the Europe and will allow the integration of the solar power around the Mediterranean Sea locating on the Middle East and North Africa.

The HVDC technology will be the backbone of the Supergrid due to its long-distance and bulk-power transmission capability. The voltage source converter HVDC (VSC-HVDC) will the main HVDC technology applied in the Supergrid due to its capabilities of flexible power transmission in a DC grid, connection to a non-source AC grid. To support the development of the Supergrid, the technical advances in the HVDC technology are also demanded. A technical roadmap of the HVDC technology for the Supergrid is proposed in [8] and is summarised in Table 1-1. Under the trend of the Supergrid development, HVDC development schemes in many European countries have been proposed, which are introduced below.



(a) Phase 1 of Supergrod



(b) Phase 2 of Supergrid

(c) Phase 3 of Supergrid

Fig. 1-6 The progress of the Supergrid construction[6]

Table 1-1 A technical roadmap of the HVDC technology for the Supergrid [8]

2012-2015 Preparation Phase	2015-2020 Phase 1	2020-2025 Phase 2	After 2025 Phase 3
Progressive shift from LCC-HVDC to VSC-HVDC HVDC links to offshore wind farms in Germany Embedded HVDC links within synchronous grids	Evacuation of remote renewable energy sources	Increased interconnectivity in line with EU target of 10% of generation capacity	Aggregation of the disparate HVDC schemes Coordination by ENTSO-E and ACER
Converter			
Increased power rating for VSC (1000 MV at 320 kV)	Development of DC/DC converter Increased power rating of VSC (1600 MV at 320 kV to 2000 MW at 500 kV)	Demonstrator DC/DC converters Bipolar Schemes of 2500 MW by 600 kV	Deployment of DC/DC converters
Cables			
Mass impregnated paper cable > 500 kV developed Extruded HVDC cable 320 kV 600 kV mass impregnated paper cables and polypropylene laminated paper cables developed	Mass impregnated paper cable > 500 kV in operation Extruded HVDC cable > 320 kV in operation 600 kV mass impregnated paper cables and polypropylene laminated paper cables in operation	Further development of Mass impregnated paper cable Extruded cable in operation at 500 kV Further development of mass impregnated paper cables and polypropylene laminated paper cables	Extruded cable development > 525 kV Mass impregnated paper cables and polypropylene laminated paper cables > 600 kV New cable system development to 800 kV
Overhead lines			
Up 800 kV overhead lines in operation	1100 kV overhead lines in planning	Deployment of new DC overhead lines	
Multi-terminal HVDC			
Radial multi-terminal HVDC in operation	Multi-terminal enabled schemes enter service	Meshed multi-terminal VSC-HVDC systems in operation	
Circuit breakers			
Development of the DC circuit breaker	Prototype test of DC circuit breaker	Deployment of DC circuit breakers	
Control and protection systems			
	Hierarchical control architecture for integrated AC and DC grid in Europe demonstrated	Deployment of grid control architecture	

1.3.1.1 The Middle East and North Africa

To transport the solar power from the Middle East and North Africa back to Europe load centres, three trans-Mediterranean power transmission corridors, as shown in Fig. will be built to connect to the Supergrid during 2020-2030. The western corridor is from Morocco and Algeria across the Iberian Peninsula up to France. The Central corridor from Algeria, Tunisia and Libya across Italy to its Northern neighbours. The Eastern corridor is from Egypt and the Middle East across Turkey to the South-Eastern countries of the EU.

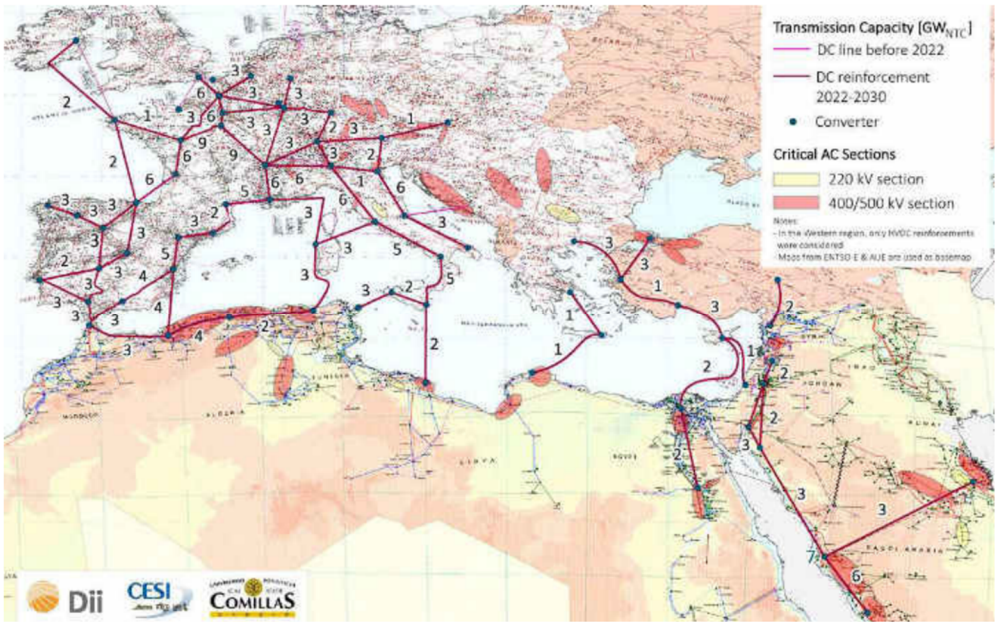


Fig. 1-7 Interconnect among the Middle East, the North Africa and the Europe [7]

1.3.1.1 UK

In the UK, the Western HVDC link [9] using line commutated converter HVDC (LCC-HVDC) technology is expected to put into operation in the 4th quarter of 2017. The renewable energy of Scotland is transported to the load centres of England and Wales through this link. The UK plans to construct multiple cross-border HVDC links as shown in Fig. 1-8 to enhance the grid interconnections with other European countries, which will increase the availability of the power and security of the power supply. Currently, four HVDC links using line commutated converter HVDC (LCC-HVDC) technology are in operation and connect to the France, Ireland,

Northern Ireland and the Netherlands. Eight more HVDC links using VSC-HVDC technology will be constructed, and the detail information about these cross-border HVDC links are summarised in Table 1-2.

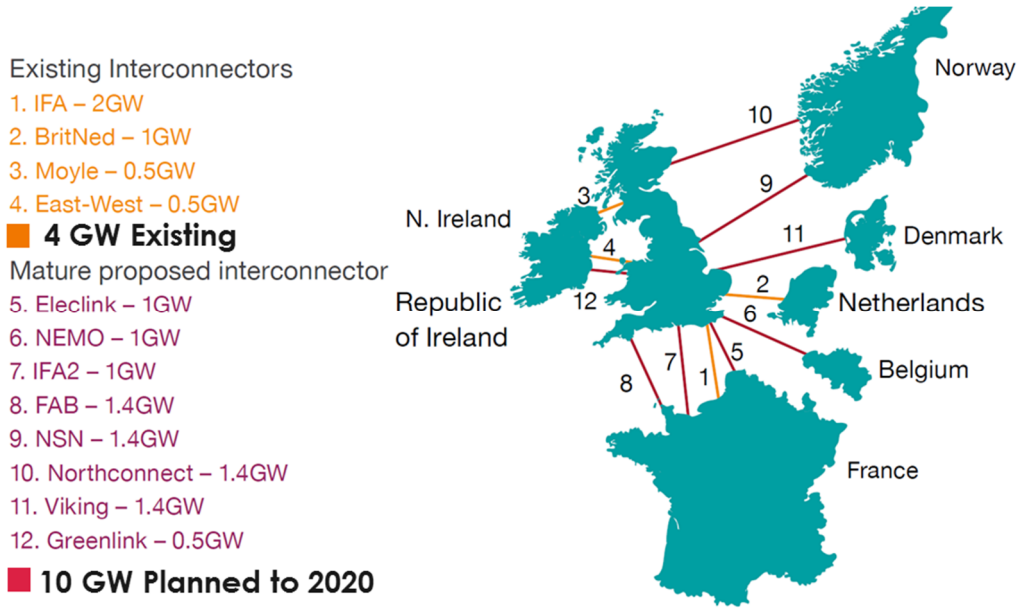


Fig. 1-8 UK HVDC interconnectors

Table 1-2 Information of UK interconnectors

Name	Interconnected country	Commissioned year	HVDC types	Transmission Distance (km)	Voltage (kV)	Power (MW)
IFA	France	1986	LCC	70	± 270	2000
Moyle	Northern Ireland	2001	LCC	63.5	± 250	500
BritNed	The Netherlands	2011	LCC	260	± 450	1000
EWIC	Ireland	2012	LCC	261	± 200	500
NeMO	Belgium	2019	VSC	140	± 400	1000
IFA2	France	2020	VSC	240	± 400	1000
ElecLink	France	2020	VSC	65	± 320	1000
FABLink	France	2021	VSC	216	± 320	1400
Aquind	France	2022	VSC	145	± 320	2000
Viking Link	Denmark	2022	VSC	766	± 400	1400
NorthConnect	Norway	2022	VSC	650	± 525	1400

1.3.1.2 Germany

Up to 2020, Germany plans to build 30 GW wind farms in the northern part. The inland wind resources and the wind resources near the coast are developed using AC technology. The

offshore wind sources that are far from the coast, are connected through the VSC-HVDC technology. The detailed information about these VSC-HVDC links is summarised in Table 1-3. To fulfil the power demand of the southern countries in Germany, three inland power transmission corridors using VSC-HVDC technology will be built before 2025 to transport the renewable power from the north to the south, as shown in Fig. 1-9.

Table 1-3 VSC-HVDCs for offshore wind farms

Name	Commissioned year	Transmission Distance (km)	Voltage (kV)	Power (MW)
BorWin1	2012	200	± 150	400
DolWin1	2014	165	± 320	800
BorWin2	2014	200	± 300	800
HelWin1	2014	130	± 250	576
SylWin1	2014	205	± 320	864
HelWin2	2015	130	± 320	690
DolWin2	2017	135	± 320	916
DolWin3	2017	160	± 320	900
BorWin3	2019	160	± 320	900

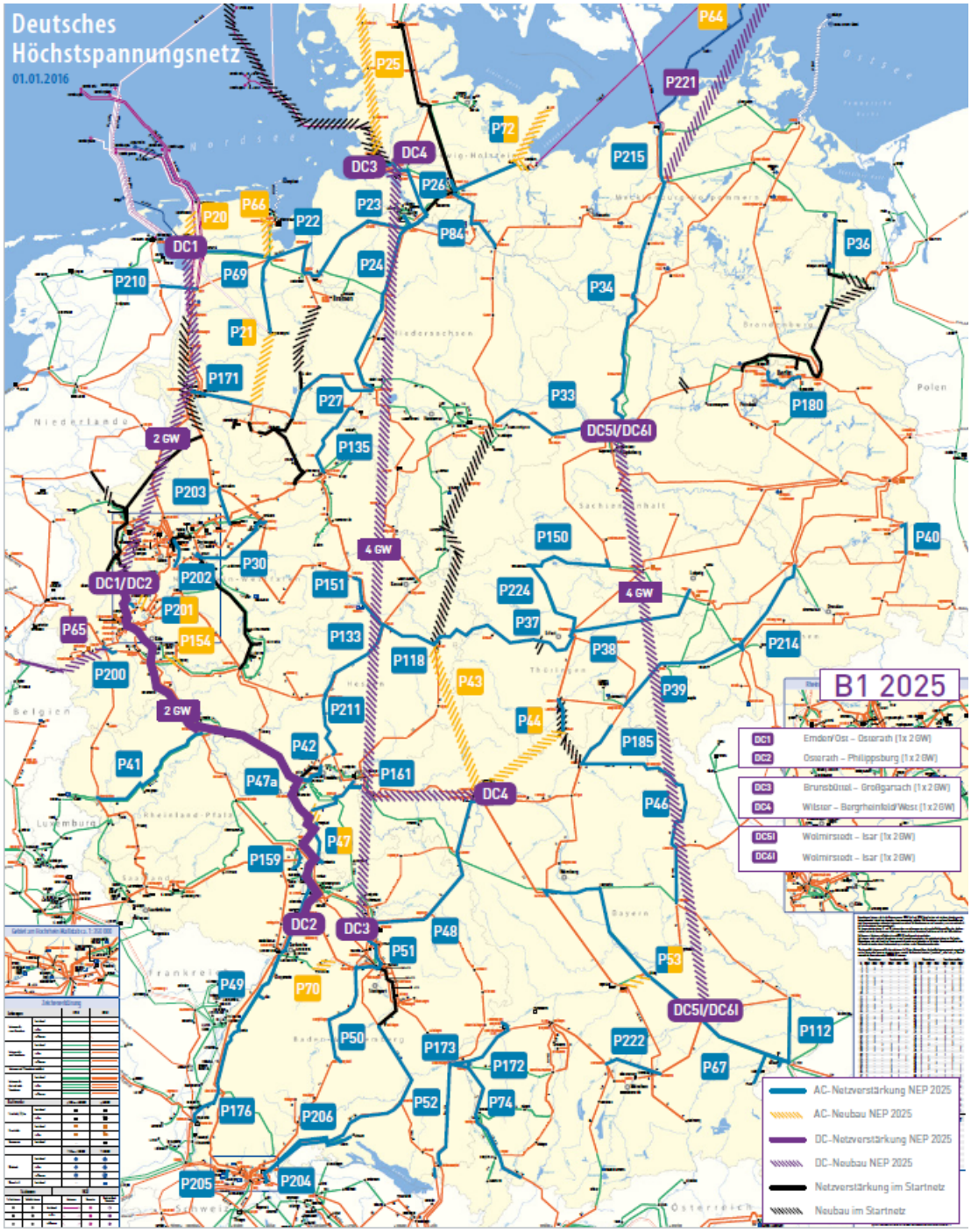


Fig. 1-9 Inland VSC-HVDC power transmission corridors of Germany [11]

1.3.1.3 Nordic countries

The development of the renewable energy and a common European framework will enhance the interconnection in the Nordic power system. The electricity exchange among Nordic countries will be balanced through the interconnection links due to the fluctuation of the renewable energy. Up to now, the total annual HVDC transmission capacity is 81 TWh

[12], which makes the HVDC links be important for the stable operation of the Nordic power system and the commercial power trade in the European energy markets. The HVDC links which are commissioned and under construction are shown in Fig. 1-10. Four more HVDC links are under development are summarised in Table 1-4.

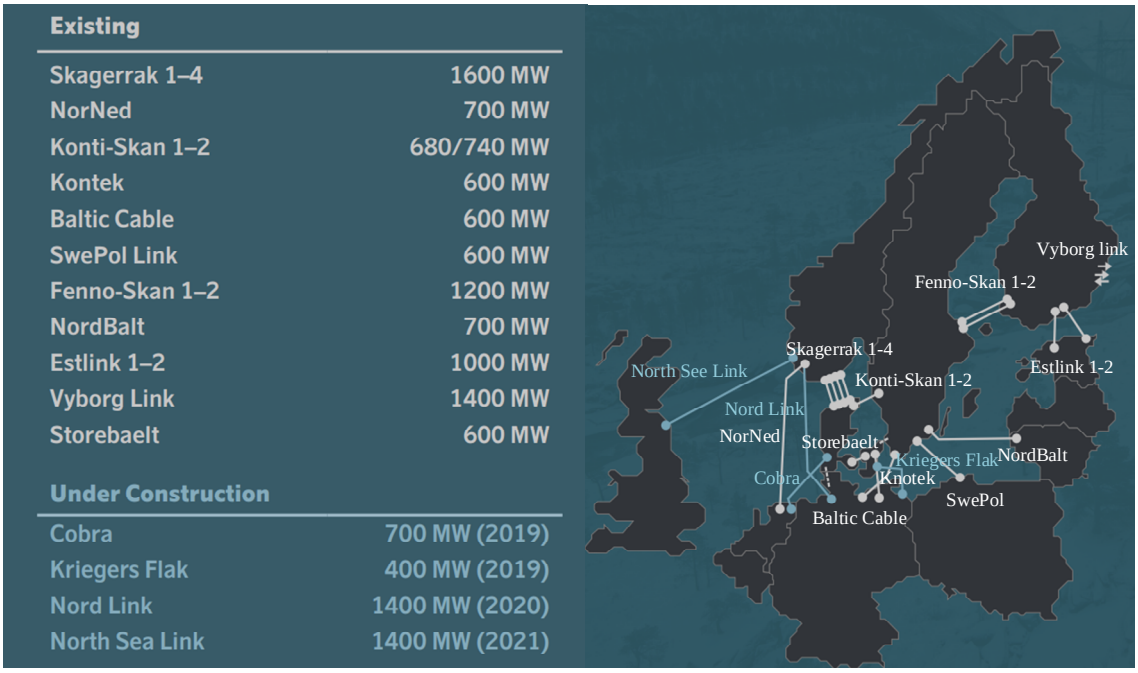


Fig. 1-10 the interconnection using HVDC links in Nordic power system [13]

Table 1-4 VSC-HVDCs for offshore wind farms

Name	Commissioned year	HVDC types	Transmission Distance (km)	Voltage (kV)	Power (MW)
Viking Link	2022	VSC	766	± 400	1400
DK West-Germany	2022	VSC	---	± 400	2500-3500
North Connect	2022	VSC	650	---	1400
Hansa PowerBridge	2025/26	VSC	300	± 300	700

1.3.2 America

America is one of the biggest countries in the world, it has various renewable resources such as the hydropower in the north, the solar power in the south, the offshore wind power, and inland wind power in the centre. In America, there are some of the best wind sources, which can produce 10 times [14] the whole country's electricity demand. Currently, there are more

than 400 manufacturers make the productions for the wind power generation. And the solar power in America currently is well developed, the total installation capacity of the solar power has exceeded 3.1 GW.

HVDC technology is used to achieve the renewable power transmission. currently, there are ten commissioned HVDC links in America, as shown in Fig. 1-11. Quebec-New England, Pacific Intertie and Nelson River are used for hydropower transmission. Intermountain Power, CU, and Square Bute are used for coal power transmission. Transbay Cable, Cross-sound Cable, and Neptune are used for interconnection between cities. With the fast development and expansion of the cities, more HVDC systems are requested. The hydropower from Canada will continue to be developed to support the cities in the north. The coastal cities will benefit from the offshore wind farms. The renewable resources of Great Plains will be developed deeply and five clean power lines will be constructed to support the main load centres.

Fig. 1-11 Commissioned HVDC links in America [15]

1.3.2.1 New England Clean Power Link

New England Clean Power Link using HVDC technology is proposed to strengthen the regional fuel diversity support the electricity to the northern cities of America. Hydroelectric power is transported from the Canadian border at Alburgh, Vermont to Ludlow, Vermont along 156 km underwater cables and 90 km underground cables. The ratings of the converter will be 300 to 320 kV and 1000 MW. This HVDC link will be commissioned around 2020.

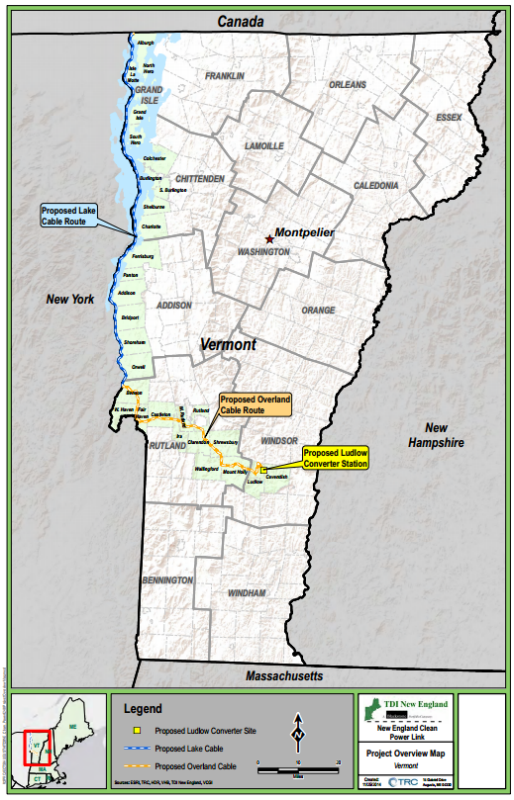


Fig. 1-12 New England Clean Power link [16]

1.3.2.2 Atlantic Wind Connection

Atlantic Wind Connection is an offshore, undersea HVDC transmission system. the transmission system will connect wind farms to coastal cities from New Jersey to Virginia. This system will help to provide the cost-effective wind energy to consumers, improve the reliability of the grid, and stabilize the electricity price. The Atlantic Wind Connection will be built in three phases over ten years, as shown in Fig. 1-13. New Jersey Energy link will be built

first as the Phase 1 project and completed in 2021. The Delmarve Energy link will be built as the Phase 2 project to transport the wind power to Delaware, Maryland, and Virginia. These two links will be interconnected at Phase 3.

Fig. 1-13 Atlantic Wind Connection [17]

1.3.2.3 Clean Line

The huge capacity of the renewable energy and the demand for clean energy make America plan to move towards a clean energy economy. The main load centres in America locate in the northern and southern area and mainly rely on the electricity generated from the nearby power plant. The AC power networks are therefore significantly developed in the northern and southern area. The advancement of electricity generation technology allows developing massive renewable energies on Great Plain at the centre of America. However, the lack of the transmission to transport the electricity to the northern and southern AC power networks is a serious challenge.

HVDC technologies due to its long-distance and bulk-power transmission ability are selected to overcome this challenge. And five electricity transmission corridors as shown in Fig. 1-14 using HVDC technology are planned to send the renewable energy evenly to the northern and southern power networks. These electricity transmission corridors are named as

Clean Lines [18]. The AC networks will send the renewable energy to the load centres according to the power demand. The detailed information about these five corridors are summarised in Table

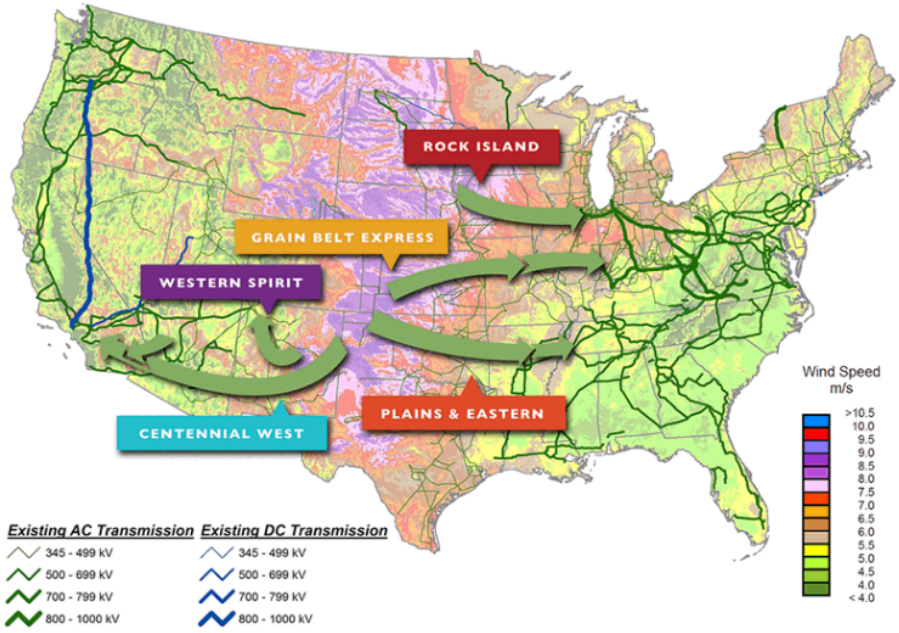


Fig. 1-14 Distribution of Clean Line [18]

Table 1-5 Planning HVDC transmission systems

Name	Transmission Distance (km)	Power (MW)
Centennial West Clean Line	1450	3500
Western Sprit	224	1000
Grain Belt Express Clean Line	1248	4000
Plain & Eastern Clean Line	1100	4000
Rock Island Clean Line	800	3500

1.3.3 China

China owns rich and variable power resources, which locate on the west mostly. The southern provinces of China request a large amount of electricity to support their fast development. The lack of local power resource in the south of China is a significant obstacle that will limit the development of southern provinces. To overcome the obstacle, China constructs many HVDC links to transport the electricity generated in the west to the southern load centres, and more HVDC links are under construction or planning. The development of

HVDC technology in China is fast. And the new HVDC technologies can be transferred into the real project quickly. The highest voltage and power rating of HVDC link and the first multi-terminal HVDC systems are all constructed in China.

1.3.3.1 Energy development in the western China

The renewable energy attracts a lot of attention in the world and long-term plans for developing renewable energy have been made by many countries, also including China. The energy resources are mainly located in the west of China, such as hydropower, fossil power, wind power and solar power, as shown in Fig. 1-15. Sichuan and Yunnan provinces have plenty of hydro energy. Gansu province has plenty of solar energy. Wind, solar and fossil fuel sources are mainly located in Ningxia, Gansu and Xinjiang provinces. The proportion of the electricity from solar and wind energy will be raised gradually and the development of fossil fuel power plant will be slow down. The energy development plan of China is summarised in Table 1-6.

Fig. 1-15 Energy resource distribution in the west of China

Table 1-6 The plan for electricity generation distribution to 2030 [19]

Sources of electricity	2020 (MW)	2030 (MW)
Fossil fuel energy	810,000	1070,000
Hydro energy	388,000	450,000
Wind energy	100,000	220,000
Solar energy	160,000	350,000

1.3.3.2 HVDC development

The uneven distribution of loads and sources promotes the development of the HVDC technologies. Currently, there are more than 40 commissioned HVDC projects. The electricity will be transported from the west and north to the east and south, see Fig. 1-16. In recent years, HVDC technologies advance quickly in China. Many HVDC technologies are put into operation firstly in China. And some representative HVDC projects are selected and shown in Table 1-7. In the future, a big HVDC grid may be constructed in the west to connect variable power sources into one grid to achieve economical and efficient electricity transmission.

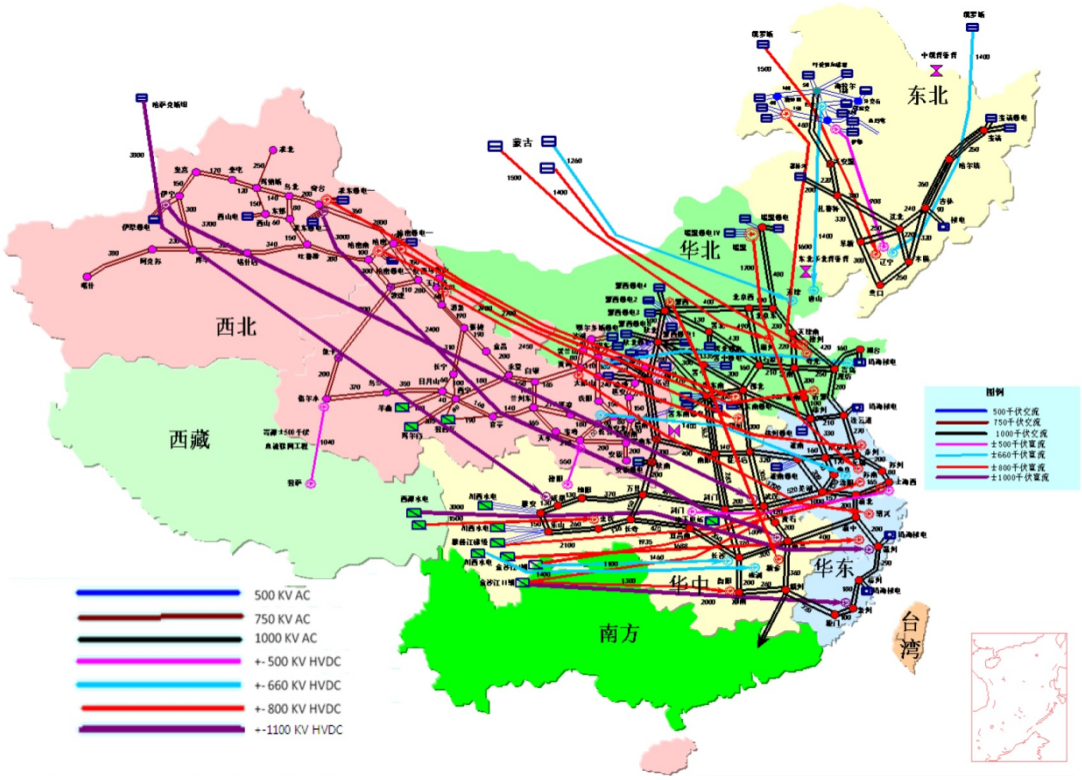


Fig. 1-16 Distribution of HVDC transmission systems in China

Table 1-7 Selected world leading HVDC projects

Name	Commissioned year	HVDC types	Voltage (kV)	Power (MW)	Description
Zhundong-Chengdu	2015	LCC	± 1100	12000	HVDC system with highest voltage rating
Nanao	2013	VSC	± 160	200	First multi-terminal HVDC system
Zhoushan	2014	VSC	± 200	1000	First multi-terminal HVDC system using DC breakers
Xiamen	2015	VSC	± 320	1000	First bipolar HVDC system
Luxi	2017	LCC-VSC	± 350	1000	First back-to-back system using LCC-MMC
Zhangbei	2018	VSC	± 500	3000	VSC-HVDC system with highest voltage rating

1.4 **Technical challenges**

The large-scale development of renewable energy and the increasing electricity demand promote the development of HVDC transmission technologies. A large number of HVDC projects as the backbones of electricity transportation has been commissioned in the world. Most of them are point-to-point links, which at the moment are the proper way to fulfil electricity demands. Although the HVDC grid having more advantages over the HVDC links is conceptually achievable and some multi-terminal HVDC projects have been commissioned as the start of the HVDC grid exploration, there are still many challenges which have to be addressed:

- DC grid protection: Compared to an AC transmission system, the impedance within a DC grid is much lower. Therefore, the propagation of a fault in a DC grid will be much faster than that in AC systems, which further leads to the fast DC fault current rising and DC voltage drop. The DC fault current has no zero crossing. Traditional mechanical circuit breakers are not suitable for protecting a DC grid from a DC fault.
- Interconnection among HVDC system: To achieve a large-scale DC grid, interconnecting HVDC systems is an efficient way. Voltage ratings of these HVDC

systems are normally different due to lack of the uniform voltage standards. And their operations are different. These features increase the difficulties of the interconnection.

- Grid level control system: A HVDC grid is a complicated system which crosses a wide area. The subsystem in the HVDC grid normally has their own operations. A robust grid level control system is requested to coordinate the operations of the whole HVDC grid to avoid the conflict between subsystems. This grid level control system should achieve the optimal power flow under static state and have a quick response to the transient state.
- Upgrade of existing HVDC devices: The higher voltage and power ratings of an HVDC grid will increase its abilities of expansion and electricity transportation. More renewable energy sources can be reached by the HVDC grid. The exploration of the higher ratings of HVDC devices will not stop until the power demand is fully fulfilled.

1.5 **Research objectives**

In this thesis, the cost reduction of the HVDC grid protection and the interconnection between LCC-HVDCs are studied.

The future HVDC grid will be protected via the hybrid HVDC circuit breakers due to its high interrupting speed and low conduction losses. However, the cost of a hybrid HVDC circuit breaker is high. There will be a huge amount of cost to achieve the grid-level protection because two terminals of each transmission line have to install hybrid HVDC circuit breakers. The research question in this part is how to reduce the cost of the hybrid HVDC circuit breaker.

Most of the commissioned HVDC projects are point-to-point LCC-HVDCs. The interconnection of LCC-HVDCs will achieve the benefits of the grid operation, such as highly efficient and flexible power transportation, and high security of power transportation.

However, benefits of the interconnection are hindered by the disadvantages of the LCC-HVDC. First one is that an LCC-HVDC has to reverse its voltage polarity in order to reverse its power. The second one is that an LCC-HVDC is at risk of the commutation failure, which will cause a DC fault when a commutation failure occurs. The research question in this part is how to achieve the interconnection of LCC-HVDCs with the benefits of the grid operation.

The objectives of this thesis are summarized below:

- Cost reduction of hybrid HVDC circuit breaker via structure optimization, which will reduce the number of applied components.
- Cost reduction of hybrid DC circuit breaker via current rating reduction
- Interconnection of LCC-HVDCs with the capability of power reversal
- Interconnection of LCC-HVDCs with the capability of commutation failure mitigation

1.6 **Research contributions**

The research contributions of this thesis are shown below:

- Interlink hybrid HVDC circuit breakers, which can be used as the unidirectional interruption or bidirectional interruption, are proposed in order to reduce the size of main breaker branches. Comparing to the unidirectional and directional hybrid HVDC circuit breakers, the number of MOVs of the main breaker branch of a unidirectional interlink hybrid HVDC circuit is reduced by 50%, and the numbers of IGBT modules and MOVs of the main breaker branch of a bidirectional interlink hybrid HVDC circuit breaker are reduced by 25%.
- The protection of an HVDC grid through coordination of converters and hybrid HVDC circuits breakers is proposed to reduce the current rating of the breaker. A bypass operation of a modular multilevel converter is proposed to avoid the converter's contribution to the fault current. Therefore, the current rating of the

hybrid HVDC circuit breaker is significantly reduced, because most of the fault current comes from the converter.

- Interconnection of LCC-HVDCs with the capability of power reversal is studied. A power regulation control is proposed for the interconnection device to transfer the power between LCC-HVDCs flexibly and smoothly. A low-cost solution-a switchyard design is proposed for the interconnection device to work under the condition of one LCC-HVDC reversing its power. An isolation control is proposed to protect the LCC-HVDC from the disturbances during the period that the other LCC-HVDC changes its operation from the normal to the power reversal.
- Interconnection of LCC-HVDCs with the capability of commutation failure mitigation is studied. A commutation failure mitigation control system is proposed for the interconnection device to mitigate the commutation failures of the LCC inverters. Compared to the conventional commutation failure mitigation control system, the proposed strategy has better results.

1.7 List of Publications

Conference Papers

[1] Tianqi Zhang, **Chuanyue Li** and Jun Liang, "A Thyristor Based Series Power Flow Controller for Multi-Terminal HVDC Transmission", 49th International Universities Power Engineering Conference (UPEC14), Cluj-Napoca, Romania, 2-5 September 2014.

[2] **Chuanyue Li**, Xiaobo Hu, Jingli Guo and Jun Liang, "The DC grid reliability and cost evaluation with Zhoushan five-terminal HVDC case study", 50th International Universities Power Engineering Conference(UPEC15), Stoke on Trent, UK, 2-5 Sep. 2015.

[3] Yingmei Liu, **Chuanyue Li**, Qing Mu and Jun Liang, "Side-by-side connection of LCC-HVDC links to form a dc grid", 17th European Conference on Power Electronics and Application, Geneva, Switzerland, Sep. 2015

[4] Sheng Wang, **Chuanyue Li**, Oluwole Adeuyi, Gen Li, Carlos E Ugalde-Loo and Jun Liang, "Coordination of DC circuit breakers and MMCs on protecting HVDC grids", 2016 International High Voltage current Conference (HVDC 2016), Shanghai, China, 25-27 Dec. 2016.

[5] **Chuanyue Li**, Sheng Wang, Jun Liang, "Bypassing sub-module strategy applied in MMC-based DC/AC/DC converter within interconnected LCC-HVDCs for commutation failure mitigation ", 13th IET International Conference on AC and DC Power Transmission, Manchester, UK, 14-16 Feb. 2017.

[6] **Chuanyue Li**, Sheng Wang, Jun Liang, "Dual-circuit hybrid HVDC circuit breaker", 19th European Conference on Power Electronics and Application, Warsaw, Poland, Sep. 2017.
[7] **Chuanyue Li**, Sheng Wang, Jun Liang, "Switchyard and isolation design for DC/AC/DC converter based on half-bridge sub-modules operating at power reversal condition in LCC-HVDC system", 19th European Conference on Power Electronics and Application, Warsaw, Poland, Sep. 2017.

Journals

[8] Sheng Wang, Jingli Guo, **Chuanyue Li**, Senthooran Balasubramaniam and Rui Zheng, "Coordination of DC power flow controllers and AC/DC converters on optimising the delivery of wind power", IET Renewable Power Generation, pp. 1-9, 2016.
[9] Qing Mu, Jun Liang, Xiaoxin Zhou, **Chuanyue Li**, and Yalou Li, "Systematic Evaluation for Multi-rate Simulation of DC Grids", International Journal of Electrical Power & Energy System, Vol. 93, pp.119-134, Dec. 2017.
[10] **Chuanyue Li**, Jun Liang and Sheng Wang, "Interlink hybrid DC circuit breaker," IEEE Transaction on Industrial electronics. (Submitted on Aug. 2017)
[11] Sheng Wang, **Chuanyue Li**, et.al. "Coordination of MMC converters and hybrid DC circuit breakers for HVDC grid protection", IEEE Transactions on Power delivery. (submitted on Sep. 2017)

Book Chapter

[12] "HVDC Grids: For Offshore and Supergrid of the Future", the second author of the 3rd chapter: "HVDC Technology Review", WILEY, John Wiley & Sons, Inc. 2016.

1.8 Project participation

[1] Overview of HVDC grid R&D and reliability of HVDC stations, China Electric Power Research Institute, Lead project executor, 06/2013-12/2015.
In this project, I am the only project executor. My work includes preparing all reports and presentations, doing research and writing papers.
[2] DC-DC converters for DC grid interconnection, North China Electric Power University, Project executor,01/2016-12/2017.
In this project, I am the only project executor. The types of work are same to first one.
[3] Multi-terminal HVDC grid control and the interaction with AC grids, Natural Science Foundation of China, 01/2012 -12/2013, project executor.
In this project, I work on preparing one chapter of the final report.

1.9 Outline

It is cost-effective to construct a High Voltage Direct Current (HVDC) grid via interconnecting existing HVDCs. The grid protection and the interconnection between HVDCs are studied in the thesis. A literature review is introduced in Chapter 2 in terms of the history of HVDC development, AC/DC conversion technologies, and devices used in an HVDC grid. An interlink hybrid HVDC circuit breaker is proposed to reduce the size of main breakers comparing to the conventional hybrid HVDC circuit breakers in Chapter 3. Chapter 4

introduces a coordination control of the MMC and the hybrid HVDC circuit breaker to reduce the current rating of the breaker. The studies on the interconnection of two LCC-HVDCs are introduced to cope with the power reversal of LCC-HVDCs and mitigate the commutation failures of LCC-HVDCs in Chapter 5 & 6. The conclusion and future work are drawn in Chapter 7.

Chapter 2. OVERVIEW OF HVDC GRID TECHNOLOGIES

HVDC grid is an efficient and cost-effective power system. It is also a complex system and should maintain the high power-transmission security like AC system. At the moment, most of the commissioned HVDC projects are HVDC links. A few multi-terminal HVDCs have been commissioned recently as the start towards a real HVDC grid. To build a real HVDC grid, more HVDC technology accumulation are requested.

This chapter will describe the technologies used in HVDC grid detailly. These technologies will include the types of the converters, control methods of converters, transmission lines, multi-terminal HVDC systems, DC circuit breakers, and DC/DC converters. The description will follow the sequence of the history, the state-of-the-art, and the future trend of HVDC grid technologies.

2.1 History of HVDC technology

Since the first HVDC project was put into operation in the 1950s, two HVDC technologies based on different AC/DC conversion theories have been developed. The earlier one is the HVDC technology using line commutated converter (LCC). The other one is the HVDC technology using voltage source converter (VSC), which is the second generation HVDC technology. The LCC-HVDC and the VSC-HVDC have their own expertizes and currently both of them serve for power transmission.

2.1.1 Development of Line commutated converter HVDC

In an LCC-HVDC, the valves for AC/DC voltage conversion experience one iteration. The first generation is the mercury-arc valves. The second generation is the thyristor valves, which are used until today. The mercury-arc valve was invented in 1901 and firstly used for the AC/DC conversion in 1932. The project is an experimental 3 MW, 45 kV DC link between Switzerland and Germany. In 1954, the technology of the mercury-arc valve had been mature

and first commercial 20 MW, 100kV HVDC transmission based on LCC technology (using mercury-arc valves) named Gotland HVDC link is commissioned. Since then, more and more LCC-HVDCs using mercury-arc valves are put into operation for power transmission.

The mercury-arc valve reaches the limit of blocking voltage soon in the 1960s. It cannot withstand the increasing operation voltage of HVDC technology for future development. And the mercury vapour released from mercury-arc valves is harmful to the environment. The thyristor has higher blocking voltage and no mercury vapour release. Therefore, after 1970, all commissioned LCC-HVDCs use thyristor valves, and the previous LCC-HVDC systems are upgraded from the mercury-arc valves to thyristor valves. The detailed development of the AC/DC conversion valves is drawn in Fig. 2-1.

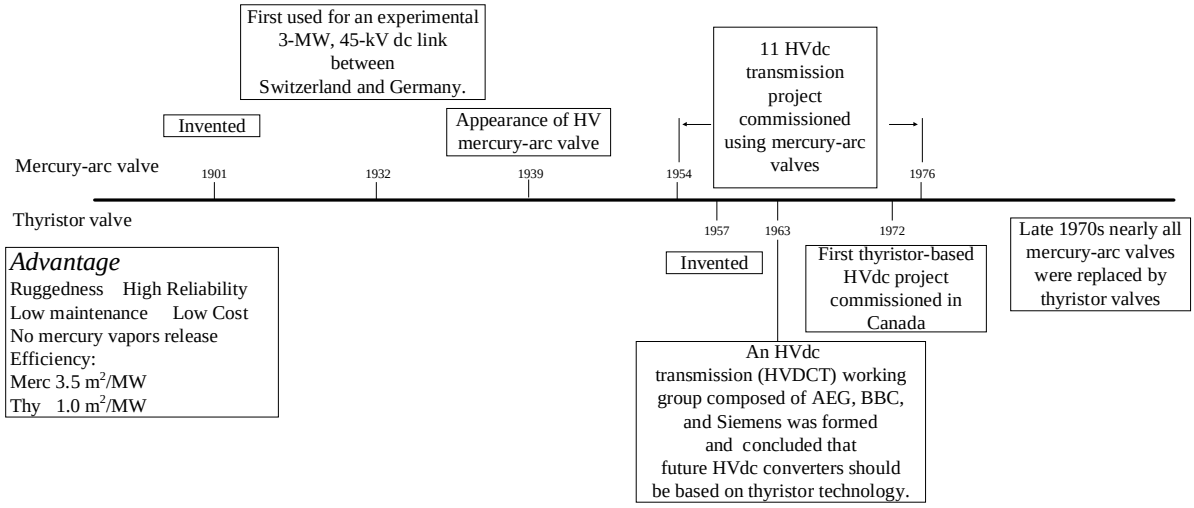


Fig. 2-1 The development of the valves in LCC-HVDC

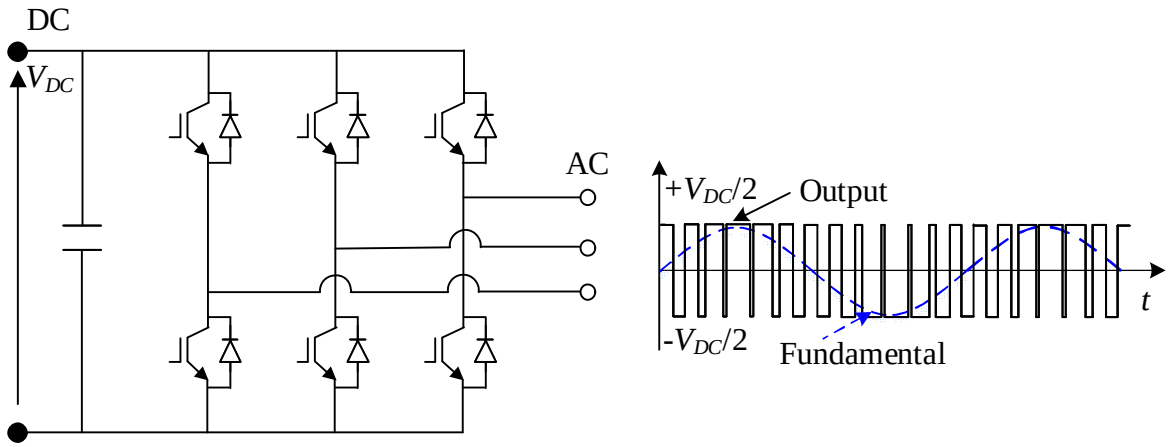
To date, the LCC-HVDC is a mature technology for long distance and bulk power transmission. Most of the commissioned HVDC projects used LCC-HVDC technology. Its maximum voltage and power rating reaches to 1100 kV and 12 GW as shown in Table 1.7 Zhundong-Chengdu project.

2.1.2 Development of voltage source converter HVDC

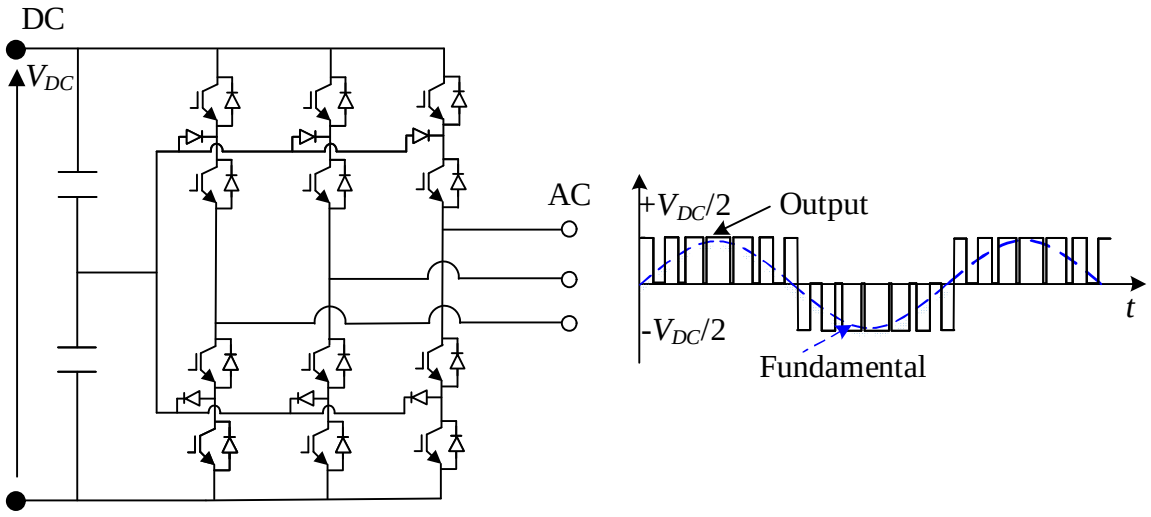
In the 1980s, a fully controllable transistor switch-insulated gated bipolar transistor is invented. Comparing to the thyristor with only turn-on ability, the IGBT is capable of being

turned on and turned off. The combination of IGBTs and capacitors brings a new approach to AC/DC conversion. The converter using this approach can work as a controllable AC voltage source. Therefore this type of converter is named as voltage source converter.

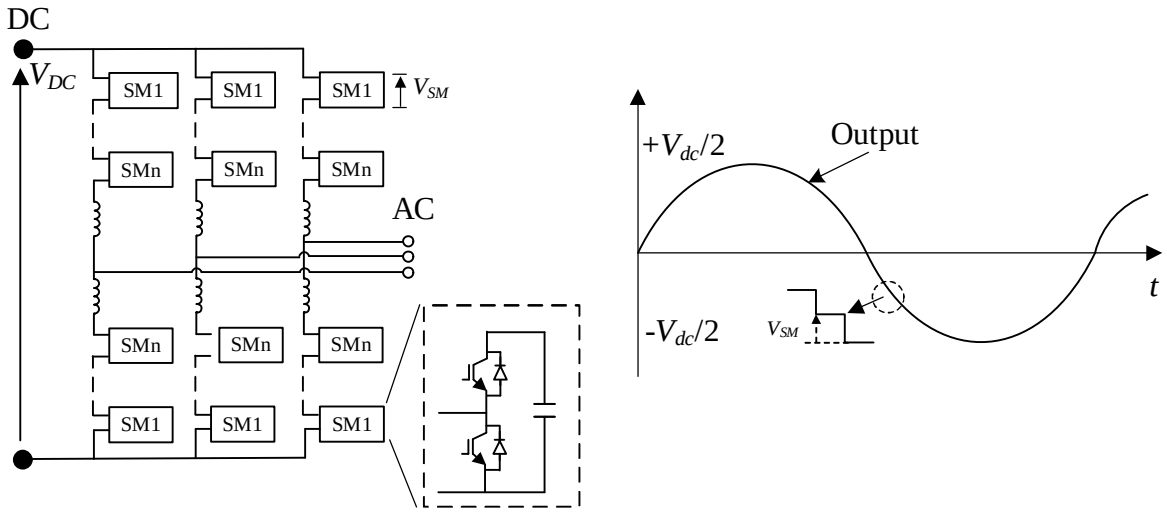
In 1997, the first commercial VSC-HVDC project was commissioned. Up to now, the technology of the VSC has been upgraded two iterations from the two-level VSC, 3 level neutral point clamped VSC then to the current vision modular multilevel converter (MMC). The topologies of them and their output AC voltages are shown in Fig. 2-2. The MMC can operate without filters due to the pure sine output AC voltage. And Its operation frequency is lowest among these VSC technologies, which reduces its converter losses significantly to about 1%. The first commercial MMC-HVDC named as Trans Cable Bay is commissioned in 2009. Since then, most of the commissioned VSC-HVDC projects use MMC technology. The MMC technology in different companies is given different names: MMC(Siemens), cascaded two-level converter (CTL) (ABB), and MaxSine (GE grid). Most commissioned VSC-HVDC projects are summarized in Table 2-1.



(a) Two level VSC and its output AC voltage



(b) Three level neutral point clamped VSC and its output AC voltage



(c) Modular multi-level VSC and its output AC voltage

Fig. 2-2 Technology upgrade of the voltage source converter

Table 2-1 Commissioned VSC projects

Project Name	Commission year	Power /MW	DC Voltage/kV	Length	Topology
Hällsjön, Sweden	1997	3	±10	10 km Overhead line	2 level
Gotland HVDC light, Sweden	1999	50	±80	70 km submarine cables	2 level
Eagle Pass, USA	2000	36	±15.9	Back-to-back converter	3-level NPC
Tjaereborg, Denmark	2000	7.2	±9	4.3 km submarine cables	2 level
Terrenora Interconnection (Directlink), Australia	2000	180	± 80	59 km land cables	2 level
Murray Link, Australia	2002	220	± 150	180 km land cables	3-level NPC
Cross Sound, USA	2002	330	±150	40 km submarine cables	3-level NPC
Troll A Offshore, Norway	2005	84	±150	70 km submarine cables	2 level
Estlink, Estonia-Finland	2006	350	±150	31 km land cables 74 km submarine cables	2 level
NordE.ON 1, Germany	2009	400	±150	75 km land cables 128 km submarine cables	2 level
Trans Bay Cable Project, USA	2010	400	±200	85 submarine cables	MMC
Caprivi Link Interconnector, Namibia	2010	600	-350	950 km overhead lines	2 level
Valhall, Norway	2011	78	-150	292 km submarine cable	2 level
BorWin 1, Germany	2012	400	±150	75 km land cables 125 km submarine cables	CTL
East West Interconnector, Ireland	2012	500	±200	75 km land cables 186 km submarine cables	2 level
Dolwin 1, Germany	2013	800	±320	90 km land cables 75 km submarine cables	CTL
BorWin 2, Germany	2013	800	±300	125 submarine cables 75 land cables	MMC
HelWin 1, Germany	2013	576	259	85 km submarine cables 45 km land cables	MMC
South-West Link Sweden	2014	2×660	±300	192 km land cables	CTL
Inelfe, Spain-France	2014	2×1000	±320	65 km land cable	MMC
Skagerrak, Pole 4 Norway-Denmark	2014	700	500	140 km submarine cable 104km land cable	CTL
Mackinac, USA	2014	200	±71	Back-to-back converter	CTL
SylWin 1 Germany	2015	864	±320	160 submarine cables 45 land cables	MMC
HelWin 2, Germany	2015	690	±320	85 submarine cables 46 km land cables	MMC
Troll A 3-4, Norway	2015	50	±60	70 km submarine cables	---
AL link, Finland	2015	100	±80	158 km submarine cables	---
Nordbalt, Sweden-Lithuania	2017	700	±300	400 km submarine cables 50 km land cables	CTL
Dolwin 2, Germany	2017	900	±320	45 submarine cables 90 land cables	CTL
DolWin 3 Germany	2017	900	±320	83 km submarine cables 79 km land cables	MaxSine

Compared to the LCC-HVDC, the ability to generate a full AC voltage brings more advantages, which are shown below:

- Rapid control of the active and reactive powers
- Ability to operate in all four quadrants of the PQ diagram
- Smaller footprint of the converter station
- Rapid AC voltage control at the converter bus via the reactive power support
- Ability to connect a non-source AC grid
- Black-start ability
- Power reversal by simply reversing the direction of the DC current
- Help to mitigate the harmonics existing in the AC grid
- NO commutation failures

VSC-HVDC is more suitable for offshore power transmission and multi-terminal HVDC applications. However, VSC-HVDC is a relative younger HVDC technology, its voltage and power ratings are not as high as the LCC-HVDC's. The achievable highest voltage and power ratings are 400 kV and 1000 MW NeMO project, which is constructed from 2016 and will be put into operation in 2019, as shown in Table 1-2. LCC-HVDC is a mature electricity transmission technology. For ultra-high voltage and bulk power transmission, the LCC-HVDC will be a better choice.

2.2 **Line-commutated converter HVDC**

2.2.1 AC/DC conversion

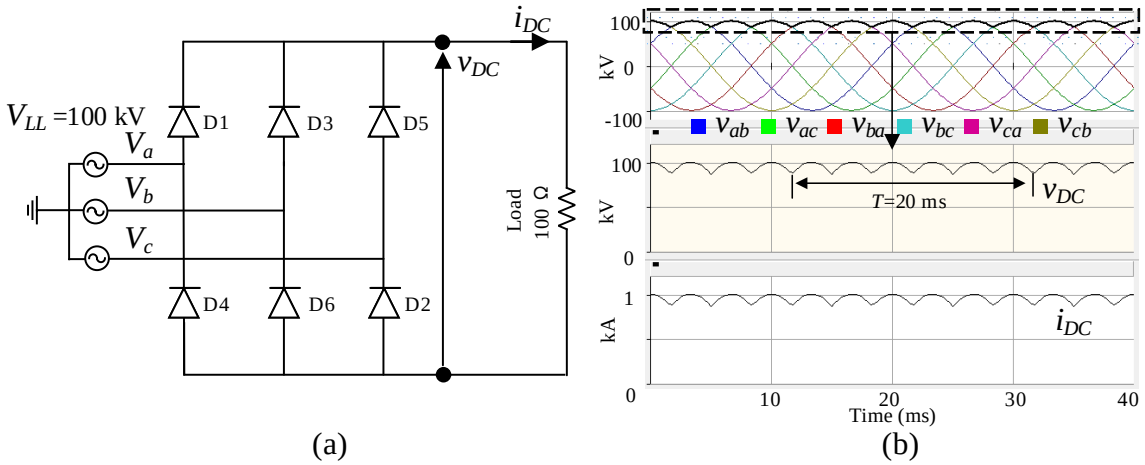


Fig. 2-3 Six-pulse bridge rectifier using diodes

The AC voltage can be converted into the DC voltage through a six-pulse bridge. To explain the conversion process clearly, a simple six-pulse bridge rectifier using diodes is drawn in Fig. 2-3 (a). There are two diodes in each phase, and each phase AC voltage source is connected to the middle point of two diodes. The DC voltage is the combination of the pulses of the line-to-line voltages, see Fig. 2-3 (b). In one period, the DC voltage has six pulses. That is why this bridge is named as a six-pulse bridge. The DC current appears when a 100 Ω resistor is applied on the DC side as the load. The shape of the DC current is same as the shape of the DC voltage.

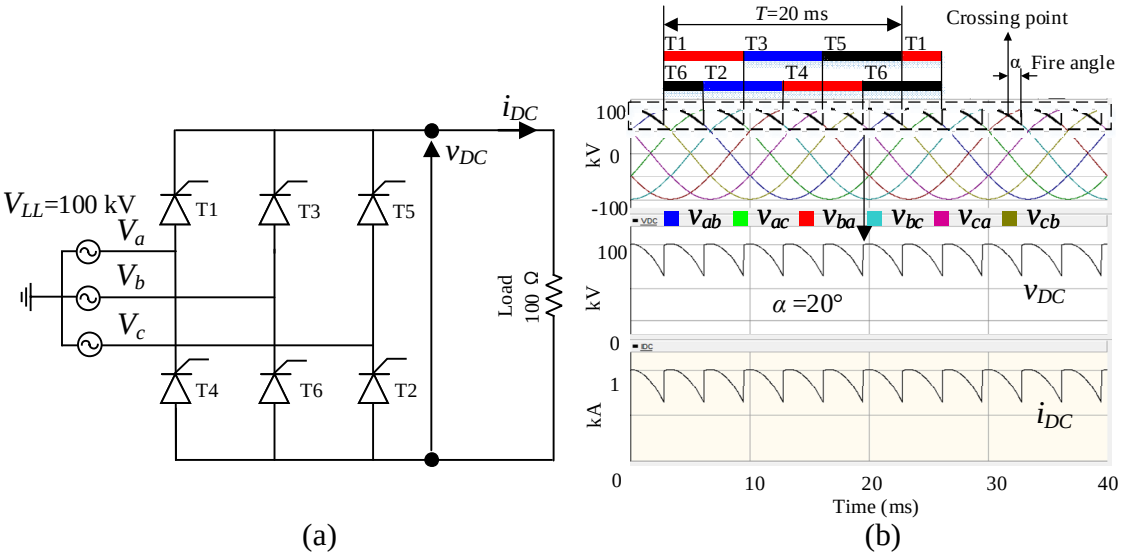
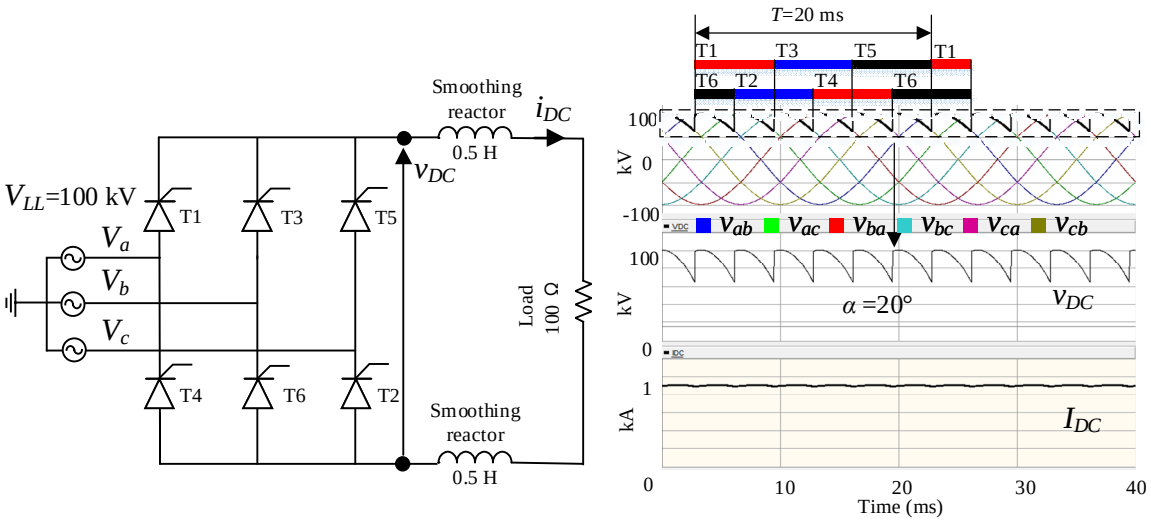


Fig. 2-4 Six-pulse bridge rectifier using thyristors

The six-pulse bridge rectifier based on the diodes cannot control the value of the output DC voltage due to the uncontrollable diode. To achieve the flexible and controllable AC/DC conversion, the thyristors are used to replace the diodes, as shown in Fig. 2-4. The operation sequence and the turn-on time for each thyristor in one period are shown in Fig. 2-4 (b). A fire angle that is the turn-on time position is defined to be followed by all six thyristors. The shape of output DC voltage can be changed via the control of the fire angle, in other words, the average value of the DC voltage can be controlled via the control of the fire angle.

The AC/DC conversion technology of LCC-HVDC is based on the six-pulse bridge using thyristors.

To reduce the ripples of the DC current, the large-value inductors are connected to the DC terminal as the smoothing reactor. After the smoothing reactors are applied, the DC current is almost a constant value, as shown in Fig. 2-5.



(a) (b)

Fig. 2-5 Six-pulse bridge rectifier with smoothing reactors

The LCC converter needs an AC transformer to change the AC voltage to the requested level. The AC transformer is a large value of inductor connected on the AC side, see Fig. 2-6 (a). The DC output voltage will be influenced by AC inductors, see Fig. 2-6 (b). An overlap period will present during the commutation from one thyristor to another because of AC inductors, see Fig. 2-6 (c). Take the commutation from T1 to T3 as an example, in the overlap period, the current in T1 will reduce the rated DC current to 0, and the current in T3 will increase from 0 to the rated DC current gradually, see Fig. 2-6 (d). This overlap period will finish when the DC current is fully commutated from T1 to T3. This overlap period is defined as the overlap angle μ.

As one six-pulse bridge in the LCC-HVDC, each component has been introduced, and their functions have been described. The average value of the output DC voltage of the six-pulse bridge can be calculated as:

$$V_{DC} = \frac{3}{\pi}\sqrt{2}V_{LL\_rms}\cos\alpha - \frac{3}{\pi}\omega L_T I_{DC} \tag{2-1}$$

Where V_{DC} is the DC voltage, V_{LL_rms} is the AC line-to-line RMS voltage, L_t is the AC equivalent inductance, I_{DC} is the DC current, and α is the fire angle.

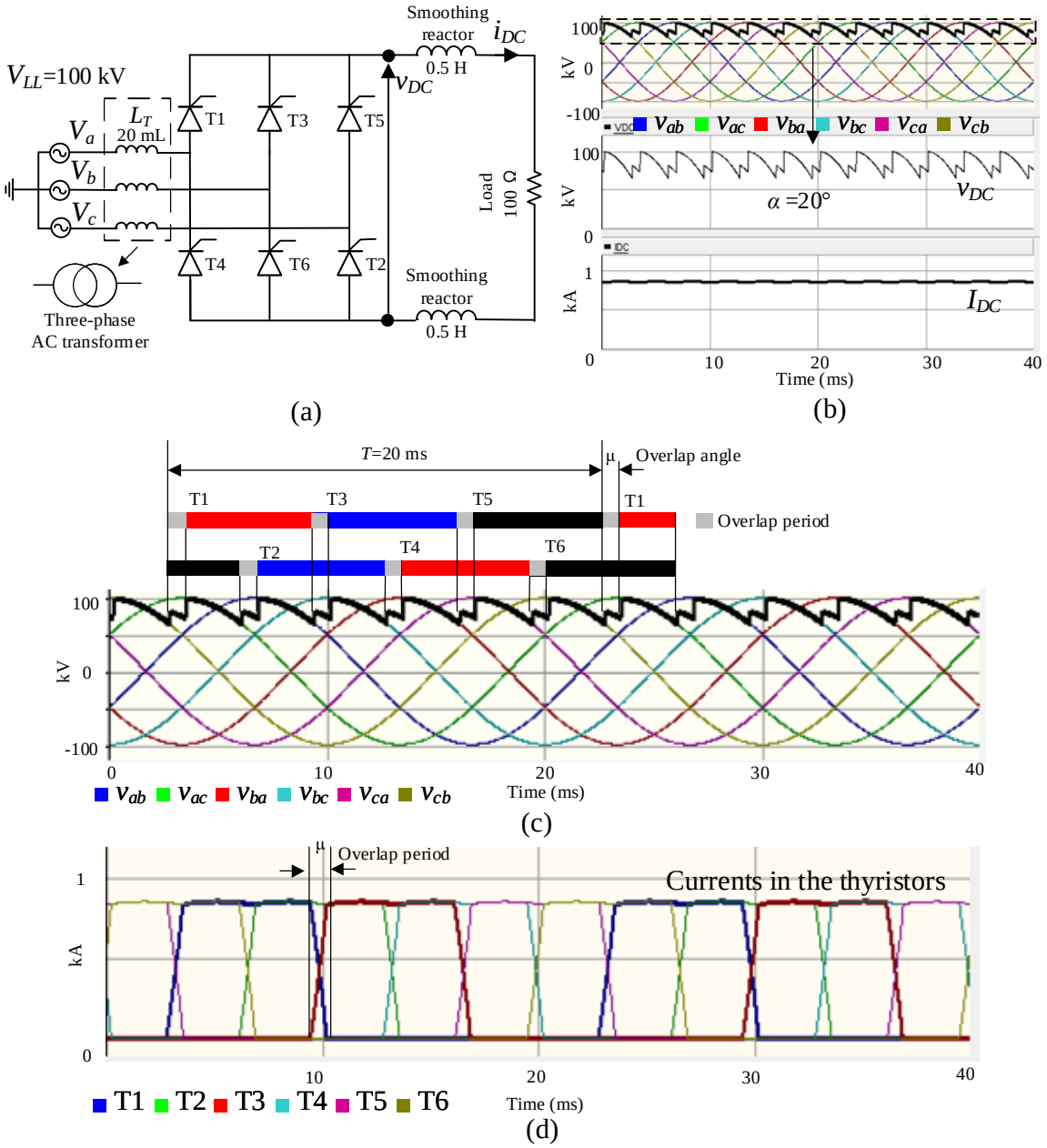


Fig. 2-6 six-pulse bridge rectifier used in LCC-HVDC

2.2.2 DC/AC inversion

For an LCC-HVDC, the rectifier sends the power to the inverter. The direction of the DC current is from the rectifier to the inverter. The connection of the six-pulse bridge in the inverter cannot be same as that of the rectifier due to the unidirectional conduction of the thyristor. The opposite connection way is proposed for the inverter to allow the same direction of the DC current, see Fig. 2.7 (a). The DC voltage of the inverter should be negative, and its value is equal to that of the rectifier.

To achieve the negative DC voltage of the inverter, the fire angle should be put into [90°,180°] according to the Eq. 2-1. An example is shown in Fig. 2-7 (b), the fire angle is controlled at 140°. The DC current is flowing from the rectifier to the inverter, and the output DC voltage of the DC voltage is around -90 kV.

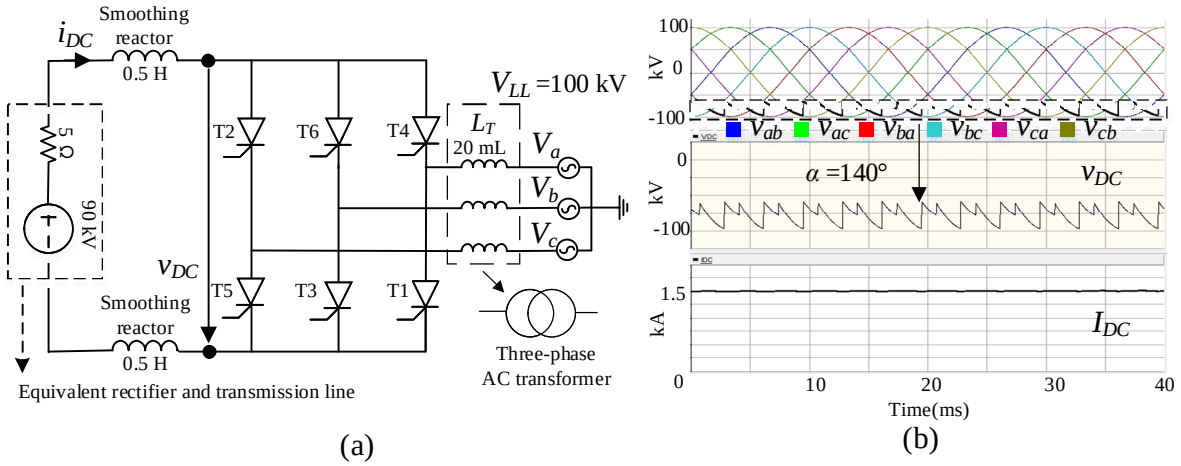


Fig. 2-7 six-pulse bridge inverter

2.2.3 Power reversal

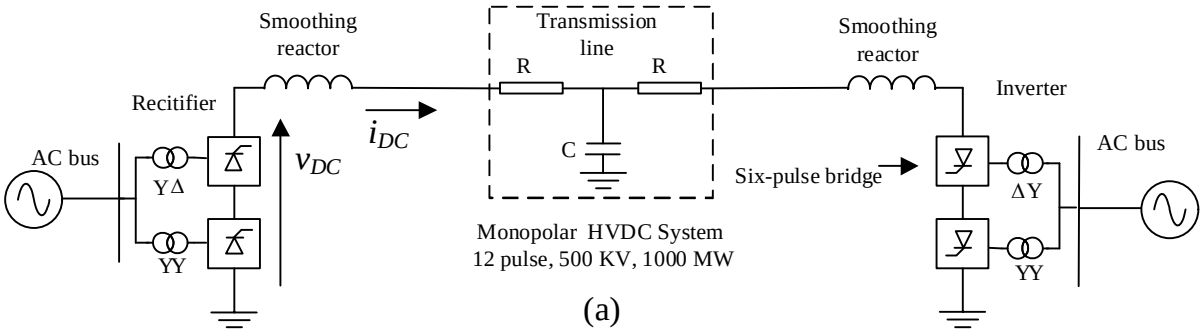
The power reversal of an LCC-HVDC is normally requested for a certain period to fit the power demand. For an LCC-HVDC link, only one direction of the DC current is allowed due to the unidirectional conduction of the thyristor. The power is equal to the DC voltage times to the DC current. To achieve the power reversal in an LCC-HVDC, the polarity of the DC voltage has to be reversed.

An example of the power reversal of an LCC-HVDC is shown in Fig. 2-8. The topology of the LCC-HVDC is shown in Fig. 2-8 (a). Two six-pulse bridges are used in the rectifier and inverter to perform 12-pulse converters. The process of power reversal is designed as below:

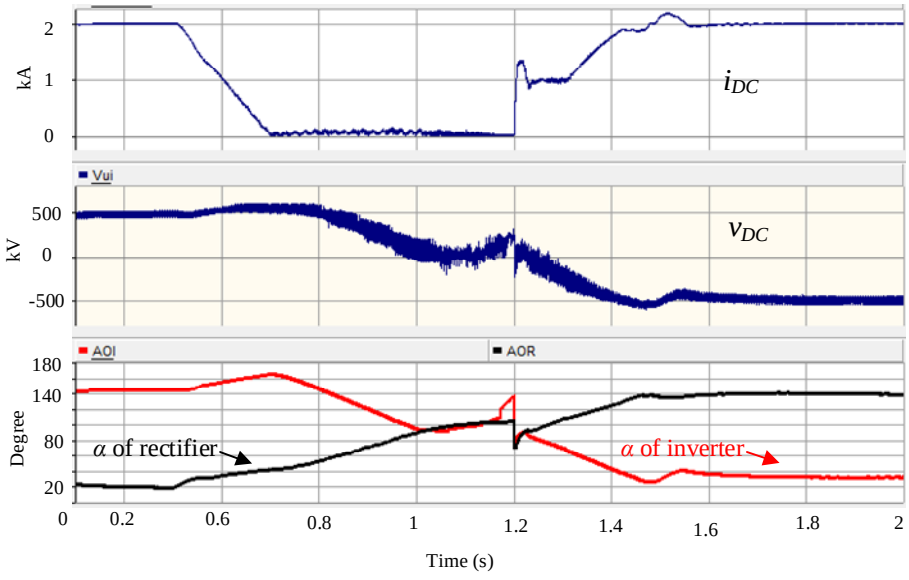
- Starting at 0.5s, from 0.5 s - 0.7 s, the DC current is reduced to 0 kA
- From 0.7 s- 1 s, reduce the DC voltage to 0 kV
- From 1 s – 1.2 s, this time slot is designed for the control setting and transformer tap change.

- After 1.2 s, the LCC-HVDC start to reach to its power reversal condition.

The DC voltage and DC current during the power reversal are shown in Fig. 2-8 (b). and the LCC-HVDC is controlled via the fire angle, the fire angles of the rectifier and the inverter are shown in Fig. 2-8 (b) during power reversal. The fire angle of the rectifier is changed from 20° to 140°, which means the rectifier will be the inverter after the power reversal to receive the power. The fire angle of the inverter is changed from 140° to 30°, which means the inverter will be the rectifier after the power reversal to send the power.



(a)



(b)

Fig. 2-8 power reversal of an LCC-HVDC

2.2.4 Commutation failure

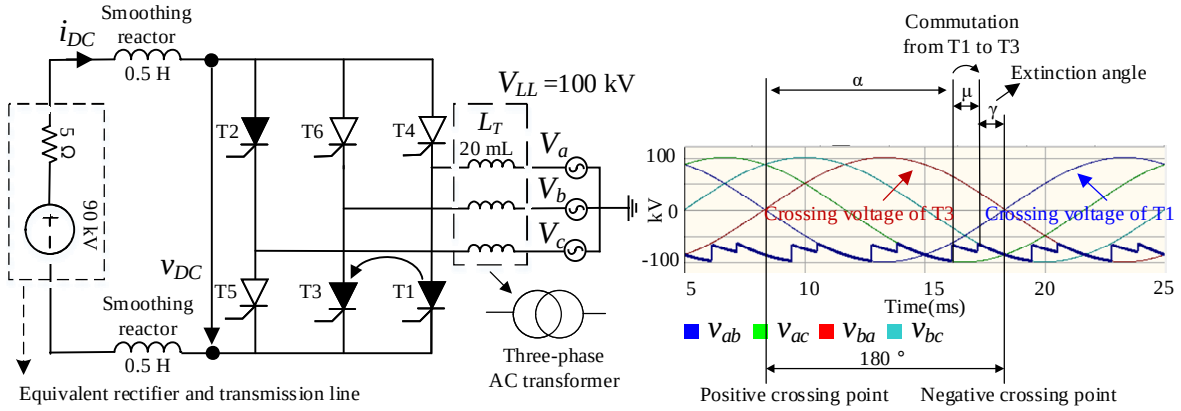
2.2.4.1 How commutation failure occurred

The thyristor cannot be turned off via the control. It can only be turned off naturally when its crossing voltage is negative, and the passing current reduces to 0. This characteristic of the thyristor may cause the commutation failure of the LCC-HVDC at some abnormal conditions.

The commutation process from T1 to T3 of the inverter is shown in Fig. 2-9. Before the negative crossing point, the crossing voltage of T3 is positive. When a fire pulse is sent to the gate of T3, T3 will be turned on. And the commutation will start from T1 to T3. If the commutation process can be finished before the negative crossing point, the T1 will be closed naturally. If the commutation process cannot be finished before the negative crossing point, the T1 will not be closed because its crossing voltage is positive after the negative crossing point. and T3 will be turned off when the DC current fully comes back to T1. The situation is named as commutation failure. After the commutation failure of T3, T2 will commutate to T4, which will cause the short circuit between two output ports, because T1 and T4 are on. This is a significant fault which will interrupt the DC power transfer fully.

An extinction angle γ is defined to describe the margin between the finish point of the commutation and the negative crossing point. The inverter normally uses extinction angle control to maintain the safe margin of the extinction angle (typically is 20°). And the relationship between DC voltage and extinction angle is shown below:

$$V_{DC} = \frac{3}{\pi}\sqrt{2}V_{LL\_rms}\cos\gamma - \frac{3}{\pi}\omega L_T I_{DC} \tag{2-2}$$



(a) (b)

Fig. 2-9 Commutation process from T1 to T3 of the inverter

The commutation failure may occur in the inverter rather than the rectifier. Because the fire angle of the rectifier is less than 90°, the starting position of the commutation is far from the negative crossing point.

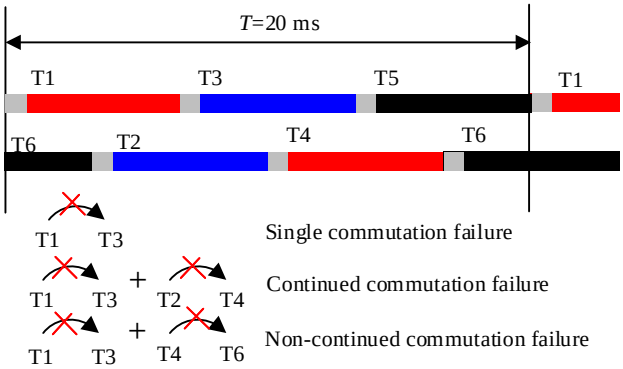
In normal operation, there will not be any commutation failures. However, the suddenly phase shift and voltage dip of the AC voltage will lead the negative crossing point, and the suddenly increased DC current will increase the overlap period, these abnormal conditions are the main reasons to cause the commutation failure.

2.2.4.2 Types of commutation failures

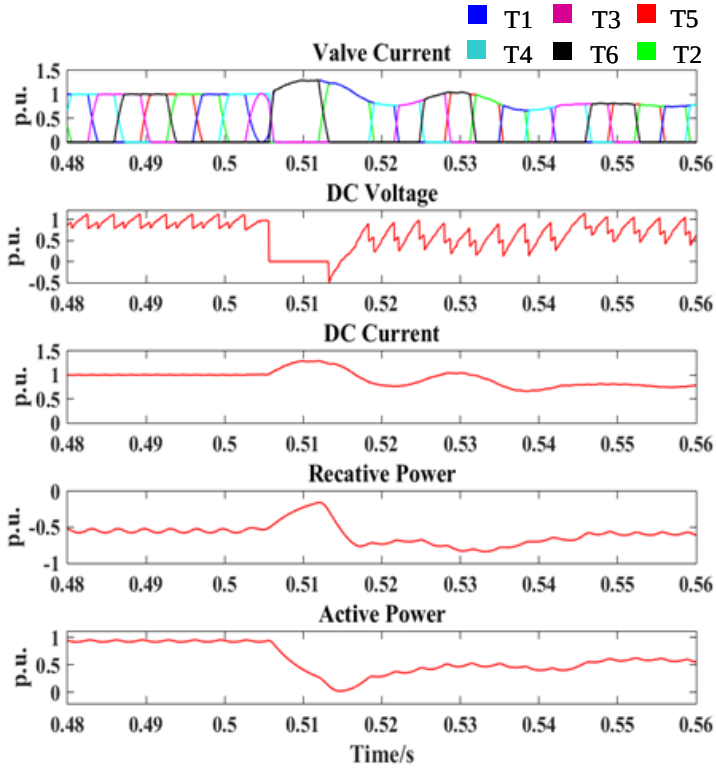
The operation of the six-pulse bridge using thyristor is cyclical. The types of commutation failures are defined in one cycle. The operation sequence of the thyristors in one six-pulse bridge is shown in Fig. 2-10 (a). If one commutation failure occurs in one cycle, it is single commutation failure. If two adjacent commutations are failed in one cycle such as T1 to T3 and T2 to T4, it is defined as a continued commutation failure. If two non-adjacent commutations are failed in one cycle such as T1 to T3 and T4 to T6, it is defined as a non-continued commutation failure.

The behaviours of these three commutation failures are shown in Fig. 2-10 (b-d). The tested system is shown in Fig. 2-8 (a). All types of commutation failures occurring in the

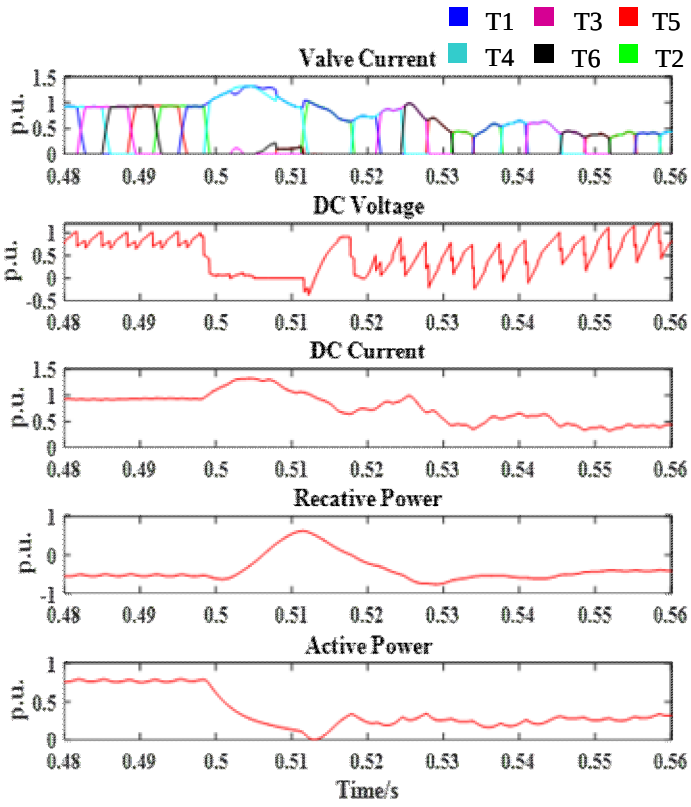
inverter will cause the interruption of active power transportation. The continued commutation failure and non-continued commutation failure need longer time to recover its DC voltage and DC current. And the continued commutation failure causes the most severe influence to the reactive power.



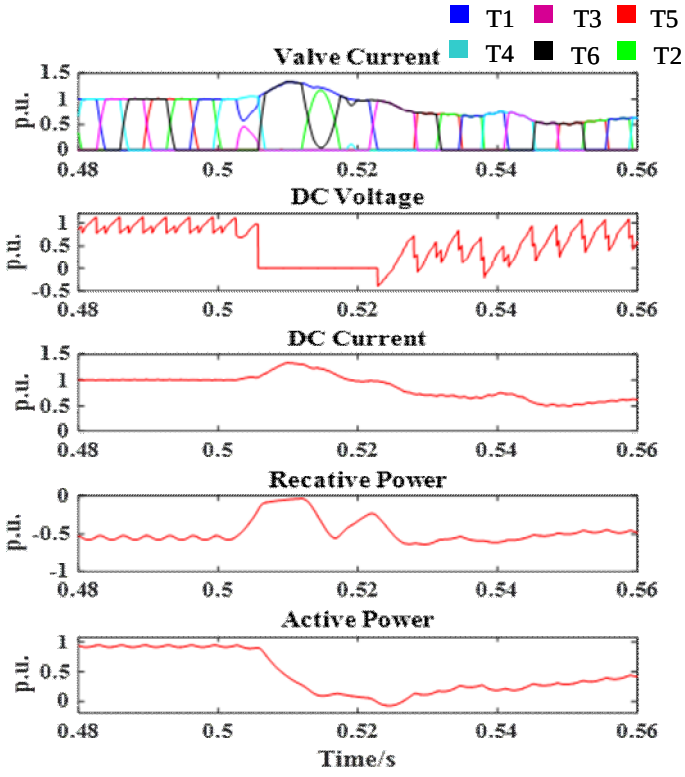
(a) Types of commutation failures



(b) Single commutation failure



(c) Continued commutation failure



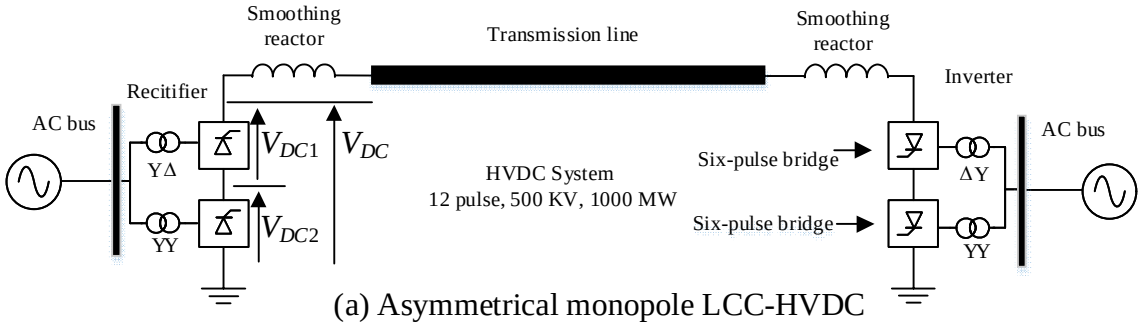
(d) Non-continued commutation failure

Fig. 2-10 Types of commutation failures and their behaviours

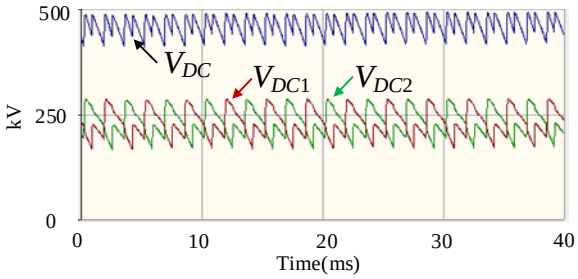
2.2.5 Configuration of line-commutated converter HVDC

LCC converter normally uses a 12-pulse bridge consisting of two six-pulse bridges, see Fig. 2-11. There is a 30° phase shift between the output DC voltages of two six-pulse bridges, which results in a 12-pulse total output DC voltage, see Fig. 2-11 (b). A 12-pulse DC voltage consists of fewer harmonics than six-pulse DC voltage. Therefore the requirement of the filters is reduced via using the 12-pulse bridge.

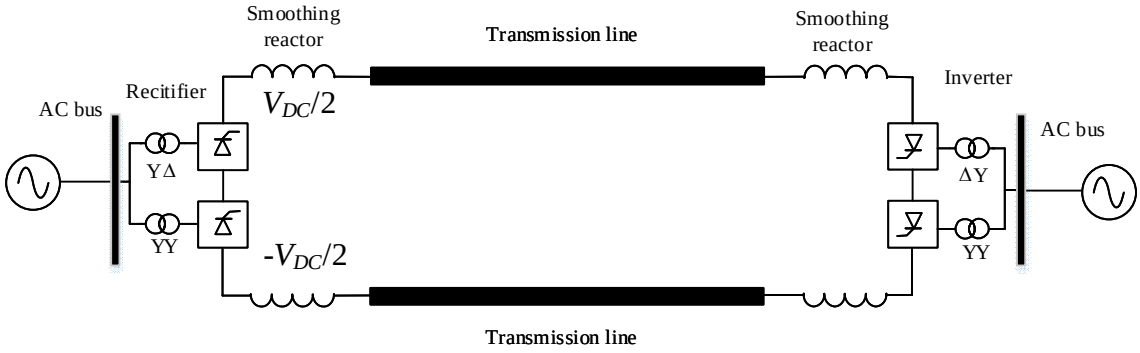
There are three configurations of LCC-HVDC, asymmetrical monopole, symmetrical monopole, and bipole, see Fig. 2-11 (a), (c), (d). Each pole contains a 12-pulse bridge. The asymmetrical monopole LCC-HVDC only has one transmission. Its terminal DC voltage is V_{dc}. The symmetrical monopole LCC-HVDC has two transmission lines. Its terminal DC voltages are $+V_{dc}/2$ and $-V_{dc}/2$. The bipole LCC-HVDC contains two 12-pulse bridges at the rectifier or inverter. It needs two transmission lines and the DC terminal voltages are $+V_{dc}$ and $-V_{dc}$.



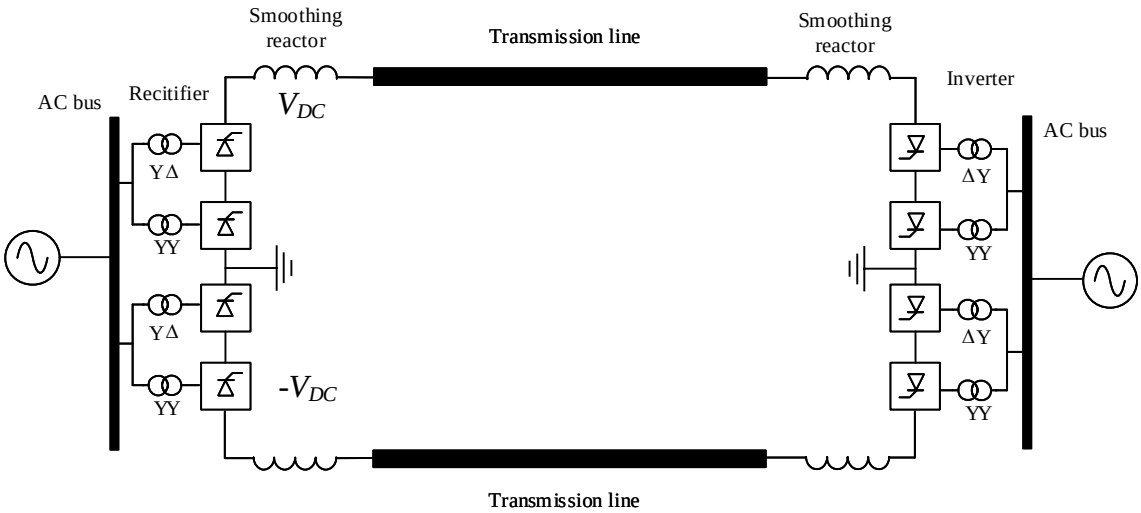
(a) Asymmetrical monopole LCC-HVDC



(b) DC voltage of 12-pulse bridge rectifier



(c) Symmetrical monopole LCC-HVDC



(d) Bipole LCC-HVDC

Fig. 2-11 configurations of LCC-HVDC

2.2.6 Control of line-commutated converter HVDC

In an LCC-HVDC, normally the inverter takes the extinction angle control to maintain a safe margin of the extinction angle in order to avoid the commutation failure because of the small extinction angle. In an inverter, controlling the extinction angle is equivalent to controlling the DC voltage, their relationship is shown in Eq. 2-2. To achieve the power transportation, the rectifier will control the DC current or DC power. The control block is shown in Fig. 2-12. It should be noticed that the load centre is located on the AC side of the inverter, and the power demand of the load centre will send to the rectifier to control the power transportation.

There are many auxiliary controls such as fire angle compensation control, voltage dependent current limitation control and so on, which have not shown in Fig 2-12. These auxiliary controls can enhance the stability of the LCC-HVDC. The information about these auxiliary controls are introduced in [20].

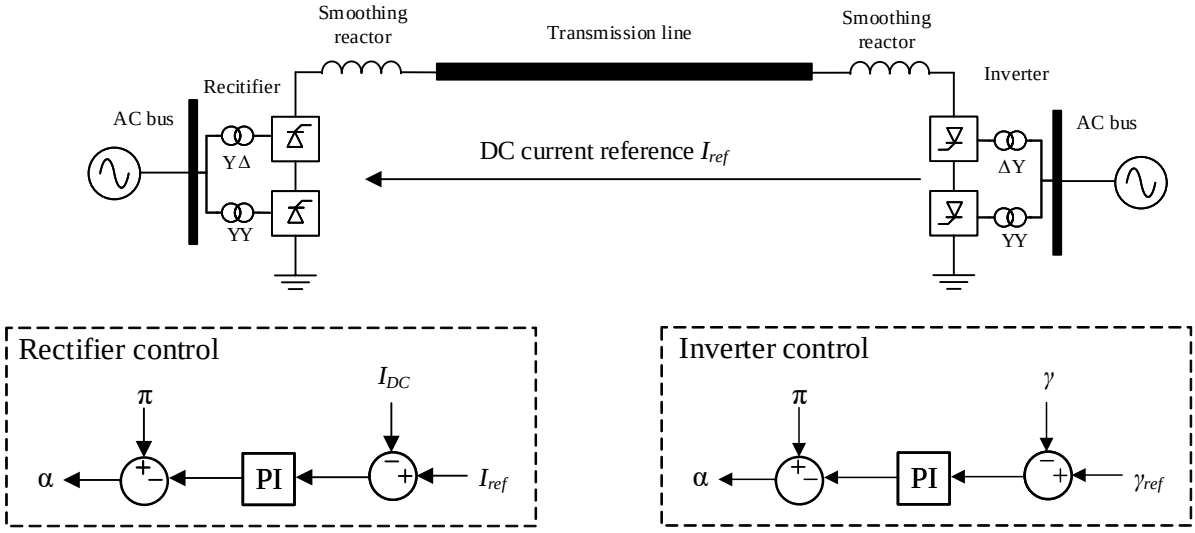


Fig. 2-12 Simplified control system of an LCC-HVDC

2.3 **Modular multilevel converter HVDC**

2.3.1 Structure of modular multilevel converter

The structure of a MMC is shown Fig. 2-13 (a). One MMC consists of three phase units. Each phase unit connects to one phase of a AC system. Each phase unit consists of two arms,

upper arm and lower arm. Each arm has n sub-modules (SMs) and an arm inductor. The arm inductor will be mainly used to suppress the circulating current. The detailed information about the design of this arm inductor is described in [21].

The sub-module can be half-bridge SM or full-bridge SM. Each SM can be seen as a constant voltage source. For a half-bridge SM, its output voltages are $+V_C$ or 0. For a full-bridge SM, its output voltages are $+V_C$, 0, and $-V_C$. The operations of a half-bridge SM and a full-bridge SM to insert corresponding voltages are shown in Table 2-2.

Table 2-2 operations of SMs

	Half-bridge SM			Full-bridge SM				
Operation	S1	S2	V_{SM}	S1	S2	S3	S4	V_{SM}
Insert	on	off	$+V_C$	on	off	off	on	$+V_C$
Bypass	off	on	0	on	off	on	off	0
Insert				off	on	on	off	$-V_C$

Both half-bridge SM and full-bridge SM can be used in a MMC to achieve AC/DC conversion. The capital cost of a half-bridge MMC is much lower than that of the full-bridge MMC because of two IGBTs reduction for each SM. Taking into account of the capital cost of a converter, all commissioned MMC projects use half-bridge SMs.

Compared to the half-bridge SM, the full-bridge SM can block the DC fault. As shown in Fig. 2-13 (b), after the SM is blocked, the fault current can flow through the diode of S1. In the full-bridge SM, there is no current path after blocking. Therefore, the full-bridge MMC can block the DC fault rapidly. The half-bridge MMC normally need AC breakers to bock the fault, which the speed of fault blocking is much lower than that of a full-bridge MMC.

Another advantage of the full-bridge SM is that a MMC using full-bridge SMs can reduce the operation DC voltage. More details are described in [22].

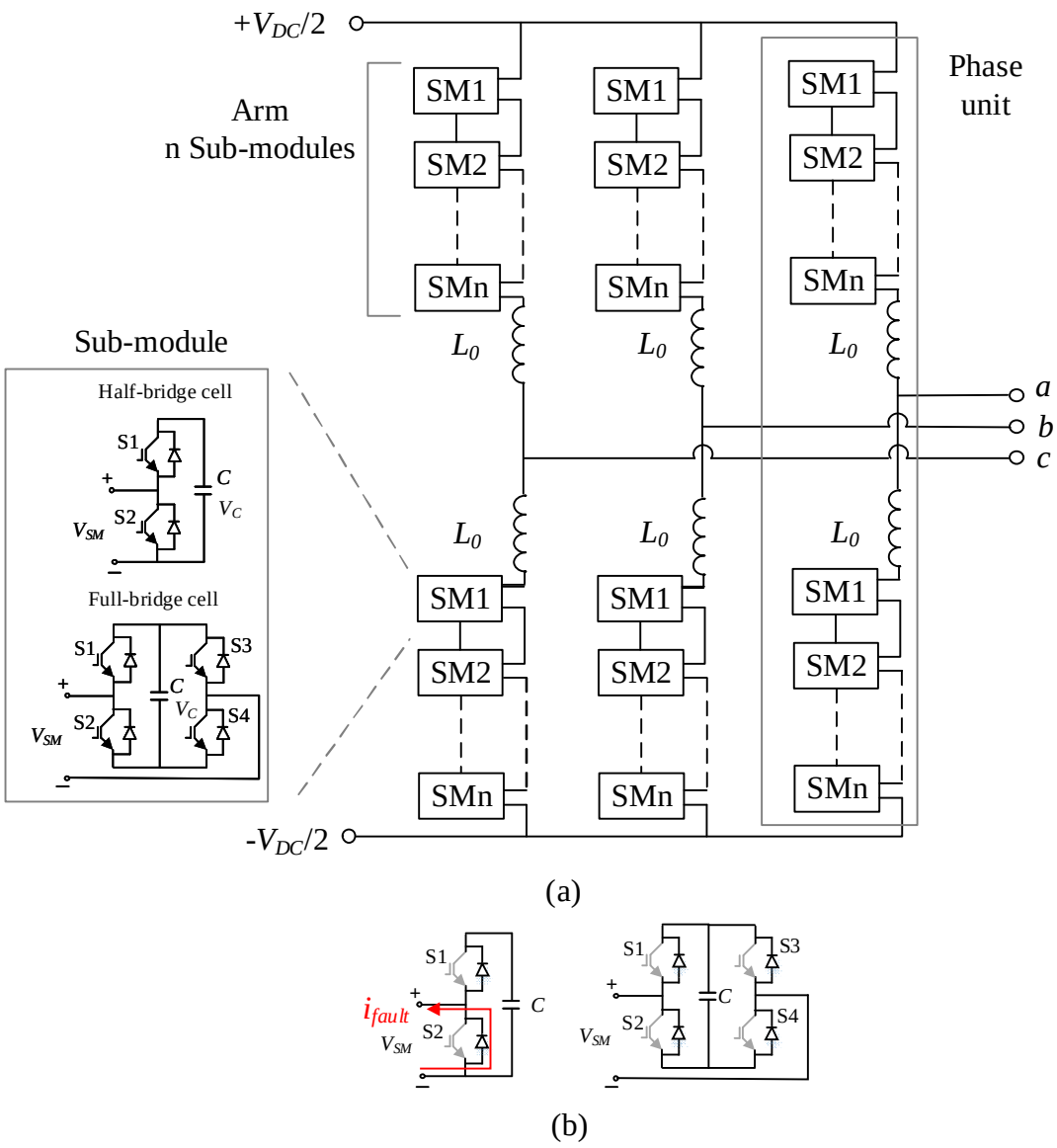


Fig. 2-13 modular multilevel converter

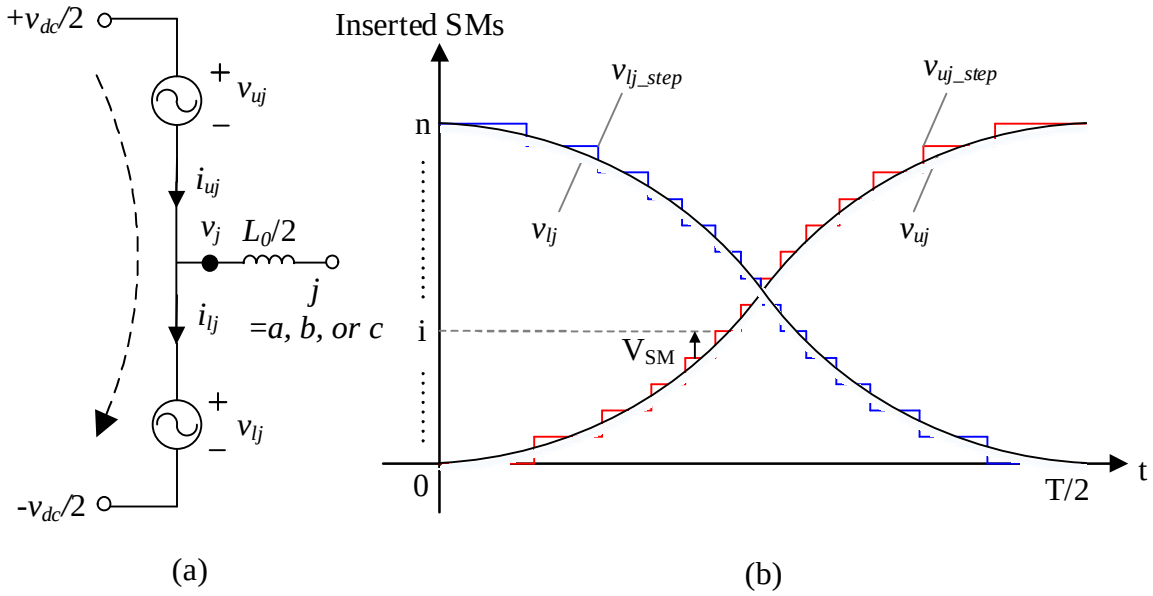
2.3.2 AC/DC conversion

All SMs of one arm can be seen as a controllable AC voltage source, and output AC voltage of a MMC is generated via controlling each controllable AC voltage source locating on all arms. The equivalent circuit of one MMC phase unit is shown in Fig. 2-14 (a), the upper arm voltage and lower arm voltage are denotated as v_u and v_l. The DC voltage is supposed to constant value $+V_{dc}/2$ and $-V_{dc}/2$. If the desired terminal AC voltage is v_{tj}, according to the KVL, the arm voltages should be controlled as:

$$v_{uj} = \frac{V_{DC}}{2} - v_{tj}(a) \qquad (2-3a)$$
$$v_{lj} = \frac{V_{DC}}{2} + v_{tj}(b) \qquad (2-3b)$$

The arm voltages are drawn in Fig. 2-14 (b), if $v_{tj} = \frac{V_{DC}}{2}\cos(\omega t)$. From the Eq. 2-3, we can conclude:

- The total voltage of all SMs of one arm is $nV_C = V_{DC}$
- The magnitude of the terminal AC voltage belongs to [0, $\frac{V_{DC}}{2}$]
- The DC voltage is impossible to be changed using the half-bridge SM, and maintain the same AC voltage magnitude at the same time.



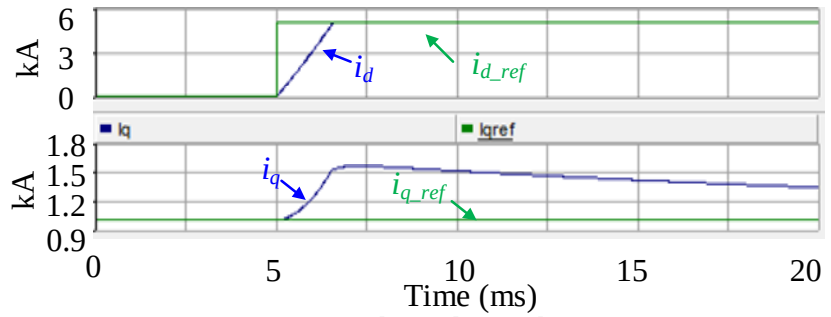
(a) (b)

Fig. 2-14 principle of AC/DC conversion of a MMC

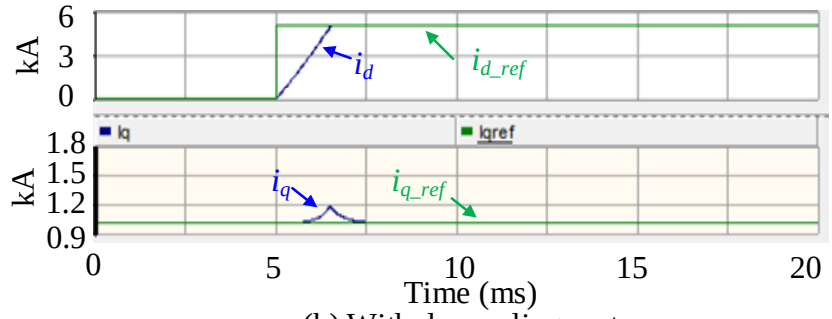
2.3.3 Control of a MMC

The control of a MMC has two layers: inner control and outer control, and is based on the d-q frame, see Fig. 2-16. The inner control must be a current control to maintain the current at a safe range, which avoids the overcurrent of IGBTs applied in a MMC. The outer control has more freedom, the control targets depend on the request of the system.

The inner control contains a decoupling part, that is because the abc-dq transfer will introduce q elements into d axis control and d elements into q axis control. Therefore, to avoid the influence between d axis and q axis controls, the decoupling part is added. A case study is shown Fig. 2-15. i_d changes from 0 kA to 5 kA at 5 ms, if there is no decoupling part, the i_q is influenced a lot, see Fig. 2-15 (a). if there is a decoupling part, the step change of i_d will not have a great influence on i_q.



(a) Without decoupling part



(b) With decoupling part

Fig. 2-15 i_d step change of inner current control

For an outer control, the active power P, DC voltage V_{DC}, or DC current I_{DC} can be controlled via the d axis. The reactive power Q or AC voltage V_{AC} of the point of common coupling (PPC) can be controlled via the q axis.

The output is the desired terminal AC voltage, and the final arm voltage reference is calculated via Eq. 2-3.

The MMC control system is a mature control system, for more information about this control system including principle of the control, parameter design of PI controller, abc-dq transformation, and phase-locked loop, please check reference [23].

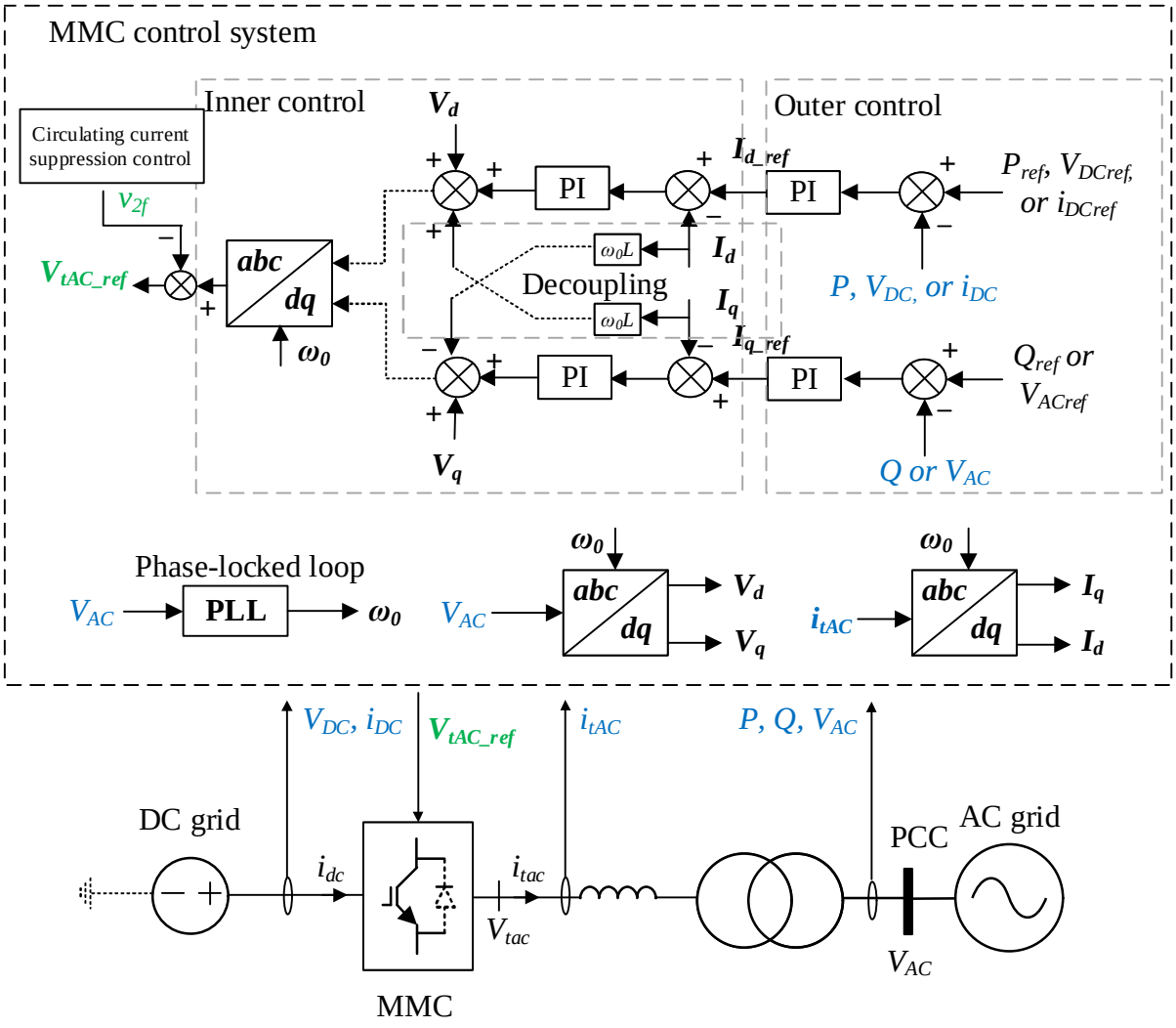


Fig. 2-16 control system of modular multilevel converter

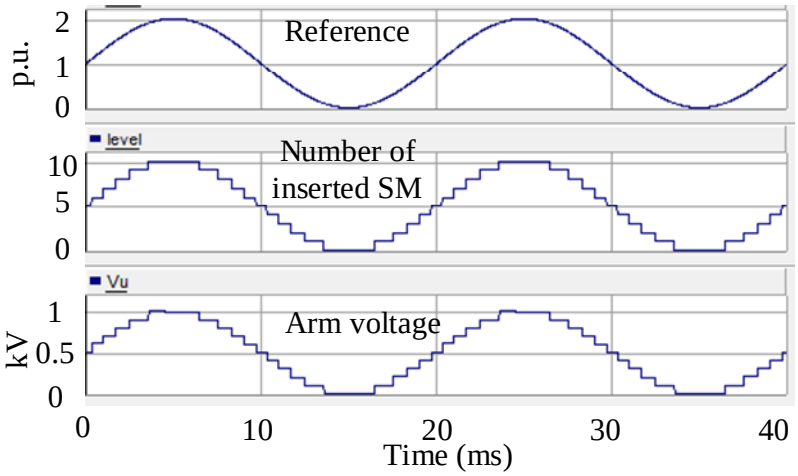
2.3.4 Modulation of MMC

The arm voltage reference cannot be read by SMs, therefore the modulation technology is requested to transfer the arm voltage reference to switching sequences of SMs. Nearest level modulation (NLM) is the most commonly used because of high efficiency and low switching losses. The alternative is phase-shift pulse width modulation (PS-PWM), which is less efficient and causes more switching losses.

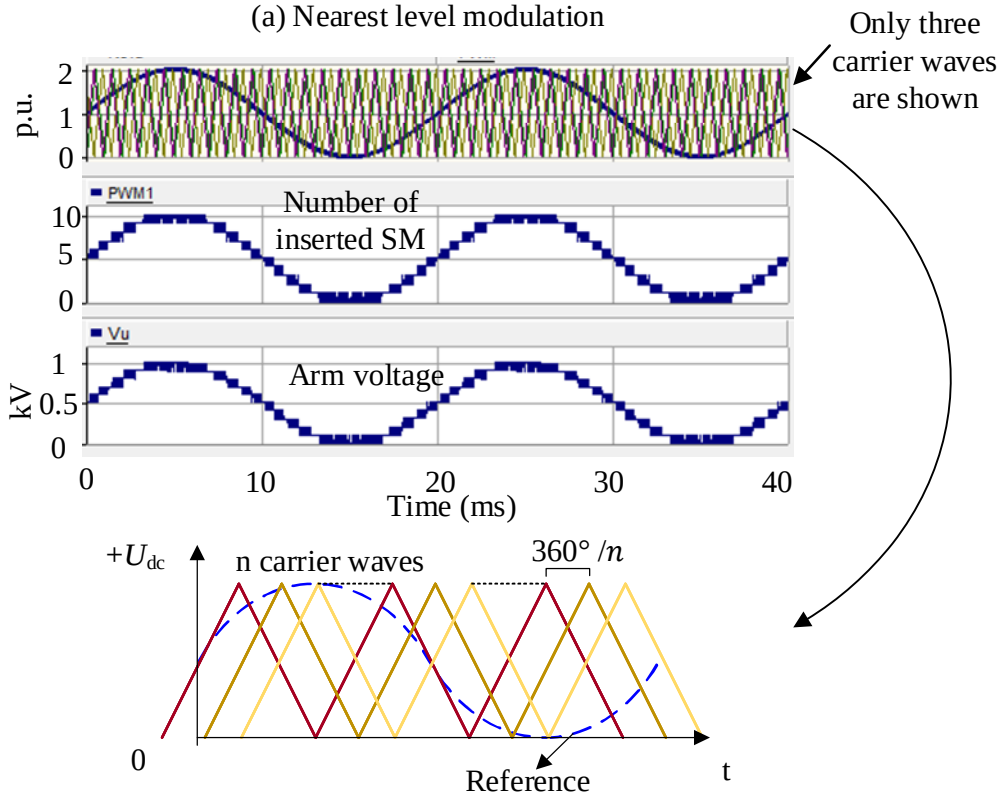
A 11-level MMC that contains 10 SMs per arm is used to show operation of these two modulation technologies, see Fig. 2-17. The reference is changed into steps with the same shape according to the rounding function. Each step means the equivalent number of SMs are inserted. the inserted SMs operate at the condition that S1 is on and S2 is off, see Table 2-2.

The other SMs are bypassed, which means S1 is off and S2 is on. And the arm voltage will follow its reference, as shown in Fig. 2-17 (a). The DC voltage of each SM is 0.1 kV.

The principle of PS-PWM is shown in the bottom figure of Fig. 2-17 (b), each SM need a carrier wave, and the number of inserted SM is varied at each step. Therefore PS-PWM needs more computing time and switching losses. For more details about the modulation technologies, check reference [24][25].



(a) Nearest level modulation



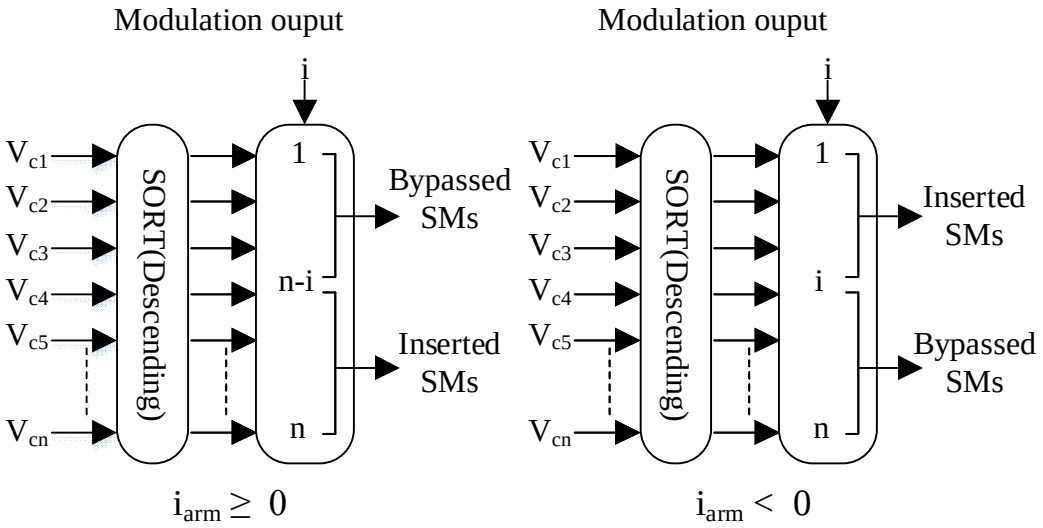
(b) Phase-shift pulse width modulation

Fig. 2-17 11-level modular multilevel converter

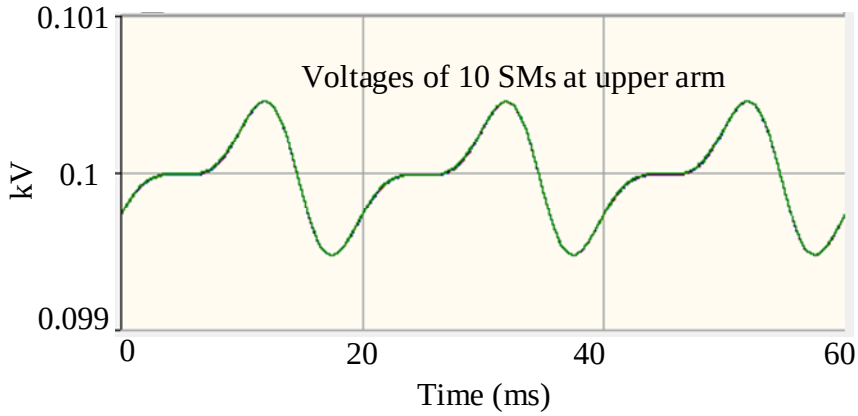
2.3.5 Voltage balancing control

After the modulation, the arm reference has been transferred to the switching sequence of SMs, which shows how many SMs will be inserted and the others will be bypassed at each step. One SM cannot hold its DC voltage all the time, because it is not real constant DC voltage source. The capacitor in one SM will be charged or discharged by the arm current. when a capacitor is charged, its voltage will increase and vice versa. To maintain relative constant and same voltages of SMs, a voltage balancing control is needed to charge or discharge each SM on balance.

The directions of upper and lower arm currents are shown in Fig. 2-14 (a), when the arm current is positive, the inserted SMs will be charged and vice versa. At i step, the number of inserted SMs is i. When the arm current is positive, i SMs with lowest DC voltages should be inserted and vice versa. Before i SMs is inserted, all SMs of one arm should be sorted first according to their voltages. The sorting method is typically based on bubble sorting method, see Fig. 2-18. The voltages of all SMs at one arm with voltage balancing control are shown in Fig. 2-18 (b)



(a) operation of voltage balancing control



(b) Voltages of SMs at one arm

Fig. 2-18 Voltage balancing control

2.3.6 Circulating current suppression control

The circulating current existing in each phase unit is an inherent problem of a MMC. It increases the arm current and the voltage ripples of SMs. Except fundamental AC voltage, the voltage of each SM contains other voltage harmonics. The circulating current is equal to these voltage harmonics divide the inductance of arm inductor. To identify the exact relation between a arm inductor and the circulating current, please check reference [26].

A 101-level ±80 kV 50MW MMC is built to describe the circulating current detailly. The voltages of all SMs at one arm are exactly same due to the voltage balancing control. One voltage of one SM is selected to do the harmonic analysis, the result is shown in Fig. 2-19. In one phase unit, both SM voltages of the upper arm and the lower arm have the same voltage

harmonic magnitude, and their 2nd-order voltage harmonic magnitudes are much higher than the magnitudes of other voltage harmonics. Their 2nd-order voltage harmonics have the same phase shift. Therefore, we can conclude:

- The 2nd-order current is the main component of circulating current
- The circulating current will not flow out to the AC side, because the upper arm and the lower arm have exactly same 2nd-order voltage harmonics in terms of the magnitude and the phase shift.
- The circulating current will not flow out to the DC side because of the symmetrical three phase units.

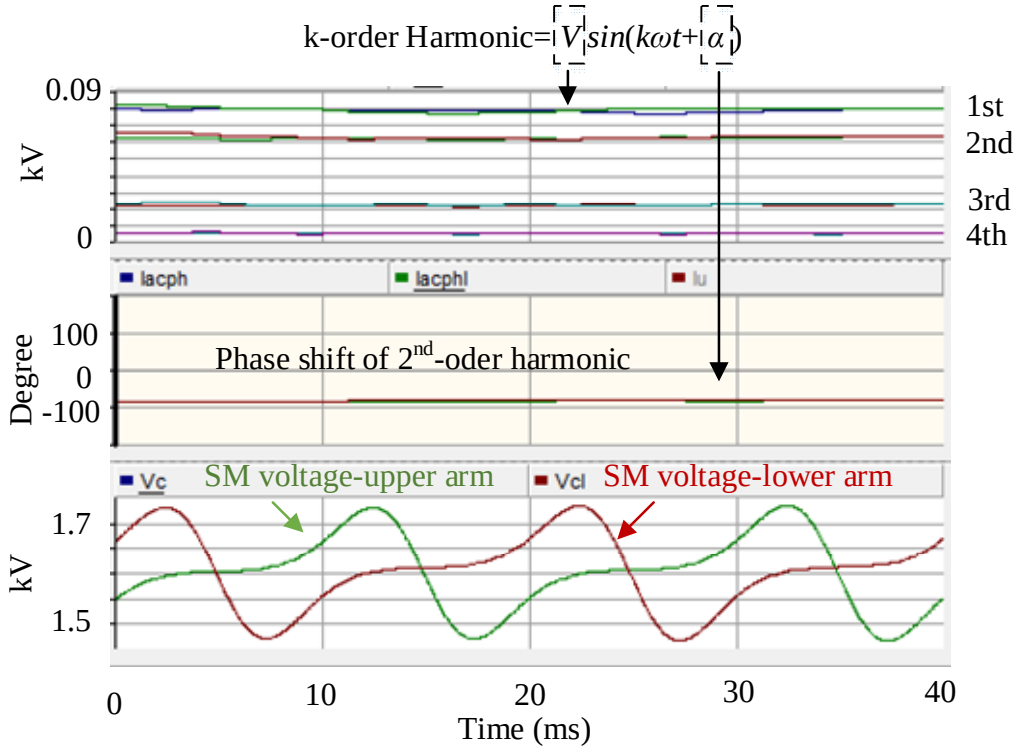


Fig. 2-19 Harmonic analysis of the voltage of SMs at upper arm and lower arm of Phase A

The suppression of the circulating current via the control will bring advantages as below:

- Reducing the arm current, which avoid using large arm inductors and high current ratings of IGBTs
- Reducing the voltage ripples of SMs, which avoid using large capacitors

The equivalent 2nd-order harmonic circuit of one phase unit is shown in Fig. 2-20. As shown in Fig. 2-20 (a), in terms of KVL, the relations between the circulating current (i_{2f}) and 2nd-order voltage harmonics of the upper arm (v_{uj_2nd}) and the lower arm (v_{lj_2nd}) can be obtained as:

$$v_{uj\_2nd} + L_0 \frac{di_{2f}}{dt} + L_0 \frac{di_{2f}}{dt} + v_{lj\_2nd} = 0 \tag{2-3}$$

As mentioned previously, $v_{uj\_2nd} = v_{lj\_2nd}$. Suppose that $v_{uj\_2nd} = v_{lj\_2nd} = v_{2f}$, then we have:

$$-L_0 \frac{di_{2f}}{dt} = v_{2f} \tag{2-4}$$

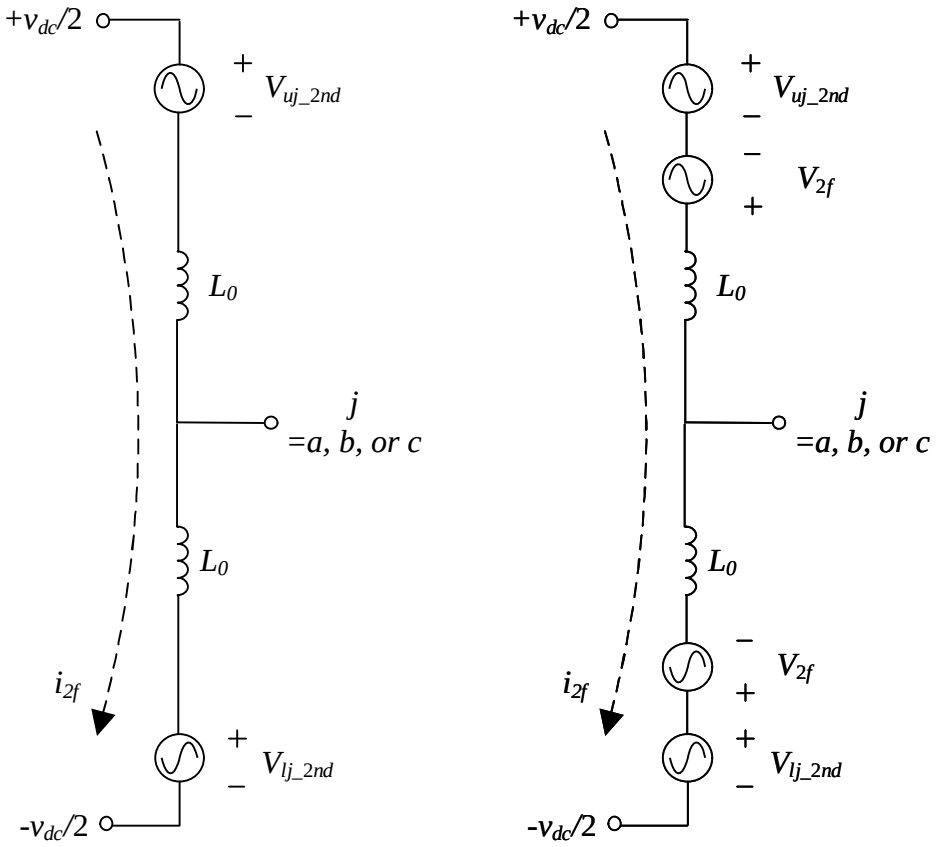
If two -v_{2f} 2nd -order AC voltage is inserted in the upper arm and the lower arm respectively, the circulating current will be eliminated. As shown in Fig. 2-20 (b), according to the KVL, the relations between the circulating current and the 2nd-order voltage is obtained below:

$$v_{uj\_2nd} + L_0 \frac{di_{2f}}{dt} + L_0 \frac{di_{2f}}{dt} + v_{lj\_2nd} - 2v_{2f} = 0 \tag{2-5}$$

Using v_{2f} to replace v_{uj_2nd} and v_{lj_2nd}, the following equation is obtained:

$$L_0 \frac{di_{2f}}{dt} = 0 \tag{2-6}$$

i_{2f} will be a constant value (can be 0 via control) according to 2-7. A circulating current suppression control is built based on Eq. 2-5 and 2-6 as shown in Fig. 2-21, the control reference is to control the circulating current to be 0. The circulating current suppression control is imbedded into the control of a MMC, as shown in Fig. 2-16



(a) Without circulating current suppression control

(b) With circulating current suppression control

Fig. 2-20 Equivalent 2nd-order harmonic circuit of one phase unit

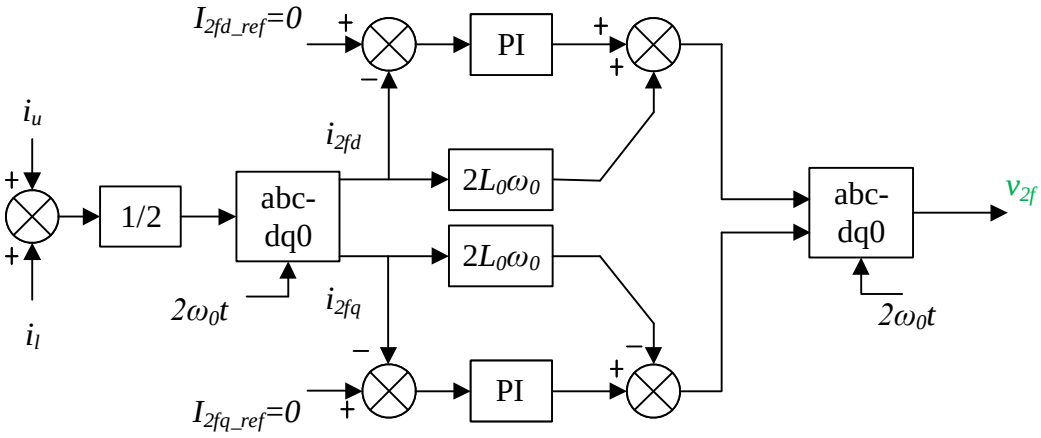


Fig. 2-21 Circulating current suppression control

The performance of the circulating current is verified in a 101-level ±80 kV 50MW MMC, see Fig. 2-21. the circulating current suppression control is activated at 40 ms, the voltage ripples of SMs locating on the upper arm and the lower arm is reduced significantly. The currents of the upper arm and the lower arm is reduced after activating the circulating

current suppression control. The bottom figure is shown that the circulating current is eliminated by the control.

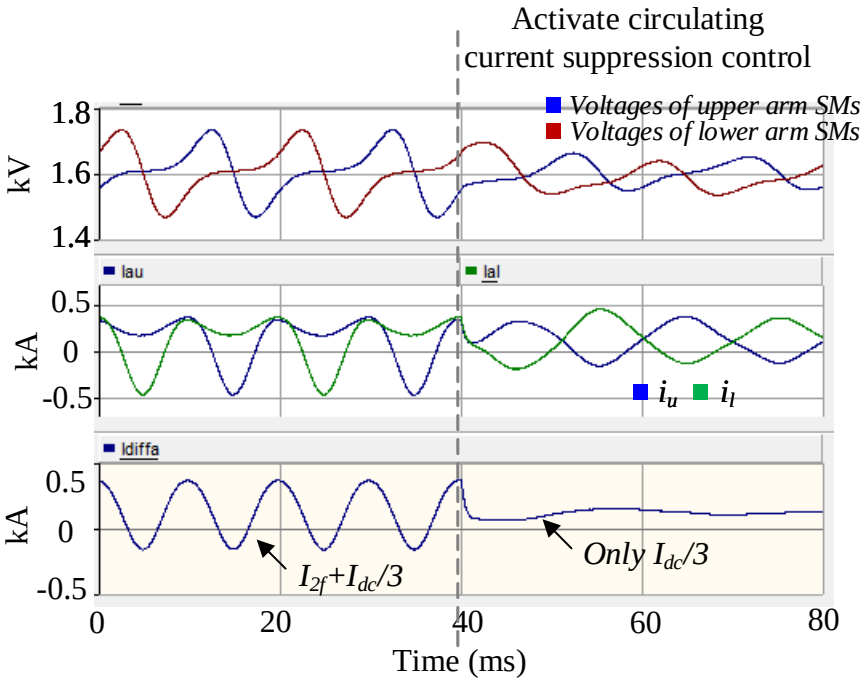


Fig. 2-22 Performance of circulating current suppression control (Phase A)

2.4 **Transmission lines**

Transmission lines are applied in HVDC system when there is a need for long-distance power transmission. Both overhead lines and cables are used for HVDC transmission. The load of an overhead line is limited by the thermal expansion (sag) and the annealing temperature of the conductor. Cables are mainly limited by the ageing of the insulator material. Comparing to buried cables, bare overhead lines working in lower temperature environment. To keep the same life with overhead lines, cables have to operate at lower temperatures.

2.4.1 Overhead lines

Overhead lines are the most economical means for bulk power transmission over a long distance due to its low installation cost. The way that HVDC makes use of overhead line is similar to AC system. There is no big difference between HVDC overhead line' tower and AC's. Of course, Overhead lines are susceptible to lightning strikes. Overhead lines are widely

used in HVDC projects, and the voltage rating and power rating reach to 1100kV and 10GW separately [27].

2.4.2 HVDC cables

Since the heat requirements of a cable system are more stringent than that of an overhead line, a higher conductor section is applied to the cable to reduce the resistance when the same amount of power demand is requested.

HVDC cables are mostly used in a submarine application for connection offshore wind farms to an inland load centre or power transmission over a long distance in the sea, that overhead line cannot be used. Smaller right-of-way makes HVDC cables be used for land power transmission in the city area. Most of the VSC-HVDCs are used for offshore wind power collection with cables.

HVDC cables usually consist of a conductor core, semiconductor screen, main insulation, sheath, armouring, and related accessories. The different characteristics of dielectric materials lead to different electrical, mechanical and thermal performance. HVDC cables are categorized into five types according to the dielectrics [28][29]: Oil-filled DC cable, Mass-impregnated cable (MI cable), extruded DC cable, gas insulated cable, superconducting cable. Today, commercial HVDC projects have been shown that MI cables and extruded cables, as shown in Fig.2-23 and Fig. 2-24, are the most suitable choices for HVDC transmission.

MI cables are defined as “solid” insulation system since there is no free oil contained in the cable. The insulation of MI cables is mass-impregnated and non-draining paper. High-density papers (≈1000 kg/cm^3) can provide higher dielectric properties. The cable length in principle is unlimited due to no external pressure and oil feeding request. As a proven reliable cable technology, MI cables have served in HVDC transmission for over 60 years. Recently, the new insulation utilizing Laminated polymeric film and paper improves the maximum conductor temperature from 55 °C to 85 °C, that increases the rating of MI cable . Such MI

cables have been applied in Westernlink project rated at 600 kV and 2200 MW [30]. Conductor sizes are typically up to 2500 mm^2.

Extruded DC cables are relatively new developments. In 2002, the first extruded cables rated at 500kV 3000MW were developed in a Japanese laboratory. To date, this cable technology has been applied in the real project up to 320 kV and 1000 MW. ABB announced the first 525 kV, 2600 MW extruded cable system in 2014 [31]. Voltage polarity reversal will enhance electric field and cause permanent failure in the insulation. Extruded cables are normally applied in VSC-HVDC because it only changes current direction to reverse the power flow. Extruded cables show a promising future in UHVDC power transmission by using the improved XLPE materials. The advantages over MI cables are shown below [32]:

- A higher conductor temperature can be used, giving a more compact cable for the same power rating;
- Lighter moisture barriers can be used, giving a lighter cable;
- Joining of extruded cables is much simpler and requires less skill;

Intensive studies of space charge behaviour, ageing, temperature and reliability have been carried out, and higher performance of extruded cables is still under developing.

Fig. 2-23 HVDC MI cables

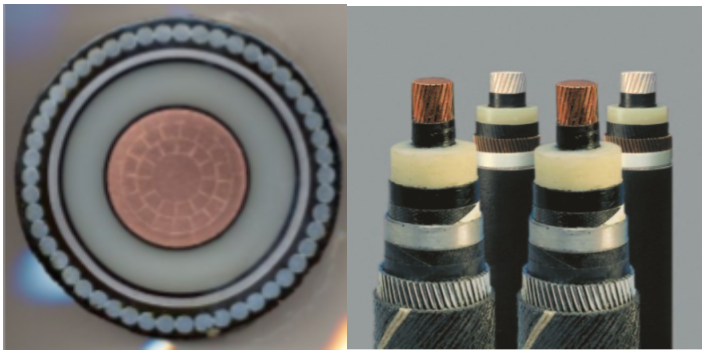


Fig. 2-24 HVDC extruded cable

2.5 Hybrid HVDC circuit breakers

For a well-built HVDC grid, the protection is important due to its ability to minimize the losses in terms of DC faults. Unlike an AC grid, a HVDC grid has much lower inductance, which makes a DC fault propagate quickly. To avoid the significant voltage drop of a HVDC grid, the DC protection is requested to isolate a DC fault within 5 ms. The traditional mechanical breaker used for the AC protection cannot be used for the DC protection due to its low open speed. A string of semiconductor switches can interrupt the fault current quickly, normally less than 1 ms. However, for the HVDC application, a huge number of semiconductors means huge conduction losses.

A mechanical ultra-fast disconnector is invented to open around 2 ms recent years [33]. This ultra-fast disconnector cannot interrupt the DC fault current directly due to no zero crossing points of a DC fault current. Therefore, the concept of a hybrid HVDC circuit breaker that is a combination of mechanical switches and semiconductor switches is proposed to operate with low reduce conduction losses and interrupt the DC fault current quickly. This concept is widely accepted by industries.

The concept of a hybrid HVDC circuit breaker is shown in Fig. 2-25. The current flows through the low loss branch containing the ultrafast disconnector under normal condition. When a DC fault is detected, the fault current is commutated to main breaker branch containing

large number of semiconductor switches. The current limiting inductor is used to limit the increasing speed of the fault current.

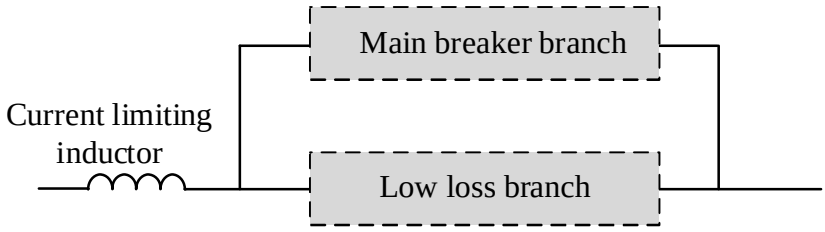
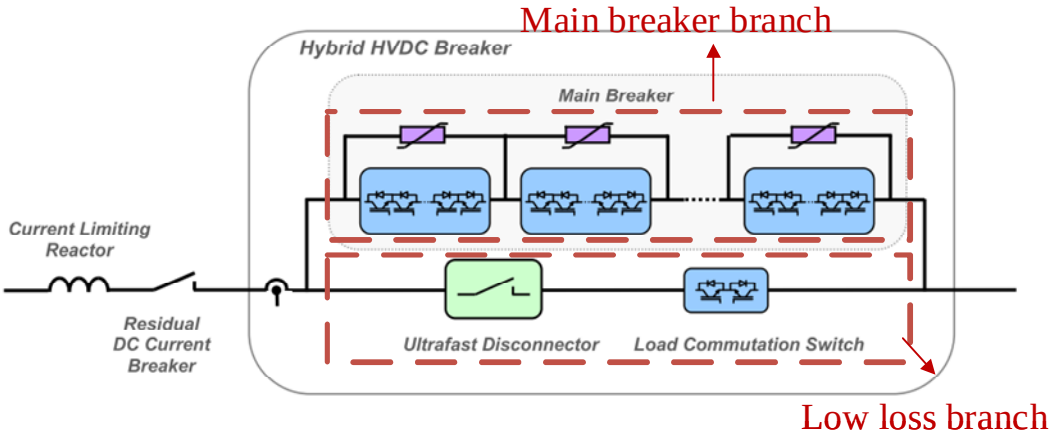
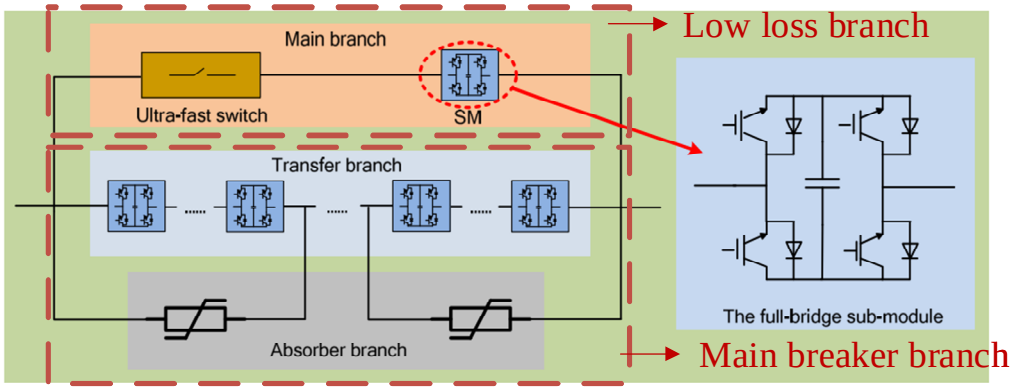


Fig. 2-25 Concept of a hybrid HVDC circuit breaker

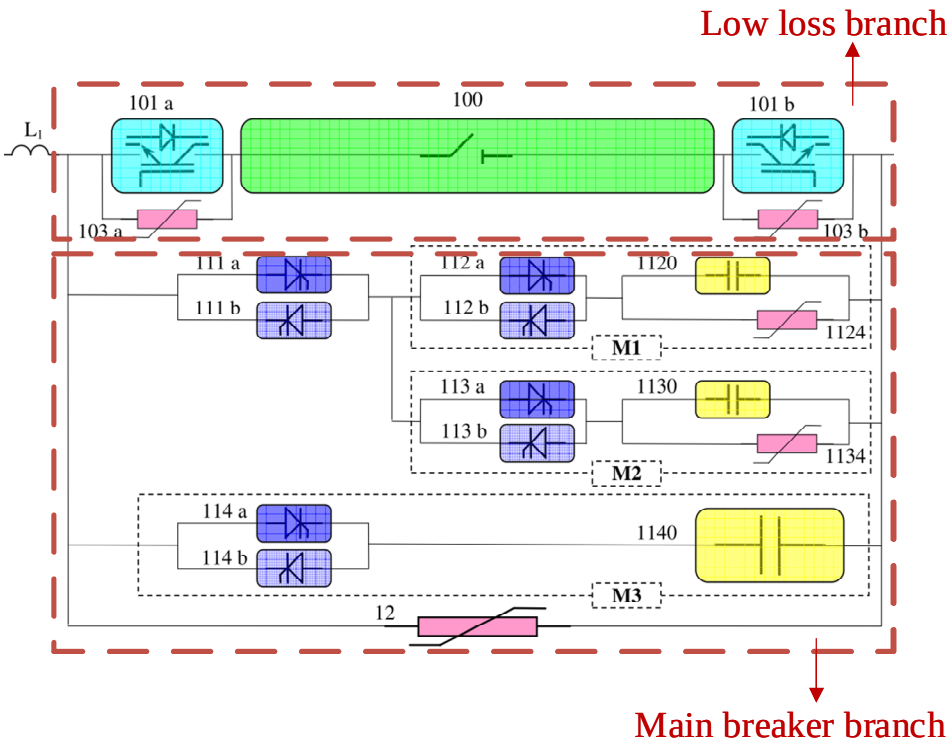
Three prototypes of hybrid HVDC circuit breakers from ABB, GE and SGRI have been produced and tested successfully in recent years. The hybrid HVDC circuit breaker of SGRI have been installed in Zhoushan five-terminal MMC-HVDC system. their topologies are shown in Fig. 2-26. Their fault current interrupting performances are summarized in Table



(a) ABB's hybrid HVDC circuit breaker [34]



(b) SGRI's hybrid HVDC circuit breaker [35]



(c) GE's hybrid HVDC circuit breaker [36]

Fig. 2-26 Hybrid HVDC circuit breakers proposed by industries

Table 2-3 Parameters of the hybrid HVDC circuit breakers proposed by industries

Industry	Voltage rating (kV)	Maximum interrupting current (kA)	Interrupting time (ms)
ABB	320	16	2.25
SGRI	200	15	3
GE	120	7.5	2.5

The hybrid HVDC circuit breaker from ABB is a first proposed hybrid HVDC circuit breaker, therefore it is selected here to explain how a hybrid HVDC circuit breaker works. At normal operation, the current flow through low loss branch, see Fig. 2-27 (a). If a DC fault happens at t1, the fault current flowing through the low loss branch will rise rapidly. The relay of the hybrid HVDC circuit breaker will take some delay to detect the fault. Load commutation switch will block immediately when the fault is detected at t2. Hence the fault current is commutated to the main breaker branch, see Fig. 2-27 (b), commutation time is 250 μs. Ultra-fast disconnector will then start to open at t3 as the current at this branch reaches zero. The

main breaker will have to keep closed until the ultra-fast disconnector opened. Therefore, the fault current flowing through the main breaker will keep rising. Once the ultra-fast disconnector is opened at t4, the main breaker will open to interrupt the fault current. The fault current will thus flow through MOV, see Fig. 2-27 (c) and the fault energy is absorbed by MOV. Once the fault current is cleared, the residual current breaker will ultimately open to disconnect MOV, see Fig. 2-27 (d). The entire interruption time of a hybrid HVDC circuit breaker is around 5 ms. The fault current distribution within a hybrid HVDC circuit breaker is shown in Fig. 2-27 (e).

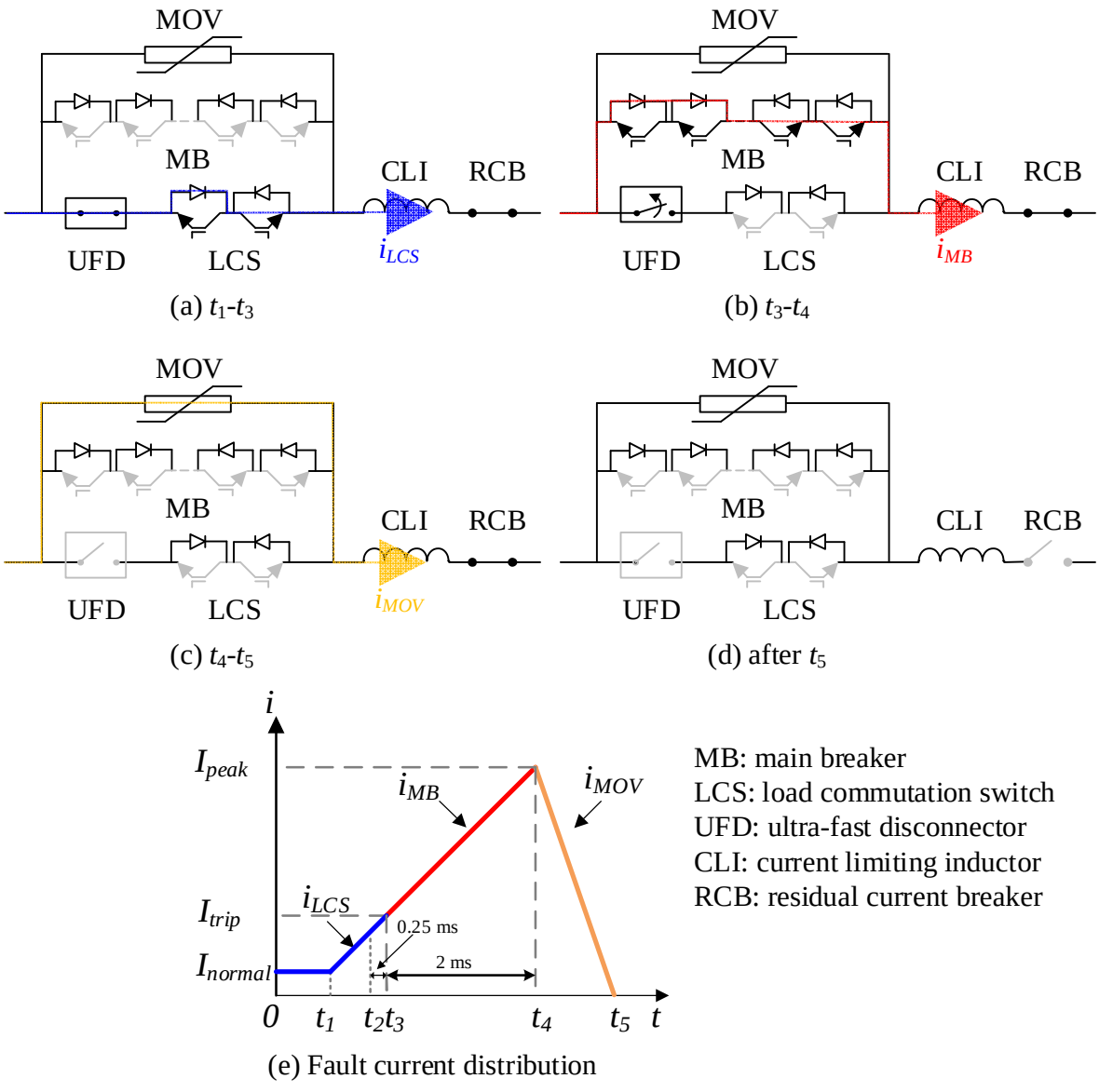


Fig. 2-27 Operation of ABB's hybrid HVDC circuit breaker

The hybrid HVDC circuit breaker provide a feasible solution for a HVDC grid protection. However, its capital cost is high due to the use of a large amount of semiconductor switches in a main breaker.

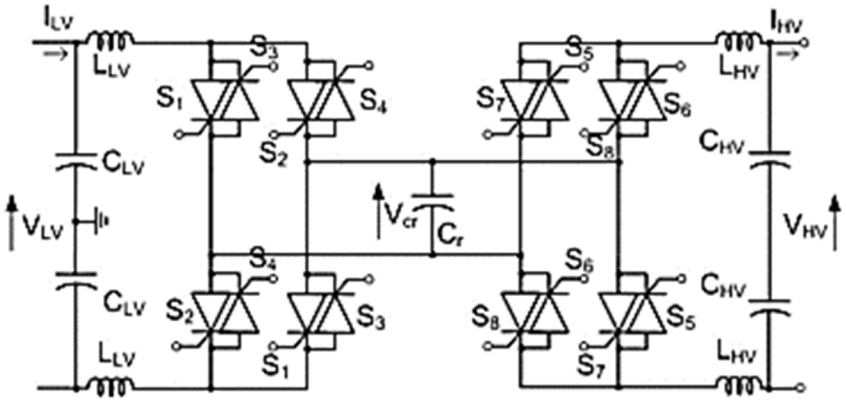
Many academic researches have been done to reduce the cost of HVDC breaker and may be transferred to products by industries. For a HVDC grid protection, many studies (including a patent of ABB) [37][38][39] work on sharing main breaker branches among hybrid HVDC circuit breakers which can reduce the size of main breaker branch. Some researches [40] propose the other concept of HVDC breaker named resonant HVDC circuit breaker to avoid the use of the main breaker, which use the combination among reactors to produce the zero-crossing point of DC fault current to let ultra-fast disconnector open.

2.6 **DC transformers**

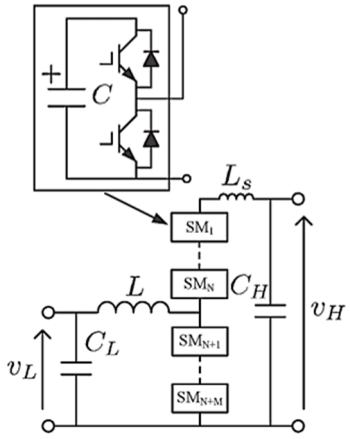
A DC transformer is the device that can interconnect two DC systems physically. The DC systems can be the HVDC grid or DC equipment. There is no one topology of a DC transformer can fit all applications. The topologies of DC transformers depend on the functions (including the increasing/decreasing DC voltage, power flow control, and disturbance isolation) and the operation characteristics of the connected DC systems. The capital cost and losses are the key points of the design of DC transformers.

DC transformer can be grouped into two categories according to their applications. One is the DC transformer for the voltage boost. The other is the DC transformer of the grid interconnection.

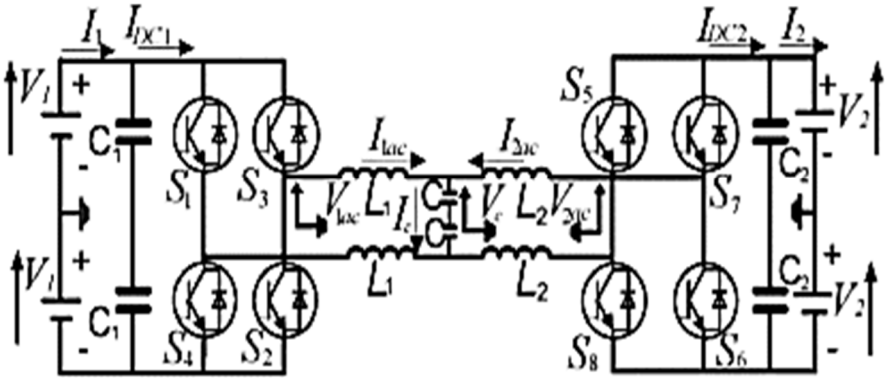
The first category of the DC transformer has a high stepping ratio to boost the DC voltage to a desired level, which normally is applied for the wind power transportation. Its topology can be DC/DC converter using the resonant circuits (see Fig. 2-28 (a)) or the combination of resonant circuits and SMs (see Fig. 2-28 (b)) or the DC/AC/DC converter based on the principles of front-to-front two-level VSCs (see Fig. 2-28(c)).



(a) DC/DC converter using resonant circuits [41]



(b) DC/DC converter based on combination of resonant circuits and SMs [42]

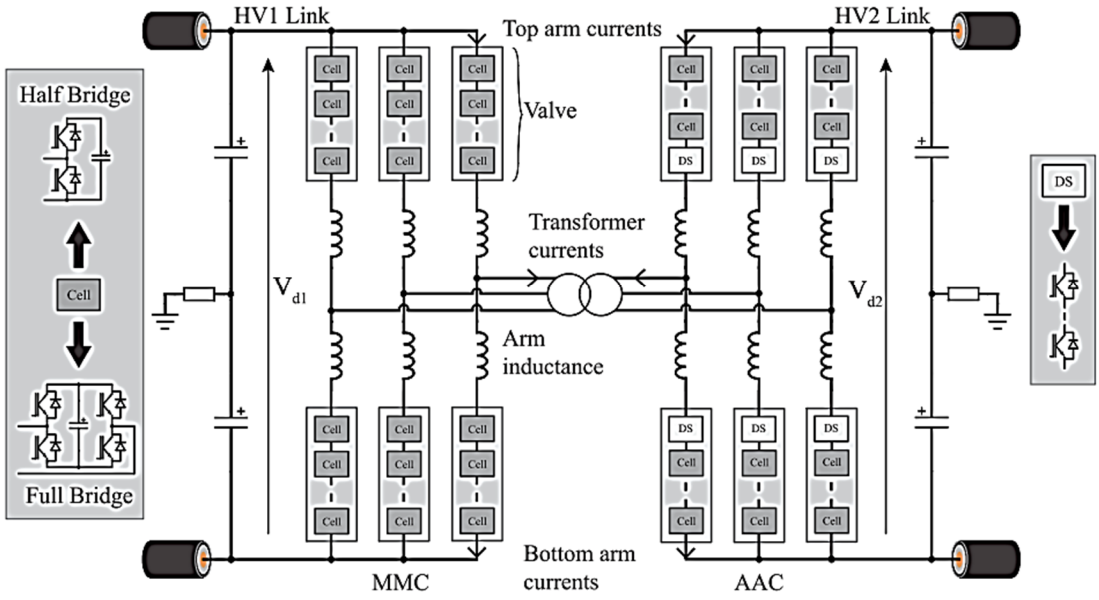


(c) DC/AC/DC converter

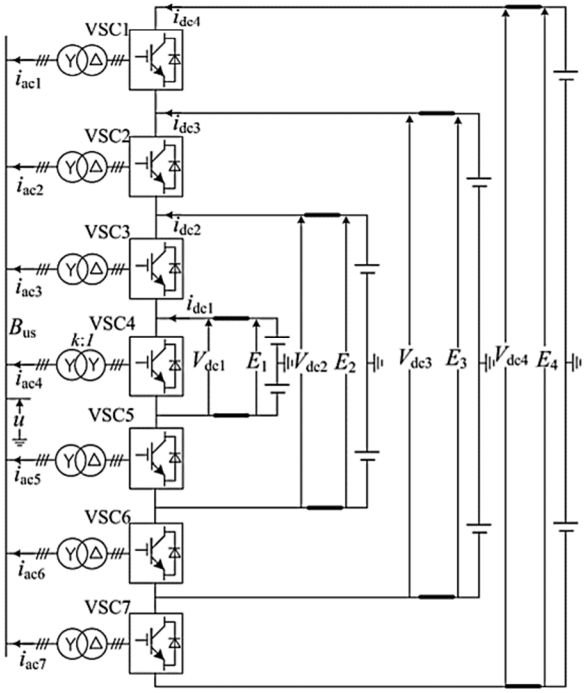
Fig. 2-28 DC transformers for the voltage boost [43]

Even DC transformers for the voltage boost can provide high stepping ratios, the qualities of their output waves are not good enough to interconnect DC grids.

Therefore, the second category of the DC transformers presents. They are DC/AC/DC converters based on the principle of the modular multilevel converter and mainly used to interconnect HVDC systems to provide a constant DC voltage connection and a continues DC power transfer. The MMC based DC/AC/DC converter are initially design as two MMCs through a front-to-front connection. The concern about this type of DC transformer is its high capital cost. Two research directions to reduce its capital cost are proposed. First one is using the high operation frequency to reduce the size of the capacitors of SMs [44][45], as shown in Fig. 2-29 (a). The second one is to share parts of SMs to reduce the number of applied SMs [46][47], as shown Fig. 2-29 (b).



(a) typical front-to-front connected DC/AC/DC converter (its AC voltage operates at high frequency) [44]



(a) typical front-to-front connected DC/AC/DC converter (its AC voltage operate at high frequency) [46]

Fig. 2-29 MMC-based DC/AC/DC converters

CHAPTER 3 Interlink hybrid HVDC circuit breaker

To protect HVDC grids from DC faults, the concept of a hybrid DC circuit breaker is widely accepted due to its low conduction losses and fast interruption speed. For a well-built DC grid, a massive number of hybrid DC circuit breakers have to be installed. This will lead to high capital costs. An interlink DC circuit breaker based on an idea of sharing main breaker branch between two circuit breakers is proposed to reduce the overall costs of circuit breakers in a DC grid. Comparing with existing hybrid DC circuit breakers, the interlink hybrid DC circuit breaker can achieve the same DC fault isolation capability with fewer components. Novel structures of main breaker branches are designed and their parameters are determined to make the interlink hybrid DC circuit breakers be capable for both unidirectional and bidirectional interruption on demand. For a unidirectional interlink hybrid DC circuit breaker, the size of MOVs is reduced by 50%. For a bidirectional interlink hybrid HVDC circuit breaker, the number of IGBTs and MOVs are reduced by 25%. The interlink hybrid DC breakers are verified and compared to the hybrid DC circuit breaker via a three-terminal HVDC grid in PSCAD/EMTDC.

3.1 **Motivation**

he DC grid based on voltage-source-converter (VSC) technology is a preferable choice for transmitting power from remote energy sources to multiple load centers. A major challenge is the DC grid protection. Compared to an AC transmission system, the impedance within a DC grid is much lower. Therefore, the propagation of a fault in a DC grid will be much faster than that in AC systems, which further leads to the fast DC fault current rising and DC voltage drop. The DC fault current has no zero crossing. Traditional mechanical circuit breakers are not suitable for protecting a DC grid from a DC fault. Technical advance in DC circuit breakers which can block a DC fault current in 5 ms is then demanded.

Semiconductor switches, such as IGBT and IGCT, can interrupt fault current within 1 ms. A string of semiconductor switches in series, as a DC circuit breaker, can easily fulfil the speed demand of the protection. However, its state-on loss is high. The loss typically is 30% of the loss of a VSC converter with same voltage rating [48]. A highly efficient cooling system is also required for this breaker to maintain its functionality.

To reduce the on-state loss of pure-semiconductor DC circuit breaker, a hybrid DC circuit breaker (HCB) was therefore proposed to fulfil the speed and loss requirements. Its basic operation principle is that the normal load current flows through the low loss branch in normal condition. When a DC fault is detected, the fault current is commutated to the main breaker branch to interrupt. The prototypes of HCBs were proposed by several manufacturers. ABB has tested its HCB [49] which interrupts a DC fault current up to 16 kA in 2.25 ms. An HCB prototype developed by Alstom Grid [50] interrupts a prospective fault current of 7 kA in 2.5 ms. The State Grid Smart Grid Research Institute has also developed a full-bridge-based HCB [51] which interrupts the fault current up to 15 kA within 3ms.

These HCBs have shown good performance for interrupting DC fault current. However, the costs of a future commercial HCB can be very high. It is estimated that the cost of only main breaker branch of an HCB is as high as one sixth of the cost of a converter with the same voltage rating [52]. In addition, other components within an HCB such as MOVs, and ultra-fast disconnector will further increase the total cost of an HCB. For a well-protected DC grid, each pole of each terminal of one transmission line should be equipped with one HCB, the cost of all HCBs will take a significant part of the cost of a DC grid.

Therefore, many studies on providing a low cost solution for the DC grid protection have been carried out. The low-loss branch is replaced by an SF_6 switch in [54]. Its arc voltage is large enough to commutate the fault current to main breaker branch. The unidirectional HCB using half number of IGBT modules can break unidirectional fault current. Its feasibility for

the protection of a DC grid is studied in [55]. For a DC bus connected with multiple transmission lines, an assembly HVDC breaker [56] uses one grounded active short-circuit breaker as a shared main breaker branch to isolate the fault occurred at any transmission line. Additional auxiliary switches installed on each line are requested. A paralleled MOV [57] to only dissipate the energy of current limiting reactor is proposed and the rating of MOV is therefore reduced. The fault energy is reduced by a hybrid current-limiting circuit [58] to reduce the size of the MOV.

For a terminal connected with multiple transmission lines, a multi-port hybrid DC circuit breaker [59] is proposed to replace the individual hybrid DC circuit breakers locating on each line. By sharing parts of the main breaker and the MOV, their sizes are reduced at the cost of adding an additional low loss branch. Active resonant HVDC circuit breakers [60][61] as a low-cost alternative, use resonant circuit instead of the huge number of semiconductor switches to achieve rapid fault isolation.

In a DC grid, there are terminals connected to multiple transmission lines. The conventional approach will have one HCB installed at each line end. Each HCB has a main breaker branch to interrupt the fault current. It is unlikely that multiple transmission lines meet fault at the same time. Therefore, if the main breaker branch is shared between the HCBs, the utilization of the device is increased and the cost is reduced. For the HCB, there are two types, the unidirectional HCB and the bidirectional HCB. Compared to the bidirectional HCB, only half number of IGBT modules are used in a unidirectional HCB.

The corresponding unidirectional and bidirectional interlink hybrid HVDC breakers (IHCB) are proposed based on the concept of sharing main breaker branch to reduce the cost of the HCB. As two HCBs share one main breaker branch, the operation between the main breaker branch and the two low-loss branches are designed to ensure correct protection against

faults on both the transmission line and the DC bus. The parameter of unidirectional and bidirectional IHCBs will be investigated and compared to the HCBs.

The IHCB studied in this paper is based on the HCB [49]. A detailed description of the HCB is introduced in Section 3.2. The topology of the unidirectional and bidirectional IHCBs and their parameter analysis are proposed in Section 3.3 and 3.4 individually. A test circuit is proposed to compare the fault blocking ability and fault current distribution of the IHCB and the HCB in Section 3.5. The summary is drawn in Section 3.6

3.2 Hybrid HVDC circuit breaker

An HCB is comprised of two branches, low-loss branch and main breaker branch. The low-loss branch contains an ultrafast disconnector (UFD) and a load commutation switch (LCS), see Fig. 3-1. The ultrafast disconnector [62] is a mechanical switch which can open within 2 ms to isolate the load commutation switch from the main circuit. The load commutation switch, that consists of a few IGBT modules [63], is designed to provide a low-loss current path for the load current. When a fault is detected, the load commutation switch is switched off and the fault current will be commutated into the main breakers. The commutation time is normally 0.25 ms [63].

The main breaker branch is sectionalized into several main break cells [64]. Each cell contains one MOV and one main breaker (MB), see Fig. 3-1. Each main breaker consists of a large number of IGBT modules. In IGBT modules, diodes are anti-series connected with IGBTs. The main breakers stay on-state during the normal condition. The load current only flows through the low loss branch due to the high state-on resistance of main breakers. The MOV is used to protect the main breaker from overvoltage and dissipate the fault energy.

The HCB can break either unidirectional or bidirectional fault current depending on the connection of IGBT modules applied in the load commutation switch and the main breaker. The connection of the IGBT modules for unidirectional blocking or bidirectional block is

shown in Fig. 3-2. The number of IGBT modules in a bidirectional HCB is twice of a unidirectional HCB.

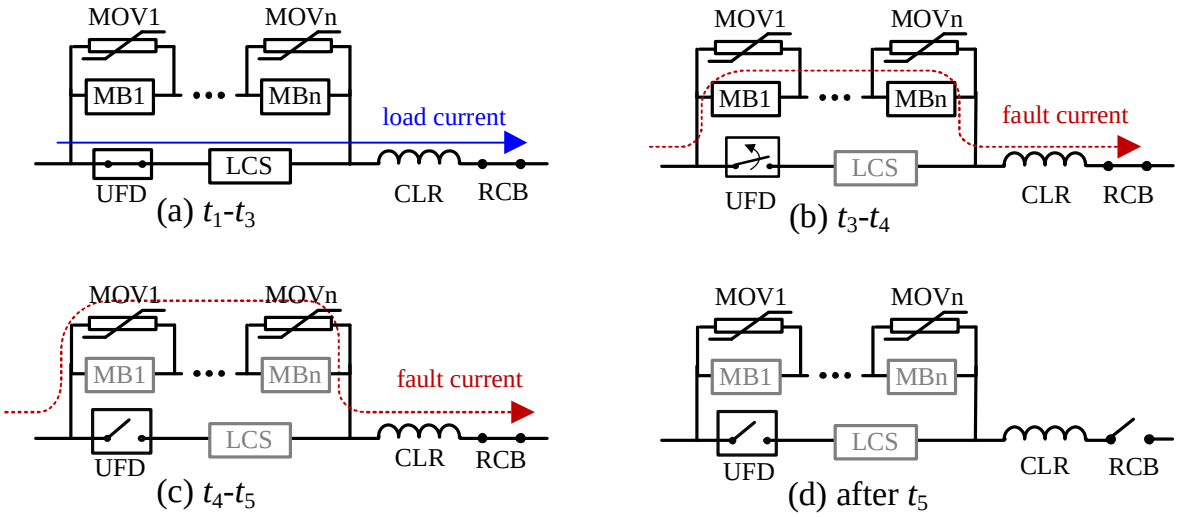


Fig. 3-1 Fault current breaking sequence of an HCB

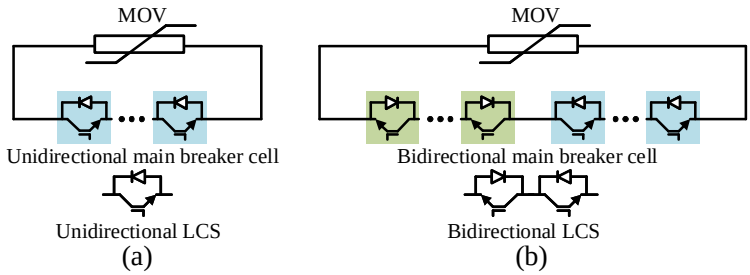


Fig. 3-2 IGBT arrangement for the unidirectional or bidirectional fault blocking

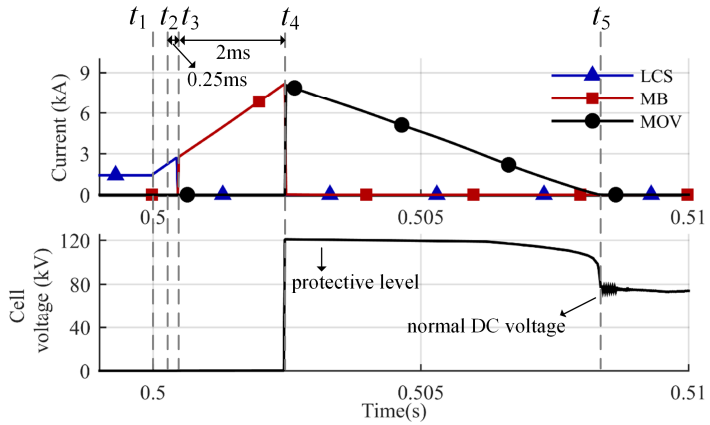


Fig. 3-3 Current interrupting sequence in the hybrid DC circuit breaker

A current limiting reactor (CLR) is used to limit the increasing speed of fault current no more than 3.5 kA/ms [48]. The residual current breaker (RCB) is used to disconnect the HCB physically, typically within 1 s when the residual current is small enough.

The operation sequence of the HCB is shown in Fig. 3-1. When a DC fault happens at t_1, the load current flowing through the low-loss branch will rise rapidly. The HCB will take some time to detect the fault (t_1-t_2). Then the load commutation switch is switched off immediately at t_2 and hence the fault current starts to be commutated to main breakers. When the fault current is fully commutated into main breakers at t_3 and the ultrafast disconnector starts to open, see Fig. 3-1(b). Once the ultrafast disconnector opens at t_4, main breakers are switched off to interrupt the fault current. The fault energy is dissipated by the MOVs and the fault current is therefore reduced to zero gradually, see Fig. 3-1 (c). When the DC current drops to zero at t_5, the fault is isolated by the HCB. If restore is not required, the residual current breaker (RCB) will open to disconnect the HCB physically, see Fig. 3-1 (d).

A simulation demonstration for the current interruption sequence in the HCB is shown in Fig. 3-3. For the load commutation switch and the main breaker, their peak fault currents appear at t_3 and t_4 respectively. For the MOV, the fault energy is dissipated lasting from t_4-t_5, and the fault current via the MOV is therefore reduced gradually. During the fault energy dissipation, the voltage of the main breaker cell is limited at the protective level of the MOV most of the time.

After the fault is isolated, the main breaker branch withstands the open-circuit DC grid voltage. The normal DC voltage of each cell is determined by the DC grid voltage dividing the number of cells. To achieve the short duration for fault current reduction, the protective level of the MOV is typically 1.5 times the normal DC voltage [64]. Therefore, the voltage rating of the main breaker in each cell is 1.5 times the normal DC voltage.

An equivalent one-line diagram of a three-terminal MMC-HVDC system, as shown in Fig. 3-4, is used to explain the design of breaker parameters. The design will consider the peak currents of the main breaker and load commutation switches, and the maximum dissipated fault

energy of the MOV under the most severe fault current. Thus a DC bus fault F_b and a transmission line fault F_l are used in the parameter design.

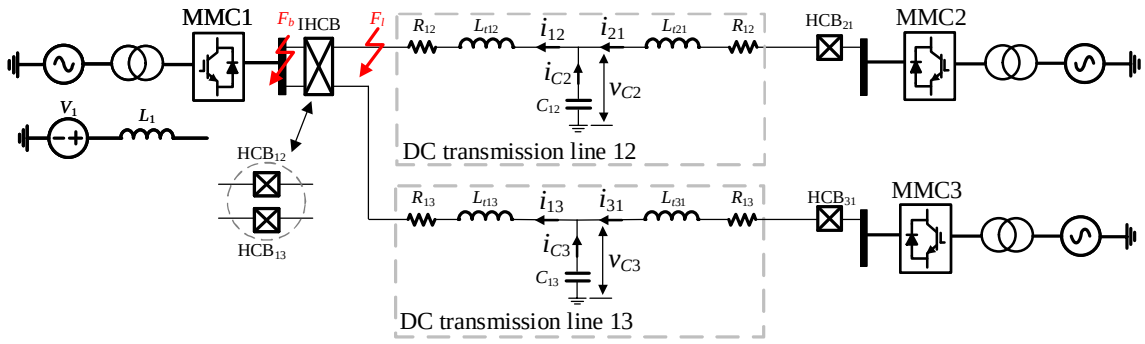


Fig. 3-4 Equivalent one-line diagram of a three-terminal MMC-HVDC for the breaker's parameter analysis

The MMC converter is considered as a constant voltage source with an inductor in series, see MMC1 in Fig. 3-4. The value of the series inductor is 1/3 of the arm inductor in the MMC. The transmission line is represented as a T-section RLC circuit. After a transmission line fault F_l occurs, the fault current flowing through the HCB is mainly contributed by MMC1, the fault current is expressed as:

$$i_{f12}(t) = I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t - t_1) \tag{3-1}$$

Where V_1 is the DC voltage of MMC1, I_{12} is the pre-faulted current of the transmission Line 12, L_{CLR12} is the inductance of current limiting reactor on Line 12, L_1 is the equivalent arm inductor of MMC1.

For the HCB, the peak currents of the load commutation switch and the main breaker appear at t_3 and t_4 respectively, see Fig. 3-3, are calculated as:

$$I_{LCS12} = I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_3 - t_1) \tag{3-2}$$

$$I_{MB12} = I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \tag{3-3}$$

Where I_{LCS12} and I_{MB12} are the peak currents of the load commutation switch and the main breaker.

For the dissipated energy calculation of the MOV, its voltage is assumed to be constant at the protection level during t_4-t_5, as shown in Fig. 3-3. The maximum dissipated energy of the MOV in each cell is calculated as:

$$E_{MOV12} = \left[I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \right] \times V_{cell} \times \frac{t_5 - t_4}{2} \tag{3-4}$$

Where V_{cell} is the voltage rating of the main breaker in each cell, also is the protect level of the MOV.

3.3 Unidirectional interlink hybrid HVDC circuit breaker

kkk DC line faults can be isolated by using only the unidirectional HCBs [55]. The design that each HCB has one main breaker branch (see Fig. 3-5(a)) can be improved by sharing a main breaker branch between two HCBs. Two unidirectional main breaker branches can be replaced by one interlink main breaker branch, which 50% MOVs is reduced, as shown in Fig. 3-5(b). The fault current of Line 12 or Line 13 can be commutated to this main breaker branch to interrupt, therefore bidirectional main breaker cells are required. The descriptions for the operation principle, the parameter design and the MOV reduction are given below.

Taking the fault F_l occurred on Line 12 as an example, the operation principle of the unidirectional IHCB is given in Fig. 3-6. Before the fault, the load currents flow through the low loss branches. A fault F_l occurs on Line 12 at t_1 and is detected at t_2, the fault current is then commutated from LCS12 to the main breakers, see Fig. 3-6 (a). At t_3, the current of low loss branch becomes zero, and UFD12 starts to open and completes action at t_4. Then MB1 will open to block the fault. From t_4-t_5, the fault energy is dissipated by the MOV1 and the fault current is reduced to 0 gradually, see Fig. 3-6(c). From t_3-t_5, the LCS13 provides the path for the fault current flowing into the main breaker branch. After the fault is isolated at t_5, if restore is not required, the RCB12 is open to disconnect the Line 12 physically and protect the MOV

from the overload. The UFD12 and LCS12 will then reclose to be a part of the interlink main breaker branch to protect Line 13 from the line fault, see Fig. 3-6(d).

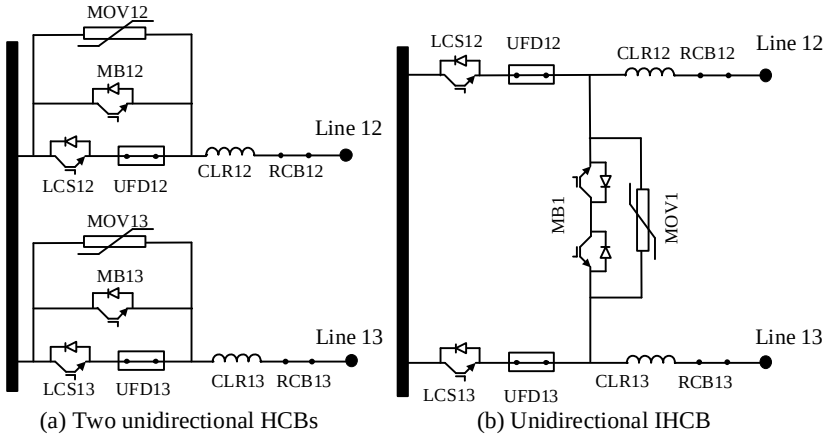


Fig. 3-5 Comparison between two unidirectional HCBs and the unidirectional IHCB

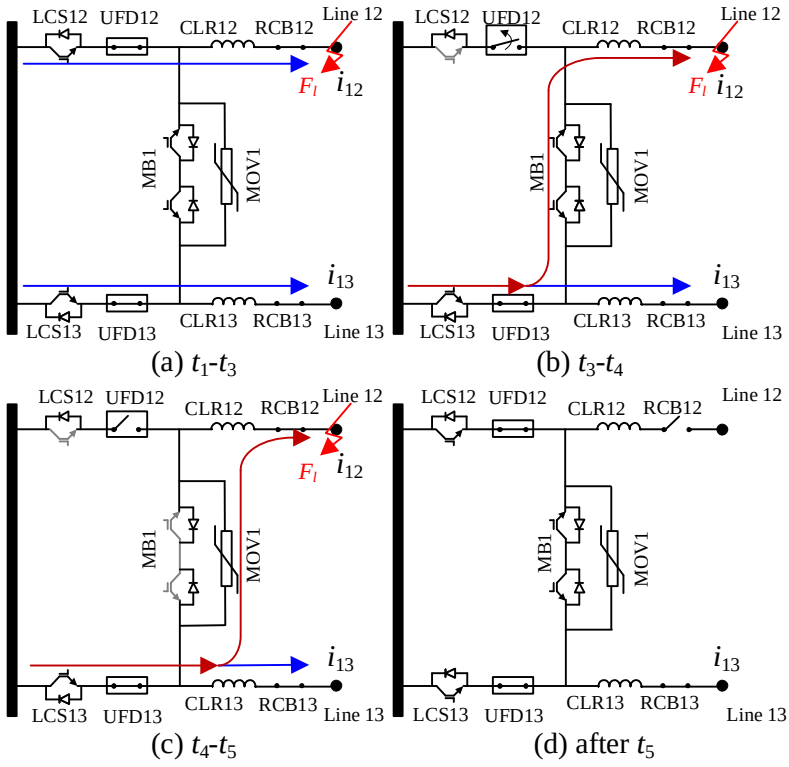


Fig. 3-6 Operation of the unidirectional IHCB for the transmission line fault

During the fault isolation t_3-t_5, see Fig. 3-6(b-c), LCS13 is the path for the fault current, which is commutated from the LCS12 to the main breakers, and the current i_{13} of Line 13. Its peak current I_{LCS13} appears at t_4, when the fault current is interrupted by the main breakers. The peak current of the load commutation switch is

$$I_{LCS13} = \left[I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \right] + i_{13}(t_4) \tag{3-5}$$

Where $i_{13}(t_4)$ is assumed to be equal to the load current I_{13} of Line 13. Because the influence of the fault on Line 13's current i_{1i} is ignored due to the quick fault current interrupting and the current limiting reactors on Line 13.

The fault current keep rising in the MB1 until the fault is blocked at t_4, the peak current of MB1 is:

$$I_{MB1} = I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \tag{3-6}$$

The MOVs in main breaker cells dissipated the fault energy evenly, and for one MOV in each cell, its maximum dissipated energy is expressed as:

$$E_{MOV} = \left[I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \right] \times V_{cell} \times \frac{t_5 - t_4}{2} \tag{3-7}$$

After the fault is isolated, the main breaker branch of the IHCB withstands the open-circuit DC voltage (V_1) of MMC1. The voltage rating of the main breaker branch denoted as V_{MB}, is $1.5V_1$. This interlink main breaker branch is composed of anti-series connected IGBT to achieve bidirectional blocking, the required numbers of IGBT modules and MOVs are:

$$\begin{cases} n_{IGBT} = \dfrac{V_{MB}}{V_{IGBT}} \times 2 \\ n_{MOV} = \dfrac{V_{MB}}{V_{cell}} \end{cases} \tag{3-8}$$

Where V_{IGBT} are the voltage ratings of one IGBT module.

If two unidirectional HCBs are used, the voltage rating of the main breaker branch is same as that of the unidirectional IHCB, which is also $1.5V_1$. The numbers of IGBT modules and MOVs applied in two HCBs' main breaker branches are:

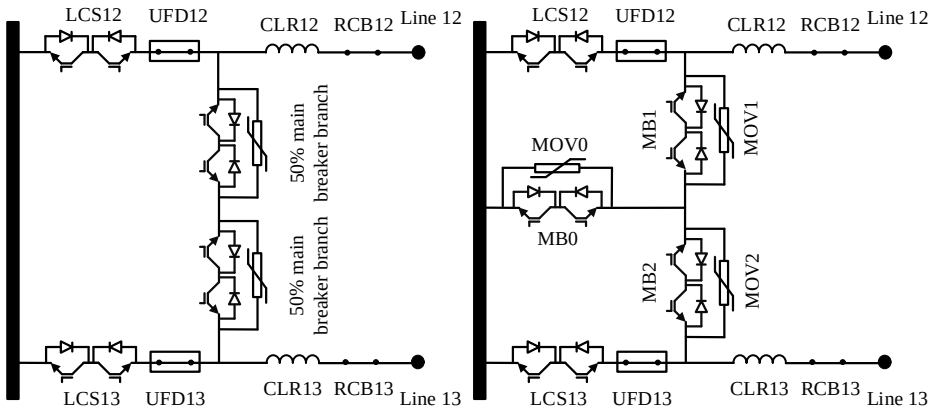
$$\begin{cases} n_{IGBT} = \dfrac{V_{MB}}{V_{IGBT}} \times 2 \\ n_{MOV} = \dfrac{V_{MB}}{V_{cell}} \times 2 \end{cases} \tag{3-9}$$

Compared Eq. 3-8 and Eq. 3-9, the number of IGBT modules are the same in the unidirectional IHCB and two unidirectional HCBs. However, only 50% MOVs are needed in the unidirectional IHCB.

3.4 **Bidirectional interlink hybrid HVDC circuit breaker**

The bidirectional HCB can be used to protect the system from not only line faults but also DC bus faults. When a DC bus fault occurs, the fault current of each line will be commuted from LCS to the main breaker branch before interrupted.

If a bidirectional IHCB would use the same main breaker branch as that of a unidirectional IHCB, see Fig. 3-7 (a), the fault current cannot be fully blocked when a DC bus fault occurs, because both LCS12 and LCS13 cannot open at the same time. Otherwise, the LCSs would be destroyed due to their low voltage rating. Therefore, a novel Y-connected interlink main breaker branch is proposed for the bidirectional IHCB in order to provide a path for the fault current after both LCSs open, and withstand the high open-circuit DC grid voltage. An additional main breaker branch, (MB0 and MOV0), is added between the DC bus and the midpoint of interlink main breaker branch, see Fig. 3-7(b).



(a) Interlink main breaker branch (b) Y-connected interlink main breaker branch

Fig. 3-7 Bidirectional IHCB

Compared to using bidirectional HCBs, the number of IGBTs and MOVs are reduced by 25% by using the Y-connected branch. For either a line fault or a bus fault, the fault current will be commutated to the Y-connected interlink main breaker branch to interrupt. The descriptions of the operation principle, the parameter design and reduction of the numbers of IGBT modules and MOVs are given below.

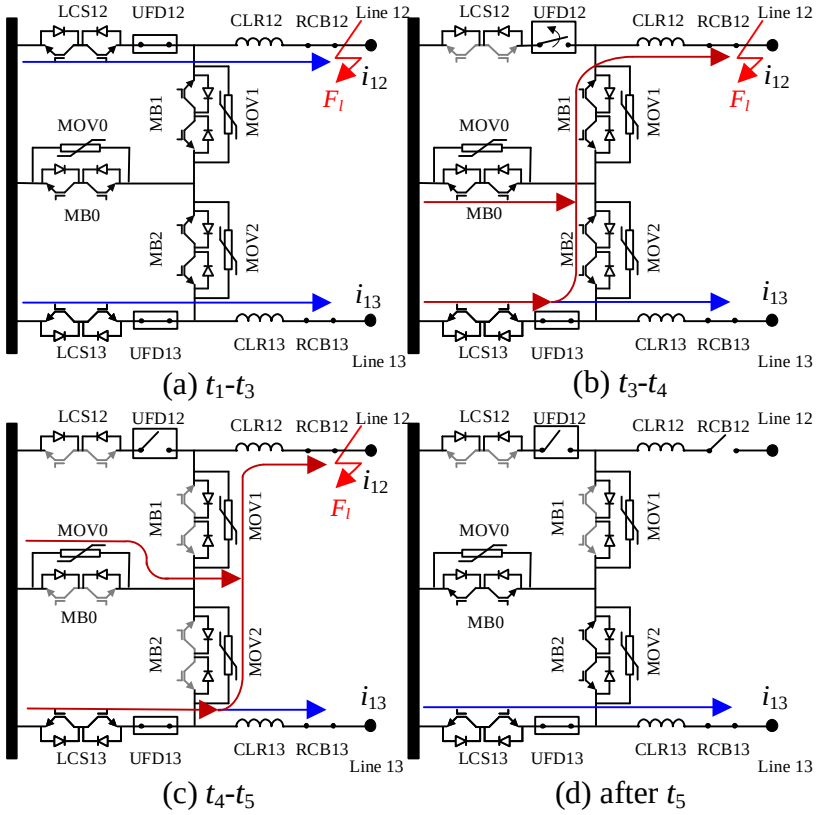


Fig. 3-8 Operation of the bidirectional IHCB for the transmission line fault

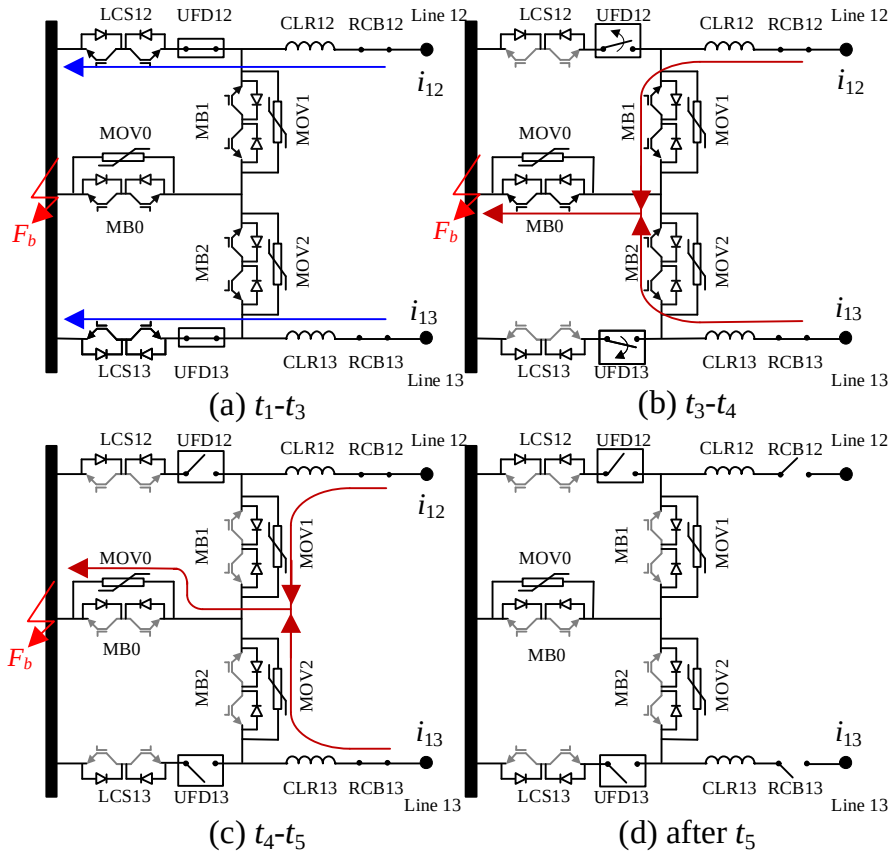


Fig. 3-9 Operation of the bidirectional IHCB for the DC bus fault

To isolate the fault at a transmission line, the operation of an IHCB is shown in Fig. 3-8. Before the fault, the load currents flow through the low loss branches. A fault occurs on Line 12 at t_1, see Fig. 3-8 (a). When it is detected at t_2, LCS12 is switched off and the fault current starts to be commutated into Y-connected main breakers. When the commutation process is finished at t_3, UFD12 starts to open, see Fig. 3-8 (b). At t_4, UFD12 is fully opened, the fault current will be interrupted by the Y-connected main breakers and the fault energy is dissipated over the MOV0, MOV1 and MOV2, see Fig. 3-8 (c). After the fault is isolated at t_5, the RCB12 is open to disconnect the Line 12 and protect the MOVs from overload. The main breaker branches 0&2 are still available to protect Line 13, see Fig. 3-8 (d).

To isolate the fault occurred at the DC bus F_b, the operation of the bidirectional IHCB is shown in Fig. 3-9. To test the breaker with the most severe fault, the load current is set to have the same direction as the fault current. Before the fault, the load current flows through the low

loss branch to the DC bus. The DC bus fault occurs at t_1, see Fig. 3-9 (a). When it is detected at t_2, both LCS12 and LCS13 are switched off and the fault currents of both Line 12 and Line 13 start to be commutated to the Y-connected main breakers. From t_3, when the commutation process is finished, UFD12 and UFD13 start to open and complete the action at t_4, see Fig. 3-9 (b). From t_4, the fault current is interrupted by MBs0, 1 and 2, and the fault energy will be dissipated by MOVs0, 1 and 2, see Fig. 3-9 (c). After the fault is isolated at t_5, both RCB12 and RCB13 open to disconnect the faulty DC bus physically, see Fig. 3-9 (d).

The line fault is normally selected to design the parameter for the bidirectional IHCB and the reason has been described in section 3.2.

During the fault isolation t_3-t_5, see Fig. 3-8(b-c), LCS13 is an alternative path for the fault current. the half fault current and the current i_{13} of Line 13 will pass through LCS13. Its peak current I_{LCS13} appears at t_4, when the fault current is interrupted by the main breakers. The peak current of the load commutation switch is shown below:

$$I_{LCS13} = i_{13}(t_4) + 0.5 \times \left[I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \right] \tag{3-10}$$

Where the influence of the fault on Line 12's current is ignored due to the quick fault current interrupting and the current limiting reactors on Line 13. $i_{13}(t_4)$ is equal to the load current of Line 13.

The main breaker 1 withstands the whole fault current, see Fig. 3-8(b). Its peak current appears at t_4, when the fault current is interrupted. The peak current of the main breaker 1 or 2 is shown below:

$$I_{MB1} = I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \tag{3-11}$$

The maximum dissipated energy of the MOV 1 or 2 located on main are calculated as:

$$E_{MOV1} = \left[I_{12} + \frac{V_1}{L_1 + L_{CLR12}} \times (t_4 - t_1) \right] \times V_{cell} \times \frac{t_5 - t_4}{2} \tag{3-12}$$

The parameter of the main breaker branch 0 is designed according to the DC bus fault, because it will withstand the high fault current from both Line 12 and Line 13 under the DC bus fault, see Fig. 3-9(b-c).

As shown in Fig. 3-4, after the DC bus fault F_b occurs, the following equations of Line 12 or Line 13 are obtained using the KVL and KCL laws:

$$R_{1j} i_{j1}(t) + (L_{CLRj1} + L_{tj1} + L_j) \frac{di_{j1}(t)}{dt} + v_{Cj}(t) = V_j \tag{3-13}$$

$$(L_{CLR1j} + L_{t1j}) \frac{di_{1j}(t)}{dt} + R_{1j} i_{1j}(t) = v_{Cj}(t) \tag{3-14}$$

$$C_j \frac{dv_{cj}(t)}{dt} = -i_{Cj}(t) \tag{3-15}$$

$$i_{1j}(t) = i_{j1}(t) + i_{Cj}(t) \tag{3-16}$$

Where j=2 or 3, V_j is the DC voltage of MMCj.

To simplify the fault current analysis, the total inductances on both sides of the capacitor C_{1j} are supposed to be equal. The values of L_{t1j} and L_{tj1} of the transmission lines should satisfy the relationship:

$$L_{CLR1j} + L_{t1j} = L_{CLRj1} + L_{tj1} = L_{1j} \tag{3-17}$$

Where L_{1j} denotes the equivalent inductance between the faulted DC bus and the capacitor C_{1j} and between the capacitor C_{1j} and MMCj.

The expression of v_c is obtained by substituting Eq. 3-14 to Eq. 3-17 into Eq. 3-13:

$$2v_{Cj}(t) + R_{1j} C_j \frac{dv_{Cj}(t)}{dt} + L_{1j} C_j \frac{d^2 v_{Cj}(t)}{dt^2} = V_j \tag{3-18}$$

Applying Laplace transformation to Eq. 3-18 yields

$$2v_{Cj}(s)+R_{1j}C_j\left[sv_c(s)-v_c(0)\right]+L_{1j}C_j\left[s^2v_c(s)-sv_c(0)\right]=\frac{V_j}{s} \tag{3-19}$$

Where $v_c(0)=V_j$ is assumed due to the small value of R_{1j}.

The expression of $v_c(s)$ is obtained by arranging Eq. 3-19.

$$v_{Cj}(s)=0.5V_j\left[\frac{1}{s}+\frac{C_j(L_{1j}s+R_{1j})}{C_jL_{1j}s^2+C_jR_{1j}s+2}\right] \tag{3-20}$$

Applying Laplace transformation to Eq. 3-14 and considering Eq. 3-20 yield:

$$L_{1j}\left[si_{1j}(s)-i_{1j}(0)\right]+R_{1j}i_{1j}(s)=0.5V_j\left[\frac{1}{s}+\frac{C_j(L_{1j}s+R_{1j})}{C_jL_{1j}s^2+C_jR_{1j}s+2}\right] \tag{3-21}$$

The expression of $i_{1j}(s)$ is thus obtained from Eq. 3-21,

$$i_{1j}(s)=0.5V_j\left[\frac{1}{R_{1j}}(\frac{1}{s}-\frac{1}{s+a})+\frac{1}{L_{1j}b}\times\frac{b^2}{(s+\frac{a}{2})^2+b^2}\right]+i_{1j}(0)\times\frac{1}{s+a} \tag{3-22}$$

Where $a=\frac{R_{1j}}{L_{1j}}$, $b=\sqrt{\frac{2}{L_{1j}C_j}-(\frac{R_{1j}}{2L_{1j}})^2}$ and $i_{1j}(0)=I_{1j}$ which is the rated current in normal condition.

The time-domain expression of i_{1j} is obtained through inverse Laplace transform of Eq. 3-22:

$$i_{1j}(t)=0.5V_j\left[\frac{1}{R_{1j}}(1-e^{-at})+\frac{1}{L_{1j}b}e^{-\frac{a}{2}t}\sin(bt)\right]+I_{1j}e^{-at} \tag{3-23}$$

As shown in 3-23, the fault current is determined by the rated current of both lines, the impedance of the transmission lines, the inductance of the CLRs and the arm inductor of converters. The fault current in the Y-connected main breakers keeps rising until the fault current is interrupted. The peak current in the main breaker 0 appears at t_4:

$$I_{MB0}=\sum_{i=2}^{3}i_{1j}(t_4) \tag{3-24}$$

The maximum dissipated energy of the MOV 0 of each cell in this sub-branch is:

$$E_{MOV0} = I_{MB0} \times V_{cell} \times \frac{t_5 - t_4}{2} \tag{3-25}$$

When a line fault is isolated by the breaker, the open-circuit voltage is the DC voltage (V_1) of MMC1. When a bus fault is cleared by the breaker, the open-circuit voltage of is $V_j - \Delta V_{1j}$, V_j is the DC voltage of MMCj, and ΔV_{1j} is the voltage drop of Line 1j. Only the rated DC voltage V_1 is considered to determine the voltage rating of the breaker as $V_1 > V_j - \Delta V_{1j}$.

For the bidirectional IHCB, two branches of the Y-connected main breaker branch share the open-circuit voltage V_1. The voltage rating of each main breaker branch is $V_{Y\text{-}MB}$= V_{MB}/2=1.5V_1/2=0.75V_1. The numbers of IGBT modules and MOVs required for an interlink main breaker branch are:

$$\begin{cases} n_{IGBT} = \dfrac{0.5V_{MB}}{V_{IGBT}} \times 3 \times 2 \\ n_{MOV} = \dfrac{0.5V_{MB}}{V_{cell}} \times 3 \end{cases} \tag{3-26}$$

If two bidirectional HCBs are used, the open-circuit voltage for each main breaker branch is V_1. The voltage rating V_{MB} of each branch is 1.5V_1. The numbers of IGBT modules and MOVs used in two main breaker branches are:

$$\begin{cases} n_{IGBT} = \dfrac{V_{MB}}{V_{IGBT}} \times 4 \\ n_{MOV} = \dfrac{V_{MB}}{V_{cell}} \times 2 \end{cases} \tag{3-27}$$

Comparing Eq. 3-26 to Eq. 3-27, numbers of IGBT modules and MOVs are reduced by 25% by using the bidirectional IHCB.

3.5 Simulation Verification

The fault isolation capability of the IHCB and the HCB proposed in [49] are compared in a three-terminal MMC-HVDC system. The positions of the line fault and the DC bus fault is

shown in Fig. 3-4. The DC transmission lines are represented as pi-sections in series. For the purpose of only testing the circuit breaker devices, the breakers are set to start to open at a fixed current, i.e. 2kA in this study. The commutation time from the load commutation switch to the main breakers is 0.25 ms. The UFD is simulated as a resistor switch with 2 ms opening delay. The main data of test system is summarized in Appendix Table A-1.

The load commutation switch consists of 3×3 IGBT modules [63]. Its current and voltage ratings are fulfilled by 2×2 IGBT modules. The rest of the IGBT modules are used as redundancy. The structure of the LCS is shown in Table 3-3. The voltage rating of each main breaker cell is 120 kV. The numbers of IGBT modules used in the main breakers of the IHCB and HCB are summarized in Table 3-1. The data of 4.5-kV StakPak IGBT module [65] are used in the simulation.

Table 3-1 Main data of test system

Items	Two unidirectional HCBs	Unidirectional IHCB	Two Bidirectional HCBs	Bidirectional IHCB
Main breaker branch	2 (480 kV each)	1 (480 kV each)	2 (480 kV each)	3 (240 kV each)
Main breaker cell	8	4	8	6
MOV	8	4	8	6
IGBT modules	216	216	432	324
LCS	9	15	9	9

3.5.1 Unidirectional interlink hybrid HVDC breaker

During normal operation, MMC2 and MMC3 receive 900 MW respectively from MMC1. The currents in transmission Line 12 and Line 13 are both 1.42 kA.

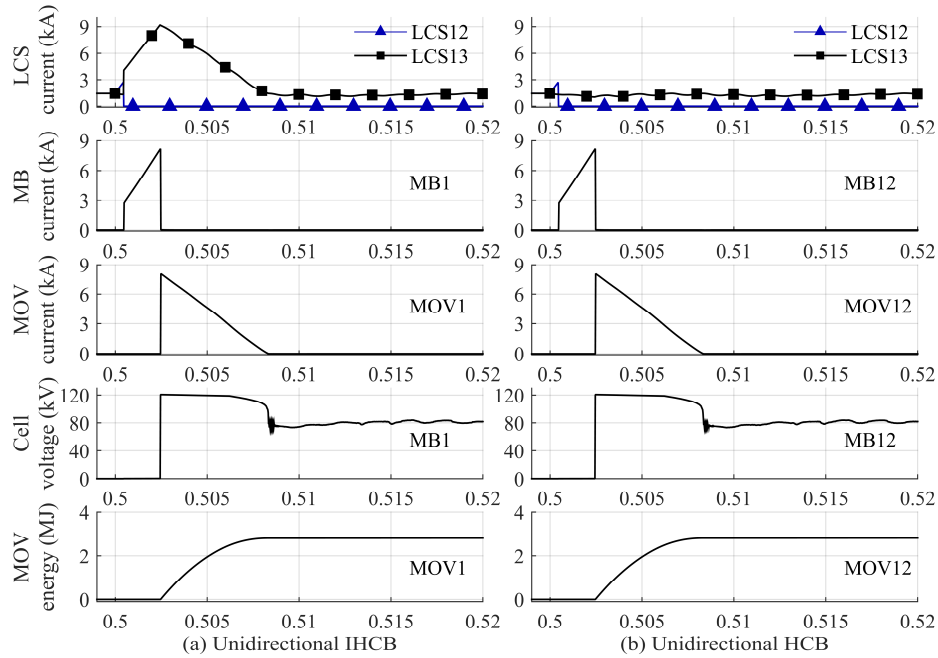
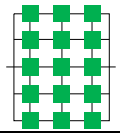


Fig. 3-10 Breaker performance under a line fault

Table 3-2 Parameters of the unidirectional breaker

Items	Unidirectional HCB simulation/calculation	Unidirectional IHCB simulation/calculation
LCS (kA)	2.72/2.74	9.20/9.66
MB (kA)	8.19/8.24	8.19/8.24
MOV (MJ)	2.82/2.90	2.82/2.90
Structure of LCS		

Where each green square is one IGBT modules.

A line fault F_l, that occurs at 0.5s on Line 12, is applied to test the fault isolation performance of the unidirectional IHCB, shown in Fig. 3-6. During the fault isolation, the performance of the unidirectional IHCB is shown in Fig. 3-10 (a). The peak currents of the load commutation switch (see LCS13) and the main breaker are 9.16 kA and 8.19 kA, both appearing at 5.025s. After the fault current is interrupted by the main breakers at 5.025s, the fault energy is dissipated by the MOV and the fault current drops to 0 kA at 0.5083s. During this period, the voltage of each cell is limited at 120 kV and then drops to the normal DC voltage 80 kV. The total dissipated energy of the MOV in one cell is 2.82 MJ.

For comparison, the performance of the unidirectional HCB12 for the same fault isolation is shown in Fig. 3-10(b). The fault current of Line 12 will not flow through LCS13 located on Line 13, therefore the peak current of the load commutation switch is 2.72kA appearing at 5.025s. The performance of other components in unidirectional HCB is exactly the same as that in the IHCB.

For both the unidirectional HCB and IHCB, the peak current of the load commutation switch and the main breaker, and the maximum dissipated energy of the MOV in one cell are summarized in Table 3-2 according to the simulation and the calculation of parameter design. The calculated parameters are close to the simulated parameters.

The current rating of the normal load commutation switch is 8kA which cannot be used in the unidirectional IHCB for 9.16 kA peak current. 4×4 IGBT modules are used for double current ratings of the load commutation switch in the unidirectional IHCB. 4×2 IGBT modules ensure the 16 kA maximum load current and sufficient voltage stress. The rest of the IGBT modules are used as the redundancy. Its structure is drawn in Table 3-2.

3.5.2 Bidirectional interlink hybrid HVDC breaker

Both the line fault F_l and the DC bus fault F_b that occur at 0.5 s respectively are used to test the fault isolation performance of the bidirectional IHCB. According to the analysis in the parameter design of the bidirectional IHCB, the line fault F_l is selected to test the parameters of the load commutation switch and the main breaker branch, LCS1 and MB1 in this case. The DC bus fault F_b is for testing the main breaker branch 0.

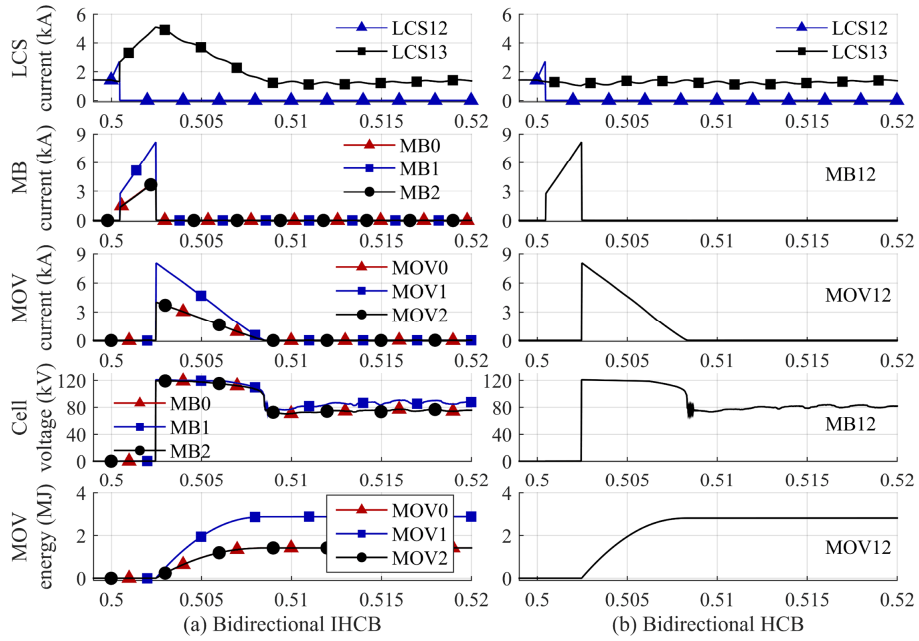


Fig. 3-11 Breaker performance under a line fault

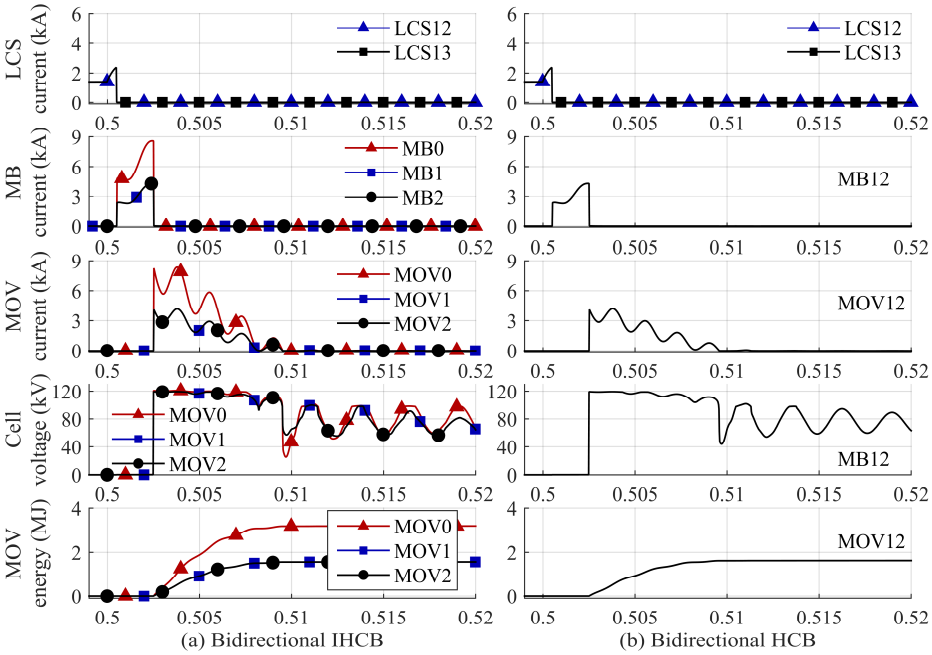


Fig. 3-12 Breaker performance under a DC bus fault

Table 3-3 Parameters of the bidirectional breaker

Items	bidirectional HCB simulation/calculation	bidirectional IHCB simulation/calculation	
LCS (kA)	2.72/2.74	5.10/5.54	
MB (kA)	8.19/8.24	MB1-2	8.19/8.24
		MB0	8.7/9.14
MOV (MJ)	2.82/2.90	MOV1-2	2.82/2.90
		MOV0	3.22/3.77

During normal operation, MMC2 and MMC3 receive 900 MW each from MMC1. The currents in transmission Line 12 and Line 13 are both 1.42 kA.

A line fault F_l, that occurs at 0.5s on Line 12, is applied to test the fault isolation performance of the unidirectional IHCB, shown in Fig. 3-8. During the line fault isolation, the performance of the bidirectional IHCB is shown in Fig. 3-11(a). The peak currents of the load commutation switch, LCS13 and the main breaker, MB1, are 5.10 kA and 8.19 kA, both appearing at 5.025s. The total dissipated energy of the MOV1 in one cell is 2.82 MJ.

The performance of the bidirectional HCB for the same line fault isolation is shown in Fig. 3-11(b). The peak current of the load commutation switch is 2.72kA appearing at 5.025s. The performance of the main breaker branch in bidirectional HCB is exactly the same as the main breaker branch 1 of the IHCB.

During normal operation, MMC2 and MMC3 send 900 MW each to MMC1. The power transportation is reversed to keep the same direction between the load current and the fault current. The currents of Line12 and Line13 are both 1.42 kA.

During the fault isolation, the performance of the bidirectional IHCB is shown in Fig. 3-12(a). The peak current of the main breaker 0 is 8.57 kA occurs at the 0.5025, when the Y-connected main breakers interrupt the fault current. The maximum dissipated energy of the MOV0 in one cell is 3.22 MJ. During the DC bus fault isolation and the post-fault condition, the oscillations of the fault current and the cell voltage occurred because of the large equivalent capacitance of the transmission line.

The performance of the bidirectional HCB located on Line 12 for the same DC bus fault is shown in Fig. 3-12(b).

As shown in Fig. 3-11 and Fig. 3-12, the fault currents through each line caused by the DC bus fault is smaller than that from line faults due to the current limiting reactors located on both line ends and the equivalent inductance of the transmission line. The peak current and

maximum dissipated energy of the load commutation switches and the main breaker branches 1&2 in the bidirectional IHCB are lower than that in the case of the line fault. Thus, ratings of those components are determined by line fault isolation requirement. And the ratings of main breaker branch in the bidirectional IHCB is determined by the DC bus fault isolation requirement, because the fault currents of both lines will flow through this branch.

For both the bidirectional HCB and IHCB, the peak current of the load commutation switch and the main breaker, and the maximum dissipated energy of the MOV of each cell are summarized in Table 3-3 in the case of the transmission line fault and the DC bus fault. The calculated parameters from the derived equations for parameter design are close to the simulated parameters. The peak current of the LCS of the bidirectional IHCB is higher than that of the bidirectional HCB. The normal load commutation switch with 8 kA current rating can still be used for the IHCB, because the peak current of its LCS is 5.10 kA. In terms of the peak current and maximum dissipated energy, the main breaker branches 1&2 of the bidirectional IHCB have the same parameter as those in the bidirectional HCB. The parameters of the main breaker branch 0 are slightly higher than that in the bidirectional HCB.

3.6 **Summary**

Novel interlink hybrid DC circuit breakers (IHCB) for unidirectional and bidirectional interruption are proposed with an aim of reduced sizes and costs of the DC circuit breakers.

For a unidirectional IHCB, an interlink main breaker branch is shared by two low loss branches to achieve the same function as that of two unidirectional hybrid DC circuit breakers (HCBs). For a bidirectional IHCB, a novel Y-connected main breaker branch is proposed for the both line and DC bus fault current interruption.

The current ratings, energy dissipation capability, and required numbers of IGBTs and MOVs of the IHCBs have been determined by considering the peak fault currents and the maximum energies dissipation. Mathematic analyses have been achieved to support the design.

Comparing to HCBs, the number of MOVs of the main breaker branch of the unidirectional IHCB is reduced by 50% and the numbers of IGBT modules and MOVs of the bidirectional IHCB are reduced by 25%.

The fault current interruption performance of the main breaker branches of both bidirectional and bidirectional IHCBs are compared to the HCBs through simulations. The proposed IHCBs can break the fault currents at the same speed. The IHCB design is able to meet all the requirements for peak fault currents and maximum dissipated energies.

CHAPTER 4 COORDINATION OF MMC CONVERTERS AND HYBRID DC CIRCUIT BREAKERS FOR HVDC GRID PROTECTION

DC circuit breakers (DC-CBs) constitute a potential solution for the protection of HVDC grids in the event of a DC fault. Although no commercial high voltage DC-CB is yet available, prototypes have been developed to clear a DC fault within 2.5 ms. However, such devices are required to withstand a very high fault current and to absorb a large fault energy. To bring down the current rating, the fault current may be limited by increasing the speed of operation of the DC-CB at the expense of increasing the cost of the device. Instead, this paper proposes a more feasible alternative by coordinating the operation of both DC-CBs and modular multi-level converters (MMCs) in an HVDC grid. In the presented scheme the MMC submodules are bypassed to suppress the DC fault current. The effectiveness of the proposed method has been assessed using mathematical models. An algorithm for fault detection and discrimination which considers an adequate coordination of the DC-CBs and MMCs has been developed. The proposed method has been demonstrated using a three-terminal HVDC system. Simulation results show that the DC fault current can be significantly reduced.

4.1 **Motivation**

The decarbonisation of Europe's energy sector is a key driver for the development of integrated HVDC grids (such as the European Super Grid [66]). A multi-terminal HVDC (MTDC) grid will enable a more reliable power transfer from offshore wind farms and will facilitate the cross-border exchange of energy between different countries. Several voltage source converter (VSC) based MTDC projects have been planned or being constructed in Europe, including the Sweden-Lithuania and the South-West Scheme [67][68] linking Sweden to Norway. In China, the Nan'ao three-terminal HVDC system and the Zhoushan five-terminal DC grid have been commissioned and are already in operation [69]. However, the widespread

deployment of DC grids is prevented by technical challenges, such as the protection of DC grids during faults.

A DC grid has, in general, a low inductance. Under the presence of a fault, it will exhibit a higher fault current rise time and a faster fault propagation time when compared to an AC system subjected to an AC fault –where the propagation of fault current is limited by the relatively large system inductance. In a DC grid, the system inductance affects the rising rate of DC fault current only, but not its magnitude. Therefore, the anticipated speed of operation of a DC grid protection system to isolate a DC fault should be much faster than that of its AC counterpart. Most of the MTDC grid protection algorithms based on DC circuit breakers (DC-CBs) found in the literature aim to reduce the time required to detect, discriminate and interrupt a DC fault [70][71][72][73]. However, these schemes do not minimise the requirements on fault current interruption or energy dissipation of DC-CBs.

The operating speed of a DC-CB constitutes the main obstacle preventing a reduction in the time for fault isolation. The fastest operating speed for manufactured DC-CBs found in the open literature is 2.5 ms [74]. However, this assumes a negligible time delay for fault detection and discrimination. DC fault current may rise to a very high value; therefore, DC-CBs have to be rated accordingly. Alternatively, large inductors could be used together with the DC-CBs to limit the rise of fault current [75]. A DC-CB capable of withstanding high fault currents or the inclusion of large inductors would increase the cost of the protection scheme.

In order to bring down the rating (and hence cost) of a DC-CB, the fault current has to be reduced before the device operates. Considering that it could be difficult to physically increase the operating speed, a more economical alternative would be to coordinate the operation of both the DC-CBs and the modular multi-level converters (MMCs) available in an MTDC grid. In line with this, a method is proposed for HVDC grid protection where the submodules (SM) within the MMCs are bypassed to reduce the fault current contribution of the SM capacitors.

This way the DC-CBs are able to interrupt the fault current at a much smaller magnitude, followed by an immediate recovery of the MMCs after fault isolation. The proposed method is tested on a three-terminal VSC HVDC system modelled in the PSCAD/EMTDC simulation tool.

4.2 Protection of HVDC Grids

4.2.1 Point-to-Point Links

Fig. 4-1 shows a typical protection circuit for a point-to-point (P2P) HVDC link using MMCs, AC circuit breakers (AC-CBs) and DC disconnectors [76].

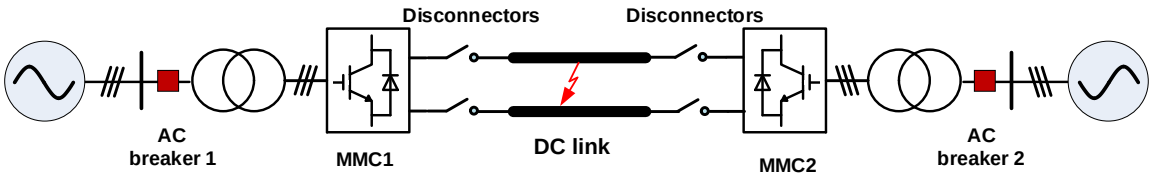


Fig. 4-1Protection of a P2P-HVDC link.

Following a DC fault, DC voltage will rapidly decrease, resulting in a fast increase of DC current. Current (and voltage) sensors located at each MMC station are employed to detect the first wave-front of fault current (and voltage). An overcurrent and undervoltage criterion is used to block the IBGTs within the MMCs. As a result, the fault current will flow from the AC sources to the fault location via the diodes of the IGBTs. Fault clearance is achieved by the AC-CBs, which open their own mechanical breakers at the zero-crossing of AC currents to quench the arc between two contacts. The DC disconnectors will ultimately open once the fault current is drawn to zero so that the faulted line or cable is isolated.

The protection strategy described above relies on mature technologies and therefore has a low investment cost. However, the slow operation of AC-CBs and the inevitable shutdown of the entire system makes it unsuitable to protect HVDC grids.

4.2.2 HVDC Grids

More HVDC grids are likely to be built through the integration of existing P2P-HVDC links in the future. Fig. 4-2 shows a simple MTDC grid consisting of three terminals and a meshed configuration to provide redundancy for system operation. DC power can flow through alternative paths in the event of failure or maintenance of a DC link.

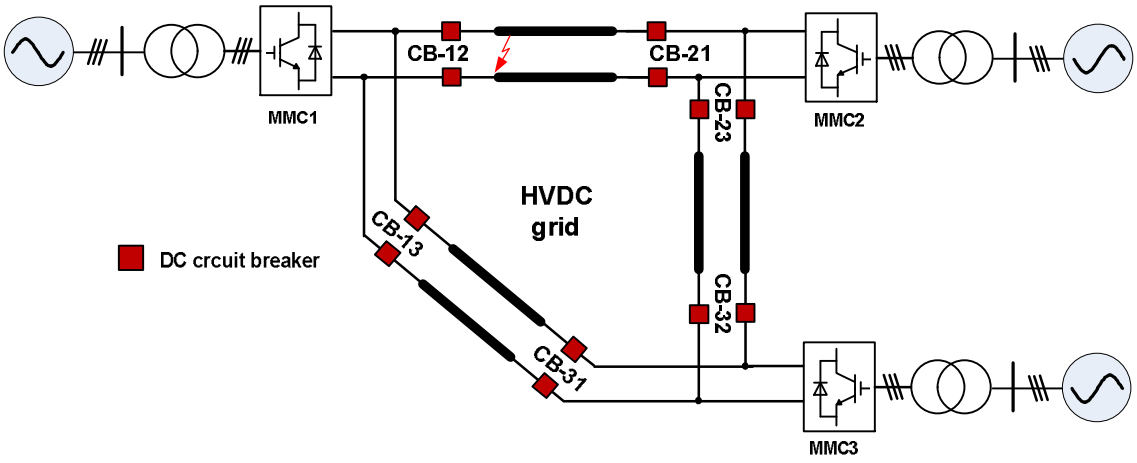


Fig. 4-2 Protection of an HVDC grid.

As in a P2P-HVDC link, DC faults will rapidly propagate across an entire HVDC grid, resulting in a DC voltage drop and a DC current increase. An effective protection system should be able to discriminate and isolate the fault and then disconnect the faulted section from the rest of the health system so that power can still be transmitted [71]. Therefore, the inclusion of DC-CBs at both ends of the DC links is necessary to achieve fast fault discrimination and isolation (see Fig. 4-2). In the event of a fault, the DC-CBs at the faulted link can detect and isolate the fault using local measurements of current and voltage.

Notice that the main protection system of an HVDC grid should avoid the use of communication as this may cause large time delays and would require an adequate synchronisation of DC-CBs. Moreover, a fault will not only affect a specific DC line but also other sections of the grid. Therefore, the protection system must be designed to discriminate the healthy circuits from the faulted section. This can be done by comparing the currents and voltages measured at the faulted lines with those of the healthy circuits. The DC-CBs located at non-faulted lines should be kept closed throughout the fault.

The conventional method described above heavily relies on DC-CBs. To be able to withstand very high fault currents, these should be highly rated or should incorporate large inductances –leading to high costs. These shortcomings may be avoided through the method proposed next section.

4.3 Principles of MMCs bypassing

When a DC line-to-line fault occurs, DC current increases sharply. The faulted point is mainly fed by the discharge of SM capacitors through S1 (see Fig. 4-3). The three-phase fault current through S2 and D2 only exists among arms. It is eliminated naturally at the converter terminal due to its three-phase symmetrical characteristic. If block the MMC (S1 and S2 are off), the freewheeling diodes D2 act as an uncontrolled rectifier and produce a high DC current through converter terminal. Therefore, DC breakers have to break the high DC current in both conditions.

Bypassing MMC will avoid the discharge of SM capacitors by turning S1 off, and keep S2 on to eliminate the AC current at converter terminal. After bypassing the MMC, DC current will stop increasing and freely decay to zero. An example seen in Fig. 4-4 is made to compare the DC fault currents. It is apparent that bypassed MMC feed the lowest current to DC system. This current is almost equal to the current when MMC is just bypassed. Therefore, the high-current interruption demand of DC breakers is reduced significantly. To achieve the benefits of bypassing, these situations below should be avoided during bypassing:

- Overcurrent of IGBTs(S2)
- Overcurrent of the AC transformer
- Activation of AC protection to cut the MMC off

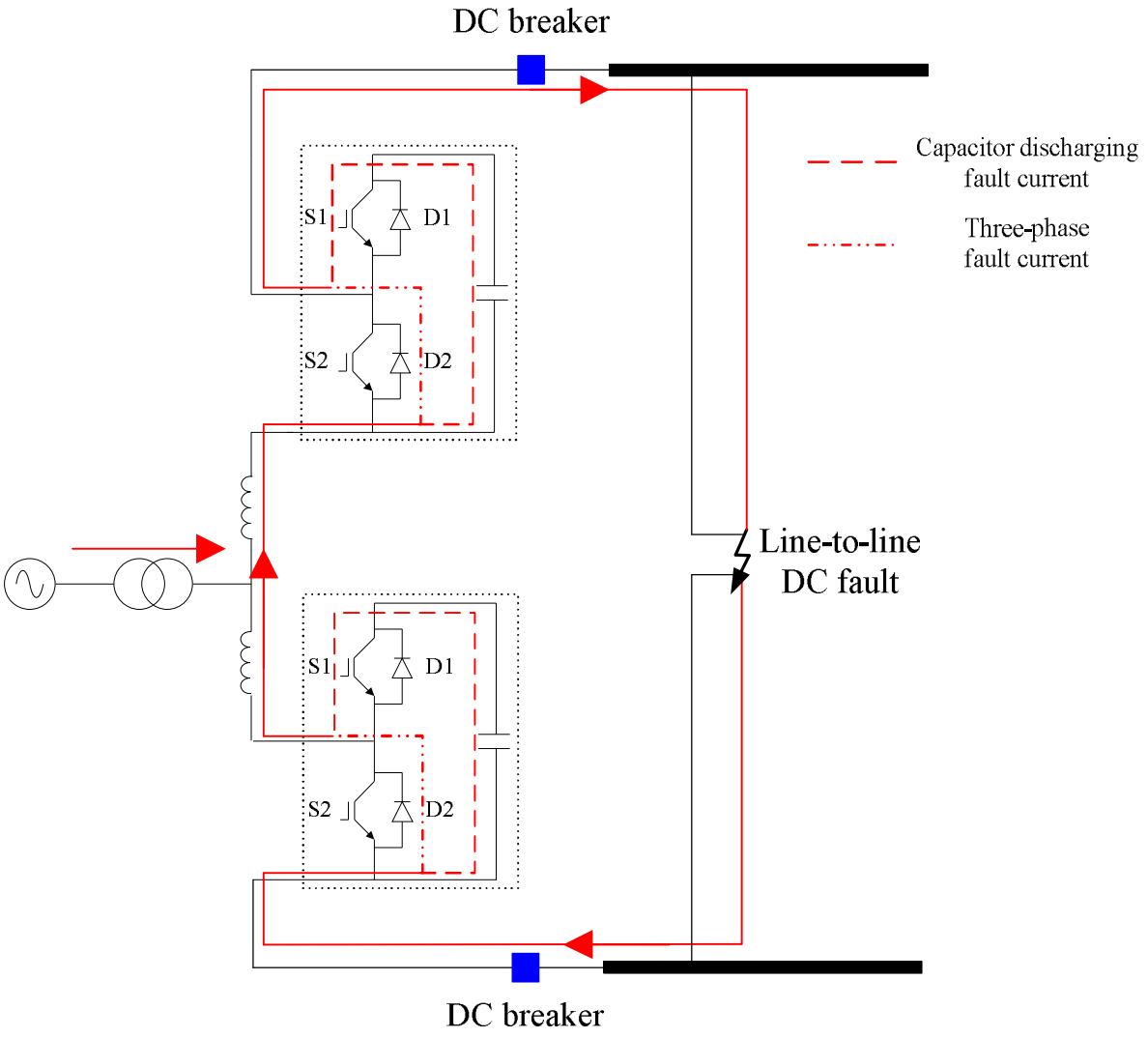


Fig. 4-3 Infeed of DC fault current

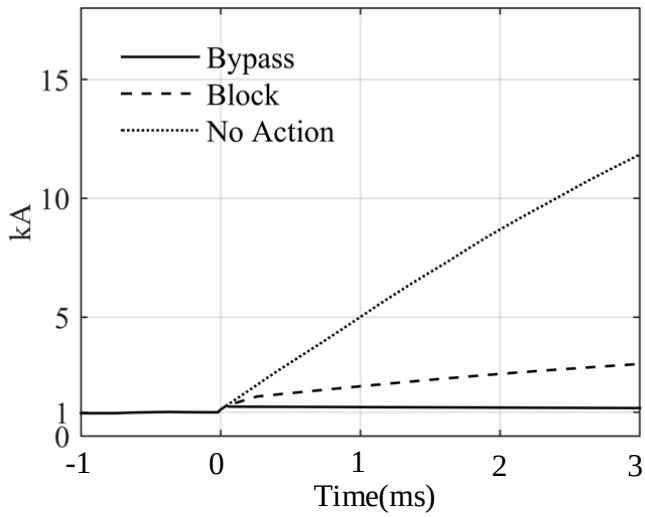
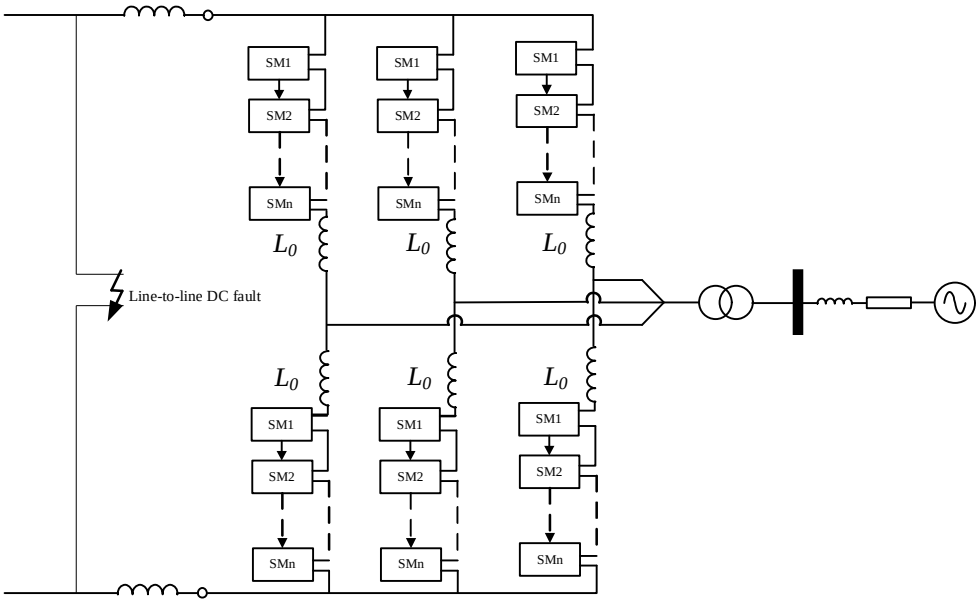
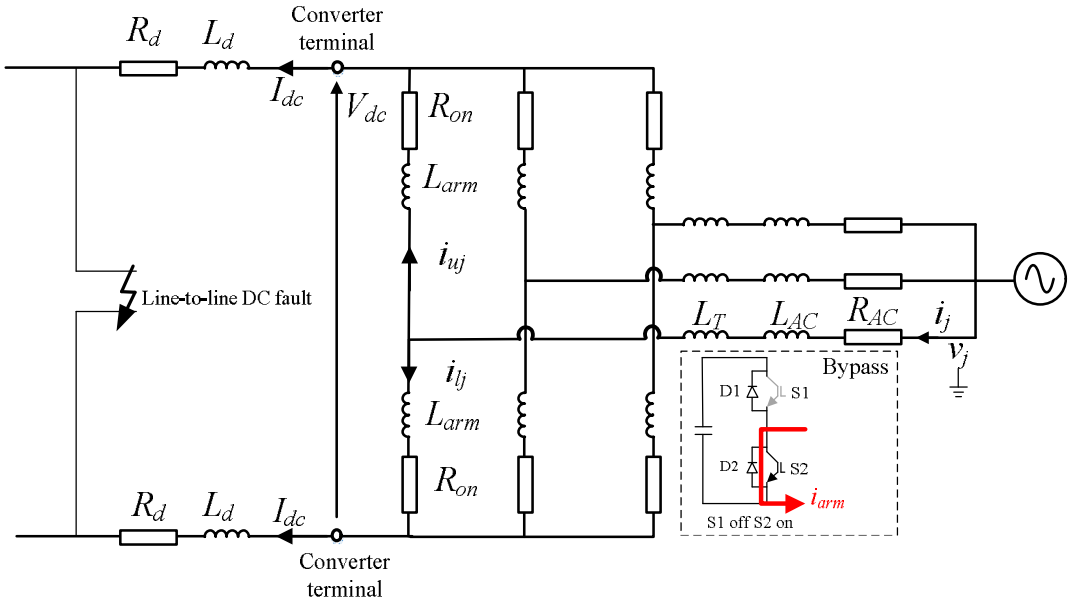


Fig. 4-4 DC fault current comparison caused by line-to-line fault at 0 ms



(a) Before bypassing



(b) After bypassing

Fig. 4-5 Equivalent circuit (per phase) after bypassing all SMs

4.3.1 Mathematical derivation

The expression of arm currents and AC current after bypassing is derived below to identify the feasibility of bypassing strategy. The equivalent circuit of bypassed MMC is shown in Fig. 4-5. L_{AC} and R_{AC} are AC system reactance. L_T is the equivalent inductance of AC transformer. To simplify the derivation, all these parameters (including AC source) have been referred to

the converter side of AC transformer. D2 and S2 are supposed to have same switch-on resistance r_{on}. R_{on} isy total switching-on resistance and its value should be N*r_{on} due to the unidirectional characteristic of D2 and S2. L_{arm} is arm inductance. L_d and R_d are equivalent DC inductance (including current limiting reactor within DC circuit breaker) and DC resistance before fault point.

After bypassing, the system can be seen as the first-order RL circuit with the initial state. The AC current (i_j), upper arm current (i_{uj}) and lower arm current (i_{lj}) can be represented as:

$$i_j = i_j^+ + (i_j^-(t_0) - i_j^+(t_0))e^{-(R/L)t} \quad (4-1a)$$

$$i_{uj}(t) = i_{uj}^+(t) + (i_{uj}^-(t_0) - i_{uj}^+(t_0))e^{-(R/L)t} \quad (4-1b)$$

$$i_{lj}(t) = i_{lj}^+(t) + (i_{lj}^-(t_0) - i_{lj}^+(t_0))e^{-(R/L)t} \quad (4-1c)$$

Where "j" represents the 3 phases *a*, *b*, *c*; "-" means the pre-bypassing steady state,"+" means the post-bypassing steady state, R and L are resistance and inductance of the bypassed circuit. t_0 is the line-to-line fault time.

Before bypassing, The MMC is under normal operation. The circulating current suppression control is applied. Only DC current and AC current go through each arm. Current components are drawn as:

$$i_j^-(t) = I_j^- \sin(\omega t + a) \quad (4-2a)$$

$$i_{uj}^-(t) = \frac{I_{dc}^-}{3} + \frac{I_j^- \sin(\omega t + \alpha)}{2} \quad (4-2b)$$

$$i_{lj}^-(t) = \frac{-I_{dc}^-}{3} + \frac{I_j^- \sin(\omega t + \alpha)}{2} \quad (4-2c)$$

where I_{dc} as a known value is the converter DC current. AC current comes from inner current loop control of MMC, and it is a known value as well.

In the case that an MMC bypasses all its SMs, converter terminal can be seen as the 0 V point (V_{dc} is supposed to 0 V here). Upper and lower arms are therefore in parallel. AC current and arm currents will be identical (in post-bypassing steady-state):

$$i_j^+(t) = I_j^+ \sin(\omega t + \beta) \quad (4-3a)$$

$$i_{uj}^+(t) = i_{uj}^+(t) = \frac{i_j^+(t)}{2} \quad (4-3b)$$

Substitution of Eq. 4-2 and Eq. 4-3 into Eq. 4-1 can obtain the extended expression of Eq. 4-1:

$$i_j(t) = I_j^+ \sin(\omega t + \beta) + (I_j^- \sin(\omega t_0 + \alpha) - I_j^+ \sin(\omega t_0 + \beta))e^{-(R/L)t} \quad (4-4a)$$

$$i_{uj}(t) = \frac{I_j^+ \sin(\omega t + \beta)}{2} + (\frac{I_{dc}^-}{3} + \frac{I_j^- \sin(\omega t_0 + \alpha)}{2} - \frac{I_j^+ \sin(\omega t_0 + \beta)}{2})e^{-(R/L)t} \quad (4-4b)$$

$$i_{lj}(t) = \frac{I_j^+ \sin(\omega t + \beta)}{2} + (-\frac{I_{dc}^-}{3} + \frac{I_j^- \sin(\omega t_0 + \alpha)}{2} - \frac{I_j^+ \sin(\omega t_0 + \beta)}{2})e^{-(R/L)t} \quad (4-4c)$$

The other parameters in Eq. 4-4 can be calculated as below:

$$I_j^+ = \frac{V_j}{\sqrt{(R_{on}/2 + R_{AC})^2 + ((L_T + L_{arm}/2) \times \omega)^2}} \quad (4-5a)$$

$$\beta = -\arctan(\frac{(L_T + L_{arm}/2) \times \omega}{R_{on}/2 + R_{AC}}) \quad (4-5b)$$

$$R = R_{on}/2 + R_{AC} \quad (4-5c)$$

$$L = L_T + L_{arm}/2 + L_{AC} \quad (4-5d)$$

where V is the magnitude of AC source voltage(v_j=$V_j$sin(ωt)).

To analysis DC current after bypassing, V_{dc} is produced by reducing DC current flowing through DC reactor. And its value cannot be ignored in DC current analysis. The expression of DC voltage and DC reactors can be represented as:

$$u_{dc}(t) = 2[L_d \frac{di_{dc}(t)}{dt} + R_d i_{dc}(t)] \quad (4\text{-}1)$$

After bypassing, the relationship between arm reactors and DC voltage is summarized as:

$$u_{dc}(t) = -\frac{2}{3}[L_{arm} \frac{di_{dc}(t)}{dt} + R_{on} i_{dc}(t)] \quad (4\text{-}2)$$

By subtracting Eq. 4-6 and Eq. 4-7, the dynamics of $i_{dc}(t)$ can be drawn:

$$(\frac{L_{arm}}{3}+L_d)\frac{di_{dc}(t)}{dt}+(\frac{R_{on}}{3}+R_d)i_{dc}(t)=0 \tag{4-3}$$

The expression of DC current can be obtained:

$$i_{dc}(t)=I_{dc}^{-}e^{-(\frac{R_{on}/3+R_d}{L_{arm}/3+L_d})t} \tag{4-4}$$

According to Eq. 4-4, after bypassing all SMs, the dynamics of upper arm current, lower arm current and AC current are determined by the value of AC reactors, arm reactors and their initial states. The expression of DC current seen Eq. 4-9 shows that after bypassing the DC current will decay to 0. The decay time is determined by the value of DC reactors and arm reactors.

4.3.2 Simulation verification

The Eq. 4-4 and Eq. 4-9 are verified through PSCSD/EMTDC simulation. The fault occurring time will influence the initial state of AC currents and both arms current due to the existing AC component. To find the maximum current of AC current and both arm currents, it is reasonable to analyse the fault occurring time in one whole AC cycle. When the fault is cleared, the converter will pull back to normal operation. it is essential to verify that there is no overcurrent during recovery time. And different short circuit ratio (SCR) will be analysed in order to find the feasible AC system for bypassing.

Dinghai substation within Zhoushan five-terminal HVDC system is selected as the simulation model. Its data is summarized in Appendix Table A-2. IGBT and diode switch-on resistance and SCR are assumed to be 0.01Ω and 3 individually. In the simulation, 11-level detailed MMC model is used rather than 251-level MMC taking into account of simulation speed. And the parameters of capacitor and switch are transferred equivalently.

The line-to-line fault occurs at 0 s, and the MMC is bypassed at the same time. As shown in Fig. 4-6, the blue line is the calculated result through Eq. 4-4 and Eq. 4-9, red dashed line is the result of the simulation. 10 cycles (200 ms) are selected to verify the correction of the equations. From Fig. 4-6, the simulated results are almost same with the calculated results. Upper arm current and lower arm current are slightly different because the Eq. 4-4 have not taken the dynamics of DC side into account. In sum, the dynamics of converter currents can be explained by Eq. 4-4 and Eq. 4-9

The operation time of DC breaker is normally around 5 ms, once the line-to-line fault is detected. After DC breakers isolate the fault, the converter is pull back to the normal operation. Therefore, bypassing time is supposed to 5 ms. Maximum currents on arms and AC side are analysed in Fig. 4-7 (a), (c) and (d). The DC fault occurs randomly. All fault occurring time which means one cycle (20 ms) is considered to find the possible overcurrent occurring on arms and AC side during 5 ms. The line-to-line fault occurs at 1 s. Maximum AC current is 5.0266 kA that is much lower than the AC transformer maximum withstanding current 20 kA. Maximum upper arm current and maximum lower arm current appear at different fault occurring time. And both are 2.8358 kA which still lower than the maximum IGBT and maximum diode peak current 3 kA. All the maximum currents occur at 5 ms. The maximum current analysis is able to identify the overcurrent risk of the MMC comprehensively during bypassing and locate the appearing time of maximum value.

The recovery current is shown in Fig. 4-7 (b), (d) and (f). Typical vector MMC control is applied all the time including bypass period. And after bypass, PI control within vector MMC control pull the AC current and arm currents into rated operation. The situations with maximum current are selected to analyse the recovery current according to Fig. 4-7 (a), (c) and (e). For the recovery current analysis of AC system and upper arm, the MMC is bypassed at 4.88 ms after the fault occurred. For lower arm, the MMC is bypassed at 1.5 ms after the fault occurred. From Fig. 4-7 (b), (d) and (f), there is no overcurrent during the recovery period. All currents are reduced to rating value gradually once MMC is pulled back to normal operation.

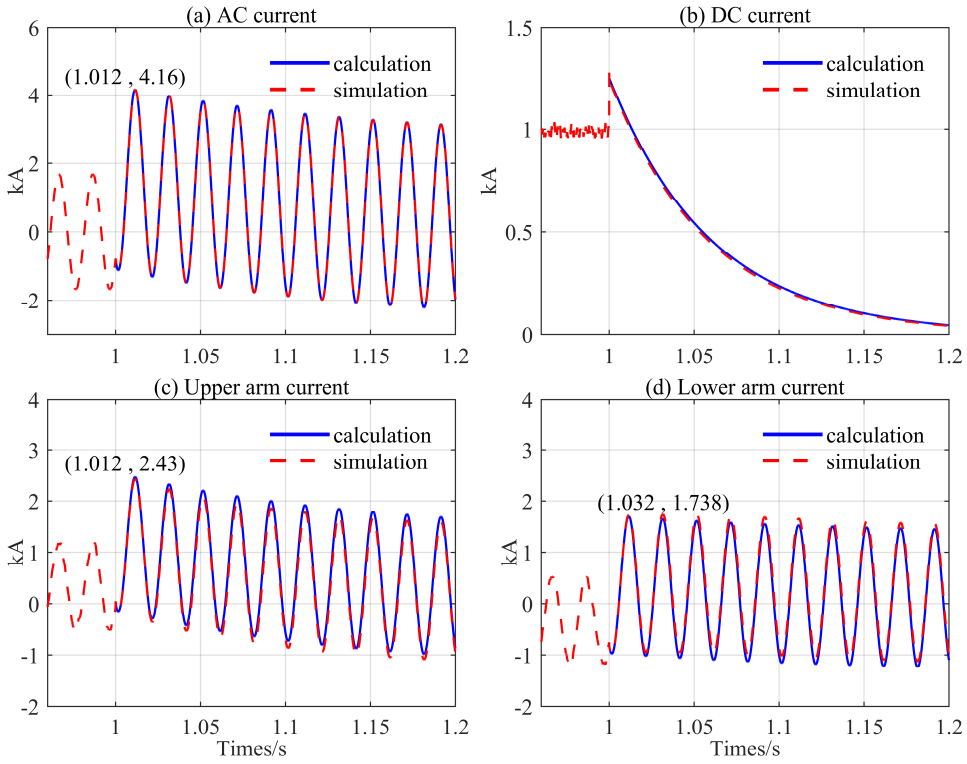


Fig. 4-6 Simulating verification of the converter currents

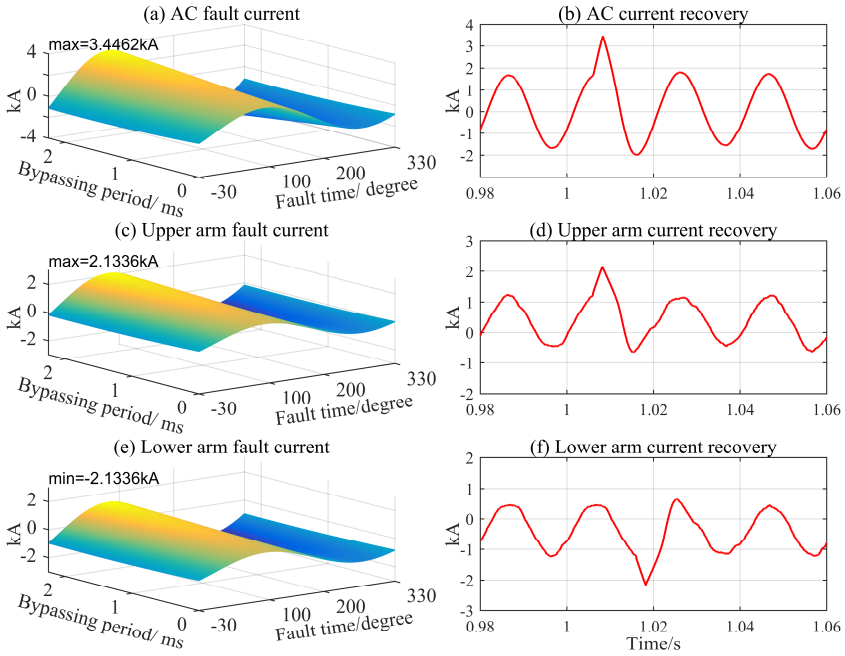


Fig. 4-7 Maximum current identification and fault recovery

Maximum AC current: fault position 6.01 ms (or 16.01 ms); bypassing period 2.25 ms

Maximum upper arm current: fault position 6.01 ms; bypassing period 2.25ms

Maximum lower arm current: fault position 16.01 ms; bypassing period 2.25ms

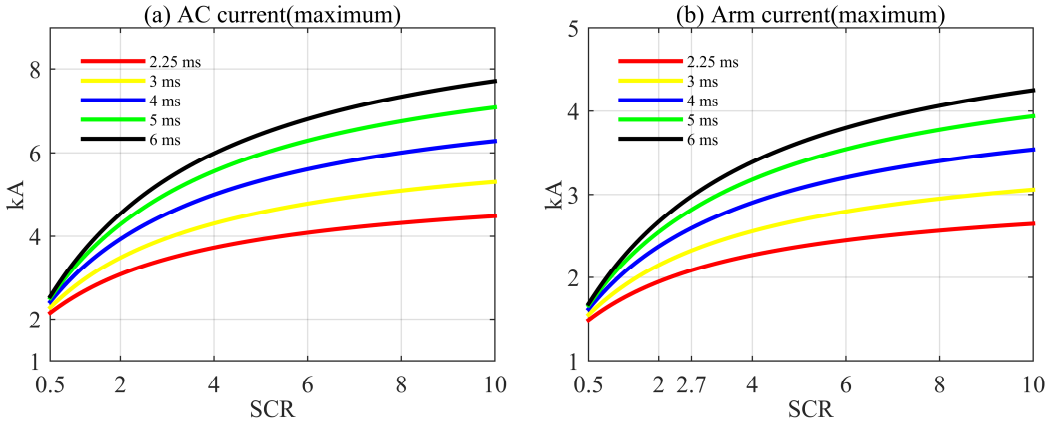


Fig. 4-8 SCR and bypassing period analysis

To analysis the feasibility of AC system, SCR is selected from 0.5 to 10, as shown in Fig. 4-8. The black line is the situation that the operation time of DC breaker is 5 ms, bypassing period is always same to the operation time. for example, if the operation time of DC breakers is 4 ms, bypassing period is 4 ms as well. The corresponding y-axis current comes from the maximum current analysis. upper arm and lower arm have the same amount of maximum

current in every condition, therefore the Fig. 4-8 (b) stands for both upper arm and lower arm. Higher SCR results in lower AC system reactance, and therefore the maximum AC current and arm current are higher. For Zhoushan MMC, the SCR of feasible AC system is [0.5 3.8]. If the operation of DC breaker is quicker such as 4 ms, the maximum current of AC system and arms are smaller under the AC system with same SCR. If the operation of DC breaker is equal to or under 3 ms, the AC system with SCR [0.5-10] is all feasible. The AC current is safe to AC transformer under any conditions.

4.4 **Protection Algorithm Design**

4.4.1 DC-CB operation

A hybrid DC-CB consists of both mechanical and power electronic switches (see Fig. 4-9). The low-loss branch includes an ultrafast disconnector and a load commutation switch. The main breaker is packed with series-connected IGBTs for fault interruption and surge arresters for fault energy absorption [75].

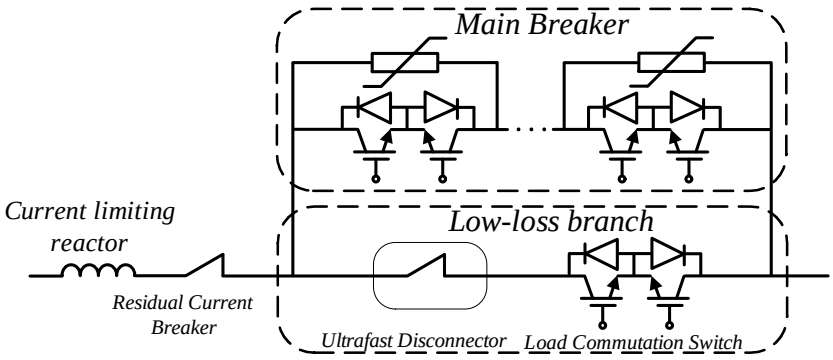


Fig. 4-9 Configuration of a hybrid DC-CB.

During normal operation, current flows through the low-loss branch only. Once a DC fault is detected, the load commutation switch is blocked to commutate the fault current into the main breaker. The ultrafast disconnector will then open (this action causes delays in the order of milliseconds). The main breaker will trip to isolate the fault, and the fault energy is absorbed by the surge arresters. The residual current breaker will also open after the fault current has reduced to zero [10].

A. Coordination of DC-CBs and MMCs

The first step in the coordination of DC-CBs and MMCs is fault detection and discrimination. For the method proposed in this work, this will be entirely based on local measurements of current and voltage at the converter stations. An example based on the grid shown in Fig. 4-2 is presented to explain the methodology. The system is rated at +/-320 kV and all branches are overhead lines (OHLs) with a length of 100 km.

A solid pole-to-pole fault at 0.6 s is applied to one terminal of a DC line as indicated in Fig. 4-2 (*i.e.* next to CB-12). Fig. 4-10 shows the voltages and currents measured by the DC-CBs at CB-12 (faulted line) and at CB-13 (healthy line). In this test, the DC-CBs remain closed, and the MMCs operate normally. It can be observed that the voltage at the faulted point (denoted as V-12) drops to zero immediately. However, the change of voltage at CB-13 (V-13) is much smaller due to the reactors associated with the DC-CBs separating the two measurement locations. Meanwhile, current at CB-12 (I-12) rises significantly (by six times) within 2 ms following the fault; conversely, the current magnitude at CB-13 (I-13) decreases, and its direction tends to reverse to infeed the faulted point.

Based on the previous observations it seems reasonable to use voltage and current characteristics to establish a method for fault detection. A simple solution may be based on an undervoltage criterion, which allows a DC-CB to trip when the voltage drops below a threshold (*e.g.* <300 kV). However, if this is used on its own in a less capacitive grid (such as a system connected by OHLs), the DC-CBs may be incorrectly tripped following an AC disturbance transferring onto the DC system –which could lead to oscillations in the DC voltages.

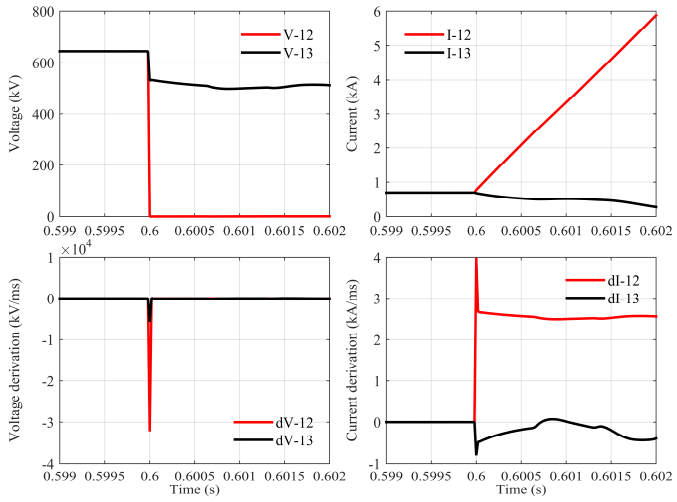


Fig. 4-10 DC pole-to-pole fault: a) current derivative; b) current; c) voltage derivative; (d) voltage.

The robustness for detecting faults in the DC system can be improved by combining the undervoltage detection with a criterion based on the derivative of the DC current. This has to be done with care as derivative signals tend to be "noisy"; thus, some filtering is required to avoid false triggering. In the following example five consecutive samples are used (a sampling time of 20μs was adopted).

The combined criterion can be expressed as:

$$if\ (V_{dc} < V_{thr}) \cap (\frac{di_{dc}}{dt} > \frac{di}{dt_{thr}})\text{for five consecutive samples, then } flag_{flt} = 1 \qquad (4\text{-}5)$$

The criterion above allows a DC-CB to turn a fault flag on (*i.e.* $flag_{flt} = 1$) when local data samples of voltages are lower, and the current derivatives are larger than their pre-set thresholds. After the fault flag is turned on, the DC-CB opens its low-loss branch to start the breaking procedure. The next step is to bypass the SMs within the MMCs to suppress the DC fault current. Similarly, an MMC could also sense a DC fault by measuring local voltages or currents. For instance, an MMC can bypass its SMs based on the detection of undervoltage and a fast decrease of DC voltage (*dv/dt*).

An MMC can be also bypassed when the local DC-CBs (*i.e.* connected to the same DC busbar) generate a fault flag. The combined criterion for MMC bypassing is expressed as:

$if\ (V_{dc} < V_{thr}) \cap (\frac{di_{dc}}{dt} < \frac{di}{dt_{thr}})$for five consecutive samples, or $flag_{flt} = 1$,then $flag_{bypass} = 1$ (4-6)

The previous criterion allows an MMC to turn on a bypass flag (*i.e.* $flag_{byass} = 1$) when either five consecutive local data samples of voltages and their derivatives are lower than their pre-set thresholds, or when the local DC-CBs turns on a fault flag ($flag_{flt} = 1$). An MMC will then immediately bypass its SMs after the bypass flag is turned on.

The MMC bypass operation should be extremely fast to prevent the SM capacitors from discharging prior to the operation of ultrafast disconnectors on the DC-CBs. Then, the DC-CBs will isolate the faulted circuit within several milliseconds.

The final step is to recover the MMC after fault isolation once the current and its derivative at the faulted circuit are close to zero. The DC-CBs can simply monitor the current profiles at the faulted circuit and allow the local MMC to turn off the bypass flag and then recover. The criterion for recovery is expressed as:

$if\ (|I_{dc}| < I_{err}) \cap (\left|\frac{di_{dc}}{dt}\right| < \frac{di}{dt_{Ierr}})$f for five consecutive samples, then $flag_{bypass} = 0$ (4-7)

When the absolute values of five consecutive samples of currents and their derivatives are less than their thresholds (which are set very close to zero), the bypass flag will be turned off ($flag_{byass} = 0$), and the MMC will immediately recover. Notice that the SM capacitors do not discharge during bypassing and hence recovery is very fast.

The coordination sequence of DC-CBs and MMCs in the event of a DC fault is summarised in Fig. 4-11. After a DC fault occurs (at $t = 0$ ms), DC current rises, and DC voltage drops. The DC-CBs and MMCs will take a time of T_1 to detect and discriminate the fault. The load commutation switch of the DC-CBs will open, and the MMCs will immediately bypass their SMs. These are IGBT based components, and hence their action takes a short time (from T_1 to T_2). The mechanical part of the low-loss branch within the DC-CBs then takes several milliseconds to open and commutate the fault current to the IGBT-based main breakers (from T_2 to T_3). The main breakers interrupt the fault current and generate the signal for the recovery

of MMCs at T_4 once fault isolation has been achieved. The MMC will subsequently recover at T_5. The residual current breaker of the DC-CBs will take a long time to open subject to the absence of fault current (at T_6).

The coordination of DC-CBs and MMCs happens between T_2 to T_4, where the ultrafast disconnector starts to open. By bypassing the MMCs SMs the increase of fault current can be effectively limited during this period. The entire coordination time takes a few milliseconds only (*e.g.* 2 ms).

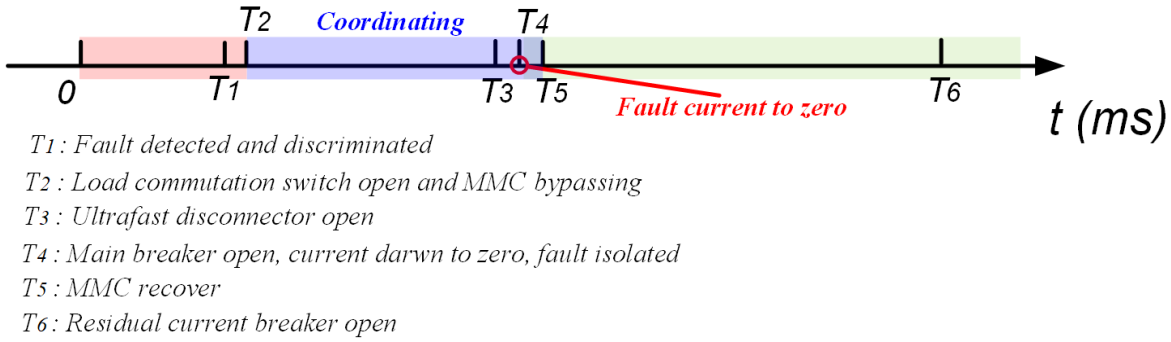


Fig. 4-11 Sequence order of coordinating DC-CBs and MMCs.

4.5 **Simulation Study**

4.5.1 Test System

The algorithm for coordinating DC-CBs and MMCs shown in Fig. 8 has been tested in a three-converter, symmetric monopole DC system rated at +/-320 kV. This system is meshed by three OHLs as shown in Fig. 4-12. DC-CBs are located at both ends of each DC line. The entire system is grounded with a high impedance at its DC side. The AC systems are rated at 230kV and have a short circuit ratio of 2.5. Converter MMC1 operates in DC voltage control mode [77][78] to regulate voltage to 640 kV, while converters MMC2 and MMC3 operate in power control mode to regulate power to 900 MW.

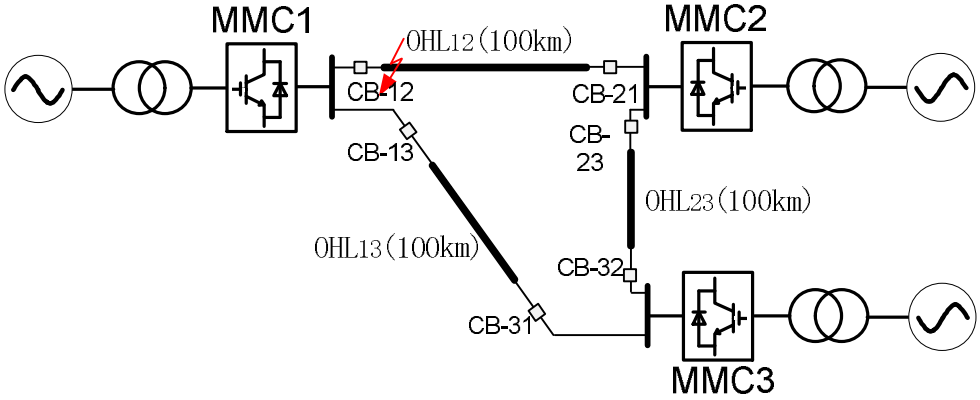


Fig. 4-12 One line diagram of meshed DC test system.

4.5.2 Modelling of DC Components

All OHLs and cables are represented using the frequency dependent model provided in PSCAD/EMTDC. The conductor data (Type AAAC-806-A4-61) and ground wire data (Type AFL CC-75-528) used for OHL modelling are given in [79][80] while the structure of the tower is provided in [81].

All DC-CBs are modelled as simplified hybrid DC-CBs (see Fig. 4-9). A delay of 2.5 ms is considered for the mechanical operation of the breakers while the actions of IGBT-based switches are assumed to have no delay. The limiting reactors are set to 0.1 H and surge arrester banks (rated at 480 kV, 1.5 p.u) are placed in parallel to absorb the fault energy stored in the DC system. All MMCs are represented through the equivalent models developed in [82].

Table 4-1 Thresholds: MMCs Protection and Control Settings

Components	Items	Description
Detection/discrimination (Turn on fault flag)	Undervoltage Large current derivative	V_{dc}< *500 kV* di_{dc}/dt> 2.5 *kA/ms*
MMC bypassing (Turn on bypass flag)	Undervoltage Small voltage derivative	V_{dc}< *500 kV* dV_{dc}/dt< *500 kV/ms*
	OR fault flag of local DC-CB is turned on	$flag_{flt}$=1
MMC recovery (Turn off bypass flag)	Current close to zero Current derivative close to zero	$\|I_{dc}\|$< *0.001 kA* $\|di_{dc}/dt\|$<*0.001kA/ms*

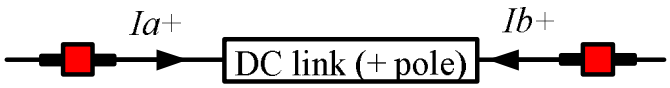


Fig. 4-13 Sign convention of current.

4.5.3 Case Studies

A pole-to-pole fault was applied (at 0.6s) at one end of OHL_{12} to show the effectiveness of the proposed coordination algorithm. The thresholds settings for the protection criterion are given in Table 4-1. The current sign convention is shown in Fig. 13. Three cases are studied for comparison:

(a) DC-CBs at the faulted circuit open, no MMCs action;

(b) DC-CBs at the faulted circuit open, MMCs block;

(c) DC-CBs at the faulted circuit open, MMCs bypass;

It should be highlighted that the blocking algorithm is similar to the one designed for bypassing.

Simulation results are given from Figs. 4-14 to 4-16. The algorithm for DC-CB fault detection (and discrimination) is kept the same for all cases. Hence, DC-CBs at CB-12 detect

the fault immediately at 0.60012 s, and those at CB-21 detect the fault at 0.60048 s. Other DC-CBs in the grid remain closed.

When the MMCs have the capability to block or bypass, only MMC1 and MMC2 sense the fault and block or bypass at 6.00010 s and 6.00044 s respectively. The MMCs recover when the DC-CBs isolate the fault (*i.e.* I-12 and I-21 decrease to zero); for MMC1 this occurs at 0.60262 s and for MMC2 at 0.60266 s.

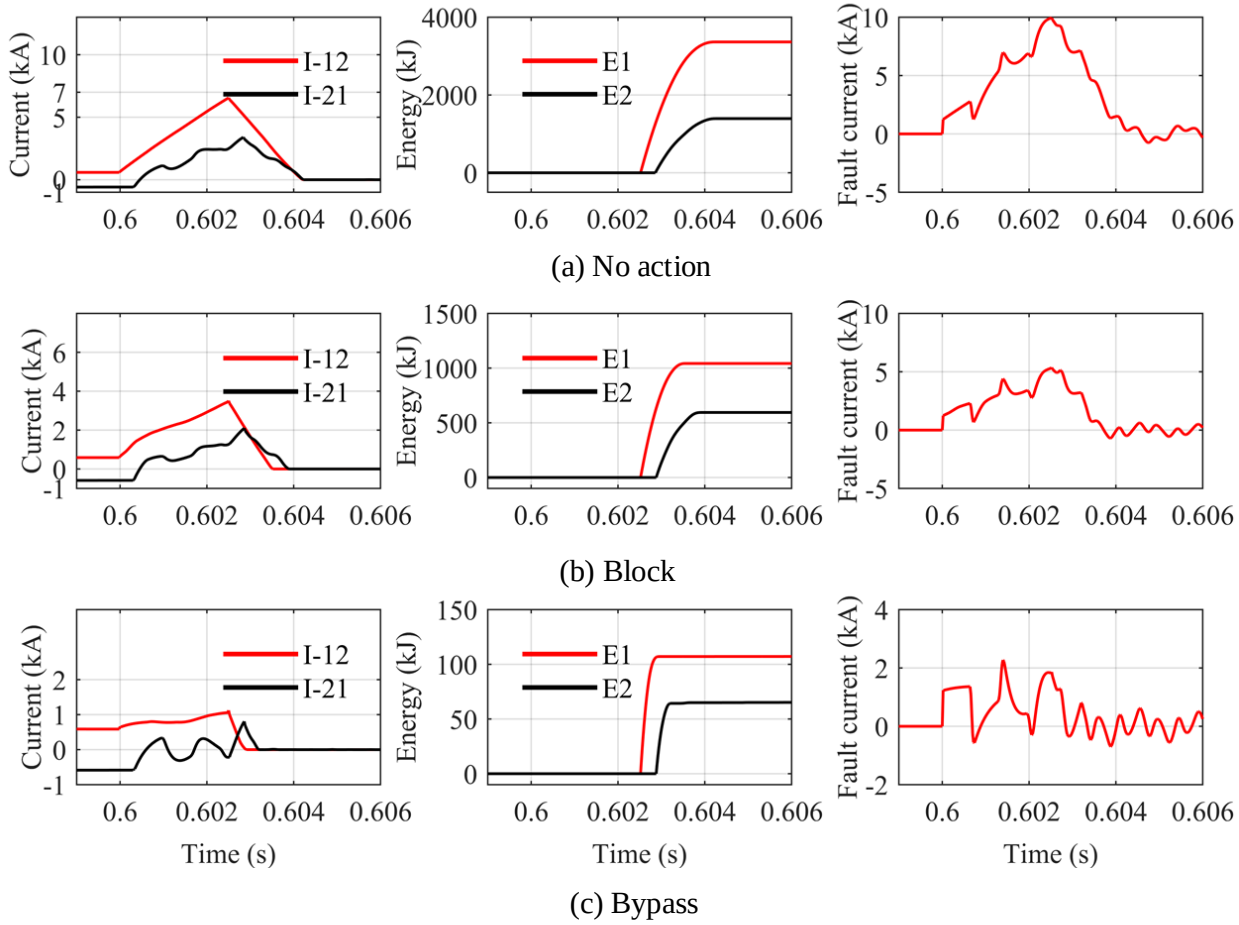


Fig. 4-14Current and energy at DC-CBs and the total fault current when MMCs (a) take no action; (b) block; (c) bypass.

Fig. 4-14 shows the current (I-12, I-21), the energy (E1, E2) measured at CB-12 and CB-21, and the total fault current. Taking CB-12 as an example, its interrupted current (I-12) is significantly reduced when the MMC is bypassed (1.1 kA) as compared to either when it is blocked (3.8 kA) or when no action is taken (6.9 kA). Additionally, the absorbed energy (E1)

is reduced by 97%, from 3400 kJ (no action) to 108 kJ with MMC bypassing. This significant reduction would allow DC-CBs to be designed at a much lower rating. Moreover, the total fault current is also suppressed to less than 2.2 kA. These results clearly demonstrate the benefits of bypassing the MMC and using DC-CBs to isolate the DC fault.

Fig. 4-15 shows the DC voltages measured at the MMCs. Bypassing of MMC1 and MMC2 allows them to temporarily operate at low DC voltages (*i.e.* V1 and V2) as if they were blocked. The MMCs can immediately recover as almost no discharge of the SM capacitor takes place. In addition, the bypassing seems to result in a lower overvoltage when compared to the other two scenarios. Fig. 13 shows the arm current of MMC1 during the fault. It should be noted that if the bypassing action is done for a long time, the arm currents will start to increase; to avoid this, the action is restricted to less than 3 ms. This demonstrates that a temporary bypass would not produce additional disturbances to the AC system.

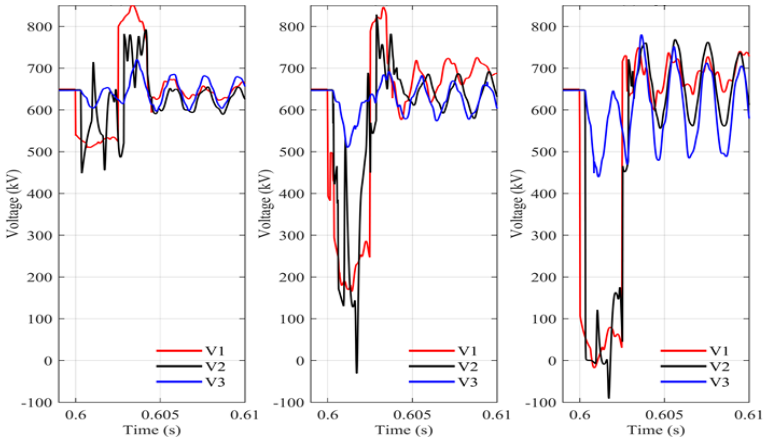


Fig. 4-15 DC voltages when MMCs (a) take no action; (b) block; (c) bypass.

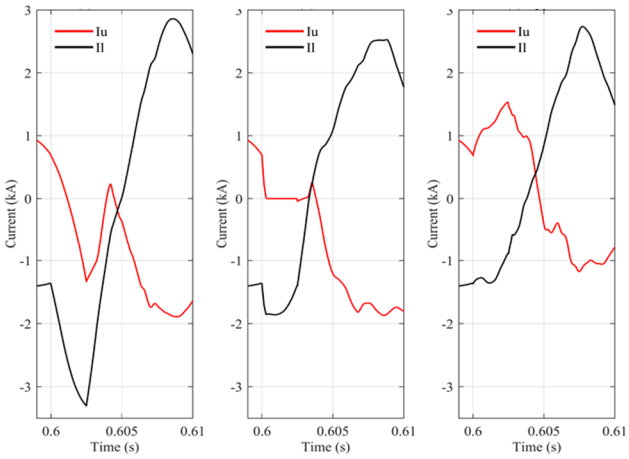


Fig. 4-16 Arm current (MMC1) when MMCs (a) take no action; (b) block;(c) bypass.

4.6 **Summary**

The coordination of DC-CBs and MMCs for MTDC grid protection has been examined and its benefits exhibited. The algorithm for an MMC bypass operation has been assessed and its effectiveness to reduce DC fault current and absorbed energy has been tested using a three-terminal HVDC system. A method for using the DC-CBs to detect, discriminate and isolate DC faults has been also included for completeness. Moreover, the coordination sequence for DC-CBs and MMCs has been established.

It has been demonstrated that if the DC fault isolation by DC-CBs takes place while the SMs of the MMCs are temporarily bypassed, a substantially lower fault current is produced. In particular, the results for the presented test system show that the bypassing of MMCs significantly reduces the interrupted current (by 84.1%) and the absorbed energy (by 97%) when compared to the case when no action is taken. Additionally, the MMC bypassing action offers a superior fault current suppression than when the MMC is blocked. Given that the temporary bypass action only impacts the arm current slightly, the use of the proposed algorithm will neither deteriorate AC system performance nor damage the IGBTs.

CHAPTER 5 INTERCONNECTION OF LCC-HVDCS WITH THE CAPABILITY OF POWER REVERSAL

For bulk-power and long-distance transmission, most of the existing HVDC systems are point-to-point LCC-HVDCs. By interconnecting existing LCC links can achieve more economical benefits and higher flexibility of power transfer. However, due to different voltage levels and control modes of these links, it is impossible to interconnect them together directly through dc cables. Interconnecting LCC links via a DC transformer at a geographic crossing point or close proximity between the LCC links is proposed. Such connection is to achieve the benefits of dc grid operation without incurring a vast amount of costs by constructing new HVDC transmission lines but making full use of existing LCC lines. As one type of the interconnected device between HVDC systems, the DC/AC/DC converter is able to achieve high-voltage connection and bulk-power transportation, which makes this device fit the interconnection of LCC-HVDCs. The DC/AC/DC converter based on half-bridge sub-modules is designed for power regulation between two LCC links under different voltage levels.

To achieve an efficient, interconnected LCC-HVDC system, the DC/AC/DC converter is possible to operate under the condition that one LCC-HVDC runs at normal operation and the other at the operation of power reversal. This requests the DC/AC/DC converter to regulate power in terms of the interconnection between the positive and the negative voltage. Considering the economy of the interconnection, the DC/AC/DC converter uses half-bridge sub-modules, which is not able to connect the negative-voltage system. To achieve the ability of negative-voltage connection, a switch yard is proposed to reverse the voltage polarity of DC/AC/DC converter. And a control system of the DC/AC/DC converter is proposed to protect the normal LCC-HVDC from the influence of LCC-HVDC during power reversal.

5.1 Motivation

The interconnection of HVDC systems is the trend for the development of HVDC grid. The interconnection will promote the increase of the flexibility and efficiency of power transportation, enhance the electricity trading and balance the demand for electricity. The LCC-HVDC has been put in operation for many decades and proven to be a mature and reliable technology. To date, LCC-HVDC projects are dominant in commissioned HVDC projects, which makes LCC-HVDC projects have a big potential to be interconnected. Many of them have geographical crossing points such as Three George-shanghai LCC-HVDC system and Jingping-Sunan LCC-HVDC system[83]. The crossing point could be used to interconnect two LCC-HVDC systems through a proper device.

As one of the interconnection devices, the DC/AC/DC converter is constituted by two modular multi-level converters (MMC) whose AC sides are connected each other. It is considered as the suitable device [84] to interconnect LCC-HVDC systems due to its ability of high-voltage connection and bulk-power transportation. its control strategy for power regulation and modulation method have been studied in [85][86] individually.

The concern about the DC/AC/DC converter is the high capital cost due to the use of two whole MMC converters. To abandon the use of filters, the MMC contains a huge number of sub-modules (SM). The isolated AC side of the DC/AC/DC converter allows for variable operation frequency. To reduce the cost, a high operation frequency is identified [87] to achieve significant volume saving of each SM's capacitor. And the value of the reactors such AC transformer and arm inductors are reduced as well. To improve the efficiency of power transportation, different types of the AC voltage waves, including triangle wave, sine wave and square wave, are compared in [88]. It is verified that the square wave can achieve higher transmission efficiency under high-frequency operation.

Flexible power transmission needs the LCC-HVDC to be cable of power reversal. As the converter valves of the LCC-HVDC, the thyristors only allow for unidirectional current flow. Reversing voltage polarity from $+V_{dc}$ to $-V_{dc}$ becomes the solution to reverse the power. For an interconnected system, it is possible that one LCC-HVDC is under power reversal operation and the other LCC-HVDC works under normal operation. To achieve a truly efficient interconnected system, the DC/AC/DC converter should regulate power under such power reversal condition.

Taking into account of the concern about high capital cost, the full-bridge SM, which can provide the ability of negative voltage connection, is not recommended to be used. The Half-bridge SM can only generate 0 or $+V_{SM}$ voltage level. It is economical to have an additional switch for changing the voltage polarity of the corresponding MMC within the DC/AC/DC converter when negative voltage connection is requested.

Except for flexible power regulation, the DC/AC/DC converter should isolate the disturbances from the other LCC-HVDC and maintain their own operation. During power reversal of one LCC-HVDC, its DC voltage will decrease slowly from +1 p.u. to -1 p.u.. A proper design of control system should be considered for the DC/AC/DC converter to maintain both LCC-HVDC at their own operation. When the process of power reversal is finished, the DC/AC/DC converter goes back to control the power flow between LCC-HVDCs.

This chapter studies the DC/AC/DC converter based on half-bridge SMs for the interconnection of two LCC links. The control system of the DC/AC/DC converter is proposed to achieve flexible power regulation, and isolate the disturbances between two LCC links, such as voltage reduction operation or power reversal operation of one LCC link. A switch yard is designed for the DC/AC/DC converter with half-bridge SMs to achieve the ability of negative voltage connection. The whole system will be simulated in PSCAD/EMTDC.

5.2 Interconnected system

The interconnected system is shown in Fig. 5-1, the two LCC links are interconnected via DC/AC/DC converter. The switch yard locating at the DC port of the DC/AC/DC converter is used to change the voltage polarity of the MMC in the DC/AC/DC converter. The structure of a DC/AC/DC converter is shown in Fig. 5-2, two MMCs connected at the AC side. If an order send to the DC/AC/DC converter to regulate the power from LCC-HVDC I to LCC-HVDC II, such amount of the power will be converted from the DC to AC at MMC I, then be sent to MC II, finally be sent to LCC-HVDC II via being converted from the AC to the DC at MMC II. There is an AC transformer locating on the AC side of the DC/AC/DC converter, which can boost the voltage or reduce the voltage to the desired level for both MMCs and provide the galvanic isolation.

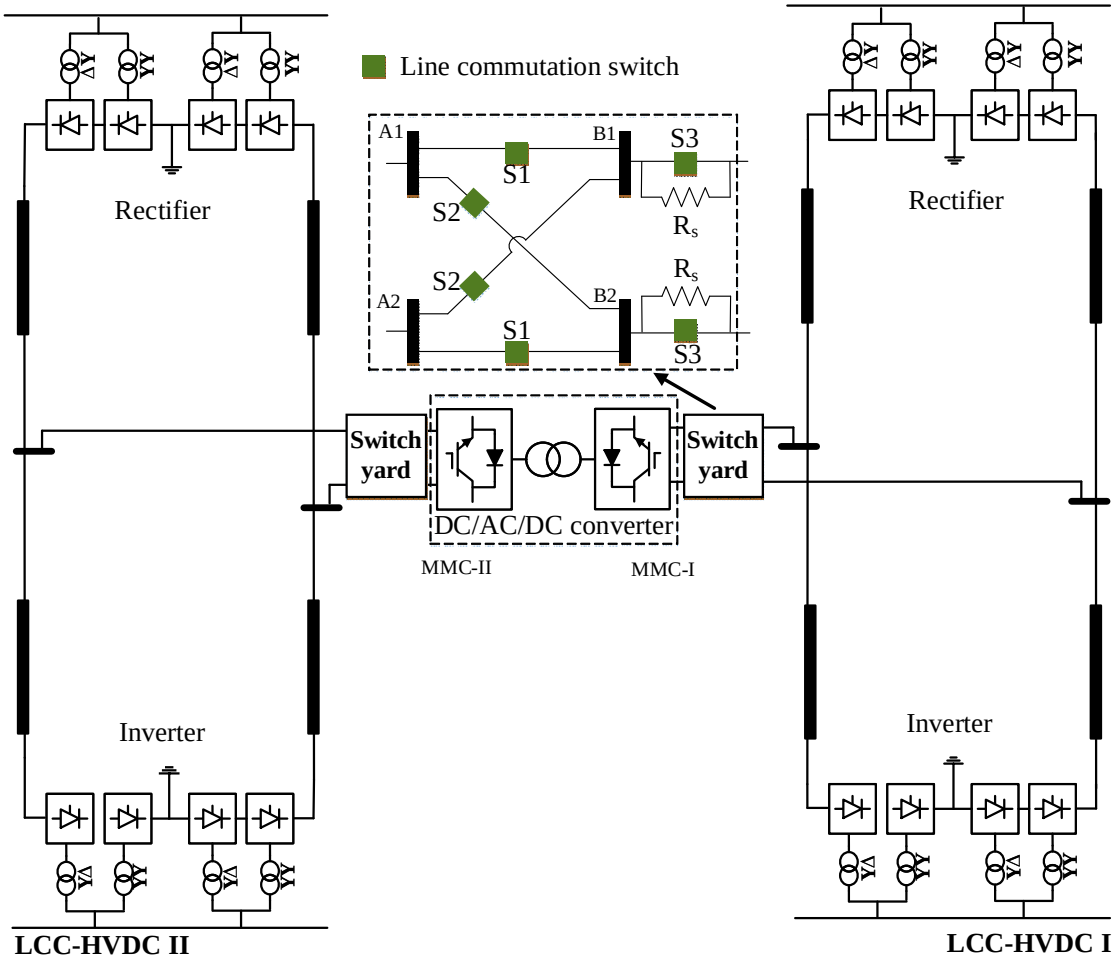


Fig. 5-1 Interconnected system

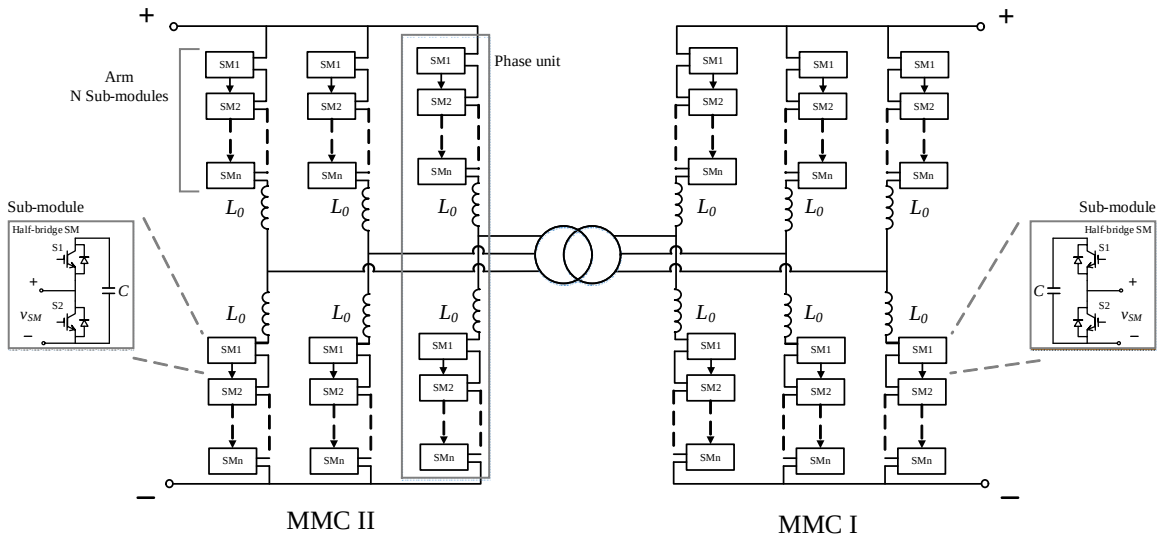


Fig. 5-2 DC/AC/DC converter based on half-bridge SMs

5.3 Control system of DC/AC/DC converter

The control system has two parts, one is power regulation control that works in stable conditions, and the other is isolation control that is used to isolate the disturbance during the process of the power reversal of one LCC-HVDC.

5.3.1 Power regulation control

Before designing the power regulation control, the power flow analysis should be made to ensure the feasibility of the power control system. One line diagram of the DC/AC/DC converter is drawn in Fig. 5-3. L_T is the equivalent inductance of the AC transformer.

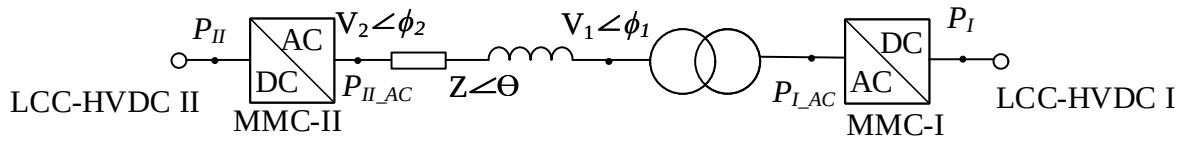


Fig. 5-3 Power flow analysis in the interconnection system

According to the active power balance between the DC side and the AC side of a MMC, the following equations can be drawn:

$$P_I = P_{I\_AC} \qquad (5-1a)$$

$$P_{II} = P_{II\_AC} \qquad (5-1b)$$

The power flow at the AC side can be calculated as:

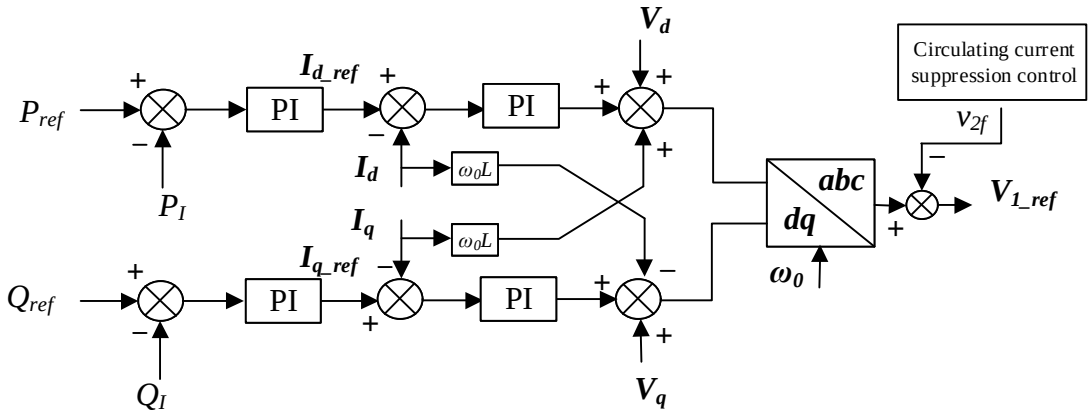
$$P_{I\_AC} = \frac{V_2 V_1}{Z}\cos(\theta - \phi_2 + \phi_1) - \frac{V_1^2}{Z}\cos\theta \qquad (5-2a)$$

$$Q_{I\_AC} = \frac{V_2 V_1}{Z}\sin(\theta - \phi_2 + \phi_1) - \frac{V_1^2}{Z}\sin\theta \qquad (5-2b)$$

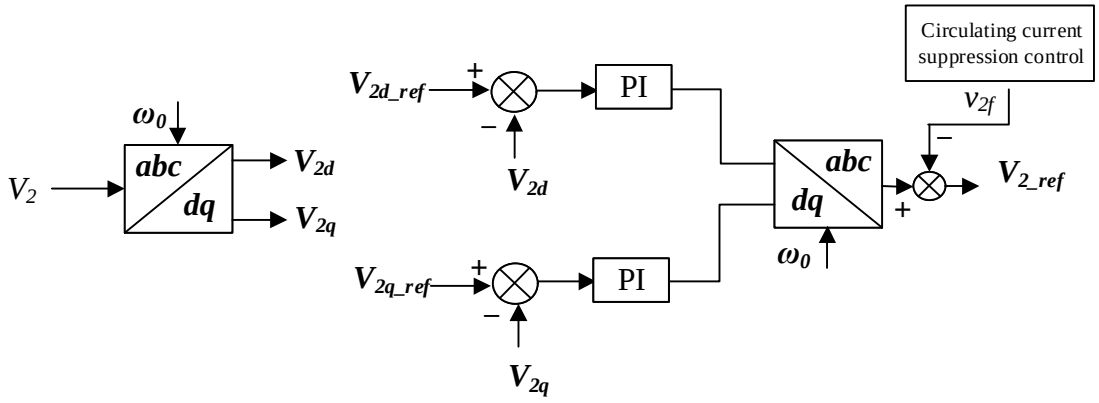
Where $P_{ACI}$and Q_{ACI} are the active power and reactive power at the ac side on MMC-I.

From power flow analysis, if MMC II can control the AC voltage and MMC I can control the power, the power flow from LCC-HVDC I and LCC-HVDC II can be achieved.

The control diagrams are shown in Fig. 5-4. In Fig. 5-4 (a), the outer loop includes active power control and reactive power control with PI controllers. The reactive power only flows within the DC/AC/DC converter. Therefore it can be controlled as any constant reasonable value. The power flow regulation between LCC-HVDC I and II is achieved by the active power control. The inner loop is designed to avoid the overcurrent. The MMC II control the AC voltage directly without inner current control, see Fig. 5-4 (b). Because MMC I and MMC II are in series connection, only one inner current control is enough to avoid the overcurrent from both MMCs.



(a) MMC-I control system



(b) MMC-II control system

Fig. 5-4 Power regulation control of the DC/AC/DC converter (circulating current suppression control is described in Section 2.3.6)

5.3.2 Isolation Control system

To avoid the disturbances from the power reversal of the LCC-HVDC and maintain the normal operation of the other LCC-HVDC, an isolation control system is designed for the DC/AC/DC converter.

The MMC works as a controllable AC voltage source to achieve desired power transfer. For normal operation of the DC/DC/AC converter, one MMC (such as MMC I) control the active power, and the other supports the desired AC voltage. Therefore, power can be regulated between two LCC-HVDCs according to power balance between the AC side and the DC side of the DC/AC/DC converter.

During the power reversal of LCC-HVDC-I, the DC voltage of MMC-I will track the voltage change of LCC-HVDC-I. To maintain its own operation of LCC-HVDC-II, two targets will be achieved by the isolation control. Firstly, the isolation control should achieve zero power flow on the AC side of the DC/AC/DC converter, which means there is no power exchange between MMC-II and LCC-HVDC-II. Secondly, the isolation control should maintain the stable operation of the DC/AC/DC converter during power reversal.

The terminal AC voltage $v_{ac\text{-}I}$ and $v_{ac\text{-}II}$ are fully controlled by MMC-I and MMC-II. The AC power is determined by the voltage difference and the total equivalent AC inductance. The MMC-I is designed to control the current, as shown in Fig. 5-5, its current reference is set to 0 to maintain none AC power flow. MMC-II is designed to support the AC voltage, a constant AC voltage reference under the frequency ω_0 will be given.

To maintain the stable operation of the DC/AC/DC converter, the influence of the DC voltage change of LCC-HVDC-I should be taken into account. To analyse the relationship between the DC voltage and the AC voltage, the equivalent circuit of the MMC is shown in Fig. 5-6. According to the KVL law, the expression of the AC voltage in terms of the DC voltage is shown below:

$$v_{acj} = V_{dc} - v_{uj} \qquad (5-3a)$$
$$v_{acj} = v_{lj} - V_{dc} \qquad (5-3b)$$

Where j is the phase a, b, c. v_{uj} and v_{lj} are the voltage of upper arm and lower arm.

The expression of the upper arm voltage and the lower arm voltage is:

$$v_{uj} = V_{dc} - kV_{dc}\sin(\omega_0 + \theta) \qquad (5-4a)$$
$$v_{lj} = V_{dc} + kV_{dc}\sin(\omega_0 + \theta) \qquad (5-4b)$$

Where $0 \le k \le 1$, k and θ are control index from the control system to control the arm voltage.

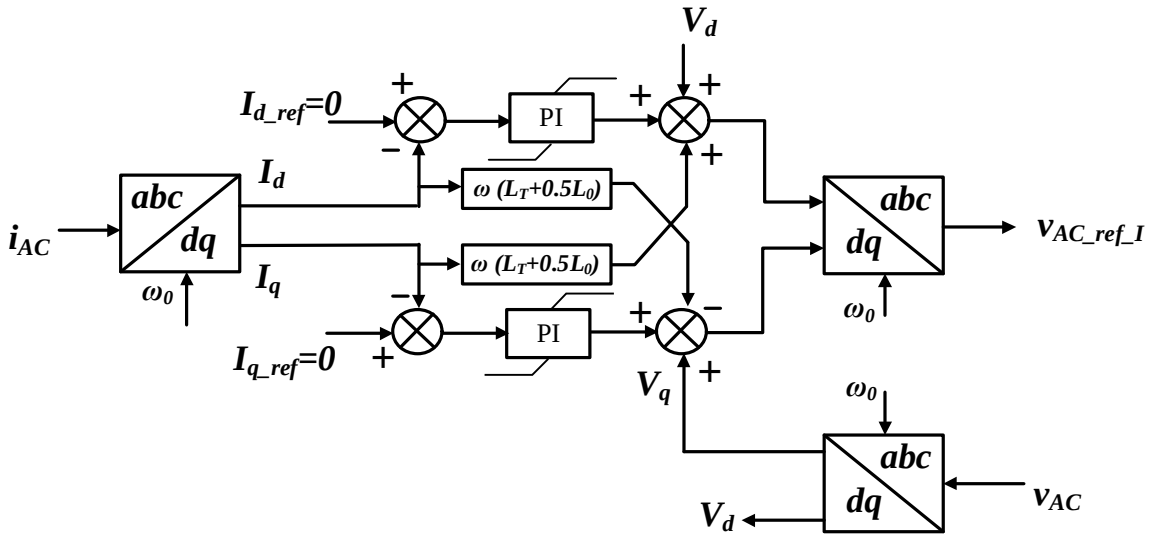


Fig. 5-5 Current control of the MMC-I

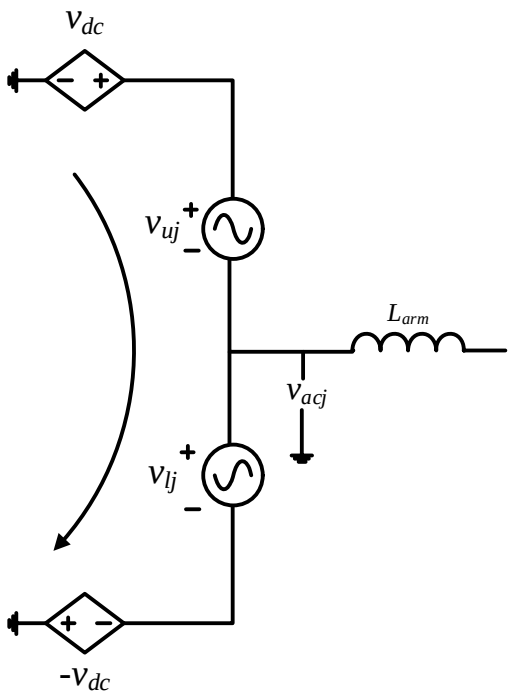


Fig. 5-6 Equivalent circuit of on phase unit of the MMC

From Eq.5-3 and Eq. 5-4, the AC voltage can be expressed as:

$$v_{ac} = kV_{dc}\sin(\omega_0 + \theta) \qquad (5-5)$$

According to Eq. 5-5, maximum AC voltage magnitude of MMC is proportional to its DC voltage. During power reversal, the AC voltage magnitude of MMC-I is reduced gradually due to the reduction of the DC voltage. If MMC-II maintains its AC voltage, the current control of MMC-I will collapse. Therefore, a coefficient g is added into AC voltage control of MMC-I to reduce the magnitude of AC voltage. It can be calculated as:

$$v_{ac\_II} = gV_{dc\_II}\sin(\omega_0 + \theta) \qquad (5-6a)$$

$$g = \left|\frac{V_{dcI}}{V_{dc\_I}}\right| \times k_{II} \qquad (5-6b)$$

Where V_{dcI} are instantaneous DC voltages of MMC I and V_{dc_I} is its rated DC voltage, k_{II} is the magnitude margin (normally set to 0.95).

5.4 **Power reversal of LCC-HVDC**

To provide a convincing LCC-HVDC system and save the description of it, the Cigre Benchmark model [89] is used. Its structure is changed from the asymmetrical monopole to the bipole. The main control of this benchmark model is that the inverter controls the extinction angle to achieve voltage control, and the rectifier controls the DC current. Some auxiliary controls within the inverter to maintain the stable operation will not be described. The power reversal strategy has not been included in this model. A design of power reversal strategy should be proposed firstly.

The DC voltage built by the extinction angle control of the inverter can be described as:

$$V_{dc} = 2 \times (1.35 V_l \cos\gamma - \frac{3}{\pi} X_s I_d) \qquad 5\text{-}1$$

Where V_l is the AC line-to-line voltage, X_s is the equivalent commutation inductance on the AC side, γ is the extinction angle.

It is supposed that C1 stands for the rectifier, and C2 stands for the inverter. For normal operation of the inverter C2, the extinction angle is controlled around 20°. Lead the extinction angle beyond 90°; then the voltage will be reversed. To reduce the possibility of commutation failure occurred at the inverter, the inverter should control the extinction angle. After the power reversal, C1 that operates as the inverter will take the extinction angle control. C2 will be the rectifier to control the current.

The process of power reversal is drawn in Fig. 5-7. A decreasing ramp is set for the reference of DC current and Extinction angle. The DC current and DC voltage will be controlled to decrease to 0 gradually from t1 to t3. During t3-t4, the control mode of the converter will change, C1 will switch to the extinction angle control with the corresponding reference to make the system works at -1 p.u. voltage level. C2 will switch to the current control. After t4, the control system will drive the LCC-HVDC to reach its desired working condition at t5.

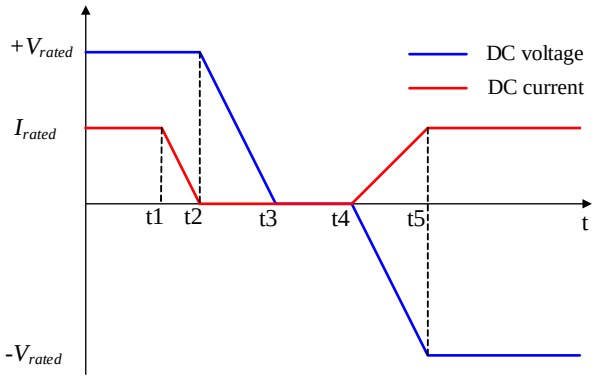


Fig. 5-7 The process of power reversal

5.5 Switch yard operation principle

Except for the power reversal strategy of LCC-HVDC, the performance of the DC/AC/DC converter will be defined during the power reversal. An interconnected LCC-HVDC system is drawn in Fig. 5-1. Suppose LCC-HVDC I need to reverse its power. The DC voltage of MMC is built by the capacitors in SMs. Increasing or decreasing its DC voltage will cause the capacitors being charged or discharged. During power reversal, MMC-I will flow the voltage change, see Fig. 5-7 from t2-t5, which will let the MMC-I be discharged from t2-t3 and be recharged from t4-t5. The recharging process will ask the MMC-I to build the negative DC voltage.

The typical topology of DC/AC/DC converter is shown in Fig. 5-2, both MMC-I and MMC-II will use half-bridge SM. The SM is inserted by turning on S1 and turning off S2. The capacitor can be seen as a V_{SM} voltage source. When SM is inserted, this voltage source is connected to phase unit. The SM, or this voltage source is bypassed by turning off S1 and turning on S2. From the DC side, a constant number of SM is inserted to produce the constant DC voltage. The DC/AC/DC converter cannot connect to the negative voltage because the SM cannot provide the negative SM voltage to produce the desired negative DC voltage.

To cope with the issue of the connection to the negative voltage, it is essential to use additional switches to reverse the DC/AC/DC converter's terminal voltage. As shown in Fig.

5-8, a switch yard is proposed. Busbar A1 and A2 are connected to the positive terminal and the negative terminal of the DC/AC/DC converter. Busbar B1 and B2 are connected to the positive pole and the negative pole of LCC-HVDC. If the voltage polarity of the LCC-HVDC is changed, S1 and S2 are designed to switch the connection from A1-B1 and A2-B2 to A1-B2 and A2-B1. The limiting resistors are applied in switch yard to avoid the large current during the period of discharging and recharging. S3 is used to bypass the limiting resistors. All switches will be a mechanical switch.

The operation principle of the switch yard is shown in Fig. 5-8. For normal operation, S2 is turned off, then current will flow through S1 and S3, as shown in Fig. 5-8 (a). Before the LCC-HVDC reverse its power, the DC/AC/DC converter stops its power regulation, the current pass through S3 is 0. Then S3 is opened. From t2-t3, the discharging current is commutated to limiting resistor branch to avoid the overcurrent, as shown in Fig. 5-8 (b). At t3, the capacitor of each SM is fully discharged. During t3-t4, S1 is opened, S2 is closed to change the polarity of MMC as shown in Fig. 5-8 (c). During t4-t5, the MMC will be charged to rated level, and R_s is still connected to avoid large charging current. After t5, R_s will be bypassed through S3 to avoid high loss, as shown in Fig. 5-8 (d). And the DC/AC/DC converter will start to regulate the power according to the power demand.

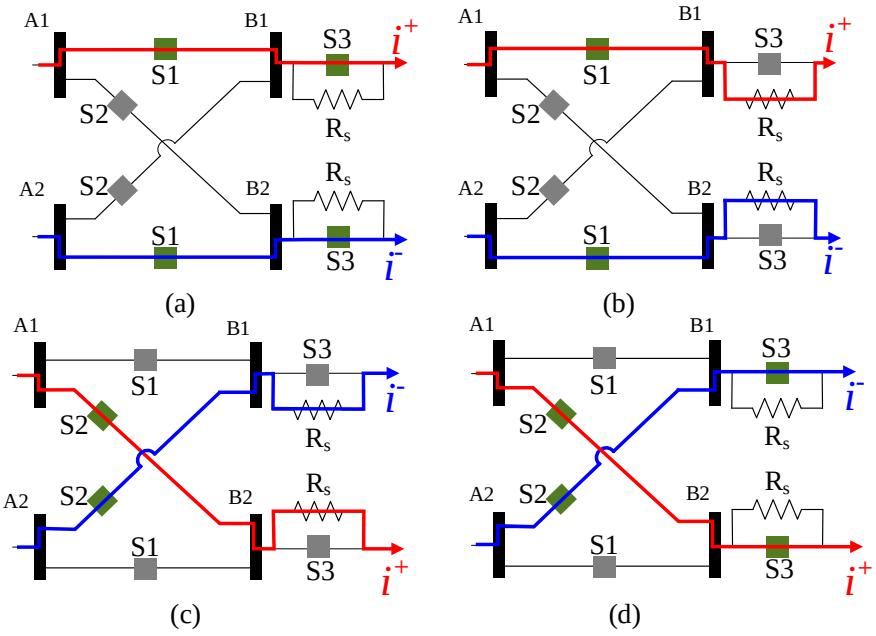


Fig. 5-8 Operation principle of the switch yard

5.6 Simulation verification

An interconnected LCC-HVDC system as shown in Fig. 1 is built in PSCAD/EMTDC; both LCC-HVDCs are modified Cigre benchmark model [89]. Equivalent detailed MMC model [90] is used for the MMC within the DC/AC/DC converter. The data about the interconnected LCC-HVDC system has been summarized in Appendix Table A-3.

5.6.1 Power regulation control verification

Two case studies are used to verify the power regulation control. First one is a step change of the active power transfer between two LCC-HVDCs. The other is to test its ability to maintain the constant power transportation of one LCC-HVDC.

At 0.6s, the rectifier of LCC-HVDC I reduce its power support, and at the same time 400MW power controlled to be transferred from LCC-HVDC II via the DC/AC/DC converter then to LCC-HVDC I. At LCC-HVDC I, After the power reduction of the rectifier, the DC current have not reduced because of the power support from LCC-HVDC II, see Fig. 5-9. At LCC-HVDC II, 0.4 kA DC current of the inverter is reduced because 400 MW power transferred to LCC-HVDC II via the DC/AC/DC converter. and the DC voltages of both LCC-

HVDCs maintain stable all the time. SM voltage ripples of MMC I and MMC II are increased because of the 400 MW power flow in the DC/AC/DC converter.

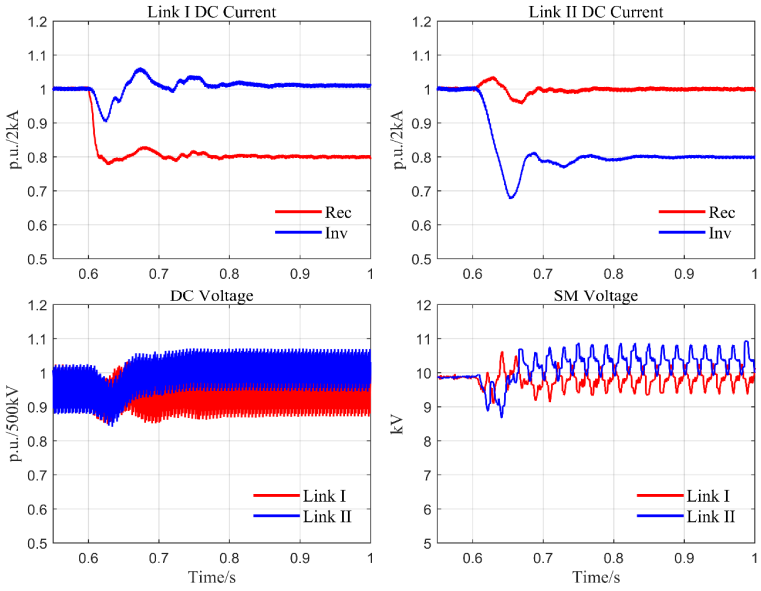


Fig. 5-9 400 MW power transfer from LCC-HVDC II (Link II) to LCC-HVDC I (Link I)

At 1 s, LCC-HVDC I reduces 15 % DC voltage. To main the same power transportation to the inverter of LCC-HVDC I, the additional power is transferred from the LCC-HVDC II to LCC-HVDC I. Therefore, the DC current of the inverter at LCC-HVDC I increased around 15%, see Fig. 5-10.

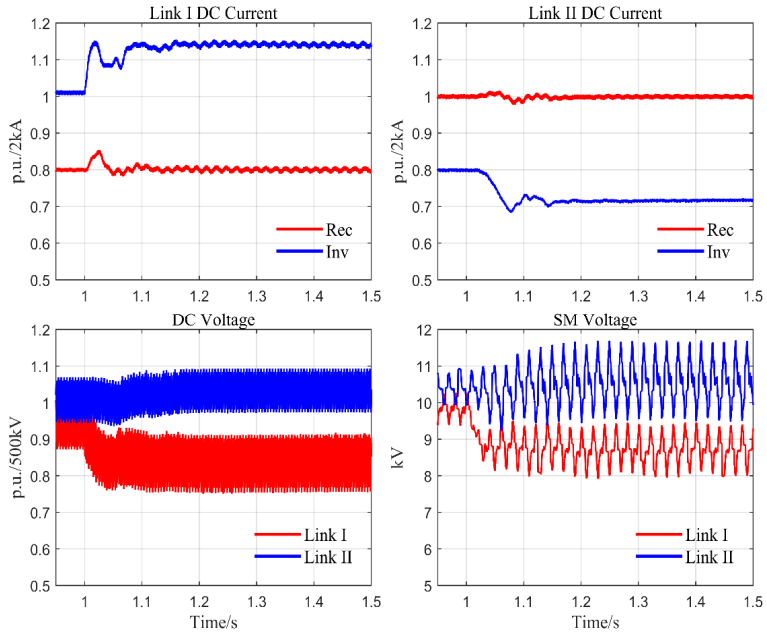


Fig. 5-10 voltage reduction at LCC-HVDC I

5.6.2 Operation of switch yard and isolation control verification

To verify the switch yard design and isolation control system, LCC-HVDC-I will reverse its power according to the steps mentioned previously, as shown in Fig. 1. The operation sequence is shown below:

Before 0.5s, the DC/AC/DC converter stops power transmission and is controlled by the isolation control system; the corresponding limiting resistor is inserted.

0.5s-0.7s, LCC-HVDC-I reduces its DC current to 0 kA

0.7s-1s, LCC-HVDC-I reduces its DC voltage to 0 kA

1s-1.1s, the switch yard changes the voltage polarity of connected MMC-I

1.1s-1.2s, the rectifier and the inverter of LCC-HVDC-I exchange their control system and start them up at 1.2s.

At 1.8s, the LCC-HVDC-I reached to rated value, and get stabled, the process of power reversal is finished.

At 1.9s, starting resistor is bypassed.

At 2s, the LCC-HVDC-I reduces 0.2 p.u. power. To compensate the power reduction, the DC/AC/DC converter transport 0.2 p.u. power from LCC-HVDC-II to LCC-HVDC-I.

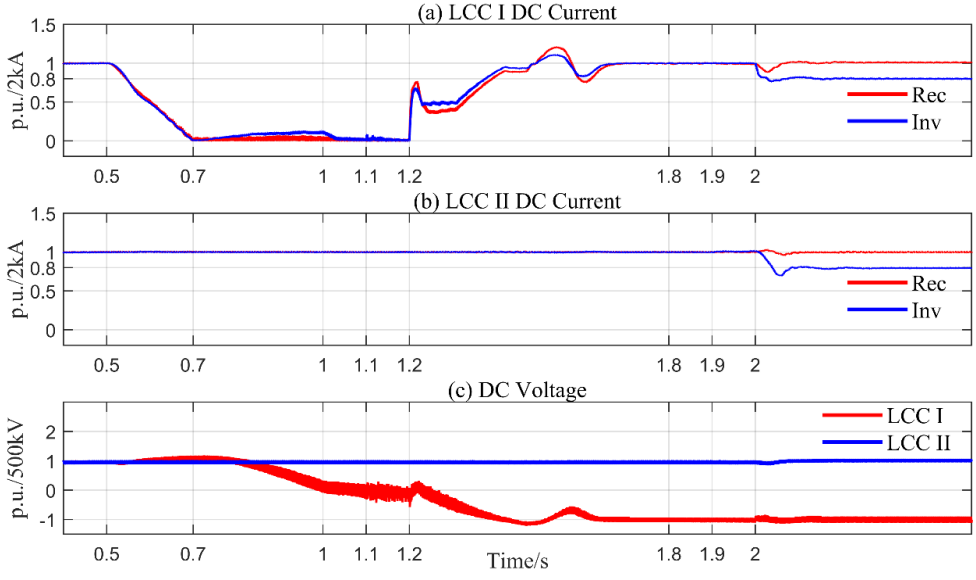


Fig. 5-11: Performance of two LCC-HVDCs

The operation characteristics of both LCC-HVDC are shown in Fig. 5-11. The LCC-HVDC-I follows the power reversal strategy. The whole power reversal process of LCC-HVDC-I lasts from 0.5s to 1.9s，see Fig 5-11 (a) and (c). During the restarting period lasting from 1.2s to 1.8s, the maximum transient DC current is no more than 1.2 p.u. and the transient voltage is no more than 1.1 p.u. . During the power reversal, the voltage and current of LCC-HVDC-II are stable and does not be influenced by the LCC-HVDC-I, see Fig 5-11 (b) and (c). After the power reversal, the inverter of LCC-HVDC-I as the sending end reduces 0.2 p.u. current at 2s, see Fig. 5-11 (a). To compensate the power reduction of LCC-HVDC-I, the DC/AC/DC converter absorb the equivalent power from LCC-HVDC-II, which causes a 0.2 p.u. the current difference between the rectifier at the sending end and the inverter as the receiving end, see Fig. 5-11 (b). Therefore, the rectifier of LCC-HVDC-I is able to maintain the current at 1 p.u., see Fig. 5-11 (a).

The performance of the DC/AC/DC converter during power reversal is shown in Fig. 5-12. During power reversal, SM voltage in MMC-I will follow the voltage change of LCC-HVDC-I. The SMs firstly is discharged due to the reduction of corresponding DC voltage of LCC-HVDC-I from 0.7s to 1s, see Fig. 5-11 (c) and Fig. 5-12 (a). From 1.1s to 1.2s, the switch yard changes the polarity of MCC-I, the SM voltage, therefore, is charged to positive rated value, see Fig. 9 (a). and the SM voltage of MMC-II is always stable. During the whole process, there is no overvoltage occurred over SMs. After 2s, the DC/AC/DC converter transport around 430 MW power from LCC-HVDC-II to LCC-HVDC-I, the arm current increases see Fig. 5-12 (d) and the voltage ripples of SMs are increased, see Fig. 5-12 (a). The generated AC voltage of MMC-II tracks the change of DC voltage of LCC-HVDC-I, and the current control of MMC-I track the AC voltage change of MMC-II to maintain the power transportation is 0, see Fig. 5-11 (c), Fig 5-12. (b) and (c). The arm current is shown in Fig. 5-12 (d), during power reversal, there is no overcurrent occurred.

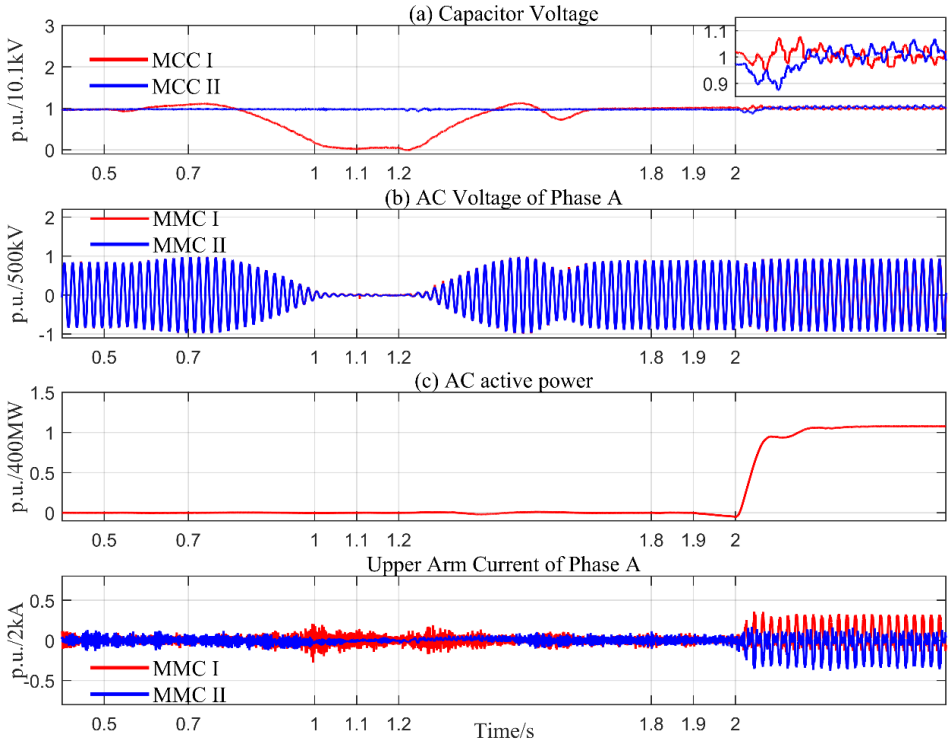


Fig. 5-12: Performance of the DC/AC/DC converter

5.7 **Summary**

An interconnection system is developed using a DC/AC/DC converter based on half-bridge SMs to interconnect two LCC links in PSCAD/EMTDC. The control system of the DC/AC/DC converter is developed and verified. This control system can regulate the power flow between two LCC-HVDC system on requested, and it can be used to maintain the constant power transportation of one LCC-HVDC.

The feasibility of a switch yard design and isolation control for power reversal in the interconnected LCC-HVDC system are verified in PSCAD/EMTDC. During power reversal of the LCC-HVDC, its DC voltage will change the polarity. The switch yard is able to let the DC/AC/DC converter to connect the system with negative voltage level. The isolation control is able to isolate the disturbances of the power reversal and maintain the normal operation of the other LCC-HVDC. This control also ensures that this no overcurrent and overvoltage occurred during power reversal.

CHAPTER 6 INTERCONNECTION OF LCC-HVDCS WITH THE CAPABILITY OF COMMUTATION FAILURE MITIGATION

MMC-based DC/AC/DC converter (MDC) has a bright future as a reasonable interconnection device for LCC-HVDCs due to its high voltage and power ratings. Last chapter studies on the power flow control of the MDC and the strategy to cope with the power reversal of an LCC-HVDC. This chapter continues with the DC/AC/DC converter for the interconnection of two LCC-HVDCs. The contributions from the DC/AC/DC converter to the commutation failure mitigation of the LCC-HVDC will be studied.

For an individual LCC-HVDC, DC current reduction control for commutation failure (CF) mitigation is applied at LCC-HVDC's rectifier. In an interconnected LCC-HVDC system through an MDC, DC CURRENT REDUCTION CONTROL can be placed at the MDC, and a bypassing sub-module (SM) strategy within MDC is proposed to achieve better commutation failure mitigation. DC current reduction control within MDC for CF mitigation will be introduced. Bypassing SM strategy including bypass level prediction and bypass modulation is proposed to enhance the performance of DC current reduction control. The whole system is built and verified in PSCAD/EMTD.

6.1 **Motivation**

The most commissioned HVDC projects are point-to-point LCC-HVDCs due to its high rating and mature technology. The interconnection through a geographical cross point or close point among these existing LCC-HVDCs will improve the efficiency and flexibility of power transmission significantly. As a possible and most economical interconnection option, the transmission line has many limits. It is unable to interconnect the LCC-HVDCs with different voltage levels or different voltage control mode, isolate the disturbance from the other LCC link including faults and polarity reversal, regulate power flow. Therefore, MMC-based DC-DC converter (MDC), which can achieve the objects mentioned above, is considered as a

reasonable device for high-power and high-voltage interconnection between LCC-HVDCs [91].

As an MDC, two MMCs tied in AC side act as a DC-DC converter. It has the freedom to control operation frequency. A higher frequency 350 Hz [92] allows for significant volume saving due to the reduced capacitance in SMs. The research on power regulation and fault isolation strategy has been carried out in [93][94].

In LCC-HVDC, commutation failure (CF) is one of frequent inverter failures because of the employed thyristor valves. The valves need a certain negative voltage-time area to ensure the current commutation from one valve (such as T1) to another valve (T3). Otherwise, the commutation will not be completed; the current still flows through T1, such unwanted phenomenon is named as CF [95]. When the valve in the same phase with T1 is conducted, temporary short circuit appears until the valve sequence follows the required order. CF results in DC current increasing significantly, that shortens valves' lifetime. And it leads to temporary power interruption or even power outage in severe condition.

It is reported that CF may happen during an AC system disturbance on the inverter side, where the voltage reduction is only as small as 10% [102]. Therefore, CF is predicted through AC component detection. Zero-sequence and abc-αβ transformation voltage for single-phase and three-phase disturbances prediction are studied in [96]. And a faster CF prediction system based on AC power component is proposed in [100] to achieve faster activation of CF mitigation control.

When CF is predicted, CF mitigation control is activated to prevent the CF. Although CF mitigation control cannot avoid all CFs, it effectively reduces the risk of inverter suffering CF during AC disturbances.

As the part of CF mitigation control, advancing fire angle control (AFAC) [96][97][98][99] to reduce fire angle properly is widely applied in inverters. However, fire

angle control will cause unwanted DC current increasing, which will reduce the effectiveness of CF mitigation and even lead to CF [100][101]. [101] reveals that DC current reduction will increase CF resistance of inverter. Therefore, DC current reduction control as the other part of CF mitigation control [100][101] is proposed in rectifier to reduce DC current properly when a CF is predicted. In a word, CF mitigation control is achieved by both FAC and DC current reduction control.

CF mitigation in the interconnected LCC-HVDC system through MDC is considered in this paper. DC current reduction control will be applied in MDC rather than rectifier, because

- MMC is endowed with faster current regulation due to independent active and reactive power control ability, compared with LCC current control.
- The number of SMs per arm SMs in MMC is flexible to bypass in order to quickly reduce the corresponding DC voltage, which will avoid the DC current increasing.

A redesigned DC current reduction control fitted with MDC is proposed in this paper. Bypassing SM strategy within DC current reduction control including bypass modulation and bypass level prediction (BLP) proposed to further reduce the DC current quickly. The feasibility of the whole system is validated in PSCAC/EMTDC.

6.2 DC current reduction control of the DC/AC/DC converter

6.2.1 Interconnection LCC-HVDC system

The topology of the interconnected LCC-HVDC system is drawn in Fig. 6-1. Both LCC-HVDCs' inverters own CF mitigation control and CF prediction system (CFP). Only LCC HVDC I's AC side is presented as a demonstration. AFAC and DC current reduction control , which are not drawn in Fig. 6-1, are in the inverter and MDC. The leading angle order $\Delta\alpha_{inv}$ and the current reduction order (ΔI_{CF}), which is predicted by CFP according to AC disturbance level, will be sent to FAC and DC current reduction control. An additional current

(ΔI_{CF}) will be absorbed by MDC from LCC-HVDC I to LCC-HVDC II in order to reduce the DC current in LCC-HVDC I. If ΔI_{CF} is sent from LCC-HVDC II's CFP, MDC will transport the same amount of DC current from LCC-HVDC II to LCC-HVDC I. Taking into account of the stable operation of MDC, its terminal DC voltage V_{dcI} and V_{dcII} are detected. The detail will be studied below. Bypass level (*k*) is calculated in the inverter and sent forward to MDC.

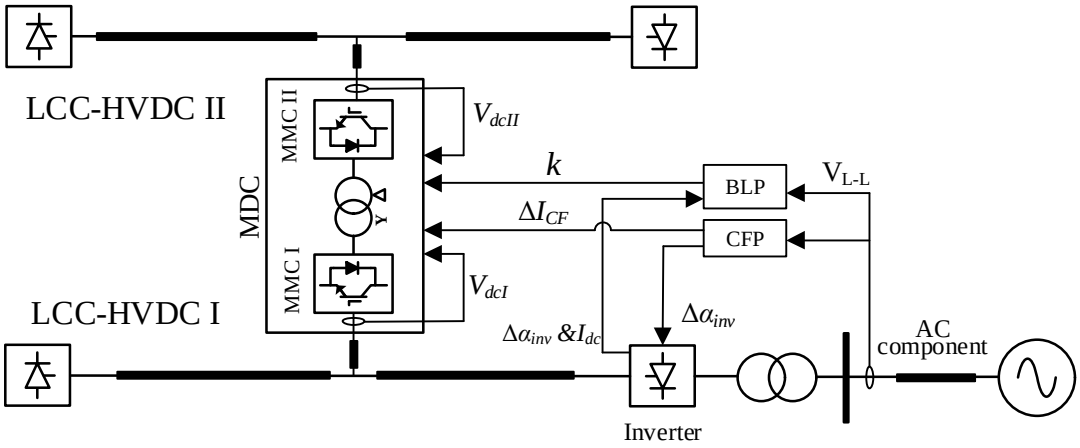
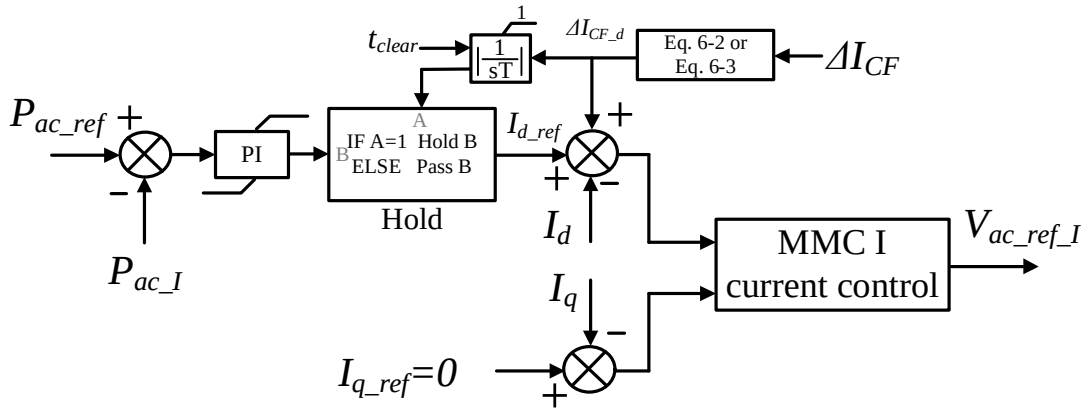


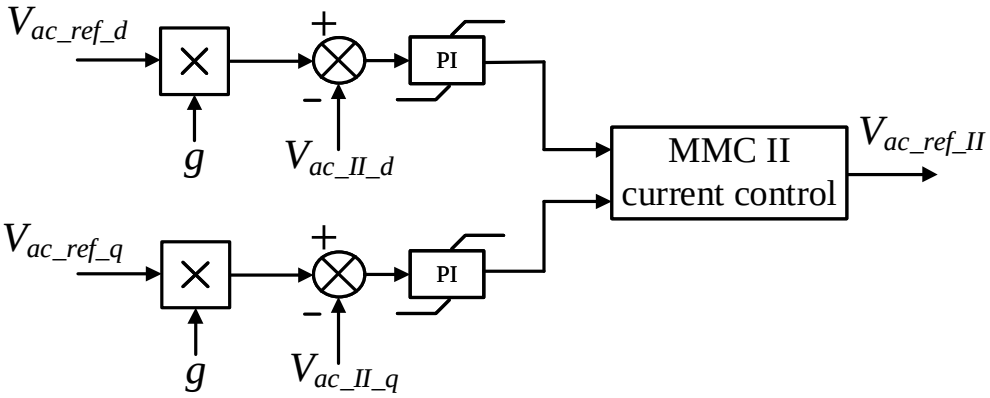
Fig. 6-1 Interconnected LCC-HVDC/MDC system

6.2.2 DC current reduction control

Before introducing DC current reduction control in MDC, it is essential to describe the control of MDC briefly. In the interconnected LCC-HVDC system, MDC acts as a DC power flow controller.



(a) MMC I Active power control



(b) MMC II AC voltage control

Fig. 6-2 MDC control system

The active power within MDC is equal to the DC power flow into/out MDC. To achieve DC power flow control, one MMC is used to control active power, and the other is used to support reasonable AC voltage. The construction of control system of MDC will follow the typical VSC control rules, as drawn in Fig. 6-2.

Under LCC-HVDC I's CF mitigation operation, additional ΔI_{CF} should be absorbed from LCC-HVDC I. To achieve this, ΔI_{CF} should be transferred from DC value to equivalent AC value ΔI_{CF_d}, then added to I_{d_ref}. The expression of power balance between MMC's DC side and AC side can be presented as:

$$2 \times V_{dc\_I} \times \Delta I_{CF} = \frac{3}{2} \times V_{ac\_II\_d} \times g \times r \times \Delta I_{CF\_d} \tag{6-1}$$

Where g is explained in Eq. 6-4, r is the ratio of AC transformer, V_{dc_I} is rated DC voltage of MMC I's DC terminal, $V_{ac\_II\_d}$ is the d-axis value of MMC II' AC voltage.

Therefore, ΔI_{CF_d} can be derived as:

$$\Delta I_{CF\_d} = \frac{4 \times V_{dc\_I} \times \Delta I_{CF}}{3 \times g \times r \times V_{ac\_II\_d}} \tag{6-2}$$

If LCC-HVDC II is under CF mitigation operation, the expression of ΔI_{CF_d} will be trimmed as:

$$\Delta I_{CF\_d} = -\frac{4 \times V_{dc\_II} \times \Delta I_{CF}}{3 \times g \times r \times V_{ac\_II\_d}} \tag{6-3}$$

As shown in Fig. 6-2 (a), under normal operation ΔI_{CF} is 0. Hold box will pass the value from port B; active power control is activated. Under CF mitigation operation, ΔI_{CF} is received from the inverter side, the time constant T is so small that integration module reaches to its limit 1 immediately. Thus the normal current reference from PI is held and a new current reference is generated by adding ΔI_{CF_d}. After the time t_{clear}, CF is prevented, ΔI_{CF} goes back to 0, the output of integration module is reset to 0. After that, active power control is put back into operation.

Maximum AC voltage magnitude of MMC is proportional to its DC voltage. During CF mitigation operation, DC voltage is reduced, the AC voltage should be reduced in order to avoid MDC's control collapse. Therefore, a coefficient g is added into AC voltage control as shown in Fig. 6-2 (b) to reduce AC voltage reference. Under normal operation, g is 1. It can be calculated as:

$$g = \min\left(\frac{V_{dcI}}{V_{dc\_I}}, \frac{V_{dcII}}{V_{dc\_II}}\right) \tag{6-4}$$

Where V_{dcI} and V_{dcII} are instantaneous MDC terminal DC voltages as shown in Fig. 6-1.

6.3 **Bypassing SM strategy**

6.3.1 Bypass level prediction

As shown Fig. 6-3, reducing the firing angle through FAC of LCC inverter will result in sudden voltage droop (reduce to V_{dc}^{1}), and the DC voltage of MDC will maintain at the previous level. A DC current following from MDC to the inverter is produced. To offset such amount of DC current, MDC will bypass equivalent SMs to reduce its DC voltage.

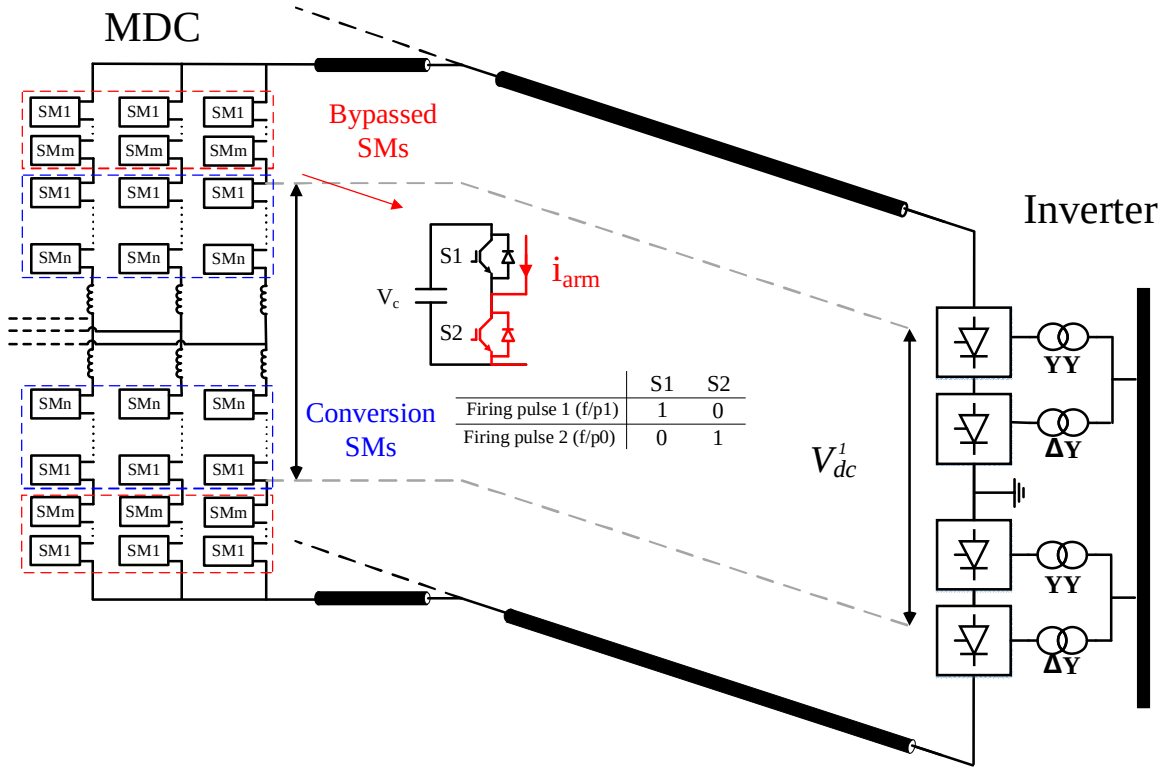


Fig. 6-3 Bypassing SM strategy demonstration

Bypass level is defined as the ratio of bypassed SMs, denoted as k ($0 \le k \le 1$):

$$k = \frac{m}{N} = \frac{N-n}{N} = \frac{V_{dc} - V_{dc}^1}{V_{dc}} \tag{6-5}$$

Where N is the total number of SMs per arm, m is the number of bypassed SMs, n is the number of conversion SMs in normal operation, V_{dc} is the rated voltage.

According to Eq. 6-5 once V_{dc}^1 is carried out; bypass level is defined. V_{dc}^1 is the DC voltage that before CF, thus it is able to be estimated through the static equation of LCC-HVDC. The DC voltage and DC current of the inverter can be expressed as [103]:

$$V_{dc} = \frac{3\sqrt{2}V_{l-l} \times (-\cos\alpha + \cos\gamma)}{2\pi} \tag{6-6}$$

$$I_d = \frac{2X_t}{\sqrt{2}V_{l\_l}} \times (\cos\gamma - \cos(\pi - \alpha)) \tag{6-7}$$

V_{l-l} is the line-to-line r.m.s. value of AC voltage, X_t is commutation reactance, γ is extinction angle, α fire angle.

Extinction angle can be derived from Eq. 6-7,

$$\gamma = \arccos(\frac{2X_t I_d}{\sqrt{2}V_{l\_l}} + \cos(\pi - \alpha)) \tag{6-8}$$

After FAC, fire angle is reduced by $\Delta\alpha_{inv}$. Substituting for the extinction angle in Eq. 6-6, reduced DC voltage can be obtained:

$$V_{dc}^1 = \frac{3\sqrt{2}V_{l-l}(-\cos(\alpha - \Delta\alpha_{inv})}{2\pi} + \frac{\frac{2X_t I_d}{\sqrt{2}V_{l\_l}} + \cos(\pi - (\alpha - \Delta\alpha_{inv}))}{2\pi} \tag{6-9}$$

For BLP, when an AC disturbance is detected, V_{l-l}, α and $\Delta\alpha_{inv}$ are sampled from the AC side, inverter and CFP individually as shown in Fig. 6-1, in order to obtain a precise bypass level.

6.3.2 Bypass modulation

SMs of one arm are categorised into two groups: bypassed SMs (the number of bypassed SMs is m) and conversion SMs (the number of Effective SMs is n). The operation of bypassed SMs is f/p0, as shown in Fig. 6-3. Conversion SMs operate at both f/p1 and f/p0 depending on its arm reference to achieve AC/DC conversion.

Bypass modulation is the modified nearest level modulation. Reference voltages of the upper arm and lower arm are determined by:

$$\begin{cases} v_{u\_ref} = \frac{V_{dc}}{2}(1 - v_{ac\_ref}) \\ v_{l\_ref} = \frac{V_{dc}}{2}(1 + v_{ac\_ref}) \end{cases} \tag{6-10}$$

Where v_{ac_ref} comes from MMC control as shown in Fig. 6-2.

After a sudden voltage droop, DC voltage decreases to V_{dc}^{1}. An equivalent number of SMs is bypassed to avoid DC current increasing at the same time, and the voltage of each SM will not change. The reference voltages of the upper arm and lower arm can be rewritten as:

$$\begin{cases} v_{u\_ref} = \dfrac{V_{dc}^{1}}{2}(1 - v_{ac\_ref}) \\ v_{l\_ref} = \dfrac{V_{dc}^{1}}{2}(1 + v_{ac\_ref}) \end{cases} \tag{6-11}$$

Substituting for the DC voltage in Eq. 11 from Eq. 5,

$$\begin{cases} v_{u\_ref} = \dfrac{V_{dc}(1-k)}{2}(1 - v_{ac\_ref}) \\ v_{l\_ref} = \dfrac{V_{dc}(1-k)}{2}(1 + v_{ac\_ref}) \end{cases} \tag{6-12}$$

The reference is modulated into small steps, then the expression of bypass modulation can be obtained:

$$\begin{cases} v_{u\_step} = round(\dfrac{V_{dc}(1-k)}{2}(1 - v_{ac\_ref})/V_c) \\ v_{l\_step} = round(\dfrac{V_{dc}(1-k)}{2}(1 + v_{ac\_ref})/V_c) \end{cases} \tag{6-13}$$

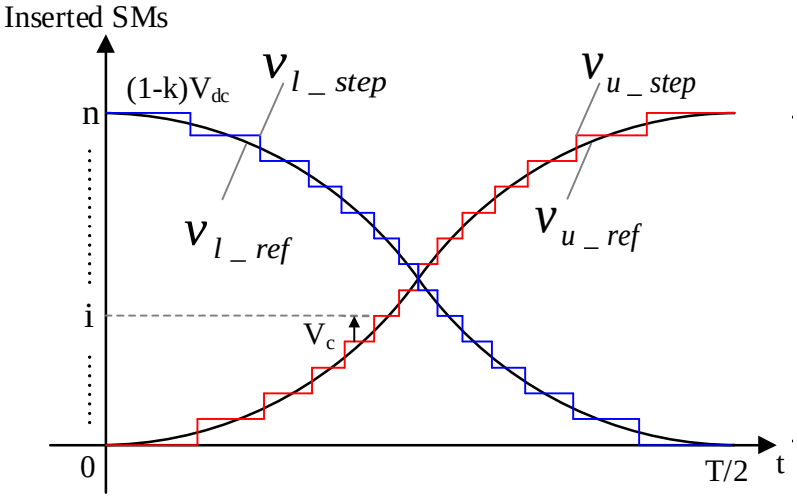
When k=0, the system is the typical NLM. V_c is the voltage of each SM.

The principle of bypass modulation and its control diagram are presented in Fig. 6-4 based on Eq. 6-13. As illustrated in Fig. 6-4 (a), the magnitude of arm reference can be adjusted by k, which determines the total number of conversion SMs in terms of constant SM voltage. Inserted SMs stand for the conversion SMs operating at f/p1, and non-inserted SMs operate at f/p0. The sequence of inserted SMs i ($0 \le i \le n$) is determined by the stepped arm references which are shown as a blue and red line in Fig 6-4 (a). V^{ref} is V_{u_ref} or V_{l_ref}, same to V^{step} as shown in Fig. 6-4 (b). V^{step} only determines the number of inserted SMs.

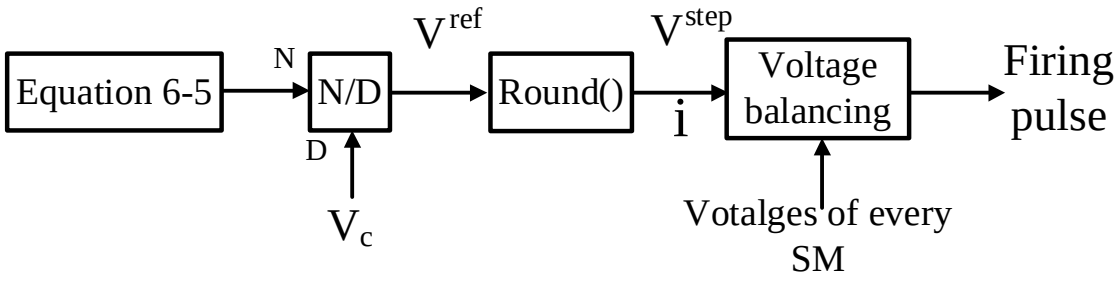
To maintain the same voltage of each SM, SMs have to be divided into Conversion SMs (inserted SMs and non-inserted SMs) and bypassed SMs by voltage balancing control

according to the direction of arm current, the voltages of SMs as shown in Fig. 6-5. Because non-inserted SMs and bypassed SMs share the same operation that is f/p0, voltage balancing control is able only to identify which part of SMs operating at f/p1 should be inserted; the rest will operate at f/p0.

As illustrated in Fig. 6-5, the total number N of SMs are sorted in ascending order. After this, there are two conditions: arm current (i_{arm} as shown in Fig. 6-1) is more than or equal to 0; i_{arm} is less than 0. For the first condition, SMs will be charged. Therefore, first i SMs whose capacitor voltages are minimum should be identified as the inserted to increase their voltage. For the second condition, SMs will be discharged, last i SMs whose capacitor voltages are maximum should be identified as the inserted to reduce their capacitor voltage.



(a) Principle of bypass modulation



(b) Control diagram

Fig. 6-4 Bypass modulation based on nearest level modulation method

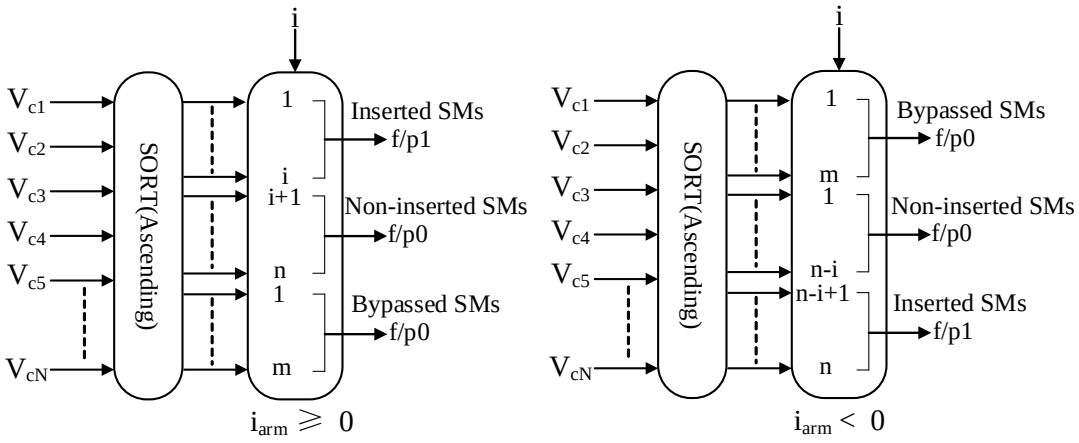


Fig. 6-5 Voltage balancing control for bypass modulation

6.4 **Simulation verification**

To verify the feasibility of DC current reduction control and bypassing SM strategy, an interconnected LCC-HVDC system is built in PSCAD/EMTDC. Cigre Benchmark [104] is modified from the asymmetrical to the bipolar as the LCC-HVDC system. MDC is built by equivalent detailed MMC model [105]. The data of the interconnected LCC-HVDC system is shown in Appendix Table A-4.

The AC disturbance is modelled as the inductive AC fault placing on the AC bus bar, as shown in Fig. 6-1. Both Single-phase fault and three-phase fault are taken into account. The ability of CF mitigation is identified through changing the inductance of AC fault. CFII index is selected to evaluate this ability, and it is defined as [106]:

$$CFII = \frac{Critical \quad fault \quad level}{Rated \quad DC \quad power} = \left(\frac{v_{l\_l}^2}{Z_{fault} \times P_{dc}} \right) \times 100 \tag{6-14}$$

Where p_{dc} is the rated DC power, Z_{fault} is the minimum fault impedance that inverter will avoid CFs.

When an AC fault is detected, the output of CFP is supposed to be constant and presented in Appendix Table A-4. Its detection time is supposed to be 2 ms. Taking into account of the communication [100], there is another 2 ms delay before MDC receive the orders. For example,

if the fault occurs at 1 s, the inverter begins to reduce its fire angle by 0.2 rad at 1.002 s, MDC begins to reduce the DC current by 0.2 kA at 1.004 s.

To evaluate the effect of CF mitigation, DC current reduction control within rectifier is chosen in comparison with redesigned DC current reduction control and bypassing SM strategy in MDC:

S1: AFAC with DC current reduction control in rectifier

S2: AFAC with DC current reduction control in MDC

S3: AFAC with both DC current reduction control and bypassing SM strategy in MDC

The primary operation of MDC before AC fault will not influence the result of the comparison. Therefore, MDC is made to work with zero power transportation (its active power control reference is set to 0) until an order ΔI_{CF} is received. For S1, MDC always works with primary condition. Two LCC-HVDC operates at their rated level. The fault is applied at different time instants between 1.000 s to 1.010 s with a 0.001 s step to test the fault time dependency of CF sensitivity.

A 0.14 H A-phase-to-ground fault occurs at 1.008s, the DC currents under different current reduction strategies flowing into LCC-HVDC I's inverter are shown in Fig. 6-6. current reduction strategies begin to work at 1.012s, and CF occurs under S1 and S2 control strategy. S3 does not suffer CF. comparing the DC currents of S1 and S2, DC current reduction control in MDC performs better in DC current reduction. Bypassing SM strategy enhances the DC current reduction ability through MDC, and reduces the risk of CF. A comprehensive comparison of CF mitigation ability is presented in Fig. 6-7 with A-phase-to-ground fault.

Higher CFII means the better effect of CF mitigation. As shown Fig. 6-7, the performance of CFII analysis in the time interval (1 s, 1.002 s) & (1.005 s, 1.01 s) supports the previous conclusion. S3 strategy has the best ability of CF mitigation. When the valve connected to the faulted phase is almost or already in the commutation process, there is no time left for the

current reduction strategy. Therefore, in the time interval (1.002 s, 1.005 s) neither of current reduction strategies works and their CFII performances are same.

The three-phase fault causes each AC phase voltage drop symmetrically, which will make the CF happen more quickly. And there is 4 ms for the detection and communication in total after AC three fault occurs. Thus before DC current reduction control contributes to CF mitigation, CF has occurred or almost occurs. That is the reason why their CFII values are same to AFAC's, as shown in Fig. 6-8,

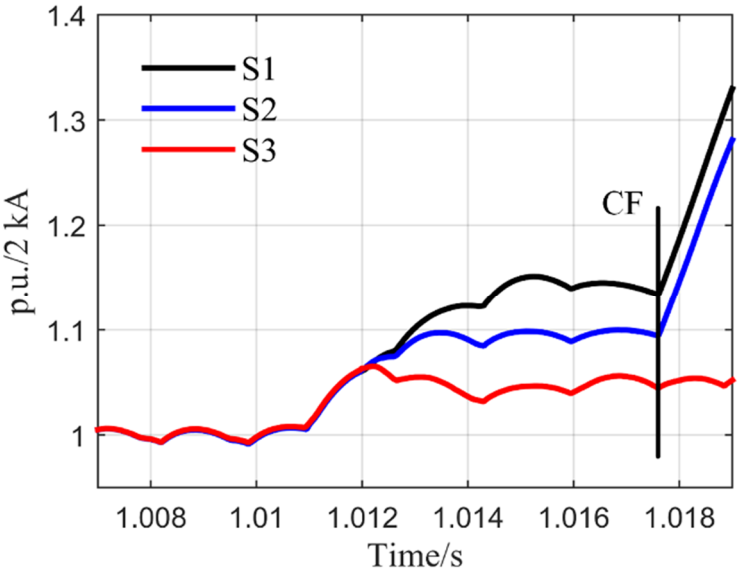


Fig. 6-6 Inverter's DC current under single-phase fault

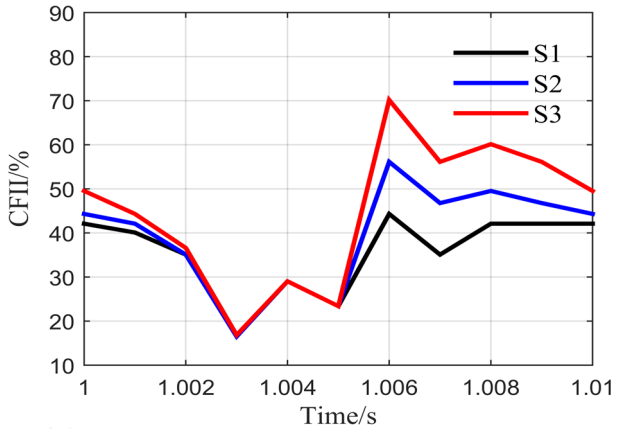


Fig. 6-7 Comparison of CFII among different control strategies under single-phase fault

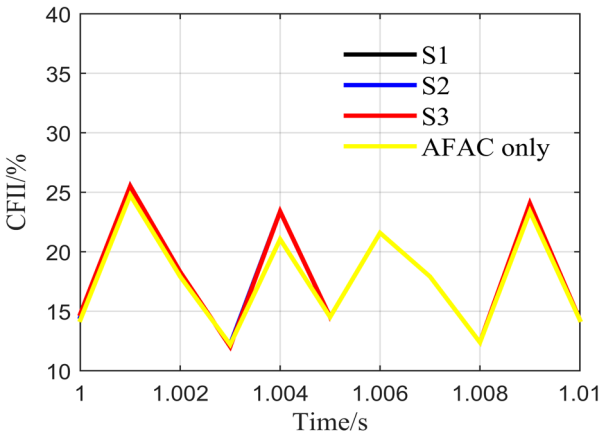


Fig. 6-8 Comparison of CFII among different control strategies under three-phase fault

6.5 **Summary**

In terms of the interconnected LCC-HVDC system, a redesigned DC current reduction control is introduced within CF mitigation control. To further enhance DC current reduction control's performance of CF mitigation, a bypassing strategy is proposed, and its mechanism is fully described. The whole system is verified in PCCAD/MTDC. Three situations (S1, S2, S3) are proposed to compare in order to find the best DC current reduction control solution. 4 ms is proposed for CF detection and communication. As S3, the redesigned DC current reduction control in the MDC combining with the bypassing strategy shows the highest CF immunity within CF mitigation control with the single-phase fault. Taking into account the time of detection and communication, the DC current reduction control cannot contribute to the CFs caused by three-phase faults, because CF occurs before DC current reduction control begins to work.

CHAPTER 7 CONCLUSIONS AND FUTURE WORKS

Two research questions have been answered in this thesis; one is how to reduce the capital cost of hybrid HVDC circuit breakers. The other is how to achieve the interconnection of LCC-HVDCs.

7.1 **Cost reduction of hybrid HVDC circuit breaker**

A Hybrid HVDC circuit breaker is widely accepted in industries as a fast and low-loss solution of the fault isolation. However, its capital cost is extremely high. two feasible solutions are provided in this thesis in order to reduce the cost. One is to reduce the number of applied components by optimising its structure, see Chapter 3. The other is to reduce its current rating by reducing the fault current via the operation of the converter, see Chapter 4.

7.1.1 Interlink hybrid HVDC circuit breaker

Novel interlink hybrid HVDC circuit breakers for unidirectional and bidirectional interruption are proposed with the aim of reduced sizes and costs of the DC circuit breakers. Comparing to the unidirectional and directional hybrid HVDC circuit breakers, the number of MOVs of the main breaker branch of the unidirectional interlink hybrid HVDC circuit is reduced by 50% and the numbers of IGBT modules and MOVs of the bidirectional interlink hybrid HVDC circuit breaker are reduced by 25%.

The design of the unidirectional interlink hybrid HVDC circuit breaker is based on sharing one main breaker branch. For a bidirectional interlink hybrid HVDC circuit breaker, a novel Y-connected main breaker branch is proposed for the bidirectional fault current interruption.

The interlink hybrid HVDC circuit breakers are tested in a three-terminal MMC-HVDC system in PSCAD/EMTDC. The fault current interruption performance of the unidirectional and bidirectional interlink hybrid HVDC circuit breakers are the same as that of the unidirectional and bidirectional hybrid HVDC circuit breaker at the same interruption speed.

7.1.2 Coordination of MMC Converters and Hybrid HVDC Circuit Breakers for HVDC Grid Protection

The coordination strategy of MMC converters and hybrid HVDC circuit breakers are proposed to reduce the current rating of a hybrid HVDC circuit breaker significantly. A novel bypass operation of an MMC is proposed to avoid the fault coming from the MMC. A method for using the hybrid HVDC circuit breakers to detect, discriminate and isolate DC faults has also been included for completeness. Moreover, the coordination sequence for DC-CBs and MMCs has been established.

The bypass operation of the MMC has been demonstrated, and the results show that during the bypass period, all arm currents stay in the safe range. The coordination strategy has been tested in a four-terminal MMC HVDC system in PSCAD/EMTDC. And the results show that the bypassing of MMCs significantly reduces the interrupted current and the absorbed energy.

7.2 Interconnection of LCC-HVDCs

Most of the commissioned HVDC projects are LCC-HVDC point-to-point links. There is potential demand for the interconnection of LCC-HVDCs in order to achieve grid operation. The MMC-based DC/AC/DC converter is suitable for the bulk-power and high-voltage interconnection among HVDC systems. For an LCC-HVDC, the characteristic of power reversal and the commutation failure bring big challenges for the interconnection via a DC/AC/DC converter. An isolation control and a switchyard design are provided for the DC/AC/DC converter to work under the condition of power reversal of one LCC-HVDC, see Chapter 5. A commutation failure mitigation control is proposed for the DC/AC/DC converter to help to avoid the commutation failures of LCC-HVDCs, see Chapter 6.

7.2.1 Interconnection of LCC-HVDCs with the capability of power reversal

The power regulation control is proposed for a DC/AC/DC converter to transfer the power between two LCC-HVDCs flexibly and smoothly. An interconnected system including one

DC/AC/DC converter and two LCC-HVDC are built in PSACAD/EMTDC. In the interconnected system, the power regulation control can achieve a power step change smoothly. Under the different voltage levels of two LCC-HVDCs, this control can still achieve the flexible power transfer.

A low-cost mechanical switch yard is verified in the interconnected system to make the DC/AC/DC converter connect to the LCC-HVDC under the condition of power reversal. A corresponding isolation control is verified during the power reversal of one LCC-HVDC. The disturbances of the power reversal on the other LCC-HVDC is totally avoided via this isolation control.

7.2.2 Interconnection of LCC-HVDCs with the capability of commutation failure mitigation

In an interconnected LCC-HVDC system, a commutation failure mitigation control is proposed in the DC/AC/DC converter to help to avoid the commutation failure of the LCC-HVDC. This commutation failure mitigation control including a prediction system, a DC current reduction control and a bypass modulation. An interconnected system including one DC/AC/DC converter and two LCC-HVDC are built in PSACAD/EMTDC in order to test the control system. The results show the better commutation failure mitigation than that of the conventional commutation failure mitigation control under various commutation failure conditions.

7.3 Future works

An efficient protection for an HVDC grid is mainly considered using breakers such as hybrid HVDC circuit breakers. For a protection of an interconnected HVDC grid, the interconnection device can be considered to replace some breakers to achieve the fast DC fault interruption, which will reduce the total cost of breakers used in the grid. The interconnection device normally uses semiconductor switches to achieve the DC/DC interconnection.

Therefore, it is potential to be used to interrupt a DC fault as the operation of semiconductor switches are fast enough to fulfil the speed requirement of an HVDC grid protection. For the future works, the cooperation of the interconnection device and hybrid HVDC circuit breakers will be studied and objectives are given below:

- Explore the capability of the fault interruption for an interconnection device
- Propose a control system for the interconnection device to interrupt the fault
- Propose an isolation control system for the interconnection device to protect the other interconnected health HVDC grid from the influence of a fault
- Evaluate the capital cost reduction of hybrid HVDC circuit breakers due to the use of the interconnection device
- Propose the coordination protection of the interconnection device and hybrid HVDC circuit breakers

APPENDIX

Table A-1 Main data of test system for interliked hybrid DC circuit breaker

Items	Value
One π-section (20 km) of overhead line	0.228 Ω, 18.7 mH, 0.246 μF
Length of Line 12 and Line 13	100 km
Voltage control in MMC1	320 kV
Power control in MMC 2-3	900 MW
Arm inductor	50 mH
SM capacitor	8 mF
Number of SMs	100
IGBT	RCE0=0.49 mΩ VCE0=1.22 V
Diode	Ron=0.39 mΩ FVD=1.09 V
CLR	100 mL
Main breaker cells	120 kV
Fault impedance	100 mΩ

Table A-2 Dinghai MMC data

Component	Item	Value
MMC	Power rating	400 MW
	Voltage rating	± 200 kV
	SMs	250 (10 in simulation)
	SM capacitance	12 mF
	Switch-on resistance (assumption)	0.01 Ω
	Arm inductor	90 mH
	Maximum IGBT peak current	3 kA
	Diode and thyristor peak current	3 kA
	DC inductor	20 mH
AC transformer	Ratio (Line-to-line voltage)	230 kV / 205.13kV,
	Rating power	450 MW
	Short impedance	15%
	Withstanding 2s symmetrical short current	20 kA
AC system	AC grid (line-to-line voltage)	220 kV
	SCR (assumption)	3

Table A-3 Datasheet about the interconnected system

Items	Value
Rated power of LCC-HVDC	2000 MVA
Rated voltage of LCC-HVDC	±500 kV
SM number per arm	99
Arm inductor	10 mH
SM capacitor	0.5 mF
Rated SM voltage	10.1 kV
Limiting resistor R_s	200 Ω

Table -A-4 Main parameters of the interconnected LCC-HVDC system

LCC-HVDC I	
Rated power	2000 MVA
Rated DC voltage	±500 kV
LCC-HVDC II	
Rated power	1800 MVA
Rated DC voltage	±500 kV
MMC-based DC/AC/DC converter	
Rated voltage	±500 kV
SM number per arm	100
SM Capacitor	0.1 mF
Arm inductor	10 mH
AC transformer ratio	500kV/480kV
Orders of commutation failure mitigation control	
ΔI_{CF}	0.2 kA
$\Delta \alpha_{inv}$	0.2 rad

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