Research article

Thirteen-level inverter for photovoltaic applications

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Abstract: With the recent cost reduction and efficiency improvement of solar photovoltaic (PV) cells, there is a growing interest towards PV systems in different applications. One promising application is solar PV powered electric vehicles. When they are moving on roads, the whole or some parts of the PV system might be shaded by trees, high buildings, etc.; which result in non-uniform insolation conditions. As a remedial measure, this paper presents a development of a cascaded multi-level inverter based PV system for electric vehicle applications. The basic architecture and switching of the converter switches are described. A laboratory prototype of the proposed architecture was implemented using MOSFETs and harmonic performance under different shading conditions was evaluated. It was found, that under shaded conditions, the 3rd harmonic content can increase and that it depends on the number of modules shaded and the loading condition. The shading performance, losses and power utilization of the cascaded multi-level inverter are compared with that of a conventional Pulse Width Modulated (PWM) inverter architecture. The proposed inverter shows better immunity for shading than a PWM inverter. Furthermore, it was found that the switching losses of the proposed inverter are one 10th to one 20th of that of a PWM inverter. Additionally, by properly selecting the switches, it is also possible to reduce the conduction losses compared to that of a PWM inverter. Even though the power utilization is compromised at full insolation, the power utilization performance of the proposed inverter is superior under shading conditions, thus ideally suited for the selected application. As the modular nature of the proposed inverter allows cascading of more H-bridges with fewer cells, the harmonic, shading, loss and power utilization performance of the proposed inverter can be enhanced with more number of steps in the output waveform.

Keywords: solar power; shading; multilevel inverter

1. Introduction

Increasing efficiencies of different cell technologies and decreasing cost of installations attracted photovoltaic (PV) systems for many applications [1]. For example, they became a mainstream power generation source bringing the total world capacity to 178 GW by 2014 [2]. Another area where PV applications are increasing is the electric car industry. In 2014, Ford has announced there concept car which has rooftop PV panels with special concentrators to charge the battery. The company said that the PV panels could provide power equal to a four-hour battery charge. Eindhoven University of Technology in Holland also announced their lightweight, wedge-shaped electric car that charges itself with PV cells. Rooftop PV panels on a car reduce the transfer of heat into the cabin by solar radiation in hot climates; thus reducing the heating of air temperature inside the car. This reduces the workload of the air conditioner, resulting in reduced fuel consumption (in a hybrid). Even though these cars provide a number of benefits, the efficiency of roof top PV panels will reduce with shading: as the shading is a dynamic process, an effective way of overcoming effects of shading is quite important.

Commonly used motors for hybrid and fully-electric vehicles are dc brushless and induction motors. They use motors having similar stators and are connected to the dc bus of the car through an inverter, usually operating on Pulse Width Modulation (PWM). This inverter requires a high voltage capacitor at the dc link and bulky filtering arrangements to eliminate unwanted harmonics. In order to overcome the limitations of PWM inverters and to facilitate PV connection, Imtiaz et. al (2013) proposed a cell-level power conversion topology based on a cascaded multi-level inverter [3]. In this inverter, a number of PV cells are connected together through H-bridge inverters. The outputs of each of different level H-bridge inverters are connected in series such that the synthesised waveform is almost a sinusoidal. Therefore the output has less harmonic distortion and switching losses are less compared to other inverter topologies [4].

A number of papers discuss different topologies, performance and control strategies for cascaded multi-level inverters [5–8]. Khajehoddin et. al in [9] presents a control strategy to control cascaded multi-level converters in a multi-string configuration for single-phase grid connected systems. The performance of symmetrical and asymmetrical single-phase cascaded multi-level inverters with respect to harmonics content, number of switches and voltage stress across the switch with photovoltaic cell as its input source is simulated in [10]. A 9-level cascaded multi-level inverter with solar energy using PWM technique that provides a high switching frequency is presented in [11]. Even though these papers discuss the performance and control of cascaded multi-level inverters, no paper discusses their shading performance.

In this paper, a cascaded multi-level inverter based PV system is presented and its shading performance is evaluated. In a PWM inverter based system, as a large number of cells are connected in series, shading a single cell causes the current in the string of cells to fall to the level of the shaded cell; thus reducing the generated PV power output [12]. In this proposed system, as each PV module (having lesser number of cells in series) generates a single voltage level in a step-wise output waveform, shading effects under partial shading conditions are expected to be much benign. Furthermore, as each string of cells is individually connected to an isolated H-bridge module, under fully shaded conditions the H-bridge can be controlled to by-pass the shaded module. The proposed system is simulated and a hardware prototype is implemented to validate the proposed system. Results are presented comparing the shading performance of the proposed system and a conventional PWM inverter system.

2. Materials and Method

Figure 1 shows the 13-level cascaded multi-level inverter based PV system used for this study. Each phase of the three-phase 13-level inverter consists of six H-bridge units connected in series.
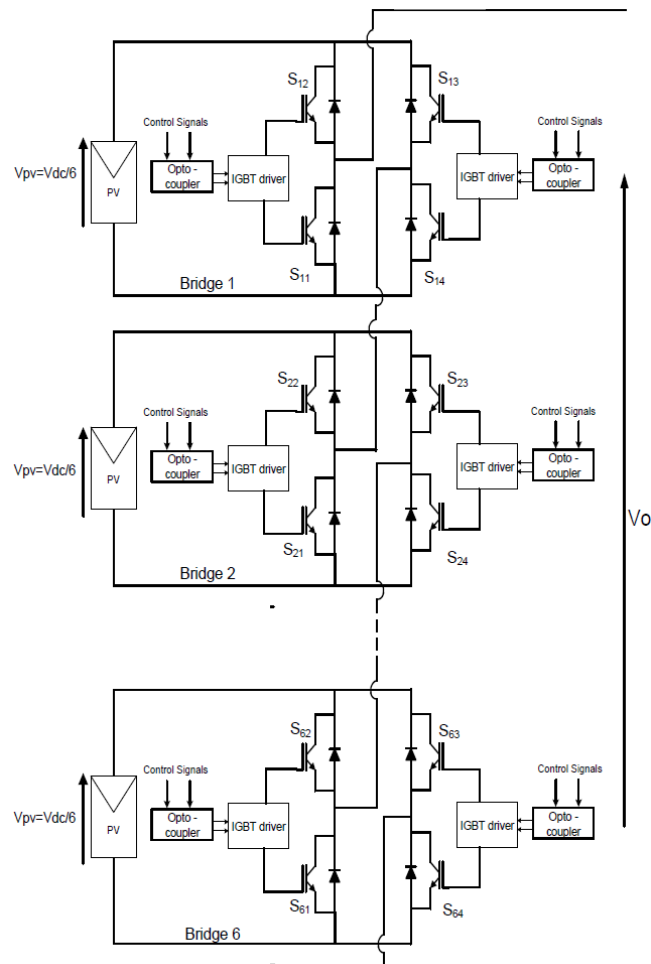
Figure 1. A single phase of the 13-level inverter.

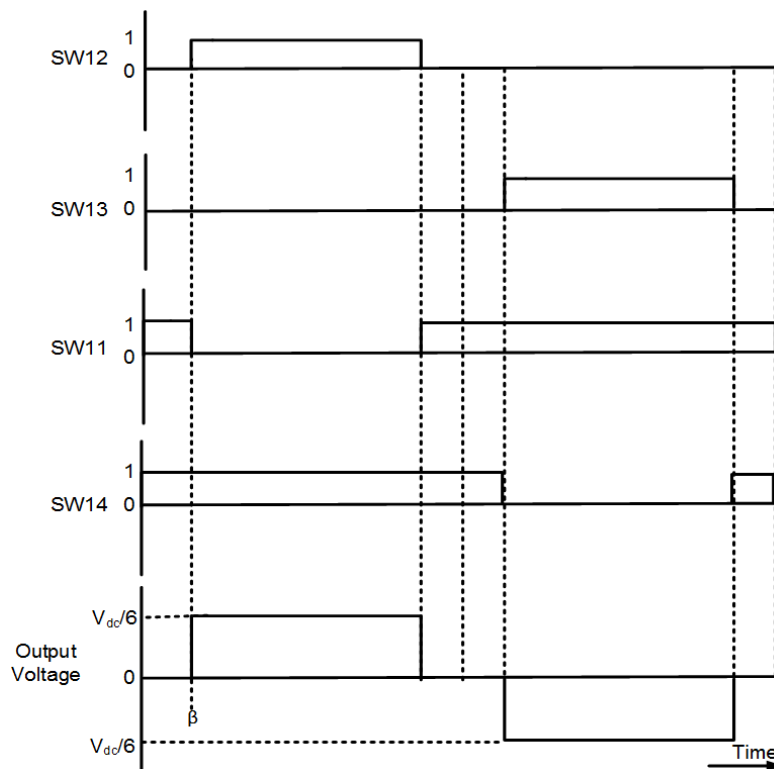### 2.1. The operation of the 13-level inverter

The principle of operation of the 13-level inverter is to synthesize the output voltage of each module to form a step-like ac voltage waveform across the output terminal. The ac voltage is produced by adding the output voltage of each module with different duty cycles. In general, with higher number of H-bridge modules in a single-phase structure, there will be more levels in the ac output voltage; thus producing an ac waveform closer to a sinusoidal wave. The number (M) of ac output voltage levels is given by $M = 2N + 1$, where N is the number of PV cells/modules. Then the output voltage, V_O, of a single phase is given by,

$$V_O = V_{O1} + V_{O2} + ... + V_{O(N-1)} + V_{ON} \qquad (1)$$

2.2. Switching pattern generator

In an H-bridge there are two modes of operations depending on the pattern of the switching signals. This is explained using semiconductor switching devices S_{11}, S_{12}, S_{13}, and S_{14} of the top most H-bridge in Figure 1.

In the first mode, S_{12} and S_{14} are turned on to produce an output of $+V_{dc}/6$ and S_{11} and S_{13} are turned on to generate an output of $-V_{dc}/6$. The second mode gives an additional voltage level of 0 V: this occurs when the switch pairs S_{12} and S_{13}, or S_{11} and S_{14}, are turned on. The fundamental operation principle of the cascaded H-bridge multilevel inverter relies on the second mode of operation. In this mode, four switches in the H-bridge module is switched in four different sequences to generate a 3-level output voltage across output terminal of each H-bridge module as shown in Figure 2.

Figure 2. Switching devices gate signal and 3-level output voltage waveform.

2.2.1. Switching pattern of the 13-level inverter

The output of the 13-level inverter is shown in Figure 3. This allows V_O to vary between $+V_{dc}$ and $-V_{dc}$ in thirteen steps. This stair-case shape is obtained by switching individual bridges at different times corresponding to angles $\beta1$, $\beta2$, ..., and $\beta6$. Switching patterns are given in Table 1 and Table 2 for the positive half cycle and the negative half cycle respectively.
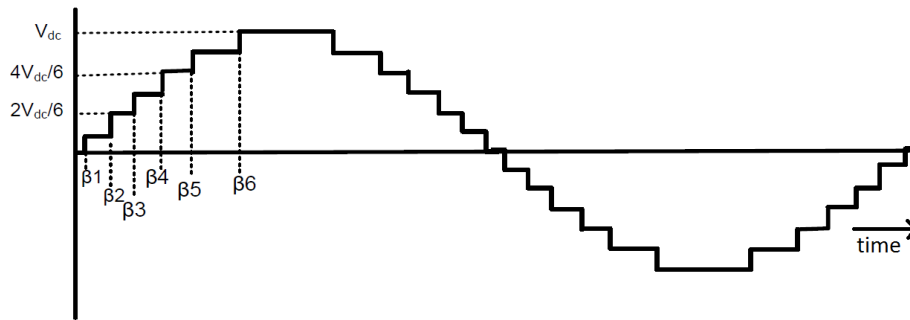
Figure 3. 13-level H-Bridge output voltage.

Table 1. Switching states for the 13-level inverter to produce positive voltages.

Inverter output voltage (V)	S_{11} to S_{61}	S_{12}	S_{22}	S_{32}	S_{42}	S_{52}	S_{62}	S_{13} to S_{63}	S_{14} to S_{64}
$V_{dc}/6$	0	1	0	0	0	0	0	0	1
$2V_{dc}/6$	0	1	1	0	0	0	0	0	1
$3V_{dc}/6$	0	1	1	1	0	0	0	0	1
$4V_{dc}/6$	0	1	1	1	1	0	0	0	1
$5V_{dc}/6$	0	1	1	1	1	1	0	0	1
$6V_{dc}/6$	0	1	1	1	1	1	1	0	1

Table 2. Switching states for the 13-level inverter to produce negative voltages.

Inverter output voltage (V)	S_{11}	S_{21}	S_{31}	S_{41}	S_{51}	S_{61}	S_{12} to S_{63}	S_{13} to S_{63}	S_{14} to S_{64}
0	0	0	0	0	0	0	0	1	0
$-V_{dc}/6$	1	0	0	0	0	0	0	1	0
$-2V_{dc}/6$	1	1	0	0	0	0	0	1	0
$-3V_{dc}/6$	1	1	1	0	0	0	0	1	0
$-4V_{dc}/6$	1	1	1	1	0	0	0	1	0
$-5V_{dc}/6$	1	1	1	1	1	0	0	1	0
$-6V_{dc}/6$	1	1	1	1	1	1	0	1	0

2.2.2. Selection of angles $\beta1$, $\beta2$, ..., $\beta6$

The switching delay angles, $\beta1$, $\beta2$, ..., $\beta6$ shown in Figure 3 are obtained by minimising the sum of the squared error between the actual output of the converter and a reference sinusoidal wave. Due to the symmetry of the output waveform, only one quarter cycle was considered in the optimization. The objective function of this optimisation algorithm is to minimise the following function:

$$\sum_{t=o_{\Delta t}}^{T/4} \left(V_{max}\ sin(2\pi ft) - \frac{V_{dc}}{6} \sum_{i=6}^{6} a_1(t) \right)^2 \qquad (2)$$

subjected to: $\forall i : 6, a_i(t) < a_i(t + \triangle t)$; where $a_i(t)$ is the state (1 when output is $V_{dc}/6$ and 0 when output is zero) of each H-bridge at time t.

Using this optimisation, it was found that $\beta 1 = 5°$, $\beta 2 = 15°$, $\beta 3 = 25°$, $\beta 4 = 36°$, $\beta 5 = 49°$ and $\beta 6 = 67°$.

2.2.3. Partial shading performance balancing

In the 13-level converter considered, the bridge switched on at the delay angle $\beta 1$ will supply power from $\beta 1$ to $(\pi - \beta 1)$. The PV module connected to this bridge will contribute more than any other PV module to form the stepwise ac waveform. On the other hand, the bridge switched at $\beta 6$ will supply power from $\beta 1$ to $(\pi - \beta 1)$ causing its PV module to contribute less than any other PV module when forming the stepwise ac waveform. In this operation, if a particular PV module is shaded, then it will always affect only a single step in the stepwise ac waveform. In order to circumvent the effect of shading on the output waveform, each bridge is switched on at different delay angle in each cycle. For example, the first bridge is switched on at $\beta 1$ in the first cycle, at $\beta 2$ in the second cycle, and at $\beta 6$ in the sixth cycle. This equalises the contribution of all the PV modules over a period of six cycles on voltage waveform and the amount of energy supplied. The switching pulse generator achieves this by comparing the modulating signal with a stair-case carrier signal of period $6T$ with a six distinct voltage levels at $sin(\beta 1)$, $sin(\beta 2)$, $sin(\beta 3)$, $sin(\beta 4)$, $sin(\beta 5)$ and $sin(\beta 6)$ as shown in Figure 4. The width of each step of the carrier signal is equal to T. Figure 4 also illustrates how a switching signal is generated for S_{13} (in Bridge 1). The 6-step stair-case carrier signal is compared to a sinusoidal modulating signal: when the modulating signal is greater than the carrier signal, the signal generator gives an output of 1; otherwise it gives an output of 0. To generate the switching signal to S_{23} (in Bridge 2), the carrier signal in Figure 4 is shifted to the right by time T seconds, such that when the carrier signal of Bridge 1 is $sin(\beta 1)$, the carrier signal of Bridge 2 is $sin(\beta 2)$.
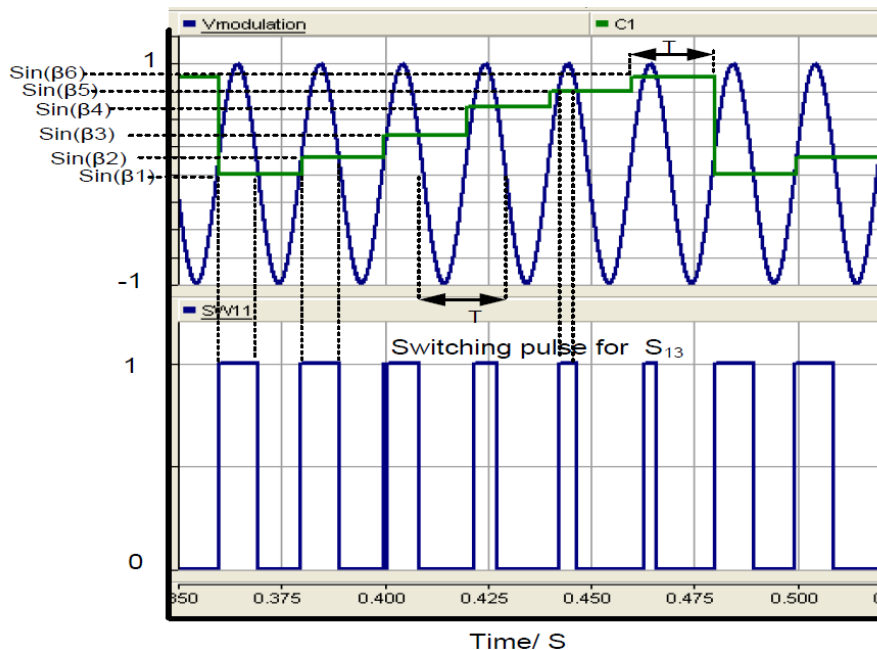

**Figure 4. Generation of switching signal for switch S_{13} of Bridge 1 of the inverter.**

3. Results

3.1. Hardware implementation of the single H-bridge module

The structure of a single H-bridge module in the 13-level inverter is shown in Figure 5. It mainly consists of a separate PV module and four semiconductor switching devices. As the data were not available for the PV modules, its I-V characteristic was experimentally obtained and shown in Figure 6. The switching devices used were IRF840 MOSFETs. Other than a dc source and semiconductor switching devices, MOSFET driver ICs, Opto-couplers and dc-dc converters were used in this H-bridge module for signal isolation purposes.
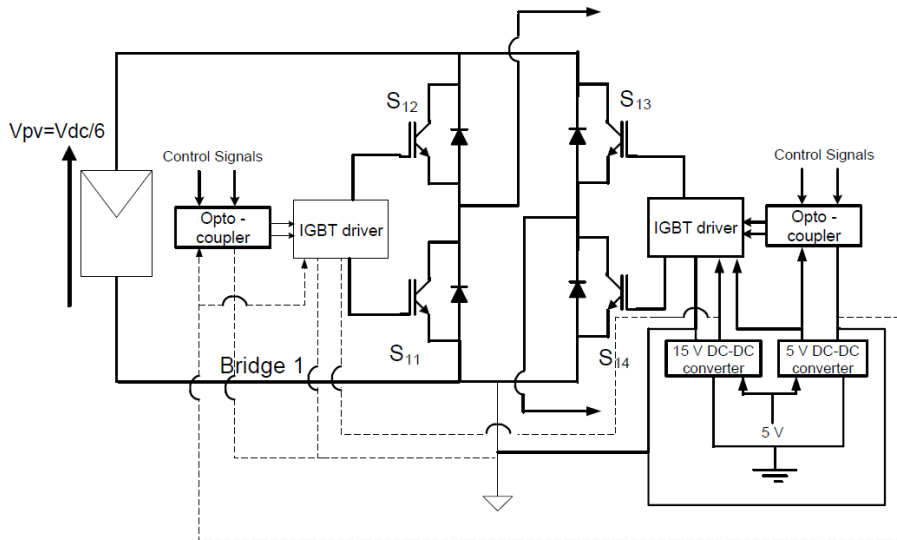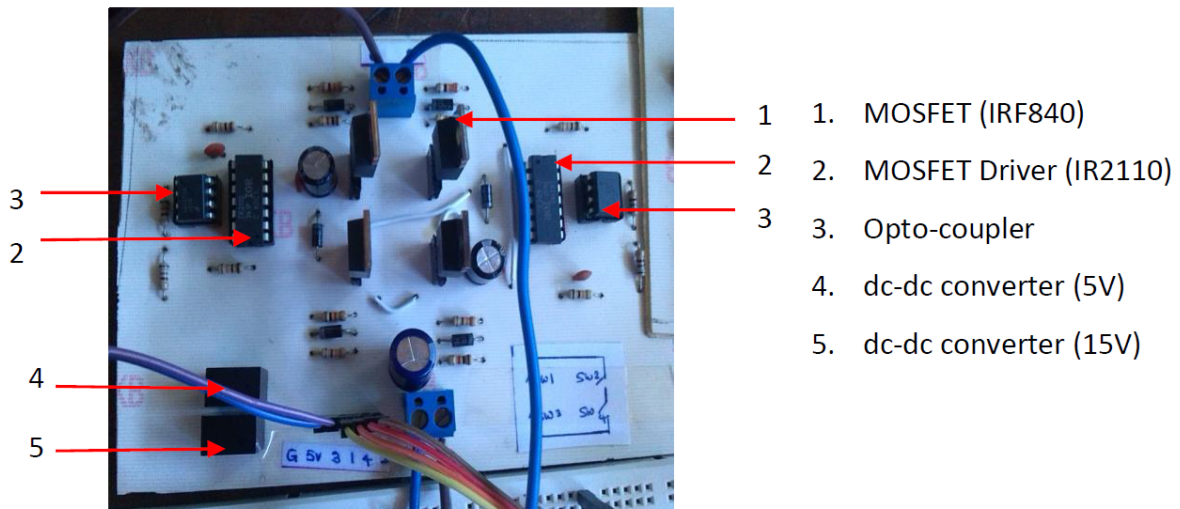

Figure 5. Single H-Bridge module.
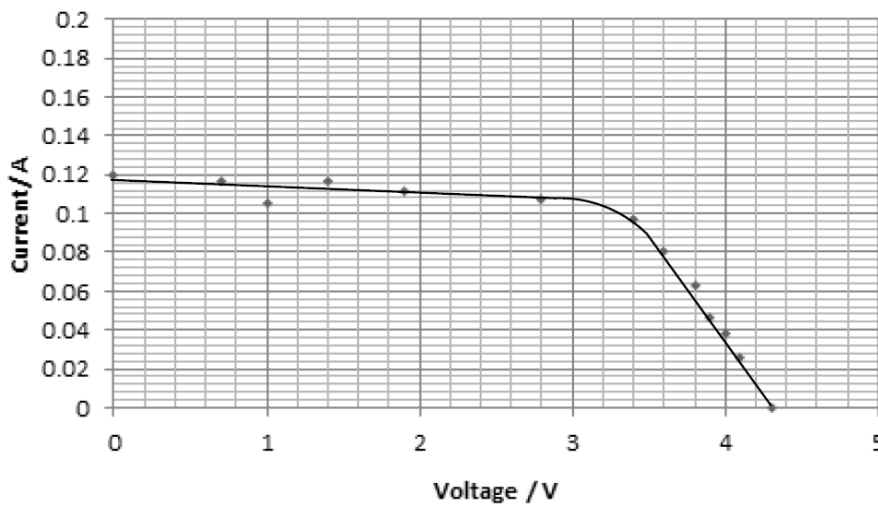
Figure 6. PV characteristic curve.

An IR2110 MOSFET driver IC was used to produce necessary high-side and low-side gate signals for the H-bridge inverter. When cascading two H-Bridges, the gate signals provided to the second tier H-Bridge need to be boosted up further with respect to the ground. Since it is not practical to boost up gate signals of each H-Bridge, isolated gate signals were provided with respect to a reference point. To isolate the driver ICs, two dc-dc converters were used to provide isolated supply voltages (5 *V* and 15 *V*). Opto-couplers were used to isolate the signal level gate signals. The single H-bridge module was fabricated on a PCB as shown in Figure 7.

1. MOSFET (IRF840)
2. MOSFET Driver (IR2110)
3. Opto-coupler
4. dc-dc converter (5V)
5. dc-dc converter (15V)

Figure 7. H-Bridge module.

The implemented H-bridge module was tested under different loading conditions where the dc link voltage was supplied from a PV module. Figure 8 shows the output voltage waveform of a single H-bridge inverter in an open circuit condition and in a loading condition (a 6 Ω resistor was connected to the output as a load) respectively.

3.2. The 13-level inverter

The 13-level inverter was implemented as a laboratory prototype by cascading six H-bridge modules. It comprises of six H-bridge modules having twenty four MOSFET (IRF840) switches along with their driver circuits. An STM32F4 discovery board was used as the control environment to generate gate pulses for the inverter switches.
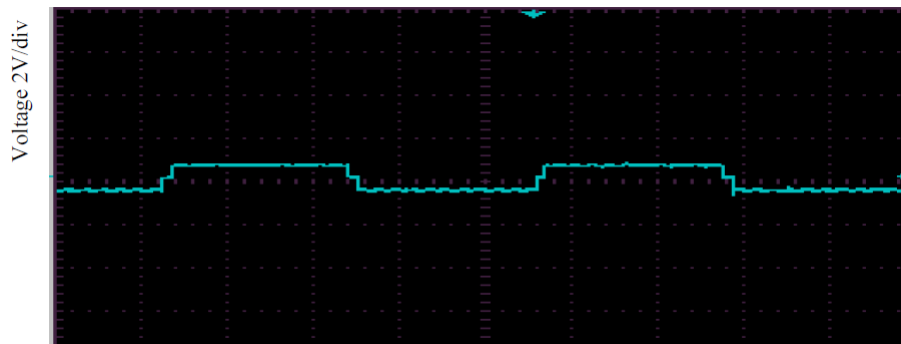
The implemented 13-level inverter is shown in Figure 9. The inverter was tested under laboratory conditions and the setup is shown in Figure 10.
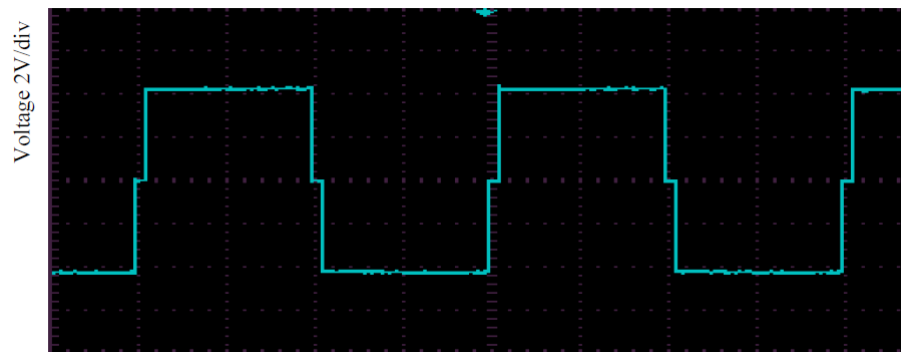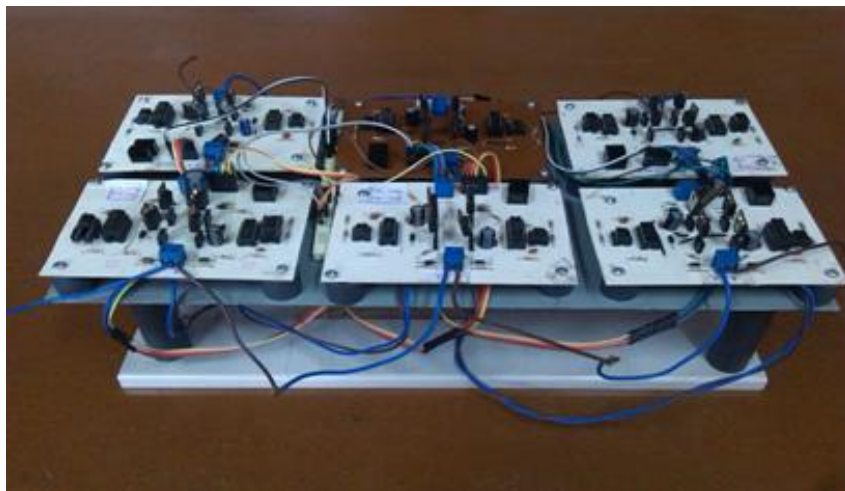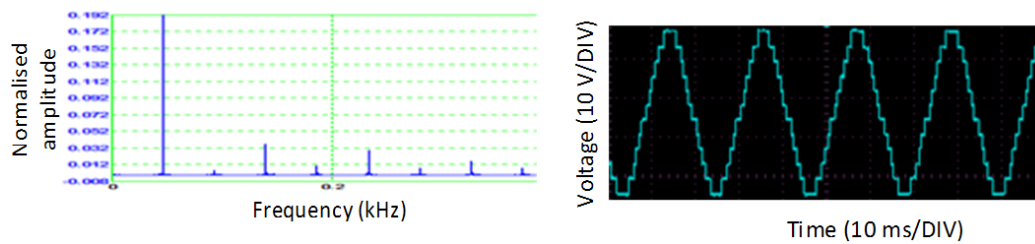
(a) open-circuited condition

(b) $R = 6\ \Omega$

Figure 8. 3-level inverter output.

**Figure 9. Hardware prototype of 13-level inverter.**

Figure 10. Testing setup.

Figure 11 shows the experimental output waveform and frequency spectrum of the output of the multi-level inverter under the open circuit condition. Figure 12 shows the experimental output waveform and frequency spectrum under loaded conditions. The load was maintained nearly at the maximum power point. Note that, in order to show the harmonic components properly, the spectrum is zoomed in: thus the fundamental component, which is 1 pu, is not properly displayed.

**Figure 11. Output voltage under open circuit condition.**
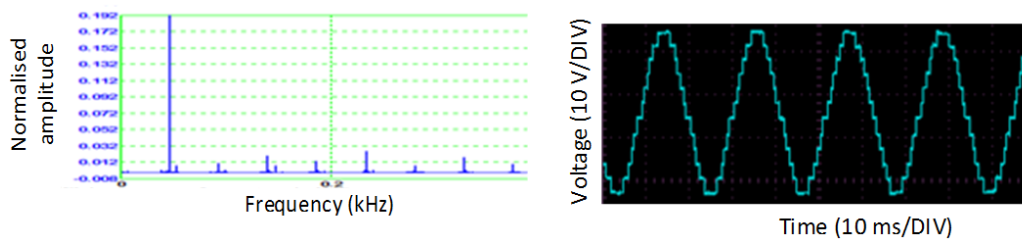
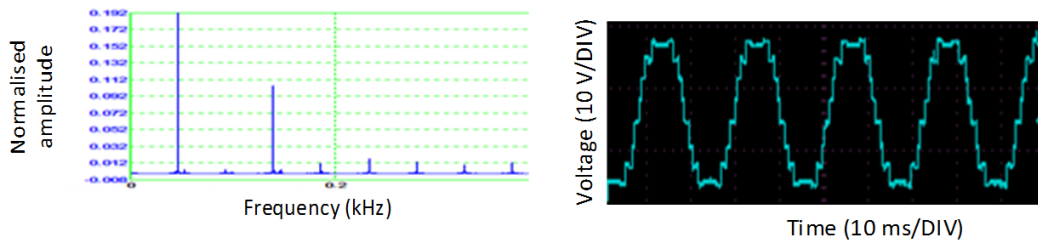**Figure 12. Output voltage under loaded condition.**

The peak of the voltage of inverter was 25.2 *V* at the open circuit condition, where the dc link (PV module) voltages of each H-bridge module were kept at 4.3 *V*.

3.3. Harmonic performance of the 13-level inverter with shading

Figure 13 and Figure 14 show the amplitude spectrum and output voltage waveform of the inverter at loading condition when one PV module is shaded and when two PV modules are shaded respectively. It was found that when two PV modules are shaded, the third harmonic component was high and the fifth harmonic component was low.
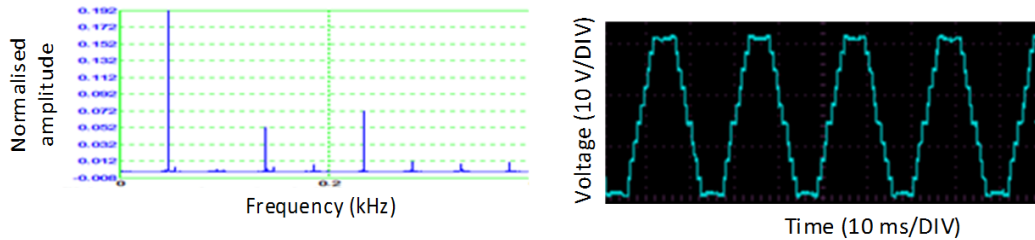
Figure 13. One module is shaded at loading condition.

Figure 14. Two modules are shaded at loading condition.

The harmonic components that appear in the output voltage for different conditions are given in Table 3. When the amplitude spectrum of non-shaded condition is considered, it can be seen that the third harmonic component is low at loading condition than the open circuit condition. The amplitude spectrum of partially-shaded condition and fully-shaded condition of a single PV module has no reasonable variation.

Table 3. Frequency analysis of multi-level inverter.

Condition		Frequency				
		Normalized amplitude				
		Fundamental	2nd	3rd	5th	7th
No load	No shade	1	0.008	0.053	0.018	0.008
	1 module is shaded	1	0.008	0.043	0.024	0.018
	2 modules are shaded	1	0.01	0.038	0.008	0.038
Loaded ($I = 40\ mA$)	No shade	1	0.005	0.028	0.023	0.018
	1 module is shaded	1	0	0.048	0.073	0.008
	2 modules are shaded	1	0.018	0.106	0.018	0.013
	1 module is partially shaded	1	0.058	0.05	0.077	0.008

4. Discussion

### 4.1. Effect of shading: RMS value of the fundamental of the output voltage

The significance of the proposed cascaded multi-level topology, in contrast to a PWM inverter (a single-phase single H-bridge unit with uni-polar PWM switching) was appreciated by examining the effect of shading on the fundamental of the output voltage value for both topologies. Using FFT analysis on the output voltages, the output voltage's fundamental component was evaluated; the results are shown in Figure 15. Here, shaded cells are randomly chosen. It can be observed that the fundamental voltage is significantly reduced in the conventional method as the shading is increased from 0% to 100%. However, the difference in the fundamental voltage levels between the two methods for same shading conditions is slightly reduced as the number of shaded cells are increased.
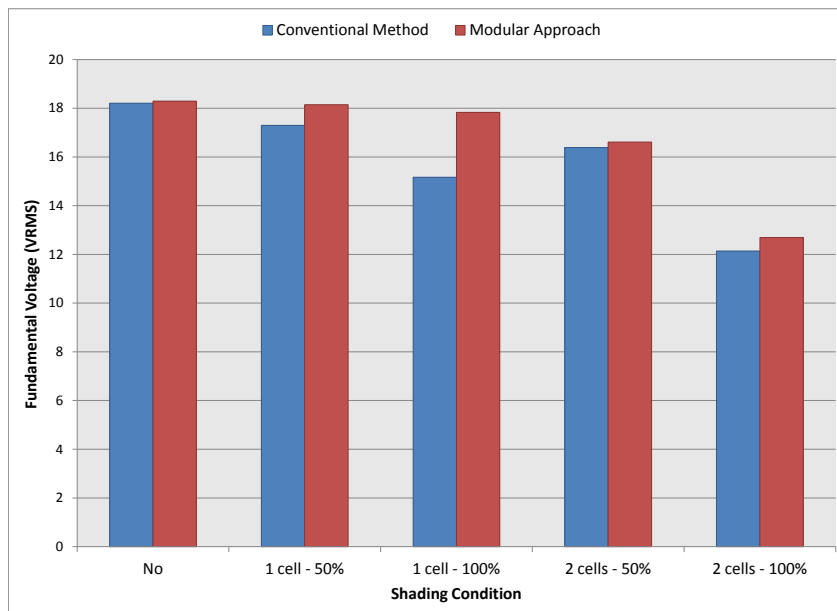
Figure 15. Effect of shading on the RMS value of the output voltage's fundamental.

4.2. Qualitative analysis on switching and conduction losses of the two approaches

A qualitative analysis on the switching and conduction losses of the total semiconductor switches associated with the two approaches is performed. Even though the prototype is based on low-power MOSFETs, in this analysis both MOSFETs and IGBTs were considered as semiconductor switches. It is shown how the switching frequency of the two methods and the ratings of the chosen semiconductors control the overall losses in the two systems.
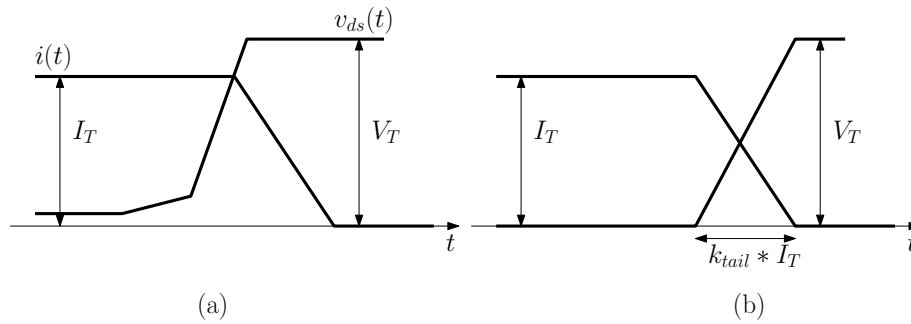
Figure 16. Turn-off switching transient: (a) ideal case, (b) approximated case.

4.2.1. Switching losses

Consider the proposed modular approach with n number of levels. Therefore, the voltage across each bridge is V_{dc}/n; and the voltage across each semiconductor switch in blocking state (V_T) is also V_{dc}/n. If the period of the fundamental is T_1, according to Tables 1 and 2, the number of switches switched for a period of $T_1/2$ is $2n$.

$$\text{Number of switches switched for a period of } T_1 = 2 * 2n \tag{3}$$

Assume that the switching loss associated with a switch is a linear function of on-state current ($k_i I_T$) and blocking state voltage ($k_v V_T$) across the switch such that the energy loss (E_{sw}) can be approximated as follows (see Figure 16);

$$E_{sw} = k_v V_T \times k_i I_T \times k_{tail} I_T \tag{4}$$

where, k_v, k_i and k_{tail} are constants assumed to be only device dependent, I_T is the constant output current of the PV system, k_{tail} determines the rise and fall time of the current through the switch during turn-on and turn-off transients; hence, the term $k_{tail} I_T$ signifies the duration of the switching transient.

Now, the total switching loss in the cascaded multi-level topology during a fundamental cycle is calculated as;

$$P_{loss-SW,M} = \frac{E_{sw} * 4n}{T_1} \tag{5}$$

Noting that $V_T = V_{dc}/n$ in eq. (4), using eqs. (4) and (5), we have;

$$P_{loss-SW,M} = \frac{4k_0 V_{dc} I_T^2}{T_1} \tag{6}$$

where, k_o is the simple product of the constants k_v, k_i and k_{tail}.

Now consider the PWM inverter; eq. (4) directly applies here as well. However, the total switching loss is defined as follows for this case;

$$P_{loss-SW,C} = \frac{E_{sw} * 4}{T_{sw}} \tag{7}$$

where, T_{sw} is the switching frequency of the PWM inverter.

Now using eqs. (4) and (7) and identifying that $V_T = V_{dc}$;

$$P_{loss-SW,C} = \frac{4k_0 V_{dc} I_T^2}{T_{sw}} \tag{8}$$

Finally, getting the ratio of the switching losses between the two methods, we have (the subscripts M and C refers to multi-level and PWM approaches);

$$\frac{P_{loss-SW,C}}{P_{loss-SW,M}} = \frac{T_1}{T_{sw}} = \frac{f_{sw}}{f_1} = f_m \tag{9}$$

where, f_m is referred to as the frequency modulation ratio.

With this result it is evident that the switching losses between the two approaches are ultimately defined by the frequency modulation ratio of the PWM approach. Therefore, in a qualitative sense, the number of levels in the modular approach has no effect on the ratio between the switching losses; however, it does have an effect on the absolute losses. As f_1 is 50 Hz and f_{sw} is usually selected around $1 - 2\ kHz$; f_m is around 10-20. That is, the PWM inverter has 10-20 times more losses than that of the multi-level inverter.

4.2.2. Conduction losses

The steady state current through the switches in on-state for both approaches is the same and equal to I_T. Therefore, at a glance it seems that the multi-level approach causes higher conduction losses due to the increased number of semiconductor switches. However, note that the blocking voltage (V_T) required in the multi-level approach is $1/n$ th of that of the conventional approach: i.e. V_{dc}/n. This means that for the multi-level approach, semiconductor switches with lower blocking voltages can be chosen; which have the advantageous characteristic of having lower on-state resistances (for power MOSFETs) or on-state voltages (for IGBTs):

$$P_{loss-CON} = I_T^2 \times R_{on} \ \text{ for MOSFETS}$$

$$P_{loss-CON} = V_{CE-on} \times I_T \ \text{ for IGBTs}$$

Therefore, the conduction losses associated with the switches would be actually lower than expected with the multi-level approach, provided that suitable semiconductor switches are chosen.

4.3. Comparison of power utilization between the multi-level method and the conventional method

With the conventional approach, with the aid of the intermediate dc-link and appropriate control, the complete PV unit is operated at the maximum power. However, the proposed method, with individual switching of each cell based upon angle β, the maximum power is not always extracted from each cell. Instantaneous utilization of this power depends upon the current operating position within the fundamental cycle (i.e. how many units are turned on) and depends upon the used load conditions as well: see Figure 17. For example, when $\beta = 30°$ (three units ON) and $R_L = 40\ \Omega$, the operation point is at *point x* marked on the plot. Therefore, as far as the zero shading condition is concerned, the conventional method implies better power utilization.

On the other hand, in practical applications there will always be the effect of shading. In such cases, the contrast between the power utilization between the two approaches is quite different. In the modular

approach, few redundant PV units are kept in the system to be used under shading conditions while the shaded unit is bypassed: therefore, the power utilization is unaltered in the modular approach.
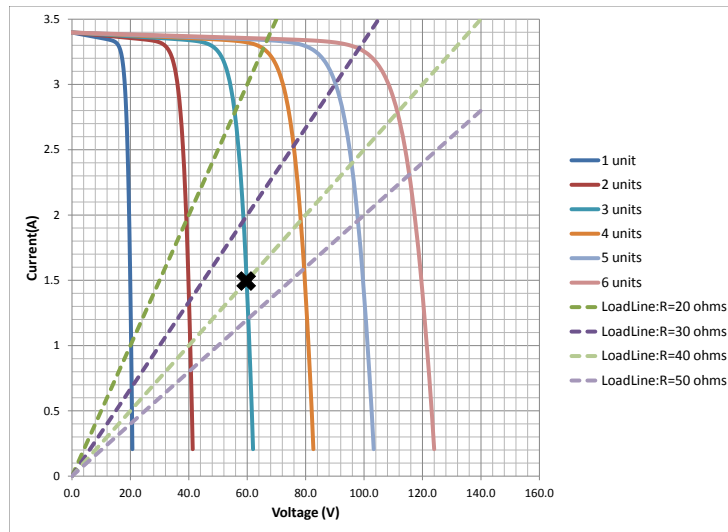
Figure 17. Load-line and I-V curve intersections depending upon instantaneous number of units that are turned ON in the modular method (for a PV unit of: $n = 36$, $R_p = 6.6\ \Omega$, $Rs = 0.005\ \Omega$, $I_o = 6.00E - 10\ A$, $I_{sc} = 3.4\ A$**).**
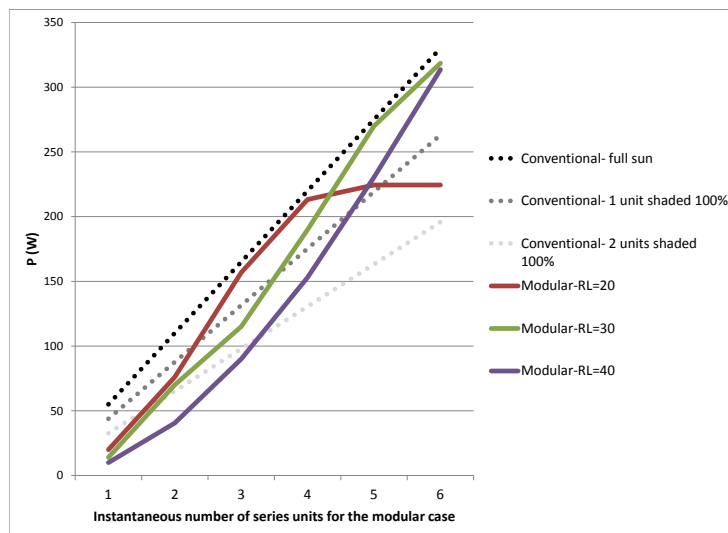
Figure 18. Comparison of power utilization between two approaches.

However, the shading will affect the conventional approach due to the series connection of the PV units in the array. The effect of this on the two systems is illustrated in Figure 18. It is evident that the instantaneous power output of the conventional method deteriorates with the increasing number of shaded units in a series-connected array (due to the drop in the available total output voltage).

Therefore, under shading conditions, the modular approach presents an appealing utilization of power: for instance, when 2 units are fully shaded, the modular approach offers an impressive advantage over the conventional method (see Figure 18).

5. Conclusion

PV systems are now considered as a promising option for electric vehicles. As these vehicles are constantly subjected to shading, and since the shading on cells is dynamically changing, a shading-proof inverter is ideally suited for such applications.

A development of a cascaded multi-level inverter based PV system is proposed for electric vehicle applications as a shading-proof inverter. The basic architecture and switching of the converter switches are described. A laboratory prototype of the proposed architecture was implemented using MOSFETs and harmonic performance under different shading conditions was evaluated. With a 13-level output, it was found that, except the third harmonic component, all the other voltage harmonics are below the values specified in the standards. It was also found that the third harmonic component increases with the shading on the cells/modules.

The shading performance, losses and power utilization of the cascaded multi-level inverter were compared with that of a conventional PWM inverter. From the results, it was found that the proposed inverter shows better immunity for shading than a PWM inverter. As the ratio of the losses of a PWM inverter to the proposed inverter is equal to the frequency modulation index, the switching losses of the proposed inverter is $1/10^{th}$ to $1/20^{th}$ of that of a PWM inverter. Furthermore, the conduction losses, when compared to a PWM inverter, can be optimized by properly selecting the blocking voltage of the semiconductor switches used. Even though the power utilization is compromised at full insolation, the power utilization performance of the proposed inverter is superior under shading conditions, thus ideally suited for electric vehicle applications.

The modular nature of the proposed inverter facilitates the cascading of more H-bridges with less cells/modules. This not only increases the number of steps in the synthesized sine wave, but also reduces the blocking voltage of the semiconductor switches. More levels will have a greater influence on the harmonic, shading, loss and power utilization performance of the proposed inverter.

Conflict of Interest

All authors declare no conflicts of interest in this paper.

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