Application of Waveform Engineering to GaN HFET Characterisation and Class F Design

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By

Christopher J. Roff

Division of Electrical and Electronic Engineering
School of Engineering
Cardiff University
United Kingdom

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ProQuest LLC
789 East Eisenhower Parkway
P.O. Box 1346
Ann Arbor, MI 48106-1346

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Summary

This thesis looks at the applications of radio frequency (RF) waveform measurement and engineering, concentrating on two specific areas: GaN Heterojunction Field Effect Transistor (HFET) characterisation and the design of class F power amplifiers.

The primary aim of this work was explain the DC-RF dispersion seen in GaN HFETs by documenting the details of the effect using RF waveform measurements. By collecting and analysing measured RF waveform data a number of trends have been identified that have led to a clear model of the DC-RF dispersion phenomena. This model, developed with QinetiQ Ltd., describes the effect for the first time in terms of velocity saturation that only severely limits channel current at the knee region.

Waveform techniques were also used to examine other areas of GaN HFET performance. Short-channel effects were characterised and the results were fed back into the device design, leading to improved performance. RF waveform measurements were also used for the first time to analyse degradation problems in RF power transistors.

The second part of the thesis looks at the use of RF waveform measurements in class F power amplifier circuit design. There is an industry wide requirement for high power and high efficiency power amplifiers, which has led to a focus on the class F mode. A class F amplifier is defined by the shape of the current and voltage waveforms at the active device, making it a logical target for a study using measured RF waveforms.

In this work, the largely theoretical existing research on class F has been extended to include a measured waveform based analysis. The results demonstrate how optimum class F performance can be achieved using real devices and highlights a number of interesting issues that a designer of a class F amplifier should consider.

Acknowledgements

Firstly I would like to thank my supervisors, Professor Paul Tasker and Dr Johannes Benedikt, who have shown great generosity in sharing their time, knowledge, ideas and passion for RF engineering with me. They have supported me throughout my course of study beyond what could ever be expected and have made my time at Cardiff tremendously enjoyable and satisfying. Other staff members at Cardiff, in particular Prof. Steve Cripps, Dr. Jonathon Lees, Dr. Adrian Porch, Dr. Richard Perks, Mr. Steve Watts and Prof. D.V. Morgan have also helped me enormously in my enjoyment and understanding of the subject.

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I would also like to thank all the fellow students in the Cardiff lab, which is a fantastic place to work and learn. I am particularly grateful to the students who have gone before me and developed the measurement systems I have used and the ideas I have built on in my own work. I have made many good friends amongst my fellow students and some have made significant contributions to helping my work, for instance (and in no particular order), Peter McGovern, Tudor Williams, Aamir Sheikh, Zaid Aboush, Dominic FitzPatrick, Randeep Sanei, Billy Su, Hao Qu, Alan Clarke, Mike Casbon, Mohammed Hashmi, Shaiful Hashim, Peter Wright, Simon Woodington and Will McGenn.

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Finally, I would like to thank all of my family and friends outside of work for their encouragement. My parents have been incredibly supportive throughout my whole education and life in general, as have my brother and sisters. All my friends who have listened patiently (trying not roll their eyes or stifle a yawn!!) as I have tried to explain what it is I "do" can at least attest to the enthusiasm I have developed for the subject.

List of Publications

Selected First Author Published Papers:

"Analysis of DC-RF Dispersion in AlGaN/GaN HFETs using RF Waveform Engineering"
C. Roff, J. Benedikt, P.J. Tasker, D.J. Wallis, K.P. Hilton, J.O. Maclean, D.G. Hayes, M.J. Uren & T. Martin
IEEE Transactions on Electronic Devices, Jan 2009, volume 56, issue 1, pages: 13-19.

Abstract: This paper describes how DC-RF dispersion manifests itself in AlGaN/GaN HFETs when the devices are driven into different RF load impedances. The localised nature of the dispersion on the IV plane, which is confined to the "knee" region, is observed in both RF waveform and pulsed-IV measurements. The effect is fully reproduced using 2D physical modelling. The difference in dispersive behaviours has been attributed to the geometry of the trap induced virtual gate region and the resulting carrier velocity saturation being overcome by punch through effects under high electric fields.

"A New Technique for Decreasing the Characterisation Time of Passive Load-Pull Tuners to Maximise Measurement Throughput"
C. Roff, J. Graham, J. Sirois and B. Noori
72nd ARFTG Microwave Measurement Symposium, Dec 2008, Portland, Oregon.

Abstract: This paper presents a technique for increasing the flexibility and the point density of passive load-pull tuner characterisation coverage from a reduced measurement collection cycle. Interpolation methods are used to enhance the resolution of available tuner positions whilst greatly reducing the time required for data collection prior to useful load-pull measurement. Results are presented to demonstrate validation of the method, showing that the mathematical accuracy in the predicted tuner S-parameters is greater than the reported physical reproducibility of the tuners. The impact of the new technique on characterisation time is demonstrated to yield a time saving of 80% - significantly increasing potential measurement throughput.

"Analysis of DC-RF Dispersion in AlGaN/GaN HFETs using RF Waveform Engineering"
C. Roff, J. Benedikt, P.J. Tasker, D.J. Wallis, K.P. Hilton, J.O. Maclean, D.G. Hayes, M.J. Uren & T. Martin
Compound Semiconductor Manufacturing Technology Conference, 2008, Chicago, Illinois.

Abstract: This paper describes an observed difference in how DC-RF dispersion manifests itself in AlGaN/GaN HFETs when the devices are driven into different RF load impedances. The localised nature of the dispersion on the IV plane has been observed in RF waveform measurements and is explained through physical modelling. The difference in dispersive behaviours has been attributed to the geometry of the trap induced virtual gate region and the resulting carrier velocity saturation being overcome by punch through effects under high electric fields.

"Utilization of Waveform Measurements for Degradation Analysis of AlGaN/GaN HFETs"
C. Roff, J. Benedikt, P.J. Tasker, D.J. Wallis, K.P. Hilton, J.O. Maclean, D.G. Hayes, M.J. Uren & T. Martin
70th ARFTG Microwave Measurement Symposium, Nov 2007, Tempe, Arizona.

Abstract: This paper employs, for the first time, RF waveform engineering to monitor device degradation over an RF "burn in" period. Measured RF current and voltage waveforms are used to monitor the degradation effects seen in GaN HFET transistors during large signal CW RF stress testing. The technique provides extra information on device performance compared with standard RF performance measures, demonstrating clearly where on the output IV plane the degradation is occurring and allowing device designers advanced insight into the degradation mechanisms limiting RF performance.

"Optimising AlGaN/GaN HFET Designs for High Efficiency"
C. Roff, A. Sheikh, J. Benedikt, P.J. Tasker, K.P. Hilton, J.O. Maclean, D.G. Hayes, M.J. Uren & T. Martin
The 2nd European Microwave Intergrated Circuits Conference, Oct. 2007, Munich, Germany.

Abstract: This paper uses measured waveforms to demonstrate how to optimise GaN HFET PA designs in order to achieve high power and high efficiency. Efficiency values of 80% were achieved at a power density of $3Wmm^{-1}$. The design procedure shows how waveform engineering, i.e. a combination of RF current and voltage waveform measurements, bias control and active harmonic load-pull, allow maximum performance to be achieved. The significant role of the device output capacitance in GaN designs that utilise large voltage swings is also explained, and a simple method for limiting the effect of C_{ds} is presented.

"Design Approach for Realization of Very High Efficiency Power Amplifiers"
C. Roff, J. Benedikt & P.J. Tasker
IEEE/MTT-S International Microwave Symposium Hawaii, June 2007, pages: 143-146.

Abstract: This paper presents a systematic methodology for overcoming the practical design problems inherent to real world high efficiency power amplifier (PA) designs. The approach is based on measured RF waveforms and hence guarantees the definite accomplishment of high efficiency modes of operation. The study highlights the important design considerations which must be understood in order to correctly engineer voltage and current waveforms at the device output. The factors limiting performance from reaching ideal efficiency values are clarified and demonstrated on a real device. The impact of device scaling is also explained, showing the increased difficulty in realising high efficiency amplifier modes in large periphery devices.

"Detailed Analysis of DC-RF Dispersion in AlGaN/GaN HFETs using Waveform Measurements"
C. Roff, P. McGovern, J. Benedikt, P.J. Tasker, R.S. Balmer, D.J. Wallis, K.P. Hilton, J.O. Maclean, D.G. Hayes, M.J. Uren & T. Martin
The 1st European Microwave Integrated Circuits Conference, Sept. 2006, Manchester, U.K., Pages 43-45.

Abstract: Detailed time-domain IV waveforms at RF frequencies are employed for characterisation of AlGaN/GaN HFETs in order to steer and advance device development. The IV time-domain data is used to isolate the separate effects of pinch-off and knee-walkout behaviour in limiting device performance. Furthermore, the waveform measurements which are obtained with a previously unseen level of detail, allowed the direct extraction of optimum device operating conditions.

List of Symbols

Symbol	Explanation
a	Voltage travelling wave entering the DUT
A	Amperes – unit of electric current flow
ACLR	Adjacent Channel Leakage Ratio
ACP	Adjacent Channel Power
Al	Aluminium
AlGaN	Aluminium Gallium Nitride
Al_2O_3	Sapphire
AM-AM	Amplitude modulation to amplitude modulation – a form of distortion
AM-PM	Amplitude modulation to phase modulation – a form of distortion
b	Voltage travelling wave leaving the DUT
C_{ds}	Drain to source capacitance
C_{gs}	Gate to source capacitance
CW	Continuous Wave signals – a time repetitive single tone excitation
D	Transistor drain terminal
dB	Decibel – logarithmic unit, typically of gain or power
dBm	Decibel – logarithmic unit with reference to 1mW
DC	Direct current
DC-IV	Direct current, current vs. voltage measurement – a typical device characterisation measurement
DUT	Device under test
E	Electric field
ECM	Electronic counter measures – a branch of electronic warfare, for instance using signal jammers
EER	Envelope elimination and restoration – a technique for achieving efficiency over a dynamic range of power levels in RF PAs
EPSRC	Engineering and Physical Sciences Research Council
ET	Envelope tracking – a technique for achieving efficiency over a dynamic range of power levels in RF PAs
eV	Electron volts
f	Frequency – speed in seconds taken for one period of signal
f_0	Fundamental frequency (also 2 f_0,, $3f_0$, nf_0 etc. for harmonically related frequencies)
Fe	Iron
FET	Field Effect Transistor
f_T	Transition frequency – frequency at which an active device has unity current gain
G	Gain or transistor gate terminal
Ga	Gallium
GaAs	Gallium Arsenide
GaN	Galium Nitride
HBT	Heterojunction Bipolar Transistor
HEMT (pHEMT)	High Electron Mobility Transistor (pesudomorphic HEMT)
HFET	Heterojunction Field Effect Transistor
Hz	Hertz - unit of frequency (also kHz, MHz, GHz etc.)
I	Electric current
I_{DC}	DC electric current
I_{DQ}	Quiescent DC electric current
I_{DS}	Drain source current
I_{GS}	Gate source current
I_{MAX}	Maximum current
I_{min}	Minimum current
I_{SAT}	Saturated current
IM3	Third order inter modulation product

IMS	IEEE International Microwave Symposium
IV	Current vs. voltage, plot, measurement etc.
J	Current density
K	Kelvin – unit of temperature
LDMOS	Laterally diffused metal oxide semiconductor (FET)
L_G	Gate length
LTE	Long term evolution – a next generation modulation scheme
m	Meter – unit of distance (also nm, μm, mm, cm etc.)
MBE	Molecular beam epitaxy
MESFET	Metal semiconductor field effect transistor
MOVPD	Metal-organic vapour phase deposition
N	Nitrogen
NIST	National Institute for Standards and Technology
NPL	National Physics Laboratory
OIP3	Output 3rd order intercept point
PA	Power amplifier
PAE	Power added efficiency
P_{DC}	DC power
P_{IN}	Input power
P_{OUT}	Output power
P_{RF}	RF power
$P_{RF\ IN}$	Input RF power
$P_{RF\ OUT}$	Output RF power
RF	Radio frequency
R_L	Load impedance
R_{opt}	Optimum impedance (usually optimum power)
s	Seconds - unit of time
SEM	Scanning electron microscope
Si	Silicon
SiC	Silicon Carbide
SiO	Silicon oxide
SiO_2	Silicon dioxide
Si_3N_4	Silicon nitride
T	Time period of one cycle
UK	United Kingdom
US	United States
V	Volts – unit of voltage
V_{bk}	Breakdown voltage
V_D	Drain voltage
V_{DC}	DC voltage
V_G	Gate voltage
V_{min}	Minimum voltage
V_{knee}	Knee voltage
v_{RF}	RF voltage
V_T	Threshold voltage
V_{sat}	Saturated electron velocity
W	Watts
W-CDMA	Wideband Code Division Multiple Access
X	Horizontal axis
X-band	6-18GHz radio frequency band
Y	Vertical axis
Z_0	System impedance (typically 50Ω unless otherwise stated)
α	Conduction angle of output current waveform
π	Pi – Constant of value 3.124...
ω	Radian frequency
λ	Wavelength
Ω	Ohms – unit of resistance

Δ	Delta – small difference
η	Drain efficiency
$\eta_{current}$	Current waveform factor (ratios DC and fundamental RF components)
$\eta_{volyage}$	Voltage waveform factor (ratios DC and fundamental RF components)
η_{offset}	Efficiency offset factor used to describe limitations of active devices that will scale achievable efficiencies down from the theoretical ideal
η_{loss}	Efficiency loss factor used to account for losses in the output matching network that will limit the reflected energy seen by the device
50 Ω	The fifty ohm system impedance settled upon by the industry as a standard interface impedance
σ	Electrical conductivity
ρ	Electrical resistivity
%	Percentage
°	Degree

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Chapter 1 - Introduction

1.1 Application space - radio communications

Radio communication can be defined as the use of electromagnetic waves above 10 kHz to transmit information. The technique has helped the modern world develop, allowing wireless communication between remote locations, facilitating television and radio broadcasts and even aiding manned space flight. Heinrich Hertz experimentally demonstrated the existence of electromagnetic waves in 1887 [1], based on the theoretical principles developed by numerous scientists, not least James Clerk Maxwell [2]. Upon discovering the existence of radio waves Hertz is alleged to have responded to the question of what applications mankind may find for these waves by saying "absolutely none!"

However, human society is largely built on the principle of communication and it did not take long for somebody to see the potential for using radio waves to send messages from one remote location to another without the restriction of a physical connection by expensive cables. The first demonstration of a successful radio communication system is widely credited to Guglielmo Marconi in 1895 (although Nicolai Tesla may well have been the true father of radio communication). Much controversy exists as to the novelty and originality of Marconi's work, but he rapidly established his reputation as the inventor of radio communication and by

the start of the 20th century Marconi had demonstrated trans-Atlantic radio transmissions and a tuned (frequency selective) transmitter / receiver architecture. Despite this revolutionary feat, the subsequent pace of development in radio communication was reasonably slow up until the 1940s. This was largely due to a lack of available radio frequency sources and the dominance of wired communication networks. However, cultural pressures associated with the second world war led to intense activity in the fields of radio communications and in particular radar – where radio signals are used for remote detection of objects many miles away.

The early radio systems were expensive, energy inefficient, fragile and physically bulky. Over time the components in these systems have been refined and all areas of performance have been greatly improved. New applications have become possible by combining RF communications principles with the powerful computational advantages of digital electronics. Probably the most significant commercial product to arise in the RF communications industry has been the personal mobile radio or mobile cell telephone. Mobile telephones first rose to prominence in the 1970s when digital electronics, solid-state RF components and integrated circuits allowed advanced functionality to be achieved in a relatively small form factor. Initial products were installed in vehicles but as the technology matured handsets became suitable for personal use. The value of communication with anyone almost anywhere on the planet has fuelled the mobile telephony boom and it is now estimated that roughly half the world's population own a mobile phone.

Mobile phone networks operate using a cellular architecture, first proposed in its current form at Bell Labratories in 1968 to more efficiently make use of the available electromagnetic spectrum – a precious commodity in the radio communication industry. The original idea continues to evolve into new schemes and standards, but essentially geographic areas are divided into cells operating at offset frequencies, with non-adjacent cells repeating the frequency allocation. This model

allows significantly more channels or users to simultaneously access the network. At the centre of each cell is a base-station that transmits and receives information with multiple mobile users within the cell and acts as the link into the standard public switched telephone network. When a handset is turned on it contacts the base-station and identifies itself to the network. The network maintains a dynamic list of which handsets are in which cell, and when incoming or outgoing calls are made a frequency channel between the handset and the base-station is set up and a conversation can be held. The process is managed by sophisticated computer algorithms that can seamlessly connect users across the globe even when the users are moving from one cell to another during the call.

Since the inception of the mobile phone, the pace of development in the radio communication industry has continued to increase, and mobile handsets now encompass growing functionality as they begin to assimilate the roles of other devices. A modern mobile phone can make real-time video calls using built in high quality digital cameras, access information from the internet and play digital audio and video files in high fidelity. The growing list of functions, in combination with the massive increase in users has strained the network and forced increasingly complex modulation schemes to be adopted to cope with the demand for data. Modulation is the process by which information is encoded onto the radio frequency carrier and essentially involves precisely defined shifts in amplitude, frequency and phase of the transmitted electromagnetic waves. The more complex the modulation scheme the more accurate or linear the radio transmission must be to successfully communicate. The increasing functionality of the handset also puts strain on the battery life.

Despite this large and growing list of functionality, the RF transmit and receive components remain a key element of the system. Indeed, energy consumption in mobile handsets has historically been dominated by the RF power amplifier (PA) – making the RF PA efficiency issue very high priority for handset designers. The PA is the final transmitter stage prior to the antenna which boosts the energy of the RF signal to allow it to be

broadcast with enough energy for the receiver to successfully decode the message. Consequently, there is a significant effort to increase the efficiency of this component. Likewise, the base-stations at the centre of each cell must also be as efficient as possible – especially given the high power levels they operate at (many hundreds of Watts).

Outside of the commercial and high volume wireless communications market there are an enormous variety of applications presenting more unusual problems and often requiring more bespoke engineering solutions. Higher frequency systems are largely dominated by space and military applications, due to regulatory issues relating to usage of the electromagnetic spectrum and the practicalities of avoiding atmospheric interference and eavesdropping from unwanted listeners. A major problem for the amplifier component in these military and space applications operating at high frequency is the need to deliver sufficiently high power in a suitably sized form factor. This has historically been a problem as high frequency signals are more susceptible to loss. Existing solutions are often bulky and therefore limit their use in applications where size and weight are crucial, for example a satellite payload.

1.2 RF power amplifiers

As stated, one of the more vital components in all these radio communication systems is the RF power amplifier. In order to transmit useful signals over significant distances it is crucially important that the output signal can be amplified with minimal distortion so that the information can be accurately recovered above the noise floor at the receiver. Simultaneously the same device must be operating in an efficient state to avoid high power consumption and consequent thermal dissipation problems. Whilst large proportions of the electronics systems that are developed in modern times are built using primarily digital techniques, the RF front end remains by and large an analogue problem, since it must interface with the analogue universe.

RF power amplifiers typically convert a small RF input signal into a larger RF output signal using energy from a DC supply. This conversion process is usually designed to occur in one frequency band for a given application. The ability to do this without creating distortions to the transmitted signal, or spurious signals outside of the original application's allotted bandwidth that may disrupt other users, requires a linear amplification process that is paramount to the successful operation of the majority of RF systems. The requirement for linear amplifiers must be balanced with the need for energy efficient systems – it is possible to use a larger transistor to linearly amplify the signal but this will dissipate significantly more DC energy and therefore heat. Additionally, as power transistors are often the most expensive component in the system, it makes little commercial sense to pay for unused power potential in the transistor. In order to boost efficiency, it is usually desirable to scale the power transistor to just large enough to amplify the signal nonlinearly, but only to the extent that any significant distortions can be removed or accounted for prior to transmission. This trade-off between efficiency and linearity is a fundamental problem that power amplifier designers are faced with.

1.3 RF power devices – a gap in the market

At the centre of RF power amplifiers are the so called active devices - the building block electronic components that actually amplify the RF signals. Historically vacuum tubes were used for RF amplification. First proposed by Lee De Forest in 1906, the vacuum tube triode was constructed from a glass tube containing three electrodes. The flow of electric current between two electrodes at either end of the vacuum tube could be controlled by adjusting the voltage on a third electrode called the gate. This important feature allowed a small signal applied to the gate electrode to be converted into a larger version of the same signal between the other two terminals – effectively amplifying the input signal.

Unfortunately even modern vacuum tubes are inherently fragile and power hungry devices that are less than ideal for many applications. A more desirable solution was not available until the advent of solid-state electronics – so called because the active devices are made from semiconductor crystals with no mechanically moving parts. The basic constituent solid-state part that almost all modern electronics are based upon is another three terminal switch called the transistor. William Shockley, Walter Brattain and John Bardeen pioneered the first transistor at Bell Laboratories in 1948. Their device used the semiconductor germanium, and could reproduce the main functionality of the vacuum tube whilst consuming less power and without the need for a fragile mechanical structure.

The primary requirement for a semiconductor material to be useful for the fabrication of modern high performance RF transistors is to allow rapid transport of carriers, and in particular electrons due to their inherently faster transport properties compared with holes [3]. The electron transport behaviour of a semiconductor is based on the electron mobility and electron density of the material. These values are fundamental properties of a semiconductor but in practical fabrication terms the

fundamental limits of a material system are rarely reached, instead they are restricted by the quality of the processed semiconductor material [4].

Material quality is generally limited by defects within the semiconductor crystal lattice such as impurities and broken bonds. These lattice defects interrupt electron transport through mechanisms including electron scattering and trapping [3]. The ability to successfully grow semiconductors without introducing prohibitive quantities of defects has advanced with the rapid improvements in growth techniques. Of particular benefit to building RF transistors has been the ability to grow more complex compound semiconductors combining multiple elements in a single crystal. Techniques such as molecular beam epitaxy (MBE) and metal-organic vapour phase deposition (MOVPD) developed since the 1970s can allow control over the composition of structures with a resolution in the order of individual atoms [5]. The increased control over epitaxial composition has led to a larger number of materials being available to RF transistor designers, as well as the ability to deposit sharp heterojunctions between different materials, resulting in the ability to engineer structures capable of extremely high switching speeds.

Perhaps the most significant compound semiconductor to emerge for high frequency transistor applications has been gallium arsenide (GaAs) and its associated alloys. GaAs has been used in a broad range of high frequency transistors such as metal semiconductor field effect transistors (MESFETs), pseudomorphic high electron mobility transistors (pHEMTs) and heterojunction bipolar transistors (HBTs) and is now generally considered a mature technology system with the majority of problems reduced to the extent that they no longer impinge significantly on device performance. Depending on the transistor design and the alloys involved, GaAs based devices can operate with useful gain at frequencies well above 100 GHz [6]. Unfortunately this performance is limited to low power levels due to the tolerable breakdown fields and the thermal capabilities of the semiconductor.

Silicon (Si) is another mature semiconductor, and the Si laterally diffused metal oxide semiconductor field effect transistors (LDMOS FETs) are a transistor technology capable of high power RF amplification [7]. Unfortunately, these transistors are not capable of particularly high frequency operation, with useful gain rolling off above 4 GHz. Therefore, a gap in the capability of solid state amplifiers has remained, with high power, high frequency amplifiers still being built using travelling wave tube technology. The opportunity for GaN solid state transistors is demonstrated by the graph in Figure 1-1 below, where the RF PA application space is shown.

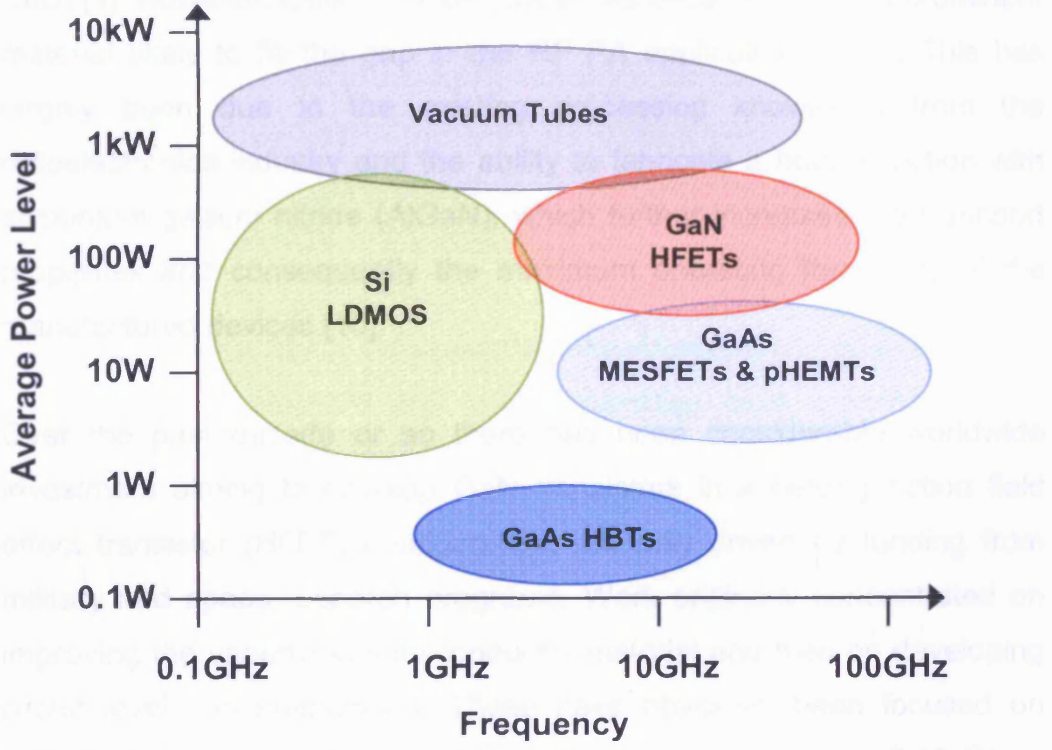

Figure 1-1 Approximate application space of various RF PA technologies (note whilst this graph indicates the typical uses, many technologies can also be used in lower power and lower frequency applications where appropriate).

1.4 Overcoming the frequency / power limitations in solid-state RF devices – introducing GaN

In order for solid-state high power, high frequency RF transistors to be developed, a semiconductor material system is required which combines good transport properties with excellent thermal characteristics and a tolerance to high breakdown electric fields. High breakdown fields allow large terminal voltages to be applied to the device, increasing its power capabilities. This attribute is an intrinsic feature of wide band-gap semiconductors, and a number of material systems have been proposed with the necessary properties, including diamond [8] and silicon carbide (SiC) [9]. However, gallium nitride (GaN) has become the most prominent material likely to fill the gap in the RF PA application space. This has largely been due to the existing processing knowledge from the optoelectronics industry and the ability to fabricate a heterojunction with alimunium gallium nitride (AlGaN), which further increases the transport properties and consequently the maximum operating frequency of the manufactured devices [10].

Over the past decade or so there has been considerable worldwide investment aiming to develop GaN transistors in a heterojunction field effect transistor (HFET) configuration, primarily driven by funding from military and space research programs. Work originally concentrated on improving the underlying semiconductor material and then on developing circuit level implementations. These have obviously been focused on military and space applications often at X-band frequencies (6-18 GHz). Recently, a number of manufacturers worldwide are beginning to offer GaN HFET based products for commercial applications in lower frequency bands. These applications include mobile phone base stations, which are attractive due to their potentially high volumes. Realistically in a cost conscious commercial environment, market traction is more likely to be built up in higher frequency applications. Opportunities include base stations for future high data rate broadband internet and long term evolution (LTE) converged communication systems and other more niche

markets where cheaper technologies such as Si LDMOS cannot compete with the potential performance enhancements of GaN HFETs.

Due to the relative immaturity of the semiconductor technology and some facets of the device structure, a number of issues can limit the performance of GaN HFETs and therefore require improved understanding and eventual solutions. Many methods exist to assess GaN device behaviour and enable the necessary analysis to help solve the performance issues. A particularly powerful tool for analysing RF transistors is the use of time domain RF current and voltage waveforms. Calibrated measurements of current and voltage waveforms have historically been difficult to achieve at GHz frequencies, and consequently very little work has been done on applying RF waveform measurements to analyse device issues in developing RF technologies. This technique holds great potential for analysing many areas of device fabrication and eventual circuit design.

The opportunity to apply measured RF waveforms on a device process that has yet to stabilise and feed information back into the device development exists within this PhD project, in conjunction with the GaN HFET process at QinetiQ Ltd. in Malvern, UK. Figure 1-2 below shows an SEM micrograph of a GaN HFET cross section from QinetiQ Ltd. It is possible to see the precisely deposited layers of semiconductors and metals that need to be manufactured correctly for the device to operate successfully.

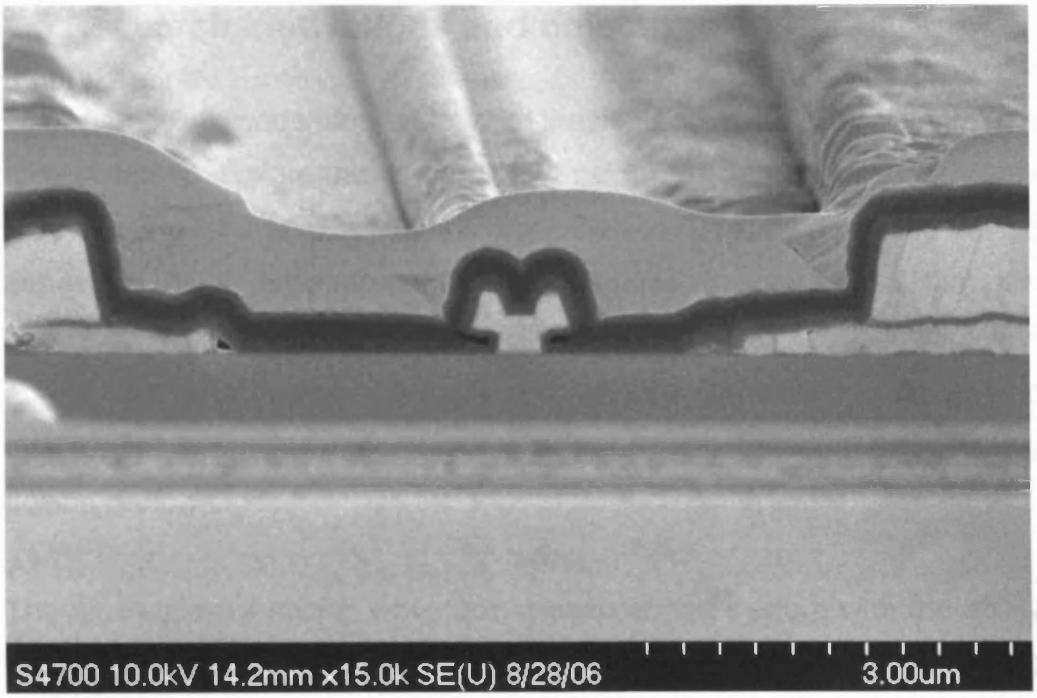

Figure 1-2 SEM Micrograph showing the cross section of a QinetiQ Ltd. GaN HFET grown on a Sapphire substrate.

1.5 Research motivations and objectives

Two parallel threads dominate this thesis. The initial objective of the project was to explore the use of RF waveform measurements to analyse a developing RF transistor technology - GaN HFETs. By analysing device behaviour using time domain measurements it was hoped that the increased insight gained would make it possible to draw conclusions about the effectiveness of different device processing steps and eventually to improve understanding of the physical mechanisms limiting device performance.

The availability of an RF waveform measurement system with the ability to engineer the RF waveforms at the device terminals in addition to measuring them leads to a natural focus on circuit emulation. Essentially the measurement system can be used to rapidly test a device's performance in different modes and configurations. Consequently, an extension of the initial objective to explore high efficiency amplifier architectures, and in particular class F operation has become the second main thread of the thesis. The analysis of harmonically controlled amplifiers within a controlled and comparable environment is typically limited to software simulator packages, but the RF time domain measurement system with harmonic load-pull loops lends itself ideally to the job of a "real-world simulator" allowing it compare actual devices without relying on non-linear models. It is a convenient environment for verifying assumptions made using such models in the simulator, and for testing and extending the sometimes overly ideal theoretical work on high efficiency PAs.

1.6 Thesis structure

Chapter 1 provides an overview of the application space - the radio communications industry - and describes the importance of the RF power amplifier within that context. The need for linearity and efficiency within the power amplifier component is highlighted, based on the system level requirements. The desirability of a simultaneously high frequency and high power solid-state transistor to enable new power amplifiers to perform better is stated, and GaN HFETs are introduced as the potential solution. Measurement of transistors using RF current and voltage waveforms is considered as an approach to analysing problems in developing transistors and circuits. The research objectives and motivations are then presented, setting the scene for the work in the following chapters on RF waveform measurement of GaN HFETs and emulation of class F PAs.

Chapter 2 describes the background theory of GaN HFETs. A brief summary of the material properties of GaN is followed by an examination of the techniques used in device manufacture. The aim of this section is to support work in later chapters that analyze device performance with reference to these growth and processing steps. The state of the art published GaN HFET performance is presented to give the reader an appreciation for the present state of the technology. The problems afflicting some GaN devices are then described as a foundation for measured results and analysis given in later chapters. Industry standard methods for characterizing an RF transistor semiconductor technology like GaN HFETs are depicted and the time-domain waveform measurement system is introduced more thoroughly.

Chapter 3 builds on this work by describing a variety of experiments conducted on GaN HFETs that highlight device level problems and can be used to identify solutions that can improve performance when fed back into the device design. Major issues tackled include current collapse, short channel effects, degradation and robustness. Physical

modelling work performed at QinetiQ Ltd. is briefly introduced and used to explain some key observations made from the measured waveform data. The work shows how insight gained from examining measured RF waveforms has led to an improved understanding of current-collapse in terms of the premature velocity saturation of the electrons in the device channel.

Chapter 4 provides an introduction to high efficiency amplifier design, looking at single device and more complex architectures. The class F mode is highlighted as a potentially important approach to gaining higher efficiency values in the power amplifier than typically seen in the radio communications industry at present. A systems level appraisal of the value of class F in modern applications, in particular those with broad bandwidth or where constant envelope modulation is not used, is given concluding that class F can retain its potential when combined with other circuit techniques. Historical and recent contributions to class F theory are discussed and some of the overly ideal assumptions of this work are highlighted.

An extension to some of the more ideal case class F literature is made in Chapter 5. Here the waveform measurement system with harmonic load-pull is used to analyse the problem in a realistic setting, using actual devices. An analysis of how to design a class F amplifier by engineering the current and voltage waveforms in a systematic way is presented and validated by the high efficiency results which closely resemble the theoretical maximums. The sensitivity of the class F mode in a real device is studied and compared back to the singular solution of ideal class F. Results of GaN class F experiments are given, showing how devices examined in Chapter 3 can be utilised in successful designs.

Chapter 6 draws conclusions from the thesis work and briefly summarises the main contributions. Chapter 7 then looks at future developments, concentrating on the way RF waveform data can be used to help bring together the two complementary fields of device fabrication

and circuit design and points towards some specific areas that would benefit from further study.

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Chapter 2 – Review of GaN HFET Technology and Characterisation

2.1 Introduction

High power, high frequency amplifiers are required for a variety of free space signal propagation applications, for instance military electronic counter measures (ECM) systems, satellites and commercial radar. It is desirable to use solid-state amplifier parts in these products due to their smaller size, reduced weight and increased reliability compared with historically dominant vacuum tube technologies. However, high power, high frequency solid-state amplifiers are only just becoming a mass-produced reality. The technology closest to making the leap from research and development into an established commercial solid-state technology is the AlGaN/GaN HFET.

This chapter discusses the AlGaN/GaN material system and its advantages for high power, high frequency transistor fabrication in a Heterostructure Field Effect Transistor (HFET) configuration. The key technology issues that have afflicted these devices are then discussed alongside some of the existing measurement techniques industrially employed to characterise their performance. Finally a time-domain

waveform measurement system is introduced as a tool for RF transistor characterisation, in preparation for the following chapters.

2.2 Suitability of GaN for high power, high frequency transistor fabrication

Compared to the incumbent solid-state high frequency, high power material systems, GaN has some inherent advantages that have made it an attractive proposition. The underlying material advantages of GaN are summarised and compared to competing technologies in table 2-1 below.

	Si	GaAs	4H-SiC	Diamond	GaN
Band-gap (eV)	1.1	1.42	3.26	5.45	3.39
Electron Concentration (cm^{-3})	$1.5x10^{10}$	$1.5x10^{6}$	$8.2x10^{-9}$	$1.6x10^{-27}$	$1.9x10^{-10}$
Mobility (cm^2/Vs)	1350	8500	700	1900	1200 (Bulk) 2000(2DEG)
Saturated Velocity ($10^7cm/s$)	1.0	1.0	2.0	2.7	2.5
Breakdown Electric Field (MV/cm)	1.0	2.7	20	5.6	27.5

Table 2-1 Theoretical material properties of various high power, high frequency material systems at room temperature, after Mishra *et al.* [1]

2.2.1 Material properties – a wide band-gap semiconductor

For a transistor to operate at high power levels it must be capable of withstanding large voltages, currents and the associated high temperatures that will arise in the device. GaN transistors can perform well at high temperature and are able to withstand high electric fields before the onset of breakdown due to the properties of the semiconductor lattice structure. The atoms in the GaN lattice (and often in its associated alloys) are densely packed and the chemical bonds between the atoms are extremely strong. This results in a wide band-gap between the conduction and valence bands; ≈3.4 eV in GaN as opposed to ≈1.4 eV in GaAs [2]. The wide band-gap also makes GaN devices more suitable for

radiation exposed operating environments, making it ideal for military and space applications.

2.2.2 Electrical properties

In terms of electron transport GaN has relatively low mobility, but this is compensated for by a high saturated drift velocity when operating in a heterojunction configuration [3]. This allows good RF performance and, dependant on the device layout geometry, f_T values in excess of 40 GHz can be achieved [4]. Single heterojunction devices are capable of current densities of approximately 1 A/mm, and higher current densities are possible by including multiple channels [5]. The wide band-gap also allows the semiconductor to tolerate high breakdown fields and subsequently RF voltage swings in excess of 100 V can be harnessed to increase output power levels.

2.2.3 Thermal properties

A key issue for designers of transistors operating at high power levels is the dissipation of heat away from the active channel. Potentially catastrophic channel temperatures can be developed in high power RF devices where efficiency values are often surprisingly low. For the majority of horizontal channel devices the heat is extracted vertically down through the device substrate layers and metalisation into packaging and heat sinks. Therefore, good thermal conductivity in the semiconductor layers below the channel is essential for successful high power operation. The thermal conductivity of GaN itself is at least three times that of GaAs, and devices grown on SiC can also take advantage of its excellent thermal performance, allowing the heat generated by the high power levels to be safely dissipated [2]. The thermal performance of various potential substrate materials is given in Table 2-2 below.

	GaAs	GaN	Sapphire	Si	4H-SiC
Thermal conductivity (W/cm K)	0.43	1.3	0.42	1.5	3.3 - 4.5

Table 2-2 - Typical thermal conductivity performance of GaAs, GaN and various candidates for GaN HFET substrate materials, after Mishra *et al.* [1]

2.2.4 Substrate availability

Despite the efforts of numerous companies, at the present time there is no affordable native GaN substrates of practical size and availability. Instead GaN material is typically grown on either SiC, sapphire (Al_2O_3) or silicon bulk substrates. The choice of substrate material is a balance between commercial pressures of cost and throughput with performance issues, such as lattice match with the epitaxially deposited GaN material and the substrate's heat dissipation capabilities.

Generally speaking, SiC and sapphire substrates are expensive and typically limited to a few inches diameter, whilst silicon wafers are cheaper and can have diameters exceeding six inches. SiC has become the favoured substrate for device performance (due to its lower lattice mismatch and higher thermal conductivity) but remains expensive and many manufacturers are now achieving good performance on Si [6]. Devices grown on silicon can be significantly cheaper but require extensive nucleation buffer layers be grown to reduce strain caused by the extreme lattice mismatch and often have to incorporate other design features such as a wider source drain separation to ease the electric field and thermal strains on the narrow band gap and less thermally efficient silicon substrate material.

2.2.5 Power performance

The ability of GaN HFET devices to simultaneously handle large current densities and large voltage swings results in devices with a relatively high power density (a metric that scales the output power by the size of the

device so that it relates the power in Watts achieved from an equivalent gate periphery of 1 mm). In a high power density transistor the fundamental impedance for optimum power will be larger, making it easier to match to the industry standard system impedance of 50 Ω. Moreover, less layout area will be required to achieve a given power level, so the transistor will have lower parasitic elements (such as capacitances arising from the gate and drain pads) again leading to easier matching and consequently broader bandwidth PA designs.

2.2.6 Drawbacks

Despite its performance, exploitation of GaN's advantages in finished systems remains relatively low. This trend is primarily due to the expense and, to a lesser extent, the relatively unproven lifetime reliability performance of the devices. However, for applications where high frequency and high power are simultaneously required alongside requirements for reduced size and weight, GaN's performance advantages can be well worth the financial cost. Accordingly, efforts continue across the RF and semiconductor industry to improve the performance and cost of GaN HFETs to increase their uptake in more financially competitive commercial markets.

2.3 Operation and Growth of GaN HFETs

2.3.1 The Heterojunction field effect transistor - HFET

The ability to form successful heterojunctions between GaN and AlGaN has made GaN HFET fabrication possible and resulted in a higher operating frequency for the devices. The HFET or HEMT (High Electron Mobility Transistor) principle is based on the isolation of active carriers into a two-dimensional electron gas (2DEG) on one side of the heterojunction. This enhances the electron mobility of the structure since the 2DEG electrons are effectively screened from the dopent atoms or other ionised scattering atoms held on the other side of the heterojunction [7]. This separation is possible because the materials are selected to have band-gaps such that one layer (in this case the GaN) acts as an electron confinement region when it is grown in a heterojunction with a wider band-gap barrier layer (AlGaN). Figure 2-1 shows the band-gap structure and 2DEG creation in the confinement region at the AlGaN/GaN heterojunction.

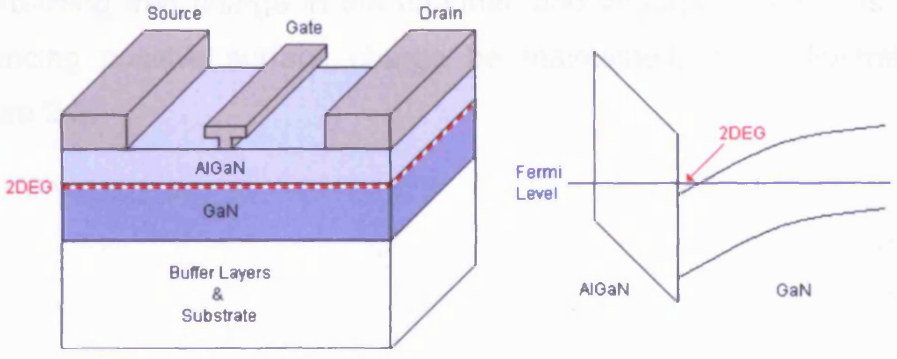


Figure 2-1 Simple AlGaN/GaN HFET structure and band diagram showing 2DEG formation at the heterojunction

2.3.2 Doping in GaN HFETs

The GaN HFET differs from the more established AlGaAs/GaAs HFET because the electrons populating the 2DEG do not arise from doping in the conventional sense as they do in the GaAs transistors (where each n-type dopent atom donates a free electron). In a GaN HFET the electrons in the 2DEG arise from two distinct processes. Firstly there is the

spontaneous polarisation present in the GaN and AlGaN lattices, which is caused by the strongly polar nature of the bonds between the atoms. The polarisation of individual bonds arranged in a uniform lattice results in a net charge distribution across the lattice which can be positive or negative at the edge of the crystal depending on the lattice terminating atom [8]. The terminating atom is engineered by maintaining either a Nitrogen or Gallium rich atmosphere.

The other mechanism providing electrons in the GaN HFET 2DEG is the piezoelectric effect, which generates electrons because of the strain the semiconductor crystal is under due to the lattice mismatch between the different layers [8]. It is through this process that the Aluminium concentration can control the density of electrons in the channel, since more Al in the AlGaN layer will increase the strain in the structure. However, too much strain can result in cracks and damage to the material and so Al content in the AlGaN layer does not usually exceed 35%. The spontaneous polarisation is believed to be the dominant effect in providing free charge in the channel, and importantly requires that a balancing positive surface charge be maintained, as is illustrated in Figure 2-2.

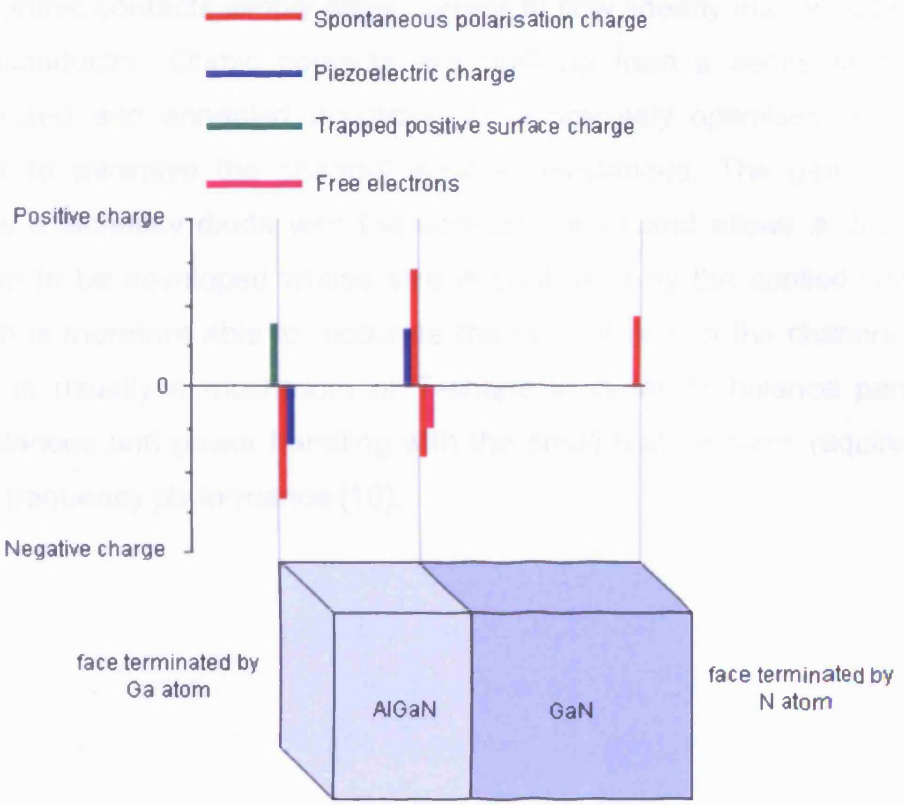


Figure 2-2 Diagram showing the location and approximate relative magnitudes of the spontaneous and piezoelectric charges in an AlGaN/GaN heterojunction, after M. Shur [9].

2.3.3 Growth of GaN HFETs

The transistor active layers are epitaxially deposited, usually in an MOPVD process on a substrate layer and appropriate buffer layers. The purpose of the buffer layers are to gradually match the lattice constants of the substrate material and the active layers above in order to reach a stage where the material is of high quality, i.e. there is a relatively low defect density. After the main epitaxy stage, metal contacts are deposited. The drain and source contacts are both ohmic contacts, whilst the gate is a Schottky contact. The contacts are usually defined by optical lithography, unless very high frequency operation is required. In this case the gate contact must be written using the slower e-beam technique which uses an electron beam instead of optical radiation to achieve a finer resolution.

The ohmic contacts simply allow current to flow linearly into or out of the semiconductor. Ohmic contacts are built up from a series of metals deposited and annealed according to a precisely optimised recipe in order to minimise the channel access resistances. The gate contact forms a Schottky diode with the semiconductor and allows a depletion region to be developed whose size is controlled by the applied voltage, which is therefore able to modulate the current flow in the channel. The gate is usually a mushroom or T-shape in order to balance parasitic resistances and power handling with the small feature sizes required for high frequency performance [10].

2.4 Advanced GaN HFET processing techniques

A number of additional features can be added to GaN HFET designs in an attempt to improve performance, and in particular to remedy undesirable trapping effects. The most common features are surface passivation layers, field plates, cap layers and gate recesses:

2.4.1 Surface passivation

Surface passivation techniques in GaN HFETs involve covering the surface with an insulating layer after the device has been processed to protect the device surface from impurities, to help accommodate strain and to reduce unwanted current flow between surface states [11]. The exact mechanisms behind the passivation techniques are not fully understood but Si_3N_4 is widely regarded as the most successful passivation material, although a number of other materials have also been experimented with including SiO_2 and SiO [12]. The process is particularly successful if performed *in-situ* (in the same reactor as the other growth steps so that no surface contamination can occur) or alternatively if a thorough surface cleaning procedure is carried out before the passivation is laid down.

2.4.2 Field plates

Field plates are metalic extrusions deposited immediately above but electrically isolated from the device except by a connection to either the gate or source terminal. The objective of incorporating field plates is to reduce the peak electric field across the high field gate to drain region by spreading the field distribution more uniformly across a larger area of the device. It is believed that this reduces the likelihood of electrons being accelerated out of the active channel and into traps by the high peak electric fields [13]. The field spreading effect also increases the breakdown voltage of the device [14]. Unfortunately field plates can have a detrimental effect on the maximum operating frequencies of devices, since they can introduce extra capacitances. Varying the connection,

positioning and size of the field plates can greatly alter their beneficial effects, and each foundry must optimise their individual design to balance their needs. Figure 2-3 below demonstrates a simple GaN HFET structure with a field plate and surface passivation.

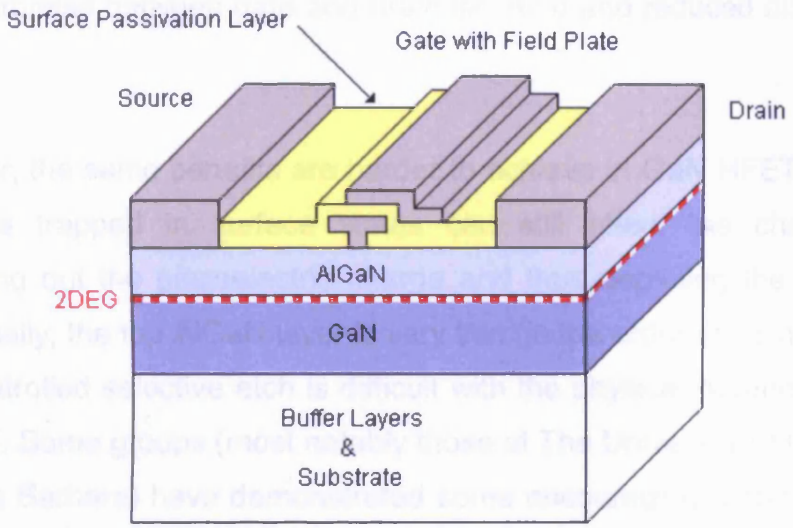


Figure 2-3 Diagram showing a simple GaN HFET with a field plate and surface passivation

2.4.3 Surface caps

Another technique which has been shown to reduce the DC-RF dispersion in GaN HFETs is to include a GaN cap layer above the AlGaN surface. The extra layer isolates fluctuations in the surface potential from the active channel and results in devices with DC-RF dispersion behaviour comparable to passivated devices [15]. However, GaN capped devices have shown problems with gate leakage. A number of solutions have been suggested, for example employing a thin SiO_2 layer on the sidewall of the gate or adopting a recessed architecture [16].

2.4.4 Recessed gate architectures

Recessing the gate to physically separate it from the surface states has historically been a successful strategy for removing dispersion problems in GaAs devices. Recessing allows the gate depletion region to start below the reach of the surface depletion region and thus the current flow

is never reduced by surface states, even when the gate is forward biased. A drawback for recessed gate architectures is that the recess reduces the isolation between gate and drain, which increases the risk of instability due to feedback. Dual recess geometries are commonly used in GaAs devices that trade-off the width of a deep and a shallow recess to compromise between gate and drain isolation and reduced dispersion. [10].

However, the same benefits are harder to achieve in GaN HFETs, where electrons trapped in surface states can still affect the channel by cancelling out the piezoelectric charge and thus depleting the channel. Additionally, the top AlGaN layer is very thin (in the order of 25 nm) and a well controlled selective etch is difficult with the physical hardness of the material. Some groups (most notably those at The University of California in Santa Barbara) have demonstrated some encouraging results using a deep recess through a thick graded AlGaN cap layer [16]. Recessing through a cap layer may allow recessed GaN architectures to become more common, since the cap layer will protect the un-gated surface areas from damage. This is vital for the success of the technique, since the spontaneous and piezoelectric nature of the GaN HFET channel doping makes the device highly sensitive to surface imperfections. Processing challenges remain if precisely timed, low damage etches are to be consistently achieved. An example recessed gate architecture through a cap layer is shown in Figure 2-4.

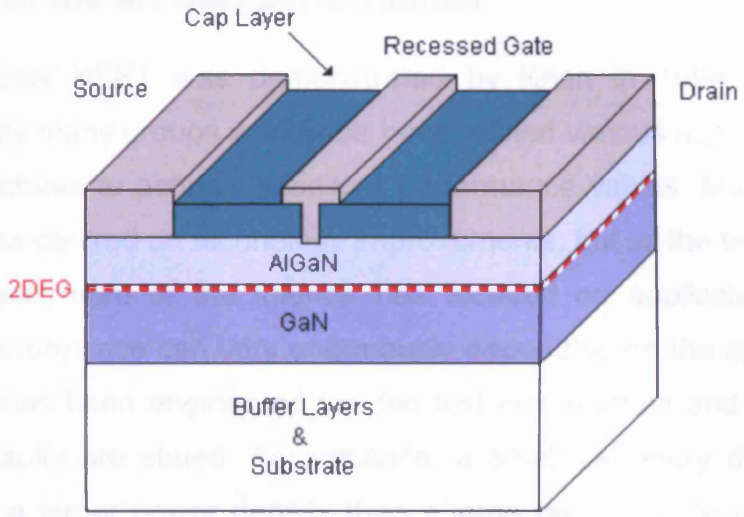


Figure 2-4 Diagram showing a simple GaN HFET with the gate recessed into the AlGaN through a cap layer

2.4.5 Future outlook

The field of GaN HFET growth and processing remains an active research topic, and improvements in device performance continue to be reported as refinements in growth and processing procedures are made. Some of the current state of the art performance results are presented in the next section.

2.5 State of the art GaN performance

The first GaN HFET was demonstrated by Khan in 1994 [17] and subsequently many groups worldwide have refined various aspects of the device structures to achieve excellent performance values. Much of the literature has centred on technology improvements, but as the technology has stabilised more of the interest has focused on applications. The reported performance can vary enormously depending on the application the device has been engineered for, the test environment and even the way the results are stated. For instance, a small periphery device will likely have a larger power density than a large periphery device, which has more heat to dissipate when delivering the same power density. This section aims to provide a snapshot overview of the current state of the art results in what is still a rapidly developing field of research.

The highest operating powers reported for GaN devices tend to be measured at reasonably low frequencies and at large drain bias values, to facilitate large output voltage swings. The highest reported powers are around 1 kW for pulsed operation, running at 1.5 GHz from a 65 V rail [18]. If the maximum power density is used as the metric of performance, the highest reported levels are above 40 W/mm at 4 GHz using drain bias values above 130 V [19]. At higher frequencies the power levels roll off but record high frequency power performance stands at 13.7 W/mm at 30 GHz [20]. Often these highest reported values are recorded using "lab-queens" or "hero devices" which are the top percentile of a given manufacturing process and are measured in extreme conditions that result in rapid stressing and even catastrophic failure. More typical power levels for commercially available parts operating in civil communication bands are 4-5 W/mm from approximately 30 V rails at power levels ranging up to approximately 100 W.

Other typical amplifier metrics such as gain, efficiency and linearity are largely a function of the application - in particular the operating frequency,

required bandwidth of operation, modulation scheme and circuit topology. Although this makes individual publications difficult to compare, a brief summary of the advantages GaN devices in some common applications is included below.

Some of the most impressive amplifiers utilising GaN take advantage of the ability to operate with high efficiency over a wide bandwidth. A notable example using Cree's 28 V rated process for broadband applications is the reference design presented at IMS 2008 which is capable of delivering greater than 45 % drain efficiency at saturated powers above 75 W between 0.5 GHz to 2.5 GHz [21]. Similarly, class J results from Wright et. al. demonstrate the ability of a 10 W GaN transistor to be operated between 60 % and 70 % drain efficiency across a bandwidth of 1.35 GHz to 2.25 GHz [22].

More narrowband high power applications of GaN parts can be broken down into two categories. Firstly, saturated power applications where a harmonically tuned device is pushed into saturation to achieve high efficiency with little concern for linearity. Good examples of this type of amplifier are participants in the IMS student high efficiency PA competition, where drain efficiencies well into the eighties are facilitated by GaN device technology [23, 24].

The other category involves more complex PA architectures such as the Doherty amplifier or envelope tracking where the GaN device is geared towards use in a particular communication standard. Here a signal with a given peak to average ratio must be accommodated, resulting in an average efficiency lower than the possible peak efficiencies. In addition the amplifier must be tuned such that it is sympathetic to digital predistortion algorithms in order to meet spectral mask constraints, which often leads to lower efficiencies again. For instance, an envelope tracking amplifier using a GaN device was able to maintain 50.7 % power added efficiency for a 7.67 dB peak to average ratio 5 MHz W-CDMA signal at

37.2 W average power [25]. Alternatively, the work presented by Delft University of Technology demonstrates a 100W peak power three-way asymmetric Doherty with a power added efficiency greater than 60 % maintained over an exceptional 12 dB back-off range [26].

2.6 Overview of key problems in GaN HFETs

GaN HFETs are complex and expensive devices to grow and process and consequently many foundries have struggled to reliably produce transistors achieving the material system's full potential. As a consequence, device technology problems leading to poor RF performance persist in GaN based devices that have already been reduced to manageable levels in more established material systems. In this section an overview is presented of the key problems still affecting GaN HFETs.

2.6.1 DC-RF dispersion, current slump or knee-walkout

The most serious problem in GaN devices has historically been the DC-RF dispersion seen in the device IVs over varying frequency. This phenomenon has been ascribed various names such as DC-RF dispersion, current collapse and the knee-walkout effect [27]. However, the terms all describe a similar behaviour characterised by the slump seen primarily at the knee region of the device IV plane between the RF and DC behaviour. The slump in RF behaviour worsens with increasing drain bias voltage and acts to limit the RF power capabilities of the devices.

The general belief is that the measured dispersion in GaN HFET structures is caused by electron trapping in the vicinity of the gate. Trapping has been proposed to occur by leakage from the gate into either the AlGaN barrier layer or onto the semiconductor surface on the drain side of the device [28], or by the trapping of hot electrons accelerated out the channel and into bulk traps [29, 30]. The process is exacerbated by the high operational drain bias voltages in many GaN applications, which exert a large electric field at the drain side of the gate edge. A diagram showing the likely locations of electron trapping in GaN HFETs can be seen in Figure 2-5 below.

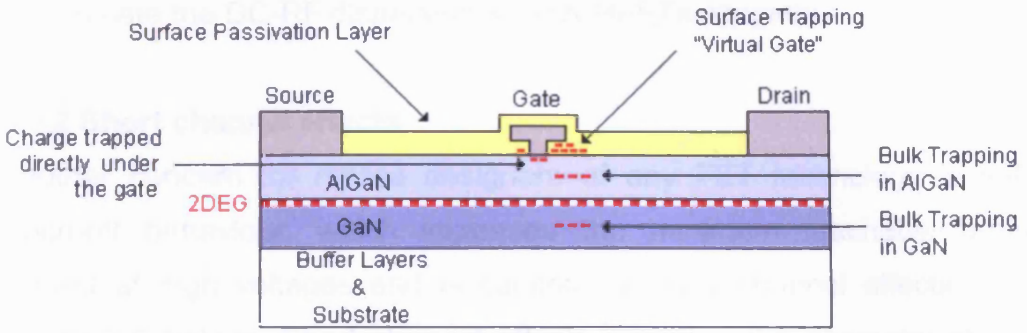


Figure 2-5 Diagram showing a simple GaN HFET structure marked with the likely trap locations, after Meneghesso *et al.* [31].

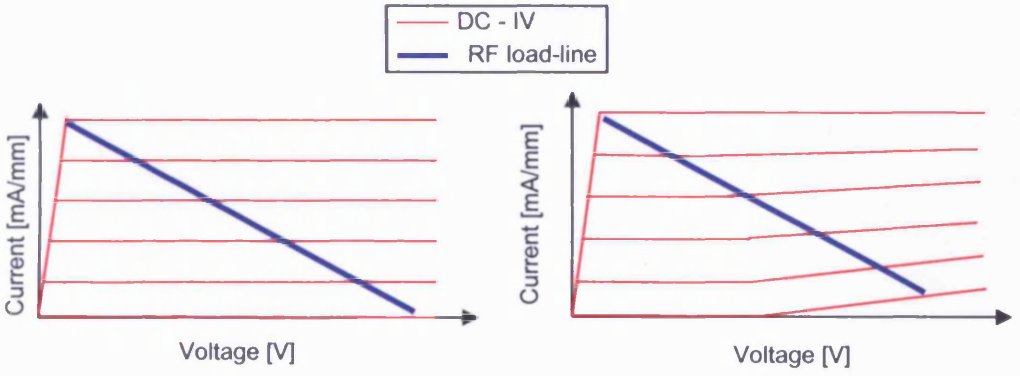
GaN devices have been shown to be highly sensitive to different surface preparation and passivation techniques, suggesting that trapped surface charge has a significant role in the dispersion [12]. Furthermore, the scanning Kelvin probe microscopy technique has been used to measure changes in surface potential as a function of distance away from the gate in stressed GaN HFETs [32]. The results of this study show that electrons are able to migrate along the surface of the device up to 1.0 µm away from the gate, depending on the electric field stress.

The accumulation of electrons into a region of trap states on the device surface is believed to lead to the "virtual gate" effect, whereby the trapped electrons generate an electrostatic charge which acts to partially deplete the conducting channel [33]. The consequence of the extended depletion region is an increase in the access region resistances, resulting in less current available in the active channel and reduced RF output power. In general it is found that the effect is to increase the source, and especially the drain resistance, rather than to increase the channel resistance under the gate [34, 35]. The behaviour of the current through these depleted regions has been described using a space-charge-limited current model [36]. This analysis has led to successful modelling of current collapse affected GaN HFET devices for use in circuit simulators using analytical

equations derived for compact models [37]. However, it remains desirable to eliminate the DC-RF dispersion in GaN HFETs altogether.

2.6.2 Short channel effects

Another concern for device designers of any FET technology is soft pinch-off behaviour, which increases the minimum reachable drain current at high voltages and is caused by short channel effects (see Figure 2-6 below). Short channel effects occur as the geometry of the control electrode (the gate) becomes comparable to that of the channel depth the electrode is attempting to deplete. Essentially the depletion region becomes too small to fully stop electrons tunnelling either through it or under it and flowing through the underlying buffer layers [38]. This is a significant problem in GaN HFETs, where a combination of small gate lengths ($L_g \approx 0.25$ µm are typically required for X-band operation) and RF voltage swings exceeding 100 V can make devices vulnerable to short channel punch through effects, which in turn lead to greatly reduced efficiency performance in RF amplifiers [39].



(a) Ideal device (b) Device with short channel effects

Figure 2-6 Simplistic diagram showing the DC output characteristics of an ideal FET device (a) and one suffering from short channel effects (b). The trajectories of RF load-lines are shown for both cases, highlighting the potential loss in RF output power and efficiency for case (b) caused by the poor pinch-off behaviour.

2.6.3 Reliability issues

A further problem for a new semiconductor technology is the demonstration of robust performance and reliability over a life-cycle

suitable for the end-use application. This is a particular concern for GaN, where many of the envisaged applications have particularly stringent reliability ratings, for instance military and space projects. Reports of GaN HFET degradation characteristics measured using standard techniques such as lifecycle tests monitoring device performance over an extended operating time have become increasingly common as the technology approaches maturity [40].

The damage is largely believed to be caused by hot-electrons accelerated out of the channel and into surrounding interfaces and layers. The resulting defect generation and trapping is thought to gradually deplete the conducting channel and reduce the available current [41]. Another potential degradation mechanism that has been identified is associated with strain relaxation and piezoelectrically induced stress creating lattice defects [42]. This process is also believed to result in reduced channel current and consequently reduced RF output power.

2.7 Standard characterisation methods

Given the issues affecting GaN HFETs, it is important to characterise their individual effects early in the device development cycle, so that the effect of different processing steps on improving device performance can be evaluated and successful transistors can be produced. In this section a number of standard RF transistor characterisation techniques are briefly described to provide a basis for the following chapters.

2.7.1 DC testing

There are a range of important DC tests carried out by device manufacturers to characterise devices. For instance, forward and reverse breakdown tests, parasitic access resistance extractions and transfer characteristics. The DC-IV measurement showing the output characteristics is perhaps the most basic description of device performance and is an important starting point for analysing a device. The output IV plane shows the effect of the gate bias on the output current at different output voltages. Each curve is measured at a different gate bias, with the lowest current traces representing the device in a pinch-off state and the highest current trace representing maximum channel current. At low voltages the IV traces are all overlaid on top of one another as the device is effectively working as a resistor because the channel resistance is dominating the output current flow. This region is called the triode region or, as the current approaches saturation, the knee region.

The DC-IV measurement can provide feedback on pinch-off problems, evident in the turn up of the traces at the high voltage, low current end of the IV plane. However, the DC-IV is unable to give information on dispersion problems as it measures the device using DC signals only. The trapping phenomena responsible for much of the DC-RF dispersion are not present in DC measurements due to the response time of the traps. Dispersive features only become visible when the frequency of the

measurement signals exceed the speed of the individual trapping mechanisms (believed to be spread across a region between 100 Hz and 10 kHz in GaN) [43]. It is also difficult to measure DC-IVs of high power devices at high drain voltages and gate voltages near to the open channel condition, as large currents flow and the device is at risk of break down. In addition, the DC traces in the upper parts of the IV plane become unrepresentative of RF device behaviour due to the increased level of self heating occurring in a static measurement which would not occur under RF excitation. Figure 2-7 shows DC-IV curves for a 250 µm periphery device.

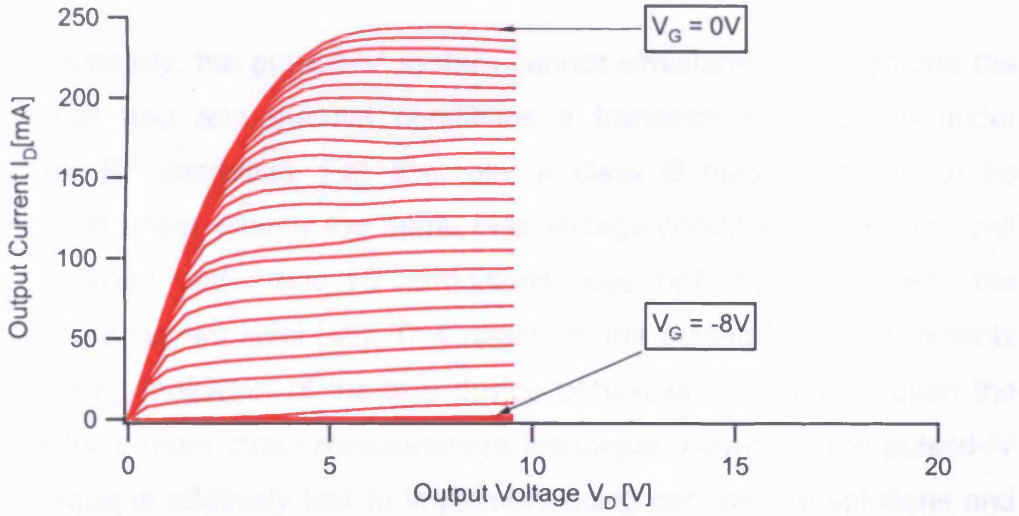


Figure 2-7 Measured DC-IV curves for a 250 µm periphery GaN HFET taken from V_G = -8 V to 0 V in 0.25 V steps.

2.7.2 Gate and drain lag measurements

In the past DC-RF dispersion and other GaN problems have been examined with gate and drain lag measurements [44, 45]. These measurements investigate device trap responses by looking at transient responses of either the gate or drain terminals to step impulse signals. The effects of surface and bulk trapping have been separated by these measurements and if a sufficiently high resolution system is used trap response time constants can be measured [27]. However, the

measurements can be susceptible to misleading artefacts and are not intuitively useful for circuit design.

2.7.3 Pulsed-IVs

Pulsed-IV measurements solve many of the problems of the two previous techniques, effectively by combining them. By pulsing to the necessary areas of the IV-plane from a quiescent bias point at speeds which are too fast for trap and thermal effects to alter during the measurements, a pulsed-IV measurement allows an IV plot of the device in a trap and thermal state set by the quiescent bias point, and is thus capable of demonstrating bias related slump problems.

Unfortunately, the pulsed-IV system cannot simultaneously replicate the identical trap and thermal conditions a transistor experiences under regular RF excitation. For example, a class B bias point cannot be achieved under exactly the same bias voltage conditions, since the self bias current under true RF conditions does not correspond with the quiescent current level [46]. This results in the pulsed-IV measurements only being indicative of the true device behaviour, and leaves open the need for a more direct measurement technique. However, the pulsed-IV technique is relatively fast to implement using commercial solutions and can be used very successfully to measure trends in behaviour and even to extract compact device models. Figure 2-8 shows a pair of pulse-IVs for a single device measured at different bias points. It is clear that the effect of bias conditions are drastically altering the measured response.

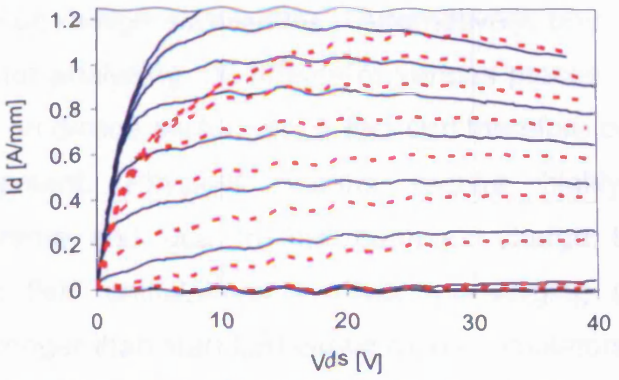


Figure 2-8 Pulsed-IVs measured from V_G = -6 V to +2 V in 1 V steps from two static bias points: V_G = 0 V, V_D = 0 V (full line) and V_G = -3 V, V_D = 30 V (red dashed line). All measurements were made with a pulse length of 1 µs and a pulse separation of 1 ms [47].

2.7.4 Small-signal RF testing

Another common technique for analysing RF amplifiers is to use their S-parameters [48]. The technique involves measuring transmitted and reflected travelling voltage waves using a sinusoidal stimulus small enough for the device to remain in its linear response region. The travelling waves can be converted to four S-parameters if the device is a two-port, as is the case in most RF amplifiers. The four S-parameters can then be processed and used for analysis of device gain, f_T, stability, capacitance extraction and model generation. S-parameters themselves are a linear mapping of behaviour at a specific frequency and cannot be used to describe device behaviour when the device is driven into nonlinear operation. However, it is possible to collate S-parameters at a range of bias conditions and develop non-linear models of transistors that are extremely useful for RF PA circuit design. Two main types of nonlinear models developed from S-parameter measurements are behavioural models, such as the Root model, or compact models that use the measurements to fit functions that describe various components in an equivalent circuit.

2.7.5 Physical modelling

Compact or behavioural models of transistors are typically created after the device has been fabricated to allow the device performance to be

replicated in circuit design simulations. Alternatively, physical modelling is a useful tool for analysing the effects of various processing steps and layer structures on device performance and can therefore be used during device development. Physical models require highly specialised computer programs and due to the complex charge transport and electromagnetic field calculations involved converging on simulation results take far longer than standard circuit model simulators.

Although physical modelling is not strictly a characterisation technique, since real devices are not actually measured, it can provide invaluable insight and allow for the testing of a hypothesis in a more controlled experimental environment than is often possible in real world transistor processing. Consequently it is another useful tool for understanding the causes of specific effects in GaN HFETs, and is particularly valuable given the economic expense of GaN wafer runs.

2.7.6 Large-signal RF testing

Since efficiency constraints require many RF PAs to operate in non-linear modes, large signal measurements are vital for quantifying performance as well as for validating and developing models. A large-signal, in the context of RF PAs, is a signal that drives the device outside of the operating regime where linear S-parameters are accurate. Essentially, above a certain power level a device will no longer be able to linearly transfer the input signal into an exact but larger copy at the output. When a device reaches the limits with which it can linearly amplify the input signal it begins to distort the input signal and create energy at harmonically related frequencies. S-parameters only consider single frequency mapping and so S-parameters alone are not able to accurately describe the device behaviour in this regime.

Scalar RF large-signal output power measurements are commonly undertaken in RF labs to measure transistor performance upto and including non-linear operation. A typical scalar large-signal measurement

sweeps the input power whilst measuring the corresponding output power, gain and efficiency as the device is driven into compression. Compression refers to the process when an increase in input power ceases to yield a corresponding size increase in output power and can be seen in Figure 2-9 below.

These tests can be performed with single tone, two-tone or complex modulated signals depending on the application and the test requirements. Quantifying the changes in magnitude and phase of the fundamental signal as the device is driven to compression is one way of measuring amplifier distortion known as AM-AM (amplitude modulation to amplitude modulation) and AM-PM (amplitude modulation to phase modulation). The complimentary technique is to measure the distortion tones generated away from the fundamental, typically the third order output intercept point (OIP3) is used as a figure of merit based on a two-tone test as it is usually the third order inter modulation product (IM3) which is the dominant distortion. For more complex modulation schemes various measures of spectral leakage can be performed to quantify the out of band distortions such as Adjacent Channel Power (ACP) and Adjacent Channel Leakage Ration (ACLR).

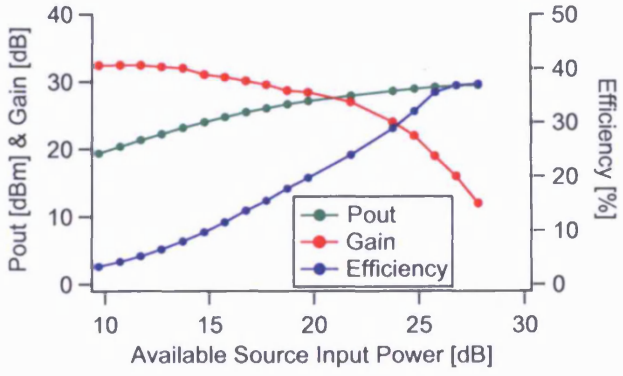


Figure 2-9 – Typical scalar RF power sweep results for a 2x50 µm GaN HFET device biased in class A and measured at 1.8 GHz. The compression is evident as gain reduces.

Although such scalar measurements as those shown in Figure 2-9 can quantify non-linear device behaviour they are often insufficient for accurately determining the cause of the underlying device phenomena. For instance, DC-RF dispersion in GaN HFETs cannot be satisfactorily measured using scalar power sweeps because the RF swing can be limited not only by the knee-walkout but also by other effects, like the pinch-off behaviour of the device and the load-line trajectory. Without evidence that the RF swing is being limited by dispersion at the knee region and not by another effect, it is often difficult to attribute the device's output power behaviour specifically to a single effect.

More sophisticated large-signal RF testing is often employed for characterisation of non-linear amplifier performance. Load-pull benches that are able to present different load and source impedances to the device under test are commonly employed, as the performance of power devices is typically a function of the impedance environment. In addition, it is ultimately desirable to relate the large-signal performance back to device level parameters to track the underlying causes of the device performance, namely current and voltage in the time-domain. Non-linear large signal measurement systems will be discussed in more detail in the next section.

2.8 The need for time-domain characterisation

2.8.1 Measuring waveforms at RF frequencies

In order to measure and understand what is actually happening in a high frequency device, the truest solution is to use time-domain waveform measurements that show categorically how the device is behaving under real RF stimulus. Using a time repetitive signal as the stimulus and employing a sub-sampling approach, it is possible to reconstruct measured waveforms at GHz frequencies using commercially available sampling instruments. Measured input and output IV waveforms at a DUT terminal can be reconstructed using couplers to sample the incident and reflected voltage travelling waves (termed *a* and *b* waves respectively). Given knowledge of the impedance environment (Z_0) these directional travelling waves can be converted to current and voltage using the following relationships:

$$i = (a-b) / \sqrt{Z_0} \qquad (2\text{-}1)$$

$$v = \sqrt{Z_0}\,(a+b) \qquad (2\text{-}2)$$

This technique for waveform capture has now become widely accepted in the industry [49] and accurate results can be obtained thanks to successful application of suitable calibration procedures [50]. All waveform results presented in the remainder of this thesis are, unless stated, measured on wafer and calibrated up to the device plane at the RF probe tips using real RF continuous wave (CW) stimulus. The four current and voltage waveforms of a two-port transistor device (input IV and output IV waveforms) provide the majority of information necessary to fully analyse transistor performance. The waveforms presented in this thesis will be plotted against phase in degrees relative to the fundamental frequency of the CW stimulus, allowing waveforms of varying fundamental frequency to be easily analysed on a per cycle basis.

The time-domain technique is especially important as the device is driven into non-linear operation and the waveforms contain energy at multiple frequencies, and are no-longer simple sinusoids. Here the time domain technique captures the phase relationship between different frequency components, important information that is overlooked by some other techniques, such as spectrum analysers.

2.8.2 Waveform engineering

In addition to measuring waveforms it is also useful to be able to interact with the waveforms in order to alter the performance of the device – a process known as waveform engineering. Waveform engineering allows for flexible and intelligent measurements to be conducted and can be achieved through bias control and impedance manipulation. Changing the impedance environment of the device is usually achieved in one of two main ways: by using passive tuning or through carefully controlled active load-pull setups.

Automated mechanical passive tuners typically consist of a conducting line between two ports where one end will be connected to the DUT and the other end to a passive load. The reflection coefficient presented to the DUT is altered using the position of a perpendicular probe relative to the centre conductor. The probe interacts with the fields around the centre line, changing the resonance of the structure and ultimately allowing for a good coverage of reflection coefficients, depending on the frequency of operation and the dimensions of the tuner model. This behaviour is summarised in Figure 2-10 below.

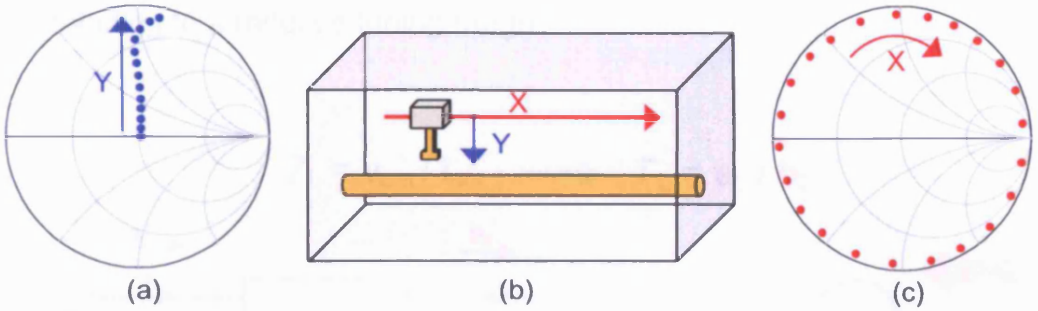


Figure 2-10 – (b) shows the simplified structure of a passive load-pull tuner, where a probe hangs above a centre conductor and is able to move in vertical or horizontal directions. (a) and (c) show the corresponding effects of vertical and horizontal probe movement on the tuner reflection coefficient presented to the DUT.

Passive load-pull systems are only capable of generating reflection coefficients within the Smith chart due to the finite losses that must exist between DUT and tuner when reflecting the signal back. This limitation is particularly damaging in a time-domain measurement system, where couplers and their associated losses are required either side of the DUT and further hamper the achievable reflection coefficients. Additionally, multi-harmonic passive tuning becomes awkward, due to the extra losses in frequency multiplexing components or the complexity of a cascaded tuner architecture [51].

Active load-pull overcomes these problems by terminating the output travelling wave in a non-reflective load and generating a reflected wave of appropriate magnitude and phase using a signal source to present the device with the reflection it would expect to see in a given impedance environment. The active load-pull concept is illustrated in Figure 2-11 below. The active nature of this system lends itself to overcoming any system losses and is therefore capable of achieving reflection coefficients outside of the Smith chart [52]. Importantly for waveform engineering, multi-harmonic active load-pull is significantly easier to achieve than in a passive system, as active loops can be added beyond a frequency

selective multiplexer without concern over the loss of such components contributing to a reduced tuning range.

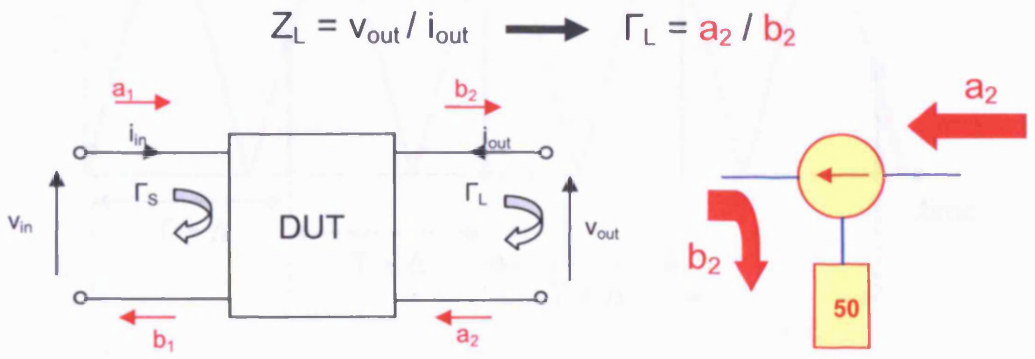


Figure 2-11 – Diagram shows the important relationship at the centre of active load-pull, which links the load impedance seen by the DUT to the ratio of a and b travelling voltage waves at the device output. By using a circulator it is possible to absorb all of the device's natural b_2 wave with no reflection, whilst sending back an a_2 wave whose magnitude and phase are set by a computer algorithm. The result is the ability to synthesise an infinite range of impedance states.

2.8.3 Time-domain measurement systems at Cardiff University

The time domain waveform measurement systems used in this thesis operate using either an Agilent 70820A Microwave Transition Analyser (MTA) or a Tektronics Digital Serial Analyser (DSA) as the sampling instrument [49, 50]. The system uses a sub-sampling technique, whereby multiple RF cycles are sampled using a periodic trigger delay to gradually build up an RF waveform. It is essential to have a time repetitive signal for this technique to accurately recreate the waveform. The sub-sampling concept is demonstrated in Figure 2-12 below.

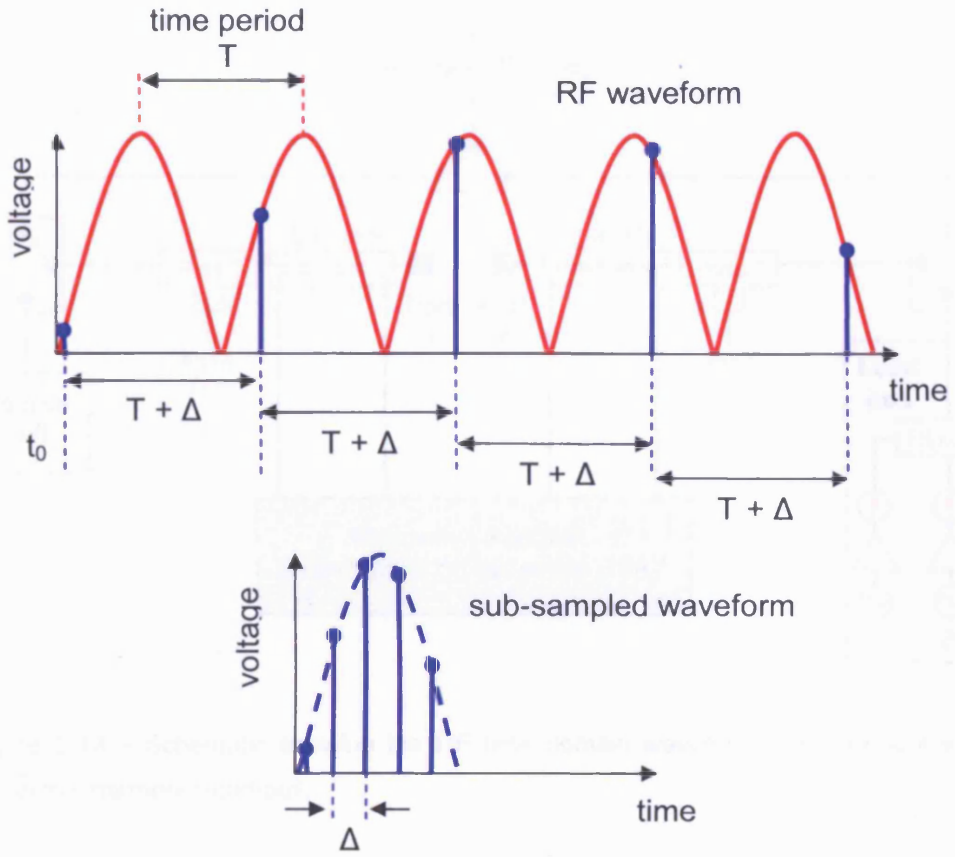


Figure 2-12 – Diagram showing the sub-sampling concept, whereby the trigger samples periodically at a frequency offset to the fundamental frequency component of the signal being measured, and builds up an image of the RF waveform over multiple cycles.

In the realised measurement system, a sweeper or broadband signal generator is used at the source to provide input power at the fundamental frequency and to allow broadband calibration. Active harmonic load-pull loops are built up where necessary to present the device with a range of loads and provide the capability for waveform engineering up to the third harmonic. The whole system is computer controlled through a flexible user interface. Figure 2-13 shows a diagram of the system architecture.

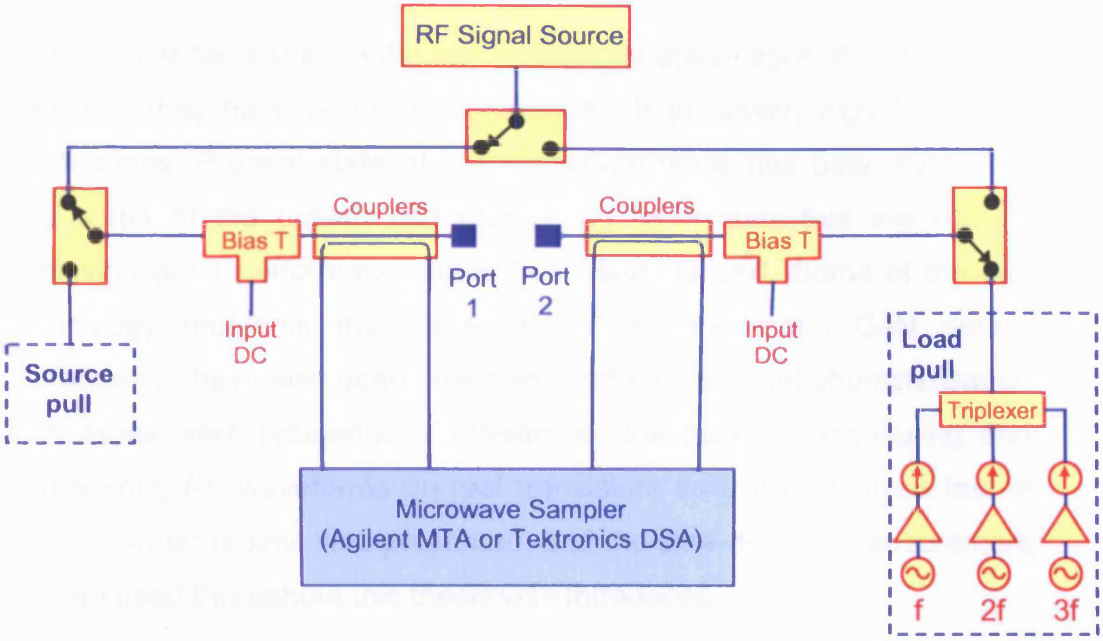


Figure 2-13 – Schematic showing the RF time domain waveform measurement system with active harmonic load-pull.

The time domain measurement system is capable of measuring waveforms at different power levels, bias voltages, harmonic impedances and frequencies. As a result, the system is extremely versatile and can capture a wealth of data about transistor and amplifier performance. The device can be presented with specific impedance environments using multi-harmonic active load-pull, rapidly emulating matching networks. The system is also capable of measuring modulated signals, so long as they are time repetitive. However, for the results presented in this thesis only continuous wave (CW) stimulus is deemed necessary, as the majority of results are geared towards investigating transistor performance in terms of device functionality, as opposed to measuring system level performance of the completed amplifier.

2.9 Summary

This chapter has explored the key technology advantages of GaN HFETs and why they have been investigated for high power, high frequency applications. Present state of the art performance has been evaluated and some of the growth and processing techniques that are vital to achieving good performance have been summarised. Some of the key technology problems that have limited developmental GaN device performance have also been described and the standard characterisation techniques were presented. Furthermore, the case for measuring and engineering RF waveforms on real transistors as a vital analysis tool in the non-linear regime was presented, and the time-domain measurement system used throughout this thesis was introduced.

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Chapter 3 - GaN HFET Characterisation using RF Waveforms

3.1 Introduction

In this chapter, time-domain RF waveform measurement and engineering techniques are employed for the analysis of GaN HFETs supplied by QinetiQ Ltd. Problems such as short channel effects, DC-RF dispersion and degradation are examined in detail. The capture of RF waveforms allows direct measurement of these effects and can therefore validate other indirect techniques such as pulsed-IV measurements and physical modelling. The results have been used to draw conclusions about the effects of specific device fabrication steps, and have been shown to be useful for feeding back into, and improving the device design process. The chapter includes a discussion of a physical simulation developed at QinetiQ to explain the measured DC-RF dispersion that provides a unique insight into the origins of the effect [1]. The measured waveform results can also, in their own right, provide a useful visualisation tool for such device level issues, allowing for the identification of trends and the observation of unique behaviours [1]. The first use of RF waveform measurements to analyse device degradation over time is presented,

showing how the waveforms can help draw conclusions about the mechanisms involved [2].

3.2 Standard waveform characterisation techniques

Analysing the four waveforms of a two-port transistor device (input IV and output IV waveforms) provides significant information on transistor performance, especially as the device is driven into non-linear operation and the output waveforms become distorted (harmonically rich). Figure 3-1 shows the waveforms measured for a GaN HFET driven into non-linear operation.

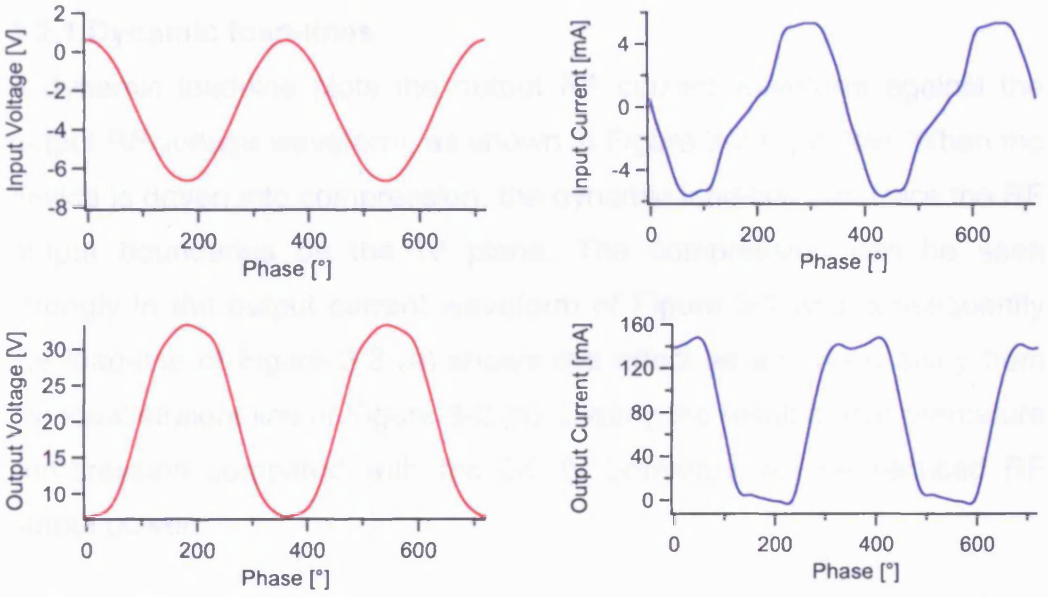


Figure 3-1 The four measured waveforms (input IV and output IV) for a GaN HFET measured at 1.8GHz, biased at V_D=20V and V_G=-3V (class A) into a fundamental impedance of 150Ω

Examining the waveforms shown in Figure 3-1, the measured input voltage waveform is a uniform sine wave. This is as expected, since it is simply connected to the source signal generator. The input current shows artefacts due to the diode turn-on characteristic and the input capacitance of the device. The output current, and to a lesser degree the output voltage waveforms show compression as they reach and trace out the IV boundaries of the transistor. It is possible to infer a significant amount of information from the measured waveforms from a single spot measurement such as those shown in Figure 3-1. However, more

valuable analysis is often possible when the waveforms are processed or if a greater range of data is collected.

Processing the waveforms can often aid analysis, for instance plotting dynamic load lines, dynamic transfer characteristics and dynamic input characteristics or source lines. These plots are briefly introduced below to clarify their use elsewhere in the chapter.

3.2.1 Dynamic load-lines

A dynamic load-line plots the output RF current waveform against the output RF voltage waveform, as shown in Figure 3-2 (a) below. When the device is driven into compression, the dynamic load-line can trace the RF output boundaries on the IV plane. The compression can be seen strongly in the output current waveform of Figure 3-1 and consequently the load-line of Figure 3-2 (a) shows this effect as a curving away from the ideal straight line of Figure 3-2 (b). Clearly the result of this premature compression compared with the DC-IV boundary will be reduced RF output power.

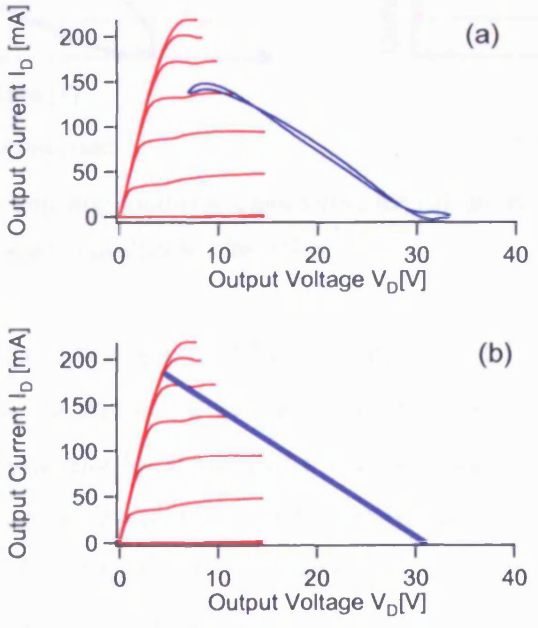
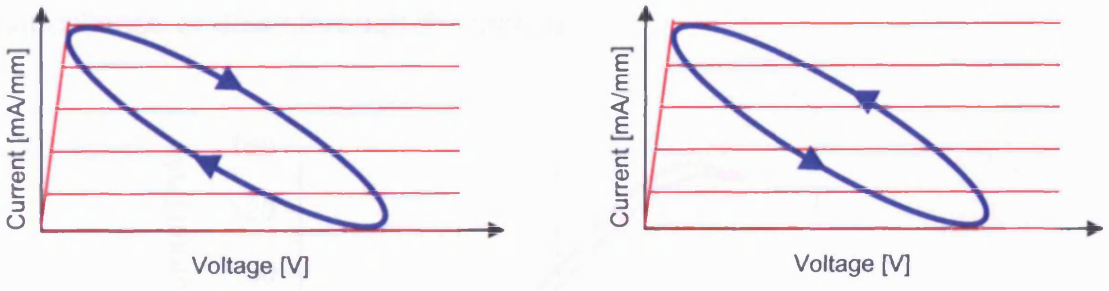


Figure 3-2 (a) Measured output dynamic load-line for the same measurement as in Figure 3-1. (b) Ideal load line without DC-RF dispersion. Both load-lines are overlaid on DC-IVs measured from V_G = -6 V to 0 V in 1 V steps.

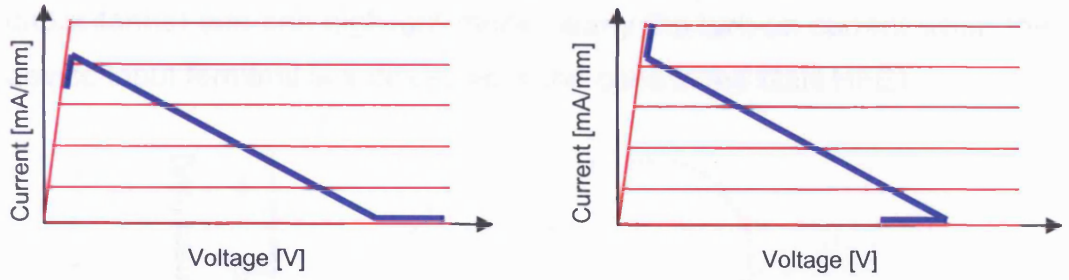
It is possible to see a kink in the DC-IVs of Figure 3-2, which is common to many GaN HFETs and is believed to be caused by slow release electron trapping in the device buffer [3]. The looping seen in the dynamic load-line is caused by the reactive nature of the load-impedance at the measured reference plane. Depending on whether the load impedance is inductive or capacitive the load-line trajectory will loop clockwise or counter clockwise (see Figure 3-3). Although in Figure 3-2 the load presented to the device is almost entirely real, a small capacitive element exists due to the device output capacitance. This is exposed during periods of the RF cycle when the device is in the off region, i.e. saturation or pinch-off. Here the device current generator is not generating current but the output capacitance will result in a parasitic current flow being visible. This effect is more prominent when the device is operating in a reduced conduction angle mode, such as class B, where the current generator is off for a larger fraction of each period.



(a) Inductive Load (a) Capacitive Load

Figure 3-3 Diagram showing load-line trajectories for (a) an inductive load impedance and (b) a capacitive load impedance, after [4].

The direction of the "tails" seen in the dynamic load-lines is dependent on the size of the harmonic impedances relative to the fundamental impedance [5]. Typically for on-wafer measurements of small devices the system impedance is small relative to the fundamental impedance and the load-line "tails" will turn anti-clockwise as in Figure 3-4 (a), but when the fundamental impedance is load-pulled to a value below the harmonic impedances, the compression will cause the "tails" to turn clockwise as in Figure 3-4 (b).



(a) R_L @ f_0 > R_L @ harmonics (b) R_L @ f_0 < R_L @ harmonics

Figure 3-4 Diagram highlighting the effect of higher harmonic impedances on the direction of compressed load-line "tails" [5].

3.2.2 Dynamic transfer characteristics

The dynamic transfer characteristic is a plot of the output RF current waveform as a function of the input RF voltage waveform. An FET can be considered as a voltage controlled current source and this plot shows the current flow in relation to the input voltage cycle. Figure 3-5 shows a measured transfer characteristic plotted from the same waveforms as shown in Figure 3-1. Here the looping is highlighting the trans-capacitance or delay through the device.

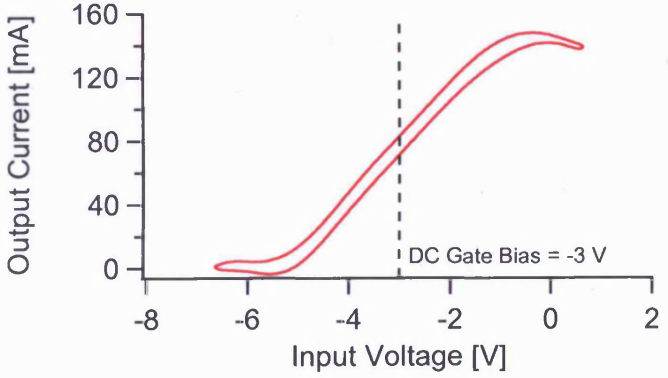


Figure 3-5 Measured dynamic transfer characteristic for the same measurement as in Figure 3-1.

3.2.3 Dynamic input characteristics / source-lines

By plotting the input RF current waveform as a function of the input RF voltage waveform the dynamic input characteristic, or dynamic source lines can be generated. These plots can help visualise the displacement current through the input reactances (usually dominated by the input

capacitance) and can highlight more clearly the turn-on current when the device input terminal is a diode, as is the case in the GaN HFET.

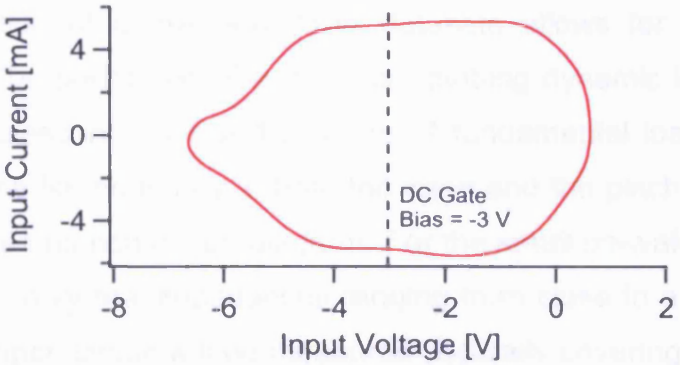


Figure 3-6 Measured input characteristic for the same measurement as in Figure 3-1.

3.3 Dense waveform data collection – the "fan" diagram

3.3.1 Introduction

The collection of dense waveform datasets allows for more detailed analysis to be performed. For instance, plotting dynamic load-lines for a common quiescent point and a range of fundamental load impedances can trace the RF boundary at both the knee and the pinch-off limits. This plot has been named a 'fan'-diagram. For the small on-wafer device sizes tested here, only real impedances ranging from close to a short circuit to almost an open circuit will be measured (typically covering the range 5 Ω < Z_L <1.5 kΩ. A 'fan'-diagram for a single quiescent bias point is shown in Figure 3-7. The compression that marks the RF boundary conditions is clearly visible at both ends of the load-lines – the knee region at low voltages and the pinch-off region at high voltages.

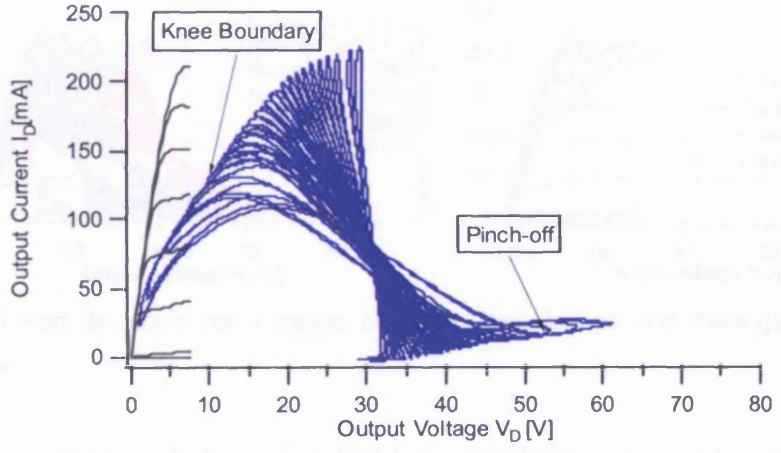


Figure 3-7 A single 'fan' showing load lines for a range of loads at a constant class A quiescent point (V_D = 30 V V_G = -3 V).

3.3.2 Observing unusual device behaviour – the effect of DC bias

As a further development of this technique, the fan diagram measurement can be repeated for a range of drain bias voltages to highlight the sensitivity of the RF boundary to static drain bias in GaN HFETs. In Figure 3-8, load line data probing the RF knee boundary condition of a GaN HFET has been collected at a constant gate bias of V_G = -3 V (approximate class A operation) and at a range of drain bias

points, varied from 5 V to 20 V in 5 V steps. Also shown are tracings of the RF boundary conditions mapped by the load lines.

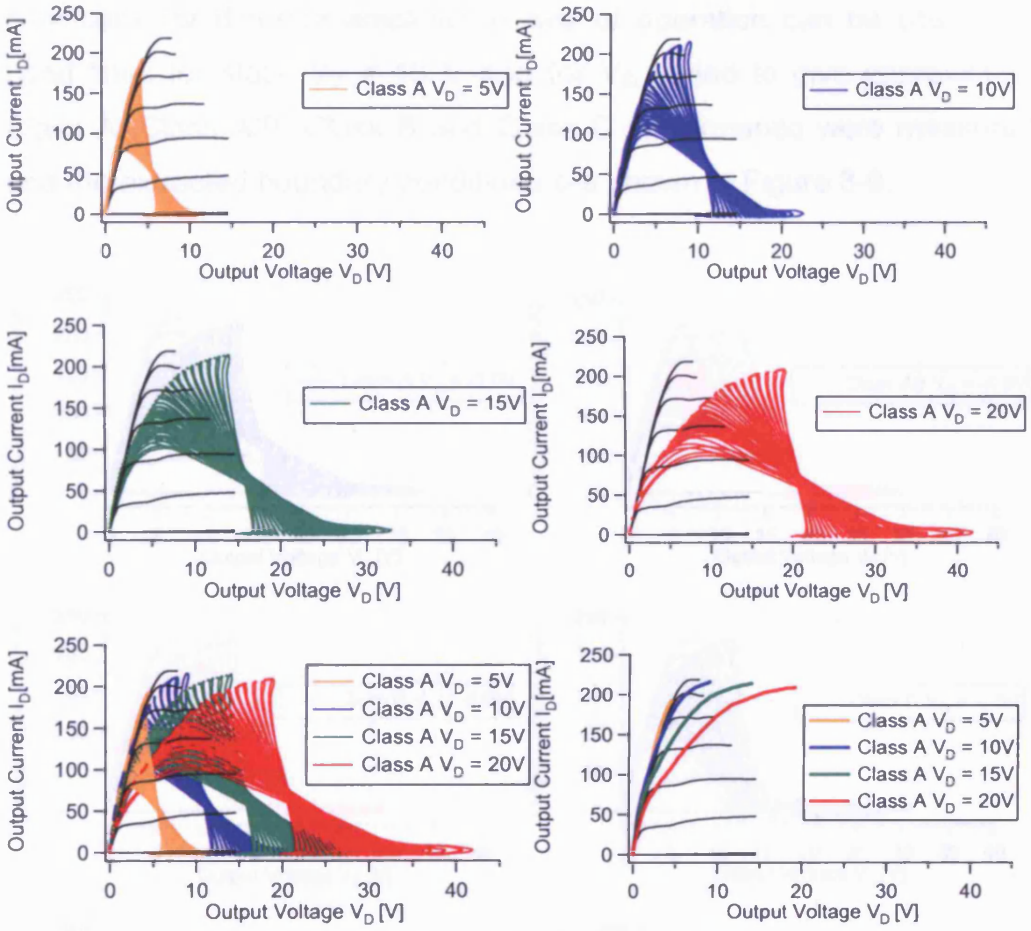


Figure 3-8 Fan diagrams for a range of static drain biases and tracings of the RF boundaries.

The V_D = 5 V trace follows the DC knee and subsequent boundaries for higher drain biases are moving further from the DC knee. This shows a strong link between drain bias and DC-RF dispersion at the knee region, believed to be caused by the higher electric fields on the drain terminal pulling more electrons into traps. The device did not degrade noticeably during the measurements and the effect was too large to be attributed purely to thermal effects. It is also interesting to note that the current collapse is most severe only at the knee region, with less dispersion occurring at lower current densities and into the saturation region.

A similar experiment can be conducted to examine the effects of gate bias on the RF boundary. By collecting similar load line data at a constant drain bias but at different gate bias values, the RF knee boundary conditions for different amplifier modes of operation can be observed. Load lines for static V_D = 15 V and for V_G varied to give approximate Class A, Class A/B, Class B and Class C performance were measured and the extracted boundary conditions are shown in Figure 3-9.

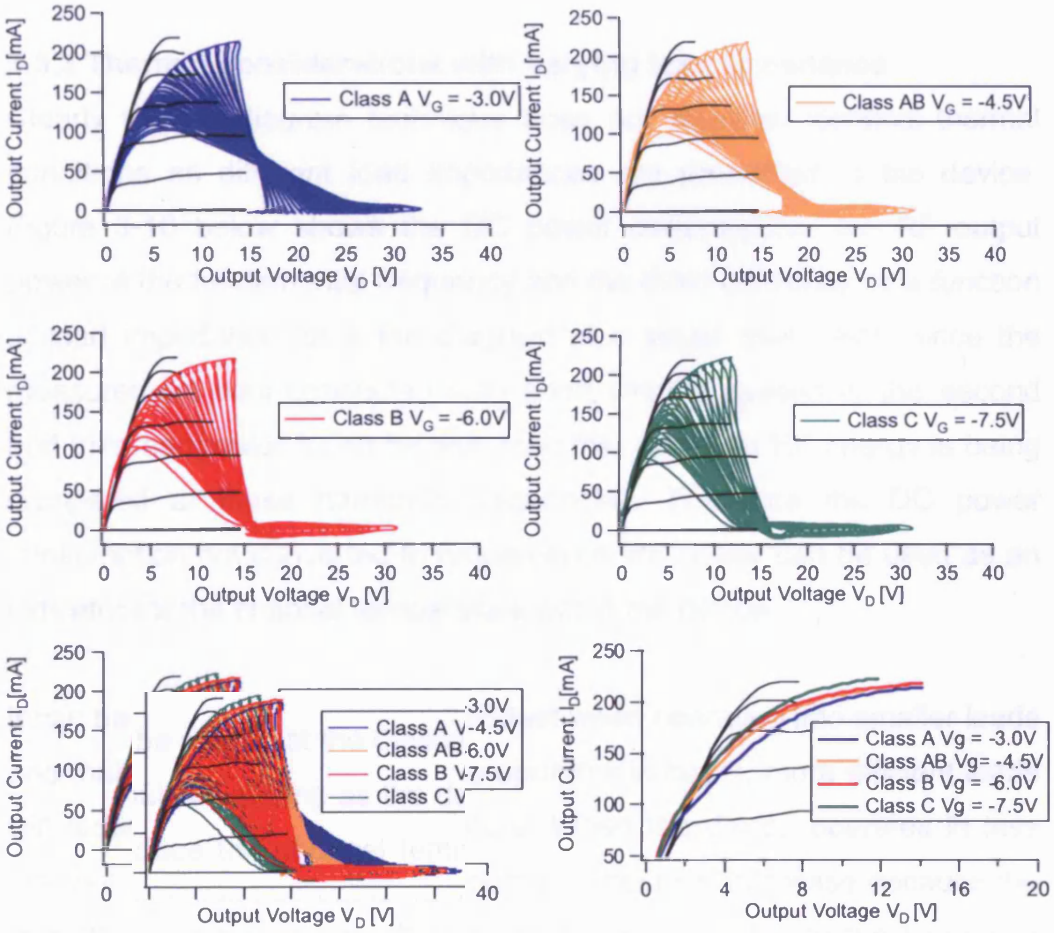


Figure 3-9 Fan diagrams for a range of gate biases all measured at a constant drain bias of 15 V. Also shown (bottom right) is the tracings of the RF boundaries from each mode of operation on a smaller scale to highlight the differences.

Clearly, the dependence on gate bias is not as strong as the dependence on drain bias. However, a trend is apparent; showing some recovery of the knee is possible by operating in higher modes, matching previous

results [6]. It is perhaps debatable as to whether or not this observed result is purely a reduction in thermal effects due to operation in naturally more efficient modes, or a combination of thermal effects with another, possibly trap related factor. In addition, due to the varying gain of the different operating modes it is difficult to maintain exactly the same compression level, making conclusions drawn from this experiment potentially less reliable than the variation of drain bias seen in the previous section.

3.3.3 Thermal considerations with varying load impedance

Clearly the fan-diagram technique does not maintain identical thermal conditions as different load impedances are presented to the device. Figure 3-10 below shows the DC power consumption, the RF output power at the fundamental frequency and the drain efficiency as a function of load impedance for a fan diagram at a single bias point. Since the measurement was conducted with short circuits applied to the second and third harmonics it can be assumed that very little RF energy is being dissipated at these harmonic frequencies. Therefore the DC power consumption not converted to fundamental RF power can be used as an indicator for the channel temperature within the device.

It can be seen that the device is hottest when operating into smaller loads and that RF cooling as the device operates in larger, more efficient loads will reduce the channel temperature. When the device operates in less efficient loads and heats up, the output current will decrease because the mobility of carriers in the channel will be reduced due to the increased scattering. The result on the measurements is similar to that seen in standard DC-IV and pulsed-IV measurements where the high current, high voltage region of the IV plane shows lower currents due to self-heating. However, the current levels measured when probed by real RF signals in the waveform measurement system are perhaps more useful than other indirect measurement techniques, since they are true

representations of the RF current available when operating in the given load and bias condition.

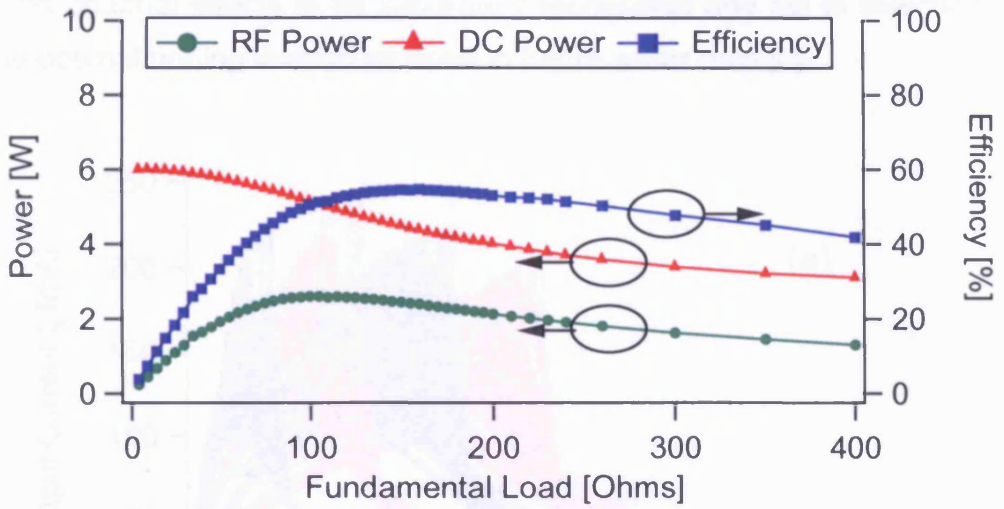


Figure 3-10 RF output power, DC power consumption and drain efficiency vs fundamental load impedance from a fan diagram measured on a GaN HFET in a class AB bias point at V_D = 28V. It is possible to see that the efficiency is very low at small load impedances where there is little RF cooling, from which it can be assumed that the device will be undergoing considerable self heating effects.

3.3.4 Evaluating device processing steps

Fan diagrams can also be a useful tool for evaluating the results of different device processing steps. In one such experiment a batch of five GaN wafers with identical processing except for varying quantities of iron (Fe) doping in the buffer region were subjected to fan diagram characterisation. The iron doping was introduced to combat short channel effects [7]. The aim of the experiment was to find the optimum doping concentration by comparing the pinch-off and knee-walkout behaviour of the devices on the different wafers.

Figure 3-11 depicts the fan diagram results for the control (no Fe doping) and optimally doped wafers. It can be seen that the control sample has poor pinch-off behaviour, which can be observed by the premature limiting of the current swing at high voltages. However, the optimally

doped sample has good pinch-off behaviour and importantly, the knee walkout behaviour in the doped case has not worsened. The fan diagram technique was valuable as it allowed the effects of knee walkout and short channel effects to be separately recognised and led to selection of the optimal doping level to be used in future wafer runs [8].

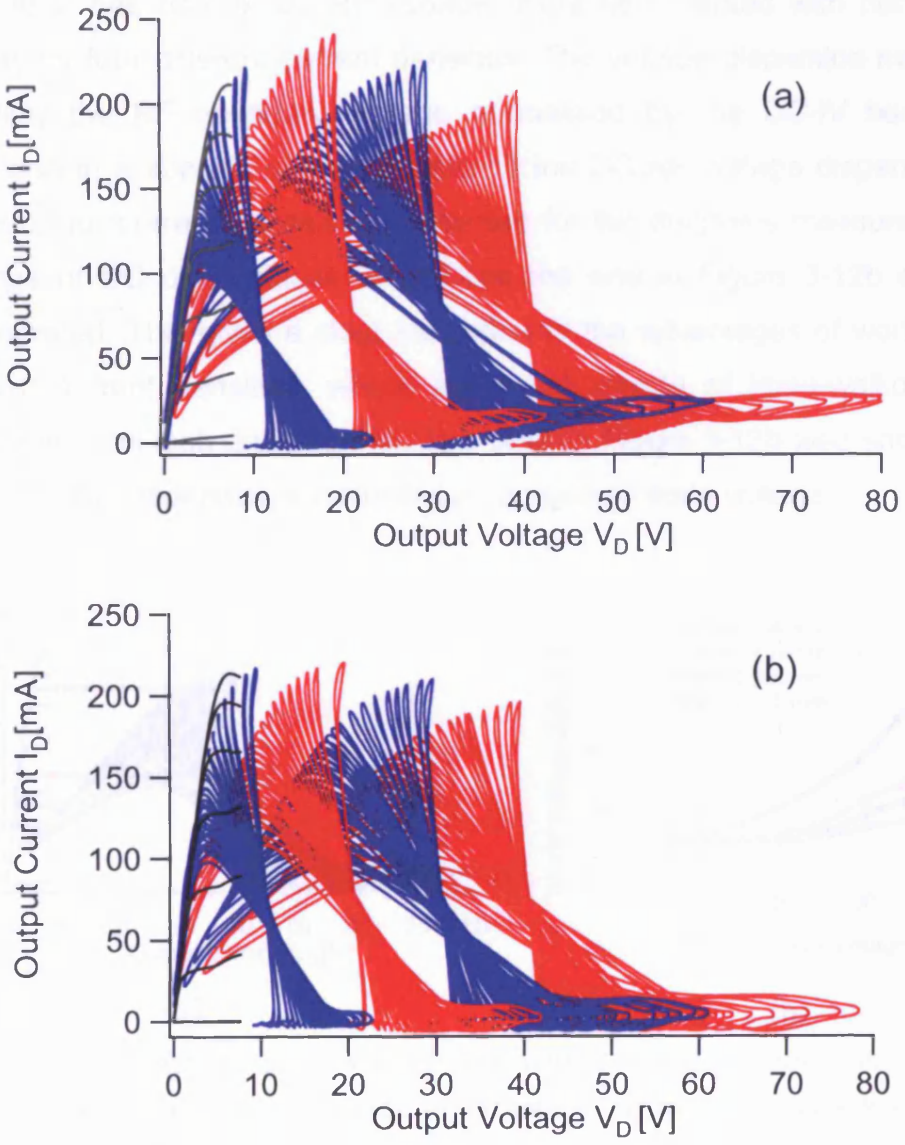


Figure 3-11 Fan diagrams showing the effect of iron doping on the knee and pinch-off regions for (a) control wafer and (b) optimally doped wafer.

3.3.5 Improving amplifier design

Given the observed deterioration in DC-RF dispersion with increasing current densities, it is possible to limit the negative effect of dispersion by deliberately operating at lower current densities. This effect can be investigated by considering only the DC-RF *voltage* dispersion at specific current densities. In Figure 3-12a below, the fan diagram for a drain bias of 40 V has had its DC-RF voltage dispersion marked with horizontal lines for four different current densities. The voltage dispersion metric is simply the RF boundary voltage normalised by the DC-IV boundary voltage at a specific current density. If the DC-RF voltage dispersion of these four current densities is recorded for fan diagrams measured at a range of DC drain biases, a plot like the one in Figure 3-12b can be generated. This gives a clear indication of the advantages of working at lower current densities, where the worst effects of knee-walkout are delayed until high drain biases. The plots in Figure 3-12b also show that the DC-RF dispersion is a non-linear function of drain voltage.

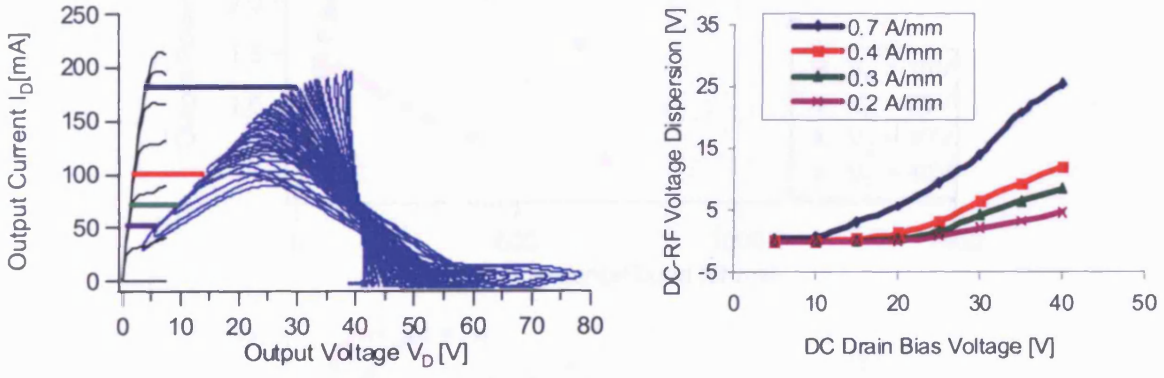


Figure 3-12 (a) 40V fan diagram with DC-RF voltage dispersion metric highlighted for four different current densities, (b) DC-RF voltage dispersion at the same four current densities plotted for a range of drain biases.

If operating at lower current densities allows designers to postpone the worst effects of DC-RF dispersion until higher drain voltages, a design trade-off must emerge where the designer can carefully choose the operating mode to achieve the best performance from GaN devices with

known DC-RF dispersion behaviour. Figures 3-13a and 3-13b respectively show the output power in Wmm^{-1} and the drain efficiency generated for the range of loads presented to the device in the 'fan' diagrams, under different drain biases (all measurements are compressed in approximate class A mode).

The plots show that different operating requirements are needed to maximise efficiency and output power. For instance, the maximum measured output power of 3.5 Wmm^{-1} is achieved only at a drain bias of 40 V into a load of approximately 300 Ω. Unfortunately this mode of operation has low efficiency (~30 %). The highest efficiency of approximately 50 % can be achieved over a range of drain biases, but only if output power is sacrificed (to ~2.5 Wmm^{-1}).

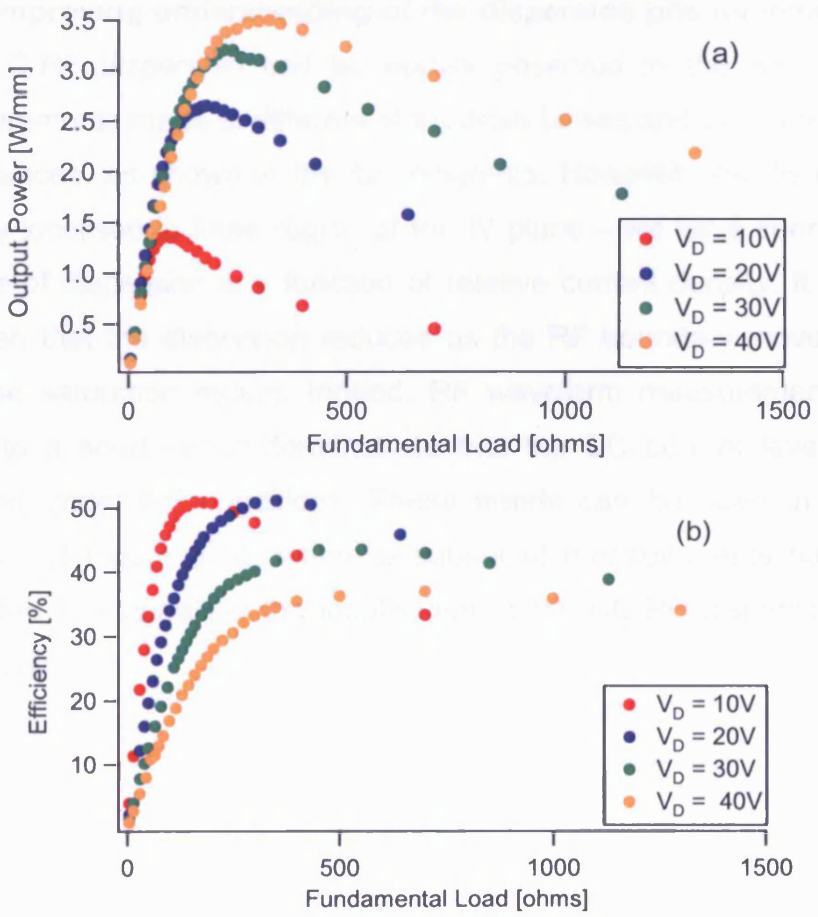


Figure 3-13 (a) Output Power and (b) Efficiency vs Load for Varying DC Drain Bias in GaN HFET

The most efficient performance is found when the device is operated into larger loads, as this means the device is operating in a region where the knee walk-out is less prominent - as demonstrated by the 'fan'-diagrams - and RF voltage swing is not critically impinged. For this mode of operation to be successful however, it is important that the device has good pinch-off behaviour. Otherwise, the benefit of avoiding the worst of the knee-walkout will be counteracted by the reduced current swing at the pinch-off end. However, total output power will be reduced by aiming for lower current densities, even though higher efficiency values will be possible for a given output power. This highlights a significant design trade-off for GaN based devices. An example of the importance of this trade-off in high power, high efficiency amplifier design using GaN will be demonstrated in Chapter 5.

3.3.6 Improving understanding of the dispersion phenomena

The DC-RF dispersion can be readily observed in the RF waveform measurements made at different static drain biases and fundamental load impedances, as shown in the fan diagrams. However, the dispersion is heavily localised to knee region of the IV plane – we have seen that the degree of dispersion is a function of relative current density. It can also be seen that the dispersion reduces as the RF boundary moves further into the saturation region. Indeed, RF waveform measurements made close to a short circuit demonstrate that the DC current level can be reached under RF conditions. These trends can be seen in the fan-diagram of Figure 3-14, where a subset of measurements have been extracted to emphasise the localisation of the DC-RF dispersion at the knee region.

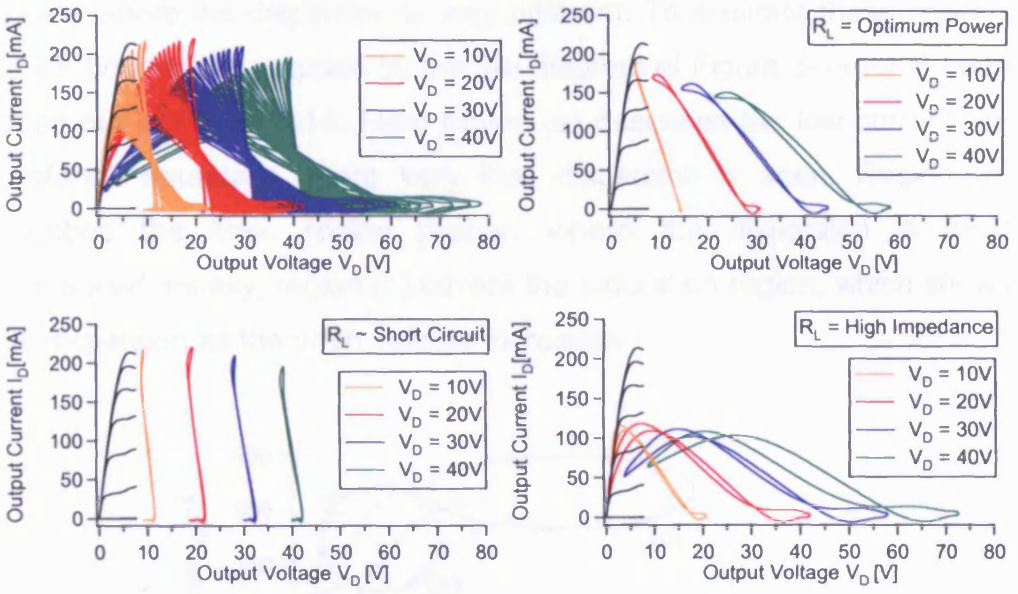


Figure 3-14 Measured RF load-line fan diagrams for four Class A bias points, V_D = 10 V, 20 V, 30 V and 40 V demonstrating increased dispersion with drain bias. Load-lines are overlaid on DC-IVs measured from V_G = -6 V to 0 V in 1V steps. A subset of load conditions are also shown to demonstrate the worse effects of the DC-RF dispersion are localised at the knee region, where R_L is tuned to optimum power. At other extreme load conditions, close to short and open circuits the amount of dispersion is lower.

The same effects can also be seen in the two pulsed-IVs measured on the same device and plotted in Figure 3-15. Here the reduced dispersion at higher drain voltages is more easily observed.

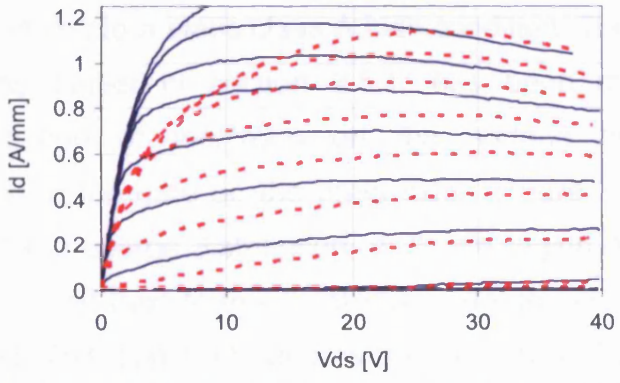


Figure 3-15 Pulsed-IV measurements showing current recovery at higher drain biases. IVs measured from V_G = -6 V to +2 V in 1 V steps from two static bias points: V_G = 0 V, V_D = 0 V (full line) and V_G = -3 V, V_D = 30 V (red dashed line). All measurements were made with a pulse length of 1 µs and a pulse separation of 1 ms.

It is possible to split the RF boundary on the IV plane into three distinct regions where the dispersion is very different. To illustrate these regions the RF boundaries mapped by the fan diagram of Figure 3-14 have been traced out in Figure 3-16. Here region (a) describes the low current on-resistance boundary where very little dispersion is seen. Region (b) describes the knee region proper, where the dispersion is most pronounced. Finally, region (c) covers the saturation region, which shows less dispersion as the drain voltage increases.

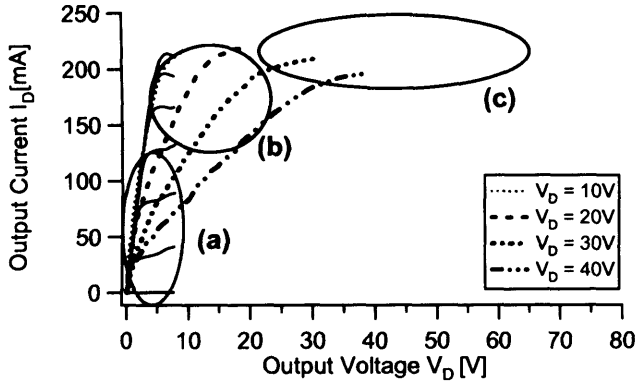


Figure 3-16 RF boundary conditions mapped out by the dynamic load-lines of Figure 3-8 showing three regions with differing dispersion behaviour.

To understand these measured results, physical model simulations were run using Silvaco ATLAS by Professor M.J. Uren at QinetiQ Ltd. [1]. Firstly the device structure was simulated with no surface trapping effects included. A second simulation was then run to model the effect of trapped charge corresponding to a static class A bias condition. The "virtual gate" effect, described earlier in section 2.6.1, has been modelled as a localised distribution of electrons on the surface of the device immediately next to the gate on the drain side. Figure 3-17 shows the location of the fixed charge distribution, a 75 nm region of 12×10^{12} cm^2 charge density placed next to the T-gate to model the electrons trapped in surface states. This approach ignores the dynamics of trap filling and emptying, and instead assumes an equilibrium steady state surface charge has been established over multiple RF cycles.

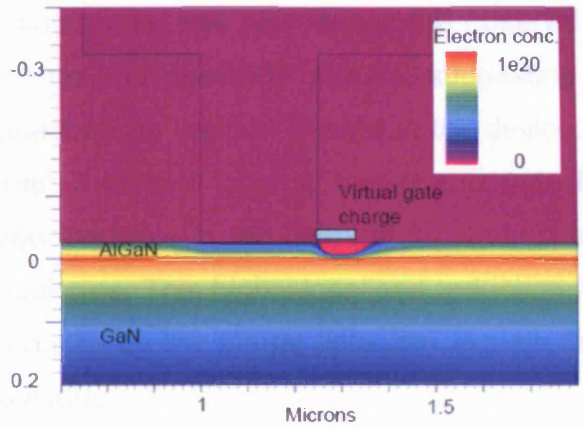


Figure 3-17 Simulated contour plot of electron concentration for V_G = 0 V, V_D = 0 V. The reduction of electron concentration in the channel due to the virtual gate can be seen on the drain side of the gate.

Using these two simulations, the virtual gate device model can then be compared with the standard device model to show the effect of localised surface charge on dispersion. Figure 3-18 shows the comparison IVs of the two simulation cases. The IVs of the standard device can be considered as baseline performance with no trap effects. The case with the surface charge included shows dispersion behaviour that is very similar to the measured waveform and pulsed-IV results. The same three distinct regions where different amounts of dispersion occur have been captured by the modelling approach.

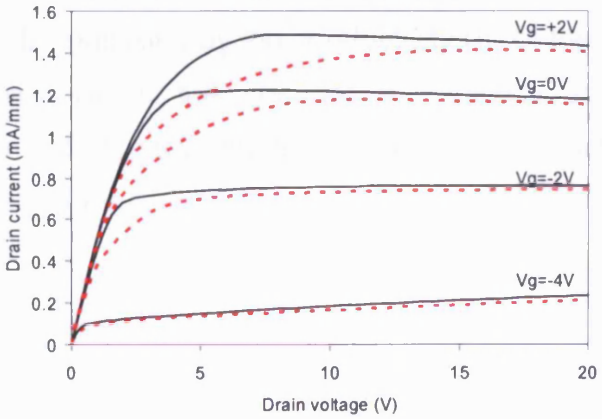


Figure 3-18 Simulated IV characteristics for the baseline case with no dispersion (full line) and the virtual gate model (red dashed lines).

The surface charge model has reproduced the observations seen in the measured waveform and pulsed-IV results, suggesting that it has also captured the impact of the trapped charge in the device. The main effect of the small area of surface charge beside the gate is to reduce the amount of charge available in the channel for a small area immediately beneath the virtual gate. This highly localised reduction in charge density in the channel caused by the virtual gate can explain the three different dispersion behaviours.

Firstly, region (a) where there is very little dispersion with increasing drain bias can be explained because the IV characteristics are dominated by the parasitic access resistance (on-resistance) which is not greatly affected by the small depleted region introduced by the surface charge. Consider the two semiconductor channels shown in Figure 3-19, one of which has a small "notch" missing. Under low electric field conditions, as would be experienced in region (a) where the drain to source voltage across the channel is typically lower than 5V, the current flowing through the semiconductor can be expressed as:

$$I = \sigma \mathbf{E} \qquad (3\text{-}1)$$

This is a simple re-statement of Ohm's law where current (I) is equal to the electric field (**E**) multiplied by the conductivity (σ) of the channel. If the reduction of electrons in the channel is relatively small, then the conductivity will not be greatly affected, and only a small difference will be seen in the IV behaviour.

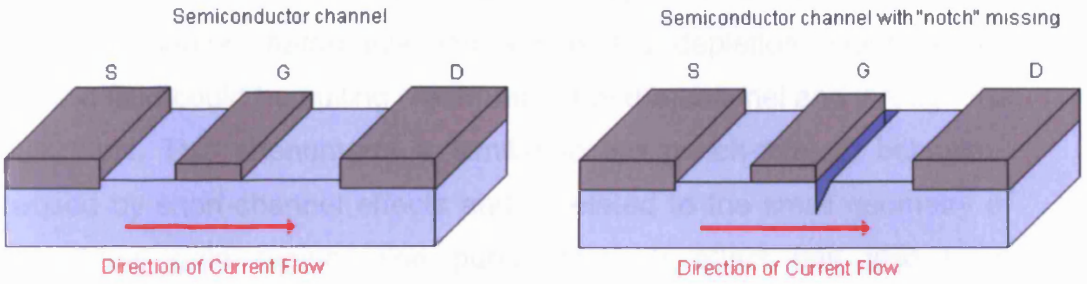


Figure 3-19 Two semiconductor channels, one of which has a small notch cut into it. The resistance of the two channels will not differ greatly under low electric fields.

Region (b) is where the surface charge has the most significant effect because the channel current saturates prematurely compared to the DC case. Under high electric field conditions where the electron velocity is already saturated, the current density in the channel becomes:

$$J = \rho v_{sat} \qquad (3\text{-}2)$$

In this case the current density (J) is a function of the charge density (ρ) multiplied by the saturated drift velocity (v_{sat}). Since there is a requirement for current continuity through whole length of the channel, the available current in the whole channel will be limited by the point in the channel with the lowest carrier concentration. It has been seen in the simulation that the virtual gate charge has the effect of reducing the carrier concentration in the channel region directly below it. In the simulation case the region below virtual gate will limit the current through the whole channel, even though the ungated areas of the channel have enough charge to carry more current. This explains why the RF current saturates prematurely compared to the DC current, because the trapped charge which forms the virtual gate has time to be redistributed under DC stimulus but not under RF stimulus.

Region (c) also suffers from reduced current, but at higher drain voltages the current shows a gradual recovery with increasing drain voltage. This is possible because the electric field at the higher drain voltages is large

enough to overcome the small depletion region. This mechanism could be either space charge injection across the depletion region or the electric field could be pulling electrons out of the channel and through the bulk GaN. This phenomena is similar to the punch-through behaviour caused by short-channel effects and is related to the small geometry of the virtual gate region. The punch through effect has also been demonstrated by the ATLAS simulation model, as can be seen in Figure 3-20. Here the electron concentration below the channel is shown to drastically increase under high drain bias.

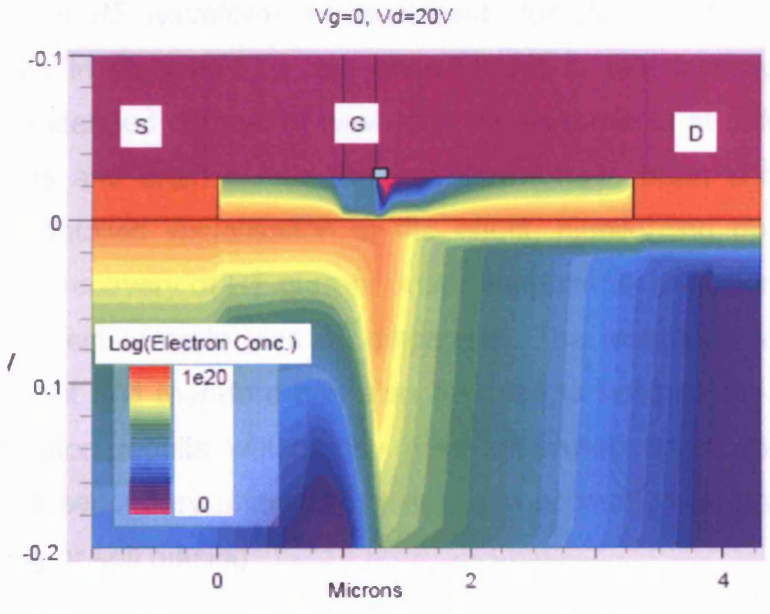


Figure 3-20 Simulated contour plot of electron concentration for a device with a virtual gate charge and a high drain voltage (V_G = 0V, V_D = 20V) showing punch-through effects resulting in a concentration of electrons below the channel that are able to support increased current flow.

3.3.7 Conclusions from waveform study of DC-RF dispersion

The measured RF waveform dataset highlighted three distinct regions of dispersive behaviour on the IV plane. The simulated virtual gate model developed at QinetiQ has been shown to explain all three behaviours, demonstrating a consistent understanding of the phenomena has now been formed. The small area of reduced charge under the virtual gate has been shown to cause a limited saturation current when the device is

excited by RF drive into the knee region. However, because the area is geometrically small it has very little effect on the overall resistance of the channel under low electric fields. Furthermore, because the virtual gate region is physically small, at high drain voltages punch-through effects (similar to short channel behaviour) occur which allow the current to recover with increasing drain voltage. Finally, the premature saturation effect caused by the virtual gate is seen only under RF stimulus and not under DC because the slow DC-IV sweeps allow enough time for the trapped virtual gate charge to be redistributed.

The value of RF waveform measurements for studying the dispersion phenomena in GaN HFETs has been shown in this investigation. By taking an extended dataset of waveform measurements at different load impedances and drain biases the waveforms have been shown to be useful for detailed visualisation of the effect, highlighting observations such as the recovery of RF current under short circuit conditions and the nonlinear effect of drain bias on dispersion. The technique uses direct measurement and therefore can also be used to validate the pulsed-IV and simulation results which may have otherwise been questionable because of secondary effects not taken into account correctly, such as self heating or self biasing.

The next stage for the development of GaN HFETs is to minimise the dispersion. Since the trapping is now believed to be accentuated by the high electric field at the gate edge, solutions which reduce the peak fields such as field plates are desirable. Other solutions that reduce the number of available trap sites, or reduce the ease of access are also likely to be successful in reducing the effect, for instance removing impurities from the surface of the device.

3.4 Degradation tracking

As with any developmental transistor technology, GaN HFETs must demonstrate robust performance before they can be utilised in end-use applications. In order to demonstrate robust performance, a new semiconductor process must be capable of a level of constant performance over a life cycle appropriate for its end application. Investigations of reliability in RF transistors employ a fairly standard characterisation procedure whereby RF output power reduction, gain reduction, DC bias drift and leakage levels are measured before, during and after various RF and DC stress tests. Elevated temperatures are often employed in accelerated life testing, where added thermal energy speeds up the degradation processes in order to condense the duration of test needed to demonstrate a given product lifetime. Reports of GaN HFET degradation behaviour measured using these standard techniques have become increasingly common as the technology approaches maturity [9].

In this section, a new measurement approach for monitoring degradation in developmental RF transistor technologies is presented. The approach constitutes the use of RF waveform measurements to monitor device performance during large signal continuous wave (CW) RF stress testing. The ability to measure current and voltage waveforms at the device input and output sampled during the stress period gives a unique insight into the degradation as it is occurring. In this work developmental GaN devices with rapid degradation issues during their burn in period were measured.

3.4.1 Measurement approach

The experiments were conducted on a batch of wafers with rapid degradation problems. Figure 3-21 below shows the extent of the degradation problems in these devices, with almost 15 % of output power being lost in a 1.5 hour burn in test. To carry out the degradation investigations, three of the same device types from fields across the wafer were tested in each scenario to ensure repeatability of results [2].

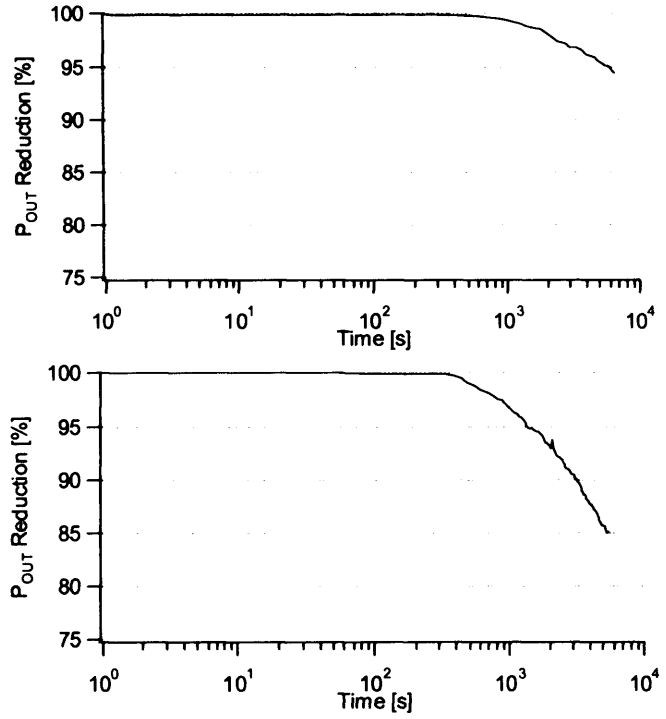


Figure 3-21 Power reduction as a percentage over time for two GaN devices operating in identical class A modes biased at a drain voltage of 20V. The top trace shows a reasonably stable device, whilst the bottom curve shows a device with rapid degradation issues.

Standard device performance parameters (output power, gain etc.) were analysed alongside the measured RF waveforms. The transistors were biased in a Class A configuration at a drain voltage of 20 V. The devices were driven approximately 3 dB into gain compression with a fundamental load tuned for optimum output power (R_L = 140 Ω at f_0) with all higher harmonics terminated into 50 Ω. Each device was then stressed for a period of 1.5 hours whilst the input and output current and voltage

waveforms were periodically sampled 100 times, resulting in a measurement similar to an RF "burn in" test, but with the addition of waveform data.

3.4.2 Standard reliability results

The results in Figure 3-22 show standard RF and DC reliability results for the same tests. The 15 % drop in output power during the stress period is the most significant problem. There is an observed increase in DC gate leakage current and a simultaneous decrease in DC drain current. These observations are consistent with charge storage on the surface of the device reducing the available channel current, in a process similar to the current collapse phenomena described in the preceding sections. It would be useful to the device designer to link these observations to a region of the device where the problem is occurring, i.e. under the gate or in the un-gated regions.

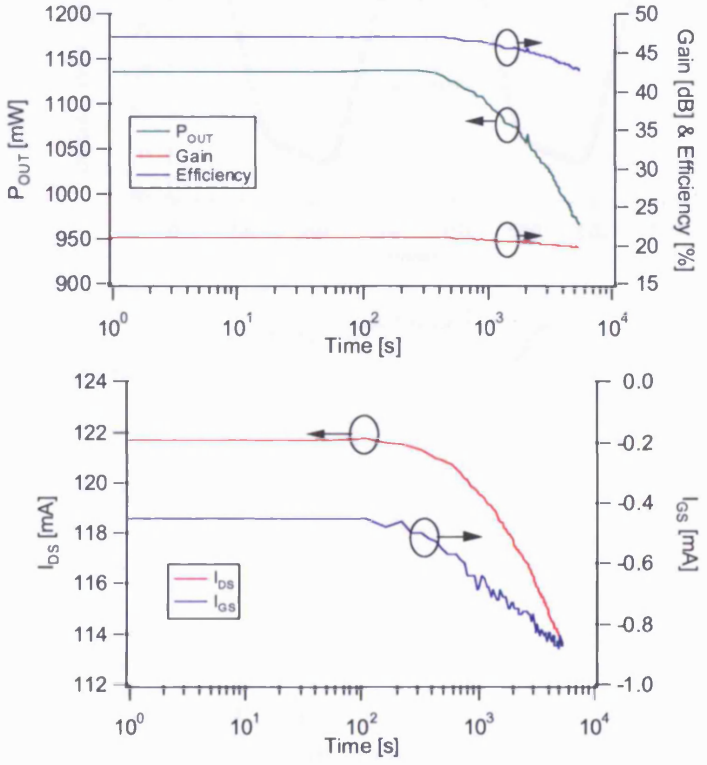


Figure 3-22 – Standard RF (top) and DC (bottom) measures of degradation for a 1.5 hour burn-in period measured in Class A at V_D = 20 V with an optimal P_{OUT} tuned load at f_0.

3.4.3 Degradation tracking using RF waveforms

Figure 3-23 shows the waveform data measured at the 100 sample points during the RF stress test. To allow easy analysis, the waveforms have been colour coded with the initial waveforms shown in dark red, the final waveforms at the end of the stress period in blue and the intermediate waveforms shown as light red. The input voltage is not shown since it was unchanged throughout the stress period.

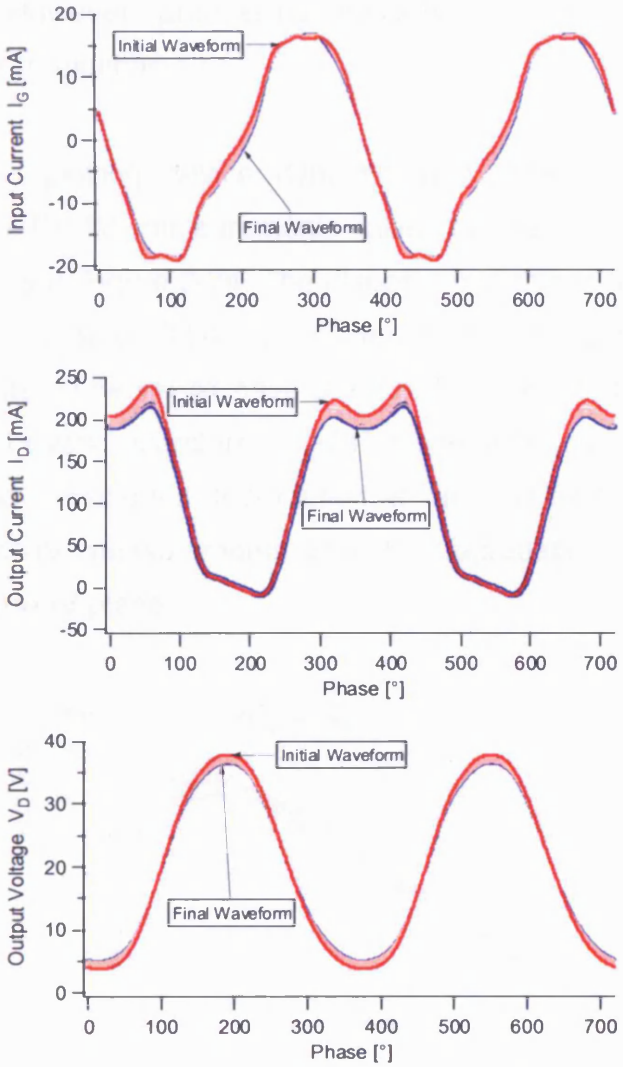


Figure 3-23 Measured RF waveforms showing from top: (a) input current, (b) output current and (c) output voltage waveforms recorded during a 1.5 hour burn-in period measured in Class A at V_D = 20 V with an optimal P_{OUT} tuned load at f_0.

There is only a very slight change visible in the RF gate current over the stress period, suggesting that the increase in DC gate current seen in Figure 3-23 is masked by the dominant RF displacement current passing through the input capacitance. The RF output current reduces over time but only at the high current end, whilst the RF output voltage waveform can be seen to be degrading gradually at both ends of its swing. The output voltage waveform alone is not particularly informative, as it is just demonstrating the reduction in output current over the static load impedance. However, processing these waveforms can make device issues easier to monitor.

For instance, plotting device dynamic load lines, which have been overlaid onto DC-IV measurements taken before and after the stress measurements in Figure 3-24. The dispersion visible in the final dynamic load line in Figure 3-24 is greater than the post-stress DC-IV measurements alone would have predicted, demonstrating that another mechanism beyond standard DC-RF dispersion (current collapse) is occurring and causing the degradation. It can also be seen in the before and after DC-IV measurements that the degradation is not occurring evenly over the IV plane.

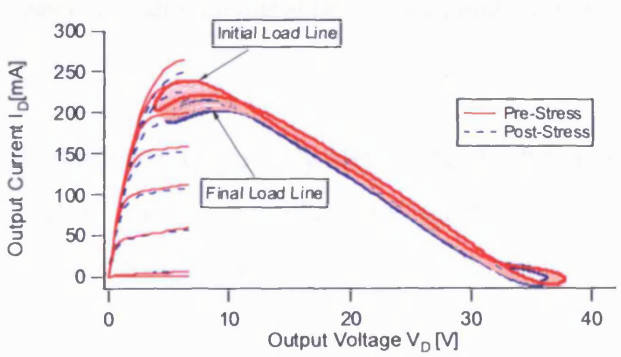


Figure 3-24 Dynamic load lines measured during the 1.5 hour stress period and DC-IVs measured before and after stressing (V_G = 0 V to -8 V in 1 V steps).

Generating the dynamic transfer characteristic as in Figure 3-25, can reinforce the observation that the dispersion is not occurring evenly over the IV plane. The degradation is concentrated in the high current region,

with very little change seen in the dynamic transfer characteristics until the gate voltage swings to values above -3 V. The lack of change observed around the threshold voltage suggests that the semiconductor under the gate is not being damaged and that any damage causing the degradation is occurring in the un-gated regions. This observation is consistent with those from section 3.3 above, where the DC-RF dispersion was found to be localised at the gate edge. Here a very similar effect is likely to be responsible for the degradation, except that the loss of current from the channel is not reversible. The permanent nature of the degradation is believed to be due to the creation of new faults in the crystal that become trap sites or counteract the natural mechanisms for introducing charge into the 2DEG - spontaneous polarisation and the piezoelectric effect [10].

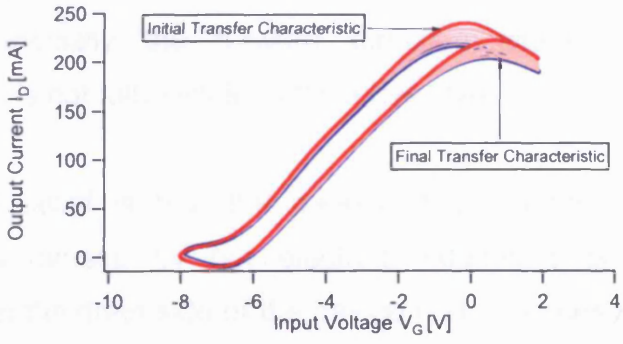


Figure 3-25 Dynamic transfer characteristics measured during the 1.5 hour stress period.

Another useful diagram is the dynamic input characteristic, shown in Figure 3-26. This plot primarily highlights the behaviour of the displacement current through the input capacitance.

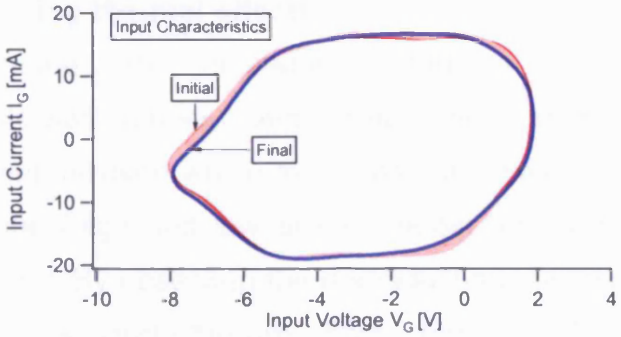


Figure 3-26 Dynamic input characteristics measured during the 1.5 hour stress period.

It can be seen that towards the more negative gate voltages there has been an increase in negative input current swing over the course of the stress test. This reduction at the breakdown end of the input characteristic corresponds with the increased DC leakage seen in Figure 3-26 and is indicative of a slight change in the properties of the gate. It can also be seen that the diode is not being heavily stressed in either direction, especially the forward direction where the exponential characteristic is not fully visible at this drive level.

The general belief is that the measured degradation in GaN HFET structures is caused by hot electron induced trapping and defect generation on the drain side of the device [11], a process exacerbated by the high operational drain bias voltages in many GaN applications. Electron trapping in defects in the AlGaN, bulk GaN or passivation act to partially deplete the conducting channel. An alternative view is that the degradation is associated with piezoelectrically induced stress leading to the creation of lattice defects [12]. The end result of both explanations is that less current is available in the active channel, particularly in the knee region, and therefore RF output power is permanently reduced. It is the permanent nature of this degradation which differentiates it from standard dispersion behaviours which will reverse themselves over time, as charge moves in and out of traps.

3.4.4 Discounting thermal effects

To test whether the degradation damage observed in these measurements was primarily electric field rather than thermally driven, an experiment was devised which independently stressed different regions of the IV plane (high and low electric fields) that were dissipating the same DC power. By observing the degradation in two specific regions, it was possible to separate the two effects. Figure 3-27 demonstrates this methodology.

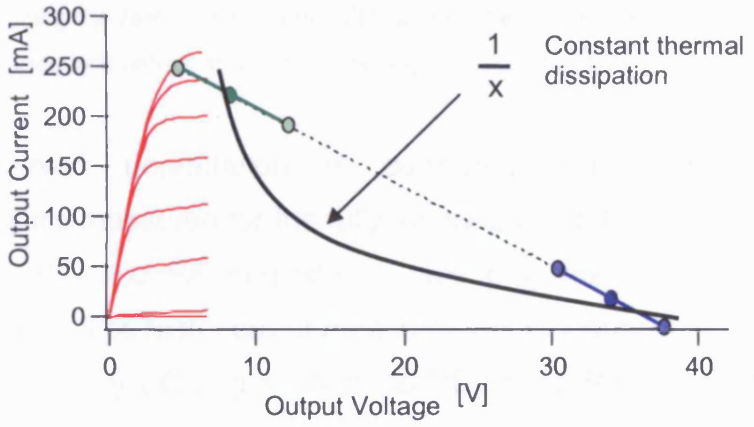


Figure 3-27 Showing two "slices" of the full class A load-line, both dissipating similar DC energy but only the blue slice excites the high electric field region.

The two regions were isolated by measuring burn in periods for "slices" of the same load line on a number of identical devices. Shown in Figures 3-28 and 3-29 are the two extreme slices of the optimum power load line. The slice shown in Figure 3-28 excites only the high current region of the IV plane without entering the high voltage region. Conversely, the slice shown in Figure 3-28 excites only the high voltage region of the IV plane without entering the high current region. Negligible amounts of RF degradation are visible during the burn in periods for both of the load line slices shown in Figures 3-28 and 3-29. However the DC degradation in the pinch-off slice of Figure 3-29 is significantly larger than that seen in the high current slice shown in Figure 3-28, as evidenced by the slump in DC-IVs at high current levels seen only in Figure 3-29.

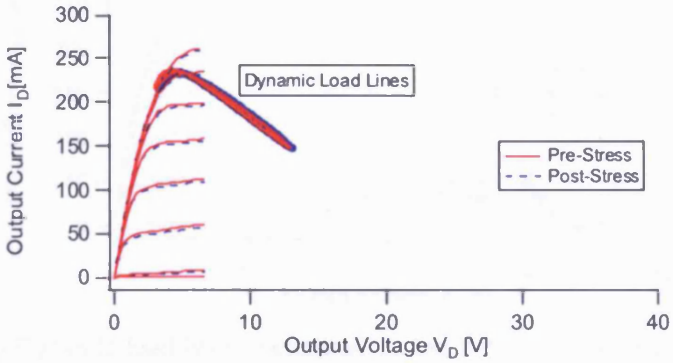


Figure 3-28 – Dynamic load lines measured during a 1.5 hour stress period for a load line slice exciting the high current, low voltage knee region only. Load lines are overlaid on DC-IVs measured before and after stressing (V_G = 0 V to -8 V in 1 V steps).

The observed degradation is consistent with the degradation characteristics measured for the fully extended load-lines in section 3.5.3, where the DC and RF degradation was only manifested in the high current region. The high current measurement in Figure 3-28 appears not to be causing any DC degradation, so little or no RF degradation would be expected. However, the pinch-off measurement shown in Figure 3-29 shows significant DC degradation, but very little RF degradation is seen in the low current only RF load-lines.

This can be understood by considering the dynamic transfer characteristic of Figure 3-25 being excited by an input signal limited to a gate voltage swing below -3 V. Based on the full load-line results of section 3.5.3 it would be expected that no RF degradation in the low current region would be visible, even though DC and RF degradation would still be seen in the high current region. These results suggest that it is the high electric field in the high voltage region rather than any thermal effects that is causing the damage to these developmental GaN HFETs.

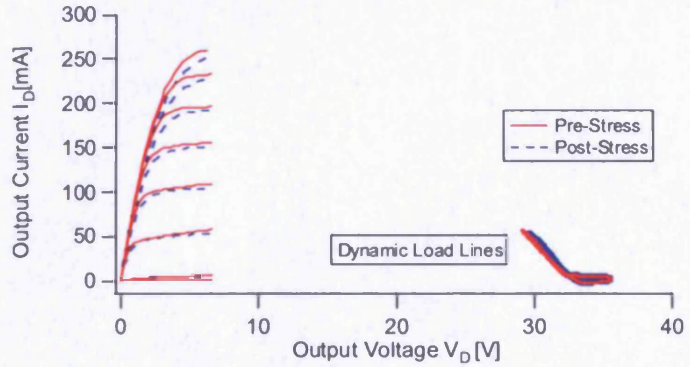


Figure 3-29 – Dynamic load lines measured during a 1.5 hour stress period for a load line slice exciting the low current, high voltage pinch-off region only. Load lines are overlaid on DC-IVs measured before and after stressing (V_G = 0 V to -8 V in 1 V steps).

3.5 Summary

This chapter has demonstrated the novel ways that RF waveform measurements can be used to analyse GaN HFET devices. The possibility for developing enhanced understanding of device level issues from a coherent set of observed behaviours is explored through the analysis of extended waveform datasets. It has been shown that the insight gained can be fed directly back into device processing – by selecting the optimal level of iron doping to control short-channel effects without damaging device performance in other areas [8]. The observations of extreme behaviours, such as short and open circuit fundamental load conditions can be used to highlight features of an effect such as DC-RF dispersion that must be included in a successful understanding of the phenomena. These observations were used to develop a successful explanation of the effect that extends the "virtual gate" concept, making it more specific by explaining the current limiting effect in terms of saturated velocity [1]. The first use of RF waveforms for studying device degradation over time has also been presented, highlighting the similarities and differences between permanent and temporary current reduction mechanisms in the devices [2].

3.6 References

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Chapter 4 – Review of Efficiency Enhancement Techniques for RF Power Amplifiers

4.1 Introduction

Amplifier efficiency is a constant concern for PA designers due to increasing system requirements for reduced energy consumption, PA size and heat dissipation. In mobile phone handsets the transmitter PA is a significant drain on the battery life, which impacts on standby time – a distinguishing feature for many consumers that can have knock-on effects on handset sales. Similarly, in a national network of base stations, thermal dissipation and electrical running costs are strongly impacted by the efficiency of the transmitter PA. Base station PA efficiency is set to become an even more important concern in the coming years, as environmental concerns grow and carrier companies are encouraged to minimise their power consumption. Furthermore, in remote areas and developing countries where fixed power supplies are not readily available, base stations are emerging that must run on renewable energy sources or local generators, heightening the importance of good energy efficiency.

Beyond commercial wireless communications, in almost all applications of wireless transmission it is advantageous for the transmitter to be as efficient as possible to reduce energy consumption, heat dissipation and consequently allow greater operating power from a given form factor. Solid-state devices running at lower average temperatures will typically last longer. In the majority of military and space applications reliability, or the life expectancy of components, is a key specification alongside size and weight. Meeting these specifications will be easier if a high efficiency RF PA stage has been designed.

In this chapter high efficiency PA theory is described with an emphasis on switch-mode architectures and the waveform shaping or engineering required to achieve good performance in these modes. Particular importance is placed on the class F mode, which is theoretically capable of providing 100% drain efficiency whilst outputting more power than a Class B amplifier built using the same device. Some of the important background literature surrounding the class F mode is discussed, focusing first on the historically important ideal case and then analysing slightly more realistic contributions. The limitations of the existing theoretical work in describing the behaviour of real active devices operating in class F and how such circuits should be designed is highlighted, paving the way for the analysis of Chapter 5.

4.2 Basics of high efficiency PA theory

There are a number of measures of how efficiently an amplifier can convert energy from its DC supply into RF energy. The most basic efficiency measure is drain / collector efficiency (η) which is simply a ratio of output RF power at the fundamental frequency ($P_{RF\ OUT}$) to DC power provided by the power supply (P_{DC}):

$$\eta = \frac{P_{RFOUT}}{P_{DC}} \times 100\ \% \qquad (4\text{-}1)$$

Efficiency is usually quoted as a percentage. It is important that only the fundamental output power is included in this measure because if the amplifier is operating in its nonlinear regime it will also be converting some of its input energy into RF power at other frequencies. In most applications energy generated at spurious frequencies is of little use and so using broadband RF power in this calculation can be dangerously flattering. The most commonly used definition of efficiency in RF system design is Power Added Efficiency or PAE. The PAE includes the RF drive signal power ($P_{RF\ IN}$) as a factor and therefore takes into account the amplifier's RF power gain (G). If the gain is large, PAE and drain efficiency can be assumed to be equivalent:

$$PAE = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}} \times 100\ \% \qquad (4\text{-}2)$$

$$PAE = \frac{P_{RFOUT}}{P_{DC}} \times \left(1 - \frac{1}{G}\right) \times 100\ \% \qquad (4\text{-}3)$$

4.3 Classes of PA operation

The majority of RF PAs are described by their class of operation. This scheme of categorising RF PA behaviour traditionally referred to the degree of quiescent bias current flowing in the active device, or more precisely, the conduction angle (α) of the current waveform produced at the output of the device. The conduction angle describes the fraction of one cycle of sinusoidal stimulus for which an active device is turned on and conducting current [1].

More recently new classes of operation have been analysed where bias point alone is not enough to describe the important features distinguishing one mode from another. In these more complex modes the properties of the output matching network at both fundamental and harmonic frequencies become important. Figure 4-1 below shows the basic structure of a single-ended RF PA, containing all the necessary components to alter the behaviour of the active device. There are also more complex techniques in PA efficiency enhancement that are usually classified by the theory of operation that the circuit must operate in, such as Doherty or Envelope Tracking.

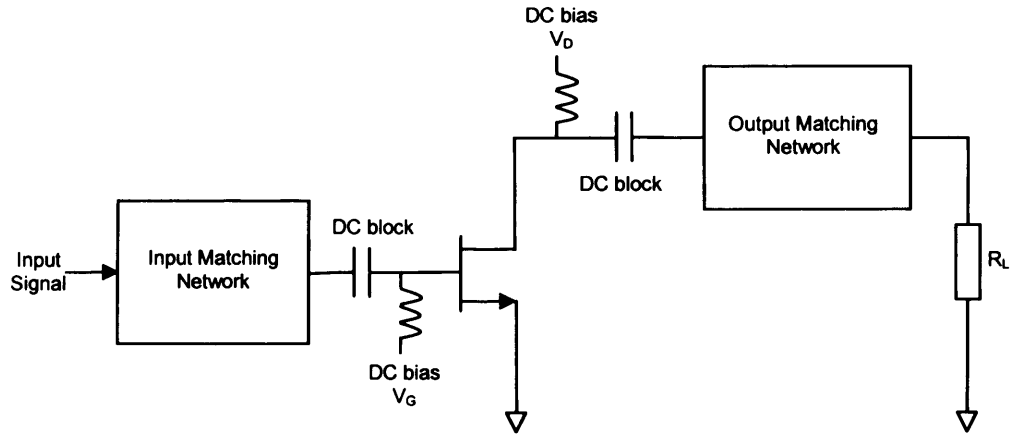


Figure 4-1 Basic schematic of an FET based RF PA.

4.3.1 Waveforms in PA classification

The majority of amplifier classes or modes of operation can be best described in terms of their output current and voltage waveforms. In fact, determining whether or not a specific class of operation has truly been achieved can often only be verified by measuring the output waveforms. The four traditional amplifier modes (classes A, AB, B and C) are ideally terminated with a harmonic trap to short circuit all harmonic components from their voltage waveform, leaving it as a sinusoid of the fundamental drive frequency. The current waveform then moves through various degrees of truncation as the conduction angle of the current waveform is reduced by appropriately biasing the active device.

Classes A and B are very specific cases with exact output current conduction angles of 360° and 180° respectively. Class A has highest gain and introduces very little distortion until heavily overdriven due to its inherent linearity. Class B has higher theoretical efficiency but with lower gain and typically more distortion. Class AB describes any mode with a conduction angle between 180° and 360° and is the most commonly implemented mode in RF PAs since it offers a compromise between class A and class B performance. Class C covers any amplifier operating with a conduction angle between 0° and 180°, allowing still higher efficiencies but with increasingly compromised gain and output power as the conduction angle is reduced. Operating in a class C bias can also result in a reduced lifetime of operation for the active device as higher electric fields are developed across the device input terminal during operation.

Table 4-1 summarises the waveforms, conduction angle and efficiency performance of the traditional amplifier classes. In order to boost efficiency beyond class B's 78.5% theoretical maximum without sacrificing output power as heavily as in class C, various techniques have been employed by designers to boost efficiency. A prominent approach in the academic literature is to expand the list of PA classes to include more

complex modes of operation. Some of the more advanced modes of operation are described in the following sections.

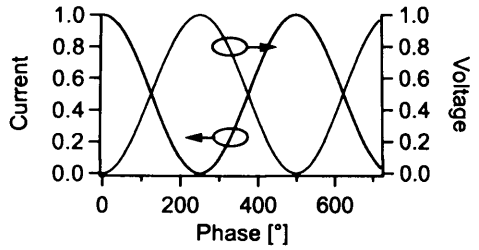
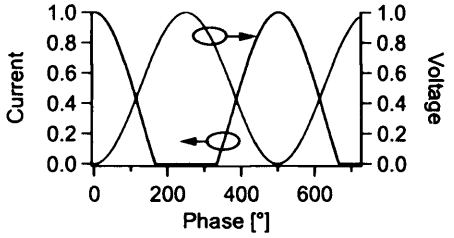
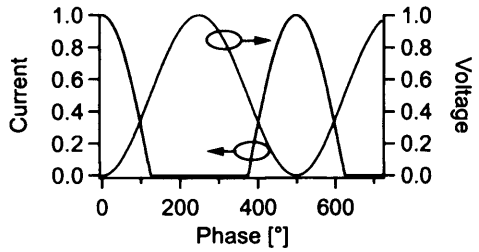
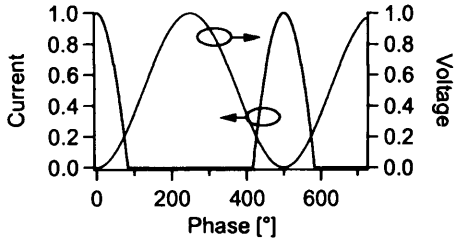
Class	Theoretical max. drain efficiency (η) (%)	Conduction angle (α) (°)	Ideal Output voltage and current waveforms
A	50	360	
AB	50 < η ≤ 78.5	180 < α < 360	
B	78.5	180	
C	78.5 < η ≤ 90	0 < α < 180	

Table 4-1 showing the output current and voltage waveforms (normalised to unity) for ideal class A, B, AB and C operation. Also shown are the conduction angles in degrees and the maximum theoretical drain efficiency.

4.3.2 Switch-mode amplifiers

One approach for boosting efficiency in PA designs is to utilise the active device as a switch so that it spends the majority of its time operating in saturation or cut-off modes, with as little time as possible spent in the dissipative region. The waveforms for some of the major switch-mode PA classes are given in table 4-2. The switch-mode concept is common at audio frequencies, using what is called a class D amplifier, where the voltage and current waveforms both resemble square waves. Unfortunately, this configuration requires a push-pull architecture that becomes difficult to implement at higher frequencies, largely because the f_T of the device must be considerably higher than the switching frequency [1]. Class E amplifiers are more common at GHz frequencies, where both current and voltage waveforms are more easily realised asymmetrical half-rectified sine waves. A class E configuration can theoretically reach 100% efficiency if the active device and circuit behaviour are considered ideal, but results in less output power than class B [2]. Consequently many class E implementations employ dangerously large voltage trajectories whilst trying to recover lost output power.

Two switch-mode PA varieties that actually enhance output power are the class F and inverse class F modes. These modes are based on designing the output matching network to separately tune various harmonics so that the output current and voltage waveforms are engineered to achieve very high efficiencies at powers greater than those in a corresponding ideal class B design. The class F mode has a half-rectified sinusoidal current waveform and a square voltage waveform. An inverse class F circuit reverses this arrangement. Both class F and inverse class F modes will have identical performance in the ideal case. Various factors such as the breakdown voltage of the device technology used or the efficiency performance at low drive levels will usually influence the selection of one or other mode. This thesis will concentrate on the class F mode.

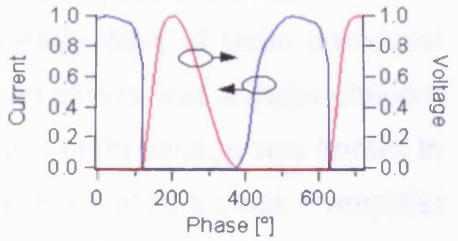
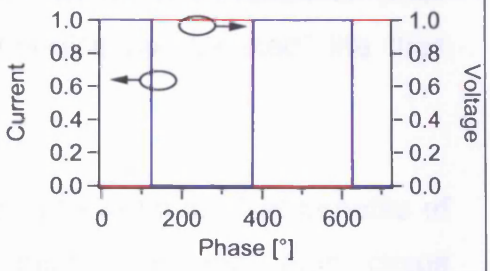
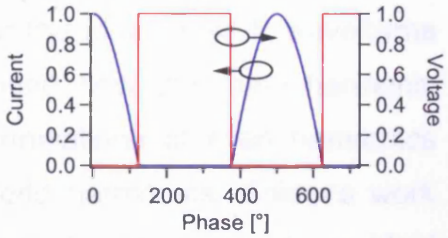
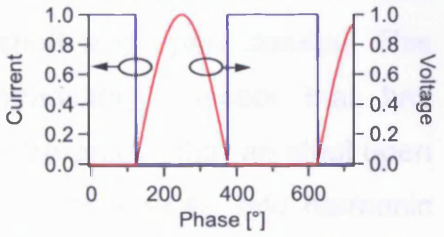
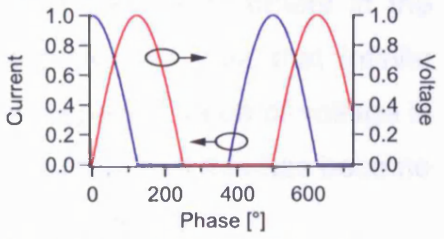
Class	Theoretical max. drain efficiency (η) (%)	Conduction angle (α) [°]	Ideal Output voltage and current waveforms
E	100	< 180	
D	100	-	
F	100	180	
F^{-1}	100	180	
J	87 (78.5)	180	

Table 4-2 showing the output current and voltage waveforms (normalised to unity) for a variety of switch-mode PA classes. Also shown are the conduction angles in degrees and the maximum theoretical drain efficiency.

4.4 Ideal class F operation

4.4.1 History

The approach of engineering the active device output waveforms to improve efficiency has existed since the early days of radio broadcast when the heat dissipation of vacuum tube amplifiers was a major concern and flattening the bottom of the vacuum tube plate voltage was known to yield efficiency advantages [3]. The first description of a class F amplifier is credited to Tyler in 1958 [4], who demonstrated a multi-resonator class F output network that shorted even harmonics but "peaked" the third harmonic.

In 1967 Snider presented an investigation of the theoretical benefits of optimally loading the harmonics with ideal open and short circuit terminations [5]. Snider's paper introduced the ideal class F waveforms (shown again in Figure 4-2) and described how the ideal harmonic terminations were perfect short circuit terminations at even harmonics and perfect open circuit terminations at odd harmonics. Snider's work also states that the efficiency performance will deteriorate at non-ideal harmonic conditions (away from perfect short and open circuits). This statement has led to a peculiarly contradictory concept that has proliferated throughout much of the class F literature - that an ideal open circuit is required at odd harmonics to generate specific odd harmonic voltage content, even though there is no odd harmonic content in the ideal half-rectified current waveform. Essentially, the idea that infinite impedance multiplied by zero current equals a specific value of voltage is not a wholly physical statement and it is unfortunate that this has become an accepted concept in many accounts of class F theory.

4.4.2 Ideal class F waveforms

The ideal class F performance is a direct result of the output waveforms. The output waveforms for the ideal case are plotted as a dynamic load-line in Figure 4-3. The ideal class F waveforms contain the fundamental and then either all odd harmonic components for voltage, or all even harmonic components for current. In both the voltage and current waveforms, the harmonic components must have a precise magnitude and phase to combine correctly to give the ideal waveforms.

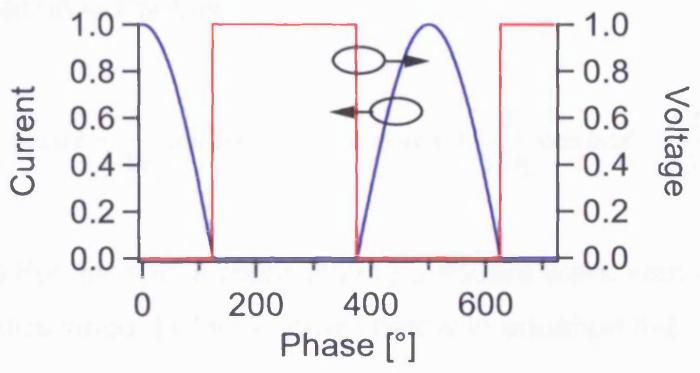


Figure 4-2 Ideal class F output current and voltage waveforms normalised to unity.

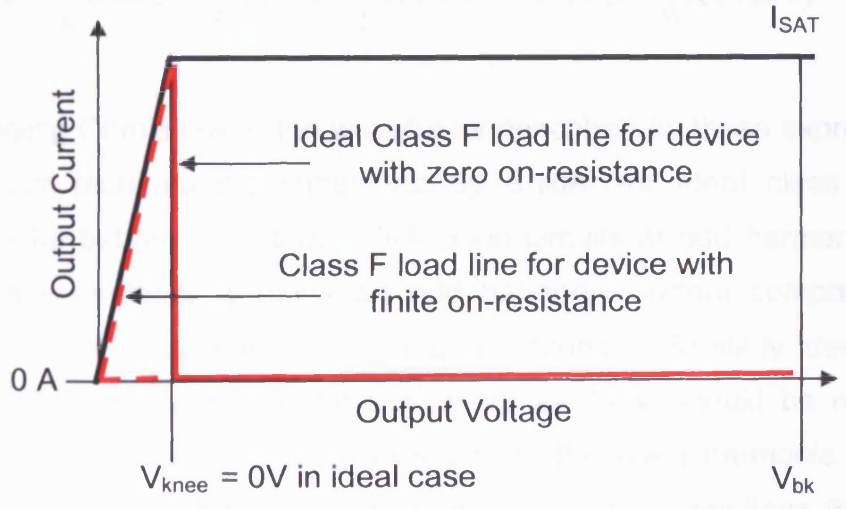


Figure 4-3 Ideal class F load-line with a vertical knee boundary. Note at no point does the load-line enter the dissipative region, never simultaneously leaving the 0 V or 0 A axis. Also shown as the broken line is the load-line trajectory for a device with a more realistic on-resistance.

There is never a mix of both odd and even harmonics in either waveform. As a result, the output RF power is only generated at the fundamental frequency and never dissipated at the harmonics because the current and voltage waveforms will never overlap. This can be expressed mathematically by looking at the Fourier series of the two ideal waveforms, which confirm that odd and even harmonics of the fundamental frequency are never simultaneously present.

The Fourier series representing the half rectified current waveform is given in equation 4-1 below:

$$f(t) = \frac{1}{\pi} + \frac{1}{2}\cos\omega t + \frac{1}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t + \frac{2}{35\pi}\cos 6\omega t - \frac{2}{63\pi}\cos 8\omega t...$$

Similarly the Fourier series representing a square wave with a dc component described as "dc" is given below in equation 4-2:

$$f(t) = dc + \frac{4}{\pi}(\cos\omega t - \frac{1}{3}\cos 3\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t + \frac{1}{9}\cos 9\omega t...)$$

By applying Ohm's law to the waveforms described by these expressions the circuit requirements suggested by Snider for ideal class F can perhaps be better understood. Ideal open circuits at odd harmonics are necessary, as there is never an odd harmonic current component to convert into the odd harmonic voltage component. Similarly ideal short circuits at even harmonics are necessary as there should be no even harmonic voltage components arising from the even harmonic current components. Without the perfect open and short terminations the ideal waveforms cannot co-exist and satisfy Ohm's law.

4.4.3 Fundamental voltage extension in class F

Class F is able to increase the efficiency and power over a class B design using the same device because it squares up the voltage waveform. The squaring effect allows the fundamental component to grow, effectively extending outside of the operating boundary conditions, because the other harmonic components combine to bring the total waveform inside the boundary. The boundary conditions in an FET based class F design will consist of the saturation limit and the cut-off limit. In an ideal square wave the fundamental voltage component can increase by a factor of 4 / π compared to a sine wave of identical peak-to-peak swing. The voltage extension effect for an ideal square wave can be seen in Figure 4-4 below.

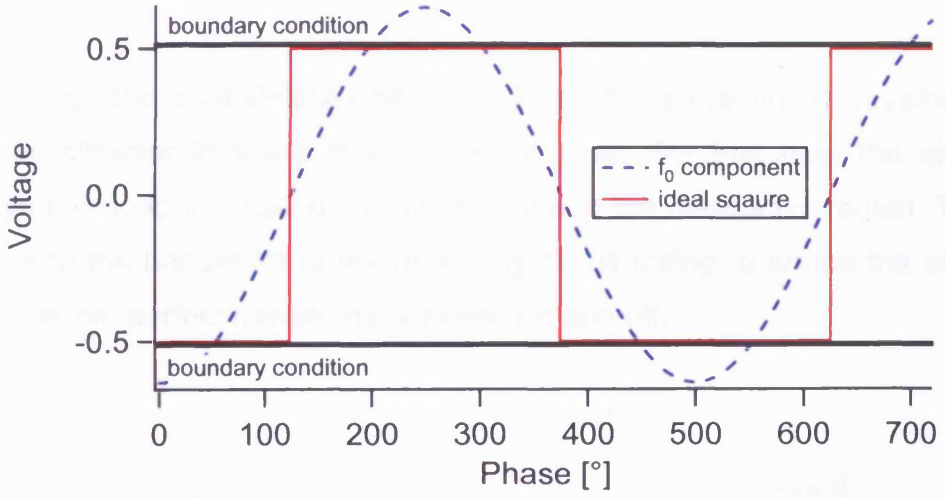


Figure 4-4 Plot showing a square wave and its fundamental harmonic component, which is able to extend 4 / π times beyond size of a pure sinusoid constrained within the same boundary conditions.

Since both the class B sinusoidal and the class F square waveforms are symmetrical, the voltage extension at the fundamental frequency does not affect the DC average. The ultimate result of the squaring up of the voltage waveform in ideal class F is an increase in output power and efficiency by a factor of 4 / π compared to an ideal class B amplifier using the same device.

4.4.4 Adjusting the fundamental load impedance

When odd harmonic tuning is applied to a device in a class F circuit, and the voltage waveform becomes square and creates the extension at the fundamental frequency, there must also be a change in the fundamental load to allow the device to see the corresponding increase in efficiency. In order to maintain a constant current waveform and achieve the full 4 / π increase in efficiency when the voltage extension occurs, the optimum fundamental load (R_{opt}) should be increased by a factor of 4 / π. This is a simple application of Ohms' law and can be demonstrated by looking at the measured waveforms and dynamic load-lines shown in Figures 4-5 and 4-6. It can be seen that the class F and class B waveforms fit within the same boundary. This would not be the case if the fundamental load impedance had not been increased in the class F case.

Perhaps the most striking observation from these measured waveforms is how different they are from the ideal case. For instance, the class F dynamic load-line spends significant time in the dissipative region. This is due to the bandwidth of the matching circuit failing to shape the voltage wave into perfect transitions between on and off.

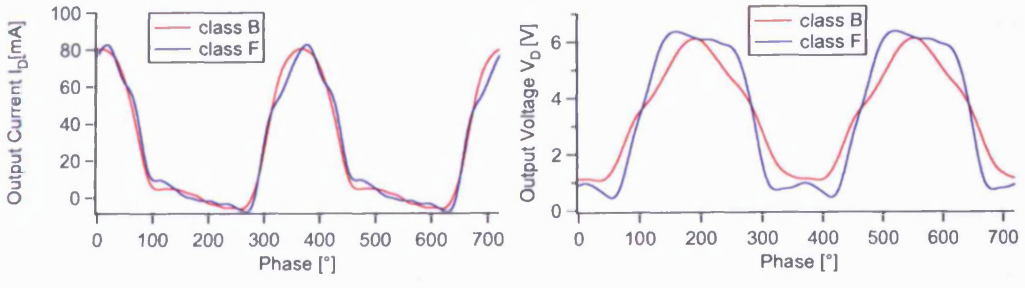


Figure 4-5 Measured output current and voltage for class F and class B in the same device. The fundamental load-impedance has been increased by 4 / π to maintain the same current waveform. Measurements made on-wafer using a 2x100 µm GaAs pHEMT at 1.8 GHz.

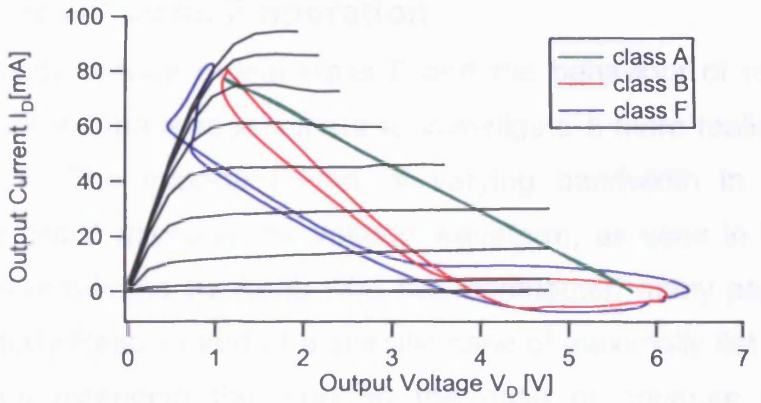


Figure 4-6 Measured dynamic load-lines for the same measurements as Figure 4-5. Also shown is the class A optimum load-line match, R_{opt}.

4.5 Non-ideal class F operation

The disparity between ideal class F and the behaviour of real class F circuits has led many researchers to investigate a more realistic version of class F. The important idea of varying bandwidth in the output matching circuit affecting the voltage waveform, as seen in Figure 4-5, has been developed by Raab who has contributed many papers to the topic. Initially Raab looked at a specific case of maximally flat waveforms [6], before extending the work to the case of optimum power and efficiency [7]. A major contribution of this work was to explain how the maximum achievable efficiency scales with the number of ideally terminated harmonics, as described in table 4-3 below. This work has helped explain why ideal class F efficiencies have not always been achieved in realised designs controlling only a limited number of harmonics.

	n = 1	n = 3	n = 5	n = ∞
m = 1	50.0%	57.7%	60.3%	63.7%
m = 2	70.7%	81.7%	85.3%	90.0%
m = 4	75.0%	86.6%	90.5%	95.5%
m = ∞	78.5%	90.7%	94.8%	100.0%

Table 4-3 showing optimal drain efficiencies based on the number of harmonics included in the analysis, where m denotes even harmonics and n denotes odd harmonics, from Raab's analysis [7].

The analysis of Rhodes [8] has helped formalise the understanding of class F circuits that are ideal except in their bandwidth of harmonic control. Rhodes restates the fact that there is only one solution for the current waveform that will produce optimum efficiency in ideal linear class B, and therefore there will only be a singular current waveform that will be optimal for ideal class F operation in an ideal device. His paper considers only this ideal current waveform, but goes on to provide a general proof that there is a singular optimum voltage waveform for all

cases of output circuit bandwidth (circuits controlling three harmonics upwards), which are not the maximally flat solution but contain a ripple with turning points at specific symmetrical locations dependant upon the bandwidth of the matching circuit. This finding has interesting connotations for practical circuit implementations, where hitting a singular solution to maximise performance with all the associated tolerances of a manufacturing process will in all likelihoods be impossible.

A more fundamental issue in achieving the ideal case class F voltage waveform from the ideal current waveform remains. The ideal current waveform contains no odd harmonics. If there are no odd harmonics present in the ideal current waveform then no passive impedance termination, including open circuits, should be able to convert zero current at a given harmonic into a specific value of voltage at that harmonic [1]. This statement precludes the existence of the theoretically ideal class F waveforms with no odd harmonics in the current waveform. A logical solution must include some small amount of odd harmonic current that a real impedance can translate into a specific sized voltage component.

The ideal class B current waveform without odd harmonic components is only possible if the transistor is still considered an ideal voltage controlled current source operating backed off from compression. Cripps explains the presence of odd harmonic content in the current waveform in terms of the current waveform being clipped as it is driven into the finite device on-resistance or the knee region [1]. In a practical device when the current waveform interacts with the knee boundary at a given drive level it will become harmonically rich. Since the current waveform is now clipping at saturation as well as at cut-off this additional harmonic content will be odd. This odd harmonic content can then interact with passive load terminations to become appropriate odd harmonic voltage content in a far more rational manner. The effect of clipping the current waveform into the knee region is shown diagrammatically in Figure 4-7.

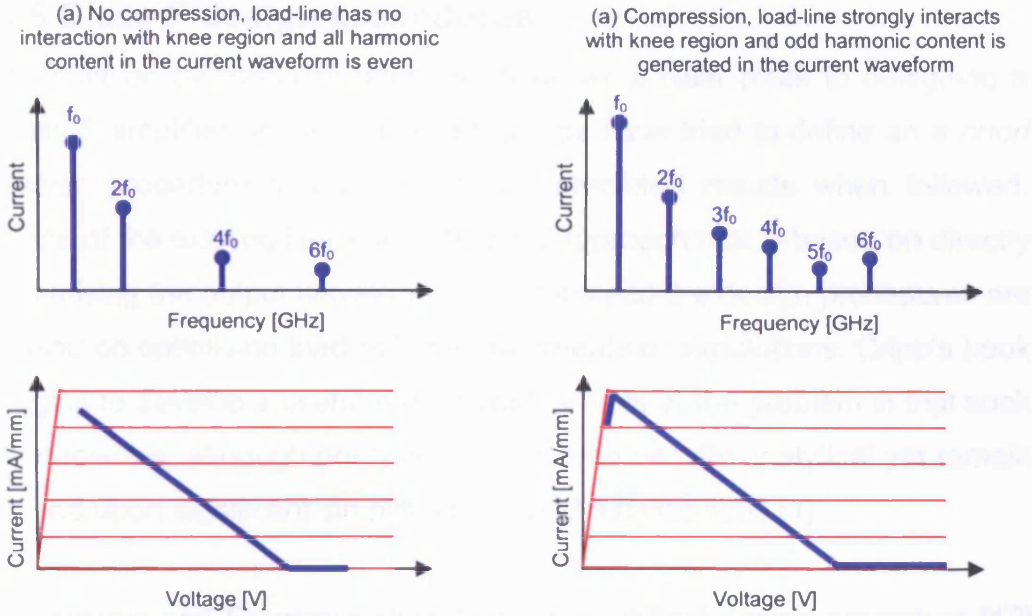


Figure 4-7 Load-lines and the corresponding frequency content of the current waveform for two cases (a) ideal class B with no interaction with the knee region and (b) at a higher drive level the load-line trajectory is strongly interacting with the knee region, clipping at saturation as well as at pinch-off and generating odd harmonic content in the current waveform.

Cripps' observation also suggests that the requirement of an ideal open circuit first proposed by Snider [5] may not be the optimum odd harmonic termination if a finite amount of current is flowing, instead a more specific lower value of odd harmonic impedance should convert the specific quantity of odd harmonic current into the required voltage components. Importantly, the effect of generating odd harmonic current components can also be achieved through biasing away from the ideal class B bias point. The transfer characteristic of most real world devices can be excited in such a way that they generate odd harmonic components in the output current [1]. Selecting the correct conditions for an optimum class F design appears to be a balancing act of harmonic terminations, drive level and DC biasing. It would be convenient if a circuit designer could follow a set procedure to optimise a class F design with a given technology.

4.6 Class F design procedures

It would be desirable to offer the designer a clear route to designing a class F amplifier and a number of groups have tried to define an *a priori* design procedure that produces the predicted results when followed. None of the existing literature offers an approach that is based on directly optimising the output waveforms [9-11] instead the design procedures are based on optimising load-pull measurements or simulations. Cripp's book begins to develop a useful procedure but hints at the problem in that such a procedure, although possible, will become heavily analytical yet remain based upon significant simplifications and assumptions [1].

Colantonio and Giannini's simplified but analytical design procedure [12] is on the whole excellent, and contains a particularly interesting remark in that it suggests that the active device should be biased for an I_{DQ} of approximately 10 % of I_{MAX}. This bold statement is somewhat counter intuitive of ideal class F theory, as this bias point will drastically reduce the efficiency of the current waveform as has been shown by [13]. The rationale for this less efficient bias point is that only at gate biases above threshold does the third harmonic current become phase inverted relative to the fundamental which is essential for achieving the square class F voltage waveform (see Figure 4-8). What is really meant by this is that only when current and voltage at the third harmonic are anti-phase can the third harmonic impedance be positive and therefore realisable.

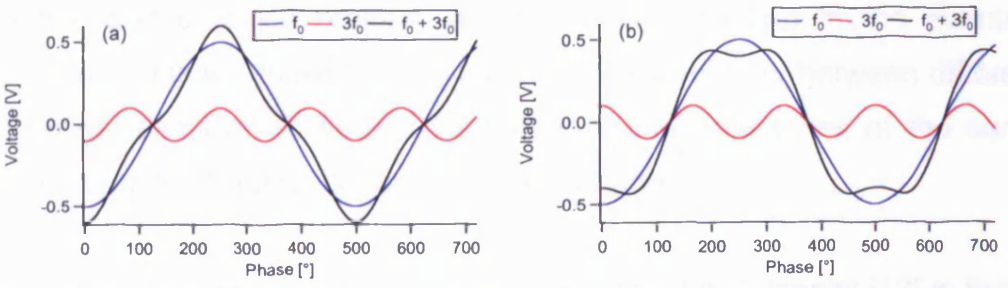


Figure 4-8 Plots showing three voltage waveforms: a fundamental tone, a third harmonic tone and the combined fundamental and third harmonic waveform. (a) shows the fundamental and third harmonic in phase and (b) shows a more efficient square wave with 180 degrees phase difference between the fundamental and third harmonic.

The difference between the ideal case, where an ideal class B current waveform is used, and that presented by Giannini is the drive level. Giannini shares the more physical view that the third harmonic current must be present through a clipping mechanism, but his analysis describes the ideal case where the half rectified current waveform is clipped and becomes a highly idealised "quartic" waveform [12], as shown in Figure 4-9 below.

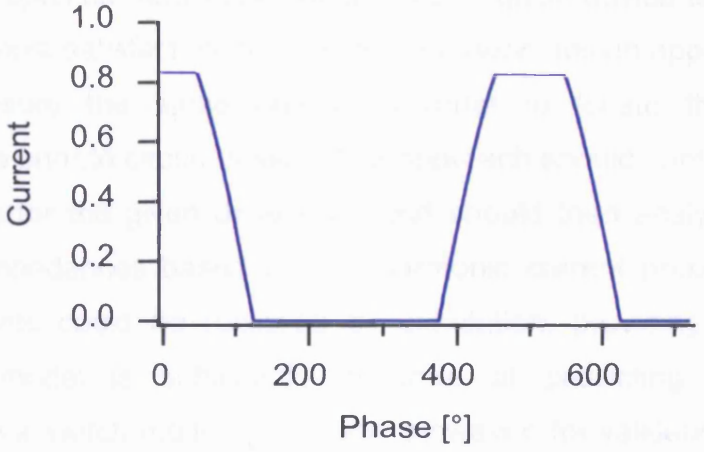


Figure 4-9 Ideal quartic current waveform with ideal hard clipping at the knee.

This analysis is highly valuable for understanding the general trend but may be overly simplistic. The true device knee boundary is unlikely to create an ideal quartic current waveform at the drive levels of interest to a PA designer, since overdriving an FET into such hard compression may result in permanent device damage. Similarly, the real world device transfer characteristic will usually have a gradual transition between the active and pinch-off regions, again causing variation in the eventual solution. This will make the appropriate bias level vary between different devices, and even between different load-line trajectories of the same device, as the transfer characteristic will change.

The main problem with the approach suggested by Giannini [12] is that it limits the designer from finding a singular optimum solution, as the designer is advised to select an arbitrary 10 % of I_{MAX} bias point, and therefore will not have minimised unnecessary dissipation due to excess

odd harmonic content in the current waveform. It therefore makes sense to alter Giannini's approach and select the biasing of the device on a measured sweep of the device transfer characteristic, preferably at RF frequencies measuring the harmonic current components.

Indeed, given the desirability of a conclusive design procedure, and the complications involved in clarifying the difference between optimum ideal class F and optimum realisable class F with a given device technology, it seems the most satisfactory solution to an *a priori* design approach would be to measure the same device in order to locate the optimum performance prior to circuit design. The approach should contain a sweep of gate bias for the given drive level and should then analyse the best harmonic impedances based on the harmonic current present. These measurements could be replaced by simulation, providing the device non-linear model is sufficiently accurate at predicting the device behaviour in a switch-mode application. However, for validation purposes it is sensible to measure the true device behaviour first hand using the RF waveform measurement system with active harmonic load-pull. The results of such investigations will be presented in the following chapter.

4.7 Disadvantages of class F

To understand the use of class F and other switch-mode techniques within the various RF transmitter applications, it is useful to consider their disadvantages as well as their advantages.

4.7.1 Bandwidth

A disadvantage that the majority of switch-mode PA architectures suffer from is the inherently narrow bandwidth of their efficiency enhancement. Experimental results for class F designs show reasonable efficiency performance is only maintained over approximately 10 % bandwidth [14], deteriorating significantly further away from the centre frequency. This limitation is not exclusive to switch-mode amplifiers, other efficiency enhancement techniques such as Doherty PAs have similarly narrowband limitations. Figure 4-10 below illustrates the limitation of harmonic control amplifiers over an octave bandwidth, using a class F matching network as its example.

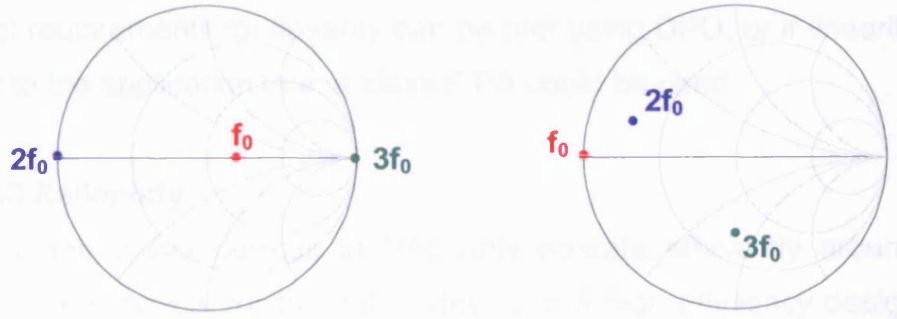


Figure 4-10 Class F matching network performance over an octave bandwidth. By doubling the fundamental frequency, the matching network will no longer present ideal class F impedances. The fundamental now sees the second harmonic short circuit and typically second and third harmonics move to uncontrolled impedances.

Although it does not have the same peak performance advantages as class F over a narrow bandwidth, the class J mode is capable of operating with better efficiency over a wider frequency range. Class J

PAs can achieve this by concentrating harmonic control to the second harmonic only. Class J requires second harmonic output terminations that can be better realised over a broader bandwidth than the specific short circuits of class F, allowing it to achieve power and efficiency performance similar to an ideal class B amplifier, but with much higher bandwidth than commonly seen in other efficiency enhanced PAs [1].

4.7.2 Linearity

A major issue for many switch-mode PAs is their linearity performance. Class F requires the active device be run into compression to keep efficiencies high and therefore tends to introduce distortion that will affect the ability to accurately transmit information or to disrupt other users. In a modern communication network this problem would typically be solved at the system level, using Digital Pre-Distortion (DPD) [1]. However, care must be taken that the power consumption of the digital circuitry does not reduce the overall efficiency to levels below what a more linear standard operating mode would have achieved. If extreme linearity is required above all costs, a class A or class AB design should be used. If system level requirements for linearity can be met using DPD, or if linearity is not key to the application then a class F PA could be used.

4.7.3 Reliability

Since the active devices in PAs only operate efficiently around peak power, it is typical for the active device in a high efficiency design to be quite heavily stressed. However, the active device will be under less thermal strain due to RF cooling, as the majority of DC input energy is converted into RF power rather than dissipated as heat. Therefore, the stress on the active device is primarily due to the high voltages involved. If the mean time to failure is a concern, for instance in a satellite transmitter or even in a base station PA, this stress should be minimised.

Inverse class F puts a greater strain on the active device than class F, as it requires the output voltage swing to extend π / 2 times further than

class F [11]. For designs using active devices with high breakdown limits, primarily wide band-gap devices based on GaN or SiC, inverse class F will be advantageous as it will allow for more power than a class F design. However, if technologies with lower breakdown limits are to be used, such as GaAs or Si LDMOS, a class F design will typically perform best [15].

4.7.4 Dynamic range

Another issue many of the switch-mode PAs suffer from is maintaining their high efficiency levels over a dynamic range of input drive levels – or power back-off. This is important for use in communication systems that use amplitude modulation, since the signal level may vary in amplitude by up to 10 dB in some modulation schemes. This problem is not unique to switch-mode PAs. Indeed class F and class B will have very similar efficiency curves vs. back-off away from compression, as shown in Figure 4-11. The next two sections briefly describe techniques that allow for improved efficiency performance with power back-off, and discuss how they can be combined with a switch-mode PA for best performance.

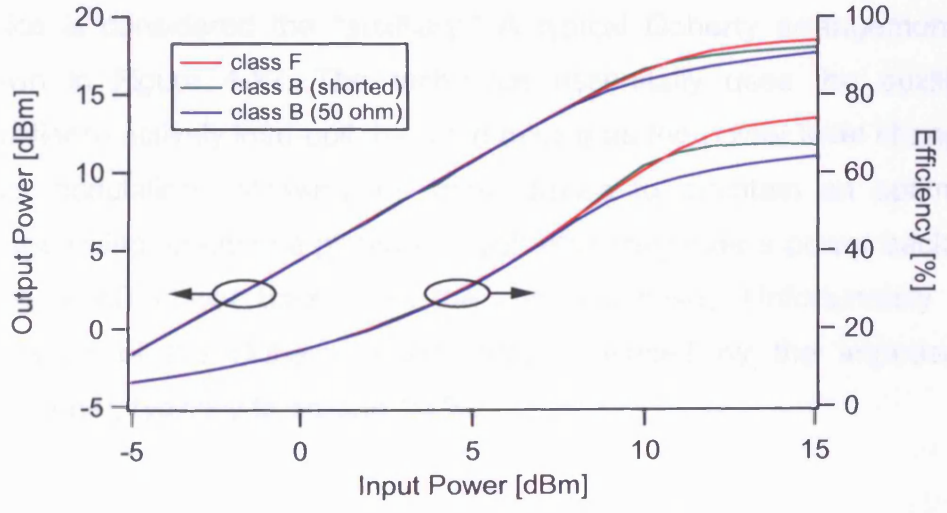


Figure 4-11 Simulated output power and efficiency vs. back-off for three amplifier modes, class F, class B with shorted harmonics and class B in a 50 Ω environment. It is possible to see that all three modes have similar efficiency performance away from compression.

4.8 Potential solutions

In many applications using complex modulation schemes it is the efficiency over various degrees of power back-off that is of primary concern to the designer, rather than the efficiency at a single power level. In this scenario a lower peak efficiency value will likely be traded for a higher average efficiency based on a more statistically representative spread of amplitudes. The class F family achieve their best efficiency enhancements when driven close to compression and as such are especially useful when combined with additional circuit techniques that allow their high peak performance to be harnessed across a dynamic range of input power levels.

4.8.1 Combining class F with load modulation

The most popular architecture in high power communications infrastructure applications to meet these criteria is the Doherty amplifier [1]. First introduced in 1936 for use with vacuum tube amplifiers and more recently implemented using solid state technology, the technique combines two active devices into one load through an impedance transformer [16]. One device is called the "main" device and the second device is considered the "auxiliary." A typical Doherty arrangement is shown in Figure 4-12. The technique essentially uses the auxiliary amplifier to actively load-pull the main device as the power level changes (load modulation), allowing the main device to maintain an optimum voltage swing, creating a plateau of high efficiency over a power back-off range (6 dB power back-off in the classical case). Unfortunately the bandwidth of the Doherty architecture is limited by the impedance transformer, typically to around 10 %.

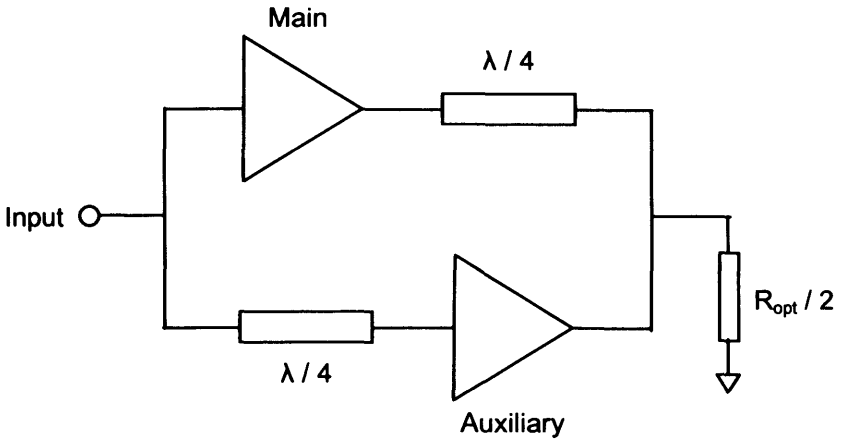


Figure 4-12 Typical Doherty structure combining two active devices through a quarter wave-length transformer (impedance inverter).

Exceptional performance has been demonstrated using a three-way Doherty architecture built with GaN devices [17]. The addition of an extra auxiliary device extends plateau of high efficiency over larger power back-off levels (12 dB). By using GaN devices it is possible to engineer larger voltage swings than possible using Si LDMOS devices, also allowing for improved Doherty performance. A Doherty improvement offering potential would be to design the main and auxiliary devices to operate in a class F mode, combining the potential 100 % theoretical peak efficiency of class F with the power back-off improvement provided by the Doherty architecture. This arrangement has been demonstrated, but overall efficiencies were disappointing [18].

4.8.2 Combining class F with drain modulation

An alternative approach to harnessing the high peak efficiencies of class F tuning over a wider dynamic range of input signals is to replace the load modulation of Doherty amplifiers with a drain modulation technique. Drain modulation can be implemented in a number of ways but effectively involves modulating the DC bias applied to the output PA stage in order to place amplitude modulation onto the RF carrier, or to accommodate the amplitude modulation within the device voltage boundaries.

There is the classical Kahn envelope elimination and restoration (EER) technique [19], where any amplitude modulation is removed from the signal at the RF PA input using a limiter after being sensed ready to be re-introduced after the now constant envelope RF carrier has been amplified using an efficient PA with no amplitude modulation to phase modulation (AM-PM) distortion. The amplitude modulation information, or the envelope, is then reapplied to the RF PA output using an additional signal path with electronics capable of responding within timescales suitable for the envelope frequency. The overall efficiency of this additional path is critical to achieving the potential benefits of the EER technique[1]. Although the relaxation on the need for a linear PA has great potential for a class F implementation, the technique relies on being able to modulate the drain bias fast enough to reapply the modulation successfully. This limitation makes it an unlikely choice for modern modulation schemes with their high complexity and stringent linearity constraints.

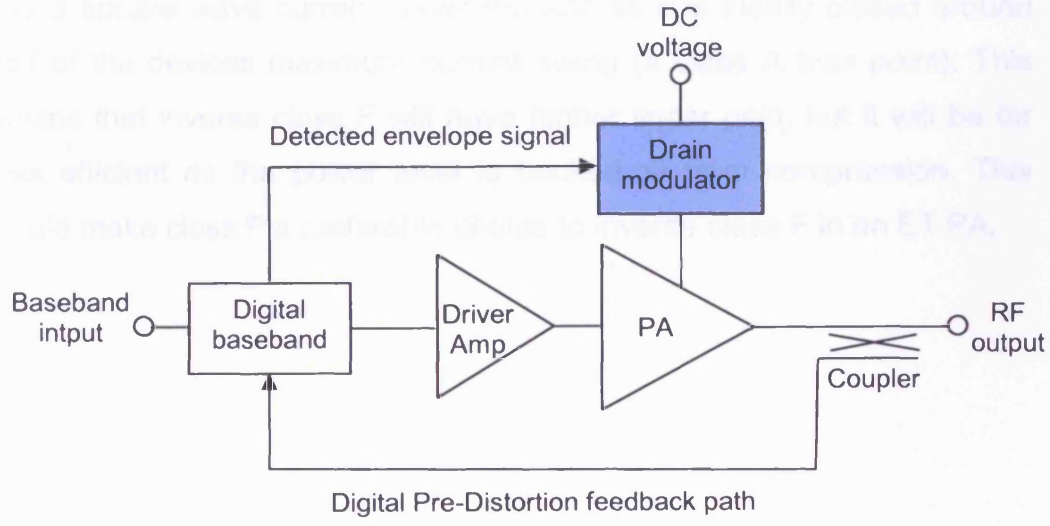


Figure 4-13 A simplified envelope tracking architecture, using a drain modulator circuit to allow the drain bias voltage to "track" changes in the envelope.

The other, more promising drain modulation technique capable of maintaining high efficiencies over a range of input power is envelope tracking (ET). A typical envelope tracking implementation is shown in Figure 4-13. ET methods alter the PA stage output rail voltage in

response to changes in the amplitude of the signal envelope in order to maintain the important rail-to-rail voltage swing required for high efficiency operation [20]. The technique differs from EER in that it allows the PA to respond more efficiently to a varying envelope signal rather than actually applying the envelope variations back onto a constant envelope signal in the PA. The ET technique is again suitable for implementation with a class F PA, although the potential efficiency enhancements are equally limited by the overheads of the additional circuitry required. The potential for greater operational bandwidths in an ET enhanced PA compared to a Doherty may be hampered by mixing the ET technique with the relatively narrowband class F PA.

In applications where the efficiency vs. power back-off is of important, the class F mode is favourable over the inverse class F mode due to the quiescent bias points. Class F has a half rectified sinusoid for its current waveform, meaning it must be biased around pinch-off. Inverse class F has a square wave current waveform and so it is ideally biased around half of the devices maximum current swing (a class A bias point). This means that inverse class F will have higher linear gain, but it will be far less efficient as the power level is backed-off from compression. This would make class F a preferable choice to inverse class F in an ET PA.

4.9 Summary

This chapter has introduced RF PA efficiency enhancement techniques, concentrating on class F. The ideal class F case has been described, as well as attempts made in the literature to introduce more realistic considerations. The disadvantages of class F have been discussed and some potential solutions have been suggested, for example combining a class F PA with an ET circuit to extend its useful dynamic range of efficiency enhancement. The limitations of the existing theoretical analysis for providing a systematic design procedure have been shown. The review has highlighted some specific experiments that could help overcome the limitations and these will be addressed in the following chapter.

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Chapter 5 – Waveform Analysis of the Class F Mode

5.1 Introduction

The existing literature describing class F design is often based on ideal assumptions and as a consequence does not help designers adjust their circuit to achieve optimum performance from real world devices. By studying measured waveforms of a real device in a class F mode it is possible to gain understanding of the necessary process to optimise class F performance in real transistors. During the analysis presented in this chapter, a systematic waveform based design methodology for class F operation is developed that is capable of including the additional considerations required for design using real transistor technologies [1].

The approach is based on waveform engineering, i.e. a combination of RF current and voltage waveform measurement, bias control and active harmonic load-pull using the waveform measurement system to emulate the class F PA environment whilst allowing direct measurement of the current and voltage waveforms. The availability of measured RF waveforms allows the exact identification of performance optimums and importantly allows for an understanding of why the performance is optimal in a given state [1].

Initially measurements are presented for a 2x100 µm GaAs pHEMT biased at a fixed drain bias of 3.5 V for mobile handset applications. The measured results are all taken on-wafer using the waveform measurement system [1]. The frequency of all measurements in this chapter is 1.8GHz. The design guidelines are extended to include an appreciation for the additional trade-offs faced by GaN HFET based class F design by measuring a 2x125 µm GaN HFET device supplied by QinetiQ Ltd. [2].

5.2 Limitations in achievable efficiency performance for real world class F designs

In real word designs it is impossible to achieve ideal class F waveforms, since distortions will be introduced by the non-ideal nature of the active device and the realised circuit environment. The consequence of non-ideal waveforms is that lower performance will be achieved. In this section, a more realistic consideration of the factors limiting class F performance is presented, allowing for realisable performance targets to be set. This is vital if optimised designs are to be achieved, since a designer must understand what the achievable optimum performance is in order to quantify how successful the design has been.

5.2.1 Bandwidth of harmonic control in the output matching network

Network complexity can make it difficult to ideally terminate infinite output harmonics, as would be required for ideal class F waveforms. If a matching network is designed carefully it can accommodate numerous shorts and opens at consecutive harmonics using half wavelength and quarter wavelength reflective sections that scale with frequency. However, this is not always possible due to layout constraints and in many high power designs, using large devices with parasitic packaging networks and sizable output capacitances, the higher harmonics are effectively filtered out before they reach the external matching elements. Therefore, in the majority of class F designs the output matching network is limited to controlling harmonic impedances only up to the third harmonic [3].

The primary consequence of a circuit which has non-ideal terminations at the higher harmonics is that both current and voltage will concurrently exist at that harmonic. As a result, power will be dissipated at this harmonic and less DC energy will be transferred into RF power at the fundamental frequency. This dissipation will lower the efficiency and can be seen as an overlapping between the output current and voltage waveforms, as shown in Figure 5-1.

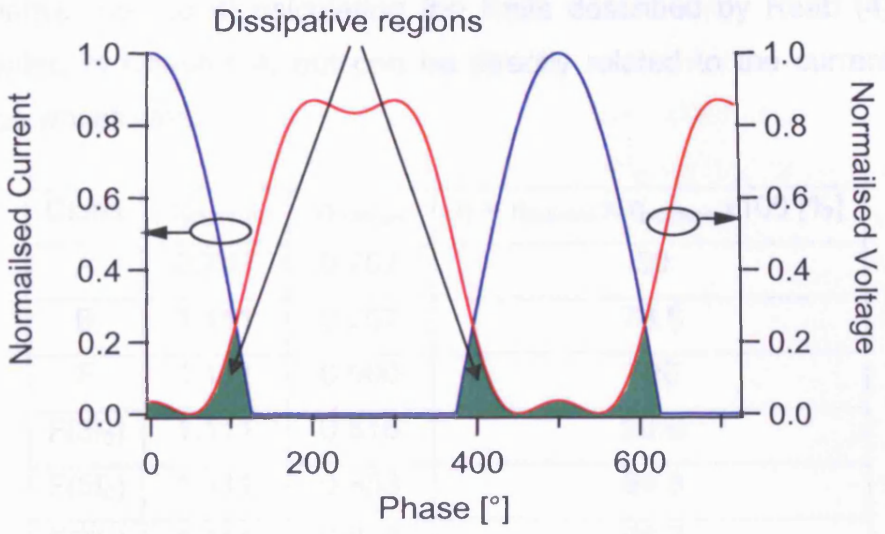

Figure 5-1 – Simulated class F waveforms showing dissipative regions where current and voltage are simultaneously present at the device output. This problem is a direct result of limited bandwidth reducing the voltage waveform to an approximation of an ideal square wave. Pictured voltage waveform contains fundamental and third harmonic only.

In order quantify the impact of a limited bandwidth in the output matching network; it is helpful to describe the circuit's ability to engineer RF waveforms for high efficiency in terms of the fundamental RF and DC components of both the current and voltage waveforms. This approach leads to two factors, termed here as $\eta_{current}$ and $\eta_{voltage}$, which are the ratios of the root mean squared (RMS) fundamental components of the RF waveforms (i_{RF} and v_{RF}) to the DC components (I_{DC} and V_{DC}):

$$\eta_{current} = i_{RF} / \left(\sqrt{2} \times I_{DC}\right) \quad (5\text{-}1)$$

$$\eta_{voltage} = v_{RF} / \left(\sqrt{2} \times V_{DC}\right) \quad (5\text{-}2)$$

Assuming ideal waveforms, the maximum efficiency in various modes of operation can be calculated from these engineered waveform factors (Table 5-1). It is important to note that these values form an upper boundary of achievable efficiency, which will be reduced by offset factors described in the following section. The factors are essentially an

alternative method of calculating the limits described by Raab [4] and presented in Chapter 4, but can be directly related to the current and voltage waveforms.

Class	$\eta_{current}$	$\eta_{voltage}$	$\eta = \eta_{current} \times \eta_{voltage} \times 100$ [%]
A	0.707	0.707	50
B	1.111	0.707	78.5
F	1.111	0.900	100
F($3f_0$)	1.111	0.816	90.6
F($5f_0$)	1.111	0.853	94.8
F($7f_0$)	1.111	0.870	96.7

Table 5-1 – Ideal waveform predicted efficiency in class A, class B, class F with infinite bandwidth and class F with variously limited harmonic control

Extending the design to control higher odd harmonics achieves higher efficiencies, but there is clearly a law of diminishing returns as the improvements in efficiency become small compared to the additional complexity required of the designer to correctly match numerous harmonics. The three harmonic case is sufficient in most design scenarios and although the 90.6 % target is a considerable drop from the ideal 100 % possible from an infinite harmonic design, the circuit will be relatively simple to design and build and forms the basis for the remaining analysis.

5.2.2 Effect of bandwidth on square wave voltage expansion

As stated in Chapter 4, the ideal case fundamental voltage expansion in class F is $4 / \pi$. However, in a bandwidth limited case it can be expected that the voltage expansion will be reduced. By following the analysis of Rhodes [5] for a three harmonic only class F design with a singular solution for optimum performance, the required ratio of third harmonic to fundamental voltage magnitude is exactly 1 / 6. If the fundamental and third harmonic are perfectly anti-phase, this optimal voltage waveform allows the fundamental voltage to extend 1.154 times that of the equivalent pure sinusoid. This gives a voltage extension of 15.4% and a

maximum achievable efficiency of only 90.6 %, assuming the device has produced the perfect class B half rectified current waveform. This is a significant reduction from the ideal 4 / π case which has a voltage extension of 28.0 %. The difference is shown in Figure 5-2 below.

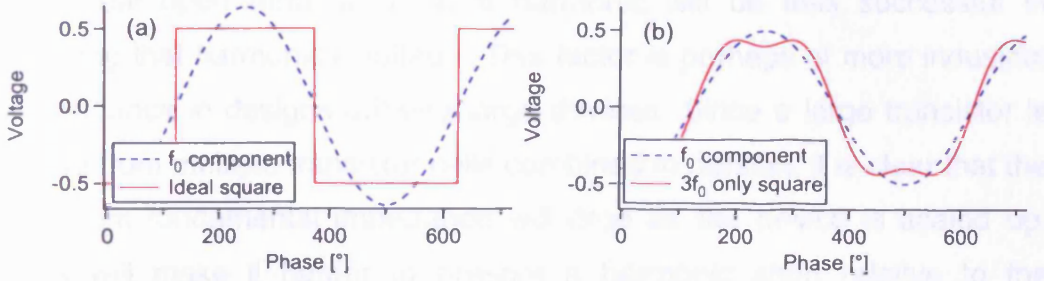

Figure 5-2 Sustained fundamental components for (a) ideal square wave and (b) optimum third harmonic only square wave approximation.

As with the ideal square wave case, Ohms' law demands that the fundamental voltage extension which occurs as the voltage waveform "squares up" to an approximate square wave must also require an equivalent increase in fundamental load impedance to maintain the same current waveform and achieve the full efficiency boost. This load increase should be by the same amount as the fundamental voltage extension, the normalised v_{RF} factor of 1.154.

5.2.3 Losses in the output matching network

In real world circuit implementations, it will not always be possible to achieve ideal terminations and as a result it will be harder to engineer the desired waveforms and efficiency performance will suffer. In Snider's ideal class F [6], the short and open circuit harmonic impedances are located right at the edge of the Smith chart. Circuit losses will introduce an obvious degradation in performance, as a passive circuit with loss will be unable to reflect back enough energy to create perfect short and open circuits. The circuit loss has many variables that relate to the specific implementation method. In this analysis a factor η_{loss} will be included as a simple general measure ranging from zero to one, where a value of one indicates a lossless circuit.

5.2.4 Impedance ratios

In terms of waveform engineering, the effectiveness of the achieved non-ideal short and open circuit terminations at the harmonics is sensitive to the fundamental impedance as well as the individual impedances at the harmonics. For instance, if the fundamental impedance is high then any non-ideal open termination at a harmonic will be less successful in peaking that harmonic's voltage. This factor is perhaps of more industrial significance in designs utilising large devices. Since a large transistor is made from multiple transistor cells combined in parallel, it is clear that the optimum fundamental impedance will drop as the device is scaled up. This will make it harder to present a harmonic short relative to the fundamental load, and again the effectiveness of the short circuit on engineering the voltage waveform will be reduced.

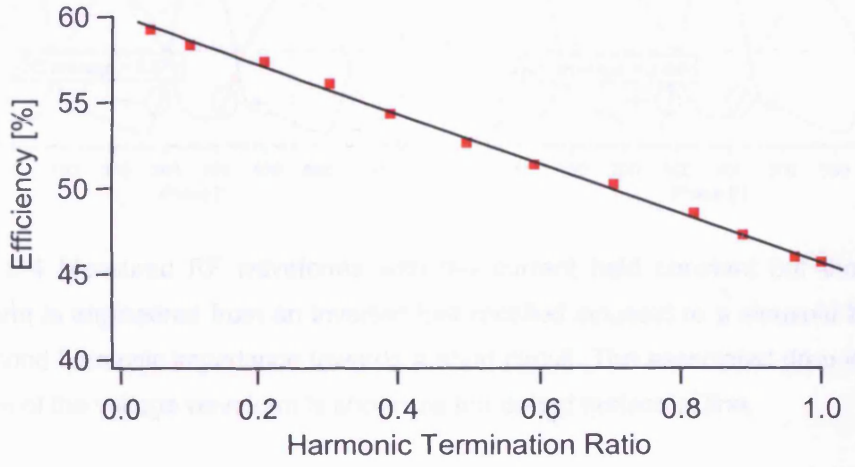

Figure 5-3 Measured efficiency vs. harmonic termination ratio: R_{L2} $2f_0$ normalised by the R_{opt} termination at f_0. A line of best fit has been included.

By considering the second harmonic short, which is used in many real-world circuit implementations for less complex amplifiers as well as class F amplifiers, the effect of impedance ratios on circuit performance can be experimentally established. With the device biased to give a class B current waveform, tuning the second harmonic to a perfect short will convert the voltage waveform from an inverted half-rectified sine wave to a sine wave. In so doing, the DC average of the voltage waveform will be

reduced by a factor of π / 2 whilst the fundamental RF component will remain constant, thus increasing the efficiency.

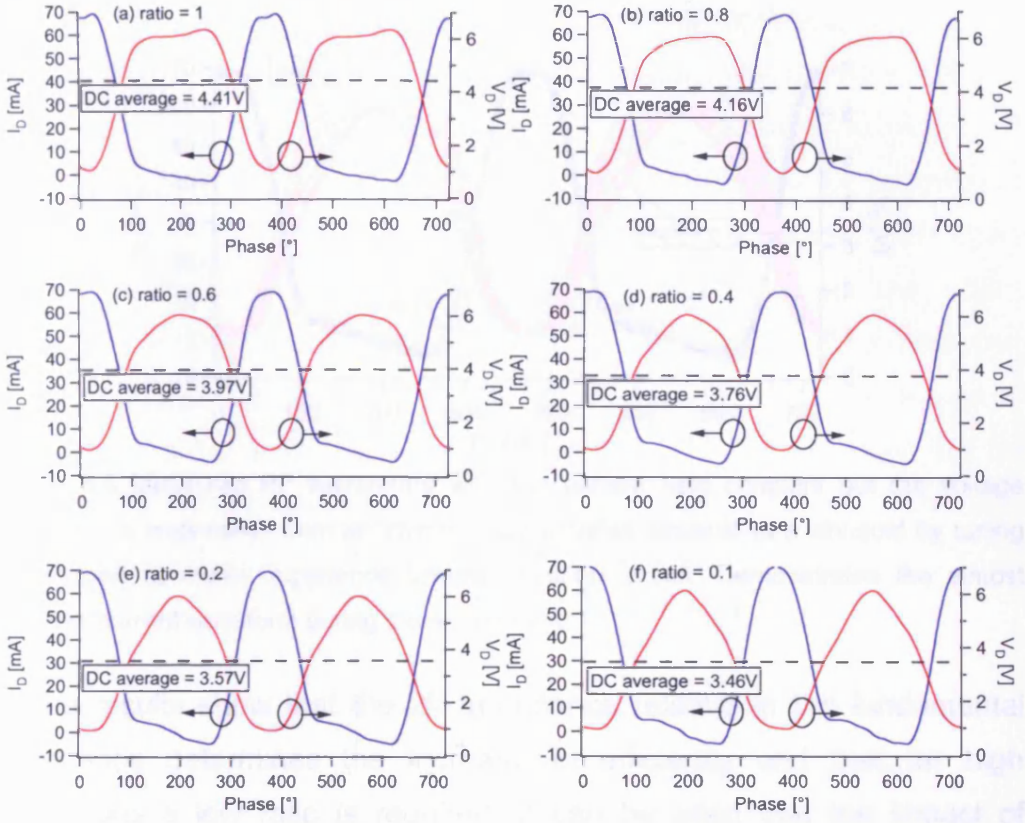

Figure 5-4 Measured RF waveforms with the current held constant but the voltage waveform is engineered from an inverted half rectified sinusoid to a sinusoid by tuning the second harmonic impedance towards a short circuit. The associated drop in the DC average of the voltage waveform is shown as the dotted horizontal line.

To demonstrate this effect, the degree of harmonic tuning at $2f_0$ has been normalised by the fundamental load, R_{opt} for a GaAs pHEMT device biased in class B and measured at 1.8 GHz. Figure 5-3 shows a plot of the measured efficiency as a function of this ratio, which is consistent with the result predicted from simulation by Curras-Francos et al. [7]. The measured waveforms for a selection of ratios are shown in Figure 5-4. These measurements were performed with f_0 and $3f_0$ tuned to R_{opt}, whilst $2f_0$ was tuned to achieve the various ratios. The measurement technique is only possible with the separate harmonic control afforded by active harmonic load-pull loops. A DC voltage offset scaled proportionally to the

ratio was applied at the drain to maintain a constant current waveform. Figure 5-5 shows multiple instances overlaid to demonstrate the constant current waveform.

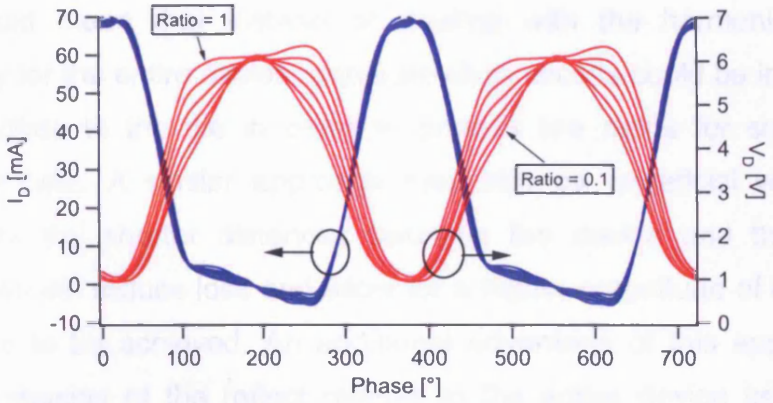

Figure 5-5 Measured RF waveforms with the current held constant but the voltage waveform is engineered from an inverted half rectified sinusoid to a sinusoid by tuning the second harmonic impedance towards a short circuit. Demonstrates the almost constant current waveform during the experiment.

These results show that the $2f_0$ impedance relative to the fundamental impedance determines the increase in efficiency and that for high efficiencies a low ratio is required. It can be seen that the impact of second harmonic tuning on efficiency can be up to 15 %, highlighting just how important good second harmonic shorting will be in achieving high efficiencies. Armed with this result, a designer can now estimate the possible efficiency enhancement for a given harmonic load impedance and decide on the trade-off between matching circuit complexity and efficiency enhancement.

5.2.5 Scaling implications

The implications of this result for the plausibility of scaling up class F designs to larger devices are significant for designers expecting to see very high efficiency values in high power designs. Low ratio values will be harder to achieve in larger devices where R_{opt} values are lower, for example a 100 W LDMOS device with R_{opt} = 5 Ω will require a $2f_0$ short circuit termination of 0.5 Ω or less in order to achieve a ratio of 0.1.

A change in matching strategy may be required to achieve better shorts at $2f_0$ in large devices. One solution may be for device manufacturers to implement harmonic control inside the package and sell the part as a specific class F integrated circuit for limited bandwidth applications [1]. This would mean that instead of dealing with the harmonic shorts externally for the entire device, separate short circuits could be integrated onto or close to the die in order to provide low ratios for subsets of transistor cells. A similar approach may also be beneficial with open circuits as the shorter distances between the device and the reflect termination will reduce loss and allow for a higher magnitude of reflection coefficient to be achieved. An additional advantage of this approach is that the phasing of the reflect relative to the active device cell will be more even across the cells in a large device than if the reflect were presented outside of the discrete packaged transistor, as shown in Figure 5-6.

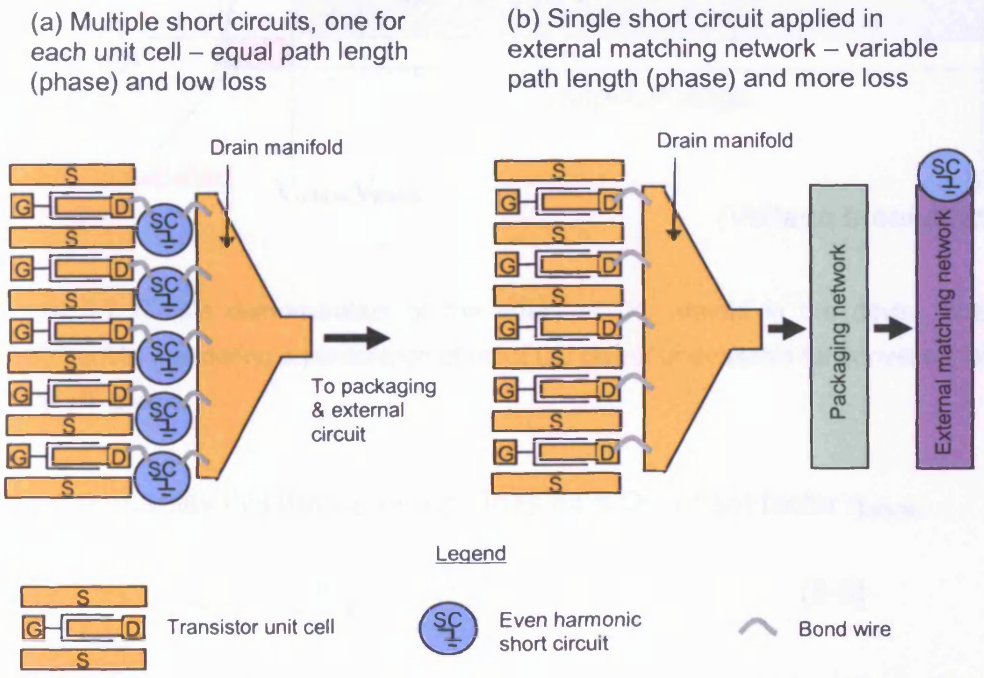

Figure 5-6 Diagram showing two possible techniques for achieving harmonic shorts in the matching network of large transistors (a) on-chip and (b) off-chip.

5.2.6 Effects of a non-ideal active device

A further limitation on achievable efficiency in practical designs arises from non-ideal nature of a real active device. Assuming an FET as the active device, there will be features of the transistor characteristic which make a fraction of the DC power unavailable for conversion into RF power. This will reduce achievable efficiencies; since DC power will be dissipated without creating useful RF power (see Figure 5-7).

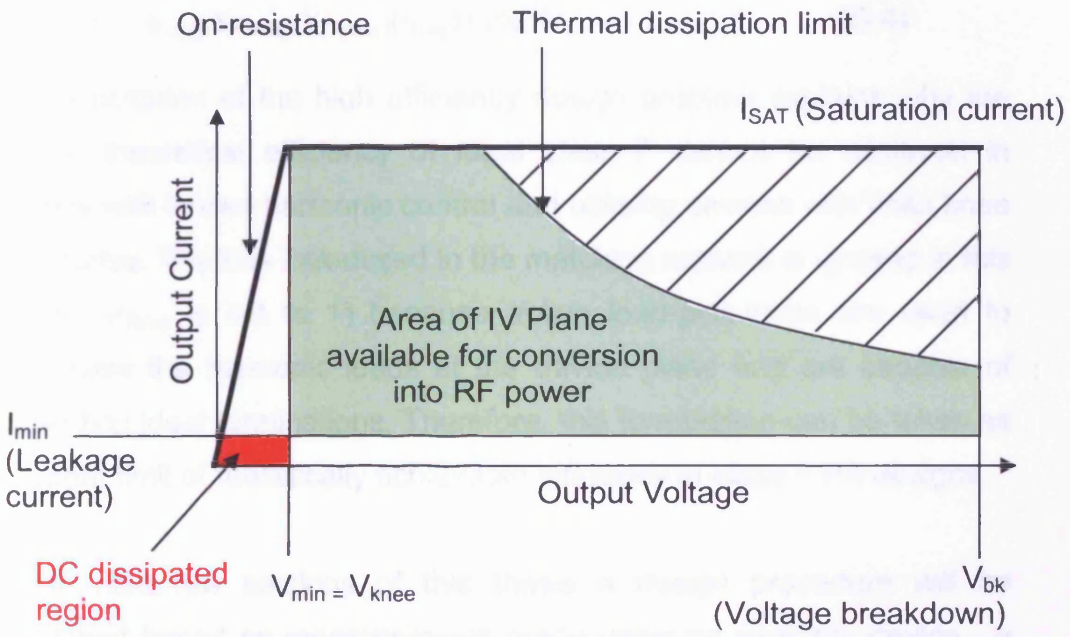

Figure 5-7 Simple demonstration of the effect of DC offsets in the device output characteristics rendering a percentage of input DC power unavailable for conversion into useful RF power.

We can quantify this device related loss as a DC offset factor η_{offset}:

$$\eta_{offset} = \left(1 - \frac{V_{min}}{V_{DC}}\right)\left(1 - \frac{I_{min}}{I_{DC}}\right) \qquad (5\text{-}3)$$

Here the current component (I_{min}) of the DC offset would be affected by a pinch-off problem but can usually be considered zero in most commercial devices. However, the DC voltage offset component in every real device will be highly sensitive to the ratio of knee voltage boundary V_{min} and drain bias V_{DC}. This factor is of particular importance in GaN designs

where current slump can result in an increasing effective V_{min} value as V_{DC} is increased. Properties unique to class F designs with GaN devices will be discussed in more detail in section 5.4 below.

5.2.7 Bounding the real world class F problem

Based on the analysis of the preceding sections that describe the practical constraints in real world class F designs, the maximum achievable efficiency can be written as the product:

$$\eta = (\eta_{current})(\eta_{voltage})(\eta_{offset})(\eta_{loss}) \times 100\,\% \qquad (5\text{-}4)$$

This description of the high efficiency design problem explains why the 100 % theoretical efficiency of ideal class F cannot be achieved in designs with limited harmonic control and utilising devices with finite knee boundaries. The loss introduced in the matching network is ignored in this chapter (η_{loss} is set to 1) because active load-pull loops are used to synthesise the harmonic loads at the device plane and are capable of presenting ideal terminations. Therefore, this formulation can be taken as an upper limit of realistically achievable efficiency in class F PA designs.

In the next few sections of this thesis a design procedure will be developed based on measurements made using an example device - a 2x100 µm periphery GaAs pHEMT device that was measured on-wafer at 1.8 GHz. A DC rail voltage of V_{DC} = 3.5 V was chosen for a mobile handset application to suit this small device. The measurements and simulations of the device can be put into context by performing a calculation of the predicted upper limit of efficiency based on equation 5-4.

If a V_{min} of 0.75 V is selected for the knee voltage (based on DC-IV measurements) and no short channel effects are assumed given the low drain bias, using equation 5-3 the η_{offset} factor can be calculated:

$$\eta_{offset} = \left(1 - \frac{0.75V}{3.5V}\right)\left(1 - \frac{0}{I_{DC}}\right) = 0.786$$

Similarly the $\eta_{current}$ and $\eta_{voltage}$ can be calculated as in table 5-1 for a three harmonic only design based on the ideal waveforms to give 0.906. Finally, assuming lossless matching networks ($\eta_{loss} = 1$) due to the use of the active load-pull measurement system gives an estimated target efficiency of $\eta = 71.19$ %. The design procedure of the following section will aim to achieve this value.

5.3 Waveform assisted class F design strategy

Analysing the output current and voltage waveforms of the device to be used in a class F design is an essential part of the class F design process. Indeed, the shape of the output waveforms defines class F operation, so without the waveform data conclusive verification that the designed amplifier is operating in class F is impossible.

5.3.1 Simulated waveforms vs. measured waveforms

For the majority of RF designers, waveform data can only be generated by device models in the simulation environment. Designing a complex PA structure such as class F in the CAD environment requires an accurate non-linear model. Constructing a non-linear model capable of reliably reproducing the waveforms and performance of a device in a class F circuit environment is not a trivial activity. Many commonly available device models are optimised towards more conventional designs, with most of the effort spent to insure sweeps of P_{OUT} vs. P_{IN} are accurately modelled. Consequently, models not optimised for harmonically tuned designs can loose accuracy or become unusable away from their intended operating region. For example, higher harmonics which are important in shaping the class F waveforms are unavailable in some models. Due to the complex nature of class F designs this can limit the accuracy of the waveform results generated by the model and can lead to final designs operating with lower performance than expected, without an explanation from the simulator.

If it is assumed that in many cases the model cannot provide sufficiently accurate waveform data for a truly optimised class F design, then performing RF time-domain measurements on the device becomes necessary. It is expected that device models capable of accurately describing switch mode PA behaviour at GHz frequencies will gradually become available. The waveform assisted design rationale described here will remain valid in a CAD based design as the current and voltage waveforms engineered using the measurement system can simply be

generated in simulation by the device model and appropriate circuit elements.

5.3.2 Design rationale

The primary rationale of the waveform assisted approach is to separate the odd harmonics into the voltage waveform and the even harmonics into the current waveform and then to optimise the various harmonic components to support the best possible power and efficiency performance. This approach to gaining a half-rectified current waveform and a square voltage waveform that have been optimised for a given transistor technology is only possible if reliable waveform data is available so that the constituent harmonic components can be analysed. The developed design procedure rapidly produces optimum bias and impedance conditions and has been shown to systematically achieve results extremely close to the theoretical limits for a number of transistor technologies [1, 2, 8, 9].

5.3.3 Engineering the current waveform

FET devices are essentially a voltage controlled current source. Therefore, in order to engineer the current waveform, the gate voltage must be manipulated. The gate voltage can only be manipulated by selecting a DC bias point, an RF drive level at the fundamental frequency and by allowing different harmonics to shape the input RF voltage wave. Work has been done at sub-GHz frequencies to suggest the effectiveness of other class F drive waveforms [10], but here we shall concern ourselves only with a sinusoidal RF drive signal at the fundamental frequency.

To set up an RF transistor in various PA classes, the designer typically selects a constant bias point for all input drive levels, without considering in detail the harmonic content of the current waveform created. In the case of a class F amplifier, it is logical to bias the gate at pinch-off to achieve a class B half-rectified current waveform. This waveform should ideally contain only even harmonic components with no odd harmonic

components present. However, in real-world devices the pinch-off characteristic is often softened, and as a result there are a number of possible bias points that can be selected for an acceptable approximation of class B. This softer transfer characteristic can be seen in Figure 5-8.

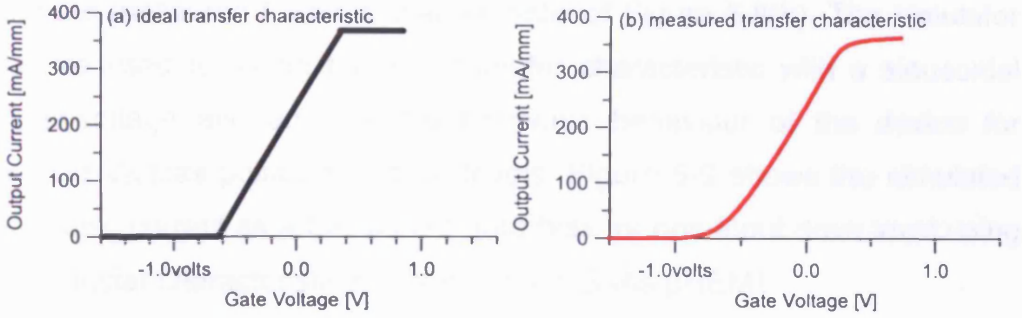

Figure 5-8 Ideal and measured DC transfer characteristics for a 2x100 µm GaAs pHEMT measured along the Ropt load-line. The softer turn-on and saturation of the measured transfer characteristic that is device specific and will generate additional harmonic content is clearly visible in (b).

Importantly, these approximations of an ideal half rectified sine wave will contain varying degrees of the odd harmonic components, depending on the transfer characteristic of the device. This consideration is complicated by the magnitude of the input drive signal, as different harmonic quantities will be generated at different drive levels. Furthermore, if the device is driven into the knee region, as is required for class F, harmonic content will also be generated from the compression process.

For ideal class F operation it is of utmost importance that the current waveform does not contain odd harmonic components. This is because odd harmonic components at the same frequencies will be present in the voltage waveform, and if they are present in both waveforms power will be dissipated at that harmonic frequency and the efficiency performance will suffer. In order to optimally engineer the current waveform to contain minimal odd harmonic components the gate bias should be carefully selected to null all odd harmonic components. Then by applying a large odd harmonic impedance the harmonic voltage components can be generated with minimal dissipation.

In order to find the optimum class F gate bias point, the device transfer characteristic must be tested to look for the odd harmonic nulls. This can be achieved by measuring the DC transfer characteristic along the load-line to be used in the design (usually R_{opt}) and then transferring this data to a simple software simulation. This was done using Wavemetrics IGOR and the measured transfer characteristic of Figure 5-8(b). The simulator can be used to excite the R_{opt} transfer characteristic with a sinusoidal input voltage and analyse the harmonic behaviour of the device for varying V_G bias points and drive levels. Figure 5-9 shows the simulated harmonic current as a function of gate bias for one input drive level using the transfer characteristic measured for a GaAs pHEMT.

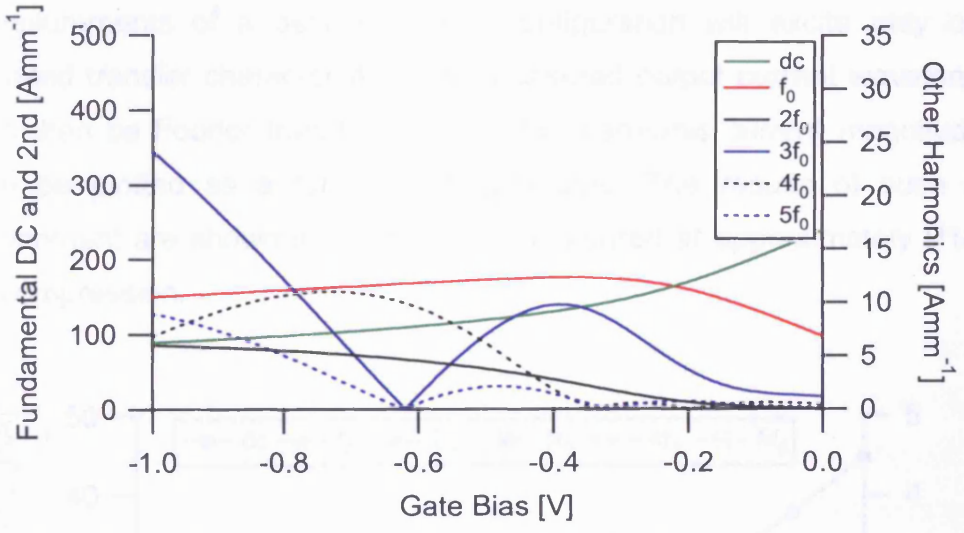

Figure 5-9 Simulated harmonic current magnitude vs.V_G for a specific drive level where odd harmonic nulls occur simultaneously. Simulation is based on a measured transfer characteristic for a 2x100 µm GaAs pHEMT.

For this device, at this specific drive level and load trajectory, it is possible to select a bias point that nulls both the third and fifth harmonics. Unfortunately this is not always possible due to the shape of device transfer characteristics. Indeed, in the same device at the great majority of power level and load trajectory combinations the odd harmonics do not simultaneously null. Therefore, the largest odd harmonic should be prioritised in designs, usually the third harmonic.

The ability to measure RF waveforms allows the RF harmonic current components to be directly analysed. This has been performed on the same GaAs pHEMT, in order to verify the gate bias sweep technique using real RF signals. A valid analysis of the effect of gate bias on the measured RF harmonic current for the R_{opt} transfer characteristic can only be achieved by sweeping the gate bias whilst all harmonic components are load-pulled to the same R_{opt} impedance and the device is driven at a constant input level. This experiment requires a resistance equal to R_{opt} be inserted into the drain feed. This resistance ensures that the DC bias point will always stay on the R_{opt} load-line, and is akin to load-pulling the DC harmonic component to R_{opt}. If the other harmonics of interest are also load-pulled to R_{opt} using active load-pull, then all measurements of a device in this configuration will excite only one isolated transfer characteristic. The measured output current waveforms can then be Fourier transformed and the harmonic current magnitudes can be plotted as a function of gate bias. The results of such an experiment are shown in Figure 5-10, measured at approximately P1dB of compression.

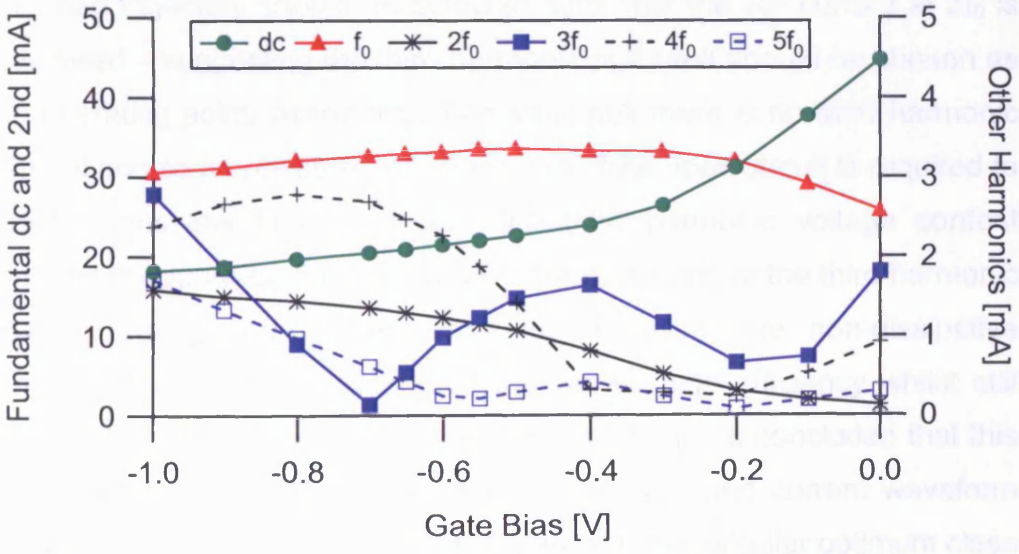

Figure 5-10 Measured harmonic current magnitude vs. V_G for a single drive level and transfer characteristic, calculated from Fourier coefficients of measured RF output current waveforms.

The measured harmonic behaviour shows that for this device, at the working load and drive conditions, no gate bias exhibits for ideal class B behaviour, since the $3f_0$ and $5f_0$ currents do not simultaneously null. The design choice for a class B operating point must instead be made on performance criteria such as power and efficiency. The question is which bias point should be chosen for class F operation?

In chapter 4 the work of Giannini [11] was described where a class F bias point was proposed at 10 % of I_{MAX}. This was to ensure that the third harmonic current was in anti-phase to the fundamental component, which is necessary for a square voltage waveform. Clearly there is a phase change in the third harmonic current after the null and for a realizable positive impedance to exist at the third harmonic, any bias point from the null point onwards will allow a squared-up the voltage waveform. However, the selection of a bias point away from the null will result in an unnecessarily dissipative current waveform when combined with the squared voltage waveform and will therefore reduce efficiency.

So for optimum class F operation the value of V_G for the given drive level and load trajectory should be selected such that the RF current at $3f_0$ is minimised – suggesting the third harmonic null itself should be chosen as the operating point. At the third harmonic null there is no third harmonic content and so no phase exists. Here an infinite open circuit is required to satisfy ohms law and still create the third harmonic voltage content required to square-up the voltage waveform. Biasing at the third harmonic null or turning point is essential for achieving the non-dissipative termination at the third harmonic required for high efficiency whilst still allowing the voltage waveform to square up. It can be concluded that this bias point alone will create the optimum voltage and current waveform combination that will present the designer with the singular optimum class F solution.

For this device, the optimal class F bias point is where the third harmonic nulls at V_G = -0.7 V. This optimum class F bias point corresponds to a

current waveform with a conduction angle slightly lower than for ideal class B resulting in a higher value of $\eta_{current}$ and therefore higher efficiency is possible than predicted using equation 5-4, but at the cost of a small reduction in fundamental output power.

5.3.4 Drive level and the current waveform

Analysing the effects of varying drive level as well as gate bias on the harmonic current for the R_{opt} transfer characteristic can be rapidly performed by using the same Wavemetrics IGOR software simulation of the measured GaAs pHEMT DC transfer characteristic used in the previous section. The simulation can be used to excite the R_{opt} transfer characteristic for a large number of drive level and bias voltage combinations. The result from this simulation can be seen in Figure 5-11 where the simulated third harmonic current null is a strong function of drive level as well as gate bias.

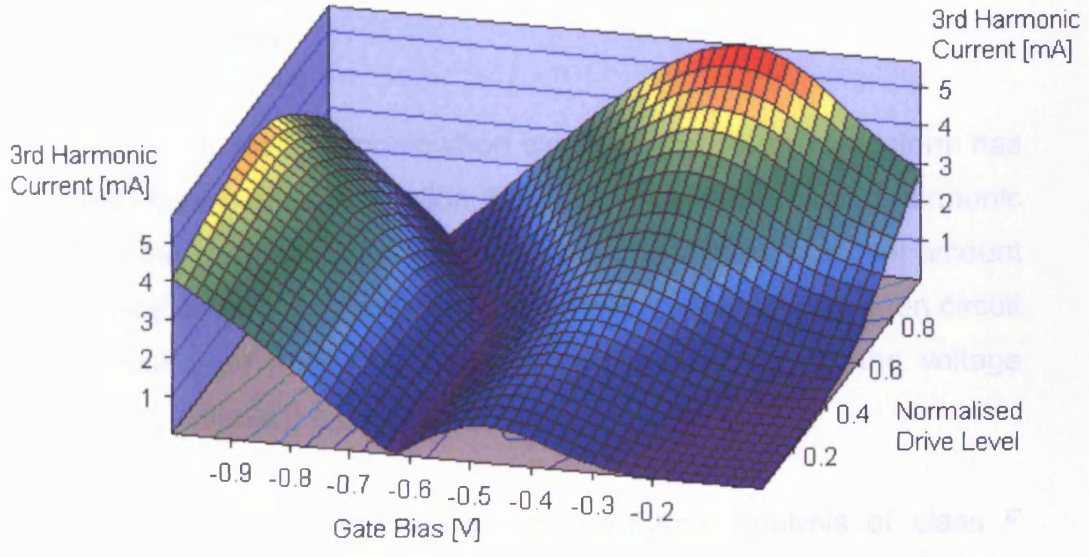

Figure 5-11 $3f_0$ current magnitude as a function of gate bias and normalised drive level (ranging from linear operation to hard compression) generated from a simulation of the device R_{opt} transfer characteristic.

Figure 5-11 indicates the combined effect of V_G and drive level on the design space, showing that the V_G value required to null $3f_0$ current becomes more negative as the device is driven harder. This is to be

expected, since biasing more negatively in an FET will reduce the gain and therefore reduce the amount of compression seen in the output current waveform as it interacts with the knee. Biasing more negatively will also reduce the output power. This detailed information about the location of the harmonic nulls or "sweet-spots," can be used by the designer select an appropriate bias point and drive level aware of where the current waveform will be correctly engineered.

5.3.5 Engineering the voltage waveform

In a systematic class F design it is best to engineer the voltage waveform after the current waveform has been correctly engineered. In a three harmonic only design, the voltage waveform is engineered to an approximate square wave by tuning 2^{nd} and 3^{rd} harmonics to short and open circuits respectively. By converting the output voltage waveform to a square wave, the fundamental voltage component is increased allowing power and efficiency levels greater than those in an equivalent class B design to be achieved.

The effect of the even harmonic short circuit on the voltage waveform has been described in detail in section 5.2.4. Given the correct odd harmonic content in the current waveform, preferably only a small residual amount when biased at the third harmonic current null, presenting an open circuit acts to peak – or maximise the odd harmonic energy in the voltage waveform to achieve the correct shape.

However, questions from the existing literature's analysis of class F remain regarding how high the third harmonic impedance actually needs to be to achieve the optimum voltage waveform. If almost no third harmonic current is present in the current waveform when it is biased at the harmonic null point, it would be desirable to present a large impedance, approaching an ideal open circuit but remaining a finite value so that exactly the correct degree of third harmonic voltage is created. An experiment was established in Agilent Advanced Design System (ADS) by constructing a simple model of the same GaAs pHEMT device to

investigate the optimum tuning ratio at the third harmonic. Figure 5-12 shows the result of this simulation where the effect of the third harmonic termination normalised by the fundamental load on drain efficiency has been plotted.

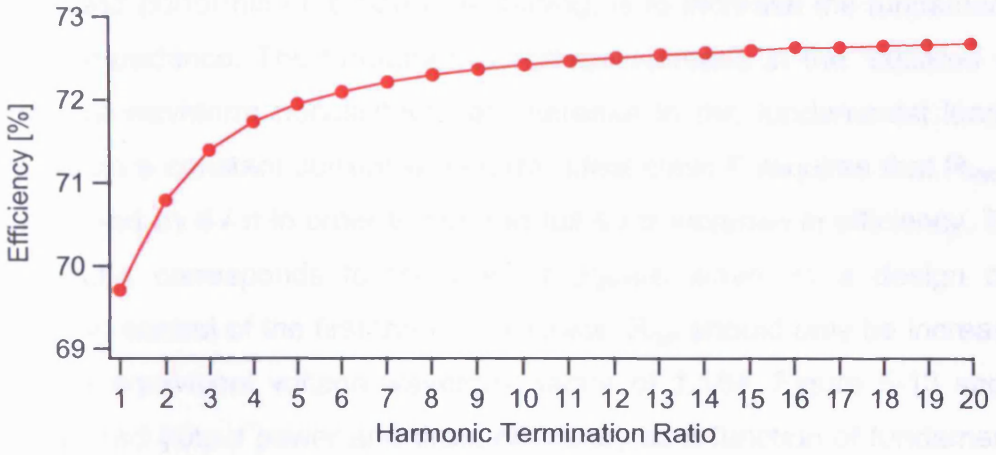

Figure 5-12 Simulated harmonic termination ratio R_L at $3f_0$ normalised by R_{opt} at f_0.

It can be seen in Figure 5-12 that increasing the third harmonic load impedance has a diminishing effect on boosting efficiency beyond a certain ratio. A ratio of approximately five times the fundamental load appears to be the breakpoint above which further increases appear to yield less than a 1 % increase in efficiency. This simulation has given an indication that the actual value of the third harmonic impedance is not overly critical, so long as it is significantly higher than the fundamental. This result is encouraging for practical circuit implementations and mirrors the conclusion of Cripps' book [12].

However, this non-critical open harmonic termination does not help in understanding why the transistor is willing to "drop" into a high efficiency state by simply biasing and tuning the device correctly and then applying a somewhat arbitrary high impedance at the third harmonic. The answer to this question may lie in the fact that the device itself has an entropic desire to reach the most efficient equilibrium where its output voltage waveform supports the maximum amount of fundamental voltage within

the boundary constraints of the device itself. This idea will be examined further in the following sections.

5.3.6 Increasing the fundamental load

The final stage in optimising a class F design, after selecting the gate bias and performing the harmonic tuning, is to increase the fundamental load impedance. The fundamental voltage increase in the "squared up" voltage waveform necessitates an increase in the fundamental load to maintain a constant current waveform. Ideal class F requires that R_{opt} be increased by 4 / π in order to see the full 4 / π increase in efficiency. This condition corresponds to the perfect square wave. In a design only utilising control of the first three harmonics, R_{opt} should only be increased by the equivalent voltage waveform factor of 1.154. Figure 5-13 shows measured output power and drain efficiency as a function of fundamental load impedance for the same class F tuned GaAs pHEMT used so far in this chapter. It is possible to confirm from these measurements that the optimum power and efficiency performance does occur at approximately 1.154 x R_{opt}.

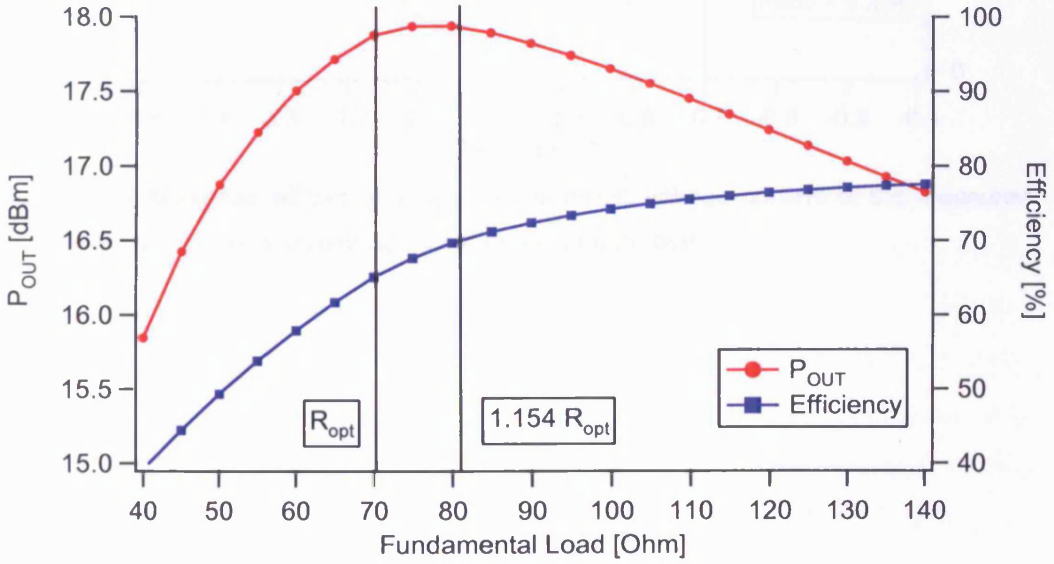

Figure 5-13 Measured output power and drain efficiency as a function of fundamental load impedance for the three harmonic class F case (second harmonic shorted, third harmonic open).

5.3.7 Verification of successful tuning

The optimum class F behaviour will only occur if the current at $3f_0$ remains null. Unfortunately, because class F requires a near open circuit termination at the third harmonic, the $3f_0$ current cannot be directly measured to ensure it has remained null. To verify that the optimum class F condition has been achieved, DC gate bias is swept and the ratio of $3f_0$ voltage to f_0 voltage, the output power and the efficiency are observed. Figure 5-14 shows the performance results of this gate sweep and Figure 5-15 shows the output waveforms. The optimum DC gate bias, V_G, is confirmed by the measurement as -0.7 V, where the efficiency has been maximised.

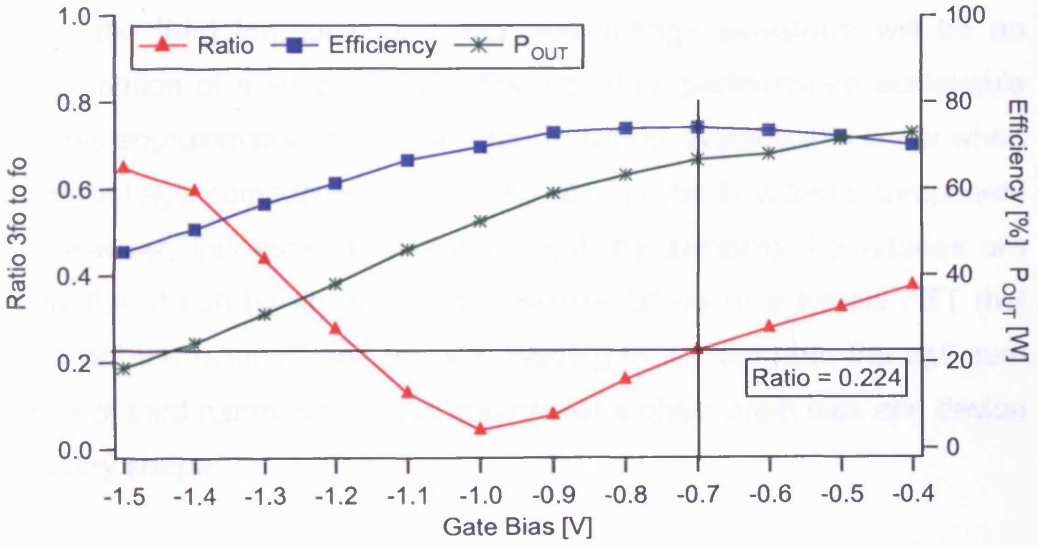

Figure 5-14 Measured efficiency, P_{OUT}, and harmonic voltage content of the measured waveforms as ratio of $3f_0/f_0$ plotted as a function of gate bias.

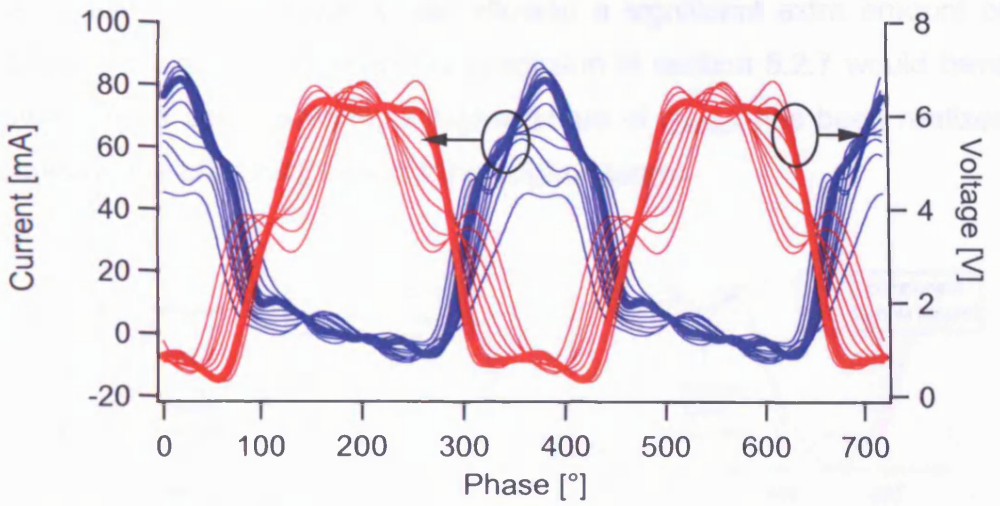

Figure 5-15 Measured current and voltage waveforms from the final V_G sweep, the optimum waveforms are highlighted with thicker lines.

If only the third harmonic is tuned, the voltage waveform will be an approximation of a square wave. The optimum performance achievable from this approximated voltage waveform can be predicted to occur when the $3f_0$ voltage component is 1 / 6 the size of the f_0 voltage component [5]. However, this estimate assumes that the transistor boundaries are ideally flat. It can be shown using a simple DC-IV of a typical FET that this is not the case in real devices, leading to a change in the optimum degree of third harmonic voltage content for a given drain bias and device boundary shape.

It can be seen in Figure 5-14 that the actual optimum occurred when extra third harmonic voltage was present at a ratio of 0.224 compared to the fundamental voltage component. This result can be explained because the predicted ratio of 1 / 6 assumes a flat vertical knee boundary. However, the finite slope of a real device's knee boundary allows a larger $3f_0$ voltage and therefore a larger f_0 voltage to be generated. This effect is demonstrated in Figure 5-16 below. The impact of the knee boundary is particularly high in this example as the device on-resistance is fairly high compared to the rail voltage. In designs utilising larger devices or operating from a larger rail voltage the boundary condition would approximate much better to the ideal flat line. However,

in the case of this device it has allowed a significant extra amount of voltage to be generated than the prediction in section 5.2.7 would have allowed. As a consequence, a higher value of $\eta_{voltage}$ has been realized increasing the efficiency beyond the original target.

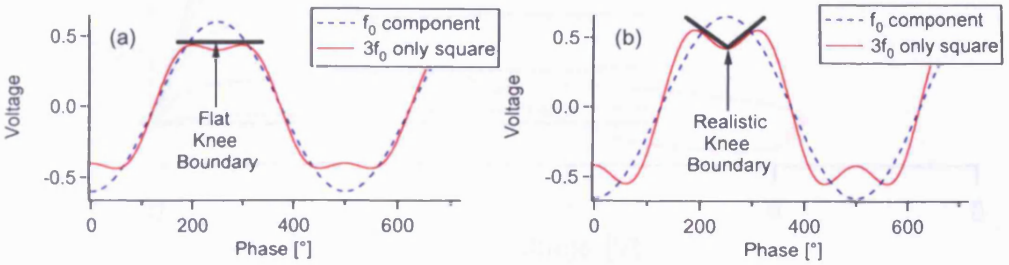

Figure 5-16 Diagrams showing the increase in third harmonic and consequently fundamental voltage that can be sustained across a sloped boundary condition (b) as opposed to a flat boundary condition (a).

5.3.8 Results

After following the above design procedure, an optimal class F experiment was completed achieving an efficiency of 75.01 %. This value exceeds the original predicted efficiency target of 71.19 % due to the influence of the real device on the engineered waveforms. This was in part to due to the selection of a current waveform with slightly lower conduction angle than the ideal class B waveform used in the calculation of equation 5-2. However, the main discrepancy came from the assumption made in the calculation using equation 5-3, which assumes a flat transistor boundary condition. Due to the scale of the device and the rail voltage used in the example, the load-line interaction with the slope of the knee is far more pronounced than would have been the case in many other applications where the output voltage swing itself is larger. This is because the variation of V_{min} with current density that forms the on-resistance would become less significant to overall efficiencies when the rail voltage is larger. This is perhaps best illustrated by looking at the dynamic load-line and DC-IV shown in Figure 5-17.

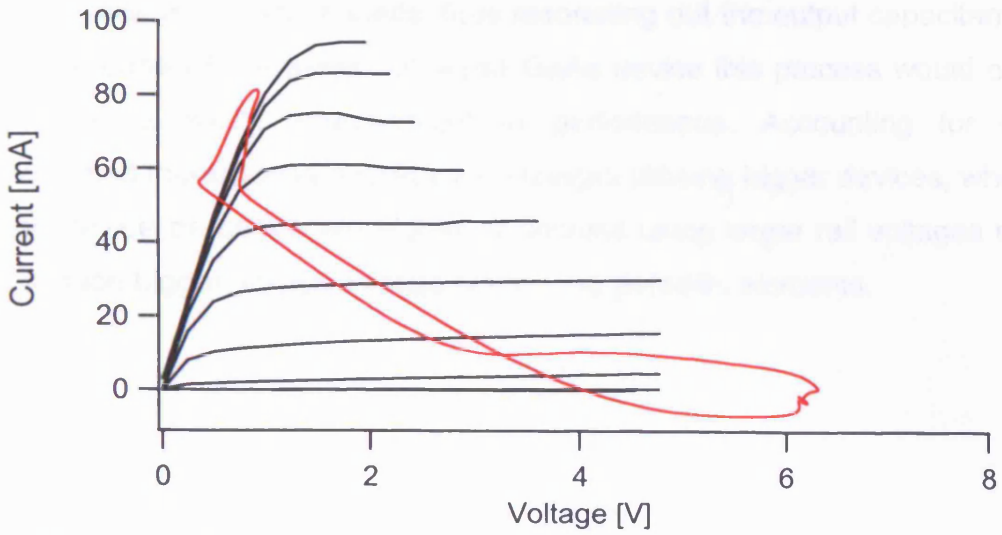

Figure 5-17 Dynamic load-line for the optimum class F case overlaid on the device DC-IV characteristic (V_G = -1 V to +0.8 V in 0.2 V steps).

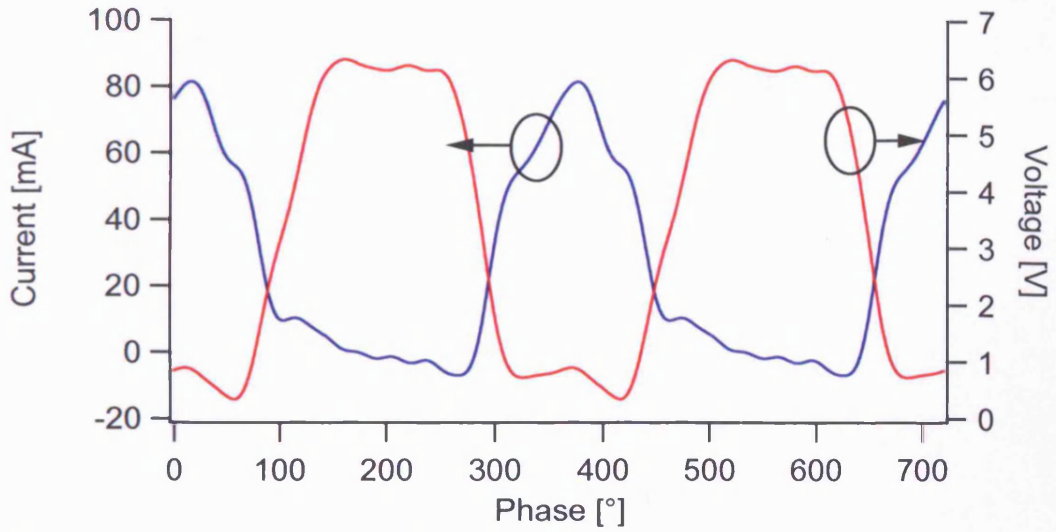

Figure 5-18 The measured output current and voltage waveforms corresponding to the dynamic load-line shown in Figure 5-17.

Figure 5-18 shows the measured output voltage and current waveforms of the completed class F design. The waveforms do not match the theoretical ideals exactly, primarily due to the tuning of only a finite number of harmonics. The device output capacitance C_{ds} also plays a minor role in distorting the waveforms. This effect can be seen in the features at the edge of the current waveform peaks, caused by the third harmonic voltage generated in class F creating a current flow across C_{ds}. The C_{ds} distortions could be removed by tuning the impedances at f_0 and

$3f_0$ to slightly inductive loads, thus resonating out the output capacitance. In the case of this small, on-wafer GaAs device this process would only provide a slight improvement in performance. Accounting for C_{ds} becomes increasingly important in designs utilising bigger devices, where the device parasitics are higher or designs using larger rail voltages that produce bigger voltage swings across the parasitic elements.

5.4 Issues specific to class F in GaN HFETs

Many device technologies which are available for use in class F design have not yet had the extensive modelling investment necessary to breed confidence in their application to the taxing class F problem. A good example of such a technology is the GaN HFET. Problems with shifting knee boundaries and other device imperfections can complicate designs but not necessarily make them impossible. In this section a class F design using a developing GaN technology is used to demonstrate how good class F performance can still be achieved [2].

An initial investigation of the optimal class B behaviour of a 2x125 μm GaN HFET device at 15 V drain bias found a drain efficiency of 60 % at a power density of 4 Wmm^{-1}. For a higher efficiency GaN class F design the maximum achievable power will be reduced in favour of higher efficiency values. By selecting a larger fundamental load, which will reduce the working current density, the effect of the η_{offset} term on the efficiency will be minimised, thus boosting efficiency.

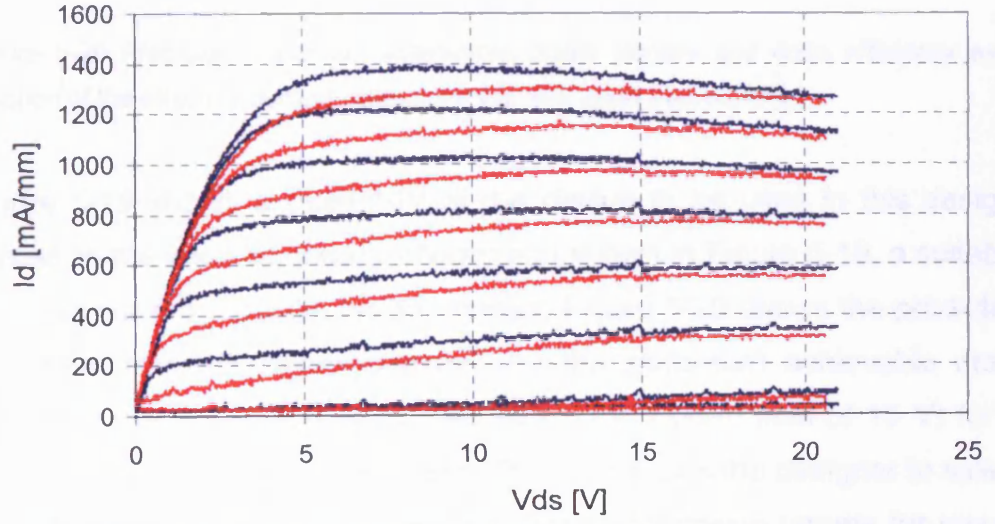

Figure 5-19 Pulsed-IV measurements showing the different RF boundaries for two bias conditions: zero bias state in blue (V_G = 0 V,V_D = 0 V) and class B bias state in red (V_G = -6.5 V,V_D = 15 V).

Fortunately GaN HFET devices have relatively high current densities and so sacrificing a fraction of the current swing in order to achieve higher efficiency values can be a desirable option, since the overall power density may still exceed rival technologies. In order to make this decision it is necessary to investigate the true RF knee boundary conditions of the device when operating in a Class B bias state. This can be achieved using pulsed-IV measurements made from an appropriate off-state bias point or a detailed RF waveform mapping of the knee region.

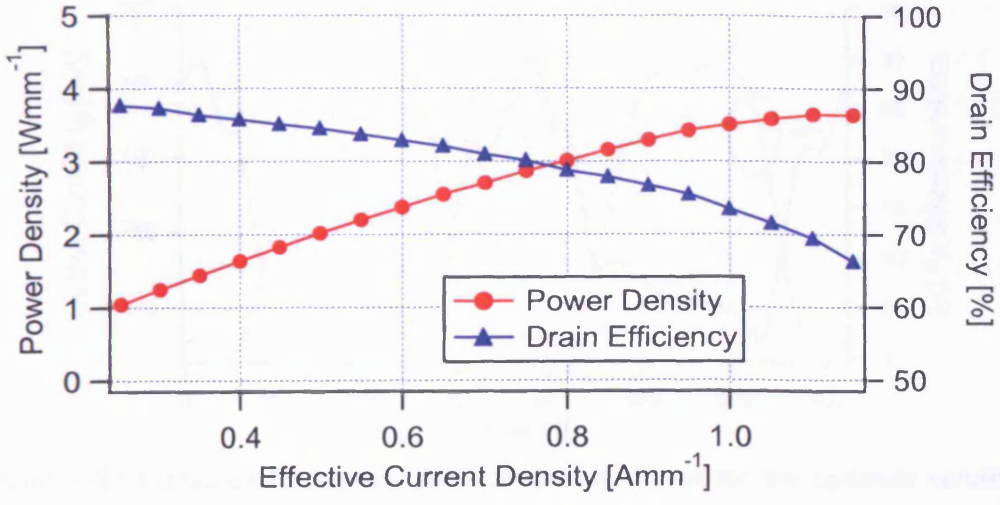

Figure 5-20 Predicted maximum achievable power density and drain efficiency as a function of the effective current density for the 15V drain bias condition.

Figure 5-19 shows a pulsed-IV of the device to be used in this design. Based on the knee boundary information shown in Figure 5-19, a suitable effective current density can be chosen. Figure 5-20 shows the predicted maximum class F power density and the maximum achievable drain efficiency (based on the η_{offset} calculation for a drain bias of 15 V) for a range of effective current densities. This plot allows the designer to select an optimum effective current density based on design targets for power and efficiency. For this design a current density of approximately 0.77 Amm^{-1} was selected, giving an expected drain efficiency of 80 % at a power density of 3 Wmm^{-1}. This operating condition requires a fundamental load impedance of 220 Ω.

With the fundamental load impedance selected, a similar design procedure as performed for the GaAs pHEMT could be performed, resulting in an optimal solution. Measured current and voltage waveforms for the optimal case when all harmonic load impedances have no reactive components are shown in Figure 5-21. Figure 5-22 shows the dynamic load-line for this mode of operation overlaid on the device DC-IV. Performance values of 76 % drain efficiency at 3 Wmm^{-1} power density were achieved in this configuration.

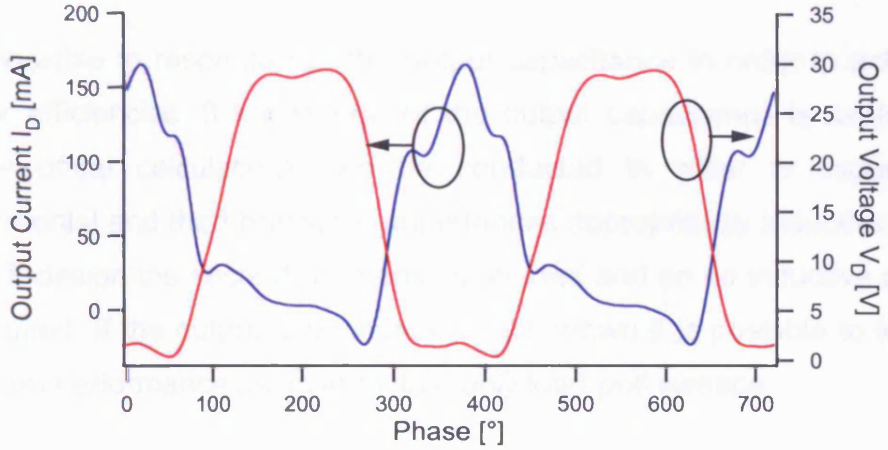

Figure 5-21 Measured RF current and voltage waveforms for the optimum condition before tuning out C_{ds}.

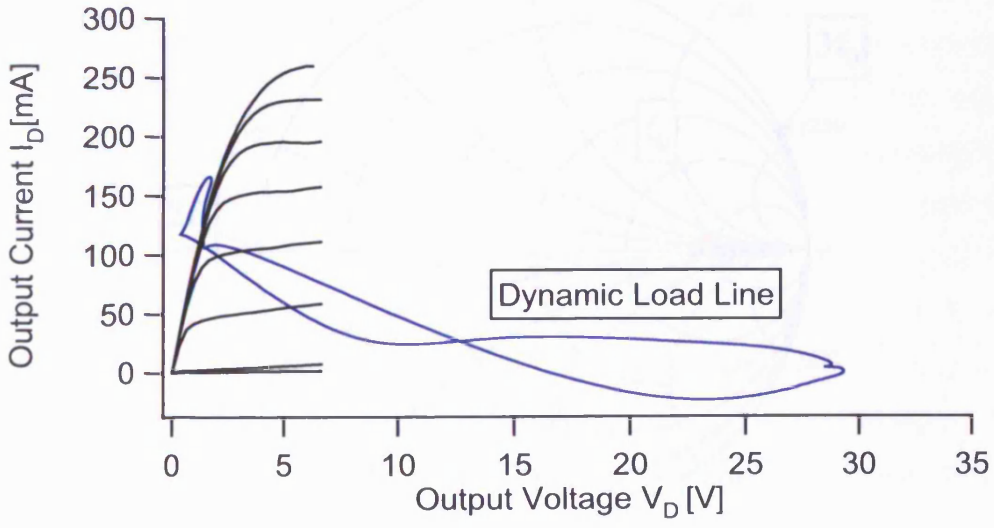

Figure 5-22 Measured RF dynamic load-line for the optimum condition before tuning out C_{ds} overlaid on the device DC-IV.

It can be seen in Figure 5-21 that the current waveform is far from the ideal half rectified sine wave expected. There are features or "wings" at either side of the current maxima and a current flow in the off period. These effects are caused by the odd harmonic voltages (in particular third harmonic voltage) generated in class F creating a current flow across the device output capacitance, C_{ds}. The result of the non-ideal waveforms is a reduction in efficiency. This problem becomes increasingly significant in GaN designs operating at higher drain biases, since the increasing voltage swings will generate larger displacement currents.

It is possible to resonate out the output capacitance in order to achieve higher efficiencies. If knowledge of the output capacitance is available, simple offset calculations can be conducted in order to make the fundamental and third harmonic impedances appropriately inductive. In a class F design the second harmonic is shorted and so no inductive offset is required. If the output capacitance is not known it is possible to locate optimum performance using inductive only load-pull sweeps.

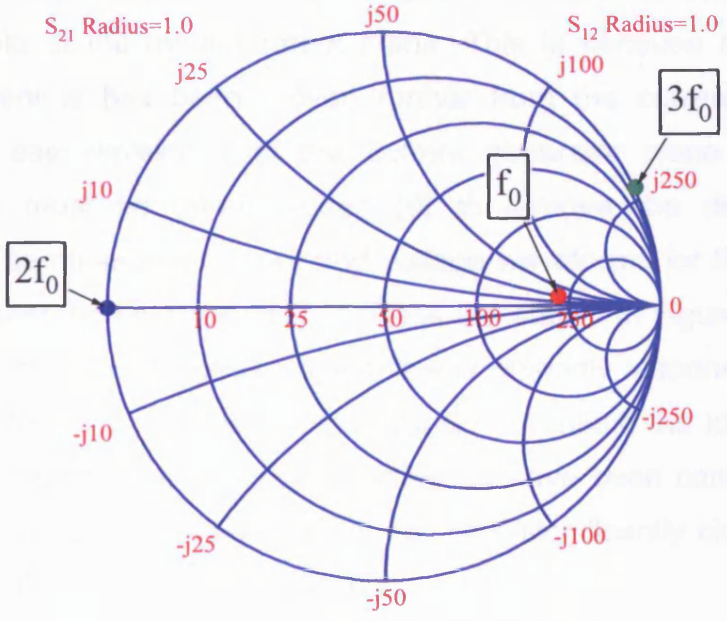

Figure 5-23 Smith chart showing the location of the first three harmonic impedances after tuning out C_{ds} with inductive offsets applied to the odd harmonics.

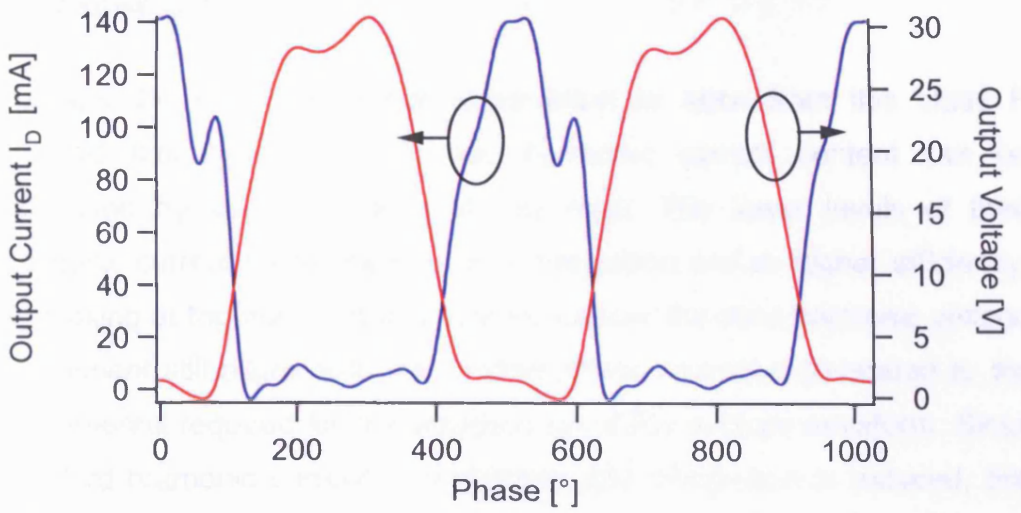

Figure 5-24 De-embedded, measured RF current and voltage waveforms for the optimum condition after tuning out C_{ds}.

When this optimisation was performed for this design, the efficiency performance was increased to meet the target value of 80 %. Figure 5-23 shows on a Smith chart the impedances presented to the first three harmonics in order to resonate out the output capacitance in this device.

After tuning the fundamental and third harmonic impedances to their inductive offset values the classic class F waveforms are no longer recognisable at the measurement plane. This is because the point of measurement is has been moved further from the current generator plane. To see waveforms at the current generator plane the output waveforms must be de-embedded [9] to remove the displacement currents. The measured current and voltage waveforms for the optimum condition after the de-embedding process are shown in Figure 5-24. The visible reduction in off period current flow is primarily responsible for the improved efficiency. The waveforms still do not match the ideal class F waveforms as only the first three harmonics have been controlled. The measured and predicted efficiencies are now significantly closer due to the larger rail voltage in this application.

5.5 Summary

Perhaps the most significant observation to arise from this class F analysis has been that the odd harmonic current content can be minimised by correct biasing at the input. The lower levels of third harmonic current mean there is less dissipation and so higher efficiency. By biasing at the null in third harmonic current the third harmonic voltage component still aligns with the correct phase inversion compared to the fundamental required for the squaring up of the voltage waveform. Since the third harmonic current is minimised and dissipation is reduced, this bias condition must be the singular optimum solution for efficiency performance in a class F amplifier.

It has also been shown that the quality of the even harmonic short circuit is vital to the achieved efficiency and that every effort should be made to ensure a good ratio between the even harmonic impedance and the fundamental impedance is achieved. This idea was extended to look at ways the short circuit termination could be improved for large devices where a low ratio is hard to reach, and building harmonic terminations internally in the package was suggested as a potential solution.

The issue of whether an ideal open circuit or finite lower impedance at the third harmonic is better for class F was also analysed, and found to be surprisingly uncritical. It is possible that this is connected with the singular solution of class F being a relaxation mode that the device finds preferable, perhaps due to entropy. If the solution that sustains the most fundamental output voltage, and therefore also contains the appropriate amount of odd harmonic voltage content to support that fundamental component, is preferred, then as long as the odd harmonic termination is significantly higher than the fundamental, the device seems willing to automatically "drop into" or "relax into" the optimum efficiency state. Ultimately this idea is somewhat academic, as in a circuit implementation an ideal open circuit cannot be achieved, so the fact that a reasonably

high impedance has an equivalent effect on enhancing efficiency is good news for the designer.

The analysis presented in this chapter has shown the need to have access to reliable waveform data, from either a simulator using a good model or a time-domain measurement system. An important point to note is that the on-wafer results presented here for small devices have very low levels of parasitic components between the measurement reference plane and the theoretically assumed current generator plane inside the device. In larger devices and those inside of packages then there will need to be a de-embedding process to access waveforms at the current generator plane, where the optimum waveforms need to exist. Any uncertainties in this de-embedding stage will result in a certain amount of empirical adjustment of parameters, particularly the phase of the harmonic terminations [9].

To summarise the class F design procedure arising from this work, Figure 5-25 outlines a generalised class F design flow that utilises knowledge of the harmonic content of the output waveforms to optimise efficiency.

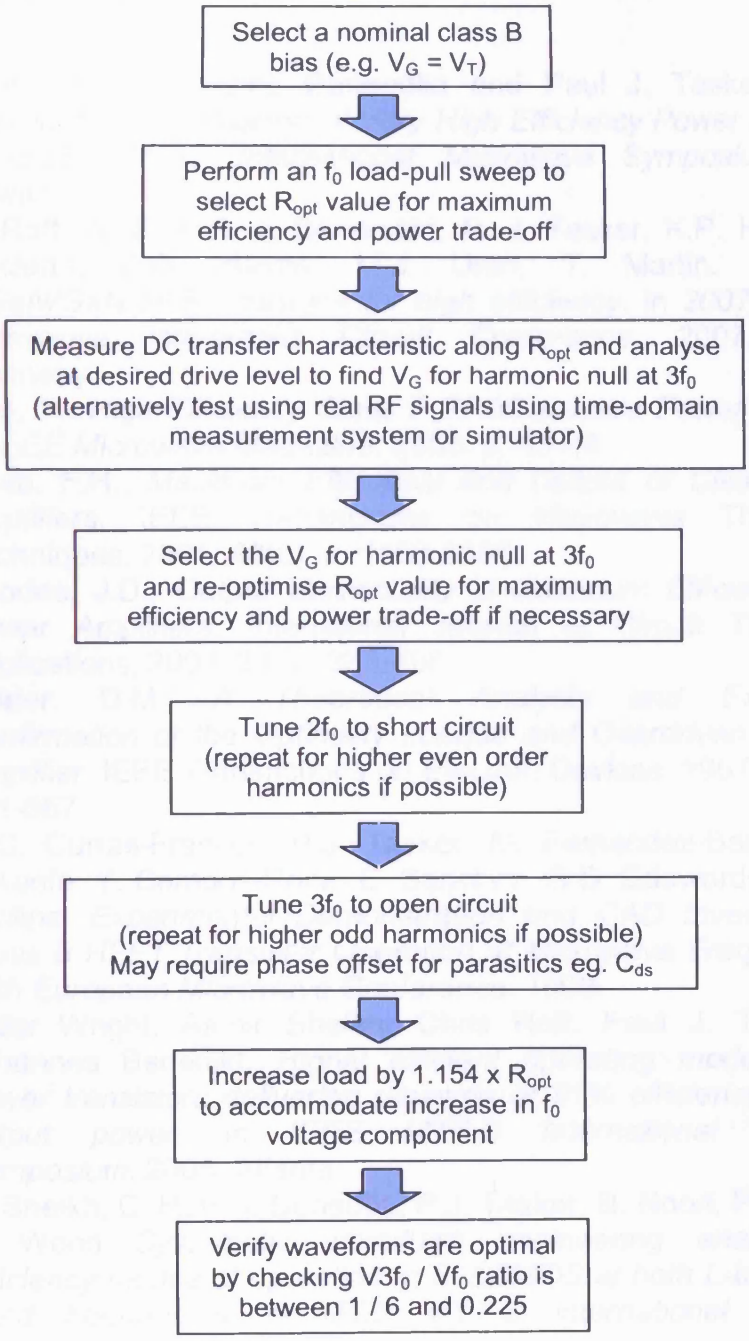

Figure 5-25 Flow chart demonstrating a logical class F design procedure.

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Chapter 6 – Conclusions

This thesis has two primary topics: characterising GaN HFET performance and investigating the design of class F amplifiers using FETs. The central theme uniting these two topics has been the use of measured RF waveforms and the ability to manipulate these waveforms using DC bias and harmonic load-pull – a technique known as waveform engineering. A key value of the waveform approach has been shown to be its ability to remove doubt or uncertainty over the results achieved using models and other measurement approaches. Since true large-signal RF stimulus can be used, a full picture of transistor performance under realistic operating conditions can be recreated from the measured currents and voltages. One illustration of this is the physical models of GaN HFET current collapse. The model reproduces all the features of the measured RF waveforms and so can be said to be validated by them. Similarly, the measured RF waveforms have also been shown to be useful for verifying less direct measurement approaches, such as pulsed-IV data for GaN HFETs or the DC transfer characteristics used to analyse harmonic current content in the class F designs.

The application of waveform engineering to characterising GaN HFETs occupied the first half of this thesis. It has been shown that using the measurement system to study why performance was being lost can

provide insight into the problems affecting a device technology. The conclusions from the measured results can potentially be fed back into the device fabrication process and hopefully fix the problem. This route was demonstrated in the case of selecting the correct iron doping profile required to reduce short-channel effects in QinetiQ Ltd.'s process. The application of RF waveforms into the design cycle of a new transistor technology has been shown to be beneficial, primarily because of the additional insight that can be gleaned from observing the real large-signal RF currents and voltages. This type of application holds huge potential since there are almost limitless iterations of changes needed to optimise new device structures, and many of the processing steps can benefit from a similar analysis using measured waveforms.

The main achievement of the work in chapter 3 was helping to improve understanding of DC-RF dispersion in GaN HFETs. When this project began there was no clear explanation in the literature as to why the current collapse was so localised to the device knee region. This important feature of the DC-RF dispersion in GaN HFETs had even led to the effect being referred to as "knee walk-out." As a consequence of the detailed pulsed-IV and waveform measurements performed during this project, specific trends were identified that were used to inform a physical model developed with QinetiQ Ltd. This model explains the localisation of the DC-RF dispersion at the knee for the first time in terms of premature electron velocity saturation that only limits channel current severely at the knee region.

Chapter 3 also presented the first time that RF waveform measurements have been used for tracking performance degradation over time in power transistors. Effects such as gradual I_{DQ} drift and gain degradation are common to many newly developed transistor technologies but device developers must rapidly quantify, understand and fix such problems or risk the devices being rejected in the market place. Using real RF waveforms has been shown to add insight to these processes beyond simple DC stress tests, for example by demonstrating that the

degradation was primarily electric field driven and not specifically caused by thermal issues.

The work presented in chapter 5 analysed the class F mode in real transistors using measured RF waveforms. The existing body of class F research prior to this project had not included measured current and voltage waveforms and had therefore been unable to provide definitive verification of class F operation. The primary contribution of the measured waveform study in chapter 5 has been to demonstrate how the theory of ideal class F must be adapted to accommodate the various effects of a real world transistor and imperfect circuit implementations.

The measured waveforms have shown why features of real transistors such as the finite on-resistance and a non-ideal transfer characteristic stop the ideal square wave voltage and half rectified current waveforms from being achieved. The work has extended this concept to shown how to systematically optimise circuit parameters to allow the device to support waveforms that are maximally efficient. For example, the transfer characteristic has been analysed to allow for the optimum selection of gate bias to precisely define the harmonic content of the current waveform. This new measurement approach has highlighted a requirement for the gate bias point to be selected to exactly null the odd harmonic content (and especially the third harmonic content) in the output current. It can be reasoned that this null bias point alone can create a singular optimum efficiency state where the dissipated power at the third harmonic is minimised.

The effect of the output matching circuit on the voltage waveform has also been tested within a controlled experimental environment by using active harmonic load-pull to emulate different circuit tunings. The conclusions from this study have shown that the harmonic impedances required to successfully shape the voltage waveform are effective relative to the fundamental impedance rather than in absolute terms. The implications of this observation for scaling up class F designs to high

powers has been explained, leading to the suggestion that a close to die matching strategy will be most effective for high power class F implementations. The assumption in much of the class F literature that an ideal open circuit is required at odd harmonics has been challenged, demonstrating that an odd harmonic impedance five times higher than the fundamental is sufficient for achieving the majority of the efficiency enhancement.

The effect of limited bandwidth of harmonic control in the output matching circuit has also been revisited by examining the popular three harmonic class F variant. Arising from this analysis has been the realisation that the fundamental load impedance should be increased by an equal factor to the fundamental voltage extension, rather than the straightforward $4 / \pi$ increase that would be predicted from ideal theory. The effect of the finite on-resistance has also been shown to allow more third harmonic voltage to develop than would be predicted for the flat boundary condition case. The consequence of this is that a larger fundamental voltage extension can be accommodated, leading to higher efficiency.

Finally, a GaN HFET based class F design was performed using the measurement system, demonstrating how the still developing technology described in chapters 2 and 3 can still be optimised to achieve respectable performance in advanced operating modes like class F by following the analysis of chapter 5.

Chapter 7 – Future Developments

7.1 Introduction

Although RF waveform measurements have been available for over twenty years at some institutions, they have yet to become widely adopted in the RF device fabrication, modeling and circuit design communities. There is a perception that the measurements are time consuming and require highly complex and often expensive setups. This preconception has limited their application in industrial settings, where time to market of new products is of such importance that a pragmatic use of existing measurement solutions has remained more popular. However, there are strong signs within the RF measurement industry that this impasse towards time-domain measurements will not remain in the future.

A number of start-up companies have begun to offer non-linear measurement solutions that have a strong emphasis on using time-domain data in device fabrication, modeling and circuit design. The two largest measurement system houses Agilent, and to a lesser degree Rhode and Schwarz, are now both marketing RF time-domain measurement solutions attached as add-ons to network analysers. Standards institutions such as the National Institute of Standards and

Technology (NIST) in the US and the National Physics Laboratory (NPL) in the UK are working to ensure sampling scope based measurements are traceable back to physical standards [1]. These advances are beginning to address the industries preconceptions about the ease of use and reliability of time-domain measurement systems and are beginning to educate the community about the value of such systems. With this growing awareness for non-linear characterization and its benefits, there will be an increased need to develop a deeper understanding of their application in fields such as device design, circuit design and nonlinear modeling.

This thesis has focused on applications of RF time-domain measurements in two narrow fields, for device fabrication and circuit design. In this chapter future developments in the application of RF waveforms in both device fabrication and circuit design will be discussed only in the context of GaN HFETs and class F design.

7.2 Developments for RF waveforms in device fabrication – GaN HFETs

In the course of this thesis, work on GaN HFETs has confirmed that the causes of both DC-RF dispersion and device degradation is strongly related to the high peak electric fields localised on the drain side of the gate edge of the device. The solution to the DC-RF dispersion and degradation problems must therefore lie in two areas:

1. Reduction of the density of trap locations
2. Reducing the likelihood of electrons being driven into the traps

Reducing the trap density will come in time as bulk material quality improves, as better quality substrates become available and as advanced processing steps become mature. At present the dislocation density in a typical GaAs pHEMT wafer is less than 10^4 cm^{-2}, compared to levels in a GaN wafer which are typically up at 10^8 cm^{-2} [2]. Similarly, the thickness uniformity of GaN wafers is often more than double that of GaAs, which leads to varying strain, lower yields and more potential lattice damage sites [2]. As the material quality improves, the quantity of likely traps sites, particularly in bulk and buffer regions, will reduce. Similarly, by developing in-situ passivations and advanced surface cleans, the number of available trap sites at the surface will also be reduced. Another approach to mitigating the effect of surface traps is to use GaN cap layers to isolate the surface from the gate to AlGaN interface.

Reducing the likelihood of electrons being driven into trap sites will also help to reduce DC-RF dispersion effects and device degradation. This can be achieved by reducing the peak electric field using electric field spreading techniques such field plates. Another approach would be to reduce the gate leakage, which is again possible through GaN cap engineering [2]. When these new devices are developed and as the various processing advancements come on line, time-domain measurements can be used to analyse their effect, in a similar way to the

analysis presented in this thesis for varying iron doping levels in the buffer [3].

In addition, new measurement variations can be employed in order to collect specific data for new tasks. For instance, as well as using the waveform measurement system as a tool for measuring degradation in devices to be operated as PAs, the system can also be employed to pre-emptively stress devices to determine their capabilities in Low Noise Amplifiers (LNAs) [4]. In a receiver application it is desirable to have as low a Noise Figure LNA circuit as possible. In the majority of LNA circuits a diode is included before the transistor to provide protection from any excessively large signals that may have strayed into the antenna. The inclusion of the diode will often add around 1 dB to the circuit Noise Figure. Given the tolerance to high breakdown fields in GaN HFETs, there is potential to use these devices in receiver front ends without including the limiting diode and thus significantly reducing the overall circuit Noise Figure.

There are two main breakdown mechanisms at the input terminal of a GaN HFET, forward and reverse breakdown of the input diode. To separately test the durability of the GaN HFET input diode to forward bias and reverse bias stress using real RF signals, the waveform measurement system can be used to test the device with an RF signal consisting of a fundamental component and a second harmonic component with an appropriate phase relationship to excite either the diode turn-on behaviour or the reverse breakdown behaviour. Examples of this sort of failure mechanism analysis can be seen in Figures 7-1 and 7-2 where power sweeps at 1.8 GHz have been used to assess the breakdown limit in either direction for 2x50 μm GaN HFETs.

Future developments such as these are particularly exciting as they have the potential to generate overlap between the fields of device fabrication and circuit design. As the device fabrication team alter the device layout to accommodate larger stress voltages, and the circuit designer tests

various designs, the measured RF waveform data can be used as direct feedback of performance.

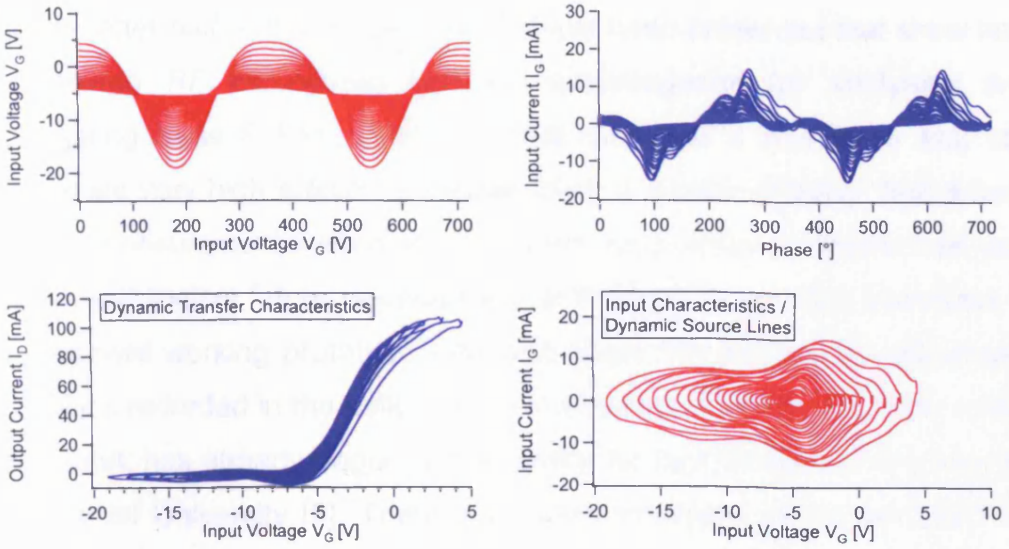

Figure 7-1 Measured waveforms from a power sweep at 1.8GHz for a 2x50 µm GaN HFET biased at V_G = -5 V, V_D = 15 V. Drive signal contains fundamental and second harmonic content phase aligned to stress the reverse breakdown without overly stressing the forward breakdown.

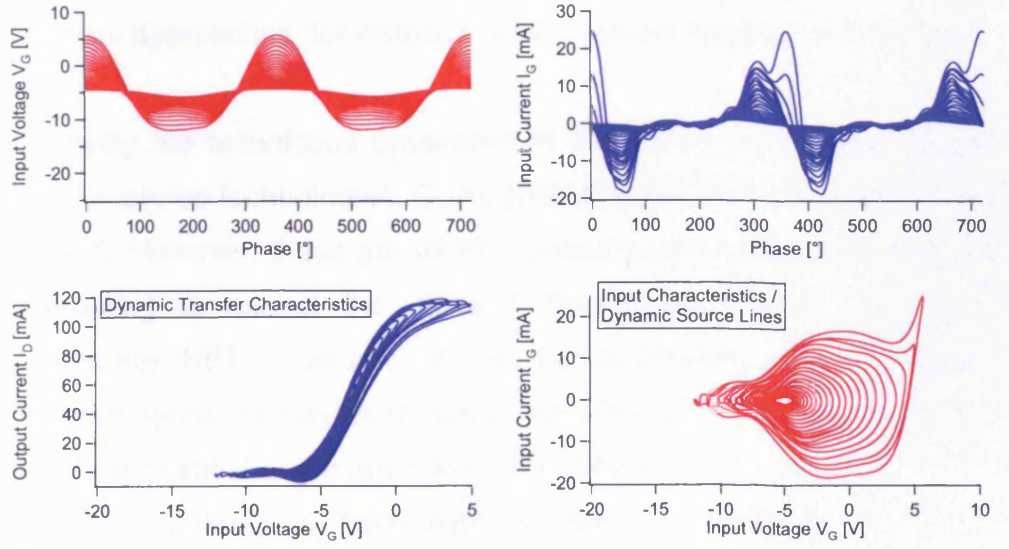

Figure 7-2 Measured waveforms from a power sweep at 1.8GHz for a 2x50 µm GaN HFET biased at V_G = -5 V, V_D = 15 V. Drive signal contains fundamental and second harmonic content phase aligned to stress the forward breakdown without overly stressing the reverse breakdown.

7.3 Developments for RF waveforms in circuit design – class F

In the latter half of this thesis, results have been presented that show how measured RF waveforms can be advantageous for analysing and designing class F PAs. The work has identified a procedure that can generate very high efficiency values when a device is being "test driven" in the measurement system environment using active harmonic load-pull. The most logical future development is to begin to use this technique to implement working prototype PAs that share the same high efficiencies as were recorded in the calibrated measurement system. To some extent this work has already begun at the centre for high frequency engineering at Cardiff University [5]. There are numerous types of implemented RF PAs, and it would be interesting to extend the methodology defined in the measurement system to take account of the factors unique to the different environments. For instance, a class F implementation using an on-wafer dye bonded into a hybrid, a full MMIC design at X-band or a high power packaged integrated circuit (IC) would all require slightly different approaches, for instance how to accommodate for packaging.

Currently the techniques presented in this thesis have been applied to various device technologies, GaAs pHEMTs, GaN HFETs and Si LDMOS [3, 5-7]. However, these are all FET based technologies, and it would be interesting to extend the class F theory for bipolar type devices, particularly HBT structures. It can be envisioned that a significantly different approach may be required, since the HBT transfer characteristic is an exponential and is therefore very different from that of an FET and would be unlikely to have such a clear null condition for the third harmonic current content.

The class F analysis in this thesis has also highlighted the necessity of achieving good harmonic terminations. It would be a useful project to design a class F tuned device that contained short and open harmonic

terminations directly on or close to the die, using individual terminations for each unit cell of transistors. This project should enhance class F circuit performance as devices are scaled up for high power applications.

Given that the work has highlighted the importance of biasing the gate in the harmonic current null for best class F performance, and that the third harmonic null moves with drive level, it would be a logical extension to add a dynamic biasing circuit to move the bias point to track with drive level. It would be particularly interesting to see if tracking the null boosted efficiency by enough to make the additional circuitry valuable, and whether the effect on overall linearity of an adaptively biased class F circuit is affected. An overall analysis of class F linearity would also be useful, especially if it was able to highlight additional circuit trade-offs between boosting efficiency and linearity.

Once you have an optimally tuned class F design, the question of how sensitive such a design will be to imperfections in the output matching circuit, variations between different wafer runs of devices and other manufacturing variables is likely to arise. The work in chapter 5 has highlighted what happens to various parameters as they are individually varied on the way to finding the singular optimum solution. However, from a manufacturing point of view it would be interesting to analyse the sensitivity of class F circuits to more general variations, such as a 5 % tolerance on all critical circuit dimensions and the rail voltages. To undertake such an analysis using time domain measurements and active load-pull would be an extremely time consuming task even with future speed improvements. Instead this sort of analysis would be better performed using a CAD package such as the Agilent Advanced Design System (ADS) suite. It would be interesting to see whether the singular optimum solution can be successfully manufactured, or whether a more pragmatic but compromised class F design would fare better in mass production.

It would be useful to perform a similar analysis for other switch-mode PAs such as inverse class F and class J to increase understanding of their implementation. A circuit architecture with a good deal of potential would be a class F PA combined with an ET modulator to allow the high efficiencies of class F to be maintained over a large dynamic range of input powers whilst operating over a reasonable narrow bandwidth such as in a wireless communications channel. It would be interesting to see if the high efficiencies of a class F design could be maintained over a range of rail voltages, since the transfer characteristic and the harmonic content will vary at different power levels. This would suggest the need for an adaptive bias circuit and potentially other additional circuitry which may make such a design overly complicated to be successful.

7.4 References

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