High Power Waveform Engineering

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Contents

1 <u>Summary</u>

For many years industry has considered RF PA design to be a "black art". This perception has been held due to the lack of availability of meaningful information for analysis and design. Due to the emergence of large signal waveform based measurements and increased understanding in the literature, it is now possible to characterise devices and correlate the information for enhanced PA design in terms of efficiency, linearity and/or reliability. This has been well documented and demonstrated using on-wafer devices but where this thesis work begins, little work had been done in expanding this capability to higher more meaningful power levels using packaged devices.

This work has successfully addressed both of these limitations and extended visibility of time domain waveform data to higher power levels. Thus, allowing for the uncovering of world record efficiency levels of 77 % (4W output power) for Si LDMOS devices at S band frequencies using waveform engineering based procedures, in this case Class F. A feat previously only reported at L-band frequencies. Other waveform based designs such as inverse Class F and Doherty modes of operation are also successfully demonstrated in this thesis. In both of these cases, voltage related issues affecting reliability were uncovered that merit further consideration in the design process.

Waveform engineering was made possible by applying de-embedding the measured current and voltage waveforms to the current generator plane. That is the plane at which the device is free from any device and package parasitics with the current and voltage waveforms seen to be in good agreement with those typically found in literature. These were successfully applied at high power levels (110W) previously not reported.

To further demonstrate the relevance of waveform de-embedding, a non-linear charge conservative model based on industry standard modelling techniques was compared against time-domain measurements conducted in several classes of

operation. This form of model verification is often overlooked and provides a unique insight into the model's accuracy highlighting new areas of improvement. In most cases the model was shown to be in good agreement with measured data, providing a high level of confidence in the application of waveform engineering principles within the CAD domain. Thus providing the PA designer the facility to apply waveform engineering on both the test bench and within the CAD domain.

2 List of Publications

I. **Aamir Sheikh**, Chris Roff, Johannes Benedikt, Paul J. Tasker, Basim Noori, John Wood, Peter H. Aaen, "Peak Class F and Inverse Class F Drain Efficiencies Using Si LDMOS in a Limited Bandwidth Design", *IEEE Mi & Wire. Comp. Letters,* vol. 19, iss. 7, pp. 473-475.

Abstract - This paper compares two popular high power, high efficiency modes of operation, class F and inverse class F, and assesses the peak obtainable drain efficiencies when using Si LDMOS devices in a limited bandwidth design. Optimum class F and inverse class F conditions are presented using active harmonic load-pull measurements, and it was found that a higher drain efficiency was achieved in the class F configuration. This result is due to the limitations imposed by the soft voltage breakdown occurring due to the extended voltage swings inherent to inverse class F, as a consequence generating unwanted current content during the off cycle. This significantly reduces the peak measured efficiency using Si LDMOS devices when implementing an inverse class F design with a drain bias of 28V. By reducing the drain bias to 18V, to accommodate the voltage extension of inverse class F, it became possible to achieve peak measured efficiencies much closer to what theory predicted.

II. **Aamir Sheikh**, Jonathan Lees, J. Benedikt, P. J. Tasker "Utilization of a Measurement Based CAD Tool for Enhanced PA Design Investigations", *Proceedings of the 38th European Microwave Conference,* pp. 1671-1674, Oct 2008.

Abstract - This paper outlines the use of a measurement based waveform CAD tool for enhanced PA design. Two measurement based models have been used to simulate a complete Doherty power amplifier together with output matching. The output matching network and auxiliary bias were optimised to produce a region of high efficiency typical of Doherty power amplifiers. Through the incorporation of a large signal de-embedding network, the current and ation of power amplifiers using well established waveform devoltage waveforms were accessed at the current generator plane. This allowed for the confirmation of Doherty operation on an individual device basis. This powerful tool allows for further optimissign procedures, previously not possible at high power levels.

III. **Aamir Sheikh**, Chris Roff, J. Benedikt, P. J. Tasker, B. Noori' [2], P. Aaen and J. Wood, "Systematic waveform engineering enabling high efficiency modes of operation in Si LDMOS at both L-band and S-band frequencies," *IEEE MTT-S Int. Microwave Symp. Digest,* pp. 1143-1146, June 2008.

Abstract - This paper demonstrates that by robust waveform engineering it is possible for high power Si LDMOS to achieve very high efficiency at frequencies up to 2.1GHz. Class F amplifier operation was realized in a

5W LDMOS device by the successful application of robust waveform engineering procedures; undertaken at the current generator plane. The peak power added efficiency was found to be 78% at 0.9GHz and 77% at 2.1GHz. In both cases the RF waveforms were optimized in terms of the gate voltage, fundamental and harmonic impedances. The main difference at 2.1GHz was the change in fundamental impedance to a more reactive impedance to compensate for the dynamic device output capacitance. To the authors' knowledge this is the highest efficiencies reported in the literature for Si LDMOS devices at 2.1GHz.

IV.   A. Sheikh, P. J. Tasker, J. Lees, and J. Benedikt, "The impact of system impedance on the characterization of high power devices," *Proceedings of the 37th European Microwave Conference*, pp. 949-952, Oct 2007.

Abstract - This paper focuses on the extension of the successful application of current and voltage waveform engineering of on-wafer devices to power levels relevant to both handset and basestation markets. Effects on the measured waveforms caused by a 50Ω characteristic impedance of the measurement system are investigated showing a significant effect at the lower and crucially at higher harmonics, which is in contrast to the current school of thought. For the first time a waveform based analysis of packaging affects is presented, allowing the effects of the system's higher harmonic impedances to be studied and considered in the context of de-embedding measured waveforms. Measured de-embedded waveforms are compared with simulated equivalents model and are found to be in good agreement.

3 <u>Glossary of Terms</u>

In order of appearance

RF	Radio frequency
TDMA	Time division multiple access
FDMA	Frequency division multiple access
CDMA	Code division multiple access
LTE	Long term evolution
OFDM	Orthogonal frequency division multiplexing
PA	Power amplifier
CAD	Computer aided design
VNA	Vector network analyzer
DUT	Device under test
POI	Points of interest
CW	Continuous wave
FET	Field effect transistor
BJT	Biplolar junction transistor
LDMOS	Laterally diffused metal-oxide semiconductor
HEMT	High electron mobility transistor
Si	Silicon
GaN	Gallium Nitride
MOSCAP	Metal-oxide semiconductor capacitor
MAG	Maximum available gain
MSG	Maximum stable gain
EM	Electro-magnetic
F_T	Frequency at unity small signal gain
NVNA	Non linear vector network analyzer
EER	Envelope elimination and restoration
ET	Envelope tracking
R_{opt}	Optimum resistance for output power
T_p	Transition point

4 Introduction

Over the last ten years, the wireless communications industry has grown exponentially with ever increasing users and applications. At the centre of this growth has been the constant requirement for communication and trade within a global "24/7" environment. The consequence of this has been the need for instant access to voice and internet services at home, the office and on the move with an estimated 2.5 billion mobile users worldwide [1]. This has been enabled by the combination of improvements in hardware and software as well as the injection of large amounts of financial investment within the mobile infrastructure.

The hardware improvements in digital processing power, speed, memory capacity and device miniaturisation allows for the implementation of complex algorithms at speeds previously not possible in a case size no larger than the palm of an individual's hand. This has been supplemented with improvements in active radio frequency (RF) technology such as power transistors, with higher gain values and higher frequencies of operation. In parallel, software and algorithm improvements and an increased effectiveness in the application of these processes in hardware have allowed for the quick transfer of mathematical processes into a commercially viable solution. This has led to the introduction of enhanced communications systems that simultaneously boost the numbers of users and data rates. This initially started with GSM leading to its enhanced version GSM Edge, both of which are still highly prevalent within the developed and developing world. These were based on time division multiple access (TDMA) based techniques that allowed for a vast enhancement in user compared to it's predecessor, frequency domain multiple access (FDMA), but the vast increase in network users led to the implementation of code division multiple access (CDMA) based techniques.

The introduction of CDMA allowed for vast increases in users and data rates typically around the hundreds of kilobytes to a couple of megabytes per second,

and is currently being used in developed countries with an estimated 400 million mobile internet users worldwide [2]. Future systems such as long term evolution (LTE) and mobile Wi-Max now based on orthogonal frequency division modulation (OFDM) based techniques allow for even higher data rates in the hundreds of megabytes per second. With these increases in data rates, the wireless communications industry has brought in significant shifts in not only mobile but also fixed infrastructure.

This has reduced the need for extensive optical based fibre networks, previously touted as the best method of achieving high data rates to each home. The data rates offered by optical based communications systems still far supersede that offered by the wireless systems but the added costs and major planning requirements in the building of a complete fibre based infrastructure make it prohibitive to cover every household. This has led to a newer model for improved communications whereby a fibre based back bone network is supplemented by a local wireless network that will deliver data to the end user.

As the numbers of users and requirements have increased the design and implementation complexities have also increased. In addition to that, the wireless communications systems designer has also had to contend with outside factors, such as costing and energy consumption to ensure the product not only has mass appeal but is also seen to be working at the peak in efficiency. This is because of the great infrastructure power consumption levels which account for approximately 2-3 % of the total global carbon emissions [2] and due to the high demands of these networks, this is expected to double by 2020. This has also been supplemented by significant increases in electricity costs. One of the components found to be the most power consuming is the power amplifier [3].

The power amplifier (PA) is the last stage prior to the antenna that amplifies the output signal to output power levels typically in excess of 100W for mobile base stations. The added complexity of modulation signals with large peak to average power ratios (PAPR) and increasing signal bandwidth have to be optimised,

whilst working within the tight controls on spectrum space [4]. This spectral requirement takes precedent in the design process, resulting in the power amplifier being operated in a backed off 'linear' mode of operation. The average efficiency of these amplifiers in these modes of operation are usually in the region of 20-30 %, which leads to the requirement of approximately 400 W of DC power plus the additional power required for cooling the amplifier in the form of air or liquid based systems. This makes the power amplifier one of the most power consuming circuits within the entire communications system and with around 51,000 base stations currently in deployment around the UK [5] the potential savings both in carbon and electricity costs are immense.

As outlined earlier, the design of efficient power amplifiers is a pivotal topic and has attracted a large amount of interest in both academic and industrial research and development centres. The research in efficiency enhancement techniques can be split into two distinct brackets [6]. The first can be identified as peak power efficiency enhancement techniques, whereby the amplifier is operating as close as possible to the ideal figure of 100 % efficiency at peak output power. This is when all of the inserted DC energy is transferred to the output of the transistor at RF. The second group of efficiency enhancement techniques are described as efficiency enhancement with dynamic range in power, whereby the amplifier is operated at a higher level of efficiency over an extended range of power levels. There is also the possibility of an amalgamation of the two previously explained research threads but little work has been achieved in this regard. In all cases, the design of efficient power amplifiers has one consequence and that is an increased amount of non-linear distortion in both harmonic and "in band" intermediate frequency (IF) components. However, with the introduction of adaptive digital signal processing techniques it has been possible to produce linearization techniques that can adhere to the strict government controls on spectrum on PAs which were previously deemed unusable [7]. With these developments in mind, it provides encouragement to look further into high efficiency PA design.

In general, the theory behind PA design has always centred on the analysis of input and output current and voltage waveforms. For simplification purposes, the input stimulus is always assumed to contain content at just the fundamental. However, the output will invariably contain signals at the desired fundamental frequency and its higher harmonics, which will distort the output current and voltage waveforms. However, whilst it is not desirable to distort the PA for linearity purposes, in the case of efficiency it is the manipulation of higher harmonic current and voltage components that produce significant strides towards the desired target of 100 % operating efficiency. The first mode of high efficiency operation was first demonstrated by Snyder [8]. Snyder, mathematically demonstrated that by applying Fourier series analysis to the desired output current and voltage waveforms it was possible to achieve 100 % operating efficiency in a mode referred to as class F. This emphasis on the waveforms provided a unique and rational insight not previously discussed in the literature. Further work has been done on other high efficiency modes of operation such as inverse class F and class E [9]. In the case of class E, high efficiency operation was achieved through the design of a charge storage circuit that operated similar to a switch. However, the explanation of class E operation is best described using the output current and voltage waveforms. These two examples emphasize the unique insight that waveforms present into PA design in explaining high efficiency operation.

The second stream of efficiency enhancement is focussed on improving efficiency over a large range of output power. This form of efficiency enhancement has attracted more interest in the commercial communications domain due to the large peak to average ratios exhibited in 3G and 4G signals. One of the first proposed methods was demonstrated by Doherty [13] in the Doherty PA. The Doherty PA produced a region of high efficiency over the peak 6 dB of output power through the process of active load pull. This is done by controlling the ratio of the two currents being generated at the output node of each device, which consequently alters the load impedance being seen by either device. Other techniques have also been investigated such as the Chireix out

phasing amplifier as well as envelope elimination and restoration [2]. Again in both cases the use of waveform analysis provides a unique insight in the design and optimisation process.

In recent times, the PA designer has shifted away from analysing the output current and voltage waveforms. Part of the reason is due to the design process focussing more on providing high output power and linearity and with a smaller focus on efficiency. More recent effort has been put into high efficiency PA design, however, without the use of waveforms it becomes difficult to confirm whether the optimum mode of operation is achieved in the design. This is because an overdriven amplifier biased in class B can produce efficiencies in excess of 70 % together with high output power and gain [3]. Producing a design that is only 10% percent lower than the optimised designs typically reported in the literature [10-12]. Whilst this difference is not majorly significant in terms of efficiency, there could be other consequences such as reliability. By looking at the input and output waveforms it becomes possible to not only quantify the performance but also more precisely account for other factors that may be overlooked in the design process.

Another reason for the lack of use of waveforms, is due to the lack of access to non-linear components in both the measurement and computed aided design (CAD) domains. Historically, power meters and spectrum analysers have been used to collect RF data, which are scalar measurements. These are typically combined with the use of vector network analyzers (VNA), to allow for s-parameter measurements. Whilst this data provides a good insight into device and PA behaviour there is not enough information present to extract waveforms. To achieve this nonlinear VNA functionality, the forward and reverse travelling wave data collected must be fully vectorial and referred to a common phase reference for correct alignment of the current and voltage waveforms. In addition to that the data must be collected over a large enough bandwidth spanning multiple harmonics. Such systems are only available in a handful of locations and the costs involved in procuring such equipment can be three to five times

higher than more traditional characterization facilities. This consequently affects the CAD simulations, where the device models are only fully validated against pseudo scalar/vector measurements, questioning the use of these models within a full vector based domain.

Having access to waveform data will allow the PA designer to investigate the device's performance in a more thorough and detailed manner. Through a process of current and voltage analysis and control at the input and output terminals it is possible to apply procedures such as class F. The application of these theoretical procedures in the field of PA design is called waveform engineering. Waveform engineering is a topic of high recent interest [14] and has provided the missing information about how high efficiencies are attainable device and frequency independent [11, 15].

Waveform engineering has typically been demonstrated on small devices usually in an on-wafer environment where package and device parasitics are kept to a minimum. This allows for the direct application of waveform based procedures such as [8] and has led to further developments as outlined in [16]. However, small devices have a limited application domain such as mobile handsets or other short range systems where the added complexity in design yields a small saving of power.

When these procedures are applied at higher power levels the savings in power become more tangible. However, the application of these procedures at high power, have yielded limited results [10] with high efficiencies so far achieved in medium power devices and at L-band frequencies. Part of the reason for this is due to the higher losses at high frequencies but the more significant reason is the lack of access to the appropriate current and voltage waveforms in the design process. For this to successfully occur, the waveform data has to be taken at the correct reference plane. The waveform data captured in time-domain based measurement systems [17] and in commercially available CAD based models are at a calibrated reference plane at the input and output tabs of the device. The

waveforms captured at this plane are altered by the device parasitics, which in this case consist of inductances and capacitances that add reactive content to the generated current and voltage waveforms. As the device size and frequency of operation increase, the size of the parasitic elements and their effect on the waveforms escalate rendering the waveforms of little or no use for waveform engineering. This is especially the case in high power devices, where direct probing the die is not possible and measurements have to be taken at the output of package. It is to be noted that the waveforms still contain all of the information required for design, such as the power and efficiency as well as impedances for matching network design. To cancel these effects, it is required to move to a reference plane within the device where waveform engineering can be more effectively applied. This and the validation of the de-embedded results, forms the first main body chapter of this thesis. There has been a lot of effort put into passive modelling of the package [18], however what has not been established is the complexity of package modelling required for accurate waveforms with regards to increasing size and operating frequency. Another factor for consideration is the extent of de-embedding necessary. Classical s-parameter based modelling techniques [19] have found it necessary to separate out the passive and active components to fully describe the transistor's behaviour. However, waveform engineering has typically been applied on-wafer yielding positive results. This provides a first reference point for de-embedding the waveforms, but with larger devices the actual device parastics such as the output capacitance C_{ds} scale linearly with size and could have a greater effect in high power devices. Two particular examples are cited, a 5 W device and a high power 110 W device.

To enable confidence in the use of waveforms at an internal reference plane, there is also a need for validating the results. For initial purposes, this is done by comparing the de-embedded current and voltage waveforms with theory. Whilst this provides a start point, this work has highlighted that high power devices can be affected by outside issues previously not considered necessary, such as the system impedance and how they generate higher harmonic content. Without

taking these factors into consideration, the valid de-embedded results can produce waveforms that initially look incorrect, which can cause an unnecessary repeat exercise in device and package network validation. One particular example discussed in Chapter 6, is the affect of the measurement system impedance environment, which stays constant at 50 Ω whilst the optimum impedances of the devices reduce to below 1 Ω. This is further investigated when the impedance transformation of the package network, transforms the 50 Ω system impedance to complex impedances at an internal plane of reference. These complex impedances can have substantial effects on the waveforms and the fundamental performance of the device.

Now with increased confidence in the resultant de-embedded waveforms, waveform engineering is demonstrated using Si LDMOS devices. Chapters 7 and 9 focus on providing evidence of the increased awareness and design knowledge waveform engineering provides to the PA designer. Chapter 7 is based on implementing high efficiency waveform engineering, in particular class F and inverse class F modes of operation. Chapter 9 focuses on the Doherty amplifier, looking at how the de-embedded waveforms can be utilised for firstly confirming Doherty modes of operation and for enhanced single device investigations that provide the designer all of the relevant information for matching network design. Both chapters showcase the enhanced insight waveform engineering provides the designer that can subsequently be used for design.

Chapter 8, validates a commercially available large signal model against measured time-domain data. To date large signal models have only been validated and evaluated using scalar measurements such as output power and operating efficiency. There has been little or no validation of models in the time domain especially at power levels more relevant for base-station applications. Large signal models consist of many layers, the intrinsic device, the extrinsic device parasitics and the package. This provides several reference points at which to validate the entire model.

Overall, the focus of this work is to forward the concept of waveform engineering to high power devices to provide a more thorough understanding of the PA mode of operation. This will provide the designer with more information and allow for more prompt optimisation of designs for efficiency and/or linearity in both the measurement and simulation domains.

5   Time Domain De-embedding

To date high power devices have typically been characterised using load-pull/ source-pull based measurement systems that are used to locate points of interest (POI) such as the impedance for maximum output power, maximum efficiency and maximum gain [20]. These impedance points can be found by conducting continuous wave (CW) load pull measurements, with the addition of multi-tone load pull features, the linearity of a device can also be measured [17, 21]. This form of characterisation can be done over a large input power dynamic range offering the PA designer vital information as to how the device will function with load and source impedance and input drive. More importantly, this data gives ample information to the RF PA designer, to design full input and output matching networks that should enable "first run" success. More recently, load pull has been used for sensitivity analysis, to aid in calculating the minimum tolerance levels of matching networks in the production phase.

Whilst load pull information has led to many successful PA designs [22, 23], there is very little information being presented in terms of describing device behaviour. Using data collected from load pull, the behaviour of a device can at best be "inferred" by cross analysing the DC parameters with the RF measurements at the fundamental and higher harmonics. For example it can be assumed that the device is functioning in class A, if the gain is rolling off steadily with increasing drive, the harmonic content is very low and the efficiency is typically no higher than 30% at 1dB gain compression. However, if the device was originally biased at a lower quiescent current value and the efficiency performance is lower than expected, it will be difficult to explain why the device is operating as inefficiently as these numbers suggest unless there is access to the RF dynamic current and voltage waveforms.

Access to the dynamic current and voltage waveforms allows for the identification of many device features, such as RF knee walkout [24] typically found in Gallium Nitride (GaN) HEMTs (High Electron Mobility Transistors).

This is when the RF current and voltage characteristics no longer correspond with the boundaries defined by the static DCIV characteristics of the device. There are also many other interesting features, such as determining the effect of feedback at the input. However, to date these investigations have typically been conducted using on wafer devices that are more often than not very small in both size and output power.

Whilst this information is useful and in most cases scalable [18], there are some extra factors that need to be taken into account. The first is related to the thermal effects of larger devices and its affect on the performance of the device. The second is the affect of the packaging with regards to the splitting of the input RF signal at the input tab of the device and the combining of the amplified RF output signal at the output tab. The third is the supplementary affect of the increased packaging, which increases the undesired displacement currents and voltages introduced by the parasitics in the transistor. The result being significantly altered current and voltage waveforms at the output tab of the device, rendering them almost useless for immediate waveform analysis.

This is shown in Fig. 5-1, which consists of a measured dynamic drain current vs. drain voltage (load line) waveform of an 110W Si LDMOS device (taken at the output tab) clearly transgressing beyond the bounds of the DCIV [25] of the device. These measurements were done using the high power waveform measurement system developed at Cardiff University [17].The dynamic IV is shown to go well beyond the knee voltage of the device showing inductance induced displacement voltage and the current is shown to dip below zero Amps, which shows the presence of capacitance induced displacement current. In addition to these lossless charge storing components the package could also contain losses such as resistive losses in the bonding wires, package tab and the transistor itself.
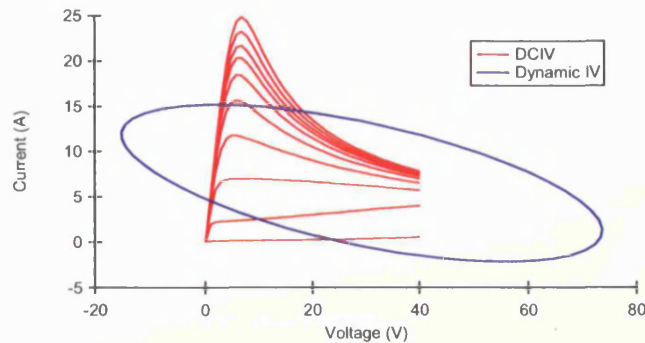
Fig. 5-1 Measured dynamic IV taken at the output tab, overlaid against the static DC IV
obtained via simulation of the MET model

For design or analysis purposes the waveforms shown in Fig. 5-1 are of little or no use. This issue can be overcome with the introduction of large signal de-embedding procedures that mathematically negate the effects of these parasitic components introduced by the package and the device imperfections. This allows for the visualisation of waveforms at a plane within the packaged device, such as the device plane or the current generator plane (I_{gen}). The resultant waveforms can then be used to characterise and optimise device performance for efficient or linear modes of operation using procedures currently being applied on smaller devices.

Chapter 5 looks at how certain components typically found in packaged devices affect the current and voltage waveforms based on an ideal transistor and then moves onto de-embedding a 5W Si LDMOS device. After this, time-domain de-embedding is applied to a high power 110W Si LDMOS device.

5.1   The Affect of Parasitic Components to Time-Domain Waveforms

Packaged transistors can be broken into two main components, the package and the device or die. In terms of the device, there are many proposed networks used for modelling FET based devices [18, 19, 26-27]. These components are combined using a segmented approach that allows for complete characterization of the input, output and feedback components present in the transistor. This is shown in Fig. 5-2 which breaks down the individual components of the device. At the measurement/package plane the device contains all of the parasitic

components but by removing the package layer, it is possible to obtain access to the waveforms at the extrinsic device plane. This is similar to where low power on-wafer measurements take place. Similarly, by cancelling the effects of the extrinsic and intrinsic network, it is possible to obtain access to the current generator, which is where the currents and voltages can be directly compared to the boundaries defined by the device. With access to this plane it is possible to directly apply waveform based engineering procedures often shown in literature [3].

The extrinsic and intrinsic components are typically modelled as lumped components and made to fit s-parameter measurements. The transistor package can similarly be modelled using lumped components but a lot of recent work has focussed on modelling these components using 3D or planar electro-magnetic (E-M) based simulators [18, 28-29]. This section focuses on providing a description of the effects of these components in terms of the current and voltage waveforms.
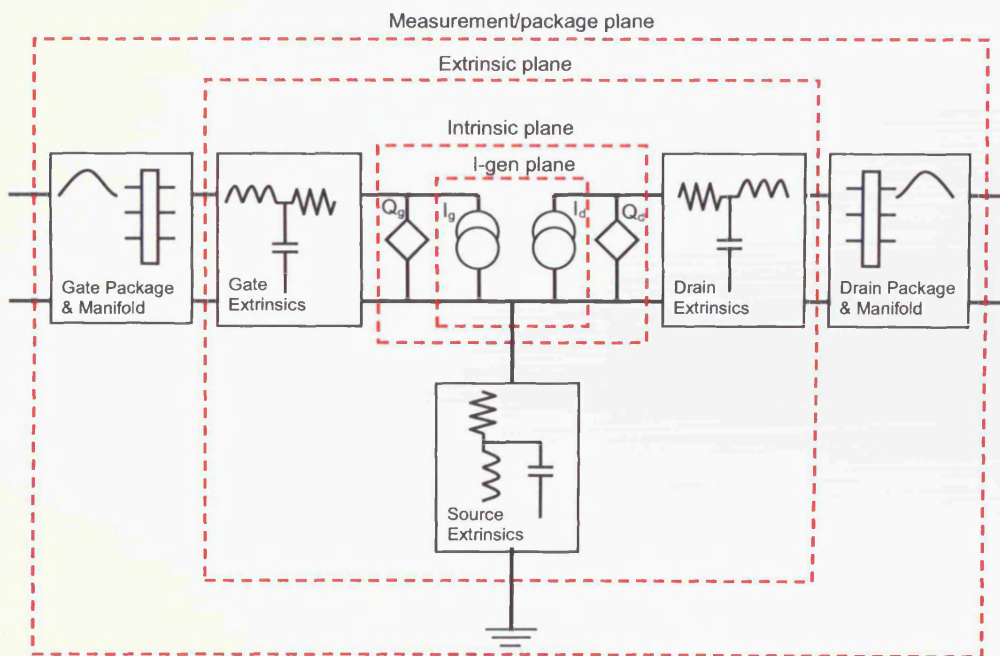

Fig. 5-2 Block diagram of a FET and the various reference planes accessible for waveform engineering

5.1.1 Intrinsic and Extrinsic Lumped Component Passive Device Modelling

There has been a large amount of work presented in the literature, relating to the equivalent circuit models typically used in device modelling [18, 19, 26-27]. This section focuses on the lumped components typically found in devices, such as capacitors, inductors and resistors and looks at their effects at the input, output and in terms of feedback.

5.1.1.1 Capacitors

Capacitors are common parasitic components found within transistors that store charge and release it as displacement current. This is modelled as a function of the time derivative of the voltage flowing across its capacitance (charge) as shown in (5-1). This is added onto the generated current I_{gen} from the transistor's current source to form I_{meas}, which is the current at the measurement port as shown in (5-2). The capacitance typically found in solid-state devices is dependent on the semiconductor material and the physical size of the device [3]. Some semiconductor materials have shown to contain a variable capacitance that is dependent on the drain and gate voltages. This has been widely reported in Si LDMOS devices [28, 30] and is discussed later.

$$I_{disp} = C\frac{dv}{dt} \tag{5-1}$$

$$I_{meas} = I_{disp} + I_{gen} \tag{5-2}$$

In terms of the waveforms, the measured current at the output of the device will now contain the extra displacement current generated by the capacitor. To demonstrate this more clearly a simulation is done with an ideal device (no parasitic components) operating in class B (all higher harmonics set to short circuit). This is shown in Fig. 5-3(b) where the measured current waveform of a device operating in ideal class B drops below 0mA and follows the displacement current curve generated by the capacitor when in the off-state part of the RF cycle. In other words, the capacitor is effectively "smoothing" the current waveform where the displacement current is the smoothing component. It is

interesting to note that if the capacitance is increased further it is possible to produce a measured current waveform that no longer resembles the initial generated current waveform. This could be the case for high power transistors where the intrinsic capacitance can be in the tens of pico-Farads. The inserted capacitor has no effect on the voltage waveform.
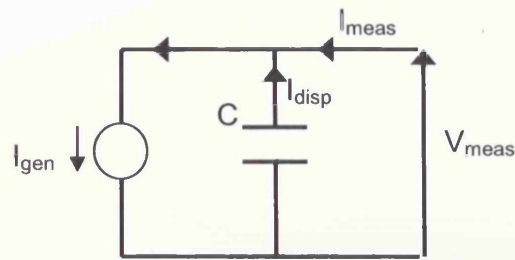
(a)
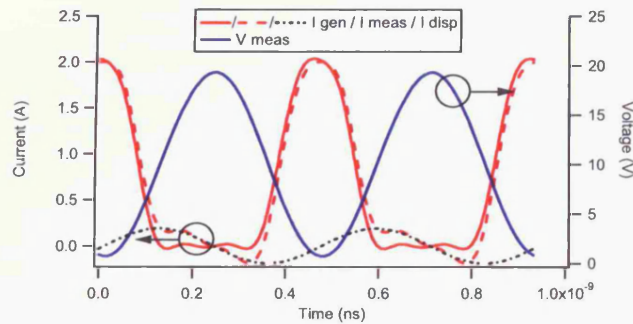
(b)

Fig. 5-3 (a) The circuit diagram denoting the currents at various parts of the circuit (b) The current and voltage waveforms before and after the capacitor

For optimum performance in terms of power at the I_{gen} plane, it is required to cancel the effects of the capacitor. If this is not done the output power of the device drops according to the phase offset at the I_{gen} plane given by the reactive component, which in this case is the capacitor [16]. To compensate for this, the impedance at the measurement plane is adjusted to negate the reactive effect of the capacitor as shown in Fig. 5-4. Since the capacitor is a parallel component, the impedance will vary along a contour of constant admittance. In this case an impedance of $8.69 + 1.59j$ Ω is required to produce a real impedance of 9 Ω at the I_{gen} plane.
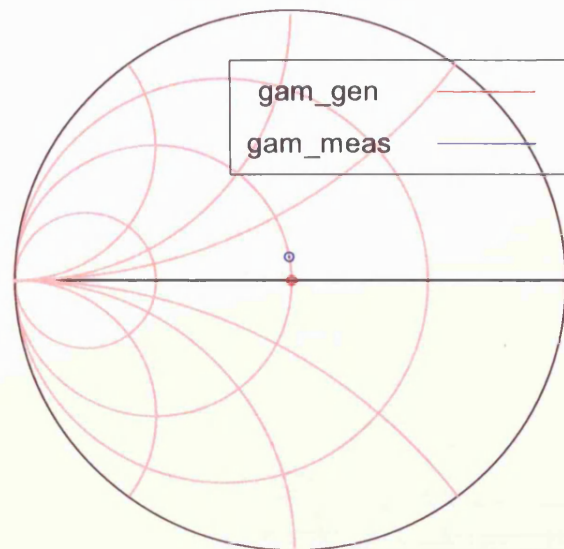
Fig. 5-4 The optimum impedance for power at the I_{gen} plane and at the measurement plane with a capacitor connected at the output of the current generator ($Y_0 = 1/9$ S)

Now, considering a "non-linear" capacitor sensitive to the drain voltage. Non-linear capacitors are typically used to model the intrinsic capacitors of semiconductor devices. The profile of the capacitor varies according to the device technology and the physical layout of the device. For analytical purposes, consider a capacitor modelled as a function of the reciprocal of the drain voltage (as shown in Fig. 5-5(a)). This dynamic capacitance behaviour is then simulated in the same environment described earlier with the results Fig. 5-5(b) showing a more significant deviation to the originally generated current waveform. The difference in the current waveform is highlighted more clearly in the displacement current generated when the RF current is high. This coincides with a low drain voltage, which causes an increase in the dynamic capacitance that generates a larger displacement current component. Despite the dynamic behaviour of the capacitor it is still possible to match to the "average" capacitance, which can be determined with respect to the voltage waveform being applied across it. For example in the case of a sinusoidal voltage waveform this results in a slight increase in capacitance.

(a)

(b)
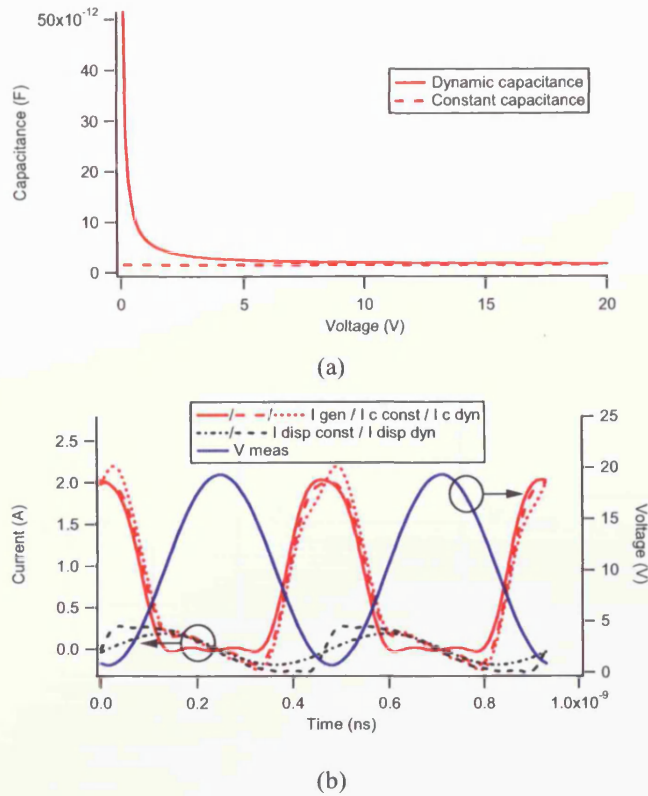
Fig. 5-5 (a) The dynamic capacitance's sensitivity to voltage (b) The current waveforms at the I_{gen} plane and at the measurement plane with a linear and non-linear capacitor.

Typically, device models consist of intrinsic charge generators (otherwise known as trans-capacitance) [18]. These charge generators behave in a capacitive manner but are functions of both the gate and drain voltages and are usually very complex. A specific implementation of a charge generator will be discussed later.

5.1.1.2 Inductors

Similar to capacitors, all semiconductor devices contain some form of inductance due to device metallization. The inductance found in devices are series components, which store charge to release it as displacement voltage. This is modelled as a function of the inductance and the time differential of the current waveform (5-3), leaving the current component unperturbed. The displacement voltage (V_{gen}) is then added onto the voltage presented at the I_{gen} plane to form V_{meas} as shown in (5-4). The inductance in semiconductor devices

is typically linear and usually accompanied with some resistive loss which will be discussed later.

$$V_{disp} = L\frac{di}{dt}$$

(5-3)

$$V_{meas} = V_{gen} + V_{disp}$$

(5-4)
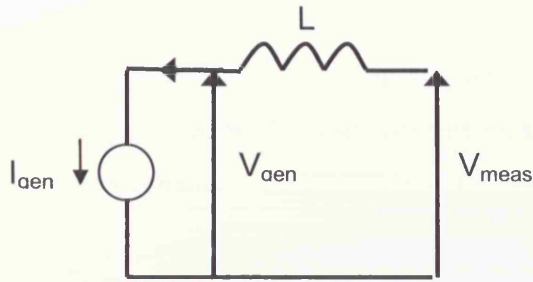
(a)
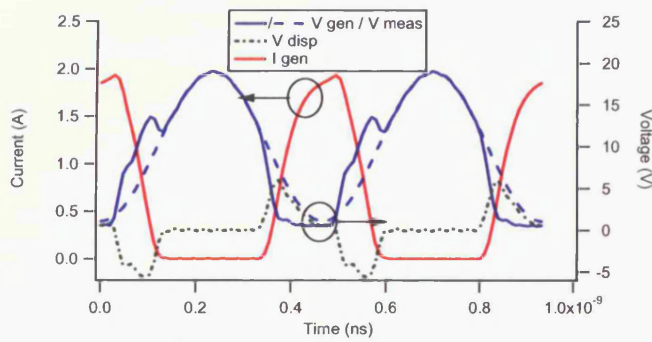
(b)

Fig. 5-6 (a) The circuit diagram denoting the voltages at various parts of the circuit (b) The current and voltage waveforms before and after the inductor

A simulation is done with an ideal device biased in class B and sinusoidal voltage being applied at the current source. The voltage waveforms in Fig. 5-6(b) highlight the affect of the displacement voltage on the output voltage waveform (Vmeas). The displacement voltage discharges when the RF current is turned on and has no affect when the RF current is off. It is important to note that the voltage waveform at the measurement plane (Vmeas) is sinusoidal in shape and not at the I_{gen} plane (Vgen). This is because of the real only impedance (at f_0, short circuit at higher harmonics) being presented at the measurement plane,

which forces the voltage to be sinusoidal. The inductance then alters the impedance being presented at the I_{gen} plane, which forces the voltage to become non-sinusoidal.

The reactive component introduced by the inductor can be negated by inserting a negative reactive impedance along a contour of constant resistance. In this case to produce a real impedance of 9 Ω at the I_{gen} plane, it is required to present 9 − 2.7j Ω at the measurement plane as shown in Fig. 5-7. In reality, the first instance of inductance occurs in the extrinsic circuit of the device model after the intrinsic capacitances. This makes the displacement voltage a function of the total current at the intrinsic plane.
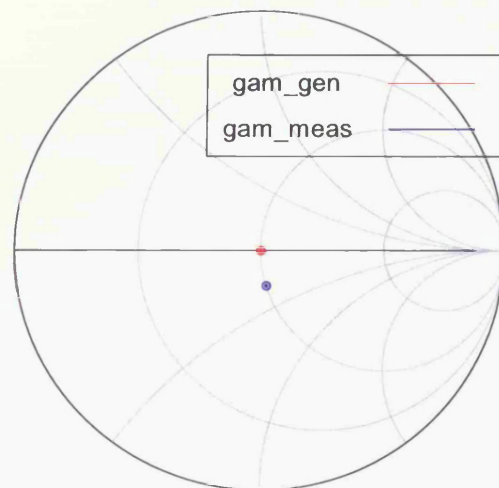
Fig. 5-7 The optimum impedance for power at the I_{gen} plane and at the measurement plane with an inductor connected at the output of the current generator (Z_0 = 9 Ω)

5.1.1.3 Resistors

Resistors are used to model the series loss of the line metallization and are placed in the extrinsic part of the device model. Since it is placed in series the resistor drops voltage as a function of current as determined by Ohm's law as shown in (5-7) and (5-8) as well as Fig. 5-8(b). This loss of voltage across the resistor reduces the output power and efficiency being measured. However, the resistance is typically small in high power devices due to the large number of cells connected in parallel. It is also important to note that the series resistor is

the only component that affects the DC content of the waveforms. Due to the DC source originating from an outside source, the actual DC voltage at the I_{gen} plane is the supply voltage V_{DD} subtracted against the DC voltage loss across the resistor.

$$V_{loss} = iR \tag{5-6}$$

$$V_{meas} = V_{gen} + V_{loss} \tag{5-7}$$

To compensate for the resistance it is required to reduce the resistance along a contour of constant reactance. In this case, this is done by reducing the impedance at the measurement plane from 9 Ω to 7 Ω.

(a)

(b)

Fig. 5-8 (a) The circuit diagram denoting the voltages at various parts of the circuit (b) The current and voltage waveforms before and after the resistor
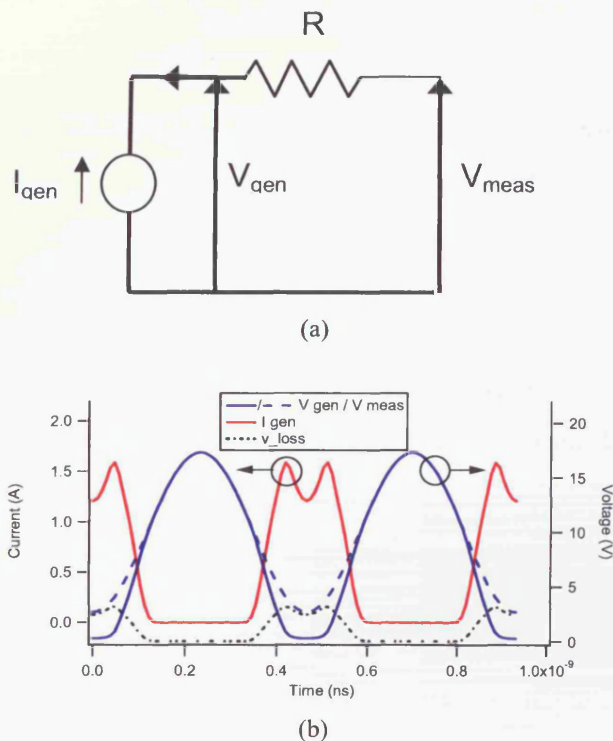
5.1.1.4   Feedback / Feed forward Components

The feedback / feed forward components in a device are lumped component based capacitors, inductors, mutual inductances and resistors. The types of

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feedback are limited to what is typically reported in literature [18, 19, 26-27]. However, it is important to note that when used in a feedback orientation the voltage and current used in the calculation is now the difference between the two connecting ports. This is shown in Fig. 5-9.

The feedback components can have a significant effect at the input port. Due to the large current and voltage swings at the output port of the device, the expressions v_{diff} and i_{diff} can be significantly larger than the currents and voltages at the input port. In this case the effect of feedback can be separated into two components, the fundamental and the higher harmonics. At the fundamental frequency of operation the feedback often negates the input stimulus resulting in a drop of gain. At the higher harmonics, the feedback introduces unwanted higher harmonics in the input stimulus that could have a positive or negative effect on the device's performance.

5.1.2 Packaging Components Passive Device Modelling

The package is a critical component of high power devices for thermal dissipation of heat and for electrical addition of the current from separate transistor cell blocks. The aim of the package is to have low loss to ensure maximum power transfer from the transistor die to the output tab, which is where measurements typically take place [18]. In medium power transistors, this includes the use of bonding wires, which bridges the transistor die and the output tab. In high power Si LDMOS devices, there is also the addition of metal-oxide-semiconductor (MOS) capacitors, which eases the requirements for matching network design [18, 23]. Recent work done by Wood et al [18, 26], has shown that there is also a need to incorporate the device manifold. Again, this is especially applicable to high power Si LDMOS devices, due to their large device periphery, which produces a large spread in phase of the load being presented to the individual transistor cells.

$$I_{disp} = C\frac{dv_{diff}}{dt}$$

where

$$v_{diff} = v_{gen} - v_{in} \qquad (5\text{-}8)$$

(a)

$$V_{disp} = L\frac{di_{diff}}{dt}$$

where

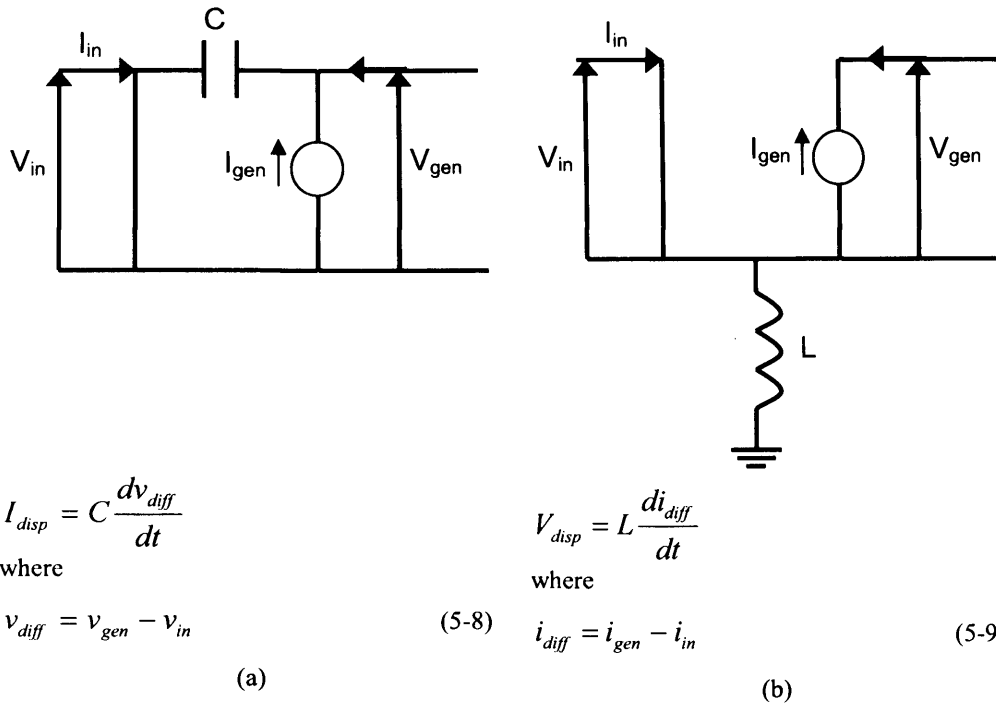$$i_{diff} = i_{gen} - i_{in} \qquad (5\text{-}9)$$

(b)

Fig. 5-9 (a) The circuit diagram denoting currents and voltages for a capacitive feedback circuit (b) The circuit diagram denoting currents and voltages for an inductive feedback circuit

5.1.2.1 Device Manifold

The device manifold connects the individual transistor cells and acts as a signal separator at the input and a signal combiner at the output and exists as part of the die. The device manifold is behaves like a transmission line with some small amounts of loss with increasing frequency. This in theory has very little effect on the waveforms other than a phase delay. In practice due to the large device periphery of high power transistors, the device manifold becomes very large and produces a spread in phase between individual cells in a transistor die [18]. This spread in phase at the output terminals makes it difficult to provide a constant impedance to each of the transistor dies, which makes it problematic in providing specific impedance terminations such as short and open circuits typically used in high efficiency PA design. To illustrate this, a simulation is done in Agilent ADS™ planar simulator Momentum™ of a device manifold for a 4.8mm Si LDMOS device supplied by Freescale Semiconductor Inc. The results in Fig. 5-10 show the phase variation that would happen if an open circuit was provided at the output port of the manifold at 6GHz. The impedances being

provided to the device is shown to vary by $0.3 \pm 1500j \; \Omega$. The zoomed in polar plots in Fig. 5-11, show the phase spreading with increasing frequency. The phase difference at 2GHz is 3°, which provides a "good enough" open circuit to the device, but at 10GHz the phase difference is approximately 16°. This consequently increases the difficulty in providing the fixed impedances typically required for high efficiency PA design [29].

(a)

(b)

Fig. 5-10 (a) Device manifold layout within ADS Momentum^{TM} (b) The phase difference between ports at 6GHz with an open circuit presented at the output of the device manifold

(a)   (b)   (c)   (d)

Fig. 5-11 (a) Zoomed in polar plot of the phase difference at 2GHz (b) Zoomed in polar plot of the phase difference at 4GHz (c) Zoomed in polar plot of the phase difference at 6GHz (d) Zoomed in polar plot of the phase difference at 10GHz

5.1.2.2 Bondwires

Bondwires are utilised to connect the device to the device output tab or to internal matching networks within the package. A bondwire is a metal wire with

a small radius, usually made of gold for high conductivity or for cost cutting purposes made of aluminium. At high frequencies, the bondwire can be modelled as a series inductance with a small of amount of resistance and a capacitance to ground to model the contact with the tab or die [18]. This is shown in Fig. 5-12, where a 3D simulation of the input and output bondwires within an H-block fixture [18, 32] is conducted in Ansoft HFSS^{TM}. The s-parameter results in Fig. 5-13 show a high level of agreement between the circuit model and the 3D simulation over a large bandwidth of frequency. Since the principle component of a bondwire is a series inductance, the voltage waveform will be altered as shown in Fig. 5-6.

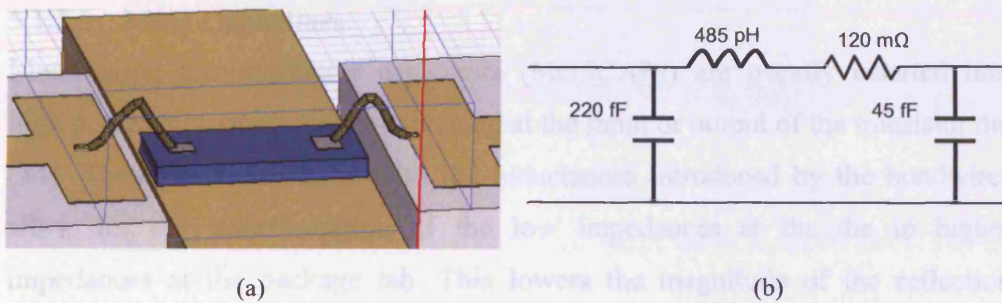(a)   (b)

Fig. 5-12 (a) HFSS simulation of the input and output bondwires (b) Equivalent circuit of a single bondwire
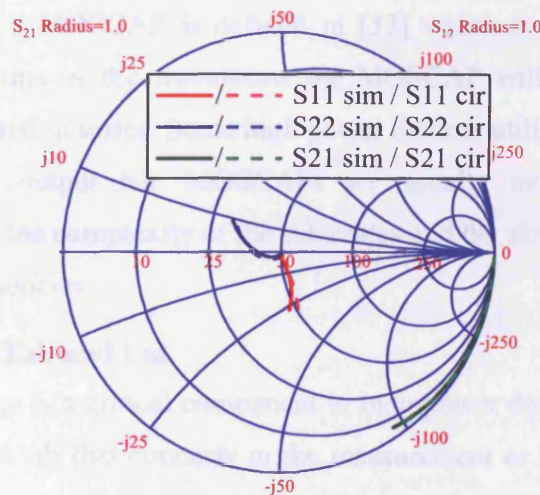

Fig. 5-13 S-parameters of the 3-D EM simulation and the equivalent circuit model

In high power transistors, multiple bondwires are necessary due to the large amounts of current present at the drain terminal of the device. These bond wires then start to interact in the form of mutual inductance. This has been shown to slightly increase the overall inductance of the sub-network [18]. Mutual inductance is also present between the input and output bondwires which as a consequence increases the amount of feedback present within the device. With all of these complex interactions, the level of difficulty in modelling these structures using lumped models increases significantly. Instead, it is preferred to conduct 3D E-M simulations that allow for the drawing of arbitrary shapes [33] or to conduct s-parameter measurements of the structures within a controlled measurement environment [7].

5.1.2.3 MOS Capacitors

Metal-oxide semiconductor capacitors (MOSCAPs) are usually inserted into high power transistors for pre-matching at the input or output of the transistor die [34]. These in combination with the inductances introduced by the bondwires allow for the transformation of the low impedances at the die to higher impedances at the package tab. This lowers the magnitude of the reflection coefficient required for matching network design, which eases the design process especially for communications based applications where the bandwidth of operation is in the tens of megahertz.

The behaviour of a MOSCAP is defined in [33] which is effectively a lossy capacitance. In terms of the waveforms the MOSCAP will affect the current waveform when used in series. Some high power devices utilize the MOSCAP in parallel with the output tab. MOSCAPs are usually modelled using 3-D simulations due to the complexity of the substrates and the skin depth effects that occur at high frequencies.

5.1.2.4 Package Tab and Lid

The device package is a critical component in high power devices. The package consists of a metal tab that connects to the measurement or PA fixture and the bondwires and can be modelled as a wide microstrip line with low characteristic impedance [18]. The effect on the waveforms is similar to the device manifold, with a small phase perturbation and a spreading of phase to each of the

individual bondwires. In addition to that the package has a ceramic lid that encloses the device as shown in Fig. 5-14. This introduces some feedback between the input and output ports of the package. Newer high power devices are housed in plastic packages, which reduces the cost of the overall package but as a consequence the feedback is shown to increase [18].
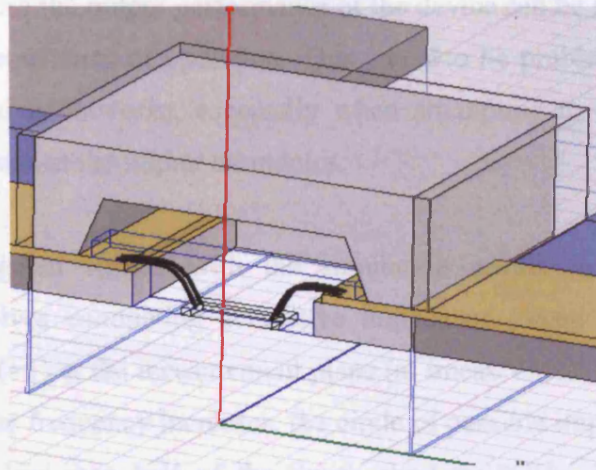
Fig. 5-14 Cross section of a packaged device, shown within Ansoft HFSS^{TM}

### 5.1.3   Circuit combinations and some possible side-effects

So far the discussion of parasitic components has been centred on one component at a time. However, in reality due to the sequential cascading of these components, the overall package network may feature unexpected properties that will not be obvious at first sight.

5.1.3.1   Low Pass Filtering

The first and most commonly found possible circuit combination is the low pass filter. This is often found in transistors and is the primary cause for the drop in maximum available gain (MAG) of transistors with frequency. This feature is usually attributed to the input series network r_g, c_{gs}. At the output port, there is another low pass filter network which coupled with the input filter network defines the overall transistor gain drop with frequency. However, the output filter network has a second effect, which is more visible in large signal measurements. At higher frequencies, the drain low pass filtering network starts

to dissipate power, which as a consequence lowers the fundamental output power and drain efficiency at the output measurement port. This is shown in Fig. 5-15(b), where a 0.5 dB loss in power and a 5% drop in efficiency occurs over the frequency sweep, using the network in Fig. 5-15(a). In this simulation the input stimulus has been held constant and the same impedance of 9 Ω (R_{opt}) has been presented at the I_{gen} plane. This can have a major effect in broadband applications where the output performance of the device can be significantly less at the higher frequencies of operation. This can also be problematic for multi-harmonic matching networks, especially when attempting to provide specific circuit terminations at the higher harmonics.

This is investigated further with the simulation results in Fig. 5-16, the simulation involves conducting a reactive impedance sweep with a constant magnitude of Γ (=1) at the measurement plane (at Imeas/Vmeas) as a function of frequency. As the frequency increases, the circle of possible impedances reduces significantly to less than half of the Smith chart by 9GHz. In this case, the network inhibits the ability to provide high impedances at the I_{gen} plane, at higher frequencies. This could have severe implications for certain high efficiency modes of operation such as class F where an open circuit is required at the third harmonic.
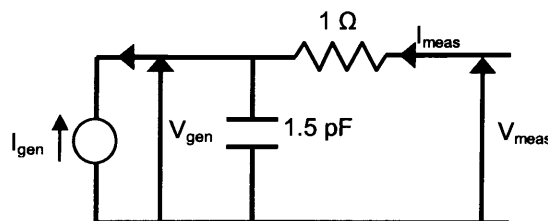
(a)
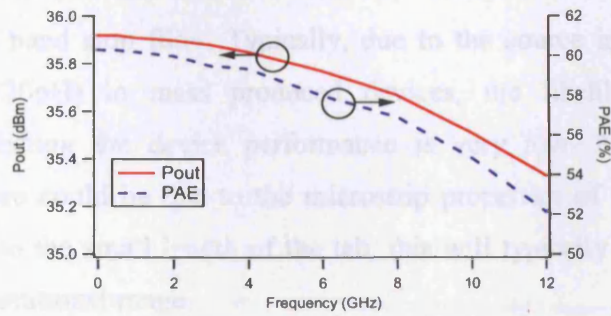
(b)

Fig. 5-15(a) The output network being simulated (b) The output power and efficiency performance against frequency with constant input stimulus
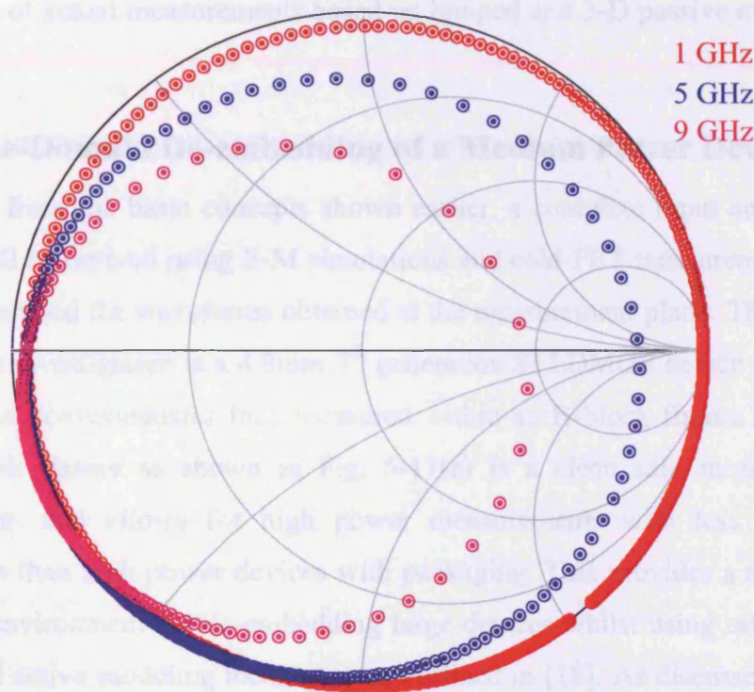

1 GHz
5 GHz
9 GHz

Fig. 5-16 Smith chart at the I_{gen} plane outlining the reduction in impedance matching capabilities with increasing frequency

5.1.3.2 Circuit Resonances

The two circuit resonances possible are either series or parallel LC networks. Series LC networks can occur between the output drain-source capacitance and the source inductance within the device or intentionally inserted in the form of internal matching networks [23]. Parallel LC networks can occur between the source inductance and the any external capacitance, for example in the form of a

bond pad capacitance that is not on the device die. This sort of resonance behaves like a band stop filter. Typically, due to the source inductance being very small (<20pH) in mass produced devices, the likelihood of circuit resonances effecting the device performance is very low. Another possible circuit resonance could be due to the microstrip properties of the device tabs. However, due to the small length of the tab, this will typically be well beyond the device's operational range.

This concludes the summary of device and package components. The work in the next two subsections covers two specific examples of time-domain de-embedding of actual measurements based on lumped and 3-D passive modelling techniques.

5.2   Time-Domain De-embedding of a Medium Power Device

Expanding from the basic concepts shown earlier, a complete input and output network will be derived using E-M simulations and cold-FET measurements and used to de-embed the waveforms obtained at the measurement plane. The device used in this investigation is a 4.8mm 7th generation Si LDMOS device provided by Freescale Semiconductor Inc., measured within an H-block fixture [18, 32]. The H-block fixture as shown in Fig. 5-17(a) is a clean safe measurement environment, that allows for high power measurements with less parasitic components than high power devices with packaging. This provides a relatively "simpler" environment for de-embedding large devices whilst using established passive and active modeling techniques as outlined in [18]. As discussed earlier the de-embedding is separated into two stages, the package and the device. These are all constructed together using the segmented approach outlined in [18]. The waveform based measurements were taken at the plane outlined in Fig. 5-17(b), this was done using a multi-line TRL calibration [35] to allow for a wide frequency bandwidth of measurements covering multiple harmonics.
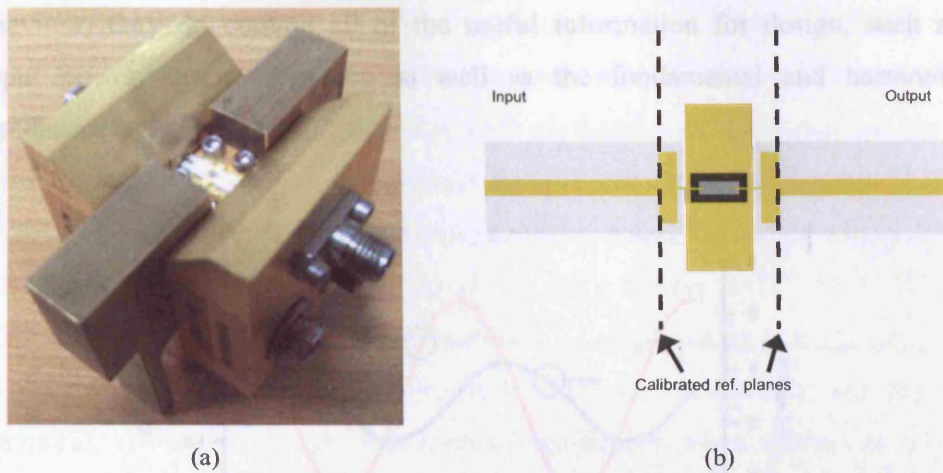
| (a) | (b) |

Fig. 5-17 (a) A picture of the H-block measurement fixture (b) The calibrated plane at which time-domain measurements were taken

Before applying any de-embedding, it is worth looking at the currents and voltages being measured. This allows for a qualitative measure of the effects of the parasitic components on the waveforms compared to what would be expected in literature. This is done using measured time domain data collected with the high power measurement system developed at Cardiff University [17]. The measured current and voltage waveforms are taken at the impedance for peak output power at 1dB compression with the device biased at I_{dq} = 5 mA/mm. The measured waveforms in Fig. 5-18, show a sinusoidal drain current waveform dropping below zero Amps and a drain voltage waveform centred around the drain bias voltage of 28V with a large fundamental component and some noticeable amounts of higher harmonic content. The sinusoidal current swing provides ample evidence of a sizeable amount of capacitance, which is significantly altered from the expected half-rectified voltage. Whilst the shape of the voltage swing is close to what is expected in theory, the amplitude of the swing is a lot smaller than what would have been predicted using load-line theory [3].

At the gate terminals both the current and voltage are sinusoidal in shape, which suggests the presence of little or no feedback. However, the voltage swing is shown to be smaller than would have been expected. However, it is still worth noting that whilst these waveforms are not showing the expected theoretical

behaviour, they do contain all of the useful information for design, such as output power, drain efficiency as well as the fundamental and harmonic impedances.
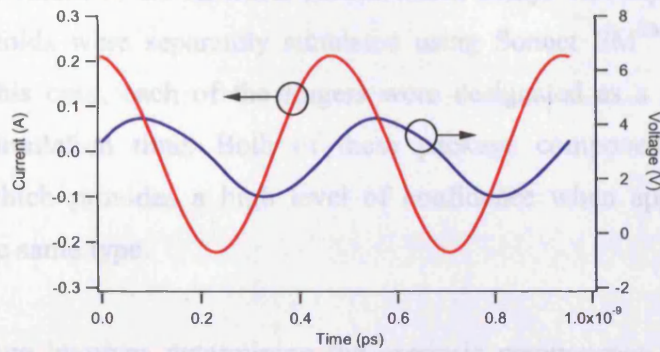
(a)
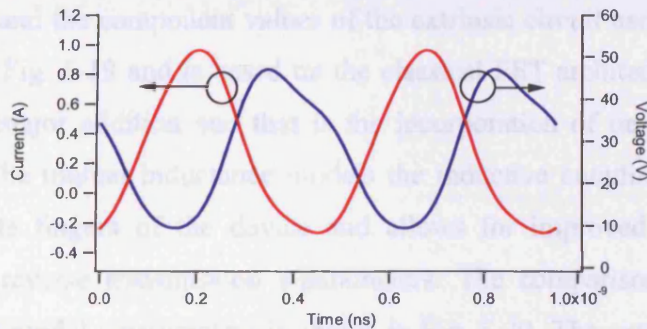
(b)

Fig. 5-18 (a) Measured current and voltage waveforms at the input terminals (b) Measured current and voltage waveforms at the output terminals

5.2.1 Passive modeling of the device

The passive model of the entire device is begun by modeling the package. In this case the package network consists of an input and output bonding wire with a small wide-microstrip feed line as shown in Fig. 5-17. To model this accurately, the dimensions of the bondwire were measured under a precision microscope in the "x", "y" and "z" directions. This 3-D structure was then simulated using HFSS as shown in Fig. 5-12(a) over a wide frequency bandwidth (300MHz – 12GHz). The simulation was set to model the features of the individual bonding wires as well as the mutual inductance between the input and output bonding

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wires [26] using internal ports in the simulator. Due to the difficulty in simulating these structures at lower frequencies, the BONDW tool in ADS™ was used to predict the DC performance of the bondwires. By removing these effects the measurements are effectively being conducted at the device plane, which is equivalent to an on-wafer measurement setup. The input and output device manifolds were separately simulated using Sonnet EM™ from DC to 12GHz. In this case, each of the fingers were designated as a single port to reduce to simulation time. Both of these package components are highly repeatable which provides a high level of confidence when applied to other devices of the same type.

The next stage involves determining the extrinsic components of the device, which was done using cold-FET small signal S-parameter measurements [26]. The network and the component values of the extrinsic circuit used in the model are shown in Fig. 5-19 and is based on the classical FET architecture. However there is one major addition and that is the incorporation of on device mutual inductance. The mutual inductance models the inductive coupling between the drain and gate fingers of the device and allows for improved fitting of the forward and reverse transmission s-parameters. The comparison between the measured and model s-parameters is shown in Fig. 5-20. The extrinsic model is shown to fit both S(1,1) and S(2,2) over a large frequency bandwidth. In turn S(2,1) and S(1,2) are shown to agree with measured data from 2GHz up to 6GHz. After that there is shown to be an increasing difference between the measured and model S(1,2) and S(2,1) phase. After further optimizing the values it was found that these component values represented the best overall fit in S-parameters considering the fundamental frequency of operation of 2.1GHz. Whilst it is important to note this difference in phase, the actual effect of this inaccuracy is not expected to be large due to a low f_T of 7.5GHz [15].

The drain and gate charges were then determined by conducting Root model based measurements [36] and fitting the charges to the measured data as outlined in [37]. This form of charge extraction incorporates the effects of both the input

and output voltages in a fully charge conservative manner. This part of the de-embedding procedure was completed by Freescale Semiconductor Inc and now allows for access to the current and voltage waveforms at the I_{gen} plane.
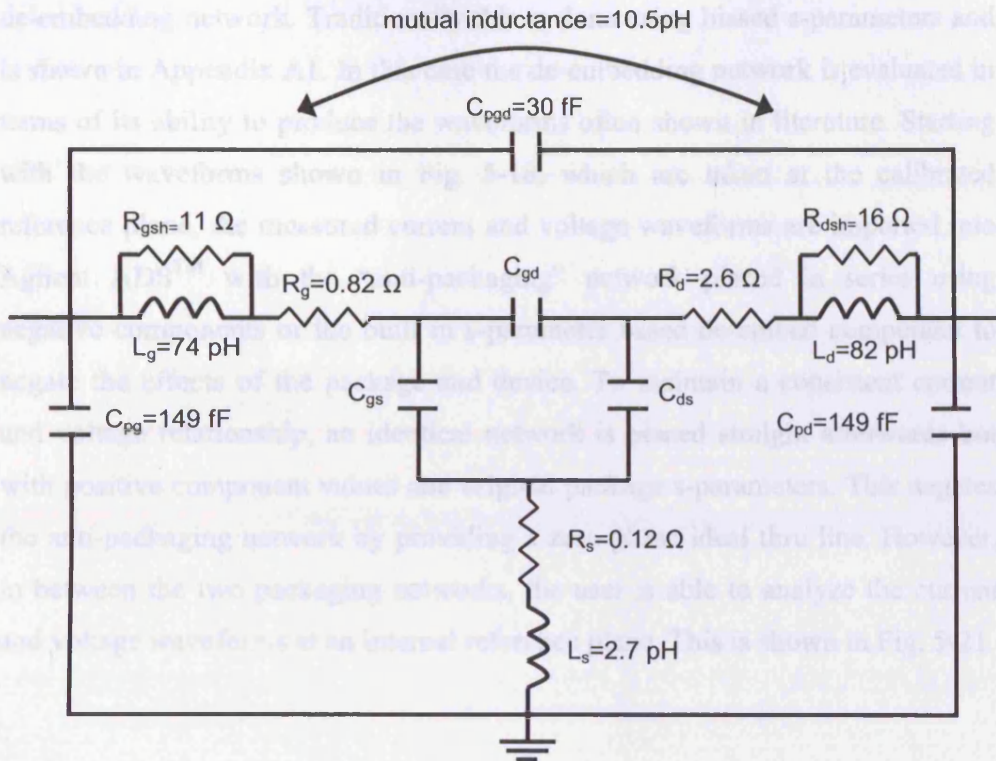
mutual inductance =10.5pH

C_{pgd}=30 fF

R_{gsh}=11 Ω

R_g=0.82 Ω

C_{gd}

R_{dsh}=16 Ω

R_d=2.6 Ω

L_g=74 pH

L_d=82 pH

C_{gs}

C_{ds}

C_{pg}=149 fF

C_{pd}=149 fF

R_s=0.12 Ω

L_s=2.7 pH

Fig. 5-19 Cold FET circuit diagram that is used to model the extrinsic components of the device [26]

S_{21} Radius=1.0

S_{12} Radius=1.0

/— — — Smeas11 / Smod11
/— — — Smeas22 / Smod22

/— — Mag meas S21 / Mag mod S21
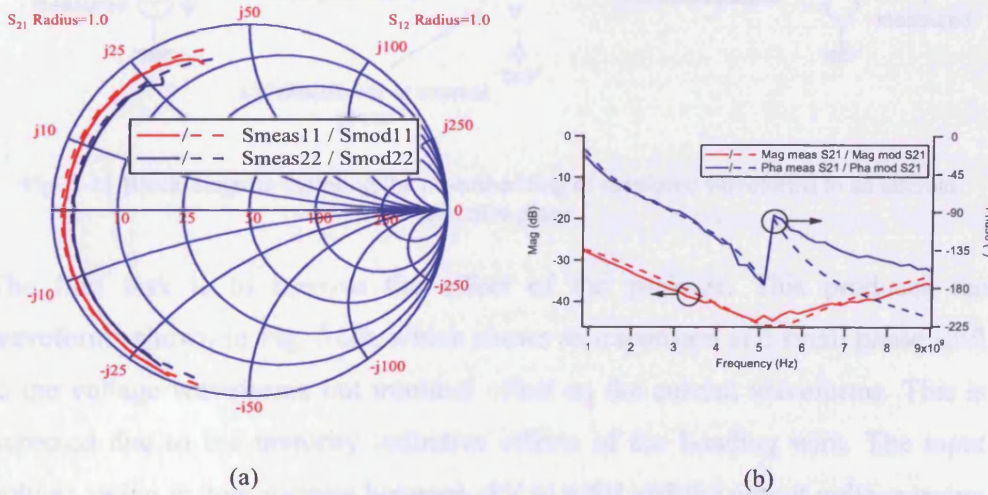/— — Pha meas S21 / Pha mod S21

(a)

(b)

Fig. 5-20 (a) Measured and model S-parameters at the extrinsic device plane shown on a Smith chart (b) Forward and reverse transmission measured and model S-parameters at the extrinsic device plane

5.2.2 Obtaining waveforms at the I-gen plane

Now that a suitable network has been developed for the package and the device extrinsic and intrinsic components, the next step in the process is to validate the de-embedding network. Traditionally this is done using biased s-parameters and is shown in Appendix A1. In this case the de-embedding network is evaluated in terms of its ability to produce the waveforms often shown in literature. Starting with the waveforms shown in Fig. 5-18, which are taken at the calibrated reference plane, the measured current and voltage waveforms are imported into Agilent ADS^{TM} with the "anti-packaging" network placed in series using negative components or the built in s-parameter based de-embed component to negate the effects of the package and device. To maintain a consistent current and voltage relationship, an identical network is placed straight afterwards but with positive component values and original package s-parameters. This negates the anti-packaging network by providing a zero phase ideal thru line. However, in between the two packaging networks, the user is able to analyze the current and voltage waveforms at an internal reference plane. This is shown in Fig. 5-21.
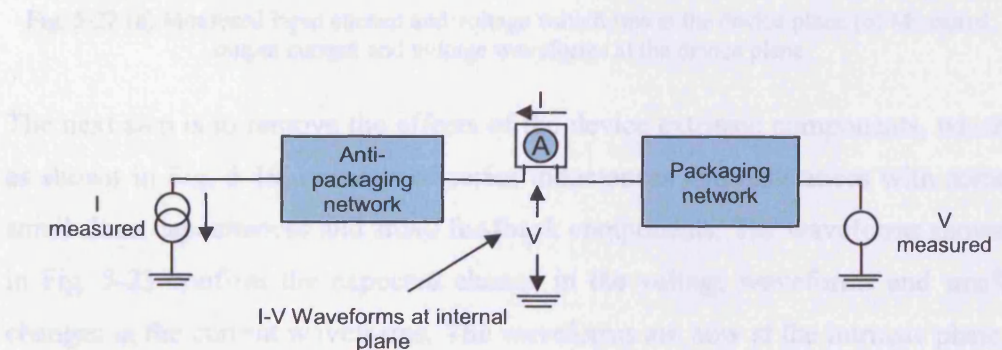

Fig. 5-21 Block diagram outlining the de-embedding of measured waveforms to an internal reference plane

The first task is to remove the effect of the package. This produces the waveforms shown in Fig. 5-22, which shows an expansion and small phase shift in the voltage waveforms but minimal effect on the current waveforms. This is expected due to the majority inductive effects of the bonding wire. The input voltage swing is now varying between -1V to 6.5V and the output voltage swing is now between 5.5V to 50.5V, each centred at their DC bias points.
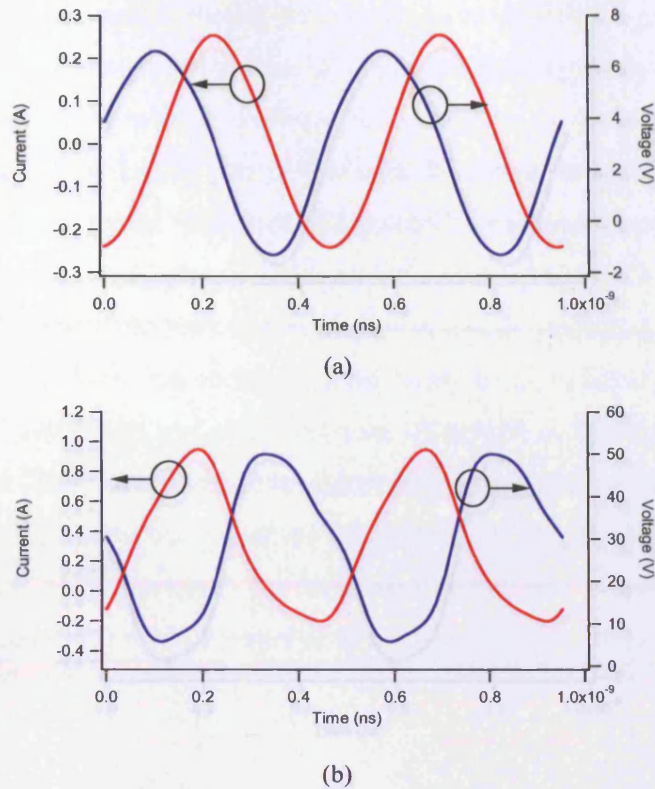
(a)

(b)

Fig. 5-22 (a) Measured input current and voltage waveforms at the device plane (b) Measured
output current and voltage waveforms at the device plane

The next step is to remove the effects of the device extrinsic components, which
as shown in Fig. 5-19, consists of series inductances and resistances with some
small shunt capacitances and small feedback components. The waveforms shown
in Fig. 5-23 confirm the expected change in the voltage waveforms and small
changes in the current waveforms. The waveforms are now at the intrinsic plane,
which implies that the only form of further de-embedding required is the
cancellation of the input and output capacitive components. This can be
confirmed by visually examining the output current waveform in Fig. 5-23(b),
and comparing it to an ideal class B waveform (see Fig. 5-8(b) for more details).
This also implies that the voltage waveform correction is now complete.
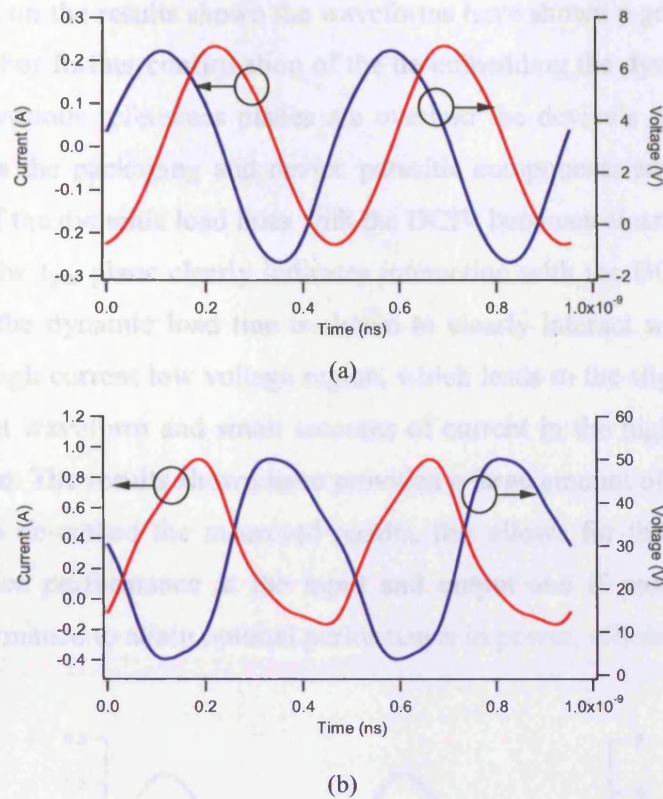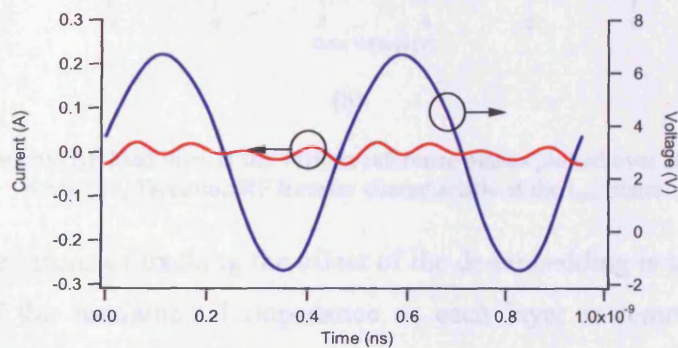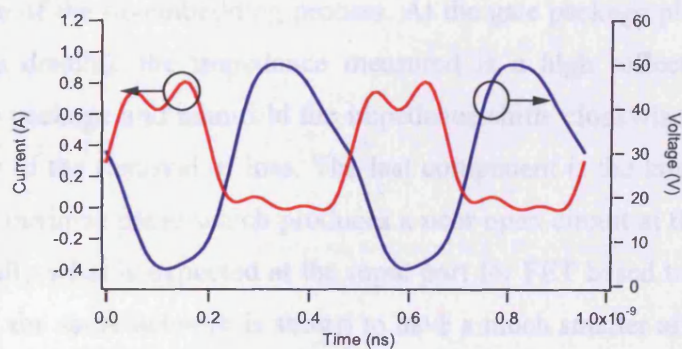
45

(a)

(b)

Fig. 5-23 (a) Measured input current and voltage waveforms at the intrinsic plane (b) Measured output current and voltage waveforms at the intrinsic plane

The next stage of de-embedding involves the removal of the input and output capacitors which are modeled as charge generators, to produce a charge conservative model [39]. This will allow for visualization of the results at the I_{gen} plane as shown in Fig. 5-24. The input waveforms show the same voltage waveform as before but a very small amount of gate current, which can be attributed to the accuracy of the measurement system used [39]. This is because Si LDMOS transistors do not contain any real current sources typically found in other device technologies such as GaAs and GaN [18]. At the output port, the current waveforms show a half-rectified current waveform with some bifurcation and the same voltage waveform as before. The current waveform is shown to be flat and at 0A in the off region, which indicates that the drain charge generator has been accurately modeled.

So far, based on the results shown the waveforms have shown a good agreement with theory. For further confirmation of the de-embedding the dynamic RF load lines at the various references planes are overlaid the device's static DCIV in Fig. 5-25. As the packaging and device parasitic components are removed the interaction of the dynamic load lines with the DCIV becomes clear. The dynamic load line at the I_{gen} plane clearly indicates interaction with the DCIV boundary, in this case the dynamic load line is shown to clearly interact with the device knee in the high current low voltage region, which leads to the slight bifurcation of the current waveform and small amounts of current in the high voltage, low current region. The results shown have provided a large amount of confidence in the ability to de-embed the measured results, this allows for the possibility to analyze device performance at the input and output and if possible optimize device performance to attain optimal performance in power, efficiency or gain.
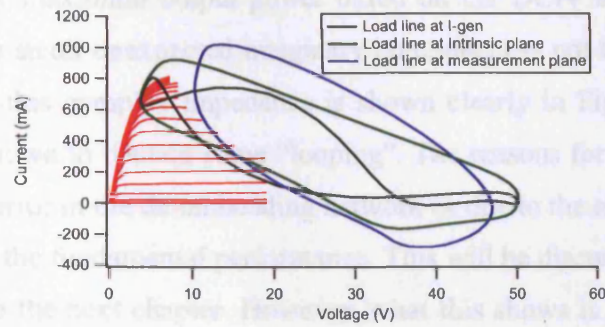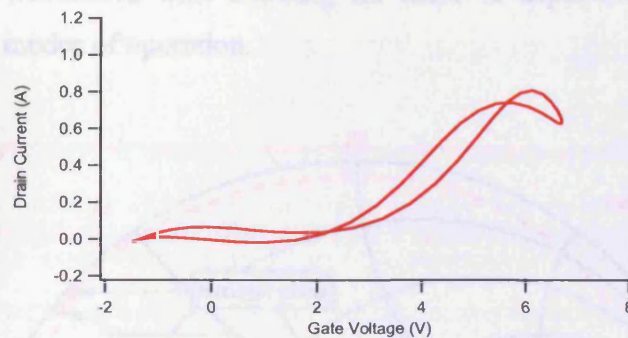

(a)

(b)

Fig. 5-24 (a) Measured input current and voltage waveforms at the I_{gen} plane (b) Measured output current and voltage waveforms at the I_{gen} plane

(a)

(b)

Fig. 5-25 (a) Dynamic RF load lines at the various reference planes plotted over static DCIV of the device (b) Dynamic RF transfer characteristic at the I_{gen} plane

An alternative means of tracking the effect of the de-embedding is to analyze the movement of the fundamental impedance as each layer is removed. This is shown in Fig. 5-26 where the impedance movement is plotted on a Smith chart for each stage of the de-embedding process. At the gate package plane (see Fig. 5-2 for more details), the impedance measured is a high reflect. After first removing the package and manifold the impedance shifts clockwise and slightly outwards due to the removal of loss. The last component is the large capacitive charge at the intrinsic plane which produces a near open circuit at the I_{gen} plane. This is typically what is expected at the input port for FET based transistors. At the load port, the same network is shown to have a much smaller affect in terms of phase movement but it can be seen that only by completely removing the parasitic effects of the package and the device does the load impedance being presented to the I_{gen} plane become a majority real impedance. The fundamental load impedance of the I_{gen} load line is 57 -10j Ω, which is close to the calculated

60 Ω load for maximum output power based on the DCIV as outlined in [3]. However, this small unexpected imaginary component is not typically reported. The result of this complex impedance is shown clearly in Fig. 5-25 where the load line is shown to contain some "looping". The reasons for this could be due to a possible error in the de-embedding network or due to the affect of the higher harmonics on the fundamental performance. This will be discussed further in this chapter and in the next chapter. However, what this shows is that with a robust de-embedding procedure, it is possible to achieve successful de-embedding of time-domain waveforms thus allowing for more in depth investigations into enhanced PA modes of operation.

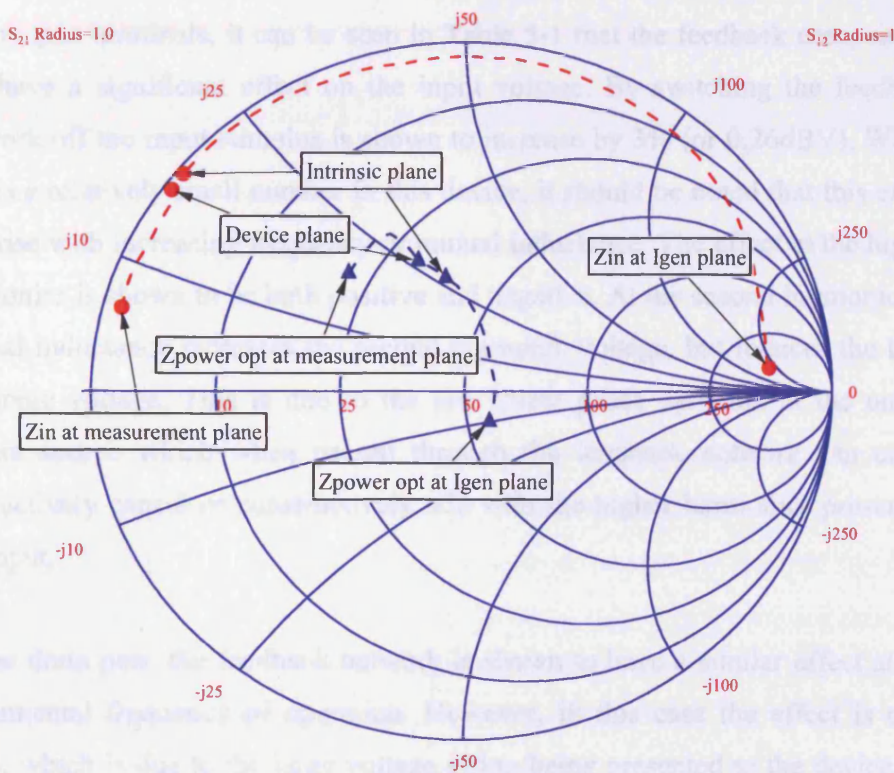Fig. 5-26 The impedance movement when de-embedding from the measurement plane to the I$_{gen}$ plane

5.2.3 Quantifying the effects of feedback in a real device

Using the derived de-embedding network, it is possible to quantify the effects of the feedback network in both a forward and reverse direction. This is done by simply enabling and disabling the feedback components in the network. In this

device it was found that the major form of feedback was caused by the 'on-device' mutual inductance. Using the waveforms shown earlier at the impedance for optimum power at 1dB compression, the effect of feedback in terms of the voltages are shown in Table 5-1.

Harmonic	Gate Voltage (mag(V))		Drain Voltage (mag(V))	
	Feedback On	Feedback Off	Feedback On	Feedback Off
F_0	4.08	4.20	23.85	23.92
$2F_0$	0.29	0.25	3.00	3.00
$3F_0$	0.02	0.04	1.71	1.70

Table 5-1 Summary of input and output voltages at the intrinsic plane with and without feedback

At the gate terminals, it can be seen in Table 5-1 that the feedback components can have a significant effect on the input voltage. By switching the feedback network off the input stimulus is shown to increase by 3% (or 0.26dBV). Whilst this is a relatively small number in this device, it should be noted that this effect will rise with increasing frequency or mutual inductance. The effect at the higher harmonics is shown to be both positive and negative. At the second harmonic the mutual inductance increases the second harmonic voltage, but reduces the third harmonic voltage. This is due to the non linear phase variation at the output current source which when passed through the feedback network can either destructively cancel or constructively add with the higher harmonics present at the input.

At the drain port, the feedback network is shown to have a similar effect at the fundamental frequency of operation. However, in this case the effect is only 0.3%, which is due to the large voltage swing being presented to the device. At the higher harmonics, the effect of the feedback network is shown to be negligible. This effectively means that the output load network can exclusively be used for load based investigations as the feedback effects in this case have been shown to be very small. At the input this is not the case because of the relative size of the two voltage components.

5.3 Uncertainty Analysis

As mentioned earlier in this chapter, one potential doubt in the effectiveness of the de-embedding is the uncertainty in the network and component values. This is investigated by varying the component values in the circuit by ±10%. This will produce a window of uncertainty in the de-embedding and provides a means of assessment as to how much further investigation is required for effective time-domain de-embedding.

The results are shown in Fig. 5-27 where the voltage waveforms at the drain and gate ports, shown to vary by a very small amount but the current waveforms exhibiting a more noticeable change. This demonstrates a low level of sensitivity to the series based de-embedding that affects the voltage waveform and a significant sensitivity of the current waveform to the drain and especially the gate charge generators. This is because the drain and gate charge generators are the most significant "shunt to ground" parallel component in this device and behaves in a non linear fashion. The increased reliance of an accurate charge model is more evident at the gate terminals due to the lack of a current generator at the gate port, which provides a well defined means of evaluation, i.e. $I_g = 0$ A. With the gate charge generator in its original state the gate current at the I_{gen} plane is always close to 0A with noise like variation, but with the ±10% variation the gate current shows periodic behaviour. At the drain terminal, the variation in drain charge is shown to have less of an overall impact on the drain current waveform at the I_{gen} plane. However, by further examining the waveforms, the sensitivity of the charge generators to the drain voltage can be seen, especially in the high current, low voltage region of the waveforms. This can be seen more clearly in the impedances at the I_{gen} plane as shown in Table 5-2, which shows a large variation in the reactive impedance component but little variation in the real impedance.
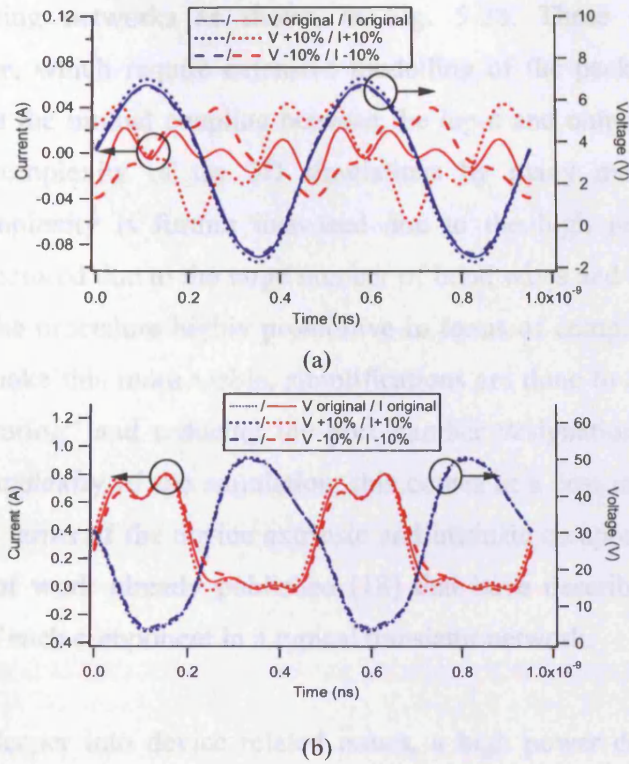
(a)

(b)

Fig. 5-27 (a) Gate current and voltage waveforms at the I_{gen} plane with a $\pm 10\%$ variation in the parasitic network (b) Drain current and voltage waveforms at the I_{gen} plane with a $\pm 10\%$ variation in the parasitic network

	-10%	Original	+10%
Z_{Igen}	$56.7 - 3.4j\ \Omega$	$57.0\text{-}10.3j\ \Omega$	$55.6 - 17.0j\ \Omega$

Table 5-2 Impedances at the I_{gen} plane with a $\pm 10\%$ variation in component values

5.4   Time-Domain De-embedding of a High Power Device

With the success in medium power time domain de-embedding, the procedure is now applied to a high power device, more suited to communications base station applications. In this case the measured waveforms of an 110W device supplied by Freescale Semiconductor Inc. measured at 2.1GHz are de-embedded to the I_{gen} plane. However, before de-embedding is applied to the measurements it is worth discussing the added complexity of de-embedding high power devices.

5.4.1   Potential issues with high power de-embedding

This first potential issue with high power de-embedding is the added complexity in modelling introduced by the inclusion of a large package, multiple die and

internal matching networks as shown in Fig. 5-28. These structures are physically large, which require extensive modelling of the package tab, bond wire arrays and the mutual coupling between the input and output ports, which increase the complexity of the 3D simulations by many magnitudes. The simulation complexity is further increased due to the high number of port designations, required due to the large number of bond wires and device fingers, which makes the procedure highly prohibitive in terms of computing resources and time. To make this more viable, simplifications are done to the simulation, such are "mirroring" and reducing the port number designations. Whilst this reduces the complexity of the simulation, this comes at a cost in accuracy and information. In terms of the device extrinsic and intrinsic components there is a large amount of work already published [18] that have described the scaling relationships of each component in a typical transistor network.

Now delving deeper into device related issues, a high power device typically consists of many multiple cells that are all fed in parallel along an input tab and then combined on the output tab of the package. This procedure introduces paths of different phase delays, thus presenting different impedances to the individual cells of each die at both the input and output terminals. The effect of this procedure is that the separate transistor cells are functioning out of phase and in different output and thermal states [40]. Another by product of this is the possibility of interaction between cells, which when combined with the effects outlined earlier could reduce the output power and operating efficiency of the entire device from what would be expected when linearly scaling. Whilst it is possible to model these networks with a reasonable amount of accuracy, it is hard to predict the viability of conducting these simulations due to potential convergence problems caused by the differing thermal and electrical states of operation.
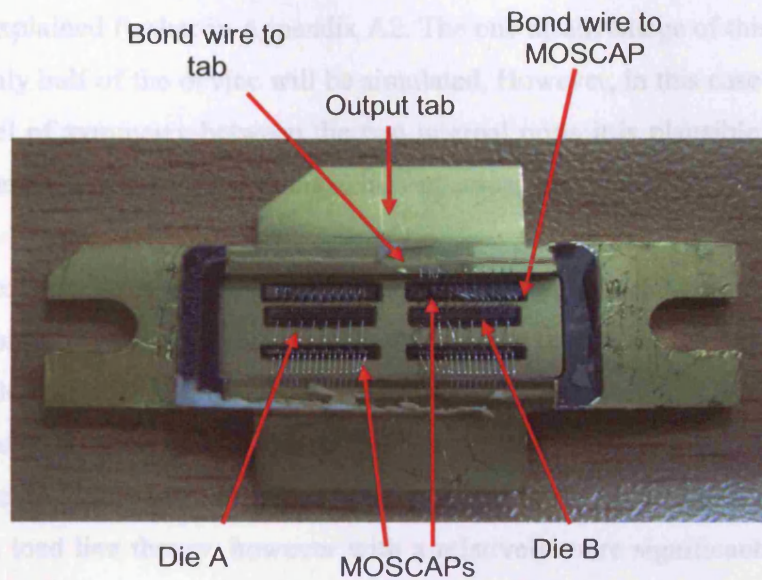
Fig. 5-28 - A photo outlining the components of a typical high power Si LDMOS device

Some other potential issues with de-embedding high power devices is the ability to measure the higher harmonic components. The stronger low pass filter properties of the high power device and package will effectively suppress the higher harmonics, making them difficult to measure. In practice the second and third harmonics are approximately 30-35dB below the fundamental, which is within the dynamic range of the measurement system. However, the fourth and fifth harmonics are usually lower than 45dB below the fundamental component and these readings could be affected by the noise inherent in the system. Whilst three harmonics describe a large proportion of the total output, it will be difficult to produce waveforms as informative as shown earlier in this chapter.

5.4.2 De-embedding a high power device

In this case the network was supplied by Freescale Semiconductor Inc. and describes the package tab, bond wires and the die in a simplified way, which will enable the viewing of waveforms at the I_{gen} plane across an entire die. The first stage was to negate the effects of the package tab and bond wires. The package tab was simulated as a three port structure, which can not be de-embedded using ADS^{TM}. To overcome this difficulty, the package tab was simplified to a two

port structure under the assumption that the two internal ports are symmetrical. This is explained further in Appendix A2. The one disadvantage of this approach is that only half of the device will be simulated. However, in this case due to the high level of symmetry between the two internal ports it is plausible to assume that the same performance is being achieved across the second die.

The waveforms were taken at the impedance for optimum power whilst at 1dB compression. As a first check of the de-embedding the impedances at each stage of the de-embedding process were recorded as shown in Table 5-3. The impedances at each plane are shown to be consistently low with a final impedance of 2.44+1.35j Ω which is close to the predicted 2 Ω power optimum based on load line theory, however with a relatively more significant imaginary impedance component. As a result the expected current and voltage waveforms will have a large overlap region.
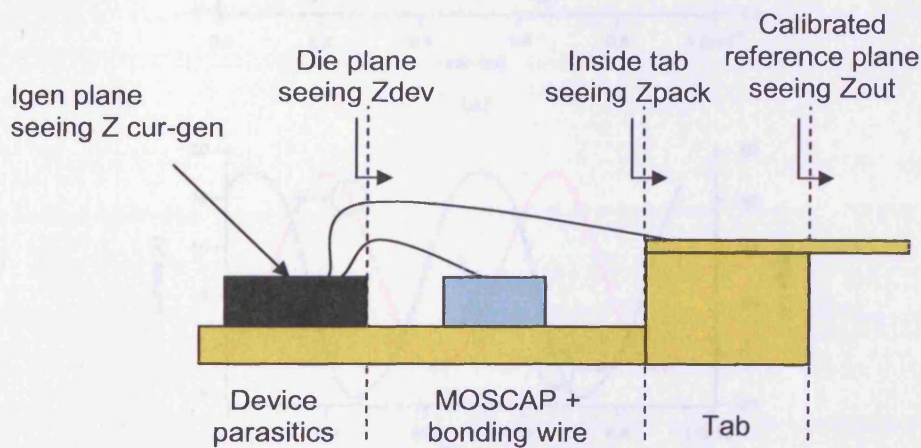

Fig. 5-29 Physical cross section of a high power device outlining the location of the internal reference planes

| Z_{Igen}	Z_{die}	Z_{pack}	Z_{out}
2.444 + 1.352j Ω	1.096 + 1.583j Ω	2.682 – 4.818j Ω	2.125 -4.098j Ω

Table 5-3 Impedances at the various internal reference planes

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The next step is to look at the measured and de-embedded current and voltage waveforms, which are shown in Fig. 5-30 and Fig. 5-31. The measured current and voltage waveforms at both the gate and drain ports exhibit sinusoidal behaviour which as mentioned earlier is due to the low pass filtering properties of the device and package. The measured voltage swing at the drain (Fig 5-31 (b)) is shown to swing as low as -17V and as high as 71V, which is clearly beyond a device's boundary of operation. This demonstrates the large amount of displacement voltage being generated in the device and package especially when compared to the medium power device shown earlier.
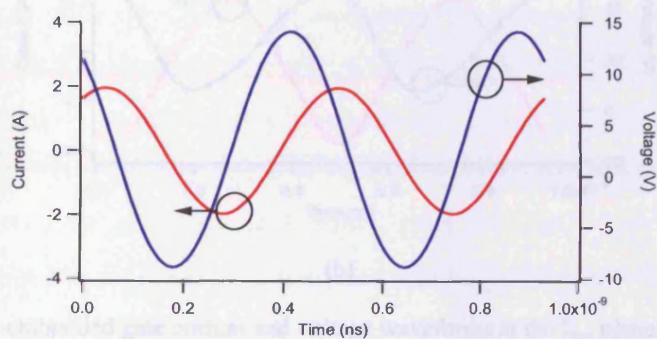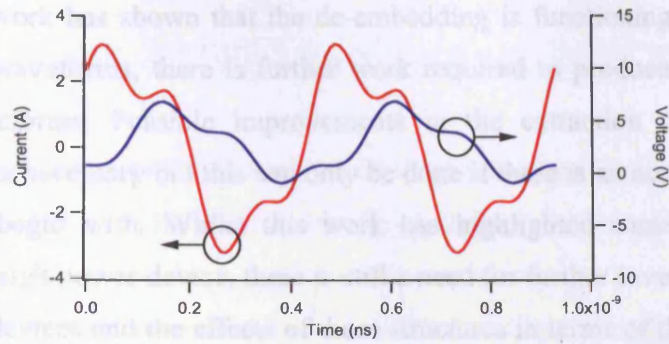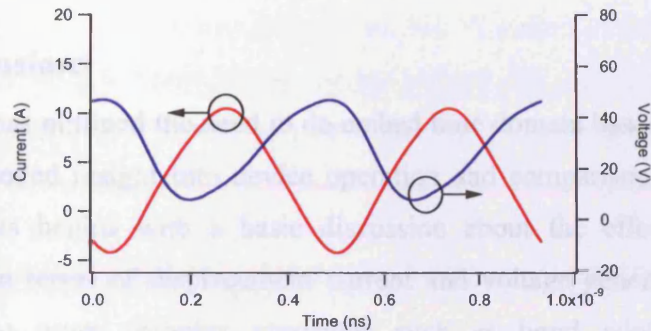

(a)
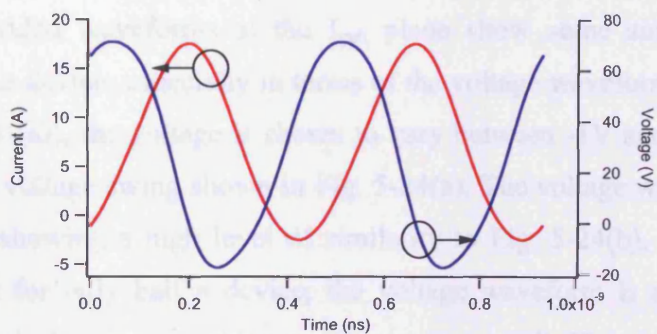
(b)

Fig. 5-30 (a) Measured gate current and voltage waveforms (b) measured drain current and voltage waveforms

56

(a)

(b)

Fig. 5-31 (a) De-embedded gate current and voltage waveforms at the I_{gen} plane (b) de-embedded drain current and voltage waveforms at the I_{gen} plane

The de-embedded waveforms at the I_{gen} plane show some similarity to the medium power device, especially in terms of the voltage waveforms. At the gate port (Fig 5-31 (a)), the voltage is shown to vary between -1V and 7V, which is similar to the voltage swing shown in Fig. 5-24(a). The voltage waveform at the drain is also showing a high level of similarity to Fig. 5-24(b), whilst the de-embedding is for only half a device, the voltage waveform is assumed to be constant at both dies and provides an encouraging result. However, the current waveform is not showing the same properties as expected. The gate current is shown to be harmonically rich and to vary between -4 to 4A which shows a large margin of error when compared to the medium power device. At the drain port the current swing is sinusoidal in shape with no half rectification. However, the amplitude is approximately what would be expected for half a device, which suggests that the de-embedding has been applied correctly at the fundamental frequency of operation.

Whilst this work has shown that the de-embedding is functioning correctly for the voltage waveforms, there is further work required to produce the expected current waveforms. Possible improvements in the extraction of the charge generators are necessary but this can only be done if there is an accurate package network to begin with. Whilst this work has highlighted some encouraging results for a high power device, there is still a need for further investigations into high power devices and the effects of these structures in terms of the current and voltage waveforms.

5.5 Conclusions

This chapter has outlined the need to de-embed time domain based measurement data for improved insight into device operation and comparison with classical literature. This begins with a basic discussion about the effects of lumped components in terms of displacement current and voltage generation and then proceeds onto more complex structures such as bond wires and device manifolds. Once this was completed the de-embedding of measured time-domain waveforms is successfully demonstrated on a medium power device with very little sensitivity on the voltage waveform but more sensitivity on the current waveforms. Finally, the same procedure was applied to a high power device and found to be successful in terms of the voltage waveforms but the current waveforms were not what was expected. Further improvement in high power de-embedding could be achieved by increasing the level of depth in the passive and active modelling process, in order to better describe the interactions between the various elements of the entire transistor.

6   The Affect of System Impedance on High Power Measurements

High power device measurements above 20 W in output power typically involve large current and voltage swings, which in general produce optimum load impedances for power at the I_{gen} plane much below 20 Ω when using load line theory [3]. As the devices increase in output power in particular output drain current the optimum load impedance for power can drop dramatically down to sub 1 Ω impedances for devices greater than 100 W output power. However, as devices are moving towards higher output powers the one constant variable when characterising high power devices is the characteristic system impedance, which is conventionally 50 Ω.

The characteristic impedance of 50 Ω was standardised due to it being the best compromise between cable loss and peak power handling in a co-axial cable of relative dielectric one and is described in more detail in [41]. As a consequence many measurement systems have been built with a 50 Ω system impedance for a variety of applications. In this case the measurement system being used is the high power measurement setup developed at Cardiff University [17], which allows for the measurement of time-domain waveforms. The system was initially developed using low power on wafer devices, with small current levels, typically leading to optimum impedances well above 100 Ω. In this case the system impedance is shown to have very little effect on the performance of low power devices [16]. This is because the 50 Ω system impedance at the higher harmonics is below the fundamental and thus, limiting the generation of higher harmonic voltage components relative to the fundamental. This enables the device to function better in classical modes of operation such as class B etc. With high power devices, the higher harmonic impedances are now above the optimum fundamental impedance for power, which is the opposite to what was occurring before hand. In this case the higher harmonic impedances generate unwanted higher harmonic voltage components due to Ohm's Law, that can significantly alter the waveforms at the measurement plane and in addition affect the

fundamental performance of the device. The end result is the synthesis of waveforms that are often different to what is presented in literature.

In reality, high power devices are housed in packages and contain significant parasitic effects that have been shown to change the waveforms. As shown in Chapter 5, these parasitic components can drastically transform the impedance at the measurement plane and present complex impedances at the I_{gen} plane. These complex impedances now not only affect the magnitude of the higher harmonic voltages but also the phase, which can distort the shape of the waveforms even further.

There has been some work [42, 20] presented using broadband impedance transformers that transforms the 50 Ω system impedance to 7 Ω as presented in [20]. However, the primary purpose for the work was to ease the requirements for fundamental load pull in both passive and active load pull measurement systems. This in theory will cancel out the effects of the higher harmonics but in practice it becomes prohibitive to construct very low impedance transformers due to the large transmission line widths and possible discontinuities when connecting to a device. Another method of limiting the effects of higher harmonics is to use harmonic load pull. This will allow the user to set short circuit impedances at the higher harmonics to cancel out the effects of the higher harmonics. However, in the case of both passive and active load pull systems harmonic load pull is both costly, complicated and in the case of active load pull, time consuming.

This chapter first looks into a practical example that demonstrates the affect of the higher harmonic impedances. After that the affect of the higher harmonic impedances is analyzed more theoretically based on the waveforms at the drain port of the device, first by comparing the scenarios, a low power device and a high power device. This is assumed using a perfect, 50 Ω characteristic system impedance and then applies some of the possible solutions to an ideal high power device. Then the work is expanded into looking at the waveforms of a 20

W LDMOS device and applying the de-embedding knowledge learnt beforehand to visually quantify this effect. After this, the affect of complex higher harmonic impedances are calculated and analyzed in terms of the current and voltage waveforms. Then the theory is applied to a 5 W Si LDMOS device as a means of confirmation.

6.1   A High Power Device Measurement in Two Different Impedance Environments

To help clarify the issue, a practical experiment is conducted where a high power Gallium Nitride (GaN) device is measured in two different impedance environments of 50 Ω and 10 Ω. The device was biased in class AB and at a drain voltage of 16V using the high power measurement system [17] at a frequency of 2.1 GHz. This was achieved through the use of broadband impedance transformers [20]. The impedance at the fundamental was set for maximum output power whilst the higher harmonic impedances were kept constant. Once this was achieved a power sweep was conducted allowing for a comparison of the performance in terms of output power, gain efficiency and the output current and voltage waveforms.

To begin with the device was measured in a 10 Ω impedance environment and the results are shown in Fig. 6-1. The device is shown to have flat gain at low power and a peak drain efficiency of 63 % whilst delivering 42.3 dBm of output power, which is expected for a device biased in class AB and is in agreement with the expected output power based on load line analysis [3]. The current and voltage waveforms at the measurement plane are both sinusoidal and clean of any higher harmonic components. The optimum impedance for maximum output power was found to be 6.8 − 11j Ω.
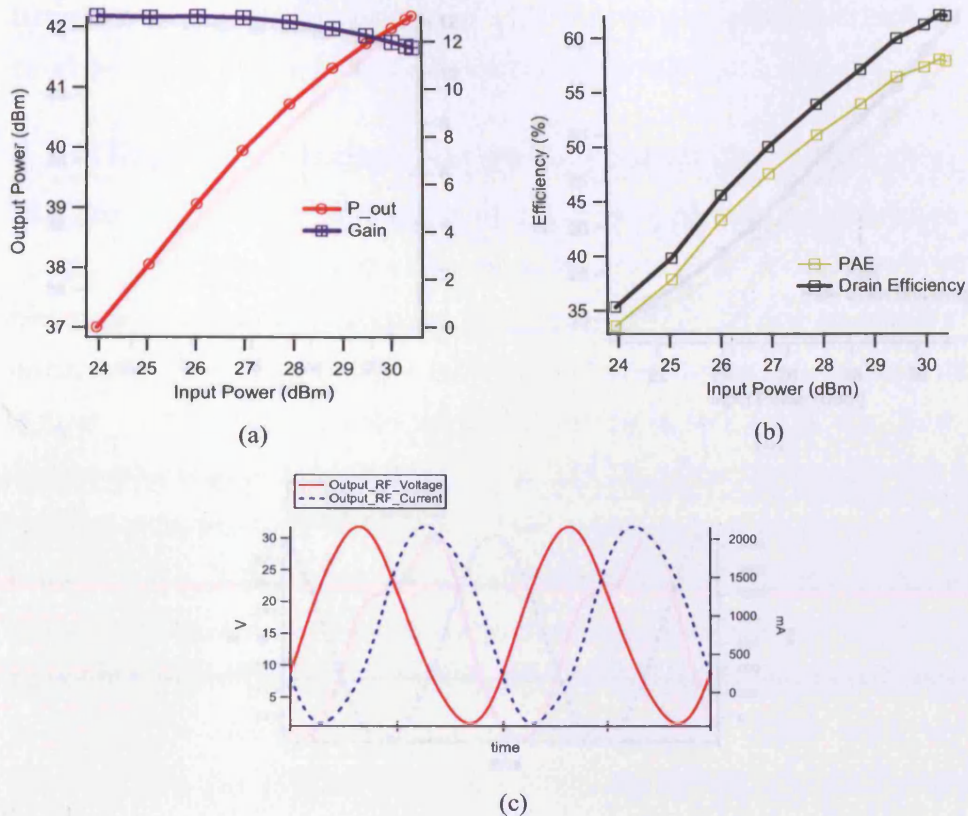
(a)

(b)

(c)

Fig. 6-1 (a) Output power and gain profile of a high power GaN device measured in 10 Ω with input power (b) PAE and drain efficiency of a high power GaN device measured in 10 Ω with input power (c) Current and voltage waveforms at the measurement plane at 1dB compression in output power

The same device was then measured in a 50 Ω environment and the results are shown in Fig. 6-2. The peak output power is found to be 42.3 dBm, which is the same as before but the gain and efficiency profiles are distinctly different than in a 10 Ω measurement environment. The gain is shown to compress from the lowest power in the sweep and the peak drain efficiency is found to be 53%, which is 10% lower than when measured in a 10 Ω impedance environment. Such a large change in drain efficiency can have a negative impact on the device, which in this case could be thermally damaging. The current waveform is similar to before but the voltage waveform is now showing an increase in higher harmonic content. The optimum impedance for power has now changed to 6 – 6.4j Ω.
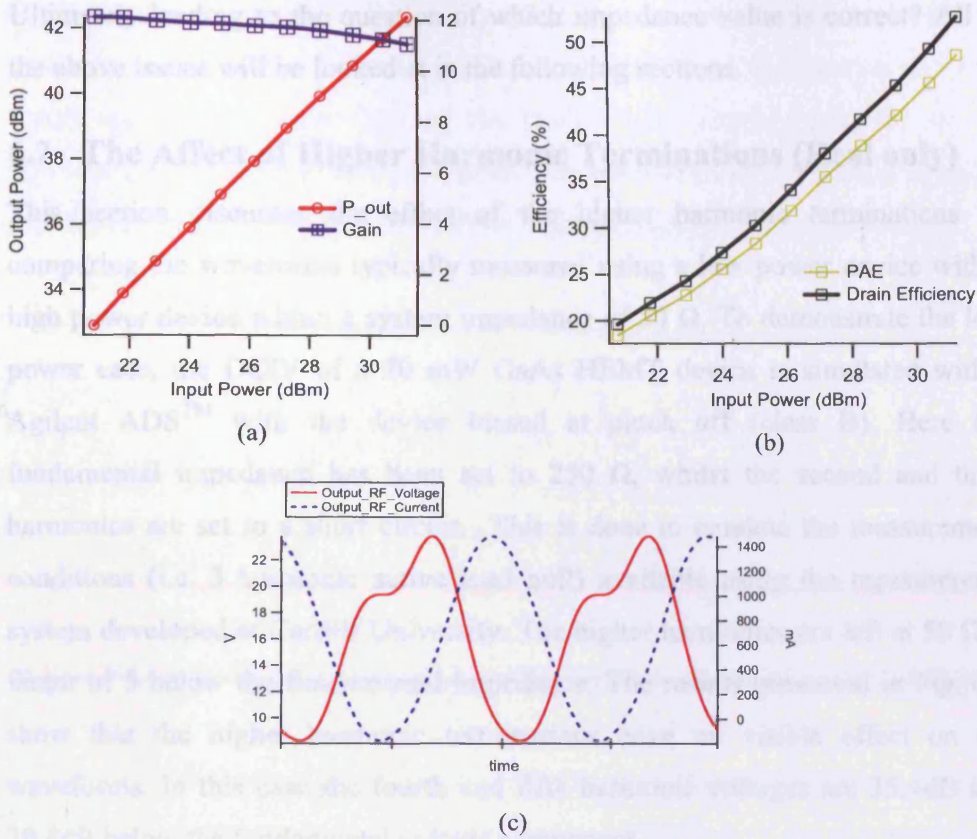
(a)

(b)

(c)

Fig. 6-2 (a) Output power and gain profile of a high power GaN device measured in 50 Ω with input power (b) PAE and drain efficiency of a high power GaN device measured in 50 Ω with input power (c) Current and voltage waveforms at the measurement plane at 1dB compression in output power

From the two sets of results it is clear to see that the higher harmonic impedances can affect the performance of a device. In this case the drain efficiency of the device was found to be severely affected with a 10% difference in performance between the two impedance environments. This makes it critical to account for the affects of the higher harmonic impedances to ensure accurate and "fair" characterisation of high power devices.

In addition to that the voltage waveforms at the drain port were shown to be different because of the higher harmonic components that are generated by the higher system impedance, which could cause the drop in drain efficiency observed in the 50 Ω measurements. Another interesting observation is that the optimum impedance for power was shown to be different in both cases.

Ultimately leading to the question of which impedance value is correct? All of the above issues will be looked at in the following sections.

6.2   The Affect of Higher Harmonic Terminations (Real only)

This section discusses the effect of the higher harmonic terminations by comparing the waveforms typically measured using a low power device with a high power device within a system impedance of 50 Ω. To demonstrate the low power case, the DCIV of a 70 mW GaAs HEMT device is simulated within Agilent ADS^{TM} with the device biased at pinch off (class B). Here the fundamental impedance has been set to 250 Ω, whilst the second and third harmonics are set to a short circuit. This is done to emulate the measurement conditions (i.e. 3 harmonic active load pull) available using the measurement system developed at Cardiff University. The higher harmonics are left at 50 Ω, a factor of 5 below the fundamental impedance. The results presented in Fig. 6-3 show that the higher harmonic terminations have no visible effect on the waveforms. In this case the fourth and fifth harmonic voltages are 35.4dB and 39.4dB below the fundamental voltage component.
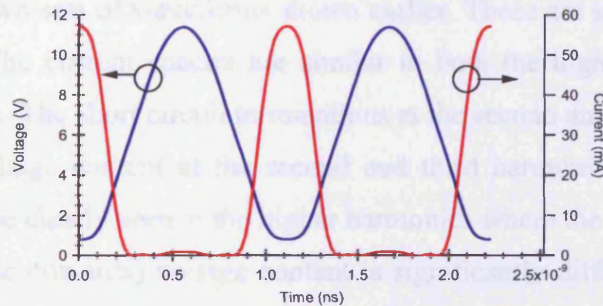

Fig. 6-3 Class B waveforms for the low power case with the higher harmonics 1:5 times lower than the fundamental, i.e. $Z_{fund} = 250\ \Omega$ and $Z_{4f0,\ 5f0..} = 50\Omega$

Based on DC-IV data, the 20 W device has an optimum impedance of 11 Ω. Using the DC-IV data as the basis of a model, a similar simulation was conducted with the device biased in class B with the same harmonic impedances presented to the on-wafer device. It should be noted that this time the higher harmonic terminations are now a factor of 5 above the fundamental impedance. Fig. 6-4 shows the voltage waveform is no longer sinusoidal, due to the presence

of large amounts of higher harmonic voltage content consisting of both odd and even components. The fourth and fifth harmonic voltage components are now 7.8dB and 19.6dB below that of the fundamental. Despite this, the device provides 21W of output power at a drain efficiency of 61.8%. It should be noted that this effect on the waveforms will be further magnified for larger devices.
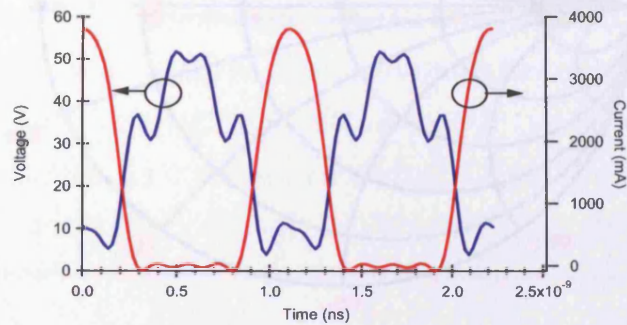

Fig. 6-4 Class B waveforms for the high power case with the higher harmonics 5:1 times higher than the fundamental, i.e. $Z_{fund} = 11\ \Omega$ and $Z_{4f0,\ 5f0\ ..} = 50\Omega$

For further clarification of the impedances being presented in the two cases, a Smith chart of the low and high power device impedances at the fundamental is plotted in Fig. 6-5. The affect of these impedances is signified in the spectral content of the two sets of waveforms shown earlier. These are shown in Fig. 6-6 and Fig. 6-7. The current spectra are similar in both the high power and low power scenarios. The short circuit terminations at the second and third harmonics remove any voltage content at the second and third harmonics. However, the difference can be clearly seen at the higher harmonics where the higher harmonic (fourth harmonic onwards) voltage content is significantly different in the high power simulation.
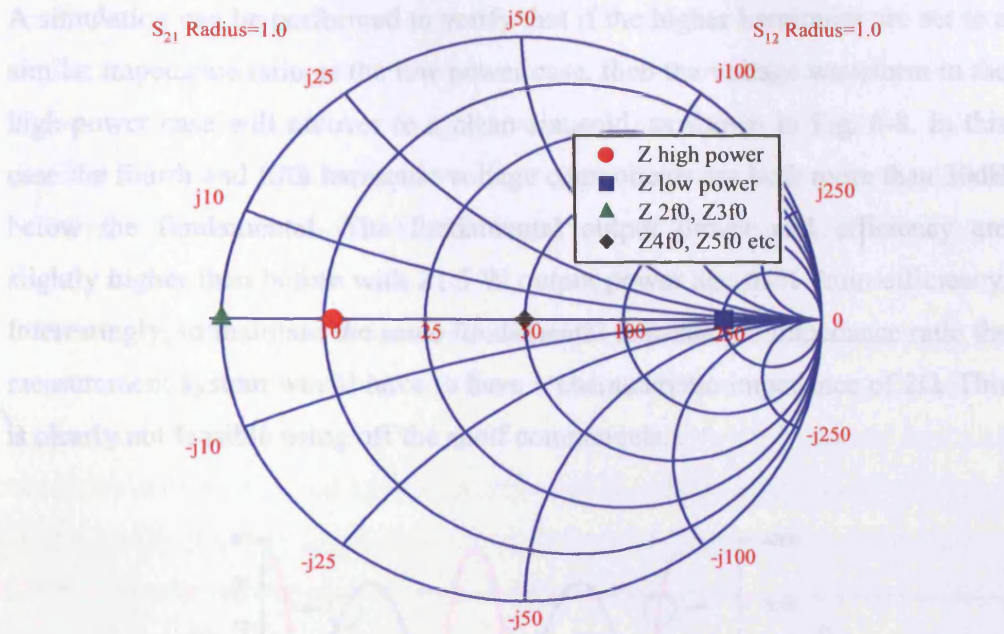
Fig. 6-5 – Smith chart showing the impedances being presented to the low and high power devices at the fundamental and the higher harmonics set by the measurement system
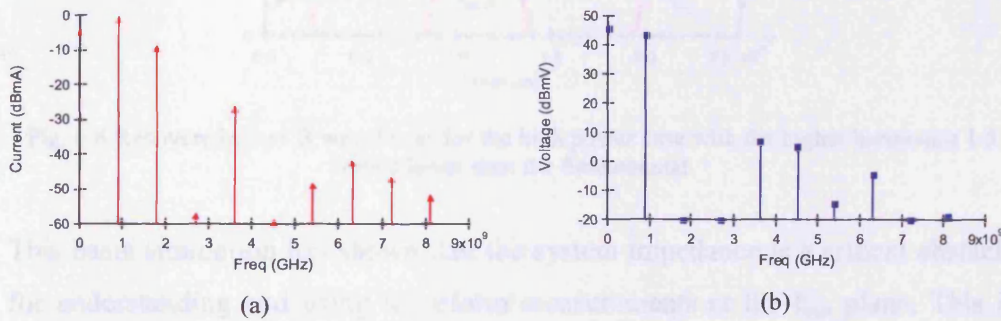

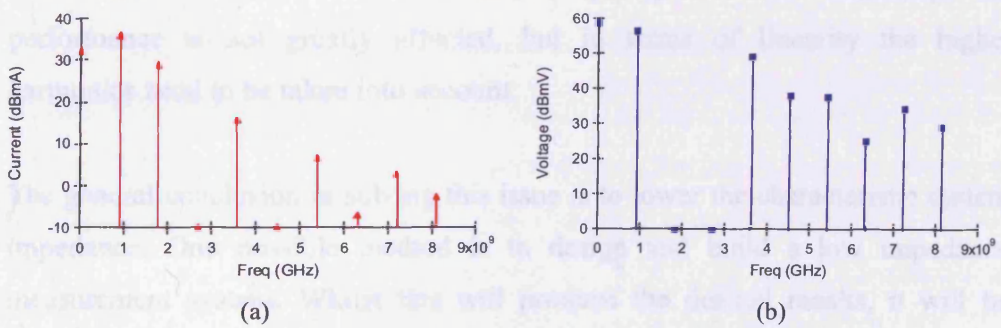Fig. 6-6 (a) Current spectrum of a low power device (b) Voltage spectrum of a low power device

Fig. 6-7 (a) Current spectrum of a high power device (b) Voltage spectrum of a high power device

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A simulation can be performed to verify that if the higher harmonics are set to a similar impedance ratio as the low power case, then the voltage waveform in the high-power case will recover to a clean sinusoid, as shown in Fig. 6-8. In this case the fourth and fifth harmonic voltage components are both more than 30dB below the fundamental. The fundamental output power and efficiency are slightly higher than before with 21.5 W output power and 63% drain efficiency. Interestingly, to maintain the same fundamental to harmonic impedance ratio the measurement system would have to have a characteristic impedance of 2Ω. This is clearly not feasible using off the shelf components.
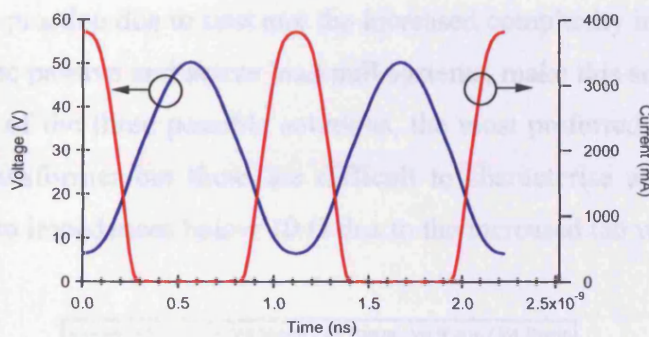

Fig. 6-8 Recovered Class B waveforms for the high power case with the higher harmonics 1:5 times lower than the fundamental

This basic simulation has shown that the system impedance is a critical obstacle for understanding and using waveform measurements at the I_{gen} plane. This is attributed to the ratio of impedances between the fundamental and the higher harmonics. In terms of fundamental output power and efficiency, the performance is not greatly affected, but in terms of linearity the higher harmonics need to be taken into account.

The general conclusion in solving this issue is to lower the characteristic system impedance. One possible method is to design and build a low impedance measurement system. Whilst this will produce the desired results, it will be difficult to source components such as couplers, dc bias tees with characteristic impedances that are not 50 Ω and will instead require special custom made components that could be very costly. The other alternative is to construct a

broadband impedance transformer that will transform the 50 Ω system impedance to a lower (in this particular case) impedance. Most broadband impedance transformers have a high pass characteristic [43, 44] and are able to provide the low impedances shown to be required to a number of higher harmonics. However, broadband impedance transformers can have a significant impedance variation in the non-operational region [43], which can lead to the device seeing impedances that could lead to potential device instabilities or possible oscillation. Another possibility is to extend load pull capability to the higher harmonics. The results in Fig. 6-9 demonstrate that 9 harmonic load pull capability will be required to sufficiently quell the effect the effect of the higher harmonics. In practice due to cost and the increased complexity in implementing multi-harmonic passive and active load pull systems, make this solution difficult to apply. Out of the three possible solutions, the most preferred is a broadband impedance transformer but these are difficult to characterise and verify when transforming to impedances below 10 Ω due to the increased tab width.
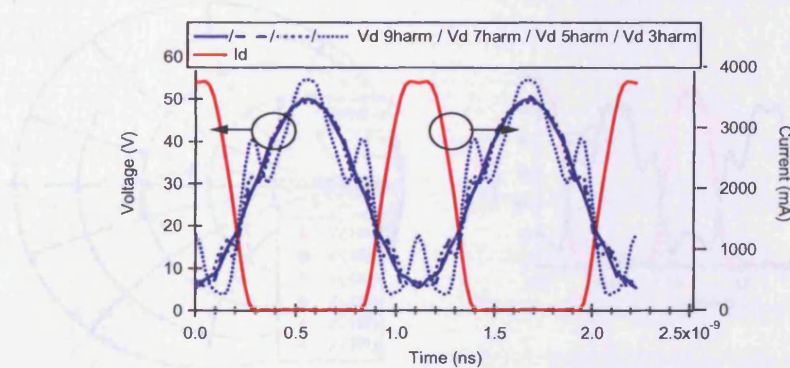

Fig. 6-9 Voltage waveforms with increasing harmonic load pull capability

However, high power device measurements are not taken at the device plane but after a packaging network. This complicates the impedances being presented at the device plane. The uncontrolled higher harmonic impedances will now consist of both resistive and reactive components due to the transformation process in the packaging. The result of this is a more complex voltage waveform that now varies in both phase and magnitude at the uncontrolled higher harmonics.

The same simulation is now extended to include a simplified device and package network typically used for a 20W device as shown in Fig. 6-10 [45]. The fundamental, second and third harmonic impedances at the outside of the device are set such that the intrinsic device sees the optimum impedance at the fundamental and short circuits at the second and third harmonics. The higher harmonics are set to 50Ω at the measurement plane. The resultant impedances presented at the intrinsic plane and the waveforms are shown in Fig. 6-11.
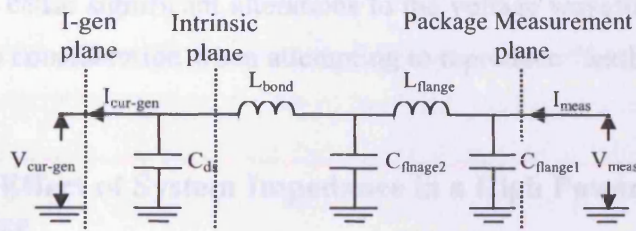

Fig. 6-10 Simplified device and package network
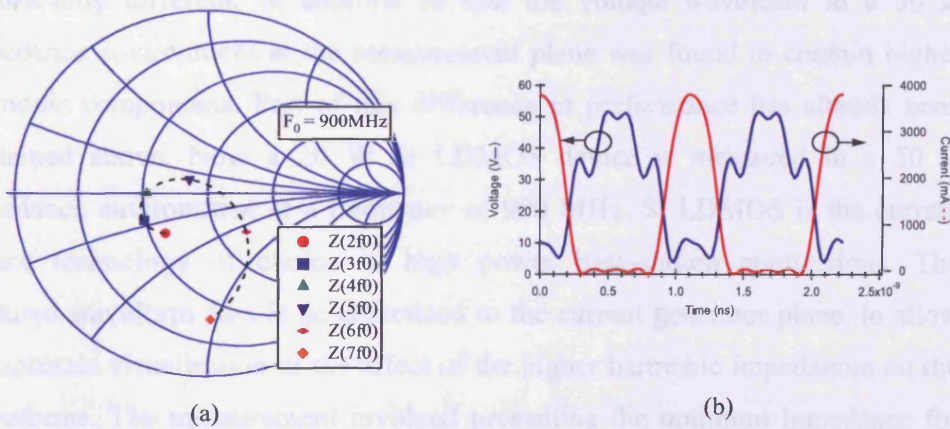
Fig. 6-11 (a)Impedances presented at the intrinsic plane when 50 Ω is presented at the measurement plane (b) Current and voltage waveforms at the intrinsic plane

The voltage waveform in Fig. 6-11(b) is shown to be similar to the waveforms shown in Fig. 6-4, but with some change in the magnitude and phase of the higher harmonics. In this case the harmonic distortion caused by the fourth and fifth harmonics is 12.2dB and 17.2dB below the fundamental voltage. There is also an increase in the sixth harmonic voltage component that is 15.8dB below the fundamental voltage component. The impedance presented at the fourth

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harmonic is shown to be approximately 28 Ω which is almost a factor of two below the system impedance and is predominantly a real only impedance. This explains the 4.4dB reduction in the fourth harmonic voltage. The impedance presented at the fifth harmonic is shown to decrease slightly but is still relatively close to 50 Ω which has interestingly resulted in an increase in fifth harmonic voltage. At the sixth harmonic the impedance is shown to be above 50 Ω, which produces the expected increase in voltage swing. This result shows that it is important to emphasize that the variation in impedance caused by the package network can cause significant alterations to the voltage waveforms and needs to be taken into consideration when attempting to reproduce "textbook" high power waveforms.

6.2.1 The Effect of System Impedance in a High Power Si LDMOS Device

Earlier in this chapter a high power GaN device was characterised in two different impedance environments and the performance was found to be significantly different. In addition to that the voltage waveform in a 50 Ω impedance environment at the measurement plane was found to contain higher harmonic components. Part of this difference in performance has already been explained above. Now a 20 W Si LDMOS device is measured in a 50 Ω impedance environment at a frequency of 900 MHz. Si LDMOS is the current device technology of choice in high power base-station applications. The captured waveform data is de-embedded to the current generator plane, to allow for accurate visualisation of the affect of the higher harmonic impedances on the waveforms. The measurement involved presenting the optimum impedance for power at the fundamental and short circuits at the second and third harmonics at the I_{gen} plane, using the de-embedding network shown in Fig. 6-10. The waveforms are shown in Fig. 6-12.
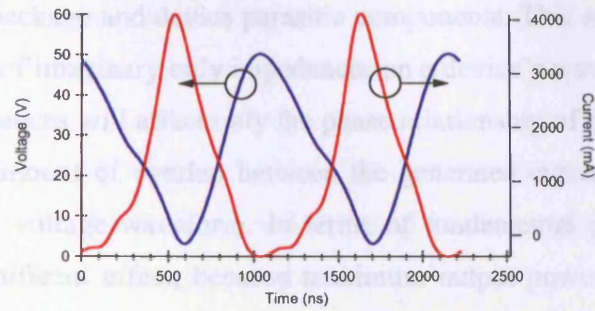
Fig. 6-12 The de-embedded current and voltage waveforms at the I_{gen} plane

The voltage waveform in Fig. 6-12 is near sinusoidal and is in good agreement with the DC-IV boundaries. There is some harmonic content in the voltage waveform, consisting of second (due to an imperfect short) and fourth harmonic voltage components which create the slight distortion in the waveform. The current waveform is shown to be half rectified and due to the distortion in the voltage waveform it too contains minor artefacts.

In this case the affect of the higher harmonics has been limited due to the large device output capacitance, which is approximately 10pF. This effectively provides an immediate short circuit to the current generator at high frequencies, as a result cancelling the effects of the higher harmonic terminations. As the device size and output power increases, the dampening effect of the large drain capacitance can come into affect at the lower harmonics, i.e. second and third. Thereby producing waveforms readily presented in literature for classical modes of operation. In GaN devices the device output capacitance is usually much lower, which consequently allows for the generation of unwanted higher harmonic voltage components as shown earlier. In this case, more consideration of the correct measurement impedance environment is required together with a thorough understanding of the effect of the complex higher harmonic impedances typically being presented at the I_{gen} plane.

6.3   The Affect of the Higher Harmonics (Reactive only)

The previous section focussed on analyzing the affect of real only impedances on a device's waveforms. In reality as discussed earlier, the current generator will be exposed to complex impedances due to the impedance transformations

caused by the package and device parasitic components. This section now looks into the effects of imaginary only impedances on a device's waveforms. Lossless complex impedances will affect only the phase relationship of the waveforms, in particular the amount of overlap between the generated current waveform and the synthesised voltage waveform. In terms of fundamental performance, this can have a significant effect, because maximum output power in conventional modes of operations can only occur when the phase offset φ of the product between the current and voltage is equal to zero [31]. This is shown below, where the power is expected to roll off as the phase offset increases. This carries on until φ = 90° when no power will be delivered to the load.

$$P_{OUT} = \frac{1}{T}\int_0^T V_{DS}(\tau)I_{DS}(\tau)d\tau = \frac{\widetilde{V}_{DS}\widetilde{I}_{DS}}{T}\int_0^T \cos\left(2\pi\frac{\tau}{T}\right)\cos\left(2\pi\frac{\tau}{T}+\varphi\right)d\tau = \frac{\widetilde{V}_{DS}\widetilde{I}_{DS}}{2}\cos(\varphi)$$

$$(6\text{-}1)$$

where,

$$V_{DS}(t) = \widetilde{V}_{DS}\cos\left(2\pi\frac{t}{T}\right)$$

$$(6\text{-}2)$$

$$I_{DS}(t) = \widetilde{I}_{DS}\cos\left(2\pi\frac{t}{T}+\varphi\right)$$

$$(6\text{-}3)$$

However, the equation given in (6-1) represents the performance at just the fundamental. What hasn't been considered before is the role of the higher harmonics and what affect they have on the performance of the device at the fundamental. It is important to note that the affect of these complex impedances will be applicable to devices of all sizes. The one difference between high and low power devices, could be the extremity of this effect and this will be discussed later.

6.3.1 Simulation

To best illustrate the effect of complex higher harmonic impedances, a load pull simulation was done of an ideal device biased in class B with no parasitic components. The performance will be assessed in terms of output power only. This is to avoid the added complication of reactive based efficiency enhancement

techniques such as class E [11]. As a point of reference a load pull simulation of an ideal device biased in class B (all higher harmonics short circuited) was conducted. The load pull contours (in red) are shown in Fig. 6-13(a). The optimum impedance for power is shown to be 71 Ω with the contours centred around the real axis. The optimum real only impedance and the elliptical shapes of the load pull contours are in good agreement with theory [3, 46]. Another load pull simulation was conducted but with a different fixed impedance at the second harmonic (higher harmonics still set to short circuit). The resultant contours (in black) shown in Fig. 6-13(a) are now centred off the real axis at 71 + 71j Ω with the contour shapes no longer elliptical and the spacing between power levels no longer uniform. The reason for this is due to the presence of a reactive second harmonic impedance of 0 − 83j Ω (all other higher harmonics are short circuited), resulting in the generation of a "reactive" second harmonic voltage component. This new voltage component significantly alters the voltage waveform and it's interaction with the current, but the output performance of the device is the same, i.e. identical output power (37.15dBm) and drain efficiency (75.2%). The current and voltage waveforms for both cases are shown in Fig. 6-13(b).

In both cases the current waveform is half rectified and identical. This is because the current waveform is a function of bias and assumed to be independent of the load impedance. Meanwhile the voltage waveform is a function of load impedance at all of the harmonics and is shown to be vastly different in both cases. The ideal class B voltage waveform is sinusoidal as expected due to the short circuits being applied at the higher harmonics. However, with the introduction of a reactive second harmonic termination, the voltage waveform has become half rectified and is shown to increase in amplitude by a factor of the square root of two producing current and voltage waveforms that are similar to a class J mode of operation [1]. The reactive fundamental termination introduces an overlapping region between the current and voltage waveforms resulting in the loss of power and efficiency. However, the combination of a larger voltage swing at the fundamental and reactive impedance offset (which in this case is

cos(45°) = 1/√2), produces a cancelling effect that results in the same output power and drain efficiency as observed in a conventional class B mode of operation.
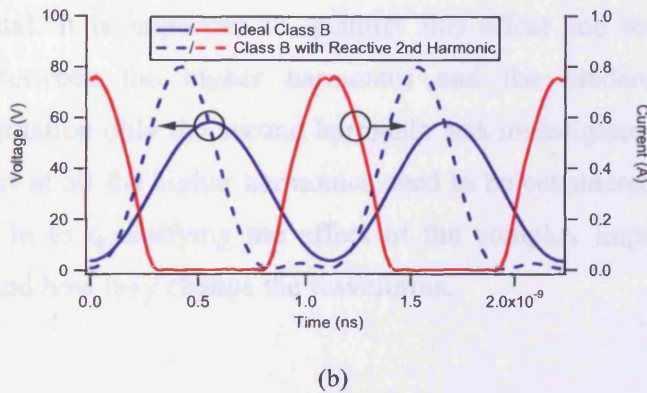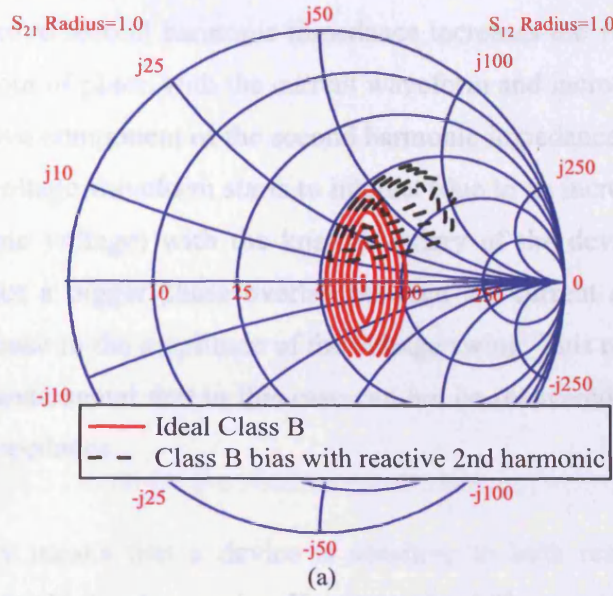

(a)

(b)

Fig. 6-13 (a) Load pull contours for output power of an ideal device biased in class B with different impedance terminations at the 2nd harmonic (0.25dBm step size) (b) Current and voltage waveforms at peak output power of an ideal device biased in class B with different impedance terminations at the 2nd harmonic

As a further check, fundamental load pull sweeps were conducted with different second harmonic impedances and the higher harmonic impedances all set to short circuit. Maximum output power can be maintained over a range of second harmonic impedances as shown in Fig. 6-14(a). However, optimum power

performance is only achieved within a certain range of second harmonic impedances. This range is given by $\pm 1.16 R_{opt}$ (normalized) where R_{opt} is the optimum impedance for power at the fundamental and is highlighted in Fig. 6-14(b). By closer analysis of the waveforms in Fig. 6-14(c), it becomes clear in that as the reactive second harmonic impedance increases the voltage waveform starts to come out of phase with the current waveform and increase in amplitude. Once the reactive component of the second harmonic impedance increases above $1.154 R_{opt}$ the voltage waveform starts to interact (due to an increasing amount of second harmonic voltage) with the knee boundary of the device. This in turn starts to produce a bigger phase overlap between the current and voltage with little extra increase in the amplitude of the voltage swing. This results in a loss of power at the fundamental that in this case can not be recovered by adjusting the fundamental impedance.

This effectively means that a device is sensitive to both real and imaginary impedances at the higher harmonics. However, the difference in this case is that the performance of the device can be recovered by changing the impedance at the fundamental. It is important to quantify this effect and to determine the relationship between the higher harmonics and the fundamental. In this controlled simulation only the second harmonic was investigated but in practice the impedances at all the higher harmonics need to be considered. The next sub section looks in to quantifying the affect of the complex impedances on the fundamental and how they change the waveforms.
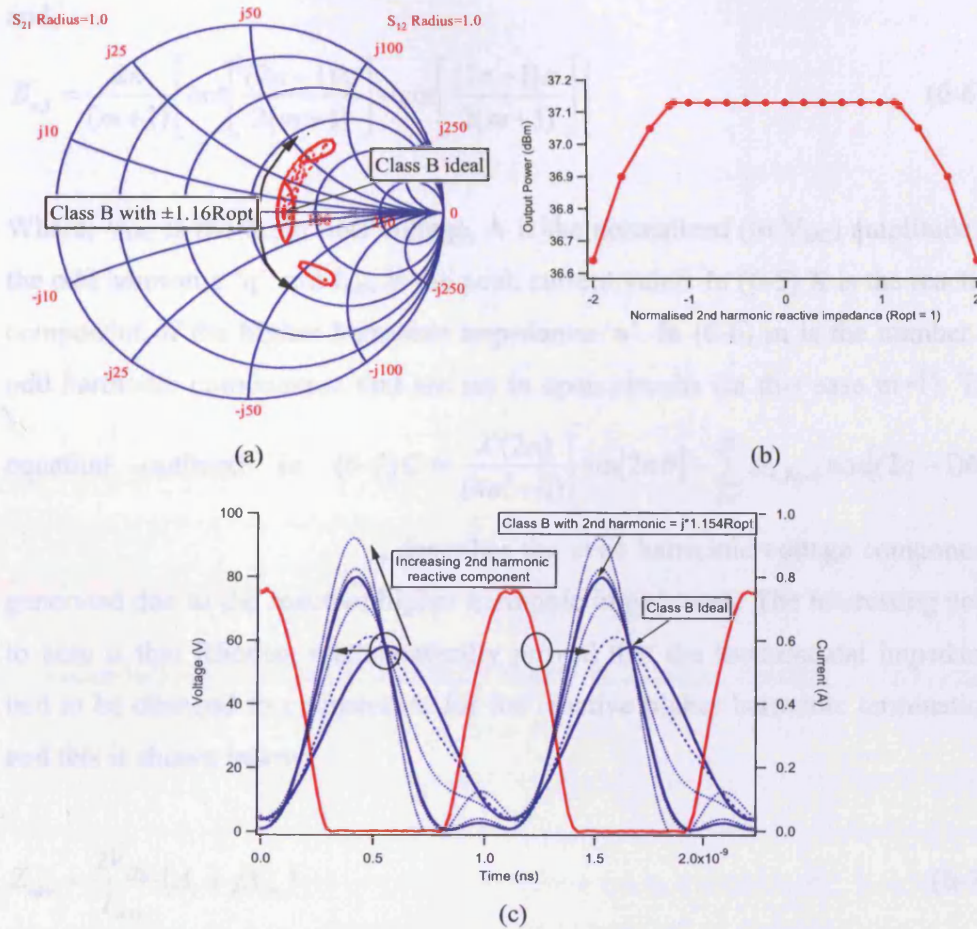
(a)

(b)

(c)

Fig. 6-14 (a) Smith chart showing the movement of the maximum output power contours with varying 2nd harmonic impedance (b) Maximum output power with varying 2nd harmonic impedance (c) Current and voltage waveforms with varying 2nd harmonic impedance

6.3.2 Theory

The theory used to explain this change in optimum impedance has been explained by Rhodes [47]. In the paper, Rhodes has derived an expression for an ideal device biased in class B (even harmonics only), that calculates the voltage as a function of the reactive higher harmonic terminations. This expression is given by

$$\frac{V_{ds}}{V_{DC}} = 1 - \sum_{q=1}^{m} A_{2q-1} \sin[(2q-1)\theta] - \frac{I_{max}}{\pi V_{DC}} \sum_{n=m}^{\infty} C \qquad (6\text{-}4)$$

where,

$$C = \frac{X(2n)}{(4n^2-1)}\left[\sin[2n\theta] - \sum_{q=1}^{m} B_{n,2q-1} \cos[(2q-1)\theta] \right] \qquad (6\text{-}5)$$

and,

$$B_{n,1} = \frac{2n}{(m+1)}\left[\cot\left[\frac{(2n-1)\pi}{2(m+1)}\right] - \cot\left[\frac{(2n+1)\pi}{2(m+1)}\right]\right]$$ (6-6)

Where, V_{DC} is the drain bias voltage, A is the normalized (to V_{DC}) amplitude of the odd harmonic 'q' and I_{max} is the peak current value. In (6-5) X is the reactive component of the higher harmonic impedance 'n'. In (6-6) m is the number of odd harmonic components that are set to open circuits (in this case m=1). The

equation   outlined   in   (6-5) $C = \dfrac{X(2n)}{(4n^2-1)}\left[\sin[2n\theta] - \sum_{q=1}^{m} B_{n,2q-1}\cos[(2q-1)\theta]\right]$

, describes the even harmonic voltage components generated due to the reactive higher harmonic impedances. The interesting point to note is that Rhodes, mathematically proved that the fundamental impedance had to be changed to compensate for the reactive higher harmonic terminations and this is shown below;

$$Z_{new} = \frac{2V_{DC}}{I_{max}}\left(A_1 + jX_m\right)$$ (6-7)

$$X_m = \frac{I_{max}}{\pi V_{DC}}\sum_{n=m}^{\infty}\frac{X(2n)}{(4n^2-1)}B_{n,m}$$ (6-8)

Where X_m is the total reactive offset produced by the higher harmonics, which is a function of the reactively terminated even harmonic voltage waveform. Using these expressions and conditions defined by the simulation, the linear current and voltage waveforms can be calculated together with the optimum impedance as a function of the reactive higher harmonics terminations. The theoretically predicted waveforms shown in Fig. 6-15, directly overlay the waveforms produced in the simulation. This provides a positive indication, that this theory is a valuable tool in quantifying the affect of the higher harmonic impedances on fundamental performance and the consequential effect on the waveforms.
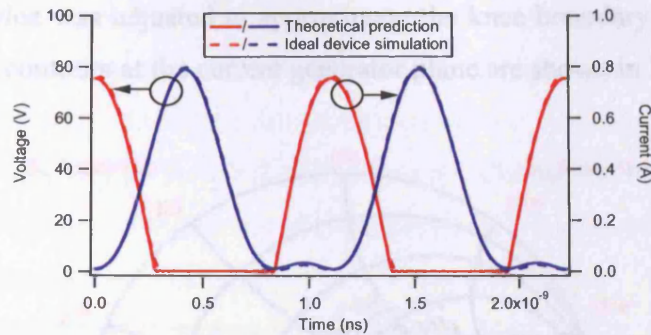
Fig. 6-15 Theoretical and simulated current and voltage waveforms with a reactive second harmonic termination

6.3.3 Measurement Comparison

To further prove the validity of the theory provided by Rhodes, a measurement comparison of the waveforms and the optimum impedance for power is shown using a 5W 7th generation Si LDMOS device provided by Freescale Semiconductor Inc. The device was biased at a drain voltage of 28V and a quiescent current of 24mA, which corresponds to a minimum in 3rd harmonic current, thereby producing the closest possible ideal half rectified class B current waveform [16]. The measurements were done at 900MHz and were conducted using the high power waveform based active harmonic load pull measurement system developed at Cardiff University [17]. Using this measurement system, the higher harmonic impedances are inherently constant throughout the measurement process, which allows for a direct comparison with theory and simulation. In order to provide a common point of reference in all cases the measurements in particular the system impedances being provided to the device were collected and de-embedded to the I_{gen} plane. This was done using the de-embedding network implemented in Chapter 5.

Before the measurements were started the even harmonic impedances (up to and including the eighth harmonic) were measured at the output of the device (i.e. the calibrated reference plane). These were then de-embedded to the current generator plane and applied to theory. The predicted optimum impedance for power using theory was 68.6 + 20.7j Ω with linear output power of 36.4dBm.

The ideal device was adjusted to approximate the knee boundary of the device. The load pull contours at the current generator plane are shown in Fig. 6-16.
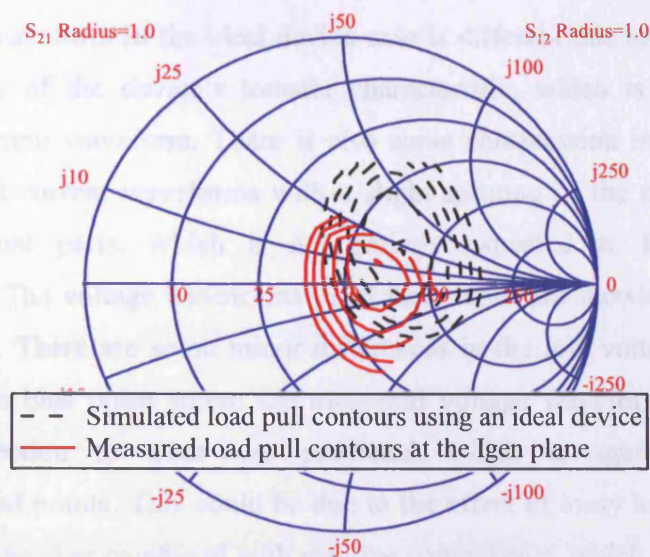

Fig. 6-16 Output power contours of a measured device at the I-gen plane and a simulation of an ideal device with the same higher harmonic impedances both with 0.25dBm step size

The load pull contours shown in Fig. 6-16, show two similarly centred load pull contours. The de-embedded load pull contours are centred at 63.3 + 12.3j Ω, whilst outputting 36.4dBm. The optimum impedance is slightly different than predicted in theory and this is due to the presence of odd harmonic current components in the real device that have not been taken into consideration in Rhodes analysis. These are introduced at higher power levels when the transfer characteristic shows compressive characteristics that introduce third harmonic current components. In addition to that, the device has a soft knee characteristic, which introduces a large area of high output power [3], thereby affecting the shape of the load pull contours.

By conducting a similar analysis now based on the device's DCIV, the simulated optimum impedance for output power is 68.3 + 12.3j Ω. This is confirmed in Fig. 6-17 where the optimum impedance is now in agreement. There is still some disagreement over the shape of the contours, which could be due to errors in the measurement data. This shows that the maths needs to be further developed to incorporate the affect of the odd harmonics. Further work has been done by

Cripps et al. [48] to factor in the odd harmonic current components, which will make the maths more applicable to other modes of operation. The predicted, simulated and measured waveforms at peak output power are shown in Fig. 6-18. The current waveform in the ideal device case is different due to the non linear characteristics of the device's transfer characteristic, which is shown in the simulated current waveform. There is also some compression in the measured and simulated current waveforms with a slight splitting of the main body into two constituent parts, which is not entirely expected at 1dB of power compression. The voltage waveforms in all three cases are showing a high level of agreement. There are some minor differences in the low voltage region and around the dc bias point where the measured voltage waveform shifts in the opposite direction to what was predicted, which is again due to the aforementioned points. This could be due to the effect of lossy higher harmonic terminations together combined with reactive components, which will have to be investigated in the future. However, overall there is a good level of correlation between theory and the de-embedded measured waveforms.
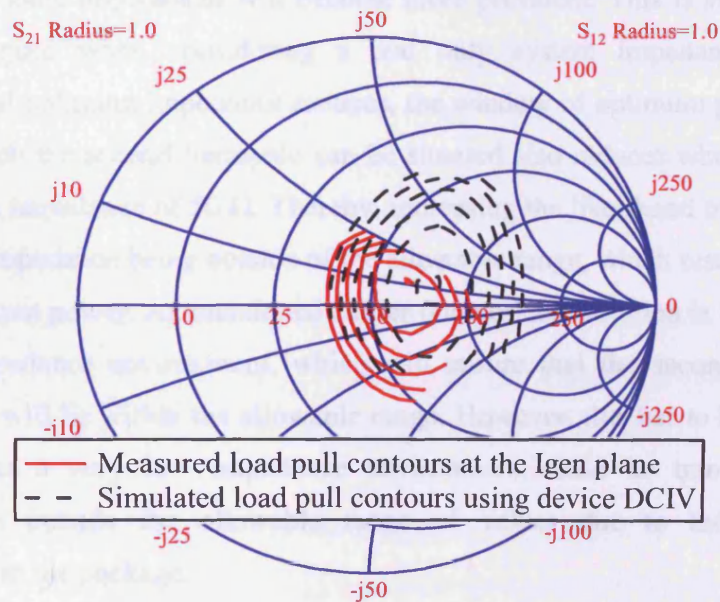

Fig. 6-17 Output power contours of a measured device at the I-gen plane and a simulation of the device DCIV with the same higher harmonic impedances both with 0.25dBm step size
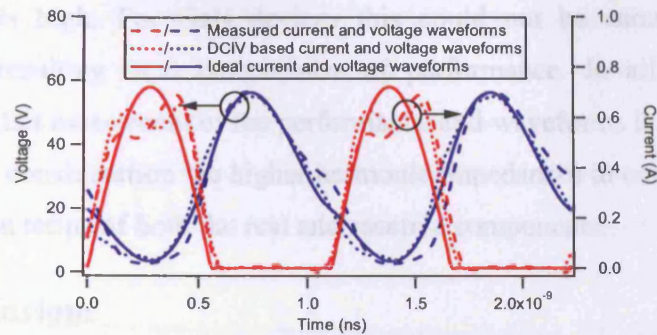
Fig. 6-18 Predicted and de-embedded measured current and voltage waveforms at 1dB compression at the I_{gen} plane

The actual shape of the voltage waveform is shown to be partially sinusoidal in all cases, with some noticeable deviations in the mid-voltage region. Since this device has a much smaller device output capacitance than in the 20W Si LDMOS device the affect of the higher harmonics is more clearly observed. This signifies the affect of the higher harmonic impedances in terms of the waveforms.

In the case of higher power devices, it is possible that the reactive affect of the higher harmonic impedances will become more prevalent. This is similar to the reasons argued when considering a real only system impedance. As the fundamental optimum impedance reduces, the window of optimum performance within which the second harmonic can be situated also reduces when operating in a system impedance of 50 Ω. Thereby, increasing the likelihood of the second harmonic impedance being outside of the allowable range, which results in a loss of peak output power. As mentioned earlier one possible solution is to lower the system impedance environment, which will ensure that the second harmonic impedance will lie within the allowable range. However, this has to be carefully managed as a very low impedance environment could be transformed to impedances outside the allowable range of values due to the bondwire inductance in the package.

Another possibility is that the larger device output capacitance in high power devices will sufficiently assure that the higher harmonic impedances are within their allowable ranges, which can be assumed for Si LDMOS devices where the

capacitance is high. For GaN devices this could not be enough at L-band frequencies resulting in a compromise of performance. In all cases for an accurate and fair assessment of the performance and waveforms it is important to take this into consideration the higher harmonic impedances in combination with the package in terms of both the real and reactive components.

6.4 Conclusions

This chapter has highlighted how factors previously left ignored such as the device package and measurement system impedance could significantly alter the fundamental output device performance, which as a consequence also affects the output current and voltage waveforms. When comparing the de-embedded waveforms to similar results achieved at low power or typically presented in theory, there are differences in the current and voltage waveforms. Whilst small differences such as a slight bifurcation in the current waveform can be more readily explained, other more disconcerting features such as the shape of the voltage waveform and the phase relationship with the current waveform can raise doubts over the accuracy in the de-embedding network.

A first example is given where a high power GaN device is shown to achieve similar output power in two different impedance environments but with significantly different efficiency performance. In addition to that, there was a noticeable difference in the optimum impedance for maximum output power. This provides a significant measurement dilemma, especially when attempting to provide load pull information for use in PA design. One clear difference in the two voltage waveforms was the presence of higher harmonic voltage components when the device was measured in a 50 Ω environment

This following section describes the cause of the difference in the voltage waveforms. Initially, focussing on the difference between a high power device and a low power device measured within a fixed 50 Ω three harmonic controlled measurement system. Whilst the low power device produced the desired waveforms, the high power device generated spurious higher harmonic voltage

components. These were shown to be mitigated by either increasing the order of harmonic control or by reducing the impedance environment. This was then applied to a 20 W Si LDMOS device, which was shown to provide little sensitivity to the higher harmonics. This was found to be due to the large output capacitance found in Si LDMOS devices which dampens the affect of the higher harmonics by providing near short circuits at the I_{gen} plane. However, with the emergence of GaN devices with higher power densities and thus lower drain capacitance, this issue can now be seen more clearly at communication band frequencies.

As high power devices are housed in a package, the system impedance will be transformed to complex impedances that introduce phase rotation in the higher harmonic voltage components. Whilst this is simply applying Ohm's Law, what was not previously clearly understood was the affect of these reactive higher harmonic terminations on the fundamental voltage component and the optimum impedance for maximum output power. Using maths developed by Rhodes, it was shown that the higher harmonic impedances have a significant effect on the voltage waveform and the fundamental impedance for maximum output power. This goes against the popular held notion that the optimum waveforms for power of a device biased in class B, are a half rectified current waveform and a sinusoidal voltage waveform with a real only fundamental impedance.

This has allowed for a re-assignment of waveform goals for confirmation of the de-embedding network. By knowing the higher harmonic impedances being presented to the current generator, the waveform goals for successful de-embedding can be adjusted accordingly. This increases the likelihood of producing a much more universally reliable output circuit model of the device's intrinsic and extrinsic parasitic components. This allows for the effective implementation of known waveform design procedures highlighted in [1]. In addition to that, the effects of the intrinsic and extrinsic parasitic components can be quantified, leading to the identification of potential dangers such as electrical or thermal breakdown.

Further work can be done to account for other modes of operation such as class AB, which are used more often in industry. A class AB bias will introduce odd harmonic current components that will also have an effect on the fundamental performance. The second additional feature is to quantize the effect of lossy higher harmonic impedances in terms of the current and voltage waveforms and the overall performance of the device. This will represent a much more relevant scenario found within matching networks.

7 Waveform Applications – Waveform Based High Efficiency Modes of Operation

The previous chapters have outlined a framework within which to better interpret the waveforms in terms of acquiring information regarding performance and identify possible perturbations within the measurement environment. The next step is to now utilise the ability to access the I_{gen} plane for improved device related investigations. This chapter will focus on two aspects of waveform utilisation. The first topic is single device based efficiency enhancement, in particular class F and inverse class F.

7.1 Efficiency Enhancement

Efficiency enhancement has been a topic of high interest in recent times due to the increasing price of energy and use of wireless systems. There are many possible modes of operation, such as class A, class AB etc [3], which are set by the conduction angle (α) of the current waveform. Class A has a conduction angle of 360 ° and class B has 180 °. In between class A and B is class AB and when the conduction angle moves below 180 ° the device is functioning in class C. Class A typically has high output power and gain but low efficiency. As the conduction angle decreases, the efficiency increases due to a reduction of the average DC component but the device gain and in the case of class C peak output power reduces. Typically a class AB bias is applied in high power PAs, due to a compromise in efficiency, output power and gain. For more information about the traditional modes of operation see reference [3].

Whilst class AB is the current most popular mode of operation, with a typical 1 dB compression drain efficiency of 60 % there is still further room for improvement in terms of efficiency. To improve this further, there are many techniques that have been shown in literature to produce a theoretical operating PA efficiency of 100 % and more. The best method in improving PA efficiency is through waveform based analysis of the current and voltage waveforms. This allows for an objective investigation into optimizing efficiency by either

increasing the RF output power at the fundamental or by reducing the DC power requirements. These are class D, class F, inverse class F and class J. There is one exception and that is class E, which reactively loads the transistor to allow for separate current and voltage generation [49]. All of these modes of operation will be discussed in the next section to provide a general summary of the current trends in performance.

7.1.1 Class D

Class D is a switch mode of operation that works involving two devices connected in parallel through a resonant filter network [3, 50]. The resonant filter network allows content at the fundamental frequency of operation through and provides an open circuit at the higher harmonics to provide a sinusoidal (fundamental only) current swing. Class D amplifiers have been shown to be highly efficient with typical values of drain efficiency around 85-90 %. The waveforms of a typical class D mode of operation, involve a square voltage waveform and a sinusoidal current swing where the device functions as a voltage source. However, these designs have been achieved at low frequencies of operation around 1 MHz. At higher frequencies, the parasitic reactances [51], limit the effectiveness of class D amplifiers, due to power losses in the output capacitance. This has been negated by inverting the amplifiers to function in a current mode of operation, in other words as a current source, with the topology shown in Fig. 7-1(a). This avoids the loss of energy through the capacitor as the filter removes any simultaneous current and voltage content, thereby reducing losses in the transistor. This has allowed for the design and fabrication of highly efficient power amplifiers around a fundamental frequency of 1 GHz using all three major device technologies.
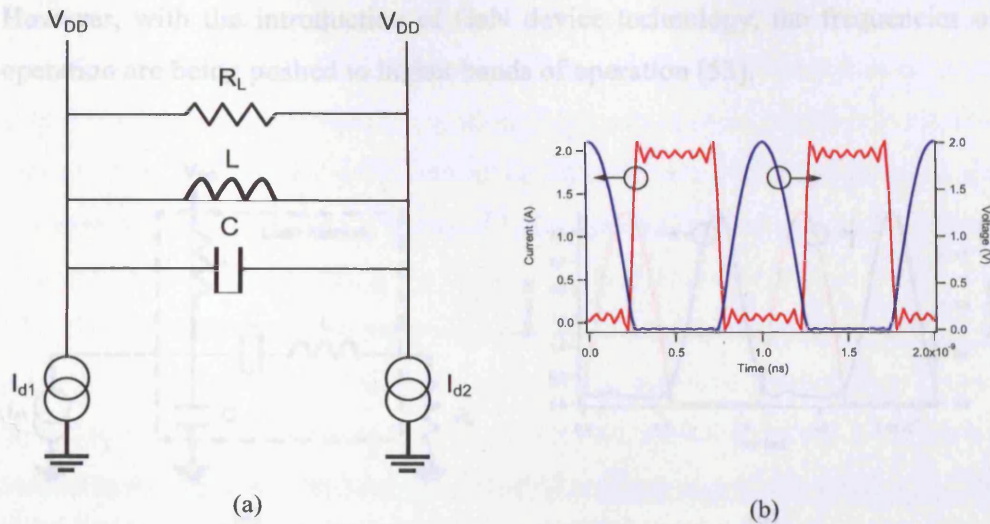
(a)

(b)

Fig. 7-1 (a) Circuit schematic of a current mode class D amplifier, (b) current and voltage
waveforms of an ideal class D amplifier

7.1.2 Class E

Class E is another switch mode of operation that functions around the concept of
a reactive LC tank that resonates out the fundamental frequency. The process
begins with the LC network charging when RF current is flowing in conjunction
with zero RF voltage. When there RF current is in the off cycle, the LC network
discharges its current (reactive component only) with the voltage now in its on
state [9]. The voltage waveform is a function of the reactive current component,
which results in a half-rectified shape. Assuming the resonant network is
completely reactive there is a loss in output power being delivered to the load but
no loss in efficiency. This ensures that class E can offer 100% efficiency in
theory assuming the ideal waveforms can be achieved in practice. Like class D,
class E is a circuit based topology but has the advantage of being easier to apply
at higher frequencies of operation, with a large amount of literature available that
can facilitate high efficiency class E design [52]. This is due to the advantageous
use of the device and package parasitics such as the output capacitance within
the design procedure. This does introduce some limitations in the design
procedure depending on the device technology being used and the expected
output power level requirements. For example high power devices have large
output capacitance values that limit the maximum frequency of operation.

However, with the introduction of GaN device technology, the frequencies of operation are being pushed to higher bands of operation [53].

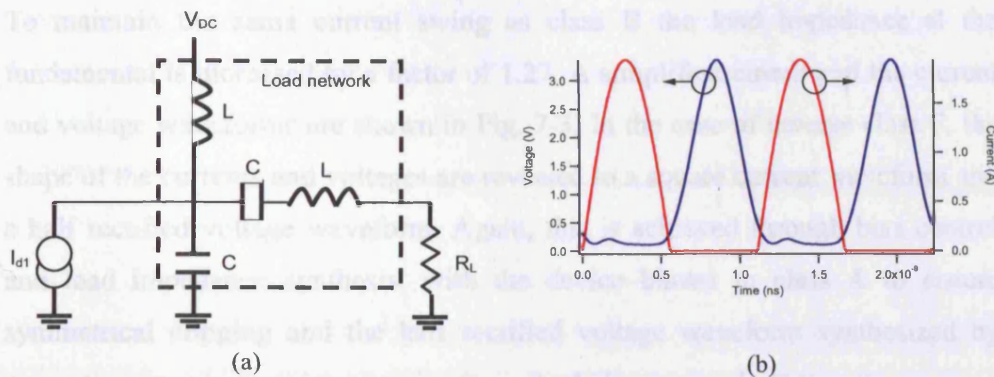(a)   (b)

Fig. 7-2 (a) Circuit schematic of a class E amplifier, (b) current and voltage waveforms of an ideal class E amplifier

7.1.3 Class F and Inverse Class F (F^{-1})

Classes F and F^{-1} are unlike classes D and E in that they are not switch modes of operation. However, they both offer high output power and 100% drain efficiency. The main difference lies in the method of achieving optimum performance. Class F was originally conceived by Snyder [8], where a thorough explanation is given in comparison to class B. He also laid the foundations for class F^{-1} but this was not fully explained until Raab [54]. Class F and F^{-1} achieve high efficiency through manipulating the current and voltage waveforms by current conduction angle and load impedance control through the process of waveform engineering. These waveform based procedures, improve efficiency in two ways by simultaneously reducing the DC requirements and by increasing the RF output power. The actual method of efficiency will be explained in terms of class F. As mentioned earlier class F is based on class B mode of operation, where the current waveform is assumed to be half rectified with no odd harmonic components. Assuming peak linear output power, class B operates at 78.5% drain efficiency. Class F improves this by shaping the voltage waveform to be square in shape when operating in compression, whilst being 90° out of phase with the current waveform to ensure zero loss. The square voltage waveform pulls the current waveform out of compression and increases the

fundamental voltage component. The voltage waveform is shaped by providing open circuit impedances at the odd harmonics and short circuit impedances at the even harmonics. This is done by synthesizing open or short circuit impedances. To maintain the same current swing as class B the load impedance at the fundamental is increased by a factor of 1.27. A simplified circuit and the current and voltage waveforms are shown in Fig. 7-3. In the case of inverse class F, the shape of the currents and voltages are reversed to a square current waveform and a half rectified voltage waveform. Again, this is achieved through bias control and load impedance synthesis, with the device biased in class A to ensure symmetrical clipping and the half rectified voltage waveform synthesized by presenting even harmonic open circuits and odd harmonic short circuits.
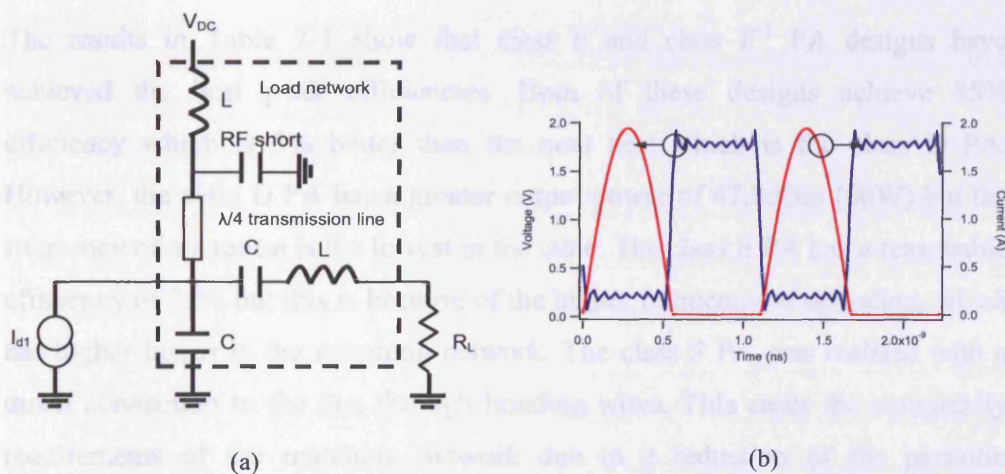

Fig. 7-3 (a) Circuit schematic of a class F amplifier, (b) current and voltage waveforms of an ideal class F amplifier

Class F and inverse class F amplifiers have been successfully made at L-band and S-band frequencies [10, 11, 55]. These have been made by designing multi-harmonic matching networks that provide the high reflects required to produce open and short circuit impedances. In practice, due to the increased complexity in designing multi-harmonic matching networks and the difficulty in producing high reflects at higher frequencies of operation, most realized PAs typically incorporate up to three harmonics. This has led to operating efficiencies greater than 80% at S-band frequencies typically when utilizing GaN devices.

7.1.4 Summary

To summarize the previous discussion, the peak efficiency performance of each mode of operation whilst outputting at least 5 W of output power is presented in Table 7-1[*].

Class of Operation	Pout (dBm)	Efficiency (%)	Frequency (GHz)	Device technology
D [56]	47.8	78	0.9	GaN
E [57]	40	74	2	GaN
F [58]	42.1	85	2	GaN
F^{-1}[59]	38	85	1.2	GaN

Table 7-1 Summary of peak efficiency performance achieved in various classes of operation

The results in Table 7-1 show that class F and class F^{-1} PA designs have achieved the best peak efficiencies. Both of these designs achieve 85% efficiency which is 7% better than the next best which is the class D PA. However, the class D PA has a greater output power of 47.8dBm (60W) but the frequency of operation is the lowest in the table. The class E PA has a reasonable efficiency of 74% but this is because of the higher frequency of operation, which has higher losses in the matching network. The class F PA was realised with a direct connection to the die, through bonding wires. This eases the complexity requirements of the matching network due to a reduction of the parasitic components and allows for the incorporation of higher harmonics, which in turn increases the peak attainable efficiency [54].

Another trend worth noting is the exclusive use of GaN transistors in all of the leading high efficiency PA designs. GaN transistors offer a higher power density than the more established semiconductor materials such as Si LDMOS and GaAs [60]. This in turn produces smaller devices, which are housed in smaller packages, which reduces both the device and package parasitic effects. The end result is an easing of matching network complexity and thus allowing for the realisation of higher efficiency PAs. However, providing access can be obtained

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[*] Table 7-1 is correct at time of publication.

at the I_{gen} plane, waveform engineering procedures can be applied to any device technology. This allows for the realisation of high efficiency PA design that is not technology dependent. The following work, outlines a waveform based engineering procedure that has been applied to a 5W Si LDMOS device. In comparison with GaN devices, Si LDMOS devices have a much lower power density and comparatively lower frequency performance such as unity gain (F_T) frequencies in the region of 5-6GHz.However, despite these performance shortcomings, Si LDMOS is the current device technology of choice in the communications sector due to low cost and high linearity. If high efficiency Si LDMOS device based PA structures can be realised, it is more likely such designs can be used in industry provided there are means for improved linearization techniques such as digital predistortion (DPD) [3] that can cancel out the increase in inter-modulation (IMD) products.

7.2 Waveform Engineering of Si LDMOS Devices for High Efficiency Modes of Operation

As mentioned earlier, all of the leading high efficiency PAs have been realized using GaN technology. A large amount of high efficiency PAs have been realized using Si LDMOS, however these have been achieved at lower frequencies of operation in the L-band around 1GHz [10, 61]. These have typically achieved efficiencies in the mid to high 70 % region with nominally 10W output power. Similar high efficiency LDMOS based designs have also been realized, but these have typically produced drain efficiencies in the low 60 % region [61], which is effectively no better than typical class AB/B performance. The reasons for this loss in efficiency were put down to the low frequency of maximum gain (F_T) of Si LDMOS devices and the high device output capacitance C_{ds}, which limits the ability to produce ideal impedances required for high efficiency modes of operation. However, no proof has been given on whether these arguments are valid. This work investigates, the feasibility of producing high efficiency modes of operation when using LDMOS devices at S-band frequencies. The procedure first starts by investigating the behaviour at L-band frequencies to ascertain a reference of the device's performance. This is then replicated at the higher frequency of operation and the

differences compared. The mode of operation being investigated in this case is class F, in particular focusing on the methodology outlined in [16].

The design methodology outlined in reference [16], involves two stages of waveform engineering. The first step focuses on manipulating the current waveform. This is done by adjusting the gate bias, which in turn adjusts the conduction angle of the output current waveform. As outlined by the original class F paper written by Snyder [8], class F is based on a half rectified current waveform, which consists of even only harmonics. In practice, it is difficult to optimize the gate bias to produce a current null in all of the higher order odd harmonics, so this step is tailored towards producing a null in the third harmonic current (the most significant undesired current component). Once the current waveform has been ascertained, the next step is to focus on the voltage waveform. In this case the voltage waveform is made to be square in shape. The work in [16] was conducted on a small device in a 'clean' on wafer environment, where the optimum impedances were found to be open and short circuits. However, as demonstrated in Chapter 5, the optimum impedance of larger devices has to be embedded out to the measurement plane where the measurements/ matching network design are done. This can confidently be done when the package and device networks are known and satisfactorily verified.

This work is focused on the 5W Si LDMOS device supplied by Freescale Semiconductor Inc, which was de-embedded successfully in Chapter 5. Waveform engineering is demonstrated at both 0.9GHz and 2.1GHz using the high power active harmonic load pull measurement system developed at Cardiff University [17]. To begin with an s-parameter measurement was conducted to investigate the frequency behaviour of the device. The device was biased at 24mA and a frequency sweep from 500 MHz to 11 GHz was done. From this the MAG was extracted and the result is shown in Fig. 7-4, where the MAG region starts from approximately 2GHz and is shown to cross 0dB close to 10GHz. However, this is due to the limited accuracy of the measurement system at low power levels. For this reason the MAG region is extrapolated as shown by the

dotted line and crosses 0dB at around 8GHz. With a fundamental frequency of 2.1GHz there should be enough scope to engineer up to three harmonics. This bandwidth limit has implications on the maximum achievable efficiency. As outlined in [47], a three harmonic class F design can have a maximum efficiency of 90.5%. This and the knee voltage will have to be taken into consideration when calculating the expected peak class F efficiency of the device based on load line analysis outlined in [1] and shown in (7-1).

$$\eta = \frac{P_{RF}}{P_{DC}} * 0.905 * 100 = \frac{0.5(V_1 - V_k)I_1}{V_{dc}I_{dc}} * 0.905 * 100\% = 80.9\%$$ (7-1)
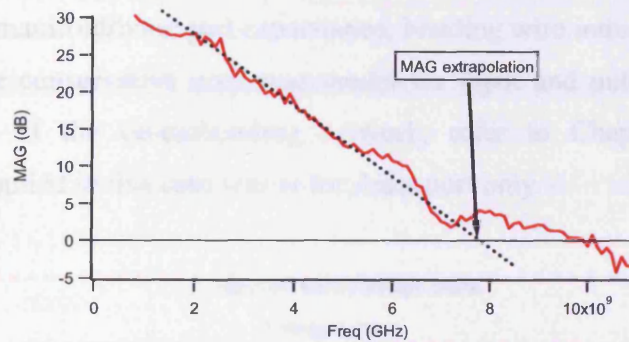
(a)
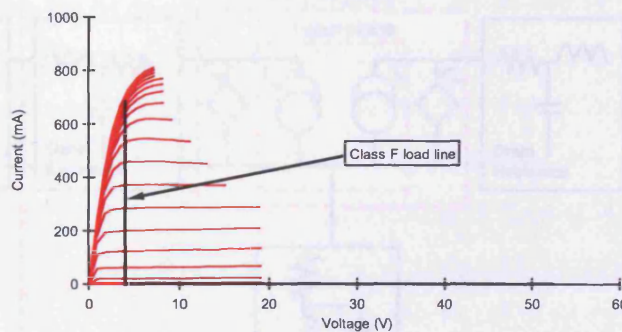
(b)

Fig. 7-4 (a) MSG/MAG of MB3 device over a large frequency range (b) DCIV of the MB3 device

Based on the DCIV characteristic shown in Fig. 7-4(b) and a fundamental voltage expansion of 1.154 (based on a limited bandwidth system of three harmonics [47]) compared to class B [47], the expected class F efficiency is

approximately 81% (assuming a class B current waveform). This now provides a benchmark in the expected performance of the device at a plane that is frequency invariant, i.e. the DCIV. With this in mind the next step is to utilize the prior knowledge in de-embedding obtained in Chapter 5 and apply it to a single device design and to confirm class F mode of operation.

7.2.1 De-embedding to the Current Generator Plane

As mentioned earlier a key requirement for waveform engineering is for procedures to be applied at the current generator plane. Only at this plane is there a direct correlation of the waveforms to the DCIV plane and the performance expected using load line theory [3]. An outline of the package and device de-embedding network is shown in Fig. 7-5. The package and device model, consists of a manifold/bond pad capacitance, bonding wire inductance combined with a charge conservative nonlinear model for input and output charges. For more details of the de-embedding network, refer to Chapter 5. The de-embedding applied in this case was at the drain port only.
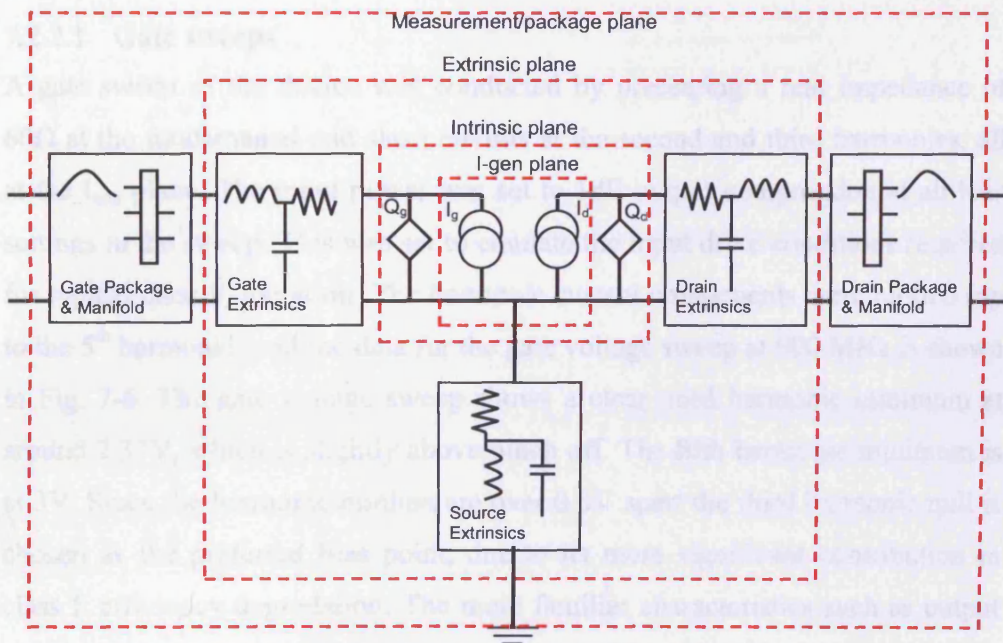

Fig. 7-5 Block diagram of a FET and the various reference planes accessible for waveform engineering

The parasitic model allowed for the calculation of output impedances required at the measurement plane to present the desired real, open or short circuit impedances at the current generator plane. The required open and short circuit impedances are shown in Table 7-2. Thus, allowing waveform engineering of class F behavior at the current generator plane.

Frequency	2nd Short	2nd Open	3nd Short	3rd Open
0.9GHz	0-10.1jΩ	0+48.7jΩ	0-13.8jΩ	0+31.5jΩ
2.1GHz	0-20.1jΩ	0+10.1jΩ	0-23jΩ	0+1.2jΩ

Table 7-2 - Summary of the impedances required at the measurement plane to produce short and open circuit terminations at the current generator plane.

7.2.2 Class F Investigation

As mentioned earlier the class F investigation is focused around the procedure developed in [19], with the first step being a gate sweep. The second step involves harmonically optimizing the voltage waveform and a third step involving a fundamental real impedance sweep is also conducted to identify the best compromise for output power and efficiency.

7.2.2.1 Gate sweeps

A gate sweep of the device was conducted by presenting a real impedance of 60Ω at the fundamental and short circuits at the second and third harmonics, all at the I_{gen} plane. The input power was set to 1dB output compression at all bias settings in the sweep. This was set to emulate the input drive conditions required for typical class F operation. The harmonic current components were plotted (up to the 5th harmonic) and the data for the gate voltage sweep at 900 MHz is shown in Fig. 7-6. The gate voltage sweep shows a clear third harmonic minimum at around 2.37V, which is slightly above pinch off. The fifth harmonic minimum is at 3V. Since the harmonic minima are over 0.6V apart the third harmonic null is chosen as the preferred bias point, due to its more significant contribution in class F efficiency degradation. The more familiar characteristics such as output power, gain and drain efficiency are plotted in Fig. 7-7 with the peak in drain efficiency occurring in the same region as the third harmonic minimum.
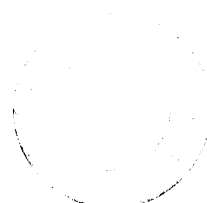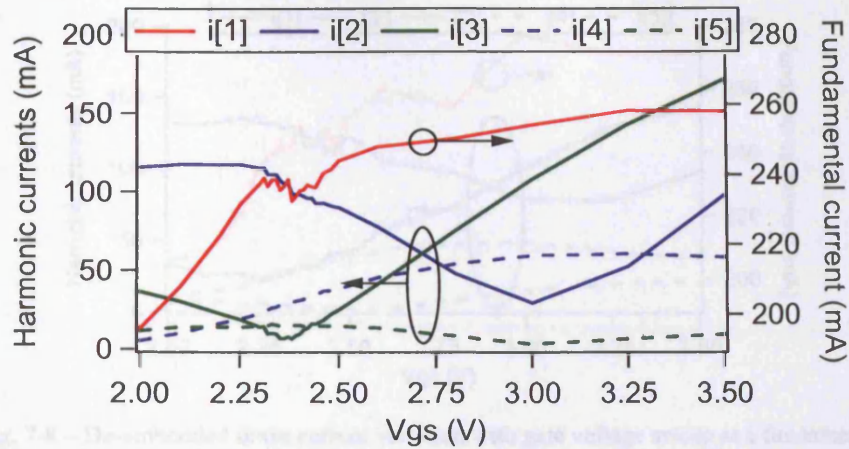
Fig. 7-6 – De-embedded drain current variation with gate voltage sweep at a fundamental
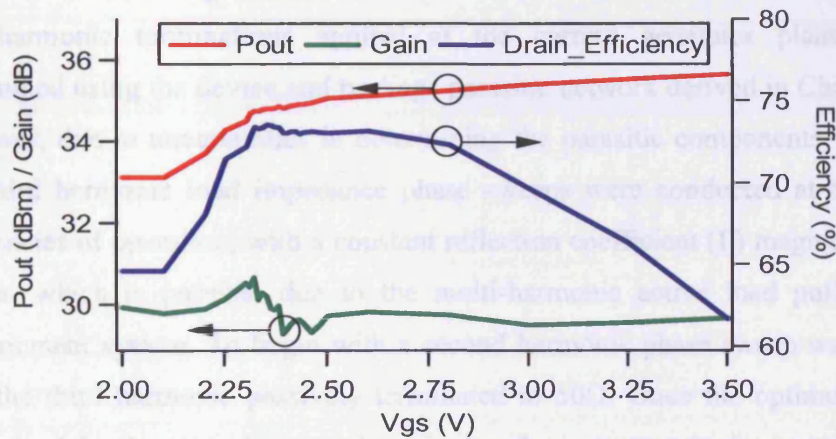frequency of 0.9 GHz with the second and third harmonics set to short

Fig. 7-7 – Output power, gain and drain efficiency variation with gate voltage sweep at a
fundamental frequency of 0.9GHz with the second and third harmonics set to short circuits

The same procedure was performed at 2.1 GHz with the results shown in Fig.
7-8. At 2.1GHz the third harmonic minimum does not occur at the same gate
voltage as 900 MHz. As well as that the third harmonic current minimum is no
longer as clearly defined as it was at 0.9GHz. In this case a minimum third
harmonic current is observed at a gate voltage of 2.25 V. The reason for this
could be due to the increased effects of feedback occurring within the device or
package. Now that the optimum gate bias values are located, the next step in the
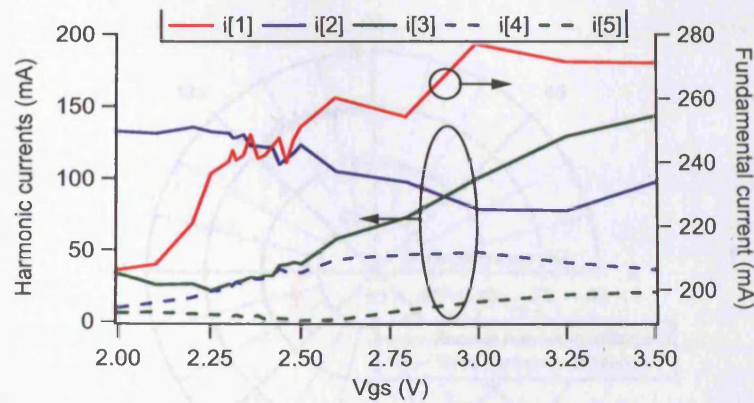process can be applied.

Fig. 7-8 – De-embedded drain current variation with gate voltage sweep at a fundamental frequency of 2.1 GHz with the second and third harmonics set to short

7.2.2.2 Harmonic Optimization

The harmonic terminations applied at the current generator plane were determined using the device and package parasitic network derived in Chapter 5. However, due to uncertainties in determining the parasitic components, second and third harmonic load impedance phase sweeps were conducted at the two frequencies of operation, with a constant reflection coefficient (Γ) magnitude set to one, which is possible due to the multi-harmonic active load pull based measurement system. To begin with a second harmonic phase sweep was done with the third harmonic passively terminated to 50Ω. Once the optimum was determined for the second harmonic a similar phase sweep was done around the third harmonic with the second harmonic now locked to its optimized value. This was first done at 0.9 GHz and then repeated at 2.1 GHz, with the results at the measurement plane shown in Fig. 7-9(a) and (b).

The results at 0.9 GHz show a low sensitivity of the second harmonic, which is due to the large device output capacitance of the device. This effectively already provides the low impedance termination required for producing a short circuit to the I_{gen} plane. The open circuit condition at 0.9 GHz, shows a much higher level of sensitivity, which is again due to the large device output capacitance, which has a very high Q-factor and therefore requires a precise termination for it to be resonated out.

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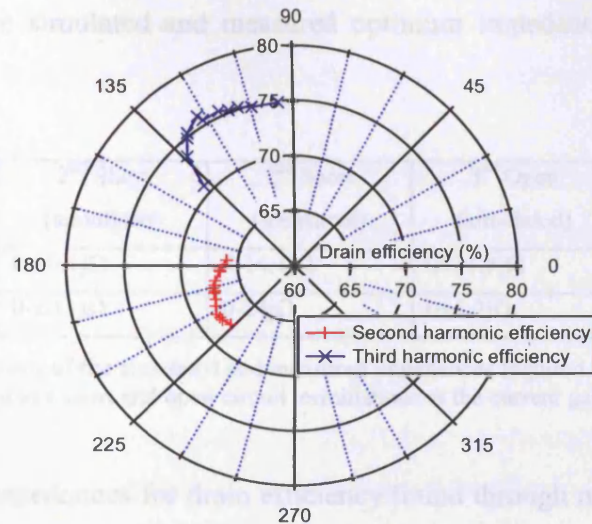
(a)
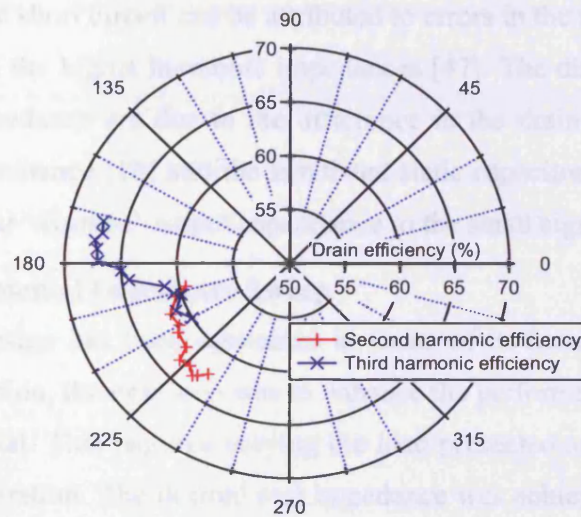
(b)

Fig. 7-9 – (a) Phase sweeps at the measurement plane of the second and third harmonic impedances at a fundamental frequency of 0.9GHz, (b) Phase sweeps at the measurement plane of the second and third harmonic impedances at a fundamental frequency of 2.1GHz

At 2.1 GHz the second harmonic becomes even less sensitive to phase, which is due to the increasing effect of the output capacitance. In turn the performance sensitivity of the open circuit condition is much greater, this is shown by the increased sharpness of the efficiency response at 2.1 GHz than seen at 0.9 GHz. This increased sensitivity in producing an open circuit is one possible reason for the difficulty in achieving the high efficiencies at S-band frequencies. A

summary of the simulated and measured optimum impedances are shown in Table 7-3.

Frequency	2nd Short (simulated)	2nd Short (measured)	3nd Open (simulated)	3rd Open (measured)
0.9GHz	0-10.1jΩ	0-14.4jΩ	0+31.5jΩ	0+28jΩ
2.1GHz	0-20.1jΩ	0-24jΩ	0+1.2jΩ	0+3.5jΩ

Table 7-3 - Summary of the simulated and measured impedances required at the measurement plane to produce short and open circuit terminations at the current generator plane.

The optimum impedances for drain efficiency found through measurement were in good agreement with the simulated short and open circuits. The small differences in the short circuit can be attributed to errors in the series inductances and the affect of the higher harmonic impedances [47]. The discrepancies in the open circuit impedance are due to the difference in the drain voltage sensitive large signal capacitance [18] and the simulated static capacitor. This produces a slightly dissimilar 'average' output capacitance to the small signal derived value.

7.2.2.3 Fundamental Impedance Sweep

Now that the design has been optimized in terms of its harmonic current and voltage composition, the next step was to enhance the performance of the device at the fundamental. This requires varying the load presented at the fundamental frequency of operation. The desired real impedance was achieved at the current generator plane by accounting for the package network. This real intrinsic load was then swept over a range of values to determine the optimum fundamental impedance in terms of power added efficiency. Typically, higher drain efficiencies are possible at high fundamental load impedances as the effect of the knee is minimized. However, in this case the power added efficiency (PAE) is used to ensure that the amplifier has sufficient gain. The results are shown in Fig. 7-10.

The results show that there is an expected decrease in power with load increase but the PAE only noticeably increases up to a fundamental load impedance of 110 Ω For this reason a fundamental load of 110 Ω is chosen as this also

provides 36dBm (4W) of output power. This impedance of 110 Ω at the current generator plane was found to be 54.2+52.6j Ω at the measurement plane.

The same process was applied at 2.1GHz, but it was quickly realized that the performance was not the same as at 0.9 GHz. This was due to the increased sensitivity and complexity of the output capacitance de-embedding, which becomes more important at higher frequencies. The device output capacitance is a non-linear function of drain voltage [18], hence is not fully accounted for when using a simple linear approximation. To improve the calculation of the required measurement plane impedance, the 'average' dynamic capacitance was determined in large signal conditions at the fundamental frequency using the charge conservative model determined in Chapter 5. This simulation involves inserting the charge model into a non linear simulation and exciting the model with a square voltage waveform, from here the capacitance can be extracted at the fundamental frequency using classical s-parameter based techniques. The improved measured 2.1GHz results, now achieved, when sweeping real fundamental load impedance at the current generator plane are shown in Fig. 7-10.
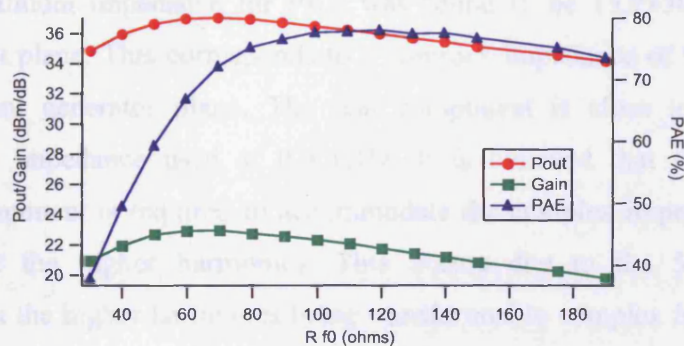
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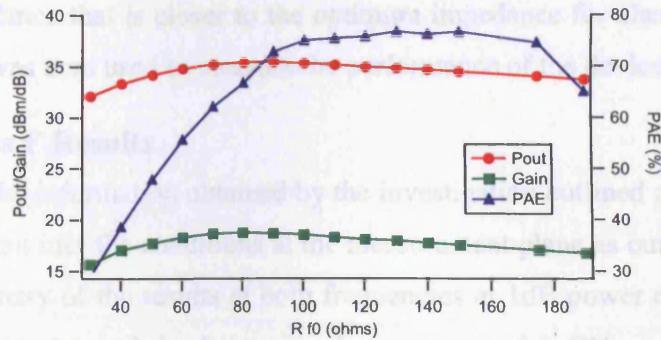
(b)

Fig. 7-10 – (a) Fundamental real only load sweep at the current generator plane measured at 0.9GHz, (b) Fundamental real only load sweep at the current generator plane measured at 2.1GHz

The results in Fig. 7-10 now outline the same performance variation at both frequencies but with a lower gain. This gain reduction was expected due to the relatively low f_T of the device. The PAE at a fundamental impedance of 110 Ω at the current generator plane was 75 %. This was three percent lower than expected and also produced less output power than at 0.9 GHz.

To further optimize the results obtained in Fig. 7-10, a high-density fundamental load pull sweep was conducted around the peak PAE area of 110 Ω. The resulting optimum impedance for PAE was found to be 13.9+30.1j Ω at the measurement plane. This corresponds to a complex impedance of 99.7+25.9j Ω at the current generator plane. The real component is close to the 110 Ω fundamental impedance used at 0.9 GHz. It is believed that the additional reactive component is required to accommodate the complex impedances being presented at the higher harmonics. This occurs due to the 50 Ω system impedance at the higher harmonics being transformed to complex impedances at the current generator plane. For indicative purposes, the second and fourth harmonic impedances were inserted into the equation outlined by Rhodes in [47], which predicted an optimum fundamental impedance of 100 + 10.5j Ω. This correctly indicates that the affect of the higher harmonics have impacted the optimum fundamental impedance for efficiency and provides the designer with a

target impedance that is closer to the optimum impedance for class F. This new impedance was then used to measure the performance of the device in class F.

7.2.3 Class F Results

With all of the information obtained by the investigation outlined previously, the device was put into the conditions at the measurement plane as outlined in Table 7-4. A summary of the results at both frequencies at 1dB power compression is shown in Table 7-5 and the large signal response at 0.9 GHz and 2.1 GHz is shown in Fig. 7-11. The results at 1dB power compression show similar performance at both frequencies of operation, outlining the relevance of performing the waveform based investigation outlined earlier. It is also worth noting that the efficiencies measured at 2.1 GHz are the highest achieved efficiencies when using Si LDMOS devices[*] and the work has been published in [23].

Frequency	Vg (V)	Z(f0)	Z(2f0)	Z(3f0)
0.9GHz	2.37	54.2 + 52.6jΩ	0-14.4jΩ	0+28jΩ
2.1GHz	2.25	13.9 + 30.1jΩ	0-24jΩ	0+3.5jΩ

Table 7-4 –Summary of device and impedance settings for optimized class F performance at 0.9 GHz and 2.1 GHz

Frequency	Pout (dBm)	Gain(dB)	PAE (%)	Drain Eff (%)
0.9GHz	36	24.1	77.4	77.6
2.1GHz	35.4	19.1	74.8	75.7

Table 7-5 - Summary of the class F performance at 0.9GHz and 2.1GHz at 1dB compression

The results at 0.9 GHz show peak efficiency at 4dB compression with a peak power added efficiency of 78%, whilst outputting approximately 4W of output power at greater than 20dB power gain. These results are in agreement with previously published work on Si LDMOS devices [10, 61]. It is important to note that due to the gate bias being close to the threshold voltage the gain profile exhibits gain expansion at lower power levels. What is also worth noting is that the device provides a region of flat high efficiency when in compression.

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[*] At time of writing
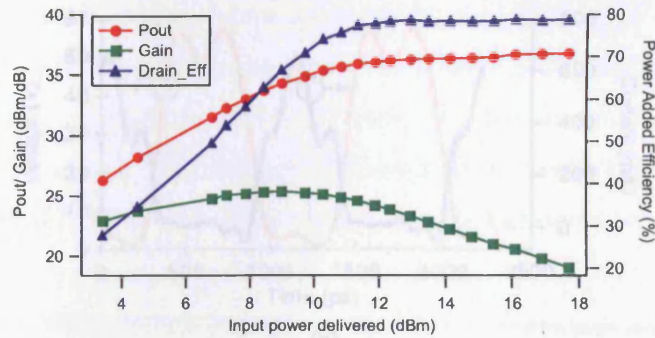
(a)
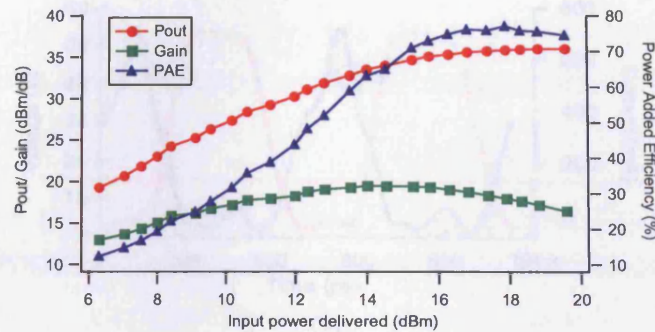
(b)

Fig. 7-11 – (a) Large signal performance of class F operation at 0.9 GHz, (b) Large signal performance of class F operation at 2.1 GHz

At 2.1 GHz, the device exhibits much of the same performance trends as at 0.9 GHz, but due to the gain roll off characteristics inherent in the device, the gain drops and subsequently affects the power added efficiency. The device achieves peak power added efficiency of 77.1 % PAE at 2 dB compression with 35.9 dBm of power being delivered to the load. The main difference is that the flat peak efficiency region at 0.9 GHz was not replicated at 2.1 GHz. This is due to the increased sensitivity of the output drain capacitor to the voltage swing at the higher third harmonic frequency of 6.3 GHz. This makes it harder to produce the required ideal open circuit for optimum class F operation with drive as the 'average' capacitance is increasing with the voltage swing extending into the knee region and spending more time in the low voltage region where the drain capacitance is at its highest [30]. For confirmation of class F operation, the current and voltage waveforms at the I_{gen} plane at 1 dB power compression are shown in Fig. 7-12.
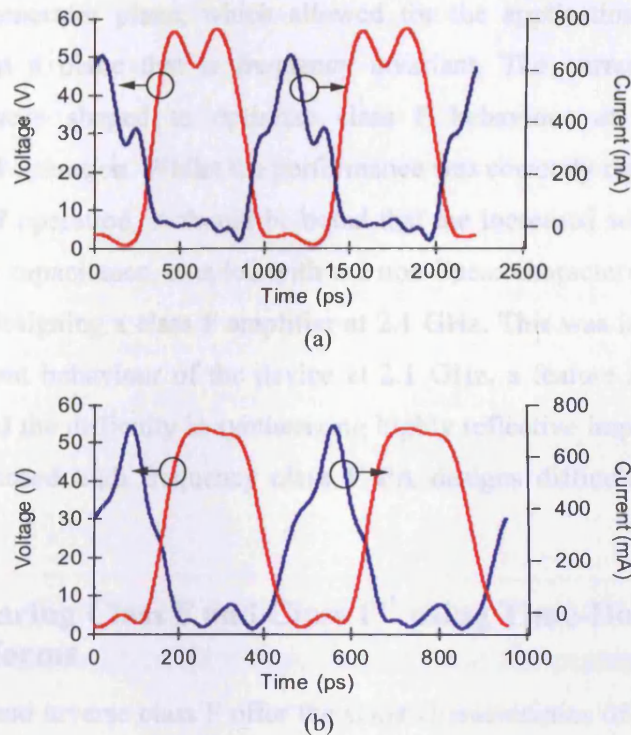
(a)

(b)

Fig. 7-12 – Measured voltage and current waveforms at 1 dB compression at the current generator plane at 0.9 GHz, (b) Measured voltage and current waveforms at 1 dB compression at the current generator plane at 2.1 GHz

In both cases the current and voltage waveforms at the I_{gen} plane shown in Fig. 7-12 are confirming class F operation. In both cases the voltage waveform is square in shape. At 0.9 GHz the voltage waveform has a slightly large third harmonic component than at 2.1 GHz. Again, in both cases the current waveform is half rectified, there are some extra harmonic components in both cases due to a small amount of compression. In both cases the waveforms are more 'well-defined' at 0.9 GHz than at 2.1 GHz but this is due to the limited bandwidth of the measurement system, which accounts for twelve harmonics at 0.9 GHz and only five harmonics at 2.1 GHz.

7.2.4　Conclusions

Through the use of de-embedding and active harmonic load pull, the demonstration of a Si LDMOS device in class F operation has been shown at both 0.9 GHz and 2.1 GHz. This has led to achievement of record levels of efficiency at S-band frequencies. This was made possible by de-embedding to

the current generator plane, which allowed for the application of waveform engineering at a plane that is frequency invariant. The current and voltage waveforms were shaped to optimize class F behaviour at both intended frequencies of operation. Whilst the performance was correctly replicated at both frequencies of operation, it should be noted that the increased sensitivity of the device output capacitance, coupled with the non-linear characteristics raises the difficulty in designing a class F amplifier at 2.1 GHz. This was indicated by the drive dependent behaviour of the device at 2.1 GHz, a feature not seen at 0.9 GHz. This and the difficulty in synthesizing highly reflective impedances makes Si LDMOS based high frequency class F PA designs difficult to achieve in practice.

7.3 Comparing Class F and Class F^{-1} using Time-Domain Waveforms

Both class F and inverse class F offer the same characteristics of high efficiency and high power and are of great recent interest in the field of PA design. However, whilst there have been numerous publications using both implementations [10-11, 16, 30, 61], there has been no conclusive evidence of why a certain mode of operation is chosen over the other. In addition to that, there have been many variations in implementation of both modes of operation and a lack of measured waveforms leave uncertainty as to whether optimum performance has been achieved. This work focuses on the same 5W Si LDMOS device used earlier and emulates the conditions required for class F and inverse class F for a more realistic comparison of their performance.

In order to compare class F and inverse class F modes this work presents the emulation of the design conditions optimised using waveform engineering at the I_{gen} plane. This is done using the active harmonic load-pull measurement system developed at Cardiff University [17] based at a fundamental frequency of 0.9 GHz. In this experiment the measurement system has been used to explore identical transistor parts in optimal bias and load conditions for the class F and inverse class F modes, but with the output matching network emulated up to the third harmonic. This allows for an excellent reproducibility of results and

removes any implementation uncertainties, making it an extremely fair method of comparing a particular device's performance in a given mode of operation. Before moving onto the results, a brief theoretical overview of the effect of limited bandwidth in both modes of operation is given.

7.3.1 The Effect of Limited Bandwidth

In order to understand the results, it is useful to quantify the peak attainable efficiencies of class F and inverse class F operation using this device. In both cases three harmonic active load pull was applied, which limits the peak performance of the device [3, 54]. The value of the knee voltage is the same in both cases.

In a class F configuration the maximum efficiency possible using three harmonics is 90.6% [54]. This value assumes that the current waveform is shaped by the device's conduction angle (controlled by the dc gate bias point) and therefore contains an infinite number of even harmonics, dependant on the device's f_T. This device has an f_T in the region of 7.5 GHz, which allows the current waveform to consist of eight harmonics describing up to 98.9% of the total performance. Assuming a knee voltage of 2.5V and dc bias voltage of 28V the peak attainable efficiency for class F is shown in (7-2).

$$\eta_F = 100 * \frac{\left(V_{DC} - V_K\right)}{V_{DC}} * 0.906 * 0.989 = 81.6\% \tag{7-2}$$

In a three harmonic implementation of an inverse class F configuration, the voltage waveform can only be shaped by the second harmonic and fundamental components. The current waveform in this case is assumed to be squared by hitting the current device boundaries in a symmetrical fashion, thus generating only odd harmonic components. In this case a similar current harmonic limit is defined in terms of the device f_T and is assumed to contain seven harmonics describing 97.5% of the total performance. This results in the peak attainable efficiency shown in (7-3).

$$\eta_{F^{-1}} = 100 * \frac{(V_{DC} - V_K)}{V_{DC}} * 0.926 * 0.975 = 82.2\% \tag{7-3}$$

Based on these ideal uncompressed waveform based calculations it can be said that the inverse class F mode of operation is 0.6% more efficient than class F. Whilst this is not a major difference, this coupled with the comparative ease of implementing an open circuit termination at the second harmonic frequency (as opposed to the third harmonic in class F), make inverse class F appear a more attractive mode of operation.

7.3.2 Results

Using the waveform based class F methodology outlined earlier and a similar inverse class F procedure [56], the device conditions for optimum operation were determined. These are outlined in Table 7-6. As discussed earlier the bias point for class F is close to class B, slightly above the threshold voltage. For inverse class F, the gate bias is much higher and closer to class A, this is done to provide symmetrical clipping of the current waveform to ensure a square shaped output. The fundamental impedance of inverse class F is also different to class F, which is due to the larger voltage swing at the fundamental.

Mode of operation	Vg (V)	Z(f0)	Z(2f0)	Z(3f0)
Class F	2.37	54.2 + 52.6jΩ	0 – 14.4jΩ	0 + 28jΩ
Class F^{-1}	3.5	55.4 + 56.7jΩ	0 +71.8jΩ	0 - 14.1jΩ

Table 7-6 - Summary of device settings for class F and inverse class F performance

7.3.2.1 Class F

The results for class F are shown in Fig. 7-13 (a), which are the same as shown earlier in this chapter. The de-embedded waveforms at 1dB power compression are shown in Fig. 7-13 (b), which correctly indicate that class F behaviour has been achieved.
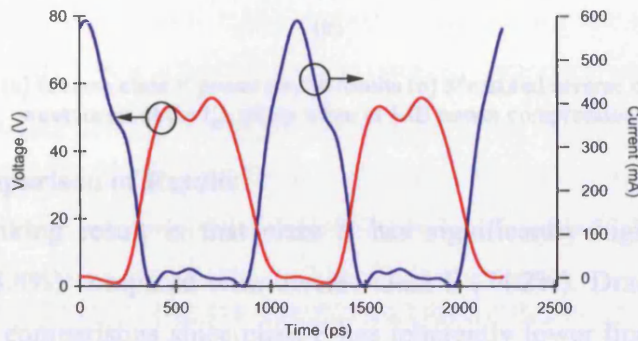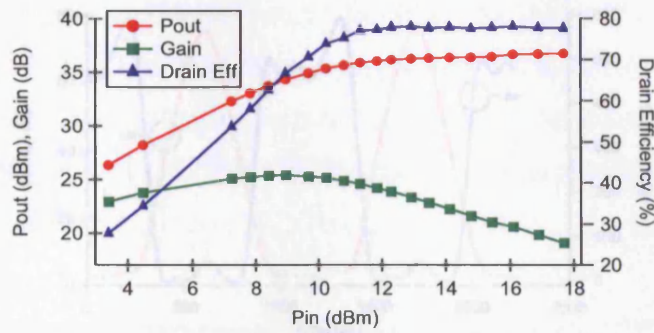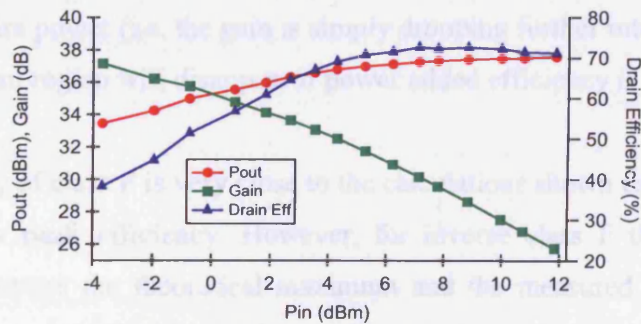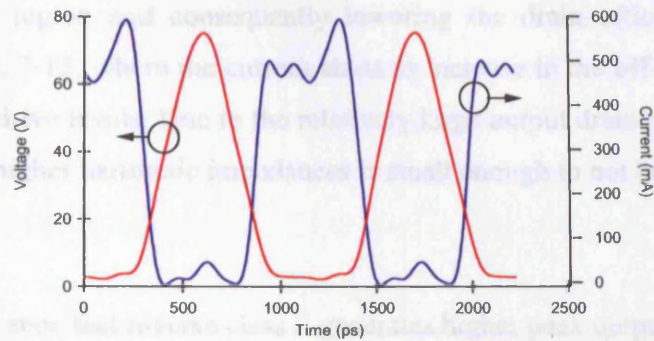
(a)

(b)

Fig. 7-13 – (a) Class F power sweep results (b) Measured class F output waveforms at the I_{gen} plane when at 1dB power compression

7.3.2.2 Inverse Class F

The results for inverse class F are shown in Fig. 7-14 (a), which show a peak drain efficiency of 74%. The de-embedded waveforms at 1dB power compression are shown in Fig. 7-14 (b), which show a square current waveform and a half rectified voltage waveform, correctly indicating inverse class F behaviour.

(a)

(b)

Fig. 7-14 – (a) Inverse class F power sweep results (b) Measured inverse class F output
waveforms at the I_{gen} plane when at 1dB power compression

7.3.2.3   Comparison of Results

The most striking result is that class F has significantly higher peak drain
efficiency (78.8%) compared with inverse class F (74.2%). Drain efficiency is
used in these comparisons since class F has inherently lower linear gain due to
the reduced conduction angle bias point and therefore PAE will be skewed
towards inverse class F. The gain profile of the class F power sweep is flat over a
large dynamic range. The inverse class F gain profile starts to compress much
earlier due to the class A bias point. However, in both cases the gain profiles
could be linearised using modern digital predistortion methods. In addition, both
modes of operation produce a region of high efficiency over a large dynamic
range. This region of high efficiency is a useful observation for modulation
schemes without constant envelopes such as GSM-EDGE and CDMA. The
plateau in drain efficiency simply occurs as the output waveforms are
compressed against the device characteristics. However, further input drive will
yield little extra power (i.e. the gain is simply dropping further into compression)
and this plateau region will disappear if power added efficiency is considered.

The efficiency of class F is very close to the calculations shown earlier with only
a 3% drop in peak efficiency. However, for inverse class F there is an 8%
difference between the theoretical maximum and the measured value. Further
analysis of the waveforms has shown that this is due to the voltage swing
approaching the voltage breakdown of the device, which generates current in the

high voltage region and consequently lowering the drain efficiency. This is shown in Fig. 7-15, where the current starts to increase in the off-state region at higher input drive levels. Due to the relatively large output drain capacitance the effect of the higher harmonic impedances is small enough to not be considered in this study.

It can also be seen that inverse class F generates higher peak output powers. This is because the inverse class F mode extends the output voltage swing, which is possible due to the lack of a hard upper voltage boundary until catastrophic breakdown is reached. At the 28V drain bias used in this experiment the breakdown limit for these devices has not been fully reached. In class F the extension is seen in the current waveform. However, the current waveform is not able to extend beyond the hard I_{MAX} boundary that limits the current at about 600mA in these devices.
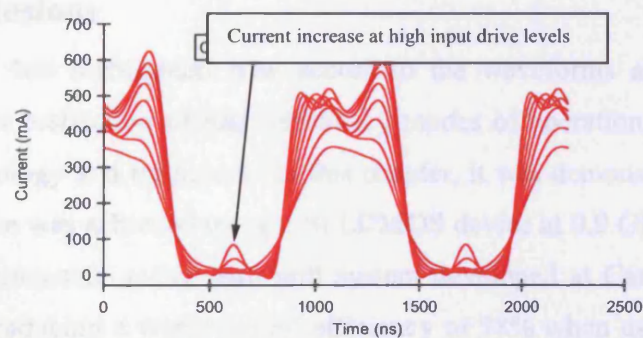

Fig. 7-15 - Measured inverse class F output current waveforms at the I_{gen} with increasing drive

7.3.3   Inverse Class F Performance Optimisation

This work has compared the performance of a Si LDMOS device, biased at the same drain bias point, operating in identically bandwidth limited class F and inverse class F circuit conditions. It was found that higher peak drain efficiency was achieved in class F, although inverse class F generated more output power and had higher gain. Both modes were shown to maintain good efficiency into power saturation over a good dynamic range of output powers. The lower peak drain efficiency in inverse class F is due to the voltage breakdown effects of the device. Further measurements were done at a lower drain bias of 18V to remove

the possibility of any voltage breakdown. The waveforms are shown in Fig. 7-16, where the current waveform behaving much flatter in the off region. At this drain bias setting the device achieved a peak drain efficiency of 79%, which is slightly higher than the efficiency obtained in class F as well as being much closer to what theory dictates.
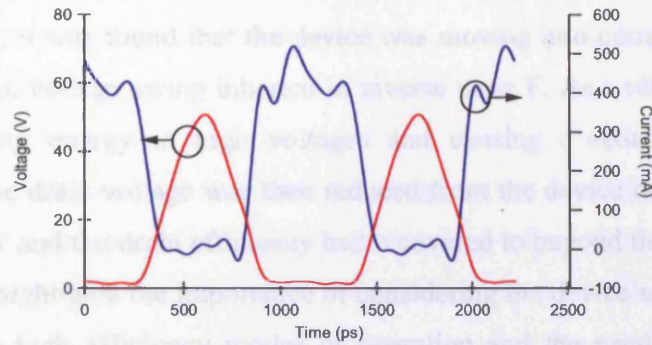

Fig. 7-16 – Measured inverse class F output waveforms at the I_{gen} plane at 1dB power compression with $V_D = 18V$

7.4 Conclusions

This chapter has highlighted how access to the waveforms at the I_{gen} plane allows for the realisation of high efficiency modes of operation, irrespective of device technology and frequency. In this chapter, it was demonstrated that class F performance was achieved using a Si LDMOS device at 0.9 GHz and 2.1 GHz using multi-harmonic active load pull system developed at Cardiff University. The latter, producing a world record efficiency of 78% when using Si LDMOS devices. This was made possible by obtaining access to the I_{gen} plane, which allowed for comparison at a plane that is invariant with frequency. This provided a firm base for applying known waveform based procedures that could be applied with confidence. The resulting systematic investigation, provided near identical performance at both frequencies of operation and some valuable evidence as to why it is difficult to produce highly efficient modes of operation with Si LDMOS devices. Namely, the difficulty in accounting for a large dynamically varying output capacitance. This makes it difficult to sustain class F behaviour at various drive levels, due to a shift in the impedance requirements for presenting an open circuit at the I_{gen} plane.

The second half of this chapter, looked into comparing two waveform based high efficiency modes of operation, class F and inverse class F. This investigation was conducted on a Si LDMOS device at 0.9 GHz and in a limited bandwidth system of three harmonics. The resulting theoretical analysis, provided evidence that inverse class F was slightly more efficient than class F, however this was initially not found to be the case when put into practice. After further investigations, it was found that the device was moving into current breakdown due to the high voltage swing inherent in inverse class F. As a result the device was dissipating energy at high voltages and causing a reduction in drain efficiency. The drain voltage was then reduced from the device data sheet value of 28V to 18V and the drain efficiency had recovered to beyond that achieved by class F. This highlights the importance of considering the device's features when implementing high efficiency modes of operation and the need for obtaining access at the I_{gen} plane for identifying such issues that would be very difficult to identify otherwise.

8 Waveform Applications – Waveform Based Verification of a Charge Conservative Model

The previous chapter outlined how access to the I_{gen} plane can allow for improvements in high efficiency PA design. Now this chapter utilises the ability to de-embed time-domain based data to various reference planes within the device for passive and active model verification in the time domain and thus assessing the model's ability to conduct waveform engineering for high efficiency PA design. Such a comparison has not been well covered in the literature due to the limited availability of high power time domain data and limited access to the internal workings of a model, making this a topic of high relevance for both the modelling engineer and the PA designer.

8.1 Introduction

The use of CAD based non-linear models is an essential part of the microwave power amplifier (PA) design process. Through the use of models the design cycle time could be drastically reduced, significantly cutting costs and resources. However, this saving in time-to-market is greatly dependent on the flexibility and accuracy of the model [18].

Device models can be separated into two main categories, the first being structural models, based on the physical properties of the materials and the layout. Whilst these models offer a high level of flexibility and accuracy, the long simulation time and difficulties in drawing the physical topology make them highly difficult to use. This is especially applicable in the high power PA domain where the devices are physically large and the fundamental frequency of operation is always increasing.

In contrast behavioral models are faster and less draining on computing resources. Behavioral models use polynomial equations that are fitted to a certain set of device measurements. They are often split into two groups, either physical models or empirical models [62]. Physical models describe the individual

passive and active components that exist within a typical equivalent circuit description allowing for an account of the relationship between the currents and voltages. Empirical models treat the device as a "black box" and accounts for the relation between the input and output content.

The model being tested in this case is a physical behavioral model based on an energy and charge conservative approach. This ensures that the model functions within a stable physical environment allowing for increased confidence in the reliability of the model. The intrinsic non-linear model called the FET^2 model is based on established passive and active modeling procedures as outlined in [18, 26, 36-37]. The complete device architecture containing the non-linear electro-thermal charge conservative intrinsic device model is shown in Fig. 8-1. The FET^2 model has been enhanced to allow for improved extrapolation of the drain and gate charges outside of the original measured region using artificial neural networks (ANN) to model the reactive current sources. The real current source is modeled using a function proposed by Fager et. al [64], which has been shown to improve prediction of the distortion products and can be adjusted to account for current breakdown properties. The extrinsic network and package consists of s-parameter measurements and electro-magnetic simulations (EM) which were explained in more detail in Chapter 5 but will be revisited briefly again within a modeling context.
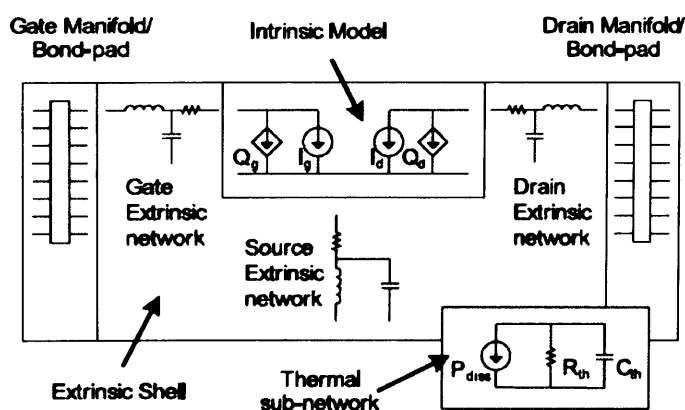

Fig. 8-1 – Block representation of the transistor model architecture

The nonlinear electro-thermal FET^2 model has been shown to accurately predict traditional large-signal power behavior of Si LDMOS devices at 2.1GHz [37]. However, this paper focuses on providing more detailed verification of the FET^2 model using time-domain waveforms. Time-domain current and voltage waveforms allow for a more intuitive look into how the device hence model works [24]. It allows for a means of determining how well the model is predicting the power performance at the fundamental and the higher harmonics. One extension of this is in the field of high efficiency PA design, where waveform engineering of the higher harmonic currents and voltages has been utilized to produce highly efficient modes of operation that are device and frequency independent [3, 65-66]. These modes allow for an assessment of the model's sensitivity to bias, input and output voltage stimuli at planes that frequency dependent and independent. Thus, allowing for a means of assessing the effectiveness of the model for different modes of operation. This chapter first focuses on providing verification of the device model through established techniques and then moves onto comparing measurements and model voltages and currents in fundamental and harmonically enhanced modes of operation.

8.2   The Benefits of Time Domain Model Validation

To enable confidence in the use of the model it is vital to have the model validated according to the needs of the user. In this case the non-linear device model is to be used for high power PA design and must show sensitivity to the higher harmonic impedances and the thermal measurement environment. Typically, non-linear models are validated using continuous wave (CW) and 2-tone measurements within a load-pull/source-pull setup. The measurements collected consist of scalar power values and vector impedances. This allows for an investigation into the performance of the device and model in terms of output power, drain efficiency, gain, harmonic distortion (CW) and inter-modulation (2-tone) as well as the sensitivity of the device and model performance with respect to the fundamental load/source impedance. Whilst this has been the established technique for model validation there can still be an element of doubt as to how the model is predicting these results. This is because of the unknown

composition of the current and voltage content. When measuring using a vector network analyzer and scalar power meter it is not possible to determine the current and voltage content in both magnitude and phase. This is because the measured power being delivered to the load consists of just the real component as pointed out in (8-1). To do this, requires the use of a non-linear vector network analyzer (NVNA).

$$\vec{Z} = \frac{\vec{V}}{\vec{I}} \tag{8-1}$$

$$P_{del} = \frac{1}{2} real(\vec{VI}*) \tag{8-2}$$

NVNA based systems allow for time-domain capture of the current and voltage waveforms, which contains all of the magnitude as well as phase information over a large frequency bandwidth spanning multiple harmonics. This allows for an improved insight for device characterization and power amplifier design [3, 24]. From the modeling perspective, this enables an in depth investigation of the high frequency time-domain properties of the charge conservative model. Thus, providing a measured dynamic environment where the model's real and reactive current generation capabilities can be tested and investigated to gain further insight into the accuracy of the predicted device behavior [65].

8.3 Measurement and Model Uncertainties

Before an accurate comparison of the measurement and model waveforms is conducted it is important to assess the possible sources of error present in both the measurements and the model. In the case of measurements the main source of error is determined by the accuracy of the equipment being used for data capture. In this case the NVNA based measurement system developed by Cardiff University [66] relies on data captured using the Tektronix sampling oscilloscope which has an absolute accuracy of approximately ±0.02dBV [67]. Assuming a 1V forward travelling wave, this equates to an error of magnitude ±0.01V or ±0.01Vmeas. The measured voltage and the associated error is given by (8-3), which is determined by the individual travelling waves.

$$V_1 = (a_1 + b_1)\sqrt{Z_0} \tag{8-3}$$

$$|V_1| = (|a_1| \pm |\Delta_a| + |b_1| \pm |\Delta_b|)\sqrt{Z_0} \tag{8-4}$$

$$|V_1| = ((|a_1| + |b_1|) \pm (|\Delta_a| + |\Delta_b|))\sqrt{Z_0} \tag{8-5}$$

Assuming that the 'a' and 'b' travelling waves are of a similar magnitude and Z_0 is exactly 50Ω the total error in the measured voltage will be ± 2%. Likewise, the same error margin of ± 2% is determined for the current. Using this error in the voltage and current components the port power is calculated using (8-2). The total error in the power is shown in (8-7).

$$|P| = \frac{1}{2}real(VI^*) \pm \sqrt{\left(\frac{0.02I}{I}\right)^2 + \left(\frac{0.02V}{V}\right)^2} \tag{8-6}$$

$$|P| = \frac{1}{2}real(VI^*) \pm 2.8\% \tag{8-7}$$

The total error in the power is determined to be 2.8%, in terms of dB this equates to ±0.13dB which is in line with the accuracy of commercially available power meters. Thus, providing significant confidence in the system's ability to accurately measure waveforms.

The second most influential source of error is in the description of the measurement conditions. In this case the measurement conditions are outlined by the electrical and thermal environment of the test setup. If these conditions are not accurately transferred into the simulation within the model, the model could produce results that could be significantly different in both output power and waveform content.

The third most significant source of uncertainty is in the accuracy of the model. The model's physical parameters are measured to sub mm accuracy and the circuit parameters are first fitted and then validated using small and large-signal

based measurement data. This places a significant requirement on the original measured data to be both accurate and repeatable.

8.4 Model Validation Results

The device used in this investigation is a 4.8mm 7th generation Si LDMOS device provided by Freescale Semiconductor Inc. and measured within an H-block fixture [18]. The time-domain measurements were conducted at 2.1 GHz in CW conditions in various classes of operation such as class AB and class F using the high power multi-harmonic active load-pull system developed at Cardiff University [17]. The measurements were collected at the input and output terminals of the transistor.

The FET[2] model was compiled through a segmented approach consisting of the package and manifold, device extrinsic components and the intrinsic device model as shown in Fig. 8-1. The first stage was to simulate the package, which consisted of input and output bonding wires. These were simulated using Ansoft HFSS™, a finite-element based electromagnetic simulator. The simulation was set to model the features of the individual bonding wires as well as the mutual inductance between the input and output bonding wires [28] over a large frequency range. The device manifold was simulated using Sonnet's EM™ and was also simulated over a large frequency range.

The next stage involved determining the extrinsic components of the device, which was done using cold-FET measurements [19]. The extrinsic network used to fit the cold-FET measurements is described in [26]. After this, pulsed I-Vs and S-parameters were taken to extract the real and reactive current sources, which were then modelled as described in [37]. The resultant transistor model is inclusive of all input, output and feedback components.

For an accurate comparison of the results it is important to maintain the same electrical and thermal conditions in the simulator as was measured on the test setup. This was done by ensuring that the model was operating at the same

quiescent current (I_{DQ}) and drain voltage as the measured device. The source and load higher harmonic impedances up to the 5th harmonic were inserted into the model schematic to maintain the same RF impedance environment [45]. The thermal conditions were emulated by adjusting the thermal resistance (R_{th}) until there was an agreement between the measured and modeled DC-IVs. Since this investigation was based on CW measurements the thermal capacitance (C_{th}) was set to zero.

8.4.1 Results comparison at the transistor output terminals

The FET[2] model was inserted into the measurement conditions outlined earlier and then simulated using Agilent ADS[TM]. Initial comparisons were done with the device biased in class AB (I_{DQ} = 5mA/mm) in terms of load pull contours at 1dB compression as shown in Fig. 8-2. This was done to establish confidence in the use of both the model and the measurements. At 1dB compression the impedance for maximum output power is shown to differ by a small amount with the measured output power 36.5dBm and the model output power 36.7dBm, therefore showing a high level of agreement between measurement and model.

The input and output waveforms both measured and modelled at the impedance for maximum output power are shown in Fig. 8-3 (a) and (b). The measured and modelled output current and voltage waveforms respectively show excellent agreement with each other. Similarly the input current and voltage waveforms shown in Fig. 8-3 (b) are in excellent agreement. There is a slight difference in the gate voltage waveform and this is due to a discrepancy in the source impedances between the measurements and the model. To avoid this issue, all further waveform based comparisons will be based upon the procedure outlined in [9]. This paper outlines the use of pre-defined voltages at both the input and output ports of the device rather than the more traditional approach of impedances, which are difficult to measure on the source port when measuring in forward operation. This approach is also more suited to model validation as the current output of FET based intrinsic models are formulated as functions of the input and output voltage stimuli. In addition to that, whilst these results are very encouraging, the individual voltage and current components are not directly

relatable to what the intrinsic model is doing. For this comparison it is necessary to de-embed the measured current and voltage components to the intrinsic model as shown in Fig. 8-1.
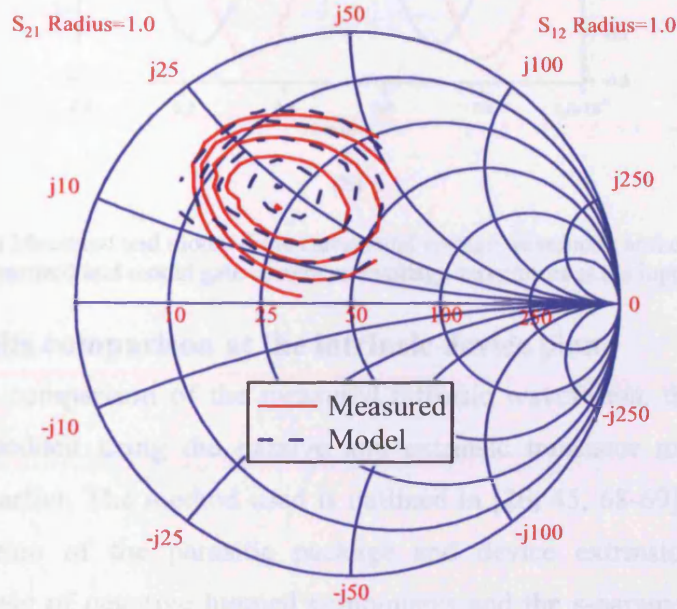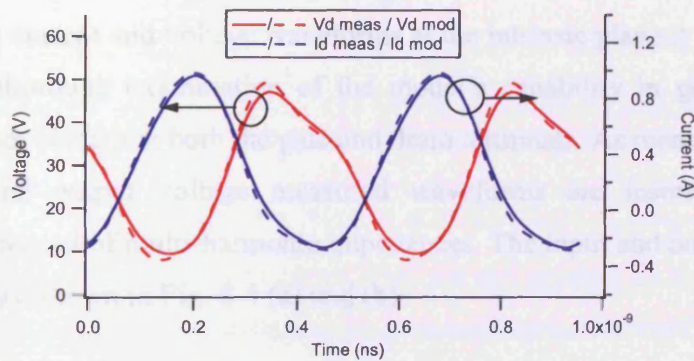

Fig. 8-2 – Measured and model output power contours at 1 dB compression with 0.25 dB step size
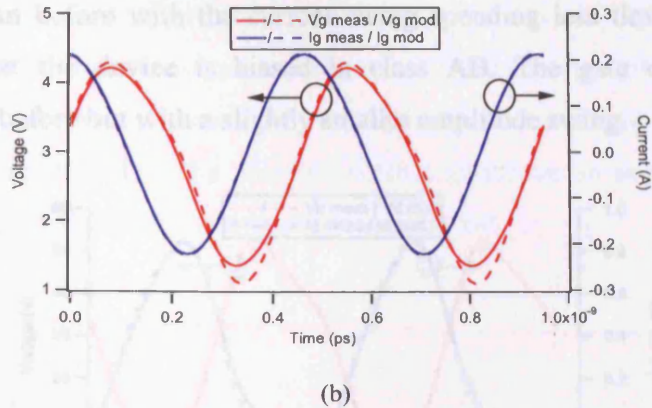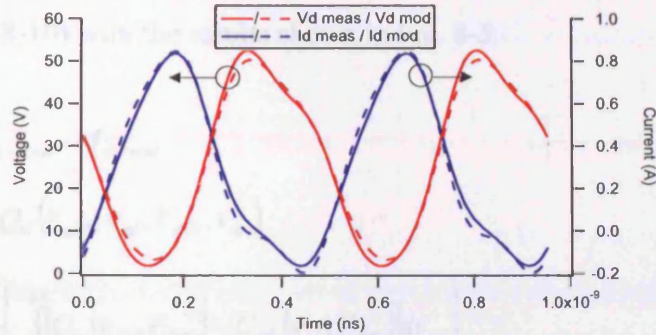

(a)

(b)

Fig. 8-3 – (a) Measured and model drain current and voltage waveforms at the output of the transistor, (b) Measured and model gate current and voltage waveforms at the input of the transistor

8.4.2 Results comparison at the intrinsic device plane

For accurate comparison of the measured intrinsic waveforms, the waveforms were de-embedded using the passive and extrinsic transistor model network determined earlier. The method used is outlined in [26, 45, 68-69] and involves the cancellation of the parasitic package and device extrinsic components through the use of negative lumped components and the s-parameter based de-embed component in Agilent ADS^{TM}. The FET^2 model was altered to allow for access of internal currents and voltages at various nodes of the transistor. With access to the current and voltage waveforms at the intrinsic plane it is possible to do a more thorough examination of the model's capability in generating the correct current content at both the gate and drain terminals. As mentioned earlier, the input and output voltage measured waveforms are inserted (and de-embedded) instead of multi-harmonic impedances. The input and output intrinsic waveforms are shown in Fig. 8-4 (a) and (b).

The waveforms shown in Fig. 8-4 (a) and (b) exhibit a greater level of agreement than shown earlier. The input and output voltage swings have increased with a fundamental swing 24.5V_{pk} at the drain (Fig 8-4 (a)) and 3.4V_{pk} at the gate (Fig8-4 (b)). The two gate voltages are shown to overlap each other except at the extreme peaks. The drain voltage waveforms are showing more harmonic content, with signs of some interaction with the device knee, which is approximately 3.5V. The drain current in Fig. 8-4 (a) also shows more harmonic

behaviour than before with the current swing spending less time below 0mA, indicating that the device is biased in class AB. The gate current is still sinusoidal as before but with a slightly smaller amplitude swing.

(a)
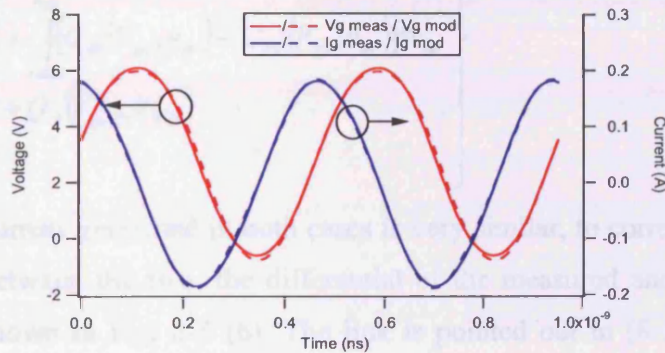
(b)

Fig. 8-4 – (a) Measured and model drain current and voltage waveforms at the intrinsic plane, (b) Measured and model gate current and voltage waveforms at the intrinsic plane

8.5　Further Analysis of the Model's Individual Components

A typical intrinsic device model consists of real and reactive current generators at both the input and output terminals. These current generators are a function of both the input and output voltage content. In the case of Si-LDMOS devices the gate terminal consists of just a charge generator Q_g [18]. This is because of the lack of any diode at the input port, which is commonly found in other device technologies. The difference between the measured and model gate current is always less than 10mA, which is within 2.5% of the peak to peak current swing in Fig 8-4 (b).

For analysis of the drain terminal, the real current is taken as the reference case and subtracted against the measured current at the intrinsic plane, leaving what should be the reactive portion from the measurements as highlighted in (8-8). This is compared against the reactive current generator at the drain port Q_d calculated in (8-10) with the results shown in Fig. 8-5.

$$I_{react-meas} = I_{int-meas} - I_{d-mod} \tag{8-8}$$

$$I_{react-mod} = \frac{d}{dt} Q_d \left(V_{gs0}, v_{gs}, V_{ds0}, v_{ds} \right) \tag{8-9}$$

$$= \frac{d}{dt} \left\{ \begin{array}{l} \int_{Vgs0}^{Vgs} \left[C_m \left(v_{gs}, V_{ds0} \right) - C_{gd} \left(v_{gs}, V_{ds0} \right) \right] dv_{gs} \\ + \int_{Vds0}^{Vds} \left[C_{ds} \left(V_{gs}, v_{ds} \right) - C_{gd} \left(V_{gs}, v_{ds} \right) \right] dv_{ds} \\ + Q_d \left(V_{gs0}, V_{ds0} \right) \end{array} \right\} \tag{8-10}$$

The charge current generated in both cases is very similar, to correlate the slight differences between the two, the differential of the measured and model drain voltages is shown in Fig. 8-5 (b). The link is pointed out in (8-10) where the reactive current generator is shown to be a function of the differential of the drain and gate voltages. The differences in Fig. 8-5 (b) correlate very well with the differences in the charge current and could be one of the sources of error. This provides a high level of confidence in the intrinsic device model for fundamental frequency design procedures.
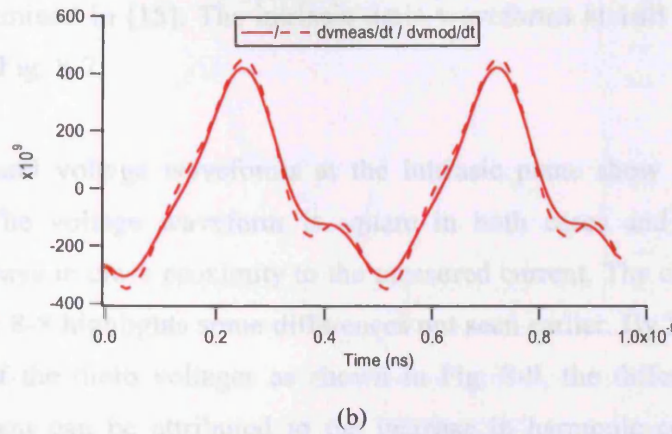

(a)

(b)
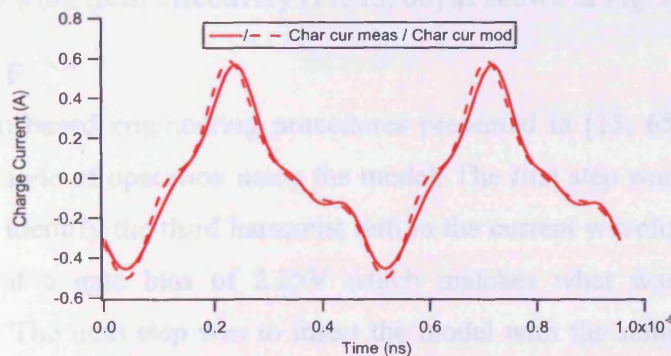
Fig. 8-5 – (a) Measured and model drain charge current waveforms, (b) The differential of the measured and model drain voltages

8.6 The Model's Ability to Conduct High Efficiency Waveform Engineering

As previously demonstrated waveform based engineering procedures are proving to be highly successful in optimizing high efficiency modes of operation [3, 66]. In single device high efficiency modes of operation, efficiency enhancement is achieved through manipulation of the higher harmonic currents and voltages. In this case the high efficiency modes of operation being applied are class F and inverse class F [3, 11, 15-16, 52, 60]. Both of these modes of operation offer high efficiency and high output power but more importantly test the model's flexibility to different drain voltage waveforms. For this to be done, the intrinsic device model was split into the real and reactive current generators allowing for separate assessment of the two current components. This allowed for access to the real current generator where these waveform engineering procedures have been shown to work most effectively [11, 15, 60] as shown in Fig. 8-6.

8.6.1 Class F

The waveform based engineering procedures presented in [15, 65] are applied for a class F mode of operation using the model. The first step was to conduct a bias sweep to identify the third harmonic null in the current waveform. This was found to be at a gate bias of 2.25V which matches what was found with measurement. The next step was to insert the model with the same impedances

as were determined in [15]. The intrinsic drain waveforms at 1dB compression are shown in Fig. 8-7.

The current and voltage waveforms at the intrinsic plane show good overall agreement. The voltage waveform is square in both cases and the model's current is always in close proximity to the measured current. The charge current shown in Fig. 8-8 highlights some differences not seen earlier. By looking at the differential of the drain voltages as shown in Fig. 8-9, the differences in the intrinsic current can be attributed to the increase in harmonic content of the voltage waveform, which the model fails to predict as well as shown earlier.
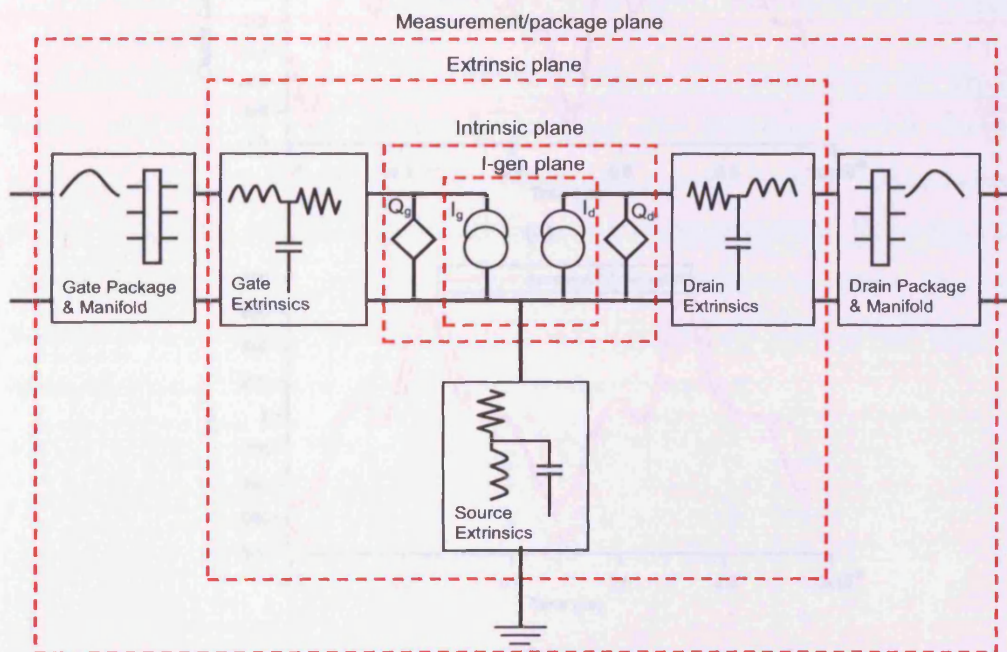
Fig. 8-6 – Block diagram of a FET and the various reference planes accessible for waveform engineering
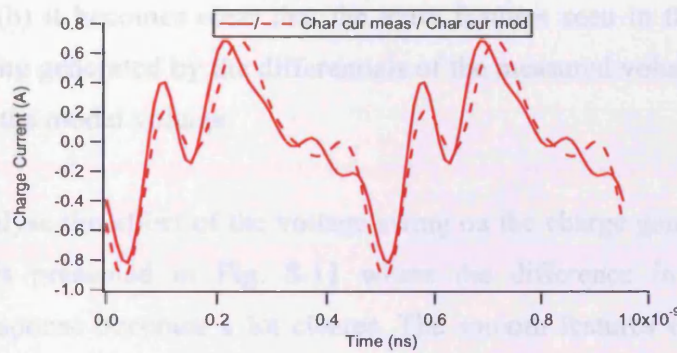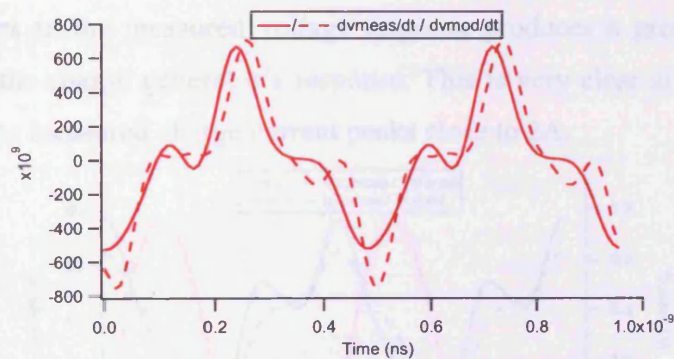
Fig. 8-7 – The measured and model class F drain current and voltage waveforms at the intrinsic plane

(a)

(b)

Fig. 8-8 –(a) Measured and model drain charge current waveforms, (b) The differential of the measured and model drain voltages

8.6.2 Inverse Class F

A similar waveform based procedure was applied to the device [11] through bias and load impedance control. The optimum bias point was found to be 3.6V, which corresponds to the optimum amount of third harmonic current within a limited bandwidth system [52]. The model was inserted into the same

impedances as were determined in measurement. The intrinsic drain waveforms at 1dB compression are shown in Fig. 8-9.

The drain current and voltage waveforms are shown to be in good overall agreement. The model's drain voltage is showing a similar amplitude swing as observed in the measurements but differs in the low voltage region, in particular the interaction with the device knee. The intrinsic drain current is shown to differ because of the difference in behaviour in the low voltage area. By looking at Fig. 8-10 (a) and (b) it becomes clear that the extra features seen in the measured charge are being generated by the differentials of the measured voltage are again not present in the model voltage.

To further analyse the affect of the voltage swing on the charge generator Q_d. A further plot is presented in Fig. 8-11 where the difference in the charge generator's response becomes a lot clearer. The smooth features of the model voltage produce a smooth response in the model's charge current. However, the sharper features in the measured voltage response produces a greater level of fluctuation in the charge generator's response. This is very clear at low voltage levels where the measured charge current peaks close to 2A.
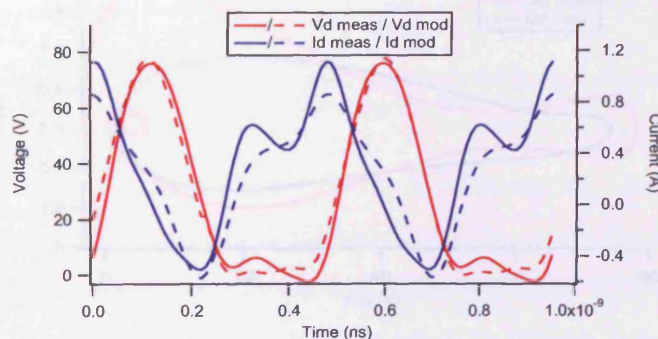
Fig. 8-9 – The measured and model inverse class F drain current and voltage waveforms at the intrinsic plane
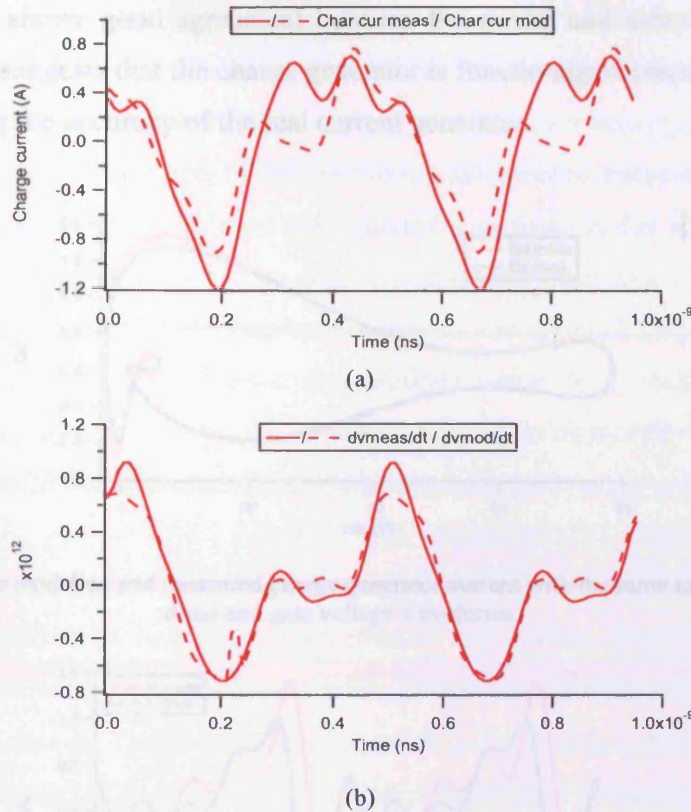
(a)

(b)

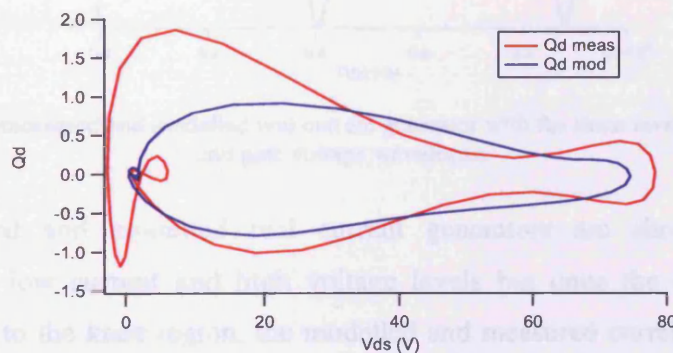Fig. 8-10 – (a) Measured and model drain charge current waveforms, (b) The differential of the measured and model drain voltages

Fig. 8-11 – The measured and modelled drain charge generator (Qd) plotted against the drain voltage (Vds)

The results in Fig. 8-11, further signify the sensitivity of the charge generator's response. One of the possible causes for the voltage variation is likely to be due to the bondwire inductance, which could have had a lower inductance value than that derived for the model. However, to confirm or deny this, the charge generator is exposed to the measured voltage at the intrinsic plane. The response

in Fig. 8-12, shows good agreement between the model and measured charge current. This suggests that the charge generator is functioning correctly and leads to questioning the accuracy of the real current generator.
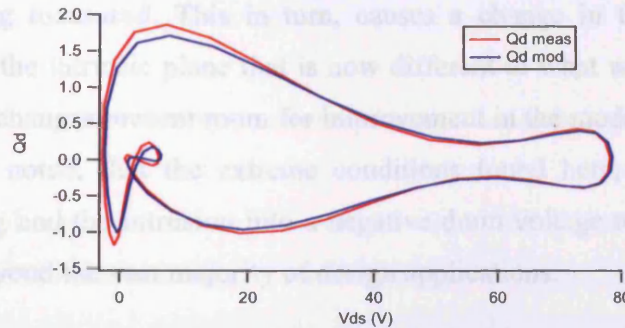

Fig. 8-12 – The modelled and measured charge generator current with the same inverse class F drain and gate voltage waveforms
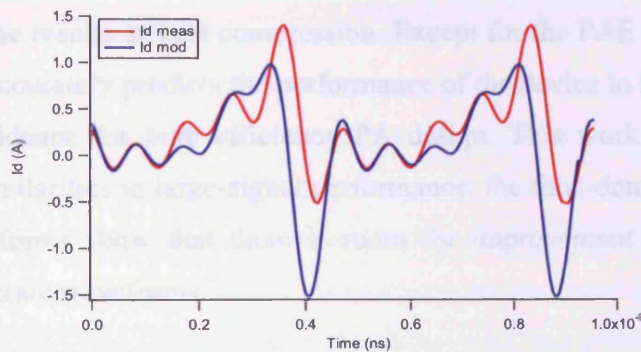

Fig. 8-13 – The measured and modelled real current generator with the same inverse class F drain and gate voltage waveforms

The measured and modelled real current generators are showing similar behaviour at low current and high voltage levels but once the drain voltage swings close to the knee region, the modelled and measured current waveforms start to deviate significantly. The largest deviation in current is in the negative region where the model is predicting a negative current of -1.5A whilst the measured current is around -0.4A. This significant difference in the current waveform identifies the real current generator as the primary cause for the difference in performance observed here.

Now that there has been a difference identified in the two real current generators, the results seen in Fig. 8-9 can be explained more clearly. Despite identical input and output voltage waveforms being applied at the measurement plane the real drain current generator in the model provides a different response than what is actually being measured. This in turn, causes a change in the drain voltage waveform at the intrinsic plane that is now different to what was de-embedded. Whilst these changes present room for improvement in the model's performance, it should be noted, that the extreme conditions found here, such as a large voltage swing and the intrusion into a negative drain voltage region has pushed the model beyond the vast majority of design applications.

The level of agreement in large signal performance between measurements and models is found to be in high in both class F and inverse class F. Table 8-1 summarizes the results at 1dB compression. Except for the PAE in inverse class F the model accurately predicts the performance of the device to allow for a high level of confidence for high efficiency PA design. This work highlights that despite the similarities in large-signal performance, the time-domain current and voltage waveforms show that there is room for improvement in the model's ability to generate waveforms.

	Class F		Class F^{-1}	
	Measured	Model	Measured	Model
Pout (dBm)	35.78	35.68	37.55	37.48
PAE (%)	76.62	74.65	67.34	74.51
Gain (dB)	18.69	20.71	20.12	19.92

Table 8-1 – Summary of high efficiency performance comparison

8.7 Conclusions

CAD based device models are becoming increasingly used and relied upon in the design process to save time and cost. The complexity of models have progressed from linear lumped element based models to complex non linear models that have been verified against realised designs. However, as RF PA designers move into the time domain, these models are now being tested in an unproven domain.

This chapter has successfully verified the use of a charge conservative model within the time domain. Model validation within the time-domain offers a more in depth insight into the model's sensitivity to the input and output voltage stimuli. This allows for an individual assessment of the real and reactive current generators of the intrinsic device model.

To begin with the model was verified using existing techniques to provide the confidence to proceed further. Initially the model current and voltage waveforms were compared against the measured waveforms at the calibrated reference plane with the device biased in class AB. The high level of agreement between the measured and modelled waveforms at the calibrated reference plane was further demonstrated at the intrinsic device plane.

The next step was to proceed into the application of waveform engineering within the CAD domain. The model was operated in class F and inverse class F and verified against measurements. In both modes of operation, the model was able to predict the power and efficiency values in line with the measurements. There was a high level of agreement seen in the class F waveforms with some minor differences observed in both the current and voltage higher harmonic components. However, there were larger differences observed when applying inverse class F operation to the model. These differences were identified to be primarily due to differences in the model's real drain current generator, which had a knock on effect in changing the model's voltage waveform seen at the intrinsic plane. This presents some room for improving the model, but it should be noted that the model was still able to produce large signal results that were in line with those found in the measurements. Nevertheless, despite these minor differences the FET^2 model is shown to be an effective tool in enabling waveform engineering within a CAD environment.

9   Waveform Applications – Waveform Based Doherty Design

This chapter now shifts focus onto waveform engineering of a multiple device based PA. The specific PA architecture being discussed in this case is the Doherty amplifier, which was initially originated in 1936 [13]. Due to the emergence of variable amplitude modulation schemes (GSM-EDGE, IS-95, WIMAX) and increases in requirements of ACPR, EVM and total spectrum mask. The PA has been forced to operate in highly backed off conditions, typically in excess of 6 dB below the 1 dB compression point [3]. This effectively negates the benefits of producing highly efficient amplifiers such as class F and inverse class F previously discussed as they revert back to a more linear, conduction angle based mode of operation. For example, a class F amplifier operating 6 dB backed off will revert to a class B mode of operation. Assuming an ideal device in class B (V_{knee} = 0V), is operated at 6 dB back off the PA efficiency drops from 78 % to 39 %. This drop in efficiency is due to a reduction in the voltage swing that reduces the area being utilised by the dynamic IV. This is further demonstrated in Fig. 9-1(b). There is also a reduction in the current swing, but the DC to RF ratio is always maintained when the device is in linear operation.

Due to the PA being the most significant portion of the transmit system's energy requirements, operating the PA in a less efficient state can severely reduce the overall system efficiency and due to the large amounts of dissipated power, there is also a need for complicated cooling systems to ensure reliable operation of the devices. This then produces a very different requirement not highlighted previously and that is efficiency improvement at lower levels of output power.

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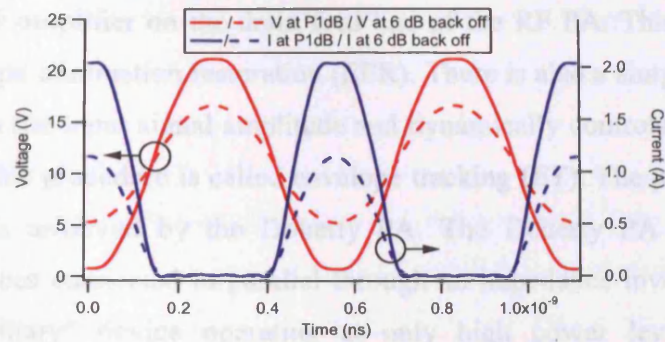
(a)
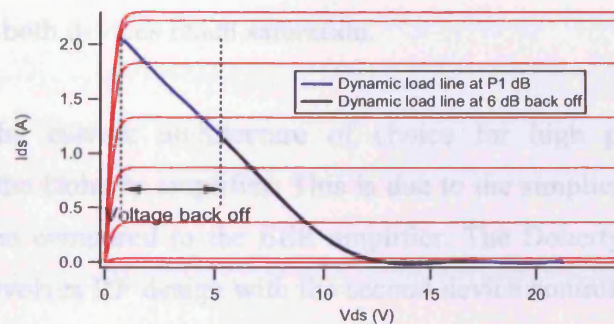
(b)
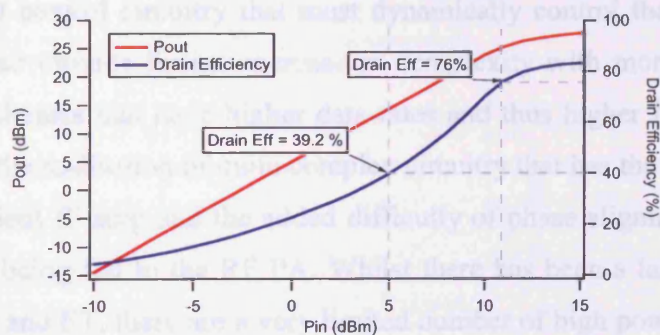
(c)

Fig. 9-1 – (a) Current and voltage waveforms of an ideal device biased in class B at 1 dB compression and at 6 dB back off, (b) Dynamic load line at 1 dB compression and 6 dB back off, (c) Typical power and efficiency performance with input of an ideal device biased in class B

Efficiency enhancement at lower power levels has been a topic of high interest in literature. There are two basic methods in improving efficiency with the drive and these are by dynamically varying the drain bias or by dynamically varying the load impedance presented to the device [3]. Either method maximises the voltage swing to the limits of the IV plane, i.e. the knee region of the transistor. The first method of bias control, measures or extracts the IF component of the input signal amplitude and dynamically alters the bias and/or IF input signal

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through an IF amplifier on the drain feed line of the RF PA. This procedure is called envelope elimination restoration (EER). There is also a simpler derivative that measures the input signal amplitude and dynamically controls the DC drain voltage and this procedure is called envelope tracking (ET). The process of load modulation is achieved by the Doherty PA. The Doherty PA involves two separate devices connected in parallel through an impedance inverter, with the second "auxiliary" device operating at only high power levels and once operational, load modulating the "main" always on device. The end result is a flat gain until both devices reach saturation.

At present the current architecture of choice for high power basestation amplifiers is the Doherty amplifier. This is due to the simplicity of the Doherty amplifier when compared to the EER amplifier. The Doherty amplifier circuit exclusively involves RF design with the second device controlled by adjustment of the gate bias. Whilst EER and ET circuits involve the use of detector circuits and additional control circuitry that must dynamically control the IF and drain DC bias. These circuits further increase in complexity with more complicated modulation schemes that have higher data rates and thus higher IF bandwidths. This leads to the realisation of quite complex circuitry that has the added need of a highly efficient IF amp and the added difficulty of phase alignment to the RF signal before being fed to the RF PA. Whilst there has been a large amount of work on EER and ET, there are a very limited number of high power basestation amplifiers shown to be utilising EER and ET techniques, whilst the Doherty PA has led to many publications [70, 71] and greater use within industry.

This chapter briefly explains the operation of a classical Doherty PA and outlines the current performance being achieved in the literature. The next section looks into the preferred design strategy applied for high power Doherty PAs and examines the behaviour of the PA in terms of current and voltage waveforms. After these observations a waveform based design procedure is applied, where both devices are investigated separately to see how waveforms can facilitate enhanced Doherty design. Finally a brief analysis is given, which identifies the

possible outcome of producing destructive Doherty amplifiers if careful design considerations are not applied.

9.1 Introduction

The classical Doherty amplifier shown in Fig. 9-2 consists of two active devices a "main" and an "auxiliary" connected in a parallel arrangement with outputs that are directly connected via a simple $\lambda/4$ impedance transformer. The intentional interaction can be considered as a form of active load-pull, which has the effect of dynamically modifying the impedance environment presented to both devices. The quarter-wave transformer at the output of the "main" device inverts the load impedance of $R_{opt}/2$ at the structure output to $2R_{opt}$ at the output of the main device. The additional quarter-wave transformer placed before the "*auxiliary*" device provides the required phase alignment that allows the main and auxiliary device contributions to sum in correct phase at the load.
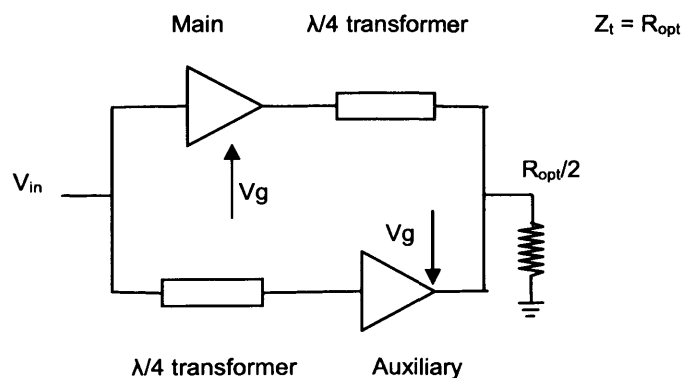

Fig. 9-2 – Schematic layout of a classical Doherty amplifier

The behaviour of the Doherty amplifier can be described in two distinct low and high-power regions of operation, separated by a notional transition point (T_p) shown in Fig. 9-3. The low-power region involves only the main device, which, in the absence of any contribution from the auxiliary device operates into a load impedance environment of $2R_{opt}$. The high-power region begins at the transition point, and extends typically 6dB to the point of maximum power. As power is increased past T_p, the auxiliary device begins to conduct current and actively load-pulls the main device. The overall effect is that the main device experiences

a load impedance that decreases from $2R_{opt}$ towards R_{opt} with increasing input drive, thus producing a constant main device voltage state and an efficiency plateau that extends typically over 6dB of dynamic range. In turn, the auxiliary device sees in an impedance variation from ∞ to R_{opt}. The interaction between the two devices is described in (9-1) to (9-3). There is a more detailed description of the operation of Doherty amplifiers outlined in ref [3, 69, 72].

$$R_{main} = \frac{2 * R_{opt}^2}{R_{opt}\left(1 + \frac{I_2}{I_1}\right)} \qquad \text{when } Z_t = R_{opt} \qquad (9\text{-}1)$$

$$R_{aux} = \infty \qquad 0 < Pin < Pin, \text{max}/4 \qquad (9\text{-}2)$$

$$R_{aux} = R_{opt}\left(1 + \frac{I_{main}}{I_{aux}}\right) \qquad P_{in, \text{max}}/4 < P_{in} < P_{in, \text{max}} \qquad (9\text{-}3)$$
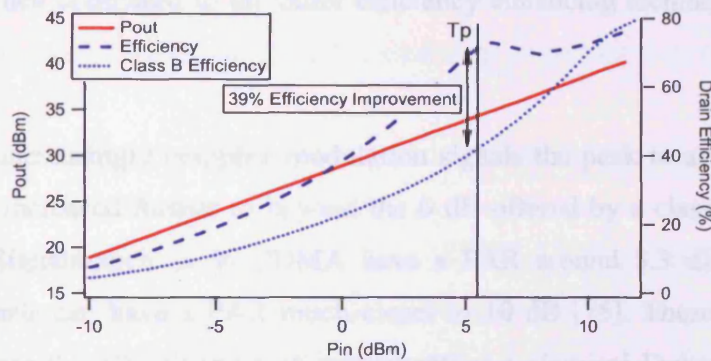

Fig. 9-3 – Output power and efficiency plotted against input power

The typical performance of an ideal Doherty amplifier is shown above in Fig. 9-3 where there is a linear increase in output power with drive and an efficiency plateau for the highest 6 dB of operation. When compared with the efficiency performance of a single device in class B there is an efficiency improvement of 39% at 6 dB back off in input drive. One potential imperfection in Doherty amplifiers are the performance requirements of the auxiliary device. Due to the delayed turn on requirements of the auxiliary device, the device is typically biased much below threshold in a deep class C bias. However, the consequence of biasing in class C is a reduction in peak output current and gain at the

fundamental. To overcome this, the auxiliary device is forced to be larger in size, which poses several problems in solid-state designs, where a separate matching network will have to be designed using a separate set of load pull data, which increases cost, complexity and time in the design process. There have been several possible methods proposed to overcome these features, such as separately controlling the input power of the two devices [3] or by adjusting the gate voltage of the auxiliary to control the output current of the auxiliary [72, 73]. However, both of these techniques require the use of actively monitoring and controlling components, which increase the overall complexity of the Doherty amplifier. A third technique more commonly used in high power applications is the use of an asymmetric input power splitter, which is designed to increase the input power to the auxiliary [74]. This helps overcome the gain drop when biased in class C at a cost in the overall gain of the entire amplifier. Another benefit of this approach is that it maintains the simplicity of the Doherty amplifier when compared to the other efficiency enhancing techniques outlined earlier.

Due to the increasingly complex modulation signals the peak to average (PAR) ratios have increased further to beyond the 6 dB offered by a classical Doherty amplifier. Signals such as W-CDMA have a PAR around 8.3 dB and newer OFDM signals can have a PAR much closer to 10 dB [75]. These larger PAR signals reduce the effectiveness of implementing a classical Doherty PA since the majority of the signal will be applied with just the main device in operation and operating below its saturating point. To overcome this, there are two distinct implementations, both functioning by extending the load modulation of the main device to a value higher than the $2*R_{opt}$ used originally [76]. These procedures can extend the dynamic range to a much larger extent than the 6 dB initially shown. However, both methods increase the role of the auxiliary in producing the required load modulation and in producing the peak output power.

This first method expands the dynamic range of Doherty amplifier by increasing the size of the auxiliary device. Due to the increased impedance modulation of

the main device ($>2*R_{opt}$ to R_{opt}), the auxiliary device needs to provide a much larger amount of current to load pull the main device down to the optimum impedance R_{opt}. This puts the requirements of the auxiliary device to not only have a larger gain than the main device to provide the gain expansion, but to now also have a higher peak output current. This higher peak current output combined with the same voltage swing, delivers a combined output power that is greater than the classical Doherty amplifier. The first successful demonstration of this was done in [77] and the theory has been further outlined in [73] and [76]. Whilst, this method has been successfully demonstrated at low power levels, the extension of this procedure at high power levels has been limited. For example, a classical Doherty amplifier with a combined output power of 200W will require two single 100W devices. If the same main device of 100W is utilised and the dynamic range is increased to 9 dB, the auxiliary device size is forced to increase to 200W. If a 12dB dynamic range of efficiency enhancement is preferred, the auxiliary device increases to 300W and this is assuming that the auxiliary device is already compensating for the expected gain drop when biased in class C.

The second method of extending the Doherty amplifier's dynamic range has been demonstrated by attaching extra "auxiliary" devices to the classical Doherty. This is best explained as an example, where the amplifier functions in three different modes of operation. The first being at low power, where the main device is operational and the two auxiliary devices are turned off. The medium power region where the first auxiliary power amplifier is turned on and load modulation starts to occur and a high power region, when the second auxiliary device turns on [78]. There have been some successful attempts in 3-way Doherty amplifiers but with mixed results, some have shown improvements in linearity [79] but no great improvement in efficiency, whilst others have successfully managed to increase the dynamic range but with increased complexity [80].

The current state of the art performance in Doherty amplifiers depend on the output power levels and semiconductor device's being utilised. In the majority of

high power Doherty amplifiers for basestation applications, the benchmark for performance is around 40 % drain efficiency at the mean output power level (depending on the modulation scheme applied e.g. 7 dB from Pmax for CDMA) [23]. This is using high power Si LDMOS devices, where a single device, will have peak drain efficiency around 50% when biased in class AB. With the emergence of high power GaN devices, higher mean efficiencies greater than 50% have been achieved [81]. However, due to relative ease in linearising Si LDMOS based devices when compared to GaN, there has been limited up take of GaN devices in the commercial domain. The next section outlines the design of a high power Doherty amplifier using current design techniques and links these load pull based designs with waveforms.

9.2 Design of a High Power Doherty Amplifier

9.2.1 Design Procedure

The Doherty amplifier being designed is for a 6 dB enhancement of efficiency with drive and is done using the Cardiff LUT model [68, 82], which is a measurement based model of a device utilising vector based data for complete capture of the current and voltage waveforms. The measurements were conducted using the high power measurement system developed at Cardiff University [17]. The device being used is a 100W Si LDMOS device developed for 3G UMTS band operation and the measurements were collected at 2.15 GHz.

Before starting the Doherty matching network design, a brief investigation of the main device and its performance variation with load and input drive has to be done. Below is a plot of the output power contours with reducing input drive, showing the optimal impedance transition for a linear increase in output power. What Fig. 9-4 shows, is that the impedance trajectory is away from the real axis and to compensate for this a matching network will be required transform the complex impedance into a real impedance, where Doherty operation can occur. A second point worth noting is the impedance movement the matching network is required to accommodate over 6dBs of input drive.
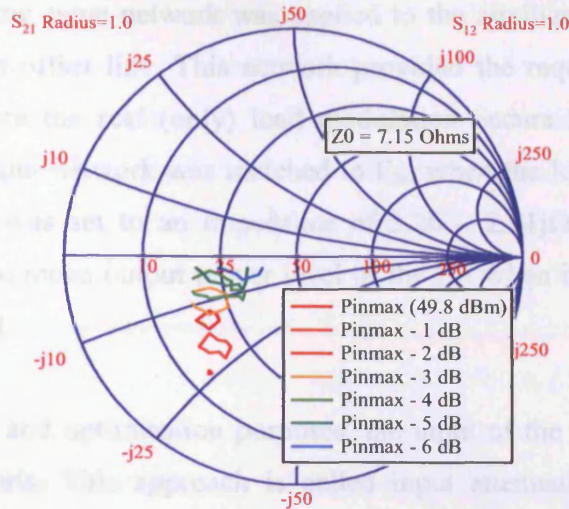
Fig. 9-4 – Peak output contours with varying input drive

The two points of interest are the impedances for peak output power at peak input power and peak power added efficiency at 6dB back off. Based on the analysis of an ideal device [572], the main device has to provide a 3 dB increase in output power once the auxiliary device is in operation. This additional information provides a basis of locating the two boundary impedance values between which the main device impedance modulates. The impedances for the two points of interest are shown in Table 9-1. The job of the matching network is to match the real only impedance where the Doherty load modulation is occurring, to the impedances outlined in Table 9-1. The matching network was designed as outlined in [74] using ideal transmission lines of characteristic impedance 7.2Ω and an offset line of 55.04°. Using this matching network design process, it was observed that the matching network was unable to match to the required low power impedance point. The closest impedance achieved and expected performance is appended in the last row of Table 9-1.

Pin	Impedance	Pout (dBm)	Gain (dB)	PAE (%)
Pin max	$2.01 - 3.31j\Omega$	49.74	15.54	49.35
Pinmax – 6dB	$3.72 - 0.89j\Omega$	46.80	18.51	51.38
Pinmax – 6dB M/N	$3.26 - 2.01j\Omega$	46.99	18.75	48.89

Table 9-1 - The impedances and performance at peak output Power and 6dB back off

As a start point the same network was applied to the auxiliary device, with no adjustment in the offset line. This network provided the required open circuit condition at where the real (only) load modulation occurs for ideal Doherty operation. The input network was matched to Γ_{in}, when the load impedance for the main device was set to an impedance of $3.26 - 2.01j\Omega$. This impedance corresponds to the mean output power level of the PA when inserting a CDMA based input signal.

For investigation and optimisation purposes, the input of the Doherty has been split into two ports. This approach is called input attenuation and has been originally proposed by Lees et. al, in [72]. A block based diagram of the Doherty amplifier is shown in Fig. 9-5. To take advantage of the two input ports, the Doherty amplifier will be implemented using the input attenuation mode of operation [3]. Input attenuation works by controlling the input power delivered to the auxiliary device. The benefit of this method is that the auxiliary device can be of the same size as the main device due to the flexibility in the input power, which can be altered to suit the auxiliary bias setting applied. Other potential benefits, could be a more detailed understanding of the AM-PM effects of each individual device and their effect on the overall behaviour of the Doherty amplifier [73].
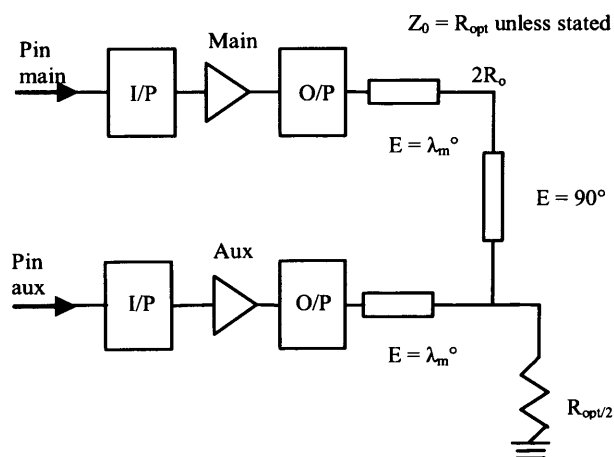

Fig. 9-5 - Schematic of a complete high power Doherty PA with 2 independent input ports

The designed Doherty was then simulated within ADS with the main device biased in deep class AB (I_{dq} = 950mA) and the auxiliary device biased in class B (I_{dq} = 0mA). The input power of the main device was set to increase linearly and the transition point (Tp) at which the auxiliary device turned on was set to 28.2dBm. The input drive of the auxiliary was set to increase in a quadratic mode as outlined in [3]. The first step was to optimise the offset line in terms of efficiency and this was updated to 40.3°. This was required because of the unaccounted effect of the drain output capacitance of both devices. The results are shown in Fig. 9-6.

9.2.2 Results

The initial results show that the there is a plateau region of 4.3dB with a drain efficiency above 50%, 52.4dBm total output power and 1.7dB gain compression. This confirms that Doherty operation has been achieved in this simulated PA. Also this Doherty PA produces a 14% increase in drain efficiency when compared to a single device operating in class AB for a peak to average envelope of 6.5dB. The gain profile shows a variation of approximately 1.5 dB, but there is a sharp deviation at around 30 dBm input drive, which is when the auxiliary device starts to have a more significant effect on the overall performance of the Doherty PA.
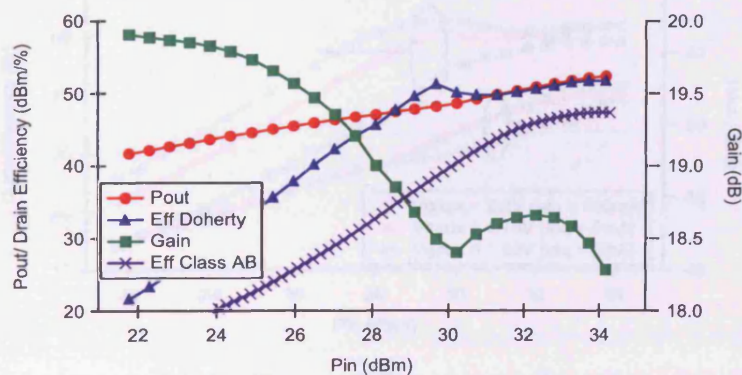

Fig. 9-6 - Output power, drain efficiency and gain of the simulated Doherty power amplifier

To further analyse the interaction of the two devices, the load impedance movement was tracked with input drive and this is shown in Fig. 9-7. The main

device is shown to start at the impedance provided by the matching network at back off and then move towards Z_{opt} in small steps with increasing drive. For the auxiliary device, the device sees an open circuit at low power levels and then proceeds towards Z_{opt} in very large steps at first and then smaller steps at higher input drive levels. However, it should be noted that the LUT model used here is extrapolating beyond its original measured impedance region. This can also explain for the heavy kink shown in the gain in Fig. 9-6.
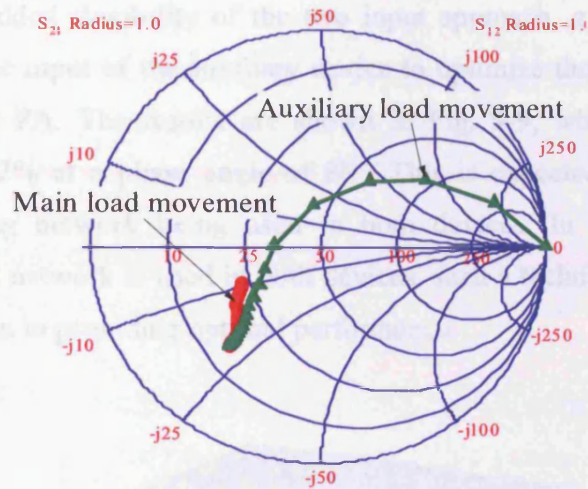
Fig. 9-7 – Impedance movement seen by the main and auxiliary device within a Doherty amplifier with increasing input drive
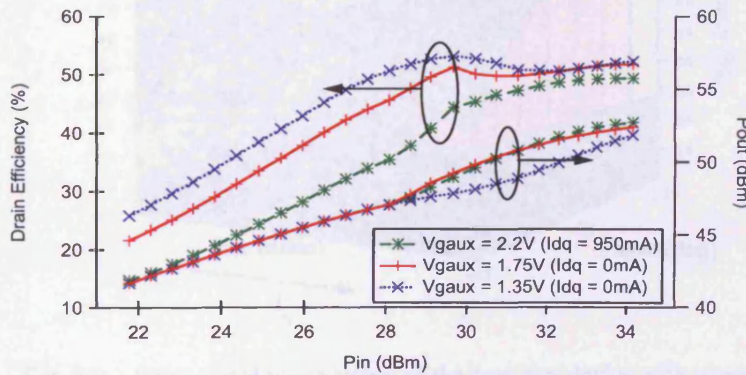
Fig. 9-8 - Output power and drain efficiency performance variation with varying gate bias on the auxiliary

The next step taken was to conduct a gate bias sweep of the auxiliary device and examine its effect on the Doherty PA, the results are shown in Fig. 9-8. As the gate bias of the auxiliary is changed to $V_g= 1.35V$ ($I_{dq}= 0mA$ class C), there is an

increased region of 6.5dB input dynamic range where a high efficiency above 50% is achieved but this comes at the price of a larger amount of gain compression and a lower total output power of 52dBm. The opposite occurs when the gate bias is increased to a deep class AB bias of $V_g= 2.2V$ ($I_{dq}= 950mA$). This produces a lower efficiency profile, which is 38% at T_p but manages to provide 52.7dBm output power which is double the output power of a single device. Out of the three bias settings shown, $V_g= 1.75V$ ($I_{dq}= 0mA$) is showing to be a good compromise of high efficiency and high output power.

To show the added flexibility of the two input approach, a phase sweep was conducted at the input of the auxiliary device to optimize the overall efficiency of the Doherty PA. The results are shown in Fig. 9-9, which shows a peak efficiency of 52% at a phase angle of 88°. This is expected due to the same output matching network being used in both devices. In the case where a different output network is used in both devices, such a technique could provide vital information in providing optimal performance.
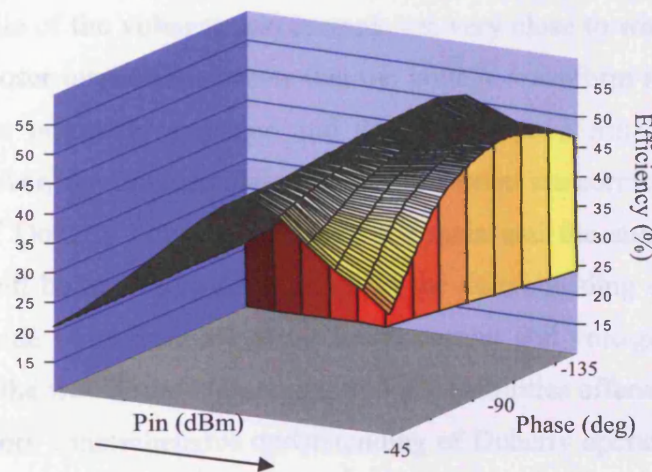

Fig. 9-9 – Input signal phase sweep of the auxiliary device with power

The next step is to analyse the current and voltage waveforms. This is done by utilising the LUT model's potential for high power waveform design. However, before that can be done, it is necessary to incorporate large signal de-embedding. As outlined in Chapter 4, the measured current and voltage waveforms are

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significantly altered due to the presence of large parasitic components in the package and the device. To overcome this the waveforms, are de-embedded using the device package parasitic derived for a 100W Si LDMOS network and the simulation based technique of extracting the current and voltage waveforms at the I-gen plane described in Chapter 4, to provide a means of assessing the true behaviour of the Doherty PA. The results are shown in Fig. 9-10.
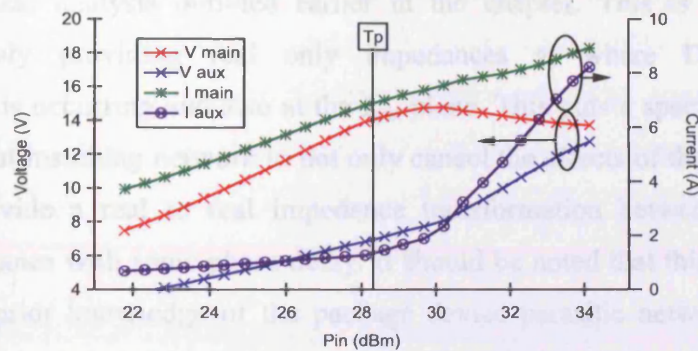

Fig. 9-10 – The fundamental voltages and currents of the main and auxiliary device in Doherty operation for half the device at the I-gen plane

Fig. 9-10 shows the fundamental voltage and current components with input drive. The profile of the voltages and currents are very close to what is required in theory. A closer inspection reveals that the voltage waveform is not as large in magnitude as originally expected and the current waveform is larger than expected. However, the fundamental voltage and current are correctly indicating the presence of Doherty behaviour in both the main and the auxiliary device. Further work will be necessary to improve on the de-embedding of these large devices to provide more accurate and reliable current and voltage waveforms, thus improving the waveform engineering design capabilities offered by the LUT model. For a more comprehensive understanding of Doherty operation based on current and voltage waveforms, a similar analysis is conducted on the 10W Si LDMOS device, where this package de-embedding problem as described in Chapter 5 has been fully addressed.

9.3 Waveform Based Doherty Design

9.3.1 Design Outline

Consider now the waveform based investigation of a Doherty PA, again using the Cardiff LUT model, now based on a 10W Si LDMOS device. This will produce a 20W Doherty PA that could be utilised within the smaller "femto" cells. In this case the design process has been altered to provide more correlation with the ideal analysis outlined earlier in the chapter. This is achieved by synchronously providing real only impedances at where Doherty load modulation is occurring and also at the I_{gen} plane. This puts a specific emphasis on the output matching network to not only cancel the effects of the package but to also provide a real to real impedance transformation between these two reference planes with some phase delay. It should be noted that this can only be done with prior knowledge of the package device parasitic network. A block diagram of the proposed output schematic is shown in Fig. 9-11.
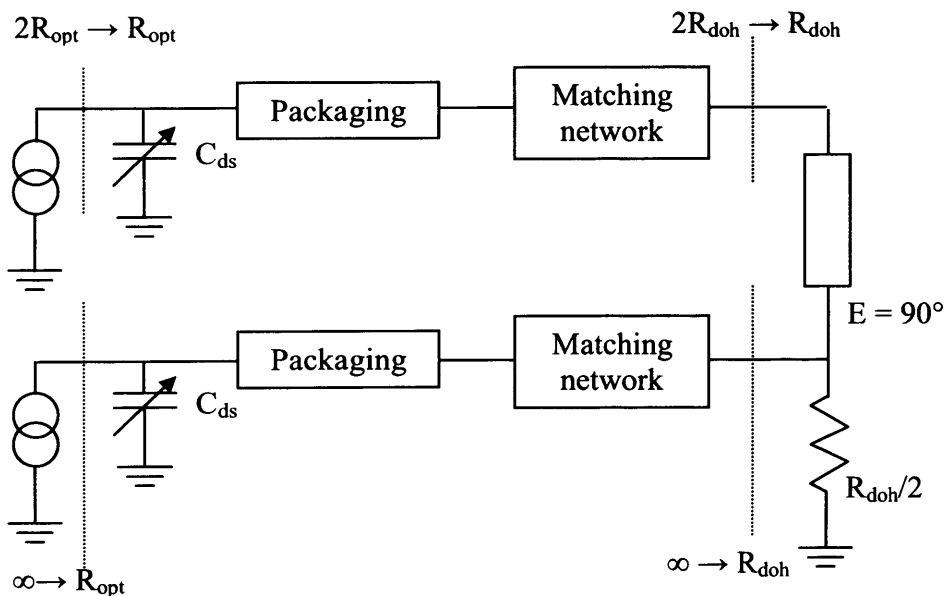

Fig. 9-11 – Output schematic of waveform based Doherty PA

With prior knowledge of the package network, it is possible to derive the required impedance route with input drive for both the main and auxiliary

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devices. The real to real impedance transformation requirements of the output matching network are shown in Fig. 9-12. Using this information the output matching network was designed at 2.1 GHz within ADS. Due to the limited availability of measurement data for processing the LUT model, both devices were biased in class AB and implemented as a two input Doherty PA using the input attenuation method outlined earlier. After analysing measured data, it was found that the device had a P1dB at approximately 8.5W of output power. This means that the 20W Doherty PA has to be revised down to 17W to ensure there is minimal voltage clipping of the main device, ensuring optimal Doherty operation [72].
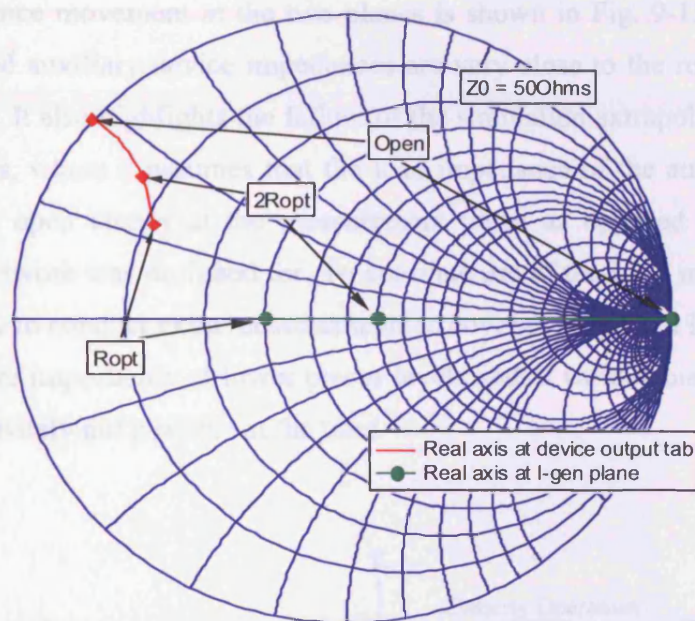

Fig. 9-12 – Impedance transformation requirements of the matching network at the package plane

9.3.2 Results

The simulated results are shown in Fig. 9-13. The results show a region of high efficiency for the top 5 dB of input drive. Below this the auxiliary device is having to rely upon the extrapolation algorithm of the simulator and this is clearly showing to have an adverse effect on the results at lower power levels. Focussing in the period where the simulation is functioning, the complete

Doherty PA delivers 42.3 dBm (17W) of output power with a peak efficiency of 55 % and less than 1 dB of gain compression. At 5dB back off the efficiency is slightly below 50 %.

The dynamic I-V load lines at the I_{gen} plane are shown in Fig. 9-14, where the main voltage swing is fixed in (a) with the current swing increasing at high input drives. In turn the auxiliary device shows an increase in both current and voltage with input drive. With deeper analysis of the auxiliary loadlines, it can be seen that the gradient (i.e. inverse of the load impedance) is becoming steeper, which correctly indicates that the auxiliary device impedance is following Doherty theory. At peak power, the main and auxiliary devices have identical waveforms. The impedance movement at the two planes is shown in Fig. 9-15, where both the main and auxiliary device impedances are very close to the real axis of the Smith chart. It also highlights the failure of the simulation extrapolation at lower power levels, where it assumes that the load impedance of the auxiliary device tends to an open circuit at the measurement plane as opposed to where the matching network was designed for. To continue use of the LUT model it would be necessary to conduct extra measurements to cover the expected impedances of use and more importantly at lower power levels and at various bias levels. This was unfortunately not possible at the time.
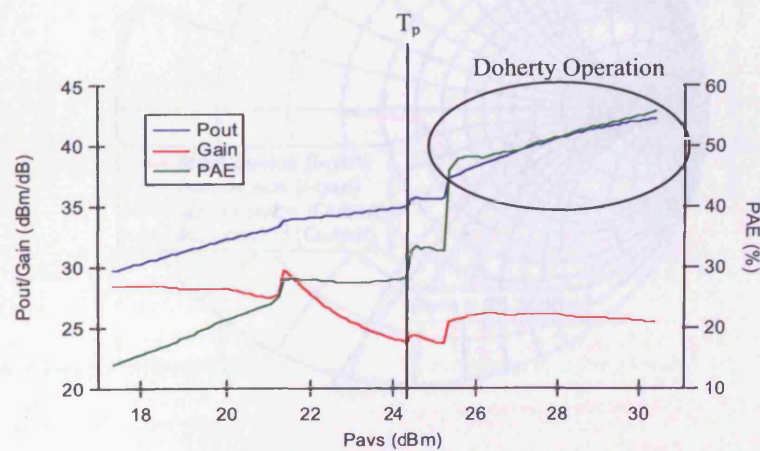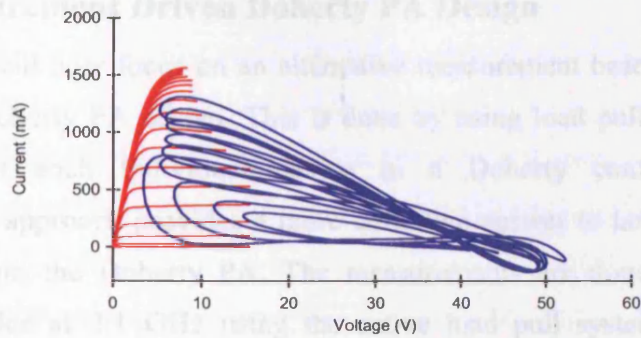

Fig. 9-13 – Simulated output power, power added efficiency and gain of the 17W Doherty amplifier

(a)

(b)

Fig. 9-14 – Simulated dynamic load lines at the I_{gen} plane for the (a) main and (b) auxiliary devices within a Doherty configuration
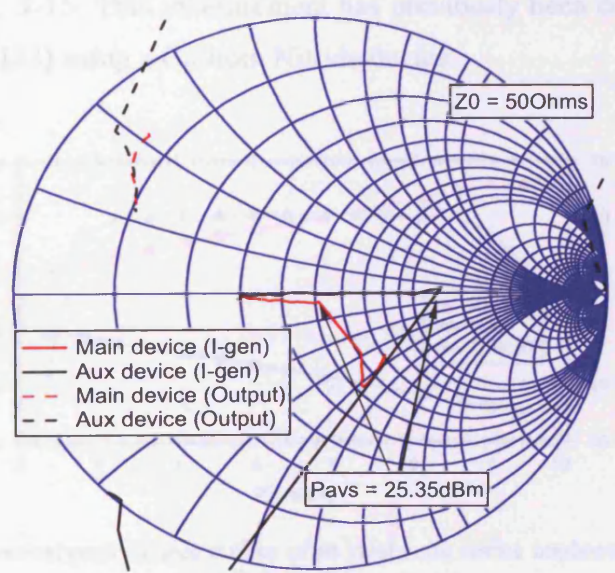

Fig. 9-15 –Simulated impedance movement of the main and auxiliary devices at the output and I_{gen} planes

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9.4   Measurement Driven Doherty PA Design

The chapter will now focus on an alternative measurement based technique for optimising Doherty PA design. This is done by using load pull to emulate the conditions of each individual device in a Doherty configuration. The measurement approach provides a more definitive answer to how a device will function within the Doherty PA. The measurements are done on a 5 W Si LDMOS device at 2.1 GHz using the active load pull system developed at Cardiff. The analysis will concentrate at the fundamental frequency of operation with the second harmonic set to a short circuit at the I_{gen} plane. The focus will start on the main device and then proceed on to the auxiliary device. The analysis will focus on the peak 6dB of input drive of a classical Doherty PA.

9.4.1   Main Device

This measurement involves using the load pull system to enable optimal Doherty operation of the main device i.e. maintaining a constant voltage swing with increasing current swing. Focussing solely on just the main device, this would produce a region of constant efficiency and a constant gain reduction of 0.5 dB per 1 dB increase in input drive leading to a total of 3 dB gain compression. This is outlined in Fig. 9-16. This measurement has previously been conducted at an on-wafer level in [83] using a Gallium Nitride device.
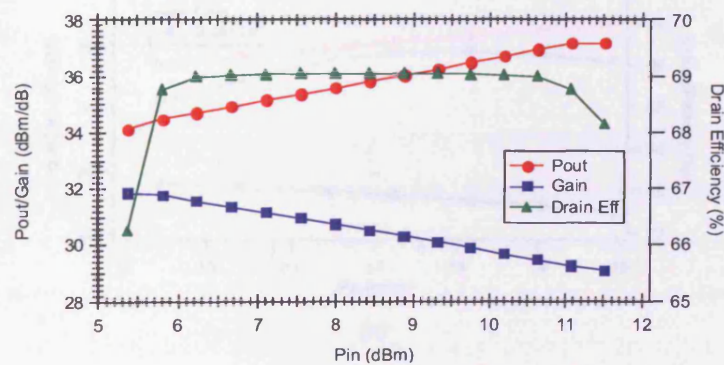

Fig. 9-16 – Theoretical performance outline of an ideal main device implemented within a Doherty PA

9.4.1.1 Results

The power performance and dynamic load lines are shown below in Fig. 9-17 (a) and (b). The device maintains a constant efficiency of 60 % for the top 4 dB of input drive but starts to lose efficiency at lower power levels. The gain of the device drops by 2.5 dB in total. By looking at the dynamic load lines it becomes clear that the efficiency drop at lower power levels is due to the lack of current clipping at higher voltages and the reduction in voltage swing. The reduction in voltage swing is due to a drop in gain. Due to the non-ideal gain characteristics of the Si LDMOS transistors, it is not possible to produce the same dynamic gm at various load impedances. In this case as the load impedance increases the transistor produces a drop in gain of 0.5 dB when compared to an ideal transistor. There could be some compensation applied, either by reducing the dynamic range within optimal Doherty operation is applied or by increasing the load modulation to a value higher than $2*R_{opt}$ over 6 dB. In turn the current swing is seen to double over the 6 dB of operation shown in Fig. 9-17 (b) with a peak current output below 700 mA (0.39 A RMS), which is 100 mA below the peak output current of the device. This reduction in current gives the auxiliary device a change to match the current output of the main device despite being in a class C bias.
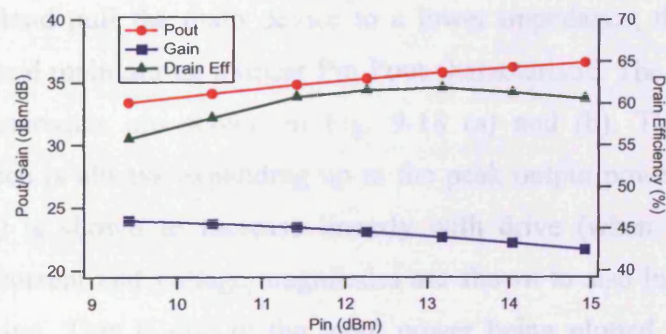

(a)
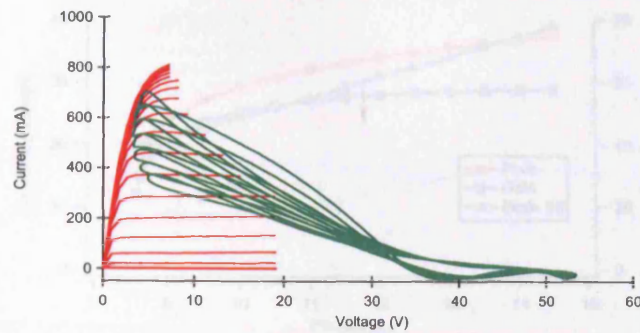
(b)

Fig. 9-17 – (a) Power performance of the emulated main device (b) Dynamic load lines at the I_{gen} plane of the emulated main device
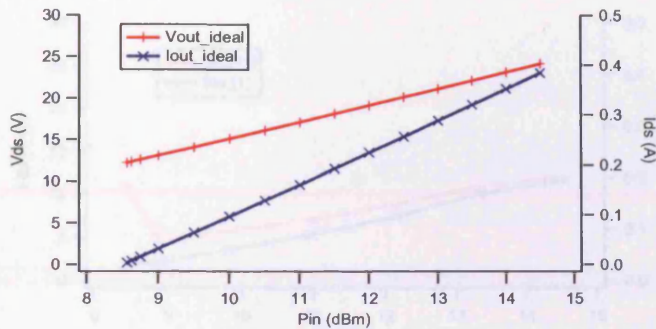
9.4.2 Auxiliary Device

The same measurement approach is now applied to the auxiliary device. In this case changing the impedance from an open circuit (at the I_{gen} plane) to R_{opt} over 6 dB of input drive. The approach taken here is now based on a classical Doherty amplifier rather than input attenuation as discussed earlier in the simulations. This has been done to mimic the design process applied in practical Doherty amplifiers, where the simplicity of a passive power splitter has been preferred whilst also keeping the same transistor used for the main.

As mentioned before, the role of the auxiliary device is to provide the current necessary to load pull the main device to a lower impedance, thus preventing compression and maintaining a linear Pin-Pout characteristic. The ideal auxiliary device characteristics are shown in Fig. 9-18 (a) and (b). The gain of the auxiliary device is always expanding up to the peak output power required and the efficiency is shown to increase linearly with drive (when in dBm). The fundamental current and voltage magnitudes are shown to also increase linearly with input drive. This is due to the input power being plotted in logarithmic form. As stated earlier, an identical main and auxiliary device will not produce a fully functioning Doherty amplifier, so the amplifier will be "tweaked" in terms input drive and gate bias until an optimum solution can be achieved. For device safety and measurement accuracy purposes the open circuit measurement will be conducted at an impedance of 300 Ω at the I_{gen} plane.
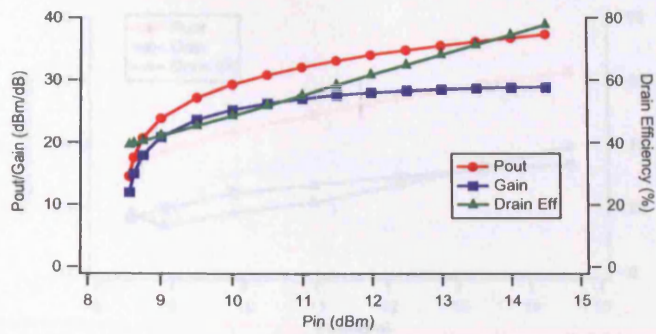
(a)

(b)

Fig. 9-18 – Theoretical performance outline of an ideal auxiliary device implemented within a Doherty PA in terms of (a) power performance (b) voltage and current at the fundamental

9.4.2.1   Results

As a start point, the device was operated with no modifications and according to classical Doherty theory, i.e. identical input drive as the main and biased in class C to turn on at the transition point. In this case the input voltage at T_p was 0.81 V_{pk} with a pinch off voltage of 2.22 V. Using the equation outlined in (9-4), this set the gate voltage to 1.41 V. The results are shown in Fig. 9-19.

$$V_{gs} = V_{th} - V_{inTp} \qquad\qquad\qquad (9\text{-}4)$$

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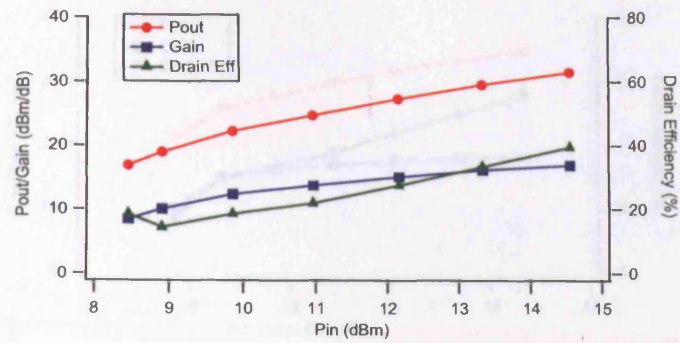
(a)
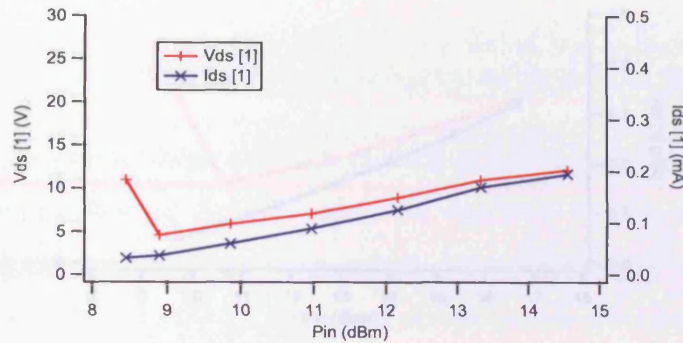
(b)

Fig. 9-19 – Performance of the emulated auxiliary device when biased in class C and with the same input drive as the main device (a) power performance (b) fundamental voltage and current at the I_{gen} plane

As expected, when implemented in this way, the auxiliary device does not provide the current required to load pull the main device. The voltage and current output at the fundamental is shown to be less than half of what is shown in Fig. 9-18. There is a discrepancy in the voltage swing at low power levels and that is due to the combination of a small amount of current present at the lowest power level and a high impedance being presented at the fundamental. However, the profile of the output power, efficiency and gain performance closely matches to what is required in theory. The next step taken is to insert an asymmetric power split. This is done in two stages, with a 1:1.5 split and a 1:2 split. In both cases the split is taken into account from the start and the power is then stepped up in 1 dB steps. The results for the 1:1.5 split are shown in Fig. 9-20 and the results for the 1:2 split are shown in Fig. 9-21.

154
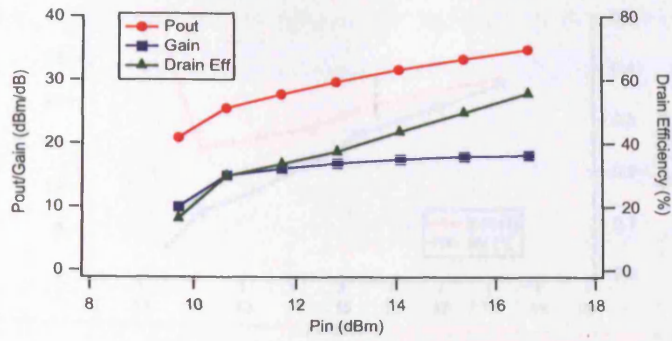
(a)
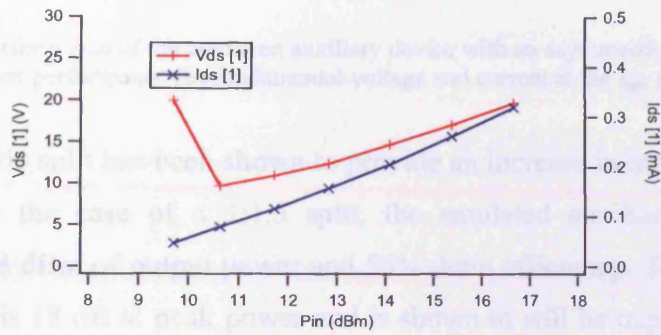
(b)

Fig. 9-20 – Performance of the emulated auxiliary device with an asymmetric split of 1:1.5 (a) power performance (b) fundamental voltage and current at the I_gen plane

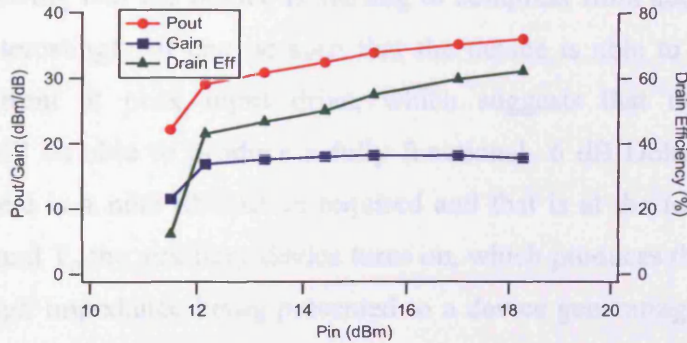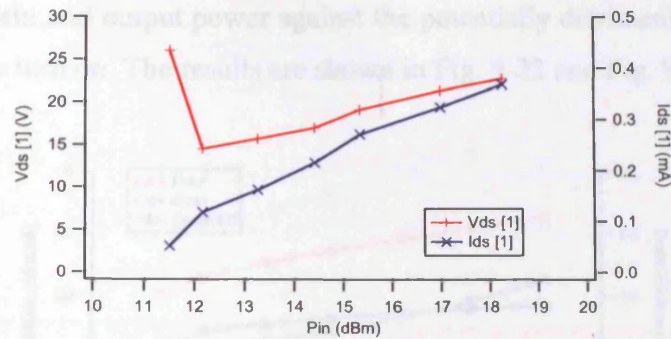(a)

155

(b)

Fig. 9-21 – Performance of the emulated auxiliary device with an asymmetric split of 1:2 (a) power performance (b) fundamental voltage and current at the I_{gen} plane

The asymmetric split has been shown to provide an increase in output power and efficiency. In the case of a 1:1.5 split, the emulated auxiliary amplifier is providing 34.8 dBm of output power and 56% drain efficiency. The gain profile of the device is 18 dB at peak power and is shown to still be expanding at peak input drive. However, the current output of the device does not quite reach the requirements of the auxiliary amplifier. The 1:2 asymmetric split provide 36 dBm of output power and has a peak efficiency of 62%. However, the gain profile is showing that the device is starting to compress from about 2 dB back off. More interestingly, it can be seen that the device is able to produce 0.35 A_{RMS} of current at peak input drive, which suggests that these auxiliary conditions will be able to produce a fully functional 6 dB Doherty amplifier. However, there is a note of caution required and that is at the low input drive level. At around T_p the auxiliary device turns on, which produces the undesirable event of a high impedance being presented to a device generating current. This results in the generation of large voltage swings at the fundamental. In this case, a voltage swing of 24 V is not detrimental to the device but it is possible to envisage similar scenarios where higher voltage swings can be generated.

To further optimise the auxiliary device, the next step is to analyse the effect of increasing the gate voltage on the overall performance. These measurements are implemented with a symmetrical split at the input drive. The measurements are conducted at V_{gs} = 1.61 V and V_{gs} = 1.81 V. The expected effect will be an

increase in gain and output power against the potentially detrimental situation of earlier device turn on. The results are shown in Fig. 9-22 and Fig. 9-23.

(a)

(b)

Fig. 9-22 – Performance of the emulated auxiliary device at a gate voltage of 1.61 V (a) power performance (b) fundamental voltage and current at the I_{gen} plane

(a)

157
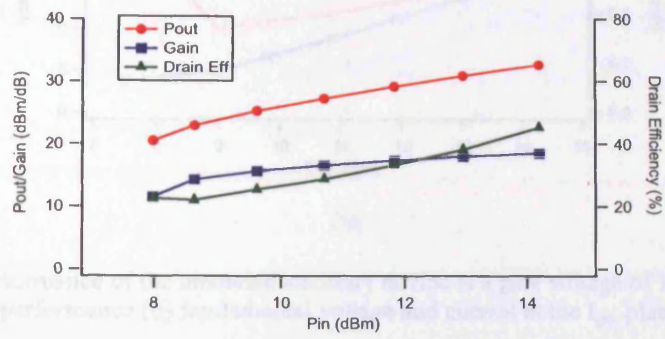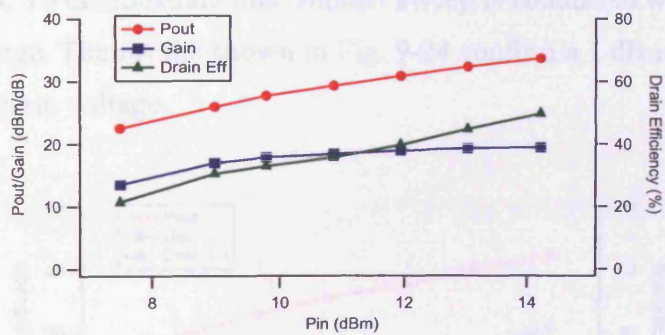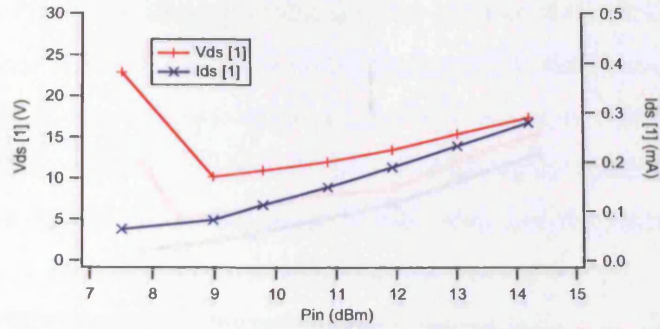
(b)

Fig. 9-23 – Performance of the emulated auxiliary device at a gate voltage of 1.81 V (a) power performance (b) fundamental voltage and current at the I_{gen} plane
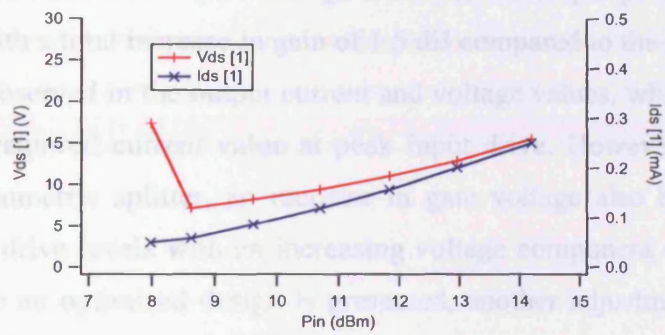
In both cases an increase in gate voltage increases the output power and gain of the device, with a total increase in gain of 1.5 dB compared to the reference case. This is also observed in the output current and voltage values, which are tending towards the required current value at peak input drive. However, as observed with the asymmetric splitter, an increase in gate voltage also has an adverse effect at low drive levels with an increasing voltage component at high current levels. Before an optimised design is presented, another adjustment is made in terms of the drain voltage, which is being increased to 32 V. In theory, this should provide no benefit in terms of performance but due to a finite output conductance, the device's characteristics improve in terms of the gm at higher drain voltages. To demonstrate this, another sweep is conducted with an adjusted impedance range. The results shown in Fig. 9-24 confirm a 1 dB increase in gain at the higher drain voltage.

(a)

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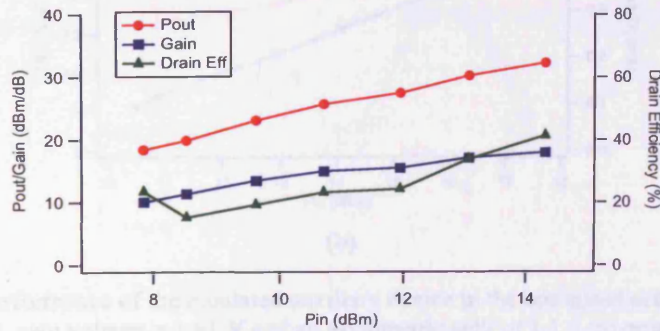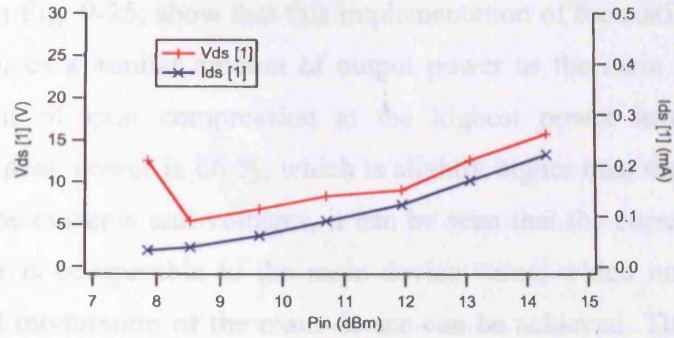
(b)

Fig. 9-24 – Performance of the emulated auxiliary device at a drain voltage of 32 V (a) power performance (b) fundamental voltage and current at the I_{gen} plane

This now leads to the optimised result, which will have a combination of the three factors to produce the required performance. The combination applied here will be a drain voltage of 32 V, a gate voltage of 1.61 V and an asymmetric split of 1:1.5. The results are shown below in Fig. 9-25.
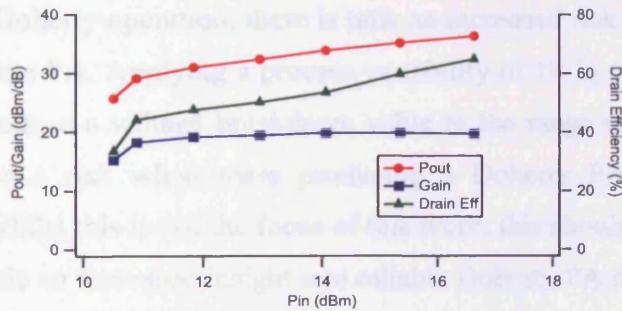
(a)
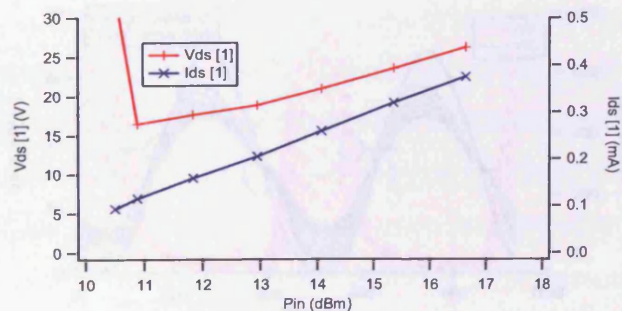
(b)

Fig. 9-25 – Performance of the emulated auxiliary device in the optimised settings of a drain voltage = 32 V, gate voltage = 1.61 V and an asymmetric split of 1:1.5 (a) power performance (b) fundamental voltage and current at the I_{gen} plane

The results in Fig. 9-25, show that this implementation of the auxiliary device is able to produces a similar amount of output power as the main device with a small amount of gain compression at the highest power level. The drain efficiency at peak power is 66 %, which is slightly higher than the main device. Examining the currents and voltages, it can be seen that the current at the peak output power is comparable to the main device value, which implies that full Doherty load modulation of the main device can be achieved. The voltage also increases linearly. Again at low power levels, due to the higher gate bias and larger input stimulus, the resulting fundamental voltage is approximately 30V. This is now approaching a critical level when using Si LDMOS technology, which typically has a high voltage breakdown limit of around 75 V. The peak voltage value achieved by the device is 69 V. This is shown more clearly in Fig. 9-26, where the individual current and voltage waveforms are shown instead of dynamic load lines to emphasize the large voltage swing at the lowest power level. Whilst this auxiliary setup will function correctly to apply the required conditions for Doherty operation, there is now an increased risk in the continued functioning of the PA. Applying a process variability of 10 % to the breakdown voltage will produce a voltage breakdown value in the range of 67.5 – 82.5 V, which produces a risk when mass producing a Doherty PA, with such an optimisation. Whilst this is not the focus of this work, this should be investigated further to provide an increased insight into reliable Doherty PA design.
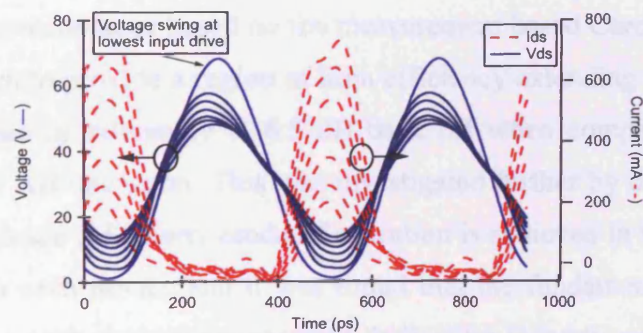
(a)
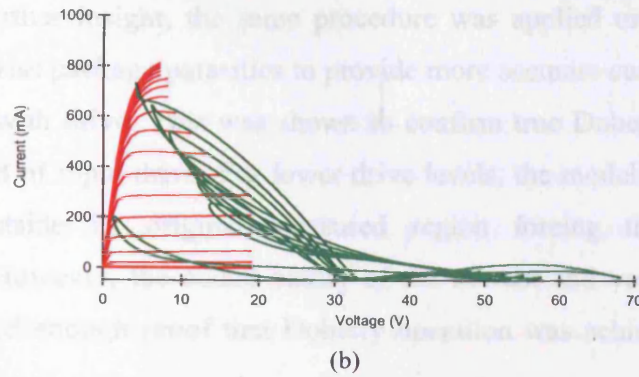
Fig. 9-26 – (a) Current and voltage waveforms at the I_{gen} plane of the emulated auxiliary device,
(b)) Dynamic load lines at the I_{gen} plane of the emulated auxiliary device

9.5 Conclusion

This chapter has outlined the efficiency benefits of implementing a Doherty PA within the high power base station market for 3rd and 4th generation based systems. Third and fourth generation systems support higher number of users as well as higher data rates, with a consequence of increased signal complexity and high peak to average ratios typically in the region of 6 – 9 dB. For linearity purposes these devices are operated backed off with a consequence of lowering the operating efficiency. A Doherty PA overcomes this, by providing an efficiency plateau over an extended region of input drive that can be varied from 6- 12 dB depending upon the arrangement applied.

To begin with a 200 W Doherty PA was designed using established matching network design techniques based on the measurement based Cardiff LUT model. This was shown to provide a region of high efficiency extending up to 6 dB with a 14 % increase in efficiency at 6.5 dB back off when compared to a single device in class AB operation. This was investigated further by de-embedding to the I_{gen} plane to see if Doherty mode of operation is achieved in the design. This was applied to each device and it was found that the fundamental voltage and current profiles with drive were correctly indicating Doherty operation of both the main and auxiliary devices. However, the exact voltage and current values were found not to be totally accurate.

To gain a further insight, the same procedure was applied on a lower power device, with less package parasitics to provide more accurate current and voltage components with drive. This was shown to confirm true Doherty operation for the peak 5 dB of input drive. For lower drive levels, the model was found to be operating outside its original measured region forcing the simulator to extrapolate. However, the added clarity of the current and voltages at the I_{gen} plane provided enough proof that Doherty operation was achieved within both devices.

An alternative approach based on the active load pull waveform based measurement system was employed by utilising the load pull system to emulate the conditions required for Doherty operation. This procedure provides useful information of assessing the device's capabilities for design and more importantly allows the user the opportunity to optimise the design of a Doherty PA in real time, simultaneously visualising the device's mode of operation. This was first applied on the main device where a constant voltage constraint was applied to the device over the peak 6 dB of input drive and compared against theory. The device used showed a close match to theory but with some reduction in the voltage swing at lower power levels, which was attributed to a non ideal gm property of the device. The same procedure was applied to the auxiliary device, where it was necessary to apply "tweaks" to achieve optimum operation. This was done by emulating an asymmetric power split and by increasing the DC gate and drain voltages. However, one potential drawback of these modifications was the presence of high voltage swings at low input drives due to the early turn on of the auxiliary device. These voltage swings were shown to be comparable to the voltage swings when at full output power and in some cases extending to high voltages that could potentially damage the device and lower the reliability of the PA. By applying these "tweaks" the designer now has all of the information required to produce a fully operational Doherty PA. In both the simulation and measurement domain, it has been shown that access to the currents and voltages at the I_{gen} plane provides an invaluable source of information in the design of Doherty PAs.

10 <u>Conclusions</u>

The work undertaken in this thesis has provided the PA designer a route back to the origins of PA design, i.e. the manipulation of currents and voltages for optimum performance in efficiency, power and gain. This has been outlined, by the achievement of world record efficiency values of 77% when using high powered Si LDMOS devices at S-band frequencies. However, before this was made possible it was important to first establish the complexity of the de-embedding required and the confidence to apply waveform based procedures. This was achieved by applying established techniques in package and device modelling and taking into account external factors such as the harmonic impedance environment. The results achieved provided access to the current generator plane, leading to the correlation of currents and voltages with theory at power levels previously not possible. These procedures were extended to two other examples of access to the current and voltage waveforms, the first being the confirmation of Doherty behaviour in high power designs and the second being the successful verification of a large signal model.

Large signal de-embedding, was initially applied on a 5W Si LDMOS device at 2.1 GHz. To begin with an accurate package and device model was formulated using 3D modelling and established measurement based techniques. The package was modelled based on physical measurements of the package and imported into a 3D simulation package. The device manifold was simulated using well-defined layer stacks of the silicon die. Both of these procedures were applied with confidence and have been validated using established techniques [18]. The extrinsic and intrinsic device properties were determined using measurement based techniques [19, 37] and modelled using physically derived equations that are fully charge conservative. The waveform data captured at the calibrated reference plane were de-embedded to various internal planes. It was found that only by completely removing all of the parasitic effects of the package and device to the current generator plane, were the current and voltage waveforms relatable to what is described theoretically in the literature [3]. The resultant

waveforms at maximum output power were shown to correctly indicate that the device was biased in deep class AB and a sinusoidal voltage swing. The majority real impedance at the I_{gen} plane was also found to be close to the optimum resistance for maximum output power.

A similar procedure was applied to a 110W Si LDMOS device, however with less success than for the smaller device. The waveforms achieved at the I_{gen} plane for half of the device produced a voltage waveform that was correctly sinusoidal, however the current waveform did not show any rectification and did not indicate the deep class AB bias setting. This was due to the increased complexity of package and device modelling required that can not be modelled using linear scaling rules. Further work is necessary in producing high power waveforms that could be more relevant for high power PA design.

The use of waveforms in high power devices has until now not been fully explored. This work has uncovered that high power waveforms are more susceptible to outside factors not previously thought necessary for consideration. In this case the major issue was the ratio of the higher system impedance to the fundamental optimum impedance of the device. On wafer devices have fundamental optimum impedances in excess of the standard system impedance of 50 Ω, therefore presenting a pseudo short circuit to the higher harmonics. In high power devices, this situation is reversed, in that the higher harmonics see impedances that are higher than the fundamental optimum. The consequence of this effect is the generation of higher harmonic voltage components that can severely distort the waveforms, ultimately questioning the de-embedding process. This effect was first investigated using real only higher harmonic impedances and expanded to complex impedances. From this work, it was found that complex higher harmonic impedances not only affected the waveforms but also affected the optimum impedance for power by forcing a reactive shift at the I_{gen} plane. This investigation was validated to a high level of agreement using measured data of a 5W Si LDMOS device, therefore providing current and voltage waveforms relevant for design at high power levels.

The next step was to apply this feature of accessing the internal waveforms for further use. The first application of waveforms at the I_{gen} plane was shown with the demonstration of class F mode of operation on a 5W Si LDMOS device at 2.1GHz leading to world leading efficiencies of 77 % when using Si LDMOS devices [15]. Si LDMOS devices are the current device technology of choice in the commercial domain due to low cost and high linearity. However, due to the high output capacitance, it has been very difficult to achieve high efficiency designs that have efficiencies comparable to the more costly GaN technology based PAs. [84]. This now provides the PA designed with two viable choices in device technology when designing high efficiency PAs with little difference in performance, but a large difference in linearity and cost. Previously class F or inverse class F operation was achieved at L-band frequencies but there was little success demonstrated in the literature at higher frequencies [49]. With access to the waveforms at the I_{gen} plane, waveform engineering principles were applied to provide the optimum current and voltage waveforms at two different frequencies of operation for class F operation as demonstrated in Chapter 7.

A further demonstration of the added insight of access to the waveforms was presented with the uncovering of voltage breakdown when implementing inverse class F using Si LDMOS devices. Inverse class F and class F both provide the desired theoretical 100% drain efficiency. However, the switching of the current and voltage profiles can have some performance degrading effects if the design has not been fully thought through. When applying the recommended 28V drain bias, the voltage swing of inverse class F expands up to a peak value of 81 V in a limited bandwidth implementation. This is clearly in excess of the 65 V voltage breakdown limit specified in Si LDMOS device datasheets 65 V [85]. In practice, the voltage breakdown was found to be approximately 75 V and was proven with the presence of an increasing current component at high voltages leading to a drop in drain efficiency and an increased risk of device failure. When the drain bias voltage was reduced to 18V, the performance of the inverse class F implementation was slightly above that found in class F, whilst producing the same output power.

A second application of waveform de-embedding was the validation of a commercially available, charge conservative large signal model. To date, models for use within CAD have been validated using load pull measurements where the impedance is a vector and the output power is a scalar value. Whilst this procedure has led to many successful designs, such a validation is not sufficient for waveform engineering within a CAD environment. The investigation conducted in this thesis has highlighted that the large signal model was in excellent agreement with measured data in class AB, with little difference in output power and in the current and voltage waveforms at the intrinsic reference plane. When implementing the same procedures in multi-harmonic designs, the model was shown to be in good overall agreement with the measured data, with little difference in output power and efficiency. The slight differences in the current waveforms were noted to be due to the higher harmonic components. However, this successful validation has promoted the concept of applying waveform engineering within a CAD environment.

The last chapter follows on a similar theme to the class F work, but is now expanded to a multiple device structure. The Doherty amplifier is the current PA architecture of choice for base-station applications. In the case of the Doherty amplifier, waveform de-embedding was applied to confirm true Doherty operation using both high and low power devices, using established matching network design methodologies [70]. The initial high power Doherty amplifier, showed encouraging signs of Doherty operation but due to the limited confidence in the de-embedding a similar procedure was applied to a medium power design, where Doherty operation was fully validated at the I_{gen} plane, within the device model's simulation range. The second part of this chapter outlined how waveform engineering and active load pull can be utilised to provide an enhanced insight into Doherty design. Using active load pull to mimic the other device, an individual device was investigated to provide the optimum performance when functioning as either the main or auxiliary. This was initially based on the main device where the voltage was shown to be constant over an extended input range. To provide these conditions for the main, the auxiliary device was optimised in terms of gate and drain bias as well as input

power split to provide the ideal design conditions for a 6 dB Doherty power amplifier. However, in all cases, it was noted that there was a risk of generating large voltage swings at the transition point and this needs to be investigated further within realised designs to better identify the reliability risks of these design tweaks.

As outlined earlier, this thesis has demonstrated the value of waveform engineering in providing an added insight in the measurement, design and validation parts of a PA design process. Whilst the classical power meter and spectrum analyser based techniques have provided an accurate means of assessing PA performance, the added insight in seeing the relevant current and voltage waveforms provides a means of rationally optimising performance and producing reliable designs for mass usage.

11 __Future Work__

The work, outlined in this thesis has provided a significant step forward in enabling high power waveform engineering and introduced the considerations required to produce accurate waveforms. This section outlines the further work necessary in moving forward the work undertaken in this thesis. At the time of writing, much of the logically following future application based work has been undertaken within the research group. For instance, a high efficiency inverse class F high power amplifier [11] and an efficiency enhanced octave band high power amplifier [86]. However, the two topics outlined below would usefully extend this work and increase understanding of some novel questions raised in this thesis.

11.1 Further Developments in High Power Modelling

The package and device model used for the high power de-embedding was a simplified approach to what was utilised in the 5W device case. This approach was taken due to the prohibitive effects of the increased complexity and simulation resource requirements. However, the waveforms produced were not fully indicative of the device's behaviour, as demonstrated by the current waveform at the I_{gen} plane not showing any signs of rectification. This section outlines how to remedy this problem for producing more meaningful waveforms at the I_{gen} plane in the case of large devices in complex packages.

One of the primary reasons for this is the large die size that is now representing a device periphery that is greater than 50mm, which can be greater than the wavelength at the fundamental frequency of operation. The exact affect on the ability to de-embed waveforms is not fully known, but the waveforms produced at this plane were not of the same quality and clarity as in the smaller device. This could be minimised by dividing the device periphery into smaller units and increase the simulation complexity by adding multiple paths to a single die as shown in Fig. 11-1 (b). For demonstration purposes a single die is broken into five separate sections, which can also be inverted using an extended t-parameter conversion. The drawback in this approach is the increased complexity required

in physically modelling the package and it's several bond wires the increased simulation time it will take in simulating a 3D model of the package over an extended bandwidth. To save simulation complexity the process can be mirrored across both die as the effects will be symmetrical, however this does overlook the mutual and capacitive coupling between two individual die and their bondwire networks.
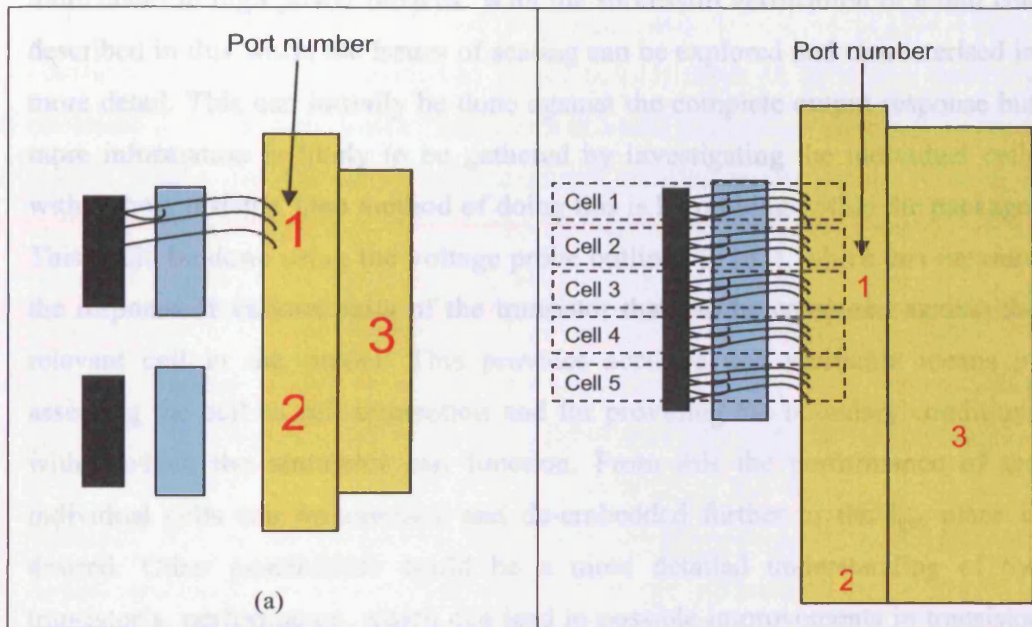
Fig. 11-1 – (a) Package model adopted in this thesis, (b) Proposed package model for future work considerations for a single die

This increased complexity must also be replicated on the silicon die. This can be done by applying the same cell divisions on the die when simulating the device manifold. From here the extrinsic and intrinsic parameters can be extracted based on existing techniques. Initially these cells can be treated in isolation, however the more stringent approach would be to incorporate the mutual coupling effects on the die as well and tailor these effects depending on the location of the cell on the die. For example the mutual effects on cell 5 will in practice be different than the mutual coupling found in cell 3 and the extrinsic and/or intrinsic device model must reflect this in some way.

Once this procedure is applied, it should be possible to insert this more detailed structure within the CAD simulations outlined in Chapter 7. However, the danger is that due to the increased complexity and undefined solution space, there is a risk that the simulator will not produce meaningful results or may not even compile. This is due to the differing non-linear responses of each of the cells which occurs due to the variation in phase lengths and how they interact with each other. For this reason, it maybe more beneficial to investigate this in more detail in high power devices. With the successful verification of a unit cell described in this work, the issues of scaling can be explored and characterised in more detail. This can initially be done against the complete output response but more information is likely to be gathered by investigating the individual cells within the transistor. One method of doing this is by probing within the package. This could be done using the voltage probe outlined in [87], which can measure the response at various parts of the transistor that can be compared against the relevant cell in the model. This provides accurate and verifiable means of assessing the cell to cell interaction and for providing the boundary conditions within which the simulator can function. From this the performance of the individual cells can be assessed and de-embedded further to the I_{gen} plane if desired. Other possibilities could be a more detailed understanding of the transistor's performance, which can lead to possible improvements in transistor layout for better power combination leading performance levels typically found in lower power devices.

11.2 Doherty Reliability Investigations

The Doherty power amplifier is the current PA architecture of choice for third and fourth generation basestation systems, making its reliability for mass deployment a critical factor. As was pointed out in Chapter 9, the voltages generated in the auxiliary device can hit the break down voltage of the device when operating close to the transition point. If this process is repeated the auxiliary transistor will be susceptible to breakdown, disabling the power amplifier and requiring extra expense in the form of replacement transistors and engineering time. Since the mean operation point of 3G systems is around 7dB backed off from peak power, the probability of this occurring over time becomes

significantly greater. To mitigate this from occurring, it is necessary to first understand how this can occur within the Doherty amplifier to then aid in providing an effective solution.

To begin with, the scenario identified in Chapter 9 is discussed further. The dynamic load lines of the optimised auxiliary settings are shown in Fig. 11-2. In this case the peak voltage swing is at the transition point at which the auxiliary device should turn on and start load pulling the main device. As no gate voltage control is applied, the asymmetric power splitter starts to drive the auxiliary device at a lower than desired input power level. This starts to generate drain current, whilst operating at a high impedance, resulting in the generation of high voltages. Such a scenario is possible in reality, as the incorporation of an asymmetric power splitter has resulted in many successful designs [70]. In addition, the optimising process can lead to higher gate voltage settings where output power and efficiency will be seen as the key driving factors. One possible solution to this would be to adopt an adaptive gate bias approach as highlighted in [73], where the gate voltage will only turn up at the correct power level. However, due to the increasing modulation frequencies and bandwidths, the design complexity makes it very similar to the difficulties encountered in envelope elimination and restoration and envelope tracking.
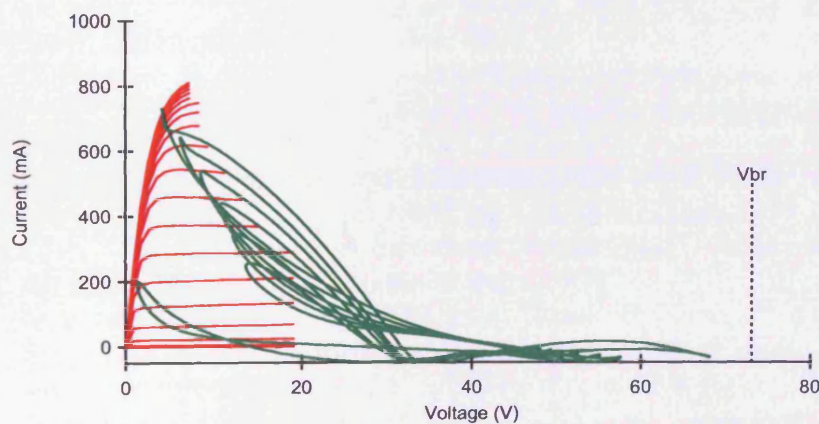
Fig. 11-2 – Dynamic load lines at the I_{gen} plane of the emulated auxiliary device

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The majority of Doherty amplifiers designed in industry are intended for extended operation beyond the classical designs of 6 dB. As discussed earlier, these designs require the auxiliary device to inject current levels greater than the main device. For this to occur, ideally the auxiliary device should be of a larger periphery. In reality, the same device is used and a compromise in performance is achieved, where the auxiliary device turns on earlier to achieve an early peak value in efficiency but reduce in overall efficiency at higher power levels. This performance is deemed to be more beneficial as the amplifier will be operating at back off for the majority of its life. However, the reliability repercussions could be significant and need to be further explored.

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A1 – Small Signal Verification of Charge Conservative Model

The small signal model is verified against measured data taken at the input and output ports of the device. This is achieved using a broadband TRL calibration. The verification process is done in two stages, the first stage involves cold FET measurements to analyse the passive performance match. The second stage looks at the active device performance with the device biased at 5mA/mm.
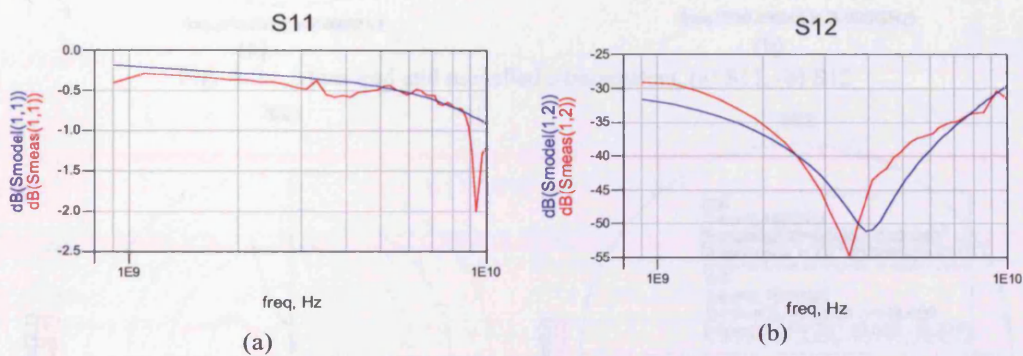
A1.1 - Cold FET Measurements

(a)   (b)

Fig. A 1 – Measured and modelled s-parameters, (a) S11, (b) S12
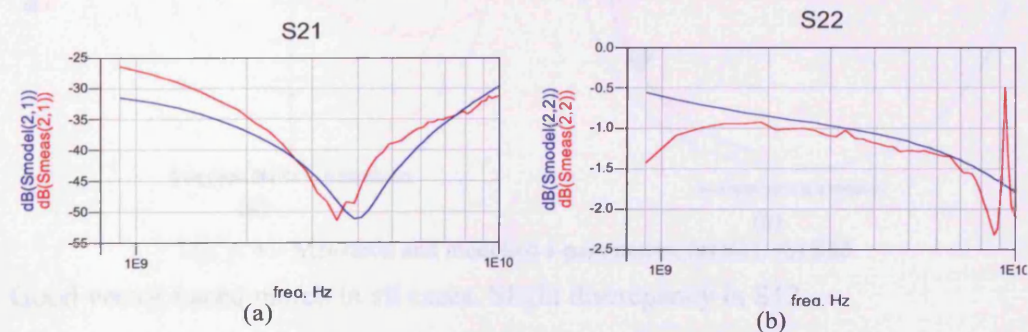

(a)   (b)

Fig. A 2 – Measured and modelled s-parameters, (a) S21, (b) S22

Good match between the model and measurements. Now looking at the vector based measurements. There is some discrepancy in S11 and S22 around 9.5 GHz.
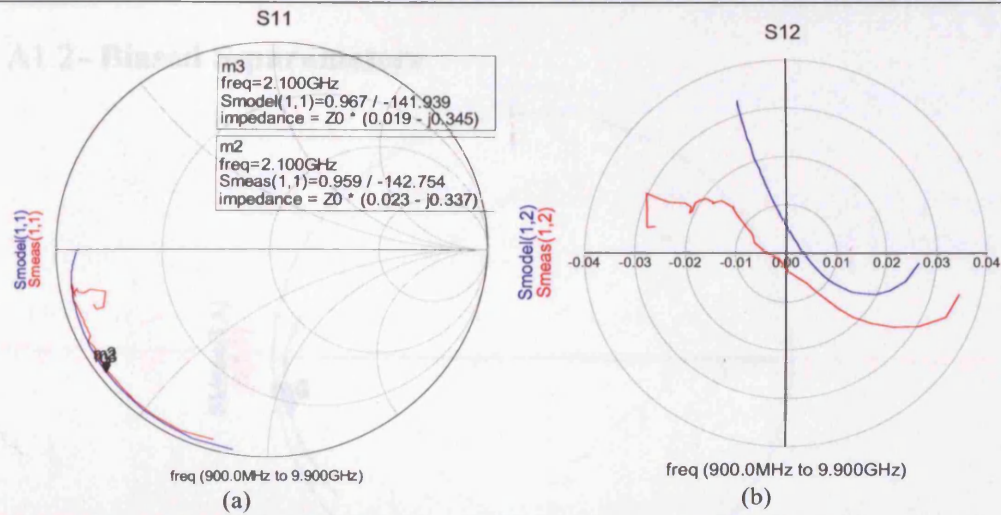
S11

m3
freq=2.100GHz
Smodel(1,1)=0.967 / -141.939
impedance = Z0 * (0.019 - j0.345)

m2
freq=2.100GHz
Smeas(1,1)=0.959 / -142.754
impedance = Z0 * (0.023 - j0.337)

freq (900.0MHz to 9.900GHz)
(a)

S12

freq (900.0MHz to 9.900GHz)
(b)

Fig. A 3 – Measured and modelled s-parameters, (a) S11, (b) S12

S21

freq (900.0MHz to 9.900GHz)
(a)

S22

m4
freq=2.100GHz
Smodel(2,2)=0.905 / -142.946
impedance = Z0 * (0.056 - j0.334)

m5
freq=2.100GHz
Smeas(2,2)=0.889 / -143.602
impedance = Z0 * (0.065 - j0.328)
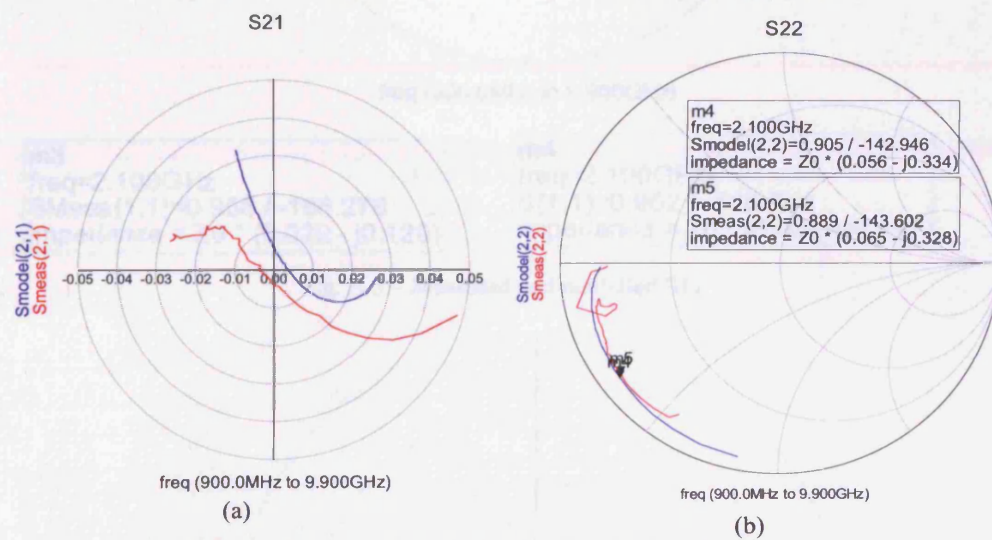
freq (900.0MHz to 9.900GHz)
(b)

Fig. A 4 – Measured and modelled s-parameters, (a) S21, (b) S22

Good vector based match in all cases. Slight discrepancy in S12.
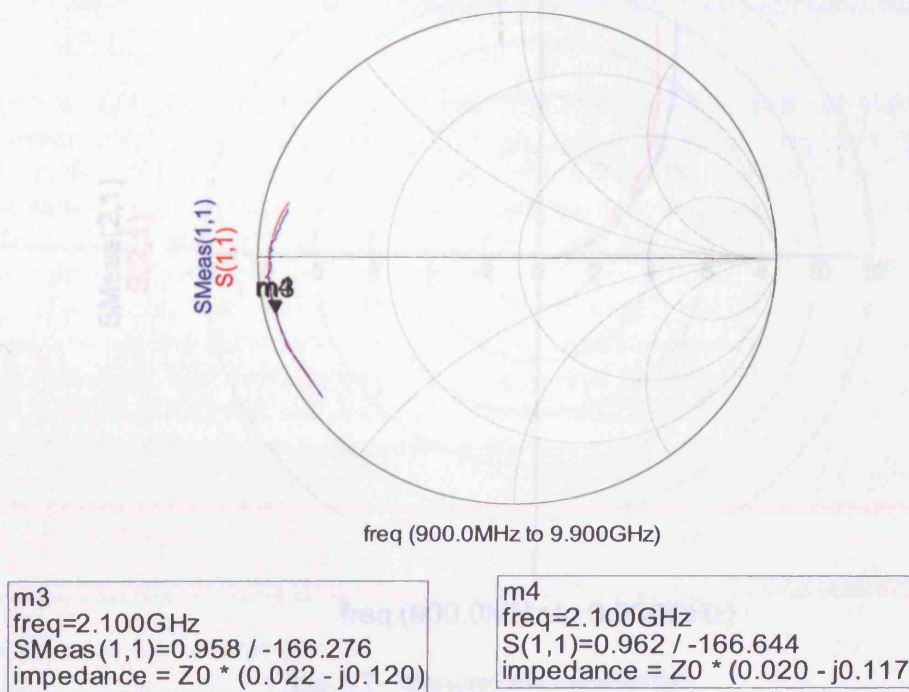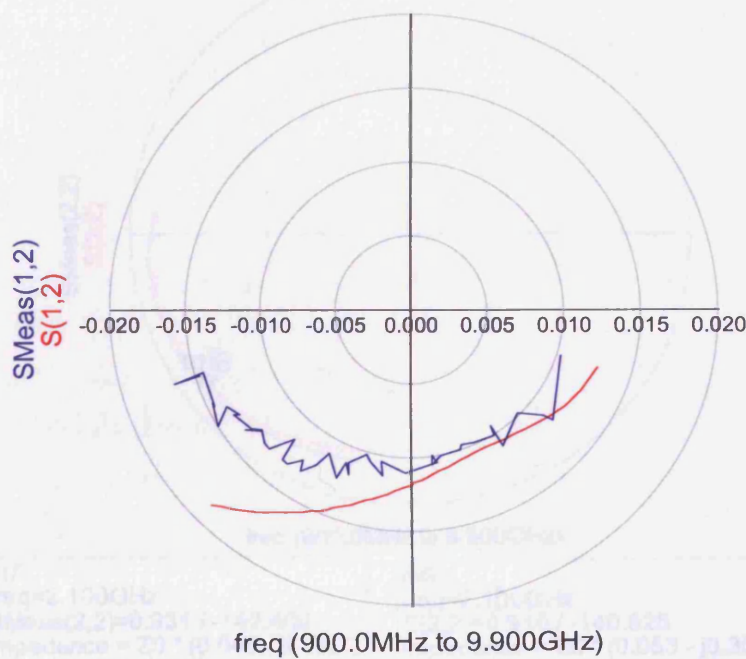
A1.2- Biased S-parameters

freq (900.0MHz to 9.900GHz)

```
m3
freq=2.100GHz
SMeas(1,1)=0.958 / -166.276
impedance = Z0 * (0.022 - j0.120)
```

```
m4
freq=2.100GHz
S(1,1)=0.962 / -166.644
impedance = Z0 * (0.020 - j0.117)
```

Fig. A 5 – Measured and modelled S11

freq (900.0MHz to 9.900GHz)

Fig. A 6 – Measured and modelled S12

As outlined earlier there is a gross mismatch between the model and measurements. The model is predicting slightly more gain than what has been measured.

SMeas(2,1)
S(2,1)

-12 -10 -8 -6 -4 -2 0 2 4 6 8 10 12

freq (900.0MHz to 9.900GHz)
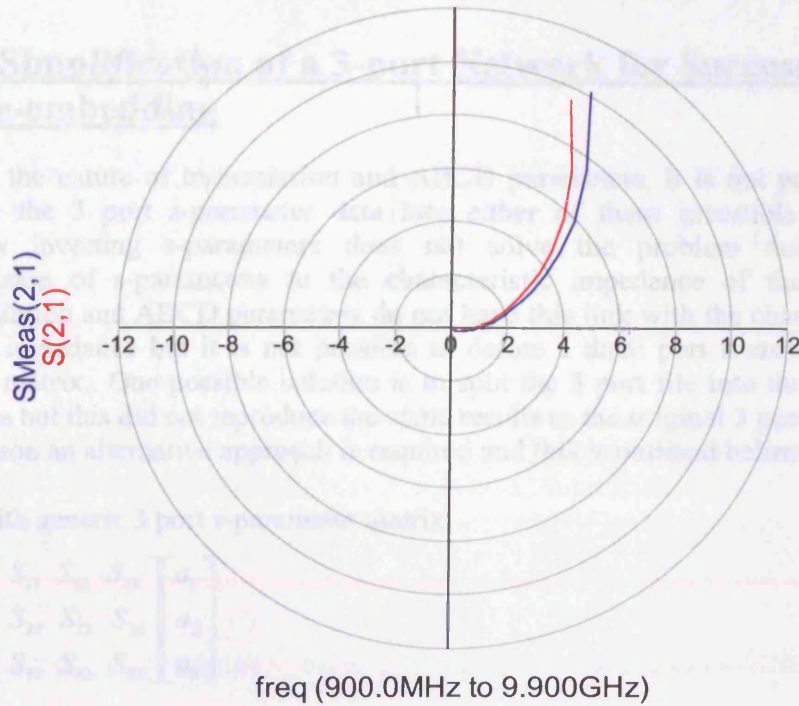
Fig. A 7 – Measured and modelled S21

SMeas(2,2)
S(2,2)

m7
m8

freq (900.0MHz to 9.900GHz)
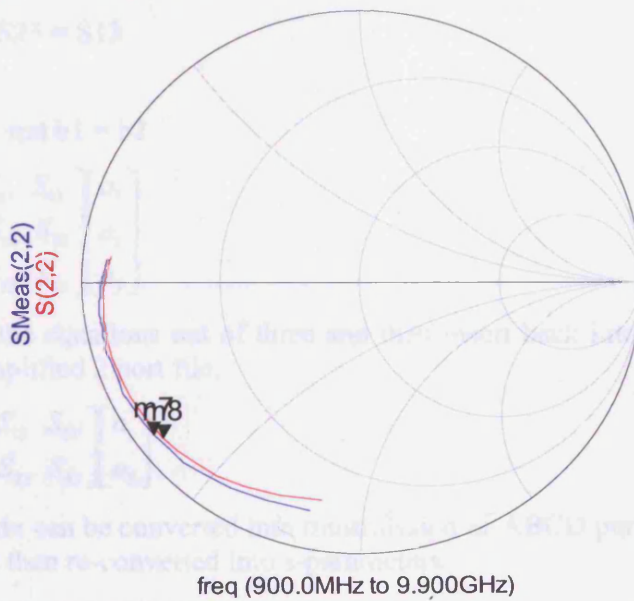
m7	m8
freq=2.100GHz	freq=2.100GHz
SMeas(2,2)=0.931 / -142.666	S(2,2)=0.910 / -140.826
impedance = Z0 * (0.040 - j0.337)	impedance = Z0 * (0.053 - j0.355)

Fig. A 8 – Measured and modelled S22

As outlined earlier there is a good match between the model and measurments. The model is predicting slightly more gain than what has been measured.

A2 - Simplification of a 3-port Network for Successful De-embedding

Due to the nature of transmission and ABCD parameters, it is not possible to convert the 3 port s-parameter data into either of these invertible formats. Directly inverting s-parameters does not solve the problem due to the relationship of s-parameters to the characteristic impedance of the system. Transmission and ABCD parameters do not have this link with the characteristic system impedance but it is not possible to define a three port transmission or ABCD matrix.. One possible solution is to split the 3 port file into three 2 port matrices but this did not reproduce the same results as the original 3 port file. For this reason an alternative approach is required and this is outlined below.

Start with generic 3 port s-parameter matrix

$$
\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}
$$
(A) 1

Assuming the structure is symmetrical, i.e.

S11 = S22   (A) 2

S31 = S32 = S23 = S13   (A) 3

S12 = S21   (A) 4

Then a1 = a2 and b1 = b2

$$
\begin{bmatrix} b_1 \\ b_1 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_1 \\ a_3 \end{bmatrix}
$$
(A) 5

Take two of the equations out of three and then insert back into matrix form to produce a simplified 2 port file.

$$
\begin{bmatrix} b_1 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} + S_{12} & S_{13} \\ S_{31} + S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_3 \end{bmatrix}
$$
(A) 6

Now the matrix can be converted into transmission or ABCD parameters for inversion and then re-converted into s-parameters.