RF IV Waveform Engineering Applied to VSWR Sweeps and RF Stress Testing

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Declaration

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Summary

This thesis looks at how the Radio Frequency (RF) waveform measurement and engineering techniques developed for Power Amplifier (PA) design can be used to investigate RF reliability. Within this area two major themes are concentrated on – firstly the effect of a load impedance mismatch and secondly an investigation into using the RF IV waveform measurement system for RF stress testing.

The initial aim for this work was to investigate the potential for removing the output protection isolator from a PA. It was seen that in doing so there is the potential to cause an impedance mismatch, which results in a portion of the power produced being reflected back. It was shown that the conditions that could be presented to a device as a result of an impedance mismatch can be found by performing a Voltage Standing Wave Ratio (VSWR) sweep. The results of the worst possible case scenario VSWR sweep, when all of the power is reflected back, can be split into three regions. One of high RF drain voltage swings, one of high RF drain currents and a transition region of simultaneously high RF drain currents and voltage swings. Each of these regions presents different operating conditions to the device, and in turn different stresses.

The second part of this thesis concentrates on an investigation into Gallium Nitride (GaN) Heterostructure Field Effect Transistor (HFET) reliability, specifically if the RF waveform measurement system can be used to provide detailed information about the state of the device during RF stress testing. A stress testing procedure was developed to allow this, which featured both DC and RF characterisation measurements before and after every stress period. It was shown that the measurements made during the characterisation stages only gives a representation of the degradation seen in the same measurements during the RF stress period.

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List of Publications

"Development of an RF IV waveform based stress test procedure for use on GaN HFETs"

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"Development of a RF Waveform Stress Test Procedure for GaN HFETs Subjected to Infinite VSWR Sweeps"

W. McGenn, H. Choi, J. Lees, M.J. Uren, J. Benedikt, P.J. Tasker

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"Continuing Development of RF Waveform Based Stress Test for use on GaN HFETs"

W. McGenn, M.J. Uren, J. Benedikt, P.J. Tasker

Reliability of Compound Semiconductors (ROCS) Workshop 2012

"RF Waveform Investigation of VSWR Sweeps on GaN HFETs"

W. McGenn, J. Benedikt, P.J. Tasker, J. Powell, M.J. Uren

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"RF Waveform Method for the Determination of the Safe Operating Area of GaN HFET's for Amplifiers Subjected to High Output VSWR"

W. McGenn, J. Powell, M.J. Uren, J. Benedikt, P.J. Tasker

European Microwave Integrated Circuits Conference (EuMIC) 2010

"Analysis of the Failure Mechanisms of VSWR Testing on GaN HFETs"

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Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE) 2010

List of Symbols

Symbol	Explanation
A	Amps
A_n	Incident voltage travelling wave, where n is the port number
Al	Aluminium
AlGaN	Aluminium Gallium Nitride
Al_2O_3	Sapphire
Au	Gold
B_n	Reflected voltage travelling wave, where n is the port number
C	Celsius
C_{DS}	Drain-Source capacitance
C-band	Frequency band ranging from 4GHz to 8GHz
dB	Decibel
dBm	Decibel, compared to 1mW
DC	Direct Current
DCIV	DC measurement of the device’s output current/voltage plane
DSO	Digital Sampling Oscilloscope
DUT	Device Under Test
e	electron
EL	Electro Luminescence
ELP	Envelope Load Pull
eV	Electron Volt
F	Farad, unit of Capacitance
f	Frequency
FOM	Figure Of Merit
Fe	Iron
Ga	Gallium
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HFET	Heterostructure Field Effect Transistor
Hz	Hertz, unit of frequency
I	Current
I_{DC}	DC drain bias current
I_{Dknee}	Drain current at the knee of the DCIV
I_{Dmax}	Maximum drain current
j	Imaginary Number
K	Kelvin

LNA	Low Noise Amplifier
LO	Local Oscillator
log	Logarithm
m	Metre
MBE	Molecular Bean Epitaxy
MOCVD	Metal Organic Chemical Vapour Deposition
MOSHFET	Metal Oxide Semiconductor HFET
MTA	Microwave Transition Analyser
N	Nitrogen
Ni	Nickel
PA	Power Amplifier
PAE	Power Added Efficiency
P_{DC}	DC Power supplied to a device
P_{Diss}	DC Power Dissipation
P_{IN}	RF Input Power
P_{Sat}	Saturated output power of the device
P_{inSat}	Input power needed to saturate the output power of the device
P_{OUT}	RF Output Power
Pt	Platinum
Q-Band	Frequency band ranging from 33GHz to 50GHz
RF	Radio Frequency
RMS	Root Mean Square
R_{therm}	Thermal Resistance
s	Second
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
SOA	Safe Operating Area
t	Time
T_a	Ambient Temperature
Ti	Titanium
T_j	Static Junction Temperature
V	Voltage
V_{DC}	DC drain bias voltage
V_{DS}	Drain-Source Voltage
V_{GD}	Gate-Drain Voltage
V_{GS}	Gate-Source Voltage

V_{TH}	Threshold Voltage
VSWR	Voltage Standing Wave Ratio
W	Watt
Z	Impedance
Z_{Load}	Load Impedance
Z_{norm}	Normalised Load Impedance
Z_{opt}	Optimum Load Impedance
Z_s	Characteristic Impedance, usually 50Ω
α	Alpha, Conduction angle of amplifier mode
Γ	Reflection Coefficient
η	Efficiency
λ	Wavelength
π	Pi
Ω	Ohm, unit of Impedance
ω	Radian Frequency, $\omega=2\pi f$
∞	Infinity
2DEG	Two Dimension Electron Gas
| |	Magnitude
∠	Angle
°	Degree

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Chapter 1 – Introduction

1.1 Background

The demands placed on modern communications systems are ever increasing, be it in a mobile phone handset, base station, wireless router or a satellite. We live in a time of 'green' thinking where wasting power is frowned upon, therefore one demand that is placed on most communications systems is the need to reduce the amount of wasted power, or in other words, increase the efficiency of the system. However increasing the efficiency of these systems also has a practical effect beyond just being 'green'. One of the key components to any communications system are the RF Power Amplifiers (PA) which are also one of the most power hungry, generally having a relatively poor efficiency often below 50% [1]. This means that less than half of the applied DC power is turned into useful RF output power, while the rest is dissipated across the device within the PA itself. This active device is the central part of a RF PA. In order to understand the state of a device the RF current and voltage waveforms at the input and output must be known [2]. Systems have been developed that are able to measure these voltage and currents, and then engineer them to present arbitrary impedances to the device at multiple harmonic frequencies [3,4]. These systems have been predominantly used to develop advanced PA operating modes, allowing for high efficiencies to be maintained across high frequency bandwidths [1, 5-7].

Another of the demands that is placed on communications systems is the size of the components that they contain; again the device within an RF PA is another key target. There is currently a huge amount of time and money being spent on research into Gallium Nitride (GaN) based semiconductor devices, particularly the Heterostructure Field Effect Transistor (HFET). The GaN HFET allows for a much higher power density than most other device technologies, which in turn allows for smaller devices and easier impedance matching [8]. However the very properties of GaN that are advantageous

are also those that lead to its reliability problems. Until recently the high potential difference between the gate and drain has been a source of major reliability problems. As such GaN HFETs have yet to achieve widespread adoption and will continue not to do so until they have shown reliable operation [9].

The over arching theme for this thesis is the use of the RF IV waveform measurement and engineering system (which will be described in section 2.3.5) for reliability applications. Two such applications are examined in the course of this thesis, the implications of a load impedance mismatch and how RF IV waveforms can benefit reliability measurements.

1.2 Thesis Outline

The beginning of chapter 2 presents an introduction to GaN HFETs as well as a review of the characterisation measurements and the systems used to characterise devices for PA design. Finally a review of the common PA operating modes is presented, including the high efficiency modes and the relatively new continuous modes of operation.

An output protection isolator is often used on the output of a PA that is driving an antenna. Its role is to protect the PA from any power that may be reflected (for whatever reason) from the antenna, however it is a large, bulky component and can cause power loss between the PA and antenna [10]. The first part of this thesis begins with the question of 'What happens if this isolator is removed?'.

The end of chapter 2 begins to answer this question by presenting a theoretical investigation of the effects of an impedance mismatch. From this it becomes clear that all of the possible states that a device could be presented with at a specific level of impedance mismatch can be presented by a VSWR sweep. However this theoretical investigation does not include the effects of the device that is driving power into this mismatched load.

Chapter 3 builds on the theoretical investigation by measuring VSWR sweeps on GaN HFETs. Firstly the worst case scenario is considered where all of the output power of the PA is reflected back, before investigating the effect of the device size, drain bias and input power. As this worst case scenario is not always representative of real world conditions, other VSWR sweeps are measured to compare with the worst case.

The second topic of this thesis investigates how the RF IV waveform measurement system can be used to perform reliability testing. This begins in chapter 4 with a discussion on current methods of reliability testing followed by the common failure mechanisms of GaN HFETs. It is established that RF IV waveforms could be complimentary to RF stress testing, allowing the exact state of the device to be known under RF operation – something that is currently, usually only inferred from measuring DC voltage and current and also RF power measurements.

In chapter 5 a stress testing procedure is developed (based on the one in [11]) which features both DC and RF characterisation measurement stages. This procedure is used to perform a series of simple stress tests, both at the optimum impedance and at impedances from the infinite VSWR sweep. The procedure is then extended to include multiple stress periods in order to carry out both drain bias and input power RF step-stress tests.

Finally chapter 6 presents a summary of the results of the two sections of this thesis as well as ideas on how these results can be used in the future.

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Chapter 2 – Review of RF Power Amplifiers and Introduction to VSWR Sweeps

2.1 Introduction

The RF Power Amplifier (PA) is a key component in many communications systems; however it is also one of the most demanding, both in terms of design time and also once it is operating in the circuit. These demands have encouraged the growth of both a first pass design methodology along with new, rugged devices and high efficiency operating modes.

Gallium Nitride (GaN) based transistors offer many potential benefits over those utilising other semiconductor technologies, including high RF power density. Section 2.2 will provide a summary of the state of the art GaN devices, as well as highlighting some of the problems that are left to be solved. This summary will be continued in section 4.2 on the subject of reliability.

A first pass design methodology is made possible by the increase in data that is being offered by RF waveform measurement systems. This allows for rapid development and prototyping of new PA operating modes, which show increased efficiency over large bandwidths. Section 2.3 will summarise different device characterisation methods and section 2.4 will present a summary of the basic, high efficiency and continuous modes of PA operation.

This chapter will then move onto a theoretical investigation of the effect of an impedance mismatch, where the device is presented with a non optimal load impedance in section 2.5. This will conclude by showing how a VSWR sweep can present all of the possible conditions that a device can experience as a result of an impedance mismatch.

2.2 High Frequency GaN HFETs

Gallium Nitride (GaN) based transistors are quickly becoming a leading choice for RF PA applications due to their high RF power density. Table 2.1 compares the material properties of GaN with a selection of other semiconductor materials.

Table 2.1 - Parameters of different semiconductors, from Mishra et al. [1]

	Silicon	**Gallium Arsenide**	**Silicon Carbide**	**Gallium Nitride**	**Diamond**
Band Gap (eV)	1.1	1.42	3.26	3.39	5.45
Intrinsic Electron Concen. (m^{-3})	$1.5x10^{10}$	$1.5x10^{6}$	$8.2x10^{-9}$	$1.9x10^{-10}$	$1.6x10^{-27}$
Electron Mobility (cm^2/Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)	1900
Saturation Velocity ($x10^7$ cm/s)	1	1	2	2.5	2.7
Breakdown Electric Field (MV/cm)	0.3	0.4	3	3.3	5.6
Thermal Conductivity (W/cm K)	1.5	0.43	3.3-4.5	1.3	20

Wide band gap semiconductors are desirable in RF PAs as they have high breakdown voltages and can operate at high channel temperatures. While it can be seen that GaN and Silicon Carbide (SiC) have very similar band gaps (and electron saturation velocities, which is important for high frequency operation) the advantage of GaN is the ability to create heterojunctions. This leads to greatly increased electron concentration and mobility in the channel of GaN Heterostructure Field Effect Transistors (HFET). It is a combination of the high operating voltages afforded by the wide band gap and the high electron density of the heterostructure that gives the high power densities.

The basic structure of a GaN HFET is shown in figure 2.1. The heterostructure is formed by depositing a layer of Aluminium Gallium Nitride

(AlGaN), which has a slightly wider band gap than GaN, over the top of the GaN. This process forms a 2 Dimension Electron GaN (2DEG) at the interface between the two layers, which allows for high current density, low channel resistance and better noise performance [1].

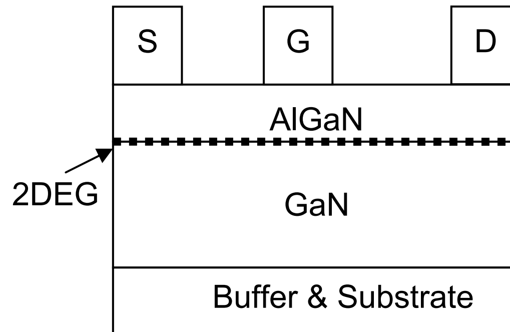


Figure 2.1 - Structure of a GaN HFET

The 2DEG is created by the polar and piezoelectric nature of the GaN HFET rather than by doping the device as would be the case with GaAs transistors [2,3]. The polar nature of the atomic bonds in GaN leads to bulk material where the top side is terminated with either Gallium atoms (Ga-face) or with Nitrogen atoms (N-face). This leads to either a net charge at the surface of the material, which is negative for Ga-face and positive for N-face material. In general Ga-face material is used for the growth of GaN HFETs, however there has been recent research interest in the possibilities of using N-face material. In addition to the charge generated by this spontaneous polarisation, further charge is generated by the tensile strain induced in the material by the lattice mismatch between the GaN and the AlGaN [2,3]. This is referred to as the piezoelectric effect.

Gallium Nitride can be grown using either Metal Organic Chemical Vapour Deposition (MOCVD) or Molecular Beam Epitaxy (MBE) on top of a substrate and buffer layers. There are three possible substrates available for GaN HFETs Sapphire (Al_2O_3), Silicon Carbide (SiC) and Silicon (Si). The favoured choice is SiC due to its excellent thermal properties allowing much higher power densities to be achieved. However GaN HFETs grown on Si are achieving reasonable performance at a lower cost [1].

Once the growth of the AlGaN is completed metal contacts are deposited on top, for the drain and source these are ohmic contacts but for the gate a

Schottky contact is formed. It is this Schottky contact that allows a depletion region to be formed, and the current flow through the 2DEG to be controlled.

As with other device technologies if the periphery of the gate fingers is increased then the drain current that the device produces will also be increased. The convention is to label the dimensions of the transistor with respect to the direction of current flow, so the electrons flow along the length of the gate. Therefore to increase the periphery of the device (and therefore drain current) either the number of gate fingers can be increased or the width of the fingers can be increased.

2.2.1 Devices Used in This Thesis

All of the measurements in this thesis were carried out on devices from the same wafer (from QinetiQ, designated as Possum) with a gate width of either 2x50μm or 2x100μm and gate length of 0.6μm, an example of the 2x100μm device can be seen in figure 2.2. All of the measurements were carried out ‘on-wafer’ requiring the use of microwave wafer probes. The small gate periphery of these devices means that the RF output power is well below the power limits for the on-wafer RF IV waveform measurement system and also minimises the thermal resistance and hence reduce the effect of self-heating.

The epitaxial layer structure is 25nm of undoped AlGaN grown on top of 1.9 μm Iron (Fe) doped GaN which were grown by MOVPE on semi-insulating SiC. The devices have a Schottky gate metallisation of Nickel/Gold (Ni/Au) and the ohmic contacts used Titanium-Aluminium-Platinum-Gold (TiAlPtAu) yielding a contact resistance of 0.4ohm.mm. The device was passivated with Silicon Nitride (SiN), over the top of which a source connected field plate was deposited (passivation and field plates are described further in section 4.3.1.5). Excellent pulse IV behaviour was obtained indicating good control of current collapse as shown in figure 2.3. Measurements showed that the pinch off voltage of the devices is -5V. The thermal resistance of the 2x50μm device is 6.38Kmm/W (63.8K/W) and 7.11Kmm/W (35.55K/W) for the 2x100μm device [4].

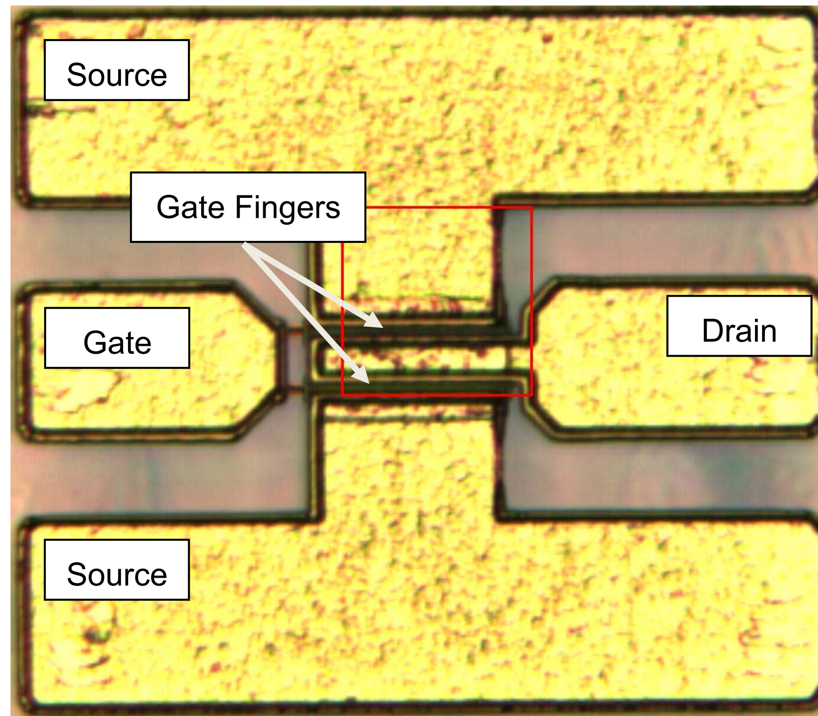


Figure 2.2 - Picture showing an example of the 2x100µm GaN HFET devices used in this thesis

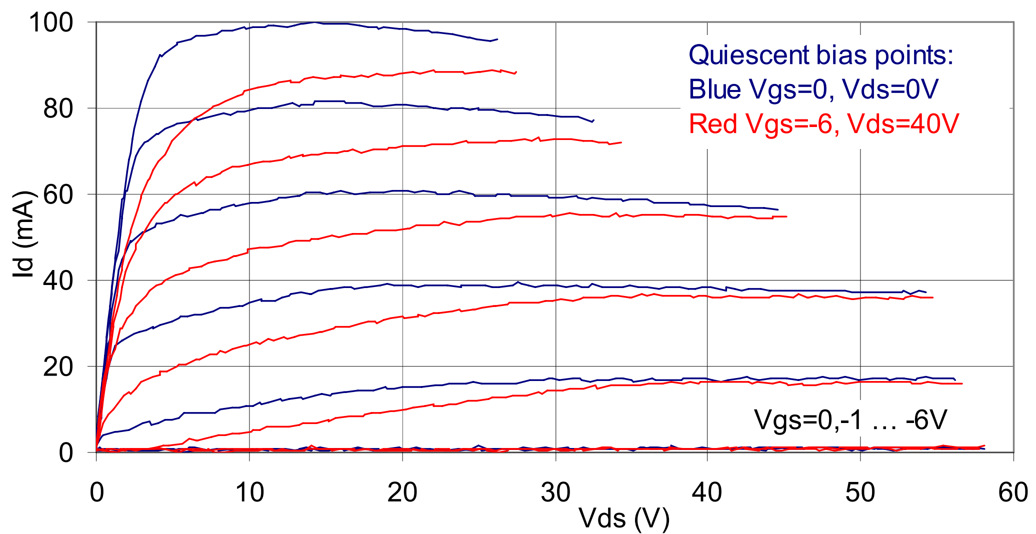


Figure 2.3 - Pulse IV measurements from bias points of V_{GS}=0V,V_{DS}=0V and V_{GS}=-6V (pinch off),V_{DS}=40V, for a 2x50 µm device

2.3 Characterisation Measurements

In RF PA design it is desirable to have a first pass design methodology, where the first design manufactured meets the requirements and post production tuning is not needed. In order to achieve this it is necessary to undertake comprehensive characterisation measurements of the device that is to be employed in the RF PA design. As will be seen in chapter 4, GaN HFETs can still be hampered by severe performance issues such as DC-RF dispersion and reliability. The characterisation measurements used for RF PA design can also be applied to device manufacturing, allowing extensive feedback early in the production cycle in order to identify any of these potential performance issues. This section discusses the device characterisation measurements, used in this thesis, that are relevant to PA design. In chapter 4 this description is extended to include how these measurements, and others, can be used for the purposes of device design and reliability.

2.3.1 DC Measurements

The most commonly used device characterisation methods involve only DC measurements, the relative simplicity of which allows for simpler, cheaper measurement setups. There are many different DC characterisation measurements used by both PA designers and device manufacturers, but those that are most used in RF PA design (and the majority of this thesis) are those that map the IV operating areas of the device. These are the transfer characteristic (drain current vs. gate voltage, figure 2.3) and the DCIV (drain current vs. drain voltage, figure 2.4), although the input characteristic also falls into this category it is generally more often used during reliability measurements so is described in section 4.2.3. These measurements are performed by either sweeping the gate voltage at different values of drain voltage (transfer characteristic) or the drain voltage at different values of gate voltage (DCIV). It is also worth pointing out that the devices' turn on voltage, known as the threshold voltage (V_{TH}) can be seen on the transfer characteristic making it useful for reliability characterisation measurements.

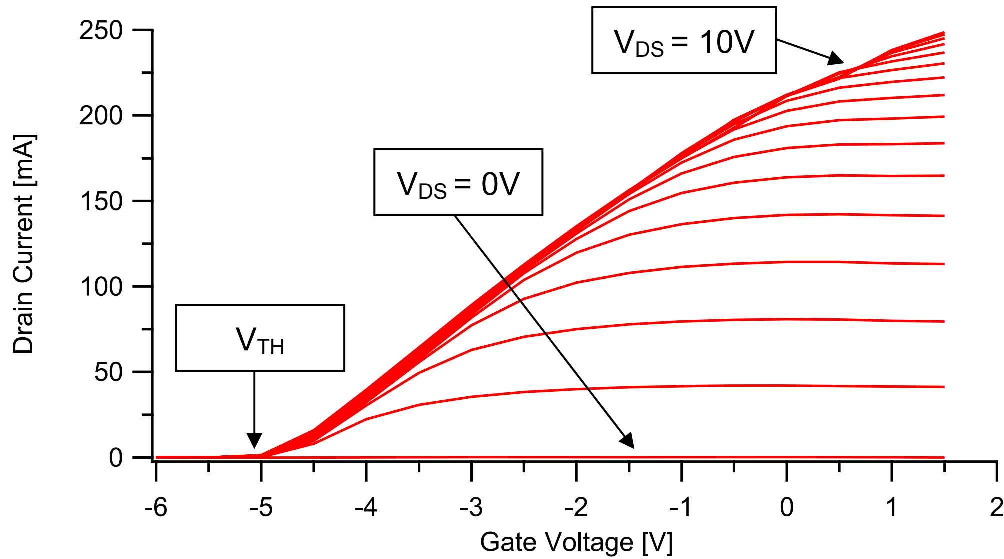


Figure 2.4 - Transfer characteristic of a 2x100μm GaN HFET

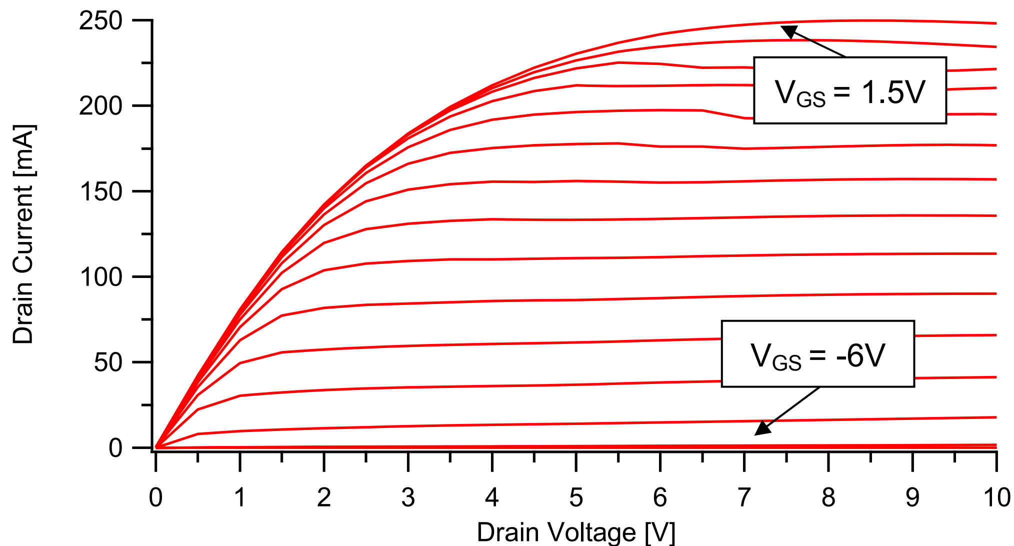


Figure 2.5 - DCIV measurement of a 2x100μm GaN HFET

During DC characterisation measurements there will be no RF output power generated by the device, consequentially all of the applied DC power will be dissipated across the device. Therefore care must be taken not to exceed the DC power that the device is capable of handling, or there is a risk of damaging or destroying the device.

Care must also be taken when interpreting the results of DC measurements for use in designing RF PA. GaN HFETs suffer from dispersive effects, which cause a difference in the RF performance of the device from that predicted by the DC measurements. Also as previously

mentioned all of the power is dissipated across the device during these measurements which can lead to the device getting hot, further skewing the measurements. This self heating is especially prevalent in the high voltage high current region of the DCIV measurements and with large devices that are capable of passing a large amount of current.

DC characterisation measurements are also commonly used in reliability studies, both as before and after characterisation measurements and as the stressing mechanism of the test. These types of measurements are described further in the reliability literature review in chapter 4.

2.3.2 Pulsed IV Measurements

As described in section 2.2, GaN HFETs suffer from dispersion which causes differences in the RF measurements compared to the DC predictions. Pulsed IV measurements offer both a solution and insight to this issue by measuring the dynamic IV characteristics of a device as opposed to the static or DCIV response [5]. In general pulsed IV measurements are very similar in nature to the DC measurements described previously; however instead of holding constant input and output voltages on the device the voltages are pulsed from a quiescent bias point. If the duty cycle of the pulses is made suitably short, and a suitable bias point chosen, then the dynamic IV characteristic that is generated can be used as an indicator of the RF IV performance of the device. An example of pulsed IV measurements taken at different bias points can be seen in figure 2.3.

2.3.3 Small Signal RF Measurements

Scattering- (or S-) parameter analysis can be used to describe the electrical behaviour of a network. It is not important what this network is comprised of, but only that it has a linear response to any input stimulus. S-parameter analysis can be performed on networks with any number of ports, at each of which there is an incident and a reflected voltage travelling wave. Equation 2.1 shows how the S-parameter matrix relates the incident voltage travelling wave (A waves) at each port to the reflected voltage travelling

waves (B waves). For an N port network there will be N^2 S-parameter terms, each of which is a complex number representing the relationship between the reflected voltage travelling wave at a specific port (B_n) and the incident travelling wave at a specific port (A_m) [6].

$$\begin{bmatrix} B_1 \\ \vdots \\ B_n \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1m} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nm} \end{bmatrix} \times \begin{bmatrix} A_1 \\ \vdots \\ A_m \end{bmatrix} \qquad (2.1)$$

Generally S-parameter analysis is limited to networks with as few ports as possible in order to simplify the analysis. A further simplification can be made when characterising a network using S-parameters which is to only supply one incident (A) wave to the network at a time. This then allows for the reflected (B) waves from each port to be measured, and from this each of the S-parameters can be calculated.

For the purpose of this thesis only one port and two port networks will be considered, and these are described in the next two sections.

2.3.3.1 One Port Network

For a one port network, such as the impedance shown in figure 2.5, equation 2.1 simplifies so that there is only a single S-parameter, S_{11}. This provides a description of the amplitude and phase of the reflected voltage travelling wave compared to the incident wave. This is calculated as shown in equation 2.2, where $\boldsymbol{\Gamma}$ is the voltage reflection coefficient, A_1 is the incident travelling wave and B_1 is the reflected travelling wave. The reflection coefficient can also be calculated from the load impedance (Z_{Load}) and the system impedance (Z_s, usually 50Ω), as shown in equation 2.3.

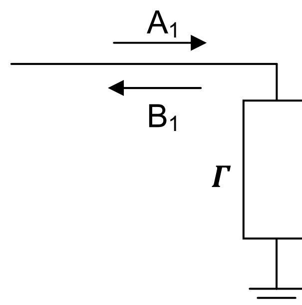


Figure 2.6 - A simple one port network

$$S_{11} = \Gamma = \frac{B_1}{A_1} \quad (2.2)$$

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S} \quad (2.3)$$

From these it can be seen that, if the load impedance is equal to the system impedance, called an impedance match condition, then the reflection coefficient will be zero ($|\Gamma|=0$). Therefore there will be no reflected voltage travelling wave. However if the impedance of the load is not matched ($|\Gamma|\neq0$) then there will be a reflection coefficient and therefore a reflected voltage travelling wave. The implications of this will be discussed later in this chapter (section 2.5).

2.3.3.2 Two Port Network

For a two port network, such as that shown in figure 2.6, the S-parameter matrix (equation 2.1) will reduce to that shown in equation 2.4.

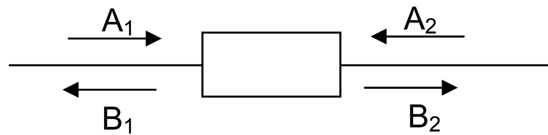


Figure 2.7 - Two port network

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \quad (2.4)$$

As previously discussed, this can be further simplified if during measurement only one of the incident (A) voltage travelling waves is applied at a time. This allows for each of the four S-parameters to be calculated as shown in equations 2.5 - 2.8, where

S_{11} is the input voltage reflection coefficient (Γ_1), when A_2=0

$$S_{11} = \Gamma_1 = \frac{B_1}{A_1} \quad (2.5)$$

S_{12} is the reverse voltage gain, when A_1=0

$$S_{12} = \frac{B_1}{A_2} \quad (2.6)$$

S_{21} is the forward voltage gain, when A_2=0

$$S_{21} = \frac{B_2}{A_1} \quad (2.7)$$

S_{22} is the output voltage reflection coefficient (Γ_2), when A_1=0

$$S_{22} = \Gamma_2 = \frac{B_2}{A_2} \quad (2.8)$$

As would be expected, the input and output reflection coefficients are identical to those described for one port networks.

For a passive network the forward and reverse gains will be equal in most cases and both will be less then unity. For an active network (such as a transistor) the gain can be higher than unity, if desired. As previously mentioned the network being analysed must be linear, so when a transistor is being characterised low power levels must be used in order to keep the device in the linear region.

2.3.4 Large Signal RF Measurements

As previously discussed the devices used in RF PAs are nonlinear and this nonlinearity is often employed to achieve the high efficiency operating conditions that are demanded. To truly characterise the device and its nonlinearities large signal RF measurements must be used. The simplest large signal measurements are those that involve measuring the input and output power of the device. From these measurements, and DC measurements of the quiescent bias point, the PA's gain and efficiency can be calculated. The gain of the device, as shown in equation 2.9, where the input and output power are expressed in watts.

$$Gain = \frac{P_{out}}{P_{in}} \quad (2.9)$$

The transistors efficiency (η), which is defined as the amount of the supplied DC power (P_{DC}, calculated as shown in equation 2.10) that is converted into RF power (P_{out}), this is shown in equation 2.11. However this does not take into account the input drive power of the PA. If the gain of the PA is low, then the input power can be relatively high compared to the output power. The Power Added Efficiency (PAE) takes this into account in the calculation, as shown in equation 2.12 [7].

$$P_{DC} = I_{DC}V_{DC} \quad (2.10)$$

$$\eta = \frac{P_{out}}{P_{DC}} \quad (2.11)$$

$$PAE = \frac{P_{out}-P_{in}}{P_{DC}} \quad (2.12)$$

The dissipated, or waste, power (P_{Diss}) in a device that is not converted into RF power is described in equation 2.13. This is usually dissipated as heat. The static junction temperature of the device can be calculated as in equation 2.14 where T_j is the static junction temperature, T_a is the ambient temperature (25°C for this thesis), P_{Diss} is the power dissipated in the device and R_{therm} is the thermal resistance of the device [4].

$$P_{Diss} = P_{DC} - P_{RFout} = P_{DC}(1-\eta) \quad (2.13)$$

$$T_j = T_a + P_{Diss}R_{therm} \quad (2.14)$$

However, in order to truly show the operating conditions of an RF device the RF voltage and current waveforms at the terminal of the device must be known. These can be calculated from the voltage travelling waves using equations 2.15 and 2.16, where Z_s is the system impedance of 50Ω. However in order to produce the waveforms it is important that not only the amplitudes of the travelling waves are measured but also the relative phases.

$$V = (A+B)\sqrt{Z_s} \quad (2.15)$$

$$I = \frac{A-B}{\sqrt{Z_s}} \quad (2.16)$$

The instantaneous RF power can be calculated from equation 2.17, where v(t) and i(t) are the time varying RF voltage and current waveforms.

$$p(t) = v(t)i(t) \quad (2.17)$$

However it is more conventional to calculate the average power over time as shown in equation 2.18, where P is the RF power, V_{RMS} is the RMS and $V_{peak\text{-}peak}$ is the peak to peak of the RF voltage, I_{RMS} is the RMS and $I_{peak\text{-}peak}$ is the peak to peak value of the RF current.

$$P = V_{RMS}I_{RMS} = \frac{V_{peak-peak}\, I_{peak-peak}}{8} \quad (2.18)$$

The ability to measure RF waveforms at the ports of a device can be complemented with the ability to present arbitrary impedances to these ports. This can be achieved by using RF source or load pull techniques. As discussed in section 2.3.3.1 (on the S-parameter analysis of one port networks), a load impedance will have a voltage reflection coefficient which will determine the portion of the incident travelling voltage wave (in this case the wave coming from the device, B_2) that is reflected back towards the device (A_2). This is shown in figure 2.7 and equation 2.19, the reflection coefficient needed to represent a specific load impedance can be calculated using equation 2.3. The theory behind all load pull techniques is to control this load reflection coefficient in order to set the impedance that the device sees.

$$A_2 = \Gamma B_2 \tag{2.19}$$

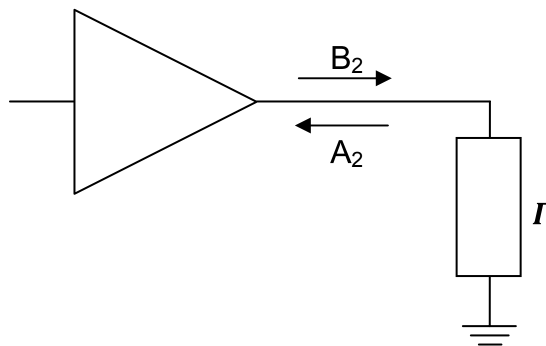


Figure 2.8 - RF device with an arbitrary load impedance and the voltage travelling waves labelled

2.3.5 RF IV Waveform Measurement System

The practical realisation of the RF waveform measurement system is shown in figure 2.8. The system features either an Agilent Microwave Transition Analyser (MTA) or a Tektronix Digital Sampling Oscilloscope (DSO) in order to measure the voltage travelling waves [8,9]. The system used for the measurements in this thesis uses the MTA, therefore this is the only instrument that will be referred to from now on.

The MTA uses the sub-sampling method where a single RF waveform measurement is built up over multiple RF cycles. This is achieved by using a

trigger signal that is slightly offset from the fundamental frequency of the waveform being measured. Due to the MTA only having two input receivers a network of switches was used to make three individual measurements, one of the input travelling waves, one of the output travelling waves and a measurements of the A_1 and B_2 travelling waves. This final measurement is needed in order to relate the phases of the input and output travelling wave measurements.

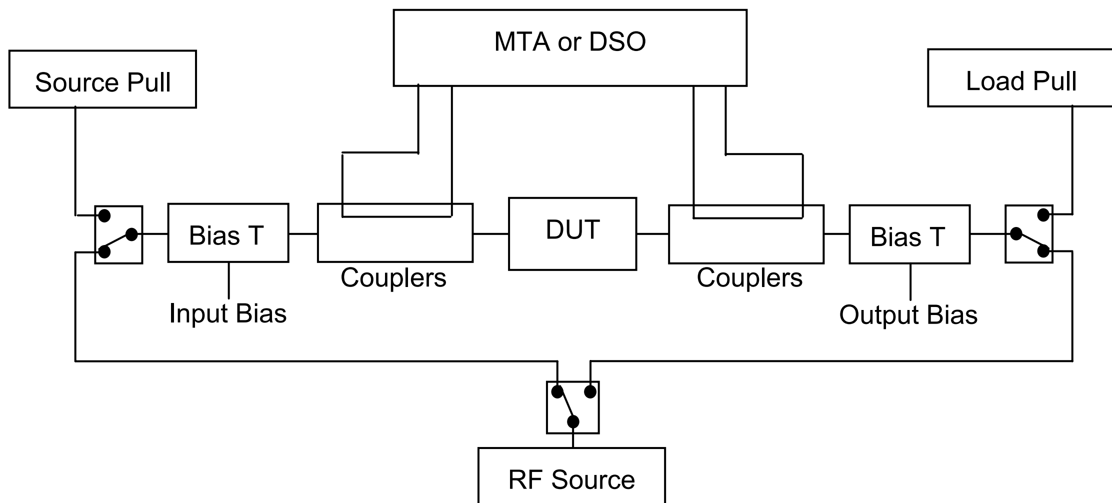


Figure 2.9 - RF IV waveform measurement system

It is important that a calibration is carried out before any measurements are undertaken in order to account for any losses and phase differences in the travelling waves between the device (where we want to know the RF voltages and currents) and the measurements equipment (where the travelling waves are actually measured) [8]. This is done by measuring a series of well defined calibration standards at the place where the device will be connected to the measurement system. These measurements can then be used to calculate the error coefficients of the network in between the terminals of a device and the measurement equipment. This allows any measurements made by the equipment to be related back to the calibration plane at the terminal of the device. In order to carry out on-wafer measurements microwave probes must be used to interface with the devices, the probes used for the measurements in this thesis are Picoprobe

40A-GSG-150-GR [10]. The system can be set up around any probing station and with the use of on-wafer calibration standards can be calibrated and operated as usual. An example of the Cascade Microtech on-wafer calibration standardsa used to calibrate the RF IV Waveform measurement system can be found here [11].

An RF device unavoidably contains many parasitic components that are part of the device structure, and therefore influence how the device operates. Of these it is the drain-source capacitance (C_{DS}) that has the largest effect on the output performance of the device and therefore on the drain RF current waveforms. Figure 2.9 shows the drain-source capacitance and how this relates to the reference planes of the measurements system. Under normal device operation when the device is pinched off there will be no drain current flowing through the channel, at the current generator plane. However the drain-source capacitance has the effect of introducing a reactive current, the effects of which can be seen at the measurement system plane when the device is pinched off. Figure 2.10 shows the same drain current waveform for a 2x100μm GaN HFET before and after de-embedding for a C_{DS} value of 0.08pF, from which the effect of the capacitance can clearly be seen. It is also important to note that due to its reactive nature the effect of this capacitance will increase at higher frequencies.

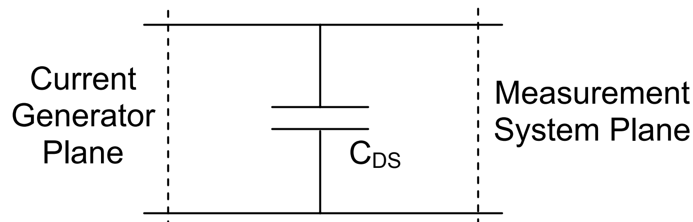


Figure 2.10 - Drain-Source capacitance and measurement planes

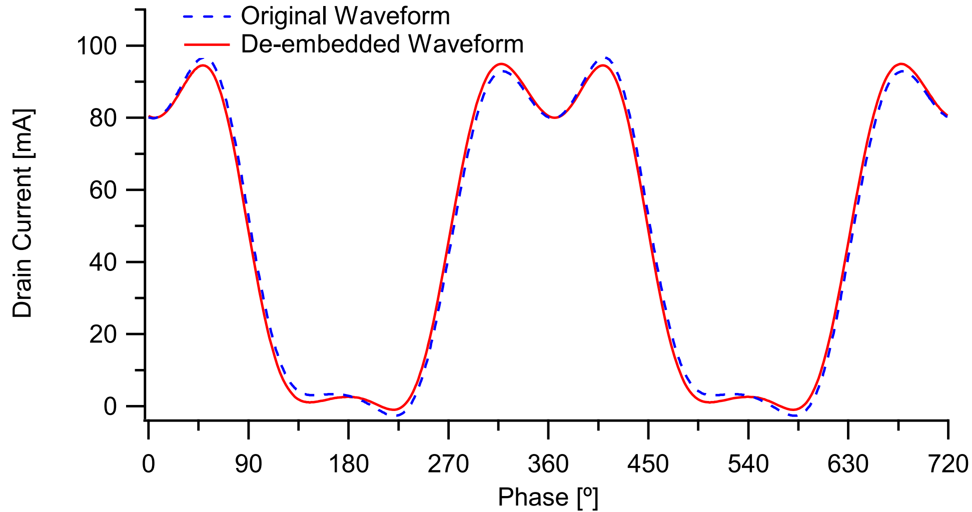


Figure 2.11 - Drain current waveform before and after de-embedding for a 2x100µm GaN HFET at fundamental frequency of 0.9GHz and C_{DS} of 0.08pF

As already mentioned the ability to measure RF IV waveforms can be complemented with the ability to manipulate these waveforms using RF load pull, often referred to as RF waveform engineering. In order to create high efficiency PA designs multiple frequencies (fundamental and harmonics) must be characterised. In order to achieve this, filters must be used in order to send the different frequencies to the different load impedances.

Broadly, there are two categories of load pull system – passive and active. Passive load pull systems, such as the one shown in figure 2.11, use mechanical tuners to transform the travelling voltage wave coming from the device in order to generate the required reflection coefficient. This is what is referred to as a close loop system, where the voltage travelling wave coming from the device (B_2) is manipulated to create the voltage travelling wave that is incident upon the device (A_2). However because of the passive nature of these systems the reflection coefficients that can be generated by them are limited by the loss inherent in the system. However, these systems are widely used in industry due to their high speed and reliability which come from the closed loop nature of the system. This allows for instantaneous changes in the reflected voltage travelling wave (A_2) if the incident travelling wave changes (B_2) [12].

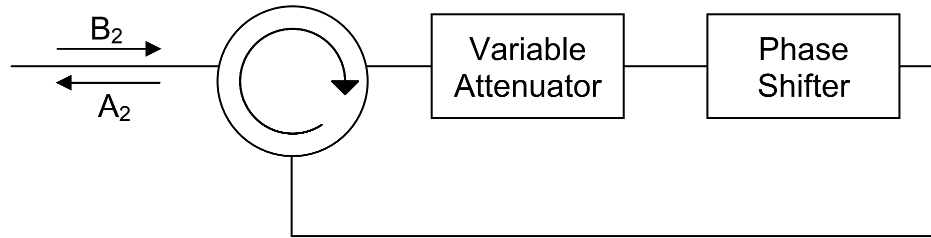


Figure 2.12 - Architecture of a passive closed loop load pull system

Active load pull systems use amplification in order to avoid the problem of restricted reflection coefficient found in passive load pull systems. Open loop systems, such as the one shown in figure 2.12, present 50Ω to the device in order to absorb all of the voltage travelling wave that comes from the device (B_2). The voltage travelling wave required to present a specific reflection coefficient to the device (A_2) is then regenerated by the signal generator [13]. However due to the open loop architecture of the system the load presented to the device is now dependant on the power level. This makes these systems slow, as every time the incident travelling wave changes the load must be re-calculated.

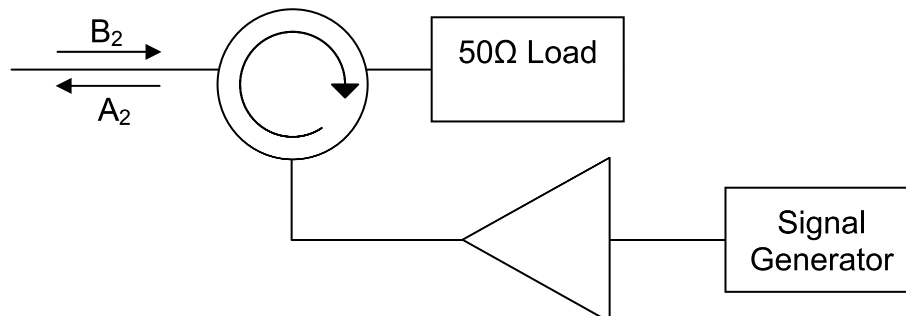


Figure 2.13 - Architecture of an active open loop load pull system

Closed loop active load pull systems exist, and are similar to the passive load pull system shown in figure 2.11 with the addition of an amplifier within the load pull loop [14]. However these systems can be prone to RF oscillation.

The Envelope Load Pull (ELP) system combines the benefits of a closed loop load pull system with the benefits of active open loop load pull. This allows for a power level invariant load impedance to be set without the loss

constraints of a passive load pull system. In addition because the loop is only closed at baseband frequencies this prevents the potential for RF oscillation [15]. The architecture for an ELP module is shown in figure 2.13, where the Local Oscillator (LO) and the modulator are contained within an ESG signal generator.

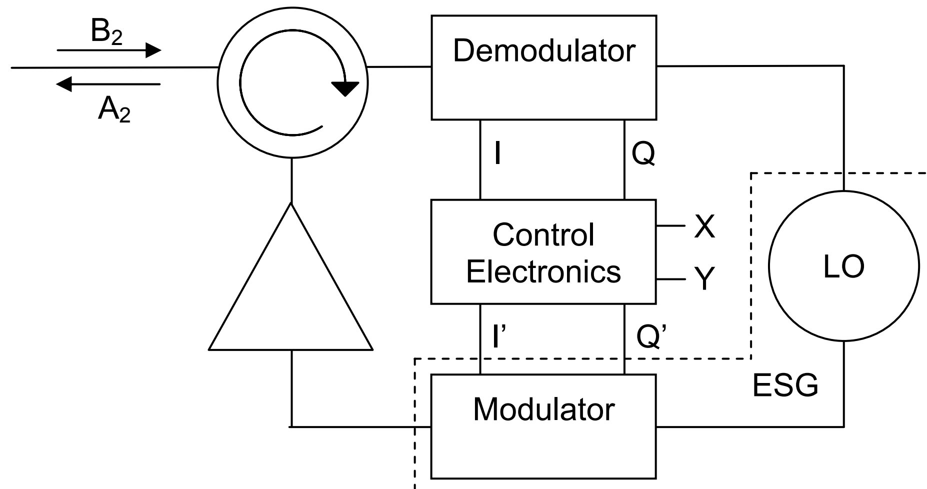


Figure 2.14 - Architecture of an Envelope Load Pull system

In the waveform measurement system used in the measurements in this thesis there are three of these ELP modules, one used for the fundamental, one for the second harmonic and one for the third harmonic.

2.3.6 RF IV Waveform Characterisation Measurements

This combination of RF load pull and IV waveform measurement allows the realisation of first pass design as devices can be tested under the exact conditions found in the PA operating mode before any circuitry is manufactured [16,17]. From a device design view point, these measurements can also provide valuable information about any potential problems, and if conducted early in the device design cycle will allow these problems to be rectified.

The RF output power can be calculated as shown in equation 2.18, from which it can be seen from that in order to achieve the maximum power both the RF voltage and RF current swings need to be maximised. This is achieved by setting the load impedance of the device so that the trajectory of

the load line is directed into the knee region of the IV plane, as in the idealised case in figure 2.14.

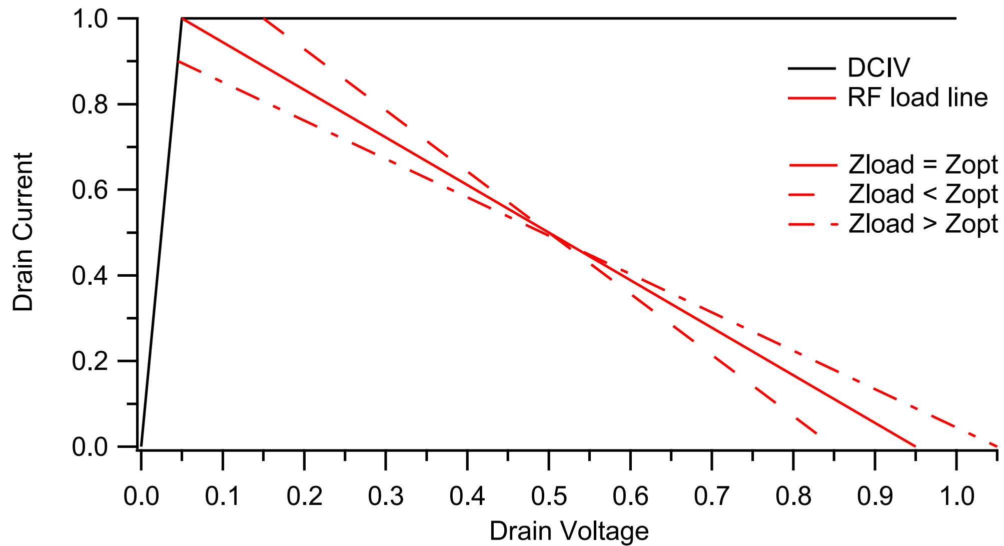


Figure 2.15 - Idealised load line trajectories for a class A amplifier with the load impedance set at the optimum impedance, less than the optimum impedance and greater than the optimum impedance

Here the effect of the knee can be seen to increase the minimum drain voltage that is possible whilst still attaining the maximum drain current. This also has the effect of reducing the maximum drain voltage, therefore decreasing the overall drain voltage swing by double the knee voltage. It can also be seen from this idealised case that at load impedances with lower magnitudes values than the optimum real impedance the peak RF drain current will be limited by the saturation current of the device. These low impedances will also cause the RF drain voltage swing to be lower than those seen at the optimum impedance. However at load impedances with a higher magnitude than the optimum real impedance the higher voltage swings will cause the load lines to interfere with the knee and turn on regions of the device, causing lower peak RF drain currents.

As mentioned in section 2.2, DC-RF dispersion causes discrepancies between the DC and the RF operating areas of the device. This will be described in more detail in chapter 4, however it is worth pointing out here that this dispersion primarily manifests as a drop in the RF drain current in the knee region of the IV operating plane. This limits the achievable RF

drain current and voltage swings and therefore the RF output power of the device. This drop in RF output power can sometimes be partially worked around by increasing the load impedance in order to increase the RF drain voltage swing and therefore the RF output power.

These RF measurements can be extended by investigating multiple input power levels or load impedances in order to find the optimum operating conditions for the device. Figure 2.15 shows an input power sweep performed on a 2x50µm GaN HFET. From this it can be seen that at an input power of 5 dBm the gain begins to show compression and the output power begins to saturate. Then at an input power of 8dBm there is peak efficiency and output power, this is what is referred to as saturated RF output power or P_{Sat}. Additionally, as the RF IV waveforms have been measured, it can be seen that it is the saturation of the RF drain current that causes the saturation in RF output power. This is shown in figure 2.16, which shows the maximum and minimum RF drain current and voltages.

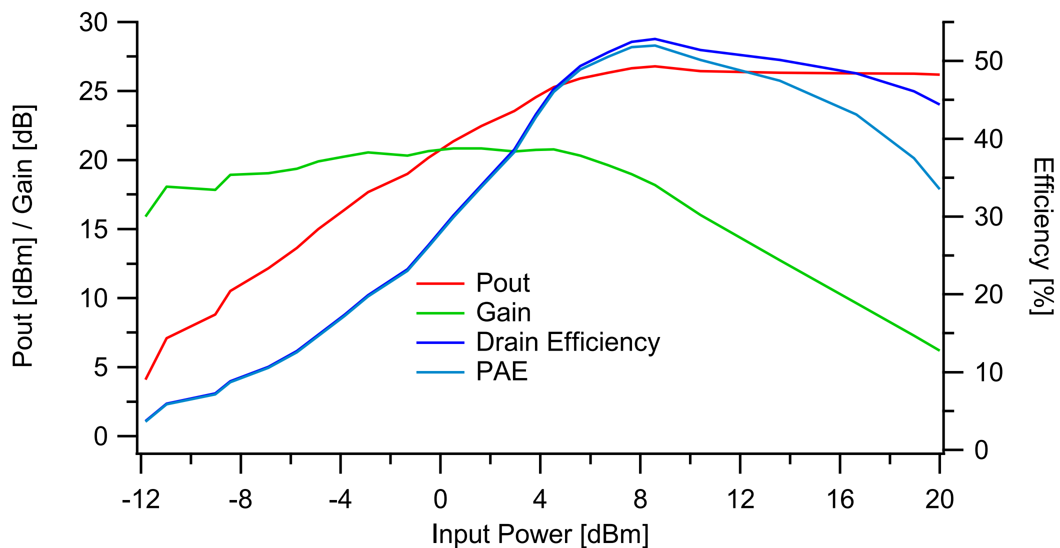


Figure 2.16 - Output power, gain, efficiency and PAE during an input power sweep performed on a 2x50µm GaN HFET operating in class B mode (V_{GS}=-5V) at a drain bias of 30V

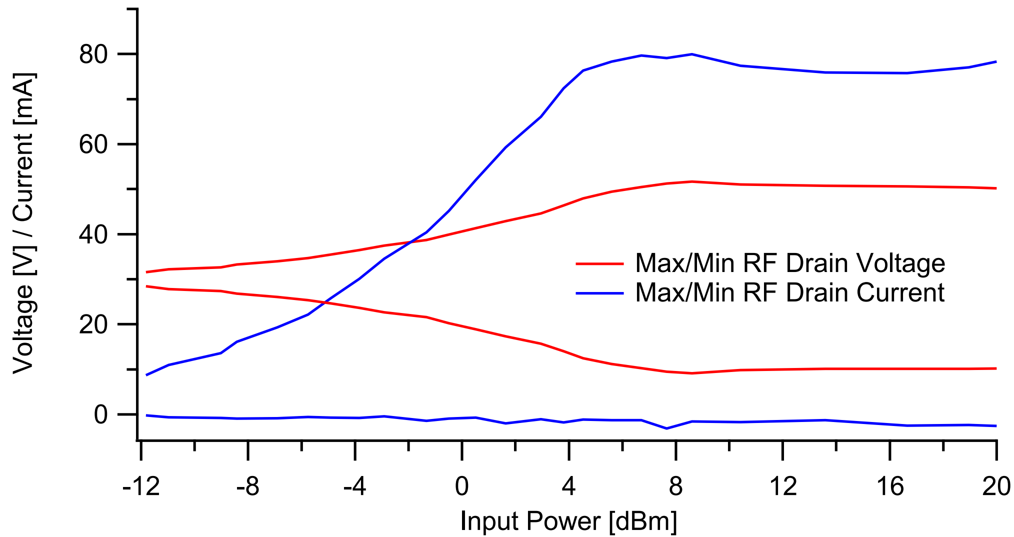


Figure 2.17 - Maximum and minimum RF drain voltage and current from during the power sweep shown in figure 2.15

Alternatively, the load impedance can be swept at a fixed input power. Generally only the fundamental frequency is of interest; however there are occasions where other harmonic impedances are the ones that a designer is interested in. Figure 2.17 shows a fundamental load impedance sweep on a 2x50μm GaN HFET, where the optimum impedance was shown to be 350Ω. It should be noted that it is unusual for a load impedance sweep to cover the entire Smith chart, the range of load impedances will usually be limited by device stability and temperature concerns.

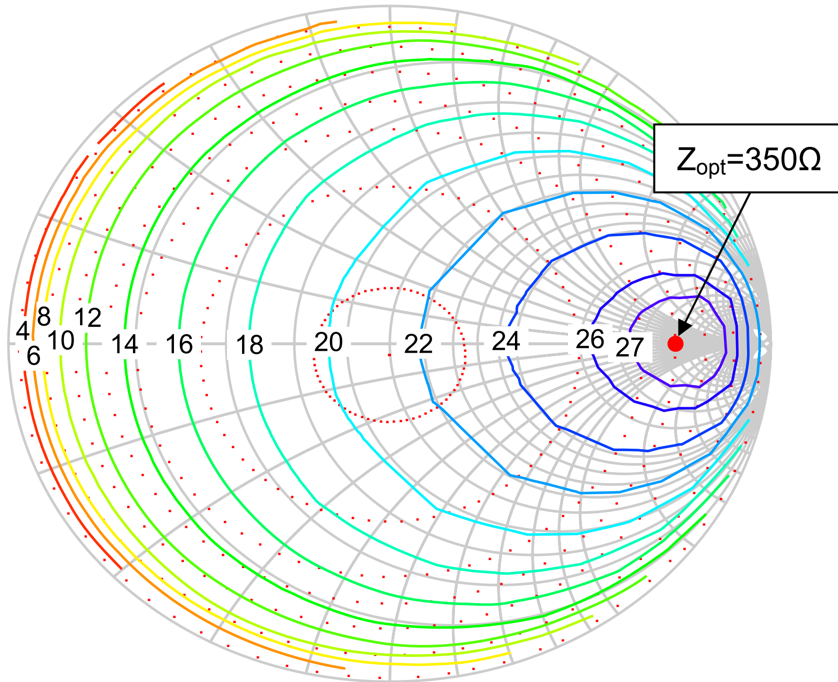


Figure 2.18 - Output power during a fundamental load impedance sweep on a 2x50µm GaN HFET operating in class AB mode (V_{GS}=-3.5V) at a drain bias of 30V. Also shown are the load impedance points measured during the sweep and the optimum impedance at 350Ω.

In addition to these more standard measurements, other unique measurements can be carried out that are only possible with RF IV waveforms. An example of these is the fan diagram, which shows the constraints of a device's RF operating area, such as the one shown in figure 2.18 [18]. A fan diagram consists of a sweep of real fundamental load impedance. In this case the second and third harmonic load impedances are set to be the same as the fundamental during the sweep in order to reduce the looping usually seen at end of the RF load lines.

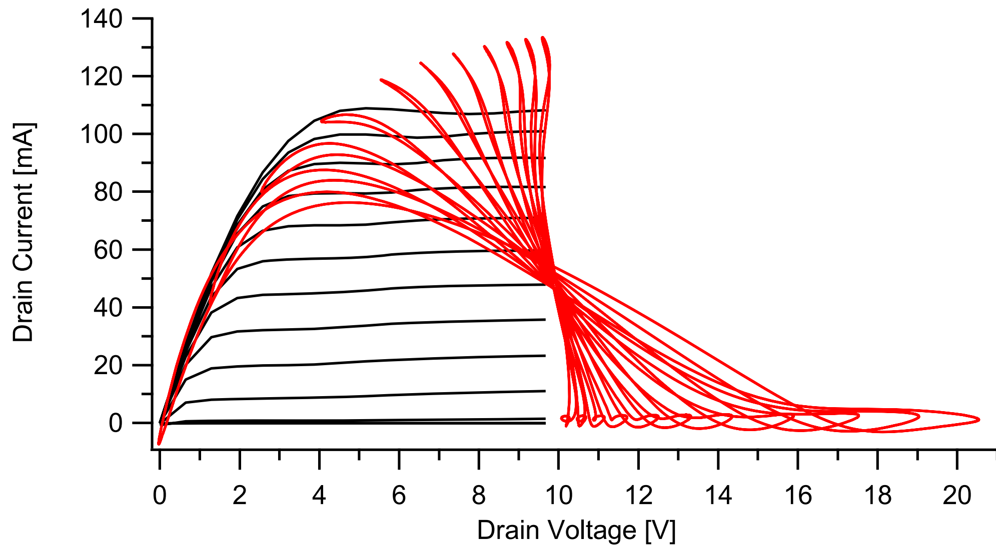


Figure 2.19 - Fan diagram measurement at a drain bias of 10V, along with a DCIV measurement both performed on a 2x50μm GaN HFET

It was shown by McGovern et al. that fan diagrams display the same operating area for the device as pulsed IV's, when the bias point of the measurements are correctly set [19]. It was also shown here that care must be taken when selecting the bias point for the pulsed IV measurements, as during RF operation the device will often 'self-bias' resulting in a quiescent drain current irrespective of the original bias point. This self-biasing results from the saturation of the RF drain current waveform leading to modification of the DC or average drain current.

2.4 Amplifier Modes

The operating efficiency of an RF PA is a constant concern for PA designers; with modern “green thinking” the need to reduce wasted power is becoming ever more important. This has led to the development of more complex PA operating modes, many of which utilise a transistors inherent nonlinearity to produce high efficiency operation. This has become one of the key roles for the RF IV waveform measurement system as it is essential to engineer the exact operating conditions of the device in order to achieve the highest efficiencies. It has also been found that it is the voltages and currents at the current generator plane within the device that define the efficiency rather than those at the terminals of the device [7]. It is therefore necessary to de-embed the waveforms to take into account the drain-source capacitance of the device when designing high efficiency RF PA.

Before describing the high efficiency modes it is first important to describe the more traditional modes of operation. It is also important to note the analysis in the following sections is for idealised devices and with no saturation in the output power.

2.4.1 Basic Modes of Operation

There are four basic amplifier modes of operation where the mode is predominantly set by the conduction angle. Conduction angle is the proportion of the input waveform that the device is conducting output current. This is set by the quiescent bias of the output current, which in turn is related to the input bias of the device and also the saturation of the output current. In order of decreasing conduction angle these are class A, AB, B and C and are shown in table 2.2 [7].

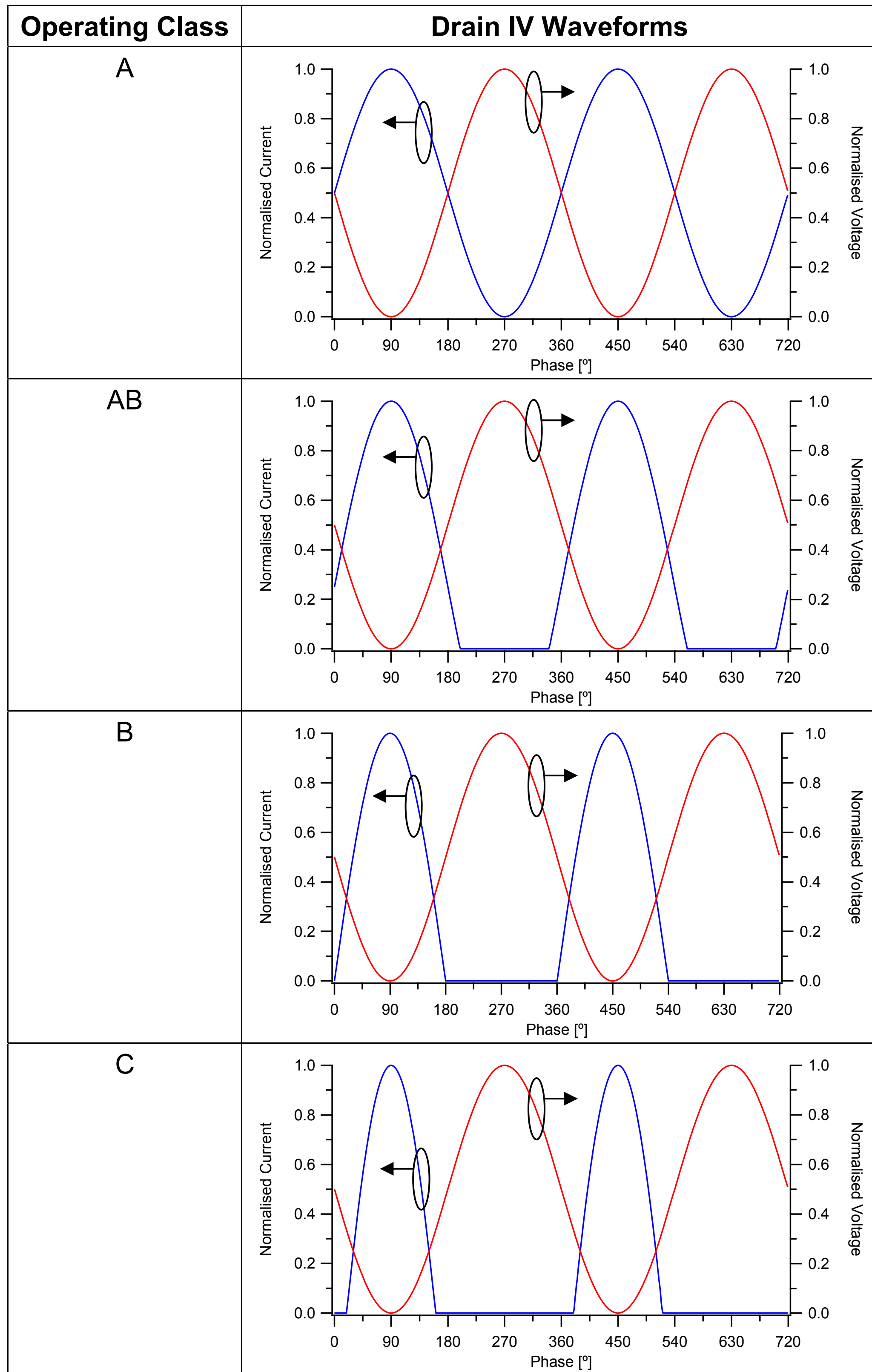
From this it can clearly be seen that as the conduction angle decreases the efficiency of operation increases. This is because as the output current waveform begins to clip against the zero current boundary the DC component of the waveform is mathematically reduced, resulting in an increase in the efficiency of operation as per equation 2.11.

Table 2.2 - Basic RF PA operating modes

Operating Class	**Drain Bias Point**	**Conduction Angle (α) (°)**	**Theoretical max. Drain Efficiency (%)**
A	$I_{Dmax}/2$	360	50
AB	0 - $I_{Dmax}/2$	180 – 360	50 – 78.5
B	0	180	78.5
C	0	0 – 180	78.5 – 90

The RF drain voltage and current waveforms for these operating modes are shown in table 2.3 where a normalised drain current of 1 corresponds to the devices saturation current and the drain bias voltage is 0.5. In each case the load resistance is adjusted to produce the maximum output voltage swing (normalised to 1) whilst also retaining the maximum output current swing. In addition as the input bias decreases it is necessary to increase the input drive level in order to keep the maximum RF drain current. This results in increasingly negative gate voltages which, as will be discussed in chapter 4, can result in reliability issues.

Table 2.3 - Drain voltage and current waveforms for the basic amplifier operating modes



Operating Class	Drain IV Waveforms
A	
AB	
B	
C	

2.4.2 High Efficiency Operating Modes

The class B operating mode has a maximum theoretical drain efficiency of 78.5%. There have been a variety of methods proposed to increase efficiency beyond this by employing harmonic content in the drain voltage waveforms.

The class J mode of operation [7] utilises reactive components at the fundamental and second harmonic impedances in order to produce a half rectified drain voltage waveform that overlaps with the drain current waveform.

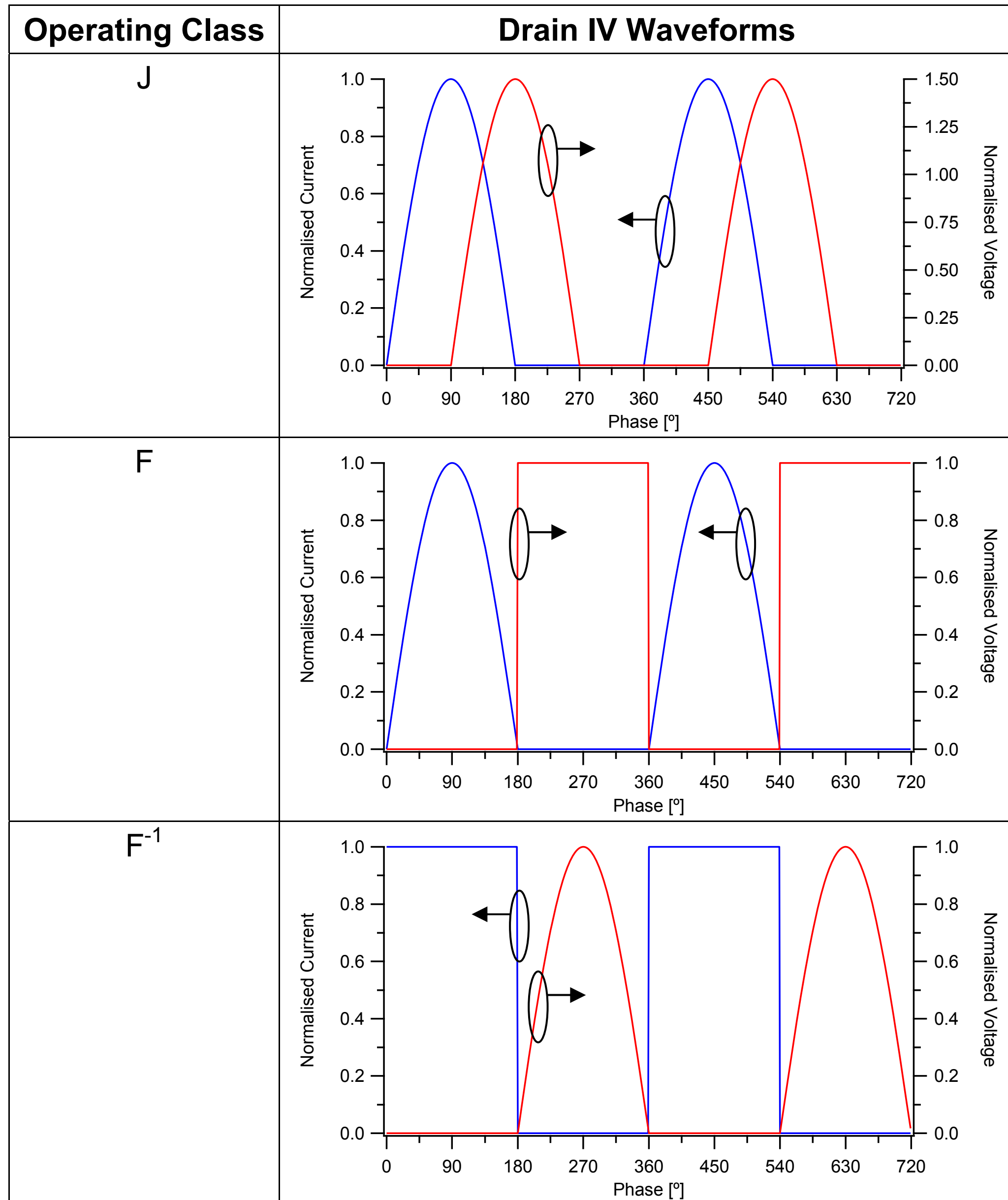
The class F operating mode is based on the class B mode described earlier, with the exception that instead of a sinusoidal drain voltage waveform a square waveform is desired [7]. This square voltage waveform allows for an increased fundamental voltage component, however as the peaks of the square waveform are lower than those of a sinusoidal waveforms the fundamental load resistance must also be increased in order to restore the (now square) voltage waveform to its maximum swing. This increase in fundamental voltage component translates to an increase in the output power produced by the PA, which as the drain bias is unaffected, results in an increase in the efficiency. This is the same for the inverse class F amplifier with the exception that the drain voltage and current waveforms are switched, giving a square drain current waveform and a half rectified drain voltage waveform. This means that in the ideal case the class F and inverse class F modes will give identical performance, however there may be practical issues that necessitate choice of one rather than the other.

Table 2.4 - High efficiency PA operating modes

Operating Class	**Drain Bias Point**	**Conduction Angle (α) (°)**	**Theoretical max. Drain Efficiency (%)**
J	0	180	87 (78.5)
F	0	180	100
F^{-1}	$I_{Dmax}/2$	180	100

In the same manner as the analysis in the previous section, table 2.5 shows the theoretical drain voltage and current waveforms for the class J, class F and inverse class F operating modes.

Table 2.5 - Output voltage and current waveforms for the high efficiency PA operating modes



Operating Class	Drain IV Waveforms
J	
F	
F^{-1}	

The high efficiency modes examined up till now have been restrained in the bandwidth that they can be used over by the necessity to present short or open circuit impedances at the harmonics. However, recently a method has been proposed for defining high efficiency operating modes compatible with operation over a significantly greater bandwidth.

The theory behind these modes of operation is to take either the drain voltage or current waveform and multiply it by equation 2.20, where if $\alpha = 0$ then the waveform will be that from the original mode of operation [20].

$$f(t) = 1 - \alpha\cos(\omega t) \qquad (2.20)$$

This produces a new family of either voltage or current waveforms, all of which produce the same output power and efficiency as the original mode. These continuous modes of operation have generally been based on either the class B or class F/F^{-1} operating modes, both of which will now be considered.

In the case where the original mode of operation is class B, the drain voltage waveform will initially be a sinusoid. Figure 2.19 shows the new family of voltage waveforms that can be produced by a continuous class B amplifier, where α is varied between -1 and 1. It is important to note that the waveforms produced when the magnitude of α is unity, are those of the class J amplifier. The impedances needed in order to generate these voltage waveforms can be calculated, and are shown in figure 2.20.

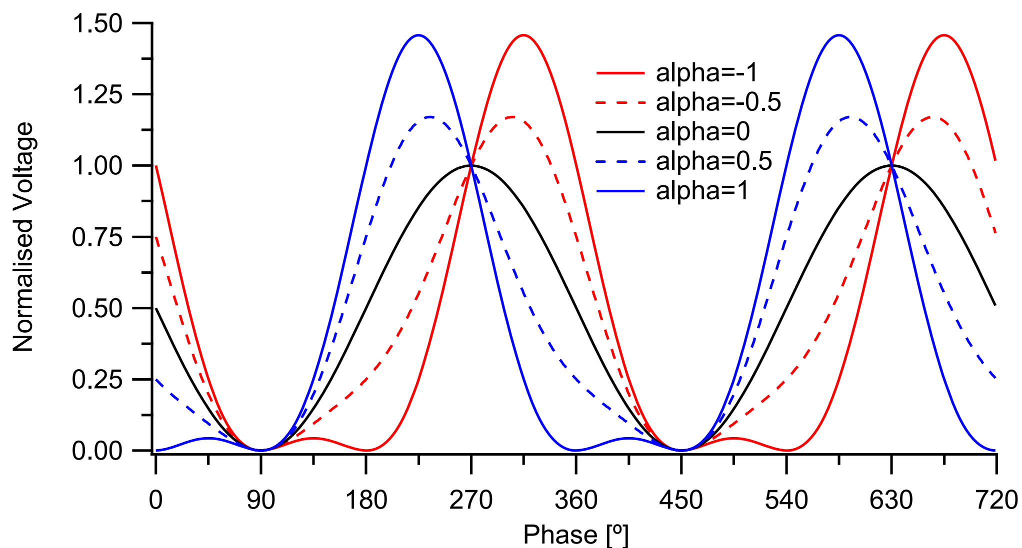


Figure 2.20 - Continuous class B drain voltage waveforms

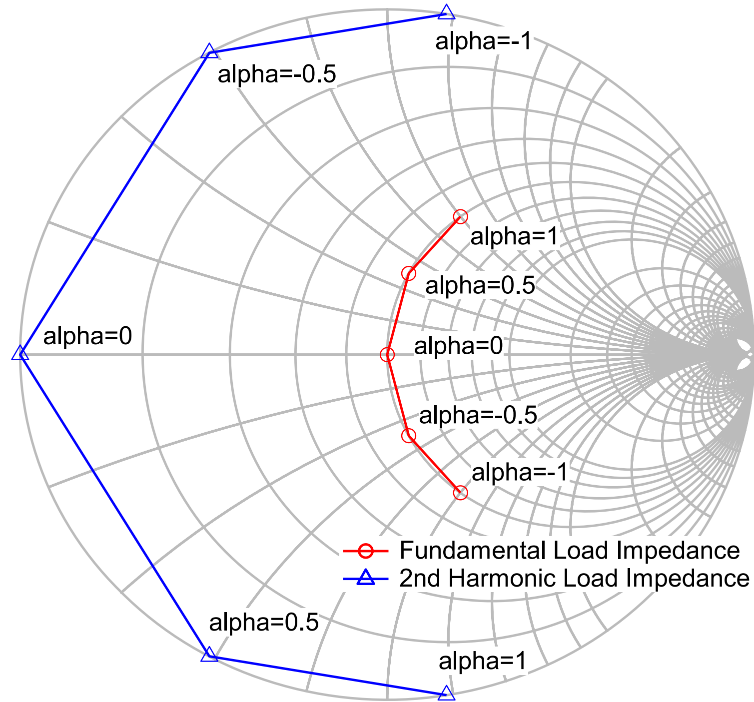


Figure 2.21 - The load impedances of the continuous class B mode

This theory can also be applied to the class F operating mode, where the drain voltage will initially be a square waveform. Figure 2.21 shows the family of drain voltage waveforms produced in the continuous class F mode, when α is varied between -1 and 1. The impedances needed to generate these voltage waveforms are shown in figure 2.22.

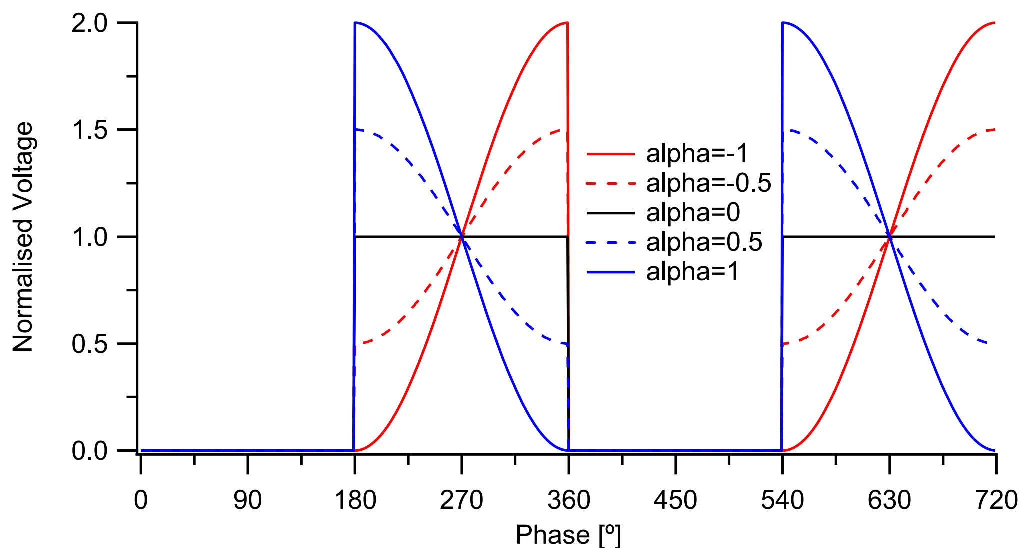


Figure 2.22 - Ideal continuous class F drain voltage waveforms

Figure 2.23 - Ideal continuous class F load impedances

It is worth observing at this point that in both the continuous class B and class F operating modes the output voltage swing has been greatly increased over that seen in the original, reference, operating mode, up to 1.5x in the case of the class J and 2x in the case of the class F. As will be discussed in chapter 4, this increased RF drain voltage swing could have severe reliability implications.

2.5 Impedance Mismatch

In order for a PA to produce the desired performance it must be loaded with the optimum impedance, which is often not the 50Ω system impedance. This is why matching networks are used. Figure 2.23 shows a PA (made up from a device and matching network) with an arbitrary load impedance, where B_2 is the voltage travelling wave leaving the PA (incident upon the load impedance), A_2 is the voltage travelling wave incident upon the PA (reflected from the load impedance) and $\boldsymbol{\Gamma}$ is the load reflection coefficient.

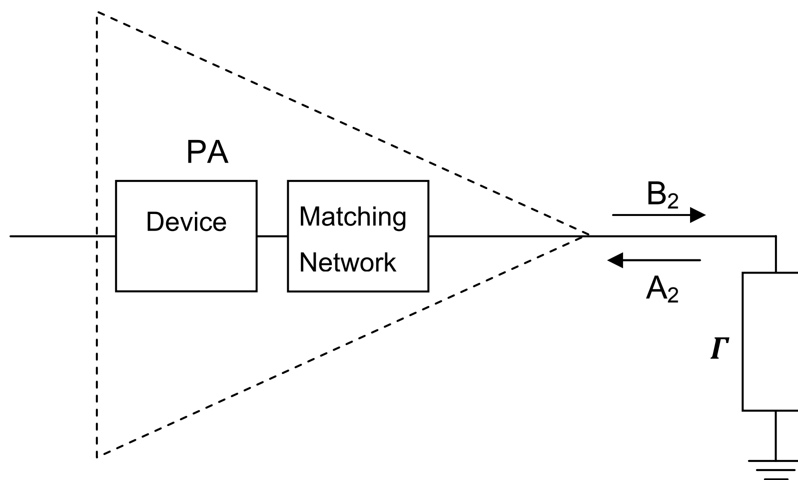


Figure 2.24 - PA and arbitrary load impedance with the voltage travelling waves labelled

In section 2.3.3.1 the s-parameter analysis of one port networks was discussed and that same analysis can now be applied to the load impedance here. In the case where the load impedance is matched ($|\boldsymbol{\Gamma}|=0$) there will be no voltage travelling wave reflected from the load impedance towards the PA. However if the impedance of the load is not matched ($|\boldsymbol{\Gamma}|\neq 0$) then there will be a reflection coefficient and therefore a reflected voltage travelling wave. The worst case scenario here is if the reflection coefficient has a magnitude of 1 ($|\boldsymbol{\Gamma}|=1$), implying that all of the power produced by the PA has been reflected away from the load impedance back to the PA.

In order to visualise the voltage travelling waves that would be present in the circuit in figure 2.23 an idealised simulation was created. In this simulation the assumption was made that the B_2 wave (coming from the device) has a normalized amplitude of one. If the reflection coefficient has a

magnitude of 0.2 then the reflected A_2 wave will have a normalized magnitude of 0.2. These are shown in figure 2.24 over a distance of two complete wavelengths before the mismatch. Also shown is the superposition of these two voltage travelling waves.

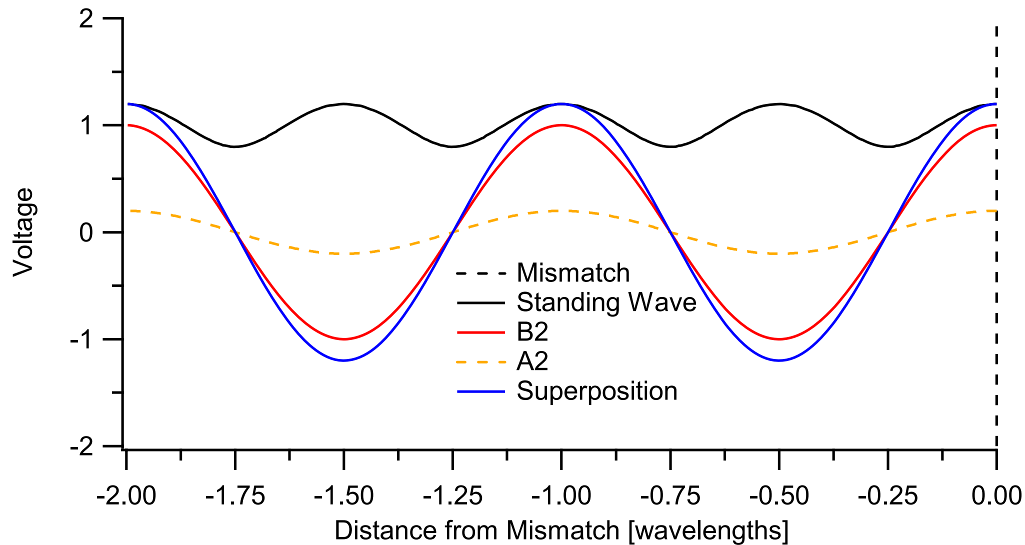


Figure 2.25 - Voltage travelling waves and their superposition for a reflection coefficient magnitude of 0.2 and phase of 0°, also shown is the resulting standing wave

In order to show how these travelling waves interfere with each other, and the standing wave that is produced, the voltage travelling waves can be re-measured at multiple instances in time over one complete waveform time period (every tenth of a period in this case). Then each of the superpositions are plotted, as shown in figure 2.25, from which it can be clearly seen that a standing wave is produced. This standing wave is also shown in figure 2.24.

The ratio of the standing wave, known as the Voltage Standing Wave Ratio (VSWR), can be calculated as shown in equation 2.21. Where V_{max} and V_{min} are the maximum and minimum points of the standing wave and $\boldsymbol{\Gamma}$ is the reflection coefficient of the load impedance [6].

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1+|\Gamma|}{1-|\Gamma|} \qquad (2.21)$$

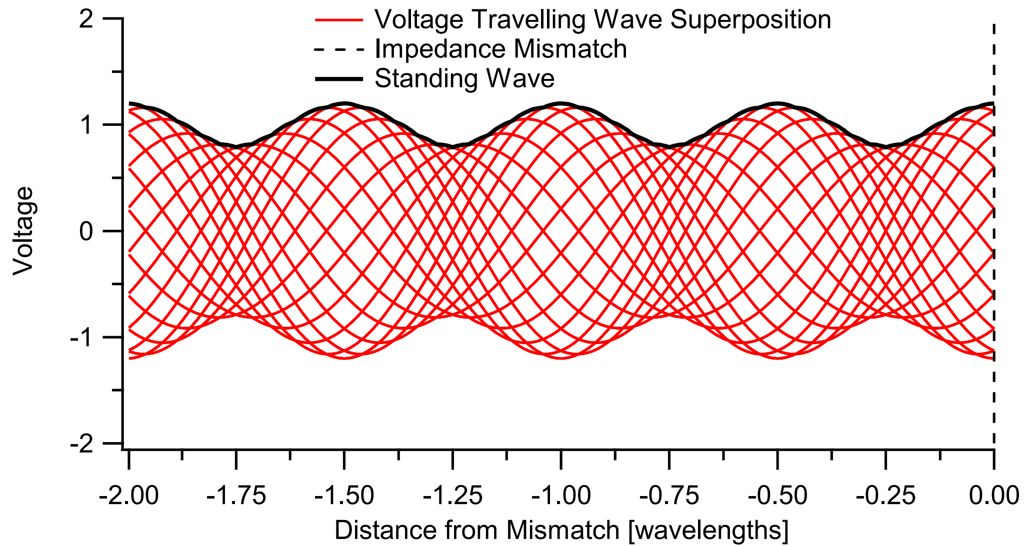


Figure 2.26 - Superpositions of the voltage travelling waves measured every tenth of a waveform time period for a reflection coefficient magnitude of 0.2 and phase of 0°, also shown is the outline of the voltage standing wave

In this case V_{max} is 1.2 and V_{min} is 0.8, and $|\Gamma|$ is 0.2, giving a VSWR of 1.5:1. Table 2.6 shows a number of other reflection coefficient magnitudes between zero and one, the VSWR that they generate and the maximum and minimum of the standing waves. The standing waves produced are shown in figure 2.26.

Table 2.6 - VSWR, reflection coefficient, return loss and V_{max} and V_{min} of the standing wave

VSWR	Reflection Coefficient Magnitude	Standing Wave	
		Vmax	Vmin
1:1	0	1	1
1.5:1	0.2	1.2	0.8
3:1	0.5	1.5	0.5
5:1	0.667	1.67	0.33
7:1	0.75	1.75	0.25
10:1	0.826	1.826	0.174
19:1	0.9	1.9	0.1
99:1	0.98	1.98	0.02
∞:1	1	2	0

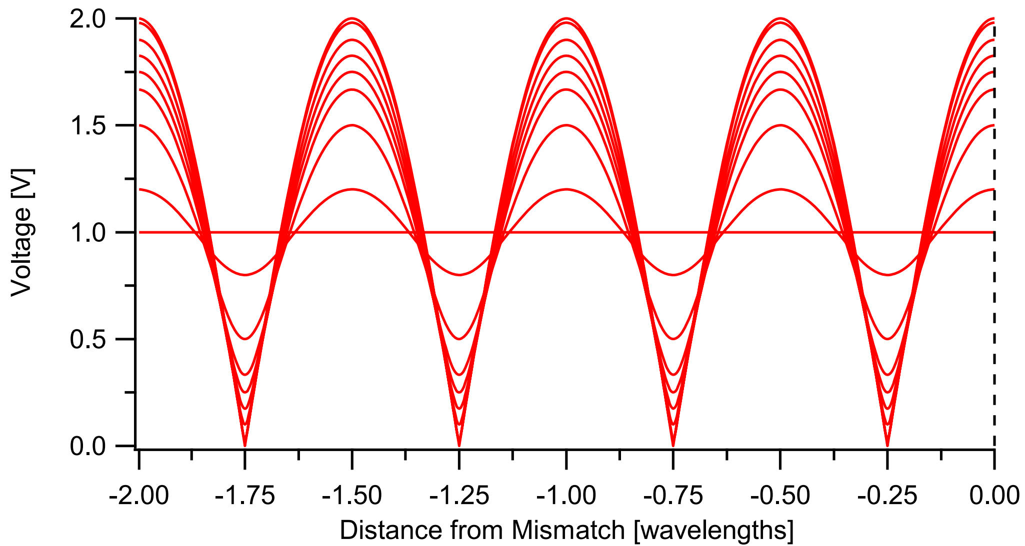


Figure 2.27 - Standing waves for the VSWR shown in table 2.6, in all cases the reflection coefficient phase is 0°

Although the phase of the reflection coefficient has no effect on the ratio of the standing wave produced, it does have an effect on the part of the standing wave that is located at the mismatch. Up till now the phase has been set to 0°, locating the maximum in the standing wave at the impedance mismatch. However if the phase is set to 180° then the minimum in the standing wave will be located at the impedance mismatch, this is shown in figure 2.27. These points are also shown on the Smith chart in figure 2.28, together with the circle of reflection coefficient magnitude of 0.2.

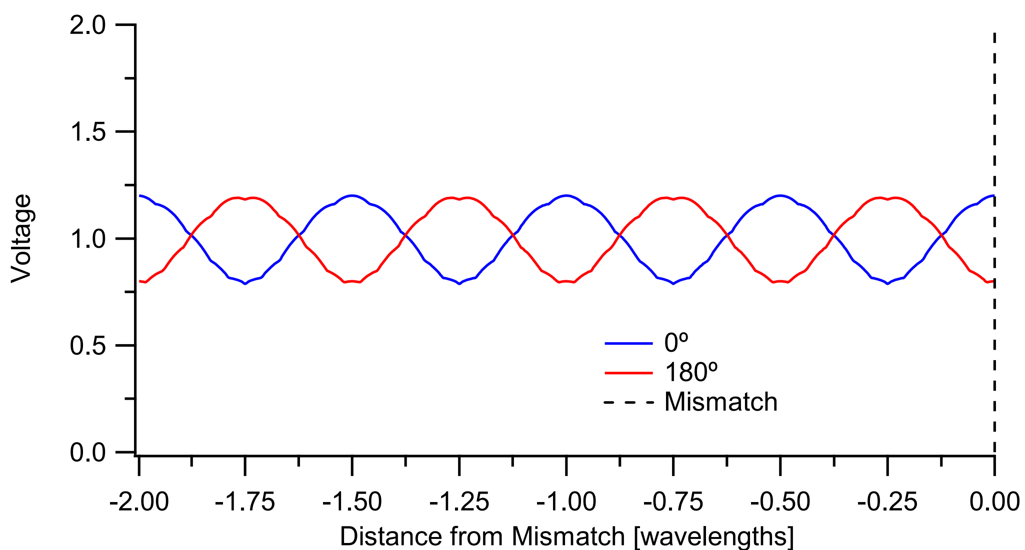


Figure 2.28 - Voltage standing waves produced by a reflection coefficient magnitude of 0.2 and phase of 0° and 180°

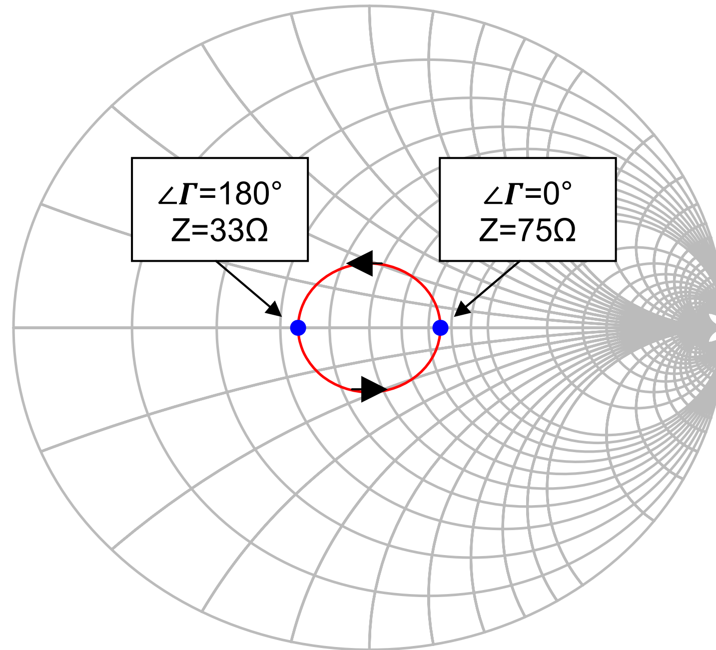


Figure 2.29 - Smith chart showing the circle of reflection coefficient magnitude of 0.2 and the points where the phase is 0° and 180°. The arrows show the direction of the VSWR sweep where the phase is swept from 0° to 360°

From this it can be seen that by setting the magnitude of the reflection coefficient and sweeping the phase from 0° through 360° the conditions that can be presented to a device by a specific level of impedance mismatch can be investigated. This is what is known as a VSWR sweep, as the ratio of the standing wave is constant throughout the sweep due to the constant magnitude of the reflection coefficient.

Obviously the matching network, or any other circuitry in between the load impedance and the device, will change the effect of the standing wave on the device. In general RF PA design it can be assumed that any well designed matching network will have minimal loss associated with it in order to minimise any loss in output power. This will also lead to minimal loss on any reflected power. In the next section (section 2.5.1) the worst case scenario will be investigated where the magnitude of the load reflection coefficient is one ($|\Gamma|=1$) and where all of the reflected power reaches the

device. The second section (section 2.5.2) will investigate less severe cases where not all of the reflected power reaches the device within the PA.

2.5.1 Infinite Voltage Standing Wave Ratio

In this section the scenario where all of the power produced by a PA is not only reflected back from the load impedance, but also reaches the device within the PA. In order for this to happen the magnitude of the reflection coefficient ($|\Gamma|$) must be equal to 1, meaning that the load impedance has no resistive (real) component. In addition, this reflection coefficient must be either presented directly to the device, or through a matching network (or any other circuitry) that has no loss associated with it. In order to simplify the rest of this section it will be assumed that the load impedance is connected directly to the output of the device, not through a matching network.

As described earlier in this section, it can be assumed that the B_2 wave coming from the device is independent of the load impedance, and that it has a normalized amplitude of one. With a reflection coefficient magnitude of one the reflected A_2 wave will also have a normalized magnitude of one. Again, as earlier, the superpositions of the voltage travelling waves at different instances in time can be plotted, as shown in figure 2.29, from which the standing wave can clearly be seen. The Voltage Standing Wave Ratio can be calculated from equation 2.21, which in this case is ∞:1.

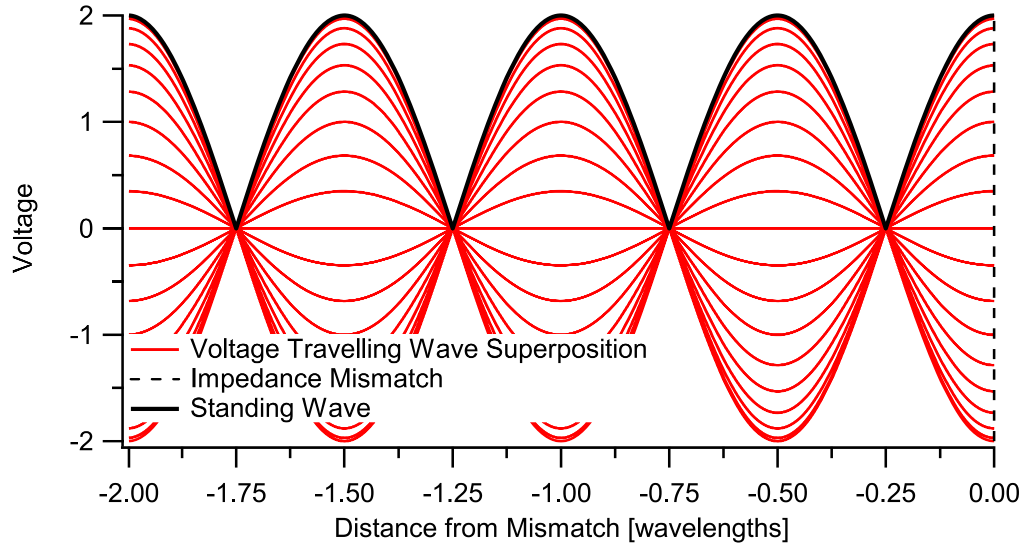


Figure 2.30 - The superpositions of the voltage travelling waves measured every tenth of a waveform time period for a reflection coefficient of magnitude 1 and phase 0, along with the resulting standing wave

It is important to note from this that the superposition of the voltage travelling waves has caused the peak of the standing wave to be double the initial amplitude of the B_2 wave entering the system. The peaks in the standing wave also occur at double the frequency of the travelling waves in the circuit.

In section 2.3.4 it was shown that the RF voltages and currents can be calculated from the voltage travelling waves using equations 2.15 and 2.16. From these it can be seen that the conditions needed to make the maxima and minima of the voltage standing waves correspond with those needed to generate the maximum RF voltage and maximum RF current swing. These conditions are described in table 2.7.

Table 2.7 - Relationship between the maximum and minimum of the standing wave and the phase difference between the travelling voltage waves and the RF voltage and RF current swings

	Standing Wave	
	Maximum	**Minimum**
Travelling Waves	In phase	180° Out of phase
RF Voltage Swing	Maximum	Minimum
RF Current Swing	Minimum	Maximum
Distance from Mismatch	0 ± λ/2	λ/4 ± λ/2

By comparing these conditions with the standing wave in figure 2.29 it can be seen that the standing wave causes variation in the RF voltages and currents leading up to the mismatch. With a reflection coefficient magnitude of one and phase of 0 the maximum RF voltage swing appears at the mismatch, however a quarter of a wavelength away from the mismatch would be the maximum RF current swing (for a 1GHz signal this would be 83mm).

In standard operation the RF IV waveform measurement system has only one calibration plane, or in other words only one point where the measurements are made. This will usually be either the ends of the coaxial cables or the tips of the probes that interface with the device and it is this point in the system that the impedance mismatch is located. It is therefore important to discuss how the standing wave varies with time at the location of the impedance mismatch. Figures 2.30 and 2.31 show how the amplitude of the standing wave varies with time at the impedance mismatch when the phase of reflection coefficient is 0° and 180° respectively. This confirms that, as expected, the voltage travelling waves are always in phase at the open circuit and 180° out of phase at the short circuit.

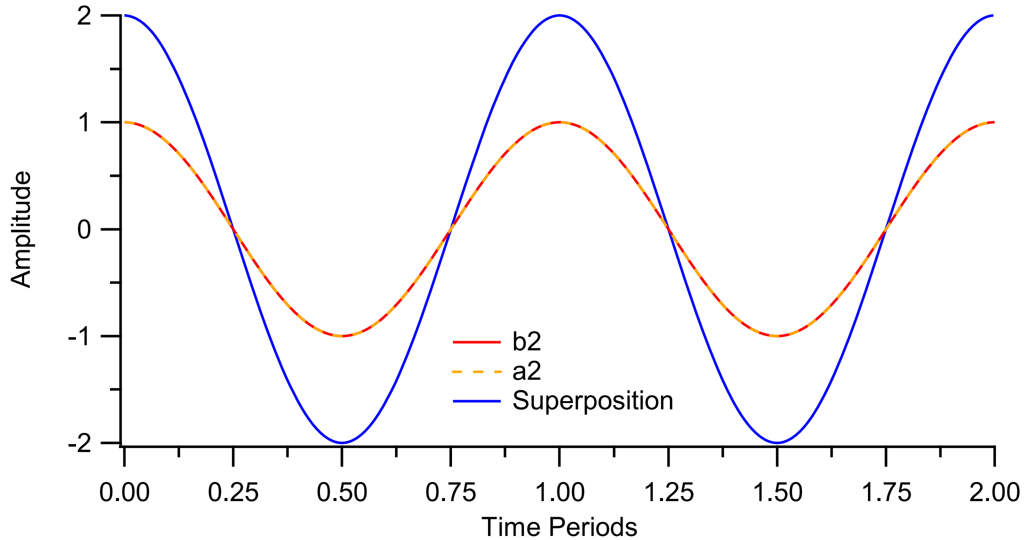


Figure 2.31 - Voltage travelling waves at the impedance mismatch as a function of time when the phase of the reflection coefficient is 0°

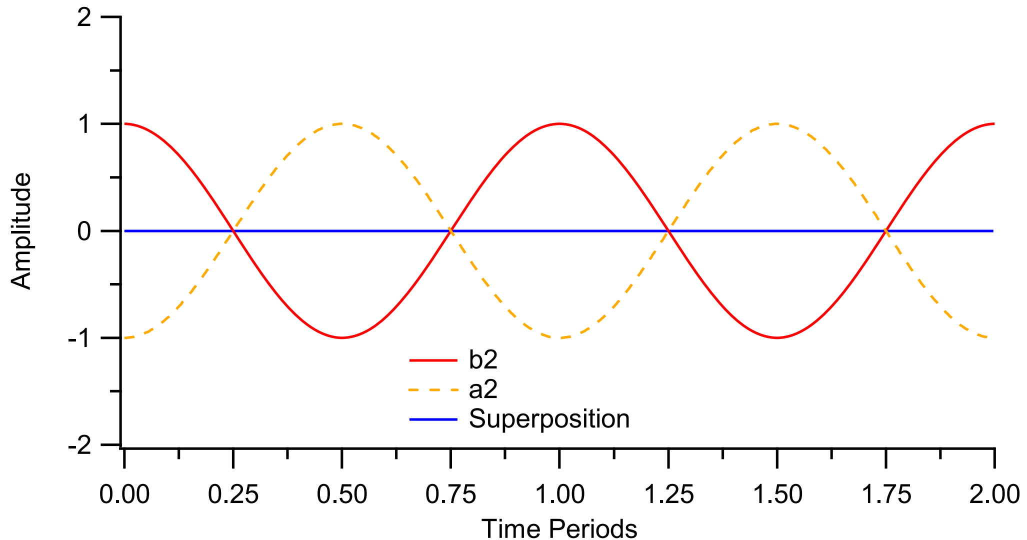


Figure 2.32 - Voltage travelling waves at the impedance mismatch as a function of time when the phase of the reflection coefficient is 180°

A VSWR sweep can be performed by setting the magnitude of the reflection coefficient and sweeping the phase from 0° through 360°. From this it can be seen that during an infinite VSWR sweep the device will be presented with both the open circuit and short circuit load points, generating both the maximum voltage swing and the maximum drain current. As both of these load impedances are purely real the phase of the load impedance will be 0° and hence the phase difference between the current and voltage will be 180°. However, in between these points the impedances will be purely

reactive and therefore have a phase of ±90°, resulting in the phase difference between the voltage and current waveforms also being ±90° away from the original 180°. This is confirmed in figures 2.32 and 2.33, which show the magnitude and phase of the load impedance and the magnitude of the voltage and currents and the change in phase difference between them during an infinite VSWR sweep (the phase difference will be 180° when the device is presented with an entirely real load impedance). As a result of the normalisation of the voltage travelling waves made earlier, the voltages and currents have a value of one when the output is matched.

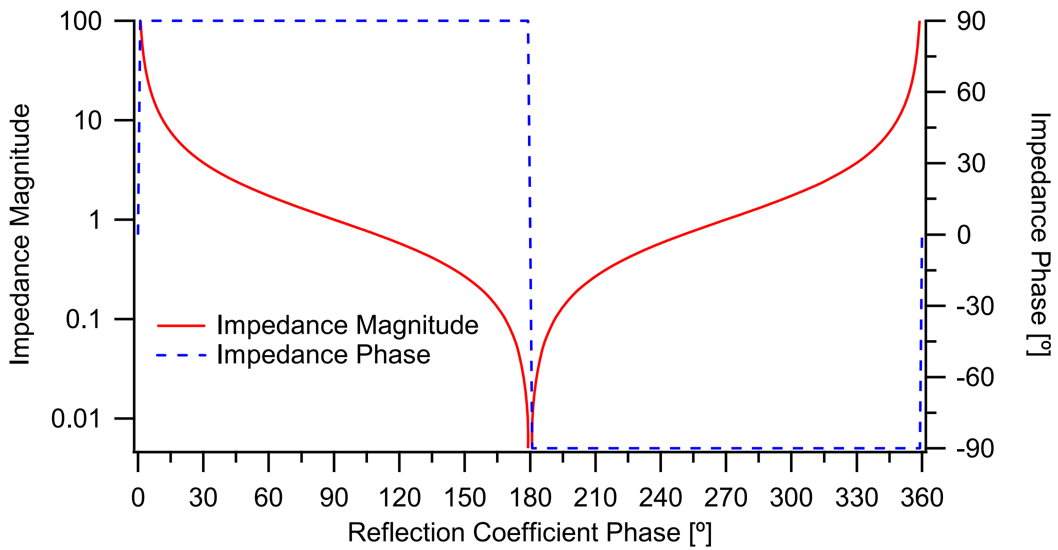


Figure 2.33 - Magnitude and Phase of the load impedances presented to a device during an infinite VSWR sweep

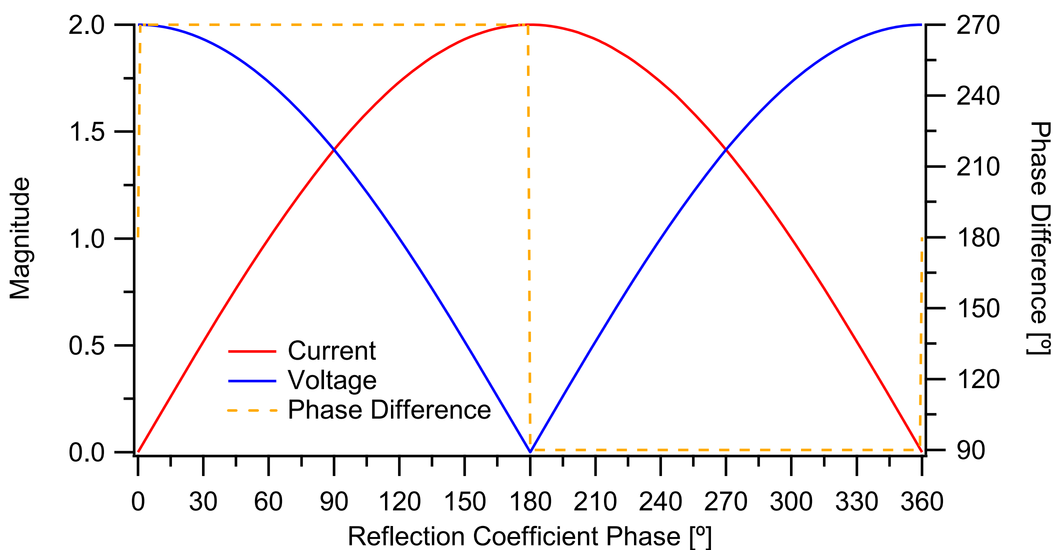


Figure 2.34 - Magnitude of the Voltage and Currents and the phase difference between them during an infinite VSWR sweep

This shows that there is potential for the voltages and currents to be twice that seen when the reflection coefficient magnitude is zero, which is confirmed by taking a closer look at the equations for calculating the RF voltages and currents (equations 2.15 and 2.16). It has already been discussed that when the reflection coefficient has a magnitude of one ($|\Gamma|=1$) the voltage travelling wave reflected from the load impedance will have the same magnitude as the one that is incident upon it.

However, so far this analysis has only concentrated on the ideal analysis of the load impedance, whereas in reality there is a transistor driving power into the load impedance. This transistor will have physical limits on the current and voltage that it can sustain; therefore limiting what can be supplied to the load impedance.

In addition to this, in order to produce an infinite VSWR the reflection coefficient magnitude must be 1. Figure 2.34 shows the effect of a small reduction in the magnitude of the reflection coefficient on the VSWR. From this it can be seen that as the reflection coefficient magnitude drops away from unity, the VSWR quickly falls away from infinity, which will result in a drop in the magnitude of the standing wave. This will also result in a drop away from the maximum RF voltage and current swings.

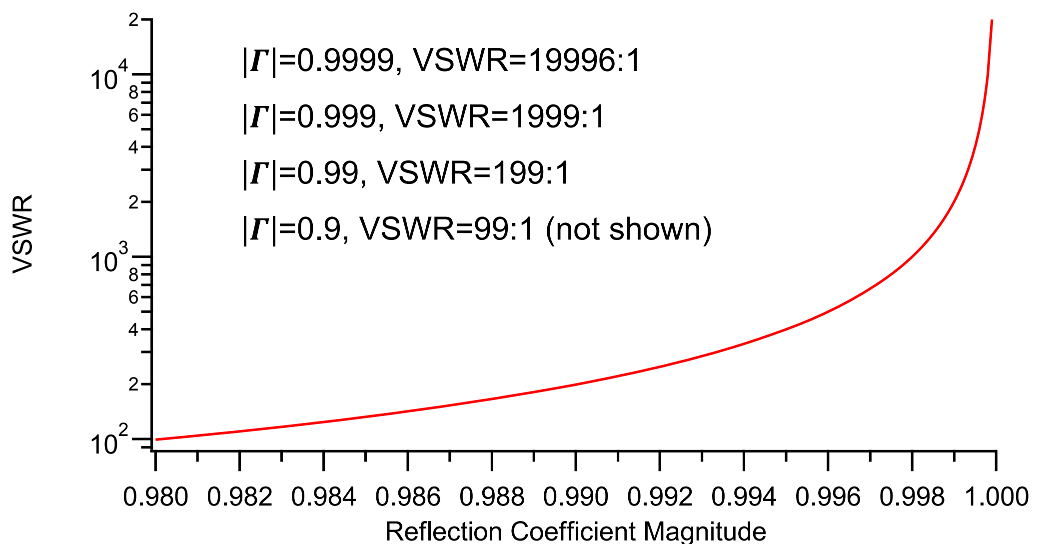


Figure 2.35 - Effect of reducing reflection coefficient magnitude on the VSWR

2.5.2 Other Voltage Standing Wave Ratios

Where the previous section dealt with the worst case scenario where all of the power produced by the device was reflected back at it, this section will deal with less severe scenarios. This is because worst case scenario testing is not always needed, or wanted, and it is often desirable to test under conditions closer to those that a device would experience in the real world.

As described at the beginning of this section, when there is an impedance mismatch in a system, such as the one shown in figure 2.23, the result is a standing wave. The ratio of this standing wave, known as the VSWR can be calculated from either the maximum and minimum values of the standing wave or from the reflection coefficient, as shown in equation 2.21. Reflection coefficient can also be described in terms of return loss, which is a measure of the amount of power not being reflected back from the load impedance [6], as shown in equation 2.22. Figure 2.35 shows how the reflection coefficient magnitude is related to both the VSWR and the return loss.

$$Return\ Loss = 20 * \log(|\Gamma|) \qquad (2.22)$$

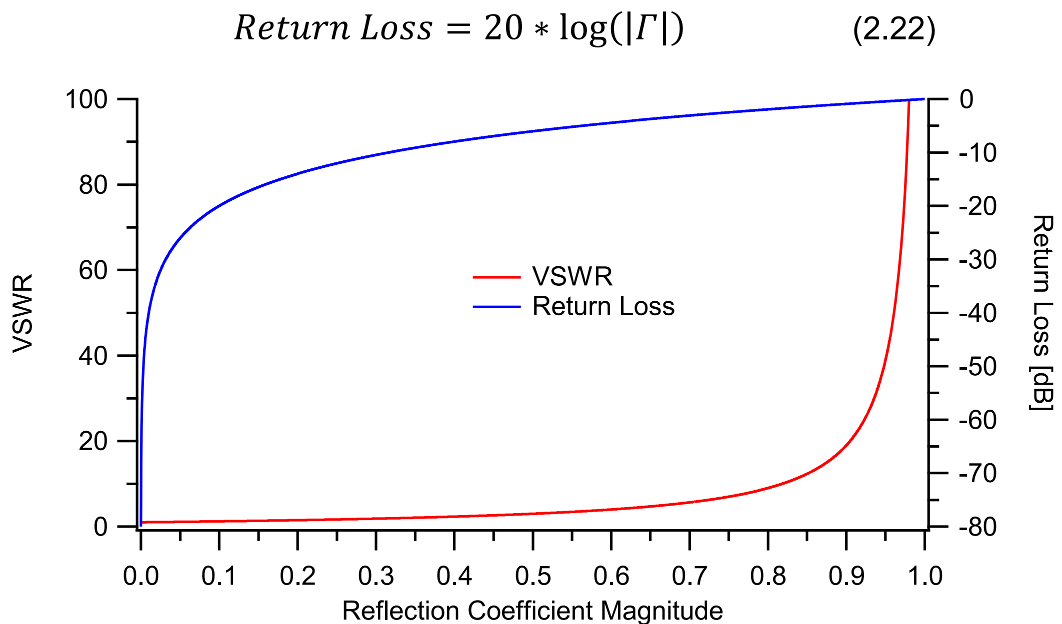


Figure 2.36 - Return Loss and VSWR as a function of Reflection Coefficient magnitude

Table 2.8 shows a selection of VSWR values, the reflection coefficient magnitudes needed to produce them and the return loss, the standing waves themselves are shown in figure 2.26, earlier in this section.

Table 2.8 - VSWR, reflection coefficient and return loss

VSWR	Reflection Coefficient Magnitude	Return Loss [dB]
1:1	0	∞
1.5:1	0.2	-14
3:1	0.5	-6
5:1	0.667	-3.5
7:1	0.75	-2.5
10:1	0.826	-1.7
19:1	0.9	-0.9
99:1	0.98	-0.18
∞:1	1	0

It is also possible to show that any loss present in the system between the output of the device and the load impedance will have an effect on the VSWR seen by the device. For example, if there is a 1dB loss present between the output of the device and a load with reflection coefficient magnitude of 1. The power coming from the device will have a 1dB loss before being reflected and then experiencing the same 1dB loss, giving an overall return loss of 2dB. This then converts to an effective reflection coefficient magnitude of 0.8 at the device, and in turn to a VSWR of 8.7:1. This is a big change from the usual infinite VSWR that would be expected with a reflection coefficient magnitude of 1 [21].

As with the infinite VSWR sweep, the reflection coefficient phase can be swept through 360° around the Smith chart. Figure 2.36 shows the impedance sweeps that would be produced by the VSWR shown in table 2.8, and figure 2.37 the maximum voltages and currents that would be produced. As with the analysis of the infinite VSWR sweep, this analysis is based around an ideal load impedance, with no consideration for the effect of the device that is driving power into the load.

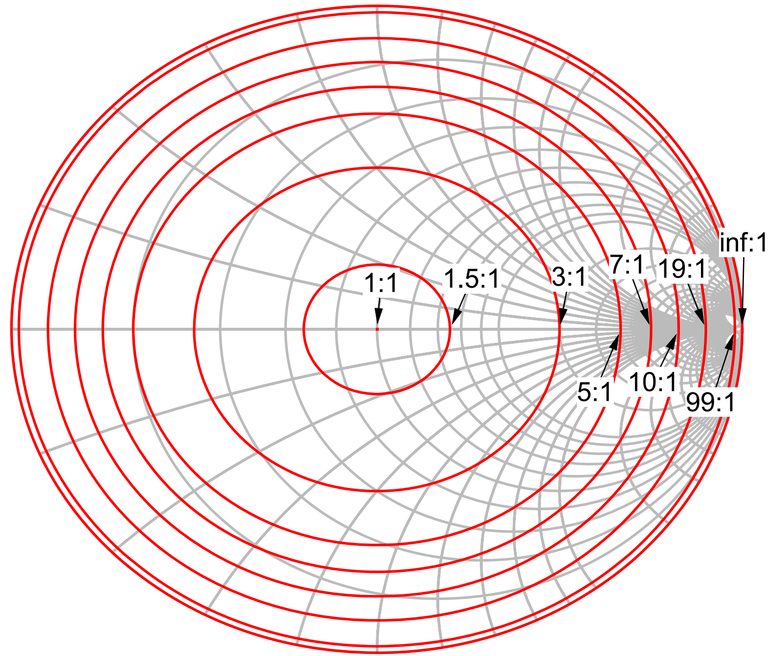


Figure 2.37 - Smith chart showing the load points for the VSWR sweeps shown in table 2.8

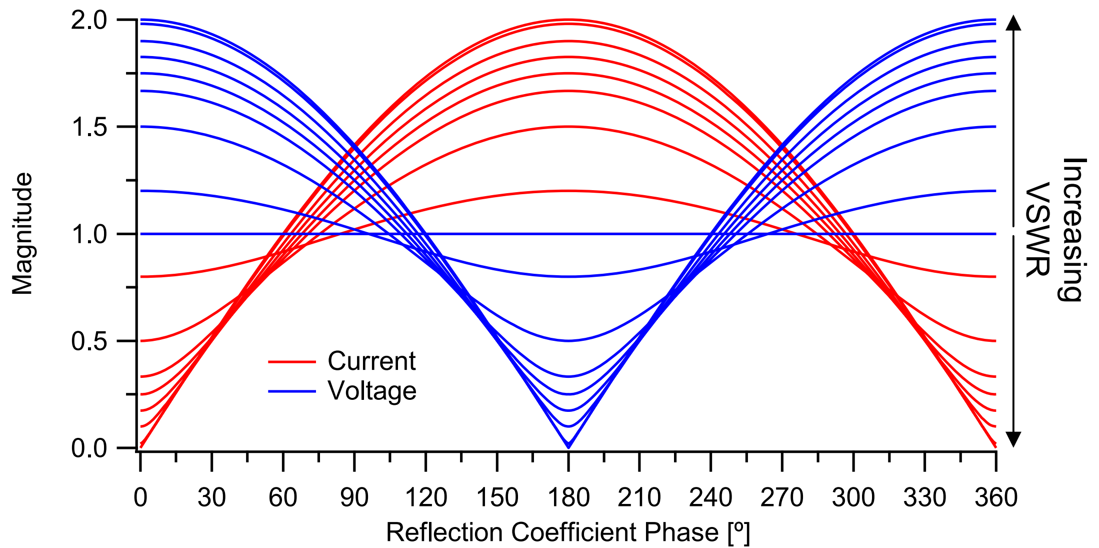


Figure 2.38 - Maximum voltage and current swing during the VSWR sweeps shown in table 2.8

2.6 Summary

The majority of this chapter has been given over to reviewing the operating modes of RF PA, the device used within them and the characterisation measurements needed to achieve first pass design success.

GaN HFETs are rapidly becoming the device technology of choice due to their excellent RF power density compared to other device technologies, as was described in section 2.2. This stems from both the wideband gap nature of the GaN, which allows for high breakdown voltages, and the ability to create heterostructures that give a high electron density in the channel of the device. This increased power density allows for smaller device sizes which, along with the obvious benefits, allows for simpler matching networks to be used. In section 2.4 the different operating modes of RF PA were described, including the new families of continuous mode which allow for high efficiency operation over an extended bandwidth. These modes involve increasing the harmonic content, and therefore the peak, of the drain voltage waveform, something that is only practically realisable in device technologies such as GaN with high breakdown voltages.

A first pass design methodology is highly desirable when designing RF PA so that costly post process optimisation and tuning is not needed. Section 2.3 presented both the more traditional device characterisation measurements that are used for PA design and also those needed to make first pass design possible. These ‘first-pass’ characterisation measurements revolve around the use of the RF IV waveform measurement and engineering system, which allows the exact state of the device to be measured under the operating conditions it will experience in the PA.

The remainder of this chapter (section 2.5) focused on providing an introduction to the implications of a mismatched load impedance. This analysis was entirely theoretical and built upon the S-parameter analysis of one port networks begun earlier in the chapter. This analysis showed that the voltage travelling wave reflected from the load impedance (A_2) will interfere with the wave coming from the device (B_2), creating a voltage standing wave. The exact conditions presented to the device by an impedance mismatch depend on the distance of the mismatch from the

device and on the phase of the reflection coefficient presented to the device by the mismatch. However all of the possible conditions that could be presented to a device by a specific level of impedance mismatch are presented during a VSWR sweep. The worst case scenario is when the mismatched load impedance is purely reactive, resulting in a reflection coefficient magnitude of one and all of the power being reflected back towards the PA. This results in a standing wave with a peak that is twice the magnitude of the travelling wave incident upon the mismatch and therefore, theoretically, voltages and currents that are twice what are seen when the device is matched. However in practice the drain currents and voltages of a transistor will be constrained by its IV operating area.

2.7 References

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Chapter 3 – VSWR Sweeps

3.1 Introduction

One of the possible uses for an isolator component in a power amplifier (PA) is as an output protection component [1]. In this application the isolator is placed in the system between the amplifier and any component that could cause power to be reflected back into the output of the PA. Without the isolator present the reflected power could have multiple effects, firstly it could interfere with the PA performance, causing a loss in output power and efficiency. Secondly this reflected power could cause damage to the PA itself, which is the main subject area for this chapter. There are a variety of reasons that could cause power to be reflected back towards the PA, everything from a faulty connection to having no connection at all. It therefore seems as though the isolator is an essential component; however it is a large, heavy component and can cause losses in the output power from the PA [1]. Therefore there are situations, e.g. in space applications, where these factors matter enough to consider removing the isolator. Although the background for this chapter is the removal of the isolator the results contained are applicable to any situation that could result in an impedance mismatch.

In this chapter we will build on the theoretical investigation of the effect of this reflected power that was begun in the previous chapter by moving on to investigate the effect on a device within an RF PA. This will begin with the worst case scenario where all of the power produced by the device is reflected back at it and then move on to consider different bias points, input power levels and device sizes. The analysis will then move on to consider less severe scenarios, where the reflection coefficient magnitude is less than one. Finally it will be shown how the harmonic load impedances can be used to influence the operation of a device in these conditions.

3.2 Removing the Isolator

Figure 3.1 shows a typical setup of a PA with a protection isolator between it and the antenna [1]. If the impedance match between the antenna and the output of the PA circuit is not exact, then it will lead to some fraction of the output power produced by the PA being reflected back from the antenna. This would usually be absorbed by the 50Ω load of the isolator, effectively isolating the PA from the impedance environment beyond the isolator. However if the isolator has been removed then the power will be reflected straight back into the output of the PA.

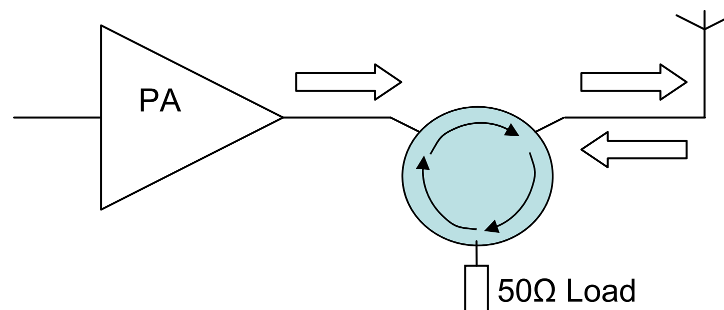


Figure 3.1 - Power amplifier with an output protection isolator connected to an aerial. The arrows show the direction of power flow.

The effect of power being reflected back to the PA was discussed at the end of the previous chapter. The results of that discussion can be utilised here if the antenna is replaced with an arbitrary load impedance, the result is a circuit that resembles the one shown in figure 2.24. In the previous chapter it was shown that an impedance mismatch can cause variations in the RF drain current and voltage compared to those seen when the impedance is matched. More specifically when the reflection coefficient phase is 0° the maximum RF drain voltage swing is produced and when the phase 180° the maximum RF current swing is produced. A Voltage Standing Wave Ratio (VSWR) sweep can be performed by setting the magnitude of the reflection coefficient, and therefore the VSWR, and sweeping the phase between 0° and 360°. This will show all of the possible states that a device could be subjected to at a specific level of impedance mismatch. It was also shown that the worst possible case scenario is when all of the power is reflected away from the load impedance back towards the device.

3.3 DC and Pulsed Safe Operating Areas

In order to find the maximum safe bias points for the device to operate under DC and pulsed conditions Safe Operating Areas (SOA) were constructed using destructive testing on 2x50µm GaN HFETs [2], which were described in section 2.2.1. First the DC SOA was constructed by setting a gate voltage and then sweeping the drain voltage upwards, stopping at regular intervals to characterise the device. This was continued until the device was destroyed, and then repeated for different gate bias voltages. The results are shown in figure 3.2. The DC failure points can be fitted with a curve of constant power, in this case approximately 1.7W (17 W/mm). Using equation 2.14, and an ambient temperature of 25°C, this corresponds to a static junction temperature of 133°C.

Next this procedure was repeated but using pulsed IV measurements, the results of which are also shown in figure 3.2. The system was limited to a maximum of 60V, so to begin with the pulse duration and bias point were set to benign levels and then increased in order to cause device failures. However as these points only cover a very limited area of the IV plane no definitive conclusions can be drawn about the cause of failure.

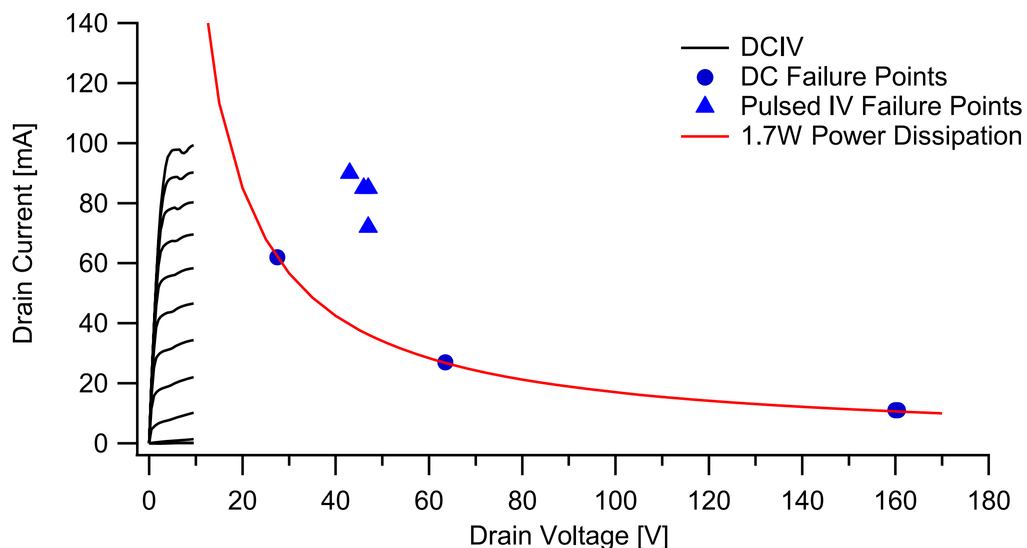


Figure 3.2 - DC and Pulsed destructive testing failure points for a 2x50µm GaN HFET, together with the 1.7W power dissipation (160°C static junction temperature) contour that fits the DC failure points

3.4 Infinite VSWR Sweep

As already discussed the worst possible case scenario for a device is if all of the power that it generates is reflected back at it. This condition results from the device having no real load impedance in which to dissipate the power that is generated. In order to investigate how these conditions affects a device the RF IV waveform measurement system [3] was used together with the Envelope Load Pull (ELP) system [4]. All of the measurements in this chapter were performed with a fundamental frequency of 0.9GHz.

3.4.1 Infinite VSWR Sweep

In order to investigate the effect of an infinite VSWR sweep on device performance a drain bias point of 20V and a gate voltage of -3.5V, giving an initial drain current of 30mA (class AB), were chosen. The input drive power to the device was set to be that required to saturate the output power at the optimum load impedance. The reflection coefficient magnitude was set to 1, to give a VSWR of ∞:1 and the phase stepped between 0° and 360° in 10° steps, both the second and third harmonic impedances were set to short circuits in order to keep the harmonic voltages to a minimum. The resulting RF load lines for a 2x50µm GaN HFET are shown in figure 3.3 and the RF IV waveforms are shown in figure 3.4 [5]. All of the RF waveforms have been de-embedded for a drain-source capacitance (C_{ds}) of 0.08pF (0.8pF/mm).

There are three features that can be seen in the RF load lines in figure 3.3, firstly the “tail” that extends to high RF drain voltages, secondly the simultaneously high RF drain currents and voltages, and finally the negative RF drain currents. All of these will be investigated in more detail in the next part (3.4.2) of this section.

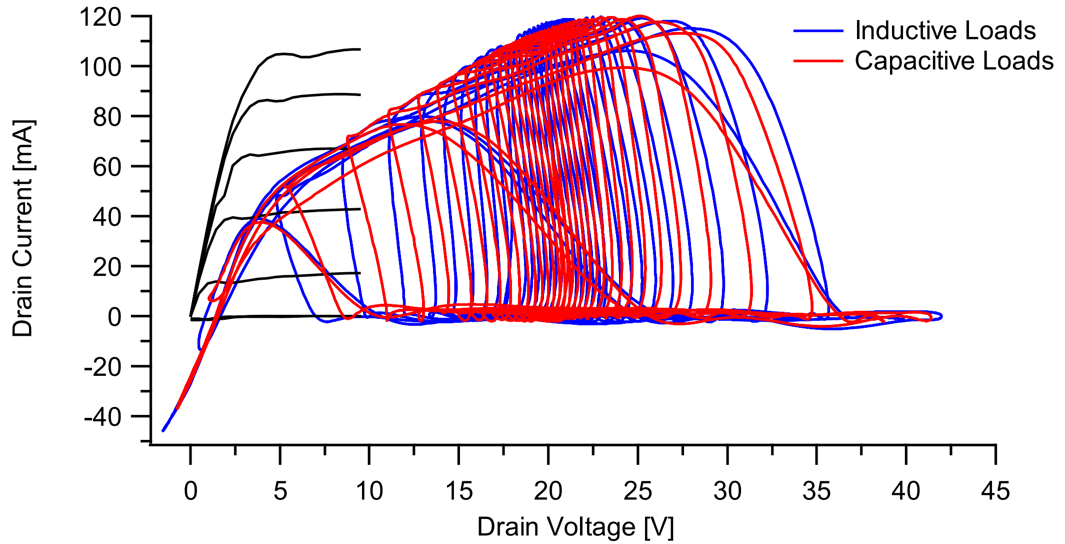


Figure 3.3 - RF Load lines of an infinite VSWR sweep, with the load phase swept between 0° and 360° in 10° steps, on a 2x50µm GaN HFET

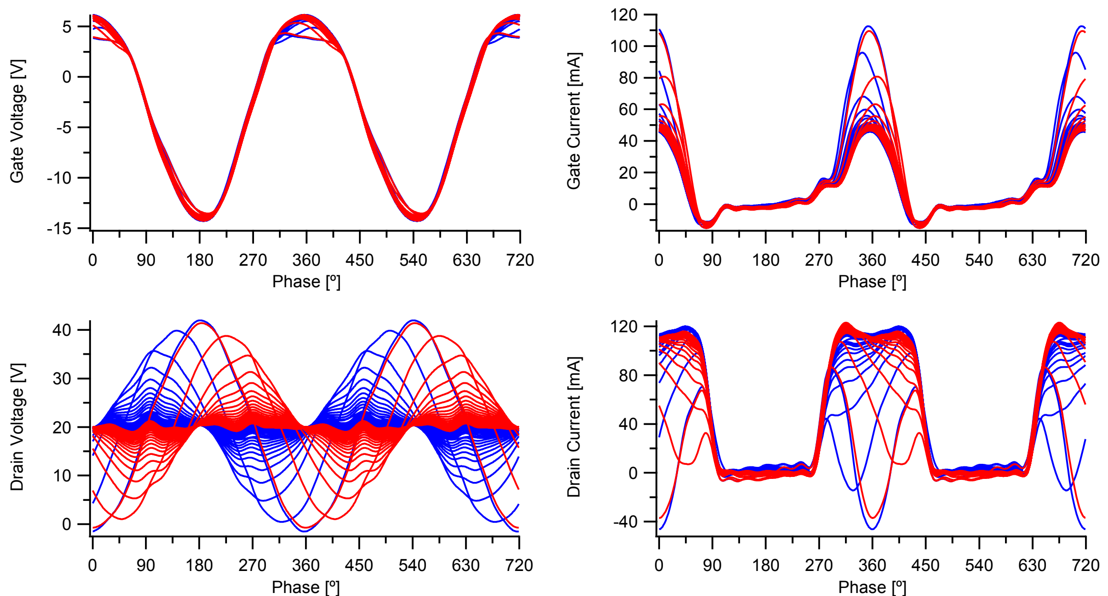


Figure 3.4 - RF voltage and current waveforms of an infinite VSWR sweep, shown in figure 3.3, with the load phase swept between 0° and 360° in 10° steps, on a 2x50µm GaN HFET

From the RF waveforms in figure 3.4 it can be seen that, as is expected, the overall shape of the RF load lines produced for the capacitive and inductive loads are symmetrical. There are small differences in the RF load lines shown here, which are caused by small variations in the impedances points measured on either side of the Smith chart.

From looking at the waveforms it can be seen that the RF drain currents are all in phase with each other, and with the RF gate voltage waveforms, which confirms that the device is behaving as a voltage controlled current

source. In contrast the phase of the RF drain voltage waveforms moves from 180° out of phase with the drain current waveforms to 90° out of phase and back to 180°, as the phase of the reflection coefficient progresses through the VSWR sweep due to the influence of the reactive load impedance. The waveforms also drop in amplitude as the impedance drops. This is shown in figure 3.5, which shows a plot of the magnitude and phase of the load impedance during the infinite VSWR sweep. This shows a good agreement to the equivalent ideal plot shown in figure 2.32.

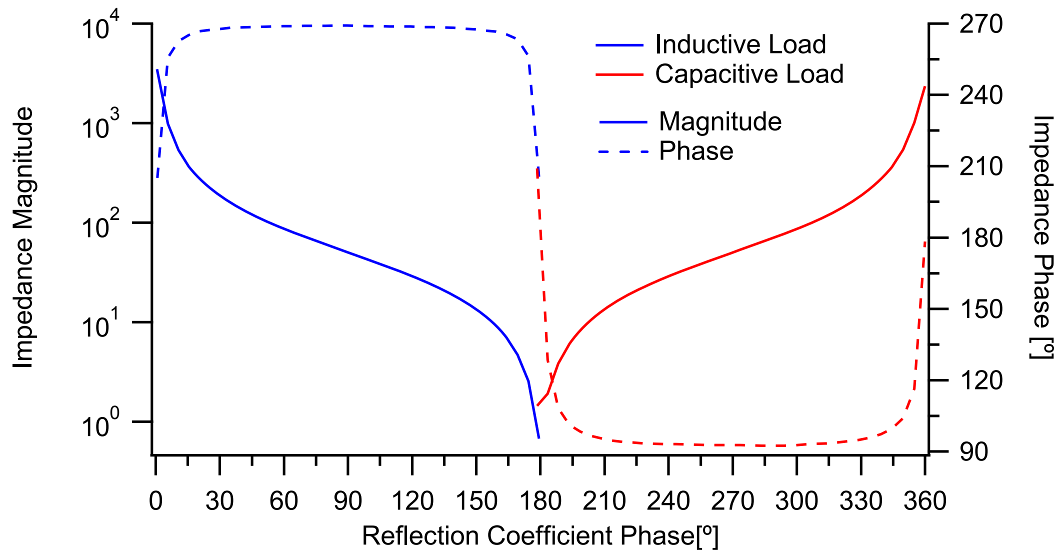


Figure 3.5 - Magnitude and phase of the load impedance during the infinite VSWR sweep shown in figure 3.3

It is also possible to compare the actual measured RF drain voltages and currents with those suggested by the ideal analysis in the previous chapter. Figure 3.6 shows the maximum RF drain current and voltages and figure 3.7 shows the phase difference between these waveforms for the infinite VSWR, which can be compared to those shown in figure 2.33 for the ideal analysis.

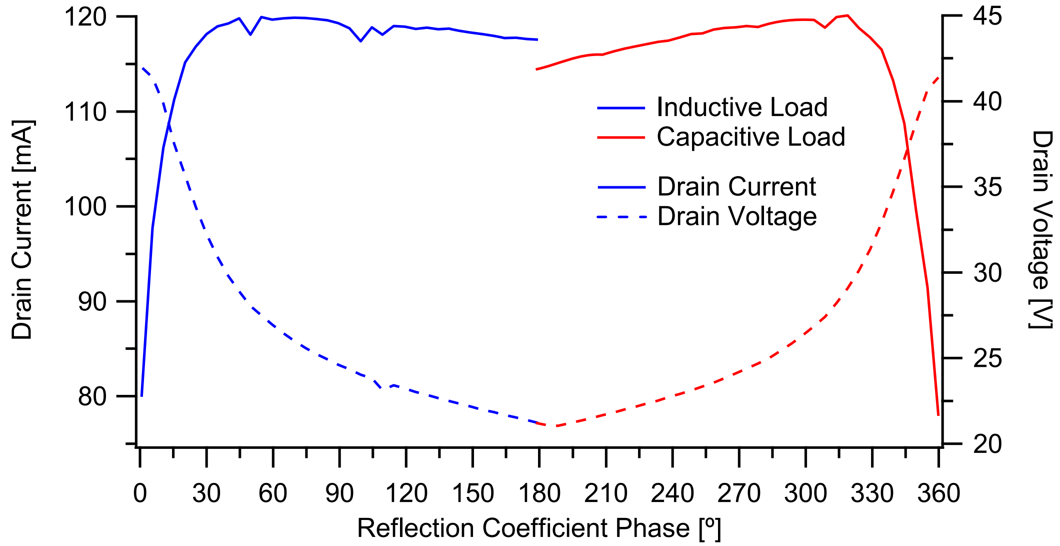


Figure 3.6 - Maximum RF drain current and voltage for the infinite VSWR sweep shown in figure 3.3

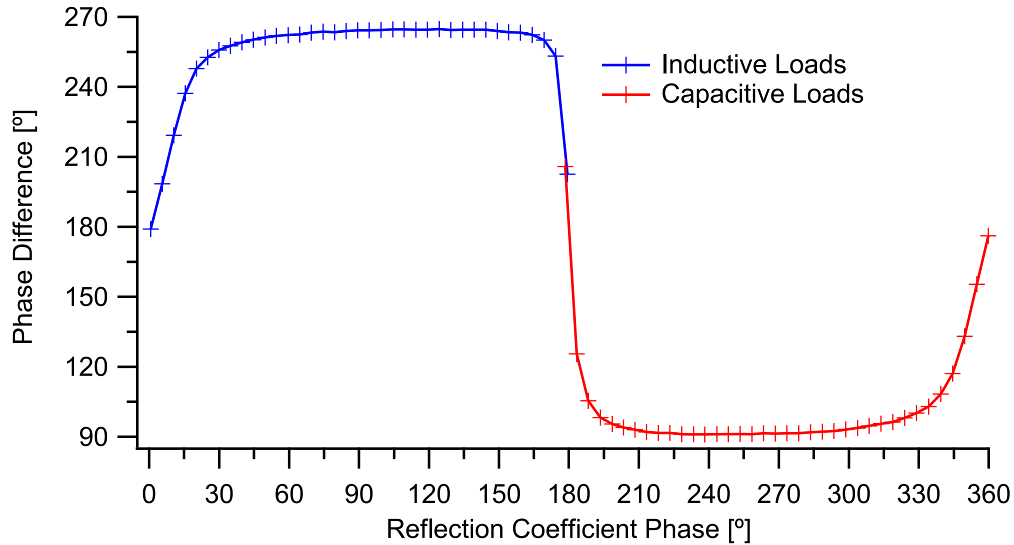


Figure 3.7 - Phase difference between the drain voltage and drain current waveforms from the infinite VSWR sweep shown in figure 3.3

It can be seen from figure 3.4 that when the RF drain voltage swing is small the RF drain current is a square waveform, as the device is being driven into saturation. However when the RF voltage swing increases it forces the RF drain current to interact with the device knee region, causing the dips seen in the peak of the waveform. These dips are seen on different sides of the RF drain current waveform for the capacitive load impedances compared to the inductive load impedances. This is due to the direction of the rotation of the RF load lines as a function of time, shown in figure 3.8.

This is a clockwise rotation for the inductive load lines and an anticlockwise rotation for the capacitive load lines. A clockwise rotation will cause the load lines to be increasing in drain current as they interact with the knee region. Whereas an anticlockwise rotation will cause the load lines to be dropping in drain current as they interact with the knee region.

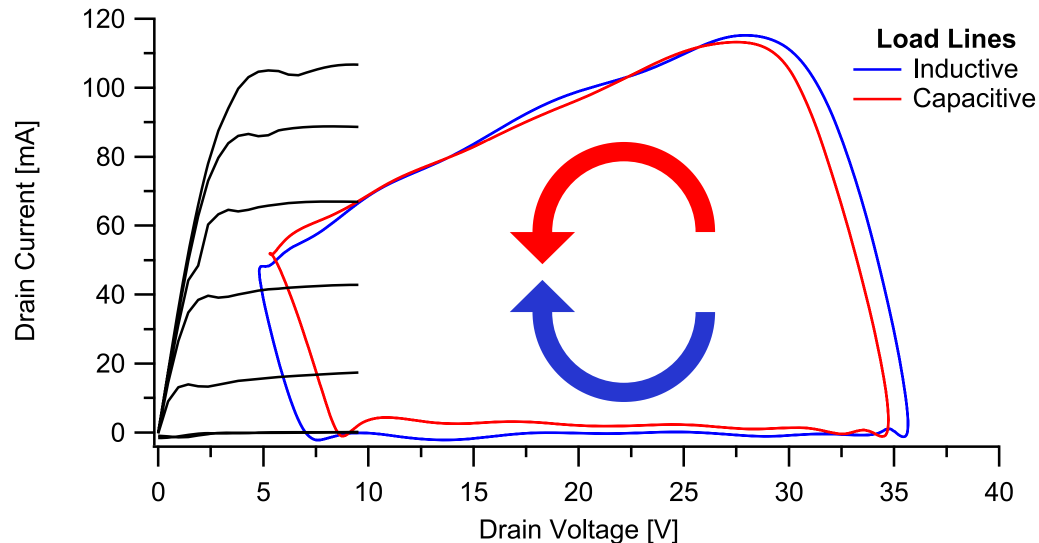


Figure 3.8 - The “roundest” RF load lines from the capacitive and inductive portions of the infinite VSWR sweep shown in figure 3.3. The direction of the rotation of each of the load lines as a function of time is marked, clockwise for the inductive loads and anticlockwise for the capacitive loads.

In the theoretical analysis of infinite VSWR in the previous chapter it was assumed that the voltage travelling wave leaving the device (B_2) was independent of the load impedance presented to the device. However this is not the case. Figure 3.9 shows the magnitudes and phases of both of the voltage travelling waves on the output of the device during the infinite VSWR sweep, from which it is clear that both the magnitude and phase of the B_2 wave are dependent on the load impedance. It can also be seen that, as expected, the phase difference between the travelling waves changes from 0° to 180° during the sweep and that the reflected A_2 wave is of similar magnitude to the B_2 wave.

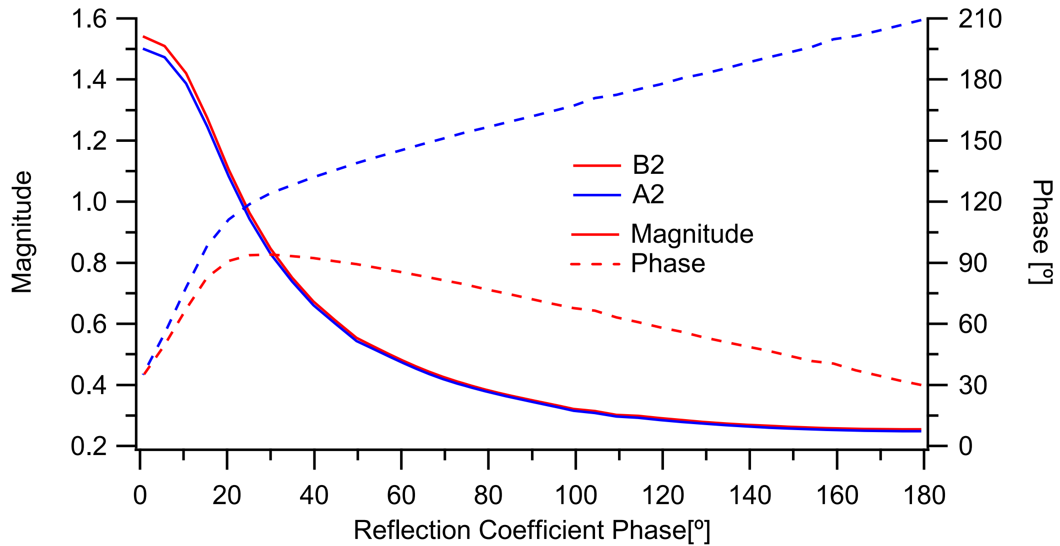


Figure 3.9 - Magnitude and Phase of the B_2 and A_2 voltage travelling waves for the inductive loads of the infinite VSWR sweep shown in figure 3.3

3.4.2 Comparison between Infinite VSWR sweep and the SOA

In order to investigate how the infinite VSWR sweep compares to the DC and pulsed SOA the previous sweep was re-measured at a drain voltage of 30V, this increases the interaction with the SOAs. These RF load lines are shown in figure 3.10 together with the DC and pulsed SOA. It can be seen that the majority of the load lines extend beyond the DC SOA and a few even reach out to and past the pulsed failure points. Additionally, figure 3.11 shows how the maximum RF drain current and voltage and the DC drain current vary throughout the sweep as a function of the magnitude of the load impedance.

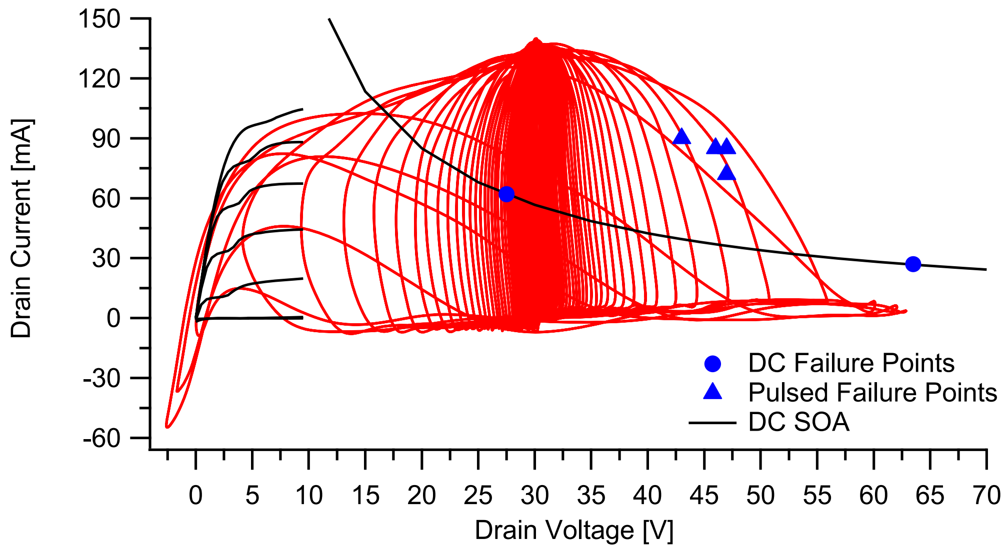


Figure 3.10 - RF load lines for an infinite VSWR sweep performed over the inductive half of the Smith chart in 5° steps together with the DC SOA and DC and pulsed failure points, performed on a 2x50µm GaN HFET

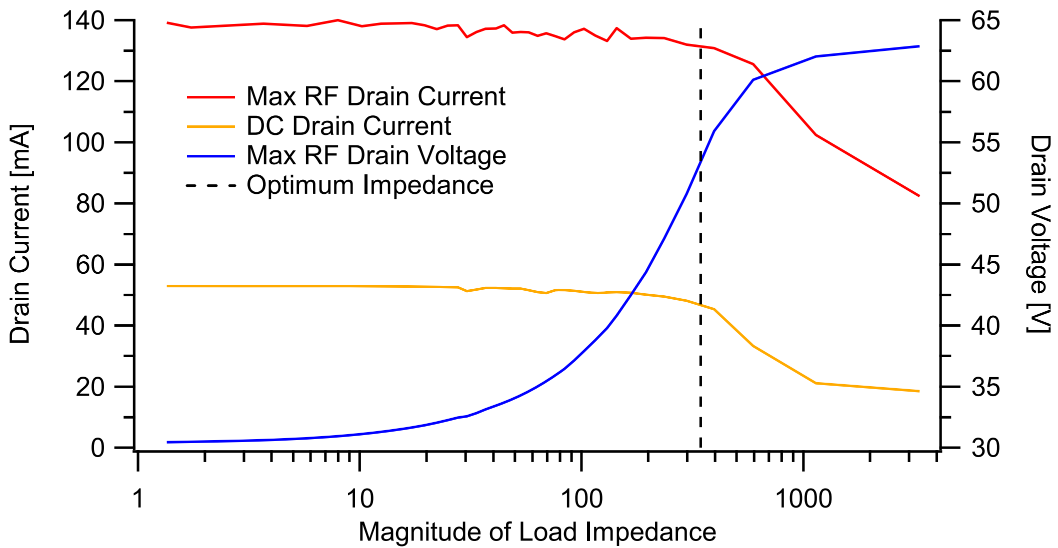


Figure 3.11 - Maximum RF and DC drain current and maximum RF drain voltage for the infinite VSWR sweep shown in figure 3.10 along with a marker for the optimum impedance of the device (in this case 350Ω)

From this it can clearly seen that the observed behaviour during an infinite VSWR sweep can be divided into three regions, one of high RF drain voltage swings, another of high peak RF drain currents and finally a transition region between the two. This can be explained by considering the optimum impedance of the device, which is also shown in figure 3.11.

The effect of load impedance on the trajectory of the RF load line in standard operation was discussed in the previous chapter (section 2.3.6). This is the same when considering the infinite VSWR sweep. When the magnitude of the impedance presented to the device is much lower than the magnitude of the optimum impedance of the device there are high peak RF drain currents. Whereas when the magnitude of the impedance presented to the device is much higher than the magnitude of the optimum impedance of the device there are high RF drain voltage swings.

In between these regions there are simultaneously high RF drain current and drain voltage swings. These occur when the device is presented with a load impedance that has no real component and a reactive component equal to the optimum real impedance of the device. It can be seen from the load lines in figure 3.12 that the RF drain voltage and current waveforms have similar magnitudes in both these circumstances. The only difference between the two load impedances is the phase difference between the RF drain voltage and current waveforms, which is the cause of the looping seen in the load lines of the infinite VSWR sweep. Figure 3.12 also shows the RF load lines of the open circuit and the short circuit load impedances, for comparison.

An observation can be made at this point that the magnitude of the impedance has an obvious effect on the state of the device during the VSWR sweep. In order to investigate this further a quantity of normalised load impedance can be defined as in equation 3.1, where Z_{load} is the load impedance measured during the VSWR sweep and Z_{opt} is the optimum impedance of the device.

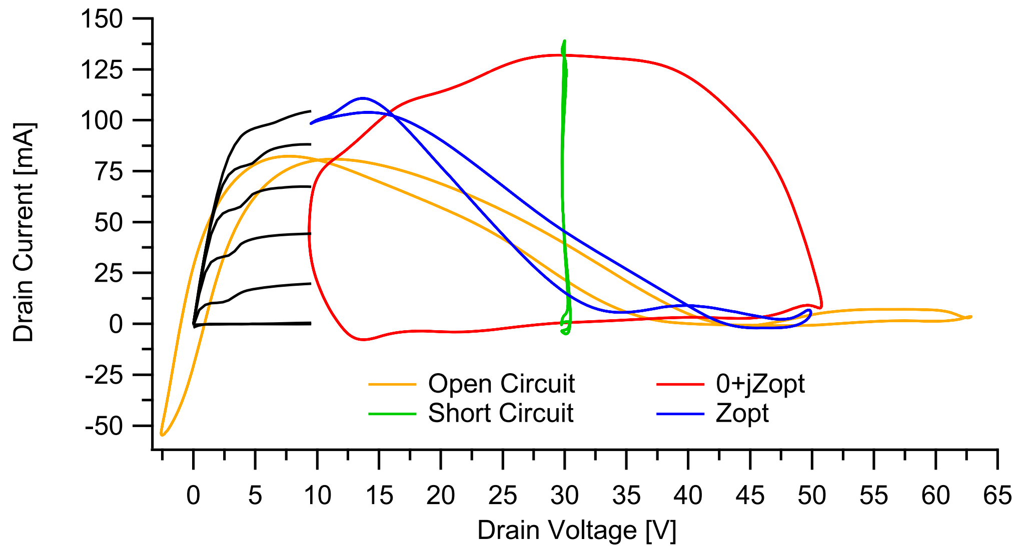


Figure 3.12 - RF load lines produced at the optimum impedance and at the open circuit, short circuit and boundary between the regions of an infinite VSWR sweep

$$Z_{norm} = \frac{|Z_{load}|}{|Z_{opt}|} \tag{3.1}$$

This normalisation procedure will allow us to compare different device sizes and bias points directly with each other. As all of the RF waveforms have been de-embedded the optimum impedance should contain minimal reactive components. Figure 3.11 can now be re-plotted with the normalised impedance in figure 3.13. In addition, figure 3.14 shows the DC and instantaneous RF power dissipated in the device, along with the failure power from the DC SOA testing earlier. From this it can be seen that although the quiescent drain current rises in the high drain current region of the infinite VSWR sweep, it does not exceed the failure power of the DC SOA.

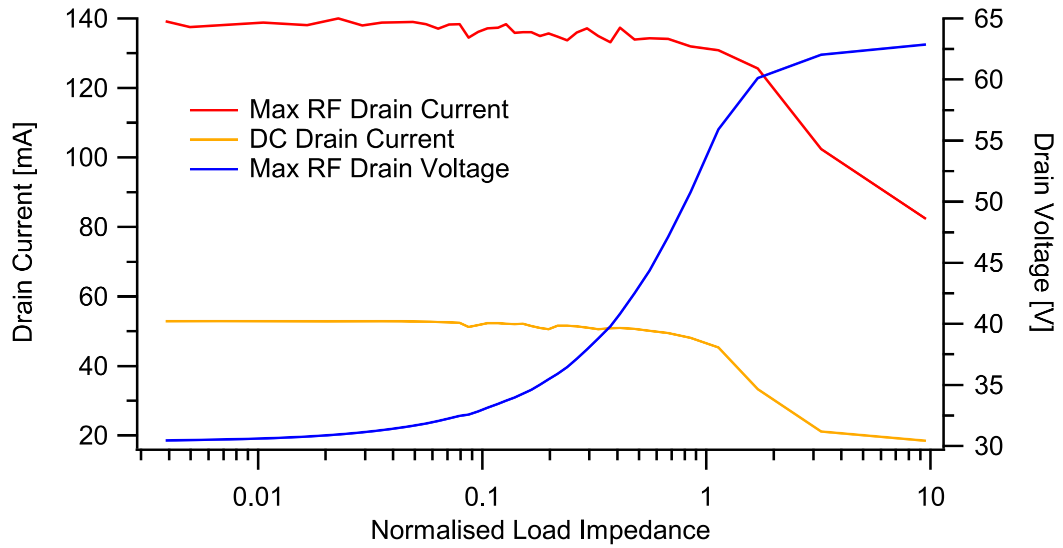


Figure 3.13 - Maximum RF drain Voltage and Current and DC drain current plotted against the normalised load impedance for a 2x50µm GaN HFET subjected to an infinite VSWR sweep at a drain bias of 30V.

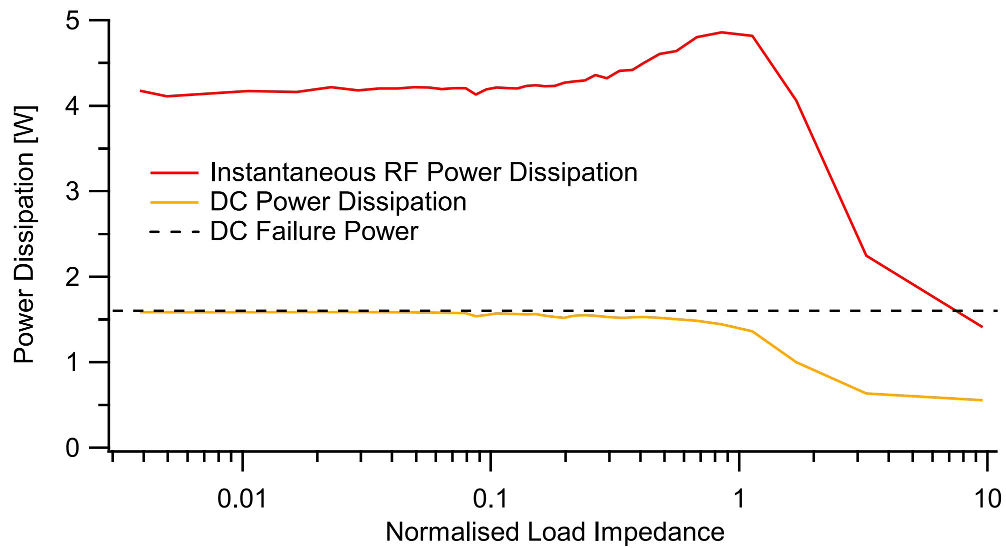


Figure 3.14 - DC and instantaneous RF power dissipation plotted against the normalised load impedance for a 2x50µm GaN HFET subjected to an infinite VSWR sweep at a drain bias of 30V

From figures 3.13 and 3.14 the three regions of VSWR sweep can be defined as follows:

1) The region of high RF drain voltage swing and low RF and DC drain current above the normalised impedance of 1
2) The region of high RF and DC drain current and low RF drain voltage swing below the normalised impedance of 1
3) Around the normalised optimum impedance there is a transition region where there are simultaneously high RF drain voltages and currents giving the large, "round" RF load lines discussed earlier

As already mentioned above, the RF drain current and voltage swings in the transition region will be comparable to those seen at the optimum impedance of the device. It therefore follows that in the high drain voltage region the drain voltage swings will be higher, and the peak drain currents lower, than those seen at the optimum impedance. Although this same line of reasoning should follow in the high drain current region, the drain current swings are limited here by the saturation of the device. Therefore there is little increase in peak drain current, however the RF drain voltage swing will still decrease from that seen at the optimum impedance.

3.4.3 Potential Failure Mechanisms

Investigating the RF waveforms from the infinite VSWR sweep shown in figure 3.10 reveals that the device is subjected to four potential failure mechanisms. These can be described in terms of the regions of the VSWR sweep found in section 3.4.1. The RF load lines corresponding to each of these can be seen in figure 3.12 [6].

1) At normalised impedances greater than unity there are large RF drain voltage swings, shown in figure 3.15.
    a. High peak RF voltages in excess of double the drain bias voltage
    b. At these high normalised load impedances the RF gate and drain voltage waveforms are 180° out of phase, and due to the high RF drain voltage swing the minimum RF drain voltage falls below the maximum RF gate voltage leading to the gate-drain diode becoming forward biased. This is turn causes an increase in both the RF and DC gate currents, the effects of which will be discussed in chapter 4.

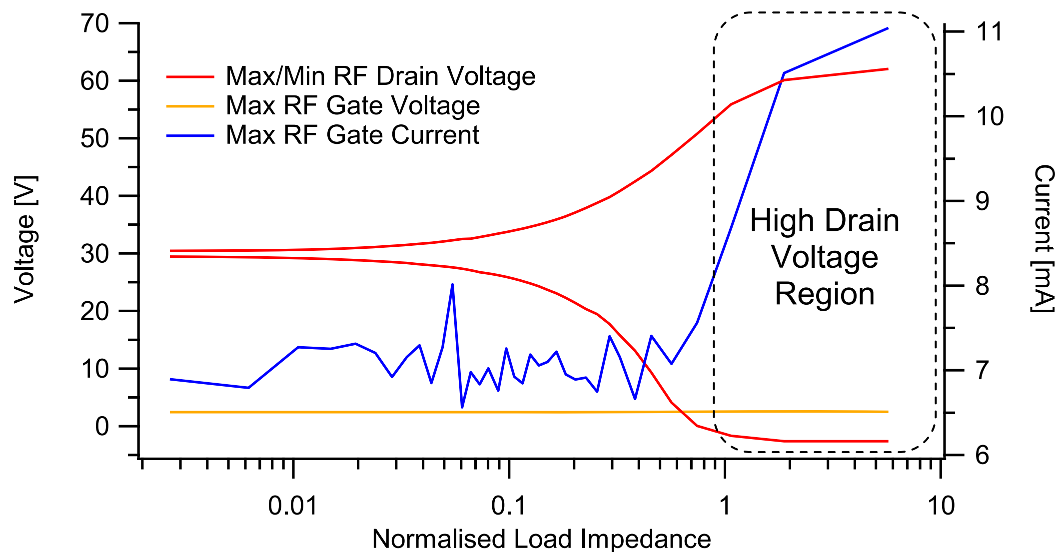


Figure 3.15 - Maximum and minimum RF drain voltage, maximum RF gate voltage and maximum RF gate current for a 2x50µm GaN HFET subjected to an infinite VSWR sweep

2) At normalised impedances less than unity there are high RF current swings, shown in figure 3.16.
    a. Device saturation, the “squaring up” of the RF current waveform, causes the DC bias component to rise up to almost the level seen in class A operation.
    b. This also leads to a rise in the DC power dissipation within the device and to an associated rise in the static junction temperature.

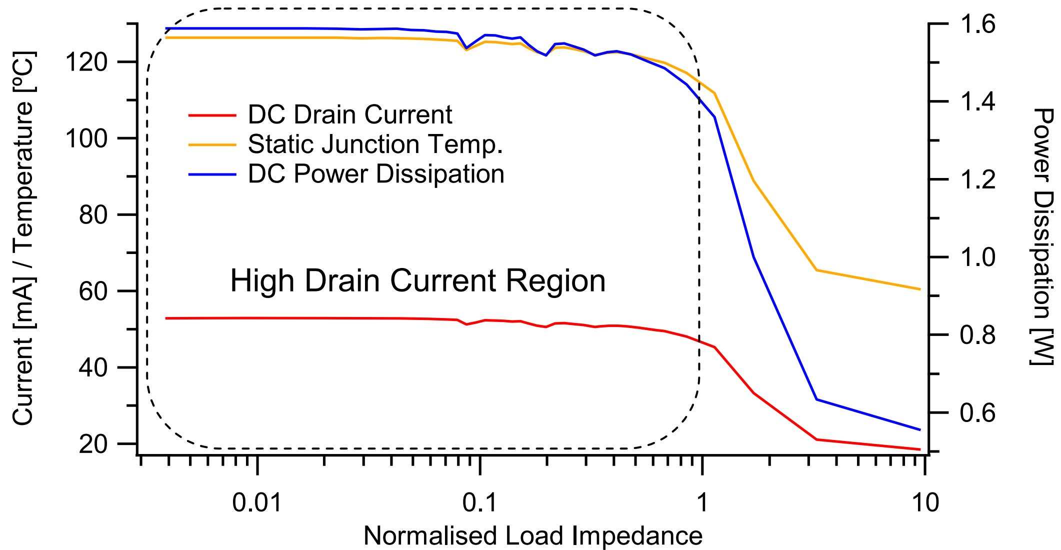


Figure 3.16 - DC drain current, DC power dissipation and static junction temperature (T_a=25°C) for a 2x50μm GaN HFET subjected to an infinite VSWR sweep

There is also a third condition that can be seen in the transition region

3) When the normalised impedance is unity the RF voltages and currents are the same as those generated at the optimum impedance, however the added phase difference between them leads to high instantaneous RF power dissipation, shown in figure 3.17.

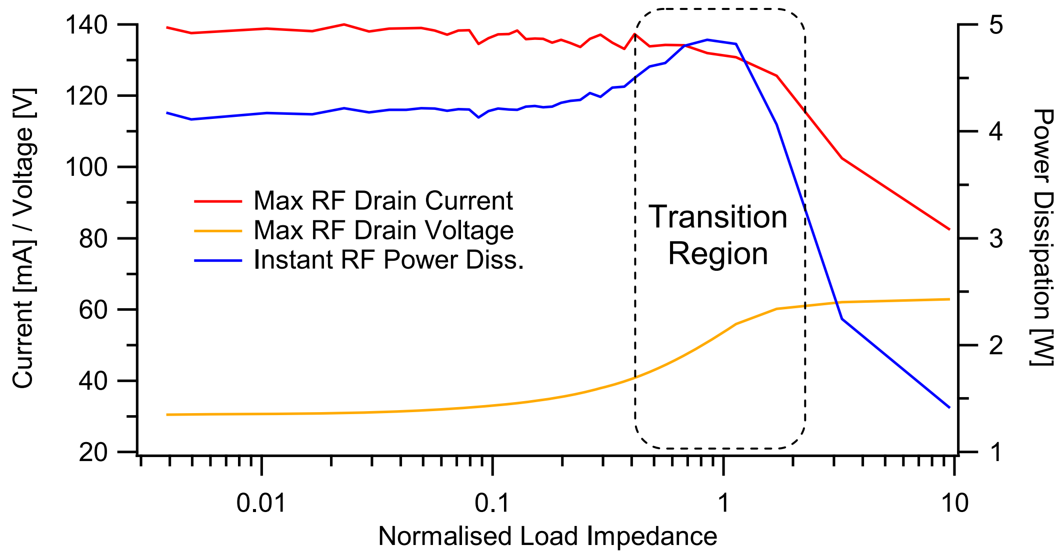


Figure 3.17 - Maximum RF drain current and voltage and instantaneous RF power dissipation for a 2x50µm GaN HFET subjected to an infinite VSWR sweep

Table 3.1 summarizes the potential failure mechanisms identified from the infinite VSWR sweep, relating them to the physical causes of device degradation. More information about the specific failure mechanisms can be found in the literature review in chapter 4.

Table 3.1 - Physical causes of degradation for the potential failure mechanisms for a GaN HFET subjected to an infinite VSWR sweep

VSWR Sweep Region	**Regime**	**Damage Mode**	**Section in Chapter 4**
High Voltage Region	High peak RF drain voltage	Soft/hard gate breakdown	4.3.1
	Forward biased gate-drain diode	Forward Gate Current – self-heating (thermal failure/trap generation)	4.3.3
Transition Region	High RF drain current/voltage	Self heating (thermal failure)	4.3.5
High Current Region	Class A bias point	Hot electron damage (trap generation)	4.3.4

3.5 Effect of Device Parameters on Infinite VSWR Sweeps

In the previous section the infinite VSWR sweep were studied and as a result three regions of the sweep were highlighted along with four potential failure mechanisms. In this section the effect of different parameters of device operation on the infinite VSWR sweep will be investigated.

3.5.1 Effect of Device Size on an Infinite VSWR Sweep

A larger periphery device will be able to conduct more current, and therefore have a lower optimum impedance than a smaller device. It was found previously in this chapter that the regions of an infinite VSWR sweep depend on the optimum impedance of the device. Therefore it can be seen that a smaller device will have a larger region of high RF drain current and a smaller region of high RF drain voltage swing than a larger device, and vice versa.

This effect is investigated below using two different device sizes, 2x50µm and 2x100µm GaN HFETs the optimum impedances of which are 350Ω and 175Ω respectively. The operating conditions used here are the same as in the previous section, a gate bias of -3.5V and a drain bias of 30V, the input power is set to saturate the output power when the device is driven into the optimum load impedance and the second and third harmonic load impedances set to short circuits. Figure 3.18 shows the load points measured during infinite VSWR sweeps on both devices, along with the contours of the magnitude of the optimum load impedance. From this it can clearly be seen that the transition region of the infinite VSWR sweep has moved due to the lower optimum impedance of the larger device.

Figure 3.19 shows the RF load lines from these infinite VSWR sweeps. The parameters associated with the potential failure mechanisms are shown in the subsequent figures; the high voltage region in figure 3.20, the transition region in figure 3.21 and the high current region in figure 3.22. It should be remembered that the transition region of the infinite VSWR is

shown around a normalised impedance of unity for both device, due to the process of normalisation.

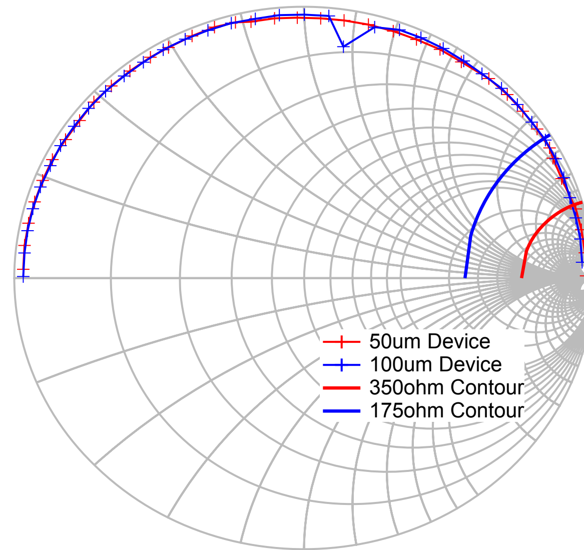


Figure 3.18 - Smith chart showing the load impedances of the infinite VSWR sweeps carried out on 2x50μm and 2x100μm GaN HFETs along with the contours of the devices optimum impedance

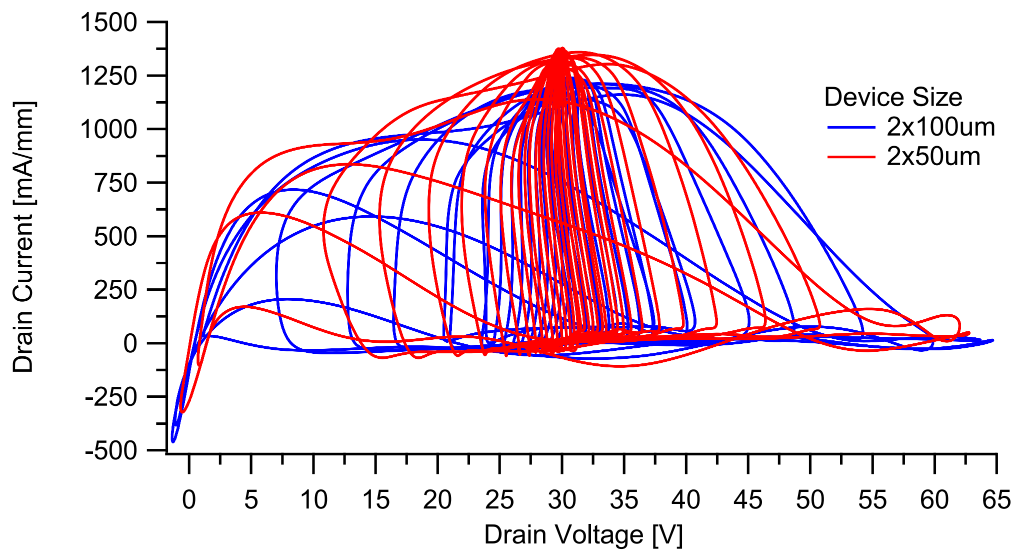


Figure 3.19 - RF load lines of infinite VSWR sweeps performed on a 2x50μm device and a 2x100μm device

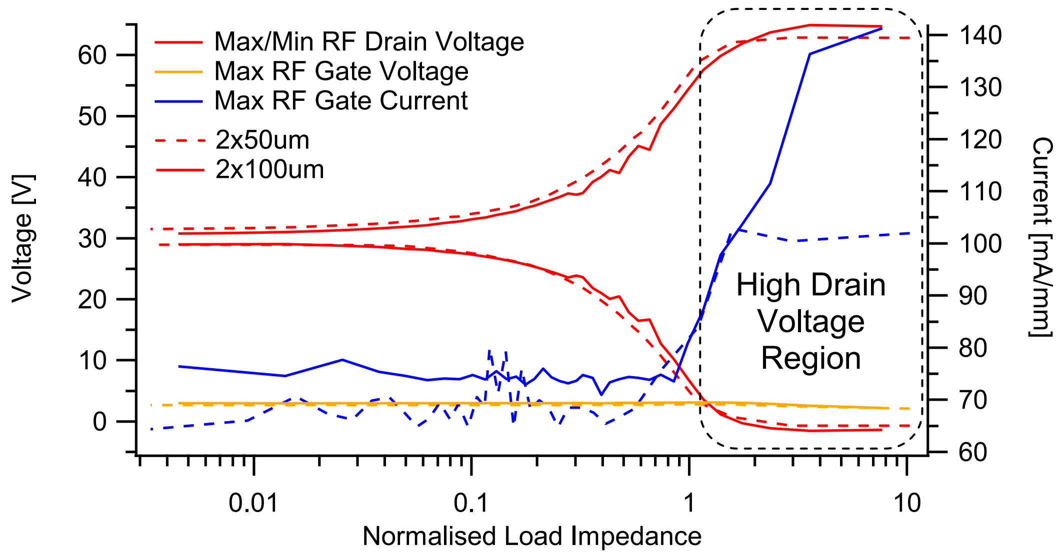


Figure 3.20 - Maximum and minimum RF drain voltage, maximum RF gate voltage and maximum RF gate current from the infinite VSWR sweeps performed on a 2x50µm device and a 2x100µm device

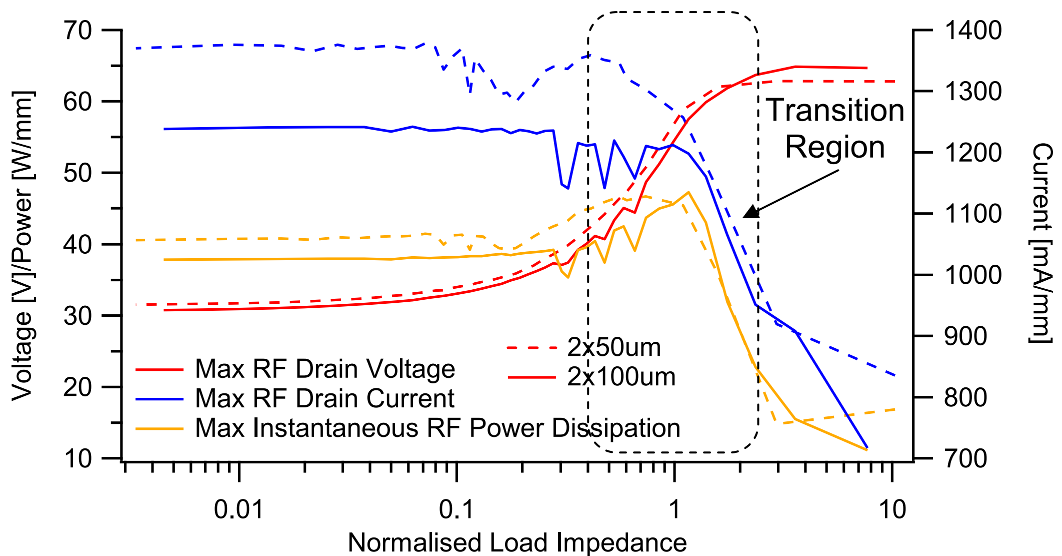


Figure 3.21 - Maximum RF drain voltage and current and maximum instantaneous RF power dissipation from the infinite VSWR sweeps performed on a 2x50µm device and a 2x100µm device

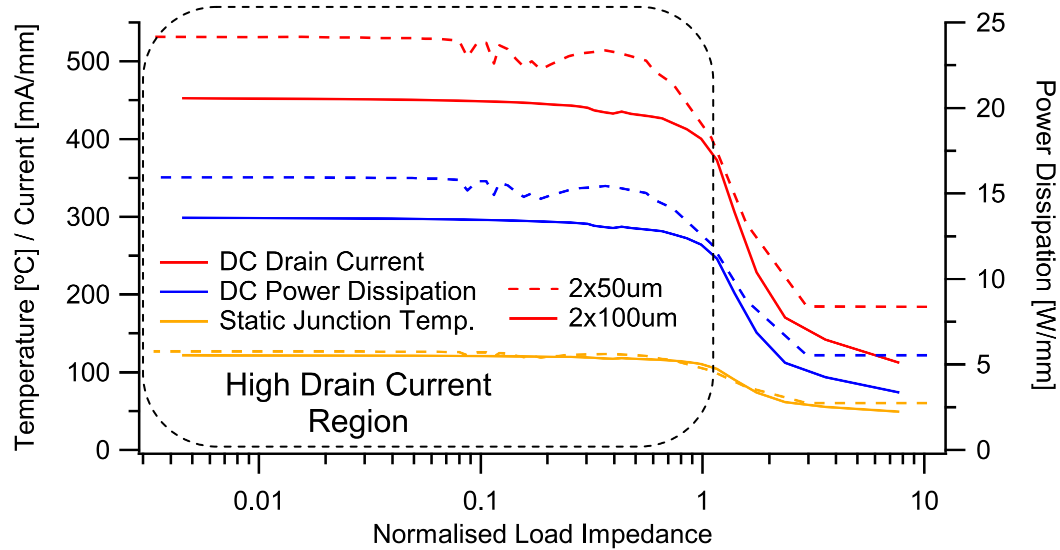


Figure 3.22 - DC drain current, DC power dissipation and static junction temperature from the infinite VSWR sweeps performed on a 2x50μm device and a 2x100μm device

From this it can clearly be seen that the infinite VSWR sweep performed on the larger device clearly displays the same three regions that were highlighted earlier. In addition the normalisation of the load impedance has succeeded in aligning the regions of both infinite VSWR sweeps for comparison. In the region of high drain voltage the RF drain voltage swings are maintained irrespective of the size of the device, as would be expected, however there is an increase in the RF gate current. When comparing the drain current densities it can be seen that they are higher for a smaller device. Whilst this appears to have minimal effect on the instantaneous RF power dissipation in the transition region, in the high drain current region this causes higher DC power dissipation per mm in the smaller device. However due to the differing thermal resistances of the two different sized devices, both have very similar static junction temperatures.

3.5.2 Effect of Drain Bias on an Infinite VSWR Sweep

A change in the drain bias voltage of the device will also cause the optimum impedance of the device to change. In this case a lower drain bias voltage will result in a lower optimum impedance. Infinite VSWR sweeps were performed at the five different drain bias voltages shown in table 3.2, starting at 10V and going up to 30V in 5V steps, on a 2x100µm GaN HFET. Also shown in table 3.2 are the optimum impedances for each drain bias voltage. For each drain bias voltage the gate was biased at -3.5V and the device driven so that the output power would saturate when presented with the optimum load impedance and the second and third harmonic load impedances set to short circuits. The load impedances measured in each of the sweeps is shown in figure 3.23, along with the contours of magnitude of optimum impedance. From this the change in boundary location due to the change in optimum impedance can be seen.

Table 3.2 - Drain bias voltages used in this section together with the optimum impedance at each voltage

Drain Voltage	Optimum Impedance
10V	65Ω
15V	105Ω
20V	145Ω
25V	160Ω
30V	175Ω

The RF load lines that represent the potential failure mechanisms found in an infinite VSWR sweep are shown below for each of the drain bias points. Figures 3.24 and 3.27 show the RF load lines and the parameters of interest for the high drain voltage region, figures 3.25 and 3.28 show the RF load lines and the parameters of interest for the transition region and figures 3.26 and 3.29 show the RF load lines and the parameters of interest for the high current region.

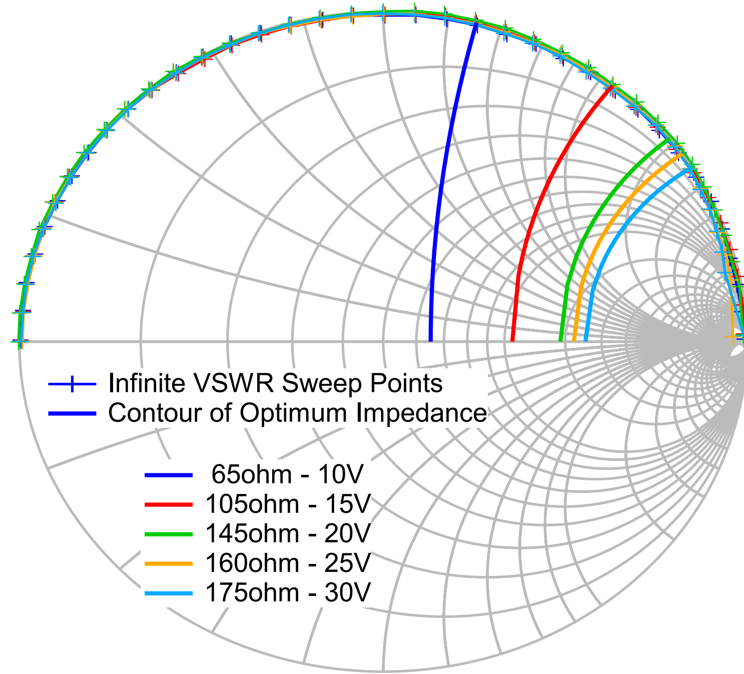


Figure 3.23 - Load impedance points of the infinite VSWR sweeps at 5 different drain bias points (shown in table 3.2) on a 2x100 GaN HFET, also shown are the contours of the magnitude of the optimum impedance for each of the 5 drain bias points

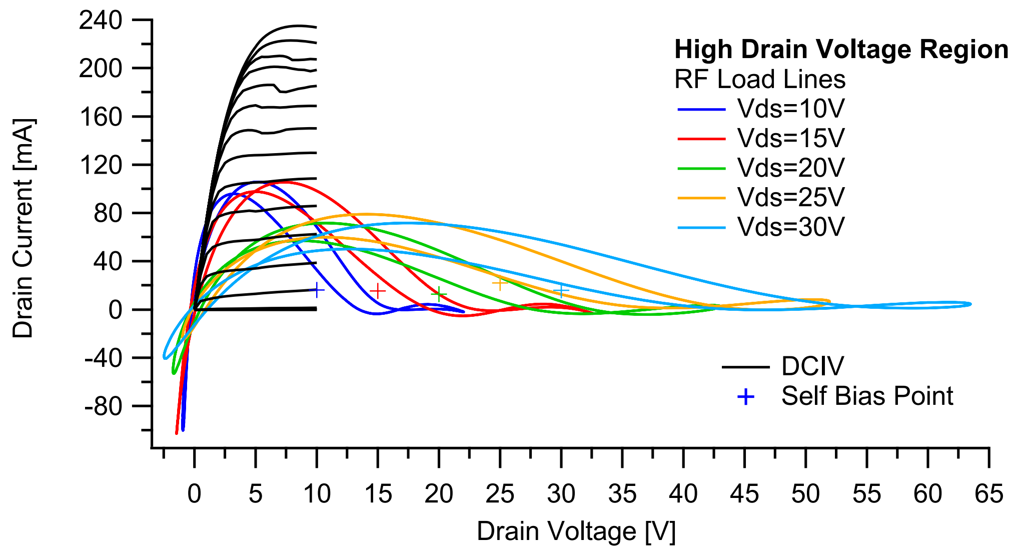


Figure 3.24 - RF load lines from the high drain voltage region of the infinite VSWR sweeps performed at the drain bias points shown in table 3.2, on a 2x100µm GaN HFET

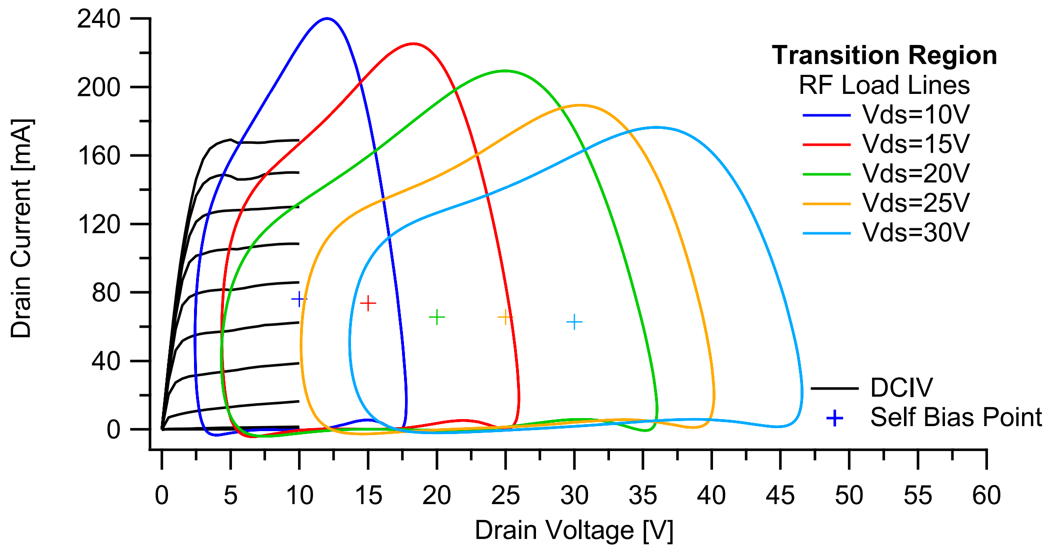


Figure 3.25 - RF load lines from the transition region of the infinite VSWR sweeps performed at the drain bias points shown in table 3.2, on a 2x100µm GaN HFET

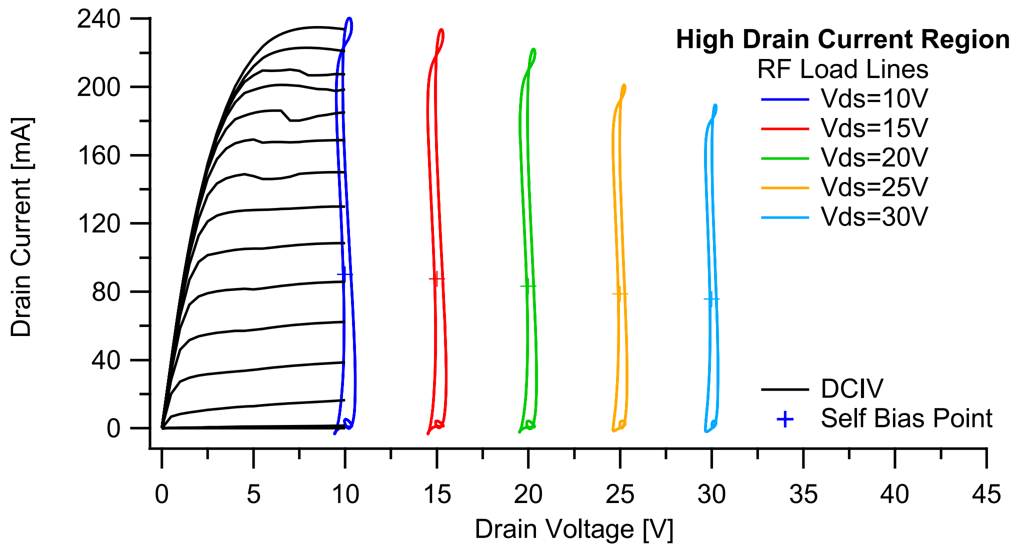


Figure 3.26 - RF load lines from the high drain current region of the infinite VSWR sweeps performed at the drain bias points shown in table 3.2, on a 2x100µm GaN HFET

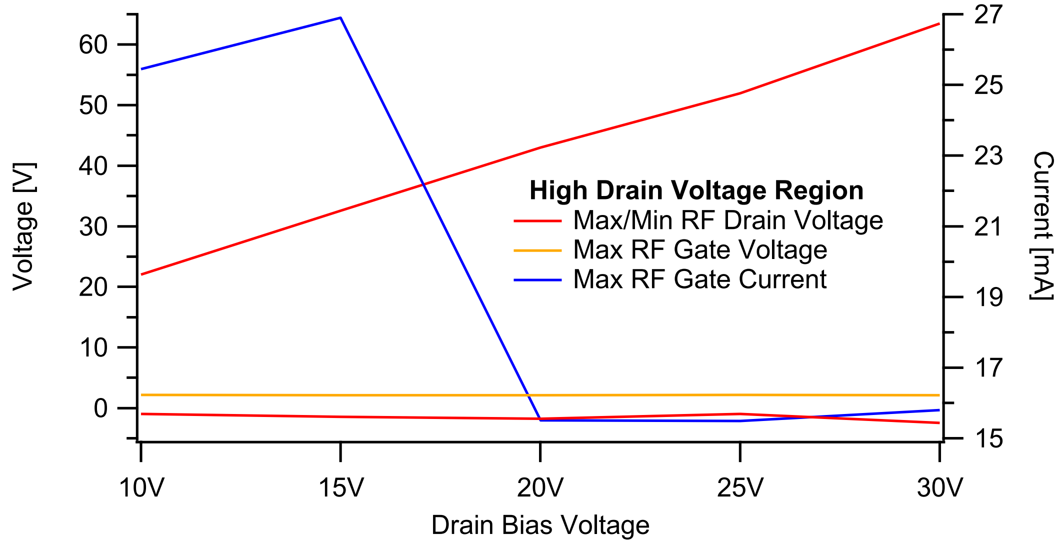


Figure 3.27 - Maximum and minimum RF drain voltage, maximum RF gate voltage and maximum RF gate current of the infinite VSWR sweeps performed at the drain bias points shown in table 3.2, on a 2x100μm GaN HFET

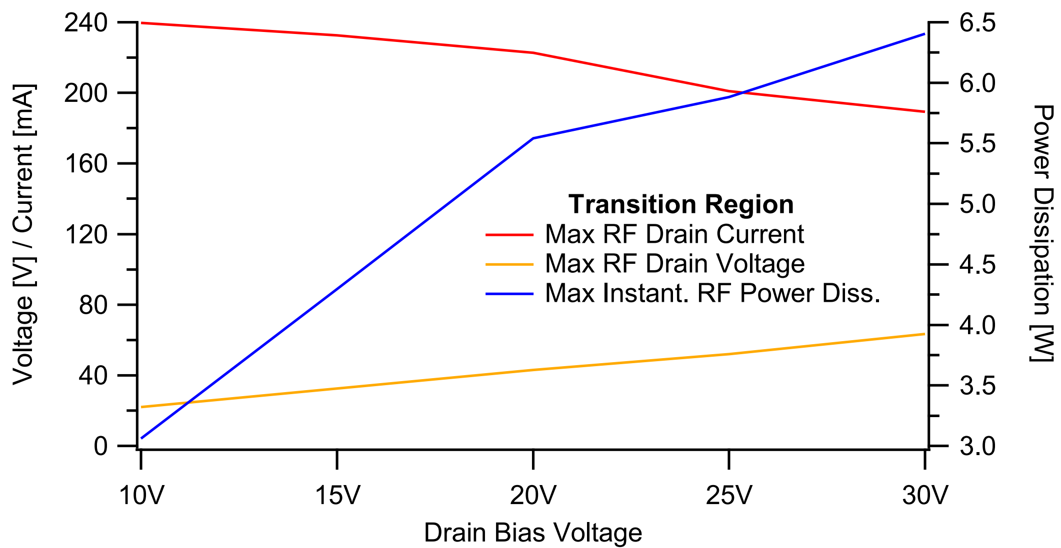


Figure 3.28 - Maximum RF drain current and voltage and maximum instantaneous RF power dissipation for the infinite VSWR sweeps performed at the drain bias points shown in table 3.2, on a 2x100μm GaN HFET

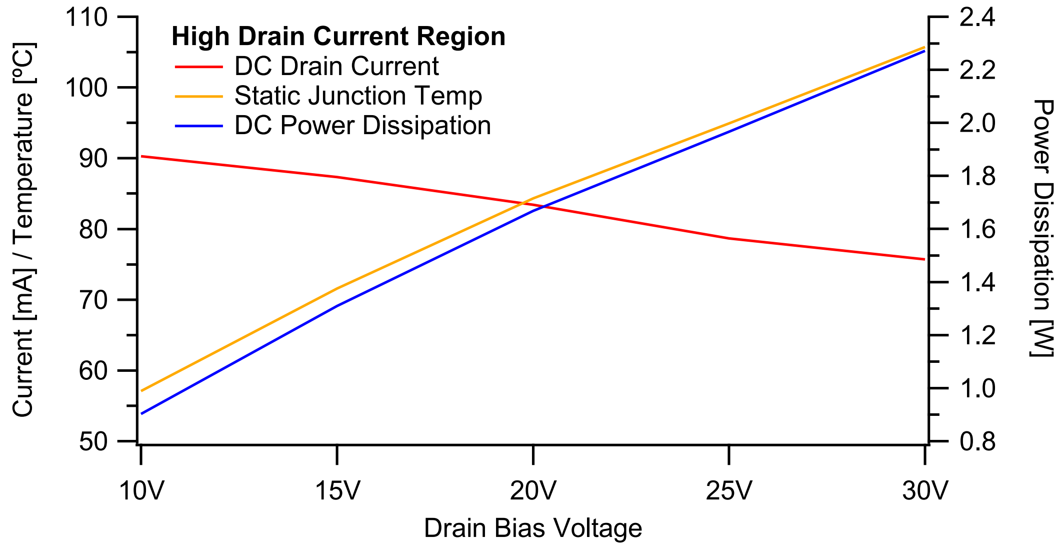


Figure 3.29 - Maximum DC drain current, DC power dissipation and static junction temperature (T_a=25°C) for the infinite VSWR sweeps performed at the drain bias points shown in table 3.2, on a 2x100µm GaN HFET

From these it can be seen that the increase in peak RF drain voltage in the region of high RF drain voltage is consistent with increasing drain bias voltage. In addition the minimum RF drain voltage always falls below the maximum RF gate voltage irrespective of the drain bias voltage, as would be expected due to the 180° phase difference between the gate and drain voltage waveforms, leading to the increased gate currents. The drain bias also has an effect on the magnitude of the peak RF current. From the high drain current and the transition regions it can be seen that as the drain bias voltage increases the peak RF and DC drain currents begin to fall. There is also an additional increase in the rate of reduction of the RF peak drain currents after the 20V drain bias. This general decrease is suspected to be due to the increase in the temperature of the device as the drain bias voltage (and therefore DC power dissipation) increases. The increased rate of RF reduction is suspected to be due to DC-RF dispersion, which is described in section 4.3.1. Despite these reductions the instantaneous RF and the DC power dissipation increase with drain bias, each doubling over the 20V range tested.

3.5.3 Effect of Input Power on Infinite VSWR Sweeps

In this section, four infinite VSWR sweeps have been measured at different levels of input power to investigate the effect on the potential failure mechanisms. The four input power levels used are shown in table 3.3, together with their relationship with the input power required to saturate the output power of the device when driven into the optimum impedance, labelled as P_{inSat}. The device is operated in class AB modes (V_{GS}=-3.5V) at a drain bias of 30V, with the second and third harmonic impedances set to short circuits.

Table 3.3 - The input powers used when measuring the VSWR sweeps and their relationship to the input power needed to saturate the output power of the device

Input Power (dBm)	Relation to P_{inSat} (dBm)
14	$P_{inSat} - 6$
17	$P_{inSat} - 3$
20	P_{inSat}
23	$P_{inSat} + 3$

The following figures show how the input power applied to the device during an infinite VSWR sweep affects each of the regions of the sweep. The RF load lines from each of the sweeps are shown in figure 3.30 for the high drain voltage region, figure 3.31 for the transition region and figure 3.32 for the high drain current region. The parameters of interest in each of the regions are shown in figure 3.33 for the high drain voltage region, figure 3.34 for the transition region and figure 3.35 for the high drain current region

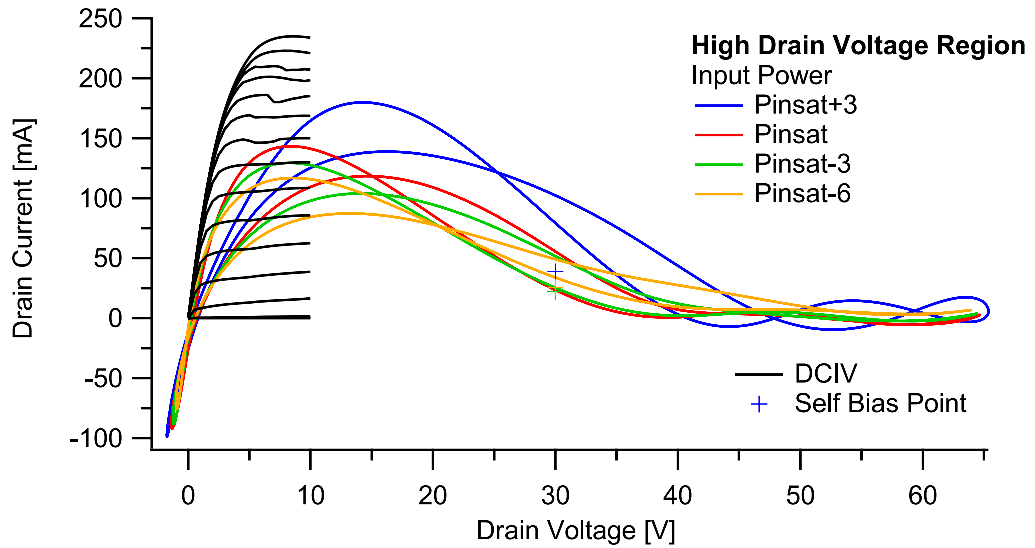


Figure 3.30 - RF Load lines from a load impedance in the high voltage region of each of the for the four infinite VSWR sweeps at the input power levels shown in table 3.3

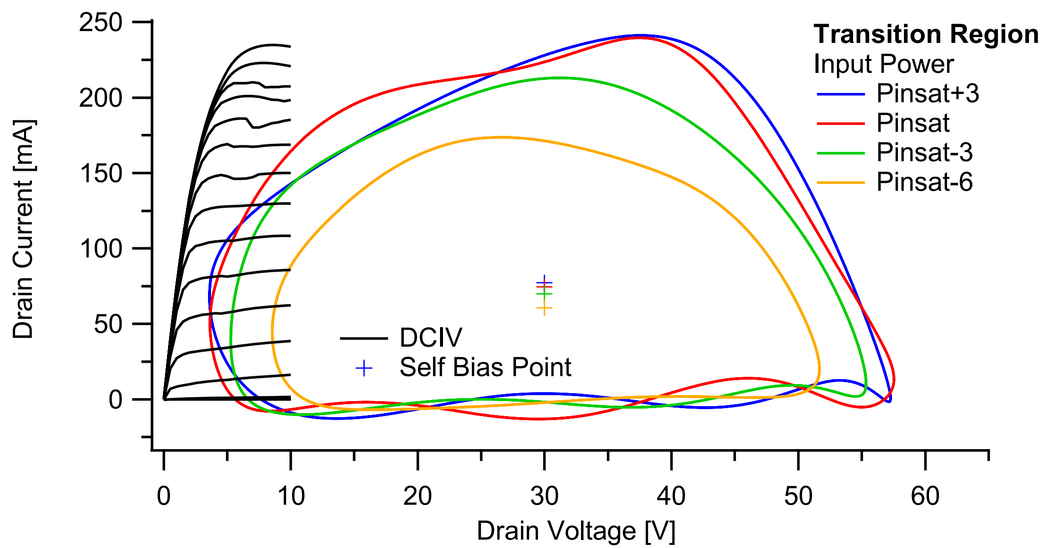


Figure 3.31 - RF Load lines from the load impedance on the boundary between high voltage and current region from each of for the four infinite VSWR sweeps at the input power levels shown in table 3.3

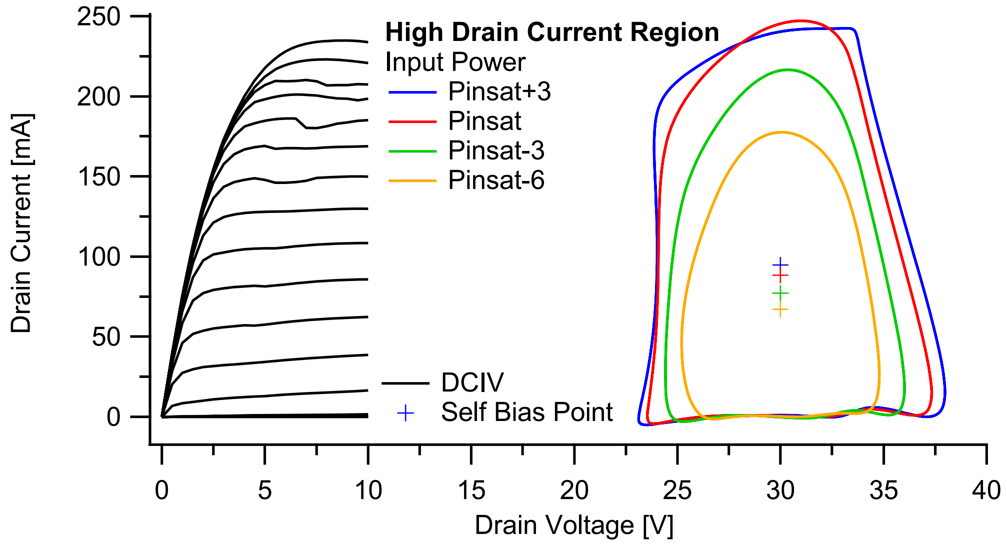


Figure 3.32 - RF Load lines from a load impedance in the high current region for each of for the four infinite VSWR sweeps at the input power levels shown in table 3.3

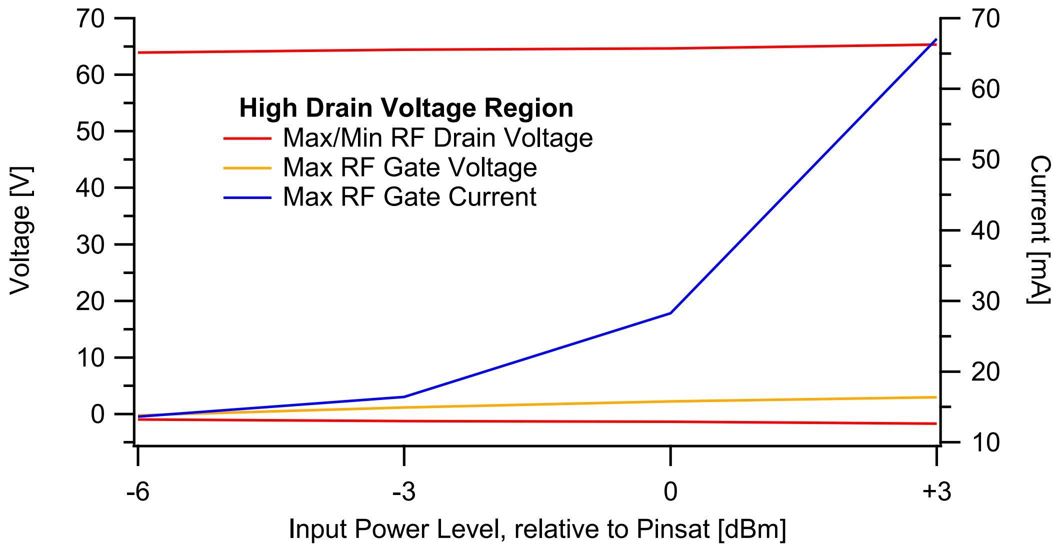


Figure 3.33 - Maximum and minimum RF drain voltage, maximum RF gate voltage and current for the four infinite VSWR sweeps at the input power levels shown in table 3.3

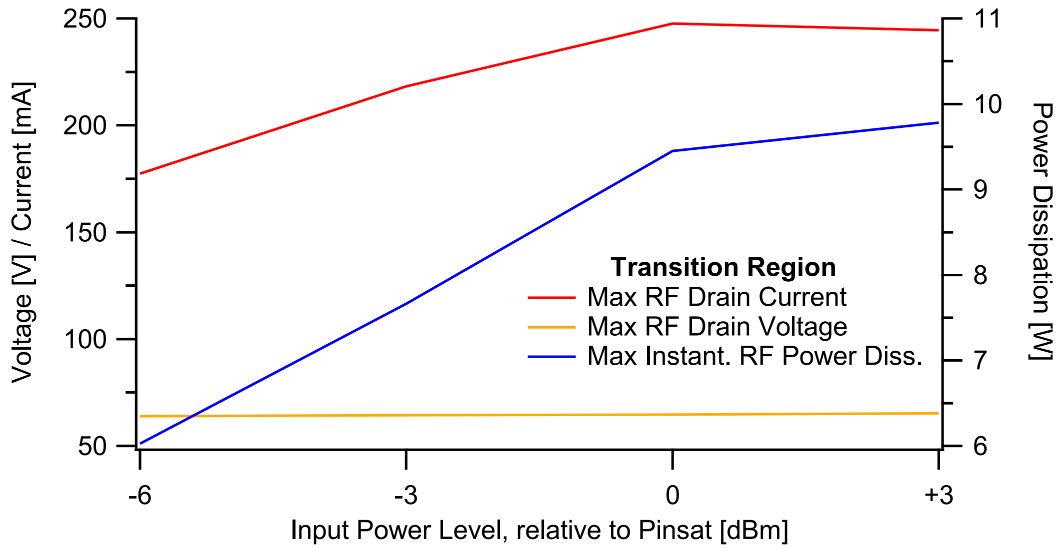


Figure 3.34 - Maximum RF drain current and voltage and maximum instantaneous RF power dissipation for the four infinite VSWR sweeps at the input power levels shown in table 3.3

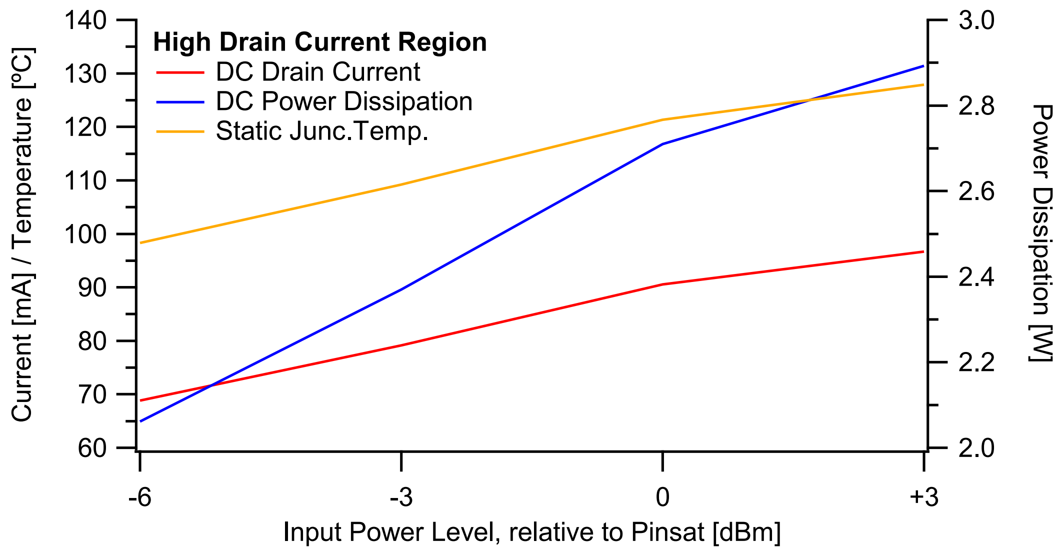


Figure 3.35 - DC drain current, DC power dissipation and static junction temperature for the four infinite VSWR sweeps at the input power levels shown in table 3.3

From this it can be seen that an increase in the input power causes an increase in the peak RF drain currents seen throughout the infinite VSWR sweep, up to when the input power exceeds that needed to saturate the device. After this drive level the peak drain current remains at the same level but the saturation causes the RF drain current waveforms to begin to “square up”, as can be seen in the load lines for the high drain current region in figure 3.35. This increase in peak RF drain current and subsequent saturation also causes a natural increase in the quiescent drain current. These increases

are also shown in the instantaneous RF power dissipation, the DC power dissipation and static junction temperature.

It can also be seen that a change in the input power causes little change in the RF drain voltage swing, which is as expected due to the fundamental being presented with a very high load impedance. This is particularly interesting in the high drain voltage regions of the infinite VSWR sweeps as it confirms that the drain voltage swing is constrained to a physical maximum.

3.6 VSWR Sweeps

In the previous section the worst possible case scenario, the infinite VSWR sweep was measured. However as previously discussed the infinite VSWR sweep may not always be the best possible test. In order to assess the impact of lower VSWR on the potential failure mechanisms seen during the infinite VSWR sweep a series of sweeps of different VSWR ratios were performed on both 2x50μm and 2x100μm devices. These VSWRs are shown in table 3.4, together with the reflection coefficient magnitude needed to generate them. As with the infinite VSWR sweep the RF waveform measurement system was used to perform the sweeps.

Table 3.4 - VSWR and the reflection coefficient magnitude needed to create them, for the VSWR sweeps performed in this section. These are the same as the VSWR shown in table 2.8

VSWR	Reflection Coefficient Magnitude
1:1	0
1.5:1	0.2
3:1	0.5
5:1	0.667
7:1	0.75
10:1	0.826
19:1	0.9
99:1	0.98

Initially the VSWR sweeps were performed on 2x100μm over the inductive portion of the Smith chart, the RF load lines for these measurements are shown individually in appendix 1. All of the RF waveforms are de-embedded for a C_{ds} of 0.08pF (0.4pF/mm). The load impedances from the VSWR sweeps are shown on the Smith chart in figure 3.36, along with the contour of the magnitude of the optimum impedance. The parameters associated with the three regions of the infinite VSWR sweep are shown in figures 3.37, 3.38 and 3.39.

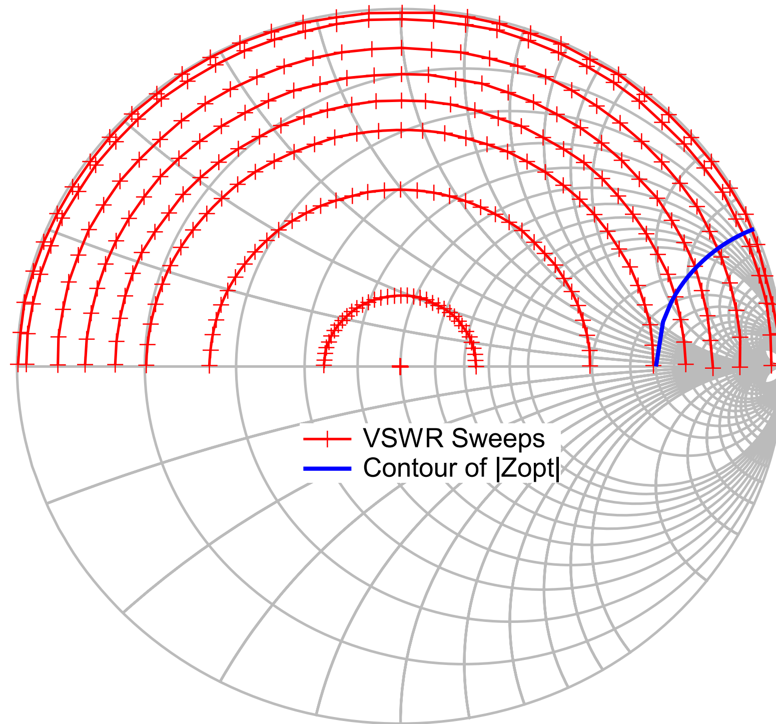


Figure 3.36 - Smith chart showing the load points of the VSWR sweeps described in table 3.4 measured on a 2x100μm GaN HFET, along with the impedance contour of the magnitude of the optimum impedance

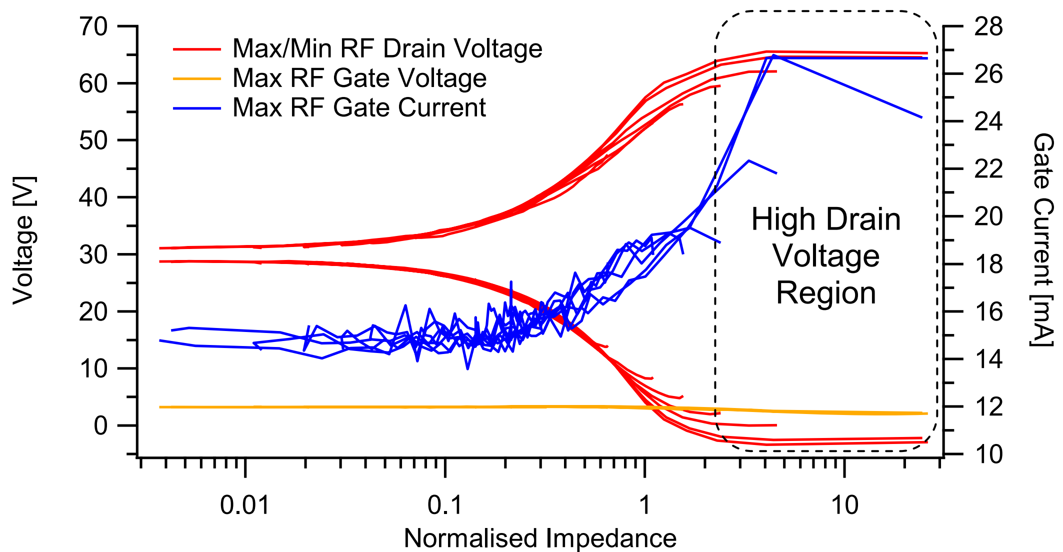


Figure 3.37 - Maximum and minimum RF drain voltage and maximum RF gate voltage together with the maximum RF gate current for the VSWR sweeps from table 3.4 performed on a 2x100μm GaN HFET

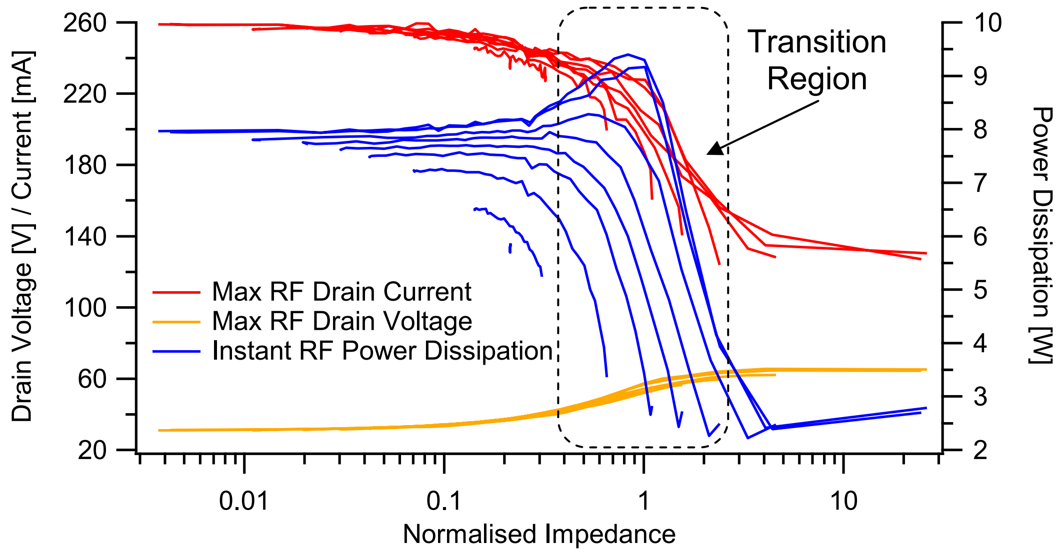


Figure 3.38 - Maximum RF drain current and voltage and the resulting instantaneous RF power dissipation for the VSWR sweeps from table 3.4 performed on a 2x100µm GaN HFET

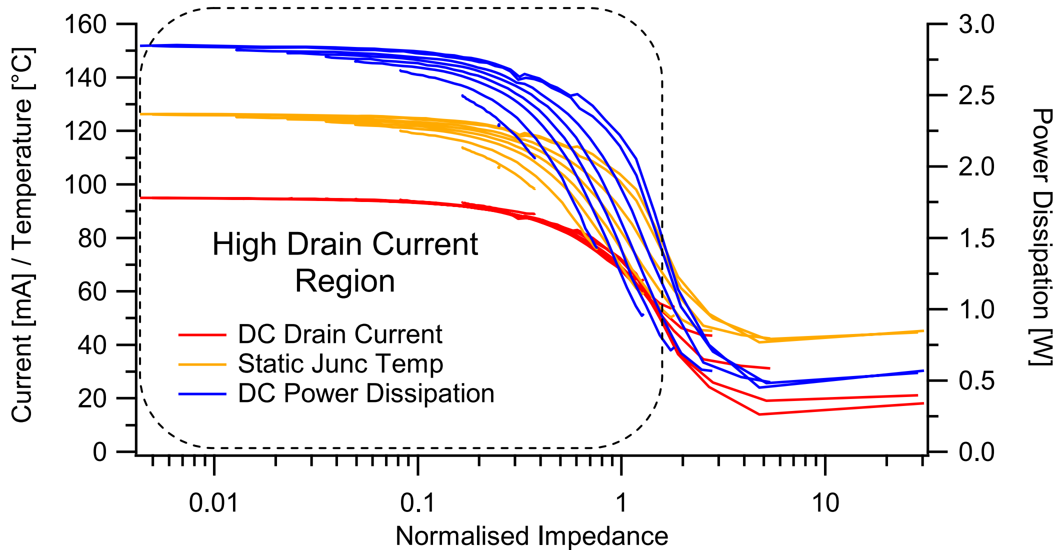


Figure 3.39 - DC drain current and power dissipation and the associated static junction temperature for the VSWR sweeps from table 3.4 performed on a 2x100µm GaN HFET

As with the infinite VSWR sweep the regions of high drain voltage swing (normalised impedance greater than one) and high peak drain current (normalised impedance less than one) can clearly be seen. It is important to note that each of the parameters follows the same trajectory on the graphs irrespective of the ratio of the standing wave, only their “length” along the trajectory is determined by the VSWR of the sweep (the exceptions are the measurements of power dissipation). The longest of these trajectories is for the infinite VSWR sweep as this sweep presents the greatest range of

impedances. It can also be seen that as the VSWR of the sweeps reduces the sweeps are no longer entering the high RF drain voltage swing region seen in the infinite VSWR sweep. This is the result of the characteristic impedance of our measurement system (50Ω) (the impedance set for the 1:1 VSWR sweep) being less than the optimum impedance of the device. As the VSWR increases the sweeps extend outwards from this point. From this it can be seen that only sweeps with VSWR above 5:1 will cross through the transition region to the high RF drain voltage swing region.

The reason for the measurements of power dissipation not staying on the same trajectories is due to the increased real component that is contained in the fundamental load impedance as the VSWR of the sweep is reduced. The increased real impedance leads to an increase in the RF power being dissipated in the load, resulting in a reduction in the DC power dissipated in the device during the VSWR sweeps. In the case of the instantaneous RF power dissipation this reduction is due to the phase difference between the drain voltage and current waveforms. The phase difference is 90° for a purely reactive load impedance during the infinite VSWR sweep. However as the VSWR of the sweep reduces and there is more real component in the load impedance the phase difference varies less during the sweep.

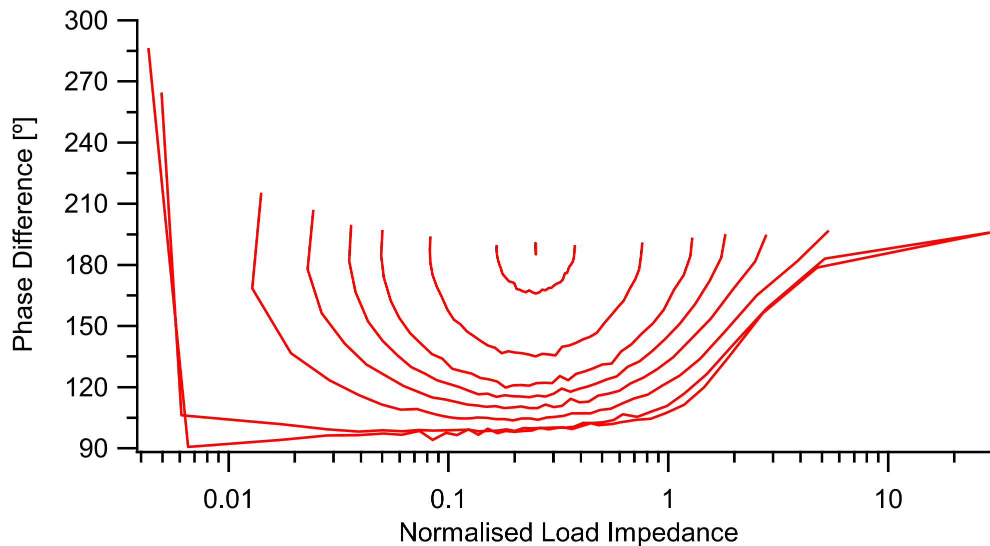


Figure 3.40 - Phase difference between the drain voltage and drain current waveforms during the VSWR sweeps shown in table 3.4, performed on a 2x100μm GaN HFET

Additionally, the parameters associated with each of the potential failure mechanisms from the infinite VSWR sweep can be plotted on Smith charts of normalised impedance [6]. This has the advantage of distributing the regions of the infinite VSWR sweep equally across the Smith chart, as shown in figure 3.41. These measurements were carried out on a 2x50µm GaN HFET, in class AB (V_{GS}=-3.5V) at a drain bias voltage of 30V and with the input power set to saturate the output power. In addition the second and third harmonic impedances set to short circuits and the results are de-embedded with a C_{DS}=0.08pF (0.8pF/mm). .

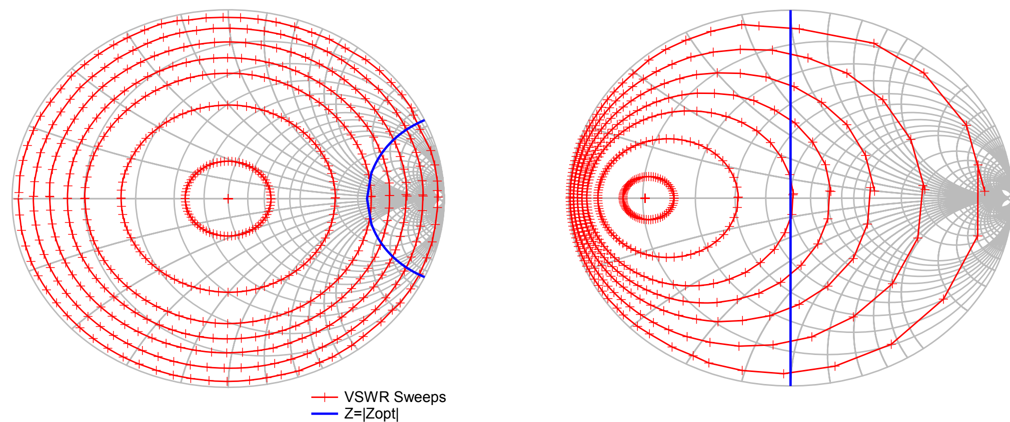


Figure 3.41 - Smith charts showing the load points of the VSWR sweeps described in table 3.4 in the 50Ω impedance environment and in the normalised impedance environment for a 2x50µm GaN HFET biased at V_{DS}=30V

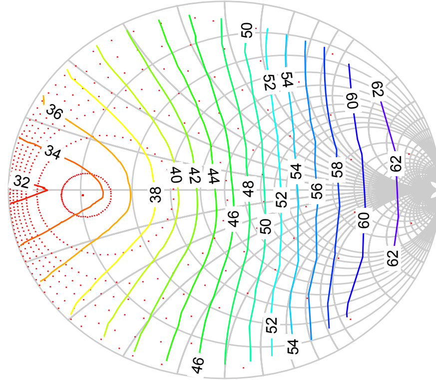
For the high voltage region of the VSWR sweeps the important parameters are the peak RF drain voltage, shown in figure 3.42, and the maximum RF gate-drain voltage and the maximum RF gate current, both shown in figure 3.43. The gate-drain voltage is defined as the minimum RF drain voltage minus the maximum RF gate voltage, the value of which becomes negative when the gate-drain diode becomes forward biased.

For the transition region between the high voltage and high current regions the important parameters are the peak RF drain voltage and current, both shown in figure 3.43, which leads to a high instantaneous RF power dissipation, shown in figure 3.44.

Finally for the high current region the important parameters are the peak RF drain current, shown in figure 3.43, the DC drain current and static

junction temperature, shown in figure 3.45, and the DC power dissipation, shown in figure 3.44.

Peak RF Drain Voltage



Peak RF Drain Current

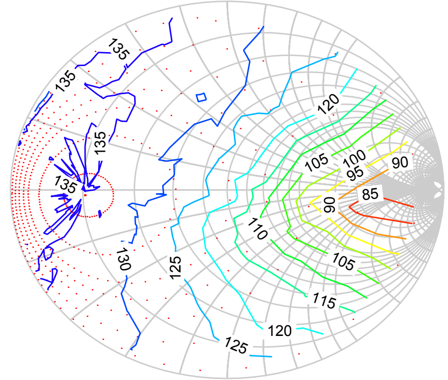
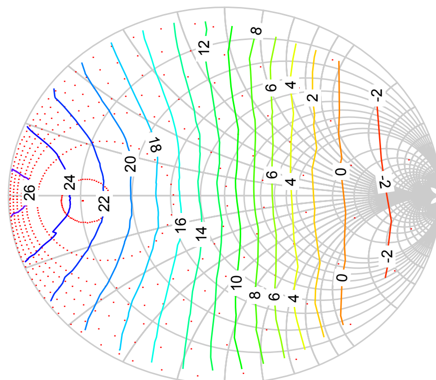


Figure 3.42 - Peak RF drain voltage and current for the VSWR sweeps on a 2x50µm GaN HFET

Maximum Gate-Drain Voltage



Maximum RF Gate Current

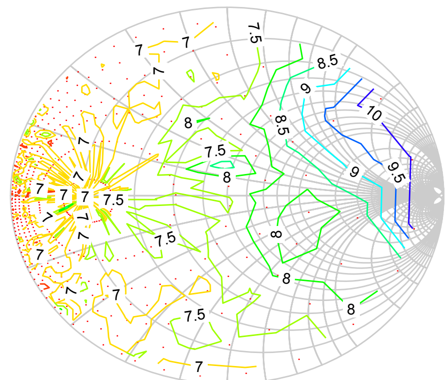
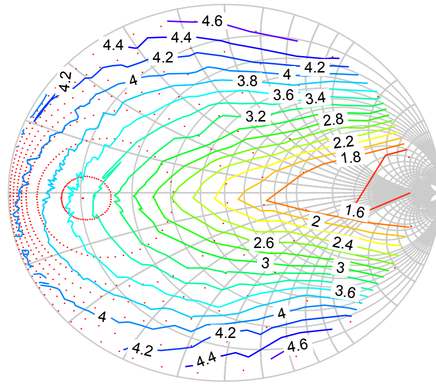


Figure 3.43 - RF gate-drain voltage and peak RF gate current for the VSWR sweeps on a 2x50µm GaN HFET

Max Instantaneous RF Power Dissipation



DC Power Dissipation

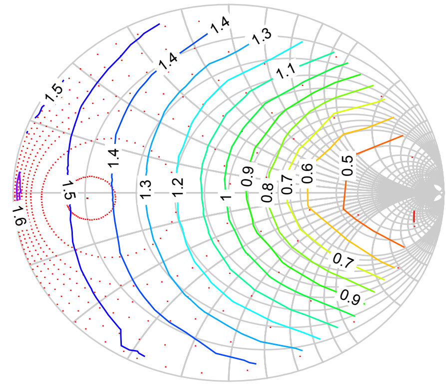
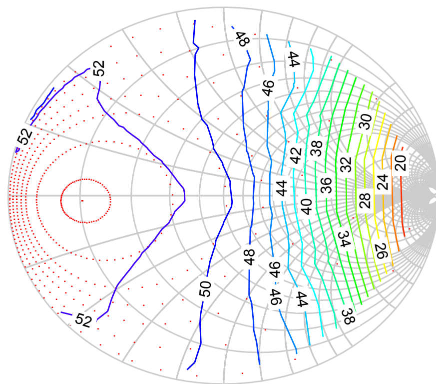


Figure 3.44 - Maximum instantaneous RF power dissipation and DC power dissipation for the VSWR sweeps on a 2x50µm GaN HFET

DC Drain Current



Static Junction Temperature

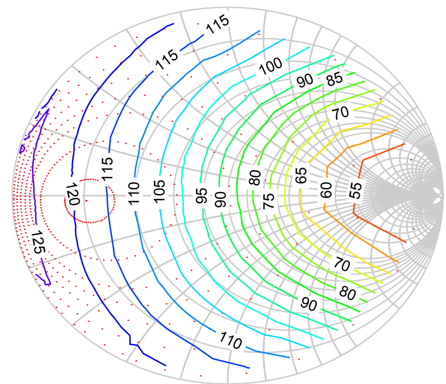


Figure 3.45 - DC drain current and static junction temperature for the VSWR sweeps on a 2x50µm GaN HFET

3.7 RF Waveform Harmonic Content

In order to investigate further the regions of the infinite VSWR sweep the results of the sweep performed in section 3.4.2 were analysed by means of a Fourier transform. The original RF load lines measured during this sweep can be seen in figure 3.10. The first five harmonics for the RF drain voltages are shown in figure 3.46, and for the RF drain currents waveforms in figure 3.47, along with the DC drain current.

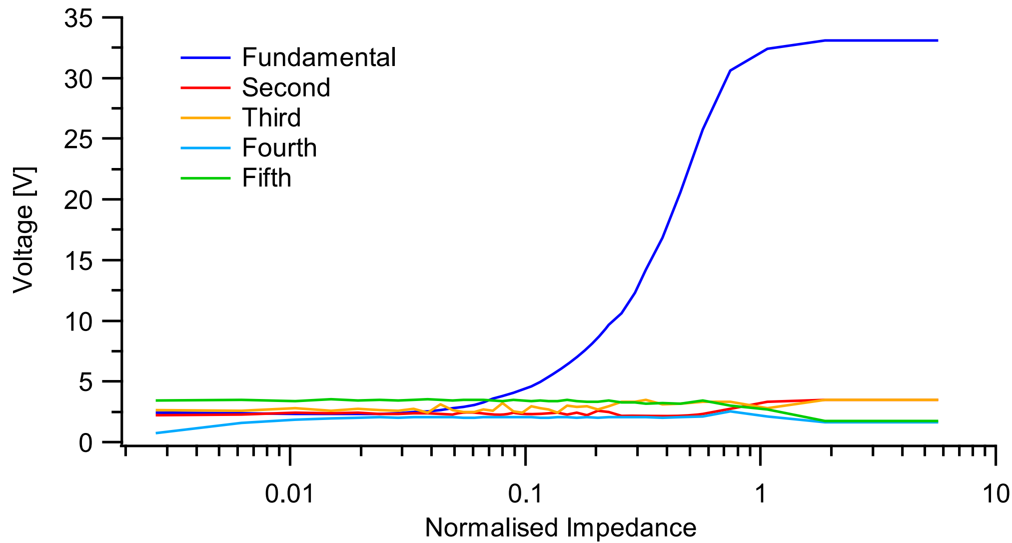


Figure 3.46 - Harmonic components of the RF drain voltage waveforms generated during the infinite VSWR on a 2x50μm GaN HFET at a drain bias of 30V, shown in figure 3.15

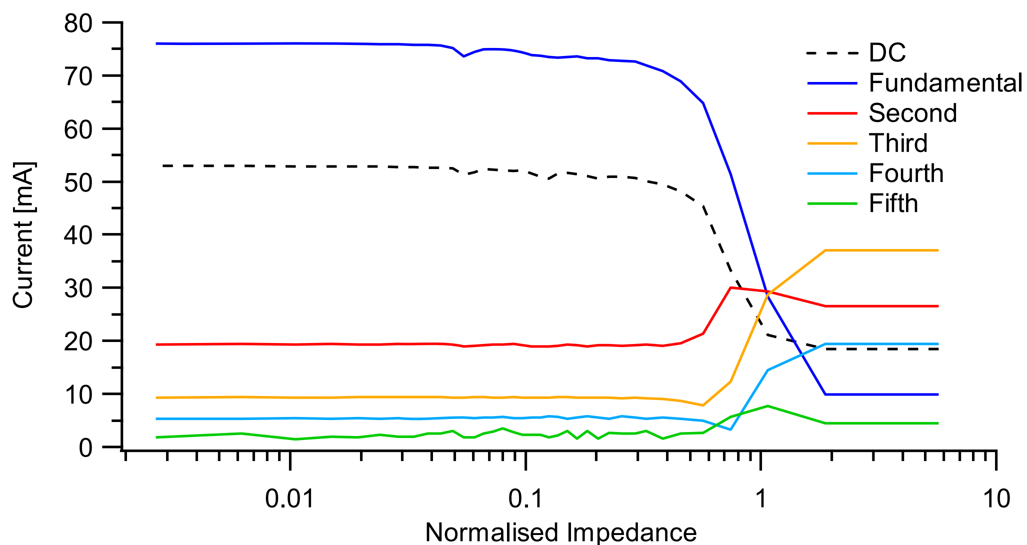


Figure 3.47 - Harmonic components of the RF drain current waveforms generated during the infinite VSWR on a 2x50μm GaN HFET at a drain bias of 30V, shown in figure 3.15

This confirms that, as already discussed, there is a small RF drain voltage swing in the high current region of the infinite VSWR sweep due to the low fundamental load impedance. As the impedance increases during the sweep the fundamental voltage swing increase until the optimum impedance is reached. At this point the interaction with the device knee causes a drop in the fundamental RF drain current, and an increase in the harmonic components. Throughout the entire sweep there is a low harmonic voltage component, due to the second and third harmonic impedances being set to short circuits and the higher harmonics being terminated with the 50Ω system impedance.

3.7.2 Influencing the Harmonic Content

The waveforms produced by a transistor can be varied greatly by changing the load impedances of the harmonics, an approach that has been used extensively to create high efficiency operating modes (section 2.42). The same approach can be used here to alter the waveforms produced during VSWR sweeps [5]. Up till now both the second and third harmonic impedances have been set to a short circuit in order to minimise any harmonic content in the drain voltage waveform. However by alternately setting these harmonic impedances to an open circuit it will force the RF drain voltage waveform to contain second and third harmonic voltages.

In this section four infinite VSWR sweeps were performed with the combinations of harmonic load impedances shown in table 3.5. It should be noted that in a couple of cases these combinations of harmonic load impedances presented stability issues for the device. Therefore in these cases the harmonic open circuit impedances were reduced to $|\Gamma|$=0.75, in order to reduce that harmonic voltage component.

In order to investigate the effect these have on the potential failure mechanisms the RF waveforms were analysed at a specific fundamental load impedance from each of the three infinite VSWR sweep regions. The infinite VSWR sweeps were performed under identical conditions to the sweep shown in figure 3.3, and described in section 3.4.

Table 3.5 - Combinations of second and third harmonic impedance for each of the infinite VSWR sweeps performed in this section.

Sweep Number	Second Harmonic	Third Harmonic
1	Short Circuit	Short Circuit
2	Open Circuit	Short Circuit
3	Short Circuit	Open Circuit*
4	$|\Gamma|$=0.75	$|\Gamma|$=0.75

Table 5.1 - * This condition presented stability problems in the high drain current region of the infinite VSWR sweeps so the open circuit impedance at the third harmonic was reduced to $|\Gamma|$=0.75

3.7.2.2 High RF Drain Voltage Region

The RF load lines observed when the fundamental load impedance is set to the open circuit, for the four infinite VSWR sweeps described above, are shown in figure 3.48, and the RF waveforms are shown in figure 3.49.

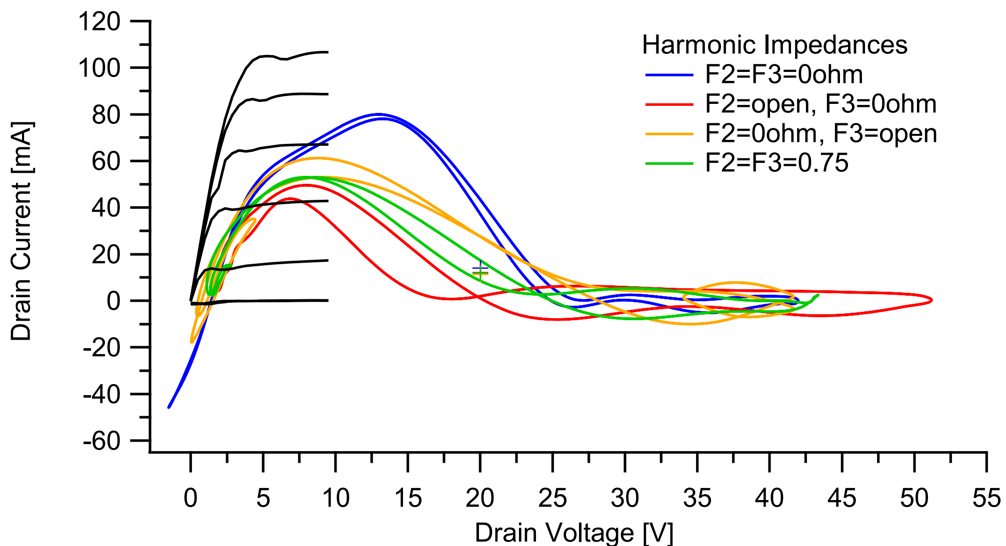


Figure 3.48 - RF load lines for the high drain voltage region of the infinite VSWR sweeps described in table 3.5, performed on a 2x50µm GaN HFET

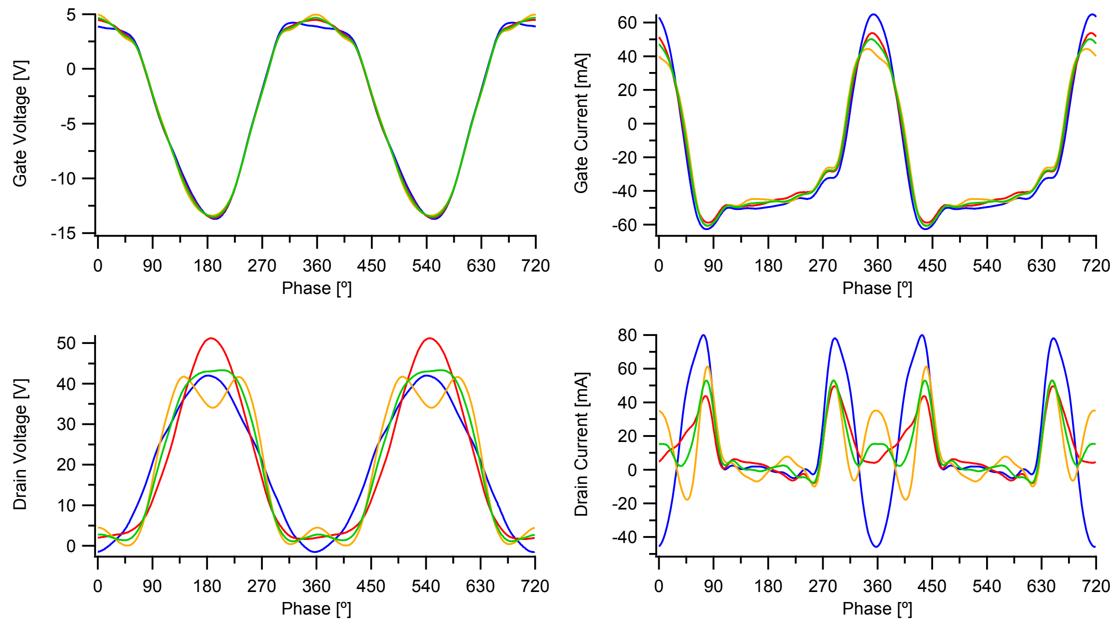


Figure 3.49 - RF waveforms for the load lines shown in figure 3.48

From this it is possible to see that when the second harmonic is set to an open circuit the RF drain voltage waveform becomes half rectified causing a much larger RF drain voltage swing. This also has the effect of limiting the low voltage region of the waveform, preventing it from dropping below 0V. When the third harmonic (whether the second harmonic is set to a short or open circuit) is set to an open circuit the RF drain voltage waveform approaches a square wave causing both the high and low voltage regions of the waveform to be constrained. In addition any combination of setting the second or third harmonic load impedances to an open circuit causes a drop in the overall maximum RF drain current, and also reduces the peak negative current. As would be expected, varying the harmonic load impedances causes minimal change in the input waveforms.

3.7.2.3 Transition Region

Figure 3.50 shows the RF load lines associated with the case where the load impedance is in the transition region of the four infinite VSWR sweeps from table 3.5. The RF waveforms are shown in figure 3.51.

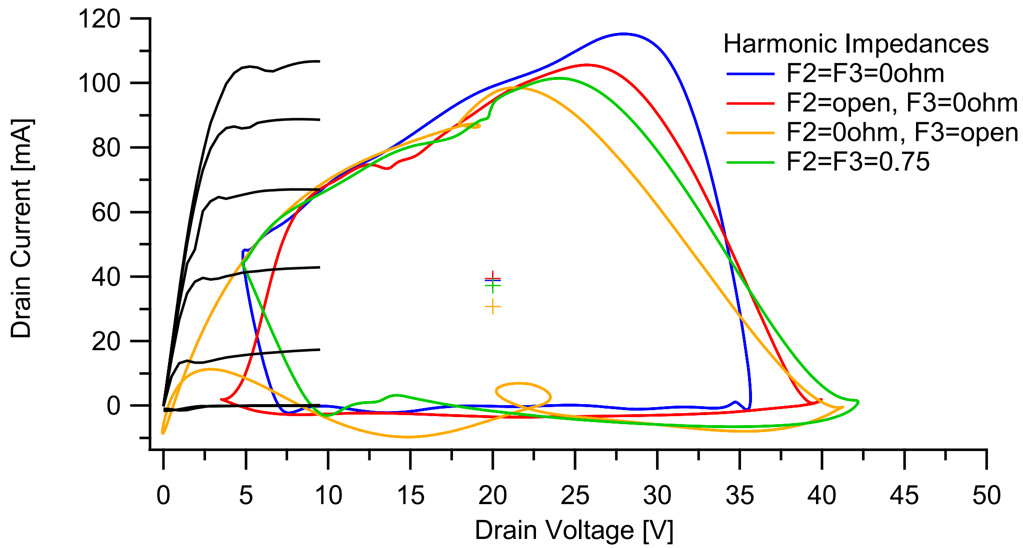


Figure 3.50 - RF load lines for the transition region of the infinite VSWR sweeps described in table 3.5, performed on a 2x50µm GaN HFET

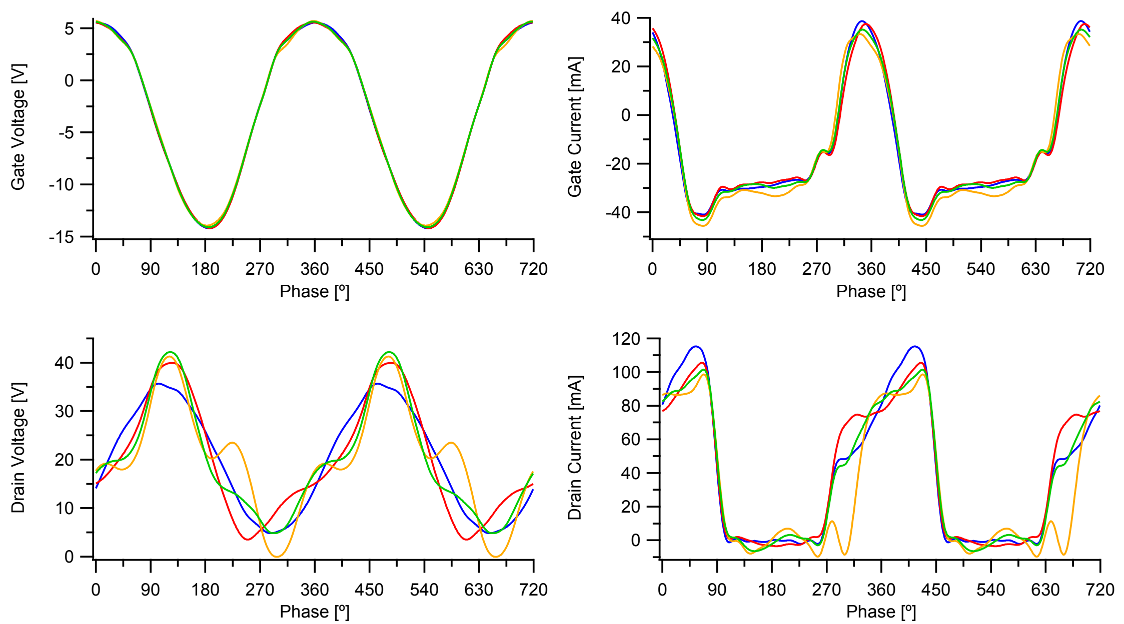


Figure 3.51 - RF waveforms for the load lines shown in figure 3.50

Unlike for the previous case the harmonic content in the voltage waveforms do not act as expected, i.e. squaring the waveform when the third is added and half rectifying when the second is added. This is due to the change in the phase of the fundamental voltage component caused by the reactive load impedance discussed in section 3.4.1. This causes the drain voltage waveforms to begin to resemble triangular waves, where both the maximum and minimum of the wave are increased. As discussed earlier the

drain current waveforms in the transition region of the infinite VSWR sweep show interaction with the knee region of the devices IV operating plane. This interaction is predominantly unaffected by the harmonic load impedances.

3.7.2.4 High RF Drain Current Region

Figure 3.52 shows the RF load lines from the high drain current region of the four infinite VSWR sweeps shown in table 3.5. The RF load lines from these RF waveforms are shown in figure 3.53.

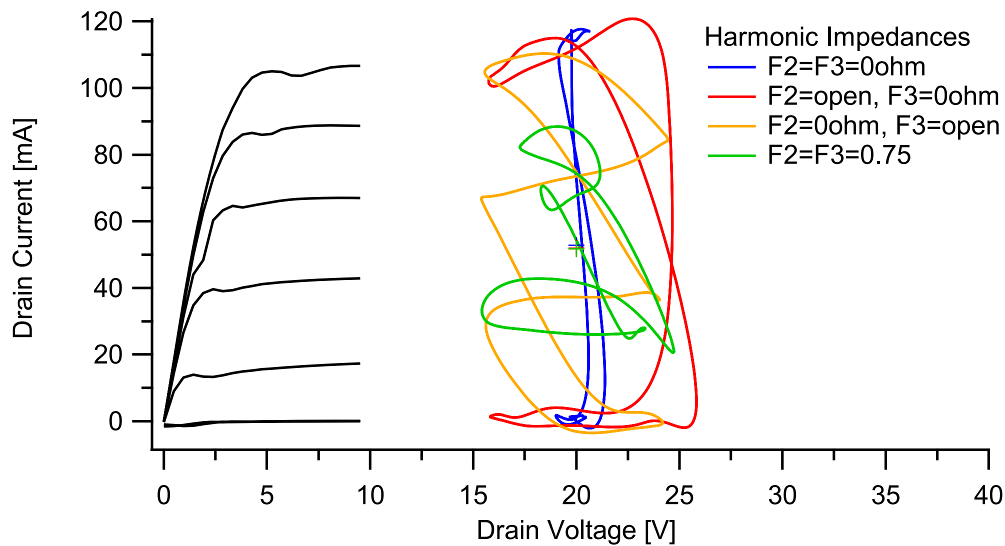


Figure 3.52 - RF load lines for the high drain current region of the infinite VSWR sweeps described in table 3.5, performed on a 2x50μm GaN HFET

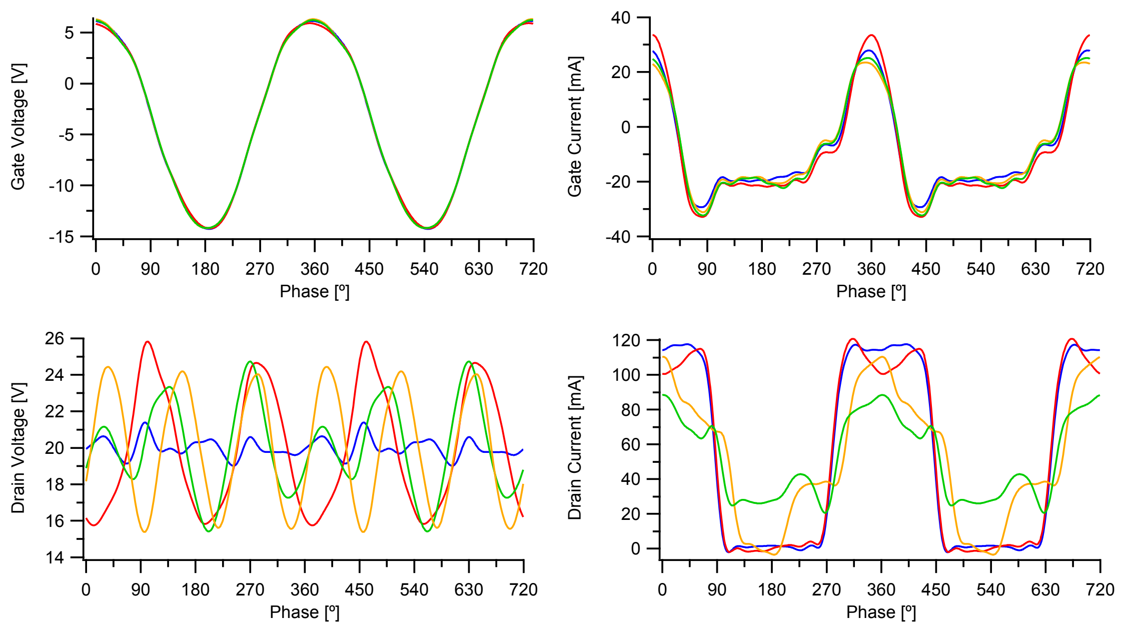


Figure 3.53 - RF waveforms for the load lines shown in figure 3.52

This time it can be seen that the combination of the reduction in the magnitude of the fundamental impedance and the different open circuit harmonic impedances causes a drain voltage waveform that has more harmonic content than fundamental. When both the second and third harmonics are set to a short circuit the drain current waveform is a square wave, with minimal ripple, indicating there are predominantly odd harmonics contained in the waveform. This explains why there is minimal change to the waveform when the second harmonic is set to an open circuit and a larger amount of change when the third harmonic is set to an open circuit. As with the other two regions of the infinite VSWR sweep changing the harmonic load impedances has little effect on the input waveforms.

3.8 Conclusions

In this chapter it has been shown how removing the protection isolator from the output of a power amplifier affects the PA. This has built on the theoretical analysis from the end of chapter 2. The worst possible situation is when all of the power produced by a device is reflected back, producing an infinite VSWR. However it has been shown that this worst case is not always representative of real world conditions. Therefore other VSWR sweeps have also been measured and compared with the results from the infinite VSWR sweep.

It was shown that for the infinite VSWR sweep the observed behaviour can be split into three regions, one of high drain current, one of high drain voltage and a transition region between the two. The location of the transition region depends on the optimum real impedance of the device. The high voltage region of the sweep is located at impedances with magnitudes that are higher than this optimum. Alternately the high current region of the sweep is located at impedances with magnitudes lower than this optimum. Additionally there are different stresses presented to the device in each region.

In the high voltage region the high impedances cause high RF drain voltage swings, potentially exceeding twice the drain supply voltage. This leads to higher than expected peak RF drain voltages and the potential for the minimum RF drain voltage to drop below the peak RF gate voltage. At these high impedances the RF gate and drain voltage waveforms are 180° out of phase, leading to the gate-drain diode becoming forward biased and an increase in the RF and DC gate current. These high drain voltage swings can be maintained across the device irrespective of the device size, drain bias voltage or input power. It was also shown that by presenting the harmonic load impedances with an open circuit the drain voltage waveform can be manipulated to increase the peak RF drain voltage or to prevent the forward biased gate-drain diode.

In the high RF drain current region the low load impedances causes the RF drain current waveforms to become saturated. This causes the DC quiescent drain current to be driven up, potentially as high as would be seen

under class A operation, irrespective of the initial drain current bias. This naturally causes high DC power dissipation and high static junction temperature. In the device size comparison it was shown that despite the current densities being higher for the smaller device, the static junction temperatures of the two devices were nearly identical. Increasing the drain bias of the device showed that there is a reduction in both the RF and DC drain currents due to heating and above V_{DS}=20V there is an additional decrease in the RF drain current due to DC-RF dispersion. However the DC dissipation, and therefore static junction temperature, will still increase with increasing drain bias. Increasing the input power drive of the device showed that the drain current will be limited by the saturation of the device, however the DC power dissipation will continue to be driven up. In this case presenting the harmonic impedances with open circuits does not lead to the same RF drain voltage waveform shapes due to the change in the phase of the fundamental component.

In the transition region there are simultaneously high RF current and voltage leading to a high instantaneous RF power dissipation. The device size comparison showed that the instantaneous RF power density is similar for both device sizes. As with the high drain current region, the increase in drain bias and input power both result in increases in the instantaneous RF power dissipation irrespective of the peak drain current. There was also a similar result for the harmonic manipulation of the RF load lines, due to the out of phase fundamental in the RF drain voltage waveform.

It was then shown that at VSWR ratios less than infinity the parameters follow the same trajectories as those produced by the infinite VSWR sweep. However their length along those trajectories is dependent on the VSWR of the sweep, as this sets the range of impedances that are covered by the sweep. It was also seen that this could cause the VSWR sweep to no longer cross the boundary between the two regions of the infinite VSWR sweep. In this case with a small device the low ratio VSWR sweeps were no longer entering the high voltage region. This means that the failure mechanisms associated with this region, and the transition region, are not seen in these VSWR sweeps.

3.9 References

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Chapter 4 – Review of Reliability Testing and GaN HFET Failure Mechanisms

4.1 Introduction

It is well established that GaN HFETs are becoming a promising prospect for the basis of RF PA, however they still have to be shown to be reliable and have adequate life times for their intended applications [1,2]. However before solutions can be found to prevent failures, it is important to understand the failure mechanisms themselves. Chapter 5 will investigating how the RF IV waveform measurement systems presented in chapter 2 can be used to increase the amount of information available during reliability testing. To support this aim, this chapter will present a review of the current understanding of the failure mechanisms and testing methods. This will begin with details about how populations of components are dealt with and how device lifetimes are often measured before expanding on the DC and RF characterisation measurements presented earlier in chapter 2. This will be followed by a review of the failure modes of GaN HFETs, as they are currently understood, along with some of the more common solutions and preventative measures taken to solve or avoid them.

4.2 Reliability Testing

In this section the methods used to perform reliability testing will be considered. At this stage it is important to point out that there will usually be two parts of any reliability measurement. Firstly there will be some form of stress inducing measurement made upon the device (usually a DC or a RF measurement) and secondly there will usually be some kind of pre and post stress characterisation measurement used to evaluate the effect this stress has on device performance.

Previously in section 2.3, the characterisation measurements that are relevant to PA design were described. In this section the description of these measurements will be extended to show how these, along with other types of measurement, can be used as the characterisation measurements in reliability testing.

4.2.1 Reliability of Populations

One of the most critical aspects of a components performance for real world applications is its expected lifetime. Figure 4.1 shows the failure rates for a population of semiconductor components (or in fact any other sort of population) plotted against time, the resulting shape of the graph is what is known as a ‘bathtub’ curve [2,3]. The increased failure rates at either end of the bathtub are due to infant mortality and end of life wear out respectively, while in between there is a region of ‘random’ failures. Infant mortality is caused by components that have defects which result in failure of the component before the expected end of life. In the case of semiconductor components, manufacturers will often perform a “burn in” on all components in order to weed out those with defects. End of life wear out refers to the natural process where components will begin to develop faults and problems at the end of their life span. The middle region of random failures is not as prevalent for semiconductors, so most studies ignore this region.

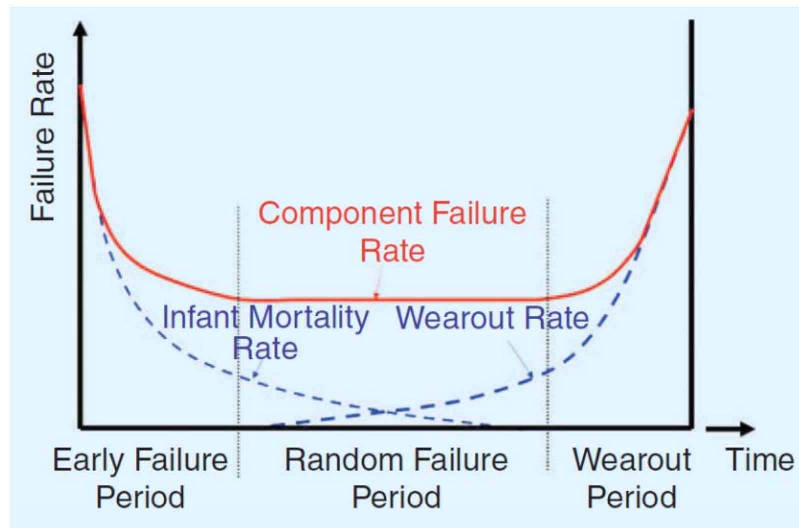

Figure 4.1 - Failure rate of a population of semiconductor components, from Trew et al. [2]

When testing the reliability of components it is important to have a representative sample size in order to avoid the impact of “rogue” component performance [2,4,5] etc. This rogue performance can be considered to be the performance of any component that is outside of the desired performance of the components being measured. For example it could be that a particular component suffers from manufacturing defects and fails early in the testing, or alternately a component could provide better than expected performance. Either way if the sample size is not large enough then the results of the testing will be skewed by such anomalous results.

4.2.2 Accelerated Life Time Test

It is important that the components that make up a system have a lifetime in excess of that expected from the overall system. Obviously for systems that are expected to have a long life span it is impractical to carry out reliability tests under ordinary conditions. This is where accelerated life time testing is used. In the case of semiconductor devices these tests speed up the failure modes of the components being tested by exposing them to high temperature operating conditions. By measuring the expected lifetimes of a the devices at multiple increased operating temperatures, and plotting the results as in figure 4.2, the lifetime of a device at the standard operating temperature can be extrapolated [2]. However the assumption with this sort

of testing is that the dominant failure mechanism under the accelerated conditions is the same failure under normal operating conditions. This has led to speculation about the accuracy of the lifetimes predicted for GaN HFETs by these tests as there is uncertainty about the failure mechanisms that are being accelerated during these tests [2,6]. For example, GaN technologies have been demonstrated with inferred lifetimes that extend to over ten million hours (over 1000 years) both at lower (C band) [7] and higher (40GHz – Q band) [8] microwave frequencies.

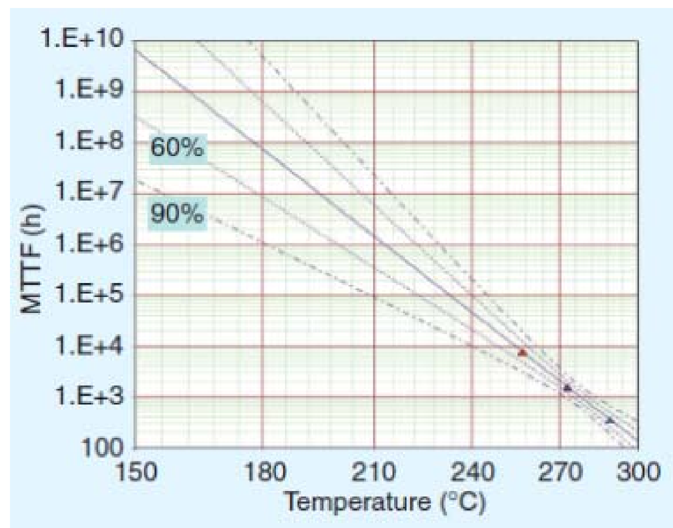

Figure 4.2 - Accelerated lifetime plot, the device technology lifetime is measured at multiple high operating temperatures from which the lifetime at standard operating temperatures can be extrapolated. Also shown are the 60% and 90% confidence bounds [2]

4.2.3 DC Testing

As previously discussed in section 2.3.1, DC characterisation measurements are generally the simplest, and hence are those most commonly employed for reliability measurements. In general the pre and post stress characterisation measurements will be those that map the IV operating areas of the device. Figure 4.3 and 4.4 show DCIV and transfer characteristic measurements made before and after a 6 hour RF stress test (before and after the first stress period of the drain voltage step-stress test in section 5.4.1). In addition to these IV measurements, a gate leakage current sweep is also often performed to assess damage to the gate edge. An

example is shown in figure 4.5 (taken from the same drain bias step-stress test), where the gate voltage is swept from 0V to -20V in 1V steps and 0V to +2V in 0.1V steps, whilst the drain and source electrodes are grounded. From these it can be seen that there is minimal degradation of the gate, however there is a shift in the pinch off voltage of about 0.5V causing a reduction in the maximum drain current.

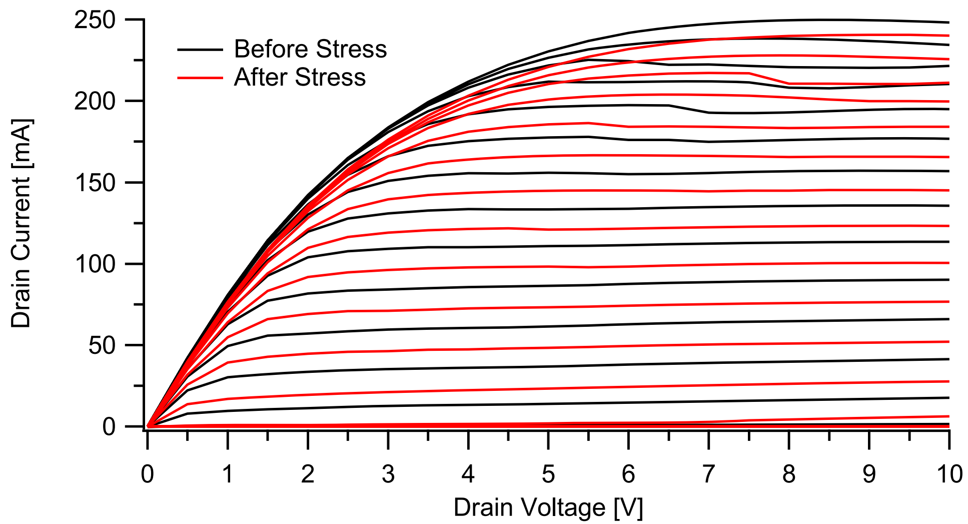

Figure 4.3 - DCIV measurements made before and after a stress test on a 2x100µm GaN HFET

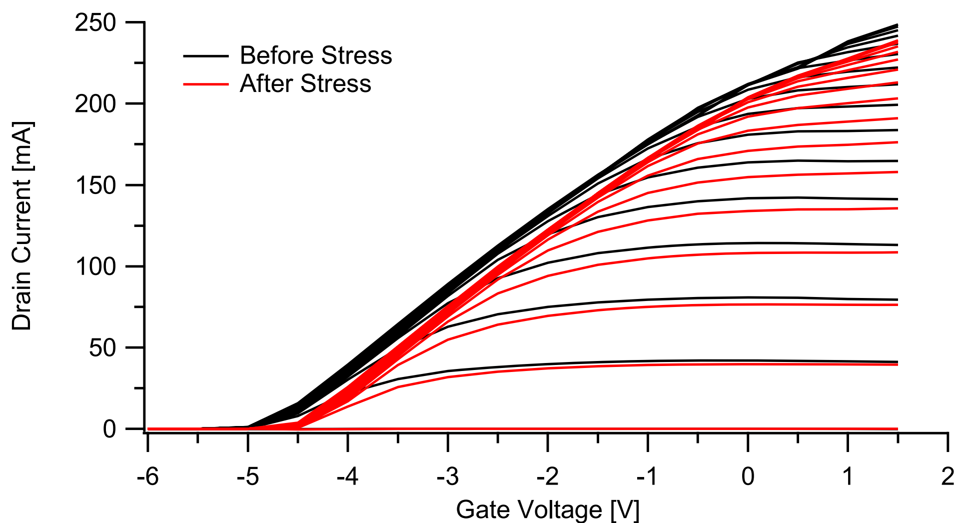

Figure 4.4 - Transfer characteristic made before and after a stress test on a 2x100µm GaN HFET

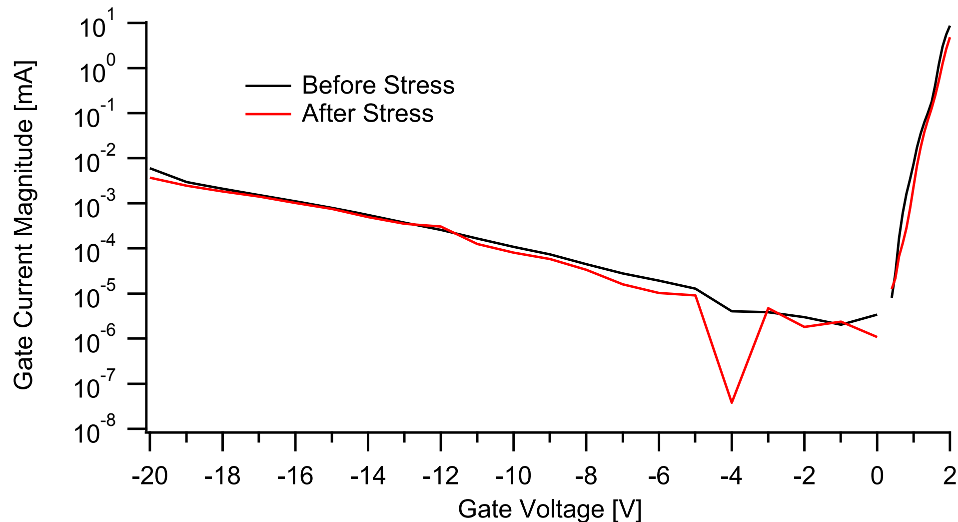

Figure 4.5 - Gate leakage current made before and after a stress test on a 2x100µm GaN HFET

There are a variety of, now quite common, DC stress tests used to investigate different effects seen in GaN HFETs. The specifics of these tests and the effects they produce will be discussed in more detail in section 4.3. Although it is worth briefly mentioning that when performing DC stress tests there are three different bias points that are often used [9], described below and shown in figure 4.6.

- The off state is where the device is completely pinched off, as in the class B mode of PA operation. In this state there is no current flowing through the channel; therefore it is used in reliability measurements to show the damage that electric fields can inflict on devices.
- The semi-on state is in between the off state and on state, with the device channel half open, as in the class A mode of PA operation. As will be explained later, this state is the optimum for hot electron generation.
- The on state is where the device channel is fully open, so the device passes the maximum possible current, I_{DSS}. The device is therefore subjected to the highest power dissipation, and junction temperature, for a specific drain voltage.

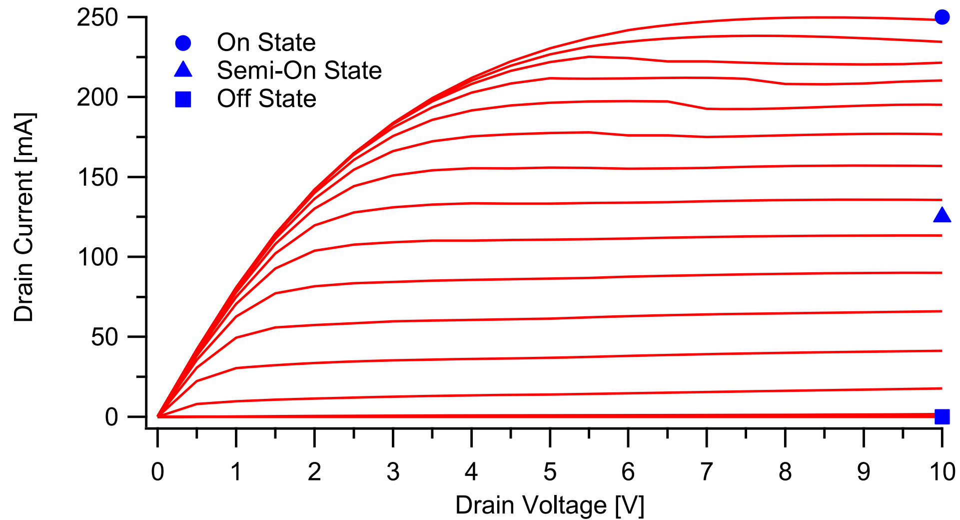

Figure 4.6 - Examples of off, on and semi-on state DC bias points, also shown is the DCIV of a 2x100μm GaN HFET for reference

A common method for reliability testing is the step stress test, where the stressing mechanism increases over multiple stressing periods. An example of which is the gate voltage stress test [9,10], where the gate voltage is held constant for the stress time period and then stepped down to a more negative value for the next stress time period. This is repeated until the device shows signs of degradation; an example can be seen in figure 4.7 where the time period is 1 minute.

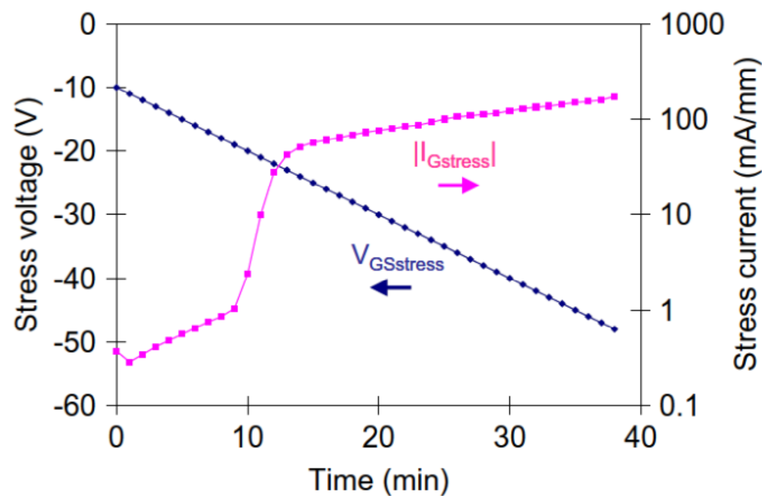

Figure 4.7 - Gate voltage step stress test, the value of gate voltage is stepped and then held for a period (in this case 1 minute) of time to ever increasing negative values, from del Alamo et al. [9]

4.2.4 Pulsed IV Measurements

As will be discussed in the next section, one of the problems that GaN HFETs experience is DC-RF dispersion. In order to quantify this effect a dynamic measurement must be used, such as pulsed IV or RF IV waveform measurements. As with DC measurement, pulsed IV measurements are often used to characterise a device before and after a stress tests in order to increase the information available on the particular failure mechanism [5,11,12].

4.2.5 RF Testing

As with DC testing, RF measurements can be used for both before and after stress characterisation measurements and also as the stressing mechanism. However, unlike with DC measurement techniques the reactive parasitic components of the device must be taken into account during RF measurements. There are two different methods for doing this. The first is to use a frequency much lower than the intended operating frequency that the GaN HFET is designed for in order to render the parasitic components negligible. In the case of Raffo et al. the frequency chosen is 2MHz, which is claimed to be high enough to avoid the devices low frequency dispersive behaviour, e.g. traps and self heating [13,14]. However if this is not the case then there could be discrepancies between the measurements made at this lower frequency and the devices behaviour at its intended operating frequency. The second method is to use the intended frequency of operation in conjunction with a de-embedding procedure, as described in section 2.3.5. As this is the technique used by our measurement equipment [15,16], it is the one that the remainder of this thesis will concentrate on.

The simplest RF stress test involves measuring the RF powers and the DC voltages and currents at the input and output of the device, from which parameters such as gain and efficiency can be calculated as shown in section 2.3.4 [11,17]. These tests also often feature DC or pulsed IV characterisation measurements before and after the stress in order to provide further information on the degradation mechanisms.

Joh et al. expanded on this by including DC and RF characterisation stages before and after the stress period as well as interrupting the stress period in order to measure DC (voltage and current) and RF (power) Figures of Merit (FOM) [18]. Their stress test procedure is shown in figure 4.8.

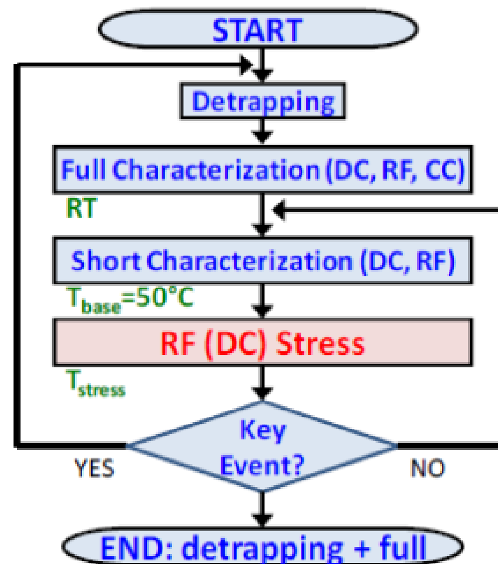

Figure 4.8 - Stress test procedure used by Joh et al. [18]

The de-trapping stage involves heating the wafer to 100°C for 30 minutes in order to remove any electrons from traps. This allows for the permanent degradation of the device to be measured. The necessity to interrupt the stressing period to measure various FOM stems from the need to increase the amount of information on the device state in order to deduce the cause of the device failures. These interruptions of the stress period can be avoided by measuring the RF IV waveforms during the stress period [19], which is the basis for the next section of this thesis.

4.3 GaN HFET Failure Mechanisms

As with any relatively new semiconductor technology, there is a lot of research going on to understanding the failure mechanisms of GaN HFETs in order to solve these problems. Although ultimately GaN HFETs are intended for RF operation, as described earlier, using DC measurement techniques to stress the device can still provide detailed information about failure mechanisms without the complexities of RF measurement techniques. This section will highlight some of the key failure mechanisms in GaN HFETs, some of which have been identified through DC measurement techniques and others through RF techniques. Of these, those associated with high electric fields have proved to be the most serious, and consequently more research has been aimed at understanding them. However with the improvements made to the devices it is now possible to identify other failure mechanisms as the cause for device degradation.

4.3.1 High Gate Reverse Bias

As described in chapter 2, GaN HFETs are able to deliver high power densities thanks to the high operating voltages and high current densities in the channel [1]. However these very properties that make GaN HFETs so attractive also cause large potential differences between the gate and the drain terminals of the device. In standard RF operation it is possible that the device will be driven hard in order to capitalise on the increase in efficiency this offers. This leads to large RF gate and drain voltage swings which are 180° out of phase with each other, producing a large potential difference between the minimum RF gate voltage and maximum RF drain voltage. Consequently this leads to large electric fields within the device, particularly concentrated at the edge of the gate contact opposite the drain electrode. Although there are also high electric fields at the source side of the gate, they are not of the same magnitude as those on the drain side due to the smaller potential difference between the gate and the source. However in certain circumstances it is possible that the degradation mechanisms

described here for the drain side of the gate can also occur on the source side [6].

These high electric fields can cause both the generation of vertical defects at the gate edge and also electron trapping on the surface of the AlGaN or in the Silicon Nitride (SiN) passivation layer, as shown in figure 4.9.

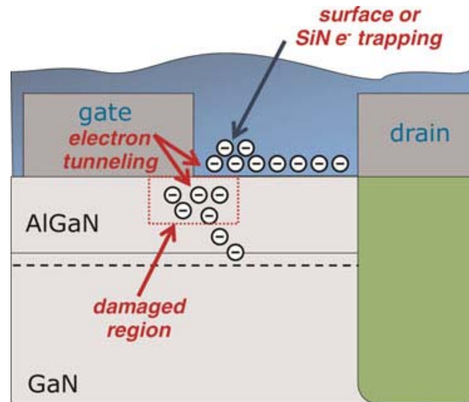

Figure 4.9 - Gate edge degradation and electron trapping on the AlGaN surface or in the SiN passivation layer resulting from high electric fields concentrated at the drain side of the gate contact, from Meneghesso et al. [12]

4.3.1.2 DC-RF Dispersion

It is surface trapping, shown in figure 4.9 that is the primary cause of DC-RF dispersion, or knee walkout, which causes a discrepancy between the RF output power predicted from the DCIV and the RF power measured from the device. An example of this is shown in figure 4.10. This dispersion is due to the tunnelling of electrons from the gate into traps on the surface of the AlGaN or in the SiN passivation layer [12]. The accumulation of charge in these traps causes the channel to become partially depleted, so effectively forming a second, 'virtual' gate which extends the depletion region of the actual gate [20].

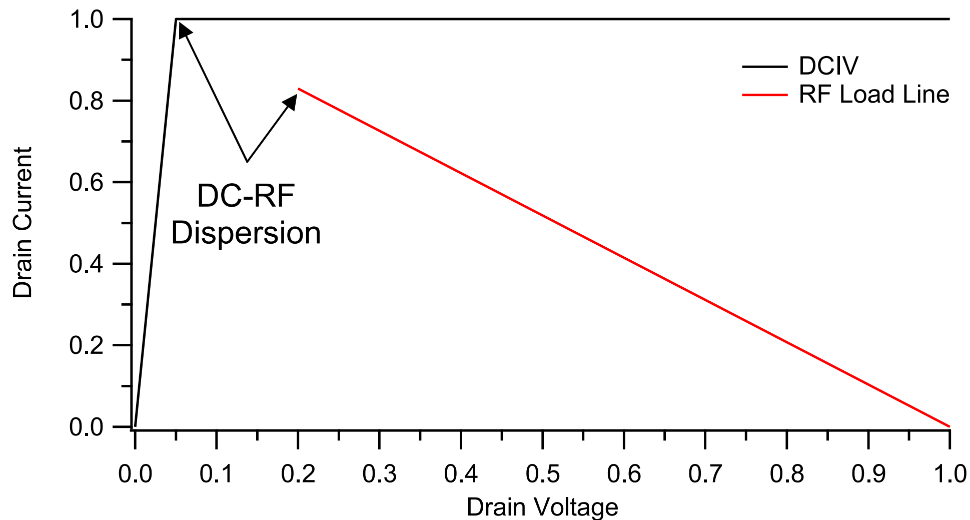

Figure 4.10 - Idealised DCIV and RF load line for a GaN HFET that is suffering from dispersive effects, the loss in output power due to DC-RF dispersion can clearly be seen.

It has been shown that devices that have suffered from electron trapping can show recovery by being left for a long period of time [12]. This can be speeded up by illuminating the device with specific wavelengths of light [12] (corresponding to the energy needed to remove the electrons from the traps) or by heating the device [18]. However this is only a temporary recovery, the next stress reduces the device to a similar level of degradation that was shown before recovery [2].

As this effect is dispersive in nature it is necessary to use a dynamic measurement, such as pulsed IV or fan diagram measurements, to compare with the DC measurement in order to quantify this phenomenon. Figure 4.11 shows the dynamic boundary conditions mapped out by four fan diagram measurements at different bias points [20]. From which it can clearly be seen that the DC-RF dispersion increases with increasing drain bias voltage. From these boundary conditions three regions have been labelled, each of which has different dispersive behaviours.

a) In this region the IV characteristics are mostly dominated by the access resistances (on resistance) which is hardly affected by the virtual gate
b) In this region the virtual gate has the most effect at the knee region causing the channel current to saturate at a lower value than in the DC case

c) In this region the RF load lines also suffer from lower saturation current, however at higher drain voltages the drain current shows recovery due to punch through effects

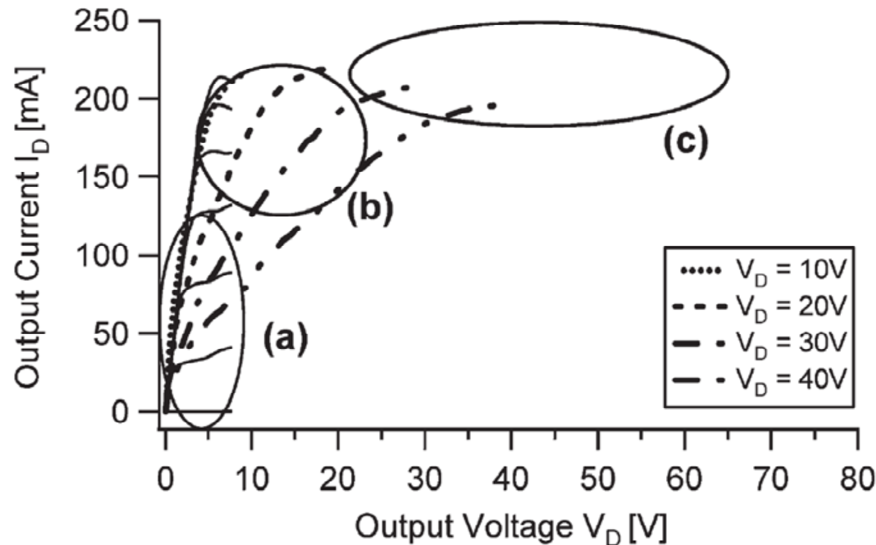

Figure 4.11 - High drain current/low drain voltage dynamic boundary conditions mapped out by using fan diagram measurements at different bias points, also shown are three regions with different dispersive behaviours, [20]

It should be noted that although this electron trapping at the gate edge is classified as a degradation mechanism, and does get worse with stress, it can also be seen in unused devices.

4.3.1.3 Gate Edge Degradation

Figure 4.9 also shows the location of the physical degradation caused by the high electric fields at the gate edge. Although there are currently two different theories on how this degradation occurs, the end result is an irreversible increase in the gate leakage current.

The first theory about this degradation was proposed by Joh et al. [10] where it was shown that there is a 'critical' gate-drain voltage above which degradation instantly occurs. It was suggested that this degradation was caused by the inverse piezoelectric effect, where the high electric field in the device causes an increase in the elastic energy in the AlGaN barrier layer above that caused by the lattice mismatch with the GaN layer below. Above

a critical value localised defects are formed in the crystal structure of the AlGaN which can become trapping sites for electrons. These trapping sites allow conduction paths to form between the device channel and the gate contact, in turn causing an increase in the gate current.

More recently it has also been shown by Marcon et al. [4] that this manner of degradation does not only occur above the 'critical' voltage, but also at lower voltages with a dependence on the stress time. It is therefore postulated that these failures are caused by an alternate time-dependant process which causes device wear out [21].

The stress test for gate edge degradation is a DC off-state step stress test where the gate voltage is stepped to, and then held at for a period of time, ever increasing negative voltages [4,10]. Depending on the gate diodes to be tested the drain and source contacts can either be held at 0V or one of them can be left floating, this is known as the V_{DS}=0V test. Obviously here if both the drain and source are grounded then both sides of the gate will be stressed with the same electric field strengths. Which, as the gate-source distance is usually less than the gate-drain distance, will result in higher electric field concentration on the source side of the gate. This test can be modified to subject the device to more realistic operating conditions if the gate is held at a fixed voltage and the drain voltage increased. It was found in these tests that the critical voltage is higher in off-state (V_{GS}=-7V and V_{DS}=10-50V) and in high-power (V_{DS}=10-50V and I_D=0.8mA/mm) tests than in the case where Vds=0. Additionally it was found that the current flowing in the channel has little effect on the critical voltage [10]. Using this test it has been found by various authors that along with an increase in the gate current there is also a decrease in the drain current and increase in the access resistances (R_S and R_D) and increase in the current collapse [10,12].

When devices stressed in this manner are investigated with Scanning Electron Microscopy (SEM) it can be seen that this degradation takes the form of pits and cracks in the structure of AlGaN along the edge of the gate contact [22], as shown in figure 4.12. Electro Luminescence (EL) spectroscopy has also been used to identify the location and extent of this degradation, where the conducting paths show up as 'hot-spots' as shown in

figure 4.13 [21,23]. From this it has been found that as the degradation worsens more of these points of damage are created, rather than the already existing ones being made worse.

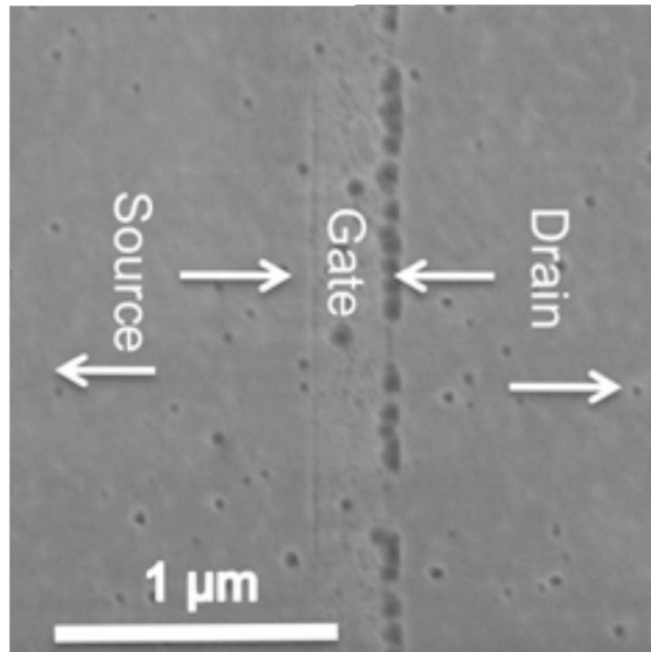

Figure 4.12 - SEM images of pits on the surface of the material under the gate contact after a reverse gate bias stress test. Both the SiN passivation and the metal contacts have been removed, from [9,22]

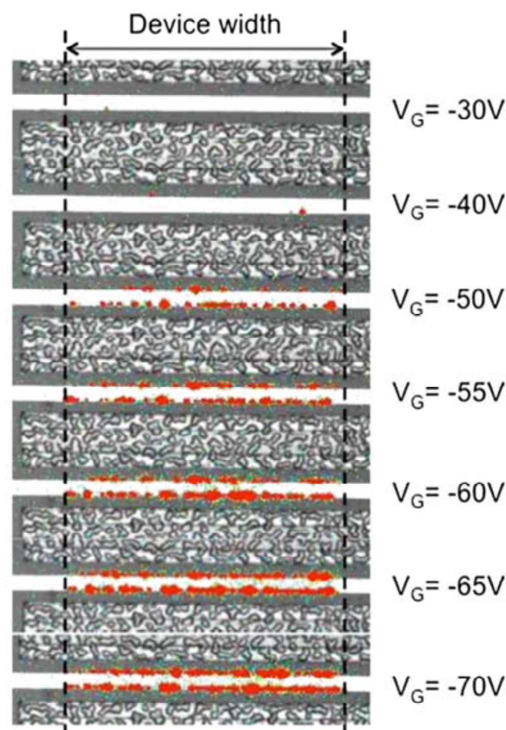

Figure 4.13 - Electro Luminescence spectroscopy measurements of devices stressed with a reverse gate bias step stress test, from [23]

4.3.1.4 Threshold Voltage Shift

In addition to these two modes of degradation, it is also possible that a shift in the threshold voltage of the device towards positive values can be caused by the build up of negative charge under the gate [24]. An example of this is shown in figure 4.4

4.3.1.5 Solutions and Preventions

There are multiple solutions for the problems associated with high electric field concentrations, some of which are described here.

In order to reduce this dispersion the surface can be passivated with a layer of either Silicon Nitride (SiN) or Silicon Dioxide (SiO_2), as shown in figure 4.14 [1,25,26]. This has been shown to increase the output power available at a specific bias point (i.e. reduce the dispersion) as well as increase the breakdown voltage of the device. The exact mechanisms through which the surface passivation improves the DC-RF dispersion are, however unknown.

Alternatively there are methods of smoothing the electric field distribution so that the peak electric field at the edge of the gate is lowered. This involves the use of T or ***Γ*** shaped gate contacts and field plates over the top of the gate, which is isolated from the device except for a connection to either the source or the gate. However, generally the field plate is source connected as then the extra capacitance caused by the field plate adds to the value of the drain-source capacitance and can be absorbed into the output matching network. Not only does this increase the breakdown voltage (and therefore maximum available bias voltage, and output power) but it also decreases the DC-RF dispersion (again increasing the output power) [1,27,28]. However the field plate can have an adverse effect on the high frequency performance of the device due to this additional capacitance.

Figure 4.14 show the structure of a GaN HFET that achieved a record RF output power density of 40W/mm [27], achieved by using a T-shaped gate, a field plate and SiN passivation in order to increase the breakdown voltage and reduce dispersion.

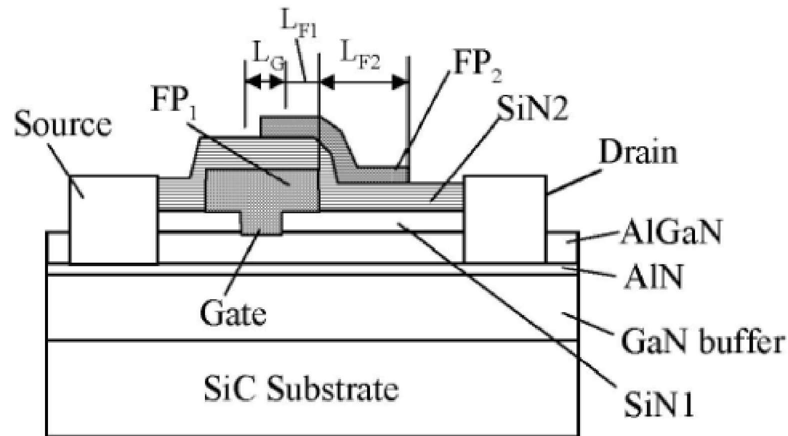

Figure 4.14 - The structure of the GaN HFET that achieved record RF output power density of 40W/mm [27], the T shaped gate, SiN passivation and field plate can clearly be seen

It has also been shown that the inclusion of an n-type doped GaN layer in between the gate contact and the AlGaN surface, a so called GaN cap, has the effect of reducing the electric field at the gate edge [29].

A slightly different approach to the problem of trapped charge on the surface of the AlGaN is to include a thick layer of either GaN or AlGaN over the top of the usual AlGaN layer. A recess is made into this layer for each of the gate, drain and source contacts, as can be seen in figure 4.15. By doing this the surface charge is moved further away from the channel, reducing the effect of the surface charge [1,30].

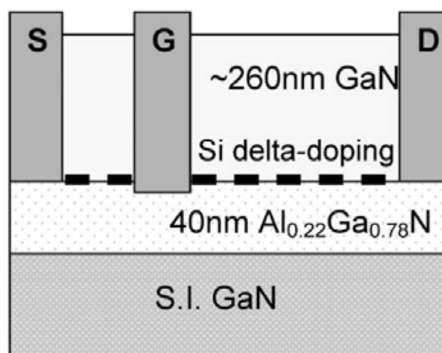

Figure 4.15 - Recessed gate GaN HFET, from [1]

4.3.2 Soft Pinch Off

As with other types of FET, GaN HFETs are vulnerable to short channel effects which cause the device to begin to pass drain current at high drain voltages. This results from the poor confinement of electrons in the channel, allowing them to 'punch-though' the GaN buffer layer due to the high electric fields. These short channel effects occur as the length of the gate contact becomes comparable to the depth of the channel, essentially the depletion region is no longer adequate to control the electron flow in the channel [31].

The effects of this soft pinch off can be seen in figure 4.16 [32], which shows a series of fan diagram measurements at increasing drain bias voltages for two different devices. For device (a) it can be seen that soft pinch off limits the minimum drain current that is achievable at higher drain voltages. One of the solutions to this is to dope the GaN buffer layer with an optimum concentration of iron during growth, the results of which can be seen in device (b) in figure 4.16. This doping improves channel confinement with no change in RF performance, including no change in the knee walkout, however does result in an increase in the PAE [31].

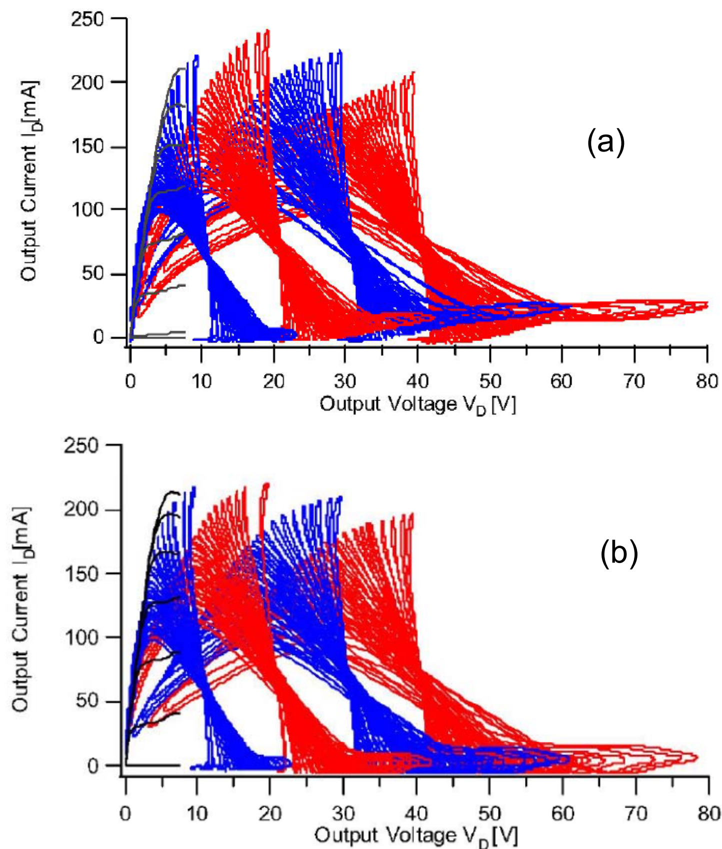

Figure 4.16 - Fan diagram measurements on two different devices, one control device (a) showing short channel effects and a second (b) where the GaN buffer layer have been doped with iron. In both cases there are similar levels of knee walkout, from Roff et al. [32]

4.3.3 Forward Biased Gate

In contrast to the high electric fields that RF operation can cause, it is also possible for the gate diodes to become forward biased and therefore pass gate current. This was investigated using a V_{DS}=0V gate step stress experiment similar to the one described in section 4.3.1.2 but stepping the gate to positive voltages [33]. The results of this test found that forward gate current will cause degradation of the Schottky junction of the device, increasing the off state gate current.

It has also been shown that forward gate current can be one of the chief degradation mechanisms under RF operation [17]. This was achieved by comparing the performance of HFET and Metal Oxide Semiconductor HFETs (MOSHFET) devices. The MOSHFET structure is similar to that of a

standard GaN HFET, with the exception that its gate contact is isolated from the AlGaN by a thin dielectric film (SiO_2), as shown in figure 4.17 [1,30,34]. This significantly reduces the gate leakage current, allowing for much higher positive and negative gate voltage swings [34]. The higher positive gate voltages allow for increased maximum drain current and therefore increased output power. The MOSHFET devices also achieved superior output power stability over time compared to HFET devices, which was attributed to the decreased gate current.

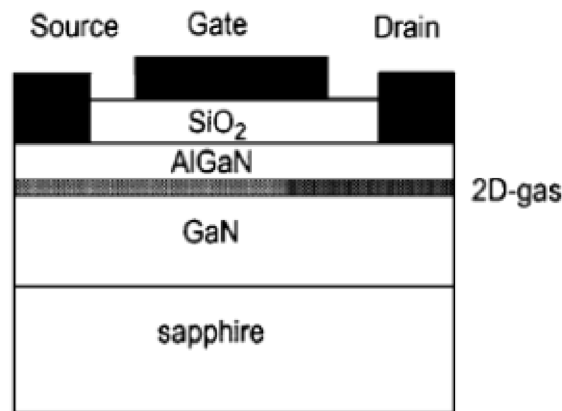

Figure 4.17 - Structure of a MOSHFET from [1], it is structurally identical to a HFET except for the Silicon Dioxide (SiO_2) layer between the surface of the AlGaN and the gate contact

Low Noise Amplifiers (LNA) are another promising application for GaN HFETs, where they have been shown to be able to handle far higher input powers then GaAs based LNA [35]. It was shown that the main cause for the degradation of the LNA was the forward DC gate current caused by high RF input power. It was also shown that by including a resistance in the gate bias network it is possible to reduce the gate current when the device is overdriven. This has the effect of lowering the gate bias voltage but also making the negative swing of the RF gate voltage waveform larger, potentially exposing the device to higher electric fields and associated effects.

4.3.4 Hot Electron Degradation

Hot electron degradation is a well explained phenomena in GaAs based transistors [5], which also occurs in many other device technologies. With the improvements made to GaN HFETs to enable higher critical voltages (and therefore operating voltages) and shorter gate lengths, hot electron degradation is becoming more of an issue. However, unlike in GaAs HEMTs the gate current in a GaN HFET is unrelated to the presence of hot electrons. However it has been shown that the intensity of the EL signal given off by a device is strongly related to the presence of hot electrons in GaN HFETs [23]. Using EL spectroscopy it has been found that hot electron generation during DC operation is maximised in the semi-on state (around class A bias point) and increases with increasing drain bias, as shown in figure 4.18. This is because this state provides a balance between electrons flowing in the channel and the electric field strength.

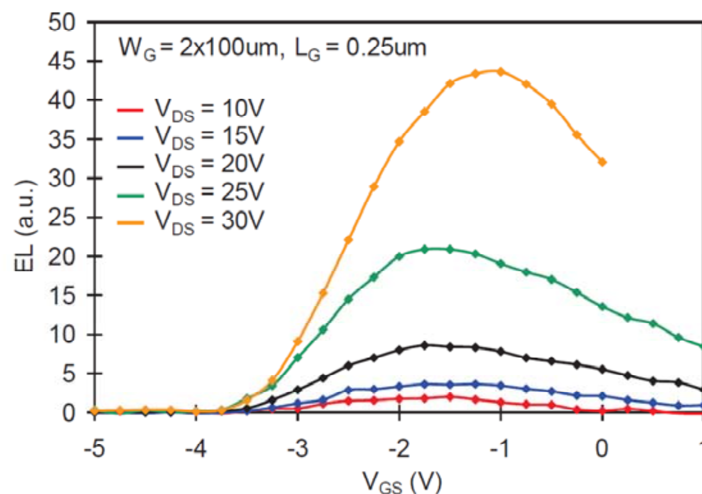

Figure 4.18 - EL intensity as a function of gate bias, at different drain biases (before any stress) on the tested GaN HFETs in [23]

It has been found by the authors of the paper and others that a device stressed by hot electrons suffers a reduction in the drain current, particularly at the knee of the device. This has been attributed to a drop in the transconductance, with no change in the pinch off voltage, caused by the trapping of hot electrons in the gate-drain region due to the high electric fields [5,23,36].

As described earlier, Joh et al. developed an RF stress test procedure to investigate the failure mechanisms of GaN HFETs under RF operating conditions [18]. The procedure was used to perform an RF input power stress test at a fixed bias and load impedance. The results of this showed that RF causes an increase in the source resistance (R_S), which in turn causes a decrease in the transconductance, output power, DC I_{Dmax} and linear RF gain. In addition there was no increase in the gate current, showing that there was no damage to the gate edge. The tests also showed that there was a good correlation between the DC and RF FOM, in particular the RF output power with DC I_{Dmax} and the transconductance with linear RF gain.

Additional Vds=0V DC step stress tests showed only a small change in the source and drain resistances for Vgs= -30V and no change for Vgs=+3V, which suggests that neither of these failure mechanisms are responsible for the degradation seen under RF operation. In a series of tests it was shown that the damage is caused in the semi-on state (high current and high voltage), and was postulated to be due to hot-carriers [18].

4.4 Conclusions

This chapter has presented some of the methods of performing reliability testing and the results of that testing. The majority of this testing has been performed using DC measurement and stressing techniques, although often pulsed IV measurements are made in order to assess potential implications of the degradation on RF performance. There is however an increase in the number of reliability studies that are being performed using RF measurement techniques, however many of these only involve RF power measurements. This will be built on in the next chapter, where the suitability of the RF IV waveform measurement system for performing reliability studies will be investigated.

The second half of this chapter described the current understanding of the failure mechanisms in GaN HFETs, which are summarised in table 4.1. Of these failure mechanisms, those associated with high electric fields have been the ones that are the most severe threat to device performance and reliability. However with the improvements that have been made in recent years this aspect of device performance has improved to the point where other failure mechanisms are now coming to the forefront.

Table 4.1 - Summary of the failure mechanisms in GaN HFETs

Failure Mechanism	Physical Manifestation	Degradation
Gate edge degradation	Pitting at the gate edge, EL from these locations	Decrease in drain current and increase in gate current
DC-RF dispersion	Reversible electron trapping on AlGaN surface and in SiN passivation leading to a second, virtual gate on the drain edge of the gate contact	DC-RF dispersion, a decrease in drain and gate current
Short channel effects	Electrons flowing through the GaN under the depletion region	Un-pinching of the channel at high drain voltage
Hot electron degradation	Irreversible trapping/trap generation in the AlGaN	Drop in transconductance
Change in Schottky barrier height	Physical damage to the gate/metal interface	Decrease in magnitude of pinch off voltage and consequent drop in max drain current

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Chapter 5 – RF IV Waveform Stress Test

5.1 Introduction

It was established in the previous chapter that the majority of reliability testing is performed using DC measurements. While this has many advantages (cost and simplicity chief amongst them) these tests struggle to show how the device performance will degrade under RF operating conditions. Therefore RF stress testing is becoming more of interest to the reliability community. The simplest test is to measure the RF power at the input and output of the device. This limits their usefulness as far as understanding the failure mechanisms that cause degradation. However some of these tests also use DC characterisation measurements in order to understand the effect of device degradation on the voltages and currents at the device terminals.

RF IV waveform measurement and engineering systems have been used to design PA modes that offer high efficiency and high bandwidth operation, importantly with a first pass design methodology [1,2,3]. This success can be attributed to the fact that the measured IV waveforms show the exact operating state of the device. As described in the previous chapter, these systems have been used to perform RF stress testing by other authors [4,5,6]. This chapter presents further developments on how these systems can be used to perform RF stress testing and how the increased data available on the state of the device can lead to identification of the failure mechanisms at work. Initially two sets of simple RF stress tests were performed where only one stress period was used. First three devices were stressed at the optimum impedance and then one device was stressed in each of the regions of the infinite VSWR sweep. The RF stress tests will then be extended into step-stress tests featuring multiple stress periods, with a variety of stressing mechanisms including drain bias and input power.

It is important to note at this point that while the devices used in this thesis are not the immediate state of the art, and due to the number of devices and amount of time available, the intention here is not to categorically define to operational states of GaN HFETs in general. It is more to show the measurement techniques that can be used to find such constraints and how RF IV waveform measurements can be used to support reliability testing.

5.2 RF Stress Test Procedure

In order to standardise the stress testing being undertaken a procedure was used as shown in figure 5.1 [7,8], which is an adaptation of the one used by Joh et al. [9]. This procedure and the characterisation measurements described below are used for all of the stress tests in this chapter. All of the RF measurements (both the RF reference characterisation stage and during the stress period) are performed using the RF IV waveform measurement system and the Envelope Load Pull (ELP) system described in section 2.3.5. The fundamental frequency was set to be 0.9GHz for all of the measurements in this chapter.

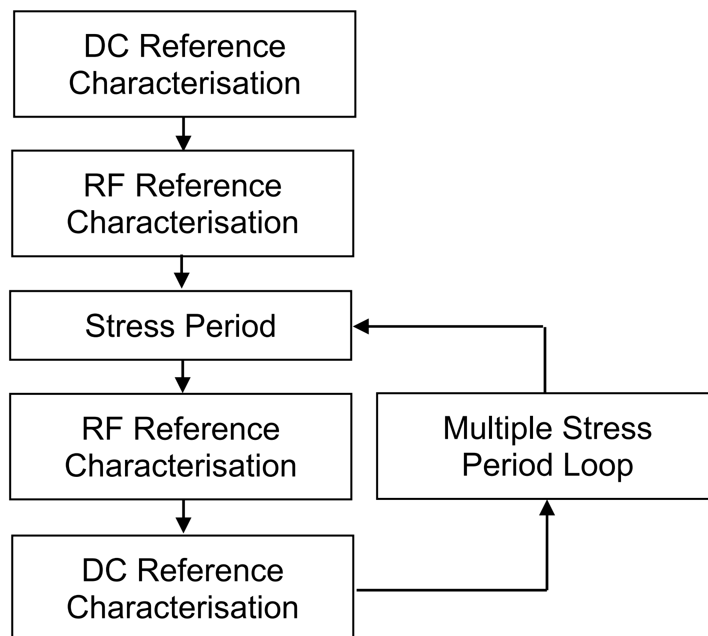

Figure 5.1 - Procedure for the stress tests in this chapter [7,8]

The DC reference characterisation stage consists of a DCIV measurement and a gate leakage current measurement, the details for which are shown in table 5.2. The knee of the DCIV was defined as being the drain current at V_{GS}=1.5V and V_{DS}=4V as shown in figure 5.2, which was used to compare to the RF measurements. The RF reference characterisation stage consists of a single RF load line that is directed at the DCIV knee, as shown in figure 5.2. In this case, as with fan diagrams (described in section 2.3.6), the fundamental, second and third harmonics are set to the same impedance in order to minimise the looping of the load line. The initial RF output power

measured during the first RF reference characterisation stage, before any stress testing was undertaken, was approximately 25dBm. During the stress period the device will be held at constant bias, input power and engineered load impedance and the RF IV waveforms will be measured every 30 minutes.

Table 5.2 - Reference characterisation measurements made during the stress test procedure shown in figure 5.1

Characterisation Stage	Measurement	Details
DC Reference Characterisation	DCIV	V_{GS}=-6V to 1.5V in 0.5V steps V_{DS}=0V to 10V in 0.5V steps
	Gate Leakage Current	V_{GS}=0V to -20V in 1V steps and V_{GS}=0V to 2V in 0.1V steps, both at V_{DS}=0V
RF Reference Characterisation	RF load line	V_{GS}=-2.5V and V_{DS}=10V Z_{Load}=50Ω (fundamental, 2nd and 3rd harmonics)

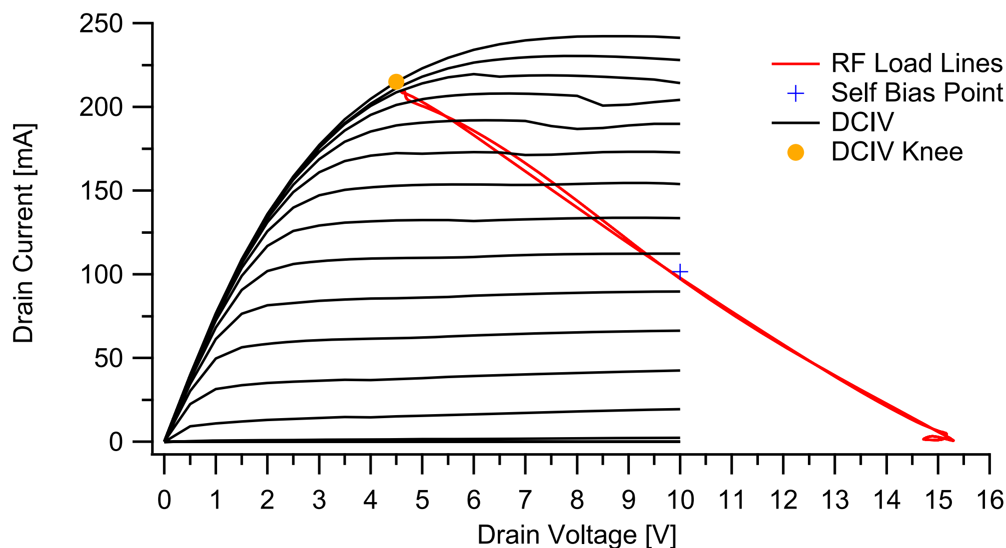

Figure 5.2 - RF reference characterisation measurement, a single RF load line directed at the knee of the DCIV, on a 2x100µm GaN HFET

This stress test procedure can easily be extended to cover multiple stressing periods by repeating the stress period and the post stress DC and RF reference characterisation stages. Thus making it possible to perform RF step-stress testing, the results of which are shown in later in this chapter

The procedure was tested to ensure the reference characterisation stages were of a benign nature by repeatedly performing them. The reference characterisation measurements were made 30 times over the course of 2 hours and 25 minutes. Figure 5.3 shows the RF output power of the RF reference characterisation measurements, from which it can be seen that there is a drop of approximately 1%. Figure 5.4 shows the DCIVs and the RF load lines from the initial and final RF reference characterisation measurements, and figure 5.5 shows the initial and final DC reference gate leakage current measurements.

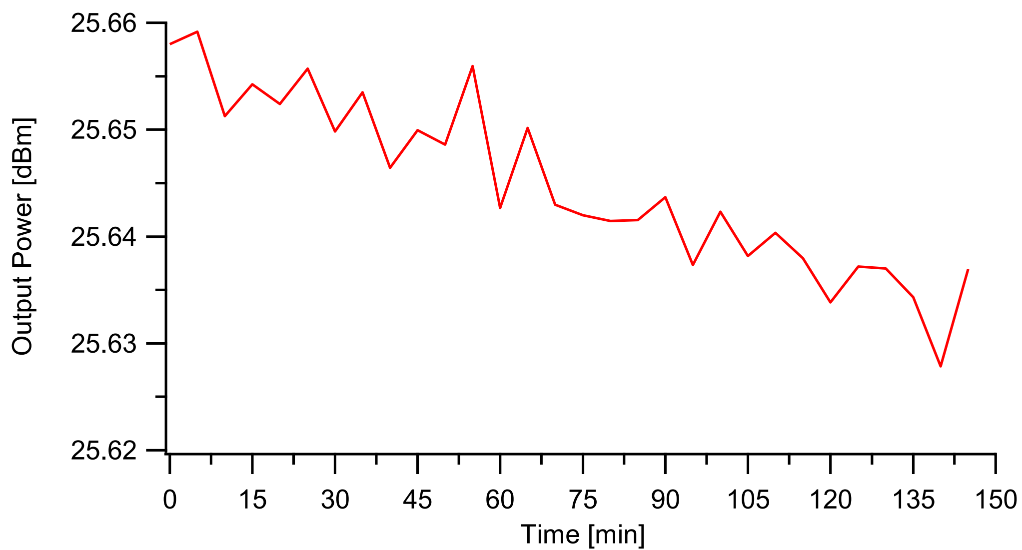

Figure 5.3 - Normalised RF output power of the reference characterisation test

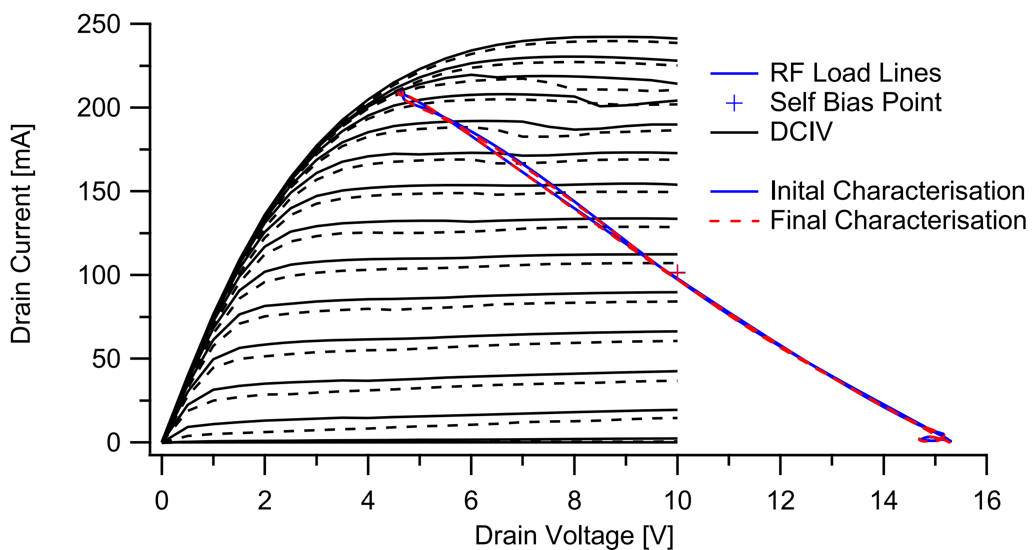

Figure 5.4 - RF load lines of the initial and final RF reference characterisation stages together with the DCIVs of the initial and final DC reference characterisation stages

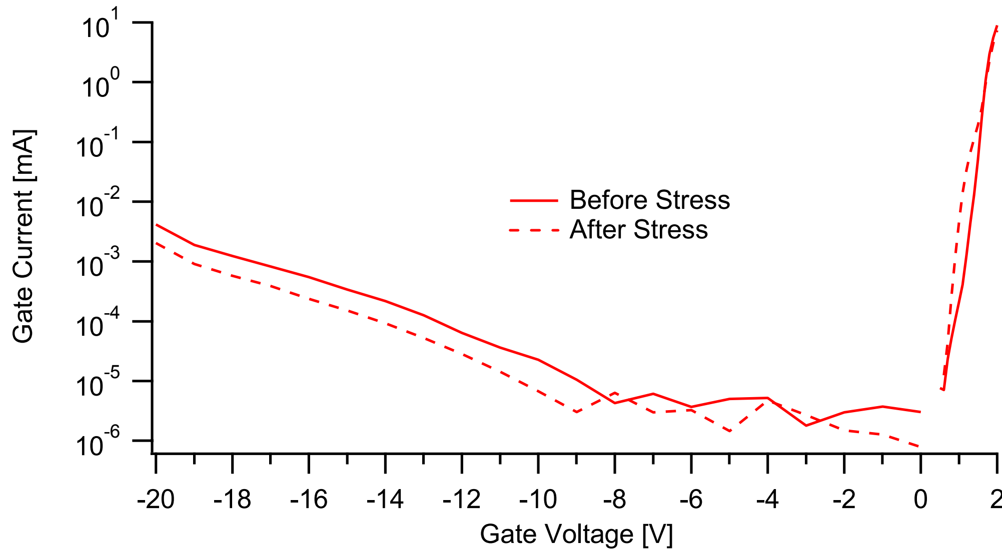

Figure 5.5 - DC reference gate leakage current measurements made before and after the reference characterisation test

In order to compare the different measurements made during the stress test a normalisation procedure is required. Equation 5.1 shows how the parameters in this chapter are normalised, where X is the original parameter, X(0) is the initial parameter before any stress and X_{norm} is the normalised parameter.

$$X_{norm} = \frac{X}{X(0)} \quad (5.1)$$

Normalising the data in this way will result in the measurements made before stress being equal to 1, this includes the measurements from the reference characterisation stages and the initial measurement made during the stress period.

All of the devices used in this chapter are nominally identical 2x100µm GaN HFETs from the same wafer, which are described in section 2.2.1. The results are de-embedded for a drain-source capacitance of 0.08pF (0.4pF/mm).

5.3 Simple RF Stress Tests

In this section two different RF stress tests are shown, the first test consists of three devices being stressed at their optimum impedance and the second test of three additional devices being stressed with an infinite VSWR [7]. For these simple stress tests the procedure used involves one 15 hour stressing period, where the devices were biased at a gate voltage of -3.5V (class AB mode of operation) which results in an initial drain current of 70mA at a drain bias of 30V.

5.3.1 At the optimum impedance

For the first set of stress tests three nominally identical devices were stressed at the optimum impedance, with the second and third harmonic impedances set to short circuits. This set of simple RF stress tests will serve multiple purposes, firstly it can be used to show how the characterisation measurements relate to those made during the stressing period and secondly it will provide a baseline to compare future RF stress testing with.

The RF output power from the measurements made during the stress period of each of the stress tests are shown in figure 5.6, also shown are the RF output powers of the RF reference characterisation measurements made before and after the stress period. For all three devices the RF output power of the initial measurement during the stress period was 30dBm. From figure 5.6 it is clear to see that of the three devices subjected to stress the performance of two has degraded (devices A and B), while the third has shown minimal degradation (device C). The reason for this variation in susceptibility is unknown; however this does reinforce the importance for a statistically significant sample size during reliability testing. Figure 5.6 also appears to suggest that the RF output power of the RF characterisation stage provides a good indicator of the level of degradation suffered by the device during the stress period.

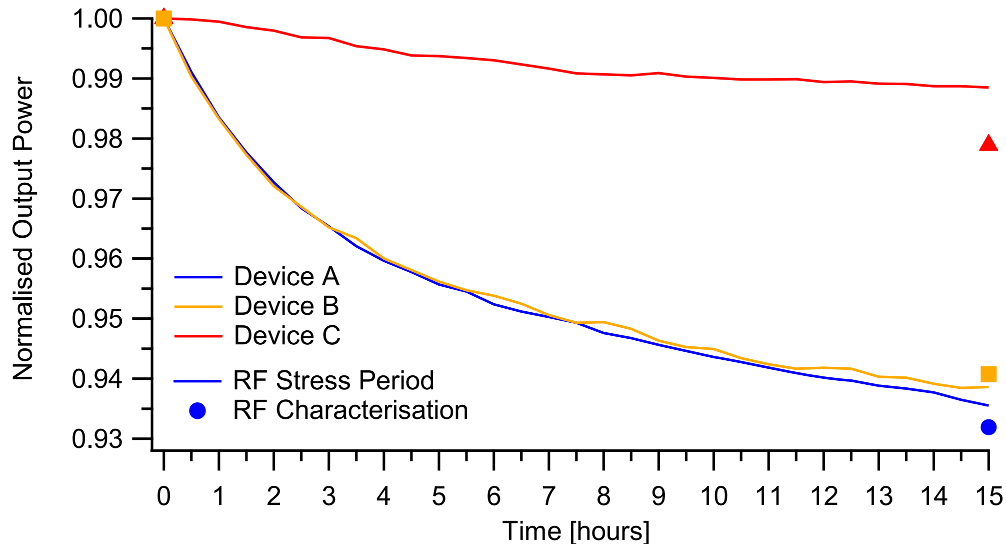

Figure 5.6 - Normalised output power measurements from during the RF stress period and from the RF reference characterisation stages, for three 2x100µm GaN HFETs

As previously described, because the RF IV waveforms have been measured during the stress period it is possible to compare the state of the device during this period with the reference measurements in the characterisation stages. Figure 5.7 shows the RF load lines observed in the RF characterisation stages before (solid lines) and after (dashed lines) the stress period. Figure 5.8 shows the initial (solid lines) and final (dashed lines) RF load lines measured during the RF stress period. Also shown in both are the DCIV measurements from the DC characterisation stage. The corresponding RF IV waveforms for these load lines are shown in figure 5.9.

The RF drain IV waveform measurements performed during the stress period can be compared to those measured from the reference characterisation stages. Firstly in figure 5.10 the maximum RF drain current from during the RF stress period is compared with the same from the RF characterisation stages and the knee current of the DCIV (I_{Dknee}, as defined in figure 5.2). Secondly, in figure 5.11 the measurements of RF drain voltage swing measured during the RF stress period and from the RF characterisation stages are compared.

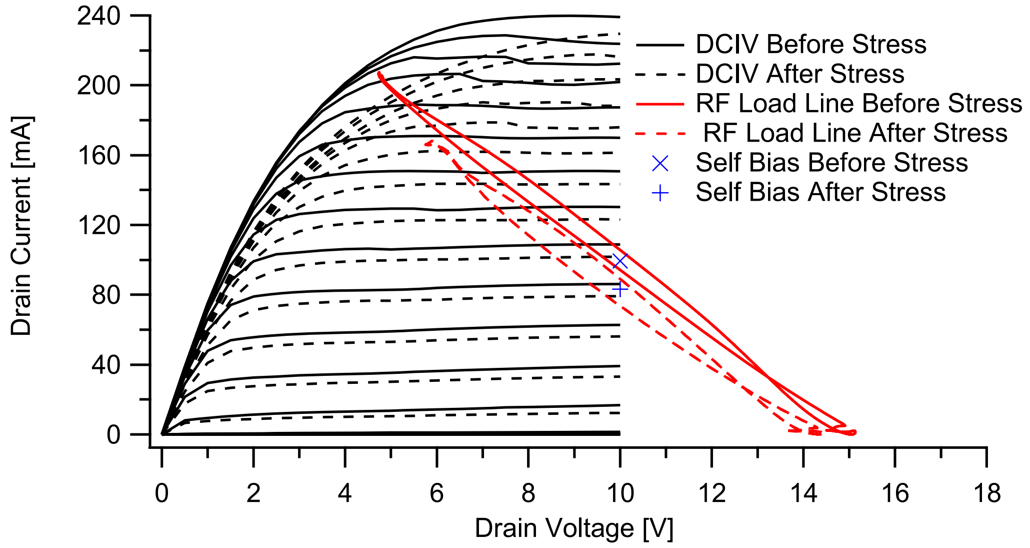

Figure 5.7 - RF load lines from the RF reference characterisation stages and DCIV measured before and after the stress period on device A

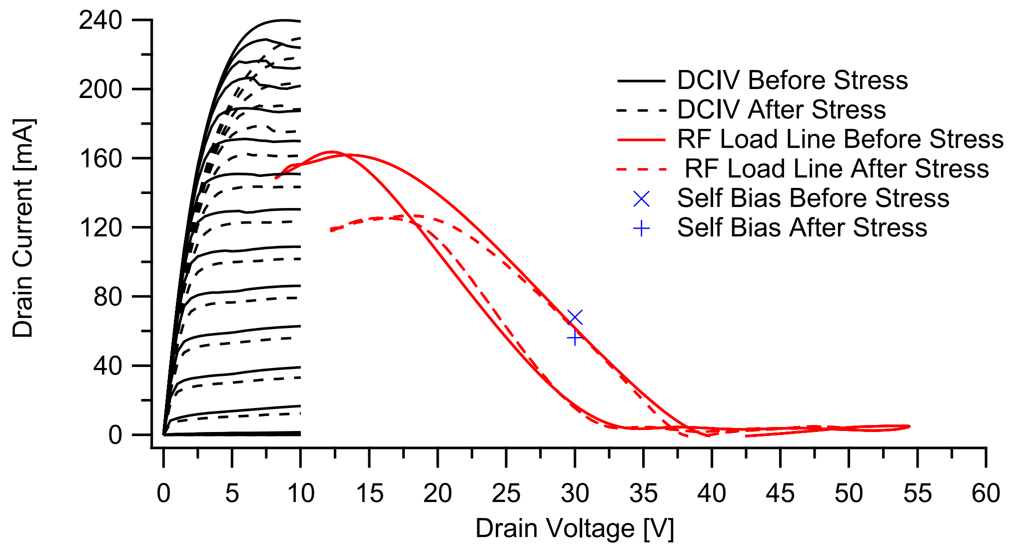

Figure 5.8 - Initial and final RF measurements during the RF stress period and DCIV measurements made before and after the stress period, from device A

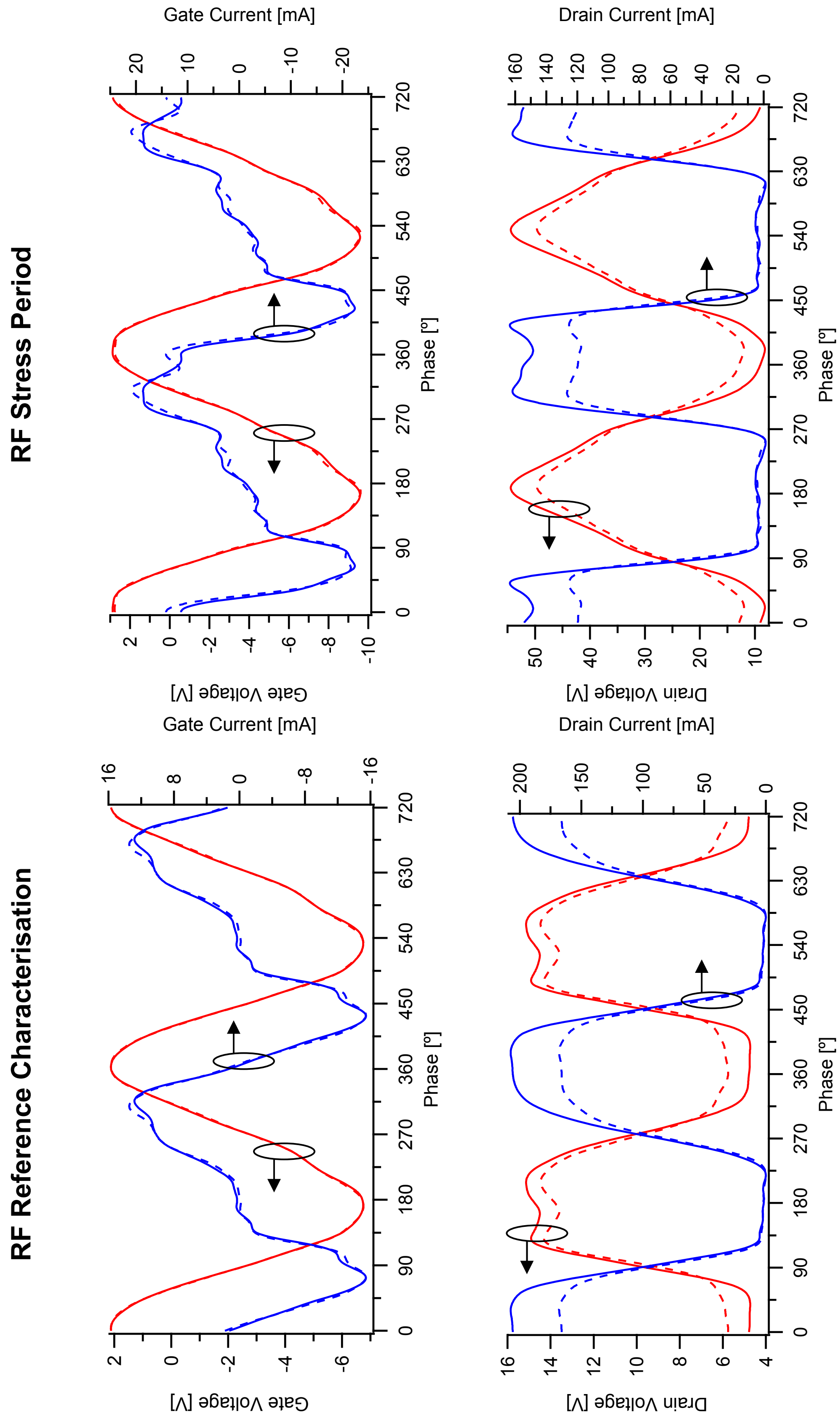

Figure 5.9 - The RF IV waveforms from the initial (solid lines) and final (dashed lines) measurements during the RF stress period and the before and after RF characterisation stage on device A

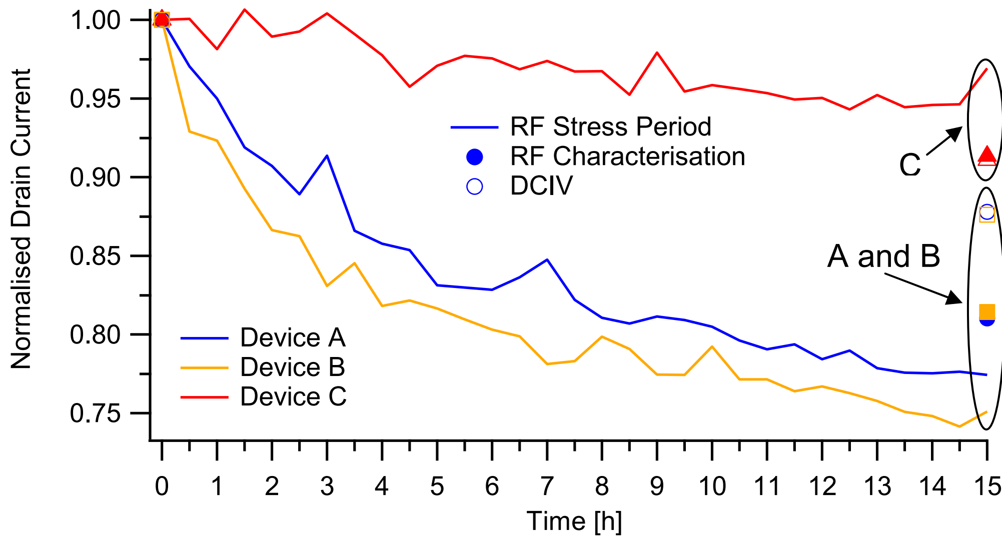

Figure 5.10 - Comparison of the normalised drain current measurements from during the RF stress period (solid traces), the RF reference characterisation stages (solid markers) and the knee of the DCIV (hollow markers)

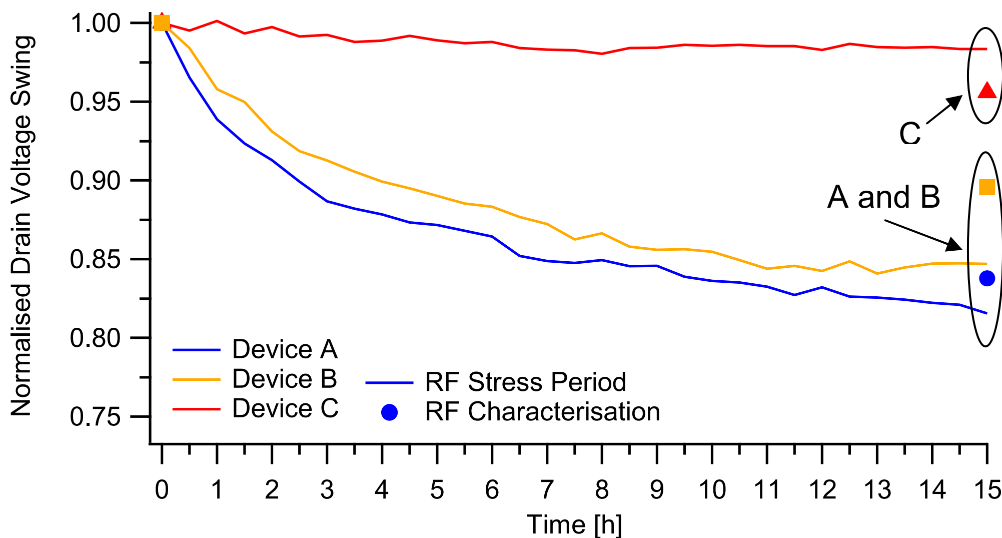

Figure 5.11 - Comparison of the normalised drain voltage swing measurements from during the RF stress period (solid traces) and the RF reference characterisation stages (solid markers)

Firstly, this shows that when a device has suffered minimal degradation (device C) the drain current measurements made in the reference characterisation stages make for a good prediction of each other. However these reference measurements do not share as good an agreement with the measurements from during the stress period. After the device has suffered degradation (A and B) the reference characterisation measurements no longer show the same agreement, however the trend observed by the RF

reference characterisation stage still shows a reasonable similarity with that observed from the measurements made in the RF stress period.

Secondly, figure 5.10 also shows that the degradation that has occurred has a much larger influence on both the RF stress period measurements and the RF reference measurements than on the DC reference measurements. In addition it can be seen that the influence of this degradation on the RF measurements is increased by the drain bias, hence the measurements made during the RF stress period show higher degradation than those made during the RF reference characterisation stage. From the RF load lines and waveforms it can immediately be seen that the majority of this degradation appears in the knee region (high drain current and low drain voltage) of the devices IV plane [8]. The RF drain current waveforms can be seen to still be squaring up after degradation (figure 5.9), implying that the RF waveform is still saturating, consistent with a current limiting virtual gate mechanism as described in section 4.3.3.1 and [10]. This dispersion causes a reduction in the fundamental component of the RF drain current, which in turn causes the symmetrical reduction of both the maximum and minimum RF drain voltage. This is an example of the unique additional insight provided by incorporating RF IV waveform measurements in to a stress test.

It is also interesting to note that there are subtle changes in the gate current waveforms, particularly in the region where the device is pinched off and at the peak of the waveform. In addition for the gate current waveforms observed during the stress period there is an increase in the current where the gate diodes turn on.

In order to identify the cause of this degradation the measurements from the DC reference characterisation stages can be analysed. Figure 5.12 shows the gate leakage current sweeps, from which it can be seen that there is a step increase in the gate leakage current of all three devices. This is due to the drain bias voltage being around the critical voltage that triggers gate edge degradation (see section 4.3.3.2), and this increase of gate leakage current is of a similar magnitude to that found by Joh et al. [11]. In addition, from the transfer characteristics (device A shown in figure 5.13) it is possible to see that for all three devices there is a small shift in the pinch off

voltage, suggesting a build up of negative charge under the gate. As all three of the devices tested show similar levels of degradation in these measurements, this suggests that these failure modes are unrelated to the increase in the DC-RF dispersion suffered by devices A and B.

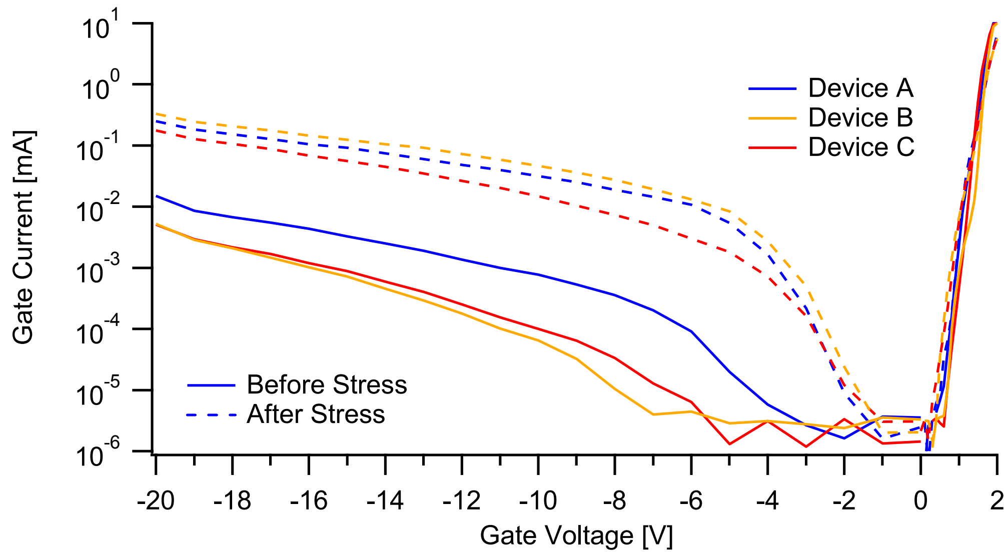

Figure 5.12 - Gate leakage current sweeps from the DC reference characterisation stages of all three devices

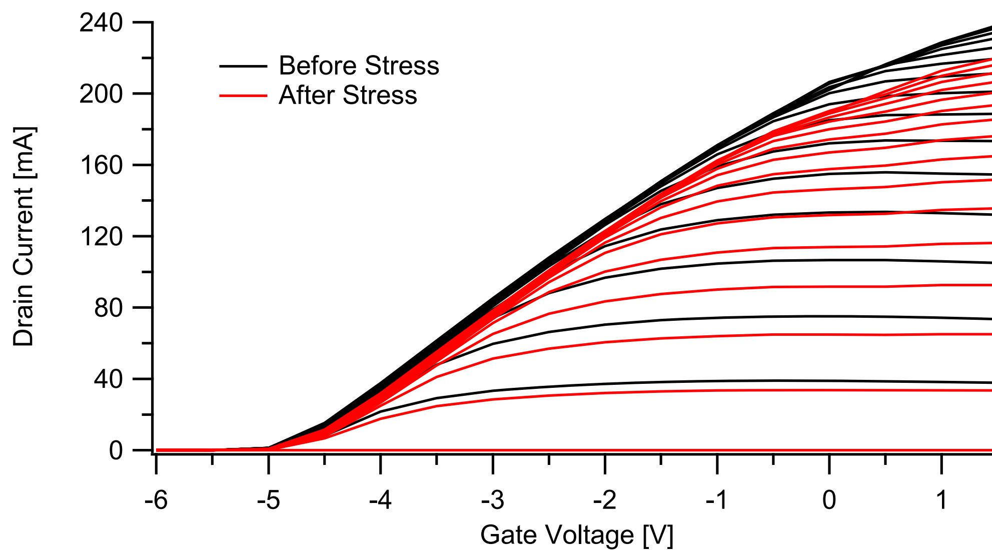

Figure 5.13 - DC transfer characteristics from the DC reference characterisation stages of device A

5.3.2 Infinite VSWR Failure Mechanisms

In chapter 3 it was shown that an infinite VSWR sweep could be divided into three different regions whose location within the sweep depends on the optimum impedance of the device, as shown in figure 5.14. Shown in table 5.1 are the failure mechanisms that are presented to the device in each of these regions. A second set of simple RF stress tests was performed in order to assess the potential for each of the failure modes associated with these regions to cause damage to a device. In this set of RF stress tests one device was stressed at an engineered load impedance from each of the regions, table 5.2 shows the load impedances used for each of the RF stress tests. Again the RF stress test procedure outlined in section 5.2 was used to perform the tests, with both the DC and RF characterisation stages performed (before and after the stress testing) as described in section 5.2. In addition, during each RF stress period the second and third harmonic impedances are set to short circuits in order to minimise the harmonic voltage components.

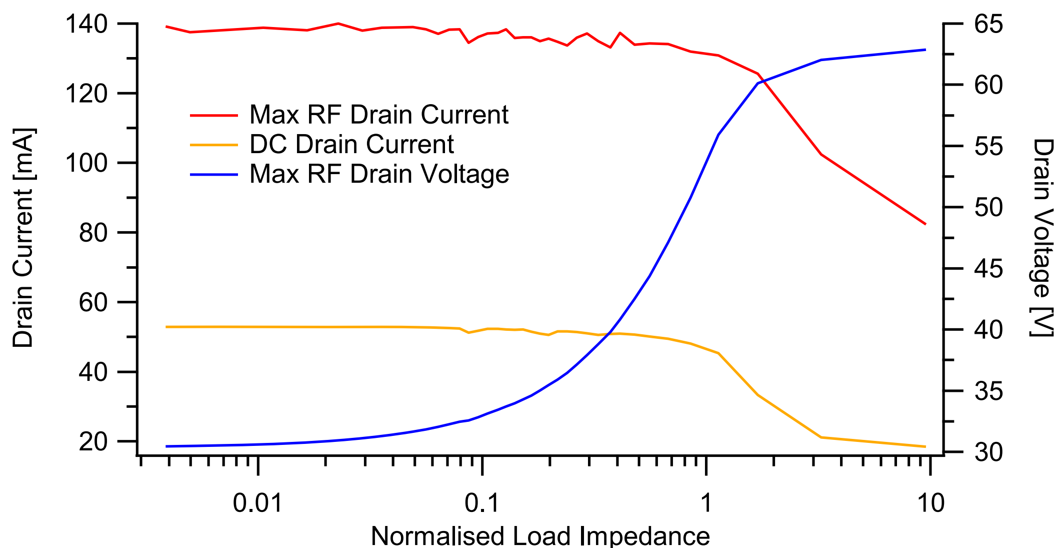

Figure 5.14 - Maximum RF and DC drain current and maximum RF drain voltage for the infinite VSWR sweep shown in figure 3.10

Table 5.1 - Regions of an Infinite VSWR sweep

VSWR Sweep Region	Regime	Damage Mode	Section in Chapter 4
High Voltage Region	High peak RF drain voltage	Soft/hard gate breakdown	4.3.1
	Forward biased gate-drain diode	Forward Gate Current – self-heating (thermal failure/trap generation)	4.3.3
Boundary	High RF drain current/voltage	Self heating (thermal failure)	4.3.5
High Current Region	Class A bias point	Hot electron damage (trap generation)	4.3.4

Table 5.2 - Fundamental load impedances used to stress the devices with infinite VSWR

Region of the Infinite VSWR Sweep	Normalised Load Impedance	Fundamental Load Impedance
High RF drain voltage region	>1	∞Ω (open circuit)
Transition region	=1	0+jZoptΩ
High RF drain current region	<1	0+j50Ω

In these RF stress tests there should be no RF output power generated during the RF stress periods due to the purely reactive load impedance required to present the device with an infinite VSWR (as discussed in section 2.5). This means that the measure of RF output power during the stress period cannot be used to compare degradation levels between devices. However, as established in the previous section, the RF output power of the RF reference characterisation stages gives a good indication of changes occurring during the RF stress period. The RF output powers of the RF reference characterisation stages are shown in figure 5.15, along with the same from the section 5.3.2 where the devices were stressed at the optimum impedance. These measurements indicate that the degradation suffered by the devices is of a similar level to that seen on the device that did not degrade from the previous section (device C). This is a surprising result as it would be expected that the stress presented by at least one of the regions of the infinite VSWR sweep ought to be more severe than the stress that caused the devices to degrade when presented with the optimum

impedance. This does, however, again emphasize the importance of performing these stress tests on a statistically significant sample size.

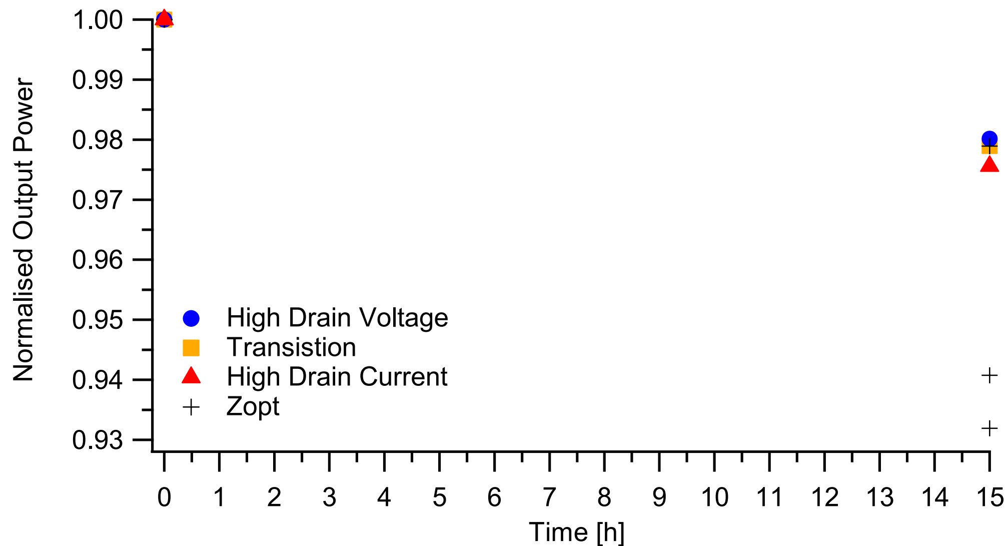

Figure 5.15 - Output power of the RF reference characterisation stages from the stress tests at infinite VSWR and at the optimum impedance

The initial and final RF load lines observed from each of the stress periods is shown in figure 5.16, along with a DCIV measurement from a device pre stress. It is important to note that during the stress test on the high drain voltage region of the infinite VSWR the de-embedding procedure has an effect on the measurement of peak RF drain current during the stress period. This is due to the shape of the waveform, as can be seen in figure 5.17, where the large dip in current is caused by the interaction of the load line with the boundary conditions of the device. It is the peaks either side of this dip that are affected by the de-embedding procedure, and hence will only be seen when the load line interacts with the boundary conditions in this way. Figure 5.18 shows the peak RF drain current measurements during the stress period, along with the measurements of maximum current from the reference characterisation stages.

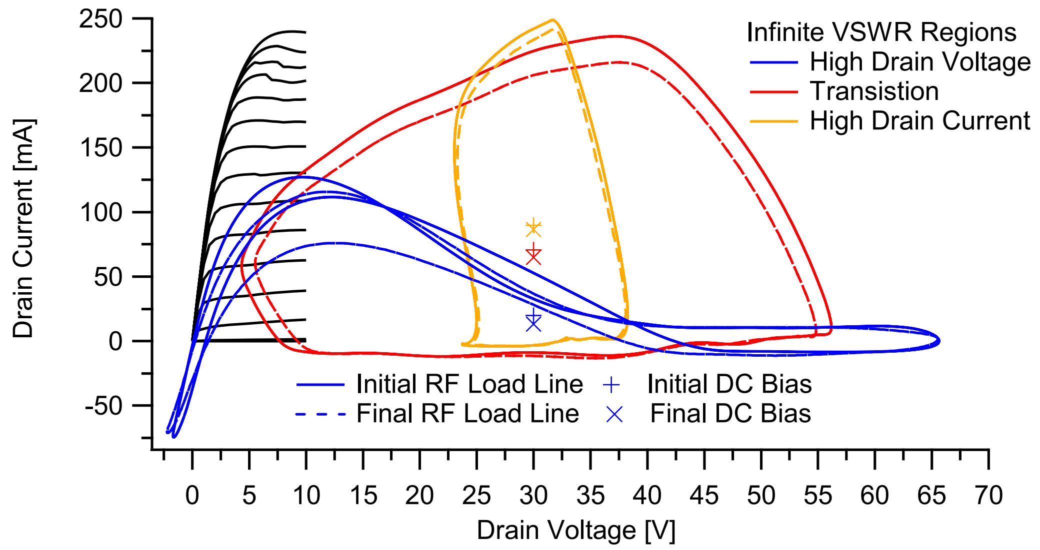

Figure 5.16 - RF load lines before and after 15 hours of stress at one of the regions of the infinite VSWR sweep, together with a representative DCIV of an unstressed device

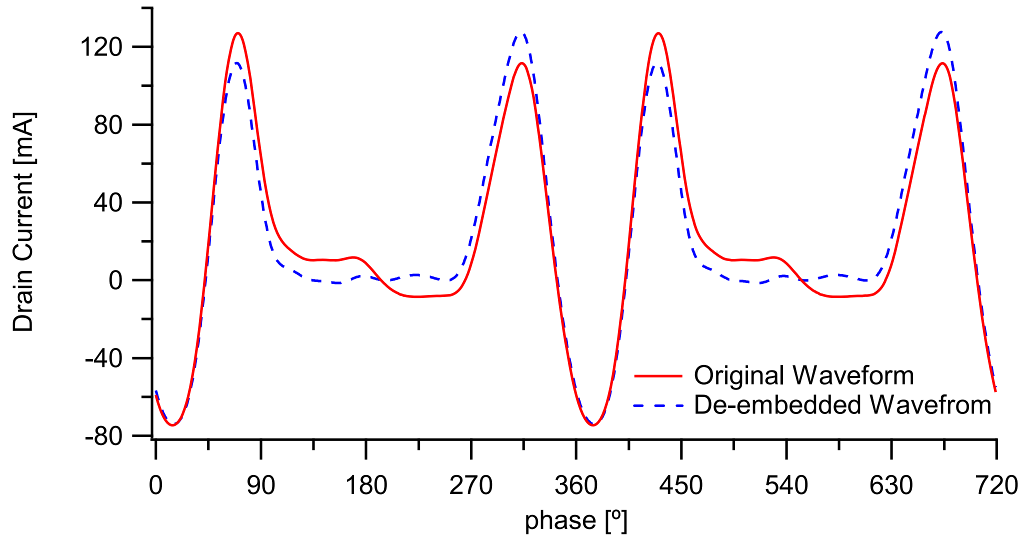

Figure 5.17 - RF drain current waveforms from the high drain voltage stress period at the device plane (original waveform) and de-embedded

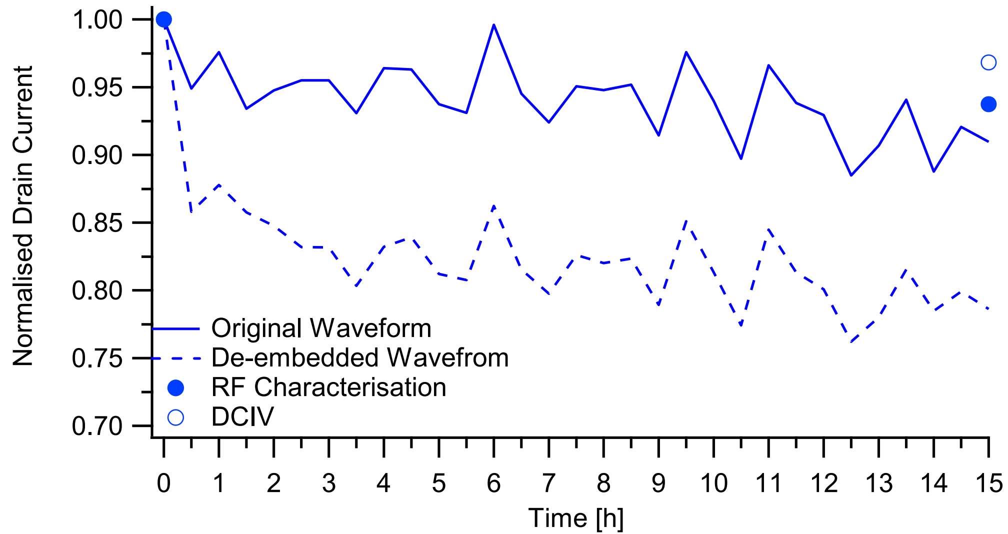

Figure 5.18 - Peak RF drain current measurements taken from the stress period for waveforms at the device plane (original waveform) and de-embedded, along with measurements of maximum drain current from the reference characterisation stages

It is possible to compare these measurements (and the ones of output power and drain voltage swing) with the same measurements from the previous set of RF stress tests. By doing this it can be seen that the level of degradation suggested by the reference characterisation stages suggests that the maximum RF drain current measurements taken from the de-embedded waveform indicate a much higher level of degradation than would have been expected. It was concluded that this has been distorted by the de-embedding procedure, therefore for the rest of this section the measurements on the device stressed with the high drain voltage VSWR load will be shown without de-embedding. It is still possible to compare these measurements to the others because the de-embedding has minimal effect on the peak drain currents of the other measurements.

It was established in the previous section that although the measurements made in the reference characterisation stages provide an indication of the level of degradation, they do not show it to the full extent seen during the RF stress period. Therefore to put the measurements made during these RF stress periods in context, they can be compared to the stress periods from the previous set of stress tests. Figure 5.19 shows the comparison between the peak RF drain currents and figure 5.20 shows the

comparison between the RF drain voltage swings, from during the stress periods at infinite VSWR and at the optimum impedance. As with the RF output power measurements shown in figure 5.15, this indicates that the three devices stressed in this section have suffered from minimal degradation.

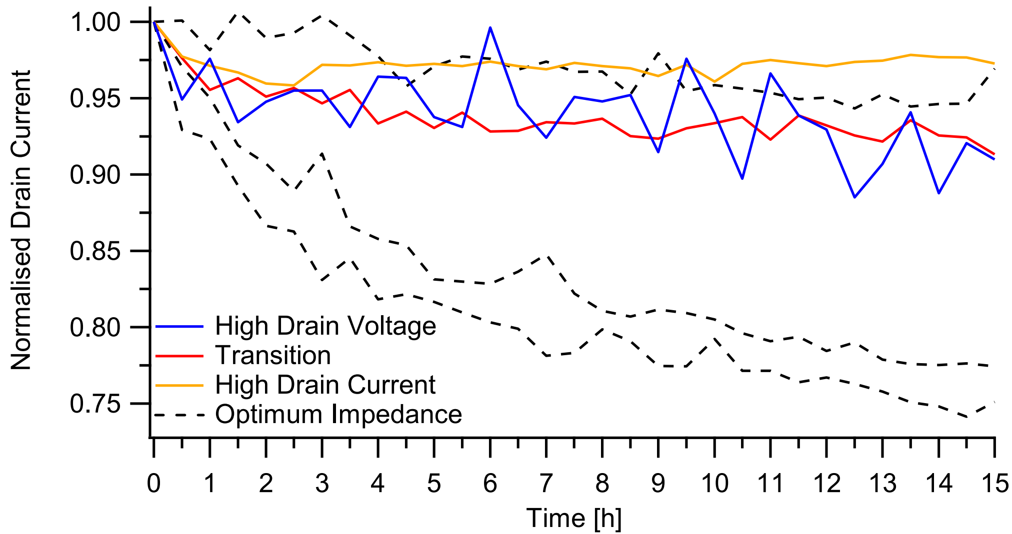

Figure 5.19 - Normalised drain currents measurements from during the RF stress periods of both the infinite VSWR and stress tests at the optimum impedance

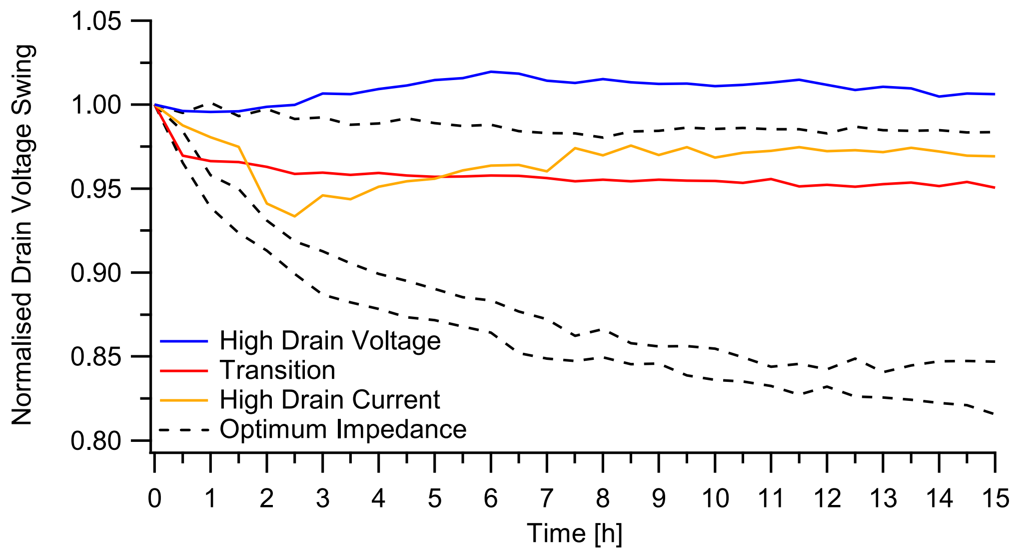

Figure 5.20 - Normalised drain voltage swing measurements from during the RF stress periods of both the infinite VSWR and the stress tests at the optimum impedance

The RF gate diode characteristics of the initial and final measurements of the RF stress period of the devices stressed with an infinite VSWR, and from

device A from the previous set of stress tests, are shown in figure 5.21. From this it can be seen that the minimum RF gate voltage swing is unaffected by the load impedance, however the peak RF gate voltage is affected by the RF gate current being drawn. The devices stressed with the high RF drain current and the transition regions both have the highest peak gate voltage, but show minimal signs of the gate diode turning on. In contrast both the devices stressed at the optimum and the device stressed with the high RF drain voltage region have reduced peak RF gate voltage, but show that the gate diode has turned on. The device stressed in the high RF drain voltage region also shows an increase in the DC gate current due to the increase in peak RF gate current. This variation in the turn on conditions of the gate diode is due to the fundamental load impedance of the device. Specifically when the device is presented with a real impedance the RF gate voltage and drain voltage waveforms are 180° out of phase with each other, which can cause the gate-drain diode to become forward biased and conduct gate current. However when the device is presented with a reactive load the RF gate voltage and drain voltage waveforms are no longer 180° out of phase, therefore preventing the gate drain diode from becoming forward biased. This was discussed in more detail in section 3.4.1.

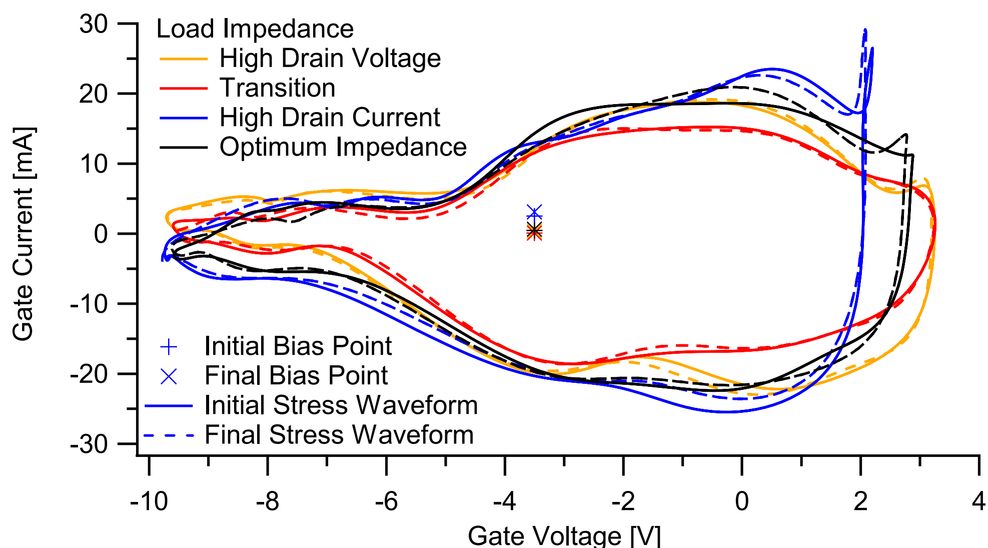

Figure 5.21 - Gate diode characteristics of the initial and final RF stress period measurements of the devices stressed with infinite VSWR and device A from the stress tests at the optimum impedance

As with the previous set of RF stress tests the measurements made in the DC reference characterisation stages can be analysed, figure 5.22 shows the gate leakage current sweeps and figure 5.23 shows the transfer characteristics from the device stressed with the high RF drain voltage region. From the gate leakage current sweeps it can be seen that the device stressed with the high drain voltage region shows the characteristic increase of gate leakage current due to gate edge degradation, whereas the device stressed with the transition region shows minimal increase. This is consistent with the idea that this degradation is caused by high electric field concentrations at the drain side of the gate edge [12]. However, the device stressed in the high RF drain current region shows a high gate current leakage even before stressing, probably due to defects in the device. After the stressing period this gate leakage current has decreased to a similar level seen in the device stressed in the high RF drain voltage region. All three devices show a small decrease in the magnitude of the pinch off voltage leading to a decrease in the peak drain current, an example of which is shown in figure 5.23 for the device stressed in the high RF drain voltage region.

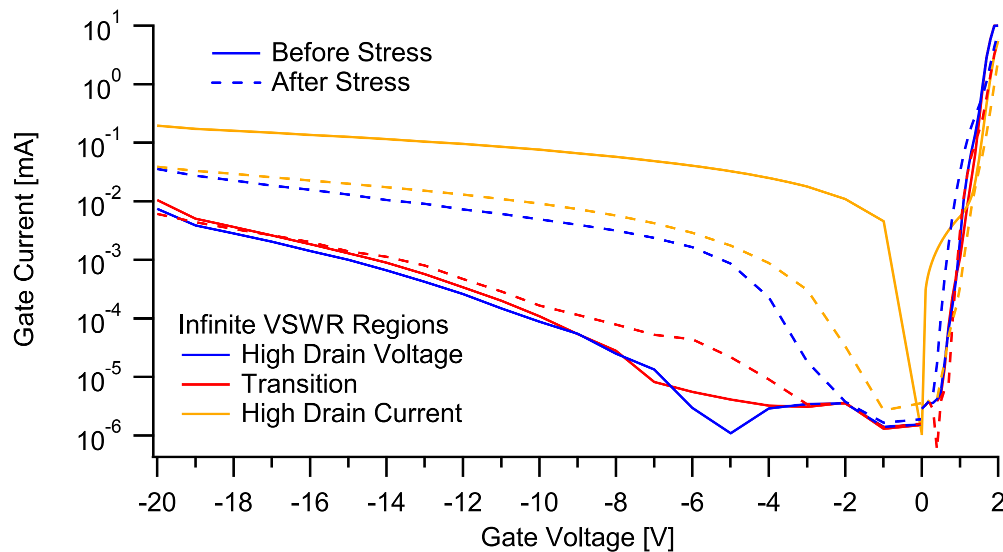

Figure 5.22 - Gate leakage current sweeps from the DC reference characterisation stages for the three device stressed with infinite VSWR load impedances

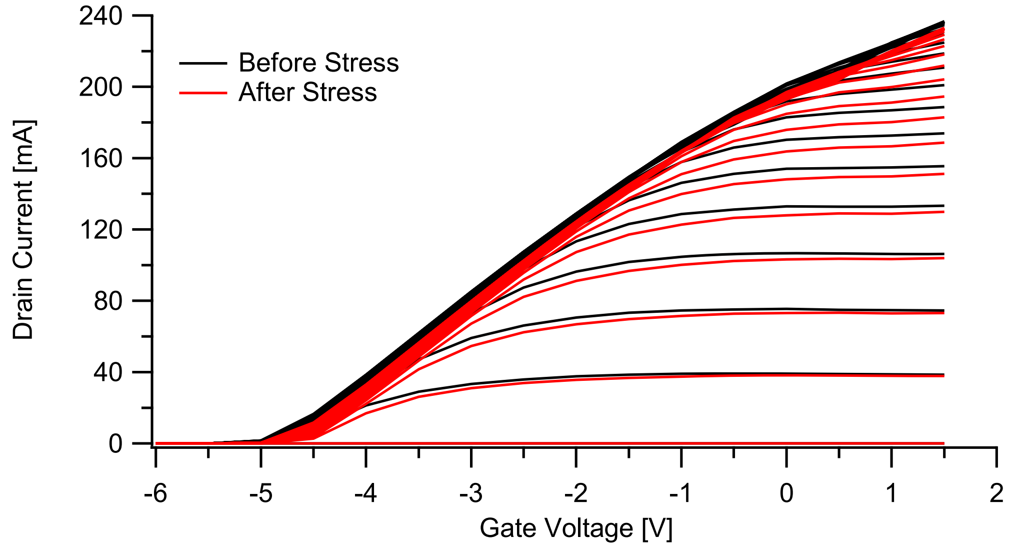

Figure 5.23 - Transfer characteristics before and after the device was stressed in the high drain voltage region of the infinite VSWR sweep

5.4 Step Stress Test

Step stress tests are commonly used in reliability studies in order to gradually increase the stress that is applied to a device. As described in section 5.2 the stress test procedure can easily be extended by including multiple stress periods and repeating the characterisation stages in between each. In this section this approach is used to measure both drain bias and input power step stress tests [8,13], with the DC and RF characterisation stages are performed as described in section 5.2.

5.4.1 Drain Bias Step Stress Test

The stress test procedure is used to stress a single device at four different drain bias voltages, starting with 15V and increasing by 5V per stress period up to 30V. In each period the device is RF stressed for 6 hours in class AB mode, with the fundamental impedance set to the optimum and the second and third set to short circuits. It should be noted that the final RF stress period will present the device with the same RF load and drain bias conditions as the RF stress tests at the optimum impedance in section 5.3.1.

The RF output power measured during the RF stress periods is shown in figure 5.25, along with the RF output power of the RF reference characterisation stages made between each of the stress periods. It can be seen that there is an increase in the RF output power for every RF stress period of the test due to the increase in the drain bias voltage. In order to show any degradation these step increases in RF output power were removed before the normalisation procedure, allowing the output powers measured during the stress periods and the characterisation stages to be more easily compared. These normalised output powers are shown in figure 5.26.

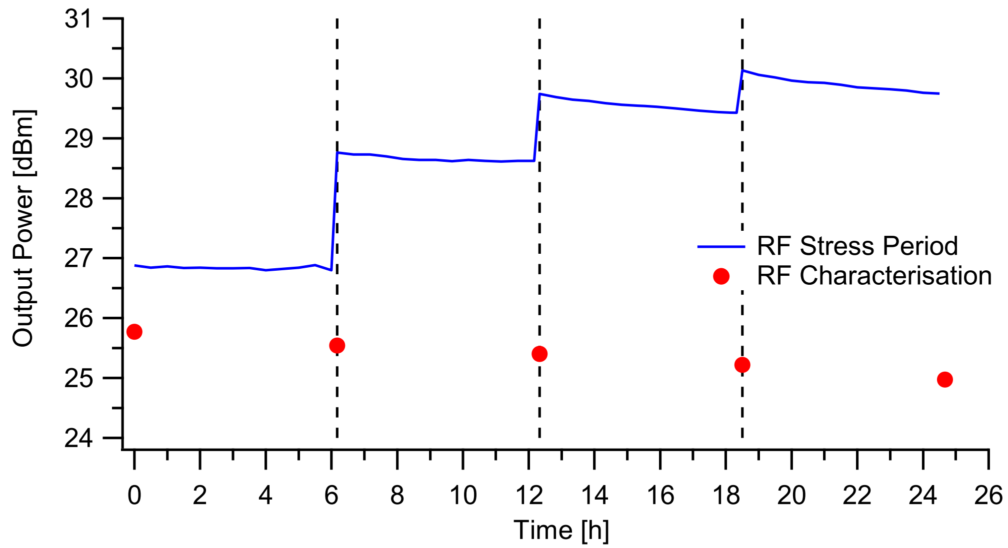

Figure 5.25 - RF output power from the RF reference characterisation stages and from during the stress periods

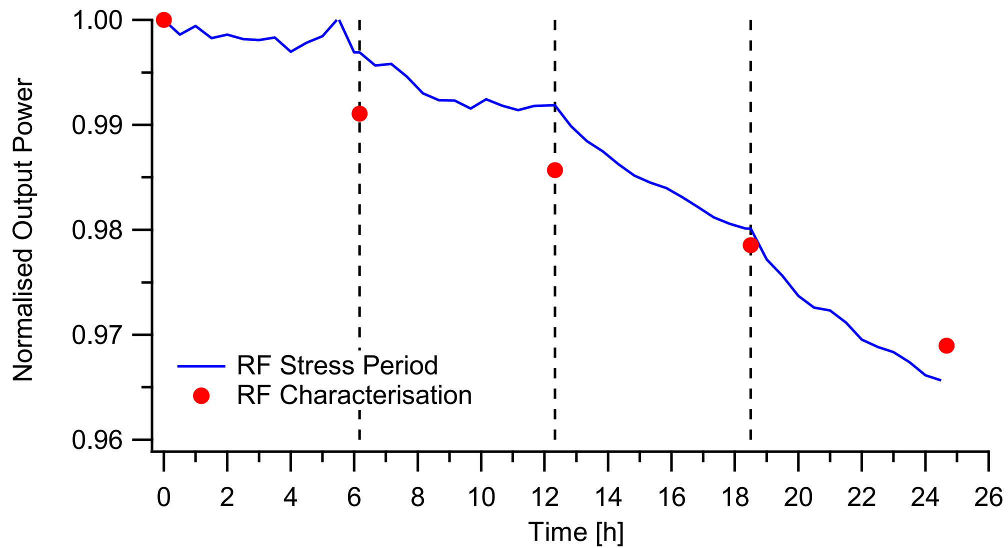

Figure 5.26 - Normalised RF output power measured during the stress period (the step increases in power due to the increase in drain bias were removed before normalisation) and from the RF reference characterisation stages

As with the simple RF stress tests at the optimum impedance, the measurements of RF output power, both during the RF stress period and from the RF reference characterisation stages, show similar levels of degradation. This again suggests that the RF output power of the measurements made in the RF reference characterisation stage can be used to assess the overall level of device degradation during the RF stress period.

The initial and final RF load lines from each of the four stress periods are shown in figure 5.27, together with the DCIV measurement made before any stress.

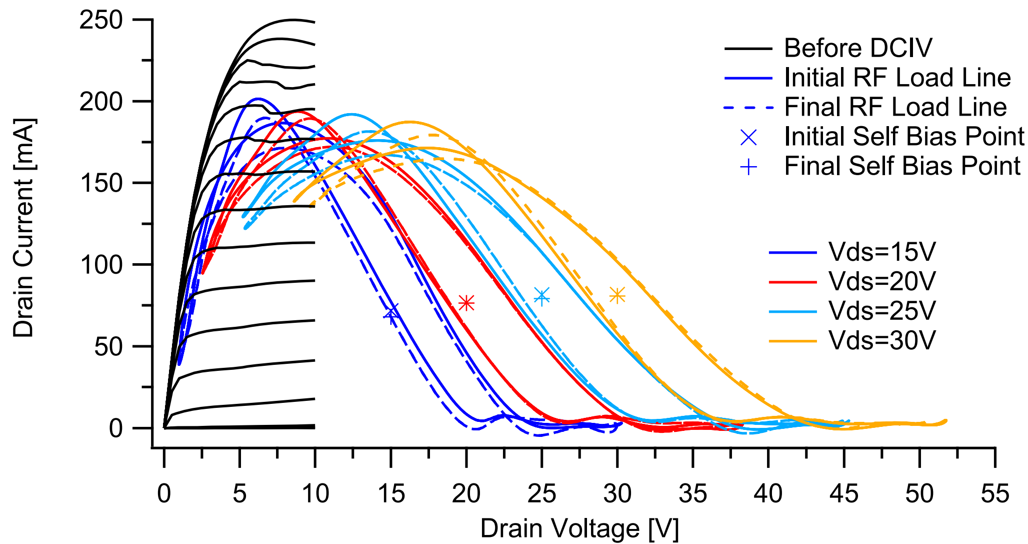

Figure 5.27 - Initial and final RF load lines from the four RF stress periods and the initial DCIV

As with the previous tests the RF IV waveform measurements made during the RF stress period can be compared to the reference characterisation stages. Figure 5.28 shows the comparison of the maximum drain currents from the RF waveforms and from the DCIV. Figure 5.29 shows a comparison between the RF drain voltage swings. As was the case with the RF output power measured during the stress period, the step increase in drain voltage swing due to the increase in drain bias has been removed before the normalisation procedure.

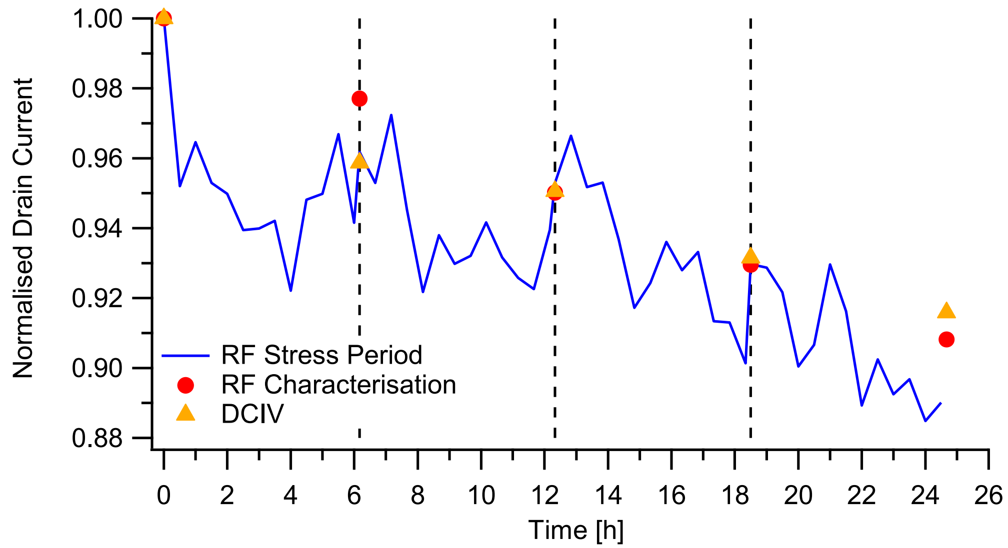

Figure 5.28 - Normalised drain currents from during the RF stress period and the DC and RF reference characterisation stages

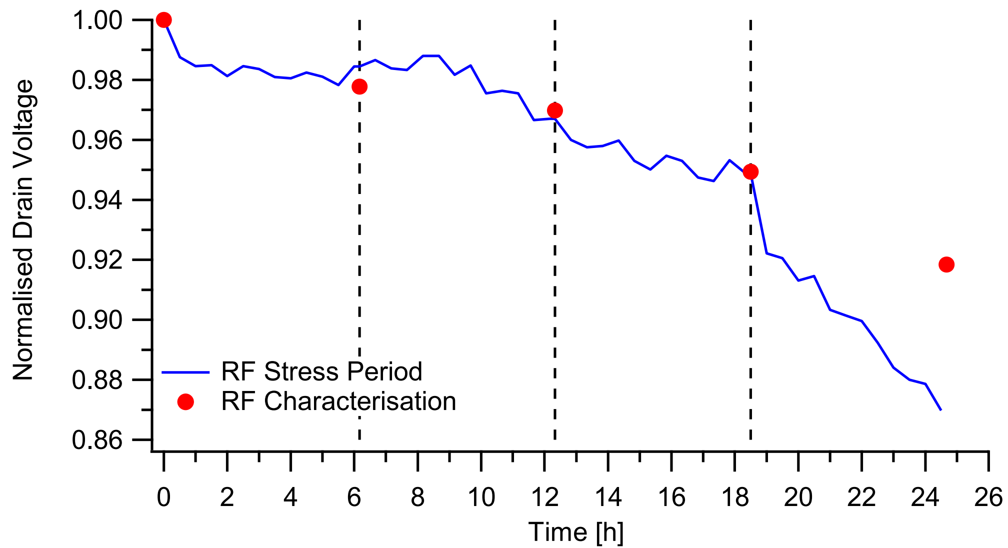

Figure 5.29 - Normalised drain voltage swings from during the RF stress periods and the RF reference characterisation stages

Figure 5.30 shows the RF gate-drain voltage measured during the RF stress periods along with the gate leakage current measured during the DC reference characterisation stages at V_{GS}=-5, as in [11]. In addition figure 5.31 shows the complete gate leakage sweeps from all of the DC reference characterisation stages. It can be seen that the gate leakage current increases by 2 orders of magnitude after the RF stress period where the device is biased at 20V. It is during this RF stress period that the RF IV waveform measurements confirm that the RF gate-drain voltage first

exceeds the critical voltage which triggers the gate edge breakdown. This is consistent with the theory that it is a field driven effect, but also suggests that it can occur on a timescale that is shorter than the RF period. The fact that the sudden increase in gate leakage current is uncorrelated with the gradual RF degradation suggests, not surprisingly, that these are essentially independent processes [8]. Gate leakage is a point failure whereas the RF degradation occurs across the entire gate width.

Figure 5.32 shows the transfer characteristic from the DC reference characterisation stages before the RF stress test and after the first RF stress period where the device is biased with 15V. This shows the pinch off voltage of the device has reduced in magnitude once again, resulting in a drop in the peak drain current. After this the pinch off voltage shows minimal further degradation.

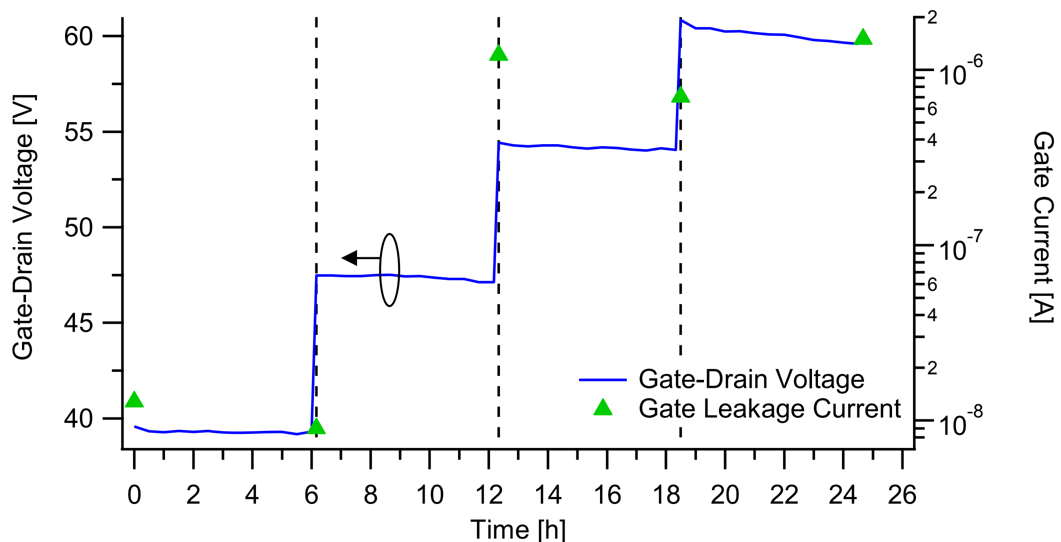

Figure 5.30 - RF gate-drain voltage from the measurements during the RF stress period along with the gate leakage current at V_{GS}=-5V measured during the reference DC reference characterisation stages

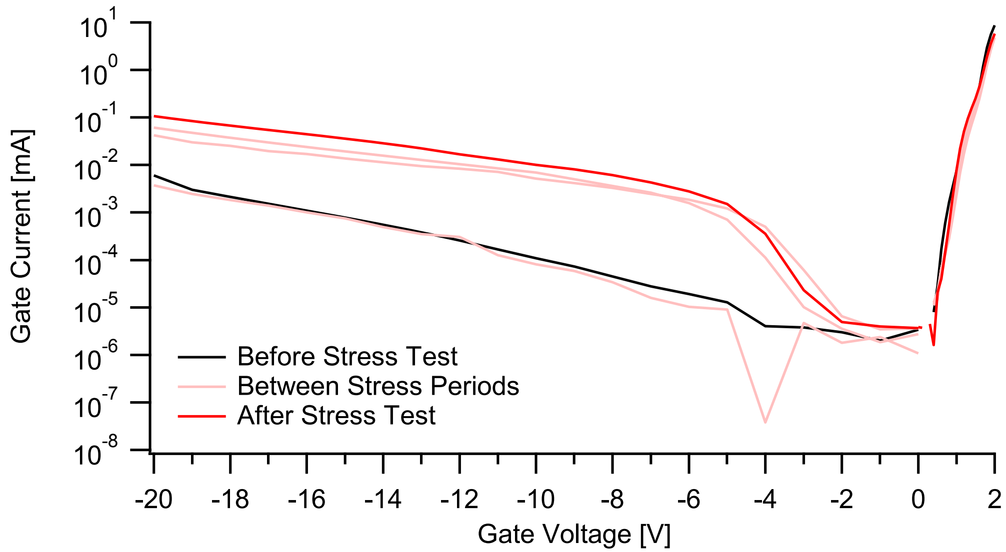

Figure 5.31 - Gate leakage current sweeps measured during the DC reference characterisation stages

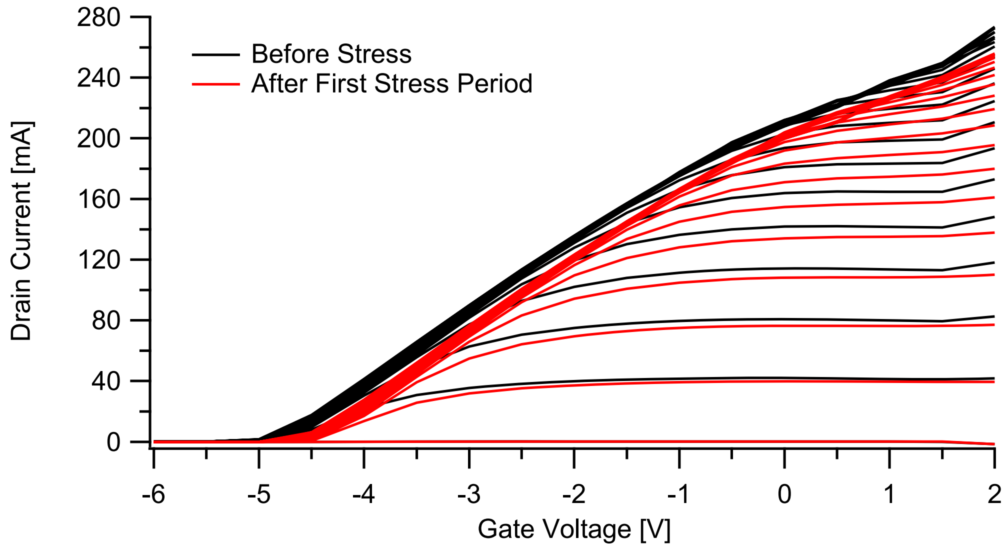

Figure 5.32 - Transfer characteristic from the DC reference characterisation stages before the stress test and after the first stress period, after this there is minimal change in the pinch off voltage

The final stress period of this drain bias step stress test presents the same conditions to the device as the simple stress tests at the optimum impedance from section 5.3.1. The only difference is that the RF stress periods are 6 hours long during the drain bias step stress test and 15 hours during the simple stress tests. Despite this is still possible to compare the measurements made during the RF stress periods of both stress tests. In doing so it appears as though the degradation in performance of the device

during the final stress period of the step stress test is closest to that seen in device C (the device that showed minimal degradation) from the simple stress tests at the optimum impedance. Table 5.3 shows the percentage degradation seen in the RF output power, peak RF drain current and RF drain voltage swing during the final stress period of the drain bias step stress test and after the first 6 hours of the simple stress test on device C.

Table 5.3 - Degradation seen during the final stress period of the drain bias step stress test and after the first 6 hours of the simple stress test on device C

	Final stress period of drain bias step stress test	**After first 6 hours of simple stress test on device C**
RF output power	1.4%	0.7%
RF drain current	2.2%	2.4%
RF drain voltage swing	3%	1.2%

5.4.2 Input Power Step Stress Test

From the drain bias step stress test in the previous section it was found that the gate leakage current showed a step increase after the stress period where the device was biased at 20V. In order to investigate this effect an RF input power step-stress test was performed on a single device biased in class AB mode of operation, at a drain bias of 15V. The input power was stepped from 17dBm to 26dBm in 3dBm steps, where an input power of 20dBm causes the RF output power of the device to saturate, for stress periods of one hour. The fundamental load impedance was set to the optimum and the second and third harmonic load impedances set to short circuits. Additionally the first stress period of the test was performed with the DC bias only in order to ensure that there is no effect on the device, as in [9].

The RF output power measured during the RF stress periods is shown in figure 5.33 along with the output power from the reference measurements made during the RF characterisation stages. It is interesting to note that there is a step change in the middle of the second stress period (first with RF applied). It can also be seen that in the final two RF stress periods there is a step decrease in the output power seen during these stress periods. This is

caused by the increase in input power pushing the device past the point where the output power is saturated. As with previous RF stress tests, the RF output powers measured during the stress period can be normalised to provide a direct comparison, as shown in figure 5.34. The normalised output powers of the fifth and sixth stress periods have had the drop in output power, caused by the increase in input power, taken into account before the normalisation.

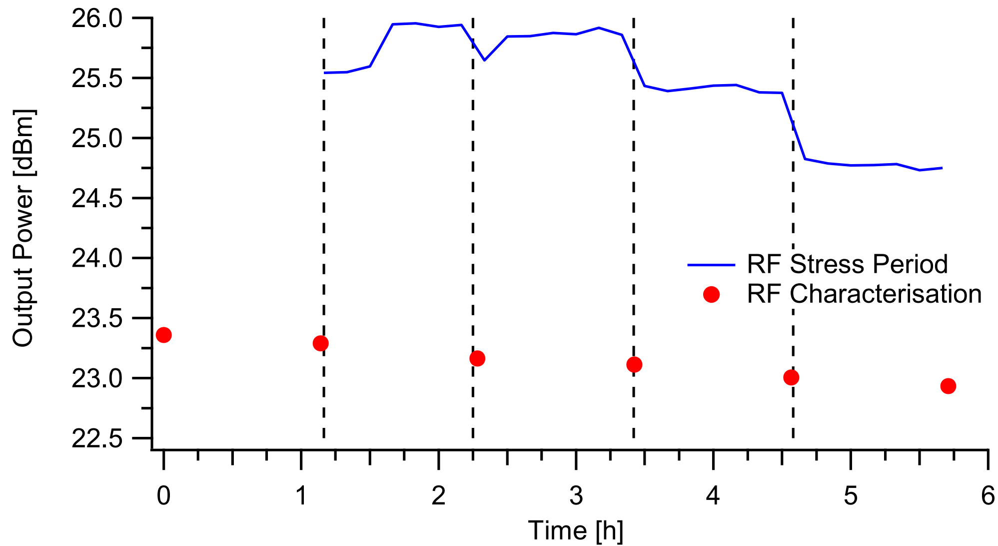

Figure 5.33 - RF output power from during the stress periods and from the RF reference characterisation stages

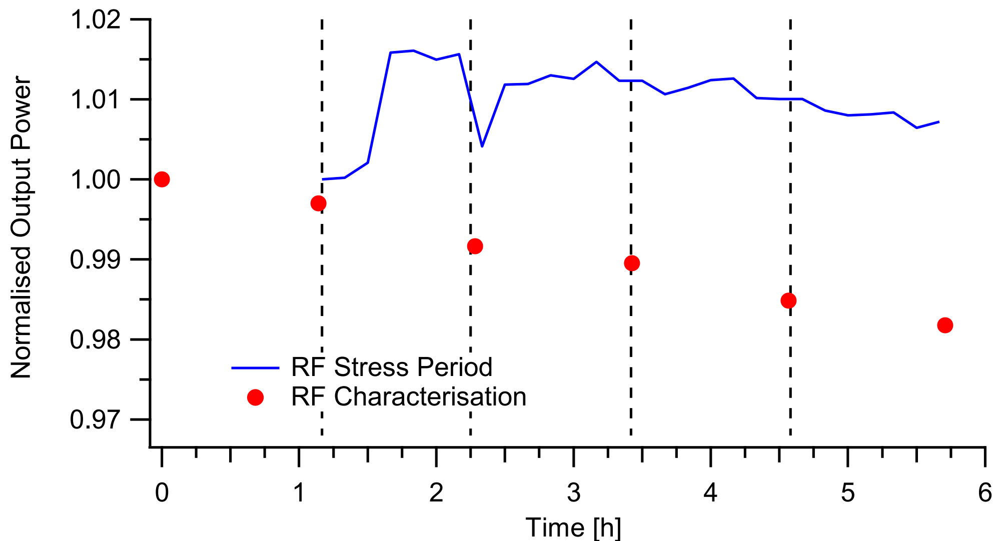

Figure 5.34 - Normalised RF output power from during the stress periods and from the RF reference characterisation stages

The initial and final RF load lines from the RF stress periods are shown in figure 5.35 along with the DCIV measured before any stress. Once again the measurements made during the RF stress periods can be compared with those of the reference characterisation stages.

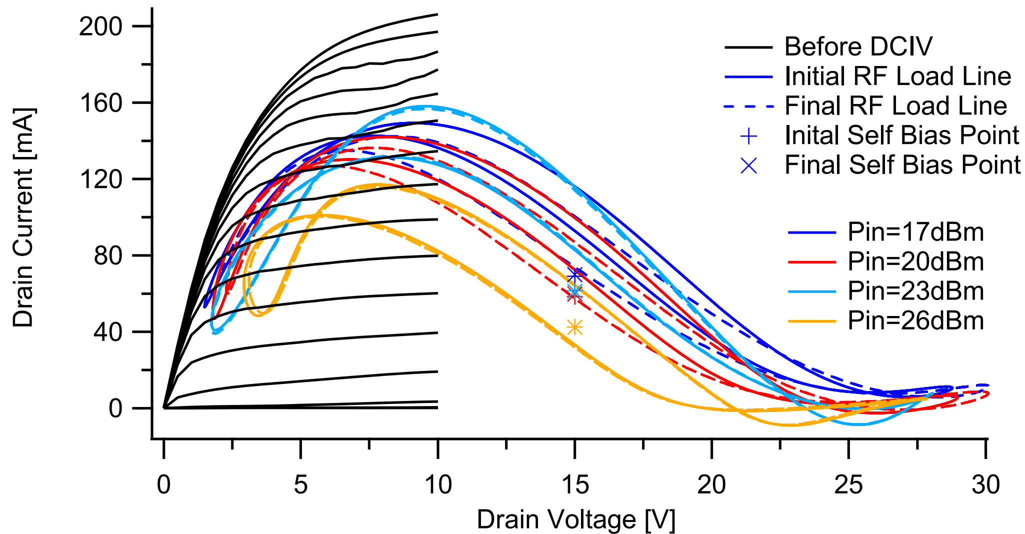

Figure 5.35 - Initial and final RF load lines from each of the stress periods along with the before DCIV

Figure 5.36 shows the peak RF drain current from the measurements made during the RF stress periods together with the same from the RF reference characterisation stage and the DCIV knee current. Figure 5.37 shows the RF drain voltage swing from the waveform measurements made during the RF stress periods and from the RF reference characterisation stages.

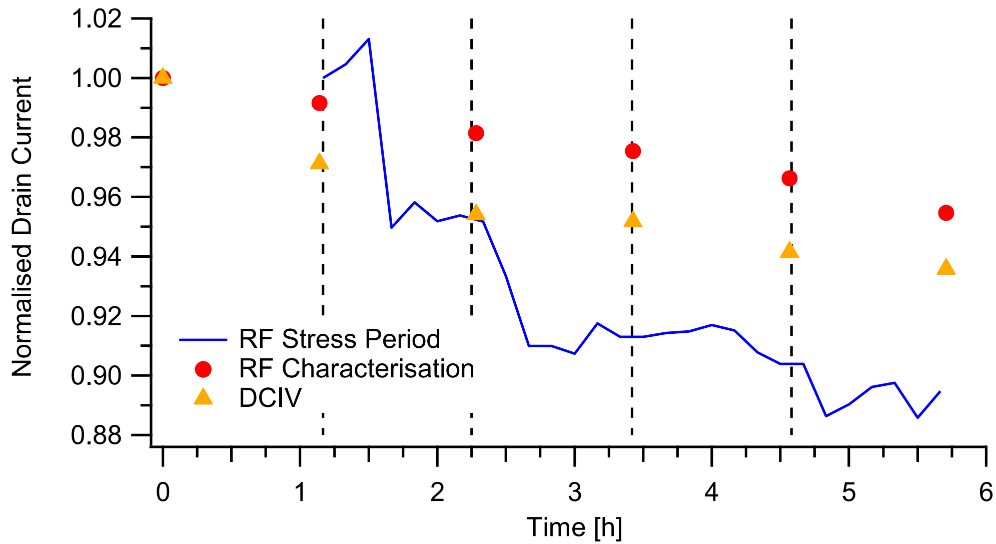

Figure 5.36 - Comparison of the peak RF drain currents from the measurements made during the stress test, from the RF reference characterisation stages and the current at the knee of the DCIV

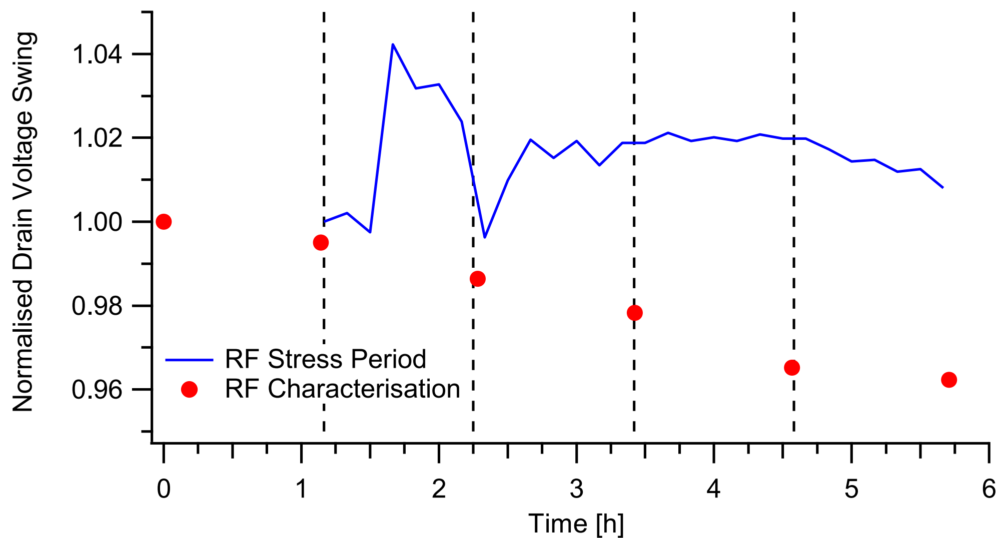

Figure 5.37 - Comparison of the RF drain voltage swings from the measurements made during the stress periods and from the RF reference characterisation stages

It can be seen that the step change in output power of the device during the second RF stress period is reflected in the RF drain current and voltage waveforms. In addition there is no change in the fundamental load impedance or in the RF gate voltage or current waveforms during this stress period.

As with the previous stress test, the measurements from the DC reference characterisation stages can be analysed. Figure 5.38 shows the

RF gate-drain voltage measured during the RF stress periods and also the gate leakage current at V_{GS}=-5V, the complete DC reference gate leakage current sweeps are shown in figure 5.39. From these it can be seen that the characteristic step increase in gate current occurs after the second RF stress period (first with RF), followed by further increases after the fourth and fifth RF stress periods. In addition there is minimal change in the pinch off voltage of the device shown on the transfer characteristics measured in the DC reference characterisation stage.

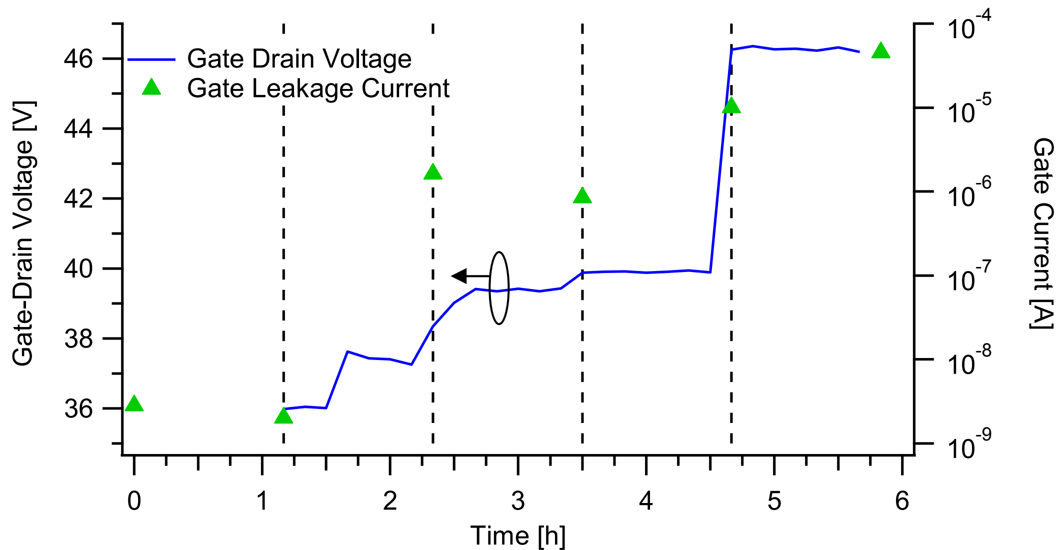

Figure 5.38 - RF drain-gate voltage measured during the stress periods and the gate leakage current at V_{GS}=-5V measured in each of the DC reference characterisation stages

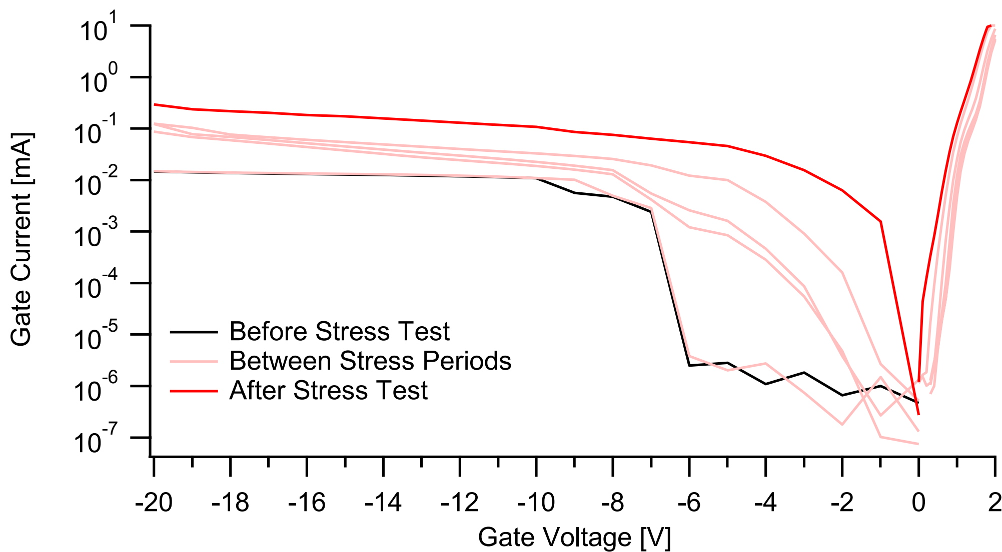

Figure 5.39 - Complete gate leakage sweeps from the DC reference characterisation stages

5.5 Conclusions

In this chapter the RF IV waveform measurement and engineering system has been used to perform a variety of RF stress tests. The results have been analysed both to look for failure mechanisms and also to investigate how DC and RF waveform reference measurements made before and after stressing compare to the RF waveform measurements made during the stress period itself. It has been shown that the percentage change in output power before and after RF stress was similar whether measured at low drain voltage (for the RF reference characterisation stage) or high drain voltage (during the RF stress period). However, when the actual RF waveforms from the RF reference characterisation stage are compared with those measured during the RF stress period it was found that there was a larger percentage degradation in the peak RF drain currents and drain voltage swing observed in the RF measurements during the stress period. Hence detailed RF IV waveform measurements are required to see the full impact of RF stress induced degradation on the RF load line.

From these RF stress tests it was shown that the cause for the RF degradation was an increase in the DC-RF dispersion caused by the virtual gate effect. In addition, these measurements suggest that the sudden increase in gate current caused by exceeding the device critical voltage is uncorrelated with the more gradual RF degradation. Although the results of the drain bias step-stress test appear to indicate that the gate edge damage caused by exceeding the critical voltage can happen at timescales shorter than the RF period. As mentioned in the introduction, the measurements performed in this chapter are by no means intended to categorically define the operational constraints of GaN HFETs, they are more to demonstrate how the RF IV waveform measurement and engineering system can be used to perform RF stress testing.

5.6 References

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Chapter 6 – Conclusions and Future Work

The work in this thesis has been split into two main sections – the consequences of a load impedance mismatch and how RF IV waveform can compliment RF stress testing. The theme throughout both of these sections has been using the RF IV waveform measurement system to make measurements that are relevant to reliability concerns.

At the end of chapter 2 a theoretical s-parameter analysis of one port networks was performed from which it was shown that all of the possible consequences of an impedance mismatch can be seen during a VSWR sweep. The conditions presented to the device depend on the physical location of the mismatch with respect to the device. It was shown that the worst case scenario of impedance mismatch is when the load impedance is purely reactive, resulting in all of the power being reflected back. Only considering the load impedance this could result in either double the RF voltage or double the RF current that would be seen in the matched condition. However it was later shown that this is not the case when a device is taken into account, both the RF drain current and voltage swings are limited by the boundaries of device operation.

Chapter 3 showed how the results of the worst case infinite VSWR sweep can be split into three regions, one of high RF drain voltages, one of high RF drain currents and a transition region between the two. In addition the potential stresses to a device are identified in each region. The location of the regions during the sweep depends on the optimum impedance of the device; the transition region is located where the magnitude of the load impedance during the sweep is equal to the optimum resistance of the device. Here the magnitude of the RF voltages and currents are the same as those found at the optimum impedance, but with a 90° phase difference between the waveforms resulting in simultaneously high voltages and currents. At magnitudes of load impedance that are higher than the optimum high RF drain voltage swings are presented to the device. In this region the high peak RF drain voltages can extend beyond twice the drain bias voltage and also the minimum RF drain voltage can fall below the maximum gate

voltage, forward biasing the gate-drain diode. This leads to an increase in the peak and DC gate currents, which is suspected to be a leading contributor to RF degradation. It was shown that the voltage swings across the device in this region are maintained irrespective of the device size, drain bias voltage or input power due to the large fundamental impedance. The final region of high RF drain currents is located when the load impedance during the sweep is less than the optimum. In this region the low impedances cause the RF drain current waveforms to saturate leading to an increase in the DC quiescent drain bias, potentially up to class A. This exposes the device to conditions that resemble both the semi-on state at the DC quiescent bias and the on state with the peak RF drain current.

It was then shown that the RF drain voltage could be manipulated by terminating the harmonic load impedances with high impedances [1]. This presents a method by which the stresses presented to the device in the regions of the infinite VSWR sweep can be restrained or increased.

It was then shown that the results for sweeps with VSWR lower than infinity also depend on the optimum impedance of the device. If the optimum impedance is higher than the match condition then as the VSWR ratio decreases the sweeps will pull out of the region of high RF drain voltage swings [2]. In contrast, it should follow that if the optimum impedance is lower than the match then as the VSWR ratio decreases the sweep will pull out of the region of high RF drain current.

Currently VSWR sweeps have only been measured on small devices due to their availability, however ideally they should also be carried out on much larger devices in order to confirm that the regions of the infinite VSWR sweep still apply. This work could be taken forward by considering the effect of the matching network of the PA on the reflected power; this would be particularly interesting for the high efficiency modes that include non-zero harmonic load impedances (e.g. class F/F^{-1}).

The second part of this thesis investigated how RF IV waveforms could increase the amount of information available on the state of the device during the stress period. Chapter 4 extended the review of characterisation techniques used for PA design (from chapter 2) to look at how they can be

used for reliability measurements as well as introducing others. This culminated in showing that although using RF IV waveform measurements in RF stress testing is not a new idea, it is not something that is widely used. The second half of chapter 4 also presented a review of the common failure mechanisms in GaN HFETs. The research on which, until recently has been focussed on those caused by the high potential differences between the gate and drain caused by the ability to bias GaN HFETs at high drain voltages. However with the improvements that are being made, e.g. field plates, passivation and overall device structure, the high breakdown voltages of GaN HFETs are allowing other failure mechanisms to be seen during testing.

In chapter 5 a stress test procedure was developed (based in the one in [1]) that featured DC and RF reference characterisation stages before and after every stress period. This was used to perform a series of simple stress tests [4], before being extended to include multiple stress periods in order to perform step-stress tests [5] [6]. The results of these showed that the RF output power of the RF reference characterisation stage has a similar percentage drop to the RF output power measured during the stress period, making for a useful Figure of Merit (FOM) for stress testing. However, when comparing the actual RF IV waveforms from during the stress period and the reference characterisation measurements it can be seen that there is a much larger degradation in those measured during the stress period. This shows that RF IV waveform measurements are required to see the full extent of the degradation during RF stress testing. In addition the RF waveforms have the potential to be used to identify the failure mechanisms that are causing the degradation.

In the future, in order to increase the amount of information that the DC and RF reference stages provide there are further measurements that can be added, including source and drain resistance measurements and full RF fan diagram measurements. To take this further there are a series of stress tests that can be performed, all of which continue to use the stress testing procedure developed in this thesis. Firstly these stress tests can be performed using DC stress during the stress period instead of RF as this will allow very specific failure mechanisms to be stressed with tests that have

been shown in the literature. Doing this will show the effect of specific failure mechanisms on the RF performance of the device. This can then be extended by using the infinite VSWR load impedances highlighted in chapter 5 to emulate these DC stresses. Another set of stress test that can be performed would be to use different PA operating modes to stress the device. This could start simply by using class A, AB, B and C before moving on to class J, F and F^{-1}. This can then lead on to performing step-stress tests exploring the class B to class J and class F to continuous class F families of waveforms.

6.1 References

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Appendix 1 – RF Load Lines of VSWR Sweeps

In this appendix the RF load lines of the VSWR sweeps measured in section 3.6 will be presented.

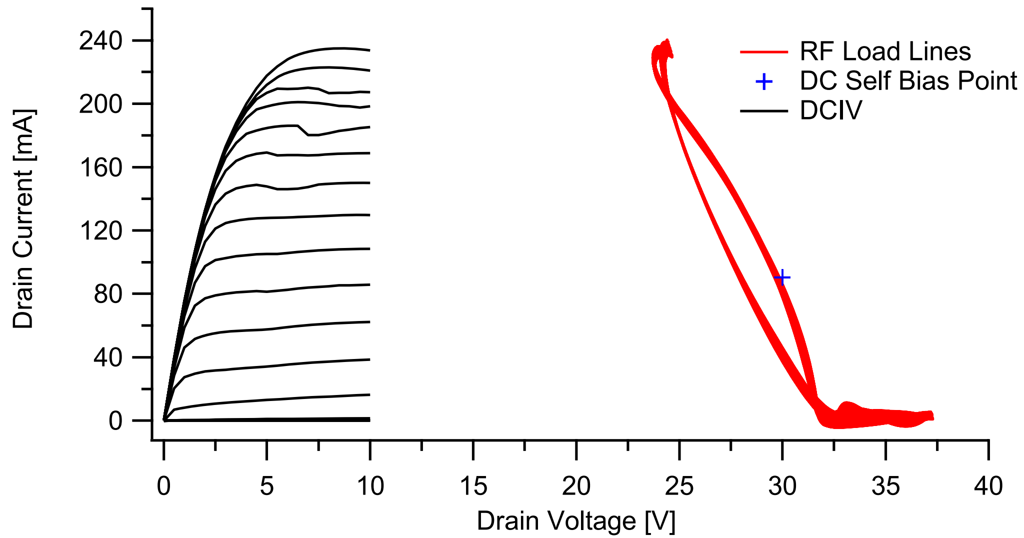

Figure A1.1 - RF load lines for the 1:1 VSWR sweep on a 2x100μm GaN HFET

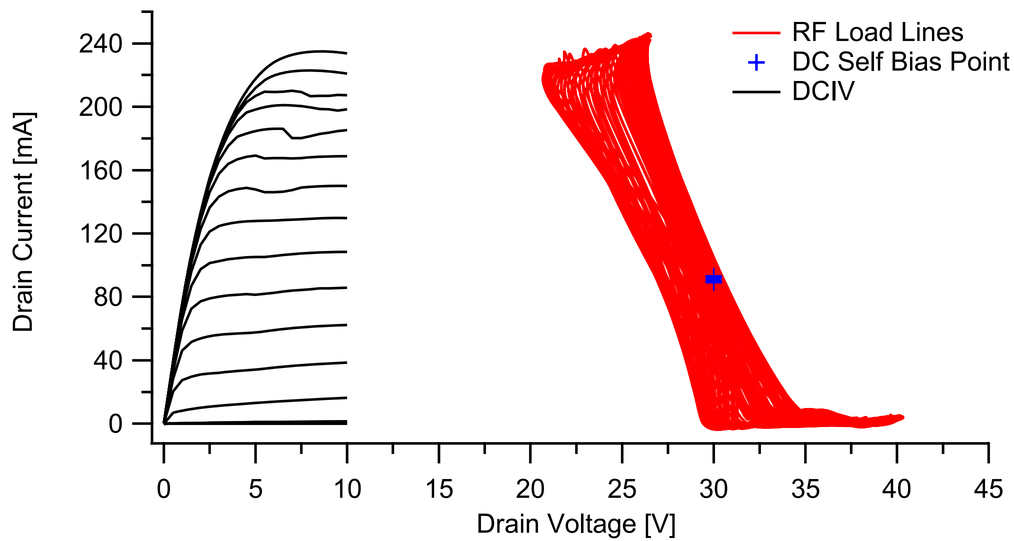

Figure A1.2 - RF load lines for the 1.5:1 VSWR sweep on a 2x100μm GaN HFET

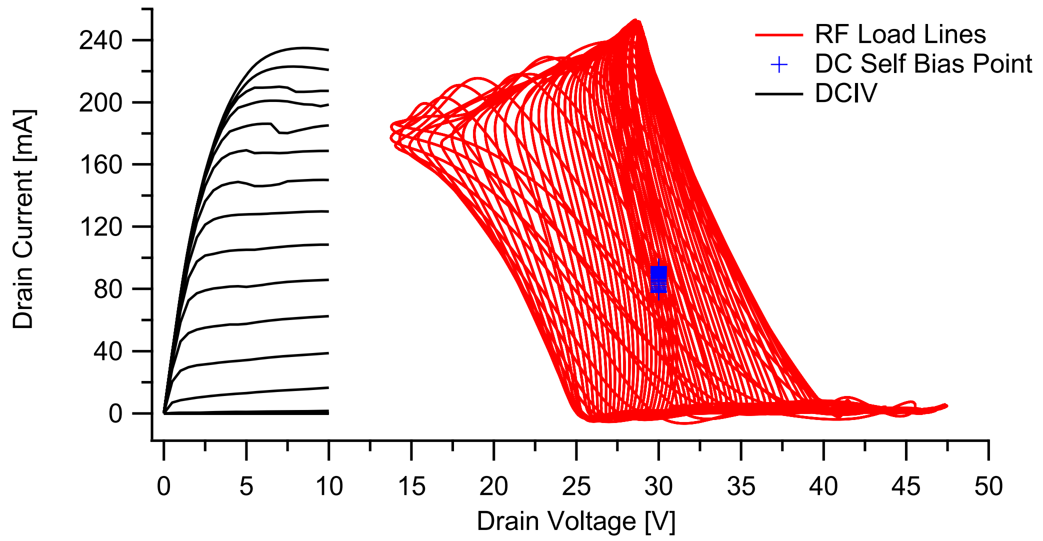

Figure A1.3 - RF load lines for the 3:1 VSWR sweep on a 2x100μm GaN HFET

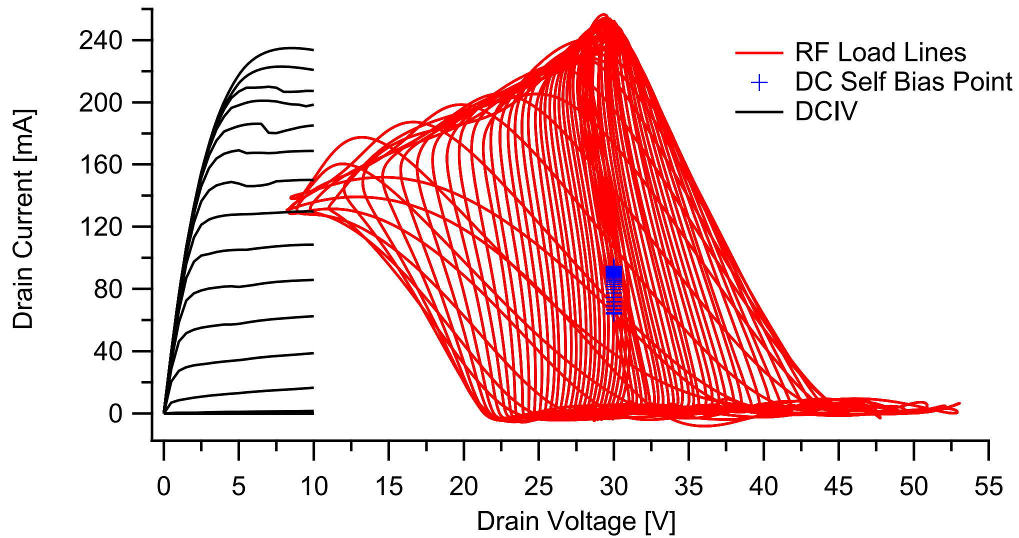

Figure A1.4 - RF load lines for the 5:1 VSWR sweep on a 2x100μm GaN HFET

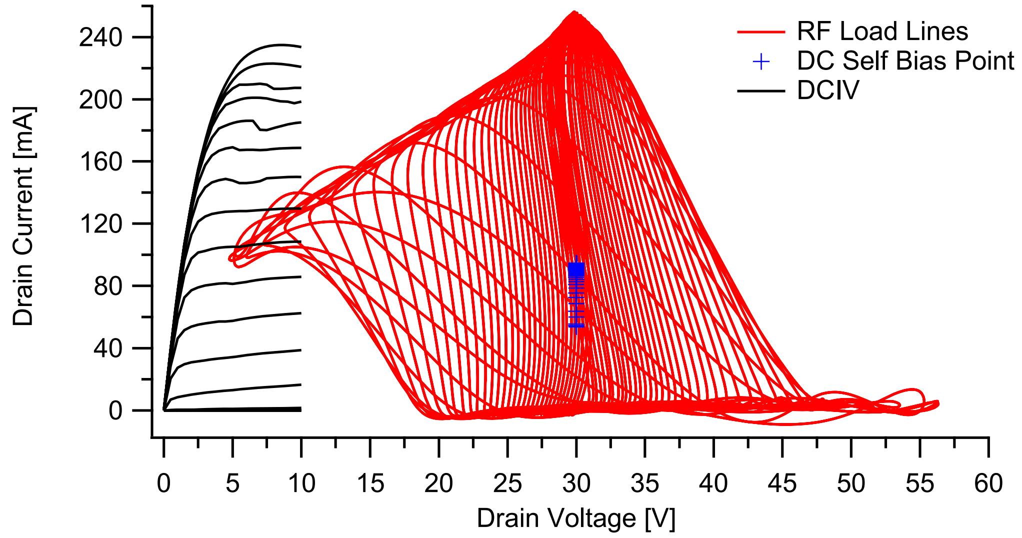

Figure A1.5 - RF load lines for the 7:1 VSWR sweep on a 2x100μm GaN HFET

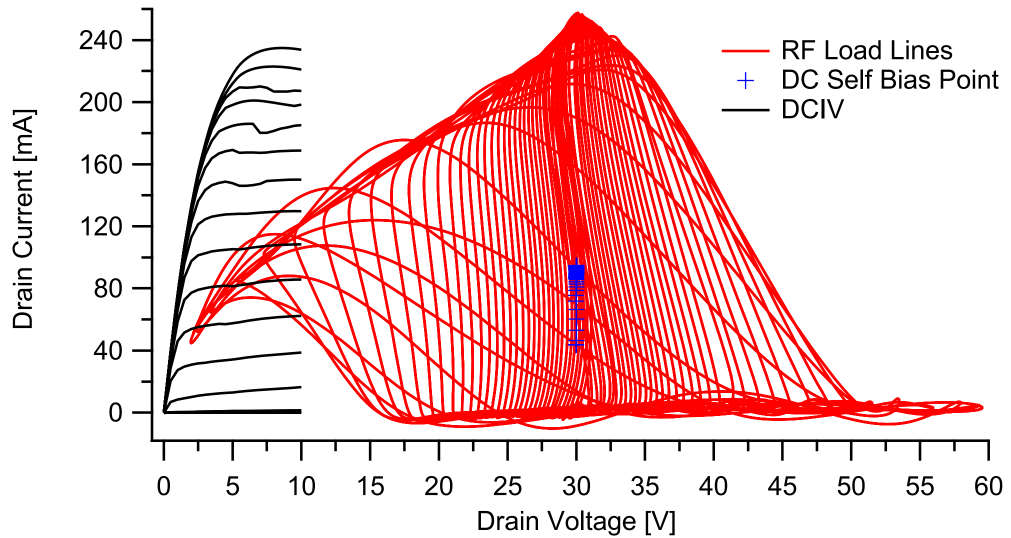

Figure A1.6 - RF load lines for the 10:1 VSWR sweep on a 2x100μm GaN HFET

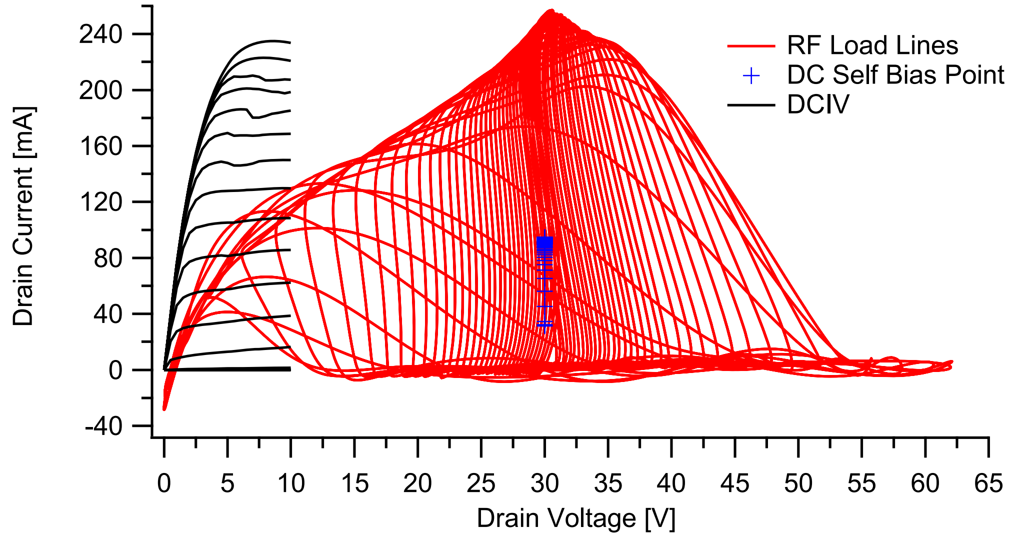

Figure A1.7 - RF load lines for the 19:1 VSWR sweep on a 2x100μm GaN HFET

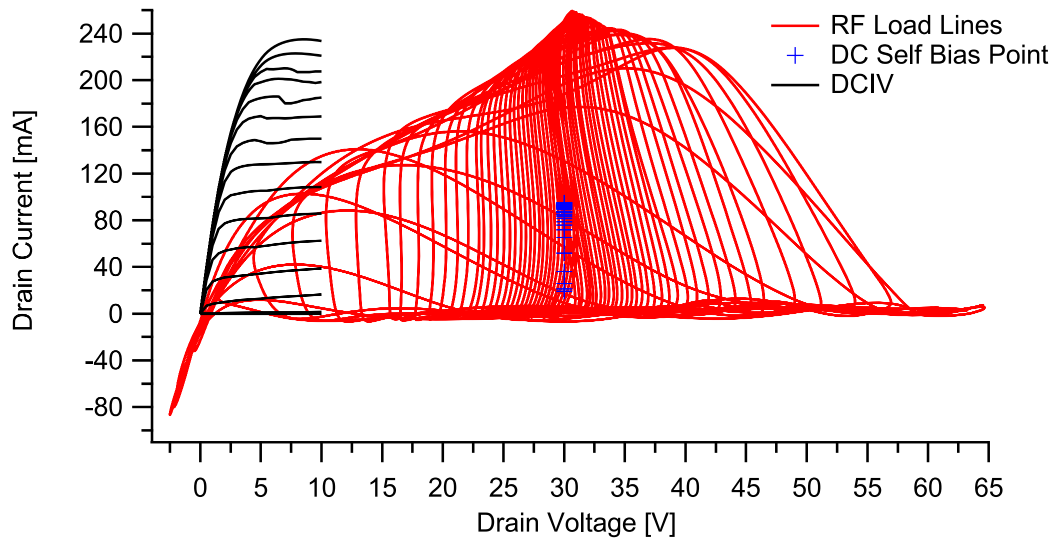

Figure A1.8 - RF load lines for the 99:1 VSWR sweep on a 2x100μm GaN HFET

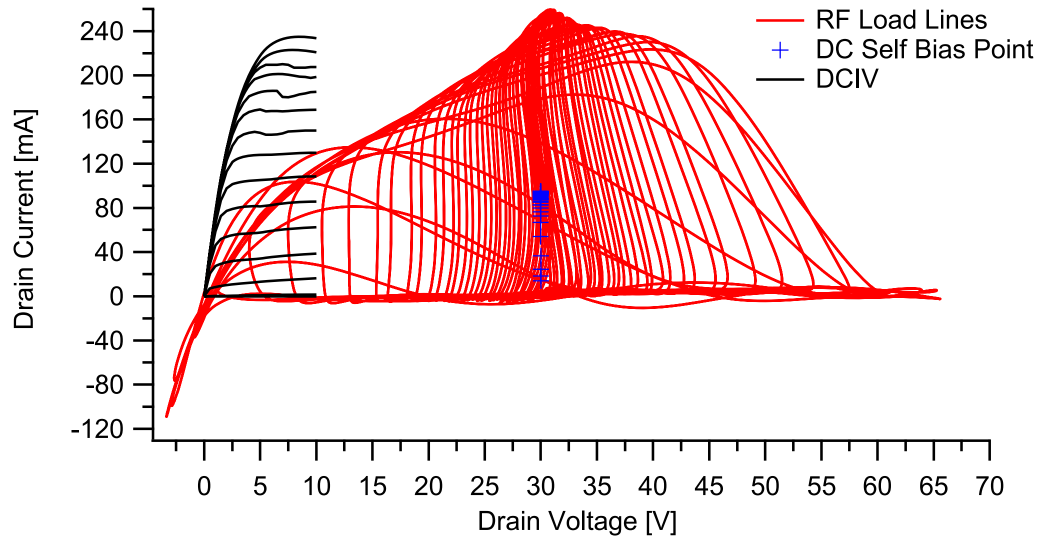

Figure A1.9 - RF load lines for the ∞:1 VSWR sweep on a 2x100μm GaN HFET