# CHALLENGES AND SOLUTIONS FOR LARGE-SCALE INTEGRATION OF EMERGING TECHNOLOGIES

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ABSTRACT

The semiconductor revolution so far has been primarily driven by the ability to shrink devices and interconnects proportionally (Moore's law) while achieving incremental benefits. In sub-10nm nodes, device scaling reaches its fundamental limits, and the interconnect bottleneck is dominating power and performance. As the traditional way of CMOS scaling comes to an end, it is essential to find an alternative to continue this progress. However, an alternative technology for general-purpose computing remains elusive; currently pursued research directions face adoption challenges in all aspects from materials, devices to architecture, thermal management, integration, and manufacturing.

Crosstalk Computing, a novel emerging computing technique, addresses some of the challenges and proposes a new paradigm for circuit design, scaling, and security. However, like other emerging technologies, Crosstalk Computing also faces challenges like designing large-scale circuits using existing CAD tools, scalability, evaluation and benchmarking of large-scale designs, experimentation through commercial foundry processes to compete/co-exist with CMOS for digital logic implementations.

This dissertation addresses these issues by providing a methodology for circuit synthesis customizing the existing EDA tool flow, evaluating and benchmarking against state-of-the-art CMOS for large-scale circuits designed at 7nm from MCNC benchmark suits. This

research also presents a study on Crosstalk technology's scalability aspects and shows how the circuits' properties evolve from 180nm to 7nm technology nodes. Some significant results are for primitive Crosstalk gate, designed in 180nm, 65nm, 32nm, and 7nm technology nodes, the average reduction in power is 42.5%, and an average improvement in performance is 34.5% comparing to CMOS for all mentioned nodes. For benchmarking large-scale circuits designed at 7nm, there are 48%, 57%, and 10% improvements against CMOS designs in terms of density, power, and performance, respectively. An experimental demonstration of a proof-of-concept prototype chip for Crosstalk Computing at TSMC 65nm technology is also presented in this dissertation, showing the Crosstalk gates can be realized using the existing manufacturing process.

Additionally, the dissertation also provides a fine-grained thermal management approach for emerging technologies like transistor-level 3-D integration (Monolithic 3-D, Skybridge, SN3D), which holds the most promise beyond 2-D CMOS technology. However, such 3-D architectures within small form factors increase hotspots and demand careful consideration of thermal management at all integration levels. This research proposes a new direction for fine-grained thermal management approach for transistor-level 3-D integrated circuits through the insertion of architected heat extraction features that can be part of circuit design, and an integrated methodology for thermal evaluation of 3-D circuits combining different simulation outcomes at advanced nodes, which can be integrated to traditional CAD flow. The results show that the proposed heat extraction features effectively reduce the temperature from a heated location. Thus, the dissertation provides a new perspective to overcome the challenges faced by emerging technologies where the device, circuit, connectivity, heat management, and manufacturing are addressed in an integrated manner.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a thesis titled "Challenges and Solutions For Large-Scale Integration of Emerging Technologies" presented by Md Arif Iqbal, candidate for the Doctor Of Philosophy degree, and certify that in their opinion it is worthy of acceptance.

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ACRONYMS

| | |
|---|---|
| **CMOS** | Complementary Metal–Oxide–Semiconductor |
| **IC** | Integrated Circuit |
| **CAD** | Computer-Aided Design |
| **QCA** | Quantum-Dot Cellular Automata |
| **EDA** | Electronic Design Automation |
| **VHDL** | VHSIC Hardware Description Language |
| **FET** | Field Effect Transistor |
| **RRAM** | Resistive Random-Access Memory |
| **DNA** | Deoxyribonucleic Acid |
| **ALU** | Arithmetic Logic Unit |
| **ASAP** | Arizona State Predictive |
| **PDK** | Process Design Kit |
| **APR** | Automated Place and Route |

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# CHAPTER 1

# INTRODUCTION AND MOTIVATION

From tiny electronic commodities to supercomputers, the electronics revolution we are witnessing today is enabled mainly by computer chips' continuous miniaturization. This miniaturization has been driven by the ability to scale digital CMOS. However, continuing scaling with 2-D CMOS, the underlying framework of today's ICs is proving to be very challenging due to device scaling limitations [1] [2] [3], growing interconnection overhead [2], and manufacturing challenges [4]-[6] at the nanoscale. Today, the beyond CMOS research can be categorized into two thrusts: a) new device and circuit, b) extension of CMOS in 3-D.

Towards that goal, the major industrial push has been with the wafer to wafer [7], die to die [7], and layer to layer [7] 3-D integrations, where individual wafer/die/layer is completed separately and joined with other wafers/die/layer either in parallel or sequential manner. While these approaches show some density gains, they inherit 2-D CMOS's challenges; despite having a higher total number of devices, connectivity constraints limit integration density. This scenario is evident because transistor-level monolithic 3-D, the most advanced 3-D IC technology in terms of integration density, can only achieve 40% area benefits compared to 2-D CMOS. In addition to connectivity, reliability degradation is also a significant challenge faced by these technologies.

Moreover, Thermal management is becoming an increasing concern at the nanoscale due to reduced dimensions of devices, interconnects, and dense integration [2][9][10]. The challenges exacerbate for Beyond-CMOS 3-D IC approaches, such as multi-lithic and monolithic 3-D CMOS [8], which lack intrinsic thermal management capabilities, mainly rely

on expensive system-level approaches such as liquid cooling [11], heat spreader [12], and have huge cost overhead [13]. Moreover, there is no established CAD flow for thermal evaluation of 3-D circuits that can capture nanoscale details (current CAD approaches are at the packaging level).

Additionally, both industry and academic researchers are looking into novel devices and technologies beyond Moore scaling. Examples of such emerging technologies include, but are not limited to, Quantum-dot cellular automata (QCA, [14]), nanomagnetic logic [15], spin-based devices (e.g., spin-wave devices [16] and spin torque majority gates [17]), Quantum Computing [18], plasmonic-based devices [19], neuromorphic computing [20]-[27]. Even though these emerging technologies present new opportunities, thoroughly assessing the feasibility and scalability requires new and specific synthesis flows. These technologies cannot take advantage of the existing software tools in general; either the tools do not have features for handling these technologies, or these novel devices pose some unique characteristics to output efficient circuit designs [28]. For instance, Quantum-dot cellular automata (QCA, [14]) leverages majority (MAJ) and inverter (INV) gates as primitives, Neuromorphic architectures exploit threshold gates, Combinational operations in quantum computing (QC) [29] can be abstracted in terms of libraries of components, such as the Toffoli gate [30], [31] that implements a generalized form of exclusive OR (EXOR) operation [32]. Therefore, extensive research is required to complete computer-aided design methodologies for these nanotechnologies if they are to replace or augment CMOS.

Crosstalk computing a novel computing model that uses deterministic interference between adjacent nanoscale interconnects (Crosstalk) for computing [33],[34]. The computing approach departs from the device switching dependent computing paradigm and relaxes

device scaling requirements. The scalability is determined primarily by circuit scheme, integration, and the ability to pattern smaller metal nano-lines and deposit dielectrics in between them. Crosstalk computing approach is functionally complete and provides vast opportunities for logic reduction [35]-[37]. Moreover, the fabric provides opportunities for reconfiguration at the gate-level [34], which can provide additional benefits for density improvement by resource sharing and can be crucial for fault-tolerance [38],[39]. However, to be a viable alternative to CMOS, Crosstalk computing needs to answer the following question: can the existing materials, device, CAD tools, and manufacturing setup be repurposed for the new computing approach to achieve smaller and more power-efficient computing chips continuously?

In this dissertation proposal, we address the scaling challenges. We show that the Crosstalk computing co-exists with CMOS by i) synthesizing large-scale design using existing EDA tool flow, ii) maintaining density, power, and performance benefits when scaled, iii) demonstrating functional correctness for large-scale design at advanced nodes, and iv) technology realization using existing manufacturing process. We propose manipulating the CMOS synthesis flow by adding two extra steps: conversion of the gate-level netlist to Crosstalk implementation friendly netlist through logic simplification and Crosstalk gate mapping and custom cell inclusion libraries for automated placement and layout. In this paper, we report on the scalability aspects of this technology and show for primitive circuits. Our logic simplification approach for Crosstalk computing shows 11%, 27%, and 32% transistor count reduction compared to the majority synthesis approach and 58%, 62%, and 24% transistor count reduction CMOS based approach, respectively. Our scalability study on the primitive gate, designed in 180nm, 65nm, 32nm, and 7nm technology nodes, reports that the

average reduction in power is 42.5%, and an average improvement in performance is 34.5% compared to CMOS for all mentioned nodes. We have also shown the implementation of three large-scale circuits from the MCNC benchmark and compared density, power, and performance results for CMOS at 7nm. Our results show significant benefits over CMOS; for the best case, there is a 62% reduction in density & power and 53% improvement in performance, respectively. Our experimental validation of the Crosstalk proof of concept chip validates that existing manufacturing flow can be used.

The dissertation proposal also presents a detailed thermal modeling approach for emerging technology, especially emerging transistor-level 3-D integrations, which is unique and a fine-grained approach that considers material properties, nanoscale effects, 3-D circuit style, and 3-D layout details. We have also proposed detailed physical fabric-level heat management features applicable for all transistor-level 3-D integration approaches and showed their effectiveness through modeling and simulations. Key contributions of this proposal include:

(i) **Logic Simplification approach for Large Scale Crosstalk Circuit Design:** Detail implementation steps: from complex Boolean function to simplified Crosstalk circuit friendly expression, manipulation of the CMOS synthesis flow, use other existing tools, taking advantage of the compressibility feature of Crosstalk, benchmark the outcome with other existing tools.

(ii) **Crosstalk Computing Scalability study:** Extensive study on Crosstalk primitive designed at 180nm, 65nm, 32nm, 7nm under different process variation and detail comparison against CMOS counterparts.

(iii) **Large-scale circuit design at 7nm:** Utilization of the primitive gates and design considerations for large-scale circuit implementation and evaluating their performance

under process variations. Examples of large circuits such as cm85a, mux, and pcle from MCNC benchmarking suits and detailed comparison with CMOS at 7nm are given.

(iv) **Experimental validation:** Experimental prototyping is carried out to demonstrate key manufacturing steps and to validate the Crosstalk computing concept

(v) Thermal management for emerging technologies:

a) Details of the proposed physical fabric level thermal management features, including material aspects, dimensions, and their generic application to emerging transistor-level 3-D ICs.

b) Details of our bottom-up FEM thermal modeling approach account for nanoscale materials, geometry, devices, layout, and circuit behavior.

c) FEM-based thermal evaluation of 3-D circuits under different operating conditions.

d) Comparison among different transistor-level 3-D ICs for static and dynamic thermal scenarios.

The rest of this dissertation proposal is organized as follows: Chapter 2 presents an overview of Crosstalk computing and details its working principle. Chapter 3 logic simplification approach for Crosstalk friendly Boolean expression. Chapter 4 and 5 detail the scalability study of Crosstalk primitive gates for different technology nodes and large-scale circuit design methodology at 7nm. Chapter 6 introduces the Crosstalk prototype chip's experimental validation, and Chapter 7 presents benchmarking results and potential application. Details about thermal management and modeling results are presented in Chapter 8.

# CHAPTER 2

# CROSSTALK COMPUTING OVERVIEW

Crosstalk computing leverages interference between closely coupled signals carrying metal lines to do useful computation. The key components necessary for this computation are: a) metal lines and their logic-specific arrangements to drive inputs, b) engineered coupling capacitance between these lines, and c) synchronous clock inputs and one transistor-based scheme to control the output behavior. Figure 2.1 presents an abstract view of a fabric that implements crosstalk computing, where the metal lines are arranged on the top, and the controlling transistors are at the bottom. We intentionally arrange metal lines such that they can interfere in a deterministic manner (Figure 2.1). Then we capture this deterministic interference in a specific timeframe to ascertain logic. Let us use an example of a two-input (*A* and *B*) logic. In Crosstalk, we would drive these inputs in two adjacent metal lines, and in between those lines, we will have another metal line to capture the interference charge (or the

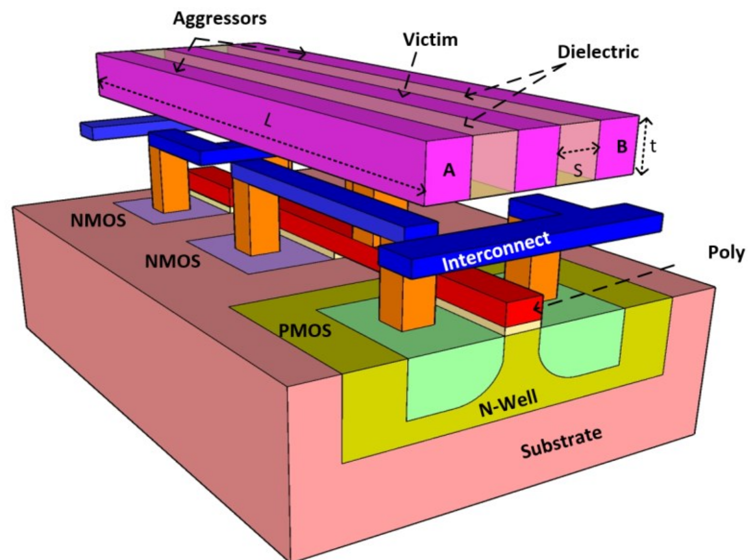


Figure 2.1 Abstract view of Crosstalk fabric. Coupling capacitances will be on the top denoted as ‘dielectric’ in between nano-metal lines denoted as ‘aggressor’ and ‘victim’.

output). In interconnect terminology, the driving inputs would be called Aggressors. The interference capturing line would be called the Victim (*Vi*). For capturing interference, the victim would be intentionally kept floating (not connected to the power supply or ground). As the aggressors' transition from 0 to 1 or 1 to 0, corresponding interference would result in voltage gain or drop in the Victim node. If any of the input transitions (*A* or *B*) from 0 to 1 results in a sufficiently high voltage induction in the victim, we would achieve OR logic, and if only when both *A* and *B* transitions from 0 to 1, we notice high voltage induction in victim node, we would call the metal arrangement as performing AND logic.

To capture the behavior in circuits for large-scale integration, we utilize a control transistor and a clock. With the help of the control transistor, we periodically preset/sink the Victim node to the ground and deterministically keep the Victim node floating (ready for charge induction) during logic computation. An inverter is attached to the victim node is required to achieve a complete voltage swing for the following stages. Fundamentally though, the logic computation happens due to the interference between interconnects and without the help of the transistor.

### *2.1 Crosstalk Primitive Gates*

An example of primitive gates along with their simulation results is shown in Figure 2.2. The schematic for Crosstalk AND and OR gates are shown in Figure 2.2i&iii. From Figure 2.2i&iii, it can be seen that both logic gates have a similar circuit configuration, with the only difference in their coupling capacitances. The coupling capacitances dictate different logic behavior by having less or more strength. Coupling strengths are denoted by $C_{NR}$ & $C_{ND}$ for

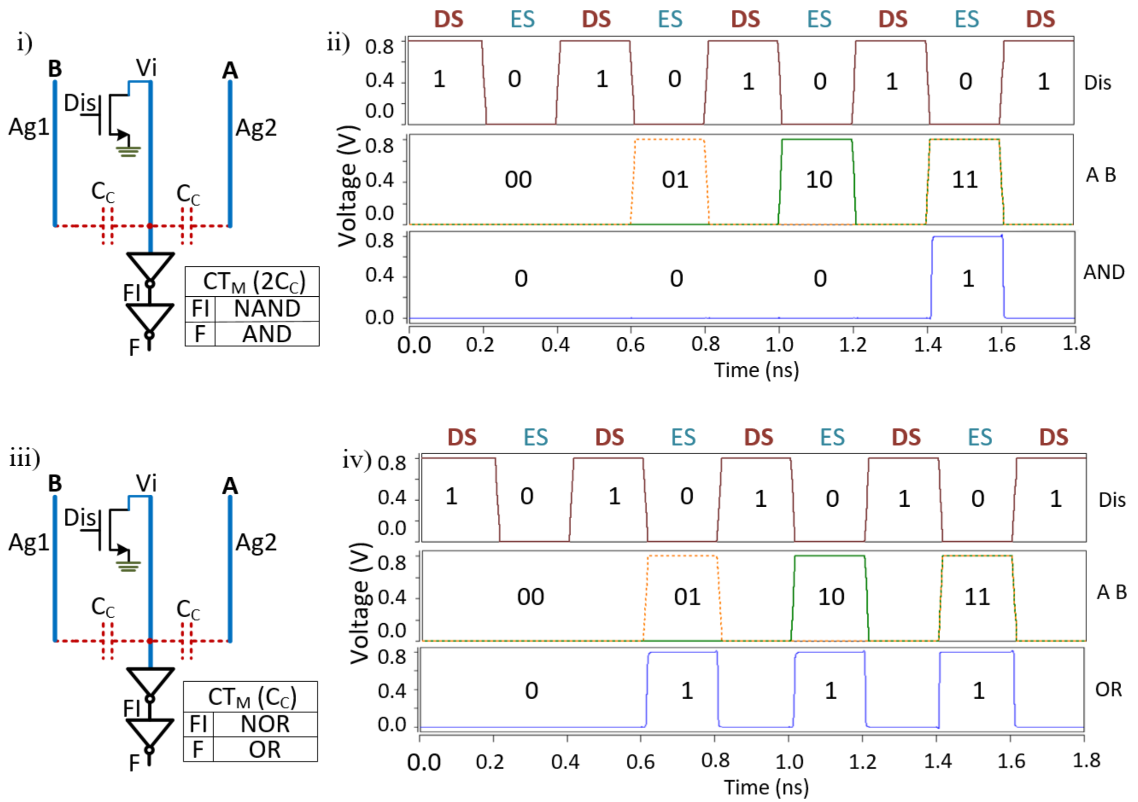


Figure 2.2 Crosstalk primitive gates (AND and OR). i) AND schematic, ii) Simulation results of AND gate, iii) OR schematic, iv) Simulation results of OR gate.

OR and AND gate, respectively. The OR gate coupling is greater than the AND gate, i.e., $C_{NR} > C_{ND}$, which ensures that 0 to 1 transition of either *A* or *B* or both results in logic 1.

Figure 2.2ii&iv shows the simulation results of the AND & OR Crosstalk logic gates. All the input signals along with the discharge signal were 0.8V. The circuit operates in two states, the Discharge state (when the victim node is connected to ground, DS) and the Evaluation state (when the victim is disconnected from power supply or ground and ready for capturing interference, ES). Figure 2.2ii shows the simulation response of an AND gate where the first row (from top to bottom) shows the discharge signal (*Dis*), the second row shows two input signals (*A* and *B*) with 00, 01, 10, and 11 combinations given Evaluation states, respectively. The third row shows the output response of the AND gate. For all the circuits,

the $F_I$ node gives inverting logic output (NAND, NOR, etc.), and the $F$ node gives a noninverting logic output (AND, OR etc.). For input combinations 00, 01, and 10, the output response is logic 0. However, for inputs 11, the output is logic 1, which shows AND behavior.

Similarly, OR gate implementation is shown in Figure 2.2iii, and the simulation response is shown in the 4$^{th}$ row (top to bottom) of Figure 2.2iv with the same input combination as AND gate. The difference between AND and OR gate is that the coupling strength for the OR gate is higher than the AND gate. We can see that when *Dis*=1, irrespective of the input state, the output becomes logic '0'. However, during Evaluation States (*Dis*=0), if there is 0 to 1 transition of either A or B or both, the output becomes logic '1'. It can also be observed from the four panes that the Victim node is discharged to 0 before every new logic computation (or inference capture).

Since NAND/NOR are universal gates (can be used to implement any logic), the Crosstalk logic is functionally complete and can be used to implement any large-scale designs. Moreover, the simplicity of logic implementation through signal inference also implies that more complex logic can be implemented without requiring multiple cascading stages.

### *2.2 Crosstalk Circuits Based on Coupling Weight*

Many complex logic functions can be achieved by assigning different coupling capacitances (equal or unequal) among the input aggressors and increasing input fan-in. Based on this principle, two different circuit styles are applied; homogeneous Crosstalk logic gates where aggressors are equally coupled and heterogeneous Crosstalk logic gates where aggressors are unequally coupled. Crosstalk Heterogeneous and Homogenous gates, i) Heterogeneous gate: AO21 ($F$= AB+C), ii) Simulation results of AO21, iii) Homogenous gate,

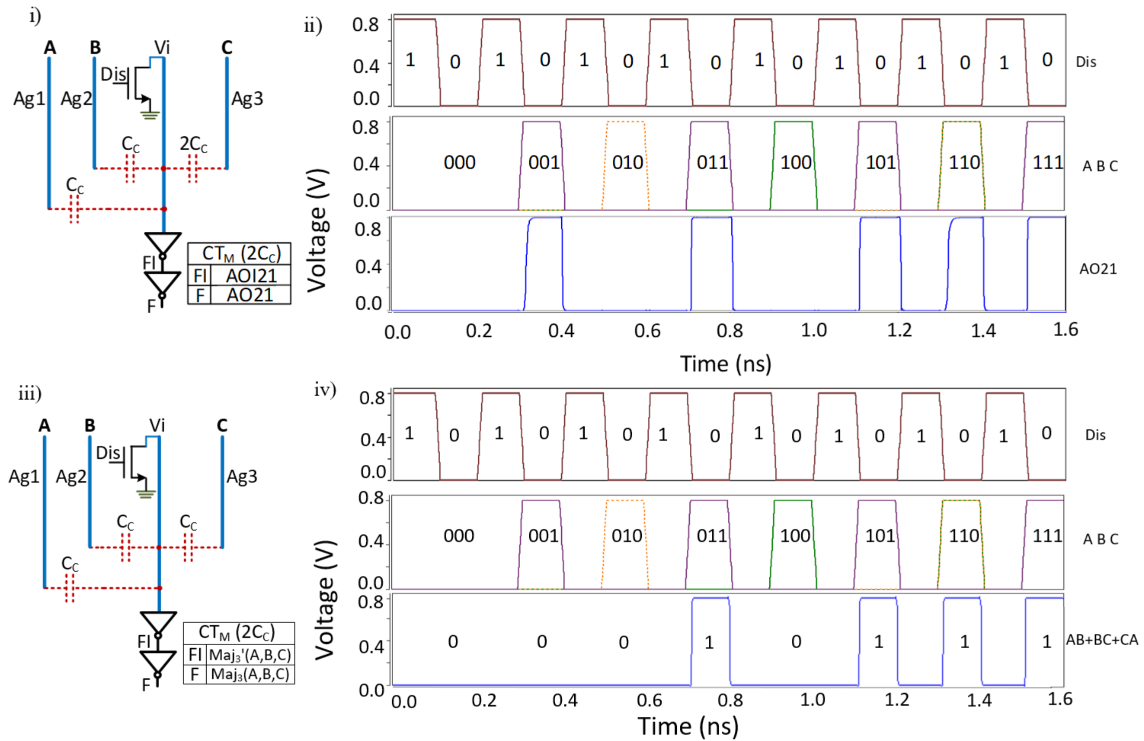


Figure 2.3 Crosstalk Heterogeneous and Homogenous gates, i) Heterogeneous gate: AO21 (*F*= AB+C), ii) Simulation results of AO21, iii) Homogenous gate, *F*=AB+BC+CA, iv) Simulation results of function *F*.

*F*=AB+BC+CA, iv) Simulation results of function *F*. shows the implementation of Crosstalk homogeneous and heterogeneous logic gates with three input fan-ins. Crosstalk Heterogeneous and Homogenous gates, i) Heterogeneous gate: AO21 (*F*= AB+C), ii) Simulation results of AO21, iii) Homogenous gate, *F*=AB+BC+CA, iv) Simulation results of function *F*.(i&ii) shows the implementation of heterogeneous Crosstalk gate, AO21 (AND-OR), i.e., F= (AB+C), where varying coupling capacitances between the aggressors achieve the functionality. Crosstalk Heterogeneous and Homogenous gates, i) Heterogeneous gate: AO21 (*F*= AB+C), ii) Simulation results of AO21, iii) Homogenous gate, *F*=AB+BC+CA, iv) Simulation results of function *F*.(iii&iv) shows the example of homogeneous Crosstalk logic. Carry function, F = MAJ3 (A, B, C) = AB +BC+CA is achieved by keeping the same coupling strength among the input aggressors. Noticeably, when we have homogeneous

functionality with multiple inputs, this has some similarity to Majority logic which means output is 1 when any of the two inputs or all three inputs are 1.

The first-row shows *Dis* pulse (from top to bottom), the second row shows the three input signals, *A*, *B,* and *C*, feeding all input combinations from *000* to *111* in Evaluation State states (i.e., when *Dis=0*). The third row shows the simulation responses of Crosstalk *AO21* gates. This behavior is achieved by giving weighted/heterogeneous couplings to the input aggressors. One input has a stronger capacitance, in this case, input *C,* than the other two. Logic expression of *AO21 (AB+C)* evaluates to 1 when either *AB* or *C*, or both are 1. That means the output is biased towards the input *C*; the output is *1* when *C* is *1* irrespective of *A* and *B* values. Therefore, input *C* has twice the coupling capacitance than *A* and *B*.

In contrast, for the *Majority* function *(AB+BC+CA)*, the output is not again biased towards any input. Instead, all inputs will get equal coupling, i.e., for output to be *1*, any two inputs should be *1*. Crosstalk Heterogeneous and Homogenous gates, i) Heterogeneous gate: AO21 (*F*= AB+C), ii) Simulation results of AO21, iii) Homogenous gate, *F*=AB+BC+CA, iv) Simulation results of function *F*.iv shows the simulation responses of the *Majority* gate, satisfying the logic for all input combinations (*000* to *111*).

# CHAPTER 3

# LOGIC SIMPLIFICATION APPROACH FOR CROSSTALK CIRCUIT DESIGN

The fast evolution of computing technologies has been enabled by extensive knowledge on how to represent and manipulate Boolean logic functions and how to optimize their realization. Logic synthesis is a crucial component of digital design. Logic functions are often extracted from high-level models or specialized hardware languages (e.g., VHDL). Their optimization is crucial to achieving practical implementations [32]. Traditionally for CMOS technology, logic reduction methods always convert Boolean functions into the simplified sum of products (SOP) or product of sums (POS) expressions, and logic circuits are implemented using AND and OR gates [40]. However, beyond CMOS, technologies cannot be simplified using existing EDA tools due to their enhanced functionality over standard FET switches [41]. Most of the emerging technologies require dedicated synthesis technology; for example, QCA, spin-wave circuits require majority logic synthesis, whereas double-gate silicon nanowire FETs [42], carbon nanotube FETs [43], graphene FETs [44], [45], and organic FETs [46] a Logic switch driven by a comparator [47].

## *3.1 Formal Synthesis Methods*

Traditional CMOS design, logic compression methods always convert Boolean functions into the simplified sum of products (SOP) or product of sums (POS) expressions. The circuits are implemented using primitive cells like AND and OR gates based on these SOP or POS expressions [40]. To prove the properties of the formal specification, two core reasoning engines are prevalent in formal methods: binary decision diagrams [48] and Boolean

satisfiability [49]. The tools recursively use Shannon's expression to decompose any Boolean function into simplified expression. From a logic circuit perspective, Shannon's expansion is equivalent to a 2:1 multiplexer (MUX), which is the logic primitive driving binary [48].

### *3.2 Majority Network-Based Synthesis*

Figure.5.1 In emerging technologies like QCA, Spin-Wave Device, RRAM, DNA Logic [50], with different basic operations regarding traditional CMOS, it is desirable to express the Boolean functions through the essential logic elements of this technology [51]. The majority function is a three-input function where output is logic 1 when at least two inputs are at logic level 1. The majority-based logic synthesis goes way back to the 1960s with the works of Akers [52], Miller and Winder [53], and Muroga [54]. However, these works are only suitable to synthesize small circuits by hand. In [55], Zhang et al. proposed a majority-based implementation for a selected set of 13 Boolean functions with three inputs representing all possible 3-input functions. However, Majority-inverter graphs (MIGs) [47] use majority and inverter gates to represent majority-based logic and show promising benefits.

### *3.3 SIS Tool*

The SIS is an interactive tool for synthesizing and optimizing sequential and combinational circuits [56]. It can serve as a framework for testing various algorithms. After reading a circuit, SIS processes it. By inputting the proper commands, SIS can state minimization, state assignment, technology mapping, timing optimization, decomposing the Boolean logic network, and so on. After the circuit is processed, a library file containing all the logic devices used during the mapping step is read. The circuit can be mapped to the given devices using the commands given in the SIS tool. SIS can output the synthesized circuit in

any of the circuit formats [57].

### *3.4 Crosstalk Computing Logic Simplification*

To implement a multi-level logic function in Crosstalk, two different circuit styles are followed: homogeneous and heterogeneous. In homogenous circuits (discussed in an earlier section), the coupling capacitance between input and output nets is equal. In contrast, in heterogeneous, the capacitances are unequal. Crosstalk circuits use these homogeneous and heterogeneous Crosstalk circuits as primitive cells with other basic gates like AND/OR. Due to the innovation in circuit style and the physical principle of Crosstalk computing, the traditional synthesis flow for large circuits is not directly applicable.

Majority logic, where the summation of signals determines logic output through thresholding function, can resemble Crosstalk's logic principles. However, existing majority synthesis approaches in the literature mainly concentrate on Quantum Cellular Automata technology where primitive cells are only inverter and majority gates [40], [57], [58]. Though some benefits can be obtained using majority synthesis methods, fundamentally, obtaining simplified expressions for Crosstalk circuits requires a different approach that utilizes fabric's native functionalities.

We propose in this paper, Crosstalk implementation friendly logic simplification approach that takes advantage of both the CMOS and majority synthesis methods for simplified Boolean expressions. First, we take an arbitrary network in Verilog form and use Cadence Genus Compiler [59] to generate a netlist of the network with logic constraints (e.g., limit the tool to use NAND/NOR, AOI, OAI gates only) to benefit from Crosstalk implementations. Then the

netlist is converted to Boolean expressions and fed to the SIS [56] tool to obtain 3-input Boolean expressions.

### *3.4.1 Overview of The Proposed Logic Simplification Methodology*

In this section, we introduce our simplification approach for Crosstalk circuit-friendly expression and detail implementation steps. We take advantage of Crosstalk's compressibility feature through custom logic, CMOS logic, Majority logic and explain in our approach that how we can combine all of them to obtain the best result.

Figure 3.1 gives a flow diagram of the Crosstalk logic synthesis methodology. Our process starts with having a Cadence RTL Compiler that generates a netlist from Verilog code with constraints such that the netlist use gates like NAND, NOR, AOI, or OAI Crosstalk friendly. It is noticeable though we cannot constrain the tool to use majority gates (AB+BC+CA) or other heterogeneous logics that are especially suitable for Crosstalk computing. Because of

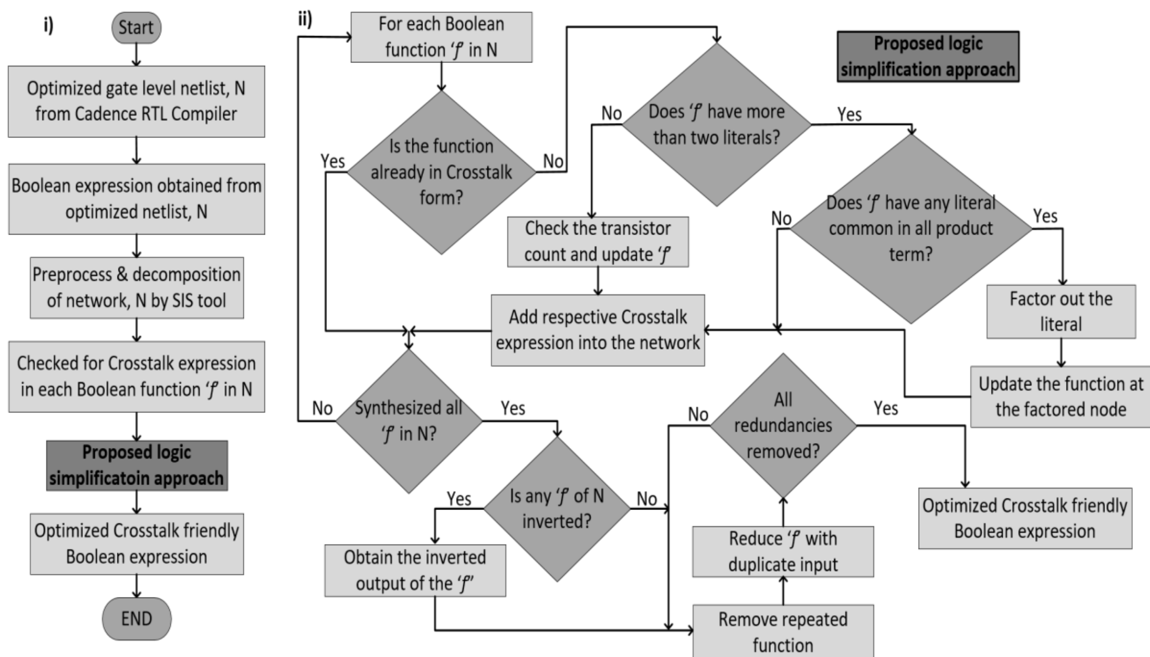


Figure 3.1 Overview of proposed logic simplification methodology. i) Top-level simplification approach, ii) Detail steps of proposed logic simplification approach.

this, after obtaining the netlist from the Cadence tool then we convert it back to Boolean expressions and feed it again through the SIS tool such that the SIS tool already works on an optimized Boolean expression and further tries to simplify it in terms of majority gates (Figure 3.1(i)). The new expression already has majority expressions and some custom expressions which can be implemented using universal gates like NAND/NOR gate. However, we look for further opportunities for simplification as given in Figure 3.1(ii) to get expressions for heterogeneous logic. If the heterogeneous logics cannot be found, we use Crosstalk NAND/NOR gate and complete the Boolean expression. Finally, we obtain an expression that can be converted into a structural netlist. A structural netlist can be used in conjunction with cell libraries to obtain complete layout and parametric results like area, power, and performance.

Figure 3.2 represents the pseudo-algorithm of our simplification approach. We check for each function of the network to be simplified as Crosstalk friendly expression. Variables that are used in the algorithm are defined as follows:

| | |
|---|---|
| $f_1, f_2, f_3$ | A function in network N |
| $S$ | Set of Crosstalk homogeneous & heterogeneous function |
| $f_n$ | Fan-in to network N |
| $S'$ | Inverted Crosstalk homogeneous & heterogeneous function |
| $l_i$ | The $i^{th}$ literal in the expression for function $f$ |
| $p_j$ | The $j^{th}$ product term for function $f$ |
| $n_l$ | No. of literals in function $f$ |
| $T$ | No. of the transistor in the function |

| | |
|---|---|
| $I$ | No. of the inverter in the function |
| $f_{dm}$ | Function $f$ after applying De Morgan's Law |

The corresponding pseudo algorithm takes in preprocessed and decomposed networks as input and returns a more simplified network that is Crosstalk friendly. After preprocessing and decomposing, each function $f$ of the network N is checked to determine whether the function $f$ is in homogeneous or heterogeneous Crosstalk form. If so, we proceed to simplify the next function. Otherwise, as shown in Figure 3.1(ii), we check to see more than two literals in the function. If there exist only two literals in the function, we check for transistor count. First, we calculate the number of transistors needs to implement function $f$. Then, we take an inverted function ($f_x$) of $f$ and calculate the required transistor. If the transistor count for $f_x$ is lower than the original function f, we update the function with $f_x$. For example, consider a function $f=a+b'$. Crosstalk mapping would require seven transistors, including an inverter for literal '*b*' to map the function f. However, inverted function $f' = f_x = (a'b)'$ would require only five transistors. If there are more than two literals present in the function, we look for any common literal present in all the product terms of the function. If a common literal exists, we factor out this literal and map with heterogeneous Crosstalk circuits. Consider, function $f = bc + ca$. If we are to map crosstalk gates directly, it will take three Crosstalk gates.

In contrast, if we factor out the common literal '*c*' from both product terms, function f, therefore, can be presented as $f = cf_1$, where $f1 = (b+a)$, thus requiring only one Crosstalk gate. If there are no common literals, we check whether all the functions are synthesized or not. After simplifying all the functions in the network N, we further investigate any function in an inverted form. If so, by using Crosstalk fabric inherent feature, we can save an additional

inverter required to make function $f$ inverted. The final process is to remove all the redundancies if exist, otherwise terminate. For redundancy removal, we follow the procedure

**Input:** Optimized Network $N$
**Output:** Crosstalk expression corresponding to $N$
begin
**1** Convert the netlist to Boolean expression
**2** Preprocess and decompose network $N$ by SIS
**3** **for** each $f$ in $N$ **do**
**4** **if** $f \notin S$ **then**
**5** **if** $n_l > 2$ **then**
**6** **if** $\exists l_i$ so that $\forall_j, l_i \in p_j$ **then**
$f_1 = f|_{li=1}$
$f = l_i f_1$
**7** **else**
Add Crosstalk expression to the $f$

**8** **else**
//check the transistor count
Count $f_{old} = T+2*I$
Apply De Morgan's Law to function $f$
$f_x = f_{dm}'$
Count $f_{new} = T+2*I$
**9** **If** Count $f_{new}$ < Count $f_{old}$ **then**
$f = f_x$
**10** **else**
Keep the original f and add
Crosstalk expression
**11** **else**
Add Crosstalk expression to the $f$
**12** **if** $f_n$ in $N$ such that $f_n = f'$ **do**
$f_n = S'$ where $S'$ is the inverted form of $S$
**13** **else**
**break**
**14** Do redundancy check
**15** end

Figure 3.2 Pseudo algorithm for Crosstalk logic simplification approach

explained in [57].

Next, we present Boolean expressions of the different networks to explain the flowchart. First, the Boolean expression is obtained from a 4-bit ALU, and later one is the network for the 2-bit multiplier. We represent the Crosstalk functions by denoting as function $X_{gate}(a,b,c)$ where *a,b,c* are the sub-functions, and subscript '*gate*' defines what type of logic the function will be implemented.

*3.4.1.1 First example*

Step 1: Boolean expression obtained from 4-bit ALU:

$((((A_1A_2+A_1B_2')+A_2(B_2'+B_1'))+B_1'B_2')A_3+(((A_1A_2+A_1B_2')+A_2(B_2'+B_1')+B_1'B_2')B_3'+(A_3+(B_0'B_3'))')+A_3B_2B_3'$

Step 2: By using SIS [10] tool to preprocess and decompose, we obtain the following expression,

$$N = f_2 + f_3' + f_5$$

$$f_1 = A_1 + B_1' \quad (1)$$

$$f_2 = A_3B_0'B_3' \quad (2)$$

$$f_3 = A_3B_2B_3' \quad (3)$$

$$f_4 = f_1A_2 + f_1B_2' + A_2B_2' \quad (4)$$

$$f_5 = f_4A_3 + f_4B_3' \quad (5)$$

Step 3: For each function of network N, presented in equation (1)-(5), we check if the function is in Crosstalk homogeneous or heterogeneous form.

- The first function, $f_1$, is neither in homogeneous nor in heterogeneous form. Next,

we find that it has only two literals. Then, we check for fewer transistor counts, which we get after applying De Morgan's law and then taking inverter of the function f. Therefore, the updated function is $f_1$ = ($A_1$'$B_1$)'. Since there are still three other functions to be simplified, we proceed to the following function, $f_2$.

- Function $f_2$ is directly in Crosstalk homogeneous form $X_{and}$(A, B, C). We proceed to simplify the following function.
- Function $f_2$ is also in Crosstalk homogeneous form $X_{and}$(A, B, C). Therefore, we update the function with Crosstalk homogeneous expression and check if there is any other function to be simplified.
- Function $f_4$ is in the Crosstalk homogeneous form Xhomo(AB+BC+CA), so we update the function with the Crosstalk homogeneous gate.
- Function $f_5$ cannot be mapper with heterogeneous or homogeneous form. Next, we check to see if the function has any common literals. We find that $f_4$ is the common literal in both of the product terms of function $f_5$. Therefore, we factor out the common term and update the function as $f_5$ = ($A_3$+$B_3$') $f_4$, which is in Crosstalk heterogeneous form $X_{hetero}$((A+B)C).
- Next, we proceed to simplify other functions.
- From equation (1), we can see that both function $f_2$ and function $f_3$ have common literals $A_3B_3$' between them, which we can factor out and get the expression as $A_3B_3$'($B_0$'+ $B_2$)+$f_5$. $A_3B_3$' term can be obtained by Crosstalk AND gate, which we can map with ($B_0$'+ $B_2$) to get Crosstalk heterogeneous form.

Step 4: Update the node function for inverted output. We check if there is any function in an inverted form. If so, we can avoid additional inverter using the Crosstalk fabric feature, which can apply to the literal $f_3$'.

Step 5: Check for redundant functions and also redundant input to any single function. We have checked and found no redundancy for the first example.

Step 6: Complete the process. Finally, we update the network N with simplified Crosstalk friendly Boolean expression, which is,

$$N=X_{or}(X_{hetero}(X_{and}(A_3,B_3'),B_0',B_2),X_{hetero}(X_{homo}(X_{nand}(A_1',B_1), A_2, B_2'),A_3,B_3'))$$

*3.4.1.2 Second example:*

Step 1: Input an arbitrary network: In a 2-bit multiplier, there are four outputs and four inputs to the network.

$$Y_0 = A_0B_0$$

$$Y_1 = A_1A_0'B_0 + A_1B_1'B_0 + A_1'A_0B_1 + A_0B_1B_0'$$

$$Y_2 = A_1A_0'B_1 + A_1B_1B_0'$$

$$Y_3 = A_1A_0B_1B_0$$

Step 2: By using the SIS [52] tool to preprocess and decompose, we obtain the following expression:

$$Y_3 = Y_0A_1B_1 \quad (1)$$

$$Y_2 = f_1B_1 \quad (2)$$

$$Y_1 = f_2 A_1 + f_3 \quad (3)$$

$$Y_0 = A_0B_0 \quad (4)$$

$$f_1 = A_0'A_1 + A_1B_0' \quad (5)$$

$$f_2 = A_0'B_0 + B_0B_1' + A_0'B_1 \quad (6)$$

$$f_3 = A_0\,A_1'B_1 \quad (7)$$

Step 3: For each function of network N, presented in equation (1)-(7), we have to check if the function is already in Crosstalk's homogeneous or heterogeneous form.

- First function $f_1$ is neither in homogeneous nor in heterogeneous form. Next, we check to see if the function has any common literals. We find that $A_1$ is the common literal in both of the product terms in function $f_1$. Therefore, we factor out the common term and update the function as $f_1 = (A_0'+B_0')\,A_1$, which is in Crosstalk heterogeneous form $X_{hetero}((A+B)C)$. Next, we proceed to simplify other functions.
- Function $f_2$ is directly in crosstalk homogeneous form $X_{homo}(ab+bc+ca)$. Therefore, we update the function with the Crosstalk homogeneous gate and check whether all the functions are simplified.
- As function $f_3$ is also directly in Crosstalk homogeneous form $X_{and}(ABC)$ and there is no other function left to be simplified, we move on to step 4.

Step 4: Update the node function for inverted output. We check if there is any function in an inverted form. If so, we can avoid additional inverter by using the Crosstalk fabric feature. We have found no function to be in inverted form.

Step 5: Check for redundant functions and also redundant input to any single function. We have checked and found no redundancy in the simplified network.

Step 6: Complete the process. Finally, we update the network N with simplified Crosstalk friendly Boolean expression.

$Y_3 = X_{and}(Y_0,A_1,B_1)$ (1)

$Y_2= X_{and}(X_{hetero}(A_1,A_0',B_0'),B_1)$ (2)

$Y_1= X_{hetero}(X_{and}(A_0,A_1',B_1),X_{homo}(A_0',B_0,B_1'),A_1)$ (3)

$Y_0 = X_{and}(A_0,B_0)$ (4)

$f_1 = A_0'A_1 + A_1B_0'$ (5)

$f_2 = A_0'B0 + B_0B_1'+ A_0'B_1'$ (6)

$f_3 = A_0 A_1'B_1$ (7)

*3.5 Section Summary*

We have presented a logic simplification approach for large-scale Crosstalk circuit integration. We have simplified different Boolean networks like complex logic networks obtained from 4-bit ALU, Multiplier, Adder, and three MCNC benchmark circuits. The logic simplification approach presented in this work is a vital step towards the full-scale synthesis of Crosstalk circuits leveraging existing EDA tools

# CHAPTER 4

## CROSSTALK COMPUTING SCALABILITY STUDY: FROM 180NM TO 7NM

The scaling of integrated circuits so far has been majorly driven by transistor shrinkage. However, sub 10 nm, the scaling has been challenging, and the road map beyond 3nm is uncertain. Alternately, reducing the number of transistors needed to implement a given functionality can also offer denser circuits, thus help to push the scaling trend (Moore's Law). The CMOS is the prevalent circuit style for digital circuit implementation because of its robustness and reliability [60], which are also the reasons for their easy adaptation to advanced technology nodes. Nevertheless, the complementary nature of these circuits demands more number transistors. Many circuit techniques [60] that reduce the transistor count of logic-gates, in turn, performance, and power, are also available in the literature. However, they lack much practical application because of their inferior quality in terms of robustness and reliability. Therefore, for any new circuit style or emerging device-circuit-and-process technology to compete or co-exist with CMOS, it has to be scalable to advanced technology nodes and pass specific quality tests. The other challenges that the current CMOS-based implementations face, besides transistor shrinkage, are interconnected bottleneck and Crosstalk [61]-[63]. Crosstalk Computing, utilizing CMOS transistors and processes, proposes an alternative paradigm that emphasizes circuit design and integration. Our benchmarking shows that 2-5x density benefits are possible over CMOS with improved power at the same node through design. Although the prospects are promising, one may question how variability and signal integrity challenges (which qualify the Quality of the circuits) can be passed by a technology that relies on noise for computation. To answer this question, we

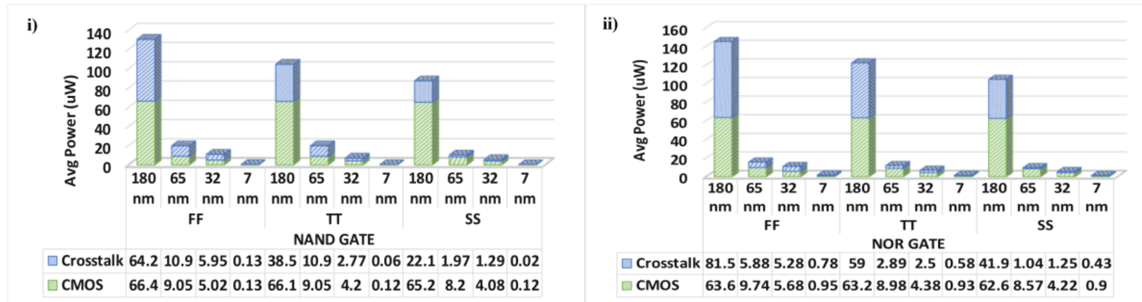

Figure 4.1 Impact on power of Crosstalk and CMOS in advanced nodes for all process corners. i) NAND Gate, ii) NOR Gate

first discuss Crosstalk-Computing's circuit aspects and then detail the design constraints. In this paper, we report on the scalability aspects of this technology and show for primitive circuits how the circuit properties evolve from one node to other. We also present comparison results for several benchmarking circuits. Some significant results are: for primitive NAND gate, designed in 180nm, 65nm, 32nm, and 7nm technology nodes, the average reduction in power is 30%, and an average reduction in performance is 34.5% compared to CMOS for all mentioned nodes.

### *4.1 Scalability Aspects of Crosstalk Circuits*

For any new emerging technology to compete/co-exist with CMOS, scalability study is one of the critical requirements. As a part of the scalability study, Crosstalk logic gates are designed using 180nm, 65nm TSMC PDK, 32nm PTM model, and 7nm ASAP PDK [64]. We

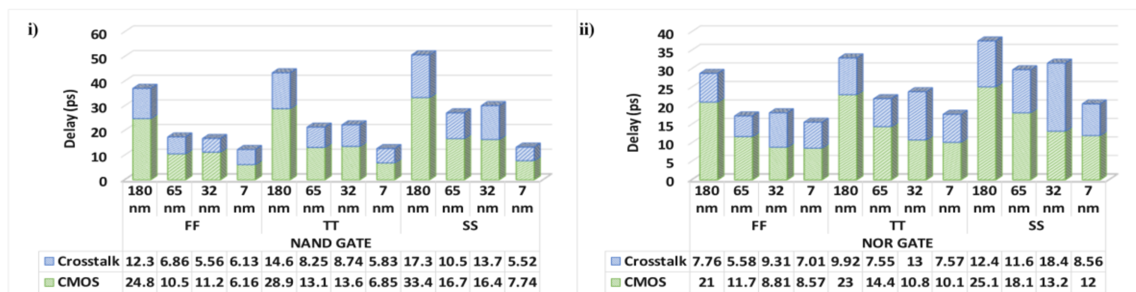

Figure 4.2 Technology scaling impact on the performance for Crosstalk and CMOS primitive gates with process variation. i) NAND Gate, ii) NOR Gate.

have designed primitive gates for both Crosstalk and CMOS in all four nodes and analyzed power and performance under various process variations. In Crosstalk computing, inverter and discharge transistors are technology dependent. Our results indicate that devices with a better $I_{ON}/I_{OFF}$ ratio and lower supply voltage contribute to lower power (Figure 4.1) and better performance (Figure 4.2) for Crosstalk circuits compared to CMOS under process variations. From Figure 4.1, it can be seen that both CMOS and Crosstalk NAND & NOR gate show reduction in power; however, Crosstalk gates show ~30% less power than CMOS gates for all the technology nodes. The improvement in power for Crosstalk gates is less active, leading to lower overall load/switching power and less cell internal power (because of fewer device dissipations and parasitics power). Figure 4.2 shows show the delay of Crosstalk and CMOS gates for various process corners. There is an average improvement of 34% in performance for Crosstalk gates compared to CMOS for all technologies for typical process corner. As shown in Figure 4.2(i&ii), the performance is the worst for the slow process corner due to slow PMOS and NMOS devices.

In contrast, for the FF corner, the performance is the best due to the fast-active devices. Such performance improvement in Crosstalk circuits is due to the absence of any series-connected transistors in Pull-up and Pull-down branches (inverter), leading to shorter RC

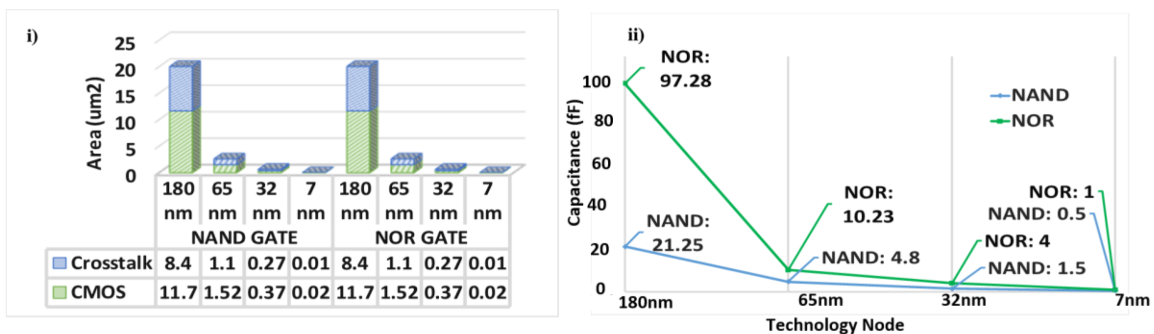

Figure 4.3 Technology scaling impact on the i) area and ii) Coupling Capacitance.

paths from VDD/GND to the gates' output and also lower gate internal parasitics. Moreover, reliance on signal interference for computation and 3-D layout scheme, fewer transistors required for implementing complex function maximizes the density gain for Crosstalk over CMOS counterparts, as shown in Figure 4.3i. Additionally, our results suggest that the input coupling capacitances of Crosstalk circuits reduce with the advanced/smaller technologies (Figure 4.3ii) because of the reduction in gate capacitance of transistors and their lowered threshold voltages.

### *4.2 Section Summary*

In this paper, we have shown that Crosstalk circuits can be designed at different technology nodes. Our results show significant improvement in density, power, and performance for Crosstalk circuits compared to CMOS even with scaling down technology nodes.

# CHAPTER 5

## DESIGNING LARGE-SCALE CIRCUITS IN CROSSTALK AT 7NM

Like any other emerging technology, scalability study is also an essential requirement for Crosstalk computing. However, to thoroughly assess the effectiveness of any new design methodologies at advanced technology node, a standard process design kit (PDK) with the complete set of collateral necessary for schematic entry, layout, design rule checking, parasitic extraction, transistor-level simulation, library generation, synthesis, and automatic placement and routing (APR) is required.

In this paper, we do a scalability study with Arizona State Predictive 7nm PDK (ASAP7) [64]. ASAP7 PDK comes with predictive technology models for transistors and design collaterals, including libraries and technology files required by the CAD tools. Through worst-case process variation analysis, we demonstrate that even at sub 10nm, Crosstalk logic gates function properly. Using these primitive logic gates, we designed larger circuits like cm85a, mux, and pcle from the MCNC benchmark suite [65] and compared the results with CMOS at 7nm. Our comparison results show 59%, 62% and 23% reduction in transistor count for cm85a. mux and pcle circuits, respectively. Our simulation results also show potentials for power and performance improvements; on average, the reduction in power and latency/performance was 57% and 10% for the three circuits.

### *5.1 Crosstalk Basic Gates Design at 7nm under Process Variation*

Figure 5.1 shows the example of two primitive cells (NAND & NOR) constructed in Crosstalk fabric. In any logic cell, the underlying principle is to emulate the behavior of aggressor-victim commonly found in interconnects. During logic computation, the victim net (*Vi*) voltage is controlled electrostatically through coupling capacitances between two aggressors (*Ag1* and *Ag2*) and the victim (*Vi*) net. To drive the *Vi* node for the next round of logic evaluation, its voltage is discharged to the ground through a transistor controlled by dis signal after every round of logic evaluation. The dis signal also ensures synchronization with the rest of the circuits. Thus, the *Vi* node is connected to an inverter on one end and connected to the drain side of the discharge transistor on the other end. After every computation, the dis signal will be turned ON to discharge the *Vi* node. Initially, the *Vi* node is kept floating at 0 (because of the previous discharge cycle). When the input transitions in *A* and *B* occur, the

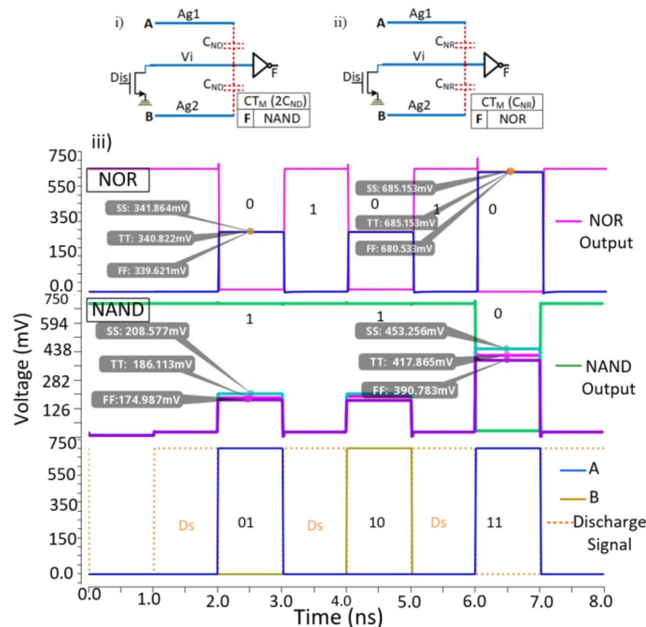


Figure 5.1 Fundamental Logic Gates: i) NAND ii) NOR iii) Simulation results of NAND and NOR gate with *Vi* node voltage under different process variation

output summation charge is induced on *Vi*, which drives the inverter acting as a threshold function. This same principle is used while implementing both NAND and NOR gates with the only difference of coupling strengths between inputs and Vi net. For the NOR gate, the coupling ($C_{NR}$) is stronger than NAND gates ($C_{ND}$). It is chosen such that whenever any inputs or inputs transition (*A* or *B*), the *Vi* node gets the summation voltage 1 (the inverter output receives 0, hence NOR gate).

For NAND, both the inputs need to transition to 1 to receive the summation voltage 1 on the *Vi* node (0 at *F*). HSPICE simulation results validate the Crosstalk principles (Figure 5.1.iii). The inverter connected to *Vi* makes the logic inverted and ensures full swings for fan-outs. The inverter is one of the key components of the Crosstalk fabric that acts as a threshold function that regenerates the signals and restores them to full swing. Figure 5.1.iii also shows that even though process variations impact the victim node voltage (Vi), Crosstalk logic circuits are still able to maintain the functionality by achieving proper output. As discussed in the previous section, if the *Vi* node voltage goes below the switching threshold voltage of 0.3V, the inverter will output logic level '0' and vice versa. Such low switching threshold voltage of the inverter is indeed a key parameter since if the output voltage does not achieve full swing, the inverter will still respond to incoming voltage.

As mentioned, Crosstalk computing fundamentally relies on interference between nodes for computation. However, transistors play an essential role in controlling the interference pattern and ensuring total swing output. Therefore, transistor-related variability challenges persist in Crosstalk. However, the overall effect is lesser due to the fewer number of transistors being used.

### *5.2 Designing Under Variation at 7nm*

Process variation may arise due to various issues and ultimately impact transistor performance. Hence the standard in the industry is to name different process corners as FF (Fast-Fast), TT (Typical-Typical), and SS (Slow-Slow), with the first letter, refers to NMOS, and later one refers to PMOS. By combining FS, FT, etc., other process corners can be obtained; however, FF, TT, and SS are representative of best, nominal, and worst-case scenarios. Fig. 2 shows the effect of process variation on the transfer characteristics curve of an unskewed inverter at 7nm. As shown in Figure 5.2, the inverter has a weak PMOS transistor causing the switching threshold (Vm) to shift more towards zero. In general, the switching threshold voltage is desirable to be equal to exactly half of VDD (0.35V) since this would provide a higher noise margin. For worst-case process variation (SS), Vm moves towards the

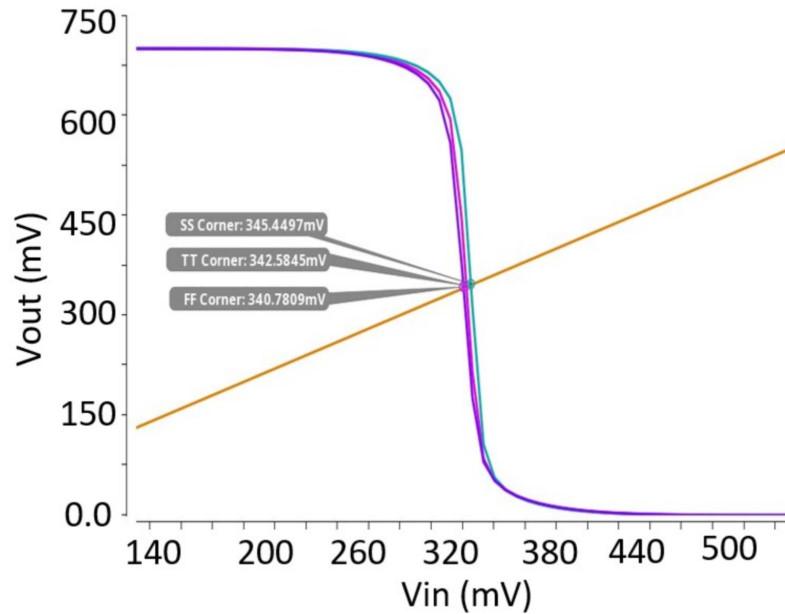


Figure 5.2 Voltage characteristics curve of an Inverter for different process variation.

left (Figure 5.2), increasing the undefined region. An incoming signal with noisy zero value would lead to erroneous values at the output under such conditions.

For Crosstalk computing, with the symmetrical inverter connected to its Vi node, the incoming input value, as can be seen from Figure 5.2, should lie within 0V to 0.33V to have perfect logic '1' at the inverter output. However, to have better noise immunity and balanced drive strength, the width of the PMOS needs to be increased since this would shift the switching voltage towards half of the VDD. The properties obtained from Figure 5.2 from different process corner is beneficial for designing Crosstalk circuits with different fan-ins and indicative of power and performance profile.

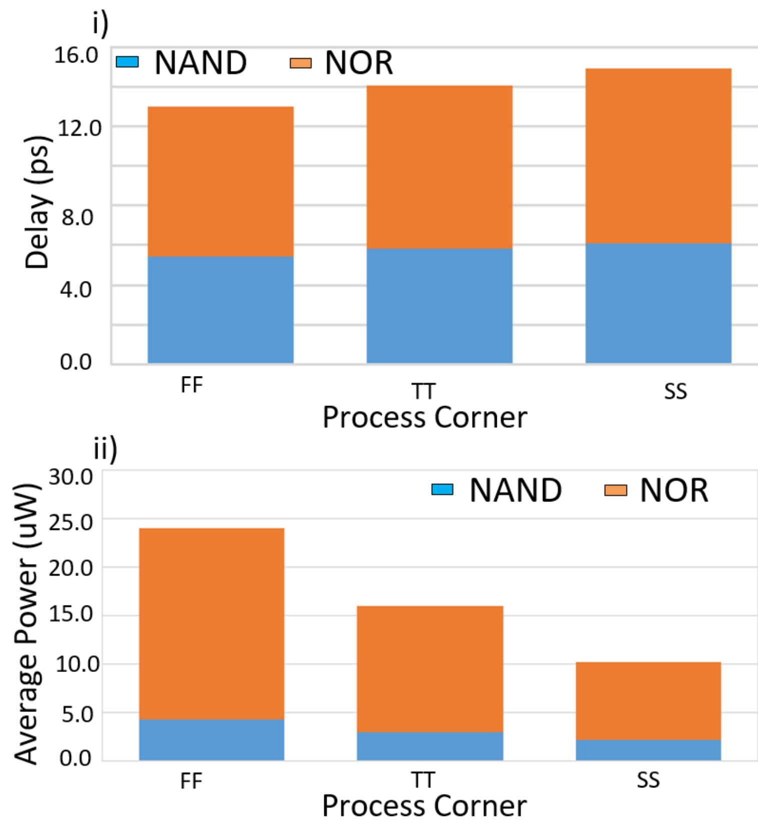


Figure 5.3 Impact of process variation on i) Performance and ii) Average power for CT NAND and NOR Gate

We used the ASAP7nm PDK [64] to evaluate Crosstalk circuits at 7nm. ASAP7 PDK is compatible with industry CAD tools for complete physical verification (Layout design, DRC, PEX, and LVS). The PDK is a 7nm FinFET technology that comes with transistor models having four different threshold voltage levels. The four devices reported in ASAP7 PDK are SLVT, LVT, RVT, and SRAM to decrease drive strength for both NMOS and PMOS transistors. The RVT type NMOS transistor has an Ion of 37.85uA and an $I_{off}$ of 0.019uA, providing an excellent subthreshold swing of 63.03 mV/decade. Similarly, the PMOS transistor also has a similar subthreshold swing of 64.48 mV/decade, having an Ion of 32.88uA and $I_{off}$ 0.023uA. Using these NMOS and PMOS transistors, for an unskewed inverter, a high noise margin is found to be 0.33V and the low noise margin to be 0.3V with switching threshold voltage at 0.34V.

Figure 5.3. (i&ii) shows the power and performance results of Crosstalk NAND and NOR gate at three process corners for PMOS and NMOS devices: SS, TT, and FF. As shown in Figure 5.3.i&ii, the slow transistors result in a slower transition of 5.53ps and 8.77ps for both NAND and NOR gate, respectively, but the functionality remains intact. The delay is minimum for the FF corner, but the power is also highest. The bar graphs show the impact of process variation on performance and power for both NAND and NOR gate, with TT being the nominal case.

### *5.3 Designing Large-Scale Circuits at 7nm*

In the previous sections, we have discussed how different Crosstalk primitive logic cells can be achieved and also shown that these cells can be designed at smaller technology nodes

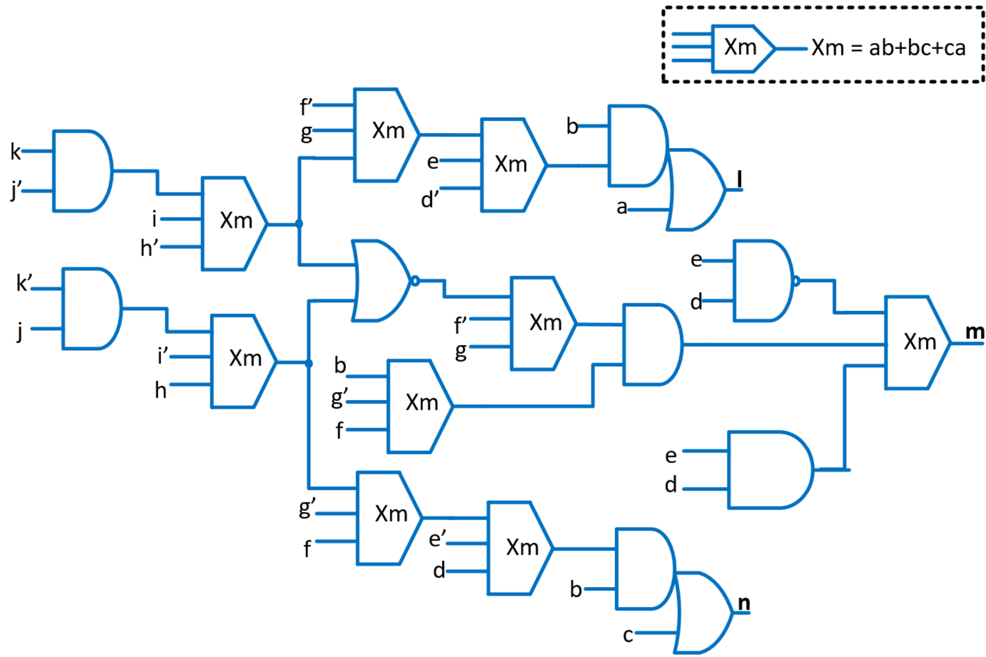

Figure 5.4 Schematic of cm85a circuit

with no functionality issue. This section shows that Crosstalk cells can be connected in a cascaded manner for large-scale circuit design at smaller technology nodes.

Figure 5.4 shows an example of a large circuit implementation of Crosstalk computing using 7nm ASAP PDK. Figure 5.5 shows the simulation results of the circuit. The circuit is the 'cm85a' circuit, one of the benchmarking circuits from MCNC suits [8]. The circuit has eleven primary inputs (a-k) and three primary outputs (l-n), as shown in Figure 5.4. The circuit's netlist is obtained from the MCNC and then further simplified to get Crosstalk friendly netlist according to the process explained in Section 3. More benefits can be achieved when the Crosstalk circuits is implemented in homogeneous ($f= ab+bc+ca$) or heterogeneous manner ($f=a+bc$).

Implementing large circuits using Crosstalk gates requires attention to maintaining signal integrity and drive strength for the following stage gates. These issues can be addressed by

adding an inverter at the end of the victim node. The inverter acts as a thresholding function. If the victim node voltage is below a specific voltage limit, the inverter restores the logic level '0' and vice versa. The strength of the inverter depends on the number of fan-out loads or type of Crosstalk gates it is driving. As shown in Figure 5.4, at the second level, Crosstalk gates drive two fan-out loads of higher coupling capacitances. The inverters are designed as a hi-skewed inverter to avoid the signal drop at the fan-in of the next stage gates.

Another vital issue specific to the Crosstalk circuit is during each evaluation state, the Crosstalk gates need a transition of the input signal from 0 to 1 for correct logic operation. So, if a logic high is retained on the victim node from the previous operation, it leads to logic failure. For example, in Figure 5.4, a Crosstalk-NOR gate, an inverting Crosstalk-logic gate, drives the next stage Crosstalk-homogenous gate, at the third level. During discharge (Ds)

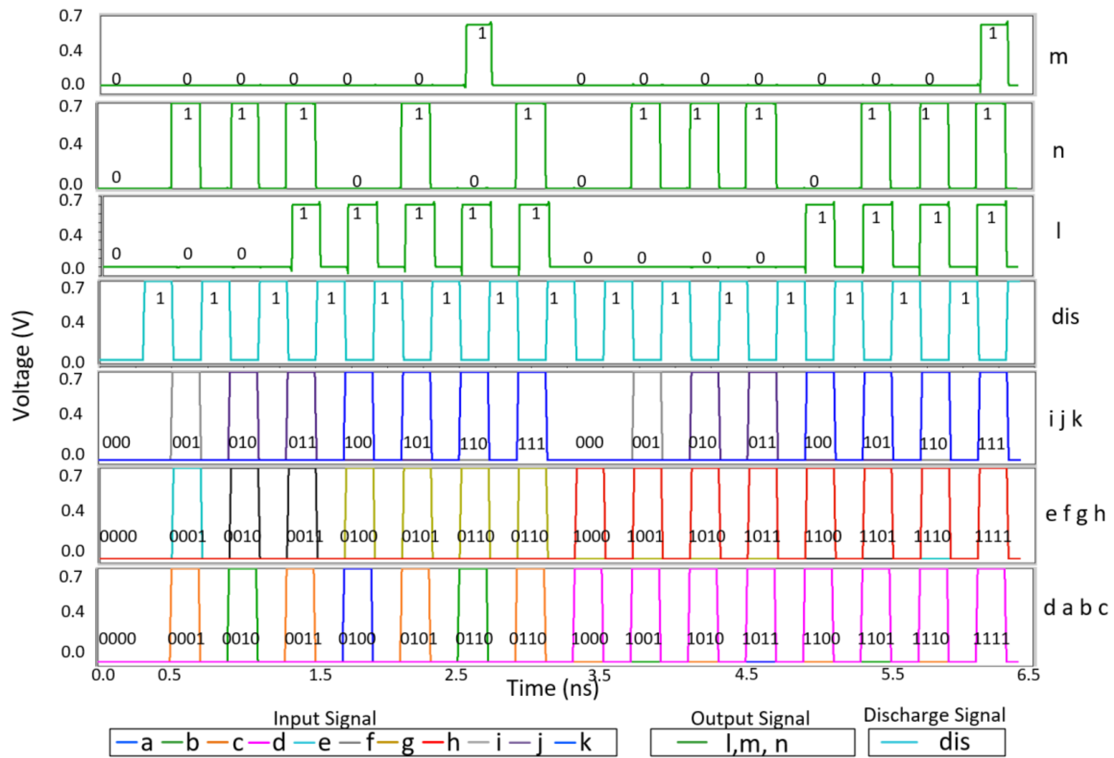


Figure 5.5 Simulation results of cm85a circuit design at 7nm

state, it receives a logic high carried to the following evaluation state, thereby preventing the transition of signal from 0 to 1 leading to logic failure. This issue can be resolved by using a pass-gate-type circuit style. In this type of circuit style, a transmission gate is placed between inverting and non-inverting gate interfaces. During the discharge state, the input signal coming from the aggressor connected to the transmission gate is discharged to the ground. The input signal is passed through the transmission gates in the evaluation stage, creating a signal transition from 0 to 1. For Crosstalk circuits with three inputs, especially for Crosstalk-OR3 gates, high coupling strength is required for proper logic function. This is because the victim node requires more charge accumulation to turn on the inverter connected to it. The inverter has a higher threshold voltage. However, since ASAP7 PDK comes with transistor models with four different threshold voltages, the transistor that requires lower threshold voltage can be used in Crosstalk-OR3 gates to avoid higher coupling.

Additionally, buffers can maintain the signal strength to drive the gates that are far placed. Using the steps mentioned above, the cm85a circuit is implemented. Only three additional buffers were needed, and simulation results in Figure 5.5 show the correct functionality is maintained. As such, any large-scale circuits can be implemented even at smaller technologies using CT-gates in this manner while maintaining correct circuit functionality and achieving improved density, power, and performance benefits.

### *5.4 Section Summary*

In this section, we presented Crosstalk computing's large-scale circuit implementation using Crosstalk at the advanced node. Using ASAP7nm PDK, we have shown that for both best case and worst-case process variations, Crosstalk circuits can be designed to function

correctly, and benefits over CMOS can be achieved. We have also shown the implementation of three MCNC benchmark circuits and compared density, power, and performance results to CMOS at 7nm.

## CHAPTER 6

## COMPARISON AND BENCHMARKING

### *6.1 Comparison of Density Benefit Using Different Boolean Network*

Comparison between the proposed approach and majority-based synthesis approaches [40], [57], [58] is presented in this section. We have simplified different functions, arithmetic blocks, and also three MCNC benchmark circuits [65]. Table 6-1 lists all the results for benchmarks. For CMOS, all the primitive cells are considered, for the majority-based approach, primitive cells are replaced with equivalent Crosstalk gates. For gate count comparison, the inverter is accounted for wherever needed for all three different approaches. Our results show significant improvement in a density benefit with respect to CMOS. The average reduction (R%) in gate count for the CMOS approach is 44%, with the maximum reduction being 77%. For MCNC benchmarks, the average gate reduction is 44%, with the maximum reduction being 58%. This is primarily due to traditional logic reduction approaches

Table 6-1 Comparison of Different Boolean Networks

| Standard Function | I/O | CMOS | | Synthesis using existing method | | Synthesis using proposed method | | R% w.r.t CMOS | | R% w.r.t existing method | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | *Transistor Count* | *Gate Count* | *Transistor Count* | *Gate Count* | *Transistor Count* | *Gate Count* | *Transistor Count* | *Gate Count* | *Transistor Count* | *Gate Count* |
| F=ab+bc+a'b'c' | 3/1 | 30 | 7 | 20 | 6 [40] | 13 | 3 | 56% | 57% | 35% | 50% |
| F=d(c+(b'+a)') | 3/2 | 18 | 4 | 25 | 6 [57] | 12 | 3 | 33% | 25% | 52% | 50% |
| Example1 | 7/1 | 94 | 21 | 62 | 16 [57] | 44 | 11 | 53% | 48% | 29% | 31% |
| **Arithmetic Block** | | | | | | | | | | | |
| Full Adder | 3/2 | 18 | 9 | 17 | 4 [57] | 10 | 2 | 44% | 77% | 41% | 50% |
| 2-bit Multiplier | 4/4 | 56 | 15 | 67 | 17 [57] | 43 | 13 | 23% | 13% | 36% | 23% |
| **MCNC Benchmark** | | | | | | | | | | | |
| cm85a | 11/3 | 264 | 64 | 125 | 31 [57] | 111 | 27 | 58% | 58% | 11% | 13% |
| mux | 21/1 | 404 | 72 | 209 | 49 [57] | 152 | 37 | 62% | 49% | 27% | 12% |
| pcle | 19/9 | 246 | 56 | 276 | 66 [57] | 186 | 42 | 24% | 25% | 32% | 36% |

for CMOS are constrained to use a limited set of standard cell functions, where more complex logic functions are not implemented because of the performance concerns that arise in CMOS logic circuits as they would require long pull-up and pull-down branches of switch (transistor) patterns. We also compared our results with majority-based simplification approaches due to the similarity between logic reduction approaches. The average reduction (R%) in the gate for other majority synthesis approach is 33%, with the maximum reduction being 50%. For MCNC benchmarks, the average gate reduction is 20%, with the maximum reduction being 36%. This is due mainly to majority logic approaches are inefficient in logic reduction as they provide a minimal number of primitive gates (majority-three, majority-five, and inverter). Any logic function needs to be transformed to these gates. However, Crosstalk computing provides holistic logic-reduction opportunities for all the cases due to its ability to effectively implement all three traditional standard cell functions, majority-logic gates, and additional complex functions.

*6.2 Benchmark of Different Large Circuits*

Table 6-2 shows the detailed comparison of density, power, and performance for different circuits between Crosstalk and CMOS technology. For comparison, both Crosstalk and

Table 6-2 Density, Power and Performance for Different Large-Scale Circuit

| **MCNC Benchmark Circuits** | **I/O** | | **Transistor Count** | | | **Average Power (uW)** | | | **Performance (ps)** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | *CMOS* | *Crosstalk* | *CMOS* | *Cross talk* | *%Reduction* | *CMOS* | *Cross talk* | *%Reduction* | *CMOS* | *Cross talk* | *%Reduction* |
| NAND2 | 2/1 | 2/1 | 4 | 3 | 25 | 0.119 | 0.075 | 37 | 7.78 | 5.79 | 25.57 |
| NOR2 | 2/1 | 2/1 | 4 | 3 | 25 | 0.376 | 0.387 | -3 | 6.56 | 8.22 | -25.3 |
| Cm85a | 11/3 | 11/3 | 168 | 69 | 59.00 | 60.63 | 28.95 | 52.25 | 21.10 | 18.93 | 10.28 |
| Mux | 21/1 | 21/1 | 506 | 190 | 62.45 | 73.70 | 29.90 | 59.43 | 9.43 | 12.75 | -35.2 |
| Pcle | 19/9 | 19/9 | 328 | 252 | 23.17 | 288 | 110 | 61.80 | 15.04 | 7.07 | 53.00 |

CMOS circuits are simulated using ASAP7 PDK and keeping nominal VDD at 0.7V. The benefits are significant in all aspects of Crosstalk logic-based implementations. The highest reduction was for the mux circuit in terms of transistor count, and it was 62%. For cm85a and pcle circuits, the reduction in transistor count is 59% and 23%, respectively. Crosstalk circuits show, on average, 58% power benefits over CMOS counterparts. The benefits are primarily due to the reduction in transistor count. For primitive cells, transistor count reduction is 25% for both NAND and NOR gates. However, the reduction in average power for the mux circuit is not much, even though transistor count reduction is maximum compared to other circuits. This is because mux circuit implementation requires many pass-gate type circuit styles circuit, resulting in more switching activities, hence less power reduction.

On the contrary, for the pcle circuit, power reduction is more because it requires fewer buffer and pass-gate type circuit styles that mean less switching activity. The effect can also be seen for performance (Table 6-2), where CMOS technology shows better performance than Crosstalk. However, for cm85a and pcle circuits, Crosstalk circuits have 10% and 53% improvement in performance, respectively.

*6.3 Section Summary*

Our results show significant density benefits over CMOS and majority-based approach; for the best case, there is a 58% and 36% reduction in density over the CMOS-based and majority-based logic reduction approach. The logic simplification approach presented in this work is a vital step towards the full-scale synthesis of Crosstalk circuits leveraging existing EDA tools. We have also shown the implementation of three MCNC benchmark circuits and compared density, power, and performance results with respect to CMOS at 7nm. Our results

show significant benefits over CMOS; for the best case, there is a 62%, 62%, and 53% reduction in density, power, and performance, respectively.

# CHAPTER 7

# EXPERIMENTAL DEMONSTRATION OF CROSSTALK COMPUTING

This section shows experimental evidence of a functioning Crosstalk Computing chip at 65nm node using the TSMC process. We demonstrate both foundational gates; 2-input OR gate and 3-input OR gate. In conjunction with our simulation results at 7nm for primitive gates, these results show 30% power reduction and 34.5% performance gain over equivalent CMOS counterparts. The unique capabilities of Crosstalk computing can provide new opportunities for future electronics.

## *7.1 Technology Description*

A Crosstalk prototype chip is fabricated using TSMC 65nm PDK. Full custom chip design flow is adopted to fabricate the chip. To suffice the coupling capacitor requirement, the NMOS

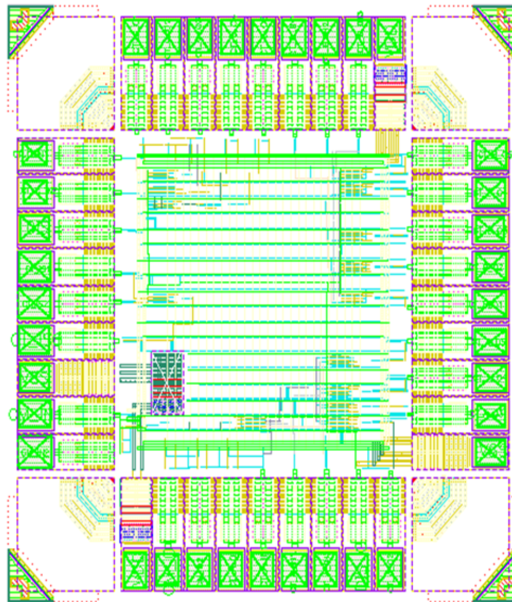

Figure 7.1 Layout of fabricated Crosstalk chip at TSMC 65nm

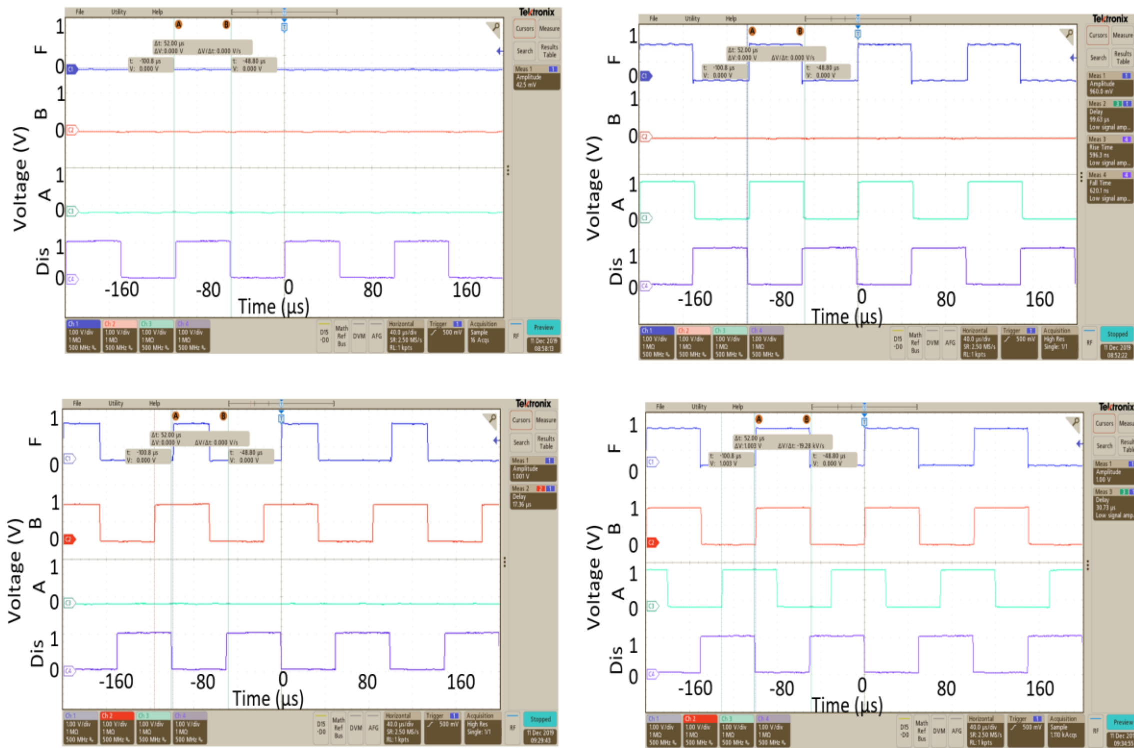


Figure 7.2 Experimental Results of Crosstalk 2-input OR Gate

device capacitor and DCAPs (MIM) are used. Custom circuit schematics are initially designed (Cadence Virtuoso) with the couplings. Subsequently, the circuits are fine-tuned for functionality, power, performance, and noise margins through iterative simulations (Synopsys HSPICE). Custom layouts are then designed, and Physical Verification steps are performed. A separate top-level circuit schematic and corresponding layout (Figure 7.1) are also designed. The custom circuits are instantiated as normal cells. It is an IO limited design consisting of 36 IO pads and IO cells, IO power ring and core power ring, Power Network to deliver the power to circuits, Crosstalk logic gates. All routing is done manually. The clock network is routed for each cell with buffers to maintain drivability. The final layout (Figure 7.1) is extracted for parasitic RCs and simulated at various corners. The chip is fabricated through the TSMC multi-project-wafer run (MPW).

*7.2 Post Fabrication Results*

Figure 7.2 shows experimental results or 2-input Crosstalk OR gate. The top left figure showed when all three inputs denoted as $V_A$, $V_B$, & $V_C$ are logic '0', and there is no output at output pin ($V_{Out}$=0). The discharge signal, in this case, is denoted as $V_{dis}$ with a period of 100 µs. The bottom left figure shows the output for the input combination of (010). In this case, the output is low even though input *B* is high at -40 µs. This is due to the active discharge cycle. When the discharge cycle goes low at 0 µs, the output becomes logic '1' and goes low again at 20 µs along with input *B*. The top right figure showed when one of the inputs denoted as $V_B$ is logic '1', there is output at output pin ($V_{Out}$=1). The bottom right figure shows the

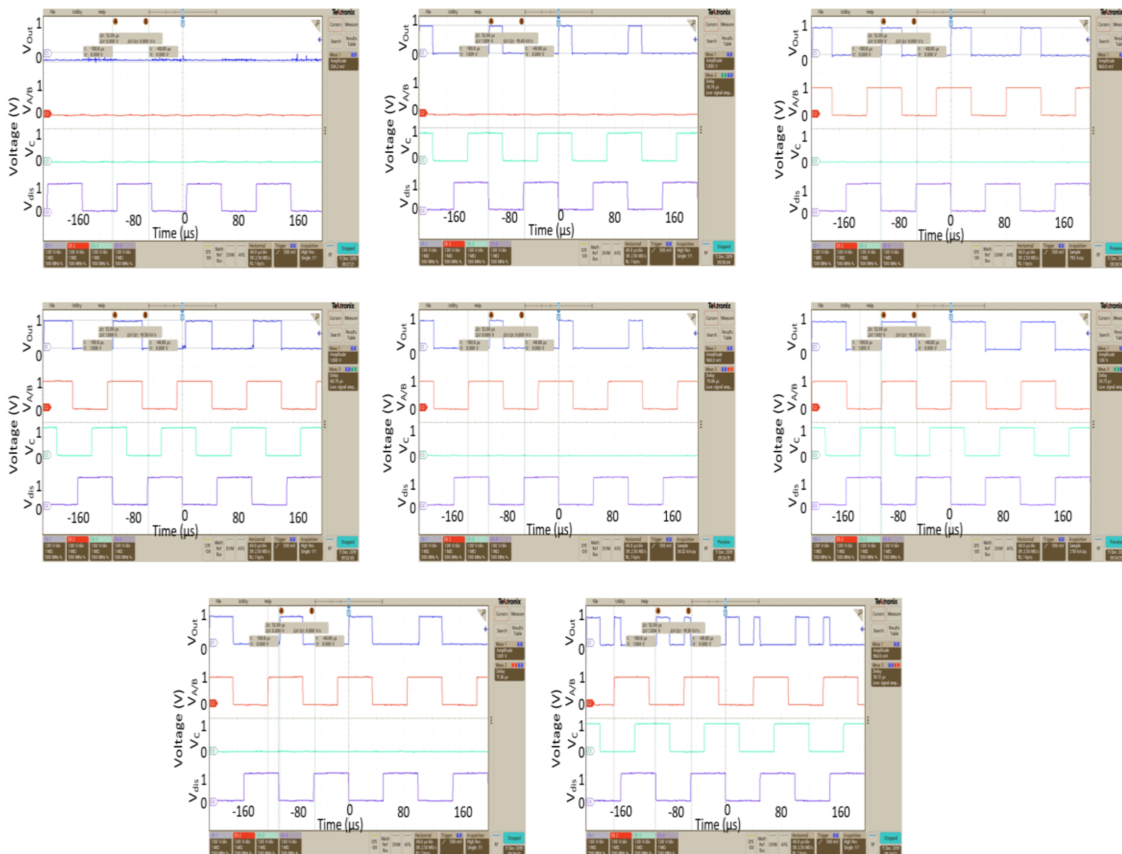

Figure 7.3 Experimental results of Crosstalk 3-input OR Gate.

output for the input combination of (11). In this case, the output is high when all the input is high and low when the discharge signal is high

Measurement for 3-input OR gate is shown in Figure 7.3. The top left figure showed when all three inputs denoted as $V_A$, $V_B$, & $V_C$ are logic '0', and there is no output at output pin ($V_{Out}$ =0). The bottom left figure shows the output for the input combination of (010). In this case, the output is low even though input $B$ is high at -40 µs. This is due to the active discharge cycle. When the discharge cycle goes low at 0 µs, the output becomes logic '1'. It goes low again at 20 µs along with input $B$. Lower right figure shows when all three input $V_A$, $V_B$, & $V_C$ are logic '1', there is logic 1 at output pin ($V_{Out}$ =1). However, it can be noticed that even though all input signals start to transition to one before the discharge signal goes too low, but the output only appears when there is no discharge signal. All the eight possible input combinations are being tested and verified. The measurements in Figure 7.2 & Figure 7.3 were captured using probestation, a high-frequency signal generator (2GHz), and an oscilloscope. All the signals are of 1V with 100µs period.

### *7.3 Section Summary*

The post-fabrication measurements validated the Crosstalk computing concept. Our benchmarking across technology nodes results show promise for elementary logic gates such as a NAND gate. These experimental and scalability results, along with our prior large-scale circuit design work, can pave the way for future adoption of Crosstalk circuits.

# CHAPTER 8

# THERMAL MANAGEMENT CHALLENGES AND MITIGATION TECHNIQUES FOR TRANSISTOR-LEVEL 3-D INTEGRATION

Keeping up with the traditional way of IC scaling is becoming very difficult due to fundamental physical limits. Migration to 3-D integration could provide possible pathways for further scaling [1,7-9,74]. Among the most promising 3-D IC research directions, transistor-level 3-D integrations such as monolithic 3-D [66], Skybridge [67], SN3D [68] hold the most promise for density gains [75–80]. However, like wafer-level 3-D integration approaches [81], transistor-level 3-D ICs also face thermal management challenges due to the stacking of transistors and lack heat dissipation paths [2,10,69]. System-level thermal management approaches like forced air-cooling [70,82], micro-fluid-based channel integration [83], metalized carbon-nanotubes, and graphite nanocomposites [71,84] or software-level solutions [72,85,86] are inadequate for such 3-D integrations, and a more fine-grained approach at circuit-level is necessary.

Previously, we proposed novel physical fabric level thermal management features to mitigate heat at the circuit level [73]. Our proposed physical level thermal management features are generic for all the 3-D integration directions and provide the flexibility to be placed anywhere in the 3-D circuit to extract heat in a customized manner based on the requirements. These features include: (i) Thermal Junction to extract heat from the heated region, (ii) Heat Conducting Nano Pillar for dissipating the heat towards the substrate, and (iii) Metal Connector for carrying the extracted heat to the thermal pillar. In order to capture the thermal profile of transistor-level 3-D integrated circuits and evaluate the effectiveness of

proposed heat extraction features, we have done both devices & circuit-level thermal evaluation using Finite Element Method (FEM) based modeling. FEM-based models can be effectively used for thermal profiling of 3-D ICs because of their ability to handle complex geometries and nonhomogeneous material, greater efficiency, and flexibility [87–91]. Although circuit and system-level heat analysis exist [92,93] in literature, FEM-based analysis that accounts for device-specific materials, circuit operating conditions, and circuit layouts are not present. We have done device-level analysis first, then expanded to circuits, applied circuit operating conditions, and information about 3-D circuit layout. Our model accounts for nanoscale material properties, nanoscale dimensions, heat flow path, 3-D circuit operation, and layout. Also, this model is capable of capturing both static and dynamic thermal behavior. Expanding on our previous work [8], where we introduced the concept of generic 3-D thermal management features, the key contributions of this paper are as follows-

- Details of the proposed physical fabric level thermal management features, including material aspects, dimensions, and their generic application to emerging transistor-level 3-D ICs.
- Details of our bottom-up FEM thermal modeling approach accounts for nanoscale materials, geometry, devices, layout, and circuit behavior.
- FEM-based thermal evaluation of 3-D circuits under different operating conditions.
- Comparison among different transistor-level 3-D ICs for static and dynamic thermal scenarios.

Our FEM simulation results indicate how material stacking and dielectric could interplay

on the final thermal profile for 3-D integrations. For example, Skybridge circuits' average temperature increased to 650 K from ambient temperature (300 K). The proposed heat extraction features effectively reduced the temperature from a heated location by 50% in the best case to around normal operating temperature at 330 K. These results are significant and can pave the way for a new circuit design paradigm with intrinsic thermal management.

### *8.1 Overview of Transistor-Level 3-D Integration Approaches*

Among various transistor-level 3-D integration approaches, monolithic 3-D IC [66], Skybridge [67], and SN3D [68] achieve the highest density benefit [94]. In the following, we give a brief overview of these transistor-level 3-D integration approaches:

#### *8.1.1 Skybridge [67]*

Skybridge, a vertical 3-D IC, relies on six core fabric components with intrinsic heat extraction features to address 3-D device, circuit, connectivity, and manufacturing requirements [67]. One of the major components is uniform vertical nanowires. Junctionless transistors are active devices of the fabric. These devices are stacked on nanowires and are interconnected using bridges and coaxial structures to implement logic and memory

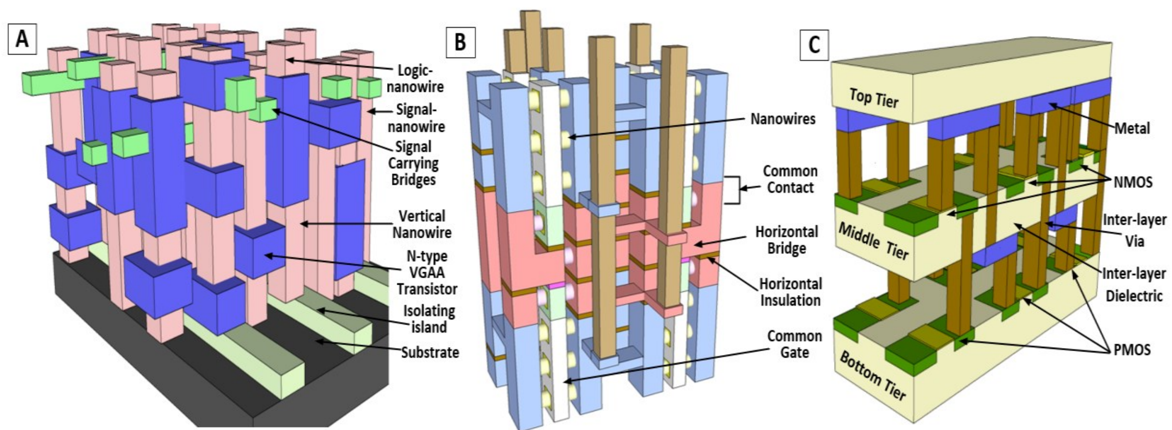


Figure 8.1 Transistor-level 3-D integration approaches in literature [66–68] A) Skybridge, B) SN3D, C) Monolithic 3-D IC.

functionalities. Figure 8.1A shows the architecture of Skybridge fabric where transistors are stacked on the prefabricated nanowires. Transistors stacked at the top are exposed to a more significant thermal resistance path to the substrate and suffer from lack of heat dissipation path, which only increases the average and maximum temperature within the device.

### *8.1.2 Stacked Horizontal Nanowire Based 3-D CMOS (SN3D) [68]*

SN3D is a different fabric concept for 3-D CMOS using stacked horizontal nanowires on a single die. It is a single die-based approach where horizontally stacked suspended nanowires serve as building blocks or templates. The architected device, connectivity, insulation are formed onto these nanowires through material depositions for fabric assembly. The high degree of connectivity in SN3D is achieved by utilizing the fabric's intrinsic features. Prefabricated and doped stacked horizontal nanowires are the building blocks, and Gate-All-Around nanowire FETs (GAA-NWFETs) are the active devices. Such 3-D integration provides an integrated solution for the nanoscale device, circuit, and connectivity. However, these approaches suffer from thermal management issues. As we can see from Figure 8.1B that dies sitting in the middle have a longer heat path to the top or bottom substrate and higher heat coupling with the neighboring dies than the dies on the boundary close to the heat sinks. Such heat dissipation and thermal coupling are translated into excess heat development.

### *8.1.3 Monolithic 3-D CMOS [66]*

Die to die stacking with TSVs is becoming the superior technology today. Monolithic 3-D is the most advanced substrate stacking technology where two separate dies/layers are bonded together with fine-grained vias. Because of the integration technique, the metal stack is always on the top layer (primary routing happens here). Vias are used to connect the top and bottom die, and their density is dependent on circuit topology [8,95–99]. In monolithic 3-

D IC, any 2-D standard cells can be placed, and connections can be made through interlayer vias. However, many devices that can be stacked within the system are restricted by thermal behavior [100]. From Figure 8.1C, we can see that monolithic 3-D integration has a higher device density per volume. Due to the dense integration of devices, heat coupling in two-tier or three-tier monolithic 3-D ICs has approximately 10 K–25 K higher maximum temperature than 2-D ICs [100].

### *8.2 Thermal Management by Architecting Specialized Physical Fabric Features*

Proposed thermal management features include three main core components: (i) Thermal Junction, (ii) Heat Conducting Nano Pillar, and (iii) Metal Connector. One of the core components, the heat-conducting nanopillar, enables heat dissipation towards the heat sink. The heat conducting nano pillar is connected with a terminal junction via a metal connector to extract heat from the logic nanowire. The thermal junction is a specialized junction to extract heat from a selected region in 3-D ICs; it allows heat conduction without interference with the electrical activities of the circuit. The metal connector works as connecting bridge

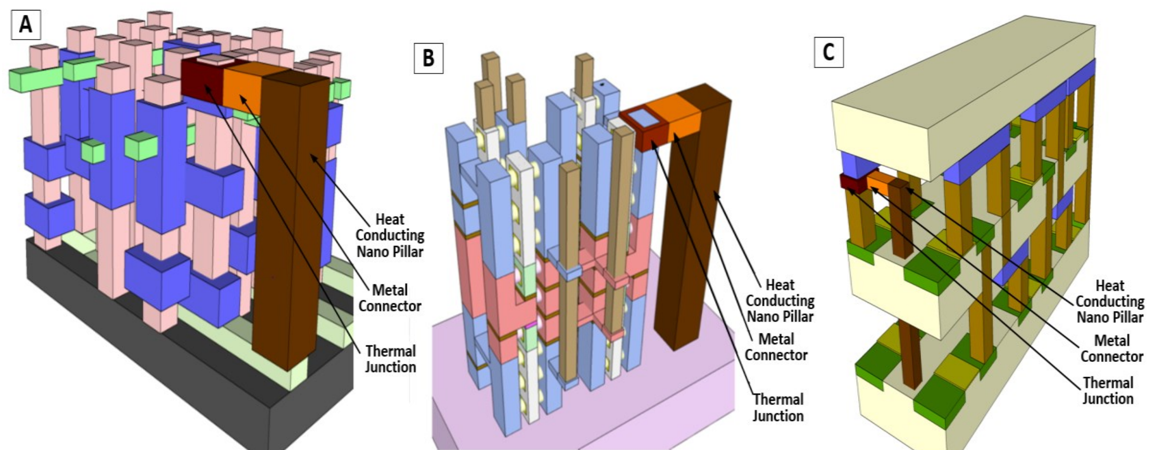


Figure 8.2 Application of thermal extraction features at transistor-level 3-D integration A-C) Customizable & adaptable heat conducting nano pillar connected with thermal junction to extract heat for **Error! Reference source not found.** 3-D integration approaches

between pillar and thermal terminal. An abstract view of integrating the features into different 3-D ICs with all core components is given in Figure 8.2. Therefore, once the heat is extracted from heated regions, it dissipates heat towards the substrate via pillar and connecting metal. These features are intrinsic to the fabric and optimizable at the physical fabric level for 3-D compatibility. They can be implemented anywhere in the circuit without any loss of circuit functionality and performance.

Figure 8.2A–C shows the generic nature of the heat management features where the features are applied to all three 3-D ICs. We can plug in specialized heat management features to all of these circuit styles without interfering with their electrical operations. For example, for Skybridge (Figure 8.2A) or SN3D (Figure 8.2B), thermal junctions are placed at the top of the logic nanowires. Because of the insulating property, thermal junctions do not allow any current conduction; it only extracts heat from that specific region and dissipates towards the substrate via pillar. The dimension of the pillar is designed in such a way that it occupies a minimum die area. For such a small cross-sectional area, the pillar can bring down overall circuit temperature to the ambient. However, the area of the pillar can be increased to facilitate further heat dissipation. Detailed dimensions and materials used for heat management features are given in Table 8-1. The formation of heat-conducting nanopillar can be done with any emerging material with high thermal conductivity at the nanoscale. In this case, Tungsten or Aluminum might be a good candidate as both materials have high conductivity. At a sub 200 nm scale, it is shown that the thermal conductivity of Tungsten can reduce significantly [101,102]. In the rest of the paper, we show the usage of Aluminum for heat nanopillars. The nanopillar is connected with a thermal junction for extracting heat from the heated region of nanowires. This thermal junction can be made from the deposition of Al2O3. Such oxide

Table 8-1 Device Materials and Their Dimensions

| Skybridge | | | | SN3D | | | | Monolithic 3-D | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Region** | **Material** | **Dimension (LxWxT) nm** | **Thermal Conductivity $Wm^{-1}K^{-1}$** | **Region** | **Material** | **Dimension (LxWxT)nm** | **Thermal Conductivity $Wm^{-1}K^{-1}$** | **Region** | **Material** | **Dimension (LxWxT)nm** | **Thermal Conductivity $Wm^{-1}K^{-1}$** |
| Drain | Silicide | 10 x 16 x 16 | 18 [109] | Drain/Source Electrode | Ni | 24 x 32 x 34 | 73.2 [115] | Drain/Source Electrode | Pt | 24 x 24 x 32 | 30 [108] |
| Drain/Sourc e Electrode | Pt | 10 x 16 x 12 | 30 [108] | Channel | Doped Si | 16 x 16 x 16 | 13 [107] | Channel | Doped Si | 16 x 32 x 32 | 13 [107] |
| Channel | Doped Si | 16 x 16 x 16 | 13 [107] | Gate Oxide | $HfO_2$ | 32 x 5 x 20 | 0.52 [112] | Source | Silicide | 24 x 24 x 32 | 18 [109] |
| Source | Silicide | 10 x 16 x 16 | 18 [109] | Gate Electrode | TiN | 32 x 28 x 28 | 1.9 [113] | Gate Oxide | $HfO_2$ | 32 x 5 x 20 | 0.52 [112] |
| Thermal Junction | $AL_2O_3$ | 36 x 36 x 26 | 30 [110,111] | Horizontal Insulation | Su-8 | 24 x 32 x 5 | 0.2 [116] | Gate Electrode | TiN | 32 x 28 x 28 | 1.9 [113] |
| Gate Oxide | $HfO_2$ | 32 x 5 x 20 | 0.52 [112] | Thermal Junction | $AL_2O_3$ | 36 x 36 x26 | 30 [110,111] | Thermal Junction | $AL_2O_3$ | 36 x 36 x26 | 30 [110,111] |
| Gate Electrode | TiN | 26 x 24 x16 | 1.9 [113] | Spacer | $Si_3N_4$ | 16 x 16 x 10 | 1.5 [114] | Spacer | $Si_3N_4$ | 16 x 16 x 10 | 1.5 [114] |
| Spacer | $Si_3N_4$ | 16 x 16 x 10 | 1.5 [114] | Metal Connector | Al | 43.5x58x16 | 50 [103-105] | Metal Connector | Al | 43.5x58x16 | 50 [103-105] |
| Heat Pillar | Al | 60x60x168 | 151 [103-105] | Heat Pillar | Al | 60x60x168 | 151 [103-105] | Heat Pillar | Al | 60x60x168 | 151 [103-105] |
| Oxide | $SiO_2$ | 36 x 36 x 20 | 1.38 [93] | Oxide | $SiO_2$ | - | - | Oxide | $SiO_2$ | 600 x 450 x 30 | 1.38 [93] |
| Substrate | Si | 600 x 450 x 235 | 148 [107] | Substrate | Si | 600 x 450 x 235 | 148 [107] | Substrate | Si | 600 x 450 x 235 | 148 [107] |
| Heat Sink | Al | 600 x 450 x 150 | 237 [104] | Heat Sink | Al | 600 x 450 x 150 | 237 [104] | Heat Sink | Al | 600 x 450 x 150 | 237 [104] |

composite is electrically insulated, which does not affect logic implementation at circuits. Thermal junction gives the flexibility to be placed anywhere on the nanowire. It can extract heat and dissipate through the heat-conducting nanopillar in conjunction with the metal connector. The metal connector can be formed from Aluminum deposition and works as a connecting bridge between conducting nanopillar and oxide terminal. In the next section, we discuss the modeling of heat conduction in 3-D devices and circuits.

### *8.3 Finite Element Modeling and Simulation Approach*

A fine-grained Finite Element Method based modeling approach is used to determine the thermal profile of 3-D devices and quantify the effectiveness of proposed heat extraction features. The modeling is done at transistor-level granularity, which accounts for material properties at the nanoscale, confined geometry, nanoscale carrier, heat transport, nanoscale thermal contact resistance, circuit operating conditions, 3-D circuit placement, and 3-D layout. Figure. 8.3 illustrates the methodology followed for thermal resistance modeling and thermal modeling of 3-D circuits.

### 8.3.1 *Methodology*

It is essential to determine electrical characteristics first to obtain the thermal profile since information about current and voltage is essential for heat source calculation. For electrical characterization, the Sentaurus Process simulator [106] is used to create the active device structure emulating actual process flow. The process emulated device structure is simulated in Synopsys 3-D Sentaurus Device [106] to characterize the behavior. We have used sophisticated and accurate models for simulation to account for various nanoscale effects like quantum transport in the confined geometry, carrier velocity saturation, and increased carrier scattering. The silicon band structure and effect of bandgap narrowing are calculated using the Oldslotboom model. The charge transport model employed to characterize the device current is the hydrodynamic carrier transport model [106]; the model solves the Poisson and carrier continuity equations, lattice and carrier energy equations, and quantum transport model

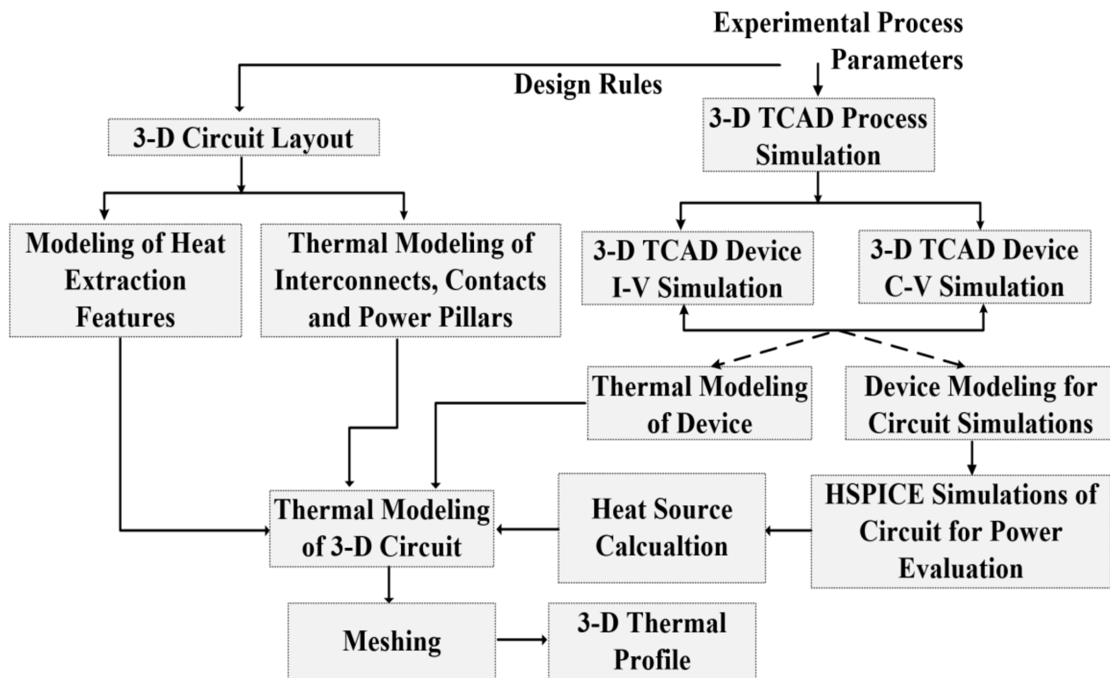

Figure 8.3 Methodology for Finite Element Modeling

self consistently to determine the device current. The quantum transport model used for accounting carriers quantum confinement in the smaller channel is the Density Gradient (DG) quantum correction model [106], which provides the most physically accurate results. Electron mobility (degradation) is modeled, taking into account the effects of high-dopant, surface, and interface scatterings, as well as velocity saturation. The characterized device ON current that accounts for nanoscale confinement, surface, and Coulomb scattering and mobility degradation effects is then multiplied by drain voltage to obtain the power and subsequently applied as a heat source at the drain side of the device following the transistor self-heating principle. Also, from TCAD simulated device characteristics, the HSPICE compatible behavioral device model is generated, which can be integrated back into HSPICE to obtain power at the circuit level.

Moreover, for accurate modeling, we also account for the 3-D circuit layout. Information about the placement of thermal management features, interconnect parasitics, contact materials, and device structure is obtained from the 3-D layout of different circuit styles. Besides, while modeling heat extraction features and interconnect, contacts are also accounted for accurate thermal profiling. The mesh generation then follows this for represented structure, and on each small granularity, we perform self-consistent evaluations. This process self-consistently calculates the heat distribution throughout the structure.

### *8.3.2 Principles for FEM Thermal Conduction Modeling*

For FEM thermal modeling, we use the following time-dependent heat equation [91]:

$$\rho Cp \frac{\partial T}{\partial t} + \nabla . (-k \nabla T) = Q \quad (1)$$

where $\rho$ is the density, $Cp$ is the heat capacity, $k$ is the thermal conductivity, and $Q$

denotes the heat generated per volume. The equation implies that if heat ($Q$) is added to the volume, this will result in a temperature change within the device. As explained in the methodology section, heat source (Q) is calculated from the ON current and drain voltage derived from the TCAD process and device simulations. Material thermal properties like thermal conductivity, for this work, are obtained from the literature. However, accurate material properties are subjected to the extensive experiment considering the exact dimensions.

Additionally, from Eq. (1), it can be observed that the variation of temperature is also a function of time from which we can calculate the dynamic behavior of the device. The dynamic thermal analysis is required to help predict the temperature on circuits during operating conditions.

Although the finite element model efficiently gives the thermal profile, there are other approaches possible like space and time-dependent Boltzmann Transport Equation (BTE) for phonons [117,118] that can be more accurate. In this case, the application of BTE would require information on the ballistic and diffusive flow of phonons and atomistic properties for the materials. Different algorithms such as almaBTE [119] may be used to solve BTE for thermal profiling. For calculation of the atomistic properties of materials, the ab-initio method [120] can be used where such approaches can be implemented using ALAMODE [121] or phono3py [122] software packages.

#### *8.3.3 Thermal Contact Resistance Modeling*

Due to thermal contact resistance formed by two interfacing materials, the rate of heat dissipation reduces significantly. The influence of thermal resistance becomes more dominant at the nanoscale since the actual contact area between two materials, found to be a small

portion of the apparent contact area [123]. Such a change in heat transfer rate creates a temperature drop at the interface, which is proportional to the value of thermal contact resistance. It can be formulated as [124]

$$R_c = \frac{\Delta t}{Q} \qquad (2)$$

The reciprocal of the thermal contact resistance is termed thermal conductance, $h_c$. Since radiation heat transfer at most interfaces is negligible or non-existent, it will not be included in this analysis. At the contact surface, the thermal contact conductance $h_c$ is expressed by,

$$h_c = h_s + h_g \qquad (3)$$

where, $h_c$ is contact conductance, $h_s$ is the joint surface conductance and $h_g$ is gap conductance. The surfaces of the two bodies are considered to be fully conforming; that is, the thermal resistance of the contacting surfaces is assumed to be governed only by their effective surface roughness and the presence of interstitial-gas (air) filled micro-gaps [125]. The surface contact conductance is given by the Cooper, Mikic, and Yovanovich correlation [126-127],

$$h_c = 1.25 k_s \frac{m}{\sigma} \left(\frac{P}{H_c}\right)^{0.95} \qquad (4)$$

where $\mathrm{k_s}$ is the harmonic mean thermal conductivity of the interface [127]:

$$k_s = \frac{2k_1 k_2}{k_1 + k_2} \qquad (5)$$

and the equivalent root mean- squared (RMS) roughness, $\sigma$, and the equivalent mean absolute surface slope, m, are respectively defined as [128]

$$\sigma = \sqrt{{\sigma_1}^2 + {\sigma_2}^2} \text{ and, } m = \sqrt{{m_1}^2 + {m_2}^2} \qquad (6)$$

where subscripts 1 and 2 are used to denote the two contacting bodies. The contact pressure is P, and Hc is the surface nano-hardness of the softer of the two contacting solids [128]. The nano-hardness is, in general, complex because it depends on several geometric and physical parameters; accurate values of nano-hardness of material are subjected to extensive experiments where exact dimensions are considered.

Moreover, gaps between the contacting materials caused by surface roughness are usually filled with air. Among various thermal gap conductance models, parallel plate gap gas conductance was used in this study. It is a simple but effective model in predicting gap conductance. This model assumes two parallel plates with a gap filled by a gas phase. The thermal conductivity of such air is typically much lower than the conductivity of the standard solid materials, which also contributes to increasing the thermal resistance at the interface. The gap conductance is given by [124,129],

$$h_g = \frac{k_g}{Y + M_{gap}} \quad (7)$$

where $k_g$ is the effective thermal conductivity of the gas in this case, air, Y the effective thickness, and Mgap is the effective gas parameter [130]. Surface contact conductance from equation (4) and gap conductance from equation (7) can be integrated back to equation (3) to calculate overall thermal conductance; the reciprocal of which will be the thermal contact

Table 8-2 Material Properties for Thermal Contact Resistance Modeling

| **Material** | **Nanohardness (GPa)** | **Surface roughness (nm)** |
|---|---|---|
| Aluminum (Heat Sink) | 0.46 [135] | 2.00 [81] |
| Silicon | 12.26 [137] | 1.96 [133] |
| Aluminum (Pillar) | 0.46 [136] | 0.20 [134] |
| $AL_2O_3$ | 10.5 [137] | 0.72 [136] |

resistance $R_c$. During modeling, four significant stages of heat removal from the device are considered; from the device to the thermal junction and then to the metal connector, pillar to the substrate, and finally substrate to the heat sink. Parameters that influence the joint-conductance (contact pressure, nanohardness of the softer material, surface roughness, and surface roughness slope) are obtained from the literature and presented in Table 8-2.

Cooper, Mikic, and Yovanovich correlation provide a prediction of thermal contact resistance between two contacting materials by accounting for key parameters like joint conductance of the materials [129]. However, detailed calculation of the thermal resistance of a nanoscale contact will also depend on various factors like contact materials, the Van Der Waals interactions at the contacts, characteristic dimensions of the contact, and the intrinsic phonon mean accessible paths of the materials in contact. Moreover, the total thermal resistance is usually dominated by the size confinement of the contact, an accurate estimation of which is, unfortunately, usually difficult to evaluate [131]. Due to these complexities involved in phonon transport through nanoscale contacts, the availability of experimental data is also minimal and requires further exploration. Additionally, various thermal interface materials are used at the packaging level [132].

### *8.3.4 Thermal Modeling of 3-D Circuits*

We integrate our thermal model in COMSOL-Multiphysics, a commercial finite element simulation tool [91], and capture the thermal profile of 3-D ICs. Our thermal model describes the transistor as blocks and sequentially stack the blocks as per the circuit style of different 3-D ICs. We place a conventional heat sink at the bottom of the substrate (Fig. Figure 8.4A–C). For the simulation purpose, the dimension of the substrate and heat sink is kept uniform. For all three different 3-D circuit styles, heat sources are assumed to be at the drain side of the

transistors. The outer surface of the heat sink is set to 300 K (ambient). All other boundaries of the stack are set as adiabatic. We assumed the thermal conductivity of Silicon nanowire to be 13 $Wm^{-1}K^{-1}$ since, at the nanoscale, Silicon conductivity reduces significantly [106].

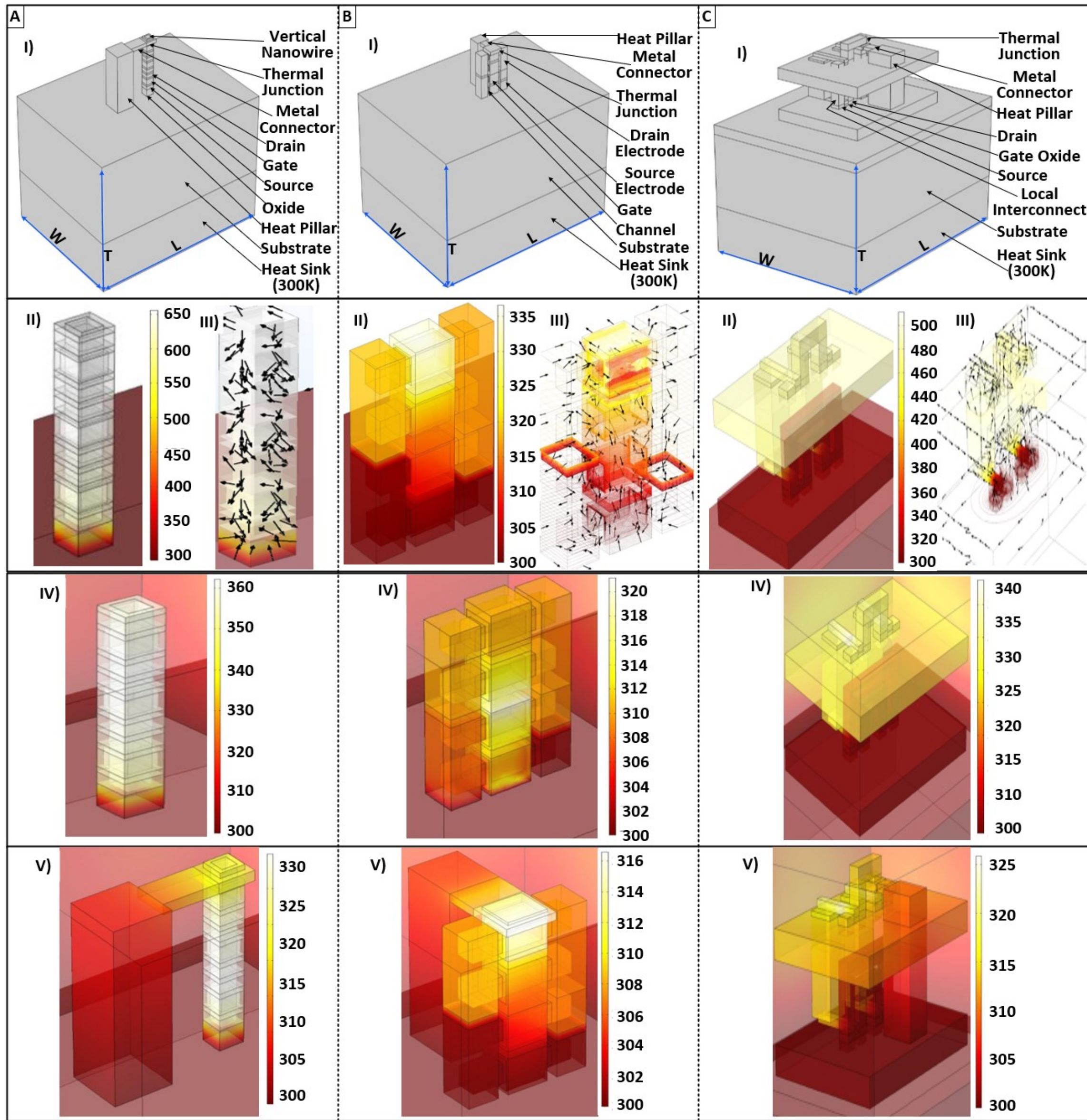


Figure 8.4 Thermal evaluation of different 3-D ICs under different conditions A) Skybridge, B) SN3D, C) Monolithic 3-D. I) Circuit level implementation of different 3-D fabric. II) Thermal profile of transistor level 3-D Integrated Circuits without any heat extraction feature. III) Heat flow path and temperature gradient of 3-D ICs. IV) Thermal behavior of 3-D Integrated Circuit under dielectric medium. V) Effectiveness of fabric's intrinsic heat extraction feature. Specialized heat extraction path reducing the temperature close to ambient by extracting additional heat from the most heated region and dissipating towards heat-sink for Skybridge, SN3D and Monolithic 3-D respectively. (Temperature units are given in Kelvin scale).

Detailed dimensions along with material specifications for all types of 3-D approaches are given in Table 8-2.

In this paper, for modeling the Skybridge circuit, we consider a dynamic NAND gate, which follows the circuit style presented in [67]. Dynamic behavior of NAND gate is controlled by precharge (PRE), evaluate (EVA) control signals. N-type uniform V-GAA Junctionless transistor is the active device for this fabric. We stack all three transistors in a single vertical nanowire [Figure 8.4A(I)]. Power dissipation around the drain and gate region is translated to heat generation due to self-heating. From the behavioral model of the active device, we obtained ON Current ($3.2 \times 10^{-5}$ A) with respect to drain voltage, VDD (0.8V). Subsequently, the amount of heat generation, Q (Watts) at the drain region, is calculated using the following equation:

$$Q = Ids * Vds \qquad (8)$$

where, $Ids$ is Drain-Source current, and $Vds$ is Drain-Source voltage. The total heat generated is found to be 25.6μW.

Similarly, the geometry of SN3D fabric is taken from Ref. [68]. In this fabric, the active device is Gate-All-Around Junctionless nanowire FET. Two n-type Junctionless nanowire FETs are placed at the bottom, and two p-type Junctionless nanowire FETs are stacked on top to achieve NAND circuit configuration [Figure 8.4B(I)]. A common metal connector is connected to the source side of the two p-type transistors as drain contact. Heat sink with the same dimension as Skybridge is placed at the bottom of the substrate. Using Eq. (8), we calculated the generated heat (13.6 μW) at the drain side; ON current (17.8 μA) and drain voltage (0.8 V) are obtained from the characteristic model of Gate-All-Around Junctionless nanowire FET by following the steps explained in previous sections. As SN3D follows

combinational circuit styles, therefore, we applied heat source at the drain contact of the two pull-up transistors [Figure 8.4B(I)].

For modeling of monolithic 3-D, we used design rules presented in Ref. [66], and detailed device dimensions are presented in Table 8-1. Like Skybridge and SN3D, we also implement a NAND gate for circuit-level thermal evaluation of monolithic 3-D. To achieve this, two PMOS transistors are placed in the bottom tier, and two NMOS transistors are placed in the top tier [Figure 8.4C(I)]. The size of the inter-layer via is 50 nm, and the length of the inter-layer via is 110 nm. The local metal connection is Aluminum. Like Skybridge and SN3D, a heat sink is placed at the bottom of the substrate. Heat sources are applied to the drain side of the two pull-up transistors due to the combinational circuit styles of monolithic 3-D IC. We applied 1.22mW to the drain side as a heat source.

Proposed heat extraction features are also placed according to fabric design principles outlined in Section 8.2. The dimensions for heat extraction features are mentioned in Table 8-1 and can be modified according to fabric specifications. The thermal junction is placed at the top transistor for all 3-D circuits. The pillars are directly connected to the substrate, enabling heat dissipation from the most heated region toward the heat sink. To account for detailed spreading resistance and boundary conditions, chip/packaging-level information like the contact area of the heat source, area of the heat sink base-plate, the thickness of the heat sink base-plate, average heat sink thermal resistance, and any additional system-level cooling mechanism are required. They will be part of our future explorations.

### *8.4 Thermal Evaluation Results*

We have done extensive simulations to capture the static and dynamic thermal profile of

3-D transistor-based circuits and evaluate the effectiveness of intrinsic heat extraction features. In the following, we present thermal simulations of vertical transistor-based devices and circuits.

### *8.4.1 Thermal Evaluation of 3-D Circuits*

We simulated the thermal behavior of different transistor-level 3-D integration approaches without any heat extraction features. Figure 8.4 shows the thermal profile and temperature gradient for Skybridge, SN3D, and monolithic 3-D ICs. Figure 8.4A(II)&(III) illustrate the worst-case thermal distribution for Skybridge without any heat extraction medium; the highest temperature at the top transistor is 650 K, which is almost 250 K rise from the ambient temperature. Such a temperature rise is primarily due to a longer thermal resistance path towards the heat sink and transistor-level self-heating. As also reported in Ref. [141], because of self-heating, temperature for a single vertical nanowire can be increased up to 60 K. Figure 8.4A(I)&(II) illustrate that transistors are stacked on top of each other where the top transistor is the furthest from the heat sink and lacks a heat dissipation path. As a result, heat has to follow the longest thermal resistance path. However, as the heat flows towards the channel, there are more heat dissipation paths through drain/gate/source contact. The source is closest to the heat sink; temperature starts decreasing at the source contact and reaches to reference temperature (300 K).

For the SN3D NAND logic circuit, the temperature rise is only 36 K. This temperature rise is lower than other 3-D approaches. This is primarily due to the fabric style of SN3D. The highest temperature is at the gate region of the top transistor since it lacks a sufficient heat dissipation path due to the confined geometry. As in the case of drain contact [Figure 8.4B(II)], which in SN3D is also a common contact for other transistors, heat is not localized

due to sharing contact configuration. Moreover, source contact is placed just below the drain contact separated by horizontal insulation. These give the benefits of extracting the additional heat created at the drain contact and dissipating it towards the substrate. However, in Figure 8.4A–C, it can be seen that for all cases, top transistors are far away from the heat sink, which increases the thermal resistance path and eventually leads to high temperature at the top transistors.

Figure 8.4C(II) illustrates that the temperature for monolithic 3-D is much higher at the top tier than the bottom tier. The highest temperature is 500 K for the top-tier, which is an almost 200 K rise in temperature; such a rise in temperature for 3-D ICs is also reported in Ref. [93]. Lack of heat dissipation path, bulk material configuration, and leakage current are the leading causes of such high temperature. From the temperature gradient [Figure 8.4C(III)], it can be seen that high heat at the top tier also contributes to increasing the temperature at inter-layer vias. On the contrary, the bottom tier being close to the heat sink, maintains ambient temperature. Also, local interconnects for the bottom tier are also at 300 K.

### *8.4.2 Thermal Behavior Under Dielectric Medium*

As all the fabrics have a dielectric medium wrapped around them, which contributes significantly towards heat dissipation, we also want to capture the thermal behavior under the dielectric medium. We simulate heat propagation under a dielectric medium for the above-mentioned 3-D ICs. In our model, we approximate a rectangular box surrounding the nanowire circuit as a dielectric medium. Even though the dielectric medium acts as a heat dissipation path, it has a very low thermal conductivity of $0.3 Wm^{-1}K^{-1}$ [142]. From Figure 8.4A–C(IV), it can be seen that due to the presence of medium dielectric temperature drops down on average 20 K–200 K. As for Skybridge, and it reduces the temperature almost by 160 K from

650 K. Since the dielectric medium is widely covered around the whole chip area, it can efficiently dissipate heat. However, the reduced temperature is still insufficient for regular circuit operation and may cause perturbation in logic implementation.

### *8.4.3 Effectiveness of Intrinsic Heat Extraction Features*

The effectiveness of the proposed fabric's intrinsic heat extraction features is depicted in Figure 8.4A–C(V). The thermal junction is placed at the top transistor in conjunction with the metal connector and the heat-conducting nanopillar to maximize heat dissipation from the most heated region of the circuit. Simulations are done considering circuit styles of different transistors and under the same dielectric medium described in the previous section. Simulated results show that the heat extraction features effectively reduce the temperature for all the circuit styles, especially transistor-level 3-D integration that suffers most from the heat management issues. The final temperature is around 315 K, which is almost close to the ambient temperature for SN3D. For Skybridge, due to heat extraction features, it gets an

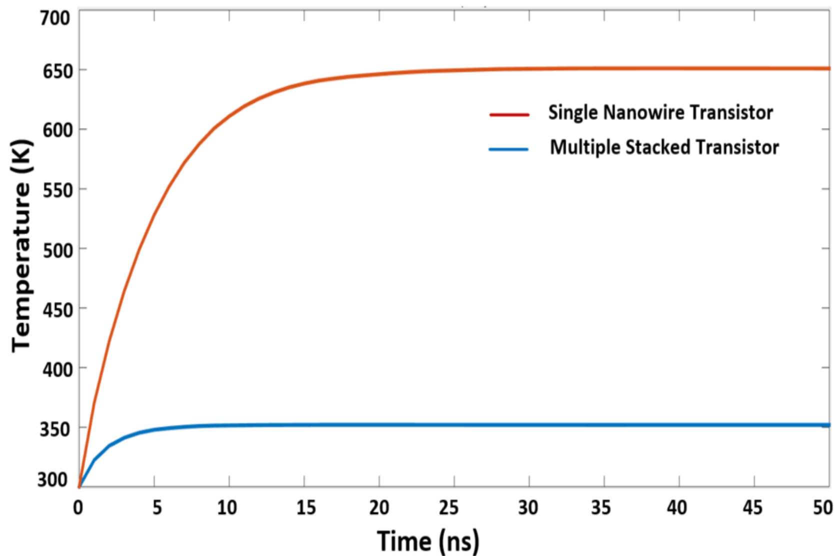


Figure 8.5 Transient thermal behavior of vertically stacked nanowire transistors vs single nanowire transistor.

additional heat dissipation path that allows bringing down the temperature by from 360 K to 330 K. For all cases, the temperature does not drop to ambient; this is mainly due to the presence of thermal contact resistance at the extraction interfaces. However, the heat extraction features have the flexibility to be placed anywhere in the circuit without any perturbation of circuit operation. It allows placement of the thermal junction even at the middle transistors, which will further bring down the temperature.

### *8.4.4 Transient Thermal Under Different Condition*

The previous analysis gives us an idea about the static thermal profile when the power source is applied. We also simulate the dynamic thermal analysis of the circuits. To capture the transient profile, at first, we simulated one single nanowire transistor. We then expanded the simulation for the whole circuit. Fig. 5 gives a comparison of the dynamic temperature profile for single and multiple stacked transistors. For multiple stacked nanowire transistors, the temperature increases over 25ns of time and then stabilizes. Over time-temperature starts to balance out because heat sources remain active during the whole simulation period. Once we remove the heat source, the temperature will start going down to ambient temperature. We

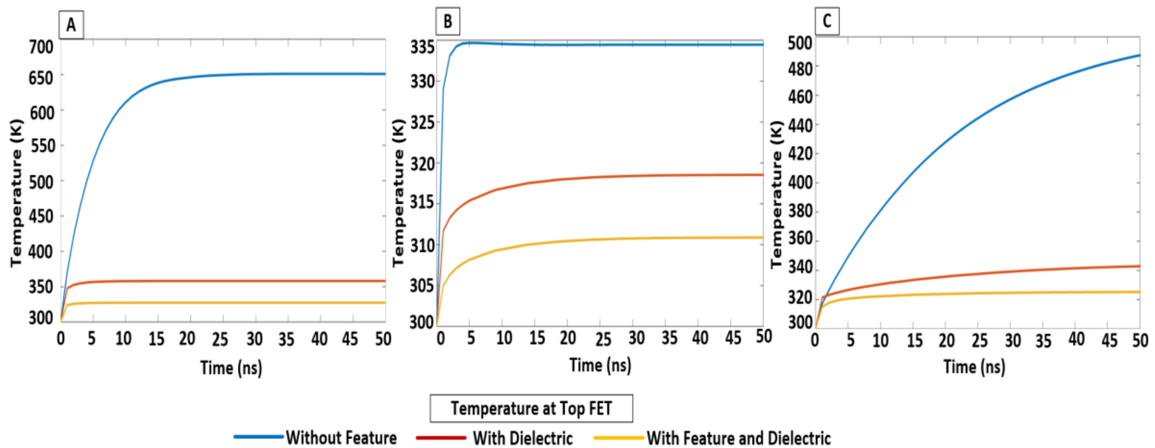


Figure 8.6 Dynamic thermal behavior of top transistor of different 3-D ICs under different condition. A) Skybridge, B) SN3D, C) Monolithic 3-D.

further extended our dynamic thermal analysis to each of the transistors of different fabrics. Fig. 6 gives a detailed comparison of the dynamic thermal profile for different fabrics at the top transistor. When the transistor is running without any heat extraction feature, the temperature gradually increases. However, the effectiveness of our proposed heat extraction can also be seen in Fig. 6A–C. With heat extraction feature under dielectric medium, the temperature always remains close to the ambient temperature during any circuit operating time.

### *8.5 Section Summary*

We showed thermal modeling (both static and dynamic) for emerging transistor-level 3-D integrations in this work. Our thermal modeling shows that the temperature can increase by 100 K–200 K without any heat extraction feature for 3-D ICs. We detailed physical fabric level heat management features applicable for all transistor-level 3-D integration approaches to address the heat issue. We also showed its effectiveness through modeling and simulations. Our FEM-based thermal modeling is a fine-grained approach that considers material properties, nanoscale effects, 3-D circuit style, and 3-D layout details. Simulation results show that our proposed heat extraction features can reduce the temperature of the heated area by 27%–48% and keep the temperature at ambient during circuit operation. Such a heat management approach is unique and can open new opportunities for thermal-aware circuits in 3-D.

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# VITA

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