# MEASURING LEVEL OF DEGRADATION IN POWER SEMICONDUCTOR DEVICES USING EMERGING TECHNIQUES

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DOCTOR OF PHILOSOPHY

by
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## ABSTRACT

High thermal and electrical stress, over a period of time tends to deteriorate the health of power electronic switches. Being a key element in any high-power converter systems, power switches such as insulated-gate bipolar junction transistors (IGBTs) and metal-oxide semiconductor field-effect transistors (MOSFETs) are constantly monitored to predict when and how they might fail. A huge fraction of research efforts involves the study of power electronic device reliability and development of novel techniques with higher accuracy in health estimation of such devices. Until today, no other existing techniques can determine the number of lifted bond wires and their locations in a live IGBT module, although this information is extremely helpful to understand the overall state of health (SOH) of an IGBT power module. Through this research work, two emerging methods for online condition monitoring of power IGBTs and MOSFETs have been proposed. First method is based on reflectometry, more specifically, spread spectrum time domain reflectometry (SSTDR) and second method is based on ultrasound based non-destructive evaluation (NDE). Unlike traditional methods, the proposed methods do not require measuring any electrical parameters (such as voltage or current), therefore, minimizes the measurement error. In addition, both of these methods are independent of the operating points of the converter which makes the

application of these methods more feasible for any field application. As part of the research, the RL-equivalent circuit to represent the bond wires of an IGBT module has been developed for the device under test. In addition, an analytical model of ultrasound interaction with the bond wires has been derived in order to efficiently detect the bond wire lift offs within the IGBT power module. Both of these methods are equally applicable to the wide band gap (WBG) power devices and power converters. The successful implementation of these methods creates a provision for condition monitoring (CM) hardware embedded gate driver module which will significantly reduce the overall health monitoring cost.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a thesis titled "Measuring Level of Degradation in Power Semiconductor Devices using Emerging Techniques" presented by Abu Hanif, candidate for the Doctor of Philosophy degree, and certify that in their opinion it is worthy of acceptance.

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# DEDICATION

This dissertation is wholeheartedly dedicated to my beloved parents and my wife, who continually provide their moral, spiritual, emotional, and financial support. They have been my source of inspiration and gave me strength whenever I thought of giving up.

# CHAPTER 1

# INTRODUCTION

In recent years, power electronics has penetrated into many industrial applications such as renewable energy systems, hybrid-electric vehicles, locomotives, space missions, and so on. One common but major concern in these aforementioned systems is reliability, which is responsible for economic or safety considerations. As an example, in PV power generation systems, low reliability will increase maintenance costs and decrease system availability, and therefore, increase the levelized cost of electricity (LCOE), which will eventually affect its market penetration. A similar issue exists in offshore wind farms, which is not conveniently or inexpensively accessible for maintenance. In automobile, locomotive, and avionic applications, safety requirements impose nearly zero failure tolerance. Many approaches to address reliability problems of power electronic systems have been proposed and intensively studied for years. Mainstream efforts include the following: (1) standard-based reliability assessment [1-5]; (2) fault-tolerant topologies with redundant components [6-8]; (3) prognostics, health management (PHM), and condition monitoring approaches [9-13]; (4) designing highly reliable power electronic devices using advanced materials [14-16]. A nice review covering approaches 1 to 3 is presented in [17]. Among approaches 1 to 4, prognostics with lifetime estimation functionality is probably the most promising one. Approach 1 is more suitable in the design stage to get an estimation of overall system reliability. The commonly used reliability index is the mean time between failures (MTBF) [1]. Although approaches 2 and 4 enhance system reliability, they do not prevent failure from happening. Indeed, failure is never completely preventable. Therefore, the preferred way is to take action before a failure occurs, and lifetime prediction, if performed appropriately, can fulfill this mission. If used in

the design stage, a lifetime prediction model enables the designer to make proper decisions to ensure higher reliability. Used in applications, such a model can provide information of any remaining useful life or level of degradation. Previous studies show that a majority of power electronic system failures are due to component failures [18]. Therefore, it is a matter of paramount importance to detect the aging of the power semiconductor devices in order to estimate the state of health (SOH) of the overall converter circuit. In fact, a lifetime estimation of power electronic devices is a multi-disciplinary task that requires the cooperation of electrical engineers, mechanical engineers, and statisticians. We need to identify the failure precursor parameters as well as understand the dominant failure mechanisms in order to predict the lifetime of power electronic devices. A proper lifetime prediction method should then be selected. Finally, the lifetime prediction can be performed.

High-power converters are the key elements in a majority of power electronic applications. The applications include but are not limited to industrial power systems, FACTs devices, commercial cooling units, electric vehicles and utility systems, aircrafts, navy and commercial ships, military applications, and so on [19]. Many of these applications may have redundancy since they support invaluable systems for homes, transportation, business, and many more. However, some of the applications e.g., aircrafts may not have the luxury of redundancy due to the weight limitations and fuel efficiency. Therefore, any application requiring highly reliable power electronic system needs an accurate estimation of state of health. The most commonly used power converters are comprised of high power IGBTs and MOSFETs. These power electronic switches are the most failure prone components in the entire power converter circuit which was inferred from the industrial survey conducted by the authors in [20]. The results are shown in Figure 1.

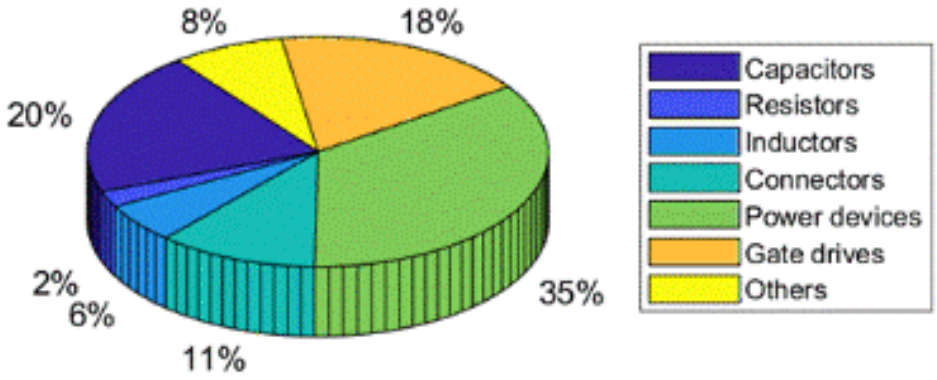



Figure 1: Survey of different components responsible for converter failure [20]

In high power applications, IGBTs are manufactured as a module which consists of more than one IGBT devices. These devices are connected through bond wires (BW) inside a module. In practical applications, these bond wires experience lift off, surface crack or heel crack etc., and the device degrades or poorly performs. In order to estimate the level of aging, electrical parameters such as current, voltage, etc. can be monitored and compared either off-line with, or in-situ alongside a healthy device. The most commonly used failure precursor parameters for an IGBT are threshold voltage ($V_t$), collector-emitter ON-state voltage ($V_{CEON}$), collector-emitter current ($I_C$), and case temperature of the semiconductor package ($T_C$) [21-33]. However, all of these precursor parameter-based condition monitoring techniques are either highly operating point dependent or extremely hard to perform in a live circuit when the semiconductor switches are pulsed with PWM signals [34-38]. In order to overcome these limitations, this research work proposes and institutes two non-invasive and in-situ methods to identify the degradation in power semiconductor devices/modules.

First method is based on spread spectrum time domain reflectometry (SSTDR) which has opened a new avenue in live condition monitoring, and can be found in many literature [39-43]. SSTDR based techniques have been successfully carried out in cable fault location in [39], and aircraft wiring fault location has been identified using SSTDR in [40]. The SSTDR technique has been effectively utilized to determine PV panel ground fault detection [39], and PV arc fault detection [42]. However, these existing methods cannot yet identify the location of the fault and if any bond wire has been detached from the substrate. In addition, these techniques are unable to detect degradation while the converter or device is live and they require accessing the high voltage nodes of the converter/inverter circuit.

In contrast, SSTDR based degradation detection has several advantages. First of all, the signal was applied at the gate-source interface of the module which will eventually make the measurement technique safer. Secondly, SSTDR frequencies (several MHz) are way above the converter's switching frequency, which ensures no interruption in the normal operation of the power converter. Using this method, any unwanted downtime can be significantly reduced by performing scheduled maintenance which will eventually provide the converter circuit a longer life resulting in a reduced overall cost .Through this research, we have overcome the limitations of the existing methods by applying the SSTDR test signal at the gate-source interface of the semiconductor device. The proposed method is able to detect aging in both Si and WBG semiconductor devices as well as the degradation of a converter/inverter circuit. The proposed method has also been validated by successful detection of the bond wire lift off related aging in IGBT modules. An RL-equivalent IGBT model of an Infineon dual pack module (FF450R12ME4) has been established for the first time in order to verify the experimental result obtained using SSTDR method. This equivalent circuit will help researchers to

understand not only the reflectometry based degradation detection but also the other researchers who will be using this module. In addition, degradation detection of SiC based power MOSFETs have been studied as well using this novel SSTDR technique.

Second method studies the degradation detection technique for IGBT modules based on ultrasound. Existing ultrasound based crack or void detection techniques are either too expensive and/or requires a fluid couplant to submerge the DUT/structure to be tested [44]. Confocal scanning acoustic microscopy (CSAM) based state-of-health identification is very popular in a semiconductor die and die-attach between the copper layer and substrate [45]-[47]. However, this technique cannot be used in a live circuit for package level degradation detection due to the size and medium constraint of the CSAM setup (requires the wafer to be submerged in water). In addition, it takes a long time to scan the device under test compared to any other existing condition monitoring method. Electromagnetic acoustic transducers (EMATs) does not require any couplant, however, they require high current injections for testing, and their efficiency is not as effective as the piezo-electric transducers [48]. In addition, the spread spectrum ultrasound technique requires highly precise transducer and couplant control to generate reasonably reliable results, and this technique has only been applied to large structures such as steel blocks [49]-[50]. The proposed ultrasound-based technique is able to detect bond wire lift off related adding in-situ and irrespective of the operating condition of the module or converter. This proposed method neither require any liquid couplant nor need measuring any precursor parameter. In addition, this method can be integrated with the gate driver module if properly scaled. Therefore, it is expected that the successful implementation of both of the methods will create a seminal impact in estimating remaining life especially for IGBTs.

## 1.1 Dissertation Outline

This dissertation is organized into eight (8) chapters. Chapter 2 explains the failure mechanism of the modern power electronic semiconductor devices and includes their classification. Chapter 3 describes the existing degradation detection and lifetime estimation methods and their advantages and disadvantages. Chapter 4 details the accelerated aging methods practiced by the industries and the researchers. SSTDR fundamentals and how this technique can be utilized in condition monitoring of power switching devices are discussed in Chapter 5. Chapter 5 also includes the development of an RL-equivalent of the IGBT bond wires and verifies the model by comparing the simulation and experimental results. Bond wire lift off related degradation detection of IGBT modules using ultrasound resonators has been discussed in Chapter 6 as well as the ultrasound propagation inside the IGBT module has been analytically modeled in this chapter. Chapter 7 includes three (3) case studies where SSTDR method has been utilized to identify the aging of SiC power MOSFETs as a discrete device as well as in a live converter circuit. Finally, the conclusions and future work are discussed in Chapter 8.

# CHAPTER 2

# FAILURE MECHANISMS OF MODERN POWER ELECTRONIC DEVICES

## 2.1 Introduction

Device degradation is a natural phenomenon. As a result, the semiconductor devices become vulnerable against the electro-thermal stresses and their durability and performance greatly downgrade. Therefore, it is an obvious question for the researchers that how these degradation related failures occur within the semiconductor devices. In other words, the mechanism behind the failures have been investigated by the scholars and, this chapter summarizes these failure mechanisms.

## 2.2 Failure Mechanisms

In general, power electronic devices comprise discrete devices and power electronic modules. These power electronic devices experience thermal, chemical, electrical, mechanical stresses, and degrade gradually, leading to a complete failure. Especially for hybrid electric vehicles (HEVs), the dominant reason of failure arises from thermal stress [51]. It is worth mentioning that vibration or shock also acts like a catalyst in the degradation process. Previous studies have grouped failure mechanisms of power electronic devices into two categories, namely chip-related (or intrinsic) failures and package-related (or extrinsic) failures [22], [52]. Intrinsic failure mechanisms are mostly related to electrical overstress, i.e., high current and high voltage, while extrinsic failures are commonly induced by thermo-mechanical overstress. The source of package related failure is the mismatch of coefficients of thermal expansion (CTE) of the different materials. It is worth mentioning that the failure mechanisms that will be introduced here are by no means comprehensive. Rather, the main purpose of this chapter is to provide the basis of understanding the underlying reasons for device failures. More

comprehensive surveys on power electronic device failure mechanisms can be found in [22], [53].

Although new technologies of die attach and bond wire materials, as well as advanced Silicon carbide (SiC) power modules, tend to tremendously increase device reliability and hence, can minimize or even eliminate many failure mechanisms; they are still at an embryonic stage or could be prohibitively expensive [16], [54]. As a result, manufactured wafers of SiC modules contain many defects. An SiC metal–oxide–semiconductor field-effect transistor (MOSFET) has a very vulnerable gate oxide layer because it experiences an electric field strength almost three times stronger compared to the similar rated Si devices [55]. Therefore, conventional power electronic devices are likely to dominate the market in the near future. Figure 2 shows the failure mechanism classification for power semiconductor devices and the following sections will briefly explain them.

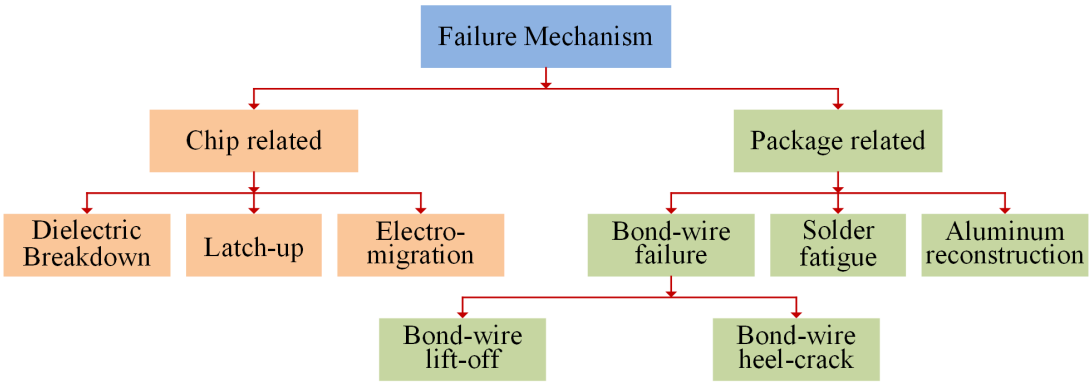



Figure 2: Failure mechanisms of power electronic devices

### 2.2.1 Chip-related failure mechanisms

A semiconductor chip is the nucleus of the device. This chips are manufactured in the form of wafers, and then they are packaged to make it suitable for field applications. Therefore,

the failures of the semiconductor devices can be classified into two major types: chip-related and package related. Chip-related failure can be further classified into several types as described below:

#### 2.2.1.1 Dielectric Breakdown

We refer to a dielectric breakdown, which results from gate oxide degradation due to accumulated defects, as a time dependent dielectric breakdown (TDDB) [52], [56]. Three defect generation mechanisms are identified in [57]: impact ionization, anode-hole injection, and trap creation. Catastrophic/acute dielectric breakdown occurs when the device experiences severe electrical or thermal stress, i.e., over voltage and electrostatic discharge (ESD) [52], [58]. Increased gate current and decreased drain current can be found in MOSFET after a dielectric breakdown [43].

#### 2.2.1.2 Latch-up

Latch-up can happen to both insulated-gate bipolar transistors (IGBT) and MOSFETs if the parasitic thyristor or bipolar junction transistor (BJT) structure is triggered, causing a loss of gate control. If the latch-up is not promptly removed, any high current will eventually destroy the device [56], [59]. High dV/dt was identified as the cause of a MOSFET [60] and IGBT [61] latch-up. In [62], operating the IGBT at a high temperature was the primary reason that induced the latch-up.

#### 2.2.1.3 Electro-migration

Metal migration, caused by high current density in silicon interconnects [22], [52], [58], is the definition of electro-migration. As a result, voids form between metal connections and cause increased resistance or an open circuit. Such degradation is rarely observed in power electronic devices due to large contact areas [22].

### 2.2.2 Package-related failure mechanisms

Since high power applications widely use power modules, the failure mechanisms discussed here are mainly consistent with power modules only. It should be noted, however, these failure mechanisms may also be applicable to low power devices. Power modules are usually constructed in multilayer structures, as shown in Figure 3. Silicon chips are soldered onto a direct bonded copper (DBC) substrate that provides necessary electric insolation, and the substrate is then soldered onto a base plate. Al bond wires are normally used to connect different chips and form terminals. Three major failure mechanisms are reported in the literature, namely bond wire failure, solder fatigue, and aluminum reconstruction [53].

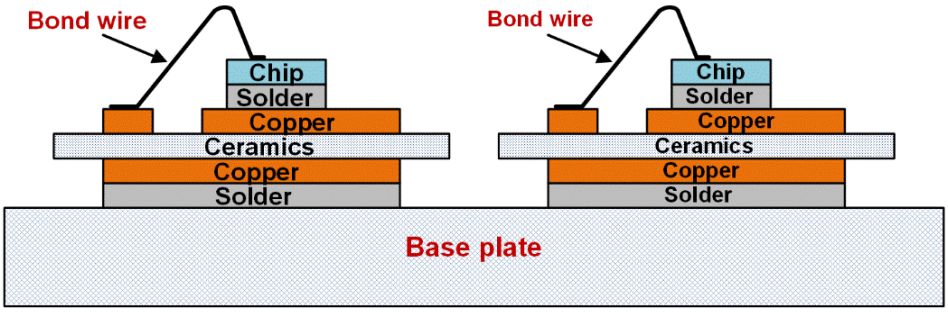



Figure 3: Typical multilayer structure of a power module

#### 2.2.2.1 Bond wire failure

Bond wire failures can be further classified into two types: (1) bond wire lift-off and (2) bond wire heel cracking. The main reason for bond wire lift-off is the mismatch of a coefficient of thermal expansion (CTEs) between Si and Al interfaces. During thermal cycling, a crack initiates and propagates in the interface between the wire and device and finally leads to a bond wire lift-off. Fracture fatigue is considered as the main reason for bond wire heel cracking. Displacement at the top of a bond wire loop creates an alternation in the bending

angle when a device is subjected to thermal cycling. Fatigue by thermal cycling is rare in advanced IGBT modules [53].

#### 2.2.2.2 Solder fatigue

As shown in Figure 1, there are two solder layers in a typical power module, i.e., one between the Si device and DBC and another between the substrate and baseplate. A larger CTE mismatch in between the substrate and baseplate makes it more susceptible to solder fatigue. Thermal and power cycling will create voids and cracks in solder-attached layers that propagate as the thermal cycle increases [63]. The voids increase the thermal impedance, resulting in a higher temperature in the die that accelerates the propagation of voids. In other words, a positive feedback loop is formed between die temperatures and voids propagation. Eventually, the large amount of heat can cause damage to the device. As stated previously, overheating can be the root cause of latch-up and failing to turn on [64]. Hence, package-related failures can sometimes induce chip-related failures.

#### 2.2.2.3 Aluminum reconstruction

Aluminum reconstruction refers to the aging mechanism of the metallization layer deposited on the silicon chips [65]. Different CTEs, between the aluminum and Si, induce compressive and tensile stresses in the aluminum layer that can exceed the elastic limit and cause aluminum reconstruction. This failure mechanism can be effectively prevented by using a passivation layer [53].

A correlative table can be constructed based on the failure modes and the failure mechanism occurs in an IGBT module to illustrate the potential locations of failure, causes, and the parameters affected due to the failure [66]. They are summarized in Table I.

Table I Comparison between failure mechanisms [66]

| Failure mechanism | Location | Causes | Modes | Parameter affected |
|---|---|---|---|---|
| Time dependent dielectric breakdown (TDDB) | Oxide layer | 1. Over voltage<br>2. High temperature<br>3. High electric field | 1. Increased leakage current<br>2. Loss of gate control<br>3. Short circuit | $V_{th}$ |
| Latch-up | Silicon Die | 1. Over voltage<br>2. Irradiation<br>3. High electric field | 1. Device burnout<br>2. Loss of gate control | $V_{CEON}$ |
| Hot electrons | Oxide<br>Oxide/substrate interface | 1. High current density<br>2. Over voltage | High leakage currents | $V_{th}$ |
| Bondwire/Solder fatigue | Bondwire /Solder | 1. High current density<br>2. High temperature | Open circuit | $V_{CEON}$ |
| Delamination of die attach/Voiding | Die attach | 1. High current density<br>2. High temperature | Open circuit | $V_{CEON}$ |

## 2.3 Conclusions

In field applications, power semiconductor devices or modules undergo one or more failure mechanisms simultaneously. Therefore, it is common to occur both bond wire lift-off and heel crack or die-electric breakdown and solder fatigue at the same time. As a result, it becomes difficult to identify the underlying reasons behind the failures. However, there exists several degradation detection techniques which can identify the aging of the devices, of course having both pros and cons, and those methods will be discussed in the following chapter.

# CHAPTER 3

# EXISTING DEGRADATION DETECTION & LIFETIME PREDICTION TECHNIQUES

## 3.1 Introduction

Lifetime prediction or reliability analysis of power electronic devices has emerged as one of the distinguished branches in engineering since the early 1950s [67]. The essence of reliability analysis evolved from the electronic tubes' failure that occurred during World War II [68]. Since then, numerous methods and standards have been used toward the analysis of the devices, components, and/or system failures that specifically occurred because of the electronic or power electronic components. In 1956, "Reliability Stress Analysis for Electronic Equipment", TR-1100, contained a mathematical model based on the component failure rate. In 1962, the first Military Handbook-217 (MH-217), which derived from this, was published to standardize the test protocol [68]. Afterwards, a multiple version of MH-217 came out in order to improve the reliability assessment models and keep up with the newest technology. It made the MH-217 standards much more complex. Later, in the 1980s, industry specific models derived from this handbook. Finally, these empirical data based lifetime models (MH-217F) were formally cancelled due to the increased complexity in integrated circuits and components [124]. The physics-of-failure (PoF) based models that developed in 1962 and gained popularity in the 1990s have since been used extensively in the lifetime prediction of both power electronics and micro-electronics [68]. The PoF identified that the root cause of failure mechanisms was influenced by environmental stress and the empirical lifetime method approaches identified the failure statistically. A constructive comparison between these two methods is shown in Table II.

Table II Comparison between failure methods [68]

| Method | Advantages | Limitations |
|---|---|---|
| Empirical model | 1. Reflects actual field failure rates and defect densities<br>2. Can be a good indicator of field reliability | 1. Difficult to keep up-to-date<br>2. Difficult to collect good-quality field data<br>3. Difficult to distinguish cause vs effect for s-correlated variables (e.g., quality vs environment) |
| Physics-of-failure (PoF) model | 1. Modeling of specific failure mechanisms<br>2. Valuable for predicting end-of-life for known failure mechanisms | 1. Cannot be used to estimate field reliability<br>2. Highly complex and expensive to apply<br>3. Cannot be used to model defect-driven failures<br>4. Not practical for assessing an entire system |
| Test data | 1. Reflects the actual reliability<br>2. Test data can be collected and applied before the system is deployed | 1. Translations to field stresses required, which requires acceleration models and adds uncertainty to the estimate |

Generally, lifetime prediction methods for power electronic modules are twofold. The first method is based on failure mechanisms. Although various failure mechanisms have been identified, the existing lifetime prediction models mainly focus on package related failures. Such models can be classified into two categories: (1) empirical models and (2) physics-of-failure (POF) based models. Most of these models describe a number of cycles to failure ($N_f$) as a function of failure-relevant parameters such as junction temperature swing ($\Delta T_j$) and mean junction temperature ($T_m$). The second method is based on failure precursor parameters. This method is an essential part of the prognostics and health management (PHM) approach, and is always implemented in applications to provide a remaining useful life (RUL). Compared to the first method, this method provides the remaining useful time in real-time units, such as minutes, days, etc., rather than in the number of cycles to failure.

### 3.2 Failure mechanism-based lifetime prediction

Existing models mostly predict two failure mechanisms, namely, bond wire failure and solder fatigue. It should be noted, however, that the models for each failure mechanism are not mutually exclusive because both failure mechanisms are due to a CTE mismatch in the interface areas. Indeed, some models are interchangeable. Generally, lifetime prediction methods for power electronic modules are twofold. The first method is based on failure mechanisms. Although various failure mechanisms have been identified, the existing lifetime prediction models mainly focus on package related failures. Such models can be classified into two categories: (1) empirical models and (2) physics-of-failure (PoF) based models. Most of these models describe a number of cycles to failure ($N_f$) as a function of failure-relevant parameters such as junction temperature swing ($\Delta T_j$) and mean junction temperature ($T_m$). The second method is based on failure precursor parameters. This method is an essential part of the prognostics and health management (PHM) approach, and is always implemented in applications to provide a remaining useful life (RUL). Compared to the first method, this method provides the remaining useful time in real-time units, such as minutes, days, etc., rather than in the number of cycles to failure.

#### 3.2.1 Bond wire failure models

As discussed in the previous section, bond wire failures can occur at a bonding interface or bond wire heel. Different models of bond wire failures will be introduced in this section. Empirical models will be introduced first, followed by the physics of failure models.

##### 3.2.1.1 Empirical lifetime models

Empirical models were initially developed by statistically studying the test data of accelerated aging experiments, which will be discussed in the next section. Due to different

test protocols and module types, the dominant failure mechanisms, observed for different power electronic devices, are different. The following models are classified in the category of bond wire failures because during the accelerated aging experiments from which these models were developed, the dominant failure mechanism observed was bond wire failure. For this reason, the accuracy of such models can only be guaranteed when used in situations similar to the test conditions from where the models were "born". One common feature of these models is that they relate lifetime to junction temperatures.

An empirical lifetime model of an IGBT module is proposed based on the fast power cycling results, in other words, accelerated aging based test results [69] as shown in equation (1):

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot \exp\left(\frac{Q}{R \cdot T_m}\right) \quad (1)$$

where $R$, being the gas constant (8.314 J/mol.K) and $T_m$ in Kelvin make $A$ = 640, $\alpha$ = -5, and Q = $7.8 \times 10^4$ J/mol.

Figure 4 is attached to illustrate the results obtained in [69] using equation (1). The parallel shift is a clear indication of thermal mechanism, and hence, it was combined with the Arrhenius approach.

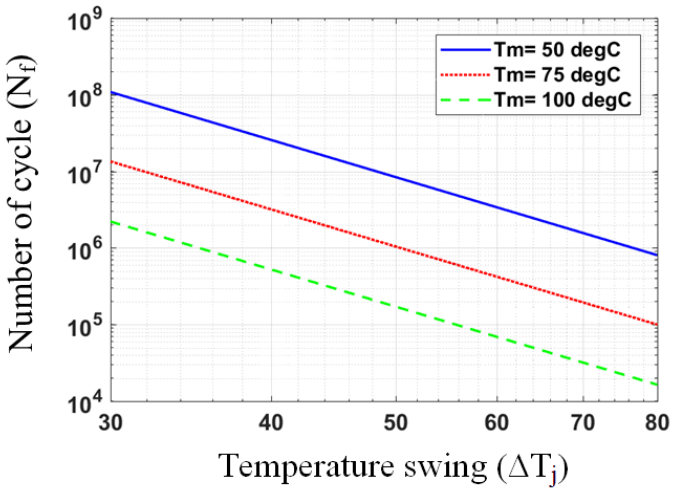



Figure 4: Number of cycles vs. temperature swing [69]

Since the model was obtained from the power cycling test, these parameters are only applicable to the conditions that are within the specified range of the test, i.e., $\Delta T_j$ between 30K and 80K. If this model were used for another module type or different test protocols, the model parameters would need to be recalibrated via an accelerated aging test. This model is somewhat coarse because it only considers the effect of $\Delta T_j$ and $T_m$. A similar experiment was performed in [70] for an IGBT module to investigate die-attach solder fatigue due to a low swing in the junction temperature. The lifetime modeling was based on the Coffin-Mansion-Arrhenius model that also considers the effect of $\Delta T_j$ and $T_m$ only. Intuitively, other parameters such as power-on-time can also affect the aging process. A more comprehensive model that considered power-on-time, chip thickness, bonding technology, diameter of the bonding wire, and current-per-bond wire was proposed in [71].

By performing regression analysis on a large set of cycling data, equation (2) was extended to the form of

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot \exp(\frac{\beta_2}{T_{low}}) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad (2)$$

Where, $t_{on}$ is the power on time, $I$ is the current-per-bond wire, $V$ is the blocking voltage, and $D$ is the bond wire diameter. Parameters $\beta_1$ to $\beta_6$ are obtained from statistical data. Like any empirical model, the validity of the model is only guaranteed within the range of selected data, and the authors of [71] also suggested using the model with caution.

#### 3.2.1.2 Physics-of-failure-based lifetime models

The model with the simplest form within this category is probably the Coffin-Manson model, which assumes that plastic strain is the main cause of the bond wire lift-off and the elastic strain is negligible. Since the model emphasizes the effects of plastic strain, it is also referred to as the plastic strain-based model [72]. The model is shown in equation (3) [73], [74].

$$N_f = C_1(\Delta\varepsilon_p)^{-C_2} \quad (3)$$

Another form of equation (3), which was initially applied to bond wire failure and presented in paper [53], is shown in equation (4). It can be obtained by substituting $\Delta\varepsilon_p$ in (4) by $L \cdot \Delta\alpha \cdot \Delta T$. It needs to be mentioned that this model is only valid when the peak temperature does not exceed 120˚C. From the deduction procedure presented in [53], $\Delta T$ in equation (4) should be the temperature swing at the bond wire-chip interface rather than the junction temperature.

$$N_f = a(\Delta T)^{-n} \quad (4)$$

The Coffin-Manson model is suitable for low cycle fatigue. As for high cycle fatigue, the Basquin equation is used to describe damage induced by stress range Δσ [75]. This model is presented in equation (5), where $C_1$ and $C_2$ are material-specific parameters.

$$N_f = C_1(\Delta\sigma)^{-C_2} \tag{5}$$

Another strain based model is shown in equation (6), where strain-intensity-factor range $\Delta K_\varepsilon$ is selected for the failure metric [76]. This paper aims at investigating thermal fatigue under low temperature fluctuation, i.e., $\Delta T$ under 40℃. The crack growth rate is calculated from the strain intensity factor by Paris' law. It assumes that failure would happen if a critical crack length is reached.

$$\frac{da}{dN} = C(\Delta K_\varepsilon)^n \tag{6}$$

$$N_f(I) = \frac{w_{pl}^{cr}}{w_{pl}(I)} \tag{7}$$

Equation (7) shows an energy based lifetime prediction model for Al ribbon bonds subjected to a heel crack failure mechanism [77], in which $w_{pl}^{cr}$ is the energy limit and $w_{pl}(I)$ is the energy dissipation per cycle under current *I*. The model assumes that the ribbon can withstand a certain amount of energy dissipation before a sudden failure. In addition, the effects of residual stress on the crack evolution were not considered in this model, which this paper later proves to have a negative impact on the ribbon lifetime. A comparison of the lifetime prediction between this model and the Coffin-Mansion model shows discrepancies. Although the model itself seems logical, there could be some over simplifications or misjudgments during model parameterization.

### 3.2.2 Solder fatigue models

Before introducing the lifetime prediction models, it is necessary to introduce the failure criteria first. It is not necessary to introduce bond wire failure criteria because they are self-evident; a bond wire fails when it is lifted or its heel cracks. As for fatigue, however, the definition of failure corresponds to a point when a certain percentage of solder becomes damaged.

#### 3.2.2.1 Empirical lifetime models

An early attempt to empirically describe the lifetime of leaded solder subjected to a thermal cycling test was proposed by Norris and Landzberg, and hence called the Norris-Landzberg model, as shown in equation (8) [78]. This model was widely used for defining the acceleration factor (AF) to map the accelerated lifetime test (ALT) time scale and lifetime in the field application [79].

$$N_f = A \cdot f^{-n_2} \Delta T^{-n_1} \cdot \exp(\frac{E_a}{K \cdot T_{max}}) \qquad (8)$$

In [80], this model was modified for lead-free solder material by a recalibration process using experimental data. The modification added a new term to the original equation considering the dynamic behavior of solder materials. This model is presented in equation (9), where $corr(\Delta T) = A ln(\Delta T) + B$, $A$ and $B$ are material dependent constants, and $c$ is a variable dependent on a thermal cycling profile.

$$N_f = A \cdot f^{-n_2} \Delta T^{-n_1} \cdot \exp\left(\frac{E_a}{K \cdot T_{max}}\right) [corr(\Delta T)]^{-1/c} \qquad (9)$$

Another modified version of equation (9) is presented in [81], in which the frequency term is replaced by the parameter $t_{hot}$ representing the time per cycle that the device is hot. The model is presented by equation (10).

$$N_f = A \cdot (\frac{1}{t_{hot}})^{-n_2} \Delta T^{-n_1} \cdot \exp(\frac{E_a}{K \cdot T_{max}}) \quad (10)$$

### 3.2.2.2 Physics-of-failure (POF) based lifetime models

As mentioned earlier, a clear boundary does not exist between solder fatigue models and bond wire failure models when the materials' physical properties are considered. The first model to be introduced is essentially the same as equation (3), but written in a more institutive form as shown in equation (11) [82] - [84]:

$$N_f = \frac{L}{a(\Delta \varepsilon_p)^b} \quad (11)$$

Where, $L$ is the length of the solder interconnect, $N_f$ is the number of cycles needed for the crack length to reach $L$, $\Delta \varepsilon_p$ is the average accumulated plastic strain per cycle, and $a$ and $b$ are material-dependent constants.

Fig 5 has been included using equation (11) to show the correlation between L and $N_f$ for two plastic strain values ($\Delta \varepsilon_p$) of an SnAg solder joint. Constants, a and b are given as 0.00562 and 1.023 for SnAg solder [85]. Since the failure is defined by the moment when the crack length reaches 20% of the solder thickness, the maximum value of L used in the equation should be 0.1mm because the solder thickness is 0.5 mm. According to these plots, the number of cycles is strongly related to the accumulated plastic strain value. However, this value of $\Delta \varepsilon_p$ is a function of the temperature swing (ΔT) and the mean temperature (Tm) of the experiment [85] – [87]. Hence, once the operating condition is defined, i.e., the mean temperature and the temperature swing are known, the number of cycles can be estimated in order to study the solder fatigue phenomenon.

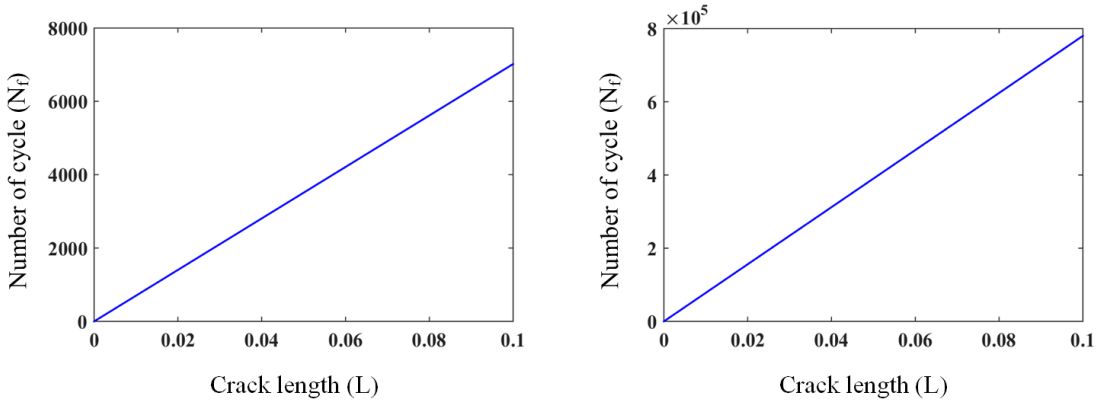



Figure 5: Number of cycles vs. crack length.

Another plastic strain based model has been described in [88]. Similar to (3), its validity relies on the assumption that elastic strain has little effect on solder fatigue. A shear strain-based model was proposed by Solomon [89], shown in equation (12), where $C$ and $n$ are material dependent constants, and $\Delta\gamma_p$ is the plastic shear strain range.

$$N_f = C(\Delta\gamma_p)^n \tag{12}$$

A model to predict large solder joint failure is given in (13), where $L$ is the lateral size of the solder joint, $\Delta\alpha$ is the CTE mismatch, $\Delta T$ is the temperature swing, $c$ is the fatigue exponent, $x$ is the thickness of the solder, and $\gamma$ is the ductility factor of the solder [53].

$$N_f = 0.5\left(\frac{L\Delta\alpha\Delta T}{\gamma x}\right)^{1/c} \tag{13}$$

Strain-based solder fatigue models are criticized as inadequate, because the solder lifetime may also be a function of stress. Therefore, an energy based approach is considered as an alternative [90]. The most widely used definition of energy to determine failure is called strain-stress hysteresis energy. Similar to the energy based models for bond wire failures, the

rationale of energy based models is shown in equation (14), where $E_f$ is the total energy to failure, $E_c$ is the energy per cycle.

$$N_f = \frac{E_f}{E_c} \tag{14}$$

An early attempt was presented in [91] to analyze the data for 60Sn-40Pb solder. A proposal for a recent application to estimate the lifetime of an IGBT module in an automotive application is shown in [92], where the lifetime of the module under a mission profile was estimated with the total known deformation energy (energy to failure).

So far, one may have found that all POF based models have some parameters to be determined. In theory, module geometry and material properties are necessary to determine the unknown parameters. Therefore, it might be more appropriate to categorize them as semi-empirical models since they also need parameterization.

### 3.2.3 Real-time lifetime estimation

Now that we have the lifetime prediction models as mentioned above, one may expect to estimate the lifetime or level of degradation of a power device in real applications; however, some obstacles still need to be tackled. The first question is which type of model do we use, the empirical model or POF model? In both experiment and simulation, temperature is more easily accessible than mechanical quantities, i.e., plastic strain. Parameters such as plastic strain and strain-stress hysteresis energy are usually obtained from thermo-mechanical finite element analysis (FEA). FEA not only requires the temperature profile of the device, but also needs the material properties and device geometry. In other words, choosing POF models requires one more intensive simulation step than choosing the empirical models. This is because the empirical models directly utilize device temperature to estimate the number of cycles to failure. Whichever model is chosen, this next problem is inevitable. The models only

take specific conditions into account, i.e., a fixed mean junction temperature and temperature swing, but power modules experience a time varying load profile. To address this problem, Miner's rule, which says the damage effect can be linearly accumulated, is commonly employed [72], [93] – [96]. The general form of Miner's rule is shown in equation (15), where $LC$ is the lifetime of the device that has been consumed in a percentage, $n_k$ is the actual cycle of a certain operating point, and $Nf_k$ is the cycle to failure of the operating point.

$$LC = \left(\frac{n_1}{Nf_1} + \frac{n_2}{Nf_2} + \frac{n_3}{Nf_3} + \cdots + \frac{n_k}{Nf_k}\right) \times 100\% \qquad (15)$$

To obtain $n_k$ at a certain operating point, we need cycle counting methods to extract useful information from the device's temperature history. There is not a uniformed definition to count the thermal cycles from a random temperature profile. Various cycle counting methods are found in [97]. The most widely used one is the rain-flow counting method [98] that groups local minima and maxima to an equivalent cycle. In [92], several definitions of a temperature cycle are discussed. The cycle counting results of different definitions from the same temperature profiles are slightly different and result in deviations in the lifetime prediction results. Therefore, selecting a proper cycle counting method can help improve the estimation accuracy. However, in the literature, there is no comprehensive comparison of which method leads to a better estimation under what condition. Conventionally, the rain-flow method is used off-line because it requires the entire load profile history. As it can only process data in chunks, if requires a large data storage system that is inconvenient to implement in a real-time application. To tackle this problem, a real-time rain-flow counting approach is proposed in [93] using a recursive algorithm.

### 3.3 Failure precursor-based lifetime prediction

Failure precursors are the parameters that change with device degradation, and thus can indicate an imminent failure. The literature identifies various failure precursors of power electronic devices by accelerated aging tests. Typical ones are summarized below.

#### 3.3.1 Failure precursors of power electronics devices

The most significant aging indicator for power MOSFETs [99] is an increase in ON-state resistance. We find similar observations in [100] – [102]. The authors in [103] concluded that a power MOSFET completely fails if the initial value of $R_{DSON}$ increases by 10%-17%. Increased gate threshold voltage of an aged power MOSFET was discovered in [104], [105]. In [62], increased threshold voltage was observed in an aged IGBT. The ringing characteristic is used as an indicator of IGBT aging in a motor drive in [106]. Brown et al. [107] identifies the turn-OFF time as an indicator of an IGBT latch-up. In addition, the rise time and fall time increase with the level of aging as reported in [108]. ON-state voltage has been identified as an IGBT failure precursor in [9], [62], [109] – [113]. However, this quantity does not monotonically increase or decrease with respect to degradation. In [62], the ON-state voltage was reported as going down due to aging, while in [109], [110], an increase was reported. In [9], a decrease was observed followed by an increase in collector-emitter voltage ($V_{CE}$). This seeming contradiction lays in two competing aging mechanisms, namely, solder fatigue and bond wire degradation. The $I_C$-$V_{CE}$ characteristic curve has a negative temperature coefficient below a crossover and a positive one above it. Solder fatigue will increase the thermal impedance, and hence, increases the temperature. If the IGBT is operating below the crossover, an increased temperature will result in a decreased $V_{CE}$, as observed in [9], [62]. However, if bond wire failure becomes dominant or the IGBT is operating above the crossover, an

increased $V_{CE}$ should be observed. It might be concluded that at a low collector current, $V_{CE}$ is more sensitive to temperature, while at a high collector current, $V_{CE}$ is more sensitive to bond wire degradation.

Experimental results obtained from the accelerated aging test conducted in [114] support the above statement. In this paper, an IGBT bond wire lift-off was studied and $V_{CE}$ was going up with the bond wire lift-off. Thermal stress was up to 120°C for the die, and it was induced from a power cycling test. A junction-to-case thermal impedance increase has been characterized as one of the precursors for solder layer degradation of the IGBT power module in [115]. Apart from the thermal impedance, the temperature of the chip surface also increases with the level of solder fatigue.

### 3.3.2 Precursor parameter measurements

Precursor parameter measurement is indispensable to predict the RUL, but such a measurement is confronted with many challenges, especially in a live converter. Aside from the additional sensors needed to perform measurements and corresponding change in the circuit structure, the high resolution measurement needed for the sensors to extract a small deviation from a high voltage high current operating context is computing intensive. Moreover, a high switching frequency induced noise imposes a burden on measurement accuracy, and most failure precursors depend on the operating point (e.g., temperature and load current) that must be taken into account during measurement. More importantly, it is preferred that such a measurement does not alter the normal operation of the system. An advanced gate drive with the capability to measure various voltages and currents within the device has the potential to resolve the aforementioned difficulties [116] – [119], but their applications in prognostics of power electronic devices have yet to be explored.

Most of the existing precursor measurement methods require a measurement window inserted in the converter's normal operation. For example, in [120], on-line monitoring of an IGBT module under power cycling stress was studied. An H-bridge inverter comprising four IGBTs was stressed by thermal cycling induced by low frequency PWM power cycling. A periodic measurement of $V_{CE}$ was carried out at the fixed current (110A) and the fixed junction temperature (125ºC). To achieve this, the normal inverter operation was interrupted by a particular switching pattern that made the current and junction temperatures vary around the fixed values. Then, the values at the fixed operating point were obtained by an interpolation.

A similar accelerated test was conducted in [121] on an H-bridge converter constructed from high power IGBTs. Aging was induced by a power cycling method with a peak current of 890A while the IGBT was attached to the cooling system. Glycol with water was used as the liquid coolant. The authors defined the $V_{CE}$ and the anti-parallel diode's forward voltage drop ($V_f$) as the aging precursor and monitored them online during the converter operation. Although the device under test (DUT) was the IGBTs on the first leg, the test set-up used in this paper initiated degradation on devices of the second and third leg but the rate of degradation was at a much slower compared to the first leg.

In [43], Nasrin proposed a way of utilizing spread spectrum time domain reflectometry (SSTDR) to evaluate resistance-based degradation in power converters. Impedance discontinuities can be detected by observing the correlated output from SSTDR. In general, an abrupt change in impedance will result in a positive or negative peak in correlated output. In turn, the peak value can be used to back calculate the impedance. However, this method can only work when the device was isolated from the converter or the converter is not pulsed with PWM signal. In addition, this method limits the application to the rated voltage of the SSTDR

hardware (1000V) since the test points are located at the drain-source interface of the power devices. Therefore, it is not feasible to apply SSTDR signal from the drain or collector terminal while the converter is live.

### 3.3.3 Remaining useful life prediction

A failure precursor-based lifetime prediction requires a predefined failure threshold, i.e., 30% increase of $R_{DSON}$ [100]. This lifetime prediction method is actually a part of the prognostic approach. In general, prognostic algorithms can be classified into a model-based approach, data-driven approach, and hybrid approach. Using a hybrid approach has the following advantages: (1) easy to implement due to the simplicity of the model, (2) ability to capture the complex systems, thanks to data-driven methods, and (3) ability to identify intermittent failures. In [104] and [122], this approach was applied to MOSFET and IGBT, respectively, where an empirical model was obtained by offline regression analysis and then fitted into an online prediction algorithm (in these cases, particle filtering), which then further tuned the model by tracking the system behavior. The RUL was predicted by comparing the failure precursor and the end-of-life threshold. A similar method was later adopted in [64], where a two-step prognostic approach was proposed. In the first step, Mahalanobis distance (MD) was used to detect anomalies in the device. If an anomaly was observed, particle filtering was used to determine RUL. Compared to the failure mechanism-based predictions, the advantage of this method is that knowledge of the entire history of the device is not mandatory. Instead, a certain amount of discrete measurement of failure precursor is sufficient. The major limitation of this method though, is that the empirical model was developed from an accelerated aging test, which means the RUL prediction was given in an accelerated time scale. Therefore, to use this method in the field application, a mapping from the accelerated time

scale to real-time scale is necessary. In [123], different acceleration factors (AFs), i.e., temperature acceleration, voltage acceleration, temperature cycle acceleration, and humidity acceleration are presented. Despite these AFs having the potential to facilitate mapping from an accelerated life test to a real-time lifetime estimation, the exactitude of such AFs has not been rigorously validated.

From the above discussion, a constructive comparison can be made for the two major lifetime prediction methods: (1) Failure mechanism-based, (2) Failure precursor-based Table III shows this comparison summary.

Table III Comparison between Lifetime Prediction Methods

| **Terms/characteristics** | **Failure mechanism-based** | **Failure precursor-based** |
|---|---|---|
| Aging type | Package related | Chip related |
| Aging information | Based on number of cycles ($N_f$) | Based on time unit (minutes, hours, days etc.) |
| Measured parameter | Junction temperature ($T_j$), strain | Voltage, current, temperature, resistance, etc. |
| External sensor | May or may not require | Always required |
| Cost | Less expensive | Expensive |
| Operating point | Non-dependent | Dependent |
| Device history | Entire history required | Not required |

### 3.4 Conclusions

It is clear from the above discussion that every degradation detection method has some advantages and disadvantages over another method. However, it should be noted that two measurements are necessary in order to quantify the aging of the device: reference data for healthy device and the data recorded after the device undergoes aging. In field applications,

the power electronic devices experience gradual degradation over the course of operation and it will require years for a device to experience significant aging that can be detected by the existing techniques. That is why a method is necessary in order to quicken the aging of the device so that the degradation can be studied and detection technique can be proposed within few days instead of waiting for months, even years. This technique is termed as accelerated aging method and will be discussed in the following chapter.

# CHAPTER 4

# ACCELERATED AGING METHODS

## 4.1 Introduction

An accelerated life test is an indispensable technique for reliability oriented issues. It can be performed for different purposes such as testing device reliability, investigating failure mechanisms, identifying failure precursor parameters, parameterizing lifetime prediction models, etc. In general, power cycling and thermal cycling are most commonly adopted accelerated aging methodologies. These methods aim at qualifying chip and package related reliability issues. During power cycling tests, devices are heated by the power loss generated inside the package; also referred to as active temperature cycling. On the other hand, thermal cycling created externally by virtue of a thermal chamber is called passive temperature cycling. Additionally, chronic thermal and electrical overstresses are also reasons for immediate failures. These methods have been used separately or in combination to study the reliability of power devices. This chapter presents existing accelerated tests. The classifications are purpose-based.

## 4.2 Device qualification tests

Qualification tests are widely used by semiconductor manufacturers to test the reliability of their products [125] – [128]. Many industrial standards exist, i.e., IEC60747, IEC60749, IEC60068, AEC-Q101, and JESD-47. An example of the Semikron test standards is shown in Table IV [125]. These standards provide a common platform to compare and improve the quality of devices. However, comparison between the products from different manufacturers is not straightforward because the test standards employed by different

manufacturers are diverse. In addition, most standards are for general purposes and hence, may not be well suited for specific usage profiles.

Table IV Standard tests for the qualification of SKiM modules [125]

| Test standard | Test conditions | Description |
|---|---|---|
| *IEC 60747* | 1000 h, $V_{CE}$ = 95% $V_{CEmax}$, $T_c$ = 160 °C | High temperature reverse bias test (HTRB) |
| *IEC 60747* | 1000 h, ± $V_{GEmax}$, T = 175 °C | High temperature gate bias (HTGB) |
| *IEC 60068-2-67* | 1000 h, 85 °C, 85 % RH, $V_{CE}$ = 80 % $V_{CEmax}$ (maximum value of $V_{CEmax}$ =80V) $V_{GE}$ = 0V | High humidity high temperature reverse bias (THB) |
| *IEC 60068-2-2* | 1000 h, + 135 °C | High temperature storage (HTS) |
| *IEC 60068-2-1* | 1000 h, - 40 °C | Low temperature storage (LTS) |
| *IEC 60068-2-14 Test Na* | 500 cycles, - 40 °C to + 125 °C | Thermal cycling (TC) |
| *IEC 60749-34* | 25,000 load cycles, ΔTj = 110 K | Power cycling (PC) |
| *IEC 60068-2-6 Test Fc* | Sinusoidal sweep, 10g, 2 h per axis (x, y, z) | Vibration |
| *IEC 60068-2-27 Test Ea* | Half sine pulse, 100g, 3 times each direction (x, y, z) | Mechanical shock |

### 4.3 Test for exploring failure mechanisms or failure precursors

Aside from industrial standards, other accelerated tests that target specific failure mechanisms or precursors can be found in the literature. In the 1990s, a few projects on enhancing the reliability of IGBT modules for traction applications were initiated in European countries. Typical projects were Leistung Elektronik Systemtechnik Informations Technologie (LESIT) (1994–1996) and reliability of advanced high power semiconductor devices for railway traction applications (RAPSDRA) (1996–1998).

These projects proposed some standardized accelerated tests for IGBT modules in traction applications and empirical lifetime prediction models were originally developed

therein. They exclusively studied package related failure mechanisms, i.e., bond wire failures and solder fatigue. The LESIT project purposed a "fast power cycling test" for IGBT modules in traction applications [69]. The IGBT under test was mounted on a water-cooled heat sink with a constant gate voltage and a periodical (2sec) load current. The power cycling test was aimed to create a swing in junction temperature $T_j$ that caused device degradation. More comprehensive test conditions (purposed by RAPSDRA) are in Table V [129] in which three test protocols are defined. It was found that bond wire failures are more susceptible to power cycling 1 (fast cycling) while solder fatigue is generally caused by slow cycling, namely power cycling 2 and thermal cycling. This test standard and its variants were used extensively to evaluate the reliability and failure mechanisms of different IGBT modules [129] – [134].

Table V RAPSDRA test protocols [129]

| **Reliability test** | **Test conditions** | **Estimated testing time** |
|---|---|---|
| Power cycling 1 (active) | $T_{min}$=55˚C<br>ΔT=50˚C, 70˚C<br>$I_c=I_{cnom}$, $t_{cycl}$=3sec | 3,000,000*3sec=104days |
| Power cycling 2 (active) | $T_{min}$=55˚C<br>ΔT=50˚C, 70˚C<br>$I_c=I_{cnom}$, $t_{cycl}$=1min | 100,000*1min=70days |
| Thermal cycling (passive) | $T_{min}$=25˚C<br>ΔT=105˚C, 125˚C<br>$t_{cycl}$=4min | Max.10,000*4min=28days |

An accelerated aging system to explore an intrinsic degradation mechanism on a power semiconductor is proposed in [135]. The system is aimed at studying intrinsic degradation precursors related to a device's physical properties. The unique feature of this system is that it isolates electrical overstress from thermal overstress. Therefore, the internal temperature of the

test subject can be controlled to avoid package related failures by eliminating thermal cycling and controlling the highest junction temperature within the rating limits.

The degradation precursor for IGBT was studied in [62] where accelerated aging, based on failure modes, mechanisms, and effects analysis (FMMEA) was performed. Selected parameters were monitored *in-situ*. Thermal-electrical stress was induced by removing the heat sink of IGBT under test so that it could heat itself. The gradual aging process of IGBT was implemented by introducing a thermal feedback loop that regulates the IGBT case temperature within a hysteresis bound. Aging was stopped when any latch-up occurred. The test bed was composed of an oscilloscope recording transient data, a function generator generating gate signals, programmable power supplies, and a data acquisition module. A similar aging technique was used in [106], where the junction temperature was set at 125% of the maximum operational junction temperature defined by the manufacturer. After latch-up was observed, the transistor was turned OFF for recovery and then subjected to aging again. The level of aging was described by the number of latch-up events. This methodology was used in [107] with a slight modification that decreased the set point of the junction temperature after each latching occurred when doing repetitions. The rationale behind this set-point reduction was that the thermal resistance increases due to die attach deterioration.

In order to obtain the failure precursor and mechanism of a super-capacitor, an accelerated test was conducted in [136]. Experimental results of this paper demonstrate that the capacitor samples failed once the temperature increased to 155°C. The degradation level was defined in terms of loss in capacitance and an increase in equivalent series resistance (ESR). The super-capacitor was considered a complete failure when there was a 30% loss in capacitance and the ESR increased by 100%.

### 4.4 Tests to verify condition monitoring methods

The ultimate goal of monitoring any condition is to detect early signs of failures in real applications and schedule maintenance accordingly, in order to prevent unexpected outages. However, when designing these methods, they have to be tested and verified under accelerated test conditions. This type of accelerated test only needs to generate parameter degradation; thus, the effectiveness of the method can be tested within a reasonable time span. In other words, the main objective is to validate the condition monitoring method, and hence, the way to perform the accelerated aging test is trivial as long as the precursor parameter of interest exhibits measureable deviation with the proper trend. Therefore, all the aforementioned accelerated aging methods can be used for this purpose. However, they can be unnecessarily complex for simply generating parameter variations and a simpler alternative might be the so-called DC aging.

In [28], MOSFETs were placed in the environmental chamber with constant gate voltage and drain-source voltage, and a resistive load was connected to the source. A higher drain-source voltage was used when a higher level degradation was expected. This test setup did not resemble the real life condition; however, it increased the ON-state resistance of the MOSFETs, which was sufficient to verify the method to measure the MOSFET ON-state resistance in the live converter proposed in this paper. In paper [137], a thermal cycling was applied to high-power MOSFETs. Those MOSFETs were placed in a temperature chamber where the temperature was -55°C. A dc current was used to heat the MOSFETs to about 100°C within 3 minutes; it held the temperature for 3 minutes, and then removed the dc current so the device temperature dropped to the chamber temperature within 2 minutes.

Another thermal cycling based accelerated aging was accomplished in [103] where the failure was identified as soon as the gate control was lost. Degradation was induced in the device in three different conditions. The drain current was maintained at 5.2A, and the junction temperature was 240°C, 220°C, and 210°C, respectively. The reliability of the power electronic components (IGBT and MOSFET) of a motor drive was investigated in [138]. The temperature of the environment was maintained at 85°C and humidity was 85%. At this condition, the leakage current and ON-state resistance of the MOSFET increased significantly during any power interruptions, but the IGBT did not show any sign of aging. A similar accelerated test was performed in [139]. The only difference between these two tests was the input power interruption that was given in the later experiment for a shorter time period and followed by an over voltage situation. Both test results show that the environmental condition acted as a positive feedback to accelerate the aging.

**4.5 Tests considering mission profiles**

A common feature of the aforementioned accelerated aging tests is that the DUTs were under uniform periodic stress. In contrast, in the field applications, the devices undergo random loading conditions. In order to compensate for this inconsistency, accelerated aging tests could be employed dedicated to expose any devices to the conditions close to the field applications. An active aging test bench that reproduced constraints similar to an automotive application was recently proposed in [140]. In this paper, thermal coupling is considered because the confined space makes this phenomenon significant. A driving cycle with given torque and velocity was converted into switching and conduction losses of IGBTs and diodes. Because the test bench could not produce any switching loss, the conduction loss during the test was set equal to the sum of switching and the conduction losses were calculated from the driving cycle

profile. The DUT was mounted on a water-cooled heat sink. The power cycling was composed of a 15s heating phase with a current that produced the desired conduction loss and a 30s cooling phase without current injection.

A power cycling test bench for IGBT, used in wind applications, is presented in [141]. A low frequency (slip frequency) operation of the rotor side inverter was considered to be the main source of the device degradation. The main feature of this test bench is that it varies load current frequency with a given RMS value. With a certain load profile, the device temperature can be collected by the data acquisition system. With the measured temperature profile, the lifetime can be estimated using a lifetime model.

Accelerated lifetime testing has not only been carried out to estimate the lifetime of IGBTs and MOSFETs but also for the lithium-ion capacitors [142], metallized film capacitors [143], lithium-ion batteries [144], capacitors used for storing energy in particle accelerators' power converters [145], and so on. Paper [146] proposed a strategy for designing an accelerated aging test for IGBT solder fatigue. The goal is to find how many cycles are needed in an accelerated aging test in order to create the same damage in the real condition. The general procedure is summarized as follows. Step 1 - experimentally determine the number of thermal cycles before failure occurs for a given aging methodology. Step 2 - use the test specifications in conjunction with finite element simulation to find out the total energy (mechanical) dissipated in the solder layer. Final step - another simulation based on the mission profile was performed to find out the time period during which the dissipated energy equaled the total energy obtained in the previous simulation. The assumption behind this methodology is that the same dissipated energy results in the same degradation level regardless of the time span.

In view of the above discussion on various accelerated test methods, there is no deniable fact that the junction temperature ($T_j$), ON-state resistance ($R_{DSON}$) for MOSFET, and $V_{CEON}$ for IGBT are the most commonly monitored parameters in condition monitoring of power semiconductor devices. It is quite evident that $R_{DSON}$ and $V_{CEON}$ measurements are more straightforward and easier compared to the $T_j$ measurement. Since the junction of a power device is not directly accessible in field applications, there exist several techniques in order to estimate the junction temperature. Following section discusses these techniques of estimating junction temperature.

### 4.6 Junction Temperature Measurement Methods

The reason that the temperature of the device junction is a crucial quantity where reliability is concerned is manifold. During all accelerated aging tests, it is necessary to obtain the device junction temperature, and the junction temperature is a part of the test protocol as discussed above. In addition, many failure indicators such as $V_{CE}$ are sensitive to temperature, and therefore, it is necessary to compare them at a fixed temperature to rule out the thermal effect. The junction temperature of the device is also an important metric for thermal management and condition monitoring, and the reliability assessment standards (such as Military Handbook 271) estimate reliability based on the device temperature. This section summarizes methods used to determine the device junction temperature. In general, the junction temperature can be measured directly or indirectly. Direct methods are accurate but intrusive, while indirect methods have moderate accuracy but are non-intrusive.

#### 4.6.1 Direct measurement methods

Direct measurement requires temperature sensors located on the die, which is usually inconvenient because the chip surface of a power module is not always accessible. However,

in laboratory conditions, such direct measurements are always performed to provide the baseline data that verify the indirect measurement methods. A thermocouple is one widely used type of temperature sensor for direct temperature measurement. Another direct method is the optical method [147, 148]. The advantage of using an optical sensor is that it has both good dynamic behavior and electric insulation that allows temperature measurement in high voltage conditions. The limitation of a thermocouple and optical fiber is that only a single point (rather than temperature distribution) can be obtained. An IR camera can be used to measure temperature distribution as well, but the devices need to be opened and painted with black paint to increase the emissivity.

### 4.6.2 Indirect measurement methods

#### 4.6.2.1 FEM Method

The finite element method (FEM) is a powerful tool to determine the device junction temperature. It can precisely simulate the chip temperature and spatial temperature distribution if a proper mesh is developed. This method is time-consuming and computationally inefficient, and thus, is not well suited to real-time temperature acquisition. However, high accuracy makes this method useful in many occasions such as calibrating compact device thermal models and providing the baseline temperature to determine the accuracy of other temperature measurement methods. A study has been performed based on FEM in [149] in order to identify the influence of a direct bond copper (DBC) metal trace layout in an IGBT module. The simulation result shows the metal trace has larger area experiences with higher thermal stress.

#### 4.6.2.2 TSEP Method

The most commonly used method to measure junction temperature indirectly is to use a temperature sensitive electrical parameter (TSEP) [64]. As for IGBT, $V_{CE}$ at a small current

(several tens to hundreds milliamps) is always chosen as the TSEP. This method requires the availability of junction temperature vs. $V_{CE}$ curve at a small calibration collector current. During the calibration, the IGBT temperature is controlled by an external heating system, i.e., a temperature chamber, to obtain $V_{CE,sat}$ as a function of the junction temperature [150]. In practice, the collector current during an accelerated test is much higher than the calibration current. Therefore, a measurement window needs to be inserted into the IGBT normal switching pattern to facilitate the temperature measurement. The measured current is maintained as small as possible to minimize generated heat. In order to eliminate the need for introducing the measurement window, which is not always feasible, $V_{CE}$ at a high current was chosen as the TSEP in [151]. It is worth mentioning that $V_{CE}$ at a small current has a negative temperature coefficient but a positive temperature coefficient is observed at a large current. In [151], this phenomenon is explained by two competing factors, namely a PN junction with $dV_{CE}/dT_j<0$ and a resistor with $dV_{CE}/dT_j>0$. In [152], a neural network is used for a junction temperature estimation in which both $V_{CE}$ at a large current and $I_C$ are chosen as model inputs and $T_j$ is the output. A comparison between results from a neural network and from a conventional polynomial curve fitting showed the superiority of this method. Compared to $V_{CE}$ at a small current, a large current would amplify the effect of resistance. Therefore, bond wire failure, which increases the resistance, will lead to an inaccuracy in the temperature estimations.

In [153], the junction temperature was estimated by a short circuit current. Although it was shown in this paper that a short circuit current is sensitive to junction temperature, it may not be appropriate to use this method in real applications for several reasons. A short circuit current will increase device self-heating, and hence, accelerates degradation that is

counterproductive to condition monitoring or thermal management. In addition, real converters are all equipped with a short circuit protection mechanism, and removing the protection circuit in favor of temperature measurements can hardly be justified. Moreover, from the examples given in this paper, an additional IGBT is needed to measure each IGBT temperature, which is very uneconomical. Another example of choosing $V_{CE}$ as the TSEP in a multi-die IGBT module is found in [154]. The unique feature of this paper is that the authors have correlated the case temperature of the IGBT module in order to find a direct relationship to the junction temperature. Their results show that the correlation between the junction temperature ($T_j$ ) and case temperature ($T_C$) gives the best match when $T_C$ is measured very close to the terminal lead or package side. However, if the case temperature is used to estimate the junction temperature, the measurement error becomes a little higher because once the IGBT module starts heating up, the temperature distribution in the different die's baseplates becomes non-uniform.

In addition to $T_C$, $I_C$ and $V_{CE}$ have been identified as the failure precursors in [155] where the authors performed the reliability analysis for the IGBTs usually used in an all-electric vehicle. Other TSEPs include gate threshold voltage $V_{th}$ and saturation current $I_{css}$ [25]. In [156], $dI_{ce}/dt$ and the trans-conductance are chosen as the TSEP for IGBT. A similar study for the MOSFET junction temperature estimation was conducted in [157], where $dI_{ds}/dt$ at a constant $V_{gs}$ was identified as the TSEP. In [158], $V_{th}$ is considered as the TSEP in order to measure the junction temperature because the experimental results illustrate that the threshold voltage shows superior sensitivity compared to the body-diode forward voltage ($V_{SD}$) of the MOSFET. Since the calibration of TSEPs is performed under a homogenous chip temperature while the temperature gradient is observed during active self-heating, discrepancy between the measured and actual temperature is unavoidable [159]. Indeed, the temperature at the central

chip is normally higher than those of the corners and edges. Therefore, the severity of the problem depends on how significant the effect that the chip geometry has on the temperature measured by the TSEPs [160]. Specifically, a larger chip dimension tends to have a larger measurement error. These methods are suitable for single chip modules or discrete devices, but might be questionable for multichip module temperature measurements. For a multichip module, the temperature measured using this method is actually the average junction temperature of all chips. However, temperature distribution of different chips is hard to obtain and can contribute to a localized failure.

#### 4.6.2.3 Thermal Test Chips

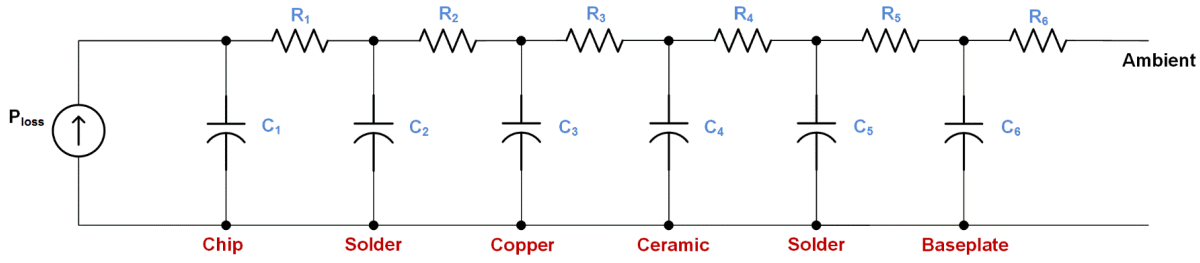
Originally developed for thermal characterization of electronic packages [161], thermal test chips (TTC) can also be used for chip temperature measurements. Commonly used TTCs are diodes and resistors. As for diodes, forward voltage is sensitive to temperature, and hence, can be used for temperature estimation. The calibration of temperature versus forward voltage consists of a linear or polynomial fitting depending on the temperature range. A resistor is very similar to the diode in terms of calibration, except that resistance is used as the temperature sensitive parameter. In [162], a string of diodes are fabricated on the IGBT chip surface for the temperature measurement. The disadvantage of this method is that the diodes or resistors will degrade along with the device usage. Therefore, the accuracy of the measured temperature will deteriorate over time.

#### 4.6.2.4 RC Thermal Models

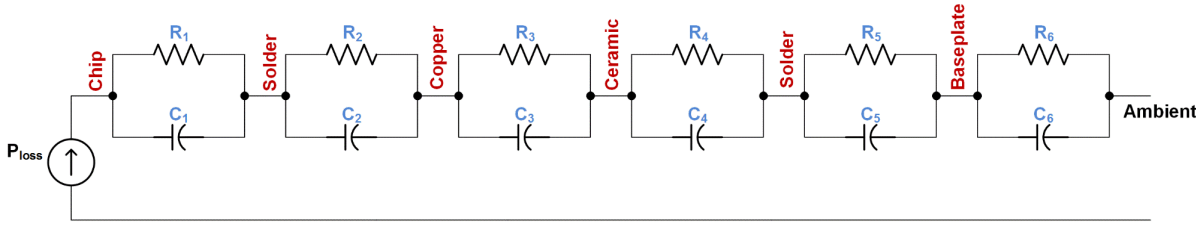
Another indirect method is using a compact device thermal model to estimate the junction temperature. Thermal models are also used to obtain temperature waveforms over a certain mission profile. A simple type is a resistor-capacitor-based thermal model [163] –

[165]. This RC type model can be further classified into the Cauer type and Foster type, which are shown in Figure 6 [163] – [165].

The parameters of the Foster model are normally provided in the device datasheet by manufacturers, and hence, can be employed conveniently. However, the thermal resistance given in a datasheet considers the worst case scenario, which means that an offset accounting for the device degradation is included. This could lead to a pessimistic estimation of junction temperature. Direct use of datasheet parameters leading to junction temperature estimation with poor tolerances was reported in [166]. The parameters of the RC thermal network can also be obtained by either a FEM or by fitting the model to an experimentally measured transient thermal impedance curve.




(a)




(b)

Figure 6: RC thermal models (a) Cauer (b) Foster [163] – [165].

Parameterization of an RC compact thermal model involves fitting a multi-exponential equation (16) to a device temperature impulse response with a zero initial condition.

$$Z_{step}(t) = \sum_{i=1}^{N} R_{thi}(1 - e^{-\alpha_i t}) \quad (16)$$

A more comprehensive form of this model for a multi-chip module considering the thermal coupling effect is shown in equation (16), where the diagonal elements are self-thermal impedance and the off-diagonal elements are mutual thermal impedance [167].The parameterization of equation (17) requires n experiments, where n is the number of chips of a power module.

$$\begin{bmatrix} T_1 \\ \vdots \\ T_n \end{bmatrix} = \begin{bmatrix} Z_{11} & \cdots & Z_{1n} \\ \vdots & \ddots & \vdots \\ Z_{m1} & \cdots & Z_{mn} \end{bmatrix} \begin{bmatrix} P_1 \\ \vdots \\ P_n \end{bmatrix} + T_{Ambient} \quad (17)$$

#### 4.6.2.5 Heat Diffusion Equation based Methods

The advantage of an RC model is that it can be conveniently incorporated in circuit simulators. However, a highly accurate model requires complex 3D finite element simulation, which is time-consuming. An alternative way involves solving a heat diffusion equation. The three-dimensional heat diffusion equation of isotropic material can be written as [166]:

$$c\rho \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = q_{int} \quad (18)$$

It is not always straightforward to solve these equations analytically. Approaches to solve such equations can be found in [124], [168] and the references therein. In addition to an analytical solution, equation (18) can also be discretized into a set of equations describing the temperature of each node. This approach has been implemented in conjunction with a model order reduction approach in [124]. Knowing the junction power dissipation and ambient temperature, the device junction temperature can be easily calculated using the thermal model. A major limitation of this approach is that the change of thermal impedance due to solder degradation is not considered. Therefore, a periodic recalibration is necessary in order to use

this model in an accelerated aging test. A comparison of different temperature measurement techniques is listed in Table VI.

Table VI Comparison of temperature measurement methods

| Methods | Examples | Accuracy | Intrusive or not | Implementation Complexity | Spatial temperature Distribution Availability | Computational Efficiency |
|---|---|---|---|---|---|---|
| Direct | Thermocouple | High | Y | Medium | N | NA |
| | Optical fiber | High | Y | Medium | N | NA |
| | IR camera | High | Y | High | Y | NA |
| Indirect | FEM method | High | N | High | Y | Low |
| | TSEP method | Medium | N | Medium | N | High |
| | Thermal test chips | Medium | Y | High | N | NA |
| | RC model | Medium | N | Low | N | High |
| | Heat diffusion equation based method | High | N | Medium | Y | Medium |

### 4.7 Conclusions

The primary purpose of accelerated aging is to quicken the degradation mechanism of the device under test so that the stresses experienced by the device induce the similar aging effects as the intended application, however, within a very short time span. In reality, it is not possible to consider all of the environmental and electro-mechanical stresses in the laboratory test set up. However, the existing literature suggest that active power cycling with high junction temperature swing will accelerate the aging mechanism faster than any other methods alone. In this research work, both active power cycling and thermal aging have been carried out in

order to accelerate the aging of the device. The details of the aging setup and process will be discussed in the following respective chapters.

# CHAPTER 5

# SSTDR BASED DEGRADATION DETECTION

## 5.1 Introduction

High thermal and electrical stress, over a period of time tends to deteriorate the health of power electronic switches. Being a key element in any high-power converter systems, power switches such as insulated-gate bipolar junction transistor (IGBT) and metal-oxide semiconductor field-effect transistor (MOSFET) are constantly monitored to predict when and how they might fail. A huge fraction of research efforts involves the study of power electronic device reliability and development of novel techniques with higher accuracy in health estimation of such devices. Until today, no other existing techniques can determine the number of lifted bond wires and their locations in a live IGBT module, although this information is extremely helpful to understand the overall state of health (SOH) of an IGBT power module. Through this research, a novel method for online condition monitoring of IGBTs and IGBT modules using spread spectrum time domain reflectometry (SSTDR) has been proposed. Unlike traditional methods, this research work concentrates at the gate terminals (low voltage) of the device instead of looking at the collector side. In addition, the RL-equivalent circuit to represent a bond wire has been developed for the device under test and simulated in CST Studio Suite to measure the reflection amplitudes. Experimental results were obtained using a prototype reflectometry hardware, and both the simulation and experimental results have been compared. These results prove that a single measurement is sufficient to predict the failure of the device instead of looking at the traditional precursor parameter ($V_{CEON}$). With only two sets of measurements, it is possible to locate the aged device inside a module and detect the number of bond wire lift offs associated to that device.

## 5.2 Fundamentals of SSTDR

Several reflectometry methods are currently being used in the field of reliability and condition monitoring. Among them, SSTDR is the most immune to noise and faces least interference, which make it an ideal test system for any power converter. The block diagram of SSTDR prototype hardware is shown in Figure 7 [19].

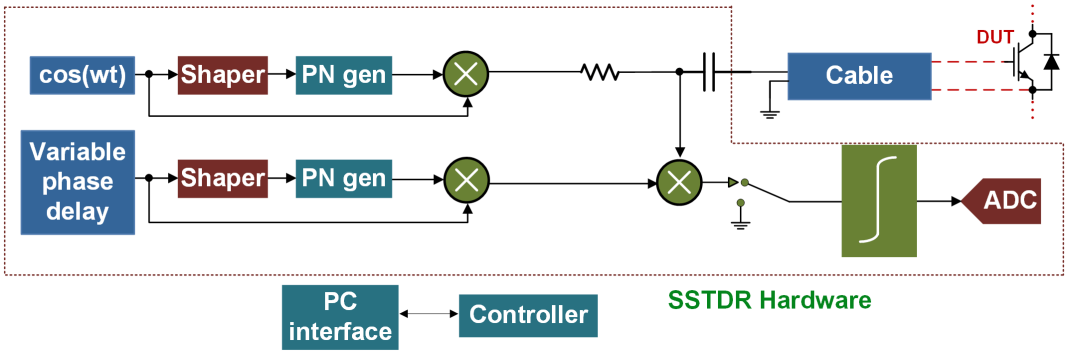



Figure 7: Schematic diagram of the SSTDR system showing the setup to characterize an IGBT in a live converter. [Courtesy: livewire innovation, 2012] [19]

Traditional time domain reflectometry (TDR) uses a high-amplitude and high-frequency signal which requires the system to be in offline so that the TDR signal does not interfere with the system. In addition, TDR requires a wide dynamic range of frequencies to transmit and to receive the reflected signals. On the other hand, SSTDR sends down a significantly lower amplitude signal (usually around or below 100mV and lowest could be 22mV) with a frequency of several hundreds of kHz to several MHz making it non-interfering with the system operation. Unlike traditional TDR, SSTDR method sends a high frequency sine wave modulated pseudo noise (PN) through the cable. When this signal finds any impedance mismatch it reflects back. The percentage of reflection depends on the impedance contrast between the characteristic impedance of its propagation path and the impedance at the point of mismatch. Then the reflected and incident signal is cross-correlated creating a peak at

the center frequency of the SSTDR. Since the incident signal and noise signals are not synchronized, their cross correlation yields a flat spectrum. That is why the SSTDR signal is highly immune to noise and interference. An example field-programmable-gate-array (FPGA)-based SSTDR evaluation kit W50A0071, which is an R&D product from Livewire Innovation, has been shown in Figure 8. This hardware works in two modes: (i) static and (ii) intermittent. In static mode, it requires external triggering for initializing each scan meaning it scans just for once after the trigger initialization. In contrast, intermittent tests scan the system continuously to detect short duration impedance change in SSTDR signal propagation path.

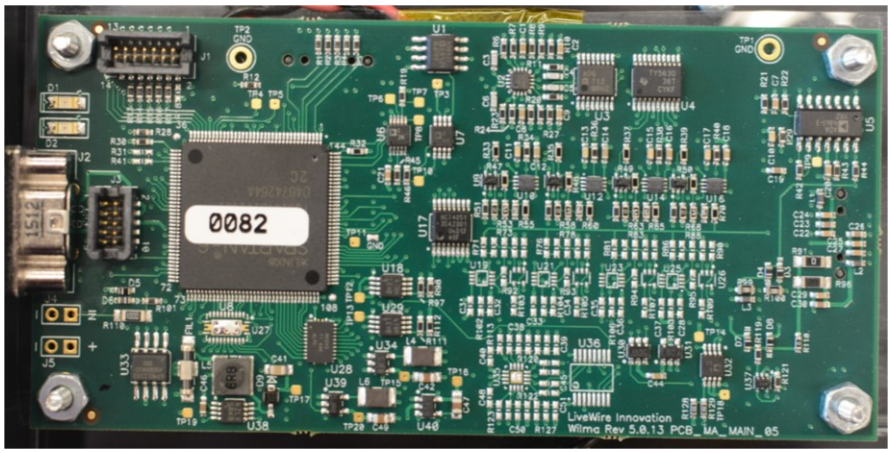



Figure 8: Photograph of the FPGA-based SSTDR hardware (an R&D product from Livewire

SSTDR is traditionally used to detect impedance discontinuity in electric power lines, and based on the experimental data, SSTDR can be used to detect the presence of cracks and voids in large IGBT modules by considering the entire module as a multi-conductor complex transmission line. This method can be made extremely sensitive (to locate small impedance changes), and extremely precise in both space and time, by using a longer PN code to increase the effective bandwidth of the system [169] – [171]. In addition, the SSTDR can be routed in a controlled way by the use of simple filters in the current trace on the PCB, leading to a very

accurate signal injection method. Like other reflectometry method, SSTDR magnitude or the reflection coefficient Γ can be expressed as:

$$\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_O}{Z_L + Z_O} \quad (19)$$

Where, $Z_O$ is the characteristic impedance of the line, and $Z_L$ is the impedance of the discontinuity [39].

SSTDR generated data could be potentially used to detect the parametric variations caused by thermal and electrical stresses in IGBT modules and the results are independent of the IGBT's operating points. The DUT is a dual pack module which consists of 6 IGBT devices, with their corresponding anti-parallel diodes. These devices and diodes are interconnected with a total of 48 bond wires. Three IGBTs and three diodes are connected in parallel, forming the top IGBT, and the remaining devices form the bottom IGBT as shown in Figure 9.

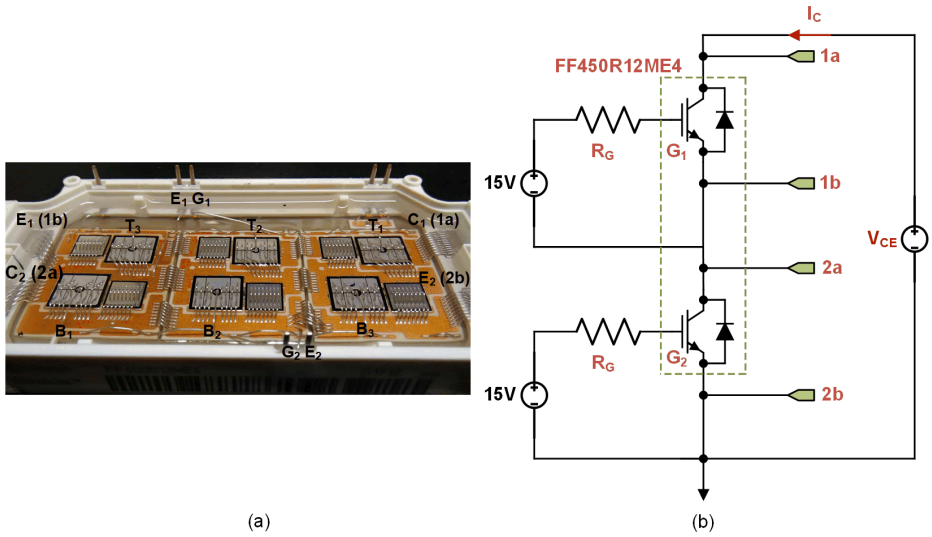



Figure 9: (a) Infineon dual pack IGBT module (FF450R12ME4) without top cover (b) Simplified schematic of the module

Each of the bond wires present in this module has its own resistance and inductance. The interconnections are made in such a fashion that they can mimic a very complex transmission line network. When any device ages, the ON-state resistance ($R_{ON}$) value will be different than that of the healthy device. Similarly, if any bond wire lift-off occurs, the overall impedance seen from any two terminals will be different than it was before.

Let the equivalent impedance for a healthy module seen from gate and emitter terminals of the top IGBT device be $Z_{G1E1,H}$ and with aging, this impedance is increased to $Z_{G1E1,A}$ , then if the change in these two measurement is denoted by $\Delta Z_{G1E1}$, we can express this value as shown in the equation (20) below:

$$\Delta Z_{G1E1} = Z_{G1E1,H} - Z_{G1E1,A} \tag{20}$$

Now, the reflection coefficient Γ, presented in equation (19), will give the impression of this difference in impedance, and a non-zero value will illustrate the aging of the module.

### 5.3 Accelerated Aging and Degradation Detection

#### 5.3.1 Active Power Cycling of IGBT

The DUT, shown in Figure 10, was placed in an accelerated aging station (shown in Figure 11) to stress it electrically and thermally. The simultaneous stress was achieved by stopping the coolant flow during the ON-state of the DUT. This active power cycling technique helps to induce aging in the device in a more efficient way than stressing it either electrically or thermally. A 600A Lambda-TDK (EMS 7.5-600-2-D-RSTL) power supply was used to push current through the device, and 313A DC current was supplied between the collector and emitter terminals during the aging process. The number of cycle was counted based on the temperature swing of the device. The swing in temperature was 100°C (ΔT) starting from 50°C

and ending at 150°C of case temperature. A k-type thermocouple was used to monitor the temperature.

A Lab-Jack T7-Pro DAQ was utilized to record $V_{CEON}$, collector current ($I_C$), and case temperature ($T_C$). Once the temperature reached 150°C, the power supply automatically stopped sending power to the device and coolant flow was activated.

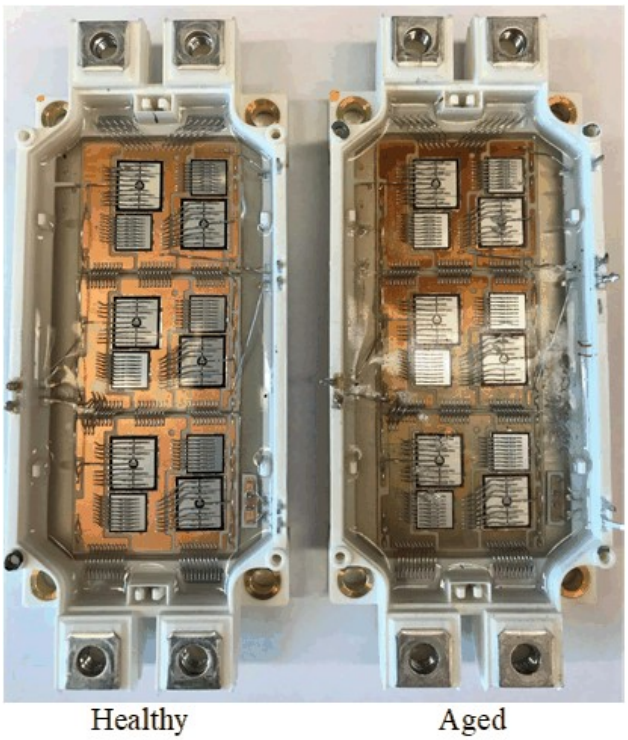



Figure 10: Infineon IGBT power module (FF450R12ME4) without top cover

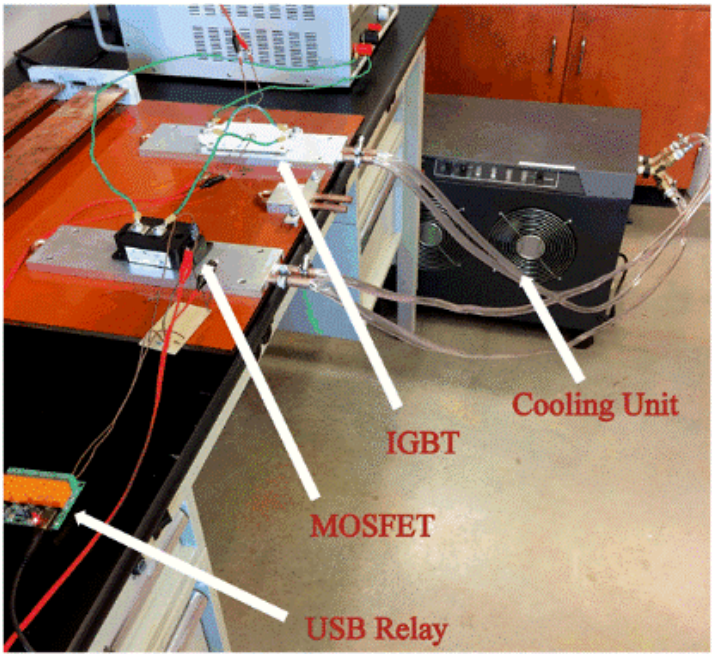



Figure 11: Active power cycling setup

Similarly, when the device's case temperature went down to 50°C, the power supply started pushing current to the collector, and the coolant pump stopped the coolant flow. This control of the power supply was incorporated by using a power MOSFET in series with the DUT at the collector side, and this switch was turned ON and OFF in order to activate or deactivate the power supply. This ensured the full conduction of the device under test. In order to make the cooling efficient, a heat sink was attached underneath the IGBT module, and Ethylene-glycol was used as the cooling agent. The overall schematic is presented is Figure 12.

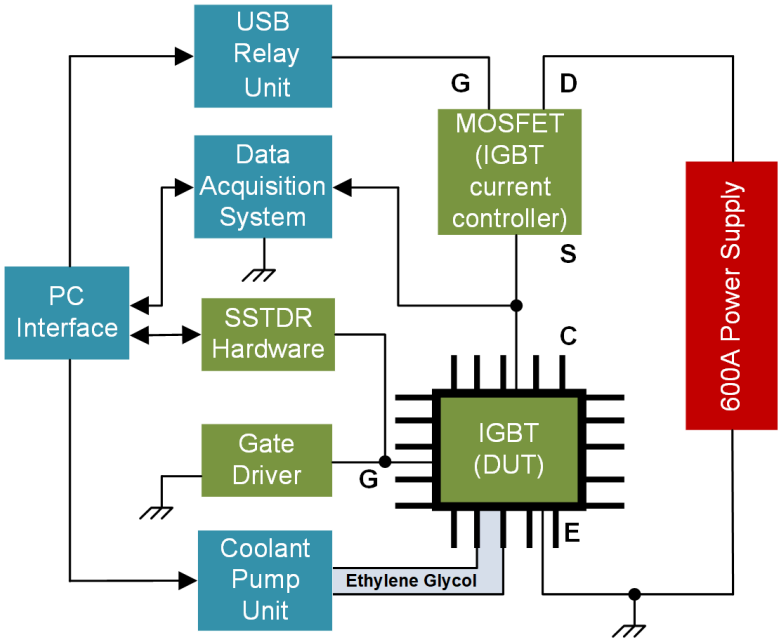



Figure 12: Schematic of the accelerated aging station

### 5.3.2 Experimental Setup and Test Results

The SSTDR signal was applied at both of the gates of top and bottom IGBT, and simultaneously the DAQ was recording the $V_{CEON}$ data (plotted and shown in Figure 13). Figure 14 illustrates the simplified Infineon module and shows the SSTDR test points: $G_1$, $E_1$ (1b), $G_2$, and $E_2$ (2b). This device was aged at two different levels, and data obtained at each level was compared with the measurements consistent to the zero aged device. Aging level 1 was defined as 400 aging cycles, and aging level 2 was considered once the device failed. The SSTDR data was recorded for frequencies 3MHz, 12MHz, and 48MHz for collector current levels of 0A, 25A, and 50A.

From Figure 13, it is apparent that with the aging i.e., as the number of cycles increases, the $V_{CEON}$ keeps increasing and gives a spike at around 800 cycles as the change is about 5%

of the initial voltage. At this point the IGBT can be considered as non-functional. This pattern of IGBT's $V_{CEON}$ is very common and can be found in many condition monitoring literatures [172], [173]. Now, according to equation (16), it is expected that when IGBT goes through aging, the ON-resistance will increase and the auto-correlated amplitude of SSTDR will produce a lower magnitude. Figure 15 shows the auto-correlated amplitude of SSTDR signal recorded between the gate and emitter terminals of the top and bottom IGBT respectively. The zoomed portion within this plot clearly shows that there is a significant difference between the healthy and aged data. As the level of aging increases i.e., $R_{ON}$ increases, the amplitude of the auto-correlated amplitude keeps falling, which supports the reflectometry theory stated in equation (19).

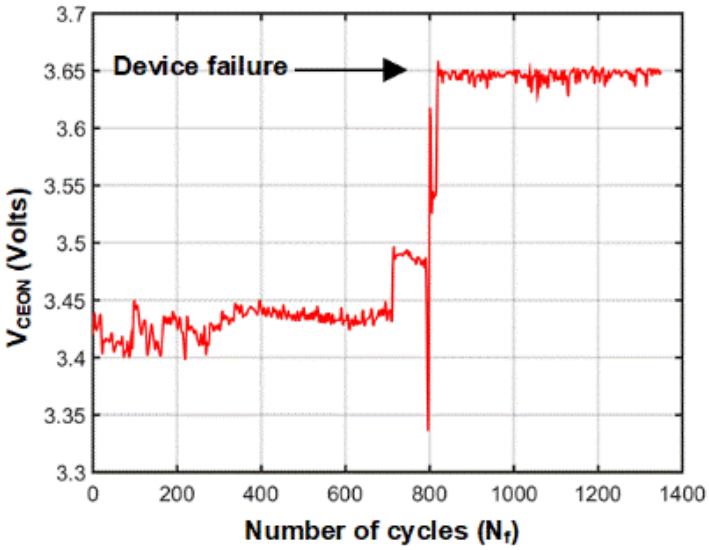



Figure 13: $V_{CEON}$ vs number of cycles plot

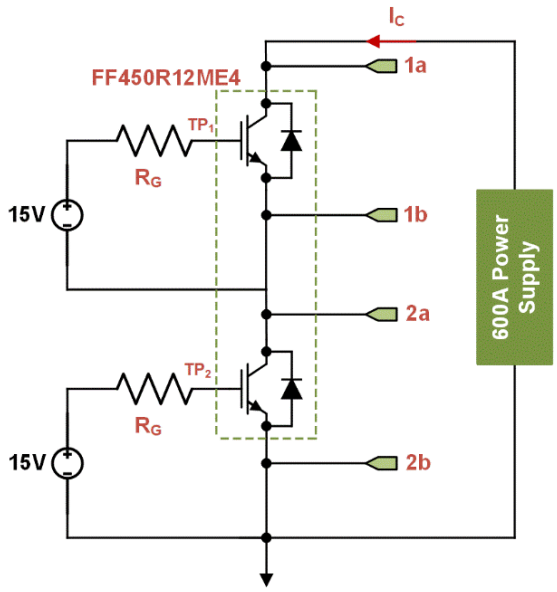



Figure 14: Simplified SSTDR test schematic: $TP_1$ and $TP_2$ represent SSTDR test points for top and bottom IGBT's gate-emitter interface respectively

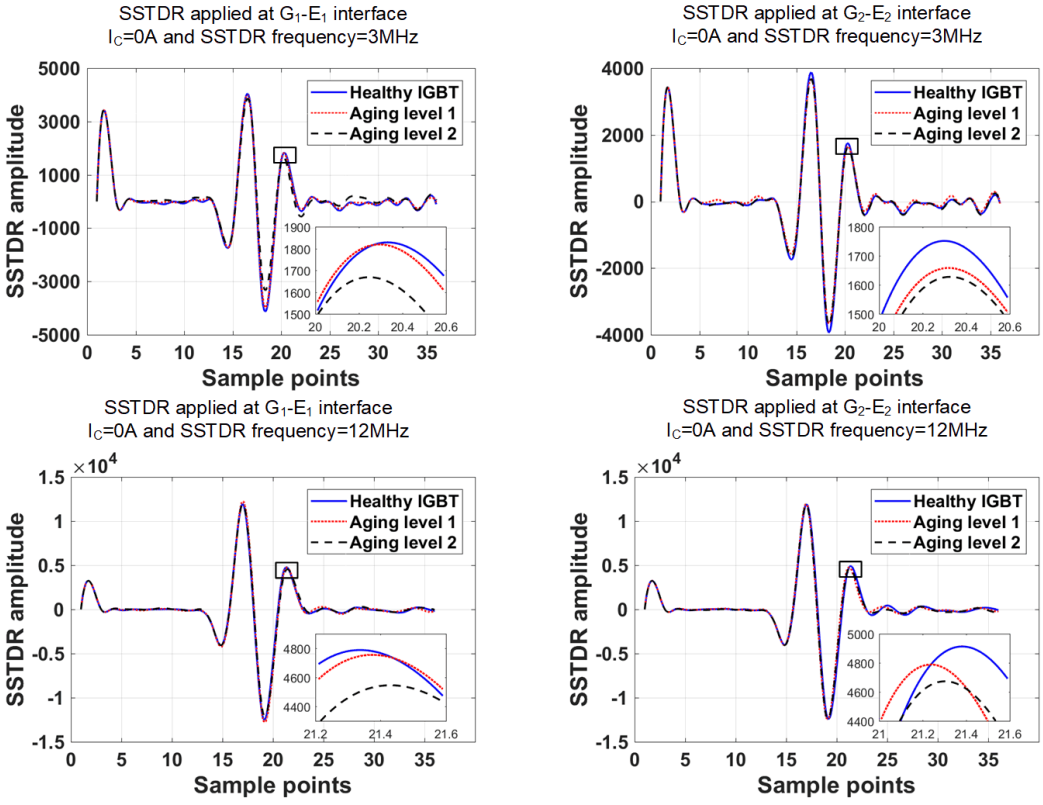



Figure 15: SSTDR auto-correlated amplitude plot

Now, it is necessary to find a correlation between the $V_{CEON}$ and the auto-correlated SSTDR amplitude in order to reach a conclusion. Table VII presents the comparison between the above mentioned quantities, which were recorded by the DAQ and SSTDR hardware respectively (also can be obtained from Figure 13, and Figure 15). From this table, it is apparent that the percent change in the $V_{CEON}$ of healthy and failed device is about 5.49%. Similarly, the percent change in the amplitude of SSTDR reading between the healthy and failed device recorded at the gate terminals are 5.83% and 5.81% respectively. These values are very close to each other and hence it can be concluded that the SSTDR measurement at the gate terminals are accurate enough to identify the failure or aging of the IGBT power module.

Table VII Correlation between $V_{CEON}$ and SSTDR Amplitude

| | $V_{CEON}$ (V) | SSTDR auto-correlated amplitude at $I_C$ = 0A | | | |
|---|---|---|---|---|---|
| | | Between terminal $G_1$-$E_1$ | | Between terminal $G_2$-$E_2$ | |
| Healthy device | 3.64 | 3MHz | 12MHz | 3MHz | 12MHz |
| | | 1820 | 4788 | 1751 | 4913 |
| Aged device (failed) | 3.44 | 1692 | 4566 | 1633 | 4673 |
| Percent change (%) | 5.49 | 7.03 | 4.63 | 6.74 | 4.88 |
| Average (%) | 5.49 | 5.83 | | 5.81 | |

However, in order to verify that the SSTDR technique is able to provide aging information independently of current level, data were recorded between the gate and emitter interface for 25A and 50A collector currents at 12MHz and 48MHz of SSTDR frequencies, respectively. These data have been plotted in Figure 16. All of these plots show the similar pattern with 0A data. None of these figures contain the aging level 2 data because the device failed by that time, and IGBT was not conducting any current at that point. Therefore, through

these measurements we can conclude that the SSTDR test data does not depend on the current level of the device, and a single measurement is adequate to identify any aging related information inside the IGBT power module.

In addition to the monitoring at the gate terminals, SSTDR were applied between the collector, $C_1$ (1a) and emitter, $E_2$ (2b) interface (nodes are shown in Figure 14) of the IGBT at different current levels (25A and 50A) and SSTDR frequencies (12MHZ and 48MHz). These data were plotted in Figure 17 including the zoomed portions to have a better clarity. Interestingly, these plots show the similar pattern of aging as depicted in previous plots. This matching information proves that SSTDR based condition monitoring is independent of nodes and frequency at which the signal is applied. However, it is advantageous to connect to the gate side for the lower voltage level and ease of access.

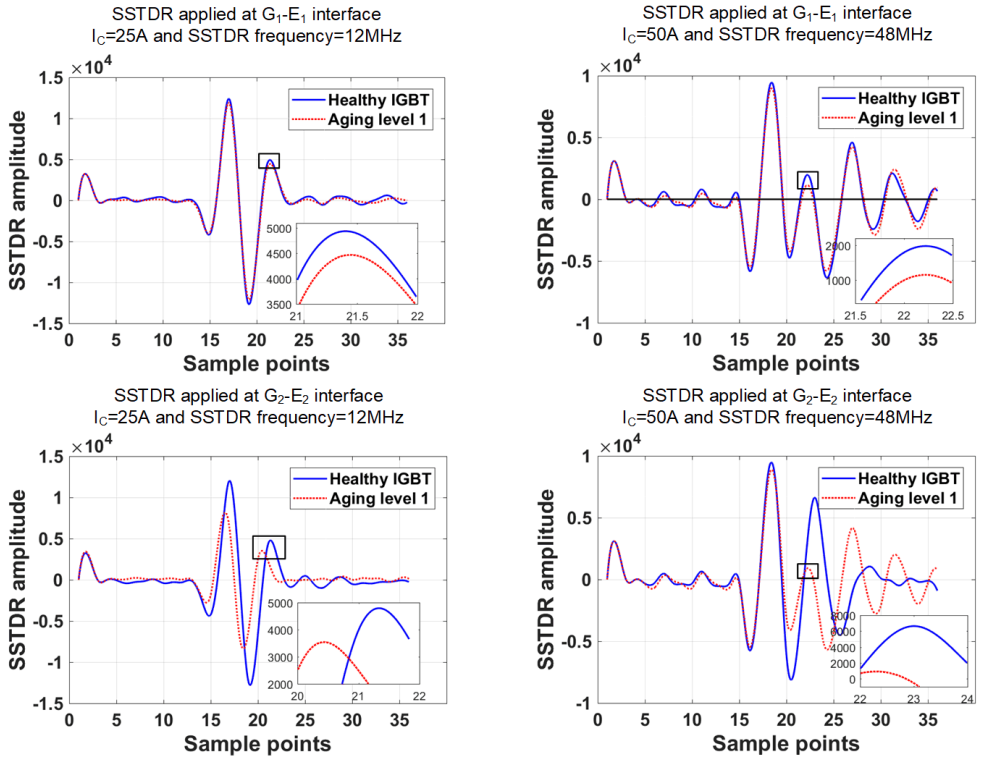



Figure 16: SSTDR auto-correlated amplitude plot

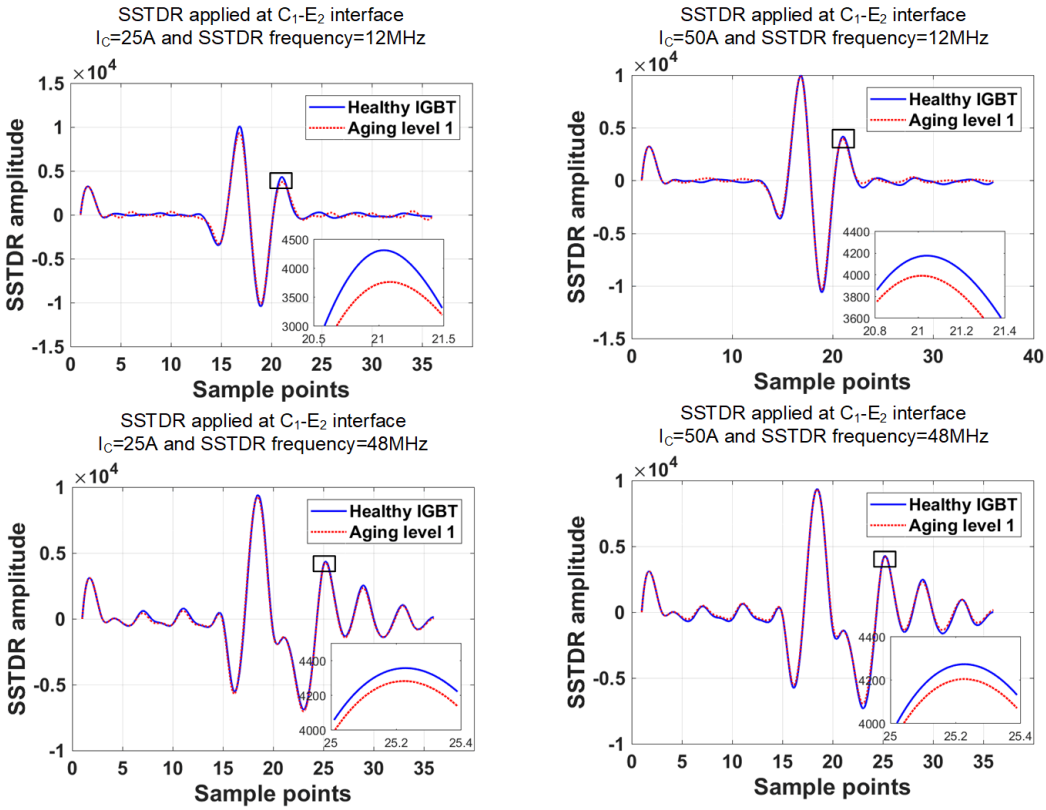



Figure 17: SSTDR auto-correlated amplitude plot

SSTDR is a relatively new technique to determine impedance discontinuity in power transmission lines [39], [40], [174]. Since 2012, Khan and his group have effectively used SSTDR to determine the level of aging in MOSFETs, capacitors, inductors, bond wire degradation in IGBTs and PV faults [41] – [43], [175]. So far, all SSTDR results are experimental, and there was no way to validate the accuracy and repeatability of the technique because no SSTDR based simulation models were available. This is the first time we have derived an accurate model of SSTDR propagation in CST Studio Suite, and we can verify all experimental results by using a newly derived IGBT model. The underlying reasons for choosing the CST Studio Suite for the simulation purpose are: (i) this software accommodates the platform to directly input a Spice model, (ii) electrical equivalent circuit can be drawn using

its own schematic and component library, (iii) this software is able to measure reflection parameters at any points of the schematic, and (iv) the SSTDR hardware's functionality is based on the reflectometry principle. The following section depicts detail description of the SSTDR simulation method and results using the CST Studio Suite.

### 5.4 RL-Equivalent of the Bond Wires in IGBT Module

There are six pairs of IGBTs and diodes in the FF450R12ME4 IGBT power module. All of them are interconnected via bond wires and each diode and IGBT device are interconnected with 8 bond wires. The devices in this dual pack module have been numbered and shown in Figure 9(a). A simplified block diagram is shown in Figure 18.

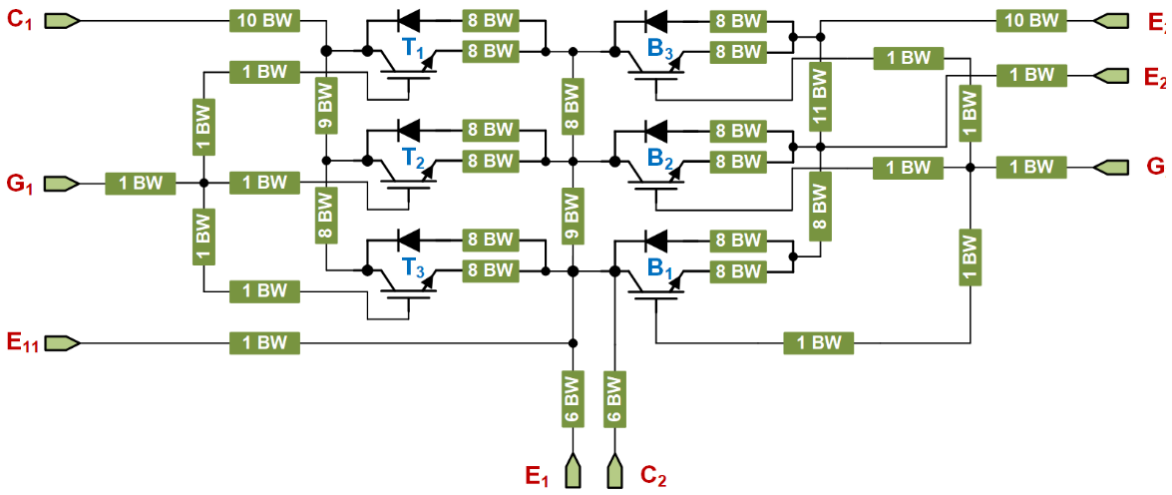



Figure 18: Simplified block diagram of FF450R12ME4 dual pack IGBT power module

Since all of the IGBT device and diode pairs are symmetrical and have the exact length and number of bond wires between them, one pair was modeled in detail, and the remaining pairs were replicated. After that, the interconnected bond wires between each pair were modeled in the similar fashion. Multiple bond wires were detached from the module to measure wire resistance (R), and the measurements were averaged for each bond wire. The length of

the bond wire was 12mm long, with 2.4mΩ resistance and 12nH inductance. For simplicity, inductance was estimated as "1mm length equivalent to 1nH inductance" according to [176]. The equivalent circuit of a single pair is shown in Figure 19(a), and Figure 19(b) depicts the equivalent branch minimized from Figure 19(a).

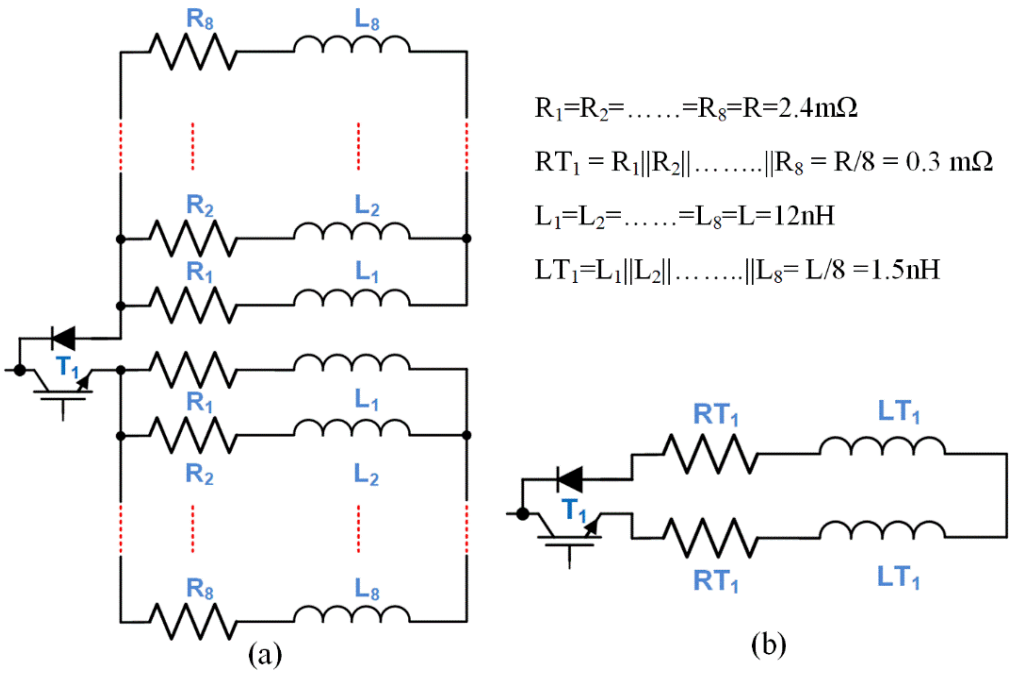



Figure 19: (a) RL-equivalent of a single pair of IGBT and diode (b) Simplified schematic of a single pair of IGBT and diode

The bond wire details are explained below:

- The collectors of the devices $T_1$ and $T_2$ are connected with 9 bond wires of 7mm length each, so as the collectors of $B_1$ and $B_2$.
- Similarly, the collectors of the devices $T_2$ and $T_3$ are connected with 8 bond wires of 7mm length each, so as the collectors of $B_2$ and $B_3$.

- The emitters of $B_1$ and $B_2$ are connected with 8 bond wires of 7mm length, and the emitters of $B_2$ and $B_3$ are connected with 8 bond wires of 7mm and 3 bond wires of 10mm length.

Bond wires at the gate and end terminals are connected as stated below:

- Gate terminals of $T_1$, $T_2$, and $T_3$ have 3 bond wires of 50mm, 10mm, and 40mm length respectively. The end points of these bond wires are then connected via a 30mm length bond wire to the external gate terminal, $G_1$.
- Similarly, gate terminals of $B_1$, $B_2$, and $B_3$ have 3 bond wires of 45mm, 15mm, and 45mm length respectively. The end points of these bond wires are then connected via a 15mm length bond wire to the external gate terminal, $G_2$.
- The collector of $T_1$ and emitter of $B_3$ are connected to the external $C_1$ and $E_2$ terminal with 10 parallel bond wires, each of 12mm length.
- The emitter of $T_3$ and collector of $B_1$ are connected to the external point $E_1$ and $C_2$ respectively with 6 parallel bond wires of 14mm length each.
- Another bond wire of 21mm length connects the emitter of $T_3$ to the ground connection of the $G_1$.
- The emitter of $B_2$ is connected with the ground of $G_2$ via a 15mm long bond wire.

Incorporating all of the above points into the equivalent circuit, the final bond wire RL-equivalent circuit will have the schematic shown in Figure 20. The values of the resistors and inductances have been enlisted in Table VIII.

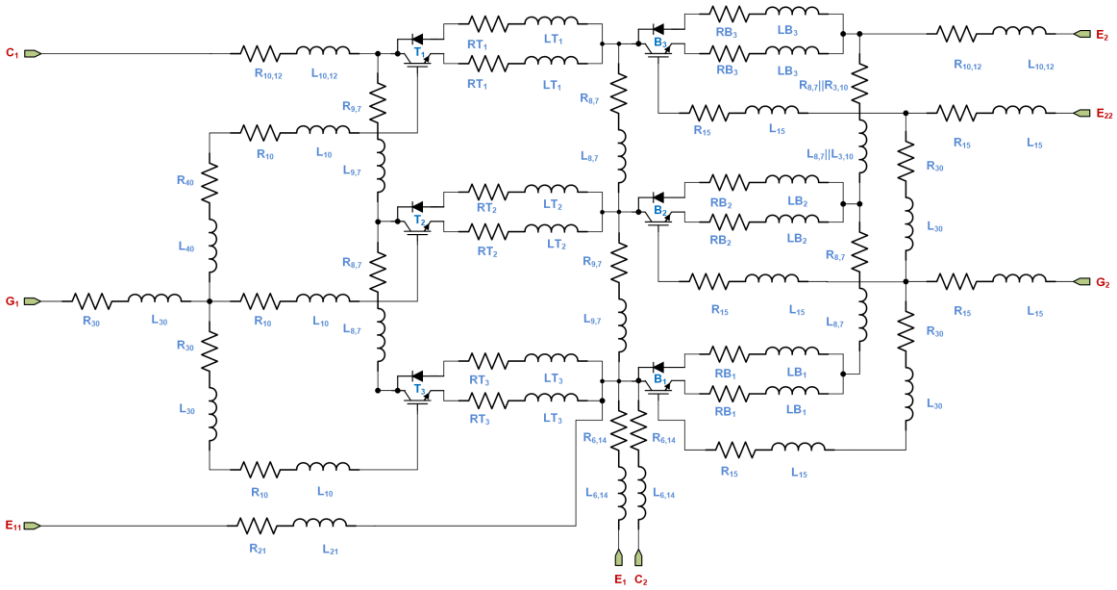



Figure 20: Finalized bond wire RL-equivalent circuit of the IGBT module

Table VIII PARAMETRIC VALUES OF THE ELEMENTS IN RL-EQUIVALENT CIRCUIT OF THE IGBT MODULE

| Resistance (mΩ) | | Inductance (nH) | |
|---|---|---|---|
| $RT_1$=$RT_2$=$RT_3$=$RB_1$=$RB_2$=$RB_3$ | 0.3 | $LT_1$=$LT_2$=$LT_3$=$LB_1$=$LB_2$=$LB_3$ | 1.5 |
| $R_{3,10}$ | 0.67 | $L_{3,10}$ | 3.33 |
| $R_{8,7}$ | 0.18 | $L_{8,7}$ | 0.88 |
| $R_{9,7}$ | 0.16 | $L_{9,7}$ | 0.78 |
| $R_{6,14}$ | 0.47 | $L_{6,14}$ | 2.33 |
| $R_{10,12}$ | 0.24 | $L_{10,12}$ | 1.2 |
| $R_{10}$ | 2 | $L_{10}$ | 10 |
| $R_{15}$ | 3 | $L_{15}$ | 15 |
| $R_{21}$ | 4.2 | $L_{21}$ | 21 |
| $R_{30}$ | 6 | $L_{30}$ | 30 |
| $R_{40}$ | 8 | $L_{40}$ | 40 |

### 5.4.1 Simulation Results

The bond wire RL-equivalent circuit was simulated using CST Studio Suite software in order to investigate lift off phenomena. Not all of the circuit simulators are equipped with both schematic and reflectometry ability, hence to serve the research goal, CST Studio Suite was chosen as the platform. The equivalent circuit was redrawn in the simulation platform and simulated data were recorded at both of the gate terminals ($G_1$ and $G_2$) over a wide range of frequencies (5MHz to 385MHz). Table IX summarizes the simulation steps or phases at a glance.

Table IX SIMULATION PHASES

| **Phase-0** | **Phase-1** Lift off @$\mathbf{T_1}$ | **Phase-2** Lift off @$\mathbf{T_2}$ | **Phase-3** Lift off @$\mathbf{T_3}$ | **Phase-4** Lift off @$\mathbf{B_1}$ | **Phase-5** Lift off @$\mathbf{B_2}$ | **Phase-6** Lift off @$\mathbf{B_3}$ | **Test points** | **Frequency range** |
|---|---|---|---|---|---|---|---|---|
| Healthy device (no lifted bond wire) | 1BW | 1BW | 1BW | 1BW | 1BW | 1BW | $G_1$-$E_1$ & $G_2$-$E_2$ | 5MHz to 385MHz |
| | 4BW | 4BW | 4BW | 4BW | 4BW | 4BW | | |
| | 7BW | 7BW | 7BW | 7BW | 7BW | 7BW | | |

As the first step, it is necessary to verify if multiple bond wire lift off incidents are detectable from the simulation results. Based on this results, location identification of the affected device will be calculated. Let us consider two random phases Phase-2 and Phase-5 and the simulation results at 48MHz is shown in Figure 21 and Figure 22, respectively.

Phase-0 is included in both of the plots to show the separation between the healthy and aged i.e., lifted bond wire cases. It is clearly distinguishable from the plots that each of the bond wire lift off case is different from each other.

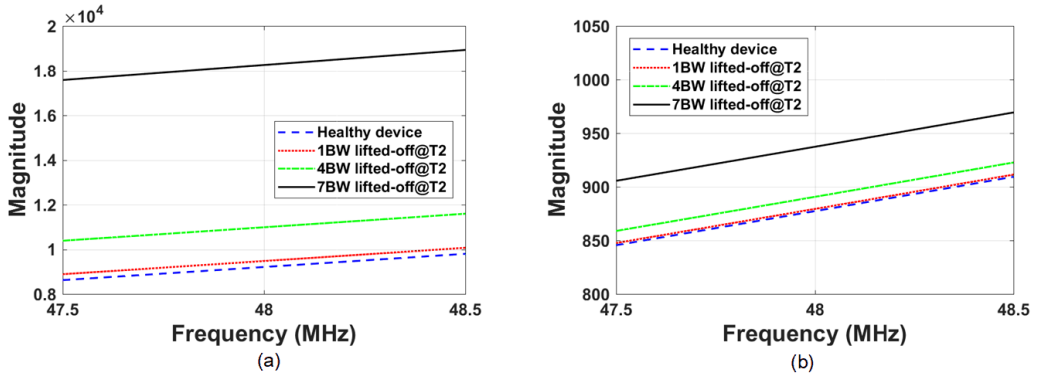



Figure 21: Reflection magnitude vs frequency plot when $T_2$ has lifted bond wire (a) recorded at $G_1$-$E_1$ interface (b) recorded at $G_2$-$E_2$ interface

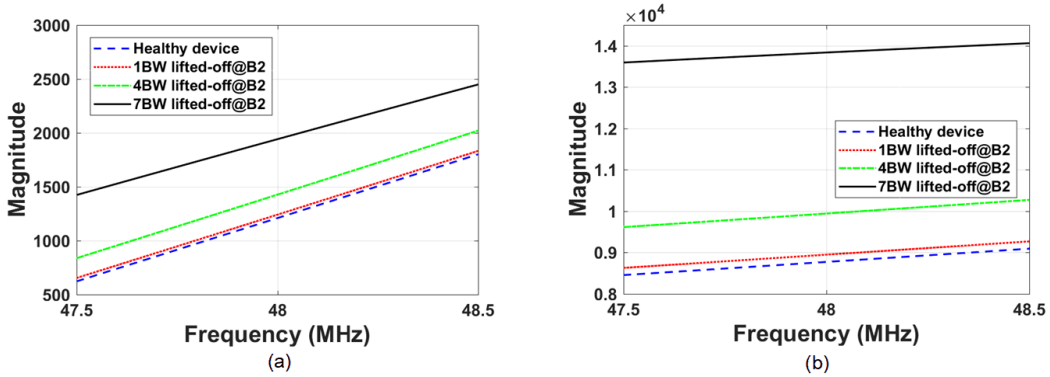



Figure 22: Reflection magnitude vs frequency plot when $B_2$ has lifted bond wire (a) recorded at $G_1$-$E_1$ interface (b) recorded at $G_2$-$E_2$ interface

Since the device $T_2$ is closer to the gate $G_1$, hence the magnitude is higher than the magnitude recorded at $G_2$-$E_2$ interface. Similarly, $B_2$ has a higher magnitude when recorded at the $G_2$ gate terminal. It is also noteworthy that the values in the y-axis are the absolute magnitude, whereas, they all are actually negative numbers. So, the true amplitude of the reflection is decreasing with increasing number of bond wires, which is consistent with equation (16) as well as with the experimental SSTDR data. In addition, the SSTDR hardware is a prototype device manufactured by LiveWire Innovation, therefore, the peaks in simulation

and experimental results are not equal in value. However, the trend in the data with device degradation is similar in both cases.

Identifying the location of the affected device is complex and requires the reflection data from both gate terminals. Instead of generating results at a certain frequency, the model was simulated over 5MHz to 385MHz frequency spectrum and the maximum amplitudes were recorded. Figure 23 shows the peak reflection amplitude from both gate terminals.

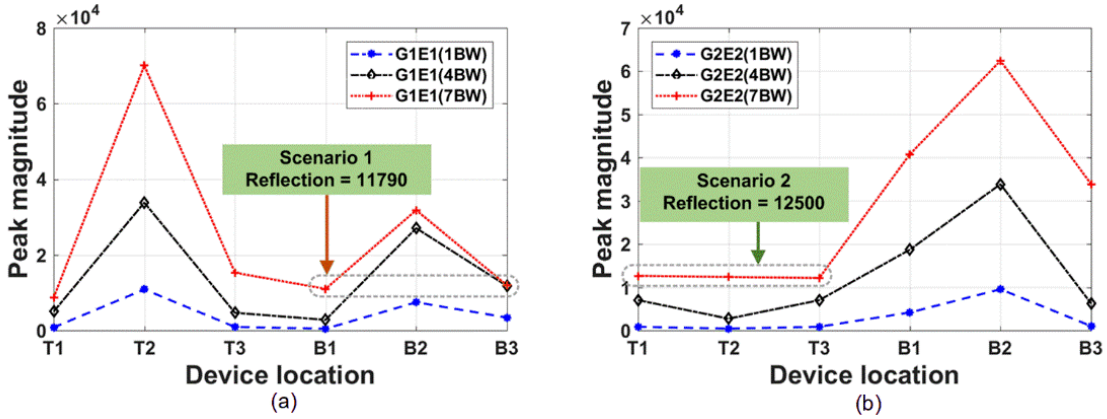



Figure 23: Peak reflection amplitude plot for six device locations (a) recorded at $G_1$-$E_1$ interface (b) recorded at $G_2$-$E_2$ interface

When SSTDR signal is applied across the gate-emitter terminals of the IGBT module, two sets of reflection amplitude readings are recorded, one for each gate terminal. These two sets of data are eventually used to identify the location of the affected device. Let us consider two scenarios as shown in Figure 23. "**Scenario 1"**: first set of data taken from $G_1$-$E_1$ interface, and the recorded reflection magnitude is 11,790. This data set could indicate the following instances (please see Figure 23(a)): (i) seven bond wire lift offs for device $B_1$, (ii) seven bond wire lift offs for device $B_3$, and (iii) four bond wire liftoffs for device $B_3$. Therefore, this single measurement is not sufficient to identify the actual incident out of these three possible cases. This is why we had to consider a second set of data recorded at a different location. Let us

consider the second set of SSTDR data recorded at $G_2$-$E_2$ interface, which generates a magnitude of 33,870. According to Figure 23(b), this magnitude is unique to seven bond wire lift offs at $B_3$. Therefore, by combining these two readings we are able to point out the location of the affected device which is $B_3$ (with seven detached bond wires) in this case.

Let us consider **"Scenario 2"**, where three different cases produce the same SSTDR amplitudes close to 12,500 obtained from $G_2$-$E_2$ interface. According to Figure 23(b), devices $T_1$, $T_2$, and $T_3$ are associated with this amplitude. In all cases, seven bond wires were detached. Therefore, this single reflection data cannot determine the location of the affected device. Let us assume we have another set of data obtained from $G_1$-$E_1$ interface with a magnitude of 70,050, and this data is only associated with the device $T_2$ (please see Figure 23(a)). Therefore, the same incident which was producing a reflection co-efficient of 12,500 when measured from $G_2$-$E_2$, it produces a reading of 70,050 when measured from $G_1$-$E_1$. Thus, by taking data from two locations, it is possible to pinpoint the number of bond wire detachments and the corresponding physical location. Table X shows these data sets.

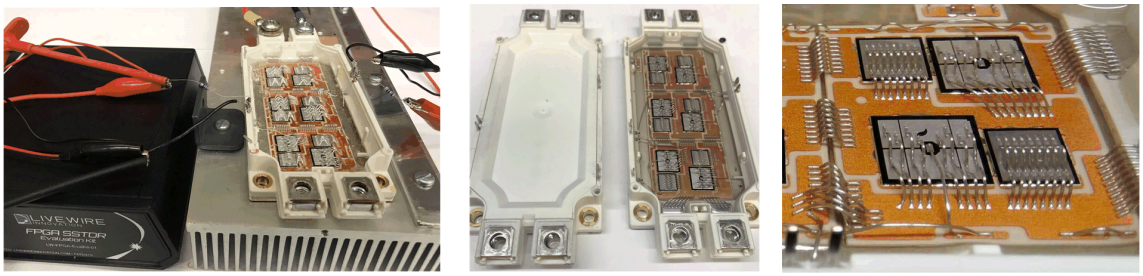
Table X ACTUAL DATA POINTS FOR BOTH SCENARIOS

| | Affected device and number of detached bond wires | Reflection magnitude recorded at $G_1$-$E_1$ interface | Reflection magnitude recorded at $G_2$-$E_2$ interface |
|---|---|---|---|
| **Scenario 1** | 7 BW at $B_1$ | **10,990** | 40,760 |
| | 7 BW at $B_3$ | **11,790** | 33,870 |
| | 4 BW at $B_3$ | **11,760** | 6,250 |
| | | | |
| **Scenario 2** | 7 BW at $T_1$ | 8,690 | **12,640** |
| | 7 BW at $T_2$ | 70,050 | **12,380** |
| | 7 BW at $T_3$ | 15,280 | **12,130** |

### 5.4.2 Simulation vs Experimental Results

Initial testing was conducted with FF450R12ME4 IGBT modules. These are EconoDUAL™3 modules with Trench/Fieldstop IGBT4 and Emitter Controlled HE diode, manufactured by Infineon Technologies. The high power density of this particular module has made it useful in several commercial, construction, and agricultural vehicle applications where extended reliability is a key. Each FF450R12ME4 has one top and one bottom IGBT and their corresponding free-wheeling diodes.

In order to mimic the bond wire lift off, we have intentionally detached the bond wires in a sequential manner and then observed the SSTDR output. We found this is the only controlled way to emulate a specific number of bond wire detachment, and the number of disconnected bond wires cannot be guaranteed using the accelerated aging techniques. This arrangement is shown in Figure 24(a), and the actual IGBT package is shown in Figure 24(b). The top IGBT's collector terminal was connected to the silicon die through 24 bond wires. The Top IGBT (shown in Figure 9) consists of three IGBT devices connected in parallel, and each of them has 8 bond wires, and 3 diodes are connected in anti-parallel fashion. Thus, the Top IGBT has total of 24 bond wires. Figure 24(c) shows the close-up view of the IGBT module. Similarly, the bottom IGBT has another 3 parallel IGBT devices with a total of 24 bond wires, and three anti-parallel diodes. The total current through the entire IGBT module is shared among these 48 bond wires. Therefore, any lift-off associated to any of these wires will lead to increase in current path resistance and will inhibit natural current flow to the IGBTs. The main task was to investigate if the SSTDR data could detect these lift-off events once we sequentially disconnected these wires.




(a) (b) (c)

Figure 24: (a) The actual test setup (b) Photograph of the actual IGBT module used with and without top cover (c) Close-up view of the IGBT bond wires.

The protective gel layer in the IGBT module was removed prior to the testing in order to get easier access to the bond wires. The module was submerged in the Digesil NC Xtra solution (a polymer remover) until the gel layer was completely removed. Isolated +15 V DC voltages were applied across the gate and emitter of both the top and bottom IGBT modules. SSTDR data were recorded for seven instances (6, 12, 18, 24, 30, 36, and 42 lifted bond wires) at SSTDR center frequency of 12MHz and 48MHz. The peak amplitudes were compared with the corresponding peak amplitudes obtained from the simulation. Figure 25 shows the comparable results at 12MHz, and Figure 26 represents the result obtained at 48MHz, and the simulation and experimental data are in very close agreement. These figures also show that when the module have 24 lifted bond wires, the magnitude is the minimum. The experiments and simulations were conducted for multiple times in multiple modules, and all of the results showed similar pattern. The reason behind this is yet unknown, however, future research will address this phenomenon and find out the underlying reason behind it. Since both results correspond to each other and are repeatable, it is apparent that the location and number of lifted bond wires can be identified if the results from the both gate terminals are compared.

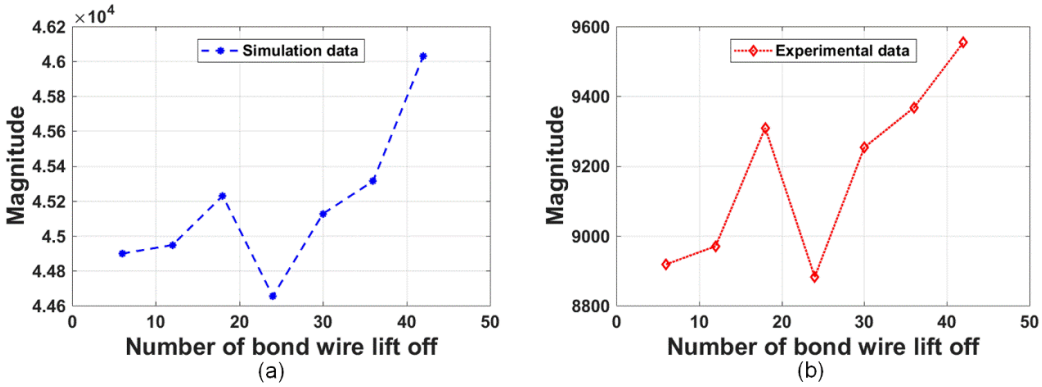



Figure 25: Simulation and experimental results show the similar pattern in the peak magnitude with equal number of bond wire lift off scenario at **12MHz** frequency (a) obtained through simulation (b) recorded from experiments

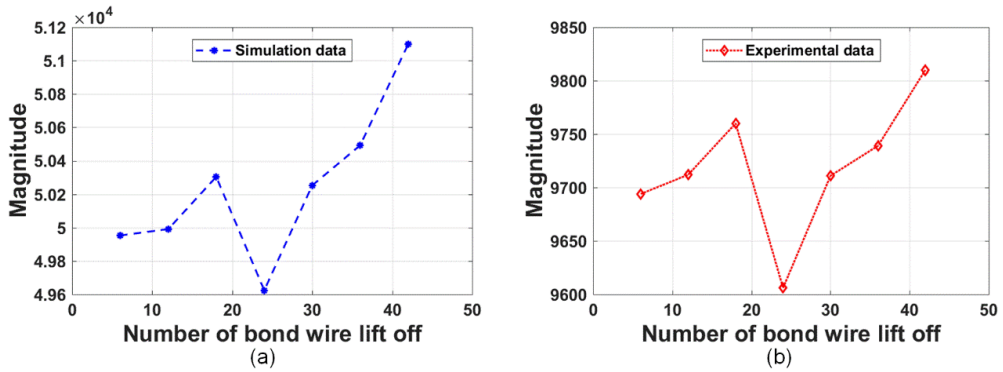



Figure 26: Simulation and experimental results show the similar pattern in the peak magnitude with equal number of bond wire lift off scenario at **48MHz** frequency (a) obtained through simulation (b) recorded from experiments

## 5.5 Conclusions

SSTDR based technique is one of the few degradation monitoring methods that is able to estimate aging and detect wire fault *in-situ*. Based on the reflectometry principle, the RL-equivalent circuit was simulated and the experimental data were recorded. These plots show that both of the results follow the similar trend, and therefore, the equivalent circuit is a true representation of the bond wires present in FF450R12ME4 IGBT power module. In addition, the SSTDR amplitudes show a direct correlation with the $V_{CEON}$ data obtained from active

power cycling. Thus, it is possible to determine the location of the lifted BW. The research outcome documented in this manuscript shows that the total number of BW liftoffs technique can be extremely helpful in the field applications where the collector-emitter nodes are not easily accessible due in high voltage applications. This method can also be extended to any converter circuit topology provided that the data are collected from the gate terminals of every module which is very feasible. Unlike collector terminal, the gate terminal is always at the lower potential level which significantly helps in the design phase of any condition monitoring hardware. Since electrical parameter measurement is not required, this technique not only reduces the measurement error but also helps in designing the SSTDR hardware at a much lower rating. Even with proper scaling the hardware can be incorporated in the gate driver board which will allow the system to be monitored autonomously.

# CHAPTER 6

# ULTRASOUND BASED DEGRADATION DETECTION

## 6.1 Introduction

Among non-destructive evaluations, ultrasound based tests have become popular in recent times. The application of ultrasound based crack-detection on large objects are well explored area. However, their potential in degradation detection of high power IGBT/MOSFET modules has not yet been utilized. Existing ultrasound based crack or void detection techniques are either too expensive and/or requires a fluid couplant to submerge the DUT/structure to be tested [44]. Confocal scanning acoustic microscopy (CSAM) based state-of-health identification is very popular in a semiconductor die and die-attach between the copper layer and substrate [45] - [47]. However, this technique cannot be used in a live circuit for package level degradation detection due to the size and medium constraint of the CSAM setup (requires the wafer to be submerged in water). In addition, it takes a long time to scan the device under test compared to any other existing condition monitoring method. Electromagnetic acoustic transducers (EMATs) does not require any couplant, however, they require high current injections for testing, and their efficiency is not as effective as the piezo-electric transducers [48]. In addition, the spread spectrum ultrasound technique requires highly precise transducer and couplant control to generate reasonably reliable results, and this technique has only been applied to large structures such as steel blocks [49] - [50]. In this research work, we have proposed a novel method based ultrasound resonators which is able to detect bond wire related aging in IGBT power modules. Although, the testing were conducted in IGBT modules, the method is equally applicable in power MOSFETs as well as in power converters/inverters.

The proposed ultrasound-based technique has the following advantages over existing methods:

i. Ultrasound resonator based method is able to detect bond wire lift off related aging in-situ, and irrespective of the operating condition of the module or converter.

ii. Unlike other ultrasound based methods, it does not require any liquid couplant, and gathers data instantly and continuously.

iii. This method significantly reduces the overall cost compared to the other condition monitoring methods where additional sensors are required to measure precursor parameters.

iv. This method can be integrated with the gate driver module if properly scaled.

Therefore, it is expected that the successful implementation of this technique will create a seminal impact in estimating remaining life especially for IGBTs.

## 6.2 Ultrasound Fundamentals and Sympathetic String Theory

### 6.2.1 Ultrasound resonator – a new way of testing electronics live

Ultrasound is one of the most common applications of non-destructive evaluation (NDE) method for crack detection and characterization in material structures [177]. This acoustic-ultrasound technique can also be used to find internal surface defects and discontinuities in power switching devices where cracks and voids along with bond wire lift-offs are formed due to package related failures. This non-destructive testing technique is based on the determination of acoustic transmission and reflection at the boundary of two materials having different acoustic impedances. In view of this fact, ultrasonic waves are also transmitted and reflected at the junction interface between materials with different acoustic impedances

that are formed due to deformation of materials in the device package such as cracks and voids formation due to delamination in the die-solder layer interface, bond wire lift-off and heel crack or aluminum metallization reconstruction. The amount of energy that is transmitted or reflected depends on the contrast in acoustic impedance (Z). The greater the impedance mismatch, the higher the percentage of energy that will be reflected at the interface or boundary between one medium and another. If the acoustic impedances of two medium is said to be $Z_1$ and $Z_2$ then the following equation can be used to express the reflection coefficient (R) [178]:

$$R = \left(\frac{Z_2 - Z_1}{Z_2 + Z_1}\right)^2 \tag{21}$$

The relationship between the spectral amplitude of the signal backscattered by an interface of two mediums and the acoustic impedances of these mediums is expressed below in equation (22) [178].

$$A_r = K_r \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{22}$$

Also, the spectral amplitude of the transmitted acoustic signal is shown in equation (23) [179].

$$A_t = K_t \frac{Z_2}{Z_2 + Z_1} \tag{23}$$

Where, $A_r$= spectral amplitude of the reflected signal, $A_t$ = spectral amplitude of the transmitted signal, $Z_1$= acoustic impedance of the first medium, $Z_2$ = acoustic impedance of the second medium, $K_r$, $K_t$= constants which depend on the transfer functions of the acoustic signal paths. For an IGBT module (for example, we used FF450R12ME4) the bond wires are encapsulated in a silicone gel layer to prevent moistures to come in contact with the die. Therefore, a contrast in acoustic impedance exists between the gel layers ($Z_2$) and the bond wires ($Z_1$). Once there is a crack or lift off associated with these bond wires, the spectral

amplitude of the reflected wave will be different than the corresponding amplitude for a healthy module. Using this phenomenon, the bond wire lift off related device degradation can be identified using the ultrasound resonators.

Ultrasonic transducers or ultrasonic resonators are a type of acoustic sensor that can be used as both transmitter and receiver. As shown in Figure 27, if this ultrasonic transducer can be mounted in such a way that the transmitted ultrasonic beam can be impinged on a surface crack and voids in a solid at an incident angle of θ, the emitted energy distribution will be the result of contribution from two components [177]. The first component (D) is the diffraction of a ray at the tip of the crack creating a spherical wave front from the mode conversion, and the second one (R) is the wave reflected from the mouth of the surface crack. The location and the depth (d) of the surface crack or void can be determined as follows:

$$d = \frac{\Delta l}{2cos\theta} = \frac{V\Delta t}{2cos\theta} \quad (24)$$

Where, V denote the velocity of the incident wave; Δt is the difference of the arrival times and Δl is the path difference between these two wave components. It is important to note that based on the incident angle (θ), depth and location of the surface defects, the position of the receiver sensor needs to be adjusted to capture the reflected signal components of maximum energy. Considering this fact, the optimized number of sensors along with their optimum locations are needed for each IGBT chip to determine their corresponding surface defects.

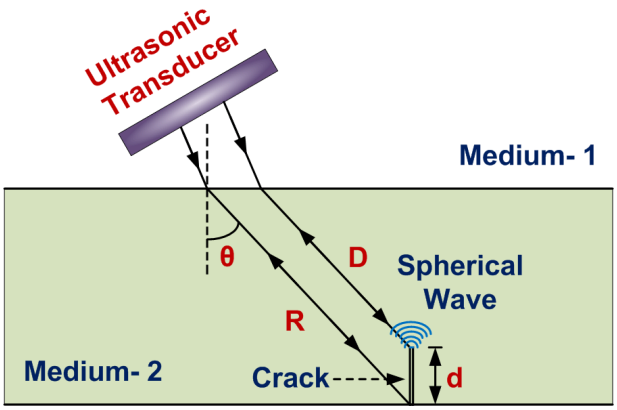


Figure 27: Interaction of an ultrasonic shear wave from a surface crack

### 6.2.2 Sympathetic resonance in acoustic string instrument

Sympathetic resonance or vibration can be defined as "resonant or near-resonant response of a mechanical or acoustical system excited by energy from an adjoining system in steady-state vibration" [180]. Several musical instruments use the sympathetic resonance in order to produce characteristic sounds. These instruments include but are not limited to Sitar (shown in Figure 28(a)), Sarangi, Viola D'amore, Baryton, Sarod, Ukelin, and so on [181]. The basic principle is to excite one string of any of these instruments, and other strings will resonate at their either fundamental or harmonic frequencies. The strings of such musical instruments are usually connected to a vibrating body, known as the soundboard. This soundboard is made of multiple materials with compound shapes. This helps in generating efficient sound propagation. Thus, creating an effective coupling between the soundboard and the strings, it is possible to vibrate one string if another string is excited. This phenomenon is referred as the sympathetic resonance [180].

The sympathetic resonance is not only important in musical applications but also plays a vital role in the field applications of electric machineries. For example, if two or more motors

are installed on the same base, then the vibration energy may transfer to the nearby motor/machine and may damage the machine even if it is in standby mode. This will only occur if the vibrating frequency of the running machine matches the resonance frequency of the nearby motor, which in other word is due to the sympathetic resonance [182]. So, the vibration signature, both the frequency and amplitude, is useful in fault diagnosis of the electric motors. Another application of sympathetic resonance can be found in [183], where the authors have measured the Young's modulus of biological electret-bone.

Ultrasonic based bond wire welding has become very popular in recent times due to its higher reliability compared to tradition soldering techniques [184]. However, to detect the bond wire related degradation using ultrasound resonators, the first and foremost task is to find out the resonant frequency of the bond wires present in the IGBT module. Authors in [185] – [186] have worked on establishing a relationship between the resonant frequency and the length of the bond wire. In order to create a damage in a bond wire two things play important role depending on the length of the bond wires; resonant frequency and the magnitude of resonance. Following two equations can be referred to explain this relationship [185]:

$$\omega_r = \frac{k_1 d}{l^2} \quad (25)$$

$$a_r = k_2 l^4 \quad (26)$$

Where, $\omega_r$ = resonant frequency = $2\pi f_r$, $k_1$ = constant based on bond wire material, d = diameter of the bond wire, l = length of the bond wire, $a_r$ = resonant amplitude, $k_2$ = constant based on bond wire material.

According to these two above mentioned equations, a longer wire requires a lower resonant frequency ($f \propto \frac{1}{l^2}$) but a higher magnitude ($a \propto l^4$). Fortunately, all of the 48 bond

wires in the FF450R12ME4 are of equal length. Therefore, the resonators could be operated at a specific frequency to initiate the resonance in the bond wires instead of sweeping the frequency. However, it should be noted that the resonant frequency would vary from module to module depending on the package dimensions. Most importantly, the resonant magnitude and/or frequency would be different if there is a bond wire lift-off or crack present in the module. Any detached bond wire will perturb the sympathetic resonance, and any crack or void will alter the tension in the bond wire resulting in altered resonance signature. Fortunately, the resonators can be excited at other harmonic and sub-harmonic frequencies which will enable us to record the vibration signatures of the affected bond wires. Thus, we will be able to differentiate between a healthy and an aged module.

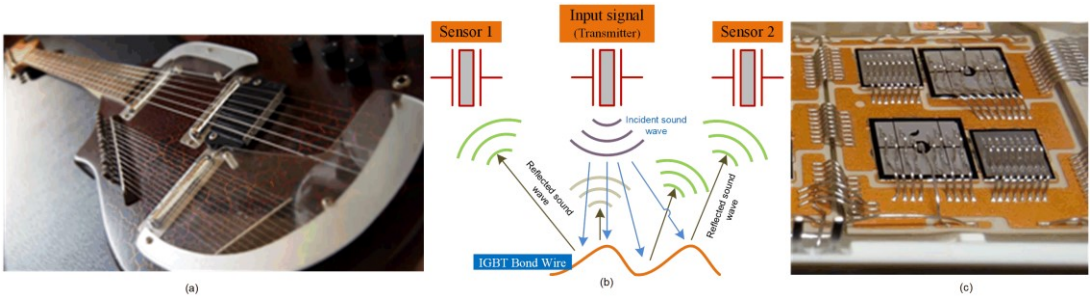



Figure 28: (a) Sympathetic strings in an electric Sitar (Courtesy: Wikimedia), (b) incident and reflected signal to and from the IGBT bond wire, (c) actual IGBT bond wires

Table XI shows the acoustic behavior of the IGBT gel layer. The ultrasound wave attenuates about 19% to propagate through the gel layer. Similarly, the reflected signal will experience a maximum 19% attenuation until it reaches the receiver transducer. Because the bond wires' curved shapes, a wire's top edge penetrates half way inside the gel layer, thus making the total travel distance through the gel layer is 0.5X + 0.5X = 1.0X, where X is the thickness of the gel layer. In our case, X was 8mm. Therefore, the total attenuation was only

6.93dB, and the input energy from the ultrasound sensors are sufficient to interact with the bond wires and to reflect back to the receiver sensors. Figure 28(b) shows several interactions between the acoustic wave and a bond wire including few possible reflection paths.

Table XI ACOUSTIC BEHAVIOR OF THE GEL LAYER INSIDE FFF450R12ME4 DUAL PACK IGBT MODULE

| Density of silicone gel (ρ) $Kgm^{-3}$ | Acoustic Velocity in gel layer(ν) $ms^{-1}$ | Acoustic impedance of gel layer (Z=ρν) MRayls | Attenuation coefficient in gel layer ($\propto$) $dBcm^{-1}$ | Output power of the resonator at 100mvp-p input voltage ($A_0 = 10\log\frac{I}{I_0}$) dB | Thickness of the gel layer (t) cm | Attenuated amplitude ($A(z)=A_0 e^{\frac{-\propto Z}{8.7}}$) | Total attenuation (dB) |
|---|---|---|---|---|---|---|---|
| 700 | 1490 | 1.043 | 2.175 | 36.81 | 0.8 | 29.88 | 6.93 (18.82%) |

## 6.3 Analytical Model of Ultrasound Wave Propagation in IGBT Module

### 6.3.1 Modes of sound wave propagation:

Multiple atoms constitute a material and each material may be subjected to oscillatory motion about their steady state positions if an external vibrational force is applied. However, this oscillatory behavior can arise only if the material or the medium is stressed within its elastic limit. The electrostatic restoration force between the particles of the medium combines with the inertia of the particles and leads to the oscillatory motion of the medium. Based on the characteristics of this oscillation, sound wave can travel through a medium in four major modes namely, (i) longitudinal waves (ii) shear waves (iii) surface waves and (iv) plate waves. In ultrasound based testing, longitudinal and shear waves are most commonly utilized modes of sound propagation [187]. It is important to know how these two waves are propagated through a medium. Figure 29 illustrates the particle movements related to the longitudinal and shear waves.

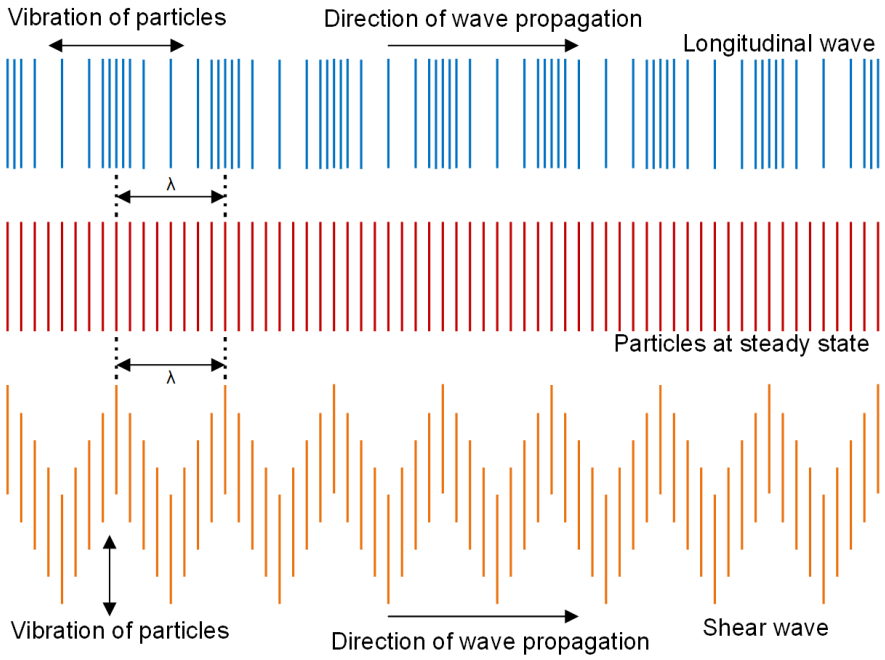



Figure 29: Particle movement illustration of longitudinal and shear waves

A brief overview of longitudinal and shear wave modes is provided below:

i. *Longitudinal wave:* The oscillation occurs in parallel with the direction of wave propagation in longitudinal wave. The energy associated with this wave propagation transfers by a series of compression and expansion movements of the atoms present in the medium.

ii. *Shear wave:* In shear wave, the particles oscillate perpendicular to the direction of wave propagation. This is why it is also called transverse wave. Transverse wave more effectively propagates in solid than liquid or gases. However, shear waves are relatively weak compared to the longitudinal waves.

In any ultrasound based condition monitoring technique, the placement of the transducer is important because the angle between the transducer and the surface to be inspected defines which wave mode or modes will effectively propagate through the medium

and/or reflect from the surface under inspection. This angle is defined as the critical angle. There are three critical angles related to the ultrasound wave propagation: first, second, and third critical angles [188]. Figure 30 shows these angles where $\theta_1$ represents first critical angle, $\theta_2$ represents second critical angle, and $\theta_3$ is defined as the third critical angle.

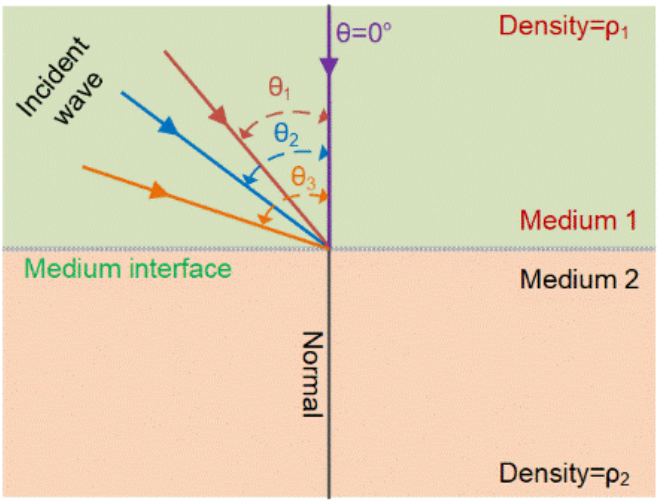



Figure 30: Critical angles for an incident ultrasound wave

Following scenarios explain the relative relations between the incident angles and the wave modes:

*Scenario-1:* When the sound wave intersects the surface under inspection at an angle of $\theta = 0°$, it only reflects or refracts longitudinal waves, there will be no shear wave in either of the mediums.

*Scenario-2:* If the angle of incident is between 0 and $\theta_1$, $(0 < \theta < \theta_1)$ both longitudinal and shear waves will reflect and travel into the second medium.

*Scenario-3:* When $\theta_1 < \theta < \theta_2$, longitudinal wave does not penetrate into the second medium, only shear wave is refracted into the second medium. However, both of these waves are reflected into the first medium from incident point of the medium interface.

*Scenario-4:* When $\theta_2 < \theta < \theta_3$, none of the waves penetrate into the second medium and both of the longitudinal and shear waves reflects back from the surface of incident into the first medium.

*Scenario-5:* When $\theta \geq \theta_3$, longitudinal waves disappear and only shear waves reflect back into the first medium.

Therefore, the location of the ultrasound transducers and receivers are highly important in order to detect the reflected wave mode coming from the medium interface.

### 6.3.2 Frequency, wavelength, and defect detection:

In non-destructive testing (NDT) such as ultrasound based defect detection is highly dependent on the ultrasound frequency and the wavelength of the propagating sound wave [189]. The detection ability in an ultrasound based technique is inversely proportional to the wavelength of the sound wave- shorter the wavelength, higher the chances of detecting smaller discontinuity i.e., better the sensitivity. The relationship between the frequency, wavelength, and velocity of the sound wave in a medium can be described by the following equation:

$$\lambda = \frac{V}{f} \tag{27}$$

Here, $\lambda$ is the wavelength of sound wave, f is the frequency, and V represents the velocity of the sound wave in the medium. Since the velocity is constant in a uniform medium, higher the frequency of the sound wave shorter the wavelength will be. Therefore, smaller surface defects, voids, bond wire lift-offs and heel cracks are more likely to be detected when the frequency is higher. It is important to note that, the discontinuity should be at least one-half wavelength long for a successful and repetitive detection [190]. Resolution is important as well since it defines the ability of the system to detect discontinuities that are close to each other. Resolution of the ultrasound technique is also directly proportional to the frequency of

the propagating sound wave i.e., shorter the wavelength higher the resolution [191]. However, selection of a very high frequency sound wave may undesirably affect the condition monitoring system. If the surface to be inspected or the material has a very high grain size and the frequency is very high, then it is possible that the spacing of the large grained surfaces may be considered as the discontinuity while conducting the ultrasound test. Therefore, it is important to know about the material to be tested and accordingly choose the frequency of the piezoelectric crystal. It is also to be remembered that the penetration depth of the sound wave is inversely proportional to the frequency, and therefore, the frequency selection is the most important criterion in ultrasound based defect detection.

Another important parameter in ultrasound based defect detection is the acoustic impedance of the medium. It is clear from equation (21) and equation (22) that higher the impedance contrast between the mediums, greater the reflection occurs. The relation between the acoustic impedance and the velocity of the sound wave can be expressed by the equation below [192]:

$$Z=\rho V \tag{28}$$

Here, Z is the acoustic impedance, ρ is the density of the medium, and V represents the velocity of sound through the medium. It is apparent that the velocity of sound varies from one medium to another because the density and elastic constant is different for different materials. Following equation shows the mutual relationship between these three parameters:

$$V = \sqrt{\frac{E}{\rho}} \tag{29}$$

Where, V is the velocity of the sound, E is the elastic constant (Young's modulus) of the medium, and ρ is the density of the medium.

### 6.3.3 Attenuation of ultrasound wave

Attenuation in the sound wave occurs due to the scattering and absorption in the medium. As a result, the intensity of the ultrasound wave reduces with distance as the wave propagates through any material. Therefore, attenuation is an important parameter in ultrasound based non-destructive evaluation (NDE). Following equation expresses the mutual relationship between the attenuation constant of a medium and the amplitude of the attenuating sound wave:

$$A = A_0 e^{-\mu_A x} \tag{30}$$

Here, $A_0$ is the un-attenuated amplitude of the sound wave, A is the attenuated amplitude at a distance x in the direction of wave propagation, and $\mu_A$ is the attenuation factor. The attenuation coefficient (α) can be experimentally measured using the following equation [192] - [193]:

$$\alpha = \frac{-20}{2(j-i)d} \log \frac{A_j}{A_i} \tag{31}$$

Where, $A_i$ and $A_j$ are the amplitude of the $i^{th}$ and $j^{th}$ echoes and d is the distance travelled by the ultrasound wave.

Now, the attenuation coefficient, α, can be expressed in terms of $\mu_A$ since 20 log ($A/A_0$) represents the amplitude reduction in decibel (dB), and therefore,

$$\alpha = 20 * \log(e) * \mu_A = 8.7\mu_A \tag{32}$$

If we replace $\mu_A$ from equation (32) into equation (30), we get that the attenuated amplitude of the propagating ultrasound wave is,

$$A = A_0 e^{\frac{-\alpha x}{8.7}} \quad (33)$$

Later in this section, equation (33) will be useful in deducing the ultrasound wave amplitude received by the piezoelectric sensors.

### 6.3.4 Snell's Law, wave equation, and reflection amplitudes

A dual pack IGBT module manufactured by Infineon has been chosen as the device under test (DUT). This module (FF450R12ME4) has 6 IGBT devices and 6 corresponding freewheeling diodes. These diodes and IGBT devices are connected via bond wires. A silicone gel is used to seal off these bond wires and devices. When piezoelectric crystals are used to apply ultrasound signal, the elastic wave produced from these resonators can propagate through the gel layer in the form of compressional (longitudinal) and transverse (shear) waves depending on the angle of incident. Figure 31 shows the reflection and refraction phenomena at the medium interface when the sound wave has an oblique incident angle and the density of two media are different i.e., the acoustic impedances are distinct.

According to Snell's law:

$$\frac{\sin\theta_{LI}}{V_{L1}} = \frac{\sin\theta_{LR}}{V_{L2}} = \frac{\sin\theta_{TI}}{V_{T1}} = \frac{\sin\theta_{TR}}{V_{T2}} \quad (34)$$

Now, consider the gel layer has the density ρ, the displacement potentials corresponding to compressional and transverse velocities are Φ and **Ψ** respectively, and then the ultrasound wave can be characterized using the well-known elastic wave equation as shown below [194]:

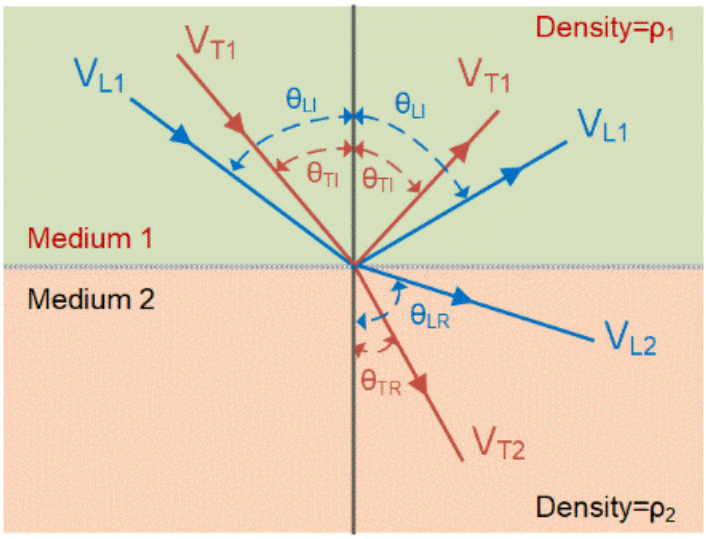



Figure 31: ultrasound wave interaction at the interface of two media.

$$\nabla\left[(\boldsymbol{\lambda}+2\mu)\nabla^2\boldsymbol{\Phi}-\rho\frac{\partial^2\Phi}{\partial t^2}\right]+\nabla\mathrm{x}\left[\mu\nabla^2\,\boldsymbol{\Psi}-\rho\frac{\partial^2\boldsymbol{\Psi}}{\partial t^2}\right]=0 \tag{35}$$

Equation (V) is satisfied if

$$(\boldsymbol{\lambda}+2\mu)\,\nabla^2\boldsymbol{\Phi}-\rho\frac{\partial^2\Phi}{\partial t^2}=0 \tag{36}$$

And,

$$\mu\nabla^2\,\boldsymbol{\Psi}-\rho\frac{\partial^2\boldsymbol{\Psi}}{\partial t^2}=0 \tag{37}$$

Equation (33) and (34) represent the wave potentials for longitudinal and shear waves respectively.

Let us assume that the ultrasound wave is traveling in the vertical plane of *x, y*. Consider that the physical quantities will be uniform in the *z*-direction. Also, suppose that all the wavenumber vectors are inclined in the positive *x*-direction, then Φ and **Ψ** will have the solution in the following form [173]:

$$\Phi=\mathrm{A_L}e^{\mathrm{i}(\xi\mathrm{x}-\varphi\mathrm{y}-\omega\mathrm{t})}+\mathrm{B_L}e^{\mathrm{i}(\xi\mathrm{x}+\varphi\mathrm{y}-\omega\mathrm{t})} \tag{38}$$

$$\boldsymbol{\Psi} = \mathrm{A_T} e^{\mathrm{i}(\zeta x - \beta y - \omega t)} + \mathrm{B_T} e^{\mathrm{i}(\zeta x + \beta y - \omega t)} \tag{39}$$

Where, $A_L$, $A_T$ are incident longitudinal and transverse wave amplitudes respectively. $B_L$ and $B_T$ are reflected longitudinal and transverse wave amplitudes respectively. Also, ξ and φ are the wavenumber component of the longitudinal wave with the polar coordinate($k_L \sin\theta_L$ , $k_L \cos\theta_L$). Similarly, ζ and β are the wavenumber component of the transverse wave with the polar coordinate($k_T \sin\theta_T$ , $k_T \cos\theta_T$). The relationship between the reflection and incident amplitudes can be expressed as shown in below [195]:

$$\begin{bmatrix} \mathrm{B_L} \\ \mathrm{B_T} \end{bmatrix} = \begin{bmatrix} \mathrm{S_{LL}} & \mathrm{S_{TL}} \\ \mathrm{S_{LT}} & \mathrm{S_{TT}} \end{bmatrix} \begin{bmatrix} \mathrm{A_L} \\ \mathrm{A_T} \end{bmatrix} \tag{40}$$

Here, $\mathbf{S}(\theta_L, \theta_T) = \begin{bmatrix} \mathrm{S_{LL}} & \mathrm{S_{TL}} \\ \mathrm{S_{LT}} & \mathrm{S_{TT}} \end{bmatrix}$ represents the scattering matrix and the subscripts represent the incident and reflected waves. Such as $S_{LT}$ represents the reflected transverse wave due to incident longitudinal wave of unit amplitude. Expressions for the index terms in $\mathbf{S}(\theta_L, \theta_T)$ are shown below:

$$\mathrm{S_{LL}} = \frac{\sin 2\theta_L \ \sin 2\theta_T - k^2 cos^2\ 2\theta_T}{\sin 2\theta_L \ \sin 2\theta_T + k^2 cos^2\ 2\theta_T} \tag{41}$$

$$\mathrm{S_{TL}} = \frac{-2k^2 \sin 2\theta_T \ \cos 2\theta_T}{\sin 2\theta_L \ \sin 2\theta_T + k^2 cos^2\ 2\theta_T} \tag{42}$$

$$\mathrm{S_{LT}} = \frac{2 \sin 2\theta_L \ \cos 2\theta_T}{\sin 2\theta_L \ \sin 2\theta_T + k^2 cos^2\ 2\theta_T} \tag{43}$$

$$\mathrm{S_{TT}} = \frac{\sin 2\theta_L \ \sin 2\theta_T - k^2 cos^2\ 2\theta_T}{\sin 2\theta_L \ \sin 2\theta_T + k^2 cos^2\ 2\theta_T} \tag{44}$$

Now, equation (40) can be extended for the FF450R12ME4 IGBT dual pack module. Since it has six IGBT devices, the general relationship between incident and reflected amplitudes at these six locations for both longitudinal and transverse waves can be written in the matrix form as shown below:

$$B_R = S_i(\theta_L(i), \theta_T(i))\, A_I \tag{45}$$

Where,

$B_R = \begin{bmatrix} B_{LR}(i) \\ B_{TR}(i) \end{bmatrix}$, $A_I = \begin{bmatrix} A_{LI}(i) \\ A_{TI}(i) \end{bmatrix}$, $S_i(\theta_L(i), \theta_T(i)) = \begin{bmatrix} \mathrm{S_{LL}} & \mathrm{S_{TL}} \\ \mathrm{S_{LT}} & \mathrm{S_{TT}} \end{bmatrix}$. Here, i represents the location of the six IGBT devices inside the dual pack module where i=1, 2, 3,4,5,6.

Also,

$$\left.\begin{array}{l} \mathrm{A_{LI}} = [\mathrm{A_{L1}}\ \mathrm{A_{L2}}\ \mathrm{A_{L3}}\ \mathrm{A_{L4}}\ \mathrm{A_{L5}}\ \mathrm{A_{L6}}]^{\mathrm{T}} \\ \mathrm{A_{TI}} = [\mathrm{A_{T1}}\ \mathrm{A_{T2}}\ \mathrm{A_{T3}}\ \mathrm{A_{T4}}\ \mathrm{A_{T5}}\ \mathrm{A_{T6}}]^{\mathrm{T}} \\ \mathrm{B_{LR}} = [B_{\mathrm{L1}}\ \mathrm{B_{L2}}\ B_{\mathrm{L3}}\ \mathrm{B_{L4}}\ \mathrm{B_{L5}}\ \mathrm{B_{L6}}]^{\mathrm{T}} \\ B_{\mathrm{TR}} = [\mathrm{B_{T1}}\ \mathrm{B_{T2}}\ B_{\mathrm{T3}}\ \mathrm{B_{T4}}\ \mathrm{B_{T5}}\ \mathrm{B_{T6}}]^{\mathrm{T}} \\ \theta_{\mathrm{LR}} = [\theta_{\mathrm{L1}}\ \theta_{\mathrm{L2}}\ \theta_{\mathrm{L3}}\ \theta_{\mathrm{L4}}\ \theta_{\mathrm{L5}}\ \theta_{\mathrm{L6}}]^{\mathrm{T}} \\ \theta_{\mathrm{TR}} = [\theta_{\mathrm{T1}}\ \theta_{\mathrm{T2}}\ \theta_{\mathrm{T3}}\ \theta_{\mathrm{T4}}\ \theta_{\mathrm{T5}}\ \theta_{\mathrm{T6}}]^{\mathrm{T}} \end{array}\right\} \tag{46}$$

Now, the reflected amplitudes at the gel layer and bond wire interface will travel through the gel layer and return to the receiver sensors. For simplicity we will consider the FF450R12ME4 dual pack IGBT module as a confined system, and therefore, each of the sensors will receive reflections from all of these six IGBT locations and the overall reflection amplitude will be sum of these six signals. Now, using equation (33), the ultrasound signals received by sensor 1 can be expressed by the following equation:

$$\mathrm{B_{R_{S1}}} = B_{R_{11}} e^{\frac{-\alpha x_{11}}{8.7}} + B_{R_{12}} e^{\frac{-\alpha x_{21}}{8.7}} + B_{R_{13}} e^{\frac{-\alpha x_{31}}{8.7}} + B_{R\_14} e^{\frac{-\alpha x_{41}}{8.7}} + B_{R\_15} e^{\frac{-\alpha x_{51}}{8.7}} + B_{R\_16} e^{\frac{-\alpha x_{61}}{8.7}} \tag{47}$$

Or,

$$\mathrm{B}_{R\_Sk} = \sum_{i=1}^{6} B_{R\_ki} e^{\frac{-\alpha x_{ik}}{8.7}} \tag{48}$$

Here, k represents the location of sensors where k=1, 2, 3,4,5,6 and i is the location of the device. $x_{ik}$ represents the physical distance between the k$^{th}$ sensor and i$^{th}$ device (For example, Figure 32 shows these distances for sensor 1 and sensor 2).

$B_{R\_ki}$ is the un-attenuated amplitude for sensor k coming from device i, and $B_{R\_Sk}$ is the received attenuated signal by sensor k.

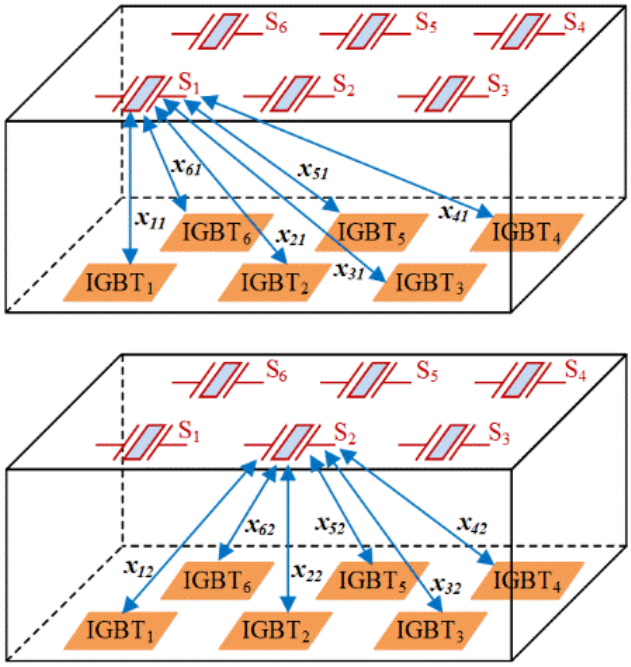



Figure 32: Representation of physical distance between devices and sensors to estimate the attenuated ultrasound signal received by the respective sensors (not drawn to scale).

Now, we can re-write equation (29) for all of the six sensor location in the matrix form as shown below:

$$\begin{bmatrix} B_{R\_S1} \\ B_{R\_S2} \\ B_{R\_S3} \\ B_{R\_S4} \\ B_{R\_S5} \\ B_{R\_S6} \end{bmatrix} = \begin{bmatrix} B_{R\_11} & B_{R\_12} & B_{R\_13} & B_{R\_14} & B_{R\_15} & B_{R\_16} \\ B_{R\_21} & B_{R\_22} & B_{R\_23} & B_{R\_24} & B_{R\_25} & B_{R\_26} \\ B_{R\_31} & B_{R\_32} & B_{R\_33} & B_{R\_34} & B_{R\_35} & B_{R\_36} \\ B_{R\_41} & B_{R\_42} & B_{R\_43} & B_{R\_44} & B_{R\_45} & B_{R\_46} \\ B_{R\_51} & B_{R\_52} & B_{R\_53} & B_{R\_54} & B_{R\_55} & B_{R\_56} \\ B_{R\_61} & B_{R\_62} & B_{R\_63} & B_{R\_64} & B_{R\_65} & B_{R\_66} \end{bmatrix} e^{X} \tag{49}$$

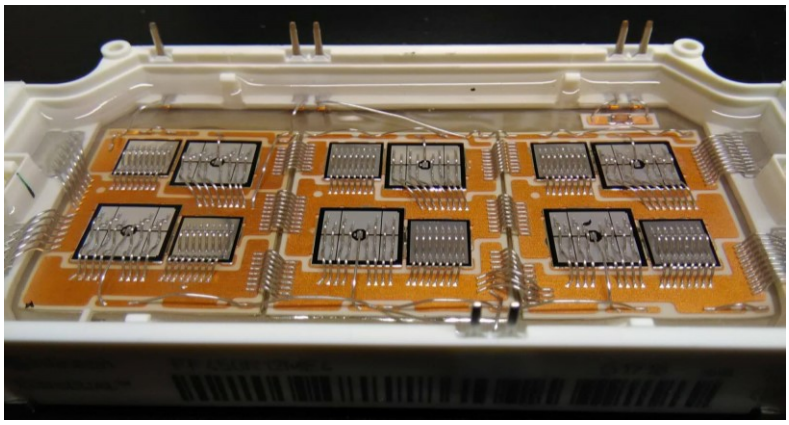
Where,

$$e^{X} = e^{\frac{-\alpha}{8.7}\begin{bmatrix} x_{11} & x_{12} & x_{13} & x_{14} & x_{15} & x_{16} \\ x_{21} & x_{22} & x_{23} & x_{24} & x_{25} & x_{26} \\ x_{31} & x_{32} & x_{33} & x_{34} & x_{35} & x_{36} \\ x_{41} & x_{42} & x_{43} & x_{44} & x_{45} & x_{46} \\ x_{51} & x_{52} & x_{53} & x_{54} & x_{55} & x_{56} \\ x_{61} & x_{62} & x_{63} & x_{64} & x_{65} & x_{66} \end{bmatrix}} \tag{50}$$

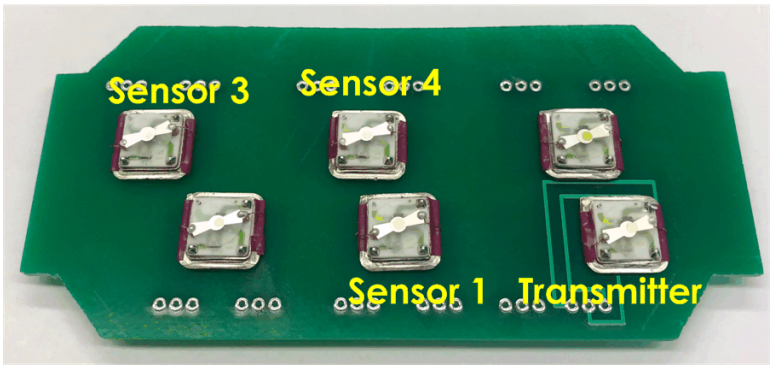
Following section will discuss the details of experiments and the corresponding results.

### 6.4 Experimental Setup and Results

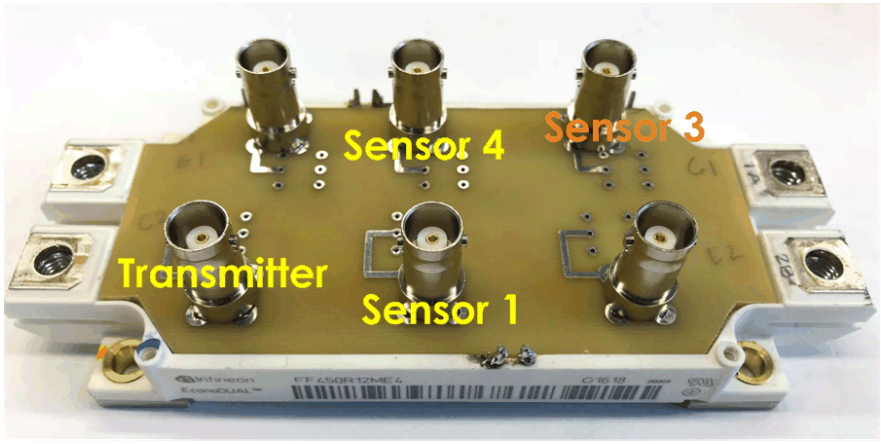
Inside large IGBT modules, the actual semiconductor devices are physically connected by multiple bond wires. For example, Infineon dual pack IGBT module (FF450R12ME4) was chosen as the DUT, which has six IGBT devices (three top and three bottom) and their corresponding free-wheeling diodes. Each of the device and diode pair is interconnected with eight bond wires, therefore, the entire module has total of 48 bond wires. At first, a healthy IGBT module (FF450R12ME4) was characterized using multiple ultrasound resonators. Tests were conducted at room temperature and data were recorded using a Keysight oscilloscope. The plastic back-plate of the IGBT was removed, and a PCB having six (6) 25 MHz acoustic resonators was used in place of the back-plate as shown in the Figure 33. Out of these six resonators, one was used as the transmitter, and the remaining five were used as receivers. The location of these resonators were consistent with the six IGBTs inside the package (IGBT package is shown in Figure 33(a)).



(a)



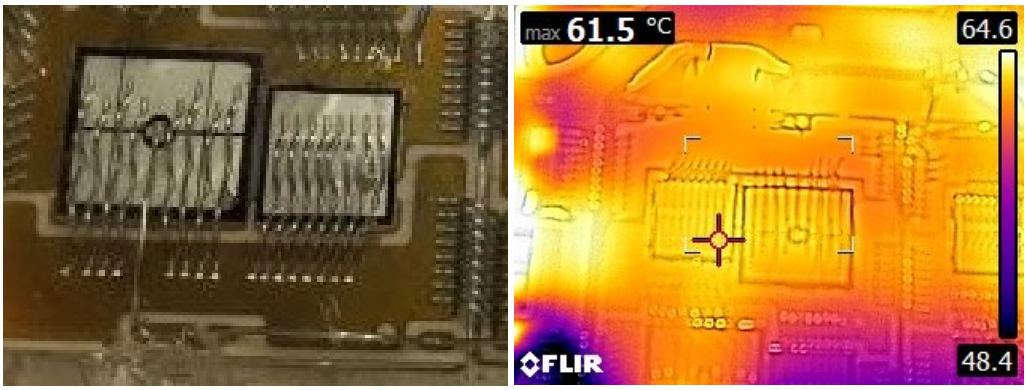

(b)



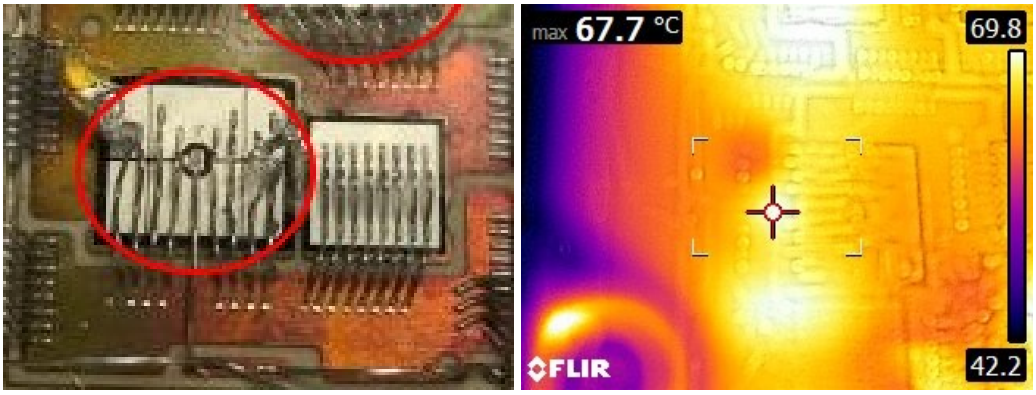

(c)

Figure 33: Experimental setup for ultrasound resonator-based condition monitoring of IGBT power module: (a) FF450R12ME4 IGBT dual pack module without top cover, (b) bottom view of the inserted PCB to show the resonators in prototype 1, (c) Top view with BNC connectors in prototype 2

To create bond wire lift off incidents in a controlled manner, we disconnected multiple bond wires in several locations rather than aging the IGBT using an accelerated aging station. We intentionally did it to avoid uncertainty and quick turn-around time to validate our theory. We also used a FLIR thermal camera to monitor the current crowding due to damaged bond wires of a device inside the package. Figure 34(a) shows a healthy IGBT device with all eight (8) bond wires intact. For this device the corresponding thermal image was uniform without any significant hotspot. Figure 34(b) shows the actual photograph of the IGBT device with 3 bond wires detached, and the corresponding thermal image shows hotspot formation.



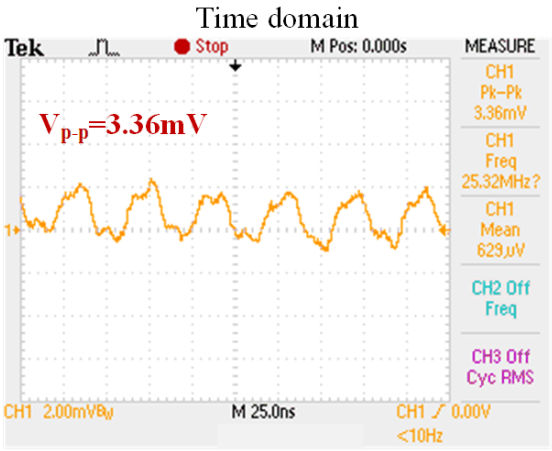

(a) Healthy device



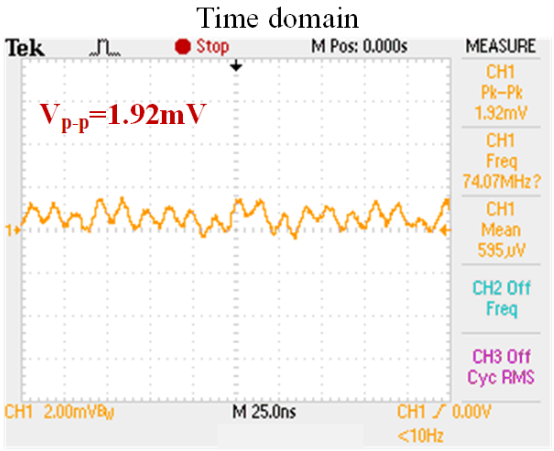

(b) Aged device

Figure 34: Bond wire lift off and corresponding current crowding (the red circle shows damaged bond wires).

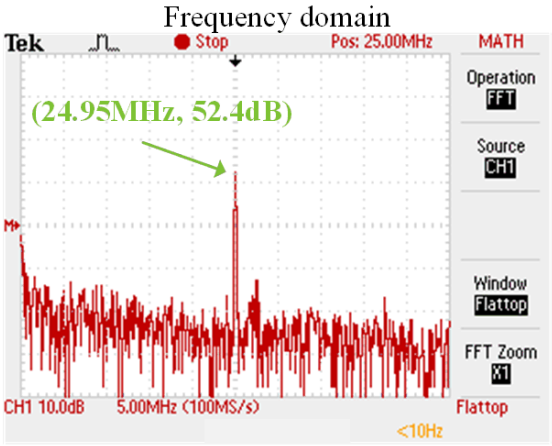
Figure 35 and Figure 36 show the ultrasound results obtained from the onboard sensors shown in Fig. 32(b). Figure 35 shows sensor 1 data in both time domain and frequency domain. Figure 35(a) shows the time domain data with all bond wires intact, and Figure 35(b) shows the time domain data when 3 bond wires are disconnected. Figure (c) and Figure (d) show the frequency domain data for these two events respectively.



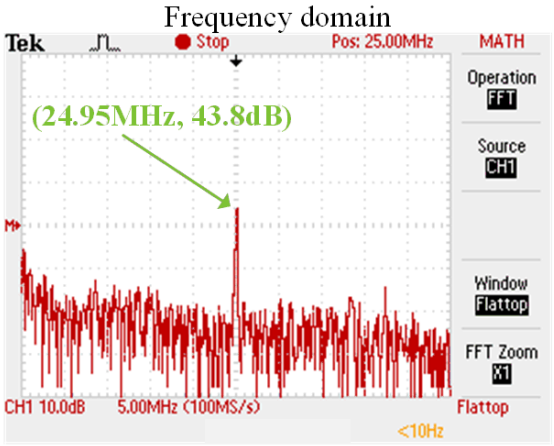

(a) Healthy IGBT




(b) IGBT with 3 damaged bond wire




(c) Healthy IGBT




(d) IGBT with 3 damaged bond wire

Figure 35: Time and frequency domain data from sensor 1


Figure 36: Time and frequency domain data from sensor 4

Figure 36 shows the time domain and frequency domain output signals obtained from sensor 4, and the results have been compared with a healthy system. It is quite evident that for any physical damage at any specific location, at least two sensors (sensors 1 and 4) produce reduced time and frequency domain output compared to a healthy module. We have observed similar response from sensors 3, and those results are shown in Figure 37. Sensor 1 detects a reduction of 8.4dB, and sensor 4 detects a huge 12dB in the frequency domain output. These reduced amplitudes are the clear indication of the IGBT's bond wire lift off phenomenon.

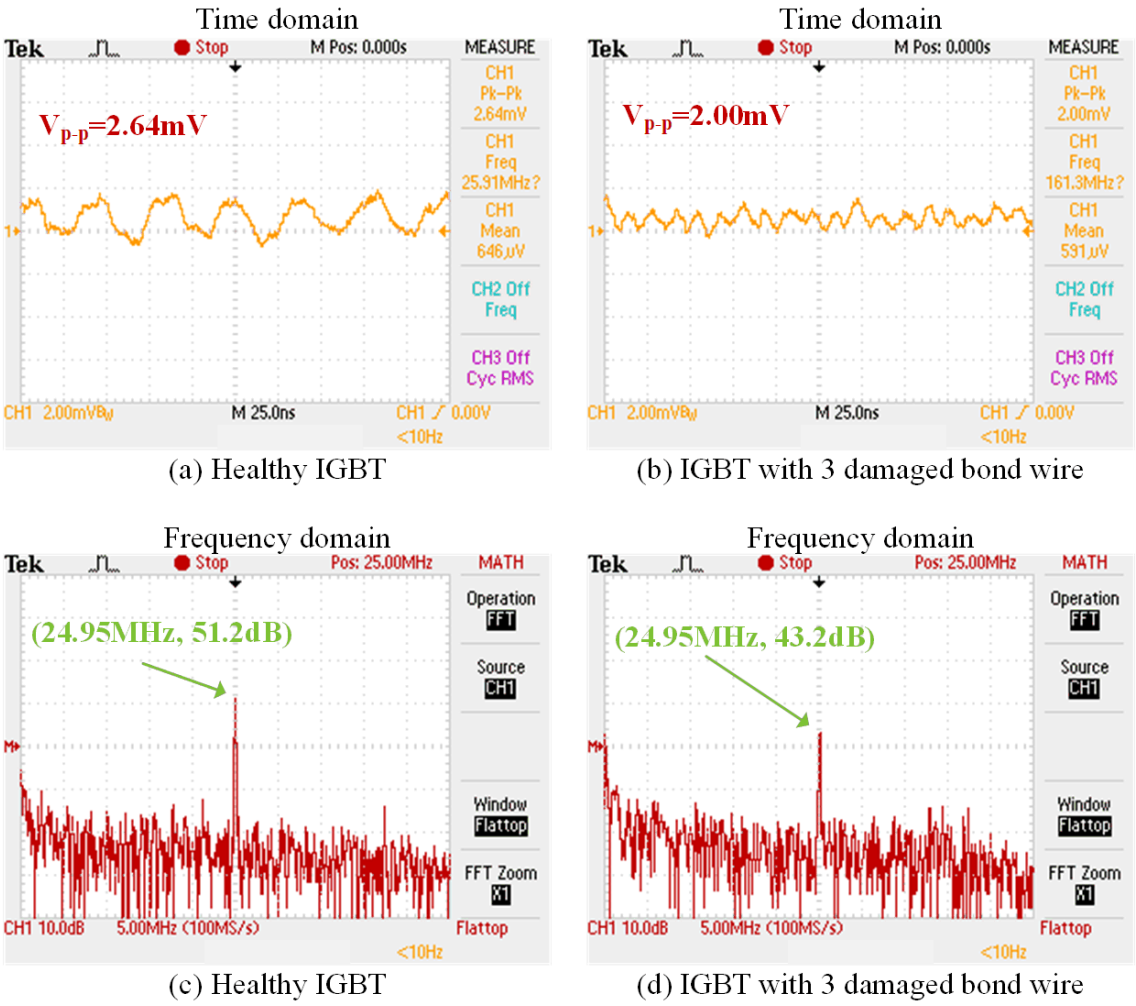



Figure 37: Time and frequency domain data from sensor 3

## 6.5 Conclusions

The research outcome documented in this chapter shows that it is possible to determine bond wire lift off related IGBT aging using the ultrasound resonators. Although the experiments were conducted on IGBT modules, this method is equally applicable to MOSFET power modules. Results obtained from experiments show a clear difference between the healthy and aged device in both time and frequency domain. The difference in the magnitude of the sensor output are the strong evidence of the aging of the device. The most attractive attribute of this method is that it is possible to detect aging *in-situ* and is independent of the

operating state of the modules- voltage and current levels. In addition, with proper scaling of the resonators, this method can also be incorporated into the future gate driver circuits in order to automate the state-of-health estimation process, making it more user-friendly as well as reducing the human error in measurement phase associated with the existing condition monitoring methods. However, there are several challenges associated with this method, and further research is necessary to mitigate those in order to successfully implement in the field applications. One of the major challenges for a successful field implementation is to determine the optimum number of sensors to detect the device location. In addition, the resonator used to verify the proposed methods are commercially available with steel enclosure, however, they need to be sourced or manufactured such that they do not require any additional effort to deploy in the field applications. Future research efforts will address all of these challenges.

# CHAPTER 7

# DEGRADATION DETECTION OF WIDE BANDGAP POWER DEVICES

## 7.1 Introduction

Silicon carbide (SiC) based power semiconductors are considered as a better replacement of Si devices due to their superior switching speed, thermal conductivity and breakdown electric field. Unfortunately SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) still have major limitations such as wafer defects, thermal runaway, electrical breakdown, and so on [196] – [197] because of not so mature manufacturing process compared to the Si counterpart. This fabrication related issue of SiC devices adversely affect the standard operation of power converters leading to a total failure of the system. Researchers have been continuously working on device reliability in order to better understand the failure modes and mechanisms in the power semiconductor devices. In doing so, the devices under test (DUTs) are aged in various methods considering the mission profiles to mimic the actual operating environment. Among these methods, active power cycling, thermal cycling, and passive thermal aging are the most commonly used techniques in recent times [103], [135], [198]. Active power cycling induces both the device related aging and package related aging, whereas, the passive thermal cycling causes the package related degradation alone. However, the ultimate target of an accelerated test is to age a device within a short time period and identify the aging either by measuring electrical parameters or by incorporating a new technique such as reflectometry. The electrical precursor parameter based detection could provide erroneous degradation information if the measurement is not fast or accurate [199] – [201]. In addition, this technique may not be used in a live circuit due to accessibility of the measurement nodes. On the other hand, reflectometry based aging detection such as SSTDR

based method can be done *in-situ* as well as it is independent of measurement error since this does not involve any electrical parameter measurement [41].

The traditional precursor parameter based aging detection having pros and cons can be found in many literature [27], [172], [202]. The experimental data recorded in [200] are reliable only if the MOSFET used in parallel with the DUT remains healthy over the time. In addition, the entire converter may fail if the MOSFET becomes short. Another live condition monitoring was achieved in [201], however, the results may provide inaccurate information if the parameters of the diodes have measurement error.

Recently, SSTDR based fault detection technique is gaining momentum in wire fault detection [39], [203], ground and arc fault detection in various photovoltaic applications [41] – [42], and in degradation detection of power semiconductor devices [43]. In case of MOSFETs, the SSTDR technique is able to identify the aging, however, it has never been used in any reliability studies for SiC based power switches so far. In addition, the previous SSTDR based methods applied the test signal either across the drain-source terminals or the output AC nodes [43], [204]. On the contrary, the proposed method can detect the device aging from the gate-source interface which remain at significantly lower potential compared to the drain-source terminals. On top of that, it was not clearly addressed how the auto-correlated amplitudes obtained from SSTDR hardware can be compared with the existing precursor parameters such as $R_{DSON}$. Through this research a direct correlation between the SSTDR amplitude and $R_{DSON}$ of the MOSFET has been established. Therefore, this research will allow us to estimate the aging of a power semiconductor device from the measurement of SSDTR amplitudes. In addition, this method can be extended to any converter topology in order to estimate the aging of the semiconductor devices.

Since this research work to identify the degradation of WBG devices based on SSTDR is a pioneer work, we have carried out three case studies in order to verify the applicability of the proposed method: (i) aging detection in discrete SiC MOSFETs, (ii) degradation detection of a SiC MOSFET based buck converter, and (ii) aging detection of thermally aged SiC and Si MOSFETs.

The experimental results suggest that SSTDR method is equally applicable to the WBG power semiconductors as well as the proposed method is able to detect aging from the gate-source terminals. As a result, the condition monitoring hardware can be designed at a significantly lower rating which will create a provision to integrate the hardware with the gate driver module of the power device.

The following sections of this chapter will discuss the method and case studies in details.

## 7.2 Aging in MOSFETs: Equivalent Impedance Approach

### 7.2.1 Origin of Aging

Aging of a power semiconductor device is generally defined by significantly poor electrical performance due to a change in electrical parameter. In addition, a device can experience mechanical damage due to the environmental or electrical stress which is another way to express the aging of a device. In both of the cases, it is highly likely that at least one of the electrical parameters such as capacitance or ON-resistance will be affected over the course of operation. Due to the manufacturing process and limitations, any MOSFET will have the ON-resistance ($R_{DSON}$) and parasitic capacitances between the terminals. A simplified electrical equivalent circuit can be shown in Figure 38 [205].

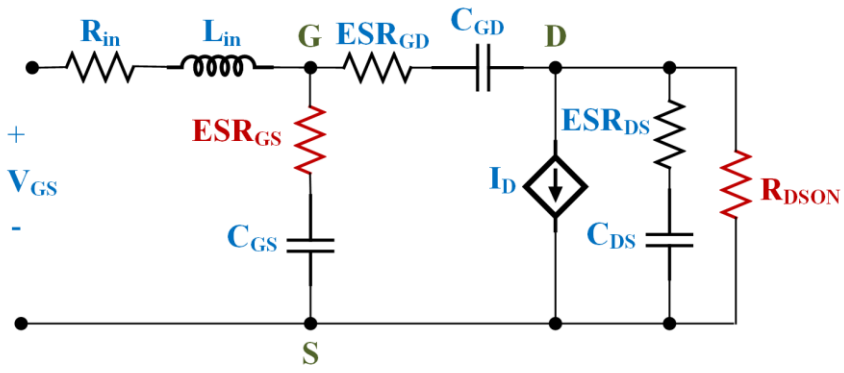



Figure 38: Simplified equivalent circuit of a SiC MOSFET [183]

In field applications, when the device is subjected to any stress, these parasitic capacitances keep decreasing and the $R_{DSON}$ increases. All of these electrical quantities contribute to the degradation of the device i.e., deteriorates the overall performance of the semiconductor switch. Eventually, when these parameters reach to their functioning limit, the device can no longer be operational, and therefore, can be considered as a failure.

### 7.2.2 Gate-Source Impedance: An Aging Precursor

The aging in a power MOSFET can be estimated in terms of gate threshold voltage ($V_t$), gate leakage current ($I_g$), junction temperature ($T_j$), drain current ($I_D$), or ON-resistance ($R_{DSON}$). However, the most widely used precursor parameter to identify or quantify the aging of a MOSFET is the increase in $R_{DSON}$ value [99] - [101]. In addition, the loss in the capacitance value can be used as another precursor according to [101]. Since the equivalent series resistance (ESR) of a capacitor is inversely related to the value of the capacitance, as the capacitor ages, the capacitance will decrease and the ESR will increase [206]. As shown in Figure 38, a MOSFET has three parasitic capacitances which are denoted by $C_{GS}$, $C_{GD}$, and $C_{DS}$ respectively. As the device undergoes degradation, these capacitance values will be different than the healthy device. All of these changes will be reflected in the equivalent

impedance seen between the gate (G) and source (S) terminals ($Z_{GS}$), and the value before and after aging will be different. Hence this change can be used in estimating the overall degradation of the semiconductor device.

Let, the equivalent impedance seen across gate and source terminals of a healthy device is denoted by $Z_{GS\_H}$, and due to degradation, the equivalent impedance is $Z_{GS\_A}$. If the difference in equivalent impedance between a healthy and an aged device is denoted by $\Delta Z_{GS}$, the relationship between these three quantities can be written as:

$$|Z_{GS\_H} - Z_{GS\_A}| = \Delta Z_{GS} \tag{51}$$

Since the SSTDR hardware is sensitive to the impedance variation, even if the changes are minor, this change ($\Delta Z_{GS}$) can be detected by the hardware. If the change in the equivalent impedance is a non-zero value, the SSTDR will produce two distinct data sets for a healthy device and aged device. Thus the SSTDR can be used in estimating the aging of a MOSFET from the gate-source terminals.

### 7.3 Case Study-1: Degradation Detection in a Discrete SiC MOSFET

In this section, the degradation of a SiC MOSFET from the gate-source interface has been studied. The online condition monitoring was achieved by Spread Spectrum Time Domain Reflectometry (SSTDR) for the first time in SiC based devices. An accelerated aging station was built to age the power semiconductor devices in a standardized way, and power cycling test was performed to induce degradation. Finally, the SSTDR data, before and after aging, were compared and plotted in order to identify the degradation from the gate terminal of the device. This proposed method can rely on monitoring only gate-source interface meaning it does not involve any high voltage at the drain.

### 7.3.1 Standardized Accelerated Aging Methodology

An accelerated aging station was built in order to induce the degradation in SiC MOSFET. The aging station, shown in Figure 39, consists of a DC power supply, gate drive circuit, data acquisition system, current sensor, thermocouple, and device under test (DUT i.e. SiC MOSFET). A 1200V, 90A rated SiC power MOSFET, shown in Figure 40, (C2M0025120D, manufactured by CREE Inc.) was selected as the DUT. Power cycling was performed, and a total 4000 cycles were recorded by the data acquisition system until the aging process was completed. During the test, LabJack T-7 Pro data acquisition system (DAQ) was used to measure and record $V_{DS}$, $I_D$ and case temperature ($T_{case}$). The case temperature was measured using a K-type thermocouple from OMEGA, and an Arduino based controller was used to control the entire process. The ON-state resistance for the new MOSFET was measured 29mΩ, and after 4000 aging cycles, it was increased to 34mΩ. This indicates an aging level of about 17%. Both readings were taken at the junction temperature of 25° C. In order to age the DUT faster, it was not attached to any heat sink, and forced air was used to drop the case temperature faster during the turn-OFF period.

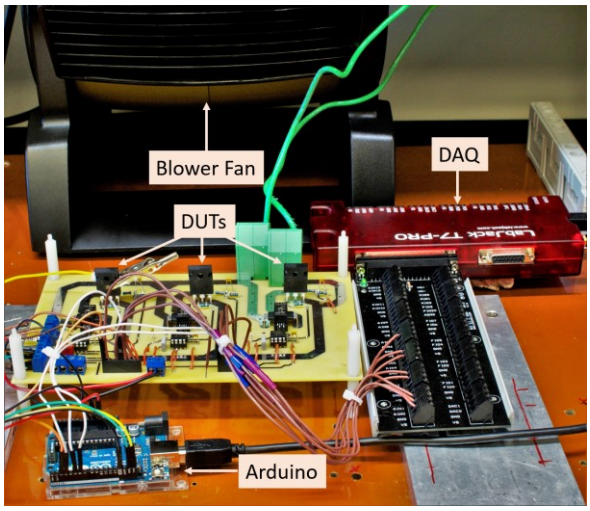
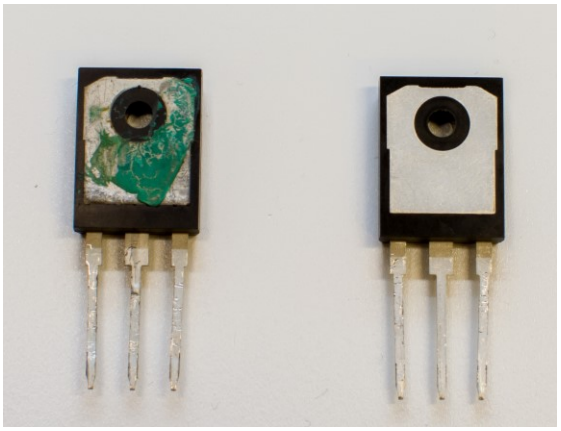



Figure 39: Accelerated Aging Station.



(a) Aged (b) Healthy

Figure 40: SiC power MOSFET (C2M0025120D, manufactured by CREE Inc.)

### 7.3.2 SSTDR Test Setup

SSTDR hardware was connected across the gate and source terminals of the device under test (DUT). The set up for both the healthy and aged MOSFETs were maintained the same for consistency. The set up shown in Figure 41 is drawn in a simplified way as depicted in Figure 42. A constant voltage of 12V was applied across the MOSFET with a 25 Ω resistor

in series to keep the MOSFET in conduction mode. SSTDR data were taken for 4 (four) different frequencies, i.e. 12 MHz, 6 MHz, 3 MHz and 750 kHz.

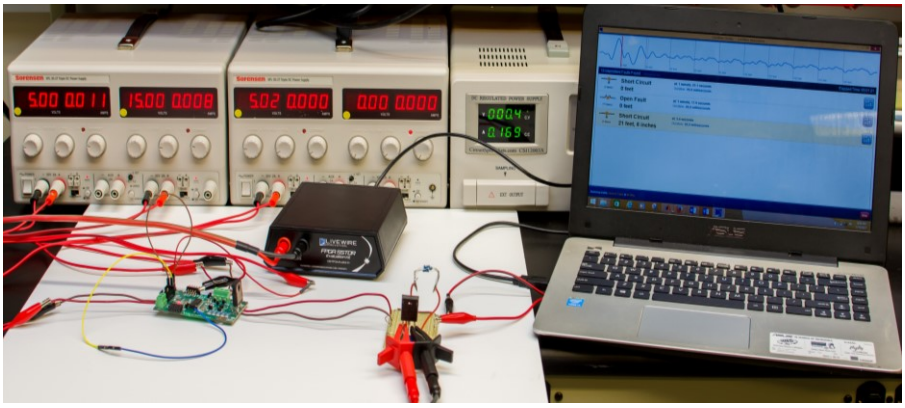


Figure 41: Experimental setup for degradation monitoring of DUT.

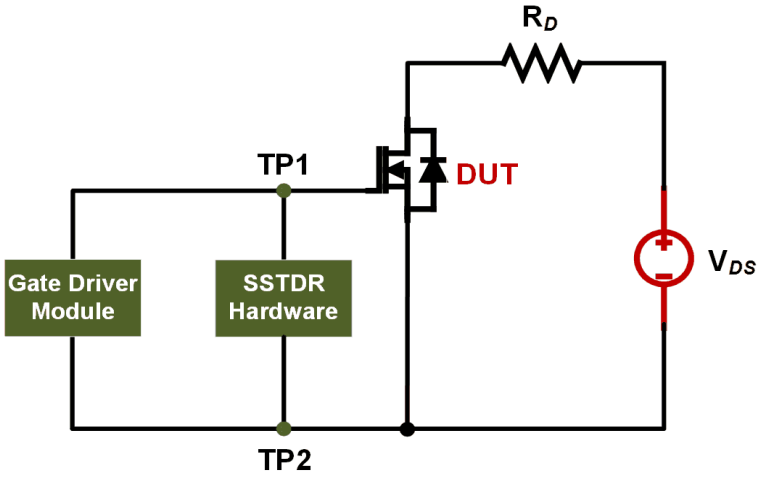



Figure 42: Schematic diagram of the experimental setup for degradation monitoring of SiC MOSFET.

### 7.3.3 Test Results

SSTDR test signals were continuously applied across the gate-source of the DUT and more than 10500 sets of auto-correlated amplitudes were generated for both the healthy and

aged MOSFET for each SSTDR frequencies. All these auto-correlated amplitudes were averaged and plotted in Figure 43 and a portion of the plot was zoomed for better clarity. These plots clearly show that the auto-correlated peak amplitudes for aged device are always less in magnitude than that of the healthy one. This variation was expected because the magnitude of the correlated amplitude is proportional to reflection coefficient (Γ) and any increase in the ESR of the gate-source capacitance and the ON-state resistance for an aged MOSFET will eventually lead to less positive values of them compared to the new MOSFET [207].

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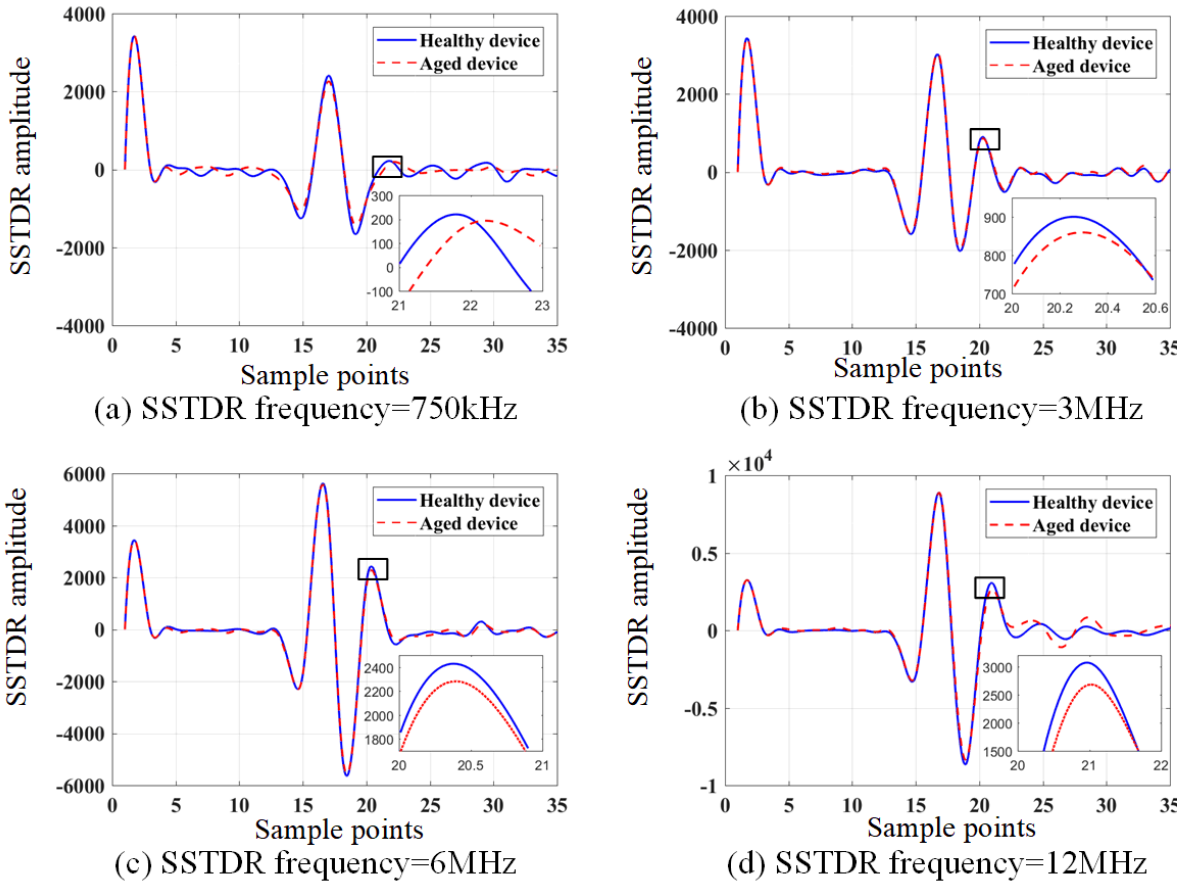


Figure 43: SSTDR auto-correlation plots for new and aged SiC MOSFETs at different SSTDR frequencies recorded from the gate-source terminals.

### 7.4 Case Study-2: Degradation detection in a SiC based buck converter

The widely-used buck converter has been chosen for this study, although the proposed method can be used with any power converter. Over the course of the operation, various components in a buck converter degrade, and their electrical characteristics change. In other words, if a device is physically damaged or the electrical performance of the device is significantly degraded, the device can be considered aged. A degradation associate to any single component is likely to propagate through the entire circuit and would alter the circuit's electrical characteristics. Therefore, it becomes very difficult to determine aging levels when multiple devices age simultaneously. To begin with, one aged device has been considered in the entire converter, and the SSTDR based degradation detection have been studied. Figure 44 shows the schematic of a buck converter, and the SiC MOSFET (M) is the device under test (DUT), which will eventually undergo aging. Since all other components of the buck converter will remain unaffected, the impedance variation of the SiC MOSFET will provide the impression of the overall buck converter's degradation. In most cases, the degradation level in a MOSFET is quantified by measuring the rise in $R_{DSON}$ [99] - [101].

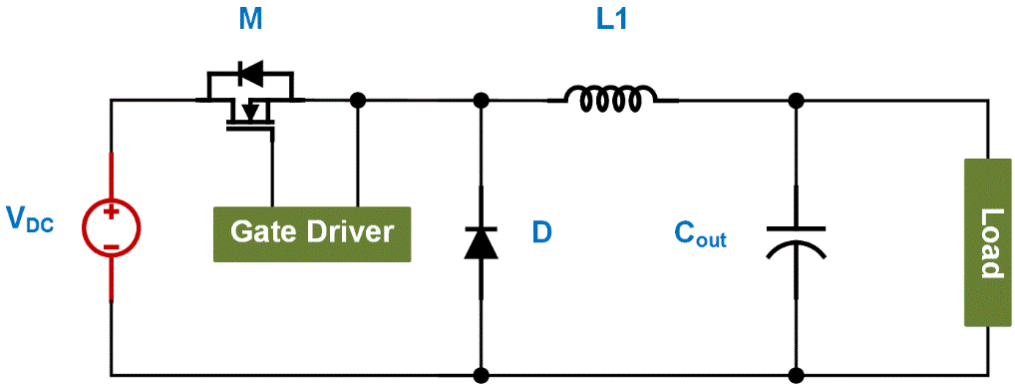


Figure 44: Schematic of a SiC MOSFET based buck converter

### 7.4.1 Aging in Buck Converter

The equivalent impedance of a healthy buck converter can be defined as $Z_{buck\_H}$ when seen across the gate and source terminals of the SiC MOSFET. Due to any degradation, the changes in the parasitic capacitances and in the ON-state resistance of the SiC MOSFET will affect the equivalent impedance of the MOSFET, as well as the equivalent impedance of the buck converter seen across those terminals. Consider, the equivalent impedance of the buck converter due to the aged device is $Z_{buck\_A}$ when seen from the gate-source interface of the MOSFET. Now, if $\Delta Z_{buck}$ is defined as the net impedance change within the buck converter when seen across the gate and source terminal of the MOSFET, then the difference in equivalent impedance between a healthy and an aged converter can be written as:

$$|Z_{buck\_H} - Z_{buck\_A}| = \Delta Z_{buck} \quad (52)$$

This impedance variation can easily be detected by the SSTDR hardware because it is able to identify any impedance mismatch on the SSTDR signal's path of propagation. Now, if the SSTDR data were taken for a healthy and a degraded buck converter, this impedance

mismatch of $\Delta Z_{buck}$, even if the magnitude is minor, can be correlated by the magnitude difference between the two readings. It will distinctly indicate the aging of the buck converter if and only if the magnitude of $\Delta Z_{buck}$ is a non-zero value.

### 7.4.2 Experimental Setup

A buck converter prototype was built, and the SiC MOSFET was selected as the switching device. The device under test was rated for 1200V, 90A, and manufactured by CREE Inc. Before starting any accelerated aging process, SSTDR data was recorded for the healthy converter across the gate and source terminal of the MOSFET, and this data will be considered as the reference for future analysis. The overall experimental process consists of three major steps, namely, SSTDR data collection for the healthy device, power cycling of the DUT, and SSTDR data accumulation for aged DUT within the buck converter.

#### 7.4.2.1 Power Cycling of SiC MOSFET

The DUT was aged by active power cycling method. The case temperature was monitored by using a K-type thermocouple, and the temperature swing was 80°C ($\Delta T$), starting from 100°C ($T_{min}$) and ending at 180°C ($T_{max}$). In order to make sure that the thermocouple was in good contact with the MOSFET case, a highly thermal conductive pad was used to reduce any unwanted air gap between the tip of the thermocouple and the case of the SiC MOSFET. Forced air was provided using a blower fan to cool down the MOSFET during the OFF-state. Once the case temperature reached 100°C, the device was turned ON and air flow was stopped, and these controls were established with the help of an Arduino UNO microcontroller. The time required to increase the case temperature from 100°C to 180°C and bring it back to 100°C was defined as a complete cycle, and a total of 4000 cycles were recorded by the data acquisition system before the device was sufficiently degraded. Using a

DC power supply, a current flow of 24A was supplied to the drain of the device under test. Since the DUT for this experiment had a very low ON-resistance compared to any similarly rated Si MOSFET, it required additional current (to be injected) as well as higher number of cycles to induce any equivalent amount of aging. Figure 45 shows the accelerated power cycling station used in this experiment.

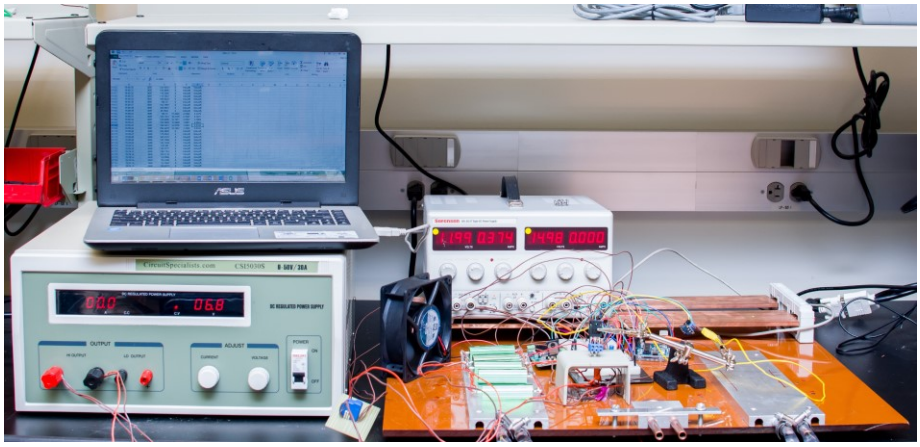

Figure 45: Power cycling station

### 7.4.2.2 SSTDR Test Setup

SSTDR measurement setup parameters were maintained identical for both the healthy and aged buck converter in order to be consistent. Figure 46 depicts the setup for recording the SSTDR readings of a SiC based buck converter, for both healthy and aged devices. The simplified schematic of the SSTDR measurement setup is presented in Figure 47. Readings were taken across the gate and source terminals of the DUT (SiC MOSFET) located inside the buck converter while it was turned ON, i.e., at steady state condition. The SSTDR signal was continuously applied at the frequencies of 3MHz, 6MHz, 12MHz, and 48MHz in order to generate multiple sets of data.

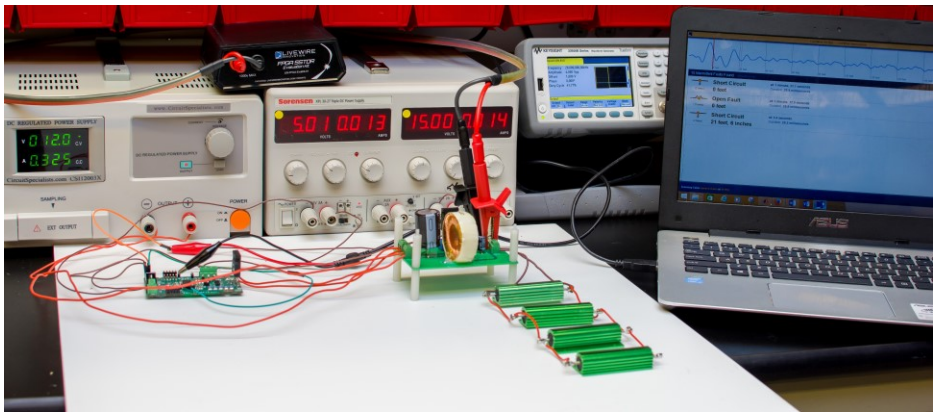

Figure 46: Buck converter setup to apply SSTDR

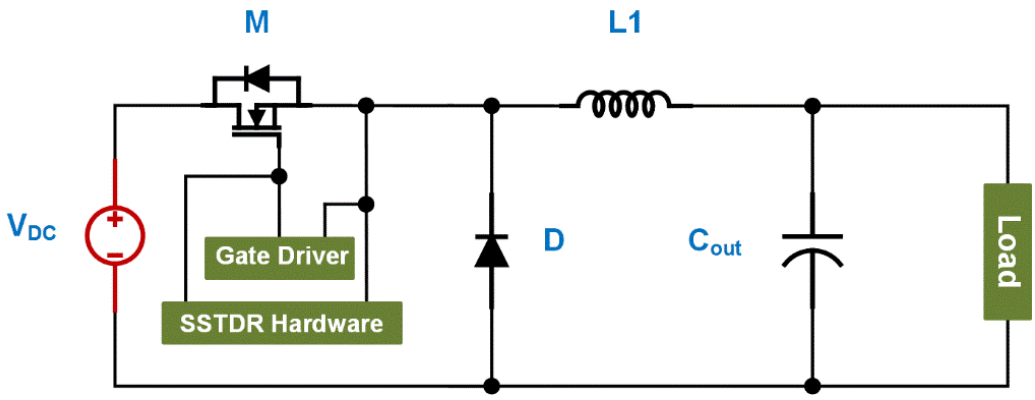


Figure 47: Buck converter setup to apply SSTDR

### 7.4.3 Test Results

Power cycling of the SiC MOSFET was initiated after taking the SSTDR data for the healthy device. At the same time, the $R_{DSON}$ was measured in order to compare the degradation level induced from power cycling. All the readings for both the healthy and aged buck converter were taken at the same room temperature. The aim was to detect aging by the well-known precursor parameter, $R_{DSON}$, and then compare the two SSTDR readings, before and after aging, to identify the aging.

To achieve the above mentioned goal, first $R_{DSON}$ was measured for the healthy device, and it was 27mΩ. After 4000 cycles, $R_{DSON}$ was measured again at room temperature, and the new $R_{DSON}$ was 31 mΩ i.e., the change in $R_{DSON}$ was 4mΩ. This is equivalent to 15% variation compared to the initial value. In the next step, SSTDR data was recorded across the gate and source terminal of the DUT. The SSTDR signal was continuously applied and close to 1700 sets of data were generated for both of the healthy and aged buck converter at each frequency. All of these data were averaged and plotted. These auto-correlated SSTDR amplitudes taken at 3MHz, 6MHz, 12MHz, and 48MHz frequencies are plotted in Figure 48. These plots show that the amplitude at the peak of interest for the aged converter is less in magnitude than the healthy peak (the first peak is due to the artifact of the hardware and the second peak comes from the probe end at the hardware side). This behavior was expected, as both ESR of gate capacitances and $R_{DSON}$ will increase with aging, and together will lead to a lower reflection coefficient, resulting in a lower magnitude of SSTDR amplitude [203]. However, to observer the changes with better lucidity, the peak of interest was zoomed and included within the plots. The non-zero magnitude difference between the healthy and aged amplitudes prove the aging of the buck converter.

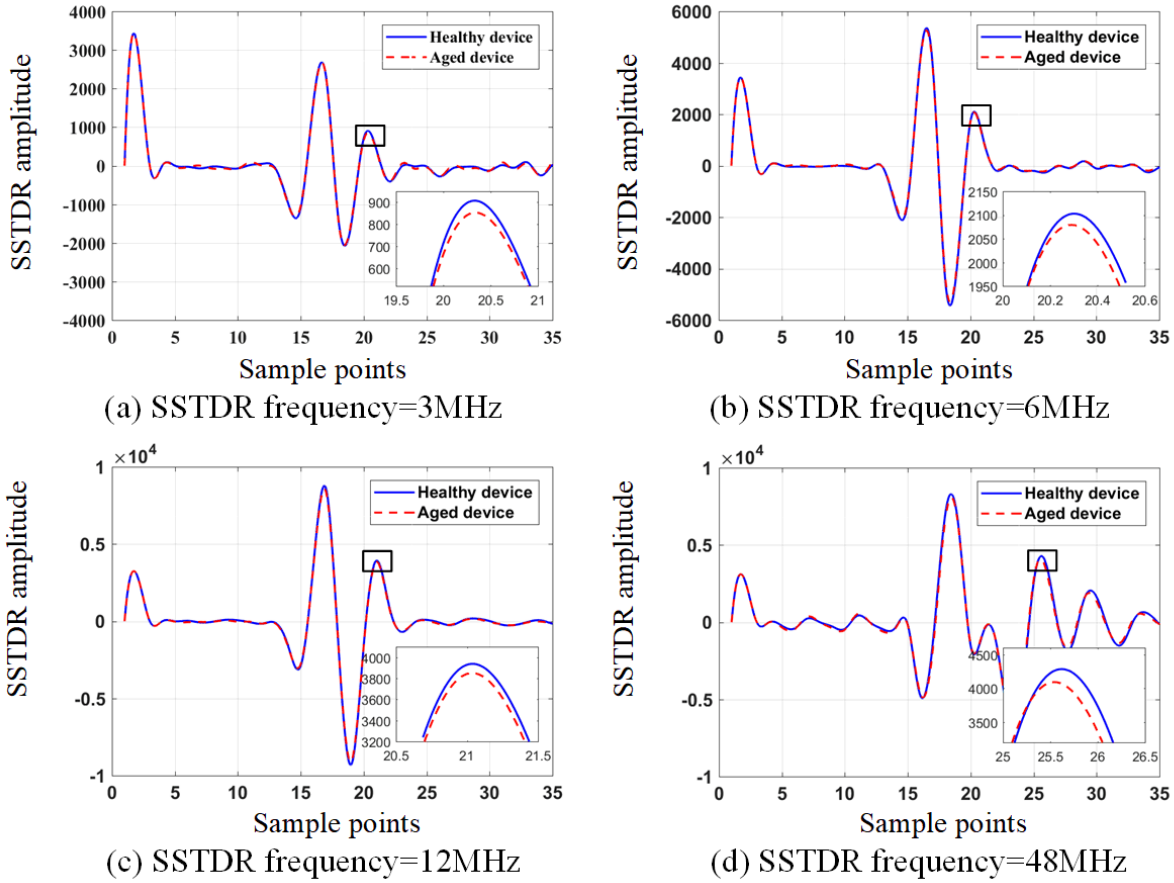


Figure 48: SSTDR auto-correlated amplitude plots for healthy and aged buck converter at different frequencies

## 7.5 Case Study-3: Degradation Detection of Thermally Aged Si and SiC Power MOSFET

In this section, degradation detection of Si and SiC MOSFET based on SSTDR have been studied. The auto-correlated amplitude obtained from SSTDR hardware have been compared with the existing precursor parameter ($R_{DSON}$) as well. A direct correlation between the SSTDR amplitude and $R_{DSON}$ of the MOSFET has been established through this research work. Therefore, this research will allow us to estimate the aging of a power semiconductor device from the measurement of SSDTR amplitudes. In addition, this method can be extended to any converter topology in order to estimate the aging of the semiconductor devices.

### 7.5.1 Experimental Setup

The primary objective of this research work was to detect the degradation induced from passive thermal aging using SSTDR technique. The overall process consists of four steps which can be listed as below:

i. Collection of SSTDR data and $R_{DSON}$ values for healthy devices.
ii. Induce thermal aging in an environment chamber for all of the devices under test (DUTs).
iii. Recording SSTDR and $R_{DSON}$ data for the aged devices.
iv. Compare the data obtained in steps i and iii in order to establish a correlation between the $R_{DSON}$ and SSTDR data sets.

In order to accomplish the above mentioned steps two experimental setup was required namely thermal aging station and SSTDR test setup which are described below:

#### 7.5.1.1 Passive Thermal Aging Station

Two (2) silicon carbide (SiC) MOSFETs and two (2) Si MOSFETs were selected as the DUT to undergo thermal aging. The SiC MOSFETs were rated for 1200V, 90A, and manufactured by Cree. On the other hand, Si MOSFETs were rated for 600V, 50A, and these voltage and current ratings are almost half of the SiC voltage and current MOSFETs. This was intentionally and wisely chosen to compare the relative reliability of SiC and Si MOSFETs. All of these DUTs were aged in a DELTA environment chamber at a temperature of 150°C. $R_{DSON}$ values were measured and recorded while the MOSFETs were in full conduction for every 10hrs of aging at the room temperature. $R_{DSON}$ values were recorded for three different current levels and averaged for each device to avoid the measurement uncertainty. The DELTA environment chamber is shown in Figure 49.


Figure 49: DELTA thermal aging chamber

#### 7.5.1.2 SSTDR Test Setup

SSTDR measurements were taken between the gate and source terminals of the MOSFETs. The devices were in full conduction while recording the data. In addition, the settings in the SSTDR parameters were maintained the same throughout the experiments in order to keep consistency in the data. The actual SSTDR test setup is depicted in Figure 50, and Figure 51 illustrates the simplified schematic of the SSTDR measurement.

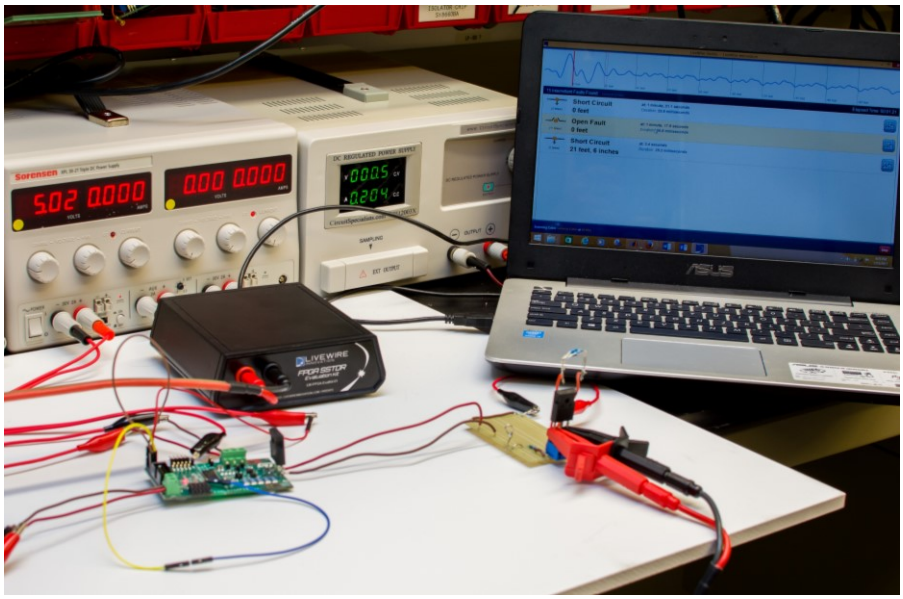

Figure 50: SSTDR test setup

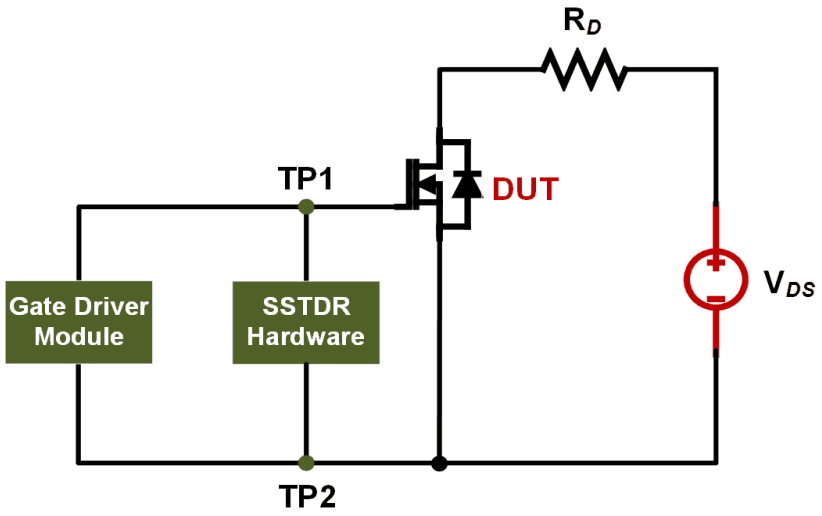


Figure 51. Schematic of the SSTDR experimental setup for degradation monitoring.

### 7.5.2 Test Results

All of the experimental data were recorded at room temperature for each device. In order to maintain the same junction and case temperature of the MOSFETs, the devices were cooled down to the room temperature with a waiting period of 12hrs before taking any measurement. A device was considered to be significantly aged when the change in the $R_{DSON}$ value was twenty percent (20%) of its initial value. And, after about 100hrs of thermal aging all four of the devices showed nearly 20% increase in their preliminary ON-resistance. The average $R_{DSON}$ values recorded every 10hr of aging are plotted and shown in Figure 52 for all of the MOSFETs.

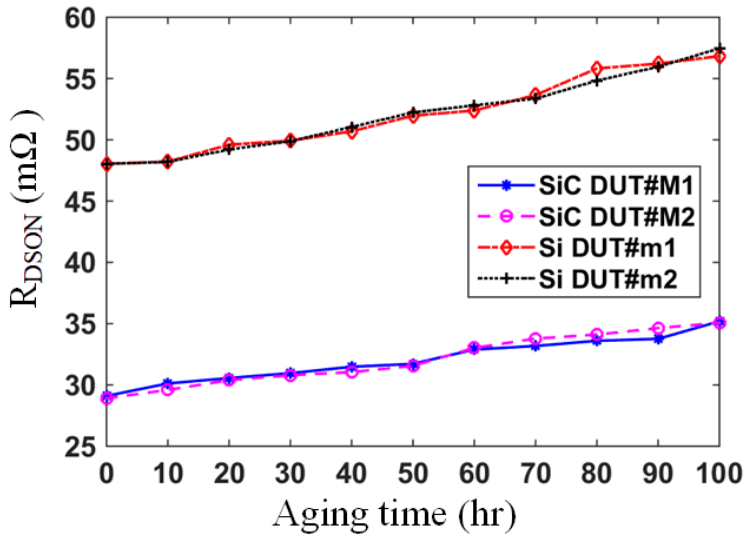


Figure 52: Changes in $R_{DSON}$ over time.

SSTDR test signals were continuously applied across the gate-source of the DUTs while the devices were in full conduction. The SSTDR center frequency was set at 48MHz and more than 3300 sets of auto-correlated amplitudes were generated and averaged for each device in both of the healthy and aged conditions. These auto-correlated data are plotted in Figure 53

for Si MOSFETs, and Figure 54 shows the plots for SiC devices. Peak of interests have been zoomed and included within the respective plots for better visualization of the distinct data points between the healthy and aged devices. The variation in these data for healthy device, 50hr aged DUT, and 100hr aged DUT show a decreasing trend which is consistent with the reflectometry theory as stated in equation (19). The equivalent impedance between the gate-source terminals of the DUT ($Z_{GS}$) can be considered as the $Z_L$ in equation (19). As the device ages, the magnitude of $Z_{GS}$ increases due to the loss in parasitic capacitances and increase in the $R_{DSON}$ value. So, for an aged device the equivalent impedance seen between the gate and source terminals ($Z_{GS\_A}$) is higher than the impedance of a healthy device ($Z_{GS\_H}$). Therefore, the reflection coefficient i.e., SSTDR peak amplitude decreases with increasing impedance seen by the SSTDR hardware.

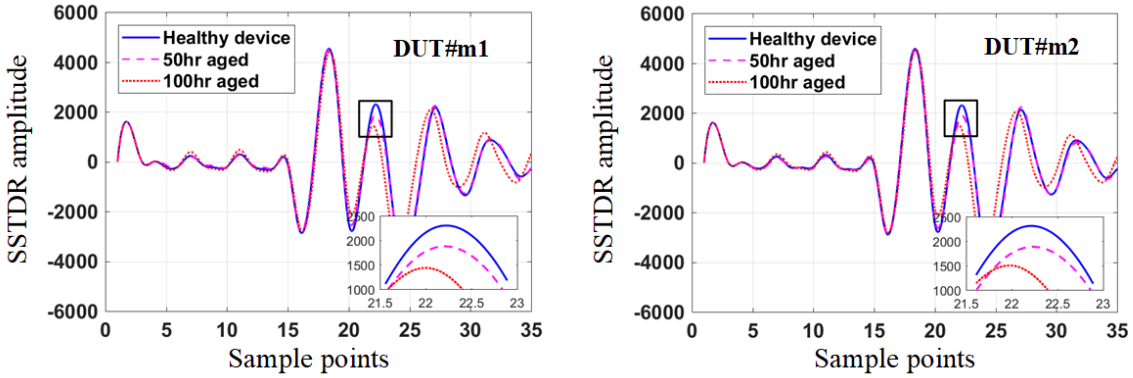


Figure 53: SSTDR auto-correlation plots for new and aged Si MOSFETs at 48MHz SSTDR frequency

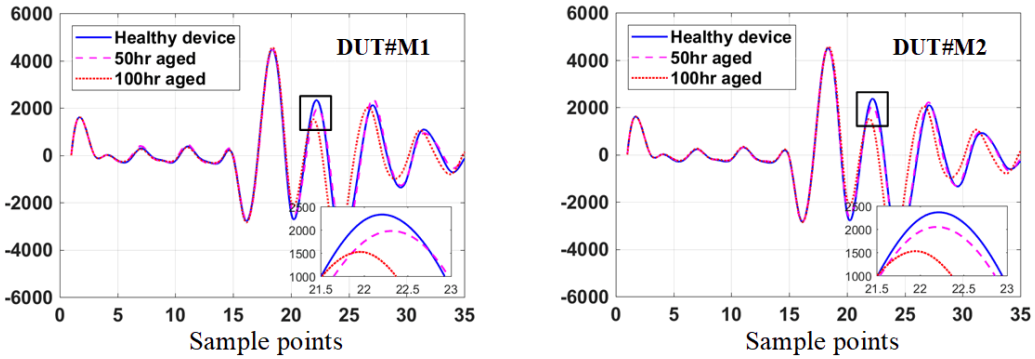


Figure 54: SSTDR auto-correlation plots for new and aged SiC MOSFETs at 48MHz SSTDR frequency

It is important to establish a correlation between the traditional precursor parameter (in this case $R_{DSON}$) and the SSTDR auto-correlated peaks. Table XII shows the changes in the $R_{DSON}$ values and SSTDR peak amplitudes for all of the DUTs after 50hrs and 100hrs of aging. Interestingly, the percent change in SSTDR amplitude after 50hrs and 100hrs of aging are about twice the percent change in the corresponding $R_{DSON}$ values. Hence, it is possible to estimate the failure from the SSTDR amplitude without measuring any electrical parameters. Interestingly, SiC devices show the similar change in their $R_{DSON}$ values although they have the double voltage and current rating compared to the Si MOSFETs. This is because the manufacturing process is not yet as mature as the process of Si technology, and therefore, the SiC MOSFETs are still less reliable than the existing Si devices.

The correlation between the relative changes in $R_{DSON}$ and SSTDR auto-correlated peak amplitude can be better understood from Figure 55. The trend in data for both $R_{DSON}$ and SSTDR peak amplitude shows the linear relationship with the aging of the devices.

Table XII Comparison between $R_{DSON}$ and SSTDR amplitude

| Device | DUT# | $\Delta R_{DSON}$ (%) | | % Change in SSTDR amplitude | |
|---|---|---|---|---|---|
| | | 50hr | 100hr | 50hr | 100hr |
| Si MOSFET | m1 | 8.18 | 18.30 | 18.48 | 37.65 |
| | m2 | 8.72 | 19.61 | 18.21 | 36.02 |
| SiC MOSFET | M1 | 9.02 | 20.93 | 16.80 | 35.55 |
| | M2 | 9.12 | 21.27 | 15.67 | 35.39 |

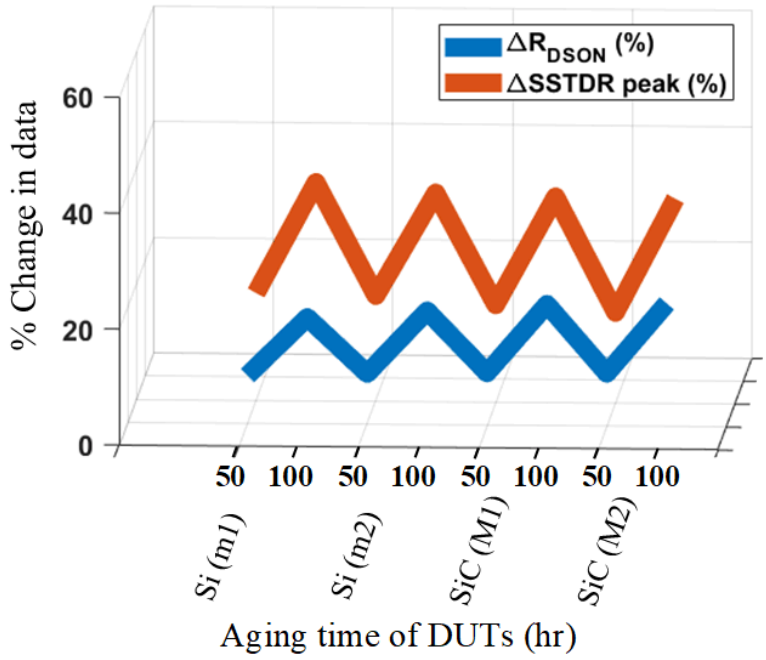


Figure 55: Correlation between $R_{DSON}$ and SSTDR amplitude

## 7.6 Conclusions

For the first time SSTDR based impedance spectroscopy has been applied to SiC MOSFETs to determine the level of aging and degradation. The experimental results

demonstrate that it is possible to estimate the state of health of a SiC MOSFET as well as of a SiC-based buck converter using SSTDR. In addition, this research work establishes a bridge between the most widely used precursor parameter of a MOSFET ($R_{DSON}$) and the emerging SSTDR based aging detection (auto-correlated peaks). According to the experimental data, Si devices are still better switching devices in terms of the thermal reliability. Although, the SiC devices have high power density compared to Si, they still suffer from maturity in manufacturing process to compete with the similar rated Si counterparts.

Unlike previous SSTDR applications, the research outcome can determine aging associated with miniscule changes inside a SiC MOSFET connected to a branched network (buck converter), and the technique can be applied to a live circuit. Another unique feature of this work is that the SSTDR was applied between the gate and source terminal of the SiC power MOSFET when the device was in full conduction. Rather than applying the SSTDR across the drain-source terminal, it has been applied across the gate-source interface for several reasons. First of all, the drain terminal is not always accessible is real converters. In addition, since the drain side is at the higher potential, the possibility of human injury is more. On the other hand, the gate side is limited to 18V for SiC MOSFETs and always accessible for any converter. Since the gate oxide layer in SiC MOSFET is the most vulnerable part, it is a necessity to identify the aging in the oxide layer while the circuit is live. Although these experiments were conducted for a single SiC MOSFET, it is possible to identify the level of aging associated to an individual MOSFET in a 3-phase H-bridge module by applying SSTDR at the gate and source terminals only. On top of that, the proposed method creates a provision to redesign the SSTDR hardware at a significantly lower rating and then the condition monitoring unit can be integrated with the gate driver module which will further reduce the overall cost. Moreover,

unlike traditional condition monitoring methods, the SSTDR based aging detection does not require measuring any electrical parameters which ensures zero measurement error. Thus, this method clearly shows advantages compared to other existing condition monitoring techniques.

# CHAPTER 8

# CONCLUSIONS AND FUTURE RESEARCH

The primary objective of any condition monitoring method is to find the remaining useful life of a power semiconductor device or a power converter. The knowledge of the mean time to failure of a device helps in scheduling the periodic maintenance and ultimately enhance the operational life of that device as well as reduce the overall cost of the system level maintenance. This dissertation presents a comprehensive solution to determine the state of health of a power semiconductor device in a live power converter using online in-situ, non-invasive technique based on spread spectrum time domain reflectometry (SSTDR) and ultrasound resonator.

Unlike traditional degradation detection methods, the proposed SSTDR based aging detection does not require measuring any failure precursor parameters such as voltage or current, and therefore, it eliminates the measurement uncertainties in live power converters. Until today, the SSTDR-based SOH monitoring techniques were only able to detect device degradation from the high voltage terminals (drain or collector side). It is worth to mention that the existing methods are able to detection aging while the converter is in idle state whereas the propose method is able to perform condition monitoring of a device or converter circuit regardless of its operating states (live or off-line) and from the gate-source or gate-emitter interface. Therefore, the SSTDR based method creates a provision to integrate the condition monitoring hardware with the gate drive module. So, the SSTDR based condition monitoring or sate of health estimation method opens a new avenue in the field of reliability and the future work will address the following challenges:

(i) The existing SSTDR hardware is only limited to 48MHz of center frequency. Therefore, a redesign of the SSTDR hardware is necessary so that it is able to send higher frequency signals. This will also increase the resolution of the defect detection.

(ii) Since the proposed method is able to detect device degradation from the gate terminals of both MOSFET and IGBT, it is natural to shift the research direction in developing a comprehensive solution of condition monitoring hardware by integrating the redesigned SSTDR hardware with the gate driver module.

(iii) The proposed method relies on the equivalent impedance of the device of the converter seen from the gate-source terminals, thus it is unable to differentiate the channel and gate-oxide layer degradation. Since gate oxide layer is the most vulnerable part of a SiC MOSFET, it is necessary to extend the research area toward decoupling the channel and gate-oxide degradation by extracting the transmission line model parameters of the SSTDR propagation path.

This manuscript also presents the bond wire related degradation detection of IGBT power modules using ultrasound resonators. The proof-of-concept results have been included in chapter 6 where it has been demonstrated that the proposed ultrasound based non-destructive evaluation is able to identify the bond wire failure (lift-off) related IGBT module failures. This research has established similar future research scopes as stated above since the proposed method is independent of the module's operating condition. However, the preliminary results do not explain the mutual relationship between the resonator frequency and the number of bond wire lift offs. Therefore, the natural direction of future research efforts includes finding the optimum number of resonators, their respective location, and the optimum frequencies of the resonator to identify the location and number of the affected bond wires.

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# VITA

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