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Vf-Constrained $\eta\rho$-Pareto Optimization of Medium Frequency Transformers in ISOP-DAB Converters

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Abstract:
This paper deals with $\eta\rho$ (efficiency-power density) Pareto optimization of medium frequency transformers (MFTs) with considerations of voltage and frequency (Vf) constraints of semiconductors for mega-watt range input-series output-parallel (ISOP) connected dual-active bridges (DABs). A simple design methodology to include the litz wire configuration in the optimization process is proposed. Based on the presented design methodology, the effects of the semiconductors blocking voltage and switching frequency on the $\eta\rho$-Pareto optimization are evaluated. First, an idealized optimization is carried out to understand the general behavior of the optimum point. Second, brute-force optimization is utilized to find the practical optimum solution based on the market availability of MFT components. Designing MFTs for a 1MW 10kV/600V ISOP-DAB converter is the subject of numerical studies. The best trade-off between $\eta\rho - Vf$ is selected as the final optimal solution and its design correctness is validated using 3D finite-element analysis (FEA). Experimental tests on a 3kW downscaled MFT prototype show that the proposed method is valid in practice.

Nomenclature

A	Core yoke width
A_c	Core cross sectional area
A_{Cub}	Copper area of the litz wire bundle
B	Core window height
C	Core window width
$Cost_{MFT}$	Total cost of MFT
$Cost_{Ucore}$	Cost of one U core
B_{mag}	Flux density magnitude
B_{max}	Maximum flux density
D	Core yoke depth
E_V	Insulation material strength
$I_{ac1,rms}$	rms value of i_{ac1}
I_{ma} and I_{mb}	Current values at switching moments
J	Current density in MFT winding conductors
L_{avg}	Windings turn average length
L_{bx} and L_{by}	Litz wire bundle width and hight
L_{iso}	Inter-winding insulation average length
L_σ	MFT stray inductance
N	number of turns in a transformer
N_x	Number of winding layers in x direction
N_y	Number of turns per layer in y direction
V_B	Semiconductor blocking voltage
V_{dc1}	Primary side DC voltage
V_{dc2}	Secondary side DC voltage
V_{MVDC}	Medium voltage level (ISOP-DAB input voltage)
V_{max}	Maximum voltage applied to a transformer
Vol_{Core}	Total volume of core
Vol_{MFT}	Total volume of MFT
R_L	Output DC load equivalent resistance
a_n and b_n	Fourier series coefficients of MFT current
a_t	MFT turn ratio
d_s	Litz wire strand diameter
d_W	Winding width in x direction
f_s	Switching frequency
h_W	Winding height in y direction
i_{ac1}	MFT ac current in primary side
k_{AR}	Aspect ratio
k_{cd}	Copper density (filling factor) of litz wire
k_r	Dowells resistance factor
k_{safe}	Insulation material safety factor
k_{tw}	Twisting factor (=1.25)
k'_{cd}	Litz wire copper density without outer insulation
n_c	Number of paralleled cores to form MFT core
n_{cell}	Number of DAB cells
n_s	Number of litz wire strands
n_{sx} and n_{sy}	Number of litz wire strands in x and y-axis direction
t_{cf}	Coil former thickness
t_{ib}	Insulation tickness
t_{ic}	Inter-core insulation material thickness
t_{iso}	Inter-winding insulation material thickness
t_{ix} and t_{iy}	Inter-layer insulation thickness in x and y-axis direction
u_V	Semiconductor voltage utilization factor
δ	Skin depth
η	Efficiency
ρ	Power density
$\rho_{Cost,Litz}$	Cost density of litz wire
σ	Cost density
σ_{Cu}	Copper conduction
φ	Phase-shift angle
ω	Angular frequency

1 Introduction

Faraday's law of induction describes the phenomenon of electromagnetic induction in transformers, quantitatively. Based on the law, transformer core cross sectional area is proportional to the inverse of frequency, $A_c = v_{max}/(2\pi f N B_{max})$ [1]. This implies that with increase in operating frequency of a transformer, f, the transformer weight and volume can be reduced. Inspiring from this notion,

medium frequency transformers (MFTs) are operated at higher frequencies than that of conventional low frequency transformers to obtain higher power density. MFTs have a wide application in power electronic converters such as in grid-connected photovoltaic systems [2], railway applications [3], offshore DC grids [4], and solid-state transformers (SSTs) [5].

MFTs are the key isolating device for emerging power electronic converters such as SSTs [5]. SSTs are expected to be an ultimate solution for stable operation of future decentralized active distribution grids by controlling grid voltages and currents at the point of interfacing with upstream grid [6]. Design of MFTs for SSTs, in both traction and power distribution applications, demands for specific characteristics such as high power, high voltage and high power density with air cooling systems.

Some specific designs of MFTs have been deployed for SST projects. Universal and Flexible Power Management (UNIFLEX-PM) project [7] was introduced with the focus on distribution applications where 12 MFTs have been used in a 300kVA prototype. The design of UNIFLEX-PM MFTs has been discussed in [8] where metglas magnetic materials are operated in frequency range from 1 to 3kHz. In the Future Renewable Electric Energy Delivery and Management (FREEDM) SST project, a 30kVA coaxial MFT have been designed with Vitroperm 500F material for frequencies higher than 20kHz. Design considerations for a 3MW MFT in offshore wind farm application have presented in [9]. Results show that high frequency behaviour of the MFT is significantly depending on the winding configuration. Three different MFT configurations have been evaluated for 1MW 20kHz 12kV/1.2kV specifications [10]. Shell-type, core-type and matrix-type were compared and U-core transformer with potted insulation selected as the best trade-off between mechanical design complexity and power density. Design of a 166kW 1000/400V 20kHz MFT has been analyzed as a part of Swiss SST project in [5]. Nanocrystalline magnetic materials were chosen. It achieved efficiency of 99.4% and power density of 44 kW/dm^3. It is notable that water cooling system dissipates 0.4% of the overall input power. A 100kW 10kHz 750/750V MFT prototype design procedure has been presented in [11]. The efficiency of the MFT in design stage is observed as 99.7% while it's actual prototype efficiency is measured as 99.3%. The focus of these researches is mainly on the MFT design for specified voltage ratings in the primary side and the effect of increasing voltage in the primary side on the Pareto optimal front behavior is not discussed.

The SST configurations in the mentioned projects are unable to provide MVDC energy port. While, MVDC energy port in SST architecture has many advantages such as low losses integration of renewable resources or direct connection to a MVDC distribution grid [12]. Therefore, suitable SST topology with medium voltage DC (MVDC) to low voltage DC (LVDC) conversion capability is required. One way to achieve this is to employ a galvanically isolated DC-DC converters with input-series output-parallel (ISOP) connection [13] where matured low-voltage semiconductors can be used.

Parameter sensitivity analysis of MFT design in an ISOP connected series resonance converter (SRC) has been performed in [14]. A 500kW 10kV/750V ISOP-SRC was the subject of the design. SRC's main problem is its controllability. SRC controllability is a function of the variation of the switching frequency. Wide switching frequency variation can adversely affect on the switching losses and limit controllability [15]. In contrast to SCRs, dual-active bridge (DAB) converters have high controllability [16] over output voltage and current. Therefore, MFT is designed based on ISOP-DAB limitations in this paper. The MFT design for ISOP-DAB has been performed in [17]. However, only one voltage level has been presented and the effects of voltage and frequency limitations from the converter side is not taken into account.

Prime motivation behind this paper is to evaluate the effect of primary side H-bridge blocking voltage and frequency limits on the optimal $\eta\rho$-Pareto front of high-power MFTs. Moreover, a simple design methodology to include the rectangular litz wire configuration with optimization is proposed. Semiconductors blocking voltage and frequency limitations effects on the $\eta\rho-$Pareto optimal front of the designs are studied for a 1 MW ISOP-DAB as a MVDC to LVDC power converter. Two optimization scenarios based on genetic algorithm (GA) and brute-force are considered for theoretical and practical designs, respectively. Finally, the achieved results are validated through 3D FEA simulations and experimental tests on a 3kW downscaled MFT prototype.

2 MFT Steady-State Analysis

Configuration of an ISOP-DAB converter is shown in Fig. 1 (a) where MFTs are used to isolate DABs' primary and secondary side H-bridges. The number of cascaded DAB modules can be calculated by:

$$n_{cell} = \frac{V_{DC,MV}}{V_{dc1}} \tag{1}$$

where V_{dc1} can be achieved by $V_{dc1} = u_V V_B$. This implies that V_{dc1} must be a percentage of V_B for safe operation of semiconductors. For example, if $u_V = 0.55$ then $V_{dc1} = 0.55 V_B$. Power losses of the MFTs greatly depend on the steady-state quantities of the flux waveform in the core and current waveforms in the primary and secondary windings. MFT's current and flux density waveforms are shown in Fig. 1 (b).

To calculate current average and rms values, analytical formula for current waveforms must be determined. Following equation defines i_{ac1}:

$$i_{ac1}(t) = \begin{cases} \frac{I_{ma}+I_{mb}}{\varphi} t - I_{ma}, & 0 \le t < \varphi \\ \frac{I_{ma}-I_{mb}}{\pi-\varphi}(t-\varphi) + I_{mb}, & \varphi \le t < \pi \\ -\left[\frac{I_{ma}+I_{mb}}{\varphi}(t-\pi) - I_{ma}\right], & \pi \le t < \pi+\varphi \\ -\left[\frac{I_{ma}-I_{mb}}{\pi-\varphi}(t-\varphi-\pi) + I_{mb}\right], & \pi+\varphi \le t < 2\pi \end{cases} \tag{2}$$

Where

$$I_{ma} = \frac{1}{L_\sigma f_s}\left[-\frac{a_t V_{dc2}}{4}\left(1-\frac{2\varphi}{\pi}\right) + \frac{V_{dc1}}{4}\right] \tag{3}$$

$$I_{mb} = \frac{1}{L_\sigma f_s}\left[-\frac{V_{dc1}}{4}\left(1-\frac{2\varphi}{\pi}\right) + \frac{a_t V_{dc2}}{4}\right] \tag{4}$$

$$a_t = \frac{N_1}{N_2} \tag{5}$$

For an adopted phase-shift angle φ, cell output power is:

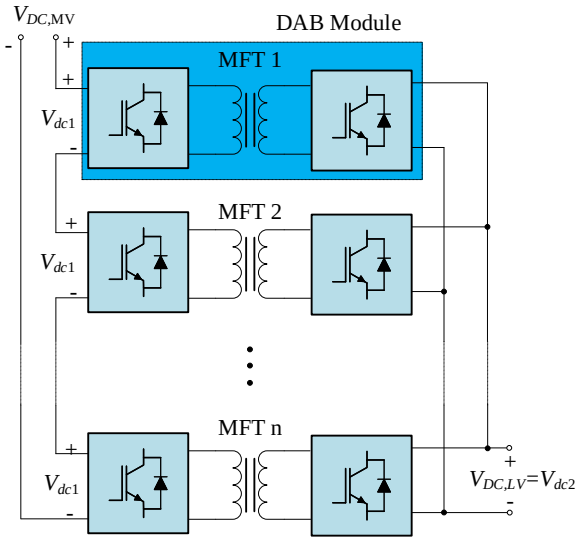
$$P_{cell} = \frac{a_t V_{dc1} V_{dc2}}{2\pi f_s L_\sigma} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right) \approx \frac{V_{dc1}^2}{n_{cell} R_L} \tag{6}$$

It is assumed that load is distributed among DAB cells equally. Hence, φ can be connected to the loading level. For the copper losses, Fourier series of its winding currents are required. Fourier series for i_{ac1} is

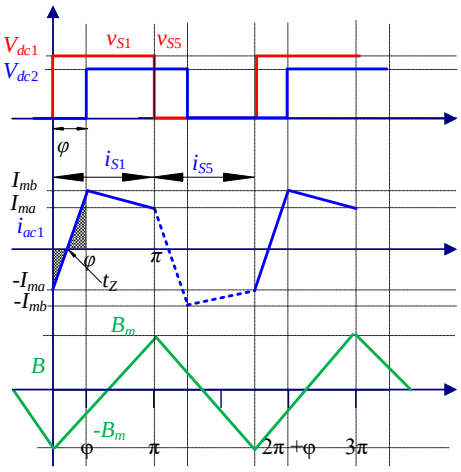
$$i_{ac1}(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega x) + \sum_{n=1}^{\infty} b_n \sin(n\omega x) \tag{7}$$

where $a_0 = 0$ because current does not include DC offset. Also, (a_n) and (b_n) can be calculated as in equations (8) and (9), respectively:

$$a_n = \frac{1}{\pi}\frac{1}{n^2}(1-\cos(n\pi))\left\{\frac{I_{ma}+I_{mb}}{\varphi}(\cos(n\varphi)-1) - \frac{I_{ma}-I_{mb}}{\pi-\varphi}(\cos(n\varphi)+1)\right\} \tag{8}$$



(a) ISOP Configuration



(b) MFT Waveforms

Fig. 1: ISOP-DAB converter as MVDC to LVDC stage of a 1MW SST.

$$b_n = \frac{1}{\pi}\frac{1}{n^2}\left(\frac{I_{ma}+I_{mb}}{\varphi} - \frac{I_{ma}-I_{mb}}{\pi-\varphi}\right) \cdot \sin(n\varphi)\,(1-\cos(n\pi)) \quad (9)$$

In addition, the rms value of the ac current is calculated as:

$$I_{ac1,rms} = \sqrt{\frac{1}{3}(I_{ma}^2 + I_{mb}^2 + I_{ma}I_{mb}) - \frac{2\varphi}{3\pi}(I_{ma}I_{mb})} \quad (10)$$

It is notable that rms current of MFT can be directly calculated from the harmonic components without integration.

3 Rectangular Litz Wire Modeling

Rectangular compact litz wires with a copper density, k_{cd}, in a range from 0.6 to 0.75 is a proper choice for high power MFTs and it can be constructed with different number of stands (n_s) and aspect ratio (k_{AR}) by manufacturers at demand [18]. Fig. 2 shows two possible litz wire strand arrangements in rectangular configuration. These configurations are called litz wire type A and B, in this paper.

3.1 Rectangular Litz Wire Type A

Width and height of litz wire type A, shown in Fig. 2 (a), can be calculated as:

$$L_{bx} = n_{sx}d_s + 2t_{ib}, L_{by} = n_{sy}d_s + 2t_{ib} \quad (11)$$

where t_{ib} is calculated based on the selected insulator material. t_{ib} is calculated for CoolPoly D5108 materials [19] with dielectric strength of 35kV/mm and utilizing a safety factor of $k_{safe} = 0.3$ as:

$$t_{ib} \geq \frac{V_{dc}}{k_{safe}E_V} \approx (1mm \text{ for } V_{dc} = 10kV) \quad (12)$$

Aspect ratio, k_{AR}, is defined as:

$$k_{AR} = \frac{L_{bx}}{L_{by}} = \frac{n_{sx}d_s + 2t_{ib}}{n_{sy}d_s + 2t_{ib}} \quad (13)$$

Also, current density and rms current can be used to compute required litz wire copper area as:

$$A_{CUb} = \frac{I_{rms}}{J} \rightarrow n_s = \frac{A_{CUb}}{\pi\frac{d_s^2}{4}} \quad (14)$$

where J is a free parameter and can be determined from optimization and I_{rms} can be determined from MFT specifications. From Fig. 2 $n_s = n_{sx}n_{sy}$. So, by substituting $n_{sx} = n_s/n_{sy}$ in (13) and rearranging it:

$$k_{AR}d_s n_{sy}^2 + 2(k_{AR}-1)t_{ib}n_{sy} - n_s d_s = 0 \quad (15)$$

which can be considered in the general form of $a_e n_{sy}^2 + b_e n_{sy} + c_e = 0$. The discriminant of this quadratic equation is always positive:

$$\Delta_e = 4((k_{AR}-1)t_{ib})^2 + 4n_s k_{AR} d_s^2 > 0 \quad (16)$$

So, it has two solutions in real number space. Additionally, $a_e c_e < 0$ implies that only one acceptable solution exists as:

$$n_{sy} = \frac{-2(k_{AR}-1)t_{ib} + \sqrt{\Delta_e}}{2k_{AR}d_s} \quad (17)$$

Consequently, all unknown variables can be calculated for litz wire type A. Filling factor or copper density factor can be defined as the ratio of copper area to total rectangular litz wire area as:

$$k_{cd} = \frac{A_{CUb}}{L_{bx}L_{by}} \quad (18)$$

This equation can be rewritten as a function of strand's parameters. Copper density is calculated without considering the outer insulation material thickness as:

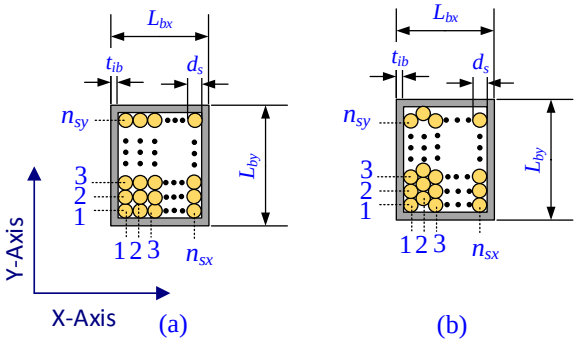


Fig. 2: Rectangular litz wire configurations.

$$k'_{cd} = \frac{n_s \pi d_s^2}{4(L_{bx} - 2t_{ib})(L_{by} - 2t_{ib})} \tag{19}$$

Therefore, $k'_{cd} = \frac{\pi}{4}$ is constant and can be used to calculate k_{cd}:

$$k_{cd} = \frac{A_{CUb}}{\frac{A_{CUb}}{k'_{cd}} + [2n_{sx}d_s + 2n_{sy}d_s + 4t_{ib}]t_{ib}} \tag{20}$$

Now, the design of rectangular litz wire type A is complete.

3.2 Rectangular Litz Wire Type B

The design for litz wire type B, shown in Fig. 2 (b), can be obtained in the same way. However, there are some differences as:

$$L_{bx} = [1 + \frac{\sqrt{3}}{2}(n_{sx} - 1)]d_s + 2t_{ib} \tag{21}$$

$$L_{by} = [n_{sy} + \frac{1}{2})]d_s + 2t_{ib} \tag{22}$$

which results in the following quadratic equation:

$$k_{AR}d_s n_{sy}^2 + [2((k_{AR} - 1)t_{ib}) + (\frac{k_{AR}}{2} + \frac{\sqrt{3}}{2} - 1)d_s]n_{sy} - \frac{\sqrt{3}}{2}n_s d_s = 0 \tag{23}$$

where the discriminant is:

$$\Delta_e = (2((k_{AR} - 1)t_{ib}) + (\frac{k_{AR}}{2} + \frac{\sqrt{3}}{2} - 1)d_s)^2 + 2\sqrt{3}k_{AR}n_s d_s^2 > 0 \tag{24}$$

and final solution is

$$n_{sy} = \frac{-(2((k_{AR} - 1)t_{ib}) + (\frac{k_{AR}}{2} + \frac{\sqrt{3}}{2} - 1)d_s)}{2k_{AR}d_s} + \frac{\sqrt{\Delta_e}}{2k_{AR}d_s} \tag{25}$$

Consequently, copper density factor without outer insulator can be calculated as:

$$k'_{cd} = \frac{n_{sx}n_{sy}\pi d_s^2}{4[1 + \frac{\sqrt{3}}{2}(n_{sx} - 1)][n_{sy} + \frac{1}{2})]d_s^2} \tag{26}$$

For litz wire type B, k'_{cd} is not constant and its minimum value is $\frac{\pi}{4}$ when the litz wire has only one strands. Also, $k'_{cd} \longrightarrow \frac{\pi}{2\sqrt{3}}$ as $n_s \longrightarrow \infty$. Now, k_{cd} can be written in term of k'_{cd} as:

$$k_{cd} = \frac{A_{CUb}}{\frac{A_{CUb}}{k'_{cd}} + [\frac{\sqrt{3}}{2}(n_{sx} - 1) + n_{sy} + \frac{3}{2})]d_s^2 2t_{ib}} \tag{27}$$

For a given set of control parameters $\{d_s, J, I_{rms}, k_{AR}, t_{ib}\}$, geometrical dimensions and number of strands can be calculated, simply. So, this method can be used as a subroutine in a MFT optimization program.

4 MFT Calculations

4.1 Dimensional Calculations

Fig. 3 (a) shows a typical winding arrangement inside a U-core. Also, Fig. 3 (b) shows top and side view of a typical structure of MFT with natural convection. Primary and secondary winding width, hight and average length can be calculated as:

$$d_{W1} = N_{x1}L_{bx1} + (N_{x1} - 1)t_{ix1} \tag{28}$$

$$d_{W2} = N_{x2}L_{bx2} + (N_{x2} - 1)t_{ix2} \tag{29}$$

$$h_W = B - 2t_{cf} \tag{30}$$

$$L_{avg1} = 2n_c D + 2n_c t_{ic} + 4t_{cf} + 4d_{W1} \tag{31}$$

$$L_{iso} = 2n_c D + 2n_c t_{ic} + 4t_{cf} + 4d_{W1} + 4t_{iso} \tag{32}$$

$$L_{avg2} = 2n_c D + 2n_c t_{ic} + 4t_{cf} + 4d_{W1} + 4t_{iso} + 4d_{W2} \tag{33}$$

where subscripts 1 and 2 are used to identify primary and secondary windings. A, B, C, and D, are core dimensions based on Fig. 3. Also, core volume and core cross-section are calculated as:

$$V_C = 2n_c AD(4A + 2B + 2C) \tag{34}$$

$$A_C = 2n_c AD \tag{35}$$

Additionally, t_{iso} is considered as the main control variable for tuning leakage inductance of the MFT. In this paper, leakage inductance is calculated based on the method given in [20].

4.2 Copper Losses

For MFT parameters, the number of turns for primary and secondary side can be calculated as:

$$N_1 = \frac{V_{dc1}}{4f_s B_{mag} A_c}, N_2 = \frac{N_1}{a_t} \tag{36}$$

In addition, number of layers are

$$N_{x1} = \left\lceil \frac{N_1}{N_{y1}} \right\rceil, N_{x2} = \left\lceil \frac{N_2}{N_{y2}} \right\rceil \tag{37}$$

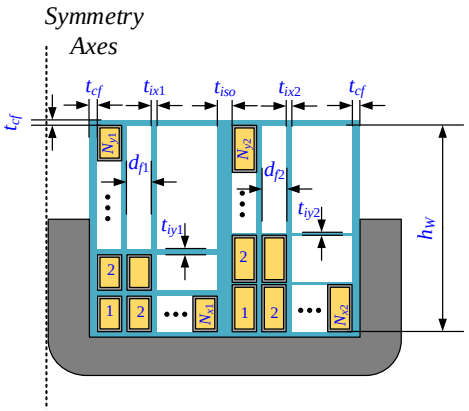
The current waveform, given in (9), flows in MFT primary winding and with a factor of a_t flows in the secondary side. So, it can be used to calculate copper losses as:

$$P_{Cu} = P_{Cu1} + P_{Cu2} \tag{38}$$

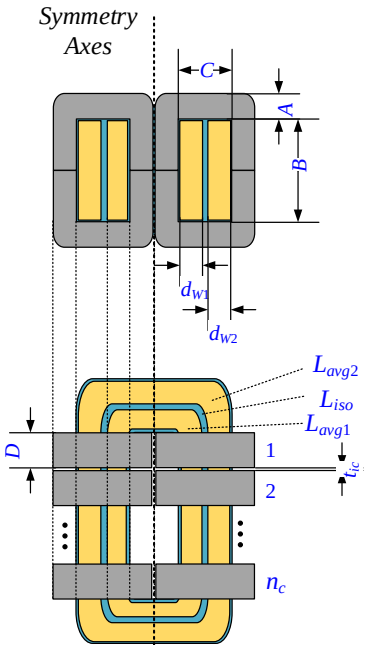
$$P_{Cu1} = \frac{k_{tw}N_1 L_{avg1}}{2\sigma_{Cu}A_{Cub1}} \sum_{n=1}^{N_h} k_{rn}\left(a_n^2 + b_n^2\right) \tag{39}$$

$$P_{Cu2} = \frac{a_t k_{tw}N_2 L_{avg2}}{2\sigma_{Cu}A_{Cub2}} \sum_{n=1}^{N_h} k_{rn}\left(a_n^2 + b_n^2\right) \tag{40}$$

where k_r emulates high frequency effects on the increase of copper resistance [21]. k_r can be approximated with a high degree of precision by given equation (41):



(a) Windings geometry



(b) Side and top view MFT

Fig. 3: MFT geometry based on U cores and its perspective showing the number of stacked cores.

$$k_{rn} = \Delta_n\left(\frac{\sinh(2\Delta_n)+\sin(2\Delta_n)}{\cosh(2\Delta_n)-\cos(2\Delta_n)} + \frac{2\Delta_n\left(N_x^2-1\right)}{3}\frac{\sinh(\Delta_n)-\sin(\Delta_n)}{\cosh(\Delta_n)+\cos(\Delta_n)}\right), \quad (41)$$

where n is harmonic order and $\Delta_n = d_f/(\delta\sqrt{n})$. This formula is valid for foil conductor. It can be adopted for rectangle litz wires by following transformation:

$$d_L = \frac{d_f}{2}\sqrt{\pi n_{sy} N_y d_s \frac{\sqrt{\pi}}{2B}} \rightarrow \Delta_n = \frac{d_L}{\delta\sqrt{n}} \quad (42)$$

4.3 Core Losses

Core losses is a function of used materials and magnetic flux density properties in the core. First approximation of this function is presented by original Steinmetz equations (OSE) in [22] for sinusoidal flux density. Later in [23], OSE formula is extended to non-sinusoidal flux density waveform by improved generalized Steinmetz equation (iGSE) formula. Core losses share in MFT, assuming flux waveform of Fig. 2 (a), can be computed as:

$$P_{V,MFT} = 2^{(\alpha+\beta)} k_i f_s^{\alpha} B_{mag}^{\beta} \quad (43)$$

This gives the specific losses per volume i.e.W/m^3. Also, k_i, α and β are constant parameters. In this paper, $k_i = 1.3368$, $\alpha = 1.25$ and $\beta = 2.35$.

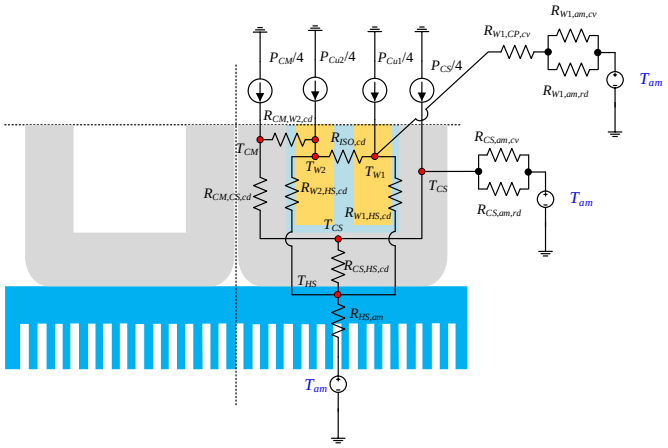


Fig. 4: Conceptualized thermal resistance network of MFT parts.

4.4 Thermal Design

In some MFT designs [2], [24] and [25], a very simple thermal model is used during optimization. The simplified model which is based on the thermal convection from the surface of the MFT to ambient air is proper for small ratings with small dimensions. While, in high-power and medium voltage applications, geometrical dimensions are large and temperature rise cannot be modeled by only surface heat convection. It demands for a detailed thermal network for estimating hot spots inside the MFT.

Fig. 4 shows the conceptualized thermal network considered for MFT. Heat can be dissipated in three ways. First way is by conduction within materials. This is modeled by thermal resistances with subscripts cd in Fig. 4. Second is by convection from the surfaces to ambient air and it is modeled by thermal resistances with a subscript cv and third is by radiation from surfaces and identified by a thermal resistance subscripted by rd. The given model is applicable for steady-state analysis. It can be extended to model transient behavior by adding extra lumped thermal capacity elements analogous to electrical capacitors. Due to symmetry, only one fourth of the MFT needs to be modeled. So, one fourth of the power losses can be used to estimate hot spots of the device. Norton equivalent of the T_{am} (voltage sources) can be employed to solve the circuit.

$$\mathbf{T} = \mathbf{Y}_{th}^{-1} \times \mathbf{I}_{th} \quad (44)$$

The details for computing thermal resistance values are presented in [26].

5 MFT Optimization Procedure

Multi-objective optimization can be applied to two or more incompatible objectives in a single problem. Four category of algorithms can be picked up to solve the problem. Brute-force or simple search is a proper choice when parameters are swept in a restricted search

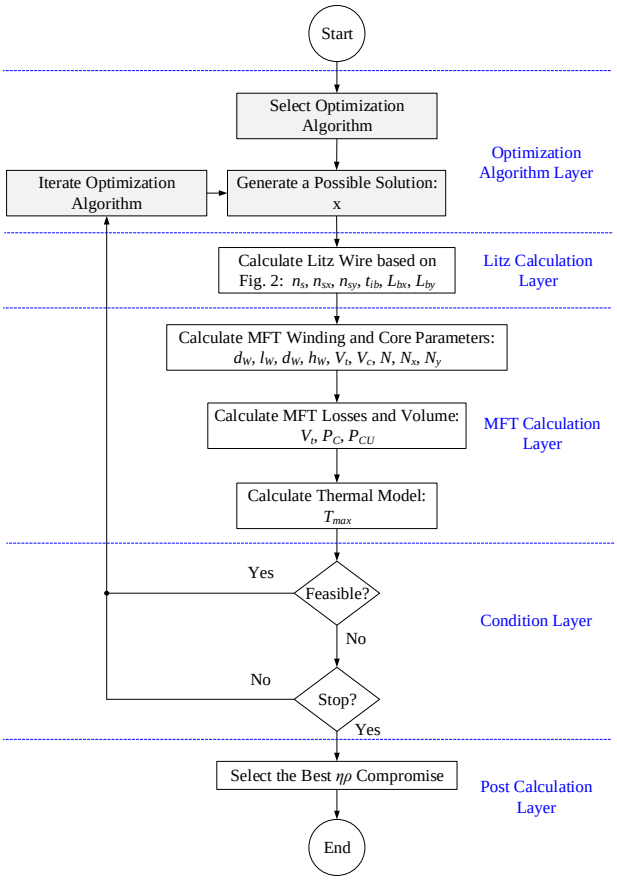


Fig. 5: Flowchart of the MFT optimization procedure.

space. Gradient based algorithms are the best suited for continuous differentiable problems with a continuous search space where hessian matrix is positive or semi-positive definite. These types of algorithm are not proper in the case of discontinuous objectives and search spaces. Heuristic algorithms, such as simplex method [27], are proper for discontinuous and non-differentiable problems. This family performs local search and it is more robust than gradient based methods. Finally, meta-heuristic algorithms are capable of reaching global optimum point without sticking at local minimums in discontinuous non-differentiable objectives with multiple singularities. GA is one the most famous meta-heuristic algorithms and it has been used in many applications successfully [28]. However, there are many meta-heuristics inspiring from the nature and physical laws [29].

In this paper, following three objective functions are considered:

$$f_1 = P_{Cu} + P_{V,MFT} \times Vol_{Core} \tag{45}$$

$$f_2 = Vol_{MFT} = (4A + 2C + t_{ic}) \times (2A + B) \times (n_c D + (n_c - 1)t_{ic} + 2t_{cf} + d_{W1} + t_{iso} + d_{W2}) \tag{46}$$

$$f_3 = Cost_{MFT} = 4n_c Cost_{Ucore} + (N_1 L_{avg,1} A_{CUb1} + N_2 L_{avg,2} A_{CUb2}) \rho_{Cost,Litz} \tag{47}$$

Where f_1, f_2 and f_3 are the total losses, total volume and total cost of the MFT, respectively. Every successful design must satisfy the geometrical and thermal constraints:

$$C - \left(d_{W1} + d_{W2} + t_{iso} + 2 \cdot t_{cf}\right) \geq 0 \tag{48}$$

$$T_{\max} - \max\{\mathbf{T}\} \geq 0 \tag{49}$$

$$L_\sigma - L_{\sigma,min} \geq 0 \tag{50}$$

$$t_{ins} - \frac{V_{ins}}{k_{safe} E_V} \geq 0 \tag{51}$$

Now, the designs can be evaluated for arbitrary solutions such as $x = [A, B, C, D, J_1, J_2, k_{AR1}, k_{AR2}, N_{x1}, N_{x2}]$. Flowchart of the MFT optimization procedure is shown in Fig. 5. Due to the discontinuous nature of control parameters and consequently non-differentiable objective functions, meta-heuristics and brute-force optimization are selected and utilized in the rest of this paper.

6 Optimization Results

The design methodology is applied to find the optimal MFT solution in a 1MW ISOP-DAB converter in the next subsections.

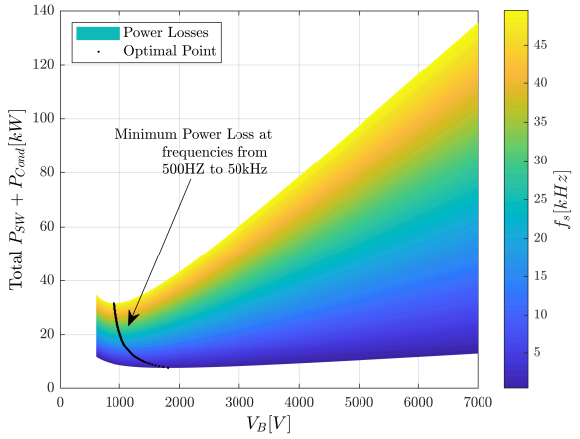
6.1 V_B and f_s Operating Constraints

Calculation of IGBT power losses as a function of V_B is carried out based on the presented work in [13] for ISOP-DAB converter. For sweeping switching frequency from 500Hz up to 50kHZ, semiconductor losses are given in Fig. 6 (a). It is assumed that ZVS condition is satisfied. Optimum V_B is obtained for every frequency and shown by a black solid line in Fig. 6 (a). It is observed that optimum blocking voltage varies from 1800 to 900V as frequency increases from 0.5 to 50kHz. In IGBT switches, switching losses are proportional to V_B^3 and f_s [30]. So, optimum value of V_B decreases versus increase in f_s, inversely.

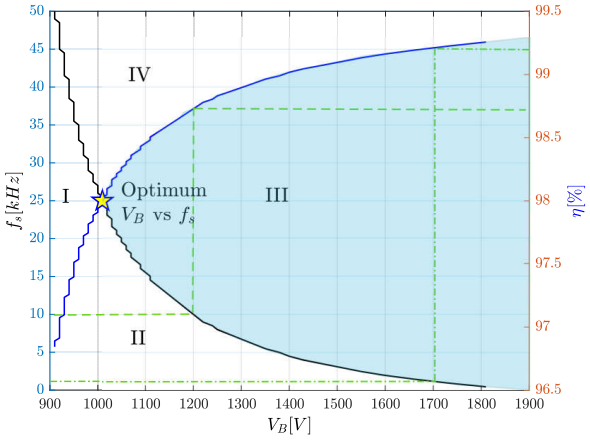
There are some positive consequences of increasing switching frequency such as small volume of MFT and filter size. However, increase of power losses and heatsink volume adversely restricts f_s [31]. Hence, a trade-off for selecting frequency must be taken into account. In [5], optimal switching frequency has been approximated as $f_{opt} = \sqrt{\frac{1}{a}(\frac{\beta}{\alpha} - 1)}$ where a includes the effect of windings AC resistance. However, the given inference is valid for a design where variation of frequency does not result in flux saturation due to limitation in the number of turns. Hence, its difficult to find the optimum frequency for a given transformer geometry where core dimension and number of turns are predetermined for the design frequency. For a given number of turns, maximum increase in the frequency is limited by flux saturation and frequency can be varied for smaller values than the design frequency.

Generally, if IGBTs' voltage is low, then the number of cells and switching frequency are high. Low voltage rating causes low dv/dt stress on the MFT windings and high frequency causes less number ferrite cores. On the other side, the number of strands and AWG (American Wire Gauge) of stands are increased to compensate the high frequency copper losses in the windings. Fig. 6 (c) illustrates the introduced trade-offs by the blocking voltage of semiconductor in the HV side of ISOP-DAB converter.

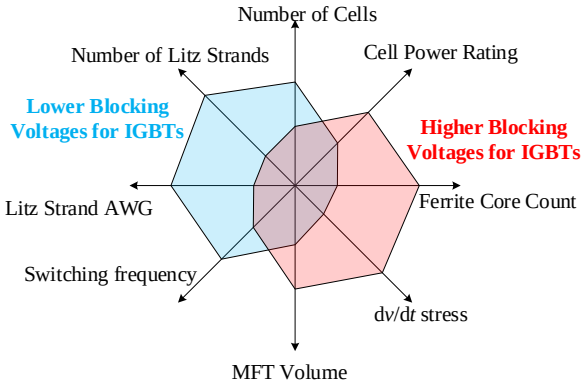
In DAB converters, switching frequency is equal to the operating frequency of MFT. Hence, this frequency can be determined based on the selected optimum V_B-f_s trade-off in Fig. 6 (a). Fig. 6 (b) shows the frequency and semiconductors efficiency versus optimal blocking voltage. Threshold efficiency of 98% is reached at optimum $V_B = 1010V$ and $f_s = 25kHz$. In practice, the nearest standard blocking voltage which is commercially available is 1200 V. Corresponding switching frequency and semiconductor efficiency are 10kHz and 98.74%. The next commercially available blocking voltage is 1700V and its optimum frequency and efficiency are 1.2kHz and 99.21%, respectively. Any switching frequency higher than 1.2 kHz is not optimal for operation of a DAB converter constructed with 1700V IGBTs. While, increase in the switching frequency is required for the reduction in volume. Optimum frequency of a DAB



(a) Semiconductor Losses vs V_B and f_s



(b) Frequency vs blocking voltage and efficiency



(c) Illustration of the trade-off introduced by the voltage rating of semiconductors in the HV side of ISOP-DAB converter.

Fig. 6: Deriving optimum V_B and f_s based on the semiconductor losses characteristics.

operating with 1700V IGBT is pretty lower than the frequency of a DAB with 1200V IGBTs. Therefore, 1200V IGBTs are preferred to reduce the volume effectively.

Region III, determined in Fig. 6 (b), is the optimum solution space and any blocking voltage can be adopted in this region in theory. In practice, there are only two options. In this paper, 1200V IGBTs are considered as a trade-off between efficiency and switching frequency.

6.2 *Multi-objective GA Optimization*

In this subsection the effect of V_B and f_s on the optimum design behavior of MFT is presented. Considered objective functions are f_1 and f_2. To this aim, multi-objective GA optimization is applied to the problem of MFT design. Two scenarios are considered. In the first scenario, the operating frequency is considered 10kHz and in the second f_s swept from 1 to 25kHz as discussed in previous subsection. In all studies, population and maximum number of iterations are 400 and 500, respectively.

In GA optimizations, all control variables are considered as continuous variables in the real number space. Their upper and lower bounds are adopted based on the selected materials in the market which are discussed in the next subsection. Fig. 7 (a) shows $\eta\rho-$Pareto front obtained by multi-objective GA for blocking voltages 600, 1200, 1700, 3300, 4500, and 6500V. From this figure, the effect of increasing the input voltage, i.e. blocking voltage of primary H-bridge, results in higher efficiency and higher power density for the same frequency. In theory, it can be concluded that for $V_B = 6500V$ maximum η and ρ can be achieved.

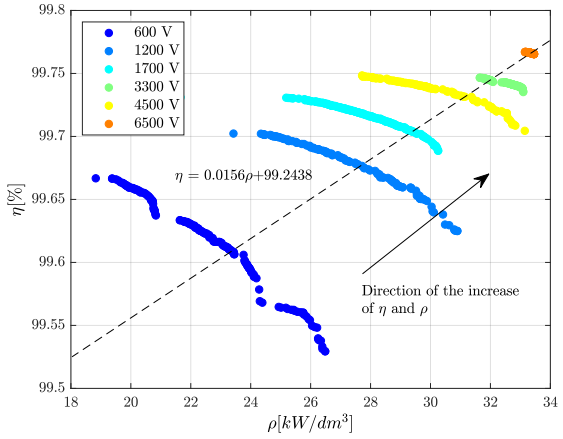
Fig. 7 (b) shows $\eta\rho-$Pareto fronts of MFT designs where frequency is varied from 1 to 25kHz and $V_B = 1200V$. As it can be observed from Fig. 7 (b), the maximum efficiency belongs to frequencies around 10kHz. But, maximum efficiency is not significantly violated by increasing frequency and it is around 99.7%. Also, maximum power density belongs to frequencies around 25kHz. Therefore, selected switching frequency for $V_B = 1200V$ is highly recommended in theory.

6.3 *Discrete Brute-force Optimization*

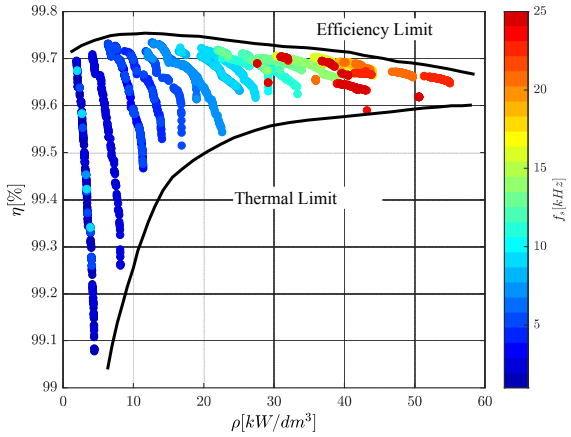
To achieve feasible solutions, parameter sweep over the defined optimization parameters is performed. Considered objective functions are f_1 and f_2. Current density in the primary and secondary windings is limited to the interval 0.5 to 5 A/mm^2. Number of 17 AWG sizes are selected for designing litz wires as in [32]. Therefore, the number of strands can be calculated as a function of current density, aspect ratio, and the strand AWG size. To keep the generated solutions manageable with a personal computer, current density is split in 6 steps with $0.5A/mm^2$ distances. Also, for aspect ratio 10 steps in the range 0.1 to 0.6 is generated. Same AWG size, current density and aspect ratios are considered for both primary and secondary side litz wires to simplify the design.

Thermally conductive insulation materials, CoolPoly D5108 of Celanese Corporation [19], are adopted as insulating material of inter-winding and inter-layer distances. These materials are electrically insulative and thermally conductive. CoolPoly D5108 thermal conductivity is $10W/m.K$ and dielectric strength is $35kV/mm$. In the case of core material, 8 N87 U-shaped ferrite cores from Epocs AG [33] are considered. Peak of flux density, B_{mag}, is considered constant 0.22T. Maximum number of layers set to 4.

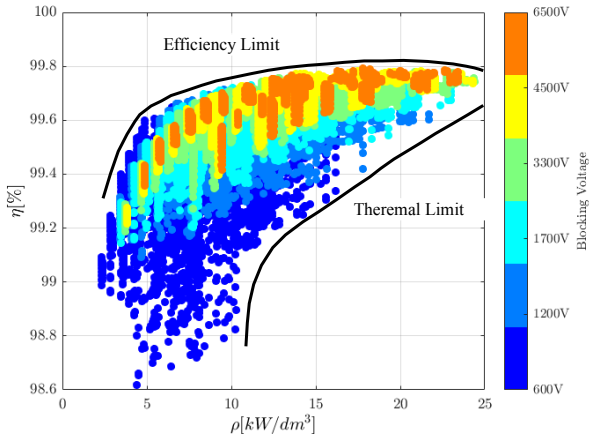
These assumptions results in $8 \times 17 \times 10 \times 6 \times 4 = 32640$ possible solutions for every design. For considered blocking voltages at frequency of 10kHz, acceptable solutions are depicted in Fig. 7 (c). The obtained results verify the correctness of the given inferences in the previous subsection. It can be seen that there is a small difference between the brute-force and GA Pareto fronts. The limited number of the selected parts is the preliminary reason. Another reasons such as thermal constraints reduce the number of acceptable solutions. As it can be seen the number of acceptable solutions for 6500V is much lower than 600V. Moreover, Fig. 7 (d) shows optimization results for frequencies from 1 to 25kHz and $V_B = 1200V$. It can be seen that the maximum realized power density is half of the achieved value by GA theoretical results. In general, brute-fore optimization results imply the correctness of the theoretical results.



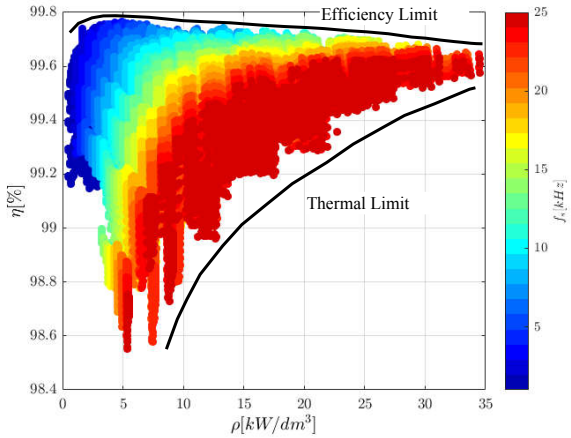
(a) GA with $f_s = 10kHz$ and V_B from 600 to 6500V



(b) GA with $V_B = 1200V$ and f_s from 1 to 25kHz



(c) Brute-force with $f_s = 10kHz$ and V_B from 600 to 6500V



(d) Brute-force with $V_B = 1200V$ and f_s from 1 to 25kHz

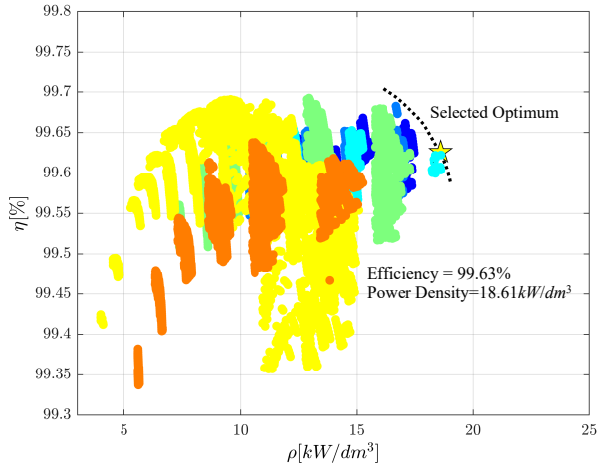
Fig. 7: Efficiency and power density Pareto optimal solutions for blocking voltages from 600 to 6500V for different frequencies.

Table 1 Selected Optimal solutions from Brute-force optimization for $V_B = 1200V$ and $f_s = 10kHz$

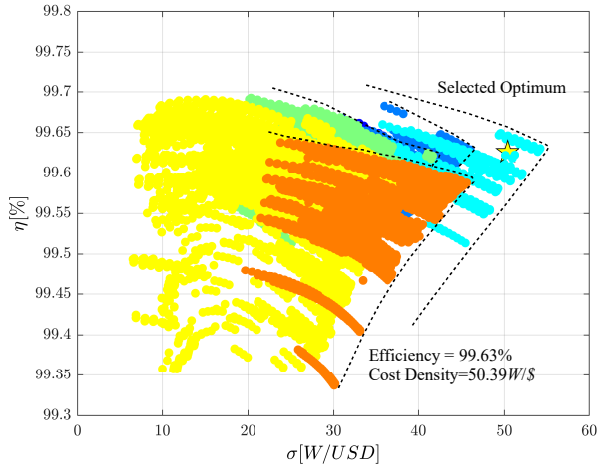
	Parameter [unit]	Litz wire type A	Litz wire type B
Specifications	$P_{cell}[kW]/n_{cell}$	67/15	67/15
	V_{dc1}/V_{dc2} $[V]$	660/600	660/600
	$I_{rms1}/I_{rms2}[A]$	102/111	102/111
Litz wire Parameters	n_{sx1}/n_{sx2}	208/230	240/83
	n_{sy1}/n_{sy2}	79/80	78/254
	$J_1/J_2[A/mm^2]$	490/490	430/430
	k_{AR1}/k_{AR2}	2/4	2/0.4
	$L_{bx1}/L_{bx2}[mm]$	10.3/11.2	10.3/4.9
MFT Parameters	N_1/N_2	15/14	15/14
	N_{x1}/N_{x2}	1/1	1/2
	N_{y1}/N_{y2}	15/15	15/7
	$L_{avg1}/L_{avg2}[mm]$	360.2/ 498.4	360.1/494.9
	$h_W/t_{iso}[mm]$	92/6.5	92/6.3
	$n_c\times$ Core Type	$3\times$ (U 93×76×30)	$3\times$ (U 93×76×30)
General Results	$Pcore/P_{CU}[W]$	91.75/157.65	91.75/140.58
	$\eta[\%]/\rho[kW/dm^3]/\sigma[W/\$]$	99.63/18.61/50.39	99.65/18.71/45.69
	Cost [$]	1323	1459

6.4 Optimal Solution of the MFT

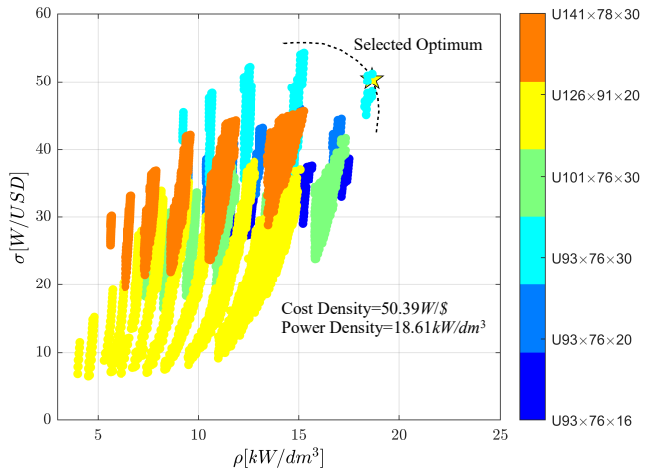
In previous subsections, 1200V is selected as the optimum value of the semiconductor's blocking voltage in ISOP-DAB converter. Consequently, optimal number of ISOP-DAB cells is 15 which results in number of 15 identical DAB converters. The power rating of each DAB is 67kW and frequency is 10kHz. Final optimization can be carried out based on the specified parameters of each MFT.



(a) $\eta - \rho$ Pareto front

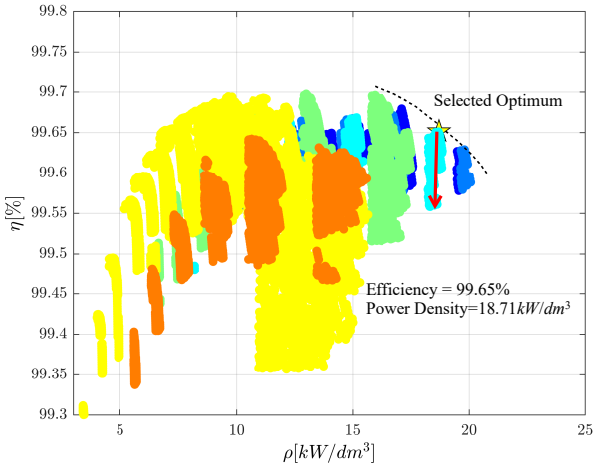


(b) $\eta - \sigma$ Pareto front

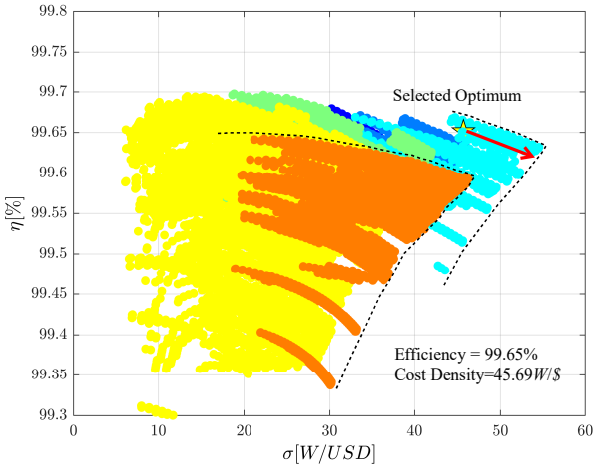


(c) $\rho - \sigma$ Pareto front

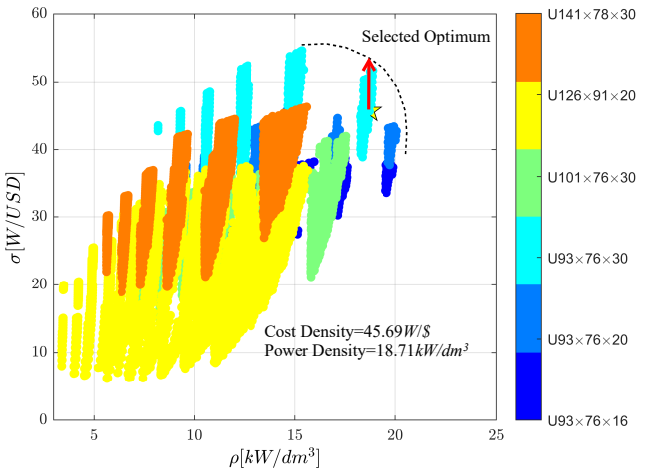
Fig. 8: $\eta - \rho - \sigma$ Pareto optimal solutions for litz wire type A at $V_B = 1200V$ and $fs = 10kHz$.



(a) $\eta - \rho$ Pareto front



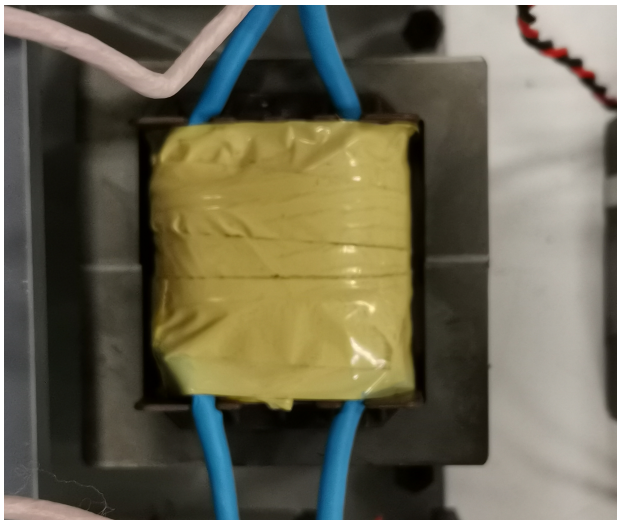
(b) $\eta - \sigma$ Pareto front



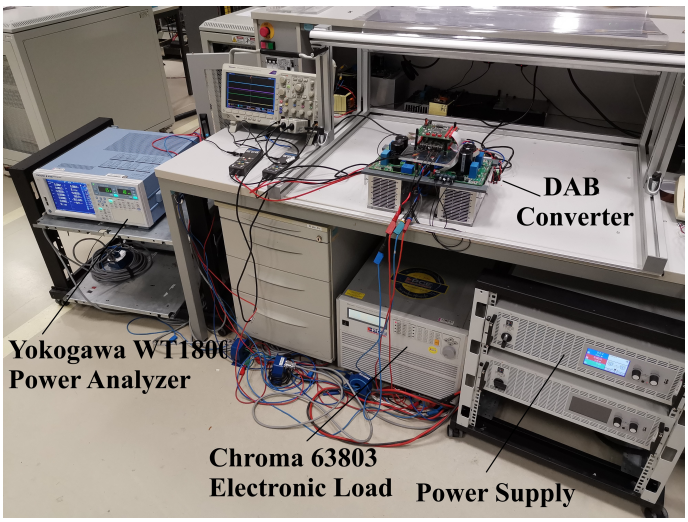
(c) $\rho - \sigma$ Pareto front

Fig. 9: $\eta - \rho - \sigma$ Pareto optimal solutions for litz wire type B at $V_B = 1200V$ and $fs = 10kHz$.

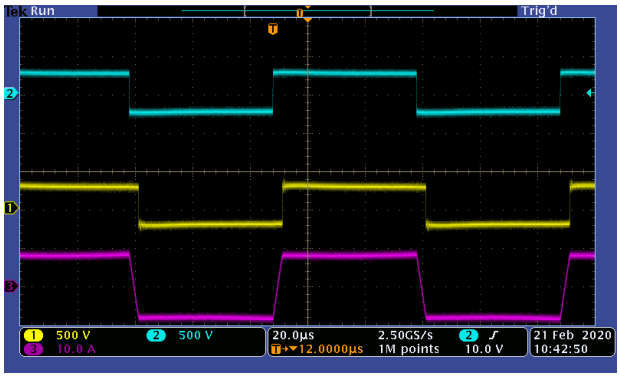
Cost (f_3) is also considered. The litz wire cost density is calculated as $\rho_{Cost,AWG46} = 3.7711USD/mm^2$ per unit length. This cost density is extracted from the price of 300ft length litz wire AWG46×300 (300 strands) from eBay website. In addition, core



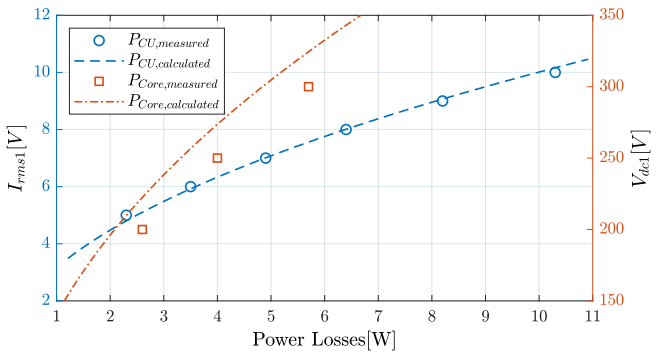
(a) MFT prototype



(b) Experimental DAB setup



(c) Voltage and current waveforms at nominal power



(d) Comparing the calculated vs measured results

Fig. 10: 3kW MFT prototype results.

prices are extracted from Digi-Key Electronics website. Brute-force optimization is carried out for litz wire type A and B. Only litz wire AWG46 is considered to increase the preciseness of the estimated cost. Aspect ratio is swept from 0.1 to 10 in 19 steps. The best designs for litz wires type A and B are selected based on the $\eta - \rho - \sigma$ compromise. Main control parameters and design objective for both litz wires types are given in Table 1. Moreover, the derived results for litz wire type A and B are shown in Fig. 8 and Fig. 9 in the same order. In these figures, the selected solution is shown by a golden star.

From the achieved results, best efficiency and power density for litz wire type A are 99.63% and $18.61kW/dm^3$, respectively. Its cost density and a single MFT price are 50.39 W/$ and 1323 USD, respectively. Therefore, total price of 15 MFTs is 19845 USD. The number of both primary and secondary turns are 15 and 14, respectively. Maximum temperature rise is 76.17°C which is far away from considered maximum temperature, i.e.100°C. The results for litz wires type A snd B are similar. So, the results of type B are not discussed.

6.5 FEA Verification

In this paper, Ansys Maxwell 3D FEA tools are utilized to verify the selected design. The calculated theoretical core losses is 91.75W and resultant core losses of 3D FEA is 86.73W. The error between analytical method and FEA is 5.79%. The difference is coming from the simplifications made (such as uniform flux density distribution) in the analytical calculation methods while the distribution of the flux in 3D FEA model is not uniform specially at core corners. Litz wire losses are directly calculated based on Ansys Maxwell capabilities and compared versus analytical results. Total copper losses are 157.65W and 146.20W for analytical method and FEA, respectively. The error of copper losses calculation is 7.26%. The error of total losses calculation from analytical method versus FEA is 6.61%. It can be concluded that the achieved solutions from the analytical method are valid.

7 Experimental Validation

A 3kW downscaled MFT prototype is build at the chair of power electronics, Christian-Albrecht University of Kiel, Germany, to validated the correctness of the given analytical calculations. The nominal current of the prototype is 10A and nominal voltage is 300V. The number of turns in the primary and secondary windings of the MFT are $N_1 = 26$ and $N_2 = 22$, respectively. Windings are arranged in three layers in both primary and secondary sides. In this prototype, round litz wire (Rupalit V155) with 90 strands, each 0.2mm diameter, are used. Two E-cores (E65/32/27, N87, TDK) are used in parallel. Total four E-cores are used in the MFT prototype construction. Fig. 10 (a) shows the built MFT prototype. Overall setup for measurements of the MFT electrical parameters are illustrated in Fig. 10 (b) where measurement devices, power supply, electronic load and the DAB converter are discriminated. Moreover, square voltage waveforms of the MFT primary and secondary sides are shown in Fig. 10 (c) as well trapezoidal current waveform in the MFT primary side. These waveforms are recorded at nominal load of the MFT prototype.

Yokogawa WT1800 power analyzer is employed to measure power losses in open-circuit and short-circuit tests. In open-circuit tests, core losses are measured at voltage level set $V_{dc1} = \{200V, 250V, 300V\}$. In short-circuit tests, currents are passed

through windings from 5 to 10A. Fig. 10 (d) shows the measured core and winding losses versus their calculated values at different operating points. It can be observed from this figure that the measured and calculated power losses mismatch is small. Maximum mismatch is 15% for core losses at $V_{dc1} = 300V$. The calculated and measured total losses are 15.04 and 16.0W at nominal load, respectively. Total power losses mismatch is 6.25%. Calculated and measured efficiency are 99.50% and 99.46% in the same order. Achieved results show the correctness of the utilized analytical calculations in the previous sections. So, it can be concluded that the proposed design methodology and results are applicable in practice.

8 Conclusion

In this paper, a comprehensive $\eta\rho$-Pareto optimization is performed for medium frequency transformers (MFTs) in a 1MW ISOP-DAB converter. A simple design method is presented for rectangular litz wires. Moreover, optimum blocking voltage and operating frequency are determined based on the semiconductor losses behavior. Two sets of theoretical and practical optimizations are executed by GA and brute-force optimization methods, respectively. The theoretical optimal results show that the efficiency and power density of MFT increase by increasing voltage of the primary side H-bridges, i.e. blocking voltage. It is shown that semiconductors impose constraints on the MFT frequency and nominal voltage rather than MFT itself in high-power high-voltage converters. 1200V IGBTs and switching frequency 10kHz are achieved as the best compromise between blocking voltage and switching frequency. In these designs, the best trade-off between efficiency, power density and cost density are 99.63%, $18.61kW/dm^3$ and $50.39W/\$$, respectively. Maximum temperature rise is approximately 76.17°C in the core. Comparing the calculated losses versus the measurement results in a 3kW MFT prototype shows a mismatch about 6.25%. The promising experimental and 3D FEA results demonstrate the applicability of the proposed design considerations.

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