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Theoretical Evaluation of Semiconductor Loss Components Behavior in ISOP-DAB Converters

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***Abstract*—Input-Series Output-Parallel (ISOP) connected Dual-Active-Bridges (DABs) form an interesting topology which enable step down MVDC to LVDC by employing medium frequency transformers. Si-IGBT semiconductor devices are commonly used in power distribution grid applications such as Smart Transformers (STs) where both MVDC and LVDC energy ports can be presented. In this paper, Si-IGBT semiconductor loss components such as conduction, switching and gate driver losses behavior are theoretically evaluated in a wide range of blocking voltage, switching frequency and phase-shift angle of DAB converters. In addition, gate driver losses are approximated as a continuous function of blocking voltage based on available datasheets. The behavior of the loss components are analyzed for two 50 and 500 kW ISOP-DAB converters where DC voltage ratio is 10 kV/400V.**

Keywords—ISOP-DAB converter, IGBT losses, Gate driver losses, Blocking voltage

I. INTRODUCTION

The notion of Smart Transformer (ST) is introduced to control both power flow and communication flow in the medium voltage (MV) distribution grids [1]. Power flow control can be achieved by adopting ST's power electronic converters at the front end of MV distribution grids. Some kind of the front end converters, such as modular multilevel converters (MMCs), can provide MVDC energy port for the ST system [2]. Thus, MVDC to LVDC conversion is necessary in this topologies. This conversion can be obtained using several configurations rooting from isolated DC-DC converters.

There are some popular isolated DC-DC converter topologies that have drawn more attention in the second decade of the 21th century. Dual-Active Bridge (DAB) converter [3] and Series-Resonant Converter (SRC) [4] are among them. DAB converter single and three phase versions are able to achieve soft switching and relatively high efficiencies as well SRC. This converters can be directly used to convert MVDC to LVDC as done in [5] where a semi-DAB semi-SRC DC-DC converter is proposed to utilize the advantages of these two converters in the same time. Another example is 3-level NPC converter utilizing SiC IGBTs which is proposed in [6]. This work addresses a 100 kW converter and do not discusses the maximum achievable power rating using this topology. 15 kV SiC-MOSFETs used in this study [7] are under development yet and are not sufficiently matured to handle power ratings in range ~1 MW by using this hybrid topology.

In spite of 2 or 3 level SiC based converters which have limited power ratings, Si-IGBT based modular DC-DC converters can be adopted to construct megawatt class DC-DC converters with efficiency up to 97.5% as reported in [8]. Si-IGBTs with capability of carrying multiple thousand amperes are the best solution in this voltage and power level as they are adopted in the ABB power electronic traction transformer project [9]. Commercially available Si-IGBTs have not enough voltage rating to be used in 2 level topologies in MV application and alternative solutions are required.

In [10], a family of DC-DC converters based on MMCs are discussed and a new control method based on the DC control, is proposed for a single-phase MMC based DC-DC converters with the same topology in [11]. In [12], a 100 kW single-phase MMC based DC-DC converter for a SST is developed to convert 3 kV to 400 V DC. In addition, its three-phase version is also proposed in the same application and voltage and power rating [13]. These researches' primary aim is to show the applicability of the MMC based DC-DC converters in distribution grids and they do not provide any theoretical or practical results in the case of semiconductors optimization.

Another solution is Input-Series Output-Parallel (ISOP) connection of DAB modules. Some papers have developed control methods for controlling ISOP DAB converters [14], [15]. These papers are describing how to control the voltage and power balance between the DAB modules and do not evaluate power losses behavior of IGBTs. In [16], ISOP DAB converter is also proposed as the MVC to LVDC stage of a solid-state transformer (SST) where it converts 18 kV DC to 700 V DC in a 720 kVA system. The focus of the work is devoted to the power quality issues of the SST integration into 10 kV AC distribution grid. Therefore, power losses analysis of the system is missed in this work, too. Hence, a study in this field can bridge the gap for the probable applications of the ISOP DAB converters in MVDC to LVDC power conversion.

In this paper ISOP-DAB converter based on Si-IGBT switches for high power medium voltage applications is considered. A theoretical analysis is done on the semiconductor losses such as IGBT and antiparallel diode conduction losses (CL), IGBT switching losses (SL), antiparallel diode reverse recovery losses (RL), and gate driver losses (GDL) versus semiconductor voltage variations, switching frequency and phase-shift angle variations. A quadratic approximation is used to model the no-load losses and frequency dependent losses of the gate driver for charging and discharging the Q_G of the IGBT gate. Numerical analysis of two 50 kW and 500 kW ISOP converters are studied to obtain the results. Voltage level is 10 kV to 400 V. Comprehensive study of every loss component is given in a separate section.

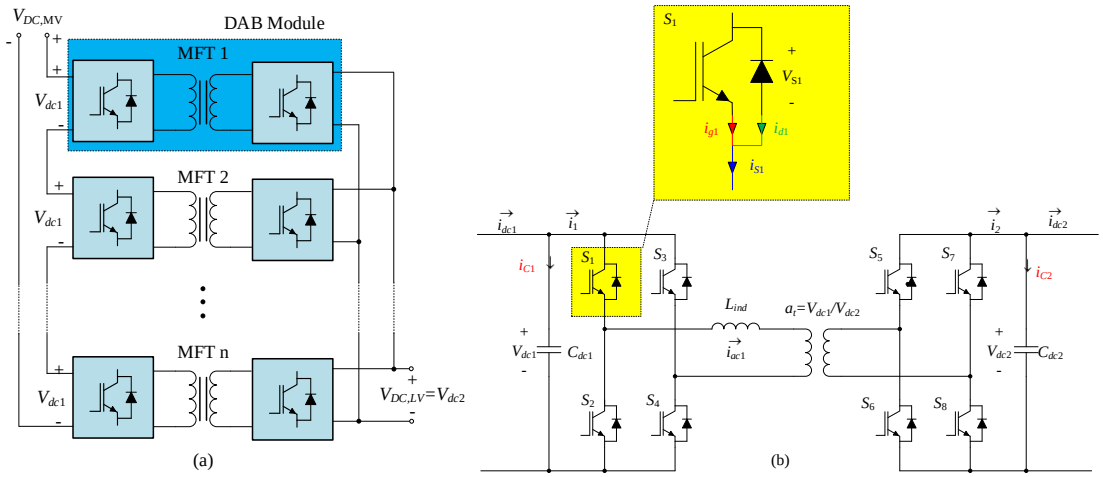

Fig. 1. (a) ISOP-DAB converter circuit topology and (b) DAB converters as building modules of the ISOP converter.

II. DAB Converter Operating Principles

Fig. 1 (a) shows ISOP DAB converter structure utilized as one of the possible DC transformer topologies. It can convert MVDC to LVDC by providing galvanic isolation. In fact, DAB converters used as building modules of the converters, are able to step down the voltage sufficiently where non-isolated DC-DC converters are unable to do. Fig. 1 (b) shows the DAB circuit and its waveforms are shown in Fig. 2. Following relations are hold for ISOP DAB:

$$V_{dc1} = uV_B \tag{1}$$

$$N_{DAB} = \frac{V_{DC,MV}}{V_{dc1}} \tag{2}$$

$$a_t = \frac{V_{dc1}}{V_{dc2}} \tag{3}$$

$$L_{eq,DAB} = \frac{a_t N_{DAB} V_{dc1} V_{dc2}}{2\pi f_s P_N}.\varphi.\left(1-\frac{|\varphi|}{\pi}\right) \tag{4}$$

Where blocking voltage is denoted by V_B, semiconductor voltage utilization factor by u, number of DAB modules by N_{DAB}, equivalent series inductance by $L_{eq,DAB}$, switching frequency by f_s and phase-shift angle by φ. Other parameters can be identified from the given figures. Also, average and RMS value of the currents, required for loss calculations, can be calculated as:

$$i_{x,avg} = \frac{1}{T_s}\int_0^{T_s} i_x(t)dt \tag{5}$$

$$i_{x,rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_x^2(t)dt} \tag{6}$$

Two 50 and 500 kW ISOP-DAB converters are evaluated for different frequencies and phase-shift angles. Frequency swept from 1 to 10 kHz in 1 kHz steps and φ swept from 30 to 50 degrees in 5 degree steps. The DAB's main parameters are calculated based on pre-specified $V_{DC,MV}$=10 kV and V_{dc2}=400 V. The DAB's main parameters are shown in Fig. 3 versus blocking voltage variation from 600 up to 6500 volts. As it can be seen for V_B=600 V about 31 DAB modules are required and for V_B=6500 V only 3 DAB modules are required to construct the ISOP-DAB converter.

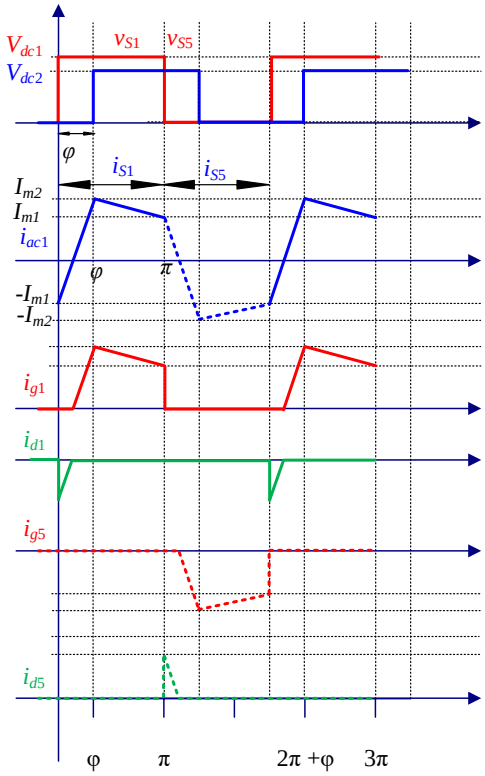

Fig. 2. Ideal waveforms inside Si-IGBTs in every DAB converter in Continuous Current Mode (CCM).

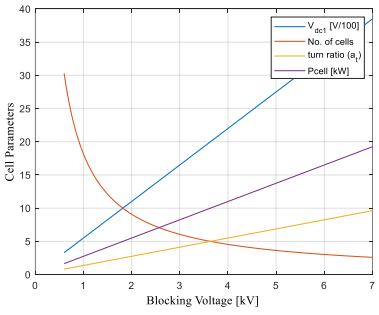

Fig. 3. Cell's main parameters as a function of blocking voltage. In this figure V_{dc1} (divided by 100) changes from 330 up to 3850 volts versus blocking voltage (f_s=5 kHz and P_N=50 kW.

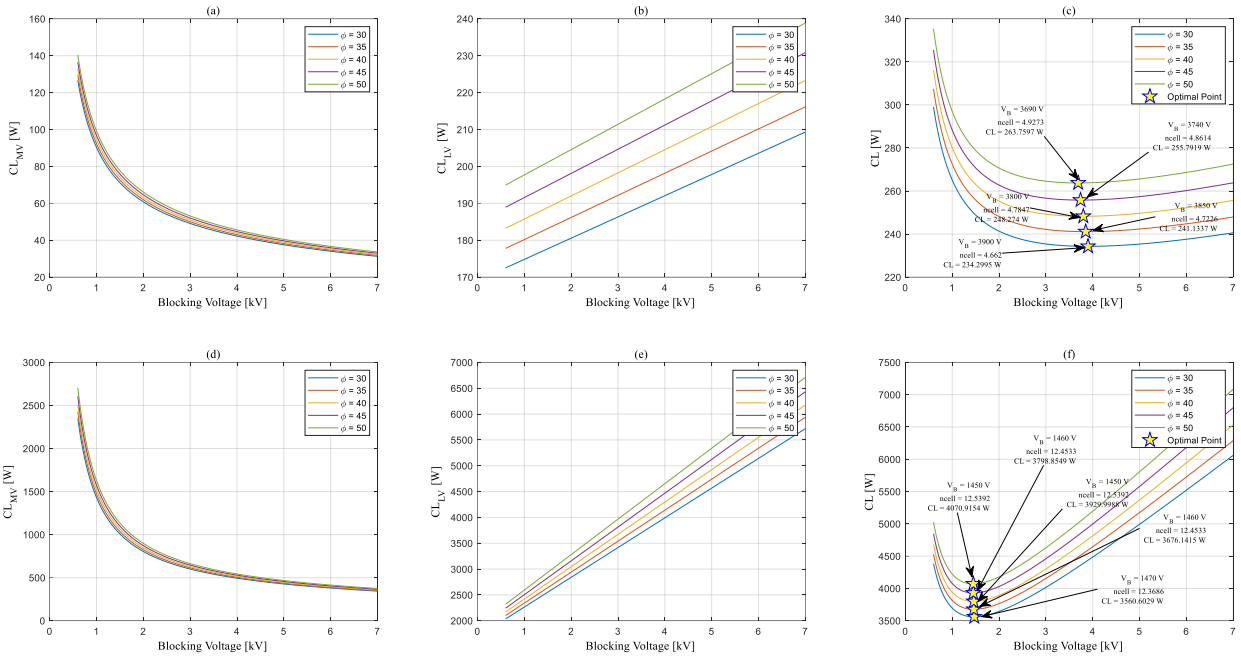

Fig. 4. Conduction losses components: (a) MV side total CL, (b) LV side total CL (c) total CL for 50 kW converter; (d) MV side total CL, (e) LV side total CL (f) total CL for 500 kW converter.

III. Conduction Losses Evaluation

CL can be calculated for IGBTs and diodes as follows:

$$P_{CL,IGBT} = v_{CE0}.i_{IGBT,avg} + r_{ON}.\left(i_{IGBT,rms}\right)^2 \quad (7)$$

$$P_{CL,diode} = v_{F0}.i_{d,avg} + r_{ON}.\left(i_{d,rms}\right)^2 \quad (8)$$

Where IGBT and diode currents are discussed in section II. Following [17], CL can be approximated as a function of blocking voltage (V_B) as:

$$P_{CL,x} = A_{v0}\log\left(B_{v0}V_B + C_{v0}\right)i_{x,avg} + \frac{i_{x,rms}^2}{I_N}A_r\log\left(B_rV_B\right) \quad (9)$$

Where A_{v0}, B_{v0}, C_{v0}, A_r, and B_r are constant values given in [17]. Also, subscript x denotes IGBT or diode device. In (9), data provided by manufacturers are interpolated into a straight forward equation that can model the IGBT or diode CL as a function of blocking voltage (V_B), rated current (I_N).

Fig. 4 (a) and (b) show the total losses in the 50 kW ISOP converter MV and LV sides at frequency 5 kHz, respectively. Evidently, CL at MV reduces with the increase in blocking voltage instead CL at LV side increases vs increase in the blocking voltage. MV and LV side CL are summed up and shown in Fig. 4 (c). As it can be seen, the conduction losses at the LV side limits the adoption of semiconductor with high V_B in the MV side. Also, it can be seen that increasing φ has higher impact on CL of LV than MV side. Golden pentagons show the optimal points in subfigures (c) and (f). This figure demonstrates that the blocking voltage near 4 kV is the optimal solution for direct power flow (PF) from the MV to LV side. Nearest available IGBT ratings are 3.3 kV and 4.5 kV IGBTs. For reverse power flow from LV to MV side, optimal V_B is a little higher than 4500 V which its results are not given. So, from the CL point of view, the optimum blocking voltage is 4500 V and optimal number of cascaded cells is 4 for 50 kW ISOP DAB converter. Fig. (d), (e) and (f) show MV side, LV side and total CL of the 500 kW ISOP converter, respectively. Same behavior is visible, however, the optimum compromise occurs in lower blocking voltages 1500 V. It can be concluded that the optimum blocking voltage has a reverse relation with the power rating of the ISOP converter.

Generally, CL is a function of on-state resistance, collector current and forward voltage drop of the semiconductor devices. In MV side of the DAB, collector current is constant and input voltage of the DAB cell is variable so small number of cascaded cells is preferred because the equivalent on-state resistance is smaller. While, in the LV side, the voltage is constant and collector current is variable and IGBTs with blocking voltages up to 1200 V can be used. In this study 1200 V IGBTs are considered. Large number of cascaded cells at LV side is preferred from CL point of view because the collector current in the LV semiconductors is reduced and therefore smaller CL is expected.

IV. Switching Losses Evaluation

Both current and blocking voltage are considered to compute SL of IGBTs

$$E_{SW} = \frac{V_{DC}}{V_B}.\frac{E_{SW}\left(I_N\right)}{I_N}.i_{SW} \quad (10)$$

Where I_N, $E_{SW}(I_N)$, V_{DC}, and V_B are nominal current of the semiconductor, switching energy given in the semiconductor's datasheet, DC voltage used for measuring $E_{SW}(I_N)$ and blocking voltage of the semiconductor, respectively. $K_{SW}=E_{SW}(I_N)/I_N$ can be specified for turn-on, turn-off and diode reverse recovery losses, respectively. Following quadratic equations can be used for approximating of normalized turn-off, turn-on, and diode reverse recovery losses vs V_B.

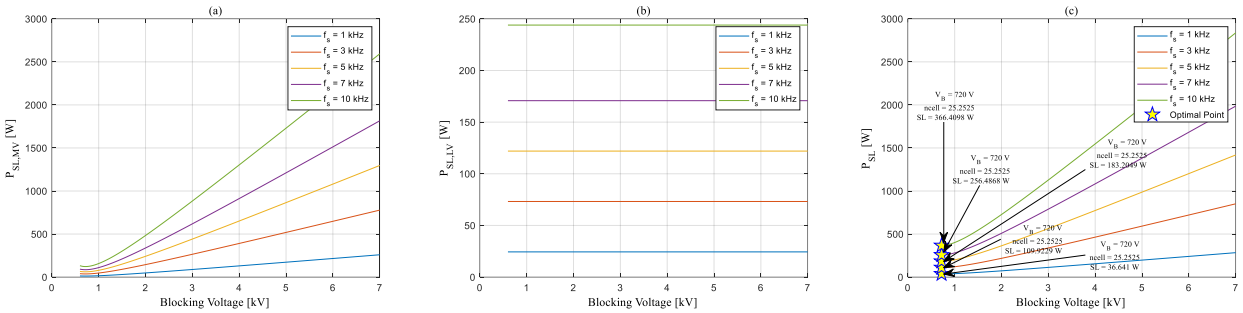

Fig. 5. SL in the (a) MV side H-bridges, (b) LV side H-bridges and (c) total for direct PF at φ=π/4 for 50 kW ISOP DAB converter.

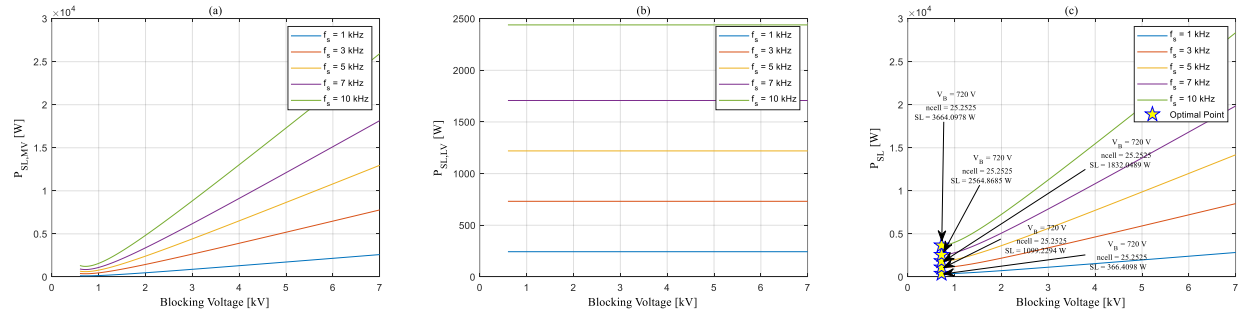

Fig. 6. SL in the (a) MV side H-bridges, (b) LV side H-bridges and (c) total for direct PF at φ=π/4 for 500 kW ISOP DAB converter.

$$K_i\left(V_B\right) = A_i V_B^{\,2} + B_i V_B + C_i \tag{11}$$

Where A_i, B_i and C_i and i = off, on, rec are given in for Si-IGBTs from 600 up to 6500V in [17]. But, for i_{SW}, average value of the IGBT switch is considered. For a given IGBT switch and antiparallel diode, total SL can be calculated using

$$P_{SW,IGBT}\left(V_B\right) = \left(K_{off}\left(V_B\right) + K_{on}\left(V_B\right)\right).i_{avg,IGBT}.\frac{V_{DC}}{V_B}.f_S \tag{12}$$

$$P_{SW,Diode}\left(V_B\right) = K_{rec}\left(V_B\right).i_{avg,Diode}.\frac{V_{DV}}{V_B}.f_S \tag{13}$$

$$P_{SL}\left(V_B\right) = P_{SW,IGBT}\left(V_B\right) + P_{SW,Diode}\left(V_B\right) \tag{14}$$

Where f_S is the switching frequency and the equation is divided by 1000 to convert mW to W.

Total SL components of 50 kW ISOP DAB converter are given in Fig. 5 (a), (b) and (c) for MV side, LV side and total SL, respectively. Switching losses in the secondary side is constant and does not change versus blocking voltage as shown in Fig. 5 (b) or Fig. 6 (b). Fig. 5 shows that for small blocking voltages near 600 V and 1200 V, SL is very smaller than the large blocking voltages near 4500 V and 6500 V. Also, increasing switching frequency intensifies the switching losses such that for V_B=6500 kV and f_S=10 kHz, approximately 6% of input power is dissipated. Another important outcome is that SL for blocking voltages close to 600 V and 1200 V in the direct PF is smaller than that reverse PF. Based on the given results, V_B=600 V is the best choice from the SL point of view. Fig. 6 gives the SL components for 500 kW ISOP converter. It can be seen that SL is not a function of the power rating of the ISOP DAB converter. Both 50 kW and 500 kW converters present a similar behavior in the case of SL. This analysis is also valid for reverse recovery losses of the antiparallel, so, its results are not included in the paper.

V. Gate Driver Losses Evaluation

In the most of power electronic designs, Gate Driver Losses (GDL) are omitted in the optimization process due to its lower losses comparing to the other power losses portions. However, in the modular power electronic converters where a large number of converters are connected in series or parallel, the number of adopted switches enhances exponentially and the GDL portion becomes significant. Also, CL and SL are depending on the gate driver switching commutation times and turn on/off resistance values in the switch gate which not the aim of this study.

Many researches have worked on the gate driver requirements such as [18] and [19]. But, there is only a few research that are discussing GDL [20] and [21]. And even this researches are satisfied with the computation of charging and discharging energy of the Q_G. For instance in [20], the commercial 1200 V IGBTs drivers are characterized based on their output powers and also Q_G.

Driver losses are depending on the charging and discharging of the input capacitance of the IGBTs, i.e. C_{ISS}. Active power that is dissipated in the input capacitance of the IGBTs can be computed in a switching period as:

$$\begin{aligned} P_{G,avg} &= \frac{1}{T_S}\int_0^{T_S} v_{GE}(t).i_G(t)dt \\ &= C_{ISS}.\left(V_{GE}\right)^2.f_S = Q_G.V_{GE}.f_S \end{aligned} \tag{15}$$

Total gate charge, i.e. Q_G, is given by manufacturers in the datasheets. Fig. 7 (a) shows the Q_G of 96 IGBT modules from three manufacturers with nominal voltage from 600 V up to

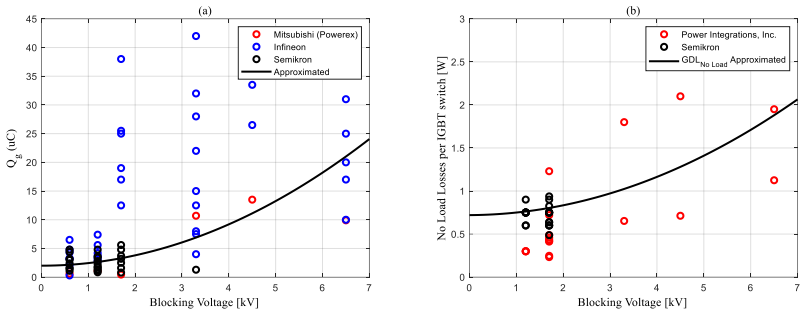

Fig. 7. (a) Q_G of the different manufacturers, and (b) Approximated GDL at no load.

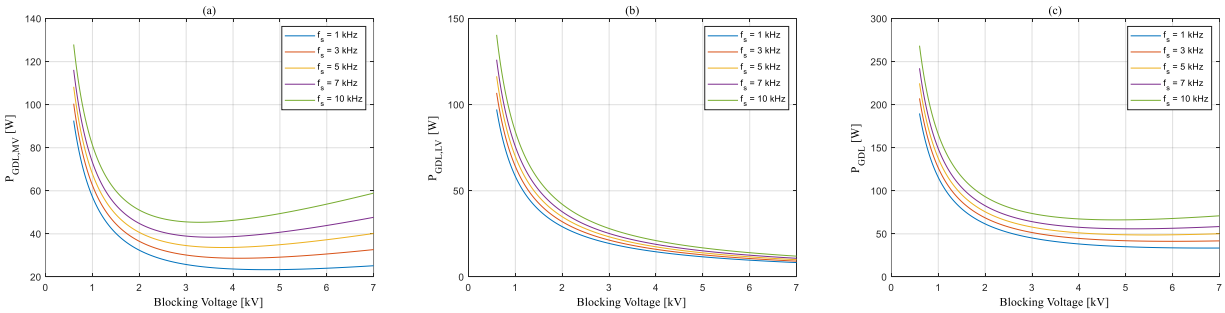

Fig. 8. GDL in the ISOP topology. (a) MV GDL at φ=π/4, (b) LV GDL at φ=π/4, and (c) Total GDL at φ=π/4.

6500 V. A quadratic equation is used to approximate Q_G based on these manufacturers' datasheets.

$$Q_G = A_G \times V_B^{\,2} + B_G \times V_B + C_G \tag{16}$$

Where V_B is the blocking voltage and final equation for P_G is given by

$$P_G = \left(A_G \times V_B^{\,2} + B_G \times V_B + C_G\right) \times V_{GE} \times f_S \times 10^{-6} \tag{17}$$

From Fig. 7 (a), Infineon IGBTs consume a higher power than Mitsubishi and Semikron IGBTs, because they have larger Q_G. In fact, IGBT driver boards and ICs are designed based on Q_G such that the driver be able to provide this amount of charge within the switching frequency.

To have an estimation of the GDL, the consumed power by the driver circuits has to be measured. One acceptable way is to evaluate the existing industrial gate drivers. For this purpose, about 100 IGBT gate driver datasheets from Infineon, Mitsubishi, Semikron, Power Integrations, Inc., and Wolfspeed are investigated. Power Integrations, Inc. offers gate driver solutions for IGBTs and MOSFETs from 5.5 kW up to MW and in blocking voltages from 600 V up 6.5 kV. These drivers are selected because enough data is reported in their datasheets to compute the actual power consumption for drivers at no load condition.

The data given in datasheets are used to approximate no load gate driver losses. No load losses per IGBT switches is approximated by a quadratic equation as shown in Fig. 7 (b). It has to be noted that these losses mainly depend on the driver technology and for a given Q_G two different manufacturer may provide gate driver with completely different no load characteristics. So selection of drivers also has a direct effect on the overall efficiency, especially, when lower V_B is used and large number of IGBT switches have to be driven. Quadratic equation that estimates no load losses is

$$P_{G0} = A_{G0} \times V_B^{\,2} + B_{G0} \times V_B + C_{G0} \tag{18}$$

As the no load losses are independent of switching frequency and the losses due to charging and discharging of Q_G are depending on switching frequency, therefore, the following equation can be used to roughly estimate the GDL as a function of blocking voltage.

$$P_{GDL}\left(V_B\right) = P_{G0}\left(V_B\right) + Q_G\left(V_B\right) \times V_{GE} \times f_S \times 10^{-6} \tag{19}$$

Parameters for calculating GDL are given in table I.

TABLE I. CONSTANTS OF GDL EQUATIONS

Q_G	A_G	B_G	C_G
	0.45	0.00	2.00
P_{G0}	A_{G0}	B_{G0}	C_{G0}
	0.027	0.003	0.72

In the case of GDL, the number of cascaded cells is the most important parameter. As can be seen from Fig. 8, GDL in MV and LV sides decreases by increasing blocking voltage. Total GDL varies from 50 up to 300 W depending on the switching frequency. It is visible that the GDL can affect the efficiency of the power electronic convertors when modular topologies are adopted. Therefore, seeking new methods for designing gate drivers in these topologies is needful. It has to be noted that gate drivers can affect both conduction losses and switching losses based on the driver on and off resistance, etc. However, in this report the focus is on the gate driver losses that are dissipated from driver operation, directly.

VI. DISCUSSION AND RESULTS

Now, semiconductor losses components can be summed up for finding the efficiency and the optimum point. Fig. 9 (a) shows the total losses of 50 kW converter for direct PF and

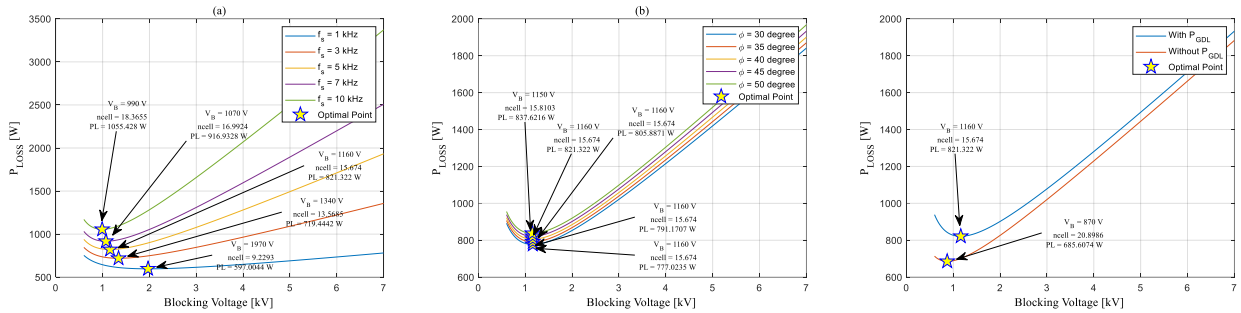

Fig. 9. 50 kW ISOP-DAB converter total losses: (a) effect of f_s on total losses, (b) effect of φ on total losses, and (c) effect of GDL.

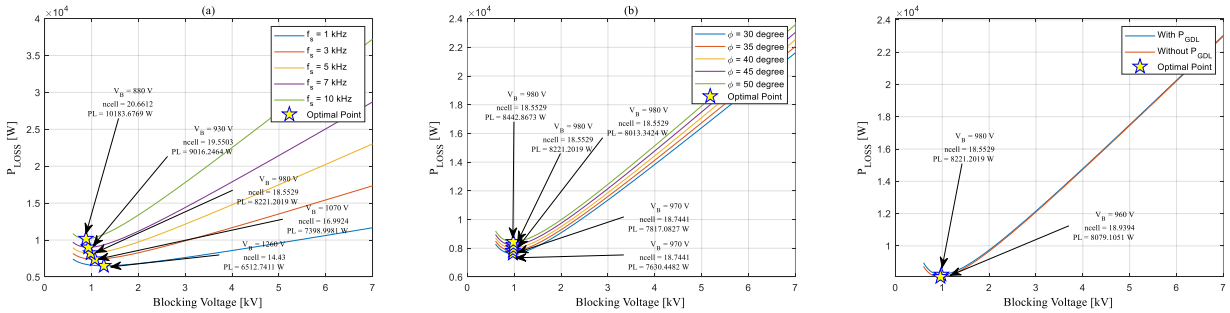

Fig. 10. 500 kW ISOP-DAB converter total losses: (a) effect of f_s on total losses, (b) effect of φ on total losses, and (c) effect of GDL.

φ=π/4. It can be seen that peak efficiency of 98% can be achieved even at high switching frequencies near f_s=10 kHz for V_B in range of 1-2 kV, i.e. 1200 and 1700 V IGBTs can be used. For f_s > 10 kHz, efficiency is lower than 98%. This high efficiency is achieved because the chip minimum area is constrained to achieve 99% efficiency for every cascaded H-Bridge as discussed in [17]. In 500 kW converter, similar results are obtained as can be seen in Fig. 10 (a). The effect of φ on the losses is respectively shown in Fig. 9 (b) and Fig. 10 (b) for 50 and 500 kW converters where small φ results in lower losses.

VII. Conclusion

Theoretical evaluation of the ISOP-DAB converter semiconductor losses is presented for MV distribution grid application such as SSTs. The CL, SL, GDL of ISOP- DAB topology are computed versus blocking voltage where both phase shift angle and switching frequency are considered. An analytical approximation which has two terms is presented for GDL. First term considers the no load losses of the gate drivers because the driver circuit consumes power for operation even at zero switching frequency. Second term is for computing losses due to charging and disgorging of the gate charges (Q_G) and it is depending on the Q_G and switching frequency. Simulation results are driven for two 50 and 500 kW ISOP-DAB converters. Conduction losses in the primary converters increase and in the secondary converter decrease versus blocking voltage. Also, switching losses of the primary converters increase and for the secondary converters remain constant versus blocking voltage. In addition, simulation results show that gate driver circuit can dissipate up to 0.5% of the input power for frequencies close to 5 kHz for power rating smaller than 50kW while its effect on 500 kW converter is negligible. It is also seen that the optimal blocking voltage is reversely proportional to nominal power. IGBTs with blocking voltage smaller than 1 kV are preferred for ratings over 500 kW.

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