Comparative study of heatsink volume and weight optimization in SST DAB cells employing GaN, SiC-MOSFET and Si-IGBT switches

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*Abstract –*Heatsink is a passive component for transferring heat due to power losses from power devices such as semiconductor switches in power electronic converters. Emerging semiconductor technologies such as GaN and SiC MOSFETs present lower conduction and switching losses than conventional Si devices which can led to increase efficiency and reduction of weight and volume. In this paper, comparative evaluation of the heatsink weight and volume optimization based on Si IGBT, SiC MOSFET and GaN is done in a dual-active-bridge (DAB) as a building block in solid-state transformers. A 5 kW DAB converter as one of the 16 modules in an 80 kW ISOP converter is considered in optimization. Heatsink design is done for three semiconductor types. Results show that GaN achieves lowest power losses while its heatsink size and volume is limited by the thermal properties of the GaN chip.

Index Terms – DAB converter, ISOP, SST, Heatsink, Weight and Volume Optimization.

I. INTRODUCTION

Advancements in semiconductor technologies in the beginning of the third millennium has introduced power electronics as one of the most important fields in electrical engineering. Many power electronic applications such as renewable power generation [1], traction systems and electric vehicles [2], HVDC power lines [3], and solid-state transformers (SSTs) [4] and [5] are based on the semiconductor industry. Emerging semiconductor technologies such as Silicon Carbide (SiC) [6] and Gallium Nitride (GaN) [7] and [8] power transistors can reach higher blocking voltage and efficiency than conventional Si IGBT technology [9]. However, they are currently under development and have not been matured enough. Some high voltage prototypes based on 10 and 15 kV SiC MOSFETs are reported [10] and [11], respectively. However, first 1200 V GaN switches are recently reported [12] and [13].

Based on the reported results in the [14], GaN devices only obstacle comparing Si and SiC devices is its lower thermal conductivity. In the other hand, GaN's lower on-resistance and switching losses and faster switching frequency outperform Si and SiC devices. It is also shown in [15] that the efficiency of a GaN based Buck-Boost converter is beter than Si and SiC ones even at high temperature and frequencies.
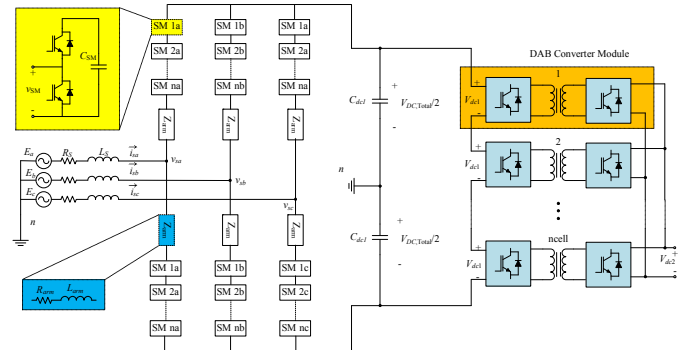

Fig. 1 SST with MMC as AC-DC front end converter and ISOP-DAB as DC-DC power conversion stage.

In [16] and [17], a bidirectional isolated DC-DC converter based on 600 V GaN devices is analysed where switching losses are modelled based on the PSpice simulation and verified for 1 kW DC-DC converter using experimental results. The work [16], claims maximum 2 W/GaN which gives 8 W losses for 4 used GaNs. This losses is responsible for 0.8% decrease in efficiency at full load which is unachievable using Si IGBTs. These works give a very good analysis of the GaN losses behaviour in the hard switching and ZVS modes but it doesn't evaluate the GaN thermal limits on the design of other components. One of the main components which its design is directly is a function of the semiconductor losses and thermal conductivity is heatsink. So, studying the heatsink sizing based on the GaN technology is also essential.

In this paper, 1200 V GaN technology is compared versus Si IGBT and SiC MOSFET from losses and heatsink requirement point of view in a DAB module of a SST, as shown in Fig. 1. For power losses analysis, analytical formulation is presented for achieving maximum utilization of the given datasheets by manufacturers. Every complementary curve in the datasheet is converted to a normalized factor and applied to the main measurements. Based on this method, a detailed analysis of the losses including switching, conduction, reverse recovery, C_{OSS}, and gate losses are derived which show the GaN superiority. The obtained losses are used to optimize heatsink volume and weight for Si, SiC and GaN. It is concluded that the SiC device can achieve minimum weight and volume for its heatsink due to its superior thermal conductivity over Si and GaN technologies.

II. SEMICONDUCTOR LOSSES ANALYSIS

Maximum utilization of datasheets for analytical calculation of semiconductor losses is studied in this section. Three 1200 modules including IKW25N120T2 [18], C2M0080120D [19] and VM40HB120D [13] by Infineon Inc., Cree Inc. and VisIC Technologies, respectively. VM40HB120D is the first 1200V GaN power module.

A. Conduction Losses

General formula for computing conduction losses is:

$$P_{Cond} = v_{CE0}.I_{avg} + r_{ON}.I_{rms}^2 \tag{1}$$

Where v_{CE0} and r_{ON} can be approximated based on the V_{CE}-I_C curves for transistors and diodes. For SiC MOSFETs and GaN v_{CE0} is zero. Also, I_{avg} and I_{rms} values depend on the current passing through the transistor or the diode.

$$v_{CE0} \triangleq v_{CE0}\left(I_C, T_j, V_{DS}, V_G\right) = k_{v0T}k_{v0V}k_{v0G}v_{CE0}\left(I_C\right) \tag{2}$$

$$r_{ON} \triangleq r_{ON}\left(I_C, T_j, V_{DS}, V_G\right) = k_{rT}k_{rV}k_{rG}r_{ON}\left(I_C\right)$$

Where

$$k_{v0T} = \frac{v_{CE0}(T)}{v_{CE0}(T_{test})}, k_{v0V} = \frac{v_{CE0}(V_{CE})}{v_{CE0}(V_{CEtest})}, k_{v0G} = \frac{v_{CE0}(V_G)}{v_{CE0}(V_{Gtest})}$$

$$k_{rT} = \frac{r_{ON}(T)}{r_{ON}(T_{test})}, k_{rV} = \frac{r_{ON}(V_{CE})}{r_{ON}(V_{CEtest})}, k_{rG} = \frac{r_{ON}(V_G)}{r_{ON}(V_{Gtest})} \tag{3}$$

Every k_r or k_{v0} factor can be defined for the corresponding given measurements in the datasheet. In the datasheet, if r_{ON} vs I_C is measured in $Tj = 175 °C$, then k_{rT} can be calculated for 125 °C as $k_{rT} = r_{ON}(125)/r_{ON}(175)$. Anti-parallel diode conduction losses can be calculated, similarly.

$$P_{d,Cond} = v_F.I_{d,avg} + r_F.I_{d,rms}^2 \tag{4}$$

Where v_F and r_F are the forward voltage and current of the anti-parallel diode. Also, v_F and r_F can be defined as functions of temperature, diode current and same formulation given in (2) and (3) can be repeated. Fig. 2 shows typical values for v_{CE0} and r_{ON}.
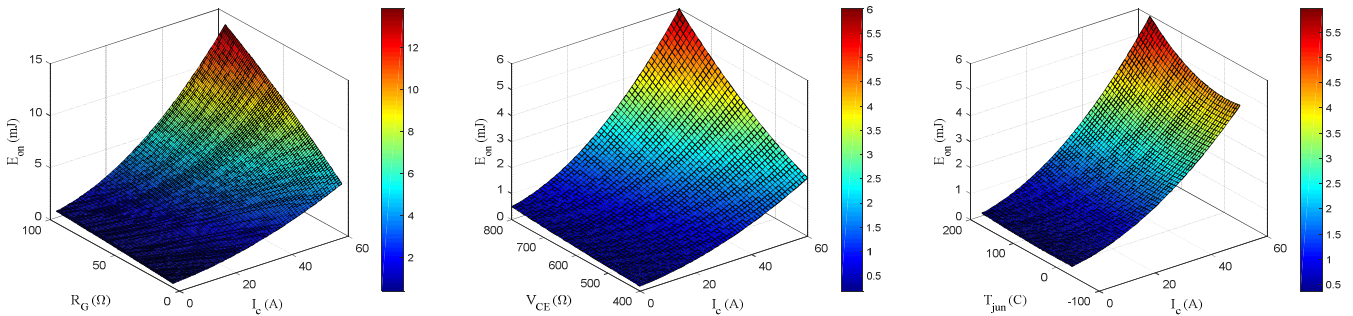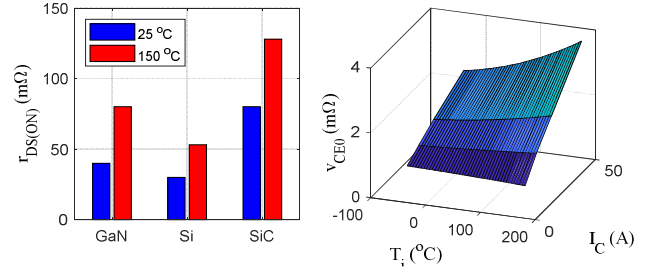

Fig. 2 On-state resistance of the considered switches with Si, SiC and GaN technologies are shown in the bar graph left side. Surf graph in right side shows the effect of temperature and collector current on the Si IGBT v_{CE0}. v_{CE0} is zero for SiC MOSFET and GaN power modules.

B. Switching Losses

Switching energy for any given current (I_C), temperature (T), voltage (V) and gate resistor (R_G) can be calculated.

$$E_i\left(I_C, T, V, R_G\right) = k_{eT,i}k_{eV,i}k_{eG,i}E_i\left(I_C\right) \tag{5}$$

Where

$$k_{eT,i} = \frac{E_i(T)}{E_i(T_{test})}, k_{eV,i} = \frac{E_i(V)}{E_i(V_{test})}, k_{eG,i} = \frac{E_i(R_G)}{E_i(R_{Gtest})} \tag{6}$$

Where K_i includes the effect of temperature, DC voltage and gate resistor in the formula. If there is no data provided by the manufacture, then corresponding k_i can be neglected. Fig. 3 shows the energy losses obtained from (5) for Si IGBT. Infineon Inc. has provided sufficient data for IGBT module IKW25N125T2 in the published datasheet, so it is considered.

So, switching losses for every single switch can be calculated considering switching frequency (f_s)

$$P_{SW} = \frac{f_s}{1000} \sum_{i \in \{on, off, rec\}} E_i\left(I_C, T, V, R_G\right) \tag{7}$$

Where subscript i denotes turn on, turn off and reverse recovery state. For SiC-MOSFETs and GaN switches, similar curves can be obtained. Fig. 4 shows a direct comparison for switching energy dissipation of the considered semiconductors. It can be seen that GaN and SiC MOSFET has similar switching loss properties which is approximately 1/10 of the Si IGBT switching losses.

Fig. 3 Variation of turn on energy losses E_{on} versus IGBT current, junction temperature, DC voltage and gate resistor for IKW25N125T2.
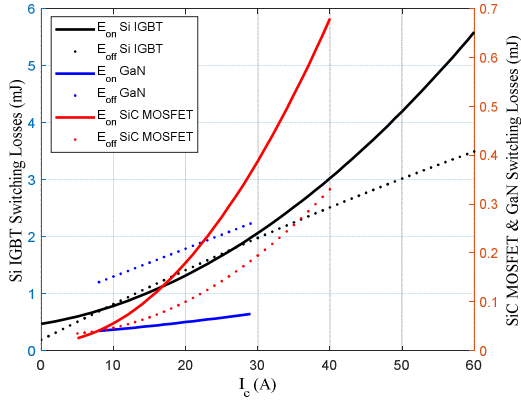
Fig. 4 Comparison of turn on and turn off energy losses based on datasheets for three switches of types Si IGBT, SiC MOSFET and GaN. Given data are for 600 V DC and junction temperature 150 °C.

Fig. 5 Comparison of E_{OSS} energy for SiC MOSFET and GaN.

C. C_{OSS} Losses

Charging and discharging of the output capacitor, C_{OSS}, dissipates energy in SiC MOSFETs and GaNs. The value of C_{OSS} energy can be significant in Mega-Hz switching frequency range based on the study given in [20]. In this study, switching frequency is lower than 100 kHz and C_{OSS} losses is not comparable to the switching losses. However, to make the study more general, C_{OSS} losses are also included in the study. C_{OSS} losses can be calculated as a function of f_s:

$$E_{OSS} = \frac{1}{2}C_{OSS}V_{DS}^2 \rightarrow P_{OSS} = \frac{f_s}{10^6}E_{OSS} \qquad (8)$$

In (7) is C_{OSS} is in pF. C_{OSS} can be approximated using sigmoid functions as follows [21]:

$$C_{OSS} = a_{c0} + a_{c1}\frac{e^{\left(\frac{-V_{DS}+a_{c3}}{a_{c4}}\right)}}{1+e^{\left(\frac{-V_{DS}+a_{c3}}{a_{c4}}\right)}} + a_{c2}\frac{e^{\left(\frac{-V_{DS}+a_{c5}}{a_{c6}}\right)}}{1+e^{\left(\frac{-V_{DS}+a_{c5}}{a_{c6}}\right)}} \qquad (9)$$

Where a_{ci} are constants that can be obtained from curve fitting. Fig. 5 shows the E_{oss} provided in the datasheets. Blue line shows the E_{oss} of the GaN switch. In the GaN datasheet, only C_{oss} is given for voltages 0 to 400 V. So, E_{oss} for voltages larger than 400 V needs measurement to be verified.

D. Gate Losses

Gate driver losses can be split into two parts. First part is due to the charging/discharging of gate charges, Q_G, for turning off and on the switch and the second is losses due to the driver circuit. Only the first part can contribute to the semiconductor junction temperature. So, it can be calculated as follow:

$$P_G = \frac{1}{T_S}\int_0^{T_S} v_{GE}(t) i_G(t) dt = C_{ISS}V_{GE}^2 \cdot f_S = Q_G V_{GE} f_S \quad (10)$$

Where C_{ISS} and V_{GE} are input capacitor and gate to emitter voltage, respectively. The value for Q_G is 120, 62 and 9.6 nC for Si IGBT, SiC MOSFET and GaN switches respectively.
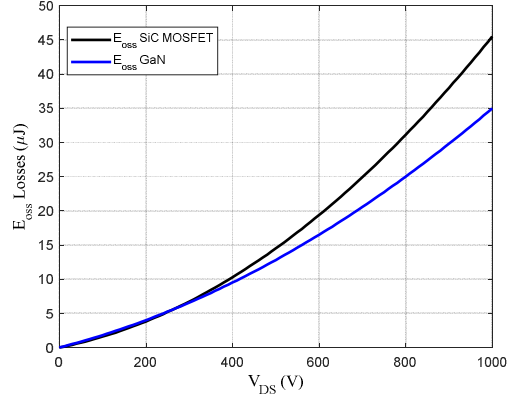
III. HEATSINK DESIGN PROCEDURE

Heatsink extrusions that are commercially available are cost effective and can be adopted for the design. First step in the heatsink design is to select the semiconductor switches. It can be done based on the voltage and current rating of the converter. Heatsink surface temperature can be obtained by computing the semiconductor power losses and using the thermal resistance of the junction to case, $R_{th,jc}$, as follows:

$$\theta_{HS} = \theta_j - R_{th,jc}P_{loss} \qquad (11)$$

Maximum required thermal resistance for a heatsink to transfer the heat from heatsink surface is:

$$R_{th} \leq \frac{\theta_{HS} - \theta_a}{N_{SW}P_{L,SW}} \rightarrow R_{th,\max} = \frac{\theta_{HS} - \theta_a}{N_{SW}P_{L,SW}} \qquad (12)$$

Where $P_{L,SW}$ and N_{SW} are power losses per switch and number of switches, respectively. Manufacturers usually provide $R_{th,n}$ for nominal length, L_n, and temperature rise of heatsink to the ambient $\Delta\theta_n$ [22]. Correction factor curves are used to compensate $R_{th,n}$ for arbitrary L_{HS} and $\Delta\theta$ as shown in Fig. 6.
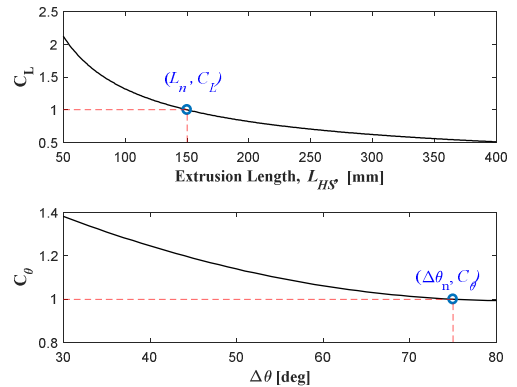

Fig. 6 Heatsink extrusion's correction factors of Aavid Permalloy LLC.

These curve can be approximated using quadratic polynomial equations:

$$C_L = a_{L0} + a_{L1}(L_{HS}) + a_{L2}(L_{HS})^2 \qquad (13)$$

$$C_\theta = a_{\theta 0} + a_{\theta 1}(\Delta\theta) + a_{\theta 2}(\Delta\theta)^2 \qquad (14)$$

Where quadratic polynomial coefficients can be calculated by selecting three points on the curves such as (a_{L0}, C_{L0}), (a_{L1}, C_{L1}) and (a_{L2}, C_{L2}).

$$\begin{bmatrix} a_{L0} \\ a_{L1} \\ a_{L2} \end{bmatrix} = \begin{bmatrix} 1 & L_{HS0} & L_{HS0}^2 \\ 1 & L_{HS1} & L_{HS1}^2 \\ 1 & L_{HS2} & L_{HS2}^2 \end{bmatrix}^{-1} \begin{bmatrix} C_{L0} \\ C_{L1} \\ C_{L2} \end{bmatrix} \qquad (15)$$

Therefore, the required length correction factor and the minimum length of the extrusion can be found from the following:

$$C_L \geq \frac{R_{th,max}}{C_\theta R_{th,n}} \qquad (16)$$

$$L_{HS,min} = \left(-a_{L1} \pm \sqrt{a_{L1}^2 - 4a_{L2}a_{L0}}\right)/2a_{L2} \qquad (17)$$

Based on the $L_{SH,min}$ total weight and volume of the extrusion are computed.

Flowchart of the heatsink design is shown in Fig. 7. Based on the figure, semiconductor rating is the start point of the design. After selection of the switch ratings, its data can be used to drive the conduction, turn on and turn of losses as well reverse recovery losses. The semiconductor loss calculation method is given in section III of the paper. So, after calculation of power loss per switch (P_{loss}) and also by using the junction to case thermal resistance ($R_{th,jc}$), the heatsink surface temperature (θ_{HS}) can be obtained. In this paper, maximum allowable junction (θ_j) and ambient temperature (θ_j) are 125 ℃ and 40 ℃, respectively.

Arrangement of the semiconductors on the heatsink surface also plays an important role in the final optimized weight and volume. For half-bridge modules, four possible arrangements are shown in Fig. 8. Every heatsink configuration is shown by a color which will be used for depicting design results.

IV. SIMULATION RESULTS

As stated in section II, three semiconductor technologies Si IGBT, SiC MOSFET and GaN are employed for optimizing heatsink volume and weight of a 5 kW 600 to 400 V DAB converter which is considered as the basic building cell of the DC-DC stage of an 80 kW SST.

A. Semiconductor Losses

Fig. 9 (a), (b) and (c) show semiconductor losses for a single switch of type Si IGBT, SiC MOSFET and GaN where GaN device exhibits lower torn off, conduction, gate and C_{OSS} losses than Si IGBT and MOSFET. For the Si IGBT switching frequency is set in range 1-20 kHz and for SiC MOSFET and GaN frequency is set to 1-100 kHz. In the case of turn on losses, dissipated energy in the junction capacitor in included

too. Using the GaN in ZVS mode can reduces the switching losses extremely because turn off losses are negligible [17].
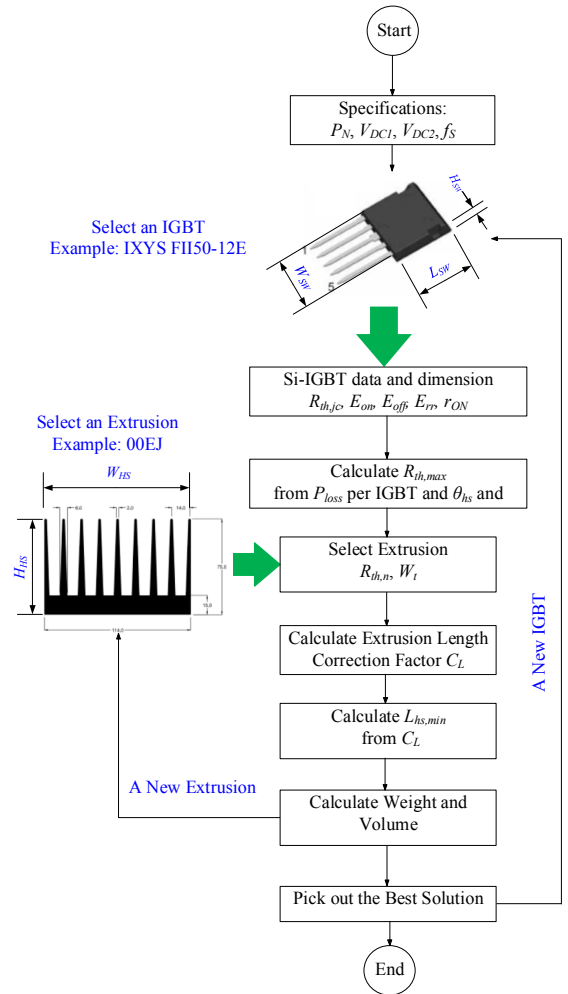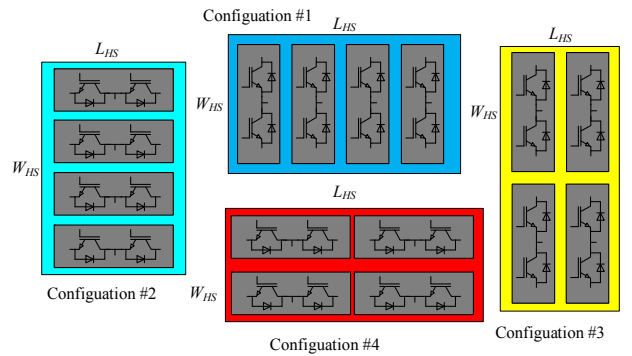

Fig. 7 Heatsink design flowchart.

Fig. 8 Arrangement of Half-Brides on the heatsink for a DAB converter.

B. Heatsink Optimal Design

Number of 138 extrusions manufactured by Aavid Permalloy LLC [22], that are proper for mounting semiconductor switches, are considered. Fig. 10 shows volume optimization results for different semiconductor technologies.
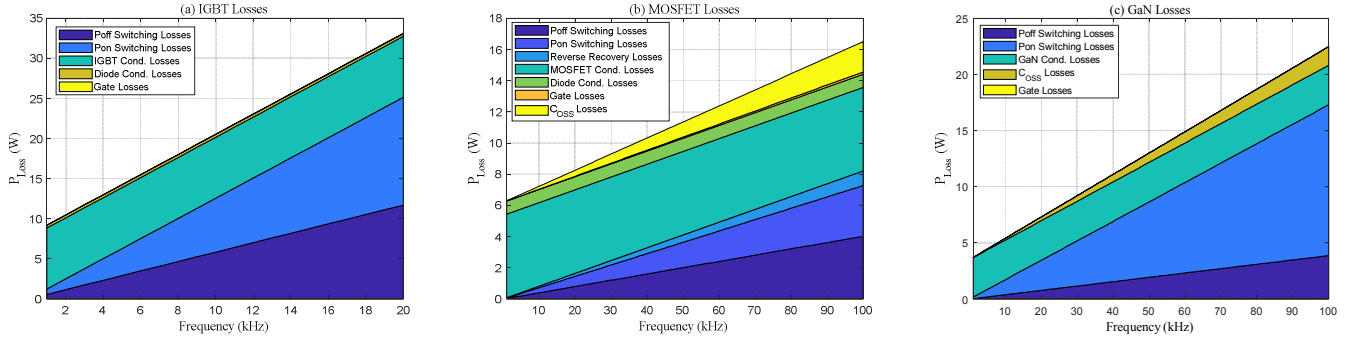
Fig. 9 Detailed power losses for different semiconductor technologies; (a) Si IGBT losses for f_s=1-20 kHz, (b) SiC MOSFET and (c) GaN for f_s=1-100 kHz.
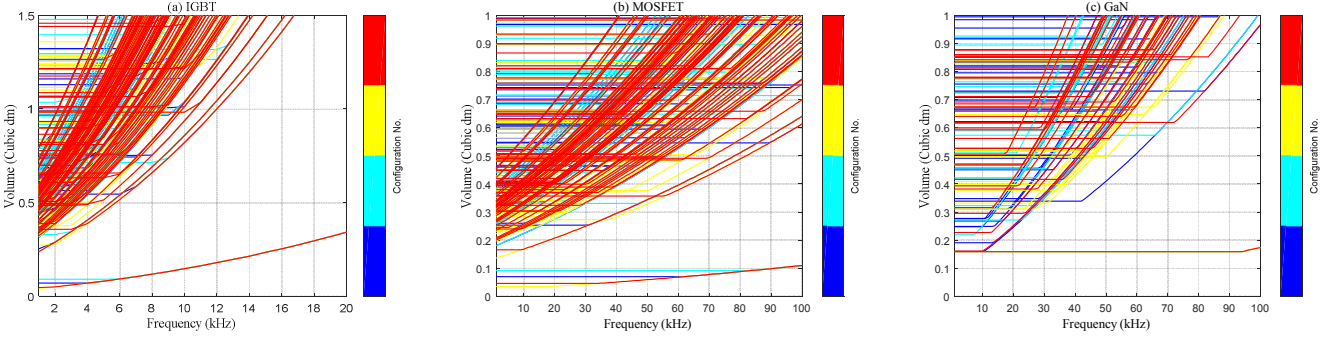

Fig. 10 Heatsink volume optimization for different semiconductor technologies; (a) Si IGBT, (b) SiC MOSFET and (b) GaN.
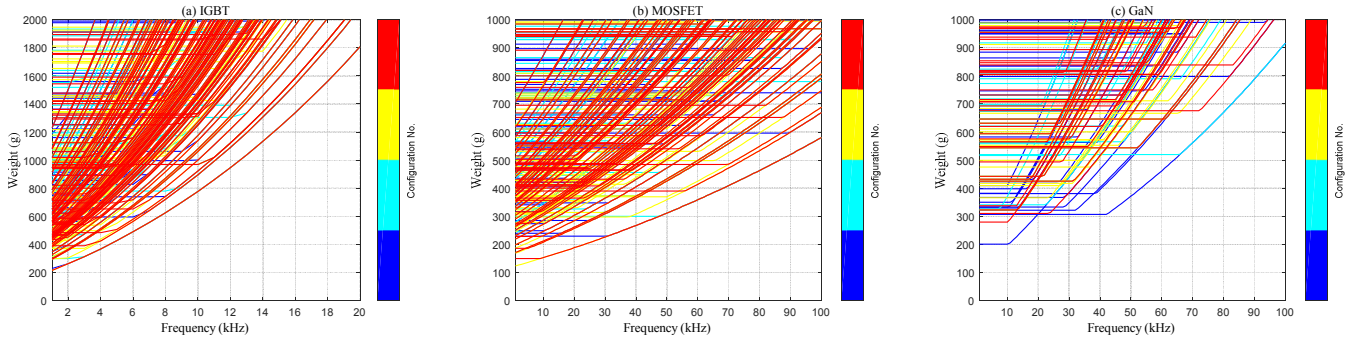

Fig. 11 Heatsink weight optimization for different semiconductor technologies; (a) Si IGBT, (b) SiC MOSFET and (b) GaN.

In Fig. 10 (a), results for IGBT are given where extrusion with part number 04870 gives the minimum volume for frequencies from 2-20 kHz. While, extrusion number 04870 is the best for 1 kHz. Minimum volume is 0.343 dm³ at f_s=20 kHz. For SiC MOSFET, volume optimization results are given in Fig. 10 (b) where extrusion 04870 is the best for f_s=1-100 kHz which gives the volume of 0.1102 dm³ at f_s=20 kHz. In the case of volume optimization for GaN device, Fig. 9 (c), extrusion 04870 is the best solution for all frequencies from 1 to 100 kHz. It gives volume of 0.1740 dm³. This value is a bit larger than SiC MOSFET due to the increase in turn on losses. Another limiting constraint on volume reduction is GaN package dimensions which typically larger than IGBT and MOSFET. Horizontal line in Fig. 10 (c) implies on the physical constraint for volume reduction in extrusion 04870.

Similar to volume optimization, weight optimization results are also derived and given in Fig. 11 (a), (b) and (c) for Si IGBT, SiC MOSFET and GaN, respectively. Extrusion BS204 is the best solution for the IGBT, MOSFET and GaN

devices at all frequencies. However, for the MOSFET in frequencies lower than 8 kHz its mounting configuration is not the same as well GaN in frequencies larger and lower than 20 kHz. In frequency of 100 kHz heatsink weight is 581 and 917 g for MOSFET and GaN devices, respectively.

Adopting ZVS for turning on switches, reduces the weight to 666 g for GaN which is not slighter than SiC hard switching mode. This is due to the thermal conductivity limitation of GaN. It is stated in [15], that the thermal conductivity can be stated as $\lambda(\theta_L) = \lambda_{300K} (\theta_L / 300K)^\alpha$ where θ_L denotes the temperature of the chip lattice, α is -0.43 and -1.61 for GaN and SiC respectively. Also, conductivity at room temperature, λ_{300K}, is 125 and 490 W/mK for GaN and SiC, respectively. Fig. 12 compares the GaN and SiC conductivity for various room temperatures. It can be seen from this figure that even if GaN can enhances the efficiency over Si and SiC technologies but its heatsink size must be larger than the size of the SiC's heatsink due to thermal conductivity constraints.

TABLE I

HEATSINK DESIGN RESULTS

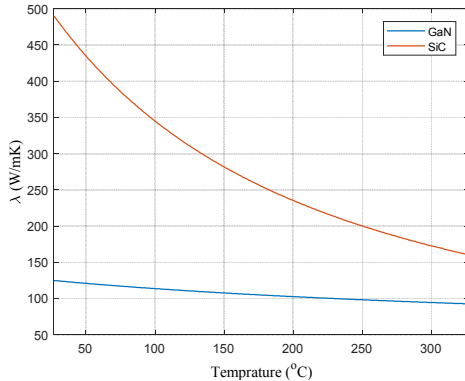| Semi.	Si IGBT	SiC MOSFET	GaN
Module	IKW25N120T2	C2M0080120D	VM40HB120D
f_s	20 kHz	20 kHz	20 kHz
Losses	33.1230 W	8.2599 W	7.3094 W
Min. Vol.	0.343 dm³	0.0459 dm³	0.1591 dm³
Extrusion	04870	04870	04870
Min. Weight	1808 g	188 g	311 g
Extrusion	BS204	BS204	000EB (437210)

Fig. 12 Comparing GaN and SiC thermal Conductivity.

Table I summarizes the obtained results at frequency 20 kHz where three semiconductor topologies can be compared. It can be seen that the minimum power losses 7.31 W is achieved using GaN. So, based on the minimum losses, minimum weight and volume can be expected. However, GaN thermal conductivity constraints are lower than the SiC MOSFET which limits the heatsink size reduction.

V. CONCLUSION

Semiconductor losses are analytically computed such that maximum utilization of the datasheets is obtained. A general formula is given which includes a factor in calculation for any extra given curve in the datasheets. Based on the loss calculation method, losses for three semiconductor technologies including Si IGBT, SiC MOSFET and GaN are computed and used as the design input for natural convection heatsink. GaN devices can achieve the minimum losses by ZVS in comparison with Si IGBT and SiC MOSFET. Therefore, minimum weight and volume of heatsink can be achieved by adopting GaN, subject to improving its thermal conductivity limitations.

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