Techniques for High-Efficiency Outphasing Power Amplifiers

by

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Abstract

A trade-off between linearity and efficiency exists in conventional power amplifiers (PAs). The outphase amplifying concept overcomes this trade-off by enabling the use of high efficiency, non-linear power amplifiers for linear amplification. However, the efficiency improvement is limited by the efficiency of the output power combiner. This thesis investigates techniques to overcome this efficiency limit while maintaining sufficient linearity. Two techniques are proposed. The first technique is called the outphasing energy recovery amplifier (OPERA), which recovers the normally wasted power back to the power supply and utilizes a resistance compression network for improved linearity. A 48-MHz, 20-W prototype OPERA system was built which demonstrates more than 2x higher efficiency than the standard outphasing system for a 16-QAM signal. The second technique to improve the efficiency of the outphasing system is asymmetric multilevel outphasing (AMO) modulation. In the AMO system, the amplitude for each of the two outphased PAs can switch independently among multiple discrete levels, significantly reducing the energy lost in the power combiner. Three different AMO prototypes were built, each of which demonstrate between 2x-3x efficiency improvement compared to the standard outphasing system. A 2.4-GHz, 500-mW prototype made in a 65-nm CMOS process achieves an average system efficiency of 28.7% for a 20-MHz 64-QAM signal. To the author's best knowledge, this is the highest reported efficiency for a CMOS PA in the 2-2.7 GHz range for signal bandwidths greater than 10 MHz.

Thesis Supervisor: Joel L. Dawson
Title: Associate Professor

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Jack Chu helped me with random tasks in the lab like soldering my PCB, and he also helped me a lot when I had general analog circuit questions. He did some

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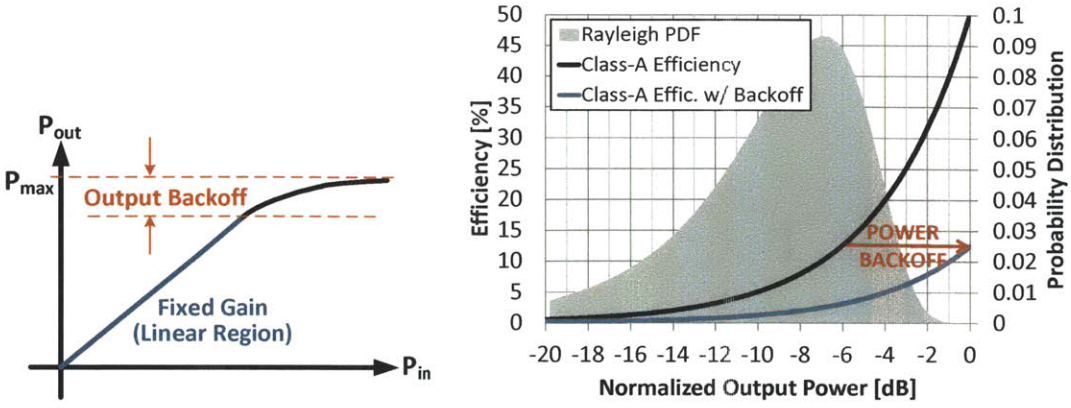
Chapter 1

Introduction

Power amplifiers (PAs) are used in many different applications. Examples include audio speakers and wireline data networks such as Ethernet, as well as biomedical applications such as magnetic resonance imaging and ultrasound. However, probably the biggest application today is wireless communication systems, which include cellular handsets and base stations, wireless local area networks (WLAN), and wireless personal area networks (WPAN) such as Bluetooth. The performance of a wireless communication system depends heavily on the power amplifier. Specifically, the wireless system's maximum achievable data rate is determined by the PA's linearity. In addition, the PA usually dominates the whole transceiver's power budget, increasing the cost of the system and limiting battery life for portable electronic devices. Thus, it is important that the PA have both high linearity and high efficiency. Unfortunately, there is typically a tradeoff between linearity and efficiency in PA design. The goal of this work is to explore techniques that overcome this tradeoff.

1.1 Motivation

In wireless communication systems, both efficiency and linearity are desired. Wideband communication standards that support high data rates such as WLAN/3G/LTE employ complex modulation methods that have considerably increased the linearity requirements of transmitter PAs. Battery life in mobile electronic devices is decreasing



(a) (b)

Figure 1-1: (a) Typical transfer characteristic for a conventional conducting-class PA. (b) Efficiency vs. output power for a class-A PA with and without power backoff. A Rayleigh output power probability distribution, which is a typical of many wireless communication standards today, is also shown for reference.

as broadband access and more diverse functionality (e.g., Wi-Fi, Bluetooth, camera, media player, etc.) are integrated into the device, and so high efficiency is also desired. In cellular base stations, a significant portion of the operating costs come from losses in the PA, including the cost of the energy drawn from the power grid as well as overhead costs such as bulky heat dissipating panels.

Unfortunately, a tradeoff between linearity and efficiency exists in conventional power amplifiers [1]. Conducting-class power amplifiers, such as class-A and class-AB, offer great linearity but are very inefficient [2,3]. Figure 1-1(a) shows the typical transfer characteristic for a conventional conducting-class PA. To maintain linearity, the PA must be operated at much lower output powers than the maximum, where the gain is constant. Since efficiency is proportional to output power, the efficiency is also lower in this region. Figure 1-1(b) shows the effect of power backoff on overall efficiency for a conventional PA. We can see that PA efficiency must be sacrificed to achieve higher degrees of linearity.

On the other hand, switching classes, such as class-D, class-E, and class-F, have excellent efficiency, but are very non-linear [4,5]. In switching-mode PAs, the transistor is used as a switch, which ideally dissipates zero power because either the current

or the voltage is zero at any given time. However, the PA input-to-output characteristic is no longer linear because the output is no longer a function of the input (the operation of an ideal switch does not depend on the input amplitude).

Traditionally, non-linear, switching-class PAs can only be used in phase- or frequency-modulated systems, while all amplitude-modulated systems require conducting-class PAs with good linearity. Since modern wireless communications usually employ both amplitude and phase modulation to achieve higher data rates, an inefficient linear PA is typically used. To achieve higher efficiency, a tremendous amount of research on radio frequency (RF) transmitters using high efficiency, nonlinear PAs has been conducted over the last few decades. One potential solution is the outphasing system.

1.2 Outphasing Power Amplification

The outphasing power amplifier concept dates back to the early 1930's as an approach for the simultaneous realization of high-efficiency and high-linearity amplification [6]. The principle of outphasing, also known as linear amplification with nonlinear components (LINC) [7], is shown in Figure 1-2. The fundamental idea of the LINC architecture is to decompose the signal to be amplified into two constant-envelope signals that are phase-modulated such that their vector sum reproduces the original signal. Since the two signals are constant-envelope, they can be amplified by highly efficient, nonlinear PAs. The output of the two PAs are then summed with a power combiner at the output to produce an amplified version of the input. The key advantage of this approach is that each amplifier can operate in an efficient albeit nonlinear mode, and yet the final output can be highly linear, breaking the usual tradeoff between linearity and efficiency in power amplifiers.

However, one of the major disadvantages of the LINC architecture is the power wasted in the power combiner. The two switching-mode PAs are constant-envelope, and so they always consume a fixed amount of power, regardless of how much power is sent to the output. Thus, when the output power is low, the efficiency is also low. By conservation of energy, any power that is not sent to the output is wasted as heat

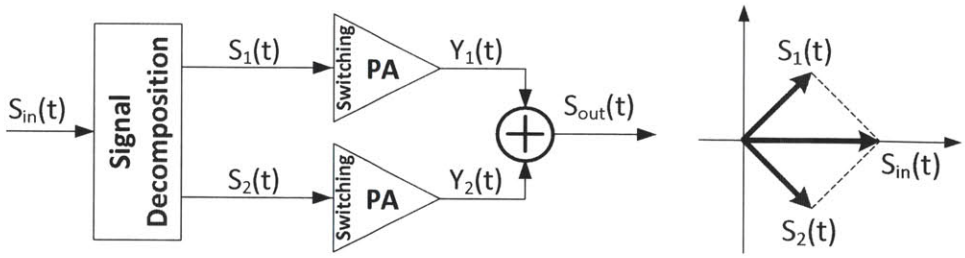


Figure 1-2: (a) LINC principle diagram. (b) LINC vector diagram.

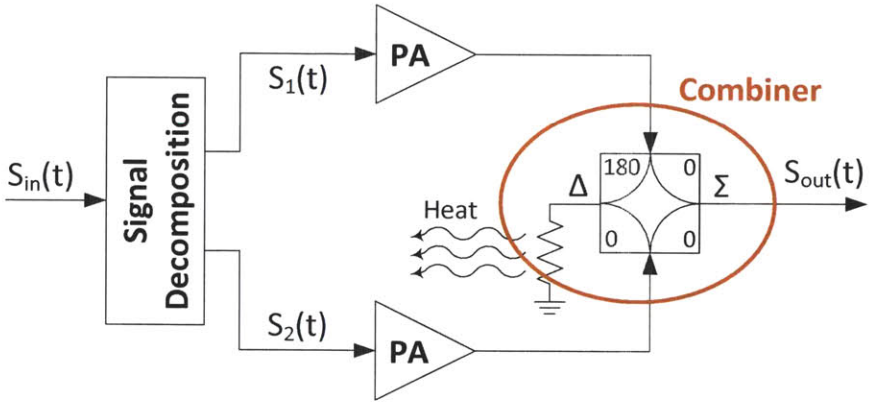


Figure 1-3: LINC system with conventional isolating combiner.

in the combiner, as shown in Figure 1-3. Specifically, a conventional combiner has two output ports, one for the sum of the two signals being combined and one for the difference. The sum port is usually connected to the output load, while the difference port is terminated by an "isolation resistor" to ensure correct impedance matching and isolation for the two PAs [8]. Since the power delivered to the combiner by the two PAs is constant, the efficiency of the LINC system is directly proportional to the power sent to the output. The time-averaged efficiency is therefore inversely proportional to the peak-to-average power ratio (PAPR) of the signal being transmitted. Unfortunately, the modulation schemes used in modern communication standards tend to have high PAPR, leading to low average efficiency when the LINC system is used. This thesis investigates techniques to improve the efficiency of the LINC architecture while maintaining sufficient linearity.

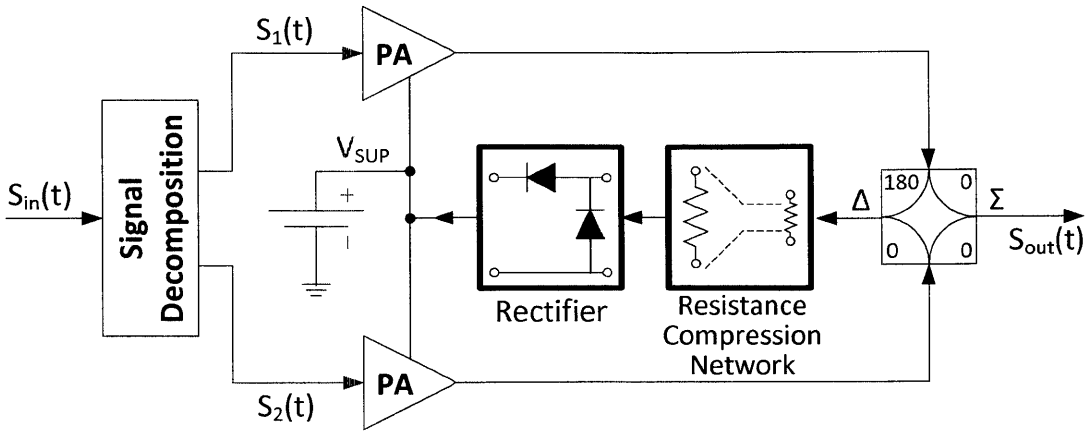


Figure 1-4: Outphasing energy recovery amplifier, utilizing a resistance compression network in the power recycling network.

1.3 Research Contributions

Two new PA architectures based on outphasing are proposed in this thesis that achieve high power efficiency and high linearity in wideband RF transmitters: (1) outphasing energy recovery amplifier (OPERA) with resistance compression, and (2) asymmetric multilevel outphasing (AMO).

The first contribution of this work is to present a new outphasing energy recovery amplifier (OPERA), shown in Figure 1-4, which replaces the isolation resistor in the conventional matched combiner with a resistance-compressed rectifier for improved efficiency [9]. The rectifier recovers the power normally wasted in the isolation resistor back to the power supply, while a resistance compression network (RCN) reduces the impedance variation of the rectifier as the output power varies. Because the combiner requires a fixed resistance at the isolation port to ensure matching and isolation between the two outphased PAs, the RCN serves to maintain high linearity as well as high efficiency in the switching-mode PAs. A 48-MHz discrete-component prototype is presented to demonstrate the feasibility of the system.

The second contribution of this work is to present a new outphasing architecture, AMO [10], shown in Figure 1-5, in which the output envelopes of the PAs can switch among a discrete set of levels. This means that when the output power is low, the out-

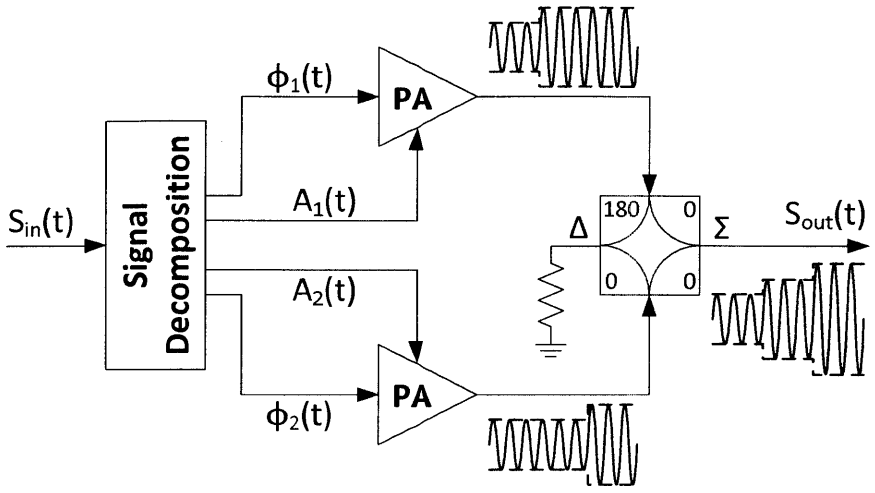


Figure 1-5: Asymmetric multilevel outphasing (AMO) architecture.

put envelope can switch to a lower level, reducing the amount of power being wasted in the combiner and improving the overall efficiency. Three different prototypes will be demonstrated. The first AMO prototype will be a 48-MHz discrete-component prototype for the purpose of demonstrating the feasibility of the system. The second AMO prototype will target cellular basestation applications, operating at 1.95 GHz with a maximum output power of 18 W. This prototype will be implemented with discrete components, utilizing a GaN device for the PA transistor. The third AMO prototype will be an integrated circuit (IC) implemented in a 65nm CMOS process and operating at 2.4 GHz, intended for mobile wireless applications.

1.4 Thesis Organization

The outline of this thesis is as follows. Chapter 2 briefly reviews classical architectures for achieving high-efficiency power amplification, including their advantages and disadvantages. Particular attention is then given to outphasing techniques, the chapter concluding with a review of previous techniques in the published literature for improving the efficiency of outphasing systems.

Chapter 3 explains the operation of the outphasing energy recovery amplifier (OPERA) system, including detailed analyses of both the rectifier used for energy

recovery and the resistance compression network used for improved linearity. The details of the 48-MHz discrete-component prototype for proof-of-concept are then presented, along with the measurement results which demonstrate a significant improvement in efficiency over the standard outphasing system.

Chapter 4 describes the operation of the asymmetric multilevel outphasing (AMO) system, including the required signal decomposition for AMO modulation and the theoretical efficiency of the system. The efficiency of asymmetric power combining is also discussed, along with the various methods of generating the discrete amplitude levels for the two outphased PAs. In addition, a method for optimizing the values of the discrete amplitude levels for maximum efficiency is presented, which is useful for supporting multiple different communication standards. Next, we describe a linearization technique for the AMO signal decomposition that uses digital predistortion based on lookup table training to correct for system nonlinearities. Chapter 4 concludes with the details of the two discrete-component prototypes built to demonstrate the feasibility of the AMO system: (1) a 48-MHz prototype for proof-of-concept, and (2) a 1.95-GHz prototype for cellular basestation applications. The measurement results for each prototype indicate the potential for the AMO system for high-efficiency and high-linearity power amplification.

Chapter 5 details the design and characterization of a third AMO prototype, an IC built in a 65-nm CMOS process and operating at 2.4 GHz, intended for mobile wireless applications. We first describe the design of the class-E PA implemented for the AMO IC prototype, including various techniques used to improve the efficiency of CMOS PAs. Then the design of the discrete supply modulator is discussed, including the techniques we used to minimize the loss in the switching network and to maximize the speed of the discrete supply modulation. The chapter concludes with measurement results of the IC prototype, once again demonstrating the high efficiency of the AMO system for wideband signal transmission.

Finally, Chapter 6 summarizes the contributions of this work and proposes new research projects to further improve the efficiency and linearity of power amplifiers.

Chapter 2

Techniques for High-Efficiency Power Amplification

As mentioned in Section 1.1, complex modulation methods used in modern wireless communication systems have considerably increased the linearity requirements of transmitter PAs. The result is that PA efficiency must be sacrificed to achieve the required linearity if a conventional PA is used. For this reason, a tremendous amount of research has been conducted in recent years on PA architectures that replace the linear PA with a nonlinear one that achieves higher efficiency. Such systems must manipulate the overall system to maintain sufficient linearity. There are several types of transmitter architectures that enable the use of high-efficiency, nonlinear PAs. Four prominent examples are (1) outphasing modulation, (2) polar modulation, (3) pulse-width pulse-position modulation (PWPM), and (4) Doherty.

2.1 Outphasing Modulation

The conventional outphasing architecture was briefly described in Section 1.2, and that description will be repeated here and expanded for the purpose of providing additional background information for this thesis. Outphasing [11], and specifically the LINC (linear amplification with nonlinear components) architecture introduced by Cox in [12], is shown in Figure 2-1. The fundamental idea of the LINC architecture

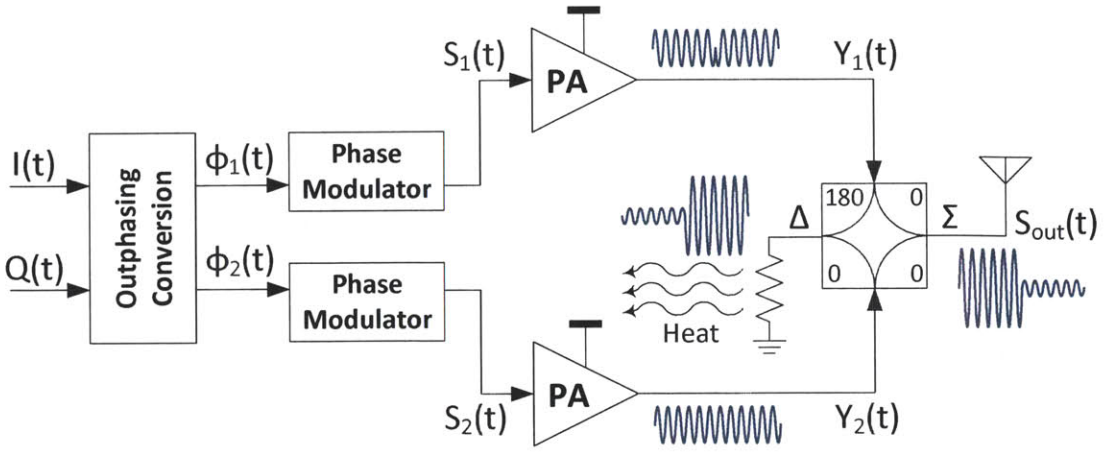


Figure 2-1: Conventional outphasing, or LINC, architecture.

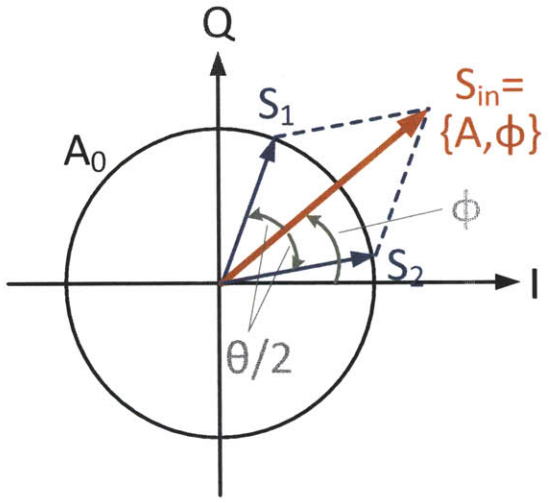


Figure 2-2: LINC vector diagram, including notational convention.

is to decompose the signal to be amplified into two constant-envelope signals that are phase-modulated such that their vector sum reproduces the original signal (see Figure 2-2). Since the two signals are constant-envelope, they can be amplified by nonlinear, high-efficiency switching PAs. The output of the two PAs are then summed with a power combiner at the output to produce an amplified version of the input.

Specifically, outphasing modulation decomposes an arbitrary RF input signal $S_{in}(t)$ into two constant-envelope signals $S_1(t)$ and $S_2(t)$ such that the sum constructs the original signal, as shown in Figure 2-2. Note that $S_{in}(t)$ can be represented as a

vector in the complex plane, and so $S_{in}(t)$ can be defined in terms of either Cartesian or polar coordinates as

$$S_{in}(t) = I(t)\cos[\omega t] + Q(t)\sin[\omega t] \tag{2.1}$$

$$S_{in}(t) = A(t)\cos[\omega t + \phi(t)] \tag{2.2}$$

where $I(t)$ and $Q(t)$ are the in-phase and quadrature components (respectively) of the RF signal being transmitted, $A(t)$ and $\phi(t)$ are the amplitude and phase components (respectively), and ω is the RF carrier frequency. Then the outphasing signal decomposition is as follows:

$$S_{in}(t) = S_1(t) + S_2(t) \tag{2.3}$$

$$S_1(t) = A_0(t)\cos\left[\omega t + \phi(t) + \frac{\theta(t)}{2}\right] \tag{2.4}$$

$$S_2(t) = A_0(t)\cos\left[\omega t + \phi(t) - \frac{\theta(t)}{2}\right] \tag{2.5}$$

$$\theta(t) = 2\arccos\left(\frac{A(t)}{A_{max}}\right) \tag{2.6}$$

$$A_{max} = \max|A(t)| \tag{2.7}$$

$$A_0 = \frac{A_{max}}{2} \tag{2.8}$$

$\theta(t)$ is called the *outphasing angle*. As can be seen in the above equations, the smaller the signal amplitude $A(t)$, the larger the outphasing angle $\theta(t)$. This can also be seen graphically in Figure 2-2.

In order for the overall outphasing system to achieve linear amplification, the output $S_{out}(t)$ should be a linear function of the input $S_{in}(t)$, or $S_{out}(t) = G \cdot S_{in}(t)$, where G is the constant gain factor of the overall PA system. If we let G be the gain of each of the individual PAs in Figure 2-1, then we have that

$$Y_1(t) = G \cdot S_1(t) \tag{2.9}$$

$$Y_2(t) = G \cdot S_2(t) \tag{2.10}$$

$$S_{out}(t) = Y_1(t) + Y_2(t) = G \cdot [S_1(t) + S_2(t)] \tag{2.11}$$

$$S_{out}(t) = G \cdot S_{in}(t) \tag{2.12}$$

Thus we can see that the outphasing system does indeed achieve linear amplification of the input signal, despite the use of nonlinear, switching-mode PAs.

The LINC architecture is able to use high-efficiency, nonlinear PAs and still achieve linear amplification by using outphasing to realize amplitude variation. However, the efficiency of the power combining is high only over a small range of output powers. To avoid signal distortion and preserve switching amplifier efficiency, an isolating combiner such as a Wilkinson combiner is typically used. Isolating combiners achieve 100% efficiency only at maximum output power. When the inputs are outphased to vary the amplitude, power is wasted as heat in the isolation resistor [13]. Since the power delivered to the combiner by the two PAs is constant, the efficiency of the LINC system is directly proportional to the output power sent to the antenna load. This trend is shown in Figure 2-3, which plots the theoretical maximum power efficiency vs. output power of the outphasing system using an isolating combiner. The plot shows that the efficiency of the LINC system is only 50% at 3-dB power backoff, corresponding to 50% of the maximum output power, as expected. At 6-dB power backoff (25% of maximum output power), the efficiency drops to 25%.

The time-averaged efficiency of the LINC system for any given application will depend on the probability distribution of the signal be transmitted. Because the instantaneous LINC system efficiency is directly proportional to the instantaneous output power, the time-averaged efficiency will be inversely proportional to the peak-to-average power ratio (PAPR) of the transmitted signal. Unfortunately, high-level modulation schemes such as 64-QAM (quadrature amplitude modulation) and OFDM (orthogonal frequency division multiplexing) tend to have high PAPR, leading to low average efficiency when the LINC system is used.

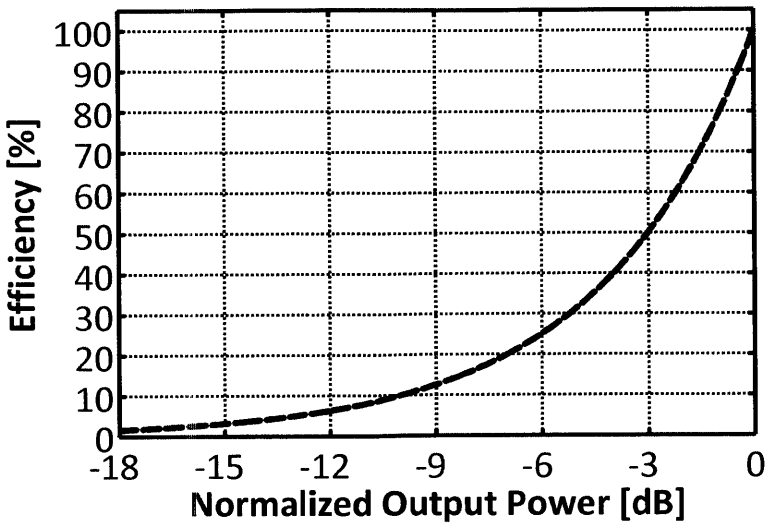


Figure 2-3: Efficiency vs. output power for the outphasing system using a conventional isolating combiner.

2.2 Polar Modulation

The fundamental idea of polar architectures (also known as envelope elimination and restoration, or EER), shown in Figure 2-4, is to divide the signal to be amplified into amplitude and phase components. The phase component is used as the input to a nonlinear, high-efficiency switching PA, while the amplitude component drives the power supply of the PA to create a varying-envelope signal [14–16]. While this improves the PA efficiency, it also requires the use of an efficient power converter for the amplitude modulator. Because power converter efficiency degrades significantly as bandwidth increases, it is very difficult to achieve high efficiency and high bandwidth simulataneously. This is exacerbated by the 5-10x bandwidth expansion that occurs during the conversion from Cartesian to polar coordinates [17]. Thus, this method is typically only effective for low-bandwidth systems. Various supply modulators such as the class-G modulator [18], two-point supply modulator [19, 20], and $\Delta\Sigma$ supply modulator [21], have been developed. However, all of these modulators still have the problem of suffering from a tradeoff between high linearity and wideband supply modulation.

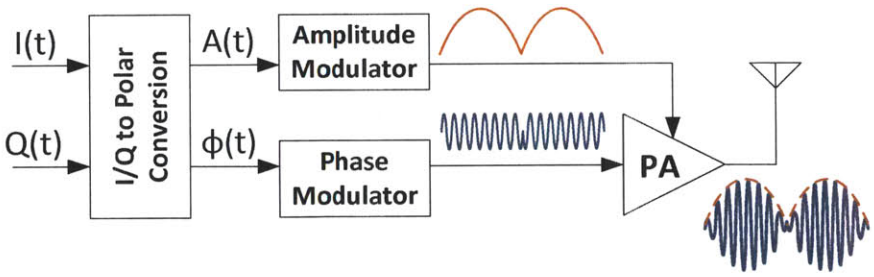


Figure 2-4: Conventional polar architecture.

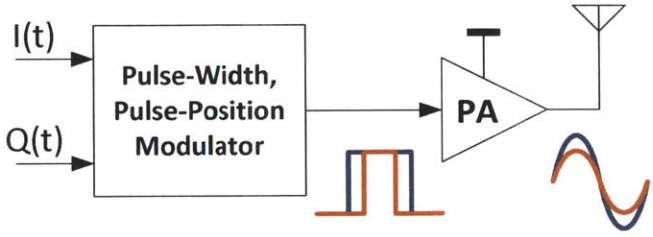
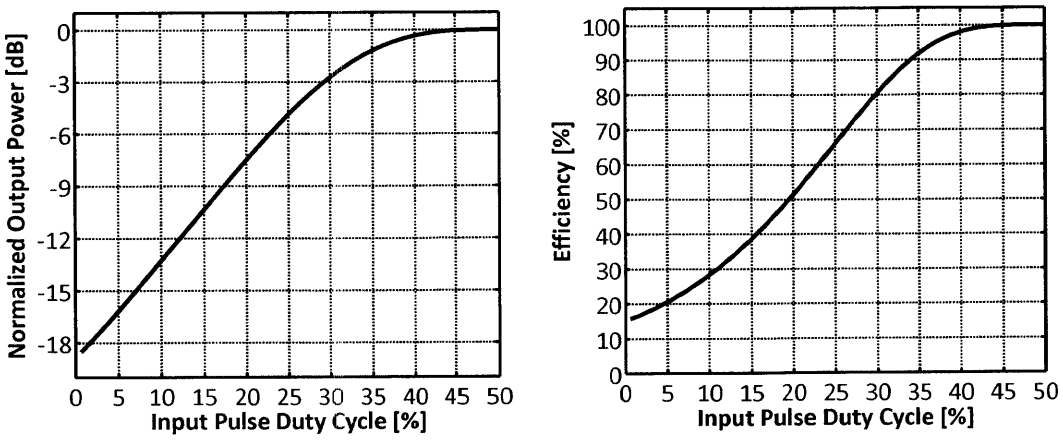


Figure 2-5: Pulse-width pulse-position modulated PA architecture.

2.3 Pulse-Width Pulse-Position Modulation

The pulse-width pulse-position modulated (PWPM) PA architecture [22,23], shown in Figure 2-5, obtains a time-varying output envelope by modulating the pulse width of the input signal to a switching-mode PA, thereby changing the conduction interval of the PA transistor and hence the PA output amplitude. The output phase is controlled by modulating the position of the input pulse. Figure 2-6 shows the simulated output power and efficiency of an ideal class-E PA depending on input pulse duty cycle, where the class-E PA has been designed for maximum efficiency at 50% duty cycle. Note that an ideal class-E PA only ideally provides 100% efficiency at one input duty cycle [24] because the zero-voltage switching condition can only be satisfied for one particular duty cycle.

PWPM achieves a higher efficiency than standard outphasing modulation. Figure 2-7 compares the power efficiency of an ideal outphasing PA and PWM PA. At 3-dB power back-off, the PWM PA efficiency stays at 78% while the outphasing PA efficiency is merely 50%. PWM is more efficient than outphasing because PWM controls the magnitude of an output fundamental tone by varying the input pulse duty



(a) (b)

Figure 2-6: Output power (a) and efficiency (b) of an ideal class-E PA with various input duty cycles.

cycle.

The main problem with PWM is that it is very difficult to generate small output amplitudes because small input duty cycles are required. Looking at Figure 2-6(a), even if the duty cycle is reduced to 1%, the output power will still be greater than -20dB, which corresponds to 10% of the maximum output amplitude. Furthermore, small duty cycles require narrow pulses, and such narrow pulses are not only difficult to generate at GHz frequencies, but are also usually filtered out by the large PA input capacitance. Typically this limits the amplitude control of the system to less than 10dB. Thus, the output amplitude dynamic range for PWM is usually too low to be used for high PAPR communication standards, significantly degrading the linearity of the system.

2.4 Doherty Power Amplifier

The Doherty PA, like the outphasing architecture, uses power combining for two PAs to achieve high efficiency. The classical Doherty architecture is shown in Figure 2-8(a), and the corresponding theoretical efficiency curve is shown in Figure 2.4 [25,26]. The "carrier" (main) PA is biased in class-B or class-AB mode (a linear PA), while

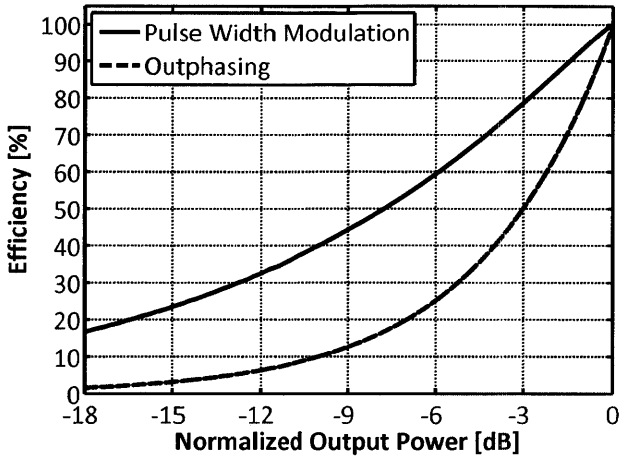


Figure 2-7: Comparison between the power efficiency of outphasing and pulse-width modulation depending on output power.

the "peaking" (auxiliary) PA is biased in class-C mode, so that it can only turn on after the input amplitude exceeds a specified threshold. Accordingly, only the carrier amplifier is operational at low power levels. As the power level increases, the efficiency of the carrier amplifier increases (just like any other PA), and it reaches the first maximum efficiency point. At this power level, the peaking amplifier is turned on. The second maximum efficiency point is reached when the peaking amplifier provides maximum efficiency. Therefore, the Doherty PA has two maximum efficiency points, enhancing the efficiency over a wide output power range. The location of the first efficiency peak can be optimized in the design to maximize the efficiency depending on the amplitude probability distribution of the signal being transmitted. A more detailed description of the operation of the Doherty amplifier can be found in [25,26].

Although the Doherty PA can achieve a high efficiency over a wide output power range, the Doherty PA uses quarter-wave tranmission lines to perform the power combining at the output as well as the power splitting at the input. These transmission lines have a narrow bandwidth around the RF carrier frequency (they are only a quarter wavelength at one particular frequency). Although a Doherty PA has been reported in [27] that achieves a fractional bandwidth of 35%, it is very difficult to achieve bandwidths much higher than this using the Doherty system. The

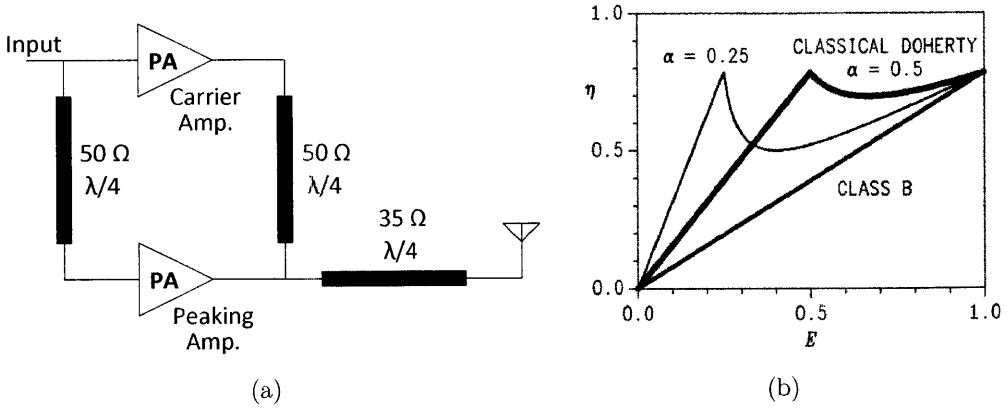


Figure 2-8: (a) Classical Doherty architecture. (b) Theoretical efficiency vs. normalized output amplitude for the classical Doherty architecture, for two different locations of the first efficiency peak. The efficiency of an ideal class-B PA is also shown for reference.

outphasing system also uses a power combiner, which can be implemented using quarter-wave transmission lines. However, it is possible to implement very wideband isolating power combiners, by using multiple transmission-line sections [28] or by using wideband transformers [29]. These wideband techniques are not possible for the Doherty system. Thus, the main drawback of the Doherty PA is that it cannot be used for multi-band operation with greater than 35% fractional bandwidth. Another disadvantage of Doherty systems is that the quarter-wave transmission lines are too long to be suitable for integration in silicon at the typical frequencies used in modern wireless communication systems (1-3 GHz).

2.5 Outphasing Techniques for Higher Efficiency

Of the four architectures discussed above, outphasing seems to be the best choice for achieving wideband RF power amplification with sufficient linearity. To alleviate the problem of wasted energy during outphasing, a number of techniques have been developed. These include Chireix combining, power recycling, and multi-level LINC.

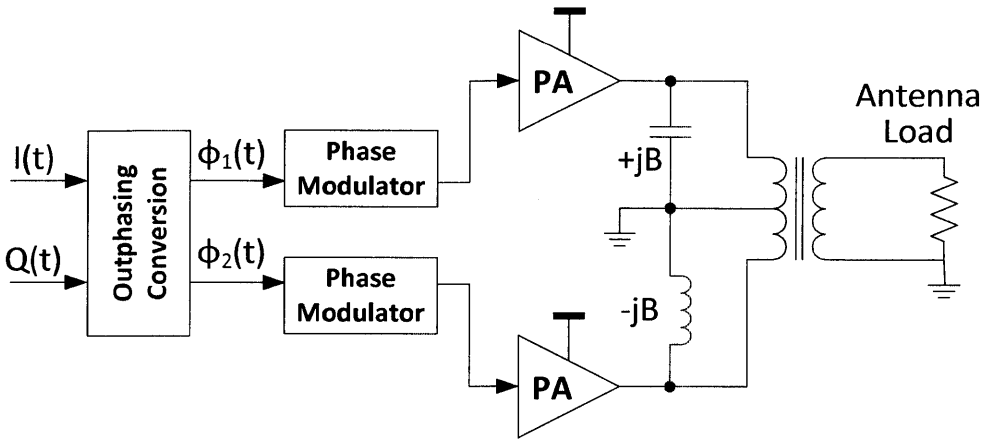


Figure 2-9: Chireix outphasing transmitter.

2.5.1 Chireix Combining

Figure 2-9 shows the Chireix outphasing architecture, which utilizes a nonisolating combiner that uses compensating reactive elements to enhance the power-combining efficiency [11, 13, 30]. However, the Chireix combiner can only be tuned to provide resistive loading of the PAs for a very small range of outphasing angles. With outphasing angles outside the tuned range, the load impedance presented to the PAs deviates too far from the nominal value and the isolation between the two power amplifiers' outputs becomes poor. The result is significant distortion and degraded PA efficiency.

One solution is to modulate the output matching network of the PAs along with the outphasing angle so that the impedance seen by the PAs is always resistive. Such adaptive termination of each amplifier was applied in [31] to improve the combiner efficiency over a much larger range of outphasing angles. However, one major problem of this technique is that it is very difficult to achieve a high quality factor in the capacitor array used to tune the output matching network. This is due to the resistance in the unit capacitor and the associated control switches. Furthermore, the maximum capacitance in the tuning array would require a very small inductance for a fixed resonant frequency. For frequencies above 1 GHz, this requires very small inductance values less than 1nH, which is difficult to achieve considering the bond-

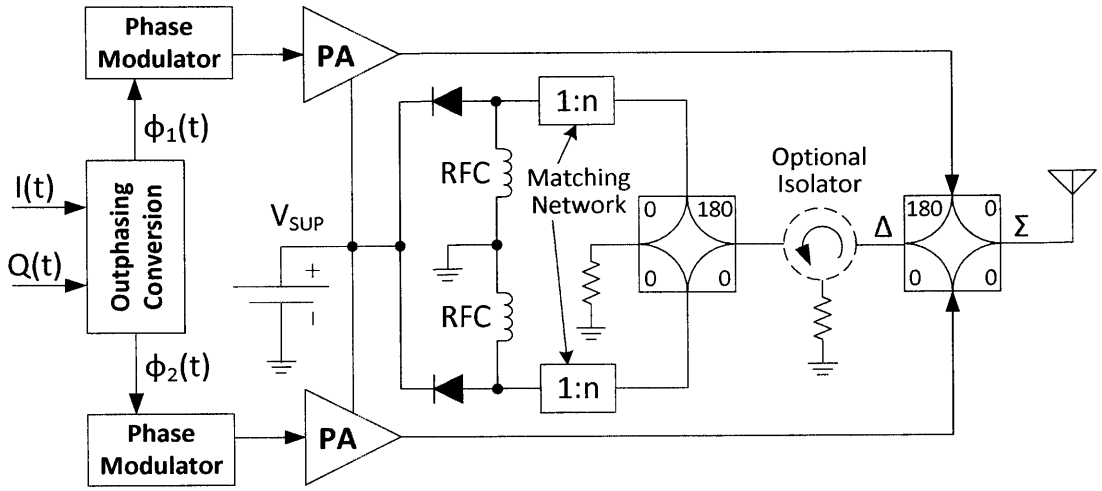


Figure 2-10: Outphasing power amplifier with power recycling network.

wire in a standard package for an IC. Flip-chip packages can be used to achieve lower package inductances, but at great additional cost.

2.5.2 Power Recycling

A power recycling technique was proposed in [32] and [33] as an attempt to enhance the power efficiency of the LINC architecture while still using an isolating combiner. The principle of the power reuse technique is shown in Figure 2-10, in which the isolation resistor is replaced with an RF-dc converter to recover the wasted power back to the power supply. While this approach has been shown to result in a significant increase in the overall efficiency, the implementation in [32] and [33] still suffers from excessive impedance variation at the isolation port and therefore incomplete isolation between the two PAs. This can lead to excessive signal distortion and lower efficiency or even breakdown in the PAs, particularly those sensitive to load impedance (e.g., class-E amplifiers). An additional isolator can be added between the isolation port and the RF-dc converter to reduce this effect; however, such isolators add additional insertion loss, area, and cost.

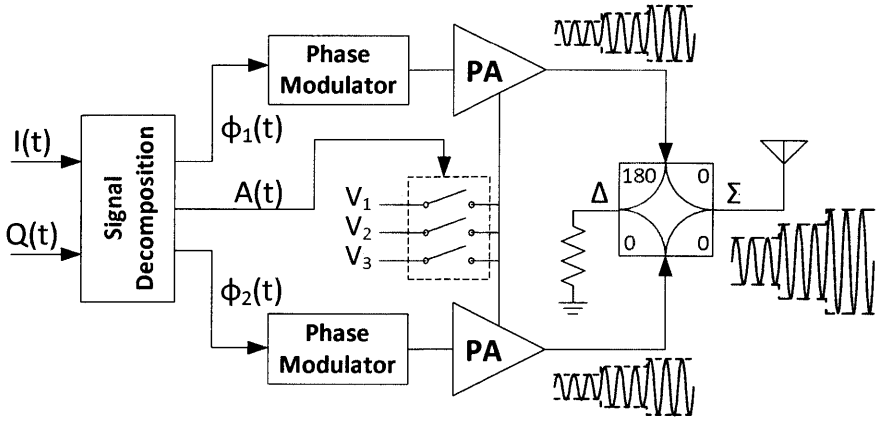


Figure 2-11: Multi-level LINC architecture. Three supply voltages are shown in the figure, but there can be any number of supply voltages greater than 1 for the ML-LINC system.

2.5.3 Multilevel LINC

A multi-level LINC (ML-LINC) transmitter, shown in Figure 2-11 was introduced in [34], which is a hybrid of polar and outphasing modulation. In the standard outphasing system, large outphasing angles must be used to create small output amplitudes, in which case most of the power from the PAs is sent to the isolation resistor and wasted as heat, resulting in low efficiency. ML-LINC reduces outphasing angles by adjusting the supply voltage according to the output amplitude. For example, if a small output amplitude is required, the supply voltage can be reduced so that the amount of power being delivered to the power combiner is reduced. This reduces the power being sent to the isolation resistor, improving the overall efficiency. Although the general idea behind the ML-LINC architecture has been proposed in the literature, a physical prototype with measurement results that prove the feasibility of the system has yet to be published.

2.6 Summary

In this chapter, we have described several transmitter architectures that have been developed to achieve high-efficiency power amplification. However, each different

system has a drawback. The outphasing architecture has a low efficiency at power backoff. The polar architecture has the problem of achieving high efficiency and wide modulation bandwidths simultaneously. The The pulse-width pulse-position modulated PA architecture cannot achieve a large amplitude dynamic range, so that sufficient linearity cannot be achieved in modern wireless communication standards. The Doherty architecture cannot support multi-band operation with greater than 35% fractional bandwidth. This thesis investigates techniques to overcome these problems and achieve high efficiency, high linearity, and wide bandwidth simulataneously. Two such techniques are proposed in this thesis, each of which will be described in detail in the next two chapters.

Chapter 3

Outphasing Energy Recovery Amplifier with Resistance Compression

As mentioned in the previous chapters, the outphasing architecture is a promising solution for breaking the tradeoff between efficiency and linearity in power amplifiers. However, the main problem with the outphasing architecture is the power wasted in the power combiner. One technique discussed in Section 2.5.2 that can alleviate this problem is to replace the isolation resistor in the conventional matched combiner with a RF-dc converter, to recover the normally wasted power back to the power supply. We call this architecture the outphasing energy recovery amplifier (OPERA). However, one problem with this system is that the impedance seen at the input of the RF-dc converter varies with input power (by Ohm's Law, $Z = V/I$, where the voltage V is approximately fixed by the DC power supply voltage), and it is difficult to maintain the correct impedance matching and isolation for the two outphased PAs. The result is degraded PA efficiency and linearity. In this chapter, we propose a solution to this problem, by using a resistance compression network (RCN) to significantly reduce the impedance variation of the RF-dc converter.

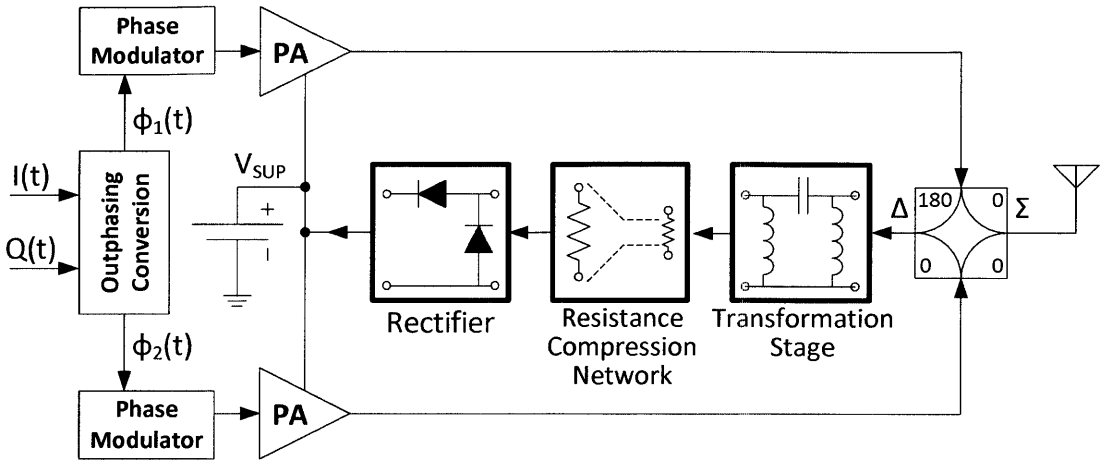


Figure 3-1: Outphasing energy recovery amplifier, utilizing a resistance compression network in the power recycling network.

3.1 Architecture Overview

The OPERA system shown in Figure 3-1 recovers the power normally wasted in the isolation resistor back to the power supply by replacing the resistor with a rectifier, which serves as the RF-dc converter. However, a rectifier alone is not enough because the equivalent input impedance of the rectifier varies with input power, as explained in detail in the next section. This impedance variation reduces the isolation between the two PAs, lowering the PA efficiency (and even possibly causing complete malfunction) and increasing signal distortion at the output. We use a resistance compression network (RCN) to reduce the rectifier impedance variation thereby mitigating this effect. As the final step, an impedance transformation stage is placed between the RCN and the combiner's isolation port to match the resistance-compressed rectifier impedance to the impedance required by the power combiner.

3.2 Resistance-Compressed Rectifier

Because the combiner requires a fixed resistance at the isolation port to ensure matching and isolation between the two outphased PAs, the RF-dc converter which recovers the wasted power should provide a constant resistive impedance at its input. A

purely resistive input impedance can be achieved with a variety of rectifier structures. One example of this kind of rectifier is an ideal half bridge rectifier driven by a sinusoidal current source of amplitude I_{in} and frequency ω_s, and having a constant output voltage V_{dc}, as shown in Figure 3-2. The voltage at the input terminals of the rectifier $v_x(t)$ will be a square wave having a fundamental component of amplitude $V_{x1} = (2V_{dc}/\pi)$ in phase with the input current $i_{in}(t)$. The electrical behavior at the fundamental frequency ω_s (neglecting harmonics) can be modelled as a resistor of value $R_{eq} = (2/\pi)(V_{dc}/I_{in})$. There are many other types of rectifier topologies that present the above-mentioned behavior (see, e.g., [35]); another is the resonant rectifier of [36,37]. Driving such a rectifier with a tuned network suppresses the harmonic content inherent in its operation and results in a resistive impedance characteristic at the desired frequency. This equivalent resistance can be represented by

$$R_{rect} = k_{rect}\frac{V_{dc}}{|I_1|} \tag{3.1}$$

where k_{rect} depends on the specific rectifier structure and $|I_1|$ is the fundamental component of the drive current. Ignoring harmonics, the power delivered to the rectifier is $P_{in} = \frac{1}{2}I_{in}^2 R_{rect}$, and we can write the rectifier impedance as

$$R_{rect} = \frac{(k_{rect}V_{dc})^2}{2P_{in}} \tag{3.2}$$

Equation (3.2) shows that the rectifier input impedance is inversely proportional to input power. Since the power delivered to the isolation port of the combiner in the LINC system varies with the outphasing angle between the two PAs, the impedance of a rectifier placed at the isolation port will vary as well. The result is incomplete isolation between the outphased PAs, leading to distortion and lower PA efficiency.

To see why it is important to present a fixed load resistance to a PA, we will consider the specific case of the class-E PA. Figure 3-3(a) shows the ideal voltage and current waveforms of the main transistor in a class-E PA [38]. Note that there is virtually no overlap between the voltage and current—either the voltage or the current

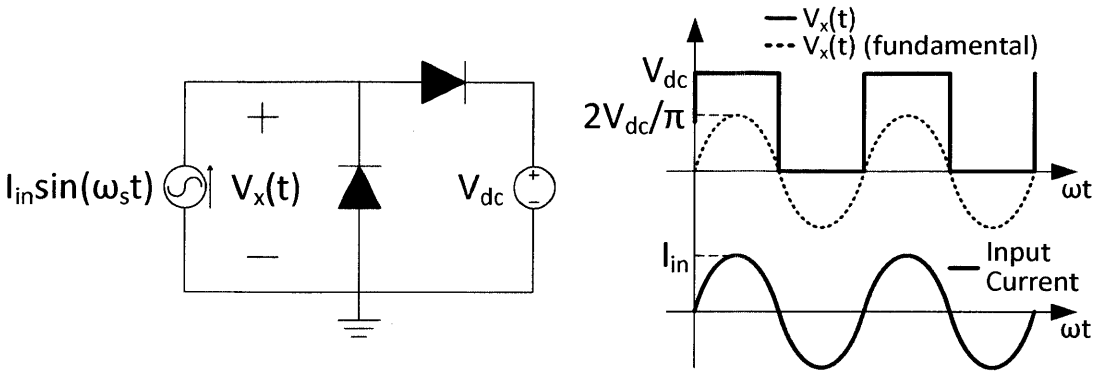
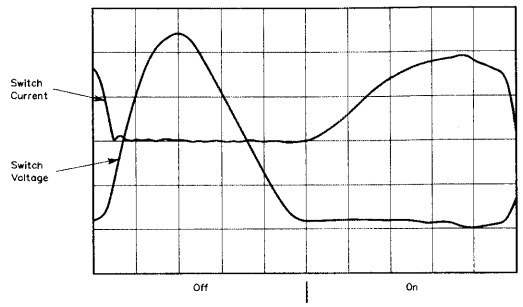


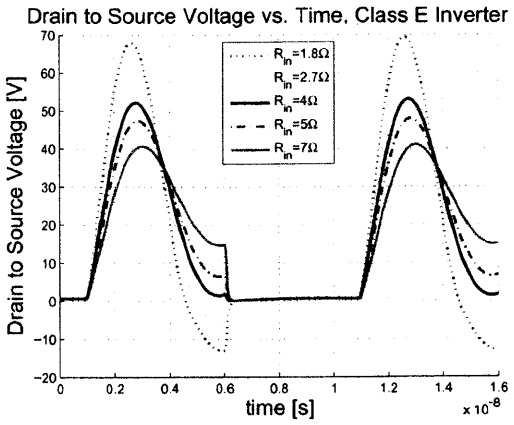
Figure 3-2: Ideal half-wave rectifier with constant voltage load and driven by a sinusoidal current source, along with characteristic waveforms. The input current and the fundamental of the input voltage are in phase.

is zero at any given time—and so there is virtually no power loss in the transistor, and so the theoretical efficiency is 100%. The fact that the voltage goes to zero before the current starts to go up is called "zero-voltage switching," or ZVS. Figure 3-3(b) shows what happens to the drain voltage as you vary the load resistance [37]. When the load resistance deviates from the ideal value (represented by the curve shown in blue), the transistor no longer exhibits ZVS, so that there will be some voltage/current overlap which will not only result in extra power dissipation, but also distortion in the PA output. This is the situation we would like to avoid. This example shows what happens when we vary the load resistance of a class-E PA, but similar distortion and efficiency loss will occur in any real PA. This is because for a non-isolating power combiner, both the real and imaginary parts of the load impedance will vary with the outphasing angle [8], which will affect the operating characteristics of any PA.

In order to improve the isolation between the two outphased PAs in the OPERA system, we introduce an RCN before the rectifier as shown in Figure 3-1 to reduce the impedance variation of the rectifer. As described in [37], an RCN can be combined with an appropriate set of rectifiers to yield an RF-dc converter with narrow-range resistive input characteristics. Figure 3-4 shows how a pair of rectifiers can be used with an RCN to build a rectifier system having a resistive input characteristic that varies little as the input power changes. The RCN applied here consists of two conju-



(a) Ideal Class-E Waveforms



(b) Class-E Drain Voltage with Varying Load

Figure 3-3: (a) Ideal voltage and current waveforms of the main transistor in a class-E PA. (b) The drain voltage waveform of a class-E PA for various values of load resistance.

gate reactances, each in series with one of two matched load resistances representing the equivalent resistances of two rectifiers as given by (3.2). The reactive branches are designed to have the specified reactance X at the designed operating frequency ω_s. It can be shown that at this frequency the input impedance of the network will be resistive with a value

$$R_{RCN} = \frac{X^2}{2R_{rect}}\left[1 + \left(\frac{R_{rect}}{X}\right)^2\right] \tag{3.3}$$

which provides compression of the matched load resistances R_{rect} about a center value of impedance X. Figure 3-5 shows the input resistance R_{RCN} of the RCN vs. load resistance R_{rect} for $X = 10\Omega$. The plot shows that the RCN compresses a 100:1 variation in load resistance to a much narrower range of 5:1.

For variations of R_{rect} over a range having a geometric mean of X (that is, $R_{rect} \in [(X/\sqrt{c_{rect}}), \sqrt{c_{rect}}X]$, where c_{rect} is the ratio of the largest to smallest resistances in the R_{rect} range), the corresponding ratio of the compressed R_{RCN} range can be shown to be

$$c_{RCN} = \frac{1 + c_{rect}}{2\sqrt{c_{rect}}} \tag{3.4}$$

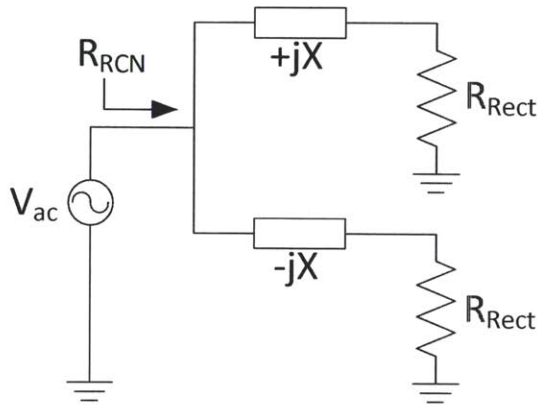


Figure 3-4: Two-element resistance compression network with reactive branches represented by impedances evaluated at the operating frequency.

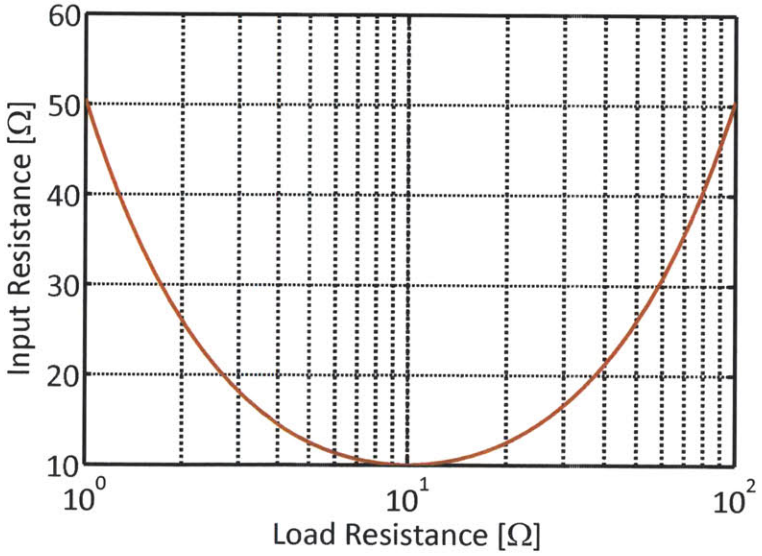


Figure 3-5: Input resistance R_{RCN} of the RCN shown in Figure 3-4 vs. load resistance R_{rect} for $X = 10\Omega$.

For example, a 10:1 variation in R_{rect} (c_{rect}=10) results in a modest 1.74:1 variation in R_{RCN}. Since R_{rect} is inversely proportional to P_{in} as shown in (3.2), this means a 10:1 variation in power delivered to the isolation port would result in only a 1.74:1 variation in isolation port resistance. This narrowed range of resistance will result in substantially improved isolation between the two outphased PAs, greatly improving their efficiency.

It should be noted that at sufficiently high output power levels (i.e., low power levels to the rectifers), the rectifier resistance can no longer effectively be compressed. The reason is that at low input power levels, the diodes will be unable to turn "on" and overcome the combination of supply voltage and the diode built-in potential. When the diodes turn "off", (3.1) and (3.2) no longer hold, and furthermore, the efficiency of the power recycling network drops considerably. However, this poses no serious problems. In this region of operation, most of the power from the PAs is delivered to the antenna load, and so the isolation port acts as a virtual open circuit. Therefore, the rectifier impedance and the efficiency of the recycling network do not matter.

3.3 Resistance Compresssion Network Bandwidth

Equation (3.3) shows how the RCN in Figure 3-4 reduces the impedance variation of two matched load resistances. However, this equation is only valid at a single operating frequency, when the two reactances in the RCN are equal in magnitude and opposite in sign. For many applications (e.g., wireless communications), wideband operation centered around a specified RF frequency is desired. Thus, it is important to consider the bandwidth limitations of the RCN.

Let us consider the case in which the reactances of the RCN in Figure 3-4 are implemented with a single inductor and capacitor. In this case, we can write the impedance of the RCN as

$$Z_{RCN} = \left(R + \frac{1}{j\omega C}\right) || \, (R + j\omega L) \tag{3.5}$$

$$= \left(R - jZ_o\frac{1}{\omega/\omega_o}\right) || \left(R + jZ_o\frac{\omega}{\omega_o}\right) \tag{3.6}$$

where C is the capacitance, L is the inductance, $Z_o = \sqrt{L/C}$ is the characteristic impedance of the tank (equal to the reactance X in Equation (3.3)), and ω/ω_o is the ratio of the driving frequency to the center frequency. It can be seen that Equation (3.6) reduces to Equation (3.3) when $\omega = \omega_o$. When the frequency deviates from the center frequency, one of the two branches in the RCN will dominate over the other, such that the RCN impedance is no longer purely resistive but also either capacitive or inductive, depending on the direction of the frequency deviation and the value of the load resistance. When such an impedance is presented to a PA, the result is degraded linearity and efficiency.

Figure 3-6 shows the RCN impedance vs. load resistance for a frequency deviation of $\pm 5\%$ of the center operating frequency. This represents a bandwidth of 10% of the center frequency, which is wide enough for most applications. Over this frequency range, the figure shows that the RCN still effectively compresses the load resistance over a large range, with only a modest reactive component in the total impedance. For a 10:1 load resistance variation, the maximum deviation in impedance phase is only $\pm 7.5^o$ with virtually no deviation in impedance magnitude. This amount of impedance variation should be suitable for most applications.

It should be noted that multiple RCNs can be cascaded to achieve even higher levels of resistance compression to further increase the bandwidth of the RCN for a given RCN impedance variation and load resistance variation [37]. For example, the impedances Z_{RCN} in Figure 3-4 can each represent the load impedance of subsequent RCN stages. An "N-stage" compression network would thus have 2^N load resistances that vary in a matched fashion. However, the efficacy of many-stage compresssion is likely to be limited by a variety of practical considerations.

The analysis presented here assumed ideal load resistances with no reactive component. The situation is more complicated when the load resistances are rectifiers, since the rectifier impedance is not always purely resistive in practical implementations, where the parasitic diode capacitance must be taken into account. The effect

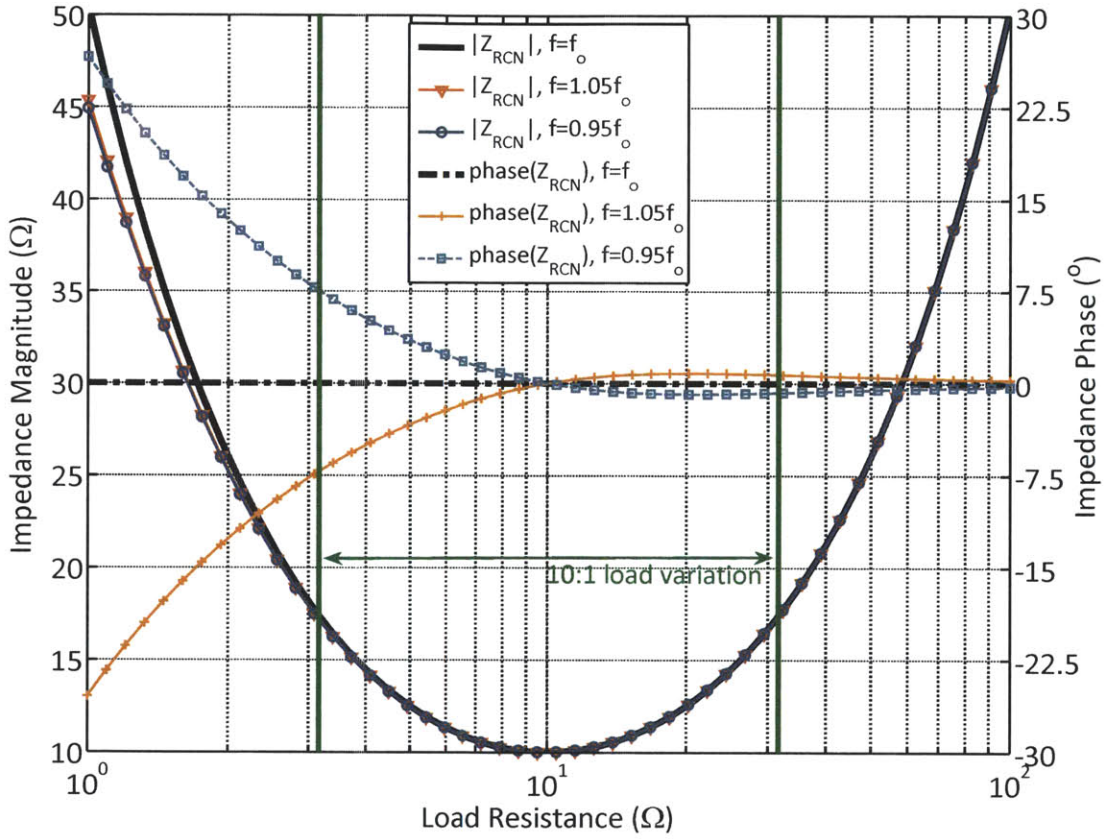
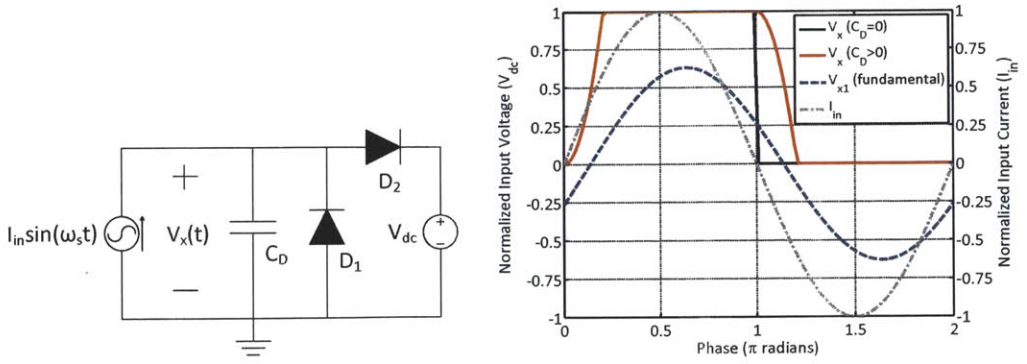


Figure 3-6: RCN impedance vs. load resistance for a frequency deviation of $\pm 5\%$ of the center operating frequency. $Z_o = X = 10\Omega$.



(a) Half-wave rectifier with parasitic capacitance

(b) Time-domain input voltage and current

Figure 3-7: Half-wave rectifier with parasitic capacitance and driven by a sinusoidal current source, along with characteristic waveforms.

of parasitic capacitance on the rectifier impedance will be considered in next section.

3.4 Rectifier Impedance with Parasitic Capacitance

In Section 3.2, it was shown that the ideal half-wave rectifier has a purely resistive input impedance given by (3.1). However, this is not true if the parasitic diode junction capacitance is taken into account [39]. Figure 3-7(a) shows the half-wave rectifier with parasitic capacitance C_D, representing the total equivalent capacitance of the two diodes. The capacitance C_D prevents the input voltage V_x from changing abruptly, resulting in the waveforms shown in Figure 3-7(b). The figure shows that the fundamental component of the input voltage is no longer in phase with the input current, resulting in a rectifier impedance that is no longer purely resistive but also partially capacitive, as one might expect. This is undesirable because the PA efficiency and linearity degrade when the load impedance is not purely resistive. The RCN can compensate for this by providing a certain amount of "phase compression" [37], but only to a limited extent. The rectifier impedance in the presence of parasitic capacitance can be determined by calculating the Fourier series coefficients of the input voltage waveform V_x.

Referring to Figure 3-7(b), there are four distinct time intervals of the V_x waveform

that we must describe in order to do the Fourier analysis. During the first time interval, both diodes are off and the capacitance C_D is being charged by the input current source. During this time, the input voltage V_x is given by

$$V_x(t) = \frac{I_{in}}{\omega_s C_D}\left[1 - \cos\left(\omega_s t\right)\right] \tag{3.7}$$

where ω_s is the frequency of the input current source. This time interval ends when $V_x = V_{dc}$, at which point the diode D_2 turns on. This occurs at time $u = \omega_s t$ given in radians by the following equation:

$$\cos(u) = 1 - \frac{\omega_s C_D V_{dc}}{I_{in}} = 1 - \frac{V_{dc}}{X_C I_{in}} \tag{3.8}$$

where X_C is the reactance of C_D at ω_s. When the polarity of the input current transitions from positive to negative, both diodes are off again and the current source discharges the capacitance C_D until $V_x = 0$ and diode D_1 turns on. During this time, V_x is given by

$$V_x(t) = V_{dc} - \frac{I_{in}}{\omega_s C_D}\left[1 - \cos\left(\omega_s t - \pi\right)\right] \tag{3.9}$$

This time interval ends at time $\omega_s t = \pi + u$, where u is the same as in Equation (3.8). Now that we have defined the input voltage V_x over the entire period, we can find the Fourier series coefficients of V_x at the fundamental frequency ω_s to be

$$a_{x1} = \frac{2}{\pi} V_{dc}\left[-\frac{u}{2\alpha} + \left(\frac{1}{\alpha} - 1\right)\sin(u) - \frac{1}{4\alpha}\sin(2u)\right] \tag{3.10}$$

$$b_{x1} = \frac{2}{\pi} V_{dc}\left[\frac{3}{4\alpha} + \left(1 - \frac{1}{\alpha}\right)\cos(u) + \frac{1}{4\alpha}\cos(2u)\right] \tag{3.11}$$

where $\alpha = V_{dc}/(X_c I_{in})$ and a_{x1} and b_{x1} represent the cosinusoidal and sinusoidal components (respectively) at the fundamental frequency (that is, $V_{x1} = a_{x1} - jb_{x1}$). Using these equations together with Ohm's Law $Z = V/I$, we can calculate the rectifier impedance as follows:

$$|Z_{rect}| = \frac{1}{I_{in}}\sqrt{a_{x1}^2 + b_{x1}^2} \tag{3.12}$$

$$\angle(Z_{rect}) = -\arctan\left(\frac{b_{x1}}{a_{x1}}\right) - \frac{\pi}{2} \tag{3.13}$$

Figure 3-8 shows the impedance of the half-wave rectifier with parasitic capacitance vs. the parameter $\alpha = V_{dc}/(X_c I_{in})$ which we have defined (similar to "reactance factor" in low-frequency rectifiers [40]). If we substitute this parameter into Equation 3.8, we can see that the diodes will no longer turn on when $\alpha > 2$, in which case the rectifier impedance will look purely capacitive with reactance X_C. This is evident in Figure 3-8, which shows that as α increases from 0 to 2, the rectifier impedance transitions from purely resistive to purely capactive, as expected. Thus, a small value of α is desired to maintain a resistive rectifier impedance.

There are four parameters which determine the value of α: the operating frequency ω_s, the diode capacitance C_D, the input current I_{in}, and the dc output voltage V_{dc}. To minimize α, I_{in} should be maximized while ω_s, C_D, and V_{dc} should be minimized. However, these parameters are subject to several constraints. One constraint is the rectifier efficiency: because real diodes have a nonzero forward voltage drop, decreasing V_{dc} will lower the efficiency, and so maintaining a specified efficiency will set a lower bound on V_{dc}. Another constraint is the maximum input power to the rectifier, which will determine the maximum value of I_{in} for a given V_{dc}. Finally, once the values of V_{dc} and $I_{in,max}$ are determined, the worst-case value of α will be determined by the operating frequency ω_s, the diode capacitance C_D, and the input power variation as given by the following equation:

$$\alpha_{max} = \frac{\omega_s C_D V_{dc}}{I_{in,min}} = \omega_s C_D V_{dc} \frac{c_{power}}{I_{in,max}} \tag{3.14}$$

where c_{power} is the ratio of the largest to smallest input power levels going into the rectifier. Thus, it is important to keep both the diode parasitic capacitance C_D and the operating frequency ω_s as small as possible. Unfortunately, this becomes difficult if high-frequency operation is required. One may conclude that the ratio $I_{f,av}/C_T$ (rated current to device capacitance) is an important figure of merit for a diode in this application. A further figure of merit (having units of frequency) is $I_{f,av}/(V_{D,ON}C_T)$,

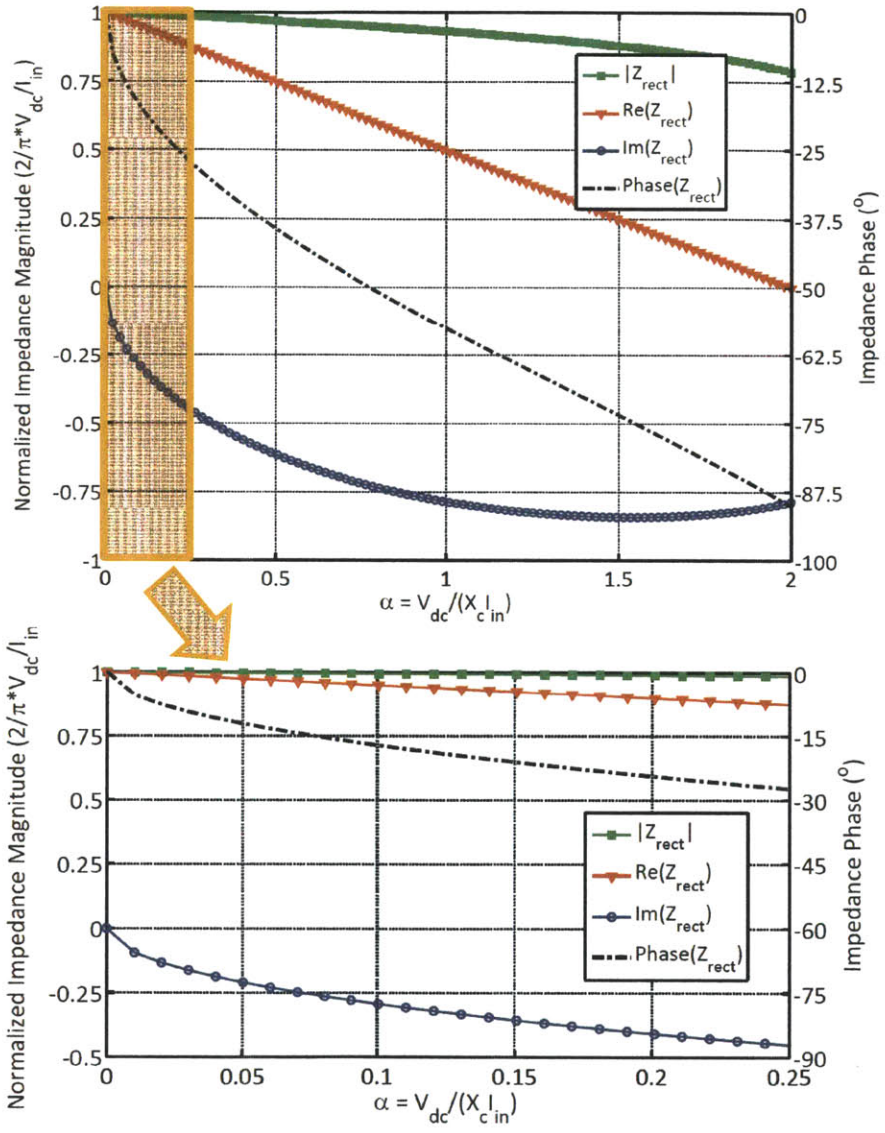


Figure 3-8: Impedance of half-wave rectifier with parasitic capacitance vs. parameter $\alpha = V_{dc}/(X_c I_{in})$. As α increases, the impedance looks increasingly capacitive.

where $V_{D,ON}$ is the forward voltage drop of the diode.

One way to overcome this problem in high-frequency applications is to use a resonant rectifier topology [36, 37, 41, 42], which reduces the effect of the parasitic capacitance by removing the diode D_1 in Figure 3-7(a) and replacing it with an inductor to partially tune out the parasitic capacitance (as well as provide a path for DC current). In this case, the bandwidth of the rectifier will be limited by the network Q of the RLC tank formed by inductor, diode capacitance, and equivalent rectifier resistance.

3.5 Theoretical Efficiency

The total efficiency of the OPERA system is given by

$$\eta_{tot} = \frac{P_{out}}{P_{dc} - P_{rec}} \tag{3.15}$$

where P_{out} is the power delivered to the antenna load, P_{dc} is the dc power delivered to the PAs from the power supply, and P_{rec} is the power sent back to the power supply from the RF-dc converter placed at the combiner's isolation port. The total power available from the PAs is

$$P_{avail} = \eta_{PA} P_{dc} = P_{out} + P_{iso} \tag{3.16}$$

where η_{PA} is the PA efficiency and P_{iso} is the power delivered to the isolation port. Using (3.16), we can write P_{rec} as

$$P_{rec} = \eta_{rec} P_{iso} = \eta_{rec} \left(P_{avail} - P_{out} \right) \tag{3.17}$$

$$= \eta_{rec} \left(\eta_{PA} P_{dc} - P_{out} \right) \tag{3.18}$$

where η_{rec} is the energy recovery efficiency. Substituting (3.18) into (3.15), we can write the efficiency of the OPERA system as

$$\eta_{tot} = \frac{P_{out}}{P_{dc} - \eta_{rec}(\eta_{PA}P_{dc} - P_{out})} \tag{3.19}$$

$$= \frac{p}{\frac{1}{\eta_{PA}} - \eta_{rec}(1-p)} \tag{3.20}$$

where $p = P_{out}/P_{avail}$ is the normalized output power. To account for any insertion loss in the power combiner, it is sufficient to replace η_{PA} with $\eta_{PA}\eta_{comb}$, where η_{comb} is the efficiency of the power combiner.

Figure 3-9 shows the predicted system efficiency in a LINC system with and without energy recovery. For illustrative purposes, the power amplifiers in the system are assumed to be 100% efficient, with no insertion loss in the combiner. As can be seen, the overall system efficiency is significantly enhanced by recycling the "wasted" power delivered to the isolation port of the combiner, and is strongly influenced by the efficiency of the energy recovery network, as one might expect. The improvement in overall average efficiency will depend on probability distribution of the signal being transmitted.

Another important metric is the total power dissipation of the system, P_{diss}, which represents the total wasted power in the system that is not sent to the output. The total dissipated power is the power delivered to the PAs from the power supply (P_{dc}), minus the output power (P_{out}), minus the power sent back to the power supply from the energy recovery network (P_{rec}):

$$P_{diss} = P_{dc} - P_{out} - P_{rec} \tag{3.21}$$

$$= P_{dc} - P_{out} - \eta_{rec}(\eta_{PA}P_{dc} - P_{out}) \tag{3.22}$$

We can normalize P_{diss} to P_{dc} to obtain the following expression:

$$\frac{P_{diss}}{P_{dc}} = 1 - \eta_{PA}p - \eta_{PA}\eta_{rec}(1-p) \tag{3.23}$$

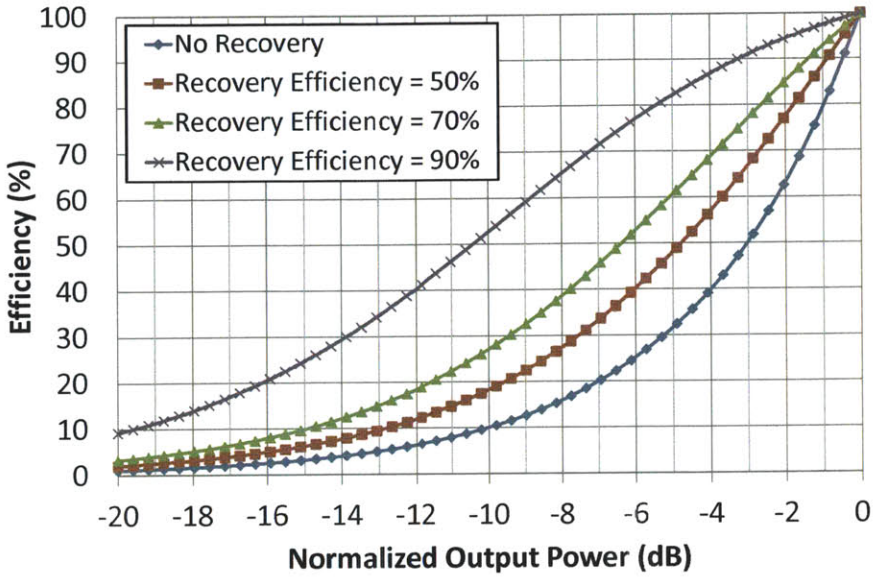


Figure 3-9: Theoretical OPERA efficiency as a function of normalized output power, showing the effect of the energy recovery network efficiency. The PAs are assumed to be 100% efficient, with no insertion loss in the power combiner.

p is the output power normalized to the available power being sent from the PAs to the power combiner, as defined previously.

Figure 3-10 plots P_{diss}/P_{dc}, the total power dissipation normalized to the total dc power sent to the PAs from the power supply, as a function of normalized output power. Again, the PAs are assumed to be 100% efficient, with no insertion loss in the power combiner. It can be seen that there is a significant reduction in the power dissipation when energy recovery is used, with the power savings directly proportional to the energy recovery efficiency. Even with only 50% efficiency in the energy recovery network, the reduction in the power loss compared to the standard LINC system can be substantial.

The efficiency of the power recycling network will depend on several factors. As mentioned in the previous section, the value of the power supply voltage in relation to the forward voltage drop of the diode used in the rectifier will heavily influence the recovery efficiency. Other sources of loss include the series resistance of the diodes and the quality factors of the other passive components used in the RCN and impedance transformation network. Given the importance of the energy recovery efficiency on

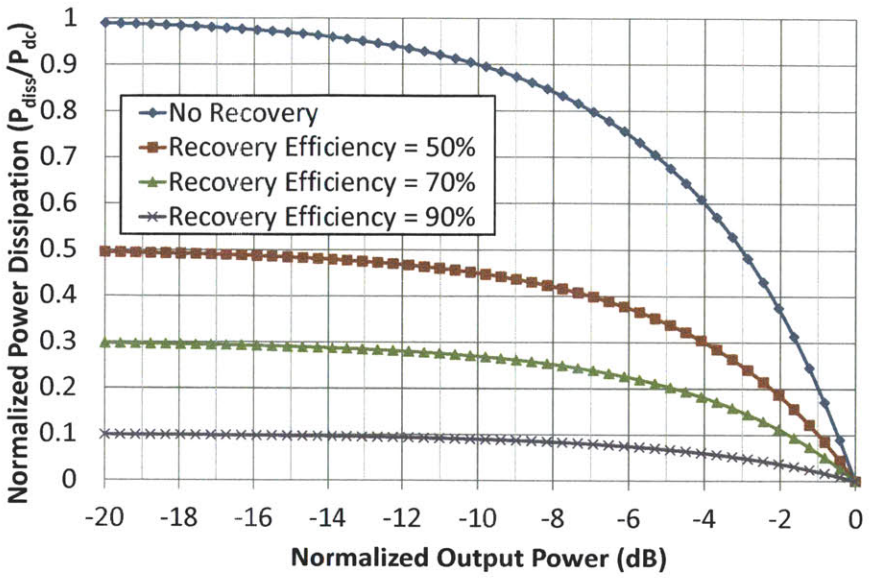


Figure 3-10: Theoretical OPERA power dissipation normalized to the total dc power sent to the PAs from the power supply, as a function of normalized output power, with the efficiency of the energy recovery network as a parameter. The PAs are assumed to be 100% efficient, with no insertion loss in the power combiner.

the overall system efficiency, the fact that the resistance-compressed rectifier obviates the need for an additional isolator between the power recycling network and the combiner's isolation port is a key advantage of the OPERA system presented in this paper, because the loss introduced by the isolator is removed.

Figure 3-11 compares the theoretical efficiency of the OPERA system with 80% recovery efficiency to that of other PA architectures. The OPERA efficiency is shown to be significantly higher than either class-A or class-B PAs. This can be attributed to the higher efficiency of the switched-mode PAs used in the LINC system, as well as enhanced efficiency due to the energy recovery network. It can also be seen that the OPERA system compares favorably to the Chireix outphasing PA (whose efficiency curve we have calculated from [8] for a given reactive compensation) when the entire power range is considered. This is due to the fact that the Chireix combiner can only be tuned for maximum efficiency around a single output power. It should also be noted that the Chireix combiner is nonisolating, making it generally incompatible with class-E PAs which have a high sensitivity to load variation [43]. Thus, the

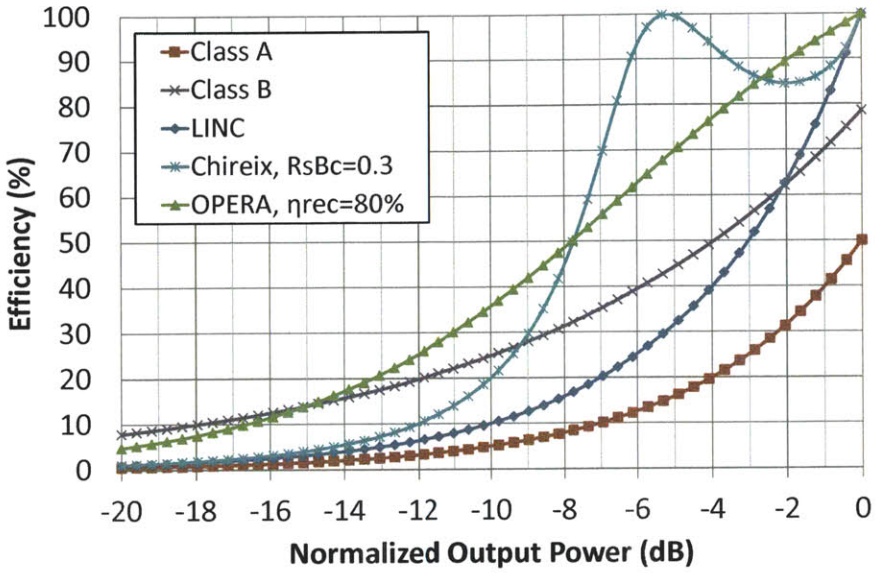


Figure 3-11: Comparison of theoretical OPERA efficiency to that of other PA architectures. Note that the Chireix efficiency curve does not reflect the efficiency degradation that will occur due to the widely varying impedance presented to the outphased PAs as the output power varies.

Chireix system must employ other PAs such as class-D, class-F[1], or saturated class-B which have generally lower efficiency. Furthermore, since the Chireix combiner presents a much wider impedance variation to the outphased PAs than the combiner in the OPERA system, both the linearity and PA efficiency will degrade significantly more. For these reasons, the efficiency of the Chireix system will be even lower than suggested in Figure 3-11.

3.6 48-MHz Prototype

To demonstrate the feasibility of the OPERA system, a prototype was designed and implemented with discrete components at an operating frequency of 48 MHz. Figure 3-12 shows a circuit schematic of the prototype OPERA system.

Figure 3-13 shows the circuit schematic of the power amplifiers used in the OPERA

[1]Class-F PAs have a theoretical efficiency of 100%, but only if all odd harmonics are tuned in the output resonant filter [44]. This is difficult to achieve in practical implementations. For example, with only the third harmonic tuned, the theoretical efficiency reduces to 88%.

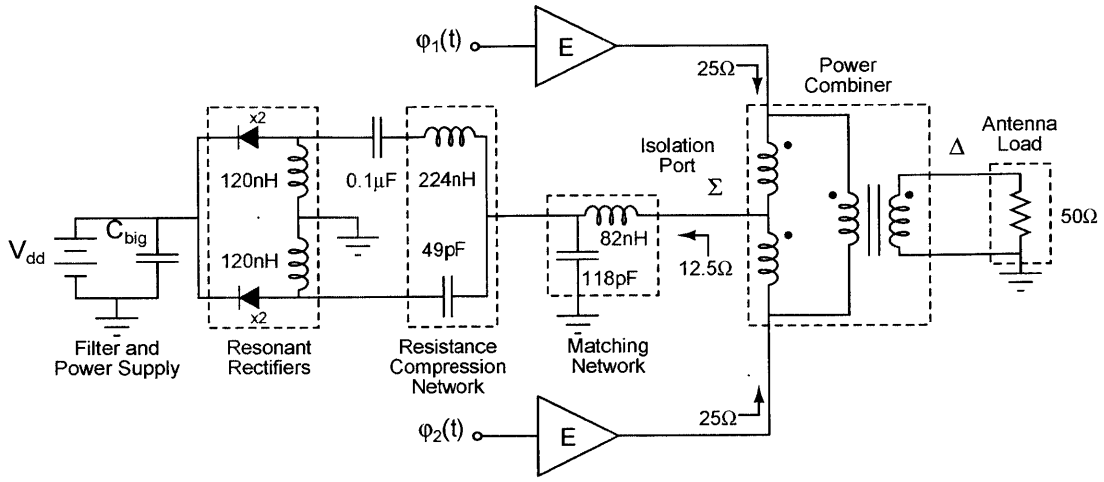


Figure 3-12: Prototype OPERA system with resistance-compressed rectifier for energy recovery. Each rectifier branch is implemented with a pair of paralleled SS16 Schottky diodes. The impedance at each port of the power combiner that is required for matching and isolation is also indicated.

prototype. Each PA is class-E, using an off-the-shelf RF power MOSFET, the ST Microelectronics PD57060, and designed for a supply voltage of 12 V with 10-W output power. Thus the maximum output power of the prototype outphasing PA is 20 W. Four parallel Fairchild NC7ZW04 CMOS inverters provide the gate drive, and operate with a 5-V supply voltage. All inductors used in the prototype are air core spring inductors from Coilcraft.

The power combiner used in the OPERA prototype consists of two 1:1 transformers, each implemented with 18-AWG 5-turn bifilar windings on a Ferronics Cobalt-Nickel ferrite toroid core ("K" material with 0.9-in outer diameter). The antenna load is connected to the difference port, while the power recycling network is connected to the summing port, which is the isolation port in this configuration. Figure 3-12 shows the impedance at each port that is required for matching and isolation between the two outphased PAs. Fixing the antenna load at 50 Ω, the required impedances at the other ports can be found through even/odd (common/difference) mode analysis [45]. The prototype was also designed with the capability to switch the isolation port load between a fixed resistance and the power recycling network, in order to compare the standard LINC system shown in Figure 2-1 with the OPERA system.

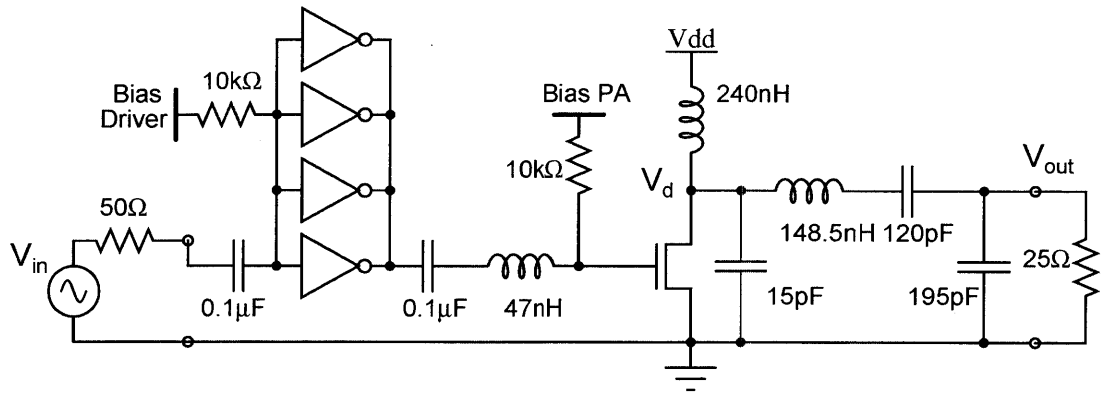


Figure 3-13: Circuit schematic of the class-E power amplifier used in the OPERA prototype.

The rectifiers in the power recycling network in Figure 3-12 are implemented with the resonant rectifier topology used in [36,37], in which an inductor resonates with the diode capacitance so that the input looks resistive at the fundamental frequency. The resonant inductor also provides a path for dc current. Resonant rectifiers have several advantages over classical hard-switched (square-wave) rectifiers, including lower component count, lower parasitics, and higher efficiency [42]. The rectifiers use On-Semiconductor SS16 1-A, 60-V Schottky diodes (two in parallel for each of the two rectifiers).

The conjugate reactances which comprise the RCN are implemented with a single capacitor and inductor. Alternatively, each reactance can be implemented with a series combination of an inductor and an capacitor as in [37] to provide additional filtering of the voltage harmonics created by the rectifiers, but it was found that the preceding matching network was sufficient for this purpose. The resistance-compressed rectifier was designed to keep the rectifiers operational over an input power range of 2–20W, a 10:1 ratio in power. This corresponds to an impedance variation of 1.74:1 at the combiner's isolation port, as described in Section 3.2. Besides providing harmonic filtering, the matching network transforms the compressed rectifier impedance to the level required by the power combiner.

Figure 3-14 shows a photograph of the prototype OPERA system.

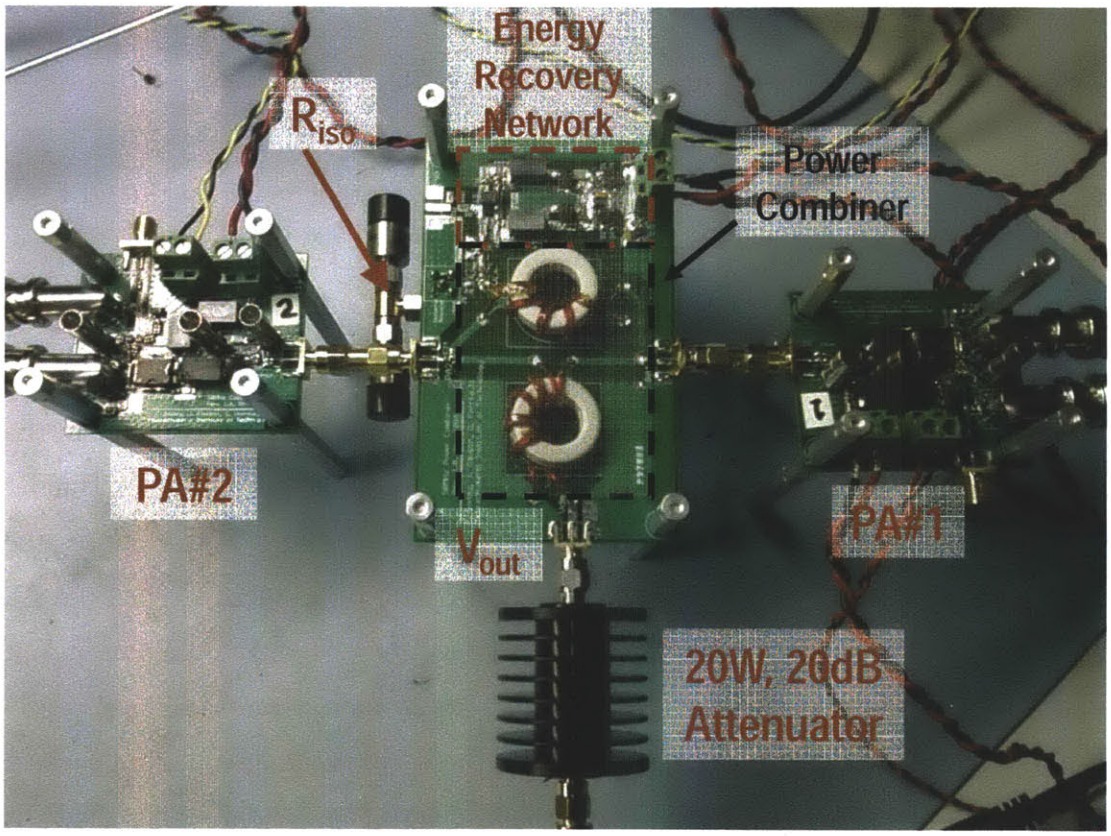


Figure 3-14: Photograph of the prototype OPERA system.

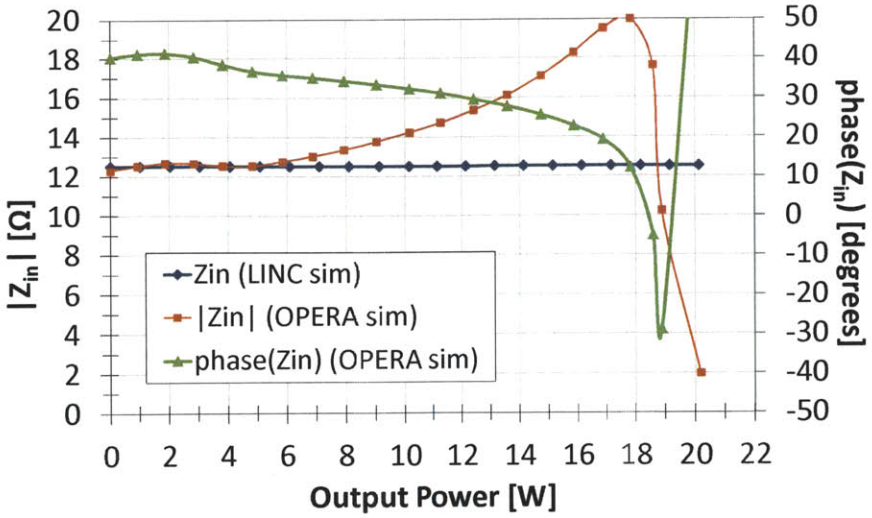


Figure 3-15: Simulated isolation port impedance vs. output power in the OPERA prototype. The desired isolation port impedance is also shown for reference.

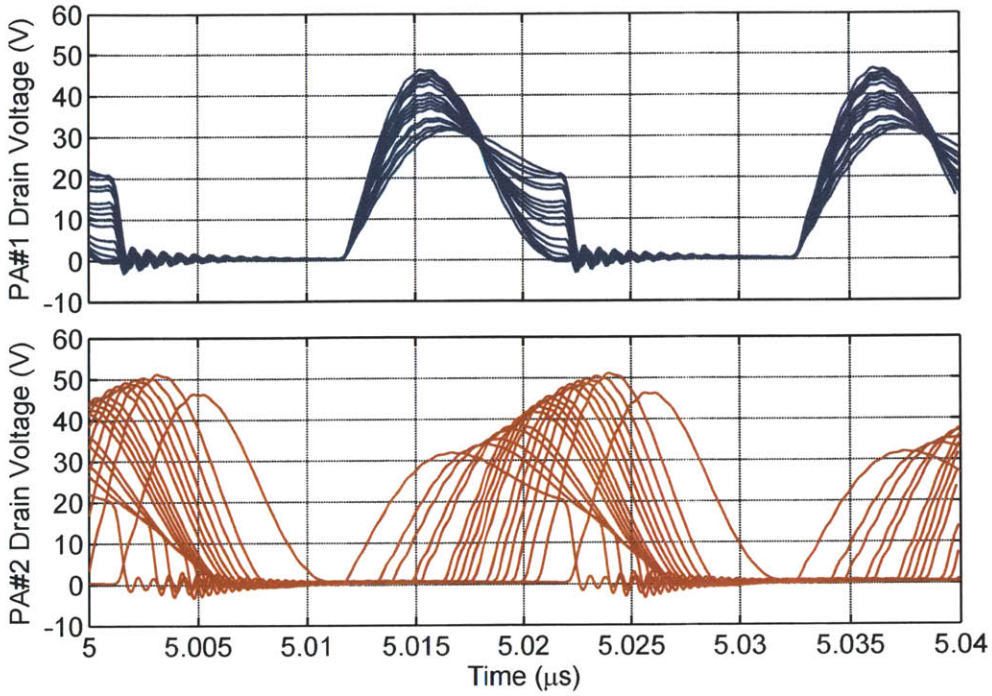
3.7 Measurement Results and Discussion

Figure 3-15 shows the simulated isolation port impedance vs. output power in the OPERA prototype, measured as the ratio of the voltage and current at the fundamental of the operating frequency. The plot shows that the RCN compresses the impedance at the isolation port to a range between 12.5 Ω and 20 Ω from 0–18W output power. Since the maximum output power of the system is 20 W, an output power range of 0–18W corresponds to roughly 2–20-W input power to the resistance-compressed rectifier, a 10:1 variation (note that this is only an approximation because the power available from the PAs varies as the load impedance varies). Thus the RCN compresses a 10:1 impedance variation into a 1.6:1 variation. This agrees well with the theoretical prediction of 1.74:1 calculated in Section 3.2. Note that at the highest output powers, the isolation port impedance drops considerably. This is because in this case very little power is delivered to the rectifier and the diodes can no longer turn "on." However, as stated previously, this should not degrade the overall system efficiency and linearity because at these power levels most of the power from the PAs is delivered to the antenna load, and so the isolation port impedance has little effect.

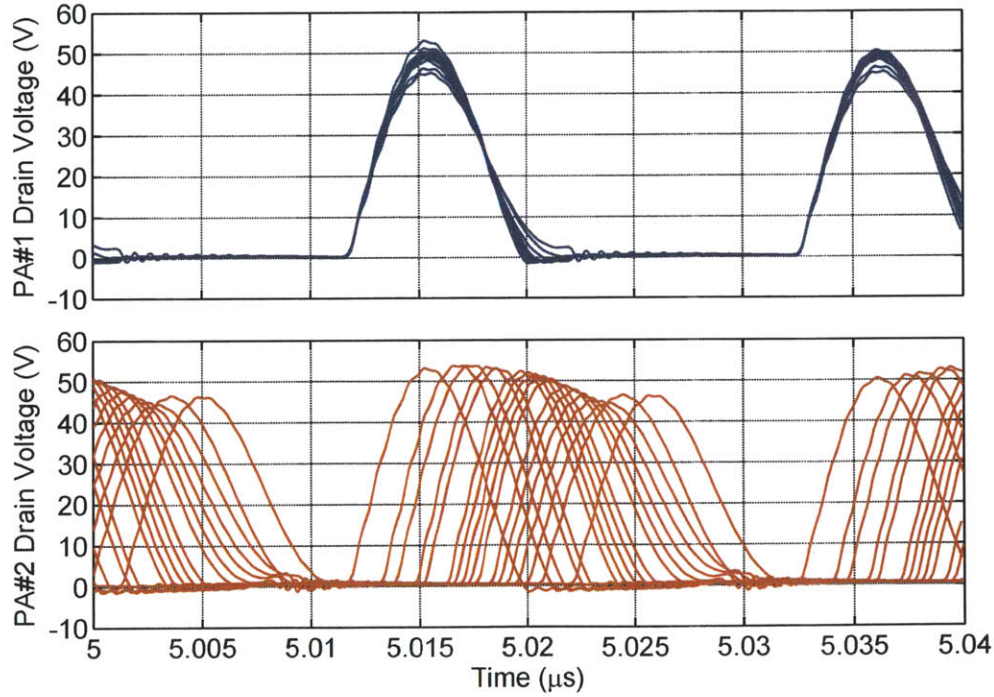
Figure 3-16 shows simulated PA drain voltages (denoted by V_d in Figure 3-13) in the OPERA prototype with and without the RCN, for various outphasing angles and output powers. The waveforms show that the RCN helps to maintain zero-voltage switching (ZVS) in the class-E amplifiers, an important characteristic for achieving high efficiency. This demonstrates that the appropriate load impedance at the PA outputs is being maintained over the entire range of outphasing angles. It should be noted that the experimental system was essentially unuseable without inclusion of the resistance compression network, owing to misoperation of the (load-sensitive) class-E amplifiers.

Figure 3-17 shows both the simulated and measured system efficiency of the OPERA prototype vs. output power, obtained by sweeping the outphasing angle from $-180°$ to $+180°$. The system efficiency is defined as $P_{out}/(P_{DC} + P_{pre})$, where P_{out} is the output power, P_{DC} is the total power dissipated from the 12-V PA power supply (accounting for any power recycled from the energy recovery network), and P_{pre} is the total power dissipated from the 5V power supply for the PA gate drivers. For the purpose of comparison, the prototype was tested both with the isolation port connected to a fixed resistance (the standard LINC system) and to the power recycling network (the OPERA system). We can see that the simulated and measured efficiencies are in close agreement, and that the system efficiency is significantly enhanced when the power recycling network is used. The double curves in the case of the measured values are due to the mismatch between the two PAs in the prototype, resulting in different results for positive and negative outphasing angles. The prototype OPERA system achieves a peak power of 20.8 W, with a corresponding peak power-added efficiency of 82.9%.

Figure 3-18 shows the simulated PA and power recycling efficiency vs. output power for the OPERA prototype. The setup of the OPERA prototype was such that direct measurement of the power recycling efficiency was difficult, so that only the simulated results are shown here. The plot shows that the efficiency of the energy recovery network remains above 87% for output powers up to 90% of the maximum. For output powers higher than this, the power going into the rectifiers is too low



(a) Energy Recovery without RCN



(b) Energy Recovery with RCN

Figure 3-16: Simulated PA drain voltages in the OPERA prototype with and without the resistance compression network, for various outphasing angles and output powers.

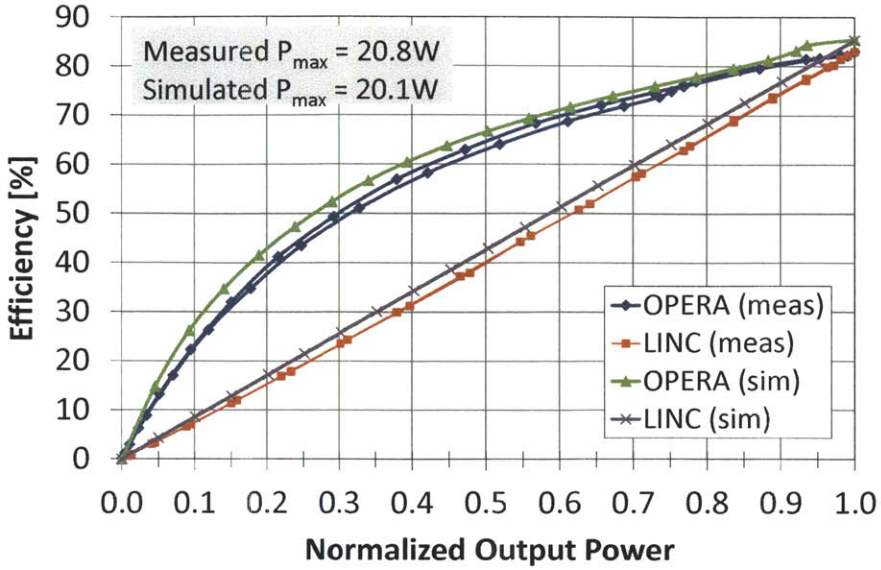


Figure 3-17: System efficiency vs. output power for the OPERA prototype.

to turn the diodes "on," resulting in a significant drop in the recovery efficiency. Also note that the PA efficiency varies with output power in the case of the OPERA system. This is due to the varying load impedance of the energy recovery network as the output power is varied. Although the RCN greatly reduces this impedance variation, some variation is still present, resulting in degraded PA efficiency.

Figure 3-19 shows both the simulated and measured dissipated power vs. output power in the LINC prototype with and without energy recovery. Again, we can see that the simulated and measured efficiencies are in close agreement, with the measured dissipated power somewhat higher due to the lower measured efficiency. The peak dissipated power of the OPERA prototype is reduced from 28.3 W without energy recovery to 7.3 W with energy recovery. This represents an energy savings of up to 4x when the OPERA system is used. As stated previously, the actual amount of energy saved for a given application will depend on probability distribution of the signal being transmitted. The energy savings has the additional benefit of significantly reducing the requirements of the heatsink used for a given system as well as the cost of the energy drawn from the power grid.

Figure 3-20 shows the measured amplitude and phase of the output voltage at

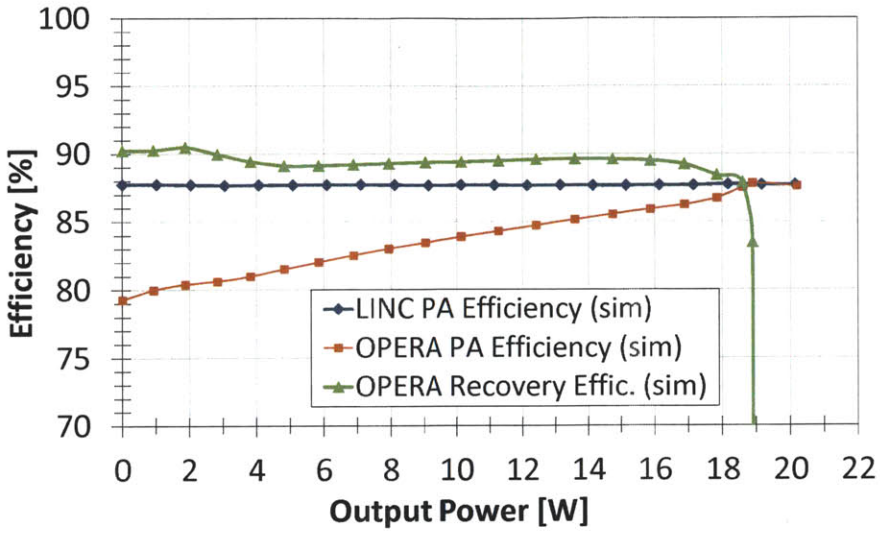


Figure 3-18: Simulated PA and power recycling efficiency for the OPERA prototype.

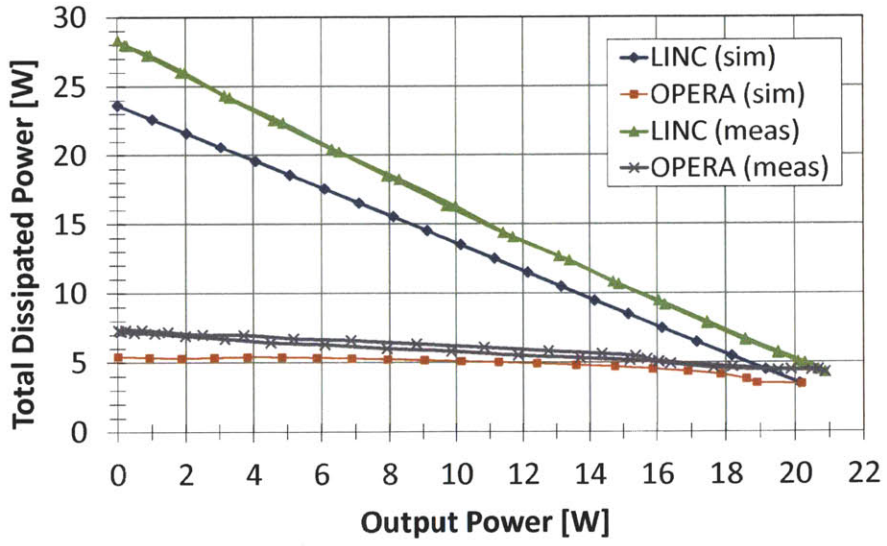
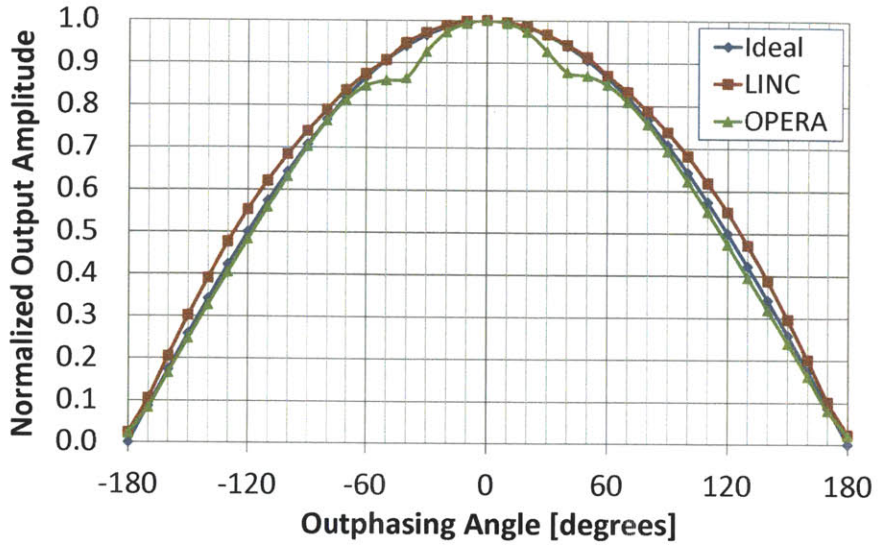


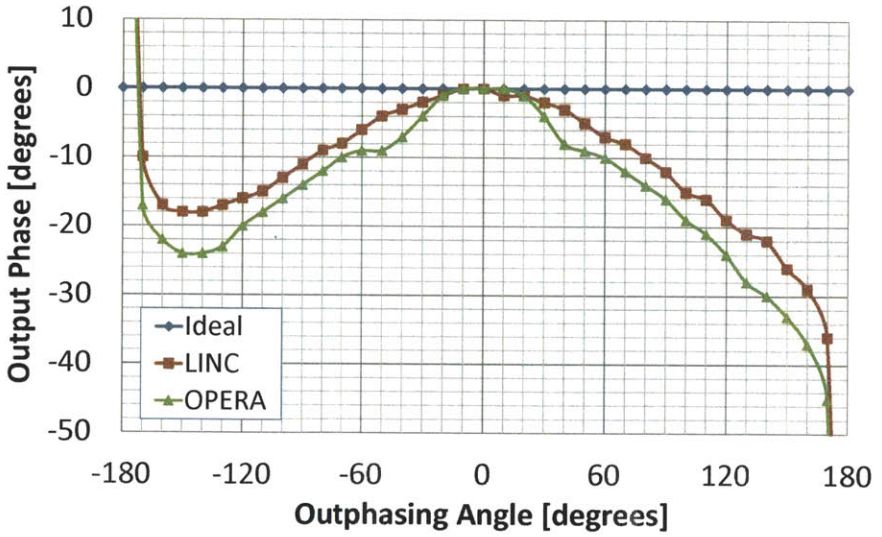
Figure 3-19: Total dissipated power vs. output power in the OPERA prototype with and without energy recovery.

the fundamental of the RF output frequency vs. the outphasing angle. The phase measurements are normalized to the output phase at maximum output power. The distortion present in both the LINC and OPERA cases is most likely due to the PA mismatch in the prototype. In another experiment, we measured the output power mismatch between the two PAs to be about 6%. Additionally, when energy recovery is used, we can see a significant distortion in the output for amplitudes between 85%–95% of the maximum. As stated before, this is due to the fact that at higher output powers, very little power is delivered to the rectifiers and the diodes can no longer turn "on", and so the rectifier impedance can no longer be effectively compressed, resulting in distortion. This can also be understood by examining Figure 3-15, which shows that in this operating region, the isolation port impedance deviates the most from the nominal value. It should be noted that for amplitudes greater than about 95% of the maximum, the distortion is reduced significantly. This is because in this case, almost all the power from the PAs is delivered to the antenna load, and so the isolation port becomes a virtual open circuit and its impedance has no effect. The static distortion exhibited by the OPERA prototype both with and without energy recovery can be significantly reduced with standard digital predistortion (PD) techniques [46]. In this paper, a simple lookup table constructed from the data in Figure 3-20 was sufficient to correct for this distortion.

To demonstrate the linearity of the OPERA system, we tested the prototype with a 50-kHz 16-QAM signal filtered with a raised cosine filter, resulting in a signal PAPR of 6.5 dB. A block diagram of the testbench is shown in Figure 3-21. The in-phase/quadrature (IQ) input sequences, including the signal processing for the outphasing conversion, are created in MATLAB and uploaded into the internal memories of two Tektronix AFG3102 arbitrary function generators (AFGs). The signal processing incorporates the optimal outphase assignment scheme described in [1, 47] which substantially reduces the amplitude variation of the two outphased signals $S_1(t)$ and $S_2(t)$. Each AFG feeds its baseband IQ outputs to the IQ inputs of an Agilent 4430 series vector signal generator (VSG) configured as an IQ modulator, which upconverts the baseband data to an RF carrier frequency of 48 MHz. The two RF signals



(a) Output amplitude



(b) Output phase

Figure 3-20: Measured output amplitude and phase vs. outphasing angle for the OPERA prototype, with and without energy recovery. (a) Output amplitude. (b) Output phase.

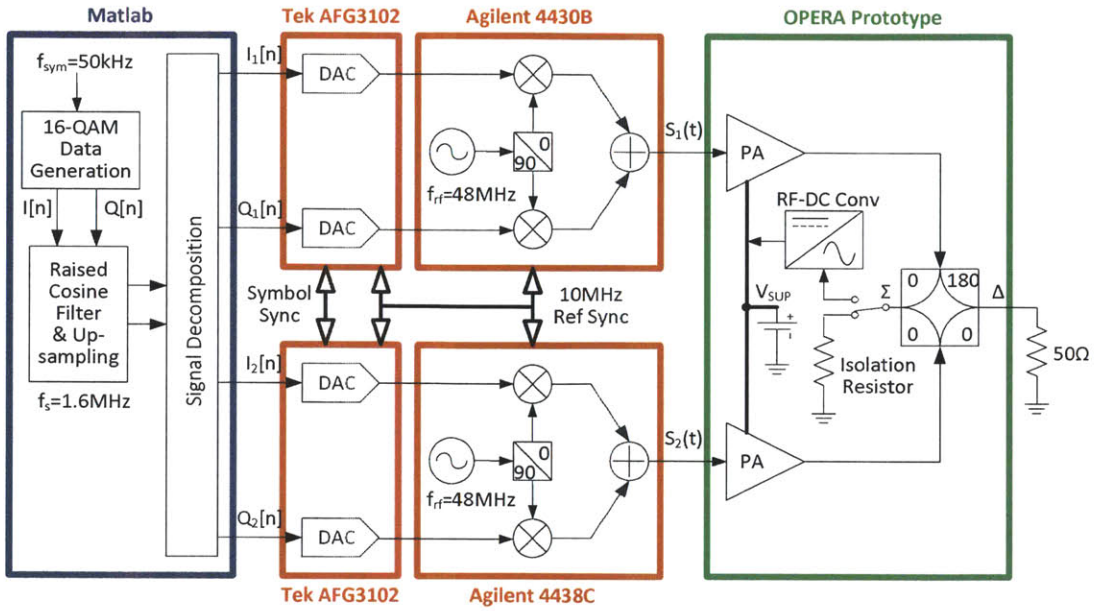


Figure 3-21: Outphasing system testbench used for the 48-MHz OPERA prototype for 50-kHz 16-QAM transmission.

are then fed to the two PAs in the OPERA prototype. The output of the OPERA prototype is fed into an HP 89400 vector signal analyzer (VSA) for spectrum and error vector magnitude (EVM) analysis.

Figure 3-22 shows the measured output spectrum for the 50-kHz 16-QAM transmission from the OPERA prototype with and without energy recovery, both before and after predistortion. From the spectrum, we can see that there is very little degradation in the transmitted spectrum with the OPERA system as compared to the standard LINC system, both before and after the predistortion is applied. Figure 3-23 shows the measured demodulated 16-QAM constellation of the OPERA prototype with and without energy recovery, both before and after predistortion. Again, we can see that before predistortion is applied, the degradation in error vector magnitude (EVM) when energy recovery is used is small, only 0.75%. After predistortion, the EVM both with and without energy recovery is reduced to less than 1%.

Table 3.1 summarizes the efficiency and linearity of the OPERA system in comparison with the standard LINC system. With predistortion, the OPERA system increases the overall efficiency from 17.9% to 42.0% compared to the LINC system,

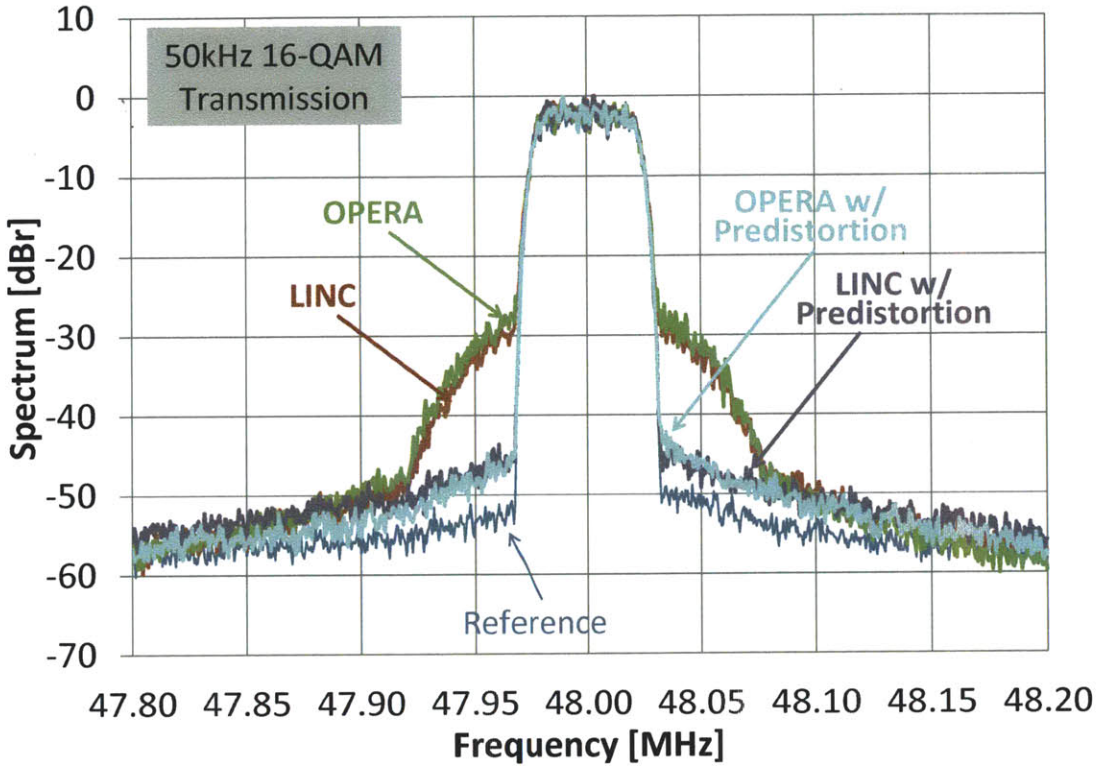
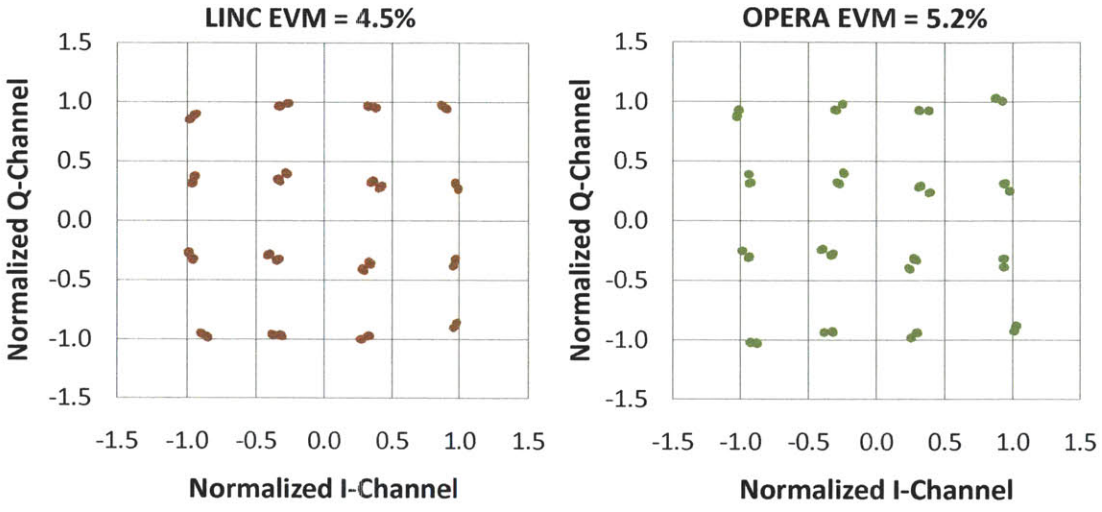
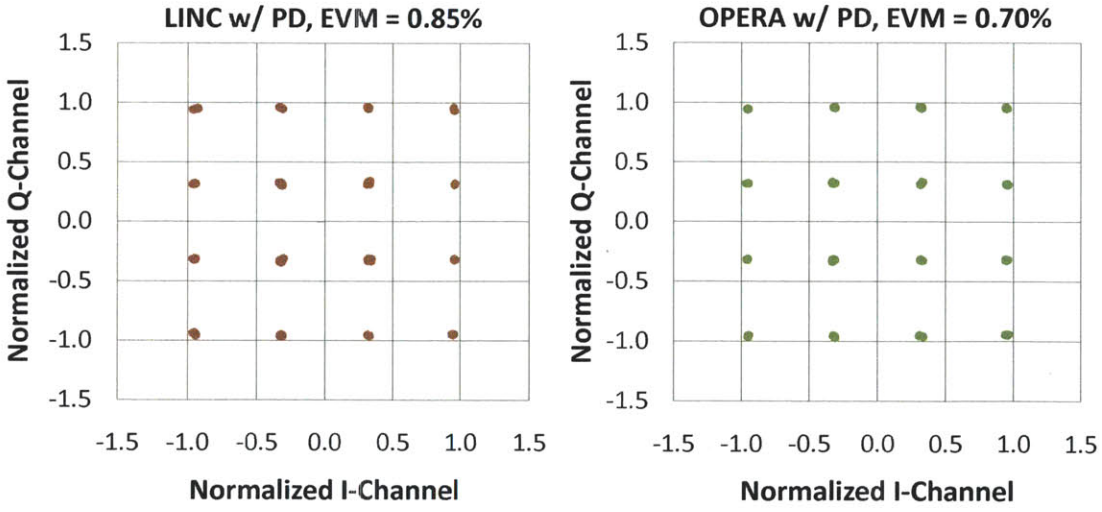


Figure 3-22: Measured output spectrum for 50-kHz 16-QAM transmission with 6.5-dB PAPR, with and without energy recovery, and before and after predistortion. The reference spectrum is the result using only the combiner with a fixed isolation port resistance.



(a) Before predistortion



(b) After predistortion

Figure 3-23: EVM for the 50-kHz 16-QAM transmission for the OPERA prototype with and without energy recovery. (a) Before predistortion. (b) After predistortion.

Table 3.1: 16-QAM Performance Comparison for LINC and OPERA

Architecture	P_{dc}	P_{diss}	P_{out}	η_{avg}	**EVM**
LINC	26.9 W	21.3 W	5.62 W	20.6 %	4.5 %
OPERA	11.5 W	7.0 W	4.47 W	39.6 %	5.2 %
LINC w/ PD	27.5 W	22.6 W	4.90 W	17.9 %	0.85 %
OPERA w/ PD	11.7 W	6.8 W	4.90 W	42.0 %	0.70 %

and the dc power consumption is reduced from 27.3 W to 11.7 W. This represents a substantial efficiency improvement and power savings of more than 2x. Another thing you can note from the table is that the output power for the LINC system without predistortion is much higher than the case with predistortion. This can be understood from Figure 3-20(a), which shows that output amplitude for the LINC system is higher than the nominal value predicted from outphasing over the entire operating range. Again, this distortion is due to the mismatch between the two PAs. The table also shows that the output power for the OPERA system without predistortion is less than the case with predistortion. Looking again at Figure 3-20(a), we see that the output amplitude of the OPERA system is less than the nominal value for most of the operating range, as expected.

One issue that has not been addressed to this point is the additional noise added to the power supply by the energy recovery network. This noise would show up in the measurement results as degraded EVM and a higher noise floor in the output spectrum. The spectrum and EVM measurements presented here suggest that the additional noise from the energy recovery network is negligible when compared with the standard LINC system. In general, this noise should not effect the overall performance if appropriate filtering (e.g., bypass capacitance or full electro-magnetic interference (EMI) filtering) is applied.

Since these measurement results were obtained at 48 MHz, it is important to discuss the effectiveness of the OPERA system at higher operating frequencies (e.g., in the microwave range). The system efficiency will most likely degrade due to the generally lower PA efficiencies obtained in this frequency range as well as the higher

insertion loss resulting from high frequency parasitics. However, as long as the efficiency of the PA and energy recovery network remains high enough, the efficiency improvement should still be significant and can be predicted by Equation (3.20). As PA peak efficiencies of up to 80% have been reported at an RF frequency of 2 GHz [48,49], and rectifier efficiencies as high as 75% have been reported at frequencies up to 10 GHz [50,51], it is likely that system efficiencies similar to those presented in this paper can be obtained in the microwave frequency range.

3.8 Summary

We have demonstrated a new outphasing energy recovery amplifier which greatly increases system efficiency while maintaining high linearity. Higher efficiency is obtained by replacing the isolation resistor in the conventional matched combiner with a rectifier, which recovers the untransmitted power that is usually wasted back to the power supply. Linearity is maintained through the use of a resistance-compression network, which reduces the impedance variation of the rectifier in order to provide isolation and matching between the two outphased PAs. A prototype system was designed and built at a carrier frequency of 48 MHz, delivering 20.8-W peak power with 82.9% system efficiency. The prototype is tested with a 50-kHz 16-QAM signal with a PAPR of 6.5 dB and improves the overall efficiency from 17.9% to 42.0% over the standard LINC system.

Chapter 4

Asymmetric Multilevel Outphasing

In the previous section, we have seen that energy recovery in the power combiner of the outphasing system can greatly enhance the efficiency of LINC transmitters. Another technique that can help alleviate the problem of wasted energy during outphasing is multi-level outphasing, discussed briefly in Section 2.5.3. In multi-level LINC (ML-LINC), the supply voltage for the two PAs can switch among multiple discrete levels depending on the output amplitude. This means that when a small output amplitude is required, the supply voltage can be reduced so that the amount of power being delivered to the power combiner is reduced. This reduces the power being sent to the isolation resistor, improving the overall efficiency.

ML-LINC requires both PAs in the outphasing system to have the same supply voltage at any given time. However, even higher efficiency can be achieved by allowing the supply voltage of each PA to change *independently*. Since the supply voltages for the two PAs can be different, we call this technique asymmetric multilevel outphasing (AMO).

4.1 Architecture Overview

A block diagram of the AMO system is shown in Figure 4-1. As shown in the figure, AMO modulates both the phase and the amplitude of the PAs, similar to polar modulation described in Section 2.2. Thus, AMO can be seen as a hybrid of the polar

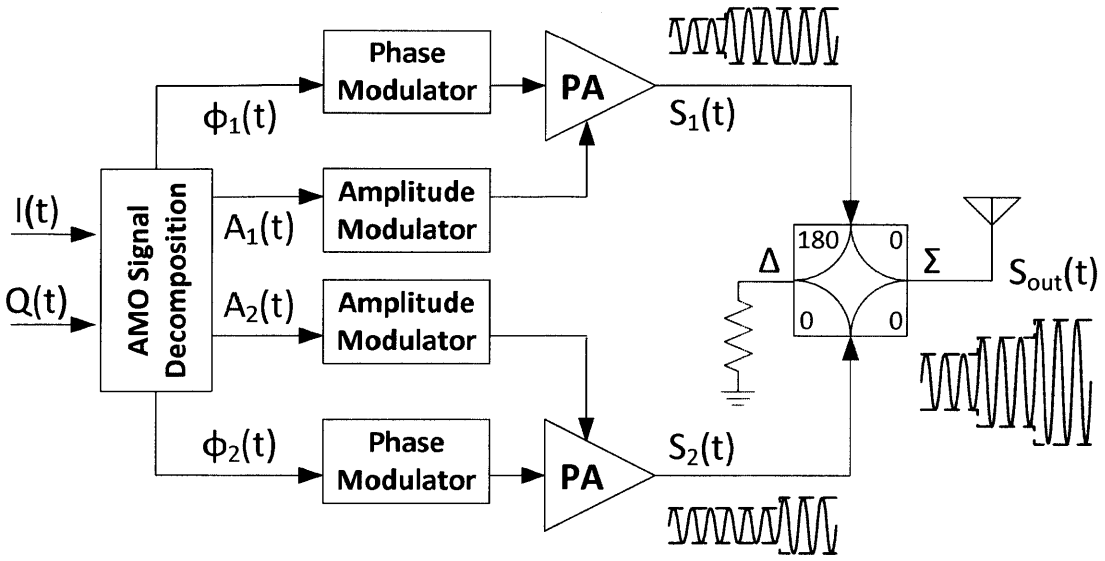


Figure 4-1: Asymmetric multilevel outphasing (AMO) architecture.

and outphasing architectures. The advantage of AMO over polar systems is that the amplitude modulators are discrete, whereas in polar systems they are continuous. Discrete supply modulators can be implemented using fast, digital switching networks, which can achieve both high efficiency and high bandwidth simultaneously. This is different from continuous supply modulators such as dc-dc converters or linear regulators, in which there is a fundamental tradeoff between efficiency and bandwidth. The AMO system only requires discrete amplitude modulation because it is only used for coarse amplitude control. Fine amplitude control is achieved using outphasing.

The original ML-LINC architecture introduced in [34] varied the amplitude levels of the two PAs by changing the supply voltages. However, in general multilevel outphasing does not require this; the only requirement is that the PA amplitude levels can switch among multiple levels. Changing the supply voltage is not the only method to modulate the output amplitude of a PA. For example, pulse-width modulation as described in Section 2.3 can also be used. This method will be described in more detail in Section 4.2.3.

Figure 4-2: Signal component vector diagram for LINC, ML-LINC, and AMO. The smallest outphasing angle is achieved with AMO.

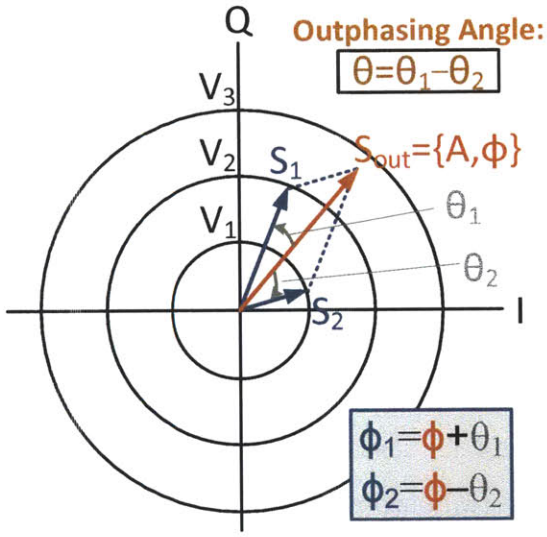


Figure 4-3: Vector diagram for AMO modulation, including notational convention.

4.2 AMO Modulation

Fundamentally, AMO modulation decomposes a complex vector, which represents a baseband constellation point, into two vectors such that the sum of the two vectors constructs the original complex vector with the *minimum* outphasing angle, as illustrated in Figure 4-2. The two vectors are the baseband representation of the two PA outputs. Compared to ML-LINC, by making *independent* changes in the supply voltage for each of the two outphased PAs, the AMO technique results in smaller outphasing angles so that higher efficiency can be achieved.

Mathematically, AMO modulation decomposes an arbitrary RF output signal $S_{out}(t)$ into two constant-envelope signals $S_1(t)$ and $S_2(t)$ such that the sum con-

structs the original signal, as shown in Figure 4-3. $S_{out}(t)$ can be defined in terms of either Cartesian or polar coordinates as

$$S_{out}(t) = I(t)\cos[\omega t] + Q(t)\sin[\omega t] \quad (4.1)$$

$$S_{out}(t) = A(t)\cos[\omega t + \phi(t)] \quad (4.2)$$

where $I(t)$ and $Q(t)$ are the in-phase and quadrature components (respectively) of the RF signal being transmitted, $A(t)$ and $\phi(t)$ are the amplitude and phase components (respectively), and ω is the RF carrier frequency. For fixed PA amplitudes $A_1(t)$ and $A_2(t)$ for the two PAs in the AMO system, the AMO signal decomposition can be performed by referring to the vector diagram shown in Figure 4-3 and using vector geometry to determine the appropriate phases for the two input signals. However, there is a subtlety in the vector addition that is not apparent from Figure 4-3 that arises from conservation of energy in the power combiner.

A conventional isolating power combiner has four ports, as described in Section 1.2 and as shown in Figure 4-1. There are two input ports for the two signals being combined, and there are two output ports, one for the sum of the two signals being combined and one for the difference. The sum port is usually connected to the output load, while the difference port is terminated by an isolation resistor to ensure correct impedance matching and isolation for the two PAs. Conservation of energy requires that the sum of the powers from the two input ports should equal the sum of the powers from the two output ports:

$$P_1 + P_2 = P_{sum} + P_{diff} \quad (4.3)$$

From this equation, it is easy to see that the vector at the output sum port cannot simply be the addition of the vectors at the two input ports ($\vec{S_{out}} \neq \vec{S_1} + \vec{S_2}$). For example, consider the case when the two input vectors are exactly the same, having the same amplitude and phase so that $P_{diff} = 0$. If we assume that $\vec{S_{out}} = \vec{S_1} + \vec{S_2}$, and we use the fact that power is proportional to the square of the amplitude, then

can write Equation 4.3 as

$$A_1{}^2 + A_2{}^2 \neq (A_1 + A_2)^2 \tag{4.4}$$

which is obviously not correct. In order to satisfy conservation of energy, the relationship between the output sum port and the two input ports is actually given by

$$\vec{S_{out}} = \frac{\vec{S_1} + \vec{S_2}}{\sqrt{(2)}} \tag{4.5}$$

This equation shows that the output vector is the sum of the two input vectors scaled by a factor of $1/\sqrt{(2)}$.

Now that the vector relationship between the output and the two inputs have been established, we can complete the AMO signal decomposition by referring to the vector diagram shown in Figure 4-3 and using the law of cosines, resulting in the following equations:

$$\begin{aligned}
S_{out}(t) &= S_1(t) + S_2(t) && (4.6)\\
S_1(t) &= A_1(t)\cos\left[\omega t + \phi_1(t)\right] && (4.7)\\
S_2(t) &= A_2(t)\cos\left[\omega t + \phi_2(t)\right] && (4.8)\\
\phi_1(t) &= \phi(t) + \arccos\left[\frac{A_1(t)^2 + 2A(t)^2 - A_2(t)^2}{4A_1(t)A(t)/\sqrt{2}}\right] && (4.9)\\
\phi_2(t) &= \phi(t) - \arccos\left[\frac{A_2(t)^2 + 2A(t)^2 - A_1(t)^2}{4A_2(t)A(t)/\sqrt{2}}\right] && (4.10)\\
\theta(t) &= \phi_1(t) - \phi_2(t) && (4.11)
\end{aligned}$$

$\phi_1(t)$ and $\phi_2(t)$ are the phases of the two PAs, and $\theta(t)$ is called the *outphasing angle.* For a given vector $S_{out}(t)$, there are multiple choices for the PA amplitudes and phases $A_1(t)$, $A_2(t)$, $\phi_1(t)$, and $\phi_2(t)$, as can be seen in Figure 4-2. The solution that minimizes the outphasing angle should typically be chosen to maximize the efficiency of the AMO system. Figure 4-4 plots the outphasing angle vs. output amplitude for LINC, ML-LINC, and AMO when there are 4 PA amplitude levels available. It can be seen that the AMO system always results in the minimum outphasing angle as compared to LINC and ML-LINC.

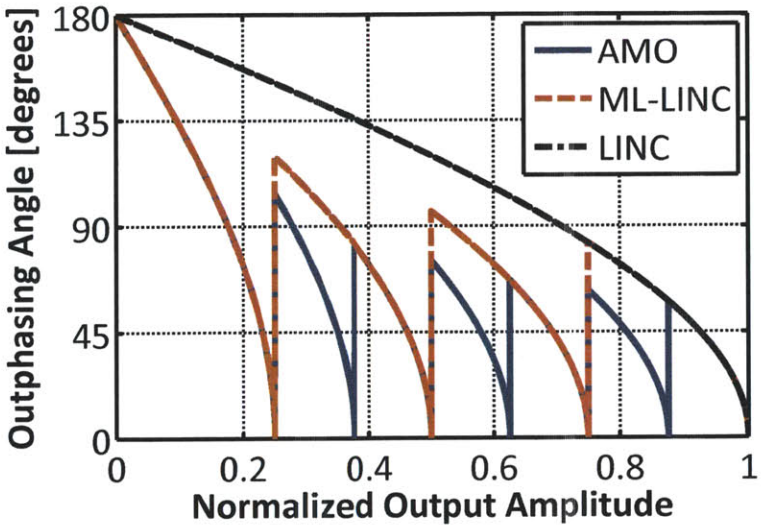


Figure 4-4: Outphasing angle vs. output amplitude of AMO modulation compared to LINC and ML-LINC, when 4 different PA amplitude levels are available. AMO always results in the minimum outphasing angle.

4.2.1 Theoretical Efficiency

To calculate the efficiency of the AMO system, we must first calculate the efficiency of the isolating power combiner for the case when the two input signals being combined are not the same power level (i.e., asymmetric power combining). In this case, there is loss in the combiner even when there is no outphasing (i.e., $\phi_1 = \phi_2$). The efficiency of power combining with an ideal isolating power combiner is given by

$$\eta_c = \frac{(A_1 \cos\theta_1 + A_2 \cos\theta_2)^2}{2\left({A_1}^2 + {A_2}^2\right)} \tag{4.12}$$

where A_1 and A_2 are the amplitudes of the two RF sinusoid inputs whose phases are θ_1 and θ_2 relative to the output phase (see Figure 4-3 for notational convention). The efficiency of asymmetric combining is shown in Figure 4-5 for the special case where $\phi_1 = \phi_2$ and the amplitude of A_2 is swept continuously between 0 and A_1. When $A_1 = A_2$, the output power is maximum and the efficiency is 100%, as expected when there is no outphasing. As A_2 is decreased from A_1 to 0, both the output power and efficiency decrease. The reason the efficiency decreases when the input amplitudes are

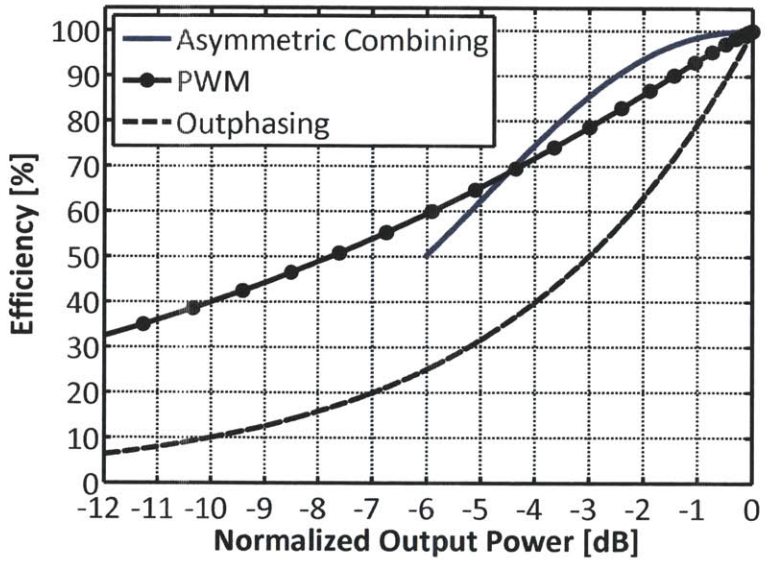


Figure 4-5: Asymmetric 2-way power combining efficiency vs. output power, for the special case where $\phi_1 = \phi_2$ and the amplitude of A_2 is swept continuously between 0 and A_1. The efficiency of outphasing and class-E PWM (described in Section 2.3) is also shown for comparison.

different is due to the fact that an isolating combiner has two output ports, one for the sum of the two input signals and one for the difference of the two input signals, as described in Section 1.2. When the input amplitudes are different, some of the power goes to the difference port (even if the input phases are the same), which is terminated with a resistor in an isolating combiner. This power is wasted as heat so that the efficiency is no longer 100%. However, as shown in Figure 4-5, the efficiency of asymmetric power combining is still much higher than outphasing.

In the AMO system, if there are N different PA output amplitudes A_1 to A_N, there are $\binom{N}{2} + N$ combinations of PA amplitudes for the two PAs. However, as shown in Figure 4-5, the combiner efficiency decreases as the difference between two amplitude levels increases. Therefore, in our implementations of the AMO system, we restrict the combinations to be adjacent amplitude levels (i.e., A_k and A_{k+1}).

Figure 4-6 compares the theoretical efficiency vs. output power for LINC, ML-LINC, and AMO when there are 4 different PA amplitude levels available. Each of the amplitude levels are spaced 3 dB apart. It can be seen that the AMO system

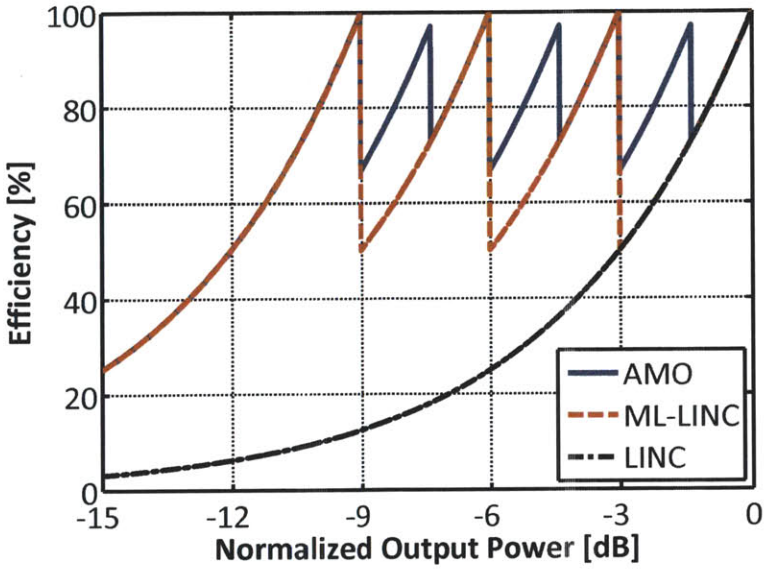


Figure 4-6: Efficiency vs. output power of AMO modulation compared to LINC and ML-LINC when 4 different PA amplitude levels are available, assuming 100% efficiency in the PAs.

always achieves the highest possible efficiency as compared to LINC and ML-LINC. In particular, note that ML-LINC has 4 efficiency peaks, corresponding to the 4 PA amplitude levels, and that AMO has 3 additional efficiency peaks (for a total of 7) corresponding to the 3 asymmetric combinations of the amplitude levels for the two outphased PAs, with the restriction that the two amplitude levels must be adjacent.

Figure 4-7 compares the theoretical efficiency vs. output power for the AMO system when there are 4 amplitude levels available vs. when there are 2 amplitude levels available. It can be seen that that the greater the number of amplitude levels, the higher the efficiency curve over a given output power range. However, as the number of amplitude levels increases, so does the complexity of the discrete amplitude modulators. There are at least two different methods to change the amplitude levels of the two PAs in the AMO system: (1) supply-voltage modulation, and (2) pulse-width modulation. Each of these methods will be described in the next two sections.

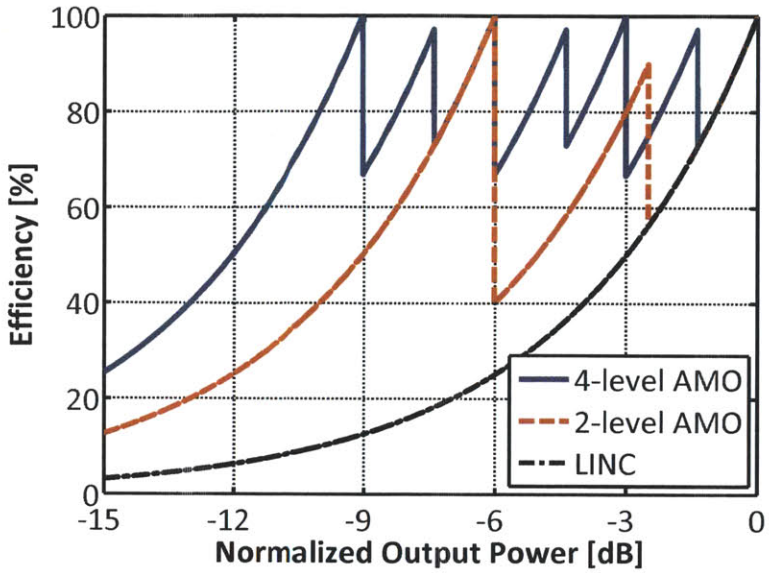


Figure 4-7: Efficiency vs. output power of AMO modulation when there are 4 amplitude levels available vs. when there are 2 amplitude levels available.

4.2.2 Discrete Supply-voltage Modulation (DSVM)

One way to modulate the PA output amplitudes in the AMO system is to vary the supply voltages of the PAs. When this is done in a discrete manner as is required by the AMO system, we call it discrete supply-voltage modulation (DSVM). Figure 4-8 shows an example of a discrete supply voltage modulator with N different levels. It consists of N switches, each of which is connected to a different supply voltage. The control logic of the switches should be such that only one switch is on at any given time. The N different supply voltages can each be generated with an efficient, static dc-dc converter. As mentioned previously, a DSVM implemented with fast, digital switches can achieve both high efficiency and high bandwidth simultaneously. This is different from continuous supply modulators such as dc-dc converters or linear regulators, in which there is a fundamental tradeoff between efficiency and bandwidth.

The DSVM shown in Figure 4-8 can theoretically achieve 100% efficiency, because an ideal switch does not dissipate any power. This means that the theoretical efficiency curve of the AMO system using DSVM is the same as shown in Figure 4-6.

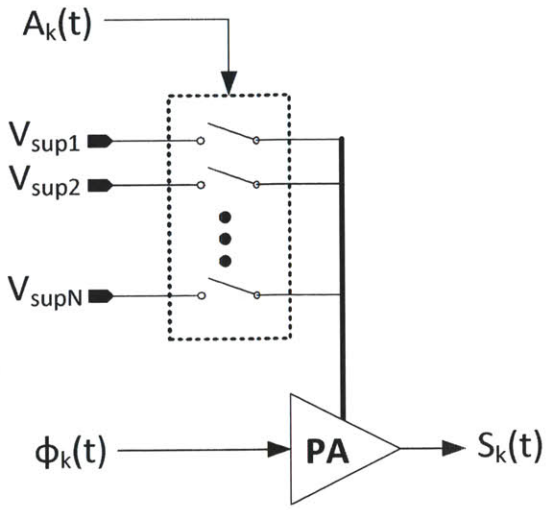


Figure 4-8: Example of a discrete supply-voltage modulator (DSVM).

However, real switches will have finite on-resistance, leakage current, and gate capacitance which must be charged and discharged to turn the switches on and off. These sources of power dissipation will lower the efficiency of the DSVM. Furthermore, the efficiency of the PA is also a function of the supply voltage and will depend on the class of the PA as well. For example, the optimal efficiency for class-E PAs is actually independent of the supply voltage [52], although parasitics such as the nonlinear junction capacitance at the drain of the transistor will cause the PA efficiency to vary with the supply voltage. Another source of power loss for the PA comes from the gate driver, which is typically a fixed loss independent of supply voltage for a switching-mode PA. This fixed loss will lower the efficiency curve at lower output power levels.

Figure 4-9 shows the efficiency vs. output power of the AMO system using DSVM with 4 different supply voltage levels, assuming there is a fixed power loss of -13dB relative to the maximum output power. This loss could represent the fixed power required to drive the gate of the switching-mode PA. The only other loss we assume in the plot is the loss due to the asymmetric power combining. The curve labeled "VDD" represents the PA efficiency as the supply voltage is varied continuously to modulate the output power. The curve labeled "AMO" is the efficiency of the AMO

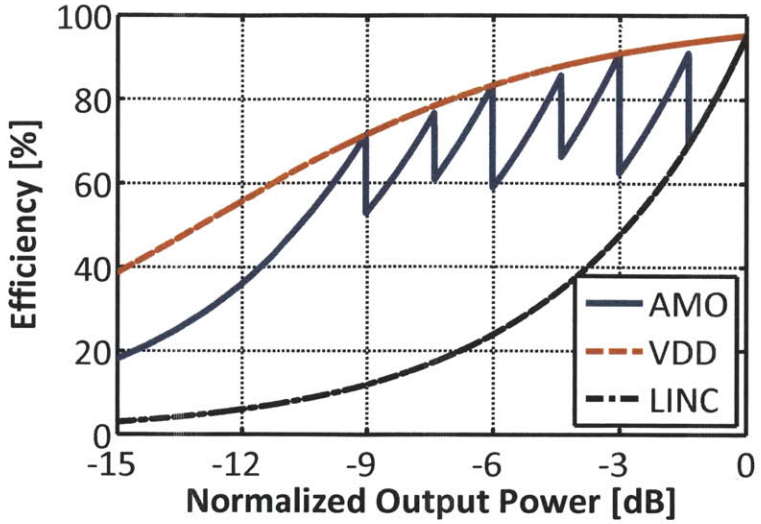


Figure 4-9: Efficiency vs. output power of the AMO system with DSVM when 4 different supply voltage levels are available, assuming a fixed power loss of -13dB relative to the maximum output power. The only other loss accounted for in the plot is the loss due to the asymmetric combining.

system with 4 different supply voltage levels to switch among. The shape of this efficiency curve is more representative of a real AMO system using DSVM.

4.2.3 Discrete Pulse-width Modulation (DPWM)

As discussed in Section 2.3, pulse-width modulation (PWM) allows switching-mode PAs like class-E/F with a fixed supply voltage to vary the PA amplitude by changing the input duty cycle [18, 22]. However, conventional PWM suffers from a number of practical difficulties. In order to achieve a wide amplitude dynamic range for carrier frequencies exceeding 1 GHz, pulse widths on the order of a few picoseconds are required to generate the smallest required output amplitudes. Such small pulses are not only difficult to generate, but are also usually filtered out by the large PA input capacitance. Futhermore, in order to meet linearity requirements, extremely fine time resolution for the pulse width modulator is required, also on the order of a few picoseconds at GHz frequencies, which is difficult to implement. Finally, low duty cycles yield low PA efficiency, as shown in Figure 2-6.

Discrete pulse-width modulation (DPWM), which we can use with AMO as an

alternative method to DSVM for generating a discrete set of amplitude levels, escapes from the problems of classical PWM. In AMO transmitters, fine amplitude modulation is accomplished by outphasing. We use DPWM only for coarse amplitude modulation. Thus, narrow pulse-width generation and precise pulse width control become unnecessary. Also, by selecting one of few pulse widths, DPWM can limit the range of duty cycle variation so that a large PA efficiency drop is avoided. The chief advantage of DPWM over DSVM for AMO transmitters is hardware simplicity, as it eliminates the need for a fast, low-loss switching network and selection of supply voltages. An example implementation of a differential 2-level discrete pulse-width modulator is shown in Figure 4-10. The input to the discrete PWM block is a square wave with 50% duty cycle at the RF carrier frequency of the PA. A 2:1 multiplexer (MUX) is used to switch between this signal and another signal that has a duty cycle less than 50%. To create the latter signal, an inverter chain delays the square-wave signal, and the result is passed to an AND gate together with the square-wave signal. This creates a pulsed signal with a duty cycle less 50%, as shown in the figure.

Figure 4-11 shows the efficiency for the AMO system using DPWM with 4 different duty cycles, along with the efficiency curve using 2 different duty cycles. With 4 different duty cycles, the AMO efficiency curve closely approximates the PWM efficiency curve over a large output power range. The advantage of the AMO-DPWM system over the conventional PWM system is that it can achieve a much higher amplitude dynamic range by using outphasing to generate small amplitude levels, rather than relying on narrow pulses which are difficult to generate and often cannot be processed by the PA due to the large input gate capacitance.

DPWM can also be combined with DSVM in an AMO system to achieve even higher efficiency than can be achieved using one technique alone. Figure 4-12 shows the efficiency of the AMO system using 4-level DSVM combined with 2-level DPWM. It can be seen that the system efficiency is significantly enhanced when the 2-level DPWM is added to the 4-level DSVM.

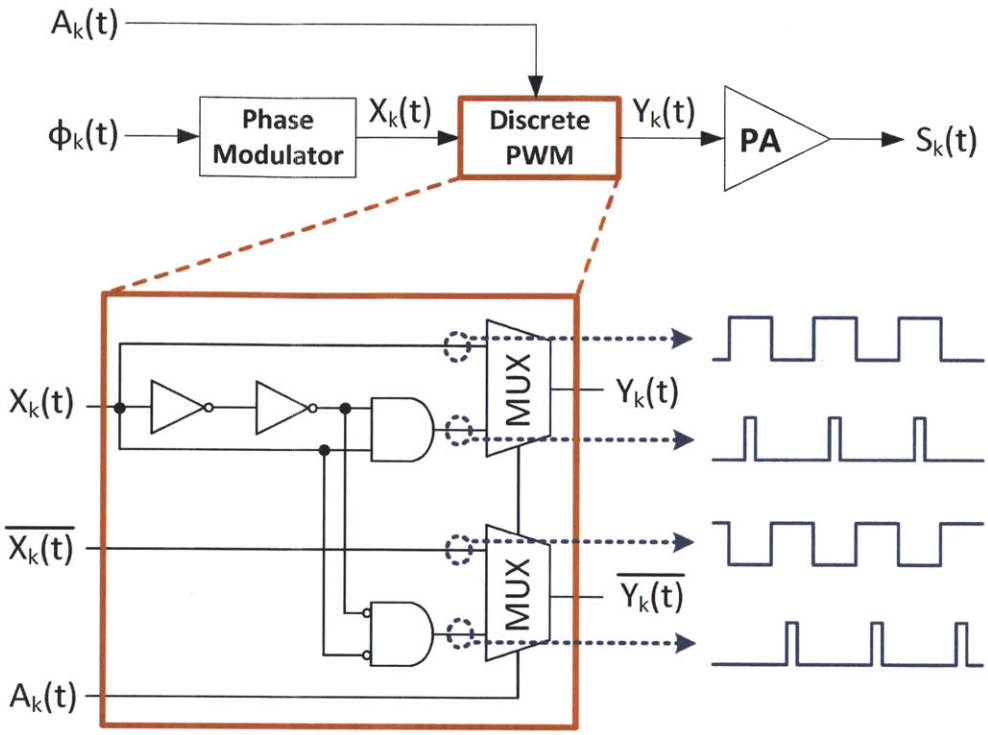


Figure 4-10: Example implementation of a 2-level discrete pulse-width modulator (DPWM).

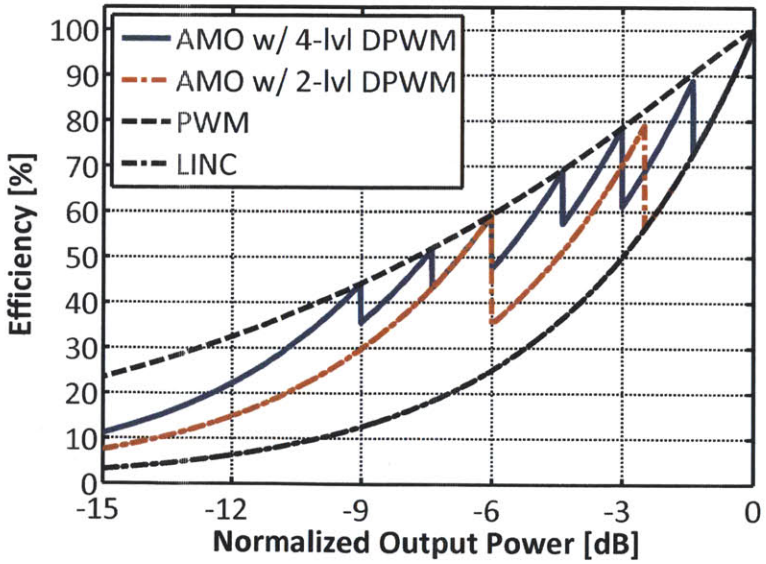


Figure 4-11: Efficiency for the AMO system using DPWM with 4 different duty cycles, along with the efficiency curve using 2 different duty cycles.

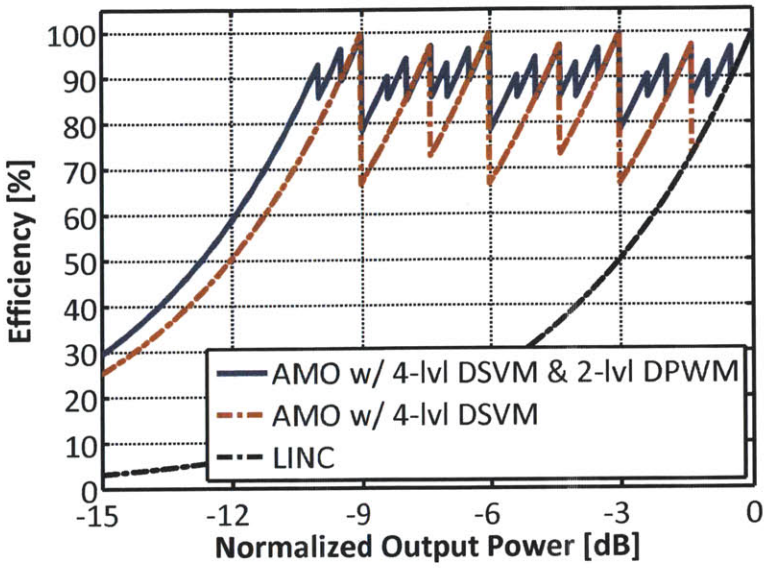


Figure 4-12: Efficiency of the AMO system using 4-level DSVM (red line) vs. the AMO system using 4-level DSVM combined with 2-level DPWM (blue line).

4.3 Multi-standard Efficiency Optimization

For a given signal's amplitude probability density function (PDF), we can choose the values of the amplitude levels in the AMO system such that the overall average efficiency is maximized. In this way, we can optimize the AMO system for multiple wireless communication standards simply by changing the PA amplitude levels. This means changing the supply voltages when using DSVM and changing the duty cycles when using DPWM. For the following analysis, let us assume we are using DSVM. The optimum values of the supply voltages can be determined as follows.

Let us define the output amplitude levels r_k to be the maximum output amplitudes for each of the different supply voltage levels $V_{sup,k}$ when both PAs are driven by the same supply. Let us also define $n_{PA}(r_k)$ to be the PA efficiency when the output amplitude is r_k (with both PAs driven by the same supply). Figure 4-13 shows an example amplitude PDF for a modulated signal, along with an example PA efficiency curve vs. output amplitude. The total average efficiency can be computed as

$$\eta_{avg} = \frac{\langle Pout \rangle}{\langle P_{DC} \rangle} \tag{4.13}$$

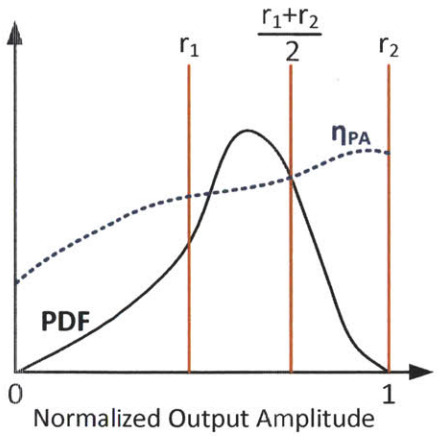


Figure 4-13: Example amplitude PDF for a signal (black line), along with an example PA efficiency curve η_{PA} vs. output amplitude (blue line). The r_k are the maximum output amplitudes for each of the different supply voltage levels $V_{sup,k}$ when both PAs are driven by the same supply. There are 2 amplitude levels available in the example above.

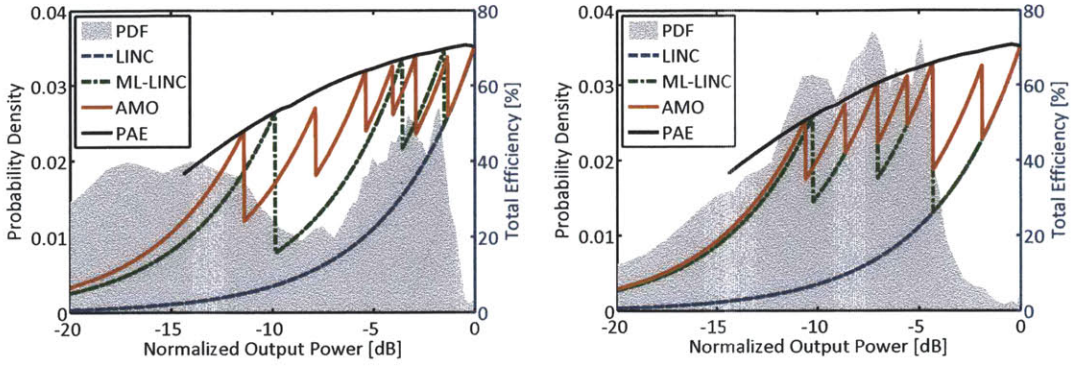
If the amplitude PDF $p(A)$ of the transmitted signal is known, then the average output power is simply

$$\langle P_{out} \rangle = \int p(A) A^2 dA \tag{4.14}$$

To determine the average DC power, we divide the PDF into several regions separated by the r_k (and their combinations), and for each region we integrate the PDF curve to find the total probability in that region and multiply that probability by the DC power consumption when the AMO system operates in that region (see Figure 4-13). With the combinations of supply voltages restricted to be adjacent supply levels, the average DC power can be computed as

$$\begin{aligned} \langle P_{DC} \rangle \;=\; & \frac{r_1^2}{\eta_{PA}(r_1)} \int_0^{r_1} p(A) dA \\ & + \sum_{k=1}^{N-1} \left[\frac{1}{2} \left(\frac{r_k^2}{\eta_{PA}(r_k)} + \frac{r_{k+1}^2}{\eta_{PA}(r_{k+1})} \right) \int_{r_k}^{\frac{r_k + r_{k+1}}{2}} p(A) dA \right. \\ & \left. + \frac{r_{k+1}^2}{\eta_{PA}(r_{k+1})} \int_{\frac{r_k + r_{k+1}}{2}}^{r_{k+1}} p(A) dA \right] \end{aligned} \tag{4.15}$$

Using this equation, the optimum set of supply voltage levels for a given amplitude



(a) HSUPA (b) WLAN

Figure 4-14: Amplitude PDF of a modulated signal and corresponding optimum efficiency curves for LINC, ML-LINC, and AMO with 4 available supply voltages. (a) HSUPA signal. (b) WLAN signal.

PDF can be found by first measuring the PA efficiency $n_{PA}(r_k)$ as a function of r_k (sweeping the supply voltage), and then performing an exhaustive search on the N values of the r_k.

Figure 4-14(a) shows the amplitude PDF for an HSUPA signal (a 3G cellular standard) and the corresponding optimum efficiency curves for LINC, ML-LINC, and AMO using 4 different supply levels. The data was generated using Agilent's ADS software, and the PA efficiency curve was obtained from simulation of a class-E PA designed in a 65-nm CMOS process. The figure shows that ML-LINC increases the efficiency over a much wider power range than the standard LINC system, and AMO increases the efficiency even further by effectively doubling the number of levels. Figure 4-14(b) shows the amplitude PDF and optimum efficiency curves for a WLAN signal.

4.4 AMO Predistortion Algorithm

Section 4.2 described the mathematical signal decomposition for AMO modulation that determines the amplitudes and phases for the two outphasing branches. However, this decomposition will not work if there is amplitude and phase mismatch

between the two branches. Because all real circuit components experience random variation, it is impossible for the two outphasing branches to be matched perfectly. Applying the formulation in Section 4.2 with two mismatched paths would result in a distorted output signal. Furthermore, the AMO signal decomposition requires the values of the PA amplitude levels A_k to be known ahead of time. When DSVM is used to generate the discrete amplitude levels, it is hard to accurately predict what the PA amplitude levels will be based on the supply voltage alone. This is due to the nonlinearity of the PA output amplitude as a function of the supply voltage, which is well-known in polar-modulation architectures [16, 53]. The PA output phase also varies with supply voltage, which is not accounted for in the ideal AMO signal decomposition of Section 4.2. AMO with DPWM suffers from similar nonlinearities in the PA output amplitude and phase that are not accounted for in the PWM theory described in Section 2.3 [22, 23]. For these reasons, some method of linearization or predistortion based on measurements of the transmitter output is required to correct for the nonlinearities in a real AMO system.

For this work, we implement an AMO digital predistortion (DPD) method based on lookup table training [54, 55]. The first step is to measure the transmitter output amplitude and phase vs. outphasing angle for each possible combination of amplitude levels for the two outphased PAs. For example, if there are 4 amplitude levels available, there would be 7 possible combinations as described in Section 4.2.1[1]. Specifically, referring to Figure 4-1, we set the inputs to the AMO system as follows:

$$A_1 = V_i \tag{4.16}$$

$$A_2 = V_j \tag{4.17}$$

$$\phi_1 = \frac{\theta}{2} \tag{4.18}$$

$$\phi_2 = -\frac{\theta}{2} \tag{4.19}$$

[1]Due to the amplitude and phase mismatch between the two outphasing paths, there are actually 10 different possible combinations for 4 available amplitude levels. This is because the combination (V4,V3) will produce different results than (V3,V4) due to the mismatch. This applies to the combinations (V3,V2) and (V2,V1) as well. Note that in our implementations of the AMO system, we restrict the combinations to be adjacent amplitude levels.

V_i and V_j represent the available amplitude levels for the PAs, and θ is defined as the outphasing angle, which can range from -180° to +180°. With these input settings, we measure the amplitude and phase of the output S_{out}, sweeping θ. We do this for every combination of amplitude levels for the two PAs (V_i and V_j). Note that negative and positive outphasing angles can yield different measurement results due to the amplitude and phase mismatch between the two outphasing paths.

The measurements of the output amplitude and phase vs. outphasing angle capture the amplitude and phase distortions of the system due to the mismatch between the 2 outphasing paths as well as the varying supply voltage (for DSVM) or the varying input duty cycle (for DPWM). An example of this measurement data is shown in Figure 4-15. There are 7 different curves, each for a different combination of amplitude levels for the two outphased PAs. Note that not all outphasing angles are measured for every possible combination. This is because we only require that all the curves together cover the entire amplitude range. As described in Section 4.2, there are multiple solutions for the PA amplitude and phases that yield the same output amplitude. The combinations with the lowest amplitude levels are favored over the others, because they result in the lowest DC power dissipation and therefore the highest efficiency. Figure 4-16 gives the amplitude and phase linearity plots for the example measurement data given in Figure 4-15. Figure 4-16(a) plots the difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. Figure 4-16(b) plots the measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2. As explained previously, the difference between the ideal and measured curves is due to the mismatch between the two outphasing paths, as well as the varying supply voltage or duty cycle.

Once the distortion data has been measured, the AMO signal decomposition with DPD proceeds as shown in Figure 4-17. The algorithm is as follows:

1. **Cartesian to Polar Conversion:** The baseband I and Q data is converted to polar coordinates A and ϕ.

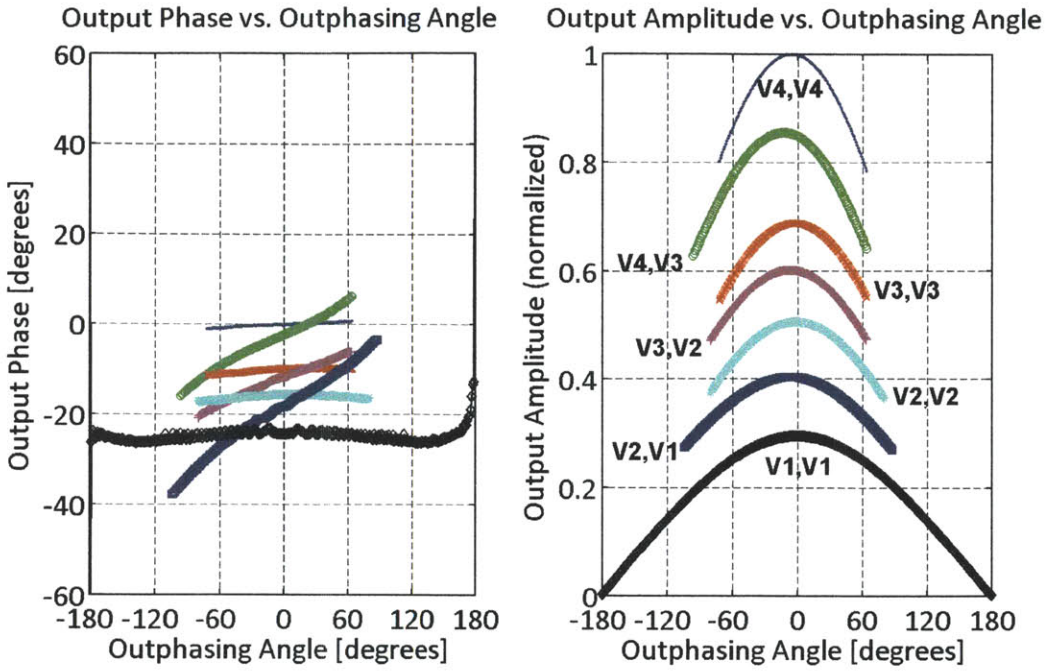
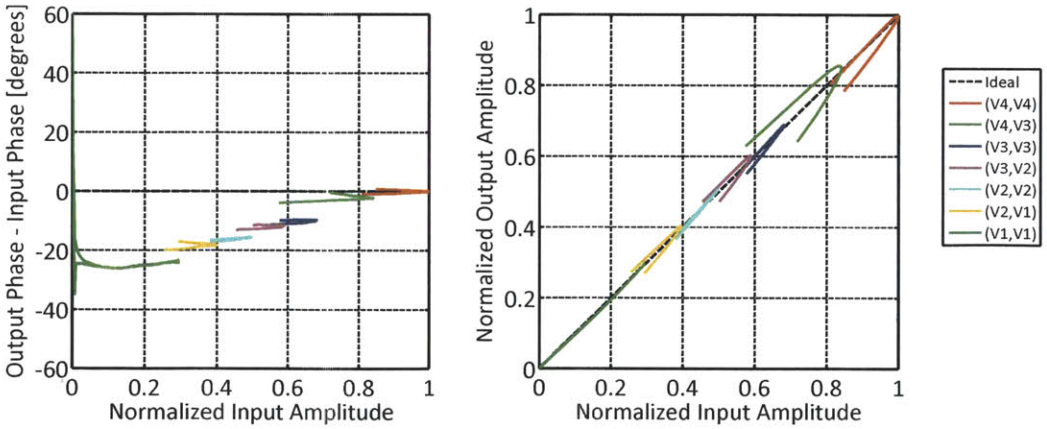


Figure 4-15: Example measurement data for the output amplitude and phase vs. outphasing angle for a real AMO system, which capture the static nonlinearities of the AMO system. Each curve corresponds to a different combination of amplitude levels for the two outphased PAs.



(a) Static Phase Nonlinearity

(b) Static Amplitude Nonlinearity

Figure 4-16: Amplitude and phase linearity plots for the example measurement data given in Figure 4-15. (a) Difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. (b) Measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2.

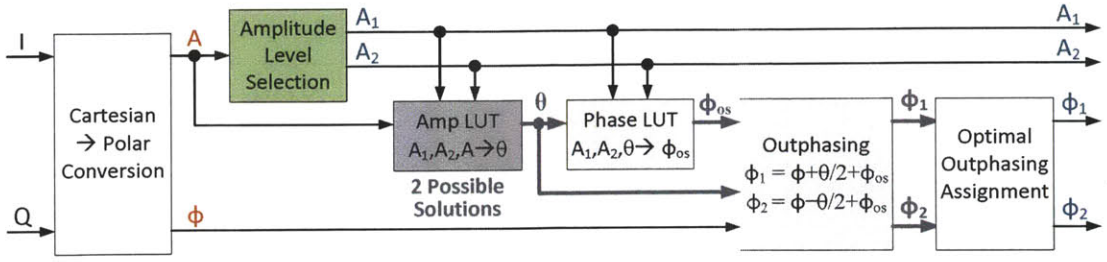


Figure 4-17: Block diagram for the AMO signal decomposition with DPD based on lookup tables.

2. **Amplitude Level Selection:** The combination of amplitude levels for the two outphased PAs (A_1 and A_2) is chosen based on A, using the measured amplitude data collected before. As mentioned previously, the combination with the lowest amplitude levels is chosen for maximum efficiency. For example, using the data in Figure 4-15, if the normalized A was 0.8, the combination (V4,V3) would be chosen for (A_1,A_2).

3. **Amplitude LUT:** The outphasing angles that resulted in the given A for the previously chosen amplitude combination is recorded. Note that there are always two possible outphasing angles, θ_A and θ_B, for a given A; typically one is positive and the other is negative, as shown in Figure 4-15.

4. **Phase LUT:** The corresponding output phase offsets, $\phi_{os,A}$ and $\phi_{os,B}$, for the two possible outphasing angles, θ_A and θ_B, are recorded.

5. **Outphasing Phase Calculation:** The phases for the two PAs, ϕ_1 and ϕ_2, are calculated as follows:

$$\phi_1 = \phi + \frac{\theta}{2} + \phi_{os} \tag{4.20}$$

$$\phi_2 = \phi - \frac{\theta}{2} + \phi_{os} \tag{4.21}$$

   Note that there will be two possible solutions for the PA phases, ($\phi_{1,A}$,$\phi_{2,A}$) and ($\phi_{1,B}$,$\phi_{2,B}$), corresponding to the two possible solutions for θ and ϕ_{os}.

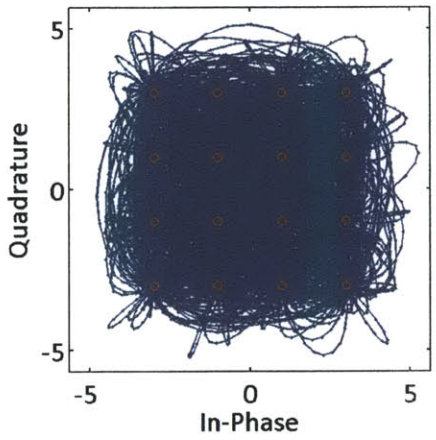
6. **Optimal Outphasing Assignment:** The final step is to choose one of the

two possibilities for the PA phases. To make this decision, we use the optimal outphasing assignment scheme described in [1, 47]. Basically, this involves calculating the phase difference between the current sample and the previous sample for both ϕ_1 and ϕ_2. The previous sample has already been chosen, but the current sample has two possibilities. The possibility that minimizes the worst-case phase difference for ϕ_1 and ϕ_2 is chosen. Large, abrupt phase changes are undesirable because the finite bandwidth of phase modulators and the PA input and output matching networks filter out these abrupt changes so that the linearity and noise of the system is degraded. Figure 4-18 shows the PA phases and phase differences after the AMO signal decomposition with and without the optimal outphasing assignment. The input data is a 16-QAM signal, and the constellation diagram and trajectory of the 16-QAM signal is also shown. It can be seen that the optimal outphasing assignment significantly reduces the magnitude of the abrupt phase changes.

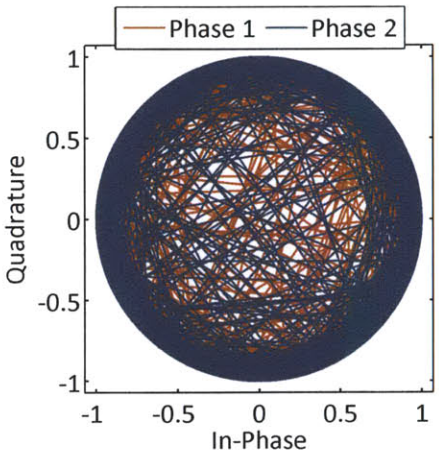
Figure 4-19 shows the time-domain waveforms of the PA amplitudes and phases, A_1, A_2, ϕ_1, ϕ_1, for a segment of the 16-QAM signal shown in Figure 4-18(a). They are the result from the AMO signal decomposition with DPD outlined above, using the example measured data shown in Figure 4-15. It can be seen that the two PA amplitude levels closely follow the amplitude of the input signal, so that the DC power consumption is minimized for the highest possible efficiency. Also note the outphasing angle remains relatively small, except when the amplitude becomes very small.

4.5 48-MHz Discrete Prototype using DPWM

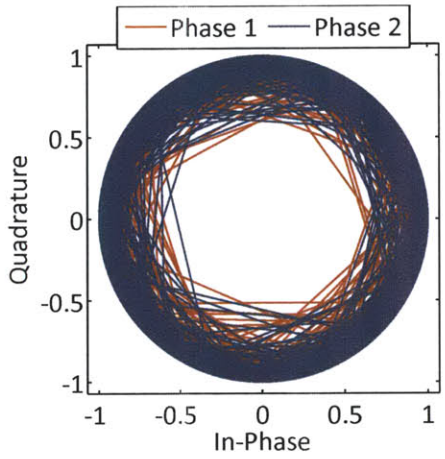
To demonstrate the feasibility of the AMO system, a prototype was designed and implemented with discrete components at an operating frequency of 48 MHz to serve as proof-of-concept. This first prototype used DPWM to generate the discrete set of PA amplitude levels required by the AMO system. A block diagram of the AMO system using DPWM is shown in Figure 4-20. We chose to use DPWM rather than



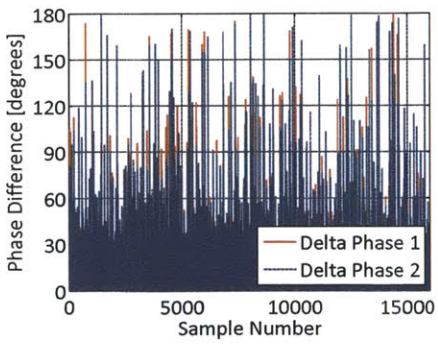
(a) 16-QAM input data



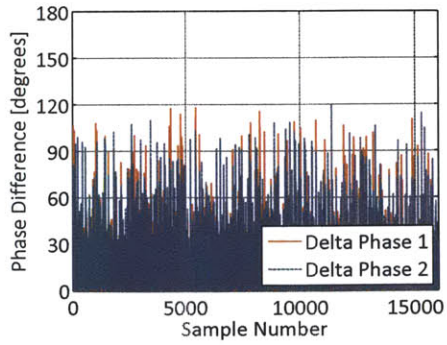
(b) PA phases w/o optimal assignment



(c) PA phases with optimal assignment



(d) Non-optimal phase differences



(e) Optimal phase differences

Figure 4-18: The PA phases and phase differences after the AMO signal decomposition with and without the optimal outphasing assignment.

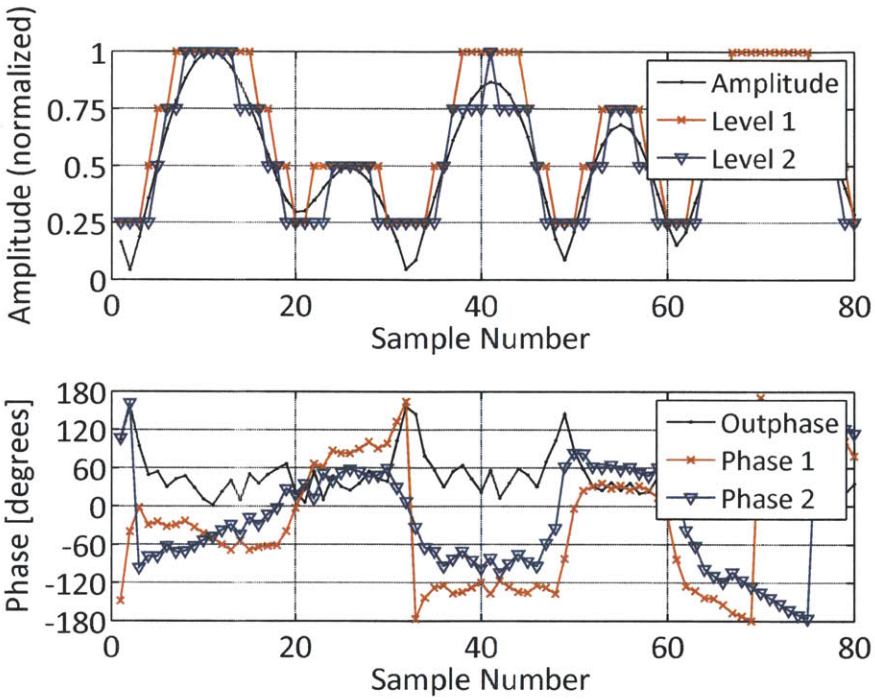


Figure 4-19: Time-domain waveforms of the PA amplitudes and phases resulting from the AMO signal decomposition with DPD, A_1, A_2, ϕ_1, ϕ_1, for a segment of the 16-QAM signal shown in Figure 4-18(a), using the example measured data shown in Figure 4-15. The amplitude of the input signal and the outphasing angle between the two PAs is also shown.

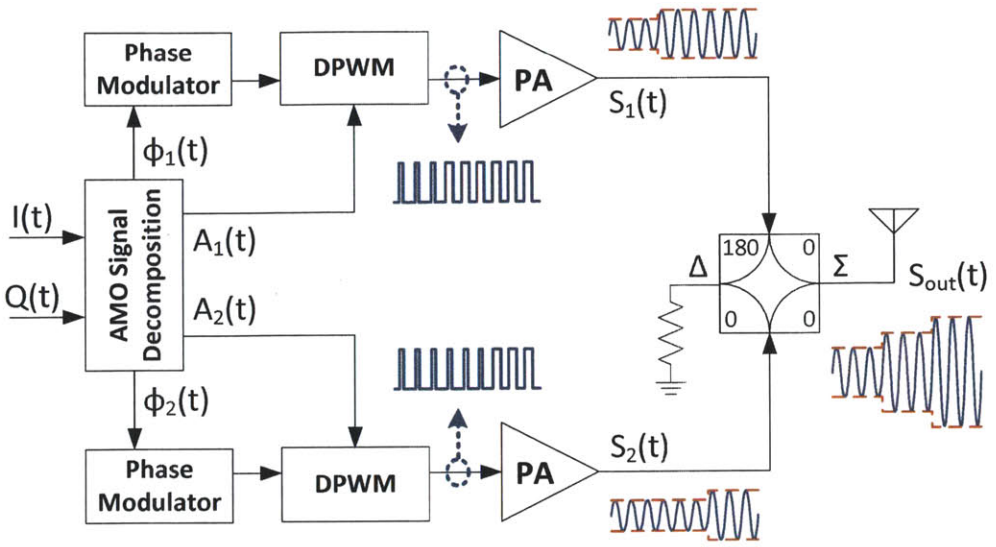


Figure 4-20: Asymmetric multilevel outphasing (AMO) transmitter with discrete pulse-width modulation (DPWM).

DSVM for the first proof-of-concept prototype because it is much easier to implement. PWM can be implemented by modulating the bias voltage of the PA input. This is easier than modulating the PA supply voltage, which involves very large voltages and currents.

4.5.1 Transmitter Implementation

Figure 4-21 shows a circuit schematic of the 48-MHz prototype. This prototype is identical to the prototype described in Section 3.6, except for the input bias network of the PA, which was modified to implement the DPWM. Each class-E PA was implemented using the ST Microelectronics PD57060 RF LDMOS, and was designed for a supply voltage of 12 V with 10-W output power. Thus the maximum output power of the prototype outphasing PA is 20 W. Four parallel Fairchild NC7ZW04 CMOS inverters provide the gate drive. The power combiner used in the prototype consists of two 1:1 transformers, each implemented with 18-AWG 5-turn bifilar windings on a Ferronics Cobalt-Nickel ferrite toroid core. The pulse width of each class-E PA is controlled by varying the gate bias voltage of the main transistor, as shown in Figure 4-21.

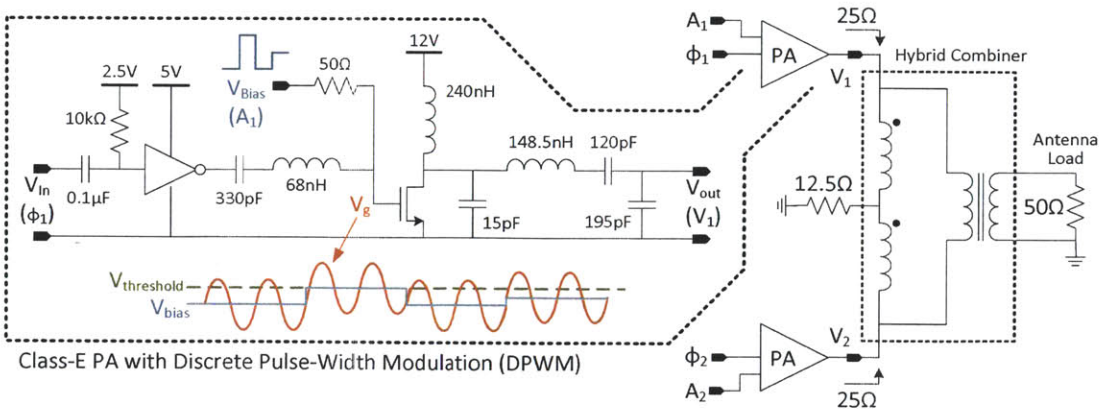


Figure 4-21: Prototype 48-MHz AMO transmitter with DPWM.

4.5.2 Measurement Results

Figure 4-22 shows the measured PWM power-added efficiency (PAE) vs. output power for the prototype transmitter. For a given number of PA amplitude levels, this data can be used to find the optimum set of DPWM levels that maximize the AMO efficiency for a given amplitude PDF. In this work we chose to use four DPWM levels, and we tested our system with a 50-kHz 16-QAM signal with a PAPR of 6.5 dB. The corresponding optimum efficiency curve for the AMO prototype is shown in Figure 4-22. It can be seen that the AMO system with DPWM provides a significant efficiency improvement over the standard LINC system over a large output power range, and that the AMO curve closely approximates the PWM efficiency curve.

Figure 4-23 shows the measured amplitude and phase of the output voltage at the fundamental of the RF output frequency versus the outphasing angle. The phase measurements are normalized to the output phase at the maximum output power. There are 10 different curves, each for a different combination of discrete pulse widths for the 2 outphased PAs. Due to PA mismatch, some combinations cannot achieve zero output amplitude even when both PAs use the same discrete pulse width and are completely out of phase, as can be seen in Figure 4-23. Thus it is important that the discrete levels and combinations are chosen to achieve sufficient amplitude dynamic range while maximizing the overall efficiency. Figure 4-24 gives the amplitude and phase linearity plots for the measurement data given in Figure 4-15. Figure 4-24(a)

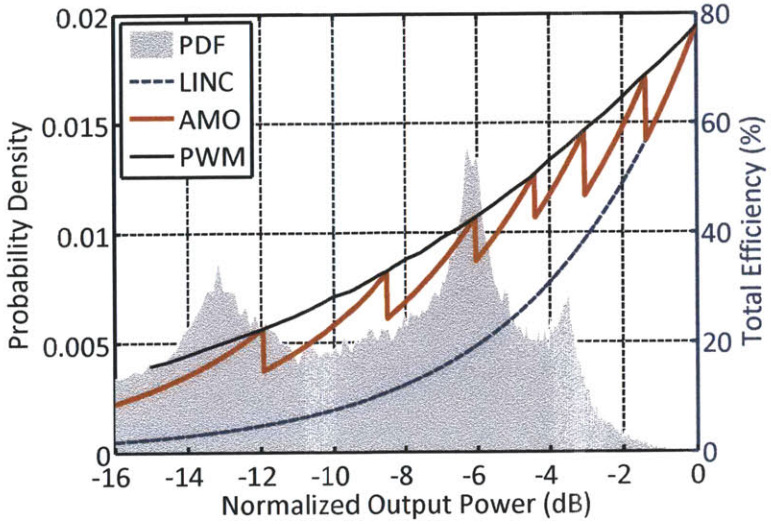


Figure 4-22: Measured PWM power-added efficiency vs. output power, along with the 4-level AMO efficiency optimized for a 16-QAM signal with 6.5-dB PAPR. The PDF of the 16-QAM signal is also shown.

plots the difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. Figure 4-24(b) plots the measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2. As explained previously, the difference between the ideal and measured curves is due to the mismatch between the two outphasing paths, as well as the varying duty cycle. A lookup table constructed from the data in Figure 4-23 is used to correct for the static nonlinearities of the prototype AMO system, following the AMO predistortion algorithm described in Section 4.4.

To demonstrate the linearity of the OPERA system, we tested the prototype with a 50-kHz 16-QAM signal with a PAPR of 6.5 dB and a carrier frequency of 48 MHz. A block diagram of the testbench is shown in Figure 4-25. The digital baseband data generation and associated signal processing were performed in MATLAB and uploaded into the internal memory of Tektronix AFG3102 arbitrary function generators (AFGs). The baseband phase data for each PA was upconverted to 48 MHz with an Agilent 4430 series vector signal generator. The output of the AMO prototype was fed into an HP 89400 vector signal analyzer for spectrum and error-vector

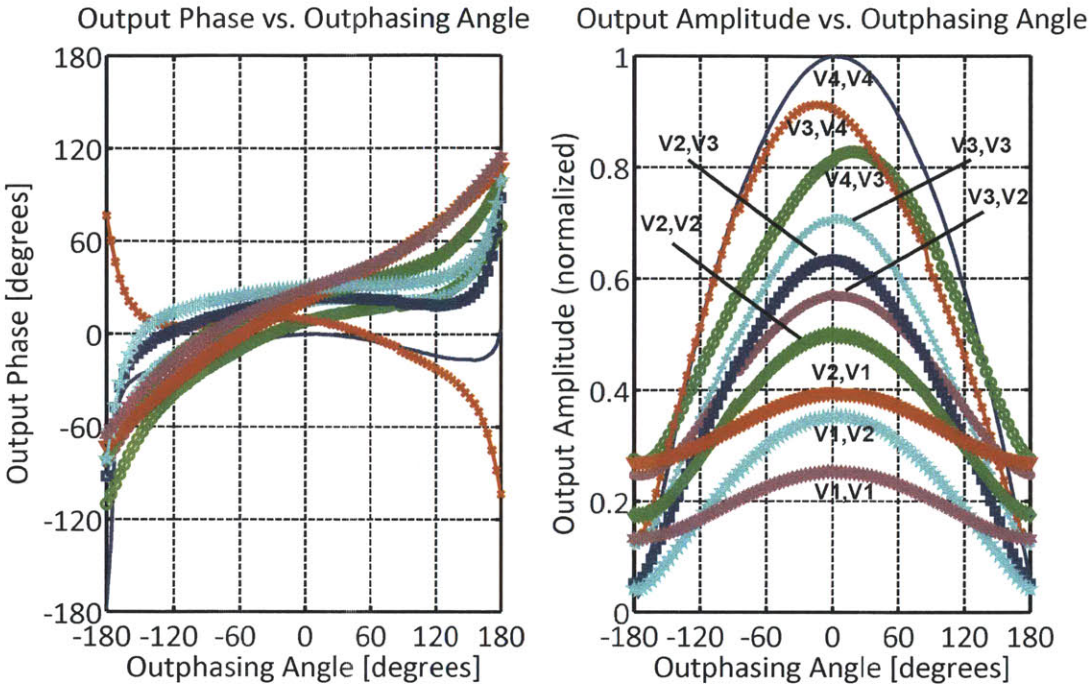
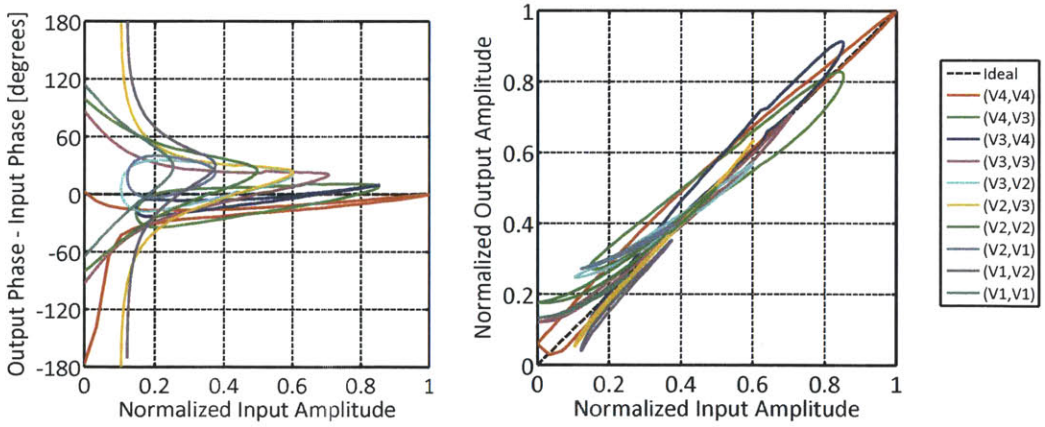


Figure 4-23: Measured output amplitude and phase vs. outphasing angle for the prototype AMO system with DPWM. Each curve corresponds to a different combination of discrete pulse widths for the two outphased PAs.



(a) Static Phase Nonlinearity

(b) Static Amplitude Nonlinearity

Figure 4-24: Amplitude and phase linearity plots for the measurement data given in Figure 4-23. (a) Difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. (b) Measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2.

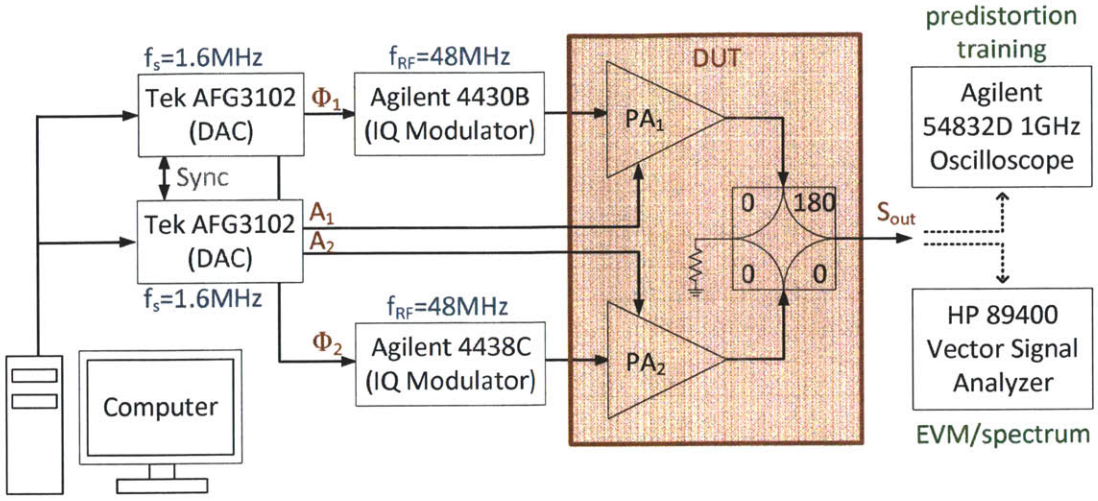


Figure 4-25: Outphasing system testbench for 50-kHz 16-QAM transmission at a carrier frequency of 48 MHz.

magnitude (EVM) analysis. Figure 4-26 shows the measured demodulated 16-QAM constellation of the prototype for both the standard LINC case and for the AMO-DPWM system after predistortion (PD). After predistortion, the EVM is reduced to about 1.0% for both LINC and AMO cases. Figure 4-27 shows the measured output spectrum for the 50-kHz 16-QAM transmission. The adjacent channel power ratio (ACPR) is better than -45 dBc after predistortion, and there is not much difference between the LINC and AMO cases, demonstrating the high linearity of the AMO system. For the 16-QAM signal with 6.5-dB PAPR, the AMO system improves the overall efficiency from 17.1% to 36.5% compared to the standard LINC system, an efficiency improvement of more than 2x.

4.5.3 Summary

The 48-MHz, 20-W AMO prototype using class-E PAs with DPWM was able to successfully demonstrate the feasibility of the AMO system to greatly increase transmitter efficiency compared to the standard outphasing system. However, this prototype operated at a frequency much lower than those used in modern wireless communcation systems, which are typically in the GHz range. Furthermore, the bandwidth of the 16-QAM test signal was quite low relative to the carrier frequency, so that wide-

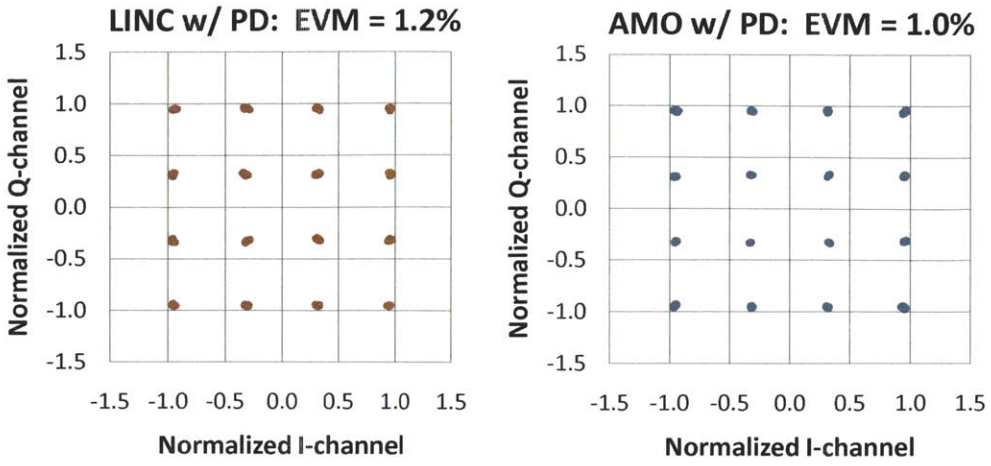


Figure 4-26: Measured demodulated 16-QAM constellation with 6.5-dB PAPR and 50-kHz bandwidth. The EVM is also shown.

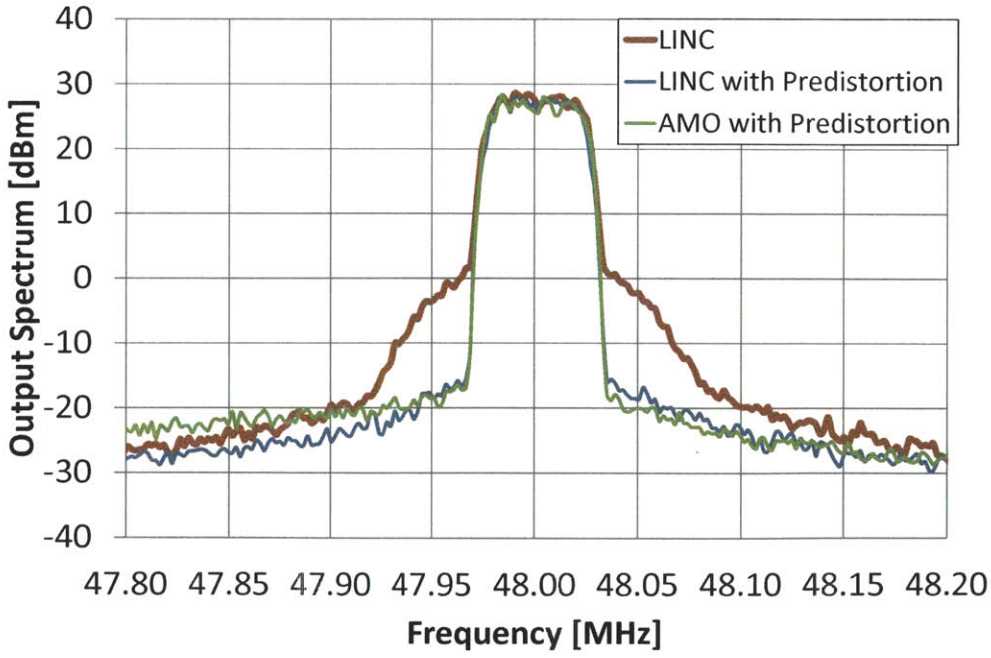


Figure 4-27: Measured transmit spectrum of the 50-kHz, 16-QAM signal for both the LINC and AMO-DPWM systems.

band RF transmission was not demonstrated. This was due to the limited bandwidth of the PAs used in the prototype. Finally, the theoretical efficiency of the AMO system using DPWM is not as high as the AMO system using DSVM. These three things—higher RF carrier frequencies, higher bandwidth, and DSVM—still needed to be demonstrated. This was the purpose of the next two prototypes, one designed for high output power intended for basestation applications, and the other designed for an integrated circuit intended for mobile wireless applications. The basestation prototype will be described next, while the details of the IC prototype will be given in Chapter 5.

4.6 1.95-GHz Basestation Prototype using DSVM

To demonstrate the feasibility of the AMO system for cellular basestation applications, a prototype was designed and implemented with discrete components at an operating frequency of 1.95 GHz and with a peak output power of 18 W. This prototype used DSVM to generate the discrete set of PA amplitude levels required by the AMO system. A block diagram of the AMO system using DSVM is shown in Figure 4-28.

4.6.1 Class-E GaN Power Amplifier

Figure 4-29 shows the circuit schematic of the 10-W class-E GaN PA designed for the AMO transmitter prototype. The PA was designed using the methodology described in [56, 57], and the target design frequency was 2.14 GHz. Load-pull and source-pull simulations were performed in the Agilent advanced design simulator (ADS) to characterize the optimum output and input impedances for the Cree GaN CGH40010 transistor at the fundamental, 2nd harmonic, and 3rd harmonic of the RF carrier frequency. The optimum impedances for maximum efficiency are shown in the Smith chart in Figure 4-30. As detailed in [57], the input and output matching networks were implemented using transmission lines, with the harmonic terminations implemented using quarter-wave open-circuit stubs. The maximum power-added efficiency (PAE)

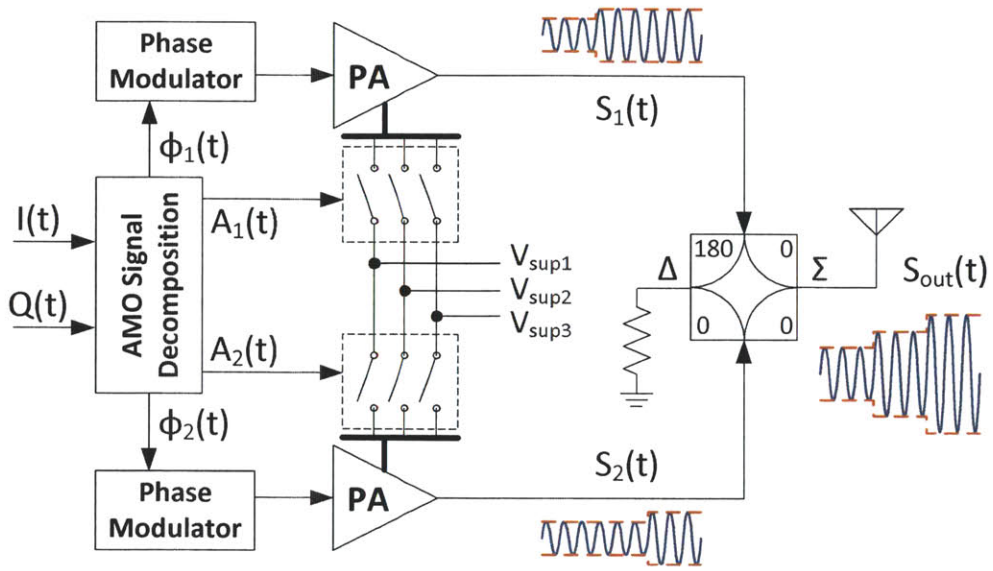


Figure 4-28: Asymmetric multilevel outphasing (AMO) transmitter with discrete supply-voltage modulation (DSVM). Three supply voltages are shown in the figure, but there can be any number of supply voltages greater than 1 for the AMO system.

from simulation, including losses from printed circuit board (PCB) traces and discrete components, was 80.1% with 39.4-dBm output power and 12.8-dB gain at V_{DD} of 28 V. Figure 4-31 shows the drain voltage and current waveforms after deembedding package parasitics, exhibiting the zero-voltage switching characteristics of class-E operation.

Figure 4-32 shows the fabricated class-E GaN HEMT PA, made with a low-loss Rogers 4350B dielectric. The PA was designed for a target operating frequency of 2.14 GHz, but after fabrication the optimum frequency was found to be 1.95 GHz. Figure 4-33 shows the measured PA output power vs. frequency for different PA supply voltages. The plot shows that the maximum output power at the highest supply voltage of 28 V occurs at 1.94 GHz. Figure 4-34 shows the measured drain efficiency and PAE vs. frequency for different PA supply voltages. Note that at 1.94 GHz, there is high efficiency at all the different supply voltages. This is important because we will use use discrete supply-voltage modulation in the AMO prototype. Thus, we chose 1.94 GHz as the operating frequency of the PA, due to the high peak output power and the high efficiency at power backoff.

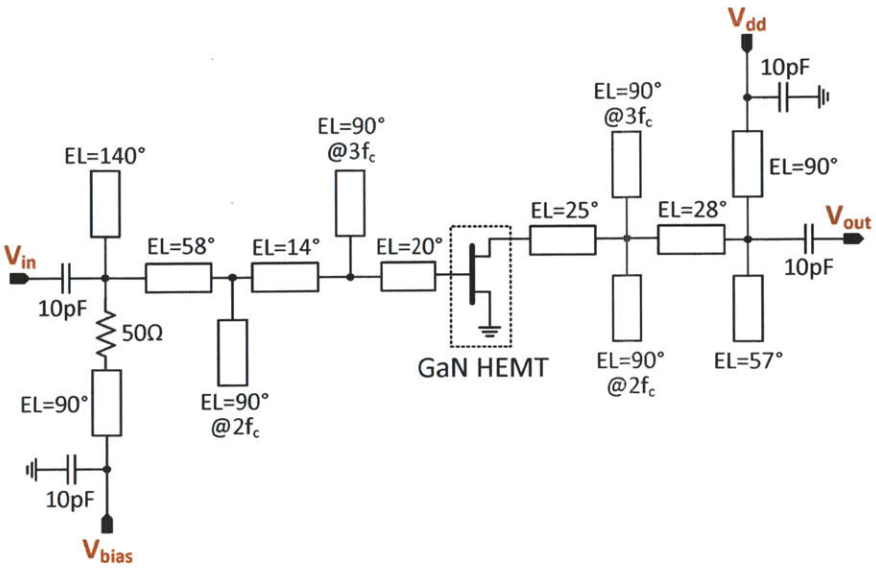


Figure 4-29: Circuit schematic of the 10-W class-E GaN PA. The design frequency was 2.14 GHz. EL stands for the electrical length of the given transmission line, and f_c stands for the RF carrier frequency.

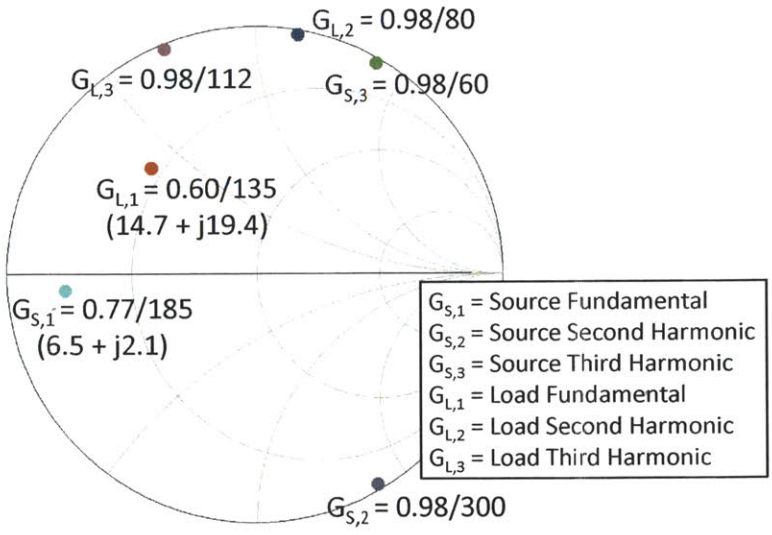


Figure 4-30: Optimum input and output impedances at the fundamental, 2nd harmonic, and 3rd harmonic of the RF carrier frequency for maximum efficiency for the class-E GaN PA.

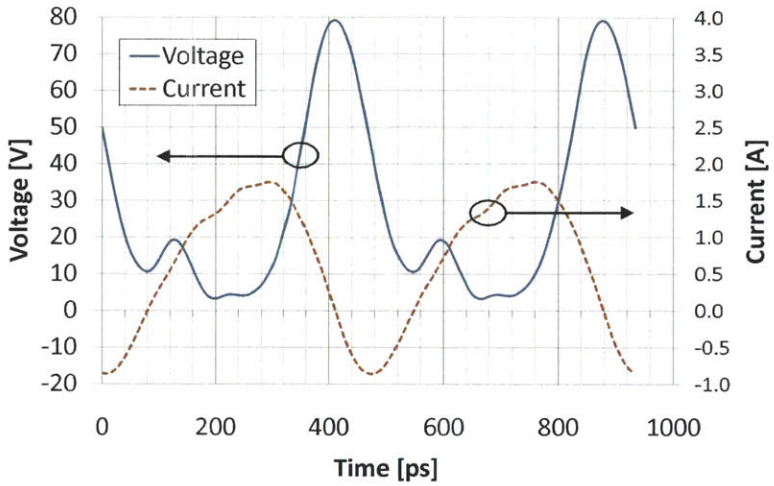


Figure 4-31: Simulated drain voltage and current for the class-E GaN PA after deembedding package parasitics, indicating class-E operation. The design frequency was 2.14 GHz.

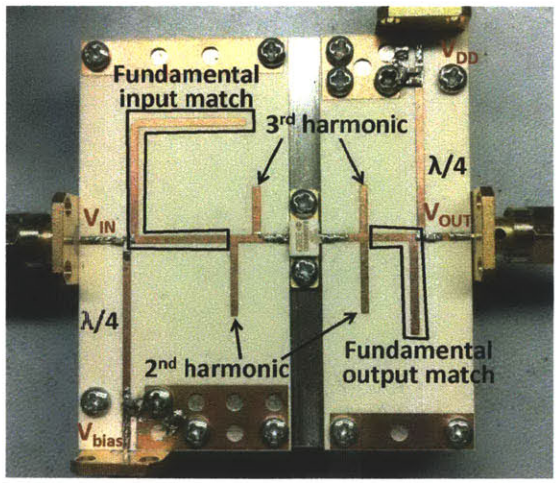


Figure 4-32: Photograph of the fabricated class-E GaN PA for the 1.95-GHz AMO prototype.

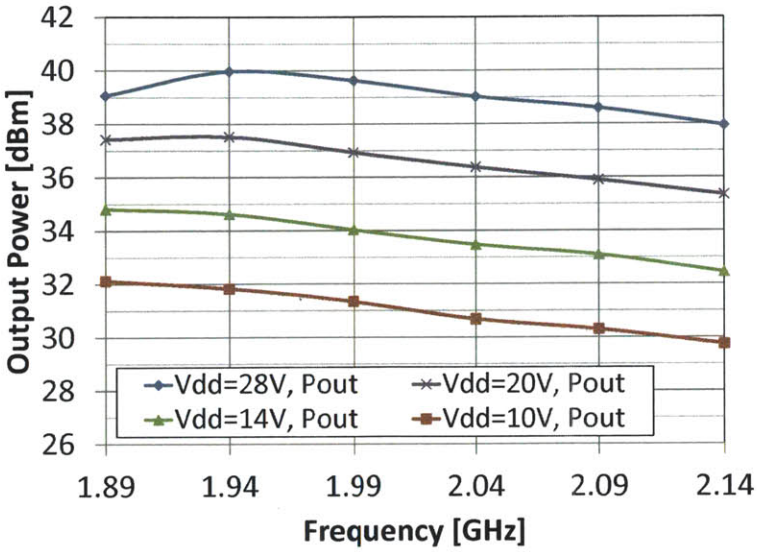
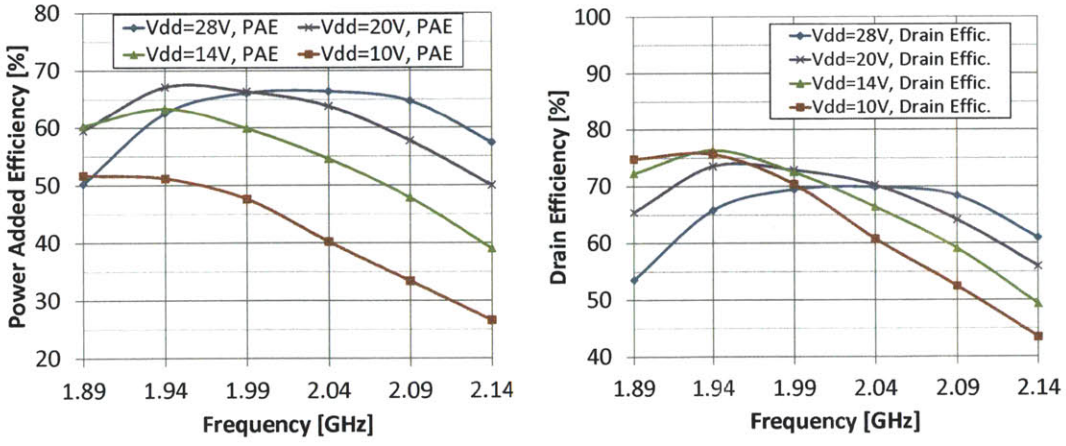


Figure 4-33: Measured output power vs. frequency at various supply voltages for the class-E GaN PA.



(a) PAE

(b) Drain Efficiency

Figure 4-34: Measured PAE (a) and drain efficiency (b) vs. frequency at various supply voltages for the class-E GaN PA.

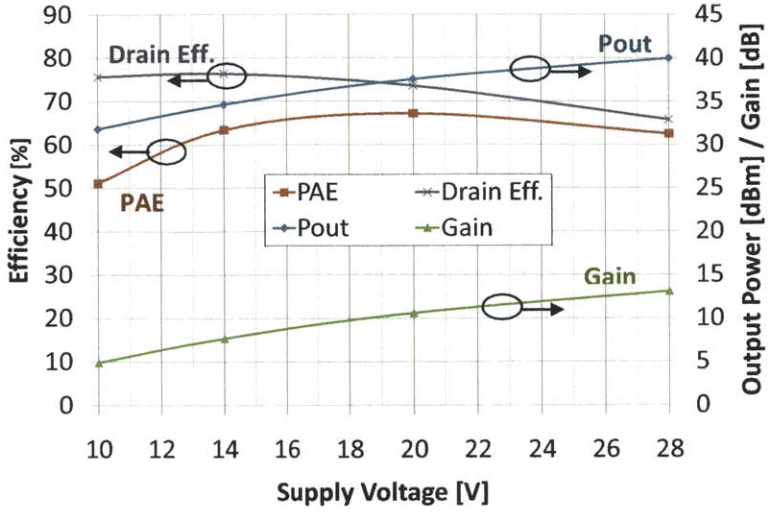


Figure 4-35: Measured PAE, drain efficiency, output power, and gain of the class-E GaN PA at 1.95 GHz.

Figure 4-35 shows the measured PAE, drain efficiency, output power, and gain of the Class-E GaN PA at 1.95 GHz. At the 40-dBm peak output power, the PAE is 62.5% with 13-dB gain. The peak PAE is 67% occurs at 20-V supply voltage. Although drain efficiency is better at lower supply voltages, the PAE is degraded due to the fixed input power used to drive the PA. It should also be noted that the PAE remains high, above 50%, over an 8-dB output power range. Because the AMO prototype will use discrete supply-voltage modulation, it is important that the PA maintain high efficiency at lower supply voltages.

4.6.2 Discrete Supply-voltage Modulator

Figure 4-36 shows the circuit schematic of the 4-level discrete supply modulator implemented in this work. Silicon LDMOS transistors from Polyfet (L8821P) were used for the supply voltage switches, and reverse current flow was prevented by using SS16 Schottky diodes from Fairchild Semiconductor. The gates of the power supply switches are driven with NC7WZ04 inverters from Fairchild Semiconductor. A 1-W isolated, unregulated dc-dc converter (TI model DCP010505BP) provides the 5-V power supply for the inverters driving the supply switch gates, whose reference

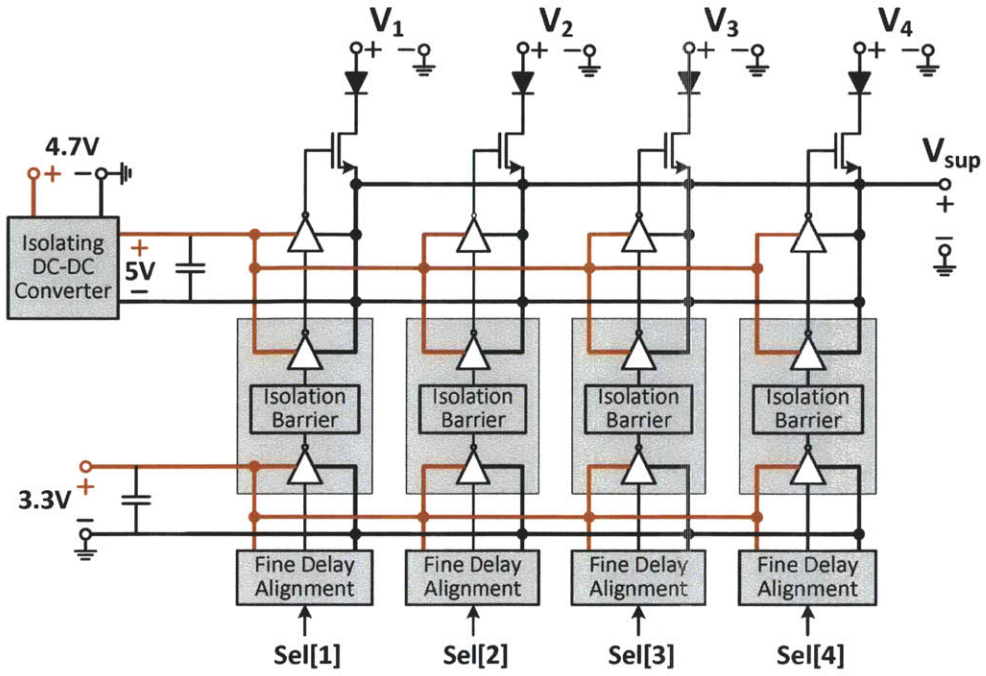


Figure 4-36: 4-level discrete supply modulator for the 1.95-GHz AMO prototype.

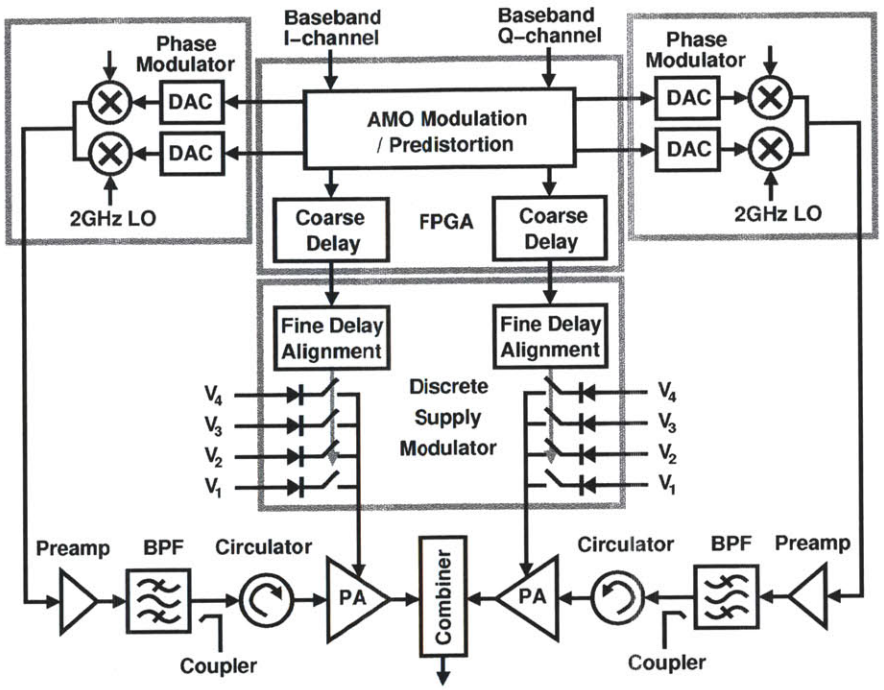
ground potential is determined by the supply modulator amplitude setting. This low-voltage configuration reduces the power loss associated with driving the gates of the power supply switches, which must block voltages up to 28 V. Another source of power loss in the discrete supply modulator is due to the diode voltage drop, which is acceptable in base-station applications where the supply voltages are as high as 28 V. The inverter gate drivers are driven by Si8423 digital isolators from Silicon Labs, which are in turn driven by MC100EP196B programmable delay chips from ON-Semiconductor. The delay chips implement fine delay adjustment for time alignment among the supply switch control signals as well as time alignment between the amplitude and phase paths.

4.6.3 Transmitter Measurement Results

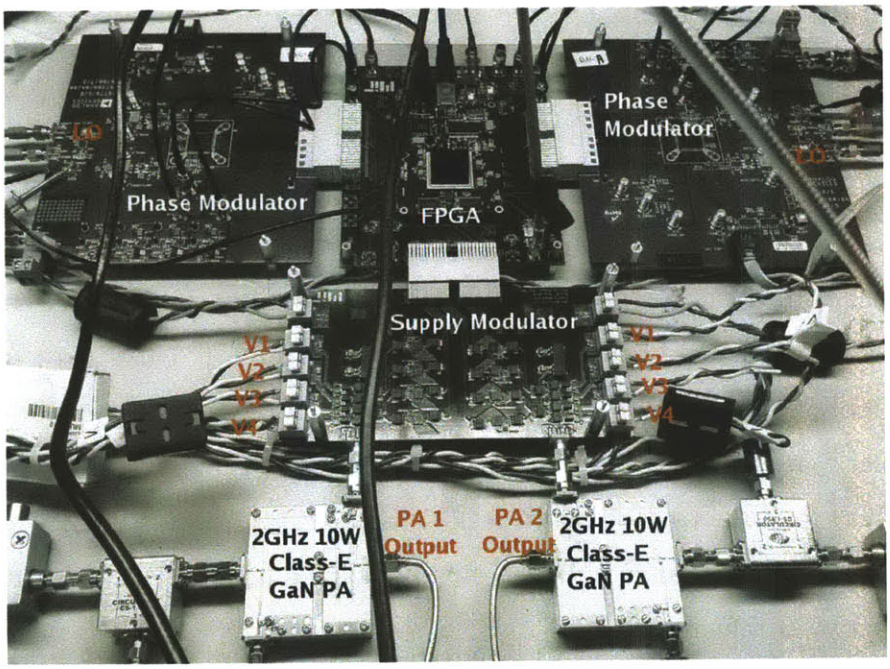
Figure 4-37 shows the prototype 18-W, 1.95-GHz AMO transmitter, which uses two class-E GaN PAs and two discrete supply modulators. Digitally pre-distorted baseband data was generated by MATLAB after characterizing the AMO transmitter with

a narrowband training signal. The two phase modulators were each implemented by a 16-bit dual-channel DAC evaluation board from Analog Devices (AD9779A). The evaluation board includes an I/Q modulator to upconvert the baseband data to the RF carrier frequency. The output of the I/Q modulators are connected to two predriver amplifiers, a Mini-circuits amplifier (ZX60-3011-+) followed by an Analog Devices amplifier (ADL5323). The output of the last predriver is connected to a Mini-circuits band-pass filter (VBFZ-2000-S+), followed by an E-Meca circulator (CS-1.950), which is then connected to the class-E GaN PA. The filter removes any undesired harmonics generated by the predriver amplifiers, while the circulator ensures that the preceding circuitry is terminated by 50 Ω and redirects reflected power from the class-E GaN PA to a load [52]. An FPGA provides the digital inputs to the phase modulators and the discrete supply modulators, and also performs coarse time alignment between the phase and amplitude paths. Fine time alignment is performed by programmable delay lines in each supply modulator. The supply modulators provide two independent supply voltages selected from four different power supplies to the two class-E PAs.

Figure 4-38 shows the measured AMO transmitter total efficiency vs. output power. Here we define the total efficiency as $\eta_{tot} = P_{out}/(P_{DC} + P_{in})$. It should be noted that the efficiency numbers include the insertion loss from the isolating power combiner, which is approximately 0.4 dB. The blue curve is the efficiency for standard outphasing using a single supply voltage, and it can be seen that the efficiency drops quickly as the amount of power backoff increases. The black curve is the efficiency as the supply voltage is varied for both PAs together. We cannot operate directly on the black curve because it would require continuous supply-voltage modulation, which suffers from the tradeoff between efficiency and bandwidth. Instead, we use the AMO system, which combines discrete supply-voltage modulation with outphasing. The red curve is the efficiency for AMO with 4 supply-voltage levels, and it can be seen that the efficiency is much higher than the standard outphasing system, and that it closely approximates the black efficiency curve over a wide output power range. The actual supply-voltage levels chosen were optimized for a 16-QAM signal with a PAPR of 6.5 dB, the PDF of which is shown in Figure 4-38.



(a)



(b)

Figure 4-37: Prototype implementation of the 18-W 1.95-GHz AMO transmitter with discrete supply modulators and class-E GaN PAs. (a) block diagram, (b) photograph.

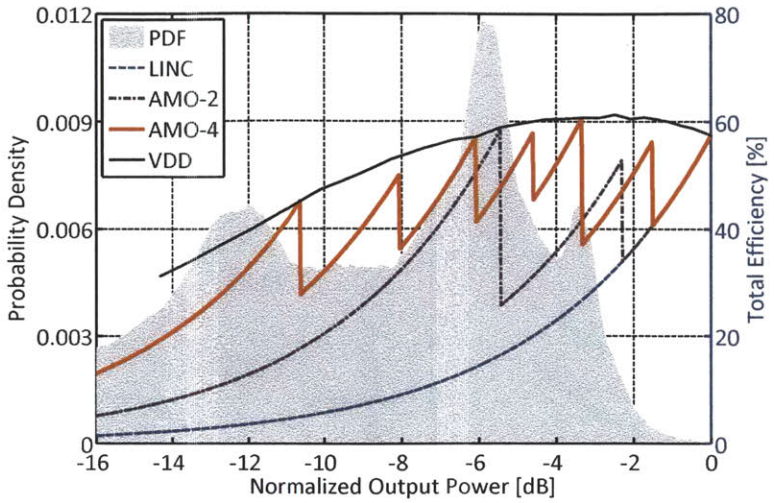


Figure 4-38: Measured efficiency vs. output power for the 1.95-GHz AMO prototype, along with the optimized amplitude levels for a 16-QAM signal with 6.5-dB PAPR. The PDF of the 16-QAM signal is also shown.

Figure 4-39 shows the measured static output amplitude and phase for the AMO transmitter depending on the supply voltage combination and the outphasing angle. There are 7 different curves, each for a different combination of supply voltages for the two outphased PAs. Figure 4-40 gives the amplitude and phase linearity plots for the measurement data given in Figure 4-39. Figure 4-40(a) plots the difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. Figure 4-40(b) plots the measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2. The difference between the ideal and measured curves represents the static nonlinearity of the prototype AMO system.

As explained in Section 4.4, there are two main sources of the static nonlinearity: (1) the mismatch between the branches of the outphasing system, and (2) the varying supply voltage. It should be noted that a mismatch between the amplitudes of the two PAs can limit the smallest amplitude achievable through outphasing, because if the amplitudes are mismatched, the two PA output signals cannot cancel each other out completely. This would result in a lower amplitude dynamic range, which can degrade linearity. To increase the amplitude dynamic range, we can tune the

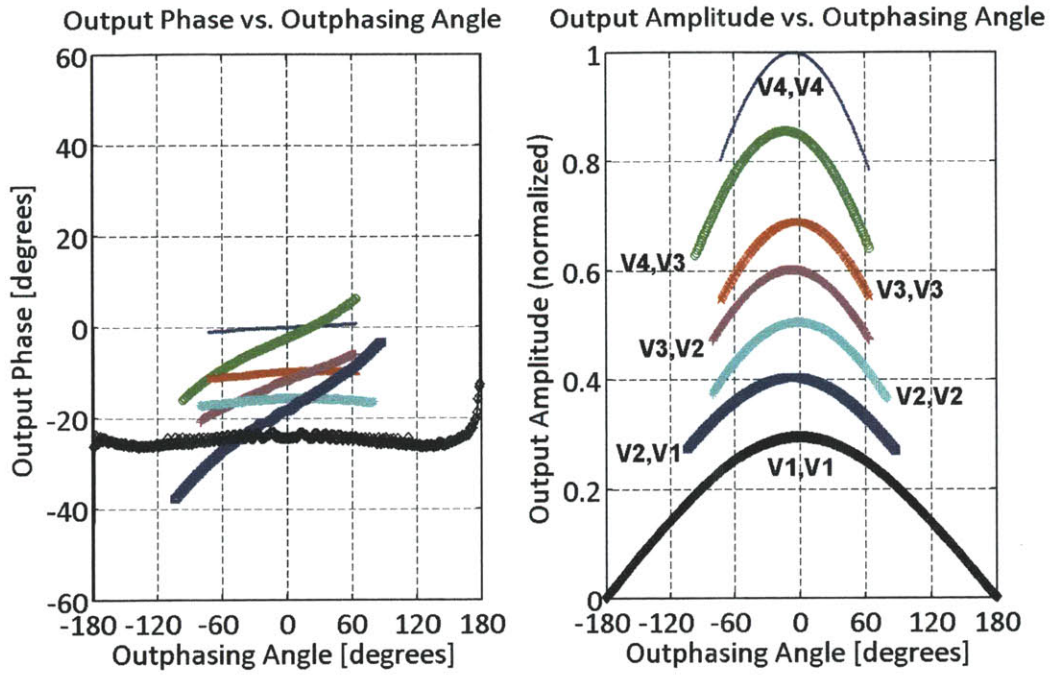
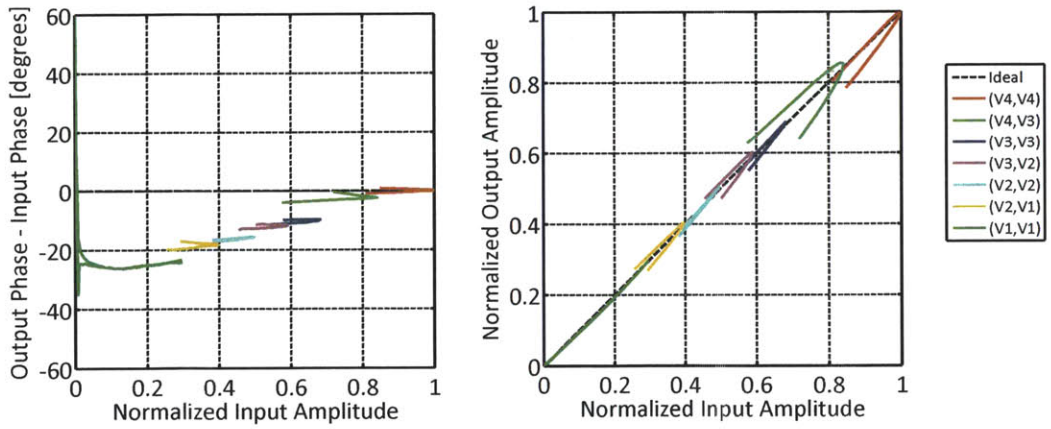


Figure 4-39: Measured static output amplitude and phase vs. outphasing angle for the 1.95-GHz AMO transmitter. Each curve corresponds to a different combination of supply voltages for the two outphased PAs.



(a) Static Phase Nonlinearity

(b) Static Amplitude Nonlinearity

Figure 4-40: Amplitude and phase linearity plots for the measurement data given in Figure 4-39. (a) Difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. (b) Measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2.

individual amplitudes for each PA by tuning the gate bias of the PAs (the V_{bias} node in Figure 4-29). Changing the PA gate bias has the effect of changing the input duty cycle of the PA, which changes the output amplitude of the PA as described in Section 2.3 and Section 4.5.1. To correct for the static nonlinearities of the prototype AMO system, we employ the AMO predistortion algorithm described in Section 4.4, using a lookup table constructed from the data in Figure 4-39.

Figure 4-41 shows the measured step response of the AMO transmitter output envelope when the supply voltage is changed from 7.5 V to 13 V for both PAs. The envelope settles in less than 15 ns. The nonzero settling time is caused by the finite bandwidth of the discrete supply modulator and/or the PA. Because the supply voltage levels switch abruptly in the AMO system, this nonzero settling time will speed of the AMO system. The effect is similar to inter-symbol interference, so that as the data-rate of the transmitted signal is increased, the higher the noise and distortion that will appear in the output. Although nonzero settling time of the PA introduces error-vector magnitude (EVM) and spectrum degradation, 30–40-dBc adjacent channel power ratio (ACPR) with up to 40-MHz channel bandwidth can be obtained without any step response calibration or correction. Because the phase modulator typically provides much faster settling time, when higher ACPR is desired, a phase-domain envelope-correction technique could be implemented. For comparison, Figure 4-42 shows the measured step response of the AMO transmitter when the outphasing angle is changed with a fixed supply voltage. Note that the envelope settles much faster for the phase step than the amplitude step, in less than 5ns. The nonzero settling time in this case is caused by the finite bandwidth of the phase modulator and/or the PA.

To validate the performance of the AMO system for wireless data transmission, a 16-QAM signal was transmitted with the prototype at various symbol rates. Figure 4-43 shows the constellation diagrams at two different symbol rates, one at 2.5-MSym/s and the other at 40-MSym/s. At 2.5 MHz, the EVM is 2.0%, and at 40 MHz, the EVM is 3.2%. As explained above, the EVM degrades at higher symbol rates due to the finite settling time of the output when the PA amplitudes and phases change abruptly

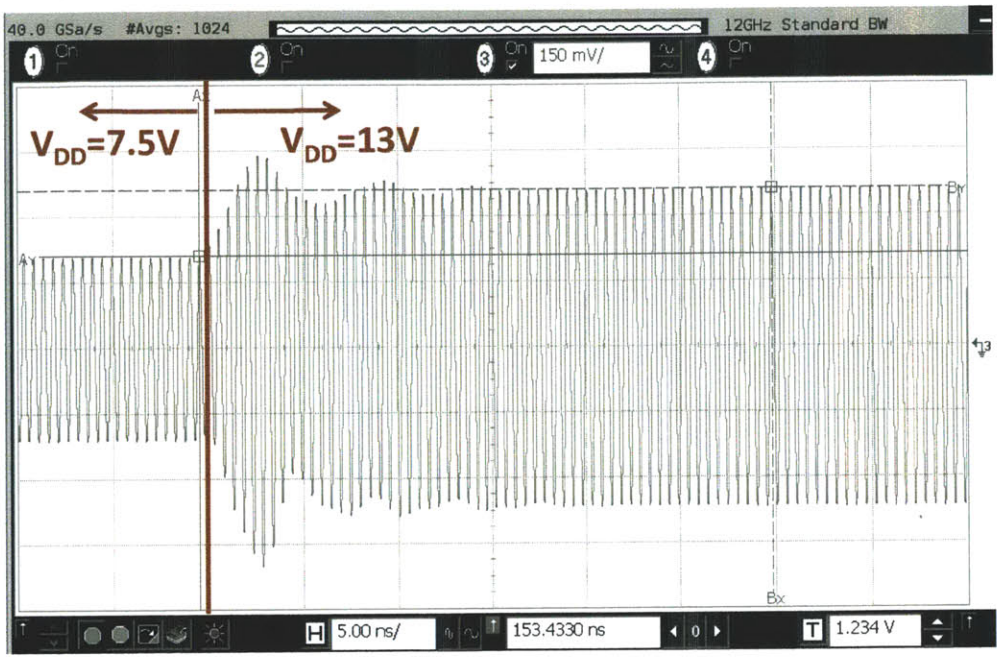


Figure 4-41: Measured step response of the 1.95-GHz AMO transmitter output envelope when the supply voltage is changed from 7.5 V to 13 V.

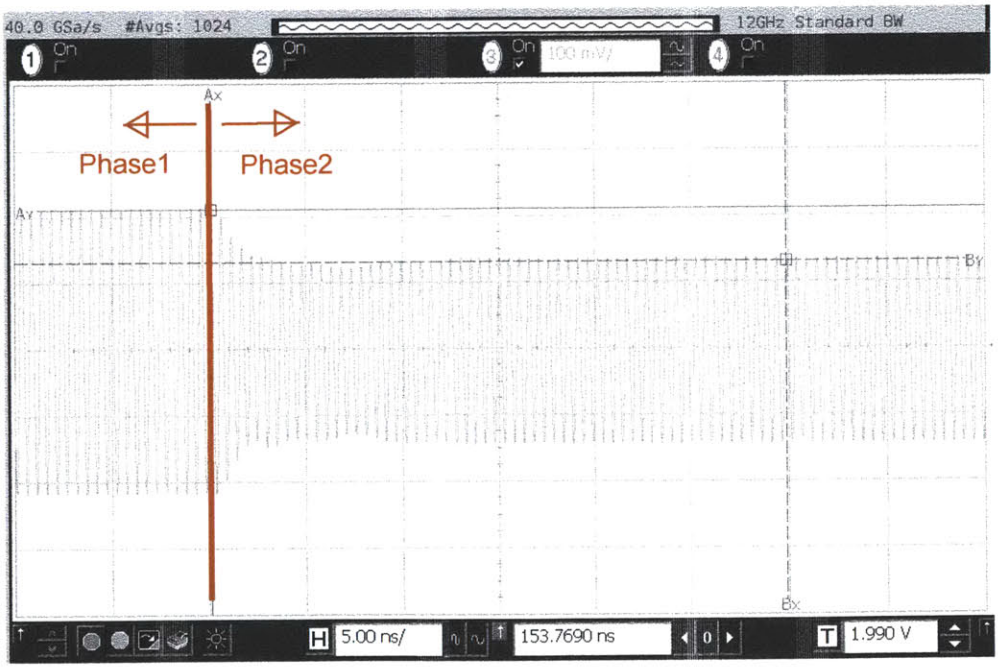


Figure 4-42: Measured step response of the 1.95-GHz AMO transmitter output envelope when the outphasing angle is changed from one value to another with a fixed supply voltage.

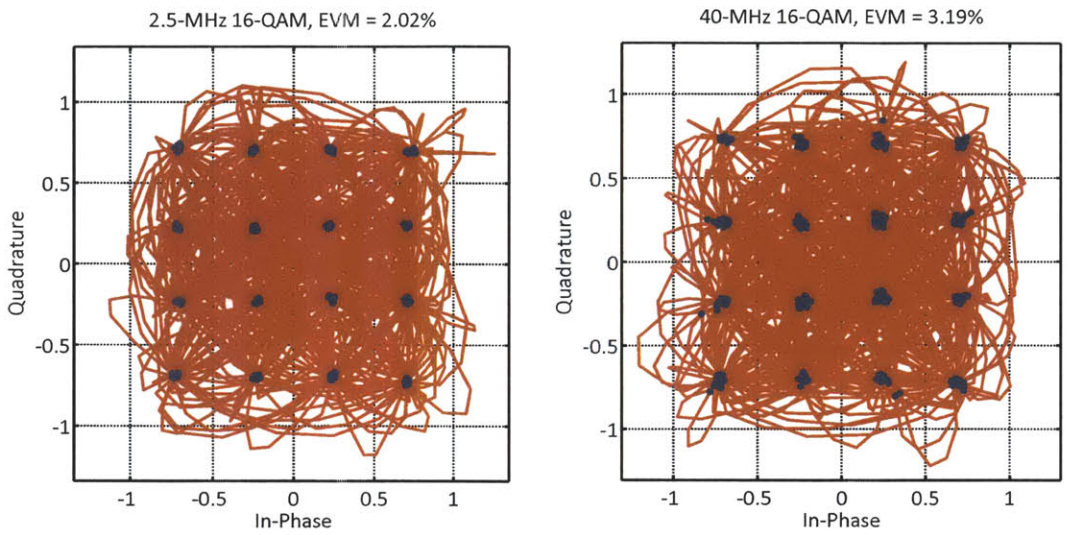
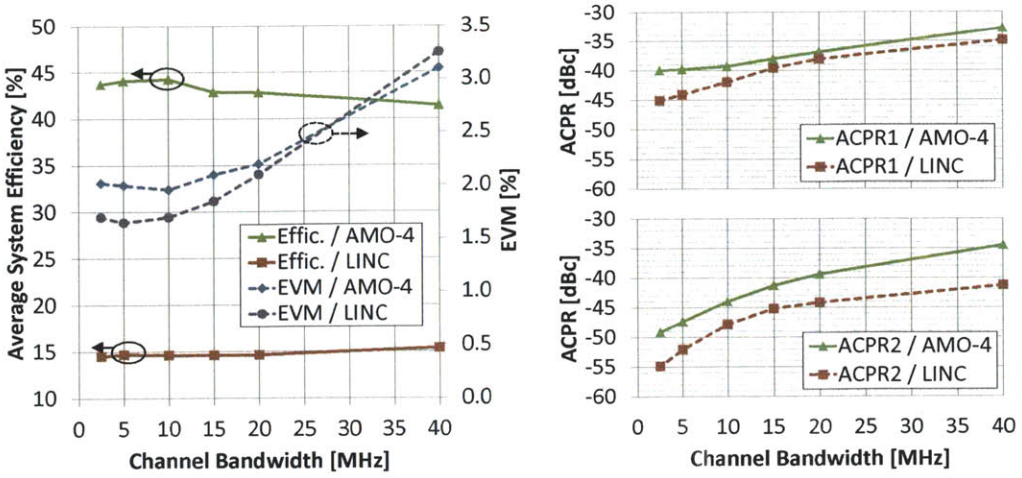


Figure 4-43: Constellation diagram of a 16-QAM signal transmitted by the AMO system at 2.5 MHz and 40 MHz symbol rate for the 1.95-GHz AMO transmitter. (a) 2.5 MHz. (b) 40 MHz.

in the AMO system. However, even the worst-case EVM of 3.2% is acceptable for most applications.

Figure 4-44 shows the average system efficiency, ACPR, and EVM of the prototype AMO transmitter for the 16-QAM signal transmission with various channel bandwidths from 2.5 to 40 MHz. For comparison purposes, we also show the results for the LINC case, when only a single supply voltage is used for both PAs. The sampling rate of the digital data was set to 10x the symbol rate for all channel bandwidths except for 40 MHz, in which case the sampling rate was 200 MHz (5x the symbol rate). This is due to the speed limitation of the DACs used in the phase modulators, which had a maximum sampling rate of 200 MHz. The average system efficiency numbers include the power consumption from the discrete supply modulators and is defined as $\eta_{sys} = P_{out}/(P_{DC} + P_{in} + P_{SupMod})$.

From the plots, we can see a significant improvement in the efficiency for 4-level AMO vs. LINC, from 15% to almost 45%. The efficiency of the AMO system drops slightly at higher symbol-rates due to the dynamic losses from the DSVM, but the



(a) (b)

Figure 4-44: Performance comparison of the LINC and 4-level AMO systems for the 1.95-GHz AMO prototype, for the transmission of a 6.5-dB PAPR 16-QAM signal at various channel bandwidths. (a) EVM and average system efficiency. (b) ACPR at 1st and 2nd channel offsets.

efficiency degradation is very small, demonstrating the high efficiency of the discrete supply modulators. The EVM for both the LINC and AMO cases is around 2% for symbol rates 20 MHz and below. The EVM is degraded slightly for the AMO system, but the degradation is very small. However, the degradation is ACPR is more significant, as shown in Figure 4-44(b). At the 1st channel offset, the degradation is 2-4dB when the AMO system is used, and at the 2nd channel offset, the degradation is 3-8dB. This is due to the abrupt amplitude and phase changes when the supply voltage is switched, which cause glitches in the output waveform that degrade the linearity and add noise to the signal.

Figure 4-45 shows the power breakdown for the 16-QAM signal transmission at various symbol-rates. The dark blue bars show the power consumption of the discrete supply modulators. Note that the power loss is small compared to the other sources of power loss in the system, and that the power loss does not increase significantly as the symbol-rate increases. This shows the relatively high efficiency of the discrete supply modulators, and demonstrates the potential of the AMO system to achieve both high-efficiency and high-bandwidth wireless transmission. Also shown in Figure 4-45 is the

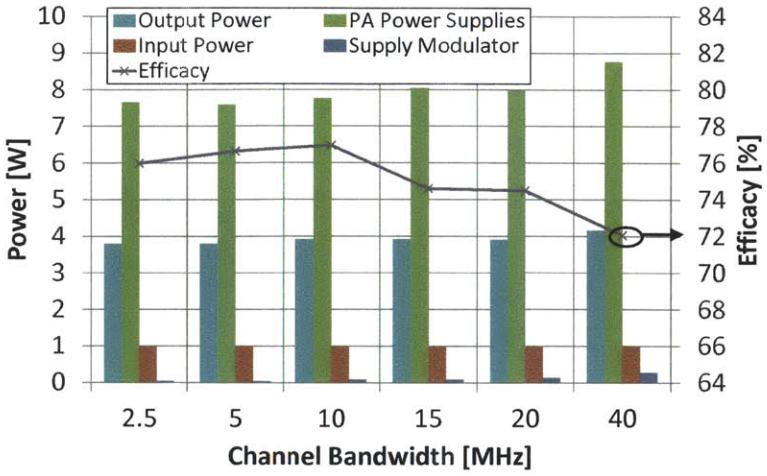
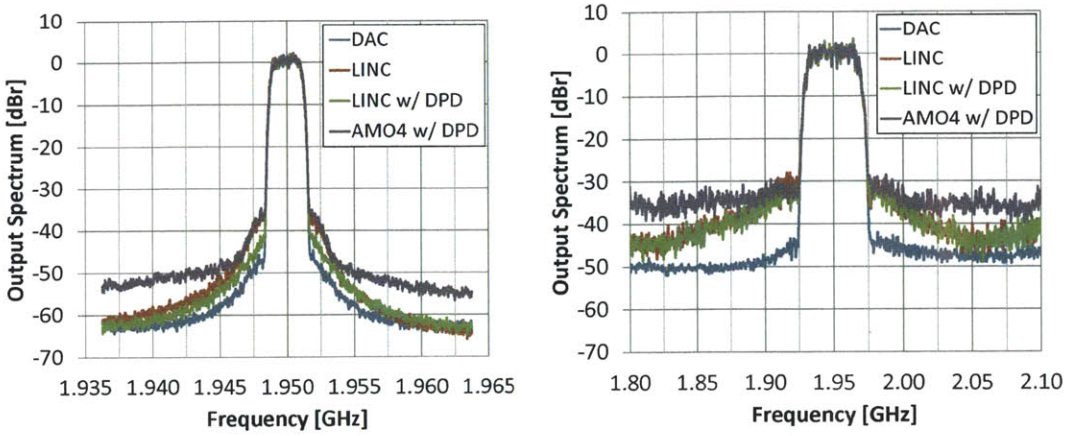


Figure 4-45: Power breakdown and efficacy of the 1.95-GHz AMO prototype for the 16-QAM signal transmission for various channel bandwidths.

efficacy of the system for the 16-QAM transmission. We define the efficacy as the ratio of the average system efficiency to the efficiency of the system at peak-envelope power (PEP). The efficacy is around 75% for all channel bandwidths up to 40-MHz, which is very high.

Figure 4-46(a) and Figure 4-46(b) show the spectrum of the 16-QAM signal transmission at 2.5-MSym/s and 40-MSym/s, respectively, for both the LINC and AMO systems. The curves labeled "DAC" show the spectrum using just the phase modulators without the PAs; these are shown as a reference for the input signal driving the AMO system. It can be seen that for either symbol rate, the noise floor of the AMO system is about 10dB higher than the LINC case. Again, this is due to the finite settling time of the PAs in response to the abrupt amplitude/phase changes, causing glitches in the output waveform which show up as a higher noise floor.

Finally, Table 4.1 compares the efficiency of the 1.95-GHz AMO transmitter with other published works in the frequency range of 2-2.6 GHz and for signal bandwidths 10 MHz or higher. Note that the AMO transmitter achieves an average drain efficiency of 50.5%, which is comparable to the state of the art. One way to further improve the efficiency is to increase the number of available supply voltages beyond the four levels used in this work. Another way is to combine the AMO system with the OPERA



(a) 2.5 MHz

(b) 40 MHz

Figure 4-46: Transmit spectrum of a 16-QAM signal at 2.5 MHz and 40 MHz symbol rate for the 1.95-GHz AMO transmitter. (a) 2.5 MHz. (b) 40 MHz.

system described in Chapter 3.

4.6.4 Summary

The 1.95-GHz, 18-W AMO prototype demonstrates the feasibility of the AMO system for cellular basestation applications. The AMO transmitter uses discrete supply-voltage modulation for fast and efficient coarse-amplitude control, and outphasing for fine-amplitude control. The 4-level AMO system improves the efficiency of the standard outphasing system by almost 3x for a 16-QAM signal with 6.5-dB PAPR and symbol rates as high as 40 MHz. The results illustrate the potential of the AMO system for both high-efficiency and wide-bandwidth power amplification.

4.7 Summary

In this chapter, we have demonstrated a new asymmetric multilevel outphasing system which greatly increases system efficiency while maintaining high linearity. Higher efficiency is obtained by dynamically switching the PA amplitudes among a discrete set of levels based on the signal envelope, reducing the amount of energy normally

System Architecture/ Author	Freq/ BW (MHz)	Modulation/ PAPR	Tech.	Peak P_{out}/ Avg P_{out} (dBm)	Peak η_D/ Avg η_D (%)	Efficacy (%)
Doherty (T. Landon, IMS 2010)	f_c=2140, BW = 10	WCDMA (2-ch), 6.5 dB	GaAs	54.5/ 48.1	72.0/ **57.0**	**79**
Doherty (J. Kim, MWCL 2010)	f_c=2655, BW = 10	WiMAX, 8.5 dB	GaN	43.5/ 36.0	73.9/ **56.8**	**77**
Doherty (I. Kim, TMTT 2010)	f_c=2655, BW = 10	WiMAX, 7.8 dB	GaN	50.5/ 42.5	59.0/ **55.4**	**94**
Doherty (H. Deguchi, IMS 2009)	f_c=2600, BW = 20	WCDMA, (4-ch), 6.9 dB	GaN	52.5/ 45.2	65.6/ **55.0**	**84**
Envelope Tracking (C. Hsia, IMS 2010)	f_c=2140, BW = 10	WiMAX, 8.8 dB	GaAs	51.8/ 43.6	77.0/ **54.1**	**70**
3-level Delta-Sigma (J. Kim, IMS 2011)	f_c=2600, BW = 10	LTE, 8.5 dB	GaN	43.0/ 34.5	–/ **53.3**	–
Class-E AMO (This Work)	f_c=1950, BW = 10	16-QAM, 6.5 dB	GaN	42.6/ 36.5	59.3/ **50.5**	**85**

Table 4.1: Performance comparison for basestation PAs in the frequency range of 2-2.6 GHz for signal bandwidths 10 MHz or higher.

wasted in the power combiner. Linearity is maintained through the use of outphasing for fine amplitude control and digital predistortion to correct for system nonlinearities.

Two different discrete-component prototype systems were presented. The first prototype, operating at 48 MHz with 20-W peak output power, used discrete pulse-width modulation to generate the discrete PA ampitude levels. This prototype was the first published work to prove the AMO concept with measurement results. The second prototype, operating at 1.95 GHz with 18-W peak output power, used discrete supply voltage modulation to generate the discrete PA amplitude levels. This prototype demonstrated the potential of the AMO system to achieve both high efficiency and wide bandwidth wireless transmission, achieving a high average system efficiency of 42% for a 6.5-dB 16-QAM signal with channel bandwidths up to 40 MHz.

Chapter 5

A 2.4-GHz, 27-dBm Asymmetric Multilevel Outphasing PA in 65-nm CMOS

To demonstrate the feasibility of the AMO system for mobile wireless applications, an IC prototype was designed and implemented in the TSMC 65-nm CMOS Mixed-Signal RF process with 9 metal layers and an ultra-thick metal (UTM) for the top layer. The target RF carrier frequency for the design was 2.4-2.5 GHz, which is the frequency band used for WLAN signals. This prototype used DSVM to generate the discrete set of PA amplitude levels required by the AMO system. A block diagram of the AMO system using DSVM is shown in Figure 4-28. Both the PA and the discrete supply-voltage modulator were implemented on the chip. These circuit blocks will be described in detail in the following sections.

5.1 Sub-optimum, Cascode Class-E PA Topology

Figure 5-1 shows the circuit schematic of the PA used in the 2.4-GHz AMO IC prototype. The single-ended version is shown for simplicity, but the PA is differential on-chip. The PA operates as sub-optimum class-E [58,59], specifically variable-voltage class-E (denoted Class-E_{VV}), in which the peak drain voltage is reduced in exchange

for a lower theoretical efficiency. The drain voltage waveforms for standard class-E and class-E_{VV} are shown in Figure 5-2(a), which shows that the class-E_{VV} waveform does not satisfy zero-voltage switching (ZVS), so that there is some power loss when the switch turns on because both the current and the voltage are nonzero at that instant. Although class-E_{VV} has a lower theoretical efficiency, the lower peak drain voltage allows for higher supply voltages so that higher output power can be obtained. The higher supply voltage also means that the required current is lower, so that the required load resistance is higher. This means that a smaller transformation ratio can be used in the output matching network, resulting is a smaller network quality factor, Q. A smaller network Q gives a wider bandwidth for the PA, and also results in less loss in the passive components (smaller Q means smaller AC currents in the inductors and capacitors, so that there is less loss in the parasitic resistances of those components). The higher required load resistance also means that the switch resistance can be higher as well, so that the transistor size can be reduced. This has the advantage of decreasing the transistor gate capacitance, reducing the power of the predriver. For these reasons, the sub-optimum class-E PA typically achieves a higher total efficiency than the standard class-E PA when implemented in CMOS, as demonstrated in [58]. Figure 5-1 shows the simulated drain voltage waveform of the PA used in the 2.4-GHz AMO IC prototype, exhibiting the non-zero voltage switching characteristic.

Referring again to Figure 5-1, the PA utilizes a thick-oxide cascode transistor (M_2) to reduce voltage stress on the main switch (M_1), a thin-oxide device. The cascode topology combines the best of two worlds: the fast switching capability of the thin-oxide device M_1 in common-source (CS) configuration, and the high voltage sustainability of the thick-oxide device M_2 in common-gate (CG) configuration [60]. M_1 has better RF characteristics than M_2, including smaller parasitic gate and drain capacitance, so that the power loss associated with charging and discharging these capacitances is reduced. The output network consists of the shunt capacitance from the cascode device and a spiral inductor for the DC feed. The matching network and series resonant filter necessary for class-E operation are implemented with the bond-

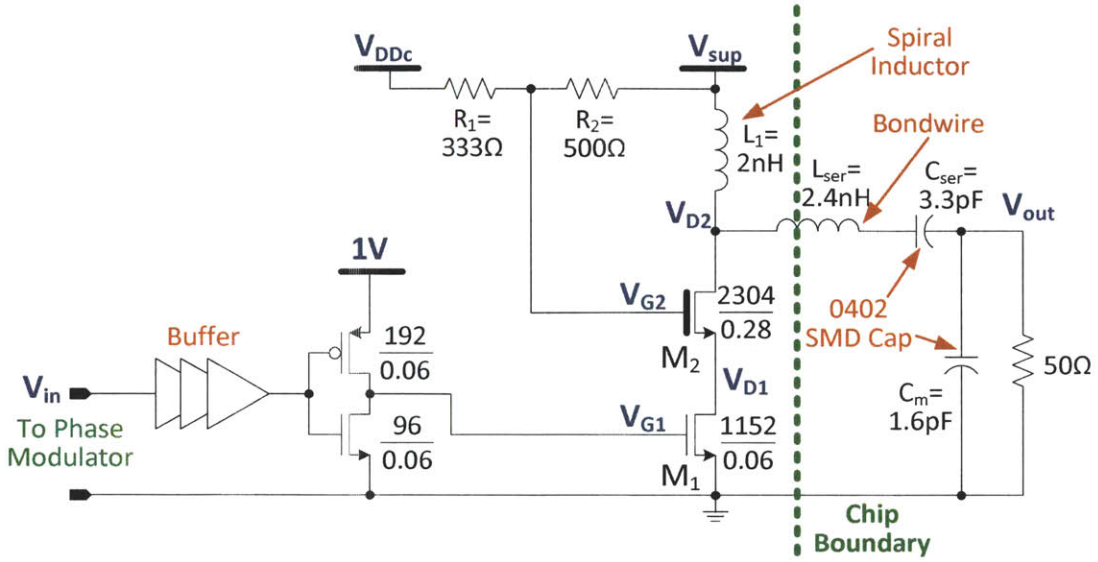


Figure 5-1: Circuit schematic of the class-E PA used in the 2.4-GHz AMO IC prototype. The single-ended version is shown for simplicity.

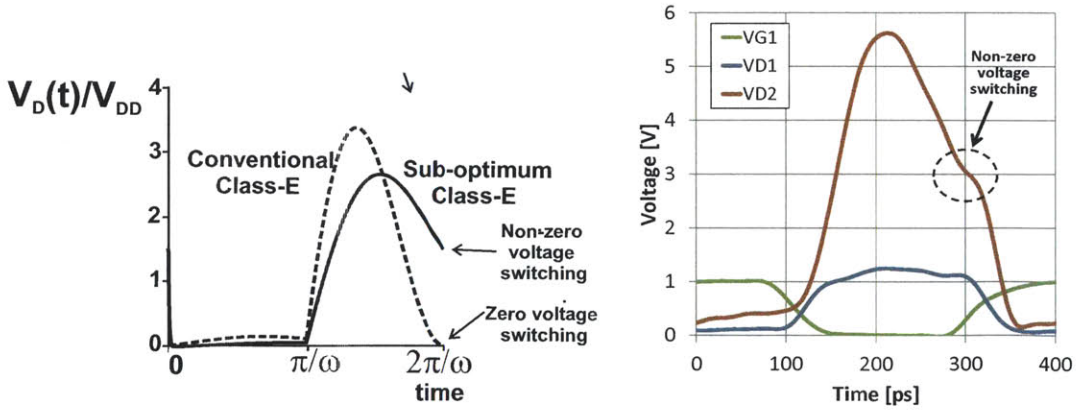


Figure 5-2: (a) Drain voltage waveforms for the conventional class-E PA and variable-voltage class-E PA. (b) Simulated drain voltage waveform for the PA used in the 2.4-GHz AMO IC prototype.

wire inductance from the chip packaging and off-chip surface mount device (SMD) capacitors.

To operate the cascode stage as a switch optimally, one needs to drive the thin-oxide device into saturation with a square-wave signal [60]. We implement an inverter-based driver utilizing thin-oxide devices (see Figure 5-1) with a sufficient driving capability. The use of an interstage matching network is redundant because of the high gain of the cascode stage and the use of the thin-oxide device as the CS device. This both eliminates the losses in this network and reduces the total die area.

5.2 Improved Self-biasing Technique for Cascode Class-E PA

The gate of the cascode device in the class-E PA is biased using a modification of the self-biasing scheme used in [60, 61]. The self-biasing topology used in their work is shown in Figure 5-3(a). For each PA supply voltage value V_{sup}, there is an optimum cascode gate voltage V_{G2}, and simulations show that the optimal value of V_{G2} depends linearly on V_{sup}. The reason for this is the parasitic capacitance at V_{D1}, the node connecting M_1 and M_2. When M_1 is turned on, V_{D1} is discharged to ground, and when M_1 is turned off, V_{D1} is charged up to $(V_{G2} - V_{T2})$, where V_{T2} is the threshold voltage of M_2. Thus, the capacitance at V_{D1} must be charged and discharged during every cycle of the RF carrier frequency. As the supply voltage is lowered, the current through M_1 and M_2 decreases, so that the cascode gate bias V_{G2} can be lowered as well. The lower V_{G2} lowers the peak voltage at V_{D1}, decreasing the CV^2 power loss and improving the overall efficiency.

The cascode bias network used in [60,61] consists of a resistive divider between the cascode drain node V_{D2}, a fixed voltage V_{DDc}, and ground, as shown in Figure 5-3(a). This configuration allows V_{G2} to track V_{sup} so that high efficiency can be maintained as the supply voltage is varied. Note that in this self-biasing topology, the resistor R_2 is connected to the cascode drain node V_{D2}. However, the V_{D2} node experiences

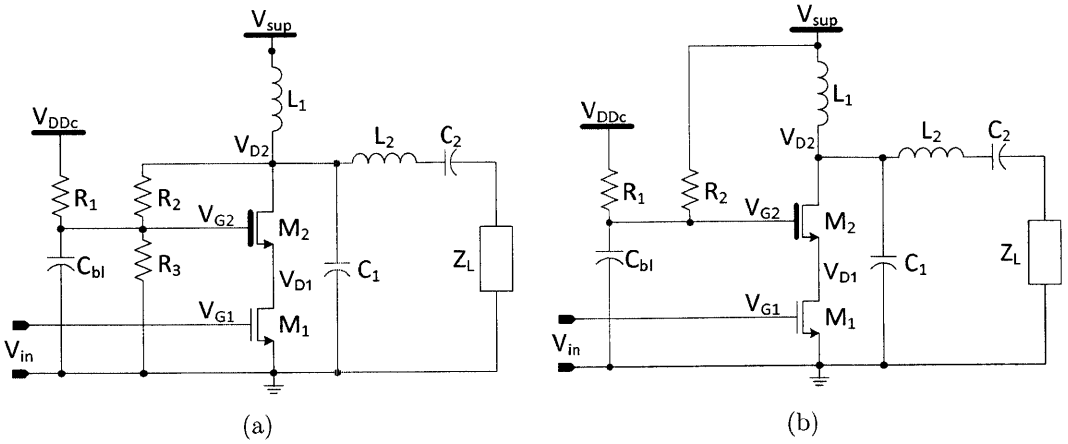


Figure 5-3: (a) Self-biasing topology for a cascode class-E PA used in [60, 61]. (b) Improved self-biasing topology used in this work.

a very large voltage swing characteristic of class-E PAs, as shown in Figure 5-2. This large voltage swing couples to the V_{G2} node through the resistive divider, which is undesirable because of the CV^2 losses associated with the parasitic capacitances attached to the node. This large AC voltage swing can be reduced by increasing the value of the blocking capacitor C_{bl} shown in Figure 5-3(a). However, since we modulate the V_{sup} node in the AMO system, a large C_{bl} would limit the speed that the V_{G2} node would change when the V_{sup} node changes, which would lower efficiency. To fix these problems, in our work, we tie the resistor R_2 directly to the V_{sup} node instead of the V_{D2} node, as shown in Figure 5-3(b). We can do this because the inductor L_1 is on-chip and the V_{sup} is also generated on-chip as the output of the discrete supply-voltage modulator. The V_{sup} node does not experience a large AC voltage swing, so that the voltage swing on the V_{G2} should be much smaller. In addition to this change, we also remove the resistor R_3 shown Figure 5-3(a) to eliminate the DC current to ground, further improving the efficiency. We can do this because R_1 and R_2 are sufficient to provide the linear relationship between V_{G2} and V_{sup}.

For the new self-biasing topology shown in Figure 5-3(b), we can calculate the required values for R_1, R_2, and V_{DDc} as follows. First, the linear relationship between

V_{G2} and V_{sup} can be written as:

$$V_{G2} = a_0 + a_1 V_{sup} \tag{5.1}$$

The parameters a_0 and a_1 can be extracted from simulations that find the optimum V_{G2} for a given V_{sup}. Looking at the resistive divider network in Figure 5-3(b), we can also write V_{G2} in terms of R_1, R_2, V_{DDc}, and V_{sup}:

$$V_{G2} = \frac{R_2}{R_1 + R_2} V_{DDc} + \frac{R_1}{R_1 + R_2} V_{sup} \tag{5.2}$$

Note that V_{G2} is set by resistor ratios, making the implementation robust to process variations. Comparing equations 5.1 and 5.2, we find the following relations:

$$a_0 = \frac{R_2}{R_1 + R_2} V_{DDc} \tag{5.3}$$

$$a_1 = \frac{R_1}{R_1 + R_2} \tag{5.4}$$

Solving for R2 and V_{DDc}, we obtain

$$R_2 = \frac{a_1}{1 - a_1} R_1 \tag{5.5}$$

$$V_{DDc} = a_0 + \frac{a_0 a_1}{1 - a_1} \tag{5.6}$$

Note that R_1 is a free variable. A large value of R_1 will minimize the DC power in the self-biasing network, but will increase the RC time constant at the V_{G2} node, limiting how quickly the V_{G2} node can track the V_{sup} node. Thus, in choosing the value of R_1 there is a tradeoff between DC power and speed.

5.3 PA Design and Implementation

The PA was designed for a target operating frequency of 2.5 GHz to meet the frequency specifications for WLAN systems; however, after fabrication, the optimum frequency for efficiency and output power was 2.4 GHz. The target maximum output

power for the differential PA was 26 dBm at $V_{sup} = 2.5$V, corresponding to 29 dBm (800 mW) for the 2 PAs in the outphasing system. This would give sufficient margin for the 27-dBm requirement of WLAN systems, a widely-used mobile wireless communication standard. 2-dB design margin is added for safety and because additional power loss would occur in the off-chip output balun and power combiner. The widths of both M_1 and M_2 were designed as a compromise between the switch on-resistance and the parasitic capacitances at the gate and the drain. Additionally, the size of M_2 should be chosen to obtain the necessary shunt drain capacitance required for the class-E operation. The finger width for both M_1 and M_2 was chosen to be 6 μm based on the results from [60, 61]. Using the same finger width for both CS and CG transistors also allows for optimal layout structure for the PA unit cell. Figure 5-4 shows the layout of the PA unit cell, which guarantees layout symmetry, good grounding, as well as the minimum parasitic capacitance between the CS and CG devices (node V_{D1} in Figure 5-1). The channel length of the thin-oxide CS device is $L = 60$nm and that of the thick-oxide device is $L = 0.28\mu$m. For each half of the differential PA, the total width of the thin-oxide CS device is $W = 1152\mu$m and that of the thick-oxide device is $W = 2304\mu$m. The inverter used to drive the gate of the CS device was sized to provide a square-wave input signal for V_{G1}.

The value of the spiral inductor L_1 shown in Figure 5-1 must be small such that PA output can settle quickly enough when the supply voltage changes from one value to another. In addition, larger inductance values consume more area and increase the DC resistance of the spiral inductor due to the additional number of turns required, lowering the PA efficiency. However, the inductance cannot be made too small or it will tune out too much of the shunt capacitance at the drain node and change the dynamics of the class-E operation. Furthermore, the smaller L_1 is, the more AC current that flows through it, increasing the power loss in the inductor due to the parasitic resistance, which can be relatively high due to the limited quality factor of integrated spiral inductors. As a compromise, 2 nH was chosen for L_1 in this design. In choosing the number of turns and the metal width for the inductor, DC resistance is the most important parameter to minimize to achieve the highest possible efficiency.

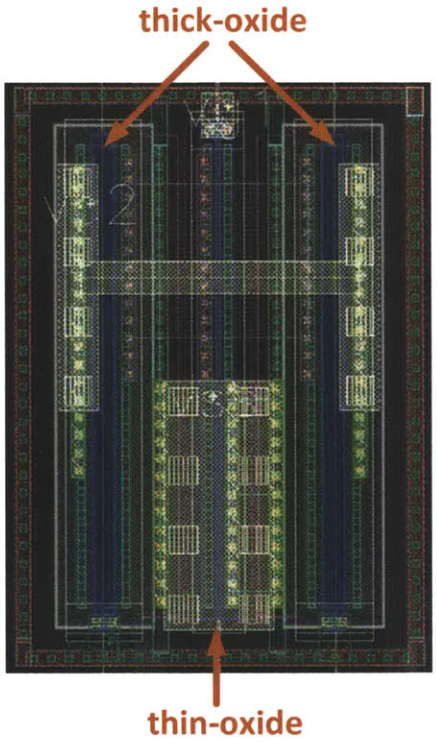


Figure 5-4: Layout view of a single unit cell for the cascode class-E PA in the 2.4-GHz AMO IC prototype.

Too many turns increases the DC resistance, as does small metal width. For a fixed inductance, typically the DC resistance trades off with the Q factor.

The output matching network consists of L_{ser}, C_{ser}, and C_m shown in Figure 5-1. These three components must implement two functions: (1) filtering the large harmonic content of the drain voltage V_{D2} from the output V_{out}, and (2) providing the correct complex impedance at the fundamental RF frequency for sub-optimum, variable-voltage class-E operation. The second step includes transforming the 50-Ω load resistance to a smaller resistance required to achieve the target output power. The three components L_{ser}, C_{ser}, and C_m are basically a combination of a series LC filter whose resonant frequency is at the RF carrier frequency, and an L-matching network to transform the 50-Ω load resistance. The network Q factor of the resonant filter should be chosen to be small to achieve a large bandwidth for the PA. A small network Q factor will also allow the PA output to settle quickly when the supply voltage changes from one value to another. In addition to filtering and impedance transformation, the three values for L_{ser}, C_{ser}, and C_m should be further tuned to obtain the required variable-voltage class-E operation shown in Figure 5-2. The drain voltage waveform was optimized for highest efficiency at $V_{sup} = 2.5$V while keeping the gate-drain voltages for both CS and CG devices below breakdown limits. For L_{ser}, we make use of the bondwire inductance from the packaging of the chip. For this design, we wirebonded the chip directly to the test PCB. The length of the bondwire was chosen to give an inductance of approximately 2.4 nH for L_{ser}. C_{ser} and C_m were both implemented with off-chip SMD capacitors (size 0402) on the PCB. In choosing their values, the parasitic inductance and capacitance of these parts should be accounted for in simulation. The values used in this design were $C_{ser} = 3.3$pF and $C_m = 1.6$pF.

To size the resistors R_1 and R_2 for the self-biasing network of the cascode device, we follow the procedure given in Section 5.2. First, the optimal values of V_{G2} for various values of V_{sup} were found in simulation. Figure 5-5 plots the simulation results, showing the linear relationshp between V_{G2} and V_{sup}. This plot give us the values of $a_0 = 1$V and $a_1 = 0.4$ to use in equation 5.6. The value of R_1 was chosen to

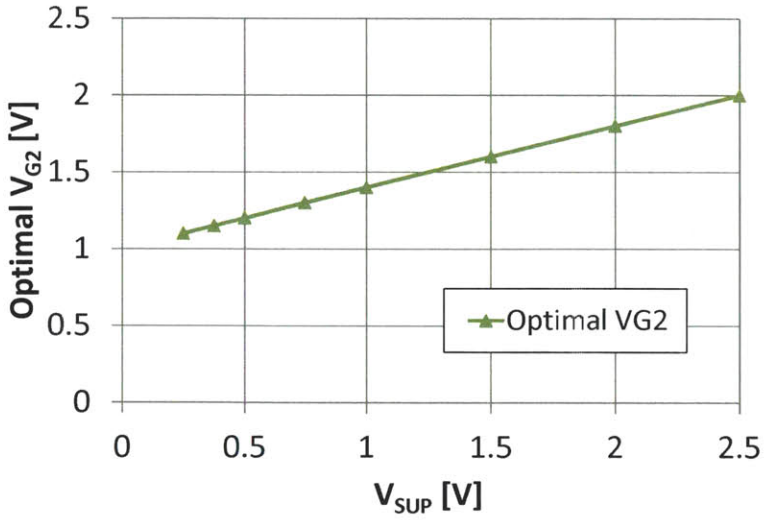


Figure 5-5: Optimal V_{G2} vs. V_{sup} for maximum efficiency from simulation of the cascode class-E PA for the 2.4-GHz AMO IC prototype.

be 333 Ω as a tradeoff between speed and DC power dissipation. This gives $R_2 = 500\Omega$ and $V_{DDc} = 1.667$V. No explicit capacitor was used for C_{bl} in Figure 5-3(b), to keep the speed of the self-biasing network as fast as possible.

Figure 5-6 shows the simulated efficiency vs. output power of the cascode class-E PA with different biasing schemes for the cascode device. The efficiency in this plot is defined as $P_{out}/\left(P_{sup} + P_{VDD1}\right)$, where P_{out} is the output power, P_{sup} is the power from V_{sup}, and P_{VDD1} is the power from the 1V supply of the inverter predriver. The green curve is the result using a fixed value for V_{G2}, the blue curve is the result using the optimal value for V_{G2}, and the orange curve is the result using the self-biasing network shown in Figure 5-1. Note that using the optimal V_{G2} for each different value of V_{sup} results in up to 10% efficiency improvement at backed-off power levels compared to using a fixed value for V_{G2}. Also note that the efficiency using the self-biasing network is almost the same as the efficiency using an ideal voltage source (the blue curve), showing that the implemented self-biasing network works as expected.

Figure 5-7 shows the simulated gate-drain voltage waveforms versus time for both the thick-oxide CG device and the thin-oxide CS device at the maximum PA supply voltage of 2.5 V. Common practice is keep the maximum voltage drops across devices below $2V_{DD-nom}$ to assume reasonable device/circuit life-times [62], V_{DD-nom} being

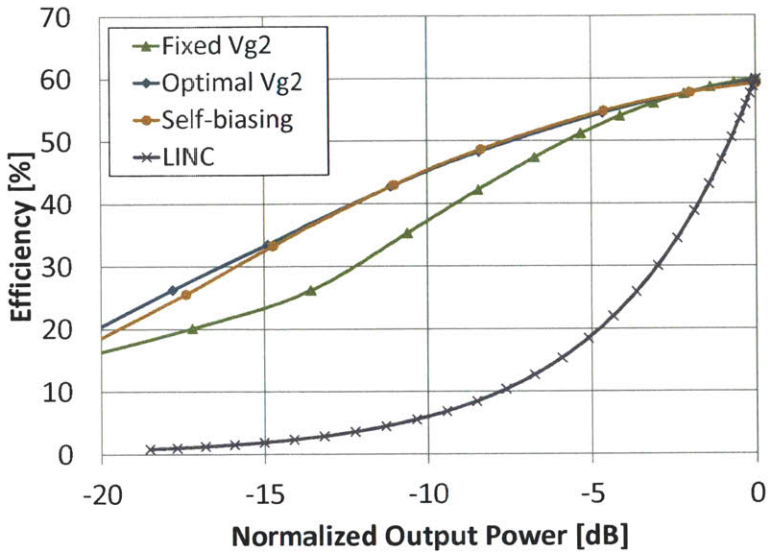


Figure 5-6: Simulated efficiency vs. output power of the cascode class-E PA in the 2.4-GHz AMO IC prototype, for different biasing schemes for the cascode device. The efficiency of the LINC system is also shown for reference.

the nominal supply voltage. In this way, oxide fields never exceed the critical oxide field, thus avoiding unrecoverable oxide breakdown to occur in DC conditions assuring safe operation also at RF. V_{DD-nom} is 1.0 V for the CS device and 2.5 V for the CG device. Note that the voltage drops are kept below the breakdown limits with sufficient margin.

The differential PA input buffer that interfaces the off-chip RF phase input to the on-chip PA is shown in Figure 5-8. It consists of a chain of 1-V inverters from the standard digital cell library. The first inverter is biased at mid-rail by a resistive divider, which also presents a 50-Ω impedance to the off-chip driver. A set of cross-coupled NMOS devices are added to the output as shown to ensure the two sides of the differential signal are complementary and non-overlapping. The output of the inverter chain is fed to other repeaters on the chip as needed before it reaches the PA predriver shown in Figure 5-1.

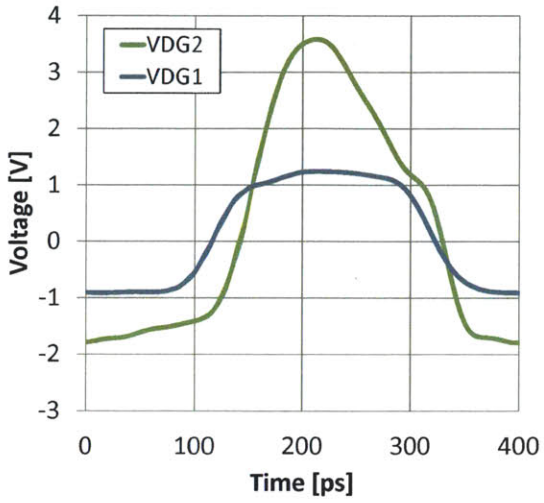


Figure 5-7: Simulated gate-drain voltages V_{DG2} and V_{DG1} across the thick-oxide CG device and the thin-oxide CS device, respectively, at the maximum PA supply voltage of 2.5 V.

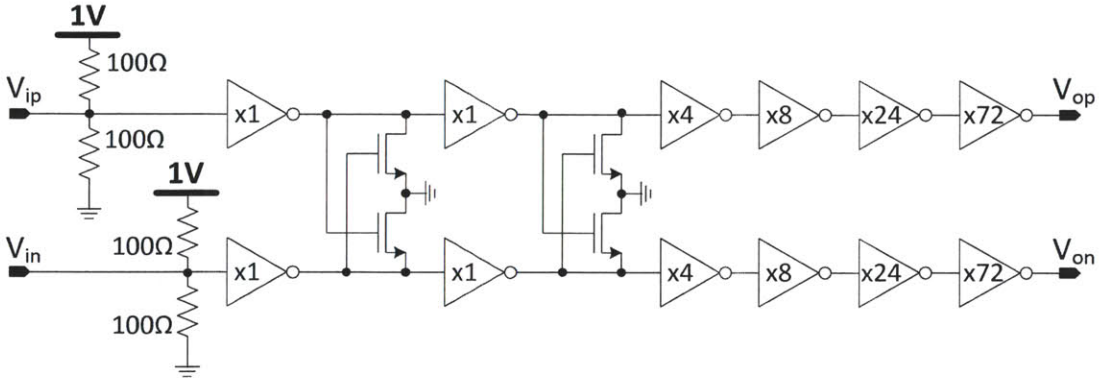


Figure 5-8: The differential PA input buffer that interfaces the off-chip RF phase input to the on-chip PA in the AMO IC prototype.

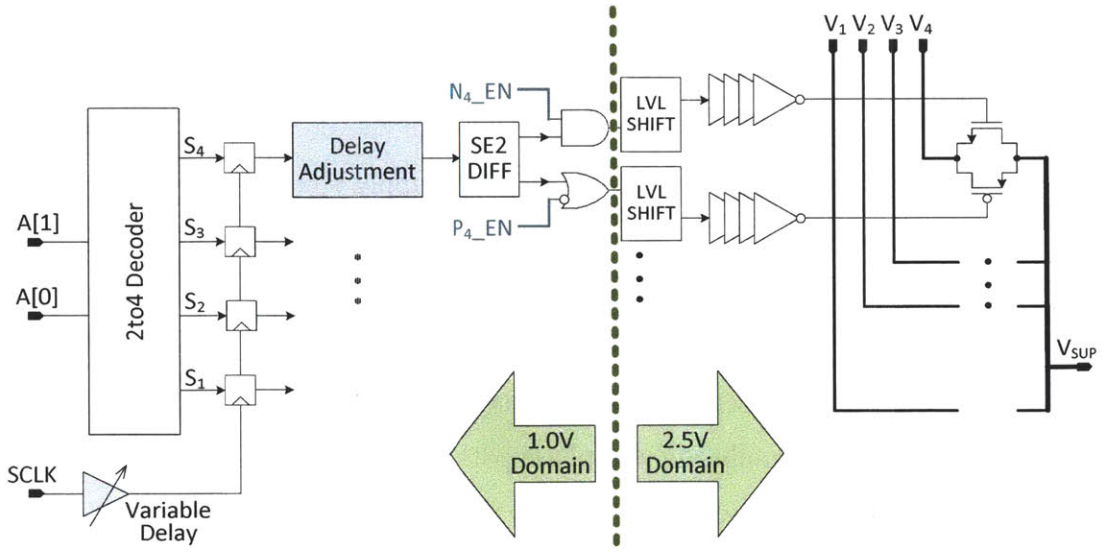


Figure 5-9: Block diagram of the discrete supply-voltage modulator used in the 2.4-GHz AMO IC prototype.

5.4 Discrete Supply-voltage Modulator

Figure 5-9 shows the block diagram of the discrete supply-voltage modulator used in the 2.4-GHz AMO IC prototype. The PA supply voltage can switch among 4 different supply voltages, which come from off-chip power supplies. The power supply switches are thick-oxide, 2.5-V devices to pass supply voltages up to 2.5 V. They consist of both NMOS and PMOS devices in parallel and are designed for small on-resistance to minimize the DC power dissipation. The large gate capacitances of the power supply switches are driven with a chain of 2.5-V inverters. All the digital logic for the digital amplitude data is implemented with thin-oxide, 1.0-V devices for faster speed and lower power dissipation. Level shifters are used to convert the digital select signals from the 1.0-V domain to the 2.5-V domain as shown in Figure 5-9.

For each different supply voltage, both PMOS and NMOS can be either enabled or disabled with configuration bits depending on the value of the supply voltage that the switch must pass. Disabling the NMOS for high voltages and the PMOS for low voltages can save the power required to switch the large gate capacitance, as well as reduce the digital power supply ringing. A delay adjustment circuit is included

for each switch control signal to tune the delay of the signal transitions (both rising edges and falling edges) to implement time alignment between the different switches. This is important because only one of the switches should be turned on at any given time. If two switches were on, then two different supply voltages would be shorted out, resulting in a large power loss due to the very small resistance of the switches. Similarly, if two switches were off, then the PA supply voltage would be an open circuit and the output power would go to zero. All the switch select signals are clocked for synchonization, and the clock signal has a variable delay to perform time alignment between the amplitude and phase paths.

Figure 5-10 shows the details of the delay adjustment circuit. The circuit implements a variable delay for both rising and falling edges of the input signal. Digital logic is used to detect either a rising edge or a falling edge, and the output transition is delayed by a variable delay line. Rising edges and falling edges have separate delay lines, and the amount of delay for each is set by configuration registers. Figure 5-11 shows the details of the delay line used for this chip. It consists of 64 cascaded delay elements whose outputs are fed to a 64:1 mux. The select signal of the mux determines the amount of the delay from input to output. The delay unit cell is a standard cell from a digital standard library and has about 70 ps of delay. This delay line is also used to implement the variable delay of the clock signal shown in Figure 5-9, which implements the time alignment between the amplitude and phase paths.

5.5 Power Supply Switch Design

In designing the size of the power supply switches, there is a tradeoff between conduction loss and gating loss. A large switch has a low on-resistance to keep the DC power loss low, but it also has a large gate capacitance that results in high dynamic power loss whenever the supply voltage levels change. In our design, we chose to size the switches so that the worst-case efficiency degration from the conduction loss was less than 3%. Figure 5-12 shows the resulting sizes of the NMOS and PMOS devices, along with the size of the inverter chains driving the transistor gates. Figure 5-13

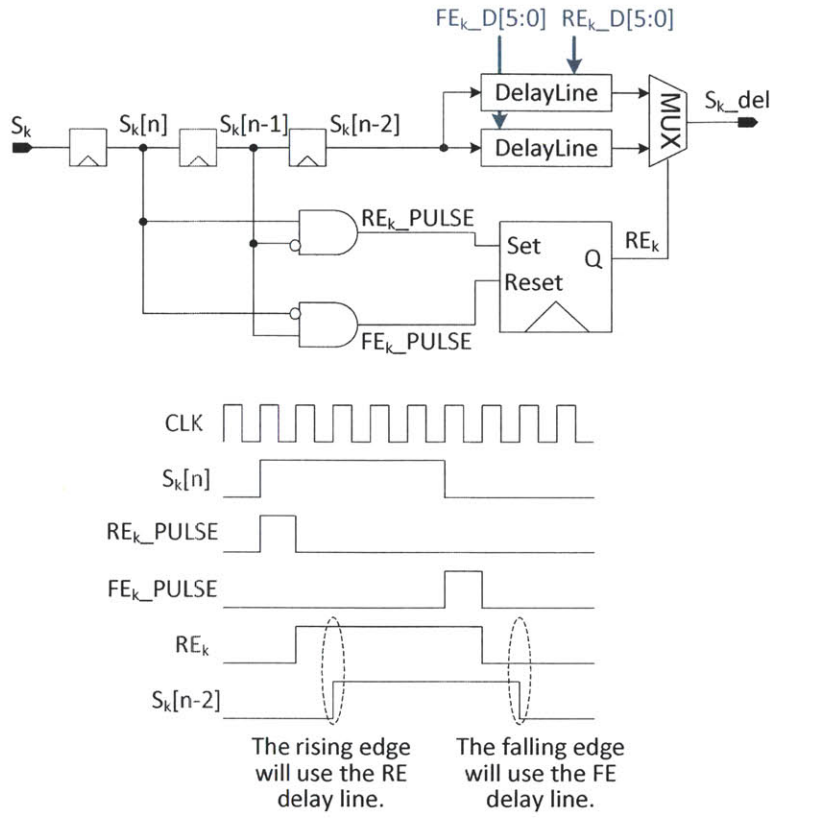


Figure 5-10: Block diagram and timing waveforms of the delay adjustment circuit used to tune the delay of the signal transitions for both rising edges and falling edges. The delay adjustment circuit implements time alignment between the different switches used in the 2.4-GHz AMO IC prototype.

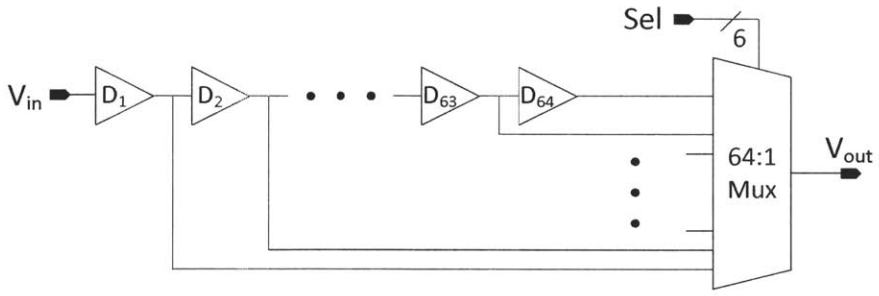


Figure 5-11: Block diagram of the delay line used in the delay adjustment circuit and to implement time alignment between the amplitude and phase paths for the 2.4-GHz AMO IC prototype.

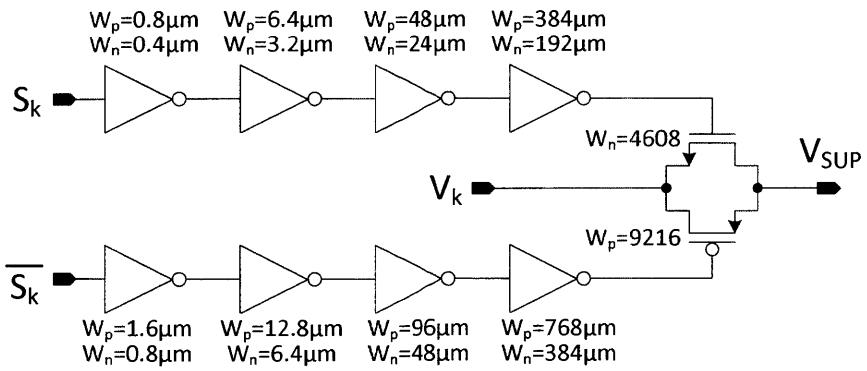
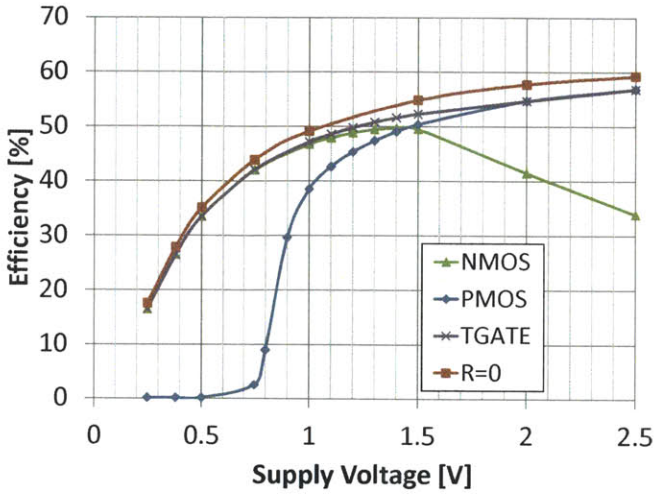


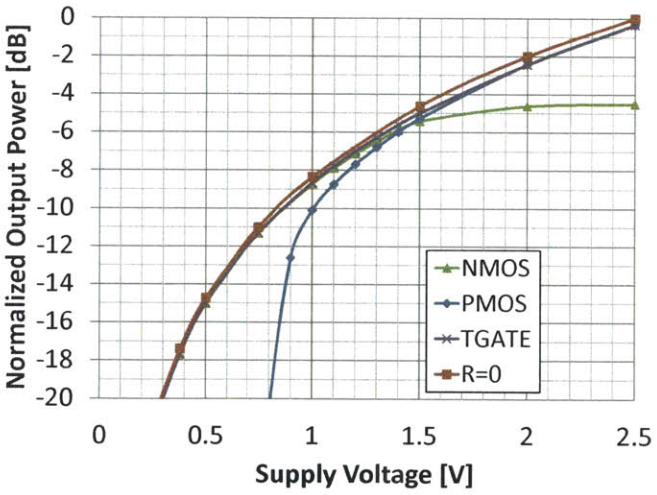
Figure 5-12: Transistor sizes for the power supply switches and the inverter chains used to drive them for the 2.4-GHz AMO IC prototype. The channel length of all the transistors is 0.28 μm.

shows the PA efficiency and output power vs. supply voltage when the power supply switch is used to connect the PA supply voltage to the PA. Four different cases are shown in the figure: (1) using only the NMOS device, (2) using only the PMOS device, (3) using both NMOS and PMOS devices, and (4) using an ideal switch with 0-Ω resistance. The plots show that NMOS device can efficiently pass voltages below 1.4 V and the PMOS device can efficiently pass voltages above 1.4 V. The worst-case efficiency loss occurs at the maximum supply voltage of 2.5 V and is kept below 3%. This voltage gives the highest output power, corresponding to the largest current through the switch and therefore the largest voltage drop. The output power is lowered due to the voltage drop across the switch, but the worst-case power degradation is only about 0.3 dB.

Figure 5-14 shows the power supply switch resistance vs. supply voltage when the switch is used to connect the PA supply voltage to the PA, defined as $R_{sw} = V_{sw}/I_{sw}$. When both NMOS and PMOS devices are used, the switch resistance is between 0.2-0.4 Ω. This means that the other sources of resistance between the external power supplies and the power supply switches should be kept below this value to maintain high efficiency in the PA. The other sources of resistance include the metal traces on the chip that connect the power supply switches to the bondpads, and the wires and metal traces on the PCB that connect the external power supplies to the chip.



(a) PA Efficiency vs. Supply Voltage



(b) PA Output Power vs. Supply Voltage

Figure 5-13: PA efficiency (a) and output power (b) vs. supply voltage when the power supply switch is used to connect the PA supply voltage to the PA in the 2.4-GHz AMO IC prototype.

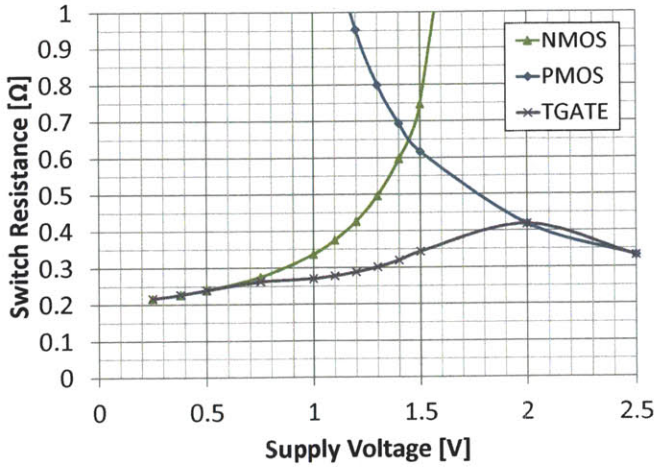


Figure 5-14: Power supply switch resistance vs. supply voltage when the switch is used to connect the PA supply voltage to the PA in the 2.4-GHz AMO IC prototype.

5.6 DSVM Transient Damping

In the AMO system using DSVM, the PA supply voltages switch among a discrete set of levels. When the PA supply voltage switches from one level to another, the PA supply node experiences a transient ringing due to the parasitic capacitances of the switches together with the bondwire inductance that connects the external power supplies to the chip (see Figure 5-15). Other sources of series parasitic inductance other than bondwires (e.g., from the package or PCB traces) can exist off-chip as well. Because the current through an inductor cannot change instantaneously, there is a nonzero settling time required for the PA supply voltage to change. Furthermore, because the resistance of the power supply switches is low to minimize DC power dissipation, the Q-factor of the 2nd-order circuit can be very high so that the transient ringing is large with a slow settling time. Transient ringing on the PA supply node is undesirable because it will cause glitches in the output waveform whenever the supply voltages are switched, increasing the noise in the output signal. The problem of power supply ringing also applies to the supply voltage of the buffers driving the large gate capacitance of the switches, as shown in Figure 5-15. To turn the power supply switches on and off, this power supply must draw a large amount of current to charge and discharge the large gate capacitance, so that a large transient ringing

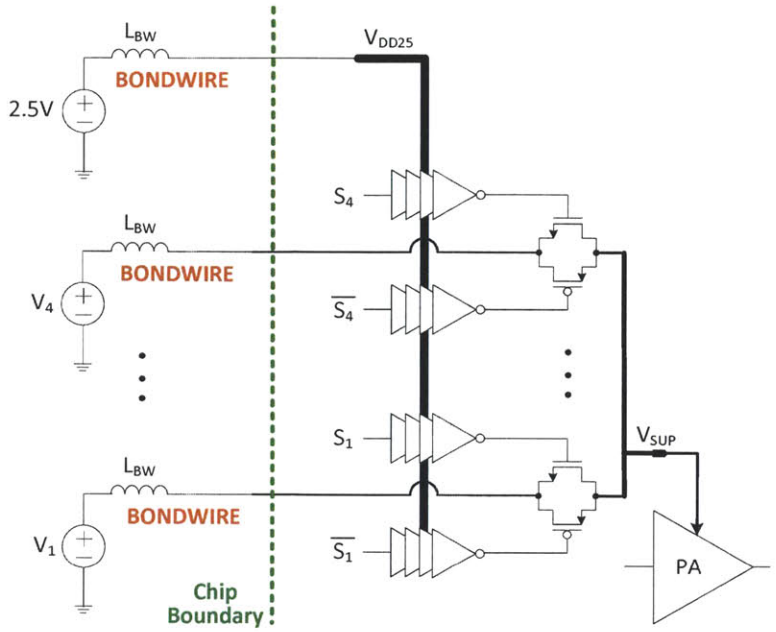


Figure 5-15: Interface between the external power supply voltages and the discrete supply voltage modulator on the AMO IC prototype, showing the parasitic series bondwire inductance that causes transient ringing on the on-chip supply voltage nodes.

occurs. The ringing on this node can easily couple to the PA output, also increasing the noise in the output signal.

To reduce the transient ringing, on-chip bypass capacitance can be added to each power supply voltage. However, large bypass capacitors cost a significant amount of area, which may not be available. In addition, for this application the bypass capacitors would have to be very large (on the order of tens of nano-Farads) to significantly reduce the ringing, due to the large currents that the PA and the power supply switch buffers must draw. Our solution to reduce the transient ringing is to add a damping leg [63] to each power supply voltage on the chip, as shown in Figure 5-16. The bondwire inductance used in simulation for each power supply was 2 nH, which was estimated from the length of the bondwires from the packaging of the chip. The damping leg component values were optimized to minimize the ringing on the on-chip power supply nodes, with a constraint on the size of the bypass capacitance due to the limited area on the chip. Figure 5-17 shows the simulation results of the

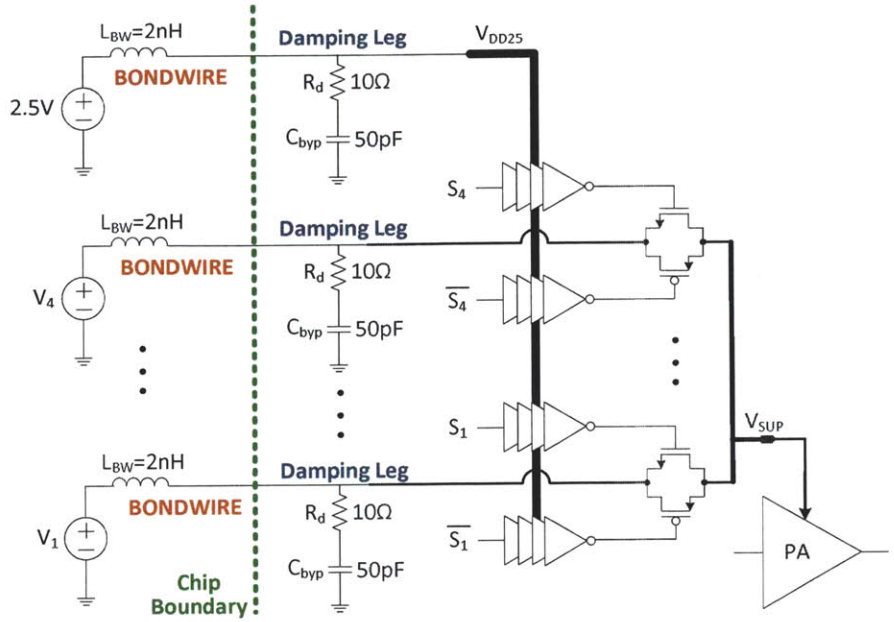
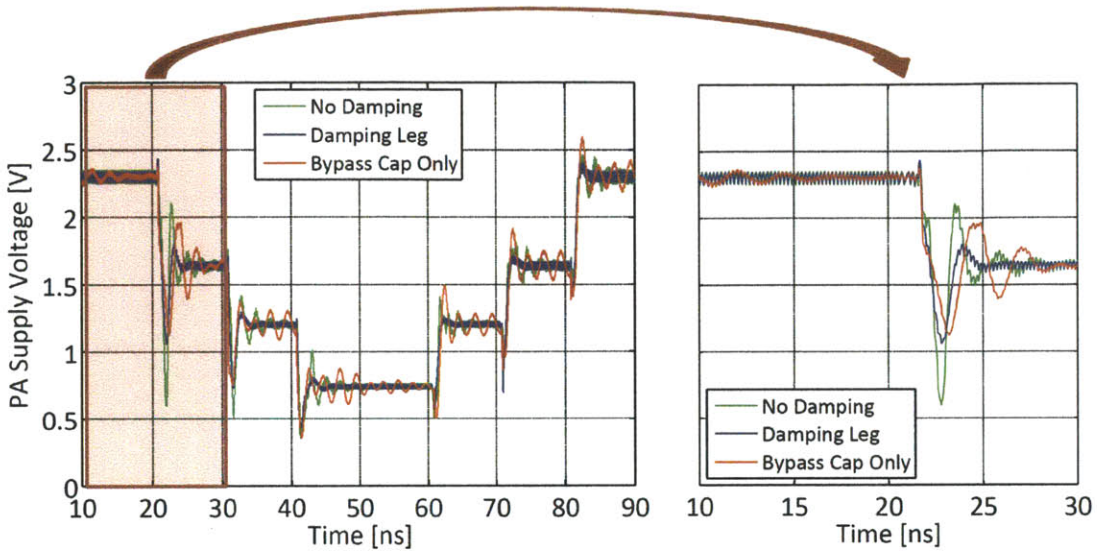


Figure 5-16: Discrete supply voltage modulator with damping legs to reduce the transient ringing on the on-chip supply voltage nodes in the 2.4-GHz AMO IC prototype.

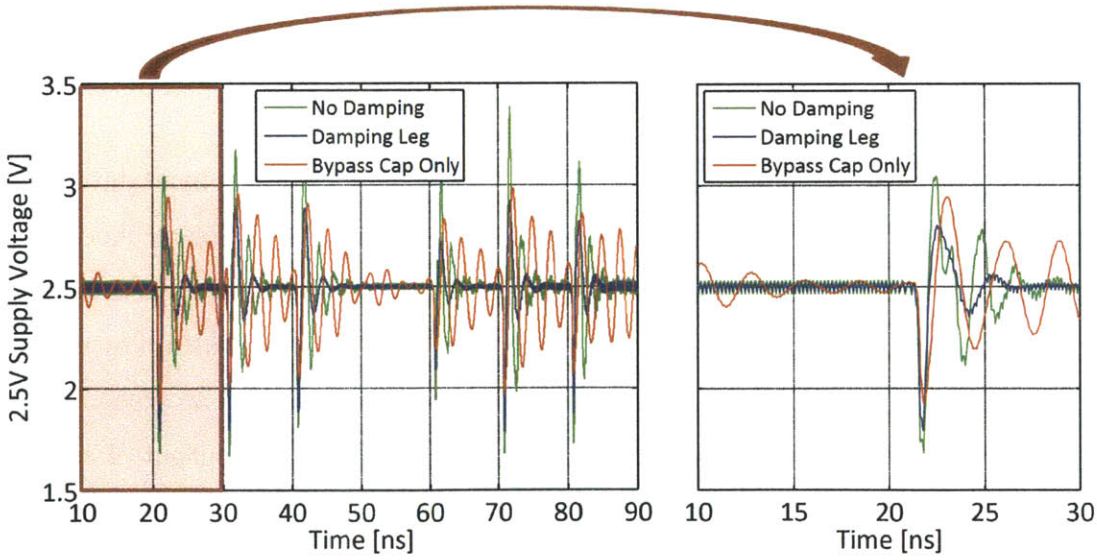
transient power supply ringing for three different cases: (1) with the damping leg, (2) with only the bypass capacitance C_{byp} without the damping resistor R_d, and (3) with no additional circuit components. It can be seen that the damping leg significantly reduces the power supply ringing compared to the other two cases.

5.7 Transmitter Measurement Results

Figure 5-18 shows the die photo of the 2.4-GHz AMO IC prototype. The entire chip is 2×2 mm^2, but the active area of the chip used for the PA, discrete supply-voltage modulator, buffers, and digital logic is about 1×1 mm^2. Due to space limitations, only one PA and one discrete supply voltage modulator were fabricated on a single chip. The outphasing system was formed by using two different chips. The testbench is shown in Figure 5-19. Digitally pre-distorted baseband data was generated by MATLAB after characterizing the AMO transmitter with a narrowband training signal. The two phase modulators were each implemented by a 16-bit dual-channel DAC evaluation board from Analog Devices (AD9779A). The evaluation



(a) PA Supply Voltage, V_{sup}



(b) Power Supply for Switch Buffers, V_{DD25}

Figure 5-17: Transient ringing for PA supply voltage, V_{sup} (a) and power supply for switch buffers, V_{DD25} (b) in the 2.4-GHz AMO IC prototype.

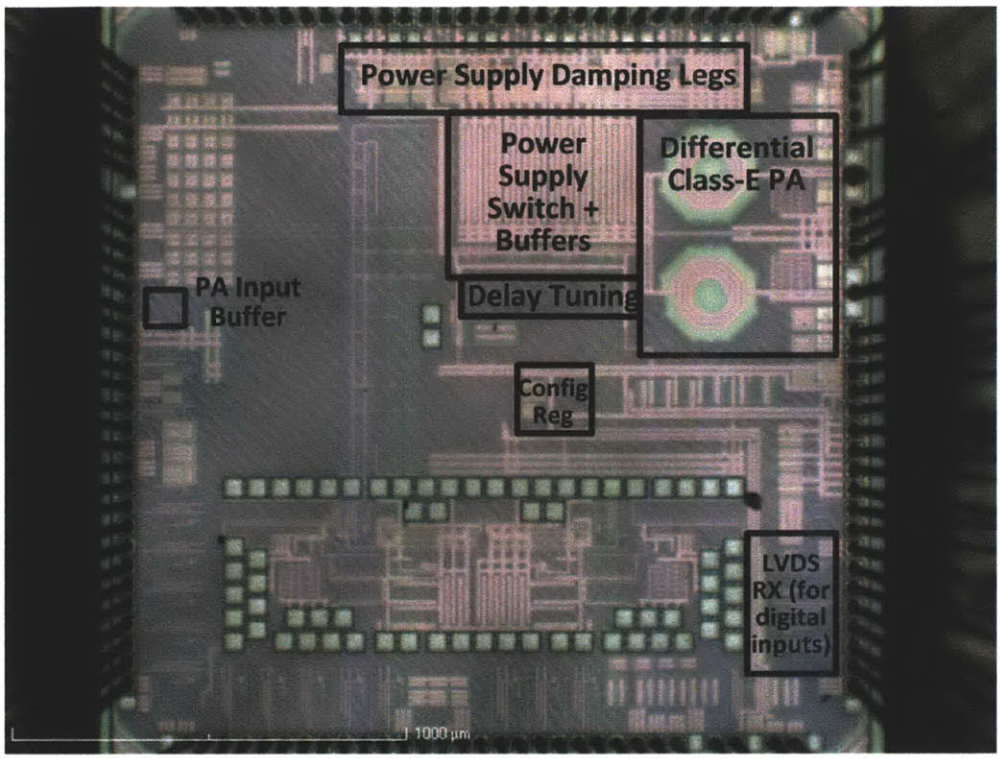


Figure 5-18: Die photo of the 2.4-GHz AMO IC prototype. The total chip area is 2x2 mm^2. Each chip has one PA and one discrete supply voltage modulator.

board includes an I/Q modulator (ADL5375) to upconvert the baseband data to the RF carrier frequency. An FPGA provides the digital inputs to the phase modulators and the discrete supply modulators, and also performs coarse time alignment between the phase and amplitude paths. Fine time alignment is performed on-chip by variable delay lines, as described in Section 5.4. The 4 PA supply voltages are generated by Tektronix power supplies (PWS4323). The differential input and output of each PA is converted to a single-ended signal using a TDK balun (HHM1520A2) rated for frequencies between 2.3 GHz and 2.5 GHz. The two PA outputs are then combined with an Aeroflex Wilkinson combiner (PD0208-S2) rated for frequencies between 2 GHz and 8 GHz.

Figure 5-20 shows the measured transmitter output power and system efficiency vs. frequency. We define the system efficiency as $\eta_{sys} = P_{out}/(P_{DC} + P_{pre})$, where P_{out} is the output power, P_{DC} is the total power dissipation from the 4 PA power

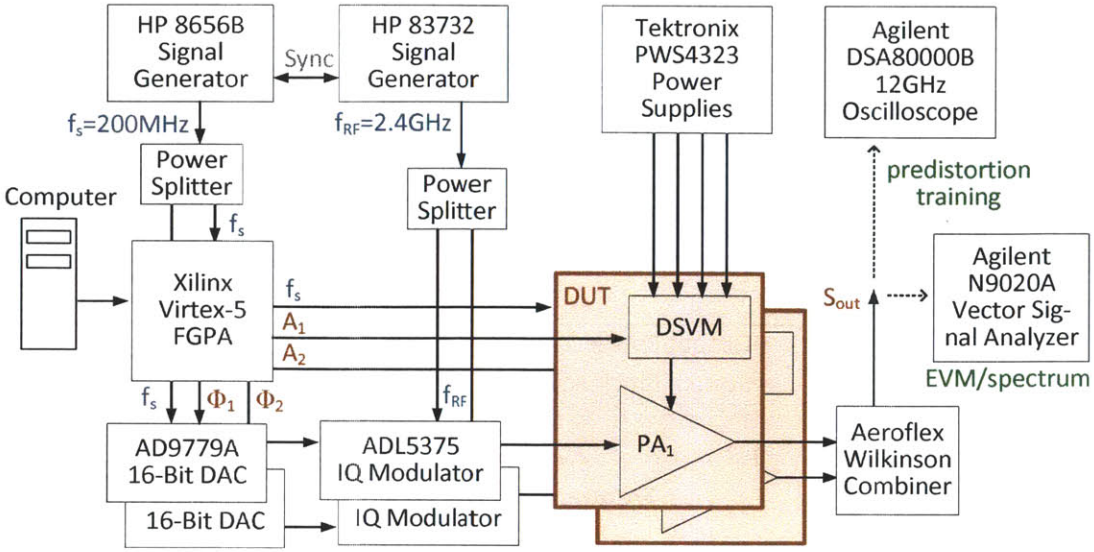


Figure 5-19: Testbench for the 2.4-GHz AMO IC prototype, composed of two CMOS class-E PAs and two discrete supply modulators.

supplies, and P_{pre} is the power from the predriver and all preceding buffers, including the power from V_{DDc}, the power supply for the cascode self-biasing network as shown in Figure 5-1. Note that all output power and efficiency numbers include the loss from the off-chip baluns and power combiner, which together give about 1 dB of insertion loss. The plot shows that the maximum efficiency occurs at 2.5 GHz, but the maximum output power occurs at 2.3 GHz. The operating frequency was chosen to be 2.4 GHz, where there is a good compromise between efficiency and output power. This is also close to our target design frequency of 2.5 GHz. Note that the off-chip baluns and power combiner are only rated for specific frequency ranges, which affect the results shown in Figure 5-20.

Figure 5-21(a) shows the measured drain efficiency, system efficiency and output power vs. supply voltage for the AMO IC prototype at 2.4 GHz. The prototype achieves a peak output power of 27.7 dBm and a peak system efficiency of 45%. Figure 5-21(b) shows the measured efficiency vs. output power at 2.4 GHz. From the plots, we can see that the efficiency remains relatively high down to about 10-dB backoff. This can be attributed to the self-biasing cascode topology, which maintains optimum biasing as the supply voltage is varied. Because the AMO prototype will

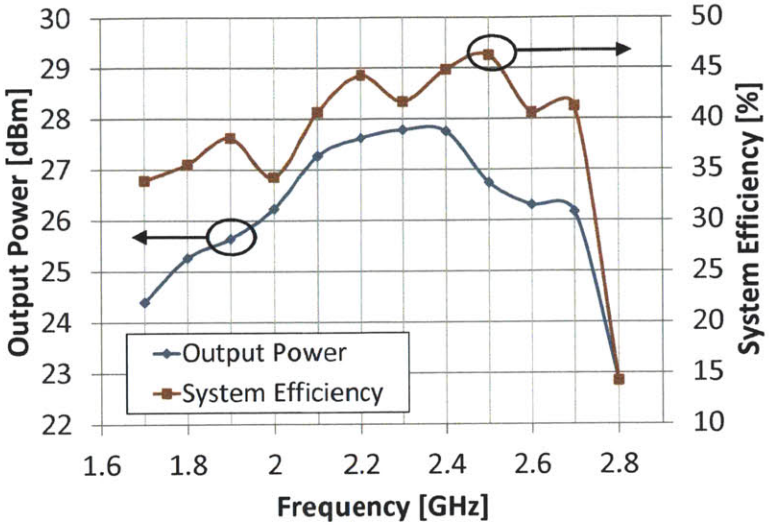
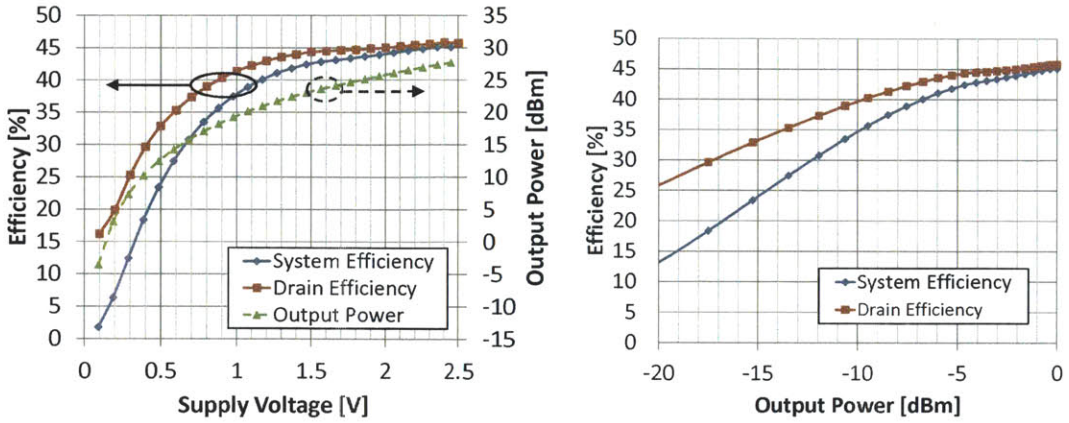


Figure 5-20: Measured output power and system efficiency vs. frequency for the AMO IC prototype.

use discrete supply-voltage modulation, it is important that the PA maintain high efficiency over a wide range of supply voltages. At powers below 10-dB backoff, the fixed power required to drive the PA begins to dominate.

Figure 5-22 compares the efficiency vs. output power of the LINC and AMO systems for the IC prototype. The blue curve is the efficiency for standard outphasing using a single supply voltage, and it can be seen that the efficiency drops quickly as the amount of power backoff increases. The black curve is the efficiency as the supply voltage is varied for both PAs together. We cannot operate directly on the black curve because it would require continuous supply-voltage modulation, which suffers from the tradeoff between efficiency and bandwidth. Instead, we use the AMO system, which combines discrete supply-voltage modulation with outphasing. The red curve is the efficiency for AMO with 4 supply-voltage levels, and it can be seen that the efficiency is much higher than the standard outphasing system, and that it closely approximates the black efficiency curve over a wide output power range. The actual supply-voltage levels chosen were optimized for a 64-QAM signal with a PAPR of 7.0 dB, the PDF of which is shown in Figure 5-22.

Figure 5-23 shows the measured static output amplitude and phase for the AMO transmitter depending on the supply voltage combination and the outphasing angle.



(a) η_D, η_{sys} and P_{out} vs. Supply Voltage

(b) Efficiency vs. Output Power

Figure 5-21: (a) Measured drain efficiency, system efficiency, and output power vs. supply voltage for the AMO IC prototype at 2.4 GHz. (b) Measured efficiency vs. output power.

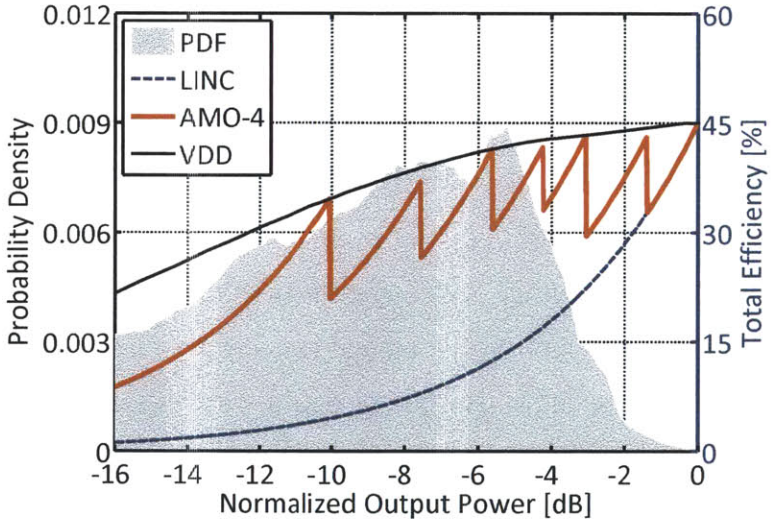


Figure 5-22: Measured efficiency vs. output power for the 2.4-GHz AMO IC prototype, along with the optimized amplitude levels for a 64-QAM signal with 7.0-dB PAPR. The PDF of the 64-QAM signal is also shown.

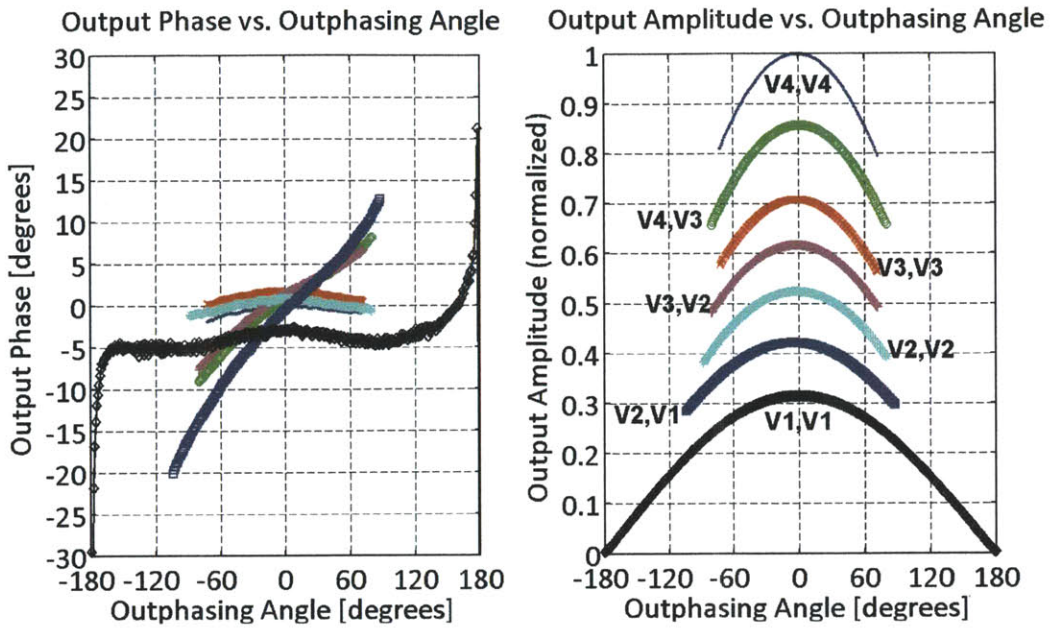
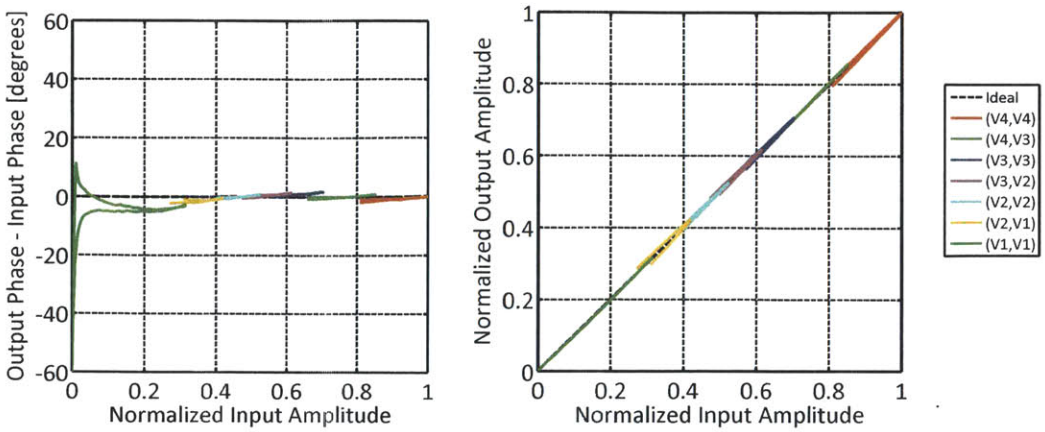


Figure 5-23: Measured static output amplitude and phase vs. outphasing angle for the 2.4-GHz AMO transmitter. Each curve corresponds to a different combination of supply voltages for the two outphased PAs.

There are 7 different curves, each for a different combination of supply voltages for the two outphased PAs. There are two main sources of the static nonlinearity: (1) the mismatch between the branches of the outphasing system, and (2) the varying supply voltage. A lookup table (LUT) constructed from the data in Figure 5-23 implements the digital predistortion (DPD) to correct the static nonlinearity.

Figure 5-25 shows the measured step response of the AMO transmitter output envelope when the supply voltage is changed for both PAs. Different supply voltage transitions are shown, as well both step-up and step-down transients. In all cases, the envelope settles in less than 3 ns, which demonstrates the relatively fast speed of the discrete supply-voltage modulator. For comparison, Figure 5-26 shows the measured step response of the AMO transmitter when the outphasing angle is changed with a fixed supply voltage. Note that the envelope settles slower for the phase step than the amplitude step, in about 6ns. Because the supply voltage is fixed in this case, the nonzero settling time for the phase step is caused by the finite bandwidth of the phase modulator and/or the PA. Since the AMO system requires abrupt amplitude



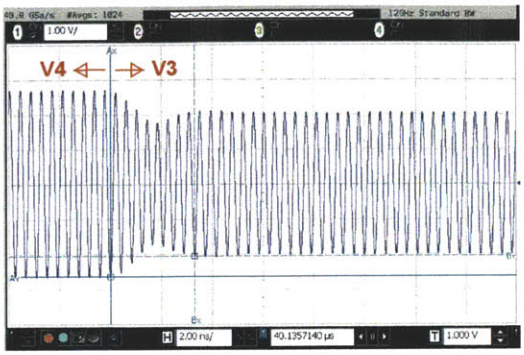
(a) Static Phase Nonlinearity

(b) Static Amplitude Nonlinearity

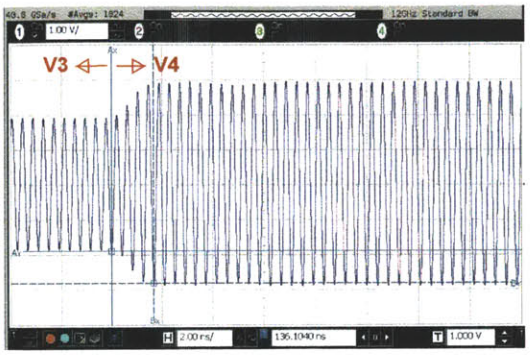
Figure 5-24: Amplitude and phase linearity plots for the measurement data given in Figure 5-23. (a) Difference between the measured output phase and the ideal input phase, plotted vs. the ideal input amplitude. (b) Measured output amplitude vs. the ideal input amplitude. The ideal input amplitudes and phases are the result from the ideal AMO signal decomposition given in Section 4.2.

and phase changes when the supply voltage is switched, the effect of the nonzero settling time for both amplitude and phase steps is to cause glitches in the output waveform that degrade the linearity and add noise to the output signal. This can be seen in Figure 5-27, which shows the AMO transmitter output for a baseband sine wave. The frequency of the baseband sine wave is 1 MHz, the sampling frequency of the digital amplitude and phase data is 200 MHz, and the RF carrier frequency is 2.4 GHz. Note that there are glitches in the output waveform when the AMO system is used that are not present when the LINC system is used. The glitches occur when the supply voltages are switched from one level to another, increasing the noise in the output spectrum.

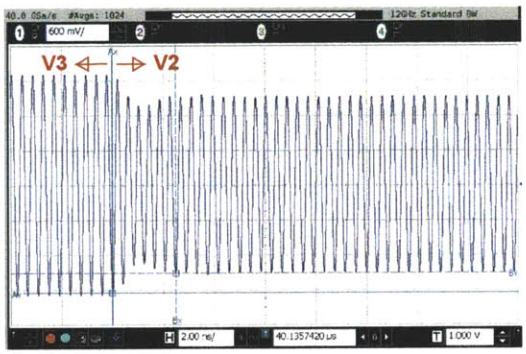
To validate the performance of the AMO system for wireless data transmission, a 64-QAM signal was transmitted with the prototype at various symbol rates. Figure 5-28 shows the constellation diagrams. As explained above, the EVM degrades at higher symbol rates due to the finite settling time of the output when the PA amplitudes and phases change abruptly in the AMO system. However, even the worst-case EVM



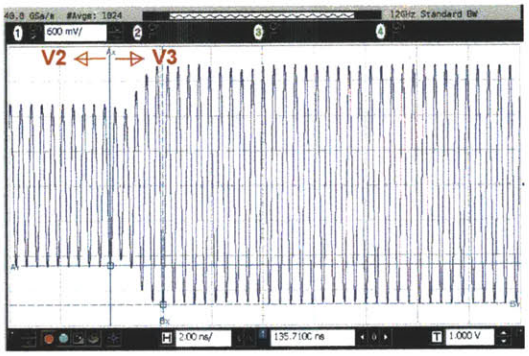
(a) $V4 \rightarrow V3$



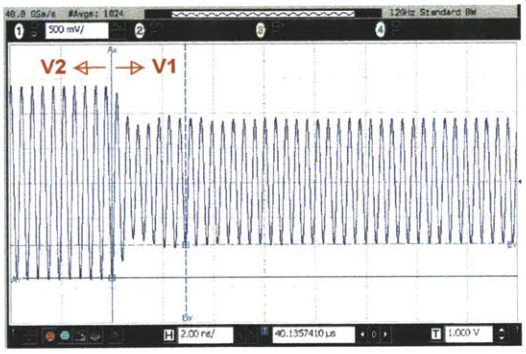
(b) $V3 \rightarrow V4$



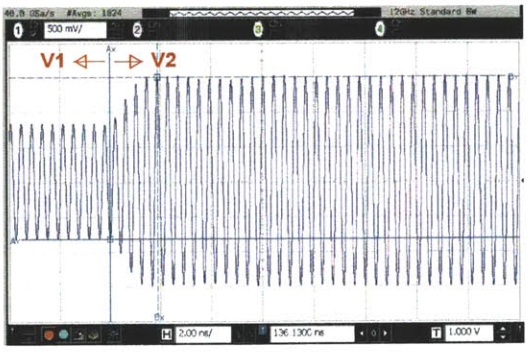
(c) $V3 \rightarrow V2$



(d) $V2 \rightarrow V3$

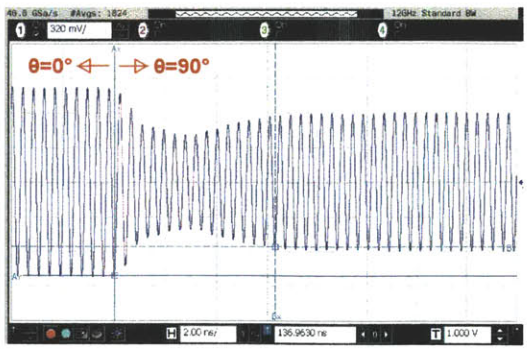


(e) $V2 \rightarrow V1$

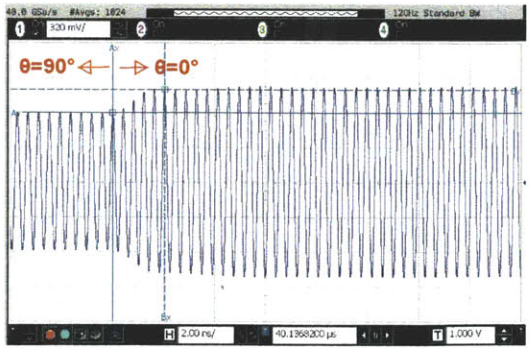


(f) $V1 \rightarrow V2$

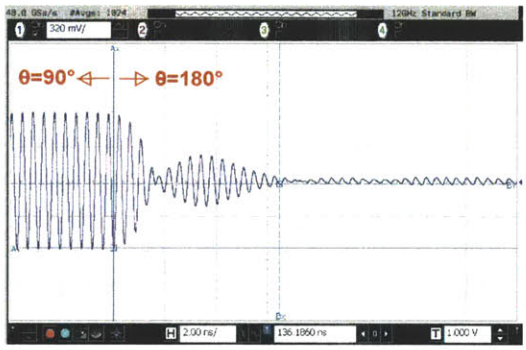
Figure 5-25: Measured step response of the 2.4-GHz AMO transmitter output envelope when the supply voltage is changed for both PAs. (a) $V4 \rightarrow V3$. (b) $V3 \rightarrow V4$. (c) $V3 \rightarrow V2$. (d) $V2 \rightarrow V3$. (e) $V2 \rightarrow V1$. (f) $V1 \rightarrow V2$.



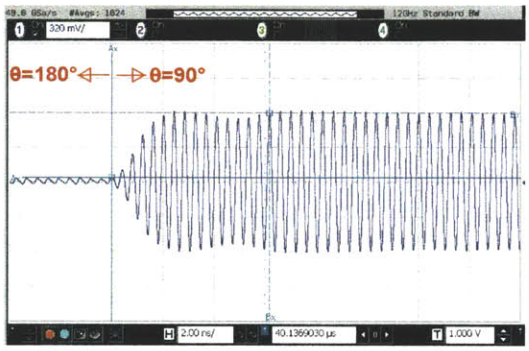
(a) $\theta = 0° \rightarrow \theta = 90°$



(b) $\theta = 90° \rightarrow \theta = 0°$

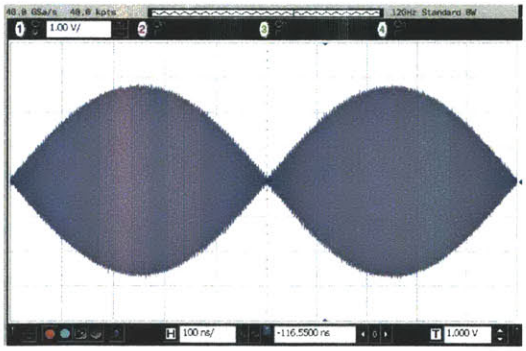


(c) $\theta = 90° \rightarrow \theta = 180°$

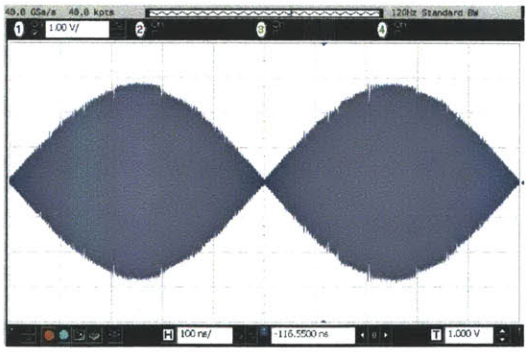


(d) $\theta = 180° \rightarrow \theta = 90°$

Figure 5-26: Measured step response of the 2.4-GHz AMO transmitter output envelope when the outphasing angle is changed with a fixed supply voltage. (a) $\theta = 0° \rightarrow \theta = 90°$. (b) $\theta = 90° \rightarrow \theta = 0°$. (c) $\theta = 90° \rightarrow \theta = 180°$. (d) $\theta = 180° \rightarrow \theta = 90°$.



(a) LINC system



(b) AMO system

Figure 5-27: Measured output waveform of the IC prototype for a 1-MHz baseband sine wave transmission. The sampling rate of the digital data is 200 MHz and the RF carrier frequency is 2.4 GHz. (a) LINC system. (b) AMO system.

of 2.5% is acceptable for most applications.

Figure 5-29 shows the average system efficiency, ACPR, and EVM of the prototype AMO transmitter for the 64-QAM signal transmission with various channel bandwidths from 5 to 40 MHz. For comparison purposes, we also show the results for the LINC case, when only a single supply voltage is used for both PAs. The sampling rate of the digital data was 200 MHz for all channel bandwidths, which was the maximum sampling rate of the DACs used in the phase modulators. The average system efficiency includes the power consumption from the discrete supply modulators and is defined as $\eta_{sys} = P_{out}/(P_{DC} + P_{pre} + P_{DSVM})$ where P_{DSVM} is the power from the 2.5-V supply for the discrete supply-voltage modulator (the other parameters were defined previously).

From the plots, we can see a significant improvement in the efficiency for 4-level AMO vs. LINC, from 9% to almost 30%, an efficiency improvement of 3x. The efficiency of the AMO system drops slightly at higher symbol-rates due to the dynamic losses from the discrete supply modulator, but the efficiency degradation is very small, demonstrating the high efficiency of the discrete supply modulators. The EVM for both the LINC and AMO cases is around 1.2% for symbol rates of 20 MHz or less. At 40-MHz symbol rate, the EVM jumps up to 3%, but this is still an acceptable level for many applications. The degradation in ACPR is more significant, as shown in Figure 5-29(b). At the 1st channel offset, the degradation is about 3 dB when the AMO system is used, and at the 2nd channel offset, the degradation is 5 dB. This is due to the abrupt amplitude and phase changes when the supply voltage is switched, which cause glitches in the output waveform that degrade the linearity and add noise to the signal.

Figure 5-30 shows the power breakdown for the 64-QAM signal transmission at various symbol-rates. The purple bars show the power consumption of the discrete supply modulators. Note that the power loss is small compared to the other sources of power loss in the system, and that the power loss does not increase significantly as the symbol-rate increases. This shows the relatively high efficiency of the discrete supply modulators, and demonstrates the potential of the AMO system to achieve both high-

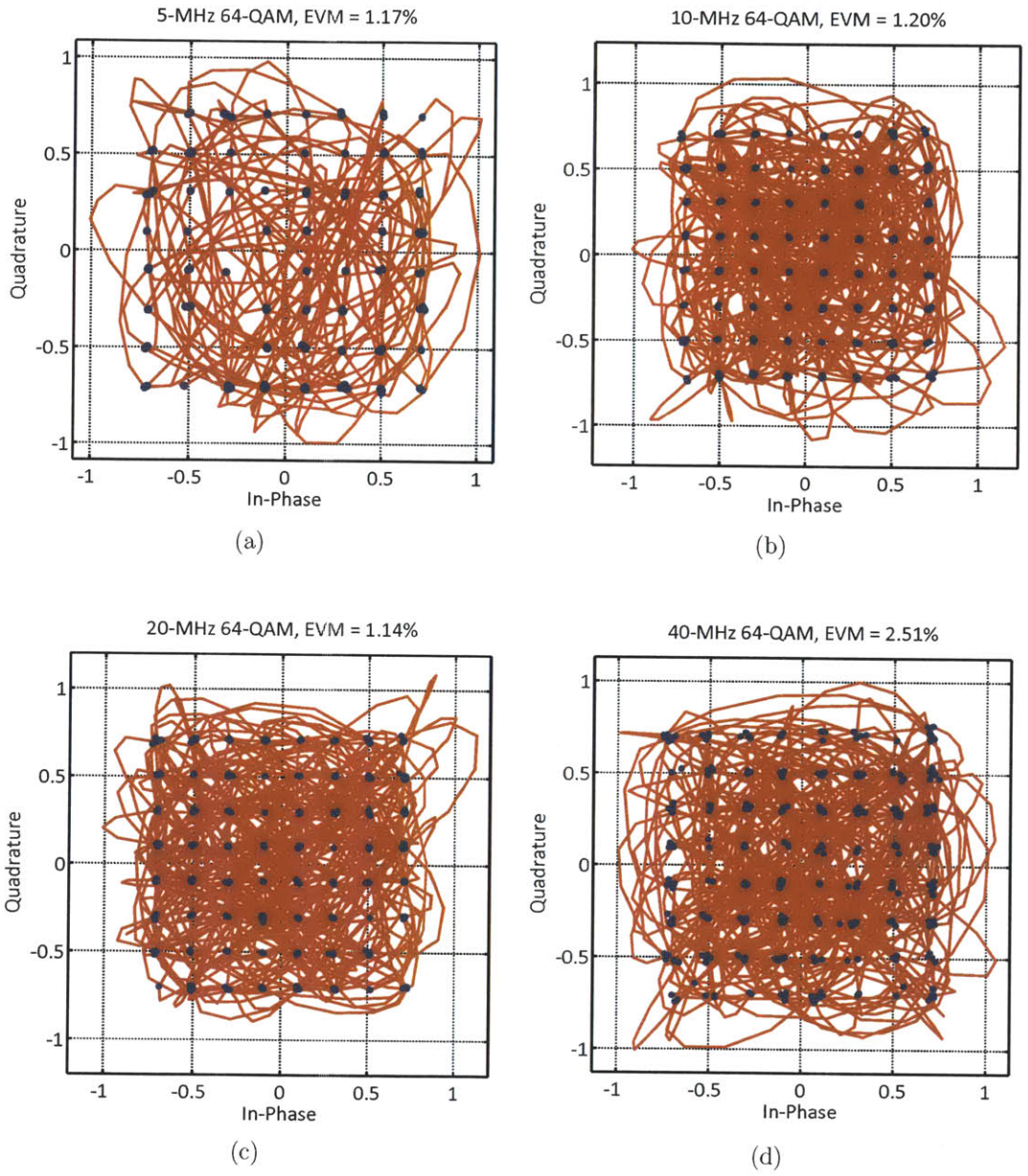


Figure 5-28: Constellation diagram of a 64-QAM signal transmitted by the AMO system at various symbol rates for the 2.4-GHz AMO transmitter. (a) 5 MHz. (b) 10 MHz. (c) 20 MHz. (d) 40 MHz.

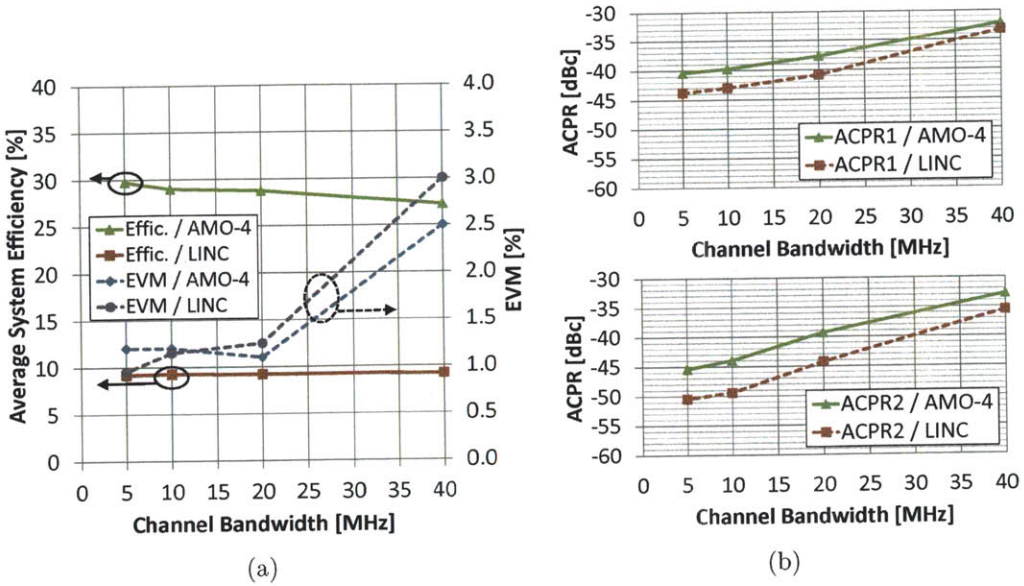


Figure 5-29: Performance comparison of the LINC and 4-level AMO systems for the 2.4-GHz AMO IC prototype, for the transmission of a 7.0-dB PAPR 64-QAM signal at various channel bandwidths. (a) EVM and average system efficiency. (b) ACPR at 1st and 2nd channel offsets.

efficiency and high-bandwidth wireless transmission. Also shown in Figure 5-30 is the efficacy of the system for the 64-QAM transmission. We define the efficacy as the ratio of the average system efficiency to the efficiency of the system at peak-envelope power (PEP). The efficacy is around 65% for all channel bandwidths up to 40-MHz, which is very high.

Figure 5-31 show the spectrum of the 64-QAM signal transmission at the various symbol rates for both the LINC and AMO systems. The curves labeled "DAC" show the spectrum using just the phase modulators without the PAs; these are shown as a reference for the input signal driving the AMO system. It can be seen that for symbol rates 20 MHz or less, the noise floor of the AMO system is about 10dB higher than the LINC case. Again, this is due to the finite settling time of the PAs in response to the abrupt amplitude/phase changes, causing glitches in the output waveform which show up as a higher noise floor. However, despite the increased noise floor, the AMO transmitter still meets the spectral mask requirements for 20-MHz WLAN signals, which requires a noise floor of -40 dB relative to the peak spectral component.

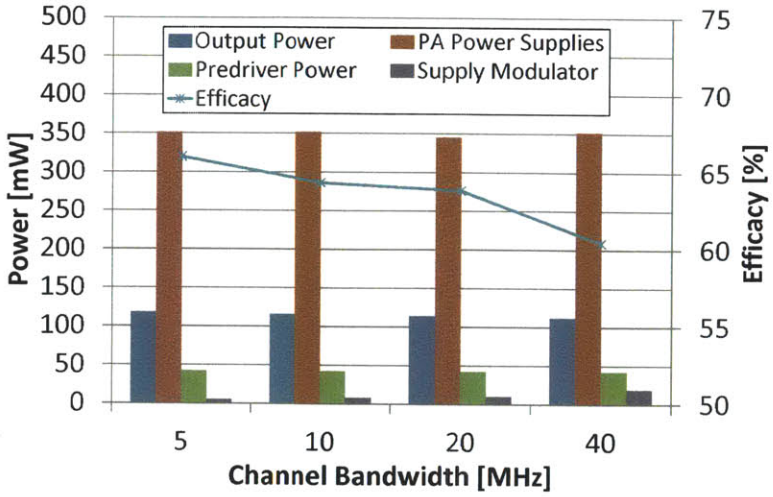
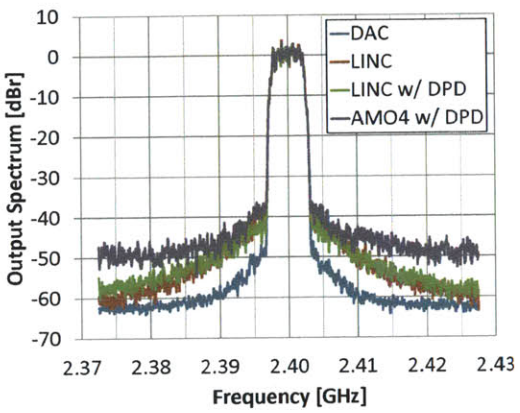


Figure 5-30: Power breakdown and efficacy of the 2.4-GHz AMO IC prototype for the 64-QAM signal transmission for various channel bandwidths.

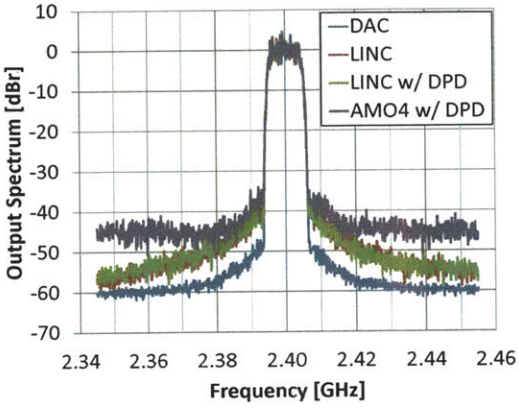
Finally, Table 5.1 compares the efficiency of the 2.4-GHz AMO transmitter with other published works made in CMOS in the frequency range of 2-2.7 GHz and for signal bandwidths 10 MHz or higher. Note that the AMO transmitter achieves an average system efficiency of 28.7%. To the author's best knowledge, this is the highest reported average efficiency in the literature for a CMOS PA in this frequency range for signal bandwidths greater than 10 MHz.

5.8 Summary

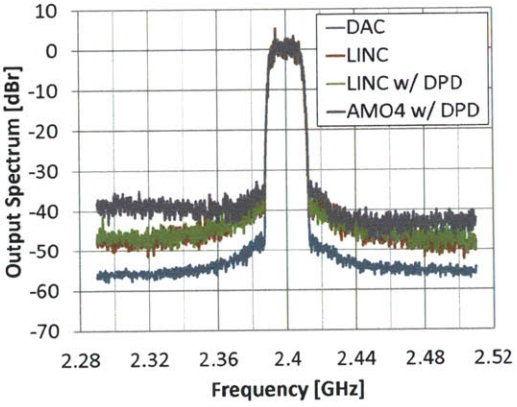
The 2.4-GHz, 27-dBm AMO prototype implemented in 65-nm CMOS demonstrates the feasibility of the AMO system for mobile wireless applications. The AMO transmitter uses discrete supply-voltage modulation for fast and efficient coarse-amplitude control, and outphasing for fine-amplitude control. The 4-level AMO system improves the efficiency of the standard outphasing system by 3x for a 64-QAM signal with 7.0-dB PAPR and symbol rates as high as 40MHz. This prototype shows that the AMO system can be integrated in silicon and still achieve a relatively high efficiency for wide bandwidth signals, making it suitable for mobile wireless applications in addition to cellular basestations.



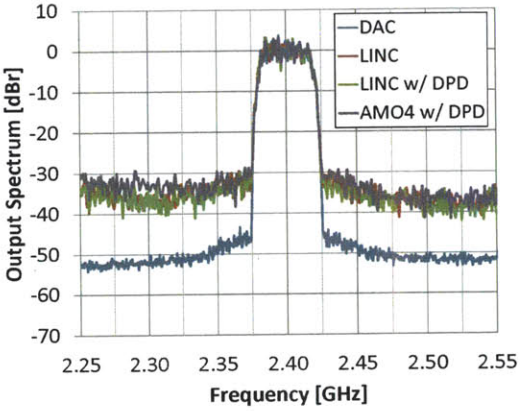
(a) 5 MHz



(b) 10 MHz



(c) 20 MHz



(d) 40 MHz

Figure 5-31: Transmit spectrum of a 64-QAM signal at various symbol rates for the 2.4-GHz AMO transmitter. (a) 5 MHz. (b) 10 MHz. (c) 20 MHz. (d) 40 MHz.

System Architecture/ Author	Freq/ BW (MHz)	Modulation/ PAPR	Tech.	P_{out} (dBm)	Peak PAE/ Avg PAE (%)	Efficacy (%)
Class-E AMO (This Work)	f_c=2400, BW = 20	64-QAM, 7.0 dB	65 nm	27.7/ 20.6	45.1/ **28.7**	**64**
Switched-capacitor PA (S. Yoo, ISSCC 2011)	f_c=2250, BW = 20	OFDM/64-QAM, 7.5 dB	90 nm	25.2/ 17.7	45.0/ **27.0**	**60**
Class-AB (O. Degani, RFIC 2009)	f_c=2500, BW = 10	WiMAX 7.0 dB	90 nm	32.0/ 25.0	48.0/ **25.0**	**52**
Class-AB (A. Afsahi, RFIC 2009)	f_c=2442, BW = 20	WLAN/64-QAM, 5.9 dB	65 nm	28.3/ 22.4	35.3*/ **23.2***	**66**
Class-G Polar (J. Walling, JSSC 2009)	f_c=2000, BW = 20	OFDM/64-QAM, 9.7 dB	130 nm	29.3/ 19.6	69.0/ **22.6**	**33**
Class-D Outphasing (H. Xu, JSSC 2011)	f_c=2400, BW = 20	WLAN/64-QAM, 5.8 dB	32 nm	25.3/ 19.6	35.0/ **21.8**	**62**
Inverse Class-D (D. Chowdhury, RFIC 2011)	f_c=2250, BW = 20	WLAN/64-QAM, 7.8 dB	65 nm	21.8/ 14.0	44.2*/ **18.0***	**39**

* Drain Efficiency, not PAE

Table 5.1: Performance comparison for CMOS PAs in the frequency range of 2-2.7 GHz for signal bandwidths 10 MHz or higher.

Chapter 6

Conclusion and Future Work

6.1 Summary of Contributions

There are two main contributions of this thesis. The first is the design, analysis, and implementation of the outphasing energy recovery amplifier (OPERA) with resistance compression, a new PA architecture for achieving high efficiency and high linearity power amplification. Energy recovery for outphasing systems has been presented in previous works, but the proposed systems still suffered from excessive load impedance variation for the two outphased PAs, resulting in degraded efficiency and linearity. In this work, a resistance compression network (RCN) is applied to the energy recovery network for the first time to effectively reduce the impedance variation to an acceptable range. Detailed analyses of both the energy recovery network and the RCN were given, including the bandwidth limitations of the technique. A 48-MHz discrete-component prototype was presented which demonstrated a significant increase in efficiency of more than 2x over the standard outphasing system while maintaining adequate linearity. Furthermore, the total power dissipation of the OPERA prototype was reduced to 30% of the value using the standard outphasing system.

The second main contribution of this thesis was the design and implementation of the asymmetric multilevel outphasing (AMO) system, another new PA architecture that has the potential to achieve high efficiency, high linearity, and high modulation

bandwidth simultaneously. A multi-level outphasing system using discrete supply-voltage modulation (DSVM) had been proposed in previous works, but a real system with measurement results had not yet been published. This thesis presented three different prototype implementations of the AMO system, proving the multi-level outphasing concept with real circuits. Furthermore, the additional flexibility of asymmetric power combining in the AMO system was also proposed and implemented in the prototypes which had never been published before. In addition, discrete pulse-width modulation (DPWM) was proposed as an alternative method for generating the multiple levels in the AMO system, and one of the prototypes used this method for demonstration of the AMO system.

This thesis includes the first detailed description of the operation of the AMO system, including the required signal decomposition for the AMO modulation and the theoretical efficiency. A method for optimizing the values of the discrete amplitude levels for maximum efficiency was presented, which is useful for multi-standard wireless communication systems. A linearization technique based on lookup table training which is specific to AMO was also developed to correct for system nonlinearities. Finally, the design and implementation of three different AMO prototypes is described in detail, each for a different purpose and application.

The first prototype was built with discrete components to prove the concept, operating at 48 MHz and employing DPWM for the multi-level outphasing. For a 16-QAM signal with 6.5-dB PAPR, this prototype improved the efficiency of the standard outphasing system from 17% to 37%, an improvement of more than 2x. The second prototype was also built with discrete components and was intended to prove the AMO concept for basestation applications, operating at 1.95 GHz with a peak output power of 18 W. This prototype used DSVM to generate 4 discrete amplitude levels and demonstrated the potential of the AMO system to achieve both high efficiency and wide bandwidth signal transmission. For a 16-QAM signal with 6.5-dB PAPR, the basestation prototype improved the efficiency of the standard outphasing system from 15% to 45% for symbol rates up to 40 MHz, an improvement of more than 3x. The third and final prototype was an integrated circuit (IC) implemented in a 65-nm

CMOS process, intended to prove the AMO concept for mobile wireless applications. This IC prototype operated at 2.4 GHz with a peak output power of 27 dBm and employed 4-level DSVM. For a 64-QAM signal with 7.0-dB PAPR, the 4-level AMO system improved the efficiency of the standard outphasing system from 9% to 28% for symbol rates up to 40 MHz. The IC prototype showed that the AMO system can be integrated in silicon and still achieve a relatively high efficiency for wide bandwidth signals, making it suitable for mobile wireless applications in addition to cellular basestations.

6.2 Future Work

Although the prototypes implemented in this thesis have shown good results, there are still many ways they can be improved. For the OPERA system with resistance compression, the prototype operated at an RF carrier frequency of 48 MHz. While this frequency is acceptable for proof-of-concept, it is much lower than those used in modern wireless communication systems, which are typically in the GHz range. Higher frequency prototypes should be designed and implemented to demonstrate the feasibility of the OPERA system for modern wireless communication.

For the AMO system, one problem that has not been addressed is the higher noise floor compared to the standard outphasing system. This noise-floor increase can be unacceptable in many applications, causing a violation in the spectral mask requirement for a given wireless communication standard. One technique that can be used to reduce this noise floor is to slow down the supply voltage transitions so that it is a linear ramp rather than an abrupt change. Because real circuits have finite bandwidth, the abrupt amplitude and phase changes are filtered such that a transient glitch appears in the output waveform. Using a slower, linear ramp for the amplitude change from one level to another would help eliminate this problem. The linear ramp would still have to be relatively fast so that high modulation bandwidth can be achieved. Futhermore, the phase would have to track the linear amplitude ramp, so that a much higher sampling rate for the phase modulator would be required.

The AMO prototypes in this thesis all employed static digital predistortion to correct for system nonlinearities. This static predistortion was based on lookup table training (LUT) at one specific frequency in periodic steady-state. However, wide bandwidth signals occupy a large frequency range where the lookup table may no longer be valid. Furthermore, when the signal amplitude and phase change from one value to another, there is a transient that must settle before periodic steady-state is reached and the LUT becomes valid. The transient behavior will depend on the specific amplitude and phase transition, such that the current signal amplitude and phase will depend on the past signal values. This is the so-called memory effect [64]. These memory effects degrade the ACPR, becoming worse and worse as the modulation bandwidth increases. There are many methods for memory-effect compensation (see, for example, [64]), but applying these methods to the AMO system is not a simple task due to the abrupt amplitude and phase changes and is another area for future research.

All the AMO prototypes presented in this thesis used isolating, lossy power combiners. However, it is possible to use the AMO system with a lossless, non-isolating combiner such as the Chireix combiner discussed in Section 2.5.1. The disadvantage of the Chireix combiner is that it can only be tuned to provide high efficiency for a small range of outphasing angles. However, since the AMO system minimizes the outphasing angles of the system through discrete amplitude modulation, a large range of outphasing angles is not required, making the Chireix combiner particularly suited for the AMO system. Because the Chireix combiner is lossless, the efficiency of the AMO system would increase significantly.

The AMO system can also be combined with the OPERA system by using an energy recovery combiner, which replaces the isolation resistor of a conventional combiner with an energy recovery network. By employing the resistance compression technique to the energy recovery network, the combiner becomes semi-isolating, providing sufficient isolation between the two PAs while enhancing efficiency by recovering the normally wasted power back to the power supply.

AMO uses 2 PAs to perform outphasing, which is used to vary the output am-

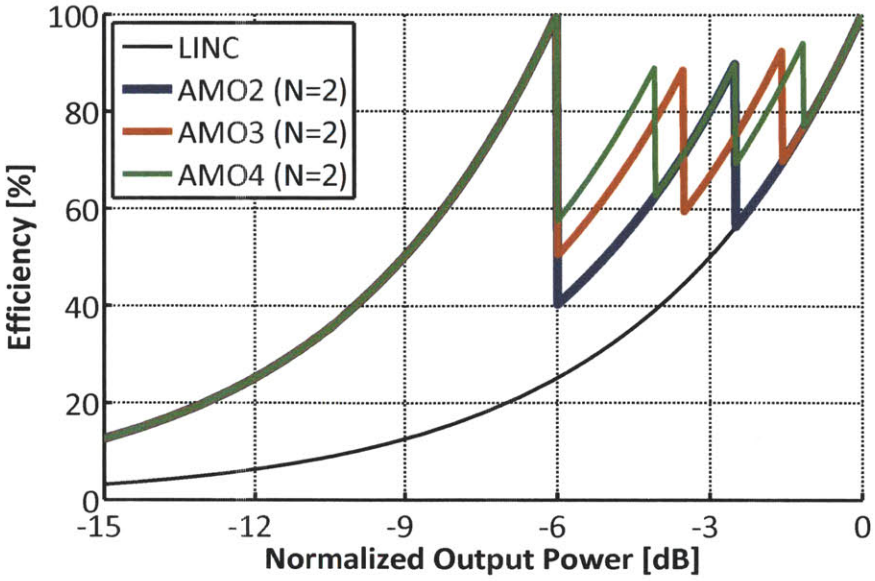


Figure 6-1: Theoretical efficiency for the AMO system using 2, 3, and 4 PAs. 2 supply voltages are available for each case, with the amplitude levels spaced 6 dB apart.

plitude for fine amplitude control. However, it is possible to apply the outphasing concept of vector addition to more than 2 PAs. If M PAs are used, an M-way power combiner could be used to combine the M PA outputs to generate a varying-envelope signal. Using more than 2 PAs in the AMO system offers more flexibility which can be used to achieve even higher efficiency. This can be seen in Figure 6-1, which compares the efficiency of the AMO system using 2, 3, and 4 PAs, with 2 supply voltages available for all cases. The efficiency enhancement afforded by increasing the number of PAs beyond 2 can be used to decrease the number of supply voltages in the AMO system, making power management simpler. However, the disadvantage is that it is harder to implement the power combiner, since more than 2 sources must be combined. This also typically increases the insertion loss of the combiner. Figure 6-2 compares the efficiency of the AMO system using 2, 3, and 4 PAs, with 4 supply voltages available for all cases.

The AMO system is a hybrid system that combines polar modulation with outphasing modulation. Another hybrid system that has potential is a multi-level PWM PA, which combines polar modulation with pulse-width modulation. Discrete ampli-

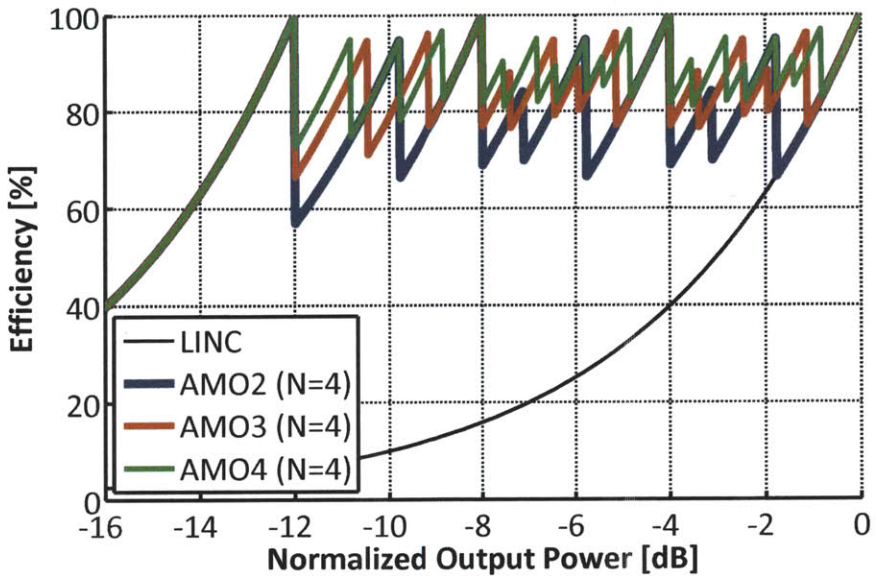


Figure 6-2: Theoretical efficiency for the AMO system using 2, 3, and 4 PAs. 4 supply voltages are available for each case, with the amplitude levels spaced 4 dB apart.

tude modulation would be used for coarse amplitude control and increased efficiency at power backoff, while pulse-width modulation would be used for fine amplitude control. Since PWM has higher efficiency than outphasing as shown in Figure 2-7, this system can theoretically achieve a higher efficiency than the AMO system used with an isolating combiner. However, the AMO system used with a non-isolating combiner as discussed above would still have a higher theoretical efficiency than a multi-level PWM PA.

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