Universidad Carlos III de Madrid

Bachelor Thesis

Biomedical Engineering

Design of Operational Amplifiers with Feedforward multistage architecture in CMOS low voltage technology for biomedical instrumetation applications.

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1 Introduction

Magnetic Resonance (MRI) is an imaging technique used to obtain anatomical and structural features of a patient's body. The creation of a measurable signal is based on the varying water concentration throughout the body. The atoms which participate actively in such event are the hydrogen atoms from water, which create a varying magnetic field in response to a radiofrequency pulse. Such radiofrequency pulse is applied perpendicular to a main magnetic field created by a gradient coil, which is in charge of aligning the magnetic moments of hydrogen atoms. Upon application of the radiofrequency pulse, magnetic moments of hydrogen atoms rotate 90º with respect to the main field, creating a varying magnetic field which can be converted into a current through the use of coils.
The detection of such current is achieved through the use of sensors, and constitutes a crucial step for the creation of an image based on the information emanating from the magnetic resonance equipment. Bearing in mind that a 1.5 Tesla MRI contains around 80 sensing components, the key element in MRI is the data acquisition block which forms part of each individual sensor. This data acquisition block contains a sensor, a band pass filter, and a band pass Analog to Digital Converter (ADC). From these three elements, the one in charge of the final resolution so that the digital part can appropriately process each sensor's information is the ADC. Therefore, the accuracy of the ADC's performance influences image processing steps to be performed afterwards for the final creation of an image.
An Analog to Digital Converter can be built in several ways, either through a subsampling pipeline or band pass Sigma Delta. In both cases, the key elements which influence the resolution of the ADC are the operational amplifiers with which they are built up. Subsampling pipelines make use of operational amplifiers in order to sample the input signal in successive steps, whereas band pass Sigma Delta circuits use them to filter the quantification noise around a specified frequency.
The ADC which will be used for the purpose of this work is a band pass Sigma Delta modulator whose bandwidth and center frequency are respectively 1MHz and 140MHz. The main objective of this work is to build a model of a real operational amplifier to be used in the filter of the ADC.

1.1 Objectives

The objectives of this work are divided as follows:

1. Design of an operational amplifier model. The design is focused on achieving a pre-defined Bode plot, and hence the objective is to create an operational amplifier which gives a magnitude and frequency response as close as possible to the Bode to be obtained.
2. Arranging the designed operational amplifier in an integrating configuration. The objective is to obtain a "low frequency response" corresponding to that of an ideal integrator circuit and a "high frequency response" corresponding to the real pre-designed operational amplifier.
3. Integrating the operational amplifier with the integrator configuration in a Sigma Delta Band Pass modulator model. Such model contains among other elements, a band pass filter formed by two cascaded integrators. The

objective is to obtain a Sigma Delta modulator model which gives a "real" response due to the pre-designed operational amplifiers, and not an "ideal" one. Therefore, this third objective consists on introducing the operational amplifier model, arranged in negative feedback with a capacitor to provide the integrating function into another Simulink model of a Sigma Delta band pass modulator which was built by a colleague at the Electronics Technology department.

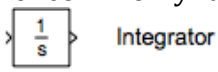
4. Simulation of each of the above mentioned objectives, as well as the entire model to extract the main imperaments such that the analog designer can use them to design the electrical circuit.

1.2 Motivation

Sigma Delta modulators represent a means of obtaining high resolution analog to digital conversion. The removal of quantization noise from the band pass allowed by the system is achieved by two characteristic phenomena of this type of circuits: oversampling and noise shaping. The "tuned" output noise is then digitally low-passed filtered, whereas for the oversampling ratio, it determines the overall resolution of the modulator (in fact, they are linearly proportional). Indeed, Sigma Delta modulators present noticeable advantages due to these two phenomena, the only drawback probably being their limitation in terms of the wideness of the frequency band that they can convert. Increasing the signal band to be digitally converted implies the specific design of the operational amplifiers which are used in integrating configuration by Sigma Delta modulators. [1]
The desire to design a model of an operational amplifier is to be able to simulate a real response of the use of such systems in integrating configuration and ultimately, to use them in a Sigma Delta Band Pass modulator. The creation of a model meeting certain pre-specified criteria will enhance the behavior of the overall system, additionally, simulating a more realistic system by substituting a purely ideal integrator by a real one allows for a precise estimation of the outcome of the circuit it is modelling. The ultimate goal of such real model is to incorporate it in a Sigma Delta Band pass modulator in order to simulate the behavior of the entire system, thereby obtaining a description of the precise behaviour of a system which is going to be implemented in sensing signals produced during the performance of magnetic resonance imaging.
The underlying motivation of the whole procedure is to predict the real performance of the sensing circuit in magnetic resonance. Through the use of the mentioned models, the response provided could be precisely adjusted by tuning the values of the parameters that build up the system.

1.3 Presenting the problem

When trying to improve a given system, the modelling and simulation of such system gives an accurate estimate of the actual behavior of the future system when built up. Data acquisition blocks which build up each of the sensors present in MRI equipment, represent a crucial step for the digitalization of the sensed signal and subsequent processing for the final formation of an image. The fidelity with which the analog to digital conversion is carried out determines the overall resolution of

the data acquisition process. A system which presents useful properties in the ADC process is a Sigma Delta band pass modulator, which is composed of operational amplifiers arranged in integrating configuration, the number of which depends on the order of the system.
When modelling a Sigma Delta Band Pass modulator, the two cascaded integrators which build up the system are commonly approximated through the use of Simulink's integrator function: 

The problem with such estimation, is that the system is treated as purely ideal, and this does not correspond to the actual, "real" behavior of the system. Furthermore, by creating an operational amplifier which meets a given criteria, the whole "integrator" can present more effective functions in the analog to digital conversion as compared to the ideal model. Hence it is needed to create a model which incorporates the functioning of a real operational amplifier. The resulting model will be manipulated in order to obtain from it the desired magnitude and frequency response. By tuning the parameters which build up the model, different responses will be created for different input frequencies.
The built operational amplifier model, will be arranged in integrating configuration and ultimatelty incorporated in a Sigma Delta band pass modulator in order to be able to simulate the behavior of the Analog to Digital Conversion process with high fidelity and accuracy.

1.4 Planning

The mentioned objectives were carried out in the following manner:

Table 1.4-1:Planning

Objective	January	February	March	April	May	June
1.Design of an operational amplifier model	✓	✓				
2. Integrator operational amplifier			✓	✓		
3. Integration in a Sigma Delta Band Pass circuit					✓	✓
4. Simulation		✓		✓		✓

1.5 Regulatory frame

In order to carry out the development of the work mentioned, several regulatory issues had to be taken into account to perform it in a legal manner.
To begin with, the most frequently used program was Simulink, where most of the modelling and simulation procedure was carried out. Simulink is a useful programming tool used frequently for modeling and simulation of dynamic systems, it also allows the analysis of such systems and is tightly integrated with Matlab's environment. This integration between both environments allowed the use of Matlab and Simulink simultaneously for the purpose of declaration of variables, saving data from Simulink models and plotting results. These programs could be used thanks to the license available through the university Carlos III, and hence both the modelling and simulation of the systems was performed at the university through the use of its computers with an installed Matlab software. Particularly, the work was developed at the Electronics Technology department.
Secondly, another program which was useful in the development of the work was Cadence Design Systems. It consists on an electronic design automation (EDA) software which results very useful in the design of integrated circuits. Once again, the license provided by the Univeristy Carlos III lead to the use of Cadence at the university's computers. Although Cadence was not used for the purpose of operational amplifier design, modeling or simulation, it was used by other colleagues at the Electronics department for the design of the Sigma Delta band pass system.
Finally, due to the confidentiality of the work which is carried out by the Electronics Technology department, a non-disclosure agreement (NDA) was signed to ensure the protection of the information shared during the development of the project.

2 Design of an operational amplifier

The first objective consists on the design of an operational amplifier model. The characteristics of the circuit were chosen to achieve a pre-defined Bode plot, hence the system was built taking into account the desire to obtain a particular response from it.

2.1 State of the art

Operational Amplifiers play a significant role in circuit design due to their active participation in processes such as data conversion, sensors, filters and many more applications. The evolution of CMOS technology has established a general trend of scaling down dimensions, which have lead to a decrease in supply voltages while transistor threshold voltages are being kept constant. The major consequences of this size reduction trend are the decrease in open loop gain, an increase in transistion frequency (speed of operation), as well as the appearance of random offsets. Subsequently, the vertical cascoding of them in order to obtain high gains is becoming less useful. These facts call out for the need to implement multistage horizontal cascading to achieve low supply voltage implementation of operational amplifiers.[2]
Therefore, the objectives in these technological developments have been primarily focused on enhancing the effectiveness of compensation techniques, achieving appropiate offsets, reducing power cosumption and system dimensions and obviously keeping the noise to a minimum. In order to achieve this multiple systems have been developed.[2]
Single stage operational amplifiers are useful in terms of stability, due to the presence of a single pole. However, these systems present limitations regarding the DC gain that can be obtained with them. It is therefore needed to use higher order systems while at the same time maintaining the phase response of the system at unity gain frequency sufficiently higher than -180º, a procedure which is known as “compensation techniques”.[3]

2.1.1 Single Stage Operational Amplifier Realization

The starting point of the discussion obviously begins with a single stage operational amplifier realization. An integrating function is desired for the operational amplifier under study, and the circuit elements which perform integrating functions are capacitors and inductors. The former which integrates current, and the latter, voltage.

Equation 2.1-1Voltage through a capacitor

$$v_c = \frac{1}{C}\int i_c dt$$

Equation 2.1-2: Current through an inductor

$$i_L = \frac{1}{L}\int v_L dt$$

However, in practice, it is easier to fabricate good quality capacitors and hence it will be capacitors the ones used for the purpose of integration.
So, in order to obtain the integrating function it is needed to convert the voltage which enters through the amplifier (Vd) to a current, which is achieved through the implementation of the following circuit:

Figure 2.1-1: Ideal integrator

By using a voltage controlled current source (also known as transconductor) with a proportionality constant Gm (also known as transconductance), a current with a value of Gm·Vd emerges from it. Such output current flows through a capacitor (C), resulting in a voltage which is equal to:

Equation 2.1-3: Ideal integrator output voltage

$$V_{out} = \frac{G_m}{C} \int V_d dt$$

Where the term left outside the integral indicates the unity gain frequency. This is the simplest implementation of an integrating operational amplifier and obviously, an ideal one. However, since a real model is desired several considerations have to be taken into account. First of all, it is impossible to create an ideal current source, they always include an inherent output resistance, giving rise to the following circuit:

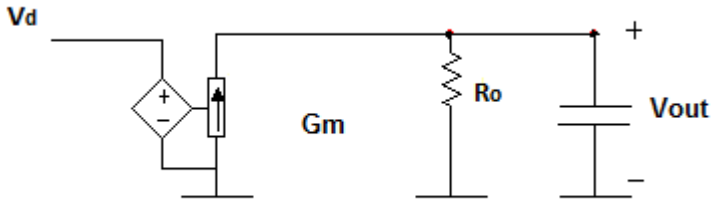


Figure 2.1-2: Real integrator

Taking this into account, and applying the Laplace transform to substitute the integrals, the difference between real and ideal circuits regarding their transfer functions is:

Table 2.1-1: Comparison between real and ideal integrator output voltage

IDEAL	$\frac{V_{out}}{V_d} = \frac{G_m}{sC}$

REAL	$\frac{V_{out}}{V_d} = \frac{G_m R_0}{sCR_0 + 1}$

This shows that actually the difference between an ideal situation and a real one lies in the location of the poles. An ideal integrator contains a pole at the origin and a real one experiences a shift of that pole to greater frequencies of the Bode plot. Also, ideally an integrator has infinite DC gain, and a real one has a finite DC gain until the location of the pole, when it starts to integrate.

IDEAL

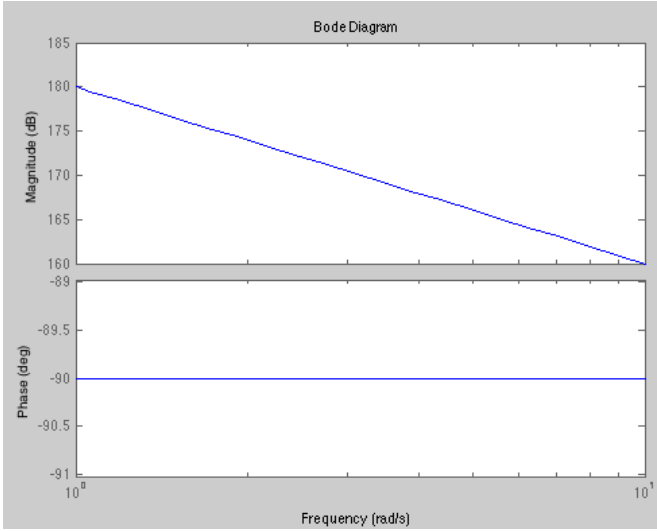


Figure 2.1-3: Ideal integrator Bode plot

REAL

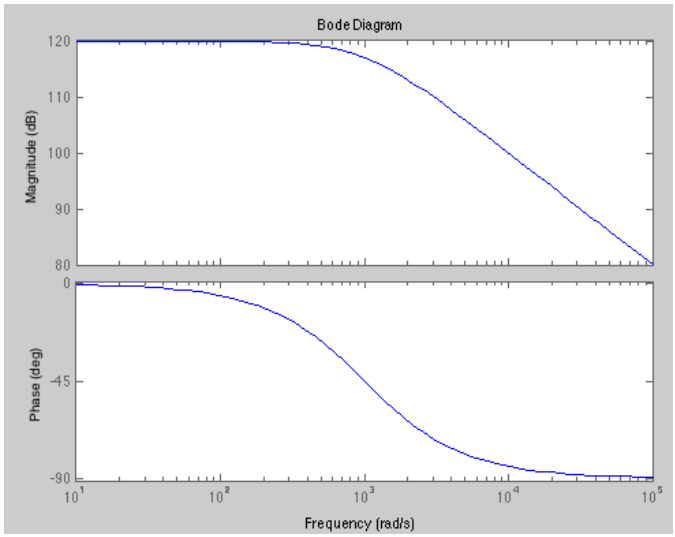


Figure 2.1-4: Real integrator Bode plot

The difference between both Bode plots lies in the frequencies which have a value smaller than ($1/CR_0$). Beyond that point, the behaviour is exactly the same. This can be explained by the impedance of the capacitor and ouput resistance; at very

high frequencies, the capacitor presents a higher impedance to the system than the resistance, hence most of the current will be flowing through the capacitor rather than the resistance. Regarding the unity gain frequency of the real system, we see that:

Equation 2.1-4: Unity Gain Frequency of a real integrator

$$\left|\frac{G_m}{jw_uC+\frac{1}{R_0}}\right| = 1$$

$$G_m{}^2 = w_u{}^2C^2 + \frac{1}{R_0{}^2}$$

$$w_u{}^2 = \frac{G_m{}^2}{C^2} - \frac{1}{C^2R_0{}^2}$$

This shows that, as long as the second term is small enough, or in other words, as long as $C^2R_0{}^2$ is sufficiently large, the unity gain cut-off frequency will be the same for the real and ideal case. This will take place in almost every operational amplifier, because if this condition is broken, it will result in a system which does not work.

Recognizing that the term $G_m \cdot R_0$ represents the low frequency (or DC) gain of the operational amplifier (A_0), and taking into account the expression derived for the unity gain frequency (w_u), the transfer function becomes:

Equation 2.1-5: Transfer function of a real integrator

$$\frac{V_{out}}{V_d} = \frac{A_0}{1+s\frac{A_0}{w_u}}$$

Due to the presence of R_0, the DC gain of the operational amplifier is finite. Hoewever, for certain applications it is required that the DC gain be greater than a certain value which is not possible to reach with this basic circuit. Hence, it is needed to use a combination of various amounts of single stage operational amplifiers in different configurations to reach the desired DC gain, without compromising the stability of the system.

To conclude with single stage operational amplifiers, it is important to state that they are stable systems. This can be reasonably explained by using Nyquist plot, but more simply, by noticing that it is a first order system and therefore contains only one pole. Due to the presence of a single negative pole, the minimum phase response that the system can reach is -90º caused by the phase lag contribution at frequencies higher than the pole of the system. [4][5][6][7][8][9][10][11][12][13][14]

2.1.2 Two Stage Miller Compensated Operational Amplifier

Single stage operational amplifiers present limitations regarding the DC gain that can be obtained with them. This is due to the presence of a finite output resistance emanating from the voltage controlled current source. Additionally, in the presence of external loads, the low frequency gain also becomes limited, since this impedance will be in parallel with the output resistor. The achievement of higher DC gains can be obtained by increasing R_0 although this approach obviously doesn't apply for the case in which another resistor is present. In this case, it becomes necessary to use alternative models.
Two stage Miller compensated operational amplifiers deal with the increase in DC gain in the presence of external loads. This problem stems from the following circuit configuration:

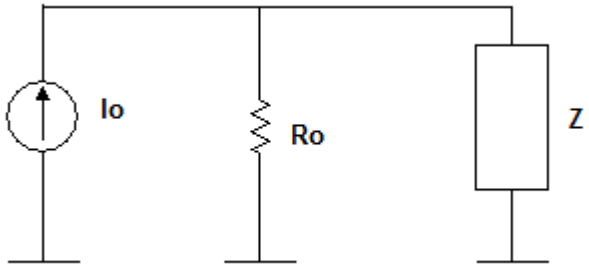


Figure 2.1-5: External load in parallel with resistor

Obviously, the output voltage will not be equal to the product of the current source and the resistor, it must be taken into account that the resistor is in parallel with another load. An effective way to deal with this problem is to place a current controlled voltage source through the use of an operational amplifier which inlcudes the capacitor load in negative feedback configuration.

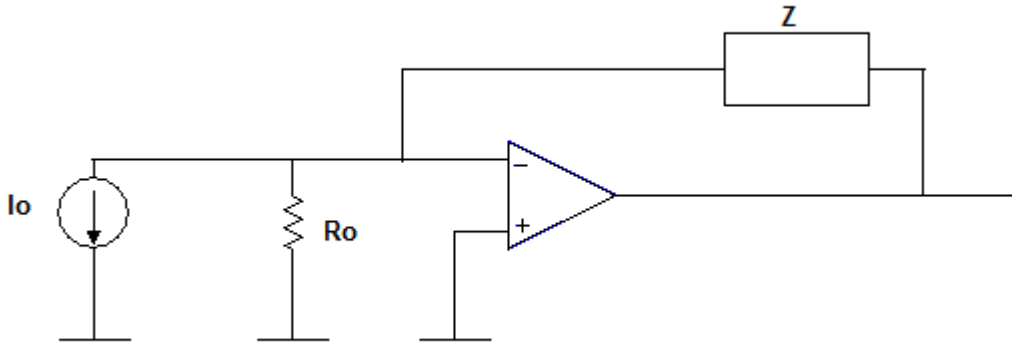


Figure 2.1-6: Circuit to deal with the presence of al external load

Ideally, even in the presence of R_0 the output of this system will be the input current I_0 times the external load. However, it must be taken into account that the operational amplifier is not ideal, and behaves effectively as a voltage controlled current source only in the range of frequencies where the loop gain is big enough.
Taking into account that I_0 represents the current resulting from a previous voltage controlled current source, and that the output resistance represents the

resistance from such transconductor, the real representation of the above circuit becomes:

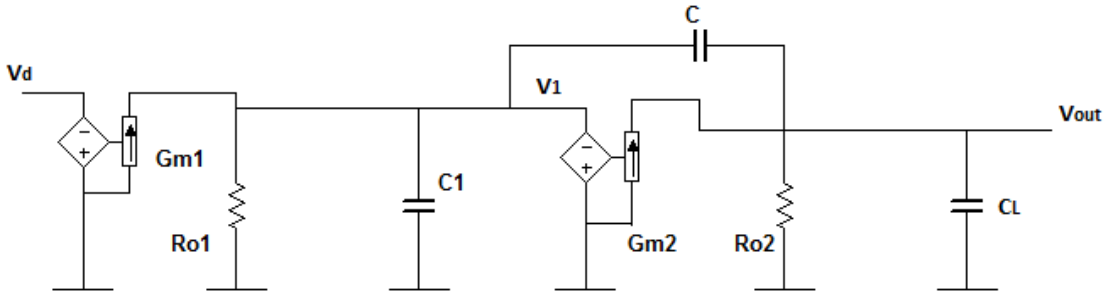


Figure 2.1-7: Two Stage Miller Compensated Operational Amplifier

For simplicity, the transfer function will be calculated in matrix form using the admittance matrix and voltage vector at each node and equating them to the total input current. The system will be solved using Cramer's rule and the reciprocal of resistances will be expressed as G:

Equation 2.1-6:: Two Stage Miller compensated Operational amplifier transfer function

$$\begin{bmatrix} s(C_1+C)+\frac{1}{R_{0_1}} & -sC \\ G_{m_2}-sC & s(C_L+C)+\frac{1}{R_{0_2}} \end{bmatrix} \begin{bmatrix} V_1 \\ V_{out} \end{bmatrix} = \begin{bmatrix} -G_{m_1}V_d \\ 0 \end{bmatrix}$$

$$V_{out} = \frac{\begin{vmatrix} s(C_1+C)+\frac{1}{R_{0_1}} & -G_{m_1}V_d \\ G_{m_2}-sC & 0 \end{vmatrix}}{\begin{vmatrix} s(C_1+C)+\frac{1}{R_{0_1}} & -sC \\ G_{m_2}-sC & s(C_L+C)+\frac{1}{R_{0_2}} \end{vmatrix}}$$

$$V_{out} = \frac{G_{m_1}(G_{m_2}-sC)V_d}{s^2(C_1C+CC_L+C_LC_1+C^2-C^2)+s\left(C\left(G_{m_2}+G_{0_2}+G_{0_1}\right)+C_LG_{0_1}+C_1G_{0_2}\right)+G_{0_1}G_{0_2}}$$

$$\frac{V_{out}}{V_d} = \frac{G_{m_1}(G_{m_2}-sC)}{s^2(C_1C+CC_L+C_LC_1+C^2-C^2)+s\left(C\left(G_{m_2}+G_{0_2}+G_{0_1}\right)+C_LG_{0_1}+C_1G_{0_2}\right)+G_{0_1}G_{0_2}}$$

By inspection one can see that the DC gain of the system is simply equal to the product of the individual DC gains at each stage, as well as for the location of the zero, which can be straightforwardly derived:

Equation 2.1-7: DC gain of Two Stage Miller Compensated Operational Amplifier

$$\frac{V_{out}}{V_d}(s=0) = \frac{G_{m_1}G_{m_2}}{G_{0_1}G_{0_2}}$$

Equation 2.1-8: Zero of Two Stage Miller Compensated Operational Amplifier

$$z = \frac{G_{m_2}}{C}$$

Regarding the poles, the common solution to a quadratic equation will not work due to the complexity of the coefficients a,b and c:

Equation 2.1-9: Solution to a quadratic equation

$$s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

and for simplicity, approximate methods will be applied. This approximation is based on the assumption that the difference of the magnitude of the roots is very big (i.e. the poles are very far apart), and consequently that both poles are real, because in the case of having roots which are complex conjugates of each other, their magnitudes will be exactly the same and the assumption does not hold.

Equation 2.1-10: Solution to a quadratic equation,in terms of the poles of the transfer function

$$as_1{}^2 + bs_1 + c = 0$$
$$as_2{}^2 + bs_2 + c = 0$$

Assuming $|s_1| \ll |s_2|$, the term $as_1{}^2$ is negligible compared to the others, hence:

Equation 2.1-11: Approximation to find the first pole

$$bs_1 + c = 0$$
$$s_1 = \frac{-c}{b}$$

As for s_2, c is negligible compared to the other terms, so:

Equation 2.1-12: Approximation to find the second pole

$$as_2{}^2 + bs_2 = 0$$

$$s_2 = \frac{-b}{a}$$

Substituting the coefficients, the values of the poles are:

Equation 2.1-13: Value of the poles

$$p_1 = \frac{-G_{0_1}G_{0_2}}{C\left(G_{m_2} + G_{0_2} + G_{0_1}\right) + C_L G_{0_1} + C_1 G_{0_2}}$$

$$p_2 = \frac{-\left(C\left(G_{m_2} + G_{0_2} + G_{0_1}\right) + C_L G_{0_1} + C_1 G_{0_2}\right)}{C_1 C + C C_L + C_L C_1}$$

For the purpose of comparing these expressions with the poles resulting from a system without the presence of the negative feedback capacitor, the first pole will be divided by G_{02} (both numerator and denominator) and the second one will be multiplied by $\frac{1}{C+C_1}$, giving rise to:

Equation 2.1-14: Scaling of the poles

$$p_1 = \frac{-G_{0_1}}{C\left(\frac{G_{m_2}}{G_{0_2}} + 1 + \frac{G_{0_1}}{G_{0_2}}\right) + \frac{C_L G_{0_1}}{G_{0_2}} + C_1}$$

$$p_2 = \frac{-\left(\frac{C G_{m_2}}{C + C_1} + \frac{G_{0_1}(C + C_L)}{C + C_1} + G_{0_2}\right)}{\frac{C_1 C}{C + C_1} + C_L}$$

Considering the case where there is no capacitor placed in negative feedback, the transfer function will simply be the multiplication of two cascaded single stage operational amplifiers, whose poles have been previously derived. The comparison of the poles of both systems is:

Table 2.1-2:Comparison of the poles in the absence and presence of a feedback capacitor

	Without C	With C
p_1	$\frac{-G_{0_1}}{C_1}$	$\frac{-G_{0_1}}{C\left(\frac{G_{m_2}}{G_{0_2}} + 1 + \frac{G_{0_1}}{G_{0_2}}\right) + \frac{C_L G_{0_1}}{G_{0_2}} + C_1}$
p_2	$\frac{-G_{0_2}}{C_L}$	$\frac{-\left(\frac{C G_{m_2}}{C + C_1} + \frac{G_{0_1}(C + C_L)}{C + C_1} + G_{0_2}\right)}{\frac{C_1 C}{C + C_1} + C_L}$

This comparison gives a clear insight into the so-called Miller effect: a capacitor connected in negative feedback presents itself to the input as a much larger value of capacitance than its actual value. This increase is actually a multiple of the gain of the amplifier, and results in a decrease in the lowest pole and and an increase in the highest one. The increase in the highest pole is justified by the fact that the numerator is increasing enormously, since G_{m2} is generally much bigger than G_{02}, whereas the denominator is only increasing moderately, hence producing a net increase in the location of the higher pole. The fact that the first pole decreases and the second one increases is known as pole splitting.
Overall, the advantage of implementing this circuit configuration compared to a single stage operational amplifier lies in the value of the DC gain, which is greater for this case than for the previous one:

Table 2.1-3: Comparison of the DC gains of single stage and two stage Miller operational amplifiers

	Single stage op amp	Two stage Miller op amp
DC gain	$\frac{G_m}{G_0}$	$\frac{G_{m_1}G_{m_2}}{G_{0_1}G_{0_2}}$

Another advantage that this configuration presents appears when a resistive load is applied. In this case, the circuits will have the following configuration and DC gains:

SINGLE STAGE

Equation 2.1-15: DC gain of single stage operational amplifier with external load

$$G_{DC} = \frac{G_m}{G_{0_1} + G_L}$$

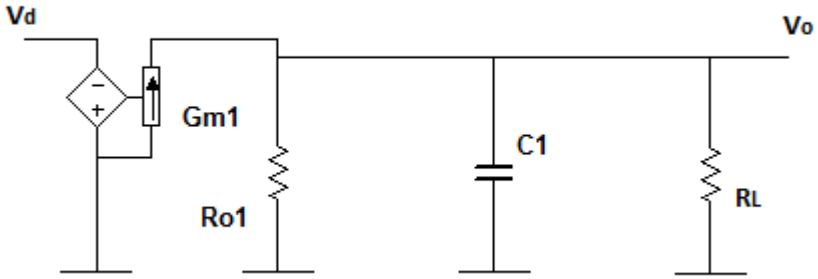


Figure 2.1-8: Single stage operational amplifier with external load

TWO STAGE MILLER

Equation 2.1-16: DC Gain of two stage Miller compensated operational amplifier with external load

$$G_{DC} = \frac{G_{m_1}G_{m_2}}{G_{0_1}(G_{0_2} + G_L)}$$

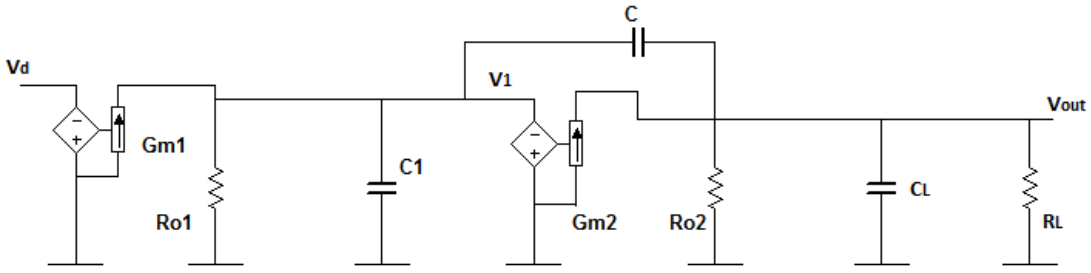


Figure 2.1-9: Two stage Miller compensated operational amplifier with external load

Regarding the single stage configuration, since $R_L \ll R_0 \rightarrow G_L \gg G_0$, the dc gain becomes: $G_{DC} = \frac{G_m}{G_L}$

As for the two stage configuration, since$R_L \ll R_{0_2} \rightarrow G_L \gg G_{0_2}$, the DC gain appears to be: $G_{DC} = \frac{G_{m_1} G_{m_2}}{G_{0_1} G_L}$

Now, since a large value can still be obtained with $\frac{G_{m_1}}{G_{0_1}}$, obviously the two stage configuration is a better alternative than the single stage for the case where a resistive load is applied.

However, due to the presence of two poles and one zero, stability cannot be always guaranteed as was the case for the single stage operational amplifier. In fact, the location of the poles and zeros must be rigurously studied before trying to implement such system. System stability is dependent on the presence of a feedback loop around the operational amplifier. The key to achieving system stability is to design a system such that the behaviour of the loop gain until the unity gain frequency, and the behaviour around it, resembles that of a single stage system. The following considerations have to be taken into account regarding the stability analysis of the system under study:

1. Negative poles introduce a phase lag of -90º each and the positive zero introduces a phase lag of -90º, hence the total phase lag at frequencies high enough will eventually be -270º
2. The phase margin, that is, the distance between the phase at unity gain frequency and -180º, has to be greater than -180º and sufficiently large.

In fact, traditionally the analysis begins with establishing a phase margin, and from there determine the values for the poles and zero. Considering the simplified transfer function to be:

Equation 2.1-17: Transfer function of a two stage Miller compensated operational amplifier

$$\frac{V_{out}}{V_d} = \frac{A_0 \left(1 - \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}$$

where A_0 represents the DC gain and z_i and p_i the zeros and the poles, respectively, then the phase response at unity gain frequency will be:

Equation 2.1-18: Phase response at unity gain frequency of a two stage Miller compensated operational amplifier

$$\measuredangle \frac{V_{out}}{V_d}(jw_u) = -\tan^{-1}\frac{w_u}{z_1} - \tan^{-1}\frac{w_u}{p_1} - \tan^{-1}\frac{w_u}{p_2}$$

and the phase margin becomes:

Equation 2.1-19: Phase margin of a two stage Miller compensated operational amplifier

$$\varphi_m = -\tan^{-1}\frac{w_u}{z_1} - \tan^{-1}\frac{w_u}{p_1} - \tan^{-1}\frac{w_u}{p_2} + 180$$

Now, since the expression for the zero has been previously identified to be $z = \frac{G_{m_2}}{C}$ it is needed to identify an expression for w_u so that the phase margin condition can be fulfilled by simply estimating the values of the poles. In this sense, the unity gain frequency results to be approximately the same as for the single stage realization $w_u = \frac{G_{m_1}}{C}$. So the problem now reduces to estimating the values of the poles in order to fulfill a certain phase margin condition, and from those values, the ones of the capacitors.
Finally, the complex expression derived for the poles can be simplified on the basis of several assumptions. First, $G_{0_2} \gg G_{0_1}$, and second $C \gg C_1$:

Table 2.1-4: Comparison of the values of the poles originally and after the assumptions

	Original values	$G_{0_2} \gg G_{0_1}$ assumption	$C \gg C_1$ assumption
p_1	$\frac{-G_{0_1}}{C\left(\frac{G_{m_2}}{G_{0_2}} + 1 + \frac{G_{0_1}}{G_{0_2}}\right) + \frac{C_L G_{0_1}}{G_{0_2}} + C_1}$	$\frac{-G_{0_1}}{C\left(\frac{G_{m_2}}{G_{0_2}} + 1\right) + C_1}$	
p_2	$\frac{-\left(\frac{CG_{m_2}}{C + C_1} + \frac{G_{0_1}(C + C_L)}{C + C_1} + G_{0_2}\right)}{\frac{C_1 C}{C + C_1} + C_L}$	$\frac{-\left(\frac{CG_{m_2}}{C + C_1} + G_{0_2}\right)}{\frac{C_1 C}{C + C_1} + C_L}$	$\frac{-(G_{m_2} + G_{0_2})}{C_1 + C_L}$

The fact that C is given a value much greater than C_1 translates into approximating C like a short circuit. With these simpler expression for the poles, it becomes easier to give values to the capacitors on the basis of the values obtained for the poles. Note that the simplified expression for the first pole gives a clear insight of the Miller effect, the term that accompanies the capacitor C is the factor by which the capacitor's value appears to increase when using this configuration.
Another consideration that must be taken into account is the fact that it is desired that the second pole be much greater than the unity gain frequency such that the integrator function is maintained until such frequency. [3][4][15][16][17][18][19][20]

2.1.3 Two Stage Operational Amplifier with Right Half Plane Zero Cancellation

The previous implementation presents problems due to the presence of a right half plane zero, which causes an unwanted phase lag which must be dealt with if the purpose of integration is to be achieved. This can be achieved by "eliminating" the right half plane zero, which can be done by subtracting the value of the zero from the numerator of the transfer function. For simplicity assume the model and the transfer function to be:

Equation 2.1-20:Transfer function of the circuit

$$V_{out} = G_{m_1} V_d \left(\frac{1}{sC} - \frac{1}{G_{m_2}}\right)$$

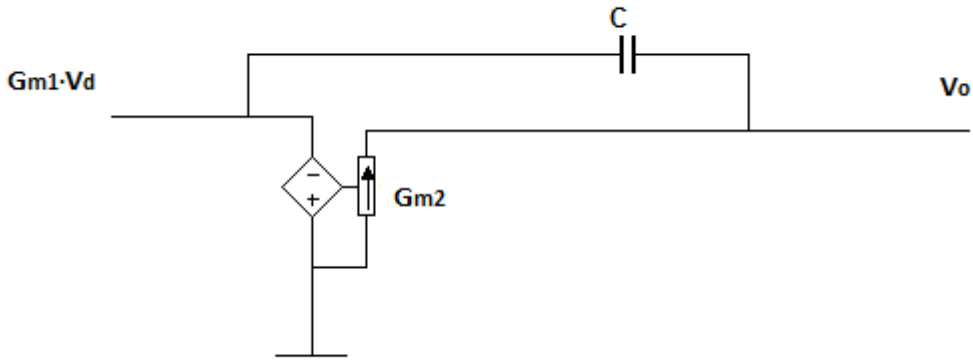


Figure 2.1-10:Circuit under study

In order to maintain the integrating function while eliminating the zero at the same time, it is needed to add a voltage to the output of the system whose value is:

Equation 2.1-21Extra voltage needed to eliminate the zero

$$V_2 = \frac{G_{m_1} V_d}{G_{m_2}}$$

The simplest way to achieve this is to introduce a resistor in series with the negative feedback capacitor:

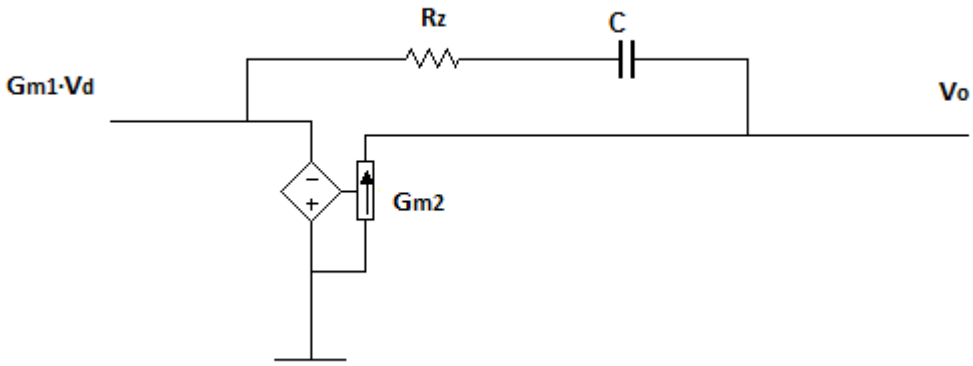


Figure 2.1-11 : Circuit configuration to eliminate the zero

Choosing the resistor to have a value of:

Equation 2.1-22: Value of resistor to eliminate the zero

$$R = \frac{1}{G_{m_2}}$$

The output voltage of the system becomes:

Equation 2.1-23: Output voltage with effective zero elimination

$$V_{out} = \frac{G_{m_1} V_d}{sC}$$

and the zero has been eliminated. For the general case where the value of the added resistor is equal to R_z the ouput voltage of the system, and the zero will be equal to:

Equation 2.1-24: Value of the zero in the presence of a resistor

$$V_{out} = G_{m_1} V_d \left(\frac{1}{sC} - \frac{1}{G_{m_2}} + R_z \right)$$

$$z_1 = \frac{-G_{m_2}}{(G_{m_2} R_z - 1)C}$$

Note that the zero could now be located in the left half plane, which is also advantageous compared to the two stage Miller compensated case. This is because it contributes with a phase lead instead of a phase lag and favours stability conditions of the system. Analyzing the overall system derived in the previous case, the following results:

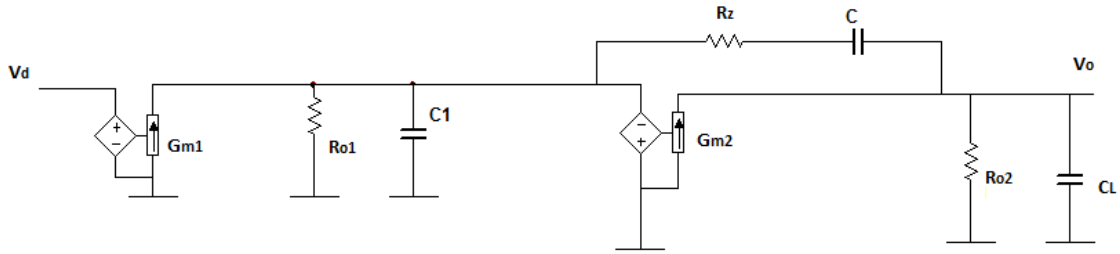


Figure 2.1-12: Two stage Miller with right half plane zero cancellation circuit

The transfer function will be derived once again by matrix analysis by equating the input current to the product of the admittance matrix times the voltage vector at each node.

Equation 2.1-25 Transfer function of two stage Miller with right half plane zero cancellation

$$\begin{bmatrix} sC_1 + \frac{sC}{1+sCR_z} + G_{0_1} & -\frac{sC}{1+sCR_z} \\ G_{m_2} - \frac{sC}{1+sCR_z} & sC_L + \frac{sC}{1+sCR_z} + G_{0_2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_{out} \end{bmatrix} = \begin{bmatrix} -G_{m_1} V_d \\ 0 \end{bmatrix}$$

Notice that depending on the value of Rz the zero either disappears or is located at different sites of the plane:

Table 2.1-5:Change in the value of the zero depending on the value of the resistor

$R_z = \frac{1}{G_{m_2}}$	$z_1 \to \infty$
$R_z < \frac{1}{G_{m_2}}$	z_1 located in the Right Half Plane
$R_z > \frac{1}{G_{m_2}}$	z_1 located in the Left Half Plane

It is important to bear in mind that the introduction of Rz has provoked an appearance of an extra pole. Regarding the "eliminated" zero and the "newly introduced" pole, it is observed that the new pole is located at a greater frequency than the old zero and the consequence of this is that less phase lag is obtained overall.
Overall, this system is better than the previous one in the sense that the positive zero can be elliminated, and better than the single stage operational amplifier in that the DC gain can be several orders of magnitude higher. [3][4][21]

2.1.4 Nested Miller Three Stage Operational Amplifier

Recalling the starting point of the two stage Miller compensated operational amplifier, where an ideal operational amplifier was substituted by a real single stage operational amplifier for the purpose of integration, the next step is to introduce in that same "ideal" operational amplifier a two stage real one and see what the behaviour of the system becomes.

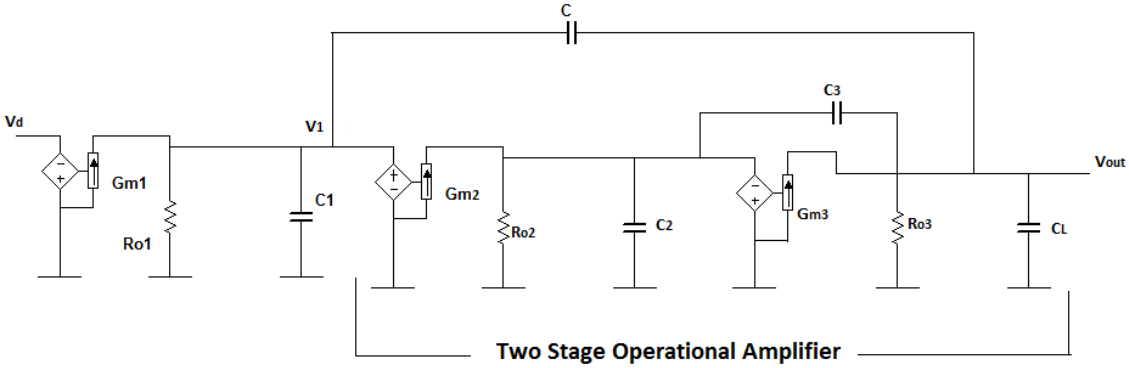


Figure 2.1-13Nested Miller three stage operational amplifier

The first reason why this three stage operational amplifier is preferred with respect to a two stage one lies is the value of the DC gain, which is obviously going to be greater:

Equation 2.1-26:DC gain of nested Miller three stage operational amplifier

$$A_0 = \frac{G_{m_1} G_{m_2} G_{m_3}}{G_{0_1} G_{0_2} G_{0_3}}$$

Recalling the unity gain frequency of the operational amplifier being realized $\left(w_u = \frac{G_{m_1}}{C}\right)$ and that of the two stage operational amplifier $\left(w_u = \frac{G_{m_2}}{C_2}\right)$, and defining the unity gain frequency of the last stage operational amplifier to be $\left(w_u = \frac{G_{m_3}}{C_L}\right)$ A necessary condition in order for the overall system to behave like an integrator is:

Equation 2.1-27: Condition for nested Miller three stage operational amplifier to integrate

$$\frac{G_{m_3}}{C_L} > \frac{G_{m_2}}{C_2} > \frac{G_{m_1}}{C}$$

This condition always applies even in those cases where the cascade is composed of more systems, meaning that the operational amplifier which is located at the last (or innermost) position must have the highest unity gain frequency and the first (outermost) operational amplifier must have the lowest. This establishes a limit as to how many cascaded systems one can construct, because at some point, a limit will be reached in which the gain of the outermost operational amplifier will have to be extremely small or that of the innermost extremely large. In practice, the largest attainable relation of Gm/C is given to the innermost stage but this means that in the case where there are many stages the outermost will eventually have an impractical DC gain due to the small value of Gm. This is the reason why systems can be built with as many stages as desired but it is uncommon to see more than five systems cascaded in this configuration. Using three stages reduces somewhat the complexity as compared to five and it is a practical configuration in terms of not compromising the transconductance of the first stage. [3][4][15][16][17][18][19][20]

2.1.5 Two Stage Feedforward Compensated Operational Amplifier

A different configuration of operational amplifiers can be constructed such that the voltage difference (V_d) at the input of the amplifier is integrated to reduce the steady state error of the system. Such system has the following configuration:

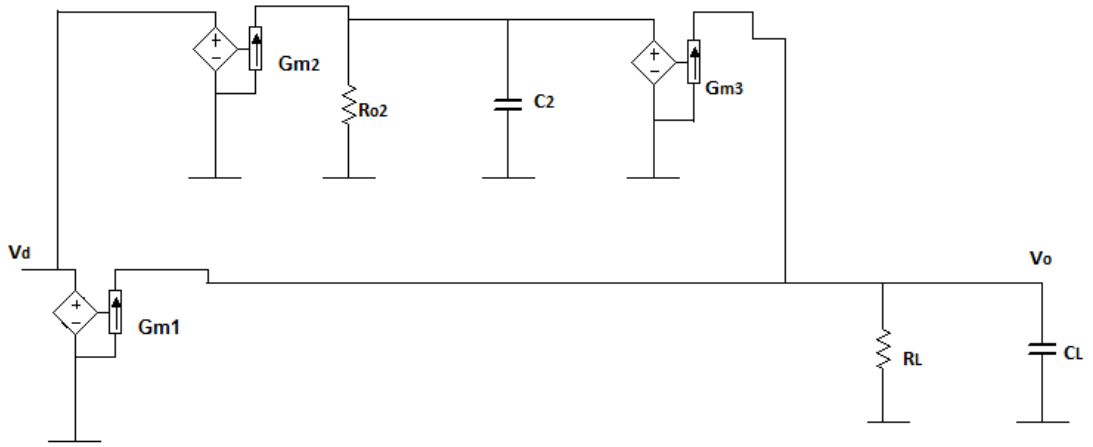


Figure 2.1-14: Two stage feedforward compensated operational amplifier

Where G_l and C_l represent the equivalent conductances and capacitances of placing G_{03} in parallel with G_{01} and C_3 in parallel with C_1. As expected, the DC gain of the resulting configuration will be:

Equation 2.1-28: DC gain of two stage feedforward compensated operational amplifier

$$A_0 = \left(\frac{G_{m_1}}{G_L} + \frac{G_{m_2}G_{m_3}}{G_{0_2}G_L}\right)$$

As it can be observed, it has a similar form to the Miller compensated DC gain, with the difference that there is one part of the circuit in charge of providing the highest amount of DC gain as possible (G_{m2} and G_{m3}) and another part in charge of the integrating function (G_{m1}). The presence of more capacitors and the different configuration among them gives an insight of the fact that there probably will be more poles and zeros, whose values will be different to those calculated previously.
This type of configuration is known as feedforward compensated operational amplifier, because the input signal (instead of the output) is being flown through a cascade of systems and fed into a distinct part of the circuit which is located downstream of the system.
The transfer function of the system will be:

Equation 2.1-29: Transfer function of two stage feedforward compensated opensated operational amplifier

$$\frac{V_{out}}{V_d} = \left(G_{m_1} + \frac{G_{m_2}G_{m_3}}{G_{0_2} + sC_2}\right)\frac{1}{G_L + sC_L}$$

Where it can be clearly observed the difference between the terms corresponding to the integrating part and the terms contributing to the increase in DC gain. The location of the poles and zeros are:

Equation 2.1-30: Value of the poles and zero for two stage feedforward compensated operational amplifier

$$p_1 = \frac{-G_{0_2}}{C_2}$$

$$p_2 = \frac{-G_L}{C_L}$$

$$z_1 = \frac{-G_{m_2}G_{m_3}}{G_{m_1}C_2} - \frac{G_{0_2}}{C_2}$$

This leads into a simplified form of the transfer function taking into account the expressions for the poles and zero, as well as the expression for the DC gain:

Equation 2.1-31: Simplified expression for two stage feedforward compensated operational amplifier transfer function

$$\frac{V_{out}}{V_d} = A_0 \frac{\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$

Regarding the stability of the system under study, due to the presence of two poles which contribute to the phase of the system with a phase lag of -90º degrees each, and a zero which contributes with a lead of +90º; the stability of the system will be guaranteed as long as the zero and the poles appear sufficiently before the unity gain frequency. This way, the behaviour of the system at unity gain frequency will resemble that of a first order system, and the phase margin will be sufficiently separated from -180º. Otherwise, if the zero is located at a close proximity to the unity gain frequency, or if the zero is at a higher frequency than the unity gain one, the phase response of the system at 0dB will be very close or even at -180º, representing an unstable system. Considering a system which has a greater number of poles, the stability criterion becomes:

Equation 2.1-32: Condition for stability

$$p_i - z_i = 1$$

In other words, before the unity gain frequency, the number of poles minus the number of zeros must be one in order for the system to behave as a first order system and hence, to be stable. [3][4][22][23][24][25][26][27]

2.1.6 Three Stage Feedforward Compensated Operational Amplifier

A way to improve the current system is to use the same idea recursively. That is, it is desired to integrate the error between the input terminals of an operational amplifier, and to "feed" the output into the resistor coming from the initial operational amplifier. This new approach substitutes the whole integrating functionality of the system for the two stage feedforward compensated operational amplifier just derived, giving rise to a three stage feedforward compensated operational amplifier which obviously will provide a higher DC gain:

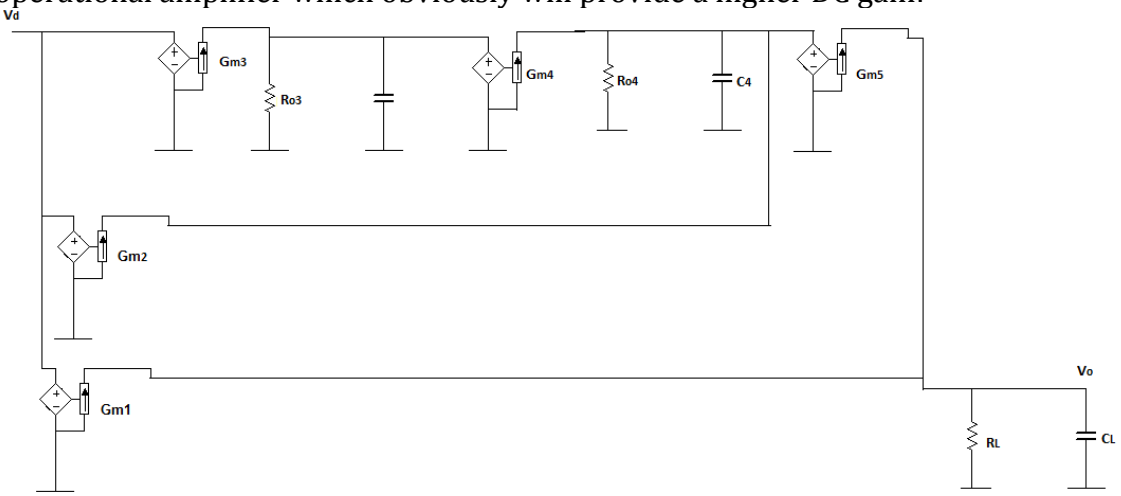


Figure 2.1-15Three stage feedforward compensated operational amplifier

The transfer function of such circuit will be:

Equation 2.1-33:Transfer function of three stage feedforward compensated operational amplifier

$$\frac{V_{out}}{V_d} = \frac{G_{m_1}}{G_L + sC_L} + \frac{G_{m_2}G_{m_5}}{(G_{0_4} + sC_4)(G_L + sC_L)} + \frac{G_{m_3}G_{m_4}G_{m_5}}{(G_{0_3} + sC_3)(G_{0_4} + sC_4)(G_L + sC_L)}$$

Identifying the DC gain as:

Equation 2.1-34: DC gain of three stage feedforward compensated operational amplifier

$$A_0 = \frac{G_{m_1}}{G_L} + \frac{G_{m_2}G_{m_5}}{G_{0_4}G_L} + \frac{G_{m_3}G_{m_4}G_{m_5}}{G_{0_3}G_{0_4}G_L}$$

Where it is easily identifiable which parts of the circuit contribute the most to the increase in DC gain. The location of the poles is derived straightforwardly:

Equation 2.1-35: Values of the poles for three stage feedforward compensated operational amplifier

$$p_1 = \frac{-G_L}{C_L}$$
$$p_2 = \frac{-G_{0_3}}{C_3}$$
$$p_3 = \frac{-G_{0_4}}{C_4}$$

Whereas the location of the zeroes comes from solving the equation:

Equation 2.1-36: Quadratic equation to find the values of the zeroes

$$z_{12} = \frac{-(b) \pm \sqrt{(b)^2 - 4ac}}{2a}$$

where:

Equation 2.1-37: Values of the coefficients of the quadratic equation

$$a = G_{m_1}C_3C_4$$

$$b = G_{m_1}G_{0_3}C_4 + G_{m_1}G_{0_4}C_3 + G_{m_2}G_{m_5}C_3$$

$$c = G_{m_1}G_{0_3}G_{0_4} + G_{m_3}G_{m_4}G_{m_5} + G_{m_2}G_{m_5}G_{0_3}$$

Assuming the values of the zeroes to be known, the transfer function can be simplified to:

Equation 2.1-38: Simplified expression of the transfer function of a three stage feedforward compensated operational amplifier

$$\frac{V_{out}}{V_d} = A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)}$$

Now, regarding the stability of the system, a necessary condition which has been previously stated is that the number of poles minus the number of zeros must be one at the point of the unity gain frequency. That way, the system will behave as a first order system, that is, as if it had a single pole, and it will be stable and the phase margin will be around 90º.
This system is superior to the two stage feedforward compensated operational amplifier in terms of the value that can be achieved for the DC gain, and superior to Miller operational amplifiers in the sense that one part of the circuit is in charge of integrating the signal, whereas another provides the gain at zero frequency. Another advantage with respect to Miller compensated configuration is the presence of negative zeros as opposed to the positive zeros present in Miller configuration.
All the systems that have been presented show different advantages and drawbacks, the choice of which one to implement depends on the characteristics of the response that is desired to come out of a system [3][4][22][23][24][25][26][27]

2.2 Operational Amplifier Design

The first objective of this work consists on the design of an operational amplifier behaving like an integrator, whose transfer function was determined prior to the design of the actual model.
In order to choose among the different options provided above, several considerations were taken into account regarding the transfer function which had to be obtained:

1. The gain of the operational amplifier at low frequencies had to have a value of 54dB
2. The unity gain frequency, and hence the Gain x Bandwidth product had to be 4.45GHz
3. The system decreased from 54dB to 0dB in approximately two decades.
4. The system could not reach a phase lower than -180º, it had to be stable.
5. The system had to have a phase margin of 94º, which means that its phase response at unity gain frequency had to be approximately equal to -86º.

Consequently, the pre-defined Bode to be imitated, had its poles and zeros located at certain frequencies whose values are:

Table 2.2-1: Poles and Zeros for the Bode plot

P_1	126. 42MHz
P_2	317.56MHz
P_3	317.56MHz
Z_1	894.99MHz

Z_2	894.99MHz

The system chosen to model such behavior was the three stage feedforward compensated operational ampifier, which can be justified with the following arguments:

1. The DC gain of a three stage feedforward compensated operational amplifier is the following:

Equation 2.2-1DC gain for a three stage feedforward operational amplifier

$$A_0 = \frac{G_{m_1}}{G_L} + \frac{G_{m_2}G_{m_5}}{G_{0_4}G_L} + \frac{G_{m_3}G_{m_4}G_{m_5}}{G_{0_3}G_{0_4}G_L}$$

Since it is required to achieve 54dB, this means that:

$$A_0 = 10^{\left(\frac{54}{20}\right)} = 501.19$$

Although this represents a large value, it can perfectly be achieved through the combination of all the terms in the expression for A_0.

2. The unity gain frequency w_u=4.45GHz and hence a gain bandwidth product of this value can perfectly be achieved with such a system
3. The fact that the desired magnitude response decreased from 54dB to 0dB in two decades means that the system has to have at least two poles before the unity gain frequency. This is justified by the fact that one pole contributes to a magnitude response of -20dB/decade. So if the system only has one pole, in two decades the magnitude decreases -40dB. Hence, it is needed that the system that has to be built has at least two poles before the unity gain frequency.
4. The system could not reach a phase lower than -180º. Due to the fact that poles contribute to a phase lag of -90º and it has been determined that the system must have two poles before the unity gain frequency, it becomes necessary that the system contains at least one zero before the occurrence of -180º phase shift.
5. Having determined that the system had to be composed of at least two poles and one zero before unity gain frequency, now it must be taken into account the overall phase response of this combination. Negative zeroes, as is the case for three stage feedforward operational amplifiers, contribute to the phase response of a system with a phase lead of +90º (as long as they are located in the left half plane, which is the case for three stage feedforward systems). This translates into an overall phase response of -90º, however, it is desired a phase of -86º at unity gain frequency. Furthermore, as it can be observed in the Bode plot above, the system actually goes further up this -86º value. Therefore, two zeroes are needed instead of one.
6. Recalling the condition that has been stated already for stability, there must be one extra pole than zero before the unity gain frequency. Therefore, the system must have three poles and two zeros, all of them ocurring before the unity gain frequency.

The development of such a system was carried out in Simulink, and variables were declared using Matlab workspace. The initial system was:

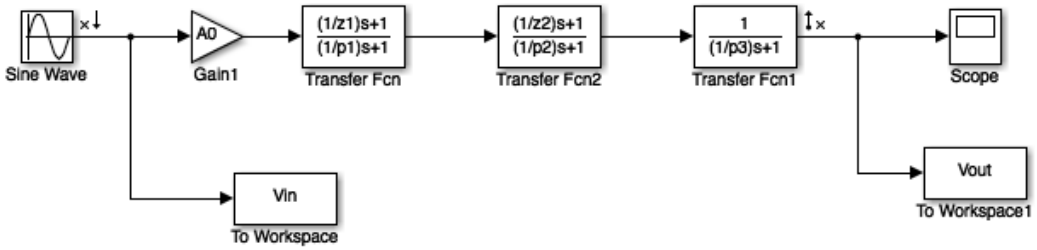


Figure 2.2-1:Simulink model of a three stage feedforward compensated operational amplifier

Several values were tried for the poles as well as for the zeros. Although theoretically a very similar Bode plot had to be obtained, the simulations showed a slightly different response to the one desired. However, since the most important considerations were the DC gain, the unity gain frequency, and making sure that the system did not present a phase response lower than -180º, the parameters which were finally chosen were:

Table 2.2-2Values for the variables of the three stage feedforward model

A_0	$10^{\frac{54}{20}} = 501.19$
P_1	$10^{8.9} = 794.33 \times 10^6$ rad/s = 126.42MHz
P_2	$10^{9.3} = 1.99 \times 10^9$rad/s = 317.56MHz
P_3	$10^{9.3} = 1.99 \times 10^9$rad/s = 317.56MHz
Z_1	$10^{9.75} = 56.23 \times 10^9$rad/s = 894.99MHz
Z_2	$10^{9.75} = 56.23 \times 10^9$rad/s = 894.99MHz
f_s	$4w_u = 1.12 \times 10^{11}$rad/s = 17.8GHz
T_s	$\frac{1}{f_s} = 8.94 \times 10^{-12}$s

Where p_i represent the poles of the transfer function and z_i the zeros. The choice for the sampling frequency comes from the fact that it is desired to observe in the Bode plot the unity gain frequency. In order to be able to observe such frequency while at the same time avoiding the aliasing problem, Nyquist theorem must be fulfilled:

Equation 2.2-2: Nyquist theorem

$$f_s \geq 2f_h$$

Where f_h represents the highest frequency component wanted to be observed. Since matlab performs the Bode plot in rad/s instead of Hertz, the choice for the sampling frequency to be entered for the sampling period was the one in rad/s.
The output of such system gave rise to the following magnitude and phase response:

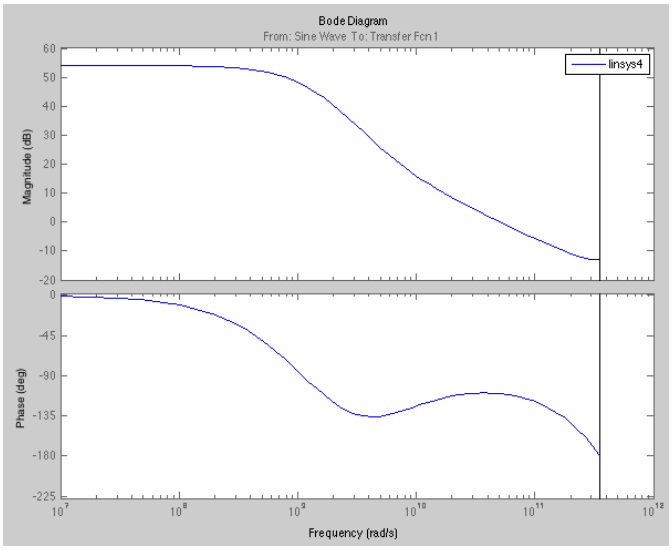


Figure 2.2-2: Bode plot of three stage feedforward model

In addition to this system, another was built in a slightly different manner, representing each stage of the transfer function of the three stage feedforward operational amplifier separately and adding them together. This was done to verify that the behaviour of this system and the previous one was exactly the same.

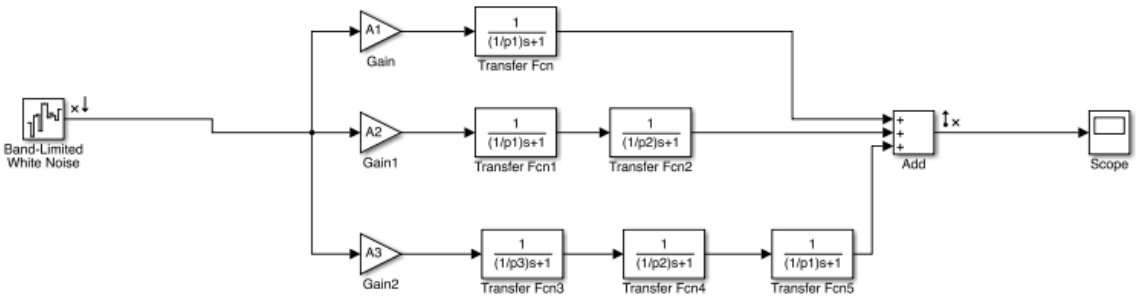


Figure 2.2-3: Simulink model 2 of three stage feedforward compensated operational amplifier

Recall the transfer function corresponding to the system under study:

Equation 2.2-3: Transfer function of three stage feedforward compensated operational amplifier

$$\frac{V_{out}}{V_d} = \frac{G_{m_1}}{G_L + sC_L} + \frac{G_{m_2}G_{m_5}}{(G_{0_4} + sC_4)(G_L + sC_L)} + \frac{G_{m_3}G_{m_4}G_{m_5}}{(G_{0_3} + sC_3)(G_{0_4} + sC_4)(G_L + sC_L)}$$

Making the analogy between the model in Simulink and this transfer function, each of the gain boxes in simulink represents the DC gains of each term which is being added in the transfer function. In this sense:

Equation 2.2-4: DC gain at each stage of model 2

$$A_1 = \frac{G_{m_1}}{G_L}$$

$$A_2 = \frac{G_{m_2} G_{m_5}}{G_{0_4} G_L}$$

$$A_3 = \frac{G_{m_3} G_{m_4} G_{m_5}}{G_{0_3} G_{0_4} G_L}$$

Therefore, each of the gain boxes in Simulink makes reference to circuit components of the system. Notice that this system is slightly different from the previous one in the sense that the poles are explicitly declared through variables in Matlab workspace, but the zeroes are not. Choosing the values of the poles to be the same as for the previous system and defining the new variables A_1, A_2 and A_3 , the results obtained coincide exactly with the previous case.

Table 2.2-3: Values of the variables for model 2

A_1	50.19
A_2	200
A_3	250
P_1	126.42MHz
P_2	317.56MHz
P_3	317.56MHz
f_s	17.8GHz
T_s	8.94×10^{-12}s

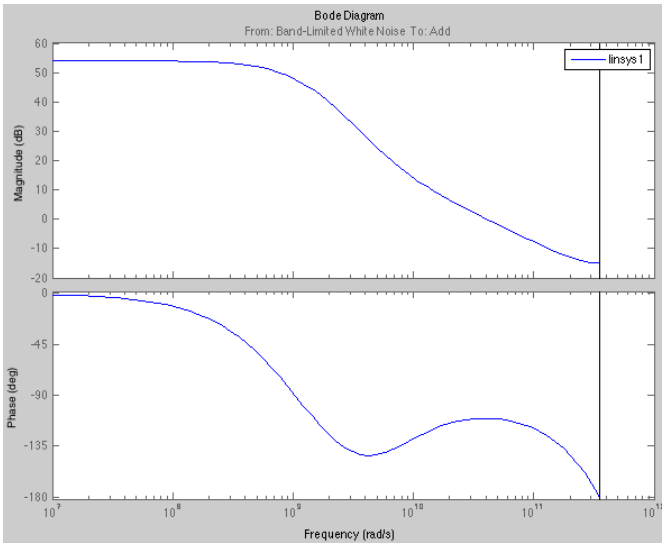


Figure 2.2-4: Bode plot of three stage feedforward model 2

A last variant of the same system was built, with the purpose of resembling the three stage feedforward circuit as much as possible.

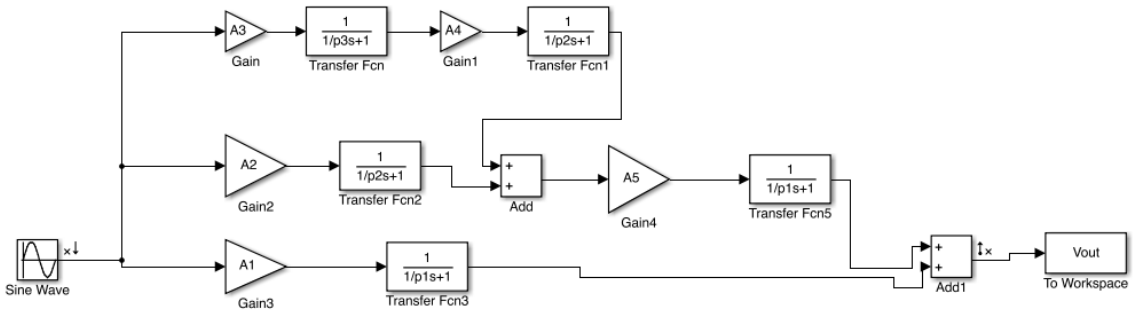


Figure 2.2-5: Simulink model 3 of three stage feedforward operational amplifier

There are a few considerations to bear in mind regarding this last version. First of all, as it can be seen:

Equation 2.2-5: DC gain of model 3

$$A_1 + A_2A_5 + A_3A_4A_5 = G_{DC}$$

which leads to:

Table 2.2-4: Values of the variables for model 3 of three stage feedforward system

A_1	50.19
A_2	10
A_3	2.5
A_4	5
A_5	20
P_1	126.42MHz
P_2	317.56MHz
P_3	317.56MHz
f_s	17.8GHz
T_s	8.94×10^{-12}s

As it can be seen, the values of the poles as well as the sampling frequency and period remain exactly the same as for the previous models so that the same Bode plot is obtained. Also, the location of each of the poles within the system was not done arbitrarily. The "innermost" system must present the highest pole, and then the system must present poles which are succesively smaller. If this rule is violated, then the integrating function will simply not work, and a completely different Bode plot will be obtained. The response of this last model was:

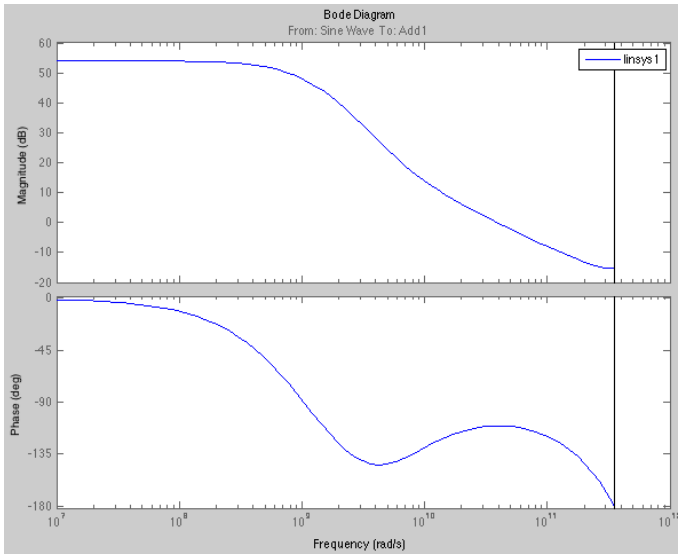


Figure 2.2-6: Bode plot of model 3 three stage feedforward system

As it can be observed by simple observation of the three Bode plots, the behaviour of the three systems is exactly the same, which was essentially what was expected, since they represent the same circuit configuration. The model chosen to work with to continue with the modelling procedure was the first one, which contains explicitly the complete transfer function with poles and zeroes. This was done because the system was simpler and smaller, although all the three systems are perfectly useful for the purpose of this work

2.3 Alternative designs

Although the model described previously works for the purpose of obtaining the initially shown Bode plot, several alternatives were also tried to confirm that the three stage feedforward compensated operational amplifier was definitively the best choice.

2.3.1 Two Stage Miller Compensated Operational Amplifier

As previously described, this configuration presents a transfer function which contains two poles and one zero, whose DC gain is:

Equation 2.3-1: DC gain of two stage Miller compensated operational amplifier

$$A_0 = \frac{G_{m_1} G_{m_2}}{G_{0_1} G_{0_2}}$$

Again, the 54dB desired DC gain can be achieved with this model, however it presents several problems, particularly regarding the presence of a positive zero, which contributes to a phase lag of -90º instead of a phase lead, and makes it impossible to obtain the desired phase response. The transfer function of this system was:

Equation 2.3-2: Transfer function of two stage Miller compensated system

$$\frac{V_{out}}{V_d} = A_0 \frac{\left(1 - \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}$$

Where the expressions corresponding to the poles and zeroes have been previously derived. The Simulink model corresponding to such system is:

Figure 2.3-1: Simulink model of two stage Miller compensated operational amplifier

The values introduced for the DC gain as well as the two poles, zero, sampling frequency and period were:

Table 2.3-1: Values of the variables for two stage Miller compensated system

A_0	501.19
P_1	126.42MHz
P_2	317.56MHz
Z_1	894.99MHz
F_s	17.8GHz
T_s	8.94×10^{-12}s

As for the output of the model, its response was:

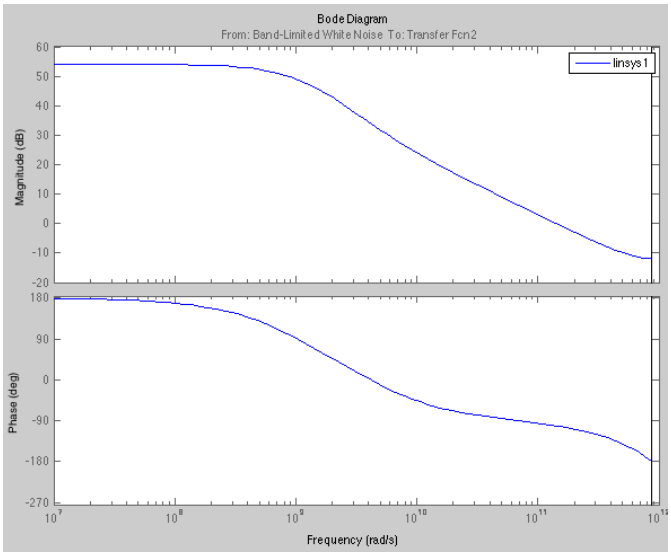


Figure 2.3-2: Bode plot of two stage Miller compensated model

This system presented problems due to the presence of a positive zero, which contributes to the response of the system with an undesired extra -90º phase lag. With this model, representing two stage Miller compensated operational amplifier, it was imposible to achieve an approximation of the phase response that was desired.

2.3.2 Two Stage Miller Compensated Operational Amplifier with Right Half Plane Zero Cancellation

The solution to dealing with the positive zero appearing in the previous model has already been discussed, it can be solved by placing a resistor in series with the feedback capacitor of the circuit the model represents. By tuning the value of such resistor, the zero can be moved to the left half plane or elliminated. For the purpose of this work, the zero plays a significant role in contributing with a phase lead of +90º, hence it is not desired to elliminate it, but to make it negative. The necessary condition to move the zero to the left half plane is:

Equation 2.3-3: Condition for left half plane zero

$$R_z > \frac{1}{G_{m_2}}$$

The model that results for this case is exactly the same as the previous one but changing the sign of the zero, and as it has been previously demonstrated, the introduction of a resistor also causes the appearance of an extra pole, giving rise to the following model:

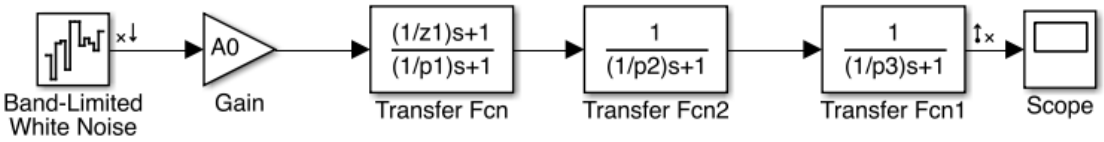


Figure 2.3-3: Simulink model for two stage Miller compensated system with right half plane zero cancellation

Regarding the circuit analog that this system represents, it has been discussed that the newly introduced pole has to be at a much greater frequency that the "shifted" zero. This has to be taken into account when fixing the values of the poles and the zero, the third pole necessarily has to have a greater value than the zero, otherwise the system will not truly be representing the equivalent circuit. The condition for stability of the system dictates that the number of poles must exceed by one the number of zeroes before the unity gain frequency. This implies that the behaviour of the system around such unity gain frequency will resemble that of a first order system. It is therefore required that the third pole be sufficiently greater than w_u (4.45GHz), this leads to an additional change regarding the value of the sampling frequency, now it will be a multiple of the highest pole since this will be the highest frequency component of the system. Hence, the chosen values for the variables of this model were:

Table 2.3-2: Values of the variables for two stage miller compensated model with right half plane zero cancellation

A_0	501.19
P_1	126.42MHz
P_2	317.56MHz
P_3	894.99GHz
Z_1	894.99MHz
f_s	$4 \times p_3 = 3579.98$GHz
T_s	4.45×10^{-14}s

And the resulting response of the model was:

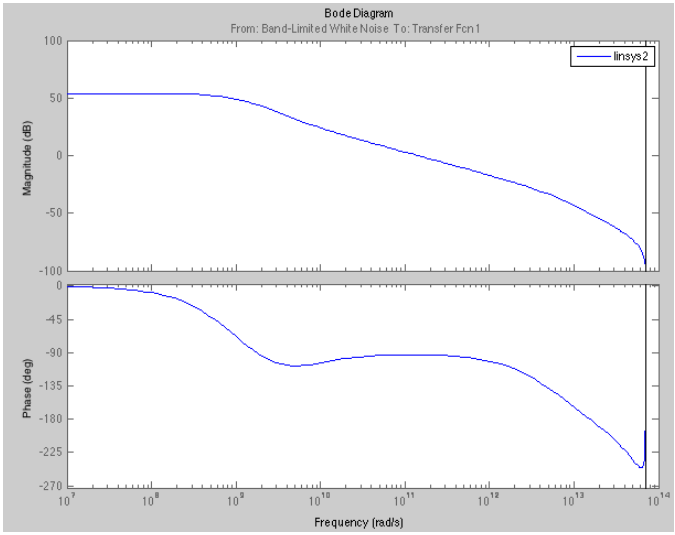


Figure 2.3-4: Bode plot of two stage Miller compensated model with right half plane zero cancellation

Despite the fact that a more accurate phase response to the one desired was obtained with this model compared to the previous one, the magnitude and phase responses are still not fulfilling the required conditions. The fact that there are three poles and only one zero causes an overall phase response of the system which eventually reaches -180º at sufficiently high frequencies, and this has to be avioded. Consequently, this model was not accepted as valid.

2.3.3 Nested Miller Three Stage Operational Amplifier

As for the case of two stage Miller compensated operational amplifier, the three stage one also contains zeroes in the right half of the plane. This is explained by the simple fact that a three stage Miller system has a two stage one inside it. It has been examined previously a way to eliminate such right half plane zeroes. Despite the possibility to elliminate (or shift) the right half plane zeroes in a nested Miller three stage operational amplifier, it has also been demonstrated that this shifting effect induced by the incorporation of a resistor also provokes the introduction of a pole into the system. Since the "two stage" model did not fulfill stability criteria or imitate the desired Bode response, the three stage system was not modelled, partly because of the additional complexity of the system and the fact that it's transfer function is not intuitive. Therefore, the possibility of moving the zeros from a third

order system was not examined, it was deduced to not be valid due to the response of the second order Miller system.

2.3.4 Two Stage Feedforward Compensated Operational Amplifier

The next system that was tried was the two stage feedforward compensated operational amplifier, which has the following transfer function:

Equation 2.3-4: Transfer function of two stage feedforward compensated operational amplifier

$$\frac{V_{out}}{V_d} = \left(G_{m_1} + \frac{G_{m_2}G_{m_3}}{G_{0_2} + sC_2}\right)\frac{1}{G_L + sC_L}$$

Identifying the DC gain as well as the poles ans zeroes:

Equation 2.3-5: DC gain of two stage feedforward compensated operational amplifier

$$A_0 = G_{m_1} + \frac{G_{m_2}G_{m_3}}{G_{0_2}G_L}$$

Equation 2.3-6: poles of the two stage feedforward compensated operational amplifier

$$p_1 = \frac{-G_{0_2}}{C_2}$$

$$p_2 = \frac{-G_L}{C_L}$$

Equation 2.3-7: Zero of the two stage feedforward compensated operational amplifier

$$z_1 = \frac{-G_{m_2}G_{m_3}}{G_{m_1}C_2} - \frac{G_{0_2}}{C_2}$$

The transfer function can be simplified to:

Equation 2.3-8: Simplified transfer function of two stage feedforward compensated operational amplifier

$$\frac{V_{out}}{V_d} = \frac{A_0\left(1 + \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}$$

and the system can be represented through the following model:

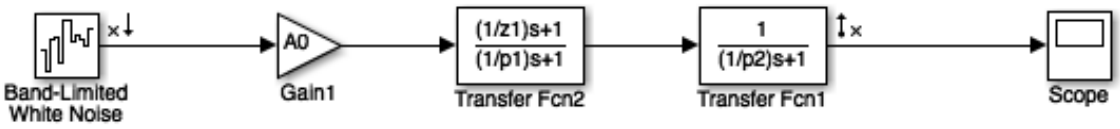


Figure 2.3-5: Simulink model of two stage feedforward system

The following values of the variables were chosen to model the output of such system:

Table 2.3-3: Values of the variables for the two stage feedforward model

A_0	501.19
P_1	126.42MHz
P_2	317.56MHz
Z_1	894.99MHz
f_s	17.8GHz
T_s	8.94×10^{-12}s

The magnitude and phase response of the model resulted to be:

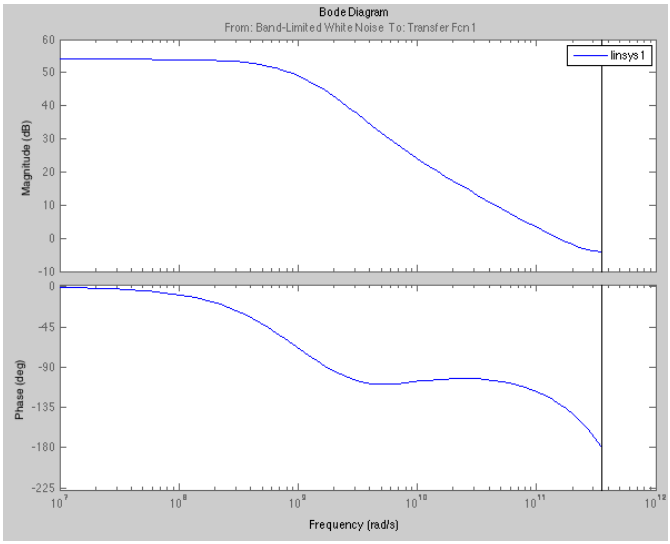


Figure 2.3-6: Bode plot of thw two stage feedforward model

Although the phase response is satisfactory, the magnitude response is not. The decay from the DC gain until the unity gain frequency should be faster, and hence the unity gain frequency should be smaller.

The responses of each of these alternative models reveal the need for the actual design of the operational amplifier to be a third order system in which all the poles and zeroes are located in the left half plane, hence contributing to the achievement of the desired magnitude and phase response. Although these alternative models could be perfectly valid for other applications, in order to obtain the initially shown Bode plot, and to fulfill the established requirements, it is necessary to build a system which represents a three stage feedforward compensated operational amplifier.

3 Operational amplifier for integration

3.1 Design of the model

The purpose of creating an operational amplifier that behaves like a real system instead of an ideal one is to use it in the following configuration:

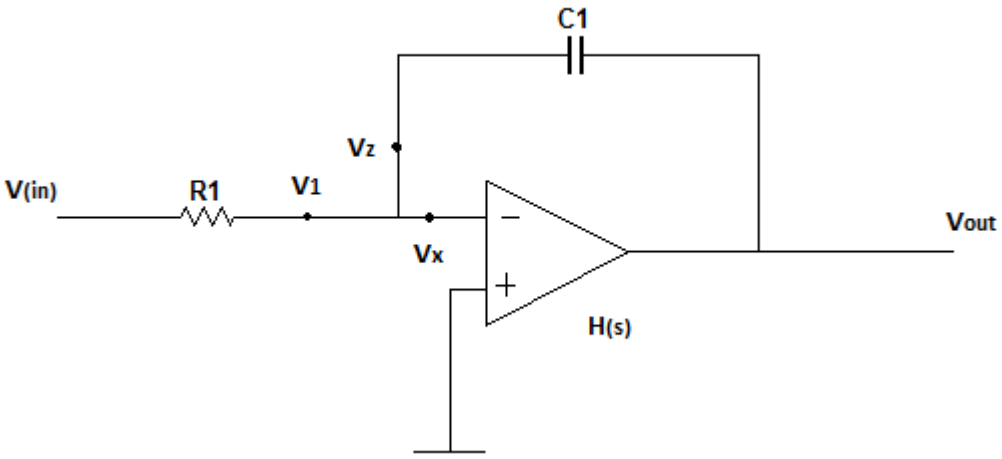


Figure 3.1-1: Ideal operational amplifier in integrating configuration

Being H(s) the operational amplifier designed, and positioning it in such configuration so that the overall system behaves like an integrator. In order to obtain a behavior of the system which is as approximate as possible to the real one, before building up the model, the following considerations must be taken into account:

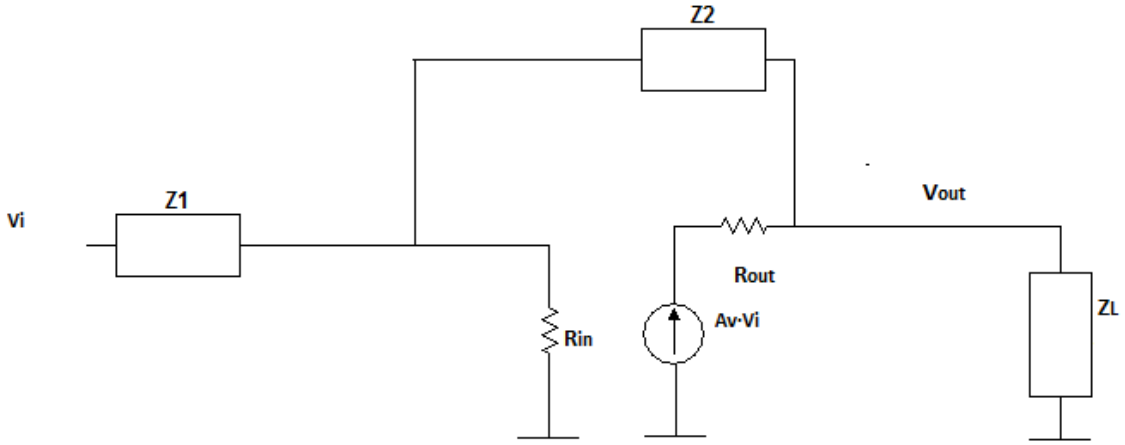


Figure 3.1-2: Small signal model of operational amplifier

1. The operational amplifier, which has been described in the schematic as Av, contains an input resistance as well as an output one. This input resistance has a value that is very large, in fact, it tends to infinity. The reason for this is so that all the voltage drops through it and eventually gets converted to current through the voltage controlled current source (the designed operational amplifier). The output resistance of the system tends to zero,

with the purpose of having a behavior similar to a short circuit, so that the output current does not get reduced when it passes through it.

2. Due to the presence of an input resistance, an extra transfer function needs to be added in Simulink which represents the parallel combination of the capacitor, the first resistance encountered by the input signal, and the input resistance from the operational amplifier. Therefore, the equivalent resistance for this node will be:

Equation 3.1-1:Equivalent impedance at operational amplifier entrance

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + sC_1 + \frac{1}{R_{in}}$$

Since the input resistance tends to infinity, the last term of the above sum vanishes, leading to the transfer function:

Equation 3.1-2: Voltage entering through the operational amplifier

$$V_2 = \left(\frac{R_1 \frac{1}{sC_1}}{R_1 + \frac{1}{sC_1}} \right) V_1$$

Being V_2 the voltage to enter through the amplifier. Therefore, the extra box to be introduced into Simulink will be:

Equation 3.1-3: Transfer function of voltage entering through the operational amplifier

$$TF = \frac{R_1}{sC_1R_1 + 1}$$

3. There is also an output resistance emerging from the operational amplifier. Such output resistance is in parallel with the feedback capacitor (as viewed from the node of the output voltage). The equivalent resistance will be:

Equation 3.1-4: Equivalent resistance at the output of the operational amplifier

$$\frac{1}{R_{eq}} = \frac{1}{R_{out}} + sC_1$$

$$\frac{1}{R_{eq}} = \frac{1 + R_{out}sC_1}{R_{out}}$$

Since this output resistance tends to zero, the transfer function resulting at the output of the operational amplifier is simply 1.

Equation 3.1-5: Transfer function at the output of the operational amplifier

$$TF = 1$$

4. Finally, the feedback capacitor presents an impedance to the output voltage which is equal to:

Equation 3.1-6: Impedance of a capacitor

$$Z_C = \frac{1}{sC_1}$$

Since impedances are entered in Simulink as "Gains" the inverse of such value should be the one entered.

Equation 3.1-7: Simulink box equivalent to capacitor impedance

$$G = sC_1$$

[28][29][30]

There was a problem encountered when trying to introduce this last expression in Simulink. It does not allow to introduce a transfer function with a numerator degree which is higher than the denominator. In order to solve this problem, taking into account that an "s" in the numerator of a transfer function in Laplace domain is equivalent to a derivative in time domain, the following model was built:

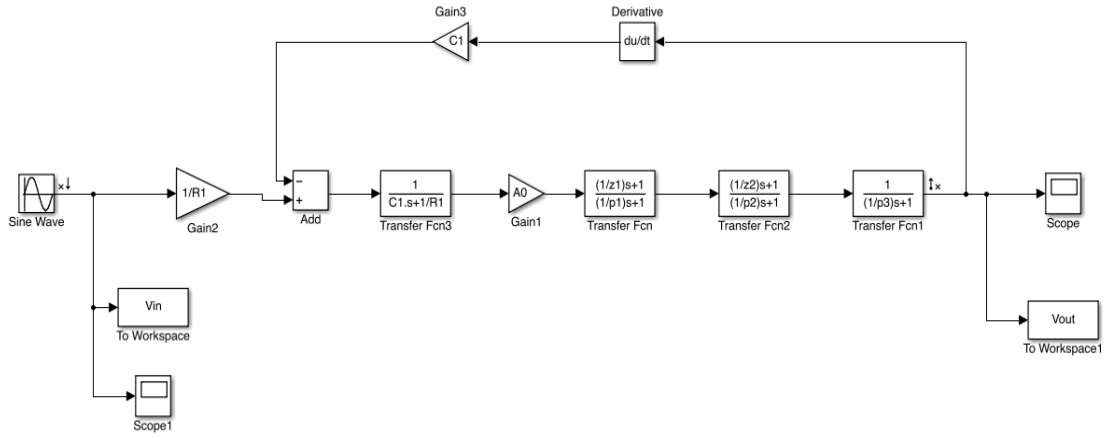


Figure 3.1-3: Simulink model of operational amplifier in integrating configuration

Regarding the model, some important considerations must be taken into account:

1. An ideal integrator is composed of an operational amplifier with a feedback capacitor, and the unity gain frequency for this circuit configuration will be:

Equation 3.1-8: Unity gain frequency of an ideal itegrator

$$f_u = \frac{1}{2\pi R_1 C_1}$$

2. The model presented is composed of a real operational amplifier, whose specific design is based upon the will to obtain a specific transfer function. This operational amplifier has a unity gain frequency of 4.45GHz. However, when the operational amplifier is placed in feedback configuration with a capacitor, the integrating functionality prevails over the operational amplifier as long as the unity gain frequency of the integrator is sufficiently smaller than the one of the operational amplifier. Hence, the unity gain frequency will also be dependent on the values of R_1 and C_1 as described in the above formula.

The fact that the unity gain frequency of the overall system has been shifted to the left due to the applied resitor and capacitor in integrating configuration, leads to the appearance of an extra pole in the overall system. Taking into account that for this model, the integrating function prevails as long as the unity gain frequency of the integrator is much smaller than that of the operational amplifier, the system experiences a -20dB/decade roll off from its cut-off frequency until the location of the first pole of the operational amplifier, where the roll-off will become -40dB/decade. The location of the cut-off frequency at which the integrating action begins is:

Equation 3.1-9: Cut off frequency of a real integrator

$$f_c = \frac{f_u}{\left(10^{\frac{54}{20}}\right)}$$

Or in other words, the cut-off frequency is 501.19 times smaller than the unity gain frequency.

3.2 Simulations

To verify such theoretical background, simulations were carried out through the use of Simulink. The values of the variables were chosen as follows:

Table 3.2-1:Values of the variables for the real integrator model

A_0	501.19
P_1	126.42MHz
P_2	317.56MHz
P_3	317.56MHz
Z_1	894.99MHz
Z_2	894.99MHz
f_s	17.8GHz
T_s	8.94×10^{-12}s
R_1	1000Ω
C_1	10^{-9}F
F_{in}	10^6rad/s
t_{sim}	10^{-4}s

A linear analysis could not be performed, as was the case for the models encountered so far. This is explained by the fact that a linear analysis requires the specification of an open loop input and open loop output. However, due to the presence of a feedback capacitor, the system can no longer be evaluated as “open loop”. The lack of linear analysis performance lead to the absence of Bode plots for this objective. Simulations were therefore performed, with a sinusoidal input signal with a frequency of F_{in}=1MHz. The choice of the resistor and capacitor were chosen so that the unity gain angular frequency coincided with that of the input signal:

Equation 3.2-1: Unity gain frequency of the system

$$w_u = \frac{1}{R_1 C_1} = \frac{1}{10^3 \times 10^{-9}} = 10^6 \text{rad/s}$$

The established values should result in an output sinusoidal signal with the same amplitude as the input signal and 90º phase shift. Being the blue signal the input and the red one the output, the simulation gave the following result:

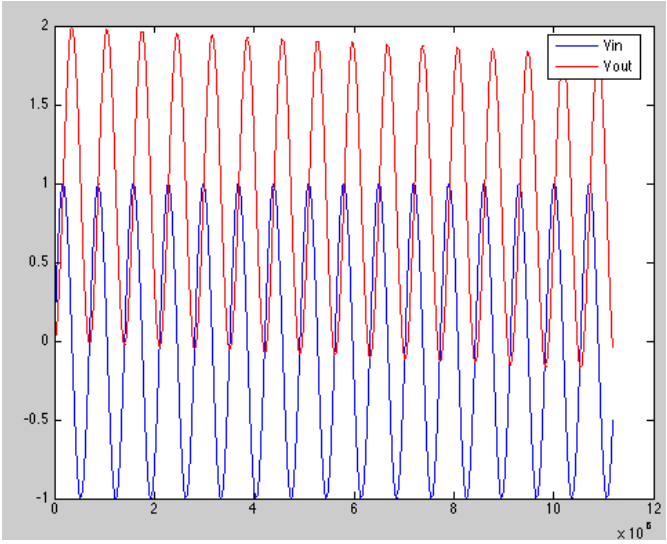


Figure 3.2-1: Simulation of the real integrator model with the specified parameters

As it can be seen, both the input and the output have the same amplitude. The fact that the output signal is initially located between [0 2] and then is shifted downwards can be explained due to the time required for the simulation to stabilize. If the simulation time (t_{sim}) is increased, then eventually both signals will be centered around 0.

In order to verify the appropriate behaviour of the system, the values of the capacitor were varied, and the input frequency signal was also changed accordingly.

1. $C_1 = 10^{-10}\text{F}$, $w_u = 10 \times 10^6 \text{rad/s}$, $F_{in} = 10 \times 10^6 \text{rad/s}$, $t_{sim} = 10^{-4}\text{s}$

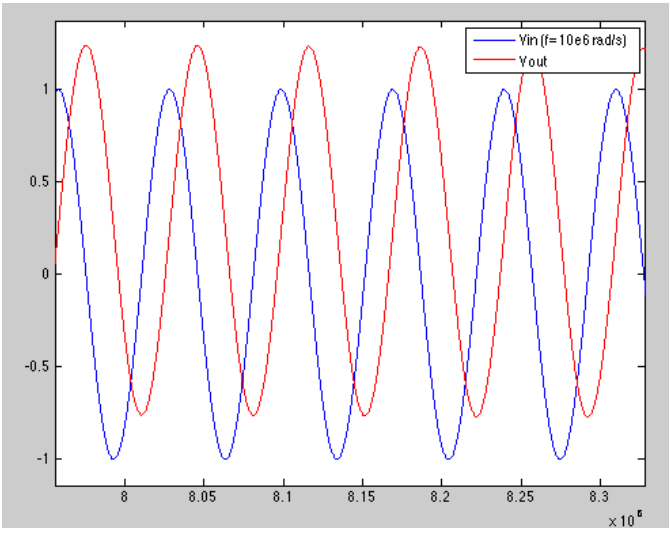


Figure 3.2-2: Simulation 2 of the real integrator

2. $C_1 = 10^{-11}\text{F}$, $w_u = 100 \times 10^6 \text{rad/s}$, $F_{in} = 100 \times 10^6 \text{rad/s}$, $t_{sim} = 10^{-5}\text{s}$

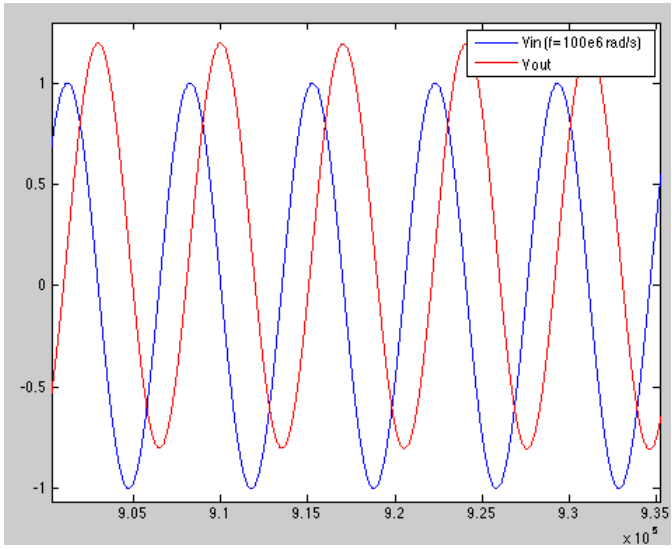


Figure 3.2-3: Simulation 3 of the real integrator

3. $C_1 = 10^{-12}\text{F}$, $w_u = 10^9 \text{rad/s}$, $F_{in} = 10^9 \text{rad/s}$, $t_{sim} = 10^{-5}\text{s}$

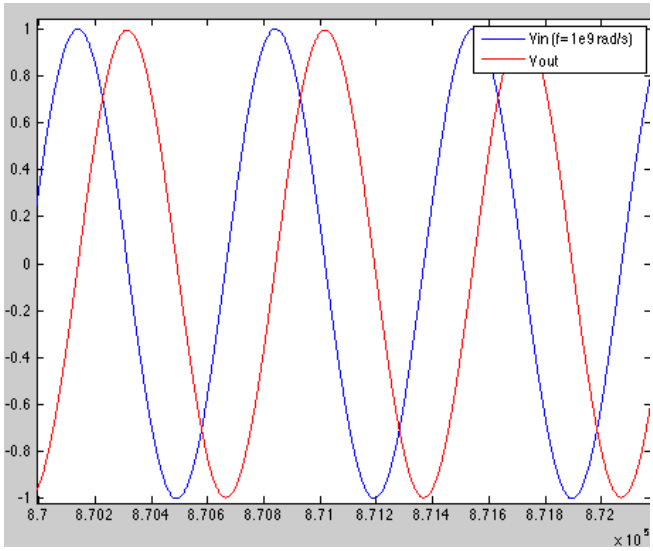


Figure 3.2-4: Simulation 4 of the real integrator

Finally, in order to confirm the theoretical background regarding the cut-off frequency of the model, which appears due to an extra pole in the overall system, a last simulation was performed. The values were maintained exactly the same as for the previous simulation, however, the input frequency to the system was changed to $F_{in} = 10^{6.3}\text{rad/s}$. It has been justified that having a unity gain frequency of $w_u = 10^9\text{rad/s}$ implies that the cutoff frequency is located $10^{\frac{54}{20}} = 10^{2.7}$ times before such frequency, which explains the choice for F_{in}. Finally, changing the simulation time to $t_{sim} = 10^{-4}\text{s}$ due to the lower input frequency to the system, the outcome of the simulation was the following:

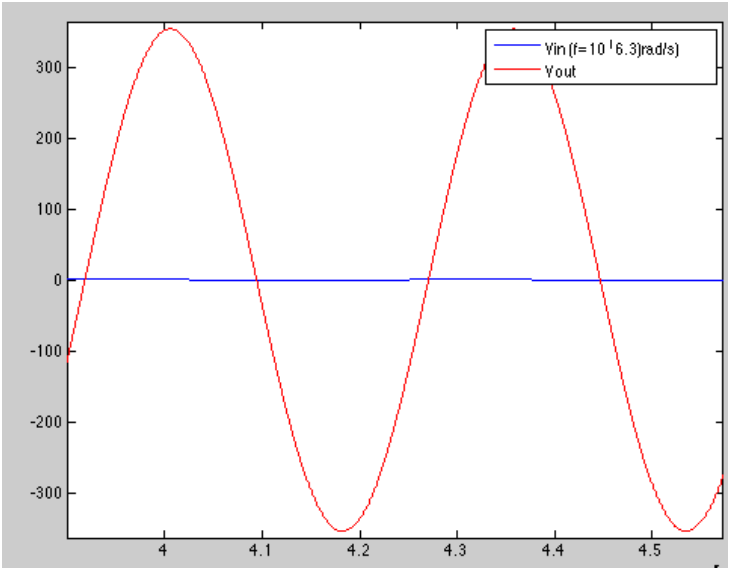


Figure 3.2-5: Simulation 5 of the real integrator

Notice that the input signal appears to be zero because of the large difference in amplitude between the input and the output (the original DC gain was 54dB). Since the definition of the cut-off frequency is also the frequency at which the gain is -3dB from the DC gain, it is therefore required that the output signal have a maximum amplitude of $V_{out} = 10^{\frac{51}{20}} = 354.81$V. In order to check the amplitude of the signal the following command was introduced in Matlab:

```
>> min(Vout)

ans =

-353.3643
```

The reason behind choosing the minimum value of Vout instead of the maximum lies in the previously discussed stabilization time required by the simulation. In this sense, the simulation output is not initially centered around 0, instead, it is focused around such point as the simulation time increases. Overall, the minimum value obtained for the amplitude of the output signal verifies that the introduced input frequency is effectively the cut-off frequency of the system.
All these evidences lead to the conclusion that the designed operational amplifier, arranged in negative feedback with a capacitor, and in the presence of an input resistor encountered by the signal prior to its entrance to the operational amplifier, work effectively as an integrating system, whose unity gain cut off frequency can be precisely tuned by changing the values of the input resistor and the capacitor.

4 Integrating the integrator in a Sigma Delta Band Pass circuit

4.1 Model design

The last objective of this work consisted on including the designed operational amplifier with integrating function into a Band Pass Sigma Delta modulator. This modulator will ultimately be the one in charge of sensing and digitizing the MRI signal. Its function is basically to allow the passage of those signals whose frequency is around 140 MHz and to convert the analog input into a digital output signal, which allows the processing of the signal which will ultimately lead to the formation of an image. Another important functionality of Sigma Delta circuits is its capability to make noise shaping. The consequence of noise shaping results in an output signal which, at a given frequency, presents a downward peak in its noise component as compared to other frequencies of the spectrum. Therefore, the output of the modulator will resemble that of a Notch (or band reject) filter, and the objective will be to place the peak of the Notch exactly at the frequency of maximum Band Pass of the Sigma Delta. This translates into effectively obtaining this noise shaping effect at the frequency of 140MHz, so that the output signal contains as low amount of noise as possible. The key factor that determines where the noise shaping effect will experience a downward peak lies in the location of the unity gain frequency of the integrator, or in other words, the values of the input resistor and feedback capacitor. Bearing this in mind, several factors are to be considered regarding the operational amplifier:

1. First, and most important of all, the operational amplifier must present an integrating function at the frequency of 140MHz , that is, it is desired that the Sigma Delta circuit effectively integrates the input signal.
2. Secondly, the outcome of the integrator must not have an amplitude bigger than 1.8 because this is the saturation limit of the Sigma Delta circuit, hence if this value is exceeded, the whole digitalization process would not be effective.
3. Thirdly, the integrator must have its unity gain frequency located at 140MHz. The reason for such pole location is explained in terms of the output from the ideal Sigma Delta modulator. This output contains the downward peak corresponding to the noise component of the signal located exactly at the unity gain frequency of the integrator. This value is determined by fixing the values of the resistor and capacitor which form the integrator.

The model of an ideal Sigma Delta second order band pass circuit is the following:

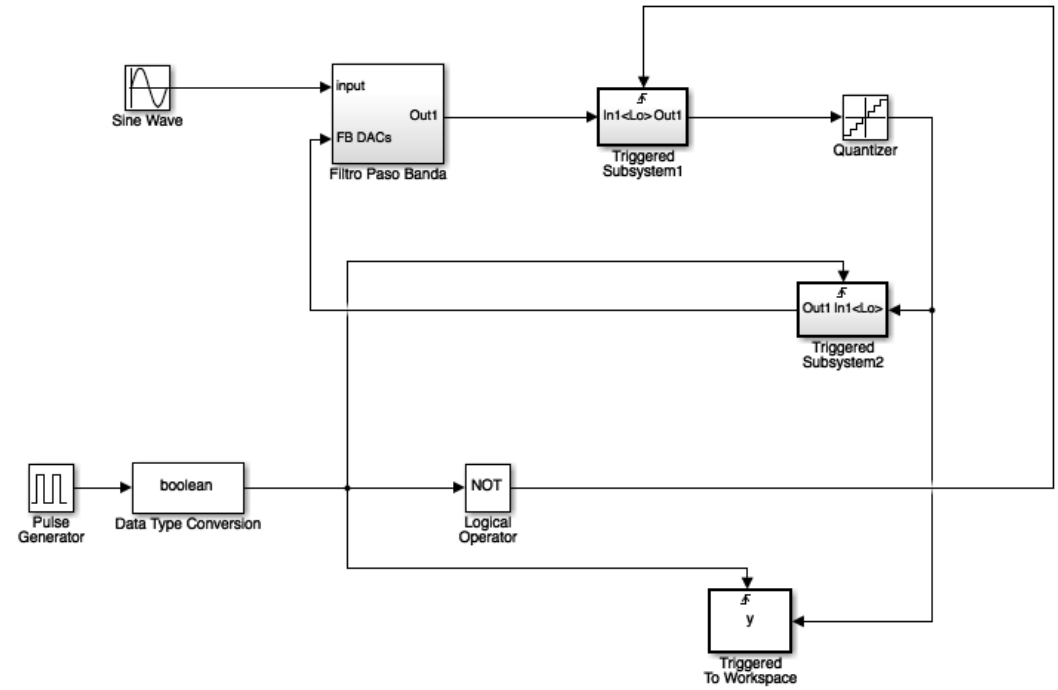


Figure 0-1: Sigma Delta second order Band Pass Simulink model

Where the part requiring integrators is the Band Pass circuit, whose model is:

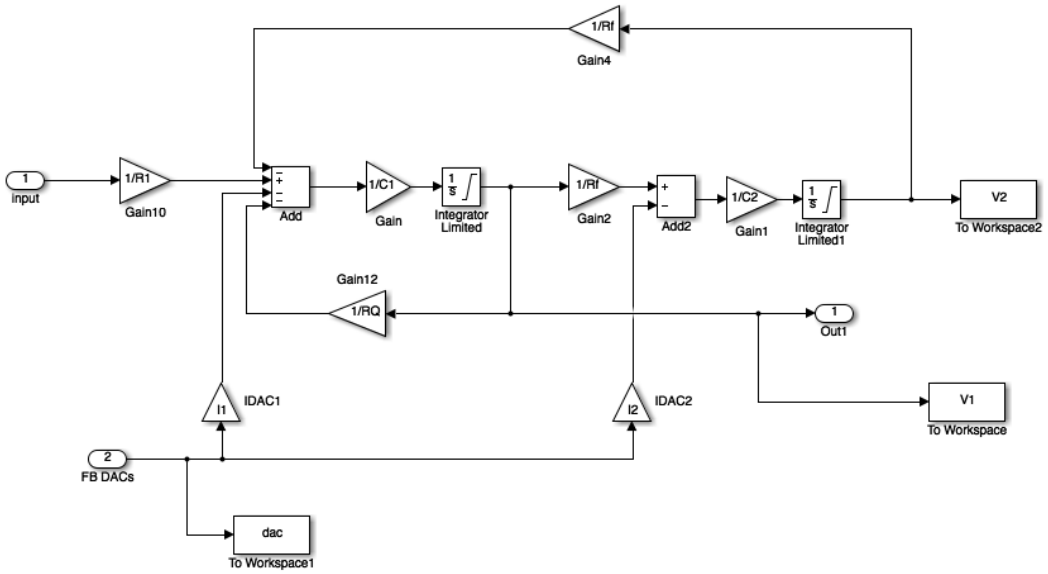


Figure 0-2: Ideal Band Pass inside Sigma Delta Simulink model

However, an ideal model gives just an estimate of the actual outcome of this circuit. The whole purpose of this project has been the design of a real integrator including an operational amplifier to be introduced into a Sigma Delta modulator. The goal is to predict a more accurate and realistic response of the system to be considered later by an analog designer of the circuit. This leads to a model in which the ideal integrator box is substituted by a subsystem which contains the model built in the second objective:

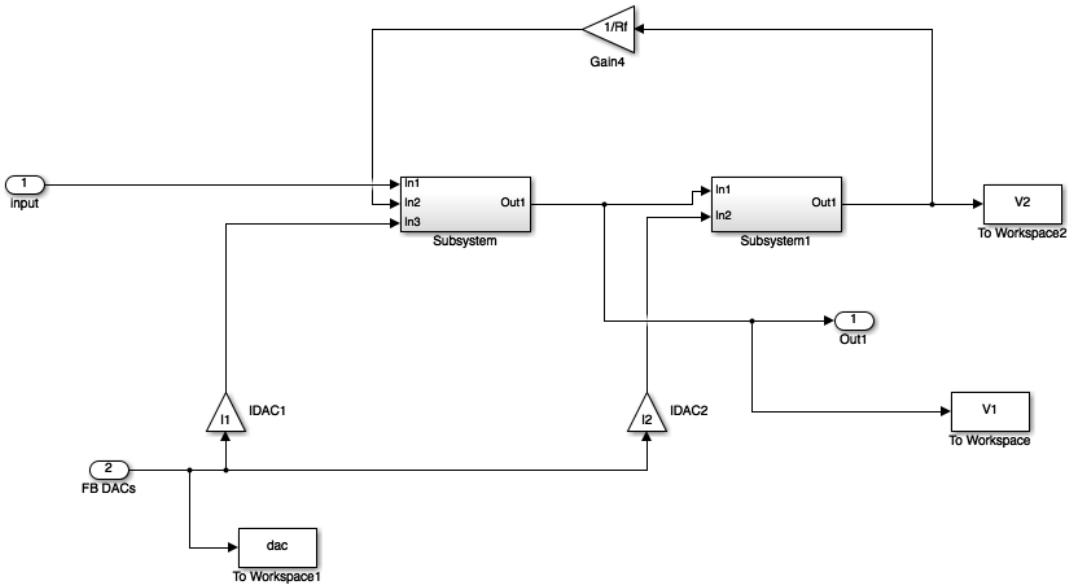


Figure 0-3: Real band pass Sigma Delta Simulink Model

The inner structure of each subsystem is slightly different. As it can be observed in the ideal model, the first integrator contains a resistor in parallel. This resistor will favor the formation of a tone in the outcome of the modulator for the frequency of interest. Hence the first subsystem has the following architecture:

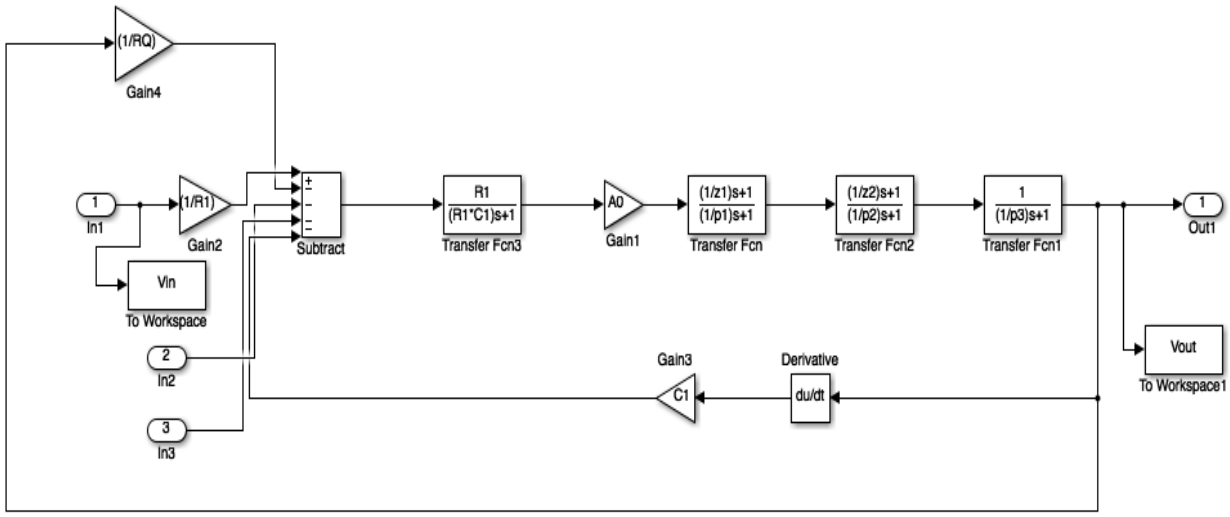


Figure 0-4: Simulink model of first real integrator belonging to Sigma Delta

As for the second subsystem being part of the band pass circuit, it will be exactly the same with the absence of Rq in parallel with the integrator:

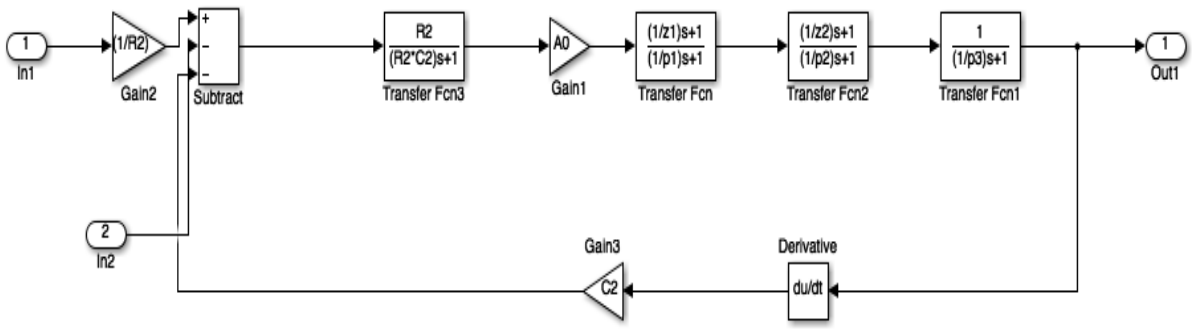


Figure 0-5: Simulink model of second real integrator belonging to Sigma Delta

4.2 Simulations

It has been previously stated that the interesting outcome of this Sigma Delta Band Pass modulator is the noise shaping effect around the frequency of interest, where it can be observed the noise reduction of the output signal. It is desired that this Notch emanating from the output of the modulator be exactly located around 140MHz so that the output signal from the modulator has the smallest amount of noise. Theoretically, this notch location is dependent on the value of the resistor and capacitors forming the integrators. Hence, in order to find the optimum noise shaping effect, several simulations were carried out. First, by fixing the two integrators with the same unity gain frequency, and then making variations among them, as will be explained. The plots that will be observed correspond to the FFT (Fast Fourier Transform) of the output signal from the modulator.

1. First of all, both integrators will have the same unity gain frequency, and the result will be analyzed. Taking into account that the notch is desired to be located at the frequency of 140MHz, and that the values of the resistors is 1000 Ω, the capacitor arranged in negative feedback configuration with the amplifier should have a value of:

Equation 4.2-1Calculation of capacitor value

$$C_1 = \frac{1}{2\pi \times 140 \times 10^6 \times 1 \times 10^3} = 1.1368 \times 10^{-12}\text{F}$$

With the previously calculated value for the capacitors, the FFT of the output signal from the modulator was the following:

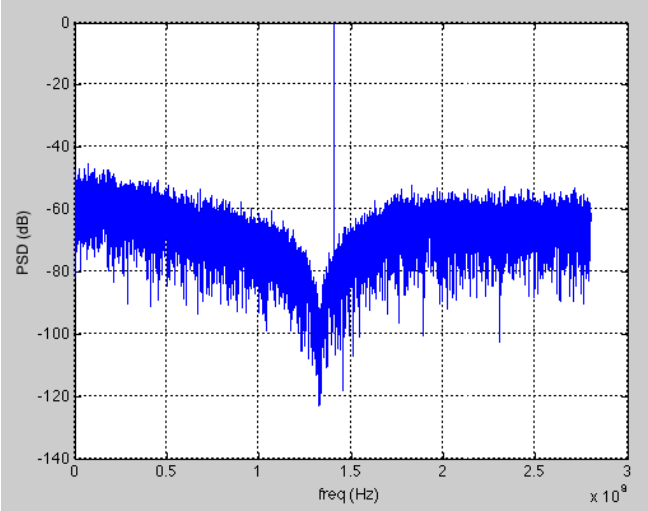


Figure 4.2-1: Simulation 1 (FFT) real model

SNR=63.8dB

This result is obviously not acceptable, since the location of the notch must coincide with the tone in order to give the maximum Signal to Noise Ratio. Hence, it will be tried to focus the notch at the frequency of 140MHz.

2. Since the system is very sensitive to slight variations of the capacitor value, by setting $C_1 = 1.07 \times 10^{-12}$F, the notch effectively becomes focused at the desired frequency.

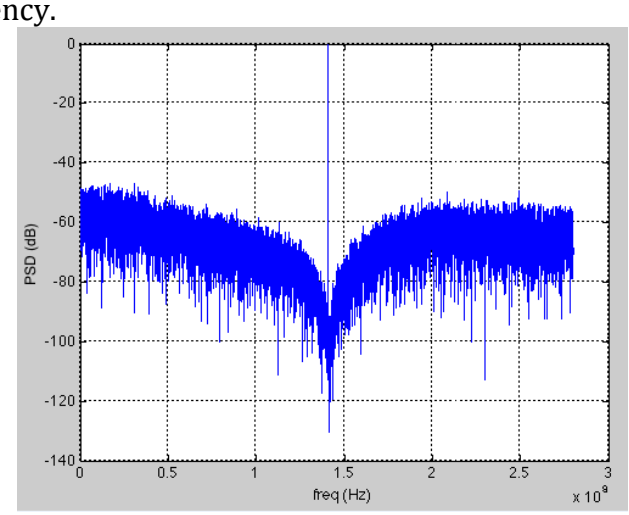


Figure 4.2-2: Simulation 2 (FFT) real model

SNR=83.2dB

Decreasing the capacitor value of the integrator results in a FFT of the output from the modulator which presents a notch that is closer to the frequency of the tone. Due to the more precise location of the notch, the Signal to Noise Ratio of the output signal effectively increases. This result is more satisfactory than the previous one, however, the capacitor should be slightly increased to be able to focus the notch exactly at 140MHz and achieve the maximum SNR.

3. Having observed that a reduction in capacitor value has the effect of moving the notch to the right, it is now desired to move the notch slightly to the left.

This implies a slight increase in capacitor value. By setting $C = 1.075 \times 10^{-12}\text{F}$, the FFT of the output from the modulator becomes:

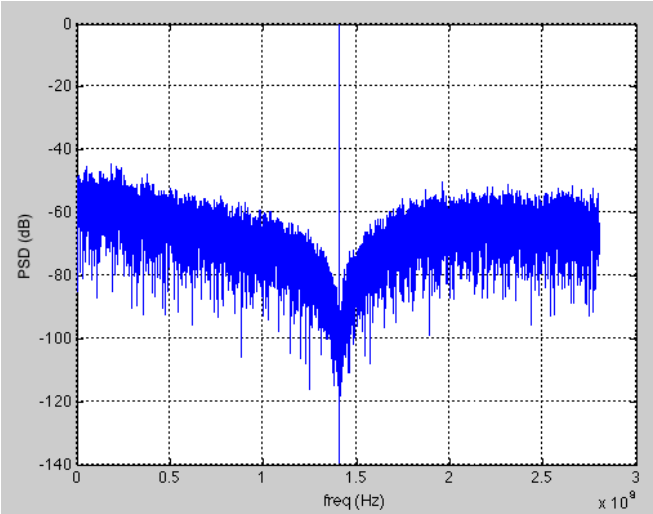


Figure 4.2-3: Simulation 3 (FFT) real model

SNR=85.3dB

As it can be observed, the notch is now placed appropriately at the frequency of interest and this implies an increase in the output's Signal to Noise Ratio.

Having established the optimum values of the capacitors in order to have the notch located at the desired frequency, now the behavior of the ideal model will be analyzed:

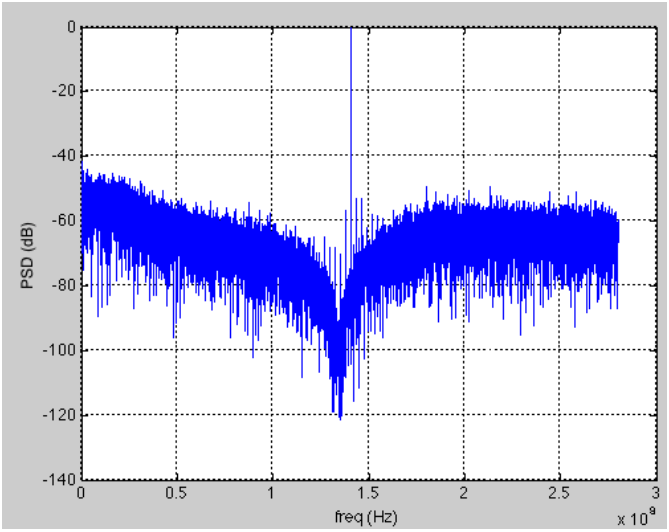


Figure 4.2-4: Simulation 4 (FFT) ideal model

SNR=64.4dB

As it can be seen, the systems do not show a similar behavior with the same capacitor values. In fact, for the specified capacitor values the ideal model has the notch located at smaller frequencies to the one desired. This is explained by the fact that the ideal model contains an integrator with

infinite bandwidth and the real one contains a finite bandwidth which influences the behavior of the complete system.

The second approach will be focused on setting different unity gain frequencies for each of the integrators and observing the subsequent effect.

1. The unity gain frequency of the first integrator will be fixed al 150MHz, and for that $C_1 = 1.0610 \times 10^{-12}$F, while the second will be fixed at 130MHz hence $C_2 = 1.2243 \times 10^{-12}$F. The FFT of the output of the modulator obtained with these values was the following:

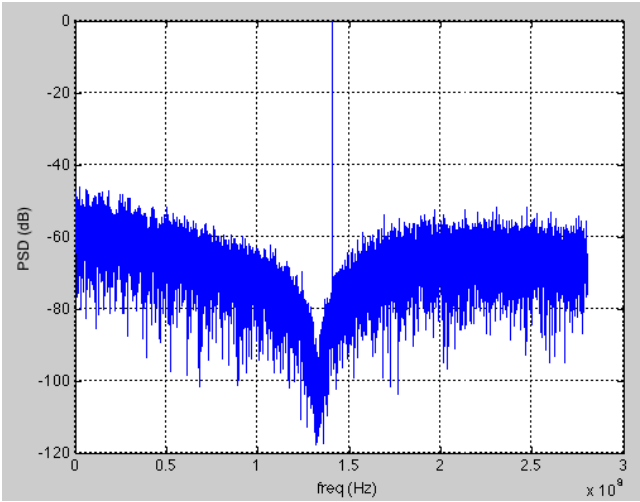


Figure 4.2-5: Simulation 5 (FFT) real model

SNR=63.9dB

The FFT of the output signal reveals that the notch is located at smaller frequencies than the desired. Hence, the capacitor values should be decreased to fix the notch at the frequency of interest. The inappropriate location of the notch becomes evident by observing the Signal to Noise Ratio of the output signal, which is 20dB lower than it should be.

2. The previous result indicates the need to shift the notch to the right (higher frequencies). Therefore, the unity gain frequencies of the integrators will be changed so that the center frequency becomes 148MHz, and the results will be examined. The choice for this center frequency lies in the fact that in the previous determination of optimum capacitor value (1.075nF) the frequency which corresponds to such value is 148MHz. Hence, the first integrator will be set with a unity gain frequency of 158MHz, meaning that $C_1 = 1.007 \times 10^{-12}$F, while the second integrator will be characterized by a unity gain frequency of 138MHz and $C_2 = 1.1533 \times 10^{-12}$F. The output of the modulator obtained with these values was the following:

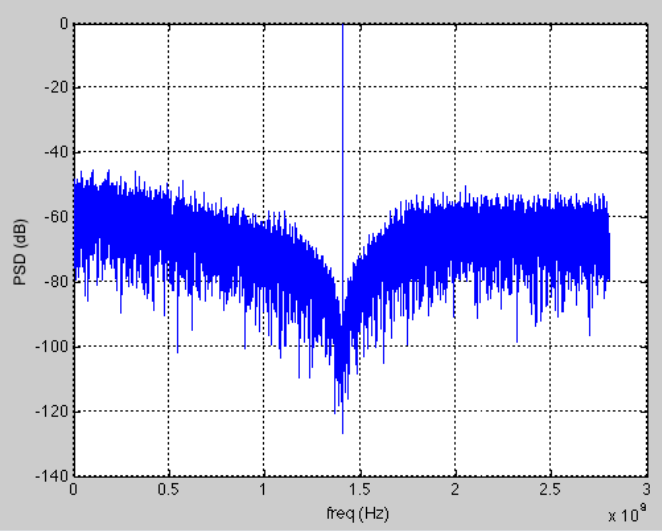


Figure 4.2-6: Simulation 6 (FFT) real model

SNR=83.2dB

The notch is now effectively located around the frequency of interest and therefore the Signal to Noise Ratio is optimum.

The next approach to center the notch at 140MHz consisted on decreasing the bandwidth between both integrators, and to observe the effect of such badwidth reduction. For the case that has just been described, the bandwidth was of 20MHz, this of course is an excessively large value. The next step therefore consists on decreasing this bandwidth.

1. First, the bandwidth was reduced to half of the previous value, 10MHz. In this sense, the first integrator was set with a unity gain frequency of 153MHz, leading to $C_1 = 1.04 \times 10^{-12}$F, and the second has a unity gain frequency of 143MHz, hence $C_2 = 1.113 \times 10^{-12}$F. The FFT ot the output from the modulator for this case was the following:

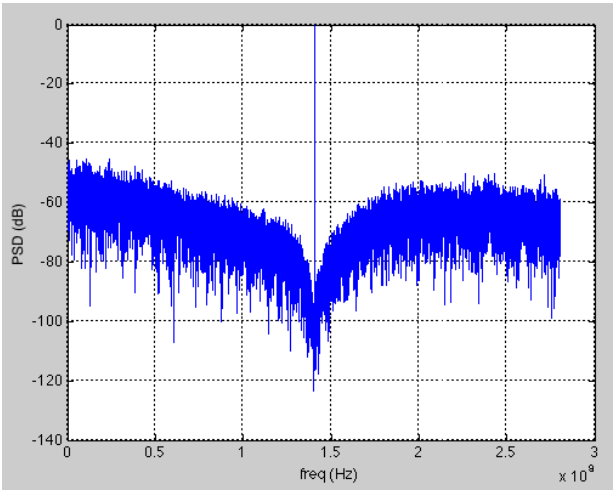


Figure 4.2-7: Simulation 7 (FFT) real model

SNR=82.4dB

2. Finally, the badwidth was set to 1MHz, which results in capacitor values of $C_1 = 1.072 \times 10^{-12}$F and $C_2 = 1.079 \times 10^{-12}$F. The FFT of the output of the modulator corresponding to these values, as well as the SNR are:

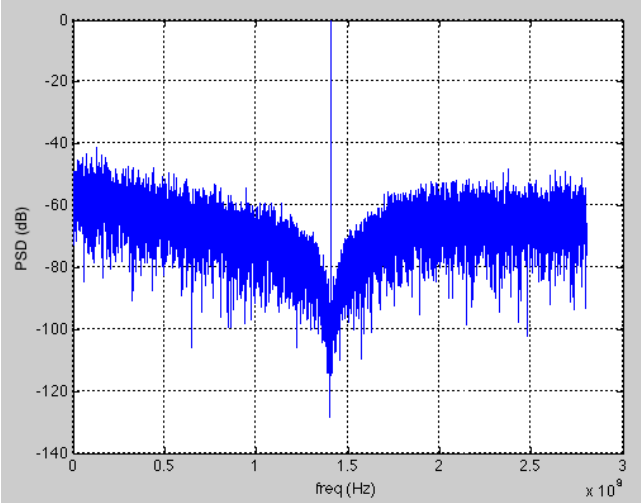


Figure 4.2-8: Simulation 8 (FFT) real model

SNR=81.8dB

To end with the simulations regarding this last objective, now another aspect will be examined. Having determined that the difference between the ideal and real Sigma Delta output lies in the fact that the bandwidth of the ideal system is infinite and the one of the real system is 4.45GHz. Taking this into account, a change in the operational amplifier cut-off frequency will result in a change in the overall output of the Sigma Delta modulator. Hence, keeping the first encountered optimum values for the capacitors, where the two are set to the same value of $C_1 = 1.075 \times 10^{-12}$F, the parameters of the operational amplifier were all decreased 50MHz so that the unity gain frequency of the operational amplifier also decreased. The poles and zeros were changed to:

Table 4.2-1: Values of poles and zeroes for an operational amplifier with reduced bandwidth

P_1	76.42MHz
P_2	267.56MHz
P_3	267.56MHz
Z_1	844.99MHz
Z_2	844.99MHz

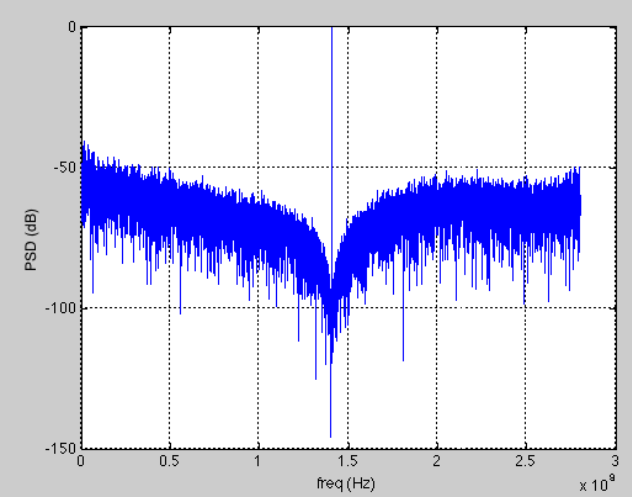


Figure 4.2-9: Simulation 9 (FFT) real model

SNR=86.1dB

Although this last result of the FFT is apparently equal to the one obtained for the previous operational amplifier which had its poles and zeroes located at 50MHz higher frequencies, in fact it is not. This simple fact emanates from the value of the Signal to Noise Ratio obtained for this case, which is different from the previous one. The interesting fact about reducing the bandwidth of the operational amplifier to be introduced into the Sigma Delta Band Pass modulator lies in power consumption. In essence, the lower the bandpass of the operational amplifier, the less power the system consumes.

From these results, it can be concluded that the ouput of the Sigma Delta band pass modulator is different in a real model than in an ideal one. This difference stems from the bandwidth of the integrators of both systems. Also, ideal models are not useful in practice because as they hay an infinite bandwidth, they would consume infite power. Therefore, real models should be substituted for ideal ones in the modeling of modulators to give a more accurate prediction to the analog designer of the circuit of the actual behavior of the system.

5 Conclusion

5.1 Concluding remarks

Operational amplifiers are usually treated as ideal systems when modelling the behaviour of circuits which contain them. However, this is just an approximation of the actual outcome of such circuit. In reality, operational amplifiers participate actively in the signal processing procedure and have an inherent transfer function. Such transfer function is the representation of the internal circuitry that builds up the operational amplifier.

With this work, it has been demonstrated that:

1. Operational amplifiers can be built taking as a reference a predetermined Bode plot, and choosing the internal circuit of the operational amplifier which will give a specific transfer function with which the established Bode plot can be achieved.
2. There are many circuit configurations which have been traditionally used for operational amplifier design. Each of them is useful for a different application, and the magnitude and phase responses of each of them differs considerably. The one chosen for the purpose of this work was the three stage feedforward compensated operational amplifier because its outcome resulted in a Bode plot which was similar enough, in terms of approximate phase and magnitude response, to the Bode plot which was to be imitated. An important concern regarding this operational amplifier was the unity gain frequency, which dictates the gain bandwidth product of the system. Although slight variations could be accepted regarding the initially given Bode plot and the Bode plot obtained after designing the system, variations of the unity gain frequency and gain bandwidth product between both plots were unacceptable.
3. The designed operational amplifier, with its specific transfer function, could be arranged into an "integration" configuration by placing a capacitor in negative feedback with the system. As well as including a resistor prior to the entrance of the input signal into the operational amplifier.
4. Regarding this integration configuration, the appropriate modelling of the system required analysis of the circuit through the "Small Signal Model", which represents a more realistic behaviour of the system, and the outcome after applying all the "real" assumptions is more precise and represents with a greater fidelity the response of a system. In the absence of such assumptions, the system did not work, hence it is a necessary condition to take into account.
5. The operational amplifier in integrating configuration effectively showed a prevailance of integrating functionality compared to the actual transfer function of the operational amplifier, as long as the integrator's unity gain frequency was sufficiently smaller from the operational amplifier's bandwidth. In fact, the overall system presented a similar response to an ideal one in this frequency range, as the unity gain frequency could be tuned by simply changing the values given to the input resistor and feedback capacitor.

6. This whole system, could be effectively introduced in a Sigma Delta Band Pass modulator. Sigma Delta is a system in charge of filtering input signals so as to allow the passage of those signals that have a very specific frequency. For the purpose of this work, the band pass region was designed to allow the passage of signals with the specific frequency of 140MHz. In addition to this filtering functionality, the system also effectively converts the analog input into a digital output. The effect of using the operational amplifier in integrating configuration in the Sigma Delta in place of the ideal integrating boxes provided by Simulink, gives a more realistic behaviour of the overall system.
7. An important property of Sigma Deltas is their noise shaping capability. This is analyzed through the FFT (Fast Fourier Transform) of the output signal of the modulator, and it translates into a downward peak at the frequency of maximum amplitude of the band pass. This notch location can be precisely tuned by changing the unity gain frequency of the integrator. Overall, this has the effect of reducing the noise component of the output signal at the frequency of interest.
8. The outcome of the Sigma Delta Band Pass modulator containing the model of the "real" integrator resuted in an output signal whose notch could be tuned by changing the values of the feedback capacitors.
9. The difference in the output of the modulator between the ideal and real models lies in the badwidth from both systems. This explains why for the same capacitor values, the systems behave in a different manner.
10. Overall, the use of representations of real systems that substitute ideal ones for the modelling of bigger systems is obviously preferred, since this gives a more realistic estimation of the behaviour of the system. Furthermore, the ideal systems corresponding to integrators can not be built in practice since their bandwidth is infinite and this implies an infitine power consumption from the system.

5.2 Future work

The future works regarding the designed real operational amplifier are:

1. To validate the designed model of the operational amplifier from an electric and physical point.
2. To design the operational amplifier at transistor level.

Whereas for the Sigma Delta Band Pass modulator with the real operational amplifier in substitution of the ideal integrator, the future works include:

1. To integrate the operational amplifier at transistor level within the Sigma Delta Band Pass modulator.
2. Perform the physical design (layout) of the complete system to validate the results at a systematic level.

5.3 Social and economic background

The work presented here has been developed at the Electronics Technology Department. The Electronics Technology Department is in charge of teaching electronics related courses for engineering bachelors and postgraduate Masters adapted to Bologna at the University Carlos III of Madrid. It is located in Leganés at

the Escuela Politecnica Superior of the mentioned university. In addition to teaching, the department is also involved in research projects related to analog electronics, digital electronics, microprocessors, microelectronics and electronic instrumentation.
The department includes five research groups which are involved in both European and national public funding projects. The outstanding effectiveness of this department becomes evident through the numerous patents that they have been able to obtain through their research projects.
The project has been carried out with the Micro Electronic Design and Applications (DMA) group, which is also part of this department, with the supervision of proffessor Enrique Prefasi. The underlying motif behind the development of this work was to collaborate with the project "Design and characterization of main building blocks for Medical Instrumentation". This project is performed by the DMA group togheter with Austria Microsystems (AMS), a company specialized in the microelectronics field. The project is basically directed towards the design of an integrated circuit to be used in an MRI readout system, and the conclusions emanating from the DMA group will be used in designing the final outcome of the project.
Regarding the economic aspects of such collaboration project, the budget available is used for scholarships, PhD research contracts and possible materials to be used for the development of the work, such as CADENCE and MATLAB licenses.

References

[1] Li,B.,Tenhunen,H.,"A design of operational amplifiers for Sigma Delta modulators using 0.35um CMOS Process", Electronic System Design Laboratory, Royal Institute of Technology.
[2]Baker, R.J., Saxena, V. "High Speed Op-amp Design: Compensation and Topologies for Two and Three Stage Designs"[Online]. Available: http://cmosedu.com/jbaker/papers/talks/Multistage_Opamp_Presentation.pdf
[3]Kumar, V., "High bandwidth low power operational amplifier design and compensation techniques" (2009). Graduate Theses and Dissertations. Paper 10766. Iowa State University.
[4]Analog Integrated Circuit Design, Op amp at the block level: Frequency compensation [Online]. Available: http://nptel.ac.in/courses/117106030/
[5]Allen, Holberg, *CMOS Analog Circuit Design*, 2nd Edition.
[6]Ames, J., *Operational Amplifiers:Basics and design aspects* [Online]. Available: http://uwf.edu/skamalasadan/final.pdf
[7]Brown, T.R., Carter, B., *Handbook of operational amplifier aplications*, Oct 2001 [Online]. Available: http://www.ti.com/lit/an/sboa092a/sboa092a.pdf
[8]CMOS Operational Amplifiers [Online]. Available: http://www.aicdesign.org/SCNOTES/2005notes/Chapter06-Web(8_3_05).pdf
[9]Gray, Hurst, Lewis, Meyer, *Analysis and design of Analog Integrated Circuits*, 4th Edition, John Wiley and Sons.
[10]Johns, D., Martin, K., *Analog Integrated Circuit Design*, John Wiley &Sons, 1997.
[11]Laker, K.R., Sansen, W.M.C., *Design of Analog Integrated Circuits and Systems*, 4th Edition, John Wiley and Sons.
[12]Peng, X., Sansen, W., "Transconductances with capacitances feedback compensation for multistage amplifiers," IEEE Journal of Solid State Circuits, vol. 40, no. 7, pp. 1515-1520, July 2005.
[13]Razavi, B., *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, August 2000.
[14]Roberge, J.K., *Operational Amplifiers: Theory and Practice* [Online]. Available: http://ocw.mit.edu/ans7870/RES/RES.6-010/MITRES_6-010S13_comchaptrs.pdf
[15]Embabi, S.H.K., Sanchez-Sinencio, E., You, F., "Multistage Amplifier Topologies with Nested Gm-C Compensation," IEEE Journal of Solid State Circuits, vol.32, no.12, Dec 1997.
[16]Eschauzier, R.G.H., Huijsing, J.H., "A 100-MHz 100-dB operational amplifier with multipath Nested Miller compensation," IEEE Journal of Solid State Circuits, vol. 27, no. 12, pp. 1709-1716, Dec. 1992.
[17]Fan, X., Mishra, C., Sanchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multistage amplifiers," IEEE Journal of Solid State Circuits, vol. 40, no. 3, pp. 584-592, March 2005.
[18]Furth, P.M., Garimella, A., Surkanti, P.R., "Pole-Zero Analysis of Multi-Stage Amplifiers: A Tutorial Overview"Klipsch School of Electrical and Computer Engineering, New Mexico State University.
[19]Grasso, A.D., Palumbo, G., Pennisi, S., "Advances in Reversed Nested Miller Compensation," IEEE Transactions on Circuits and Systems-I, Regular Papers, vol.54, no.7, July 2007.

[20]Leung, K. N., Mok, P. K. T., "Nested Miller compensation in low-power CMOS design," IEEE Transaction on Circuits and Systems II, Analog and Digital Signal Processing, vol. 48, no. 4, pp. 388-394, Apr. 2001.
[21]Grasso, A.D., Marano, D., Palumbo, G., Pennisi, S., "Improved Reversed Nested Miller Frequency Compensation Technique with Voltage Buffer and Resistor," IEEE Transactions on Circuits and Systems-II, Express Briefs, vol.54, no.5, May 2007.
[22]Saxena, V., "Indirect Compensation Techniques for Multi-Stage Operational Amplifiers," M.S. Thesis, ECE Dept., Boise State University, Oct 2007.
[23]Peng, X., Sansen, W., "AC boosting compensation scheme for low-power multistage amplifiers," IEEE Journal of Solid State Circuits, vol. 39, no. 11, pp. 2074-2077, Nov. 2004.
[24]Leung, K. N., Mok, P. K. T., Ki, W. H., Sin, J. K. O., "Three-stage large capacitive load amplifier with damping factor control frequency compensation," IEEE Journal of Solid State Circuits, vol. 35, no. 2, pp. 221-230, Feb. 2000.
[25]Leung, K.N., Mok, P.K.T., "Analysis of Multistage Amplifier-Frequency Compensation," IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications, vol. 48, no. 9, Sep 2001.
[26]Lee, H., Mok, P.K.T., "Advances in Active-Feedback Frequency Compensation With Power Optimization and Transient Improvement," IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications, vol.51, no.9, Sep 2004.
[27]Awad, I.A., Soliman, A.M., "Current Operational Amplifier (COA): CMOS Realization and Active Compensation" Analog Integrated Circuits and Signal Processing, 24, 141-152, 2000.
[28]Small- Signal Analysis of CMOS Two-Stage Op Amp [Online]. Available: http://people.seas.harvard.edu/~jones/es154/lectures/lecture_6/pdfs/lecture37.pdf
[29]Williams, J., *Analog Circuit Design: Art, Science and Personalities (EDN Series for Design Engineers) (Paperback) , Newnes; Reprint edition, 1991.*
[30]Baker, R.J., "CMOS: Circuit Design, Layout, and Simulation," 2nd Ed., Wiley Interscience, 2005.