A Study of Through-Silicon-Via (TSV) Induced Transistor Variation

by

Li Yu

Bachelor of Science, Microelectronics, Tsinghua University (2009)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Computer Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2011

Author .....
Department of Electrical Engineering and Computer Science
May 19, 2011

Certified by .....
Duane S. Boning
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Leslie A. Kolodziejski
Chairman, Department Committee on Graduate Theses

A Study of Through-Silicon-Via (TSV) Induced Transistor Variation

by

Li Yu

Submitted to the Department of Electrical Engineering and Computer Science
on May 19, 2011, in partial fulfillment of the
requirements for the degree of
Master of Science in Computer Science and Engineering

Abstract

As continued scaling becomes increasingly difficult, 3D integration has emerged as a viable solution to achieve higher bandwidth and power efficiency. Through-silicon-vias (TSVs), which directly connect stacked structures die-to-die, is one of the key techniques enabling 3D integration. The process steps and physical presence of TSVs, however, may generate a stress-induced thermal mismatch between TSVs and the silicon bulk. These effects could further perturb the performance of nearby electronic structures, particularly transistors, diodes, and associated circuits.

This thesis presents a comprehensive study to characterize, analyze and model the impact of TSV-induced stress impact on device and circuit performance and its interaction with polysilicon and shallow-trench-isolation (STI) layout pattern density. A test chip is designed with multiplexing test circuits providing measurements of key parameters of a large number of devices. These devices under test (DUTs) have layouts that explore a range of TSV and device layout choices in the design of experiments (DOEs). The test chip uses a scan chain approach combined with low-leakage and low-variation switches and Kelvin sensing connections, which provide access to detailed analog device characteristics in large arrays of test devices. A test circuit and an I_{off} measurement method is designed to perform off-chip wafer probe testing measurement.

In addition, a finite element analysis model is constructed to mimic realistic TSV structures and processes. A complete flow and methodology to analyze transistor characteristics and circuit performance under the influence of TSV stress is proposed. An efficient algorithm is also proposed to simulate full-chip circuit variation under the impact of TSV stress based on a grid partition approach. Test cases corresponding to the aforementioned test chip are simulated for comparison with measurement data.

Thesis Supervisor: Duane S. Boning
Title: Professor of Electrical Engineering and Computer Science

Acknowledgments

I can only thank MIT for giving me with the opportunity of attending such a prestigious institution, and meeting with so many fantastic and impressive people.

I would like to thank my advisor, Prof. Duane Boning, for giving me the opportunity to join his research group and guiding me through my masters. Without your unwavering support and clear guidance, my stay at MIT would not have been as exciting and fruitful. Thank you very much for all your help and guidance.I would like to thank Professor Dimitri Antoniadis for many helpful discussions on transistor physics and new transistor models.

I very much appreciate the collaboration and friendship from all my group mates at the Metrology group at MIT, present and past: Karthik Balakrishnan, Albert Chang, John Haeseon Lee, Hayden Taylor, Wei Fan, Joy Johnson, Cai GoGwilt and Jaime Diaz, thank you for all your noble help and support with the design, tape out, and testing of the test chip, not to mention all the scripts and all the support when things were not going so well. Karthik and Albert, thank you for all of your great ideas regarding the design and testing of the chip. John, thanks for all the collaboration during class and all the good times. Wei, thank you for all the laughs we shared, and all the advices you gave me, academic or non-academic. You made my life here truly fun and enjoyable. To everybody else: thanks for all the fun conversations, all the donuts, and all the good times. You will always be in my heart.

Last but not least, my family deserves all the credit for this accomplishment, as they have supported me every step of the way with complete selflessness. Thank you for your unconditional love. Lina and Yong, you are the best mom and dad one can ever wish for. You've taught me so much in every aspect of my life, academic or non-academic. Thank you for always being there with me to share the cheers during my success and comfort me during my down times. It is your encouragement that makes me go this far. Without you, my accomplishment here would mean nothing to me. You deserve every part of this thesis as much as I do. Thank you and I really love you.

Last, I would like to acknowledge Wenyao Chang, Kewei Zuo and Jean Wang from TSMC for their suggestions and tapeout of the chip. We gratefully acknowledge the support of TSMC for this research, and for their membership in the Microsystems Industrial Group of the MIT Microsystems Technology Laboratories (MTL).

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In 1965, Gordon Moore observed that the number of transistors on a single chip doubles every 18 to 24 months [12], known as Moore's Law. It has served as the driving force for an astonishing increase in the functionality and computational capability of electronic devices from then on. Minimum transistor dimensions scaled by a factor of 0.7 from generation to generation, which enabled integration of more transistors with less power dissipation. In recent years, however, several bottlenecks have appeared as we have continued to scale down to sub 28 nm technologies. The first is the difficulty and cost of continued lithographic scaling, which could make it economically impractical to scale devices beyond a certain pitch. The second bottleneck is that the increasing power dissipation stops the scaling of clock frequency. Even worse, dynamic power dissipation due to interconnect increases exponentially with scalings [13]. This suggests that it will be hard to improve system performance through scaling alone in the near future and that additional methods will be needed to achieve the desired performance.

Three-dimensional (3D) integration technology offers the promise of increasing system performance in addition to scaling. This is due to a number of characteristic features of 3D integration: decreased total wiring length (and thus reduced interconnect delay times), dramatically decreased number of interconnects between chips, and the ability to allow dissimilar materials, process technologies, and functions to be integrated.

1.1 Thesis Organization

We begin by presenting a historical perspective on the studies of 3D integrated circuit (IC) technology in Chapter 2. Although 3D is still identified as an "emerging technology," the commercialization of 3D ICs driven by the need for increasing system performance is inevitable. A summary of benefits of 3D ICs and key process steps involved in their fabrication, particularly relating to through silicon vias (TSVs), is discussed. The process steps and physical presence of TSVs, however, may perturb the performance of nearby electronic structures, particularly transistors, diodes, and associated circuits. The central focus of this work is to understand variation induced by TSV stress. Though there are few related works in this area, a comprehensive understanding for TSV stress induced variation is still needed. This includes the need for a realistic model supported by carefully designed devices under test (DUTs).

As a result of the previous analysis, we will focus on the study of TSV induced systematic circuit variation in this thesis. In Chapter 3, we discuss test structures which provide measurements of key parameters of large numbers of DUTs. These DUTs have layouts whose environments are comprised of a range of TSV and device layout choices which is enough to arrive at a quantitative understanding of the variation mechanisms and further model these variations in simulation tools. We also discuss macro-layout design to explore the interaction between TSV density and other layout pattern densities such as that of polysilicon and shallow trench isolation (STI).

In Chapter 4, we discuss our test circuit design. The test circuit is designed to perform the measurement on the test structure described in the previous chapter. We present an overview of relevant test circuits that characterize variations and present a test circuit with multiplexing test circuits that provides measurements of key parameters of a large number of devices. A novel test structure to measure both I_{on} and I_{off} is proposed in order to characterize the impact of TSV-induced stress on transistor performance.

Finally, a complete flow and methodology to analyze transistor characteristics and circuit performance under the influence of TSV stress is presented in Chapter 5. We

analyze the thermal stress contour near the silicon surface with single and multiple TSVs through both finite element analysis (FEA) and linear superposition methods. The biaxial stress profile is then converted to mobility and threshold voltage variations depending on transistor type and geometric relationship between TSVs and transistors. Next, we propose an efficient algorithm to calculate full chip circuit variation corresponding to TSV stress based on a grid partition approach. Finally, we discuss a TSV pattern optimization strategy, and employ a series of 17-stage ring oscillators using 40 nm CMOS technology as a test case for the proposed approach.

1.2 Thesis Contributions

One of the major objectives of this thesis is to give a comprehensive study of TSV induced variation. The major contributions in this thesis are summarized below:

- Design and implementation of a 60× 240 array of device under test (DUT) transistors to characterize single TSV stress induced variation and its interaction with layout pattern density and local layout pattern. In each region, a radius sampling scheme is proposed with different sampling distances and angles. Test structures are also designed with different Keep-Out-Zone materials and widths.

- Design and implementation of a 512× 512 array of DUT transistors to characterize pattern density and multiple TSV stress effects. Long range pattern density effects (STI, polysilicon and TSV pattern density) can also be tested.

- Design and implementation of a series of ring oscillators (ROs) with different RO spacings and TSV-to-transistor angles to characterize single TSV stress effects on digital circuits.

- A measurement technique utilizing leakage current subtraction and a calibration technique to effectively isolate I_{off} in DUT transistors and obtain full I-V curves.

• Design and implementation of a finite element analysis (FEA) based TSV stress model which predicts mobility and current variation of devices near TSVs. This model can be easily extended for full-chip analysis and predict the impact of TSV stress on circuit performance.

Chapter 2

Three Dimensional Integrated Circuits and Through Silicon Vias

As continued scaling becomes increasingly difficult, 3D integration has emerged as a viable solution to achieve higher bandwidth and power efficiency. Through-silicon vias (TSVs), which directly connect stacked structures die-to-die, are an enabling technology for future 3D integrated systems. However, mechanical stress is induced by the thermal mismatch between TSVs and the silicon bulk during wafer fabrication and 3D integration. This stress can cause both reliability issues at the boundary between silicon and copper, and variations in surrounding devices and circuits.

In this chapter, we present an overview of 3D integration technology and TSVs, the motivation for studying TSV-induced thermal stress on transistor performance, and the need for a physically-based variation-aware model relating TSVs to devices. We begin in Section 2.1 with basic reasoning for pursuing 3D integration, followed by a description of the detailed process technologies needed to implement 3D integrated circuits. In Section 2.2, we present an overview of TSVs, which are the primary enablers for stacking silicon devices. Specifically, via-first, via-middle and via-last, three critical TSV process choices, will be discussed and compared. In Section 2.3, we justify the need for charactering the impact of TSV-induced stress on circuit performance, which is also the goal of this thesis. Finally, in Section 2.4, we provide background and related work in this area which serve as a basis for our work.

2.1 3D Integrated Circuits (ICs)

Briefly speaking, 3D integration can be defined as a technology stacking multiple processed wafers containing integrated circuits on top of each other and using vertical interconnects between the wafers. This 3D structure provides opportunities for improving performance, enabling integration of devices with incompatible process flows, and reducing form factors [14]. The most compelling advantage of this structure is that the vertical interconnect successfully address the 2D interconnect problem by replacing long horizontal interconnects with short vertical interconnects [15]. As a result, the RC delay, crosstalk and power dissipation will be greatly improved. With the total length of interconnect fixed, a 25 percent or greater decrease in worst-case wire length [16] or interconnect power [17] could be achieved. In addition, since industry tends to adopt architectures compatible with highly multi-threaded and parallel computing systems, there are strong system needs for more memory bandwidth. The introduction of 3D integration satisfies this growing need.

The advent of 3D ICs also provides the opportunity for the on chip integration of heterogeneous devices and technologies such as memory, logic, RF and sensing circuits as the technology integration capabilities mature, as shown in Figure 2-1. Since the vertical via diameter is a primary indicator of the interconnect density, the 3D IC will be more powerful with the scaling of via diameter.

2.2 TSV Overview

As described above, an important technology for 3D integration is the vertical interconnect, in the form of through silicon vias (TSVs). Cross-sectional scanning electron microscope (SEM) images of copper-filled TSVs with different diameters are shown in Figure 2-2. Because the TSVs shown in these figures are TSVs before the wafer thinning process, the copper depth is normally $50\mu m$ to $60\mu m$, which is shallower than the thickness of the silicon bulk. As a result, the TSV process is a bottleneck for 3D integration because it requires a much deeper hole to be created vertically

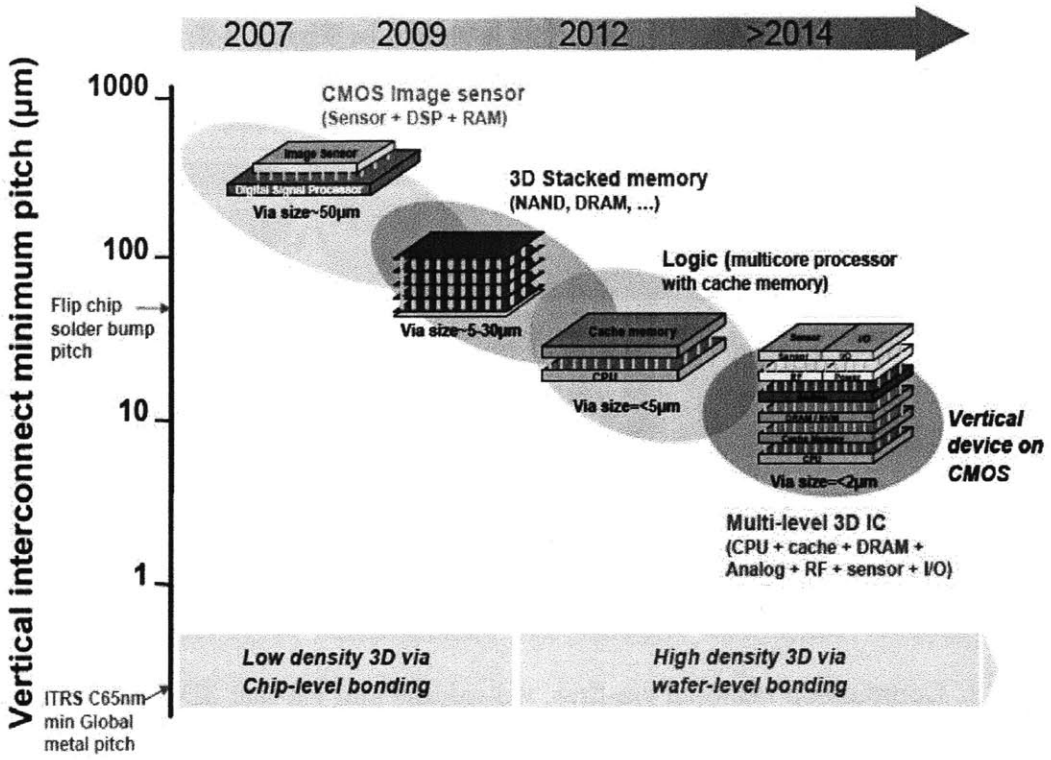

Figure 2-1: 3D applications and required via diameter [1].

through the silicon material using a special etching process.

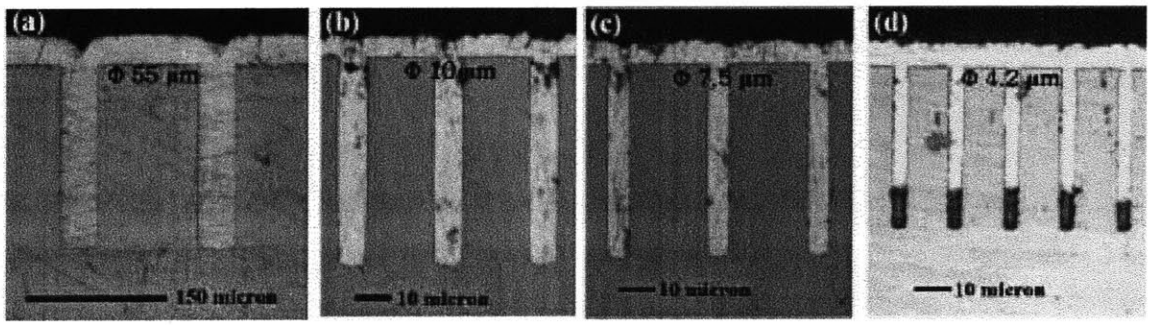

Figure 2-2: Cross-sectional scanning electron microscope (SEM) images of Cu-filled silicon via holes with a diameter and aspect ratio of (a) $55\mu m$, (b)$10\mu m$, (c) $7.5\mu m$, and (d) $4.2\mu m$ [2].

Processes in fabricating TSVs include through-wafer via formation, deep reactive ion etching (DRIE), via filling by deposition of diffusion barrier and adhesion layers, metalization, wafer thinning and alignment, and bonding. TSV integration schemes are categorized into via-first (via formation before CMOS process), via-last (via formation after BEOL) and via-middle (via between CMOS and BEOL). The sequence

of process steps in each of these approaches is shown in Figure 2-3.

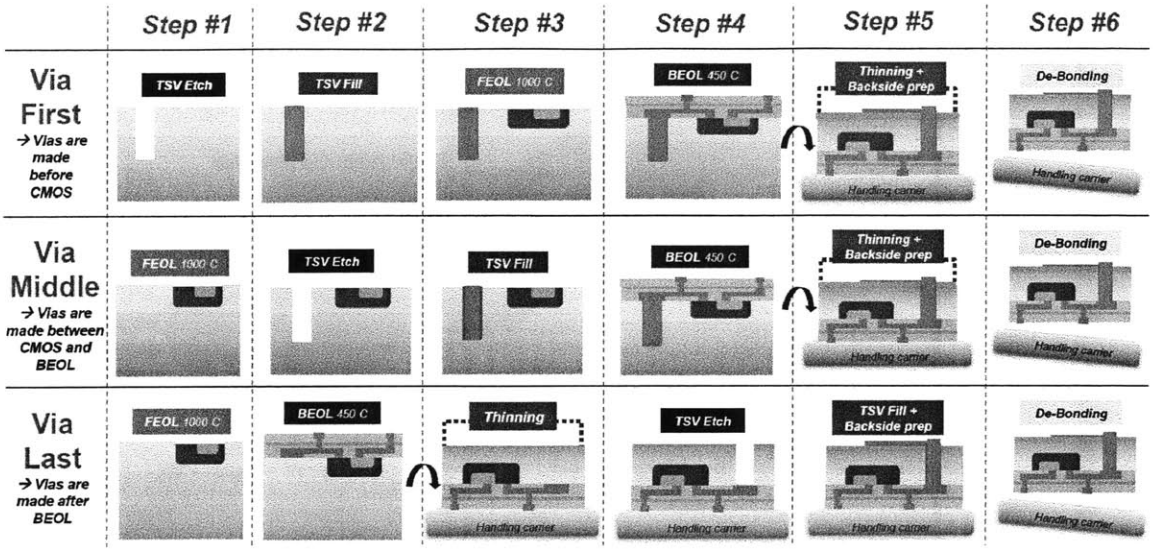

Figure 2-3: Comparison between via-first, via-middle and via-last 3D TSV integration scenarios [3].

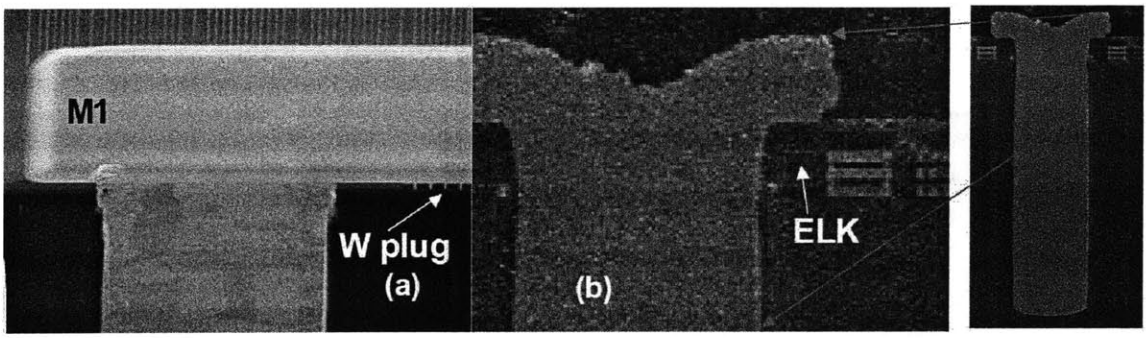

Figure 2-4: SEM comparison between via-first and via-last [4].

A via-first approach [18, 19] uses an annular via geometry for large-area contacts. The annular region is filled with isolation dielectrics, and the central core is subsequently etched and metallized. Recently, void-free fill by Cu electrochemical plating (ECP) has also been developed for high-aspect ratio TSVs in both via-first and via-last processes [4]. SEMs comparing TSVs fabricated through via-first and via-last are shown in Figure 2-4. The main difference is that the via-first scheme requires sophisticated Cu TSV CMP without damaging W plugs, while the via-last scheme requires delicate ELK etching without ELK degradation, as summarized in Table 2-1.

Table 2.1: Comparison between via-first and via-last schemes [4].

	via-first	via-last
TSV density	higher	lower
BOEL routability	good	acceptable
ELK etched by TSV pitch	not required	required
TSV CMP before M1	required	not required

2.3 Motivation for Characterizing TSV Induced Stress on Circuit Performance

The process steps and physical presence of TSVs may perturb the performance of nearby electronic structures, particularly transistors, diodes, and associated circuits. The mechanical stress in the silicon is due to the mismatch in thermal expansion coefficient (CTE) between the copper TSV (17.7 ppm/°C) and the surrounding silicon (3.05 ppm/°C)[9], as illustrated in Figure 2-5 [5]. This mechanical stress can be decomposed in two directions, radial tension and tangential compression, and further affects the carrier mobility and performance of the adjacent devices through piezoresistance effects.

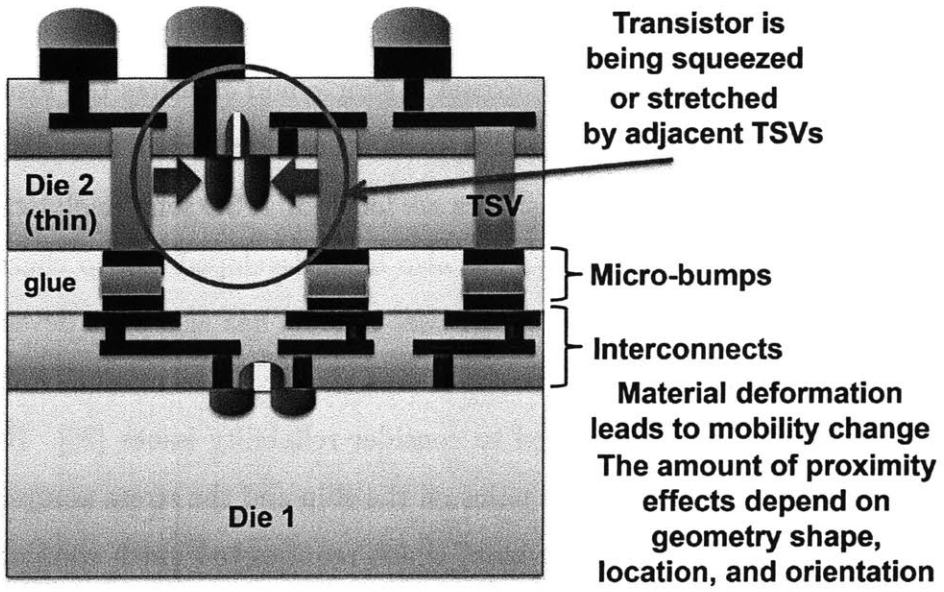

Figure 2-5: TSV structure and stress sources [5].

However, when a transistor is under the effects of several TSVs together, the problem is hard to handle. A full-chip analysis is difficult or infeasible using the simulation in the multi-TSV stress case through FEA because of the excessive computing resources required. Fortunately, linear superposition for TSV stress calculations has been demonstrated to be accurate [20]. In spite of this, however, accurate links that bridge stress to device characteristics such as mobility and threshold voltage still need to be built.

2.4 Background and Related Work

The fabrication of TSVs may induce thermo-mechanical stress due to mismatch in CTEs between a TSV fill material such as copper (Cu) and silicon (Si). This problem has existed since the first appearance of TSVs and has been widely discussed in the literature. However, most work in this area focuses on the fabrication and reliability issues [21, 22, 23]. The TSV impact on transistor performance is usually not known until the TSV process is stable and commercialized. Both finite element analysis (FEA) and analytical models have been proposed to characterize stress induced by TSVs. The analytical 2D radial stress model, known as the *Lamé* solution, was employed to address the TSV thermo-mechanical stress effect on device performance [22]. Though this closed-form formula is simple and captures the ideal stress distribution for a 1D axi-symmetric system, it does not capture the boundary stress field near the wafer surface where transistors are located. A 3D semi-analytical stress model valid for high aspect ratio TSVs has also been developed [23] to characterize the near-surface stress distribution. A FEA-based model has also been developed in this work which provides more realistic structures and accurate results. A full-chip stress analysis has also been developed to consider reliability issues [20]. However, the algorithm needs to calculate every point on the chip and the stress analysis needs a high sampling resolution within the map, which requires too much computational memory.

Tanaka first reported in 2007 that MOS transistor operation after both the post-

processing of TSVs and post-assembly was slightly affected by mechanical stress depending on the distance from a TSV to a MOS transistor, but the data was within the specification range [24]. Recently, the author in [25] provided measurements and 3D simulation results for single TSV-induced variation, but the analysis is only valid for simple TSV structures and does not capture the complex interactions with pattern density and keep-out-zone material and width. In addition, these models are only valid for simple TSV structures. Therefore a comprehensive understanding of TSV stress-induced variation is still needed. This includes output parameters - how device and circuit performance are affected by TSVs (e.g., Id(sat), Vt, leakage or ring oscillator frequency). Understanding variation also involves the consideration of input factors - what layout choices increase or minimize variation (e.g., TSV pitch, MOS location to TSV, MOS orientation relative to TSVs, device dimensions, STI, poly and TSV pattern densities). Finally, a full chip algorithm for analyzing TSV impact on transistor performance is also needed to model this effect during circuit design.

Chapter 3

Test Structure Design

In the previous chapter, we motivated the need for characterization and modeling of TSV-induced device and circuit variation. We also pointed out that transistor performance relies much more heavily on its layout context in advanced technologies. In this chapter, we motivate the importance of designing an effective test structure and analyze problems related to these test structures and ways to improve upon them. We build a test circuit that measures key parameters of a large numbers of devices under test (DUTs). These DUTs have layouts which explore a range of TSV and device layout choices in a design of experiment (DOE), which enables one to arrive at a quantitative understanding of these variation mechanisms and further model them in simulation tools.

This chapter is organized as follows. In Section 3.1, we explore different layout choices for the micro-layout, which includes layout design, pattern density, TSV pattern, radius sampling schematic and layout optimization. In Section 3.2, the macro-layout strategy for the whole chip is discussed. Finally, in Section 3.3 and in Section 3.4, we will summarize the design of experiment (DOE) and test structure design in our work.

3.1 Micro-Layout Design

Micro-layout strategy refers to layout dimensions and features of individual and small groups ofTSVs and transistors. In this thesis, the design variables include TSV design patterns, TSV-to-transistor relationships and transistor geometries. Different micro layout practices are used to accentuate one or more particular transistor variation sources.

3.1.1 TSV Layout

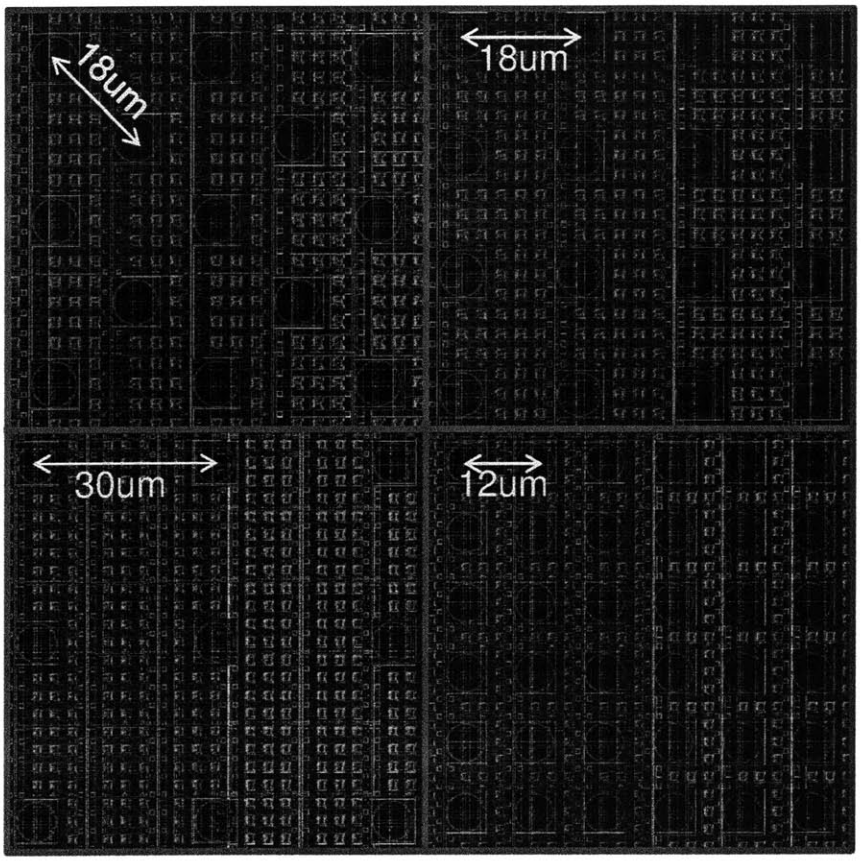

Figure 3-1: Multiple TSV pattern and sampling scheme. Upper-left: "diamond" TSV with 18 μm pitch; upper-right: "square" TSV with 18 μm pitch; lower-left: "square" TSV with 30 μm pitch; and lower-left: "square" TSV with 12 μm pitch.

The TSV layout is divided into two parts: a single TSV characterization block and a multiple TSV characterization block. For the single TSV block, each tile is designed with a size of $100\mu m \times 100\mu m$, with a single TSV located at the center. For

the multiple TSV block, both square and diamond layout patterns are explored, as is shown in Figure 3-1. In the top two figures, TSV layouts of square and diamond patterns with the same TSV pitch are compared. Also, the TSV layout of square pattern with 12 μm, 18 μm and 30 μm TSV pitches are compared. An array of sampling transistors are spread evenly around the TSV patterns with a sampling resolution of 3 μm. Different polysilicon and shallow trench isolation (STI) layout pattern densities are also explored in the multiple TSV characterization block.

3.1.2 Design of Layout Pattern Density

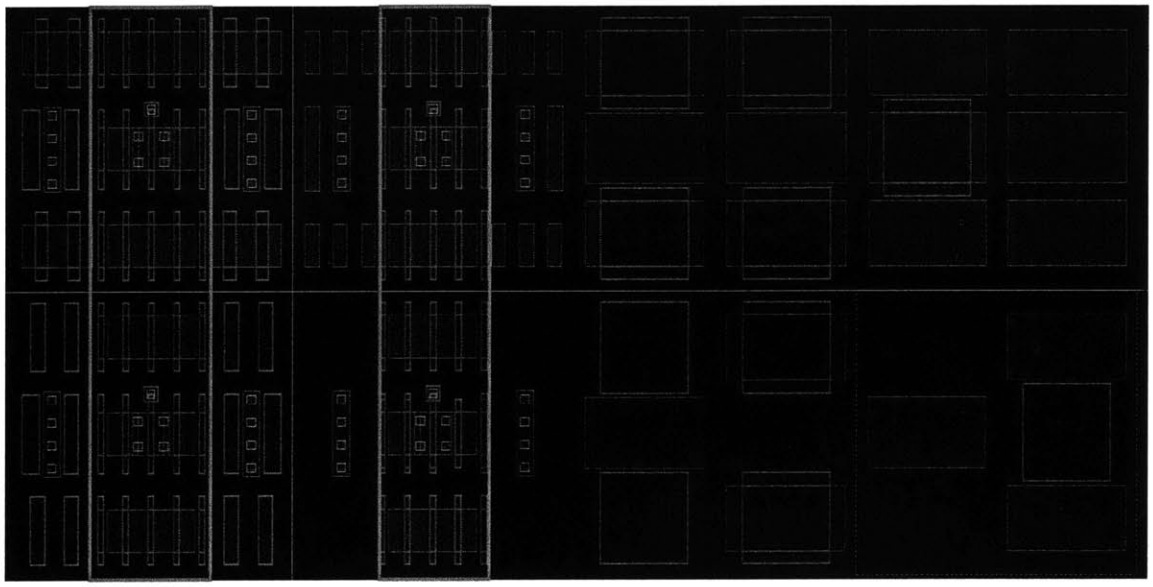

Figure 3-2: Local tile design for DUT transistors and dummy blocks where blue represents polysilicon and red represents OD.

The design of layout pattern density is also a critical issue in this work. Instead of filling the transistor tile with STI or polysilicon dummies, we separate the DUT tiles from dummy OD (complementary layer for STI) tiles and dummy polysilicon tiles. The tile context for transistors and dummies with different pattern densities is shown in Figure 3-2. The size of each tile is $2\mu m \times 2\mu m$.

The DUT tile design obeys the following rules: (1) The nearest dummy transistors or stripes to the DUT are fixed for all the tiles to avoid different local spacing for different DUTs; (2) dummy transistors are placed above or below the DUT; (3) all

dummy stripes are rectangular to mimic the shape of a realistic transistor layout.

The dummy tile designs obey the following rules: (1) The dummy tile size is the same as that of the DUT tile; (2) all dummy stripes are square with the same size to mimic the shape of a typical dummy layout.

The available set of densities for the DUTs is shown in Table 3.1. The STI and polysilicon pattern density across the whole chip is controlled by filling the area with dummy tiles and transistor tiles.

Table 3.1: Polysilicon and OD density for each transistor and dummy tile.

	Tile	Poly	OD	Poly density	OD density
1	transistor	high	high	23.2%	32.5%
2	transistor	high	low	23.3%	17.5%
3	transistor	low	high	7.6%	32.5%
4	transistor	low	low	7.6%	17.5%
5	dummy	high	high	40%	60%
6	dummy	high	low	40%	30%
7	dummy	low	high	10%	60%
8	dummy	low	low	10%	30%

3.1.3 Sampling Scheme

The stress and variation induced on transistors by TSVs are dependent on both TSV-to-transistor distance and angle, as will be discussed in Chapter 5. Therefore we develop a radius sampling scheme to characterize transistor variation at the most important distances and angles to the TSVs, as shown in Figure 3-3.

The sampling angles in this design are shown in Table 3.2, and the sampling distance are shown in Table 3.3.

Table 3.2: Sampling angles for single TSV induced stress characterization.

	1	2	3	4	5	6	7	8
Sampling angle(°)	0	45	90	135	180	225	270	315

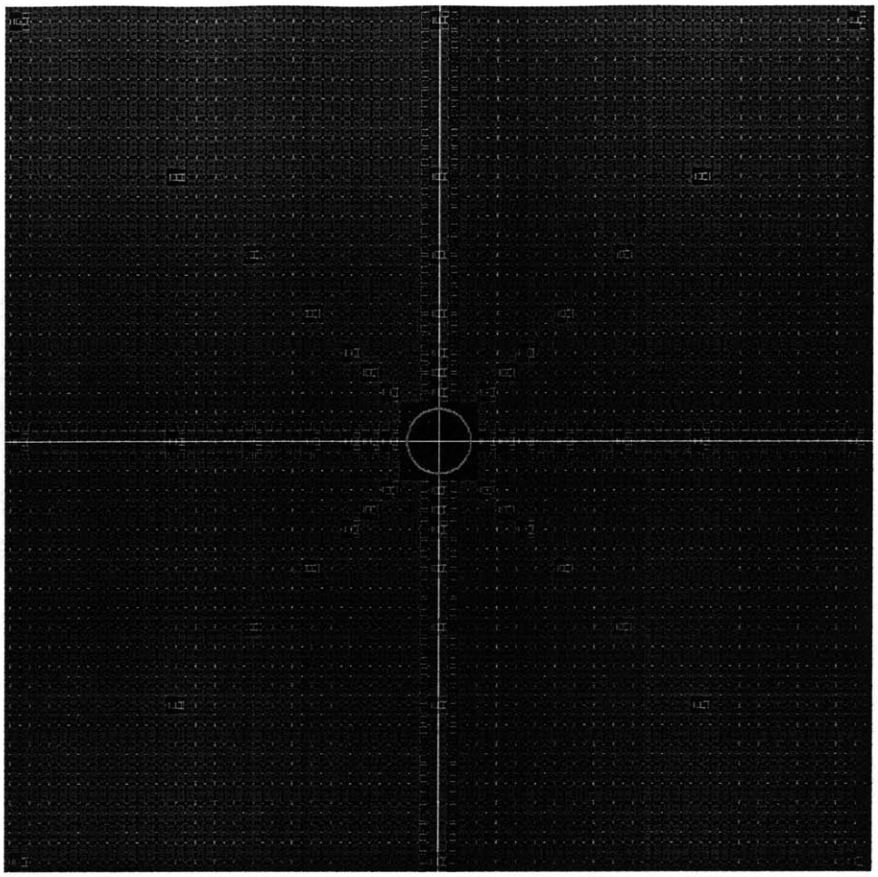

Figure 3-3: Radius sampling schematic for single TSV induced variation.

Table 3.3: Sampling distance for single TSV-induced stress characterization.

	1	2	3	4	5	6	7
Sampling distance from center of TSV (μm)	5	7	9	13	19	27	43

3.1.4 Layout Optimization for Stress Relief

In the previous sections, we explored how different DOE choices affect DUTs with regards to TSV pattern, polysilicon density, STI density, TSV-to-transistor distance and angle. However, the introduction of a keep-out-zone (KOZ) may also introduce some systematic variation on nearby transistors. In 3D ICs, the KOZ represents an area near a TSV on which circuit layout cannot exist, due to thermal, stress, and manufacturing variation management constraints. While pattern density can affect transistor performance, the parameters governing the KOZ can also affect transistor characteristics because of proximity and stress effects. Therefore, we explore different KOZ materials and distances, as shown in Figure 3-4.

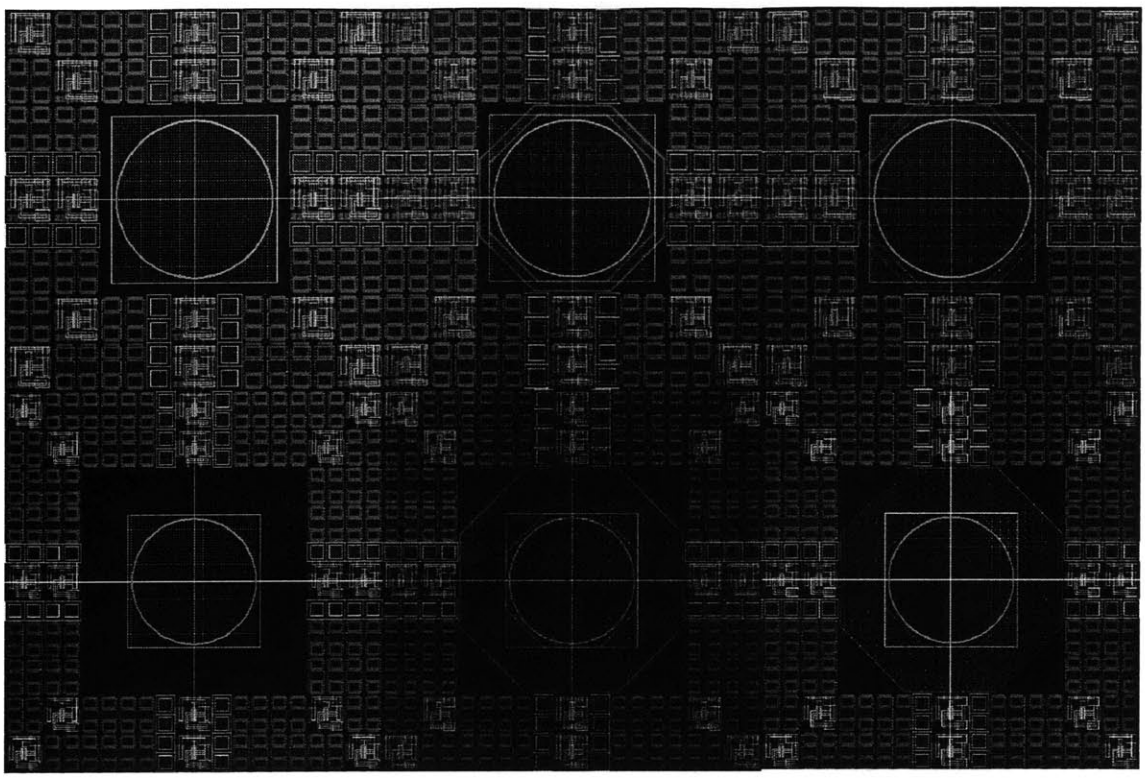

Figure 3-4: Local tile design for DUT transistors and dummy blocks where blue regions represent for polysilicon stripes and red regions represent for OD stripes.

In Figure 3-4, the first and second rows have a KOZ with a widths of $0.7\mu m$ and $2.7\mu m$, respectively. The first, second and third columns have the KOZ materials of STI, STI with polysilicon, and OD, respectively. After this experiment, the extent to which different KOZ materials and widths compensate for TSV stress will compared.

3.2 Macro-Layout Design

We further explore how macro-layout, which refers to a layout strategy on a large spatial scale, affects transistor performance. Two particular layout patterns, STI and polysilicon, are selected and their long range pattern density effects are examined. Because local layout density effects have been well-studied, our focus is on global density effects, different from prior work [8].

The detailed test structure layout is shown in Figure 3-5. The entire die is divided into four different regions: one $1mm \times 1mm$ region with high polysilicon density and

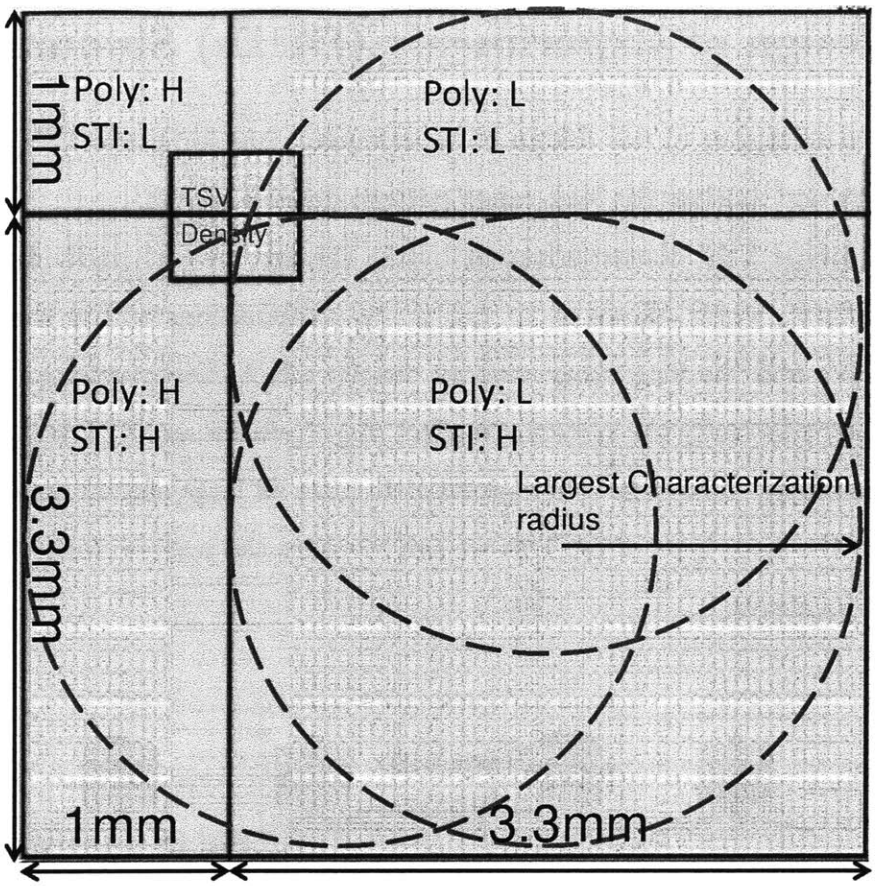

Figure 3-5: Macro-scale test structure layout.

low STI density; one $1mm \times 3.3mm$ region with high polysilicon density and high STI density; one $3.3mm \times 1mm$ region with low polysilicon density and low STI density; and one $3.3mm \times 3.3mm$ region with low polysilicon density and high STI density. The largest square size is $3.3mm \times 3.3mm$, giving us the ability to explore a long-range interaction distance on characterization radius of $3.3mm$ for both polysilicon and STI patterns densities.

This macro-layout strategy has the advantage of being able to capture long-range pattern density effects even with a relatively small chip size. The simple and uniform context also highlight the different response outputs when subject to different pattern density inputs. In the middle of the whole chip, a branch of TSVs are also designed to achieve a high TSV pattern density region. Therefore the chip is also able to capture long range TSV density effects on transistors and their interaction with polysilicon and STI pattern densities.

3.3 Design of Experiments (DOEs) Summary

We have two strategies in our design of experiments: one for single TSV characterization blocks and another for long-range pattern density blocks.

For the single TSV characterization block, the size of each individual block is $100\mu m \times 100\mu m$, which allows us to test many combinations within the DOE. For multiple TSVs and the long range pattern density effect characterization block, our main purpose is to study the systematic effect of polysilicon and STI density on transistor performance. Therefore it is important to have an large spatial map containing replicates of the same type of DUT so we can measure the performance of transistors at different locations.

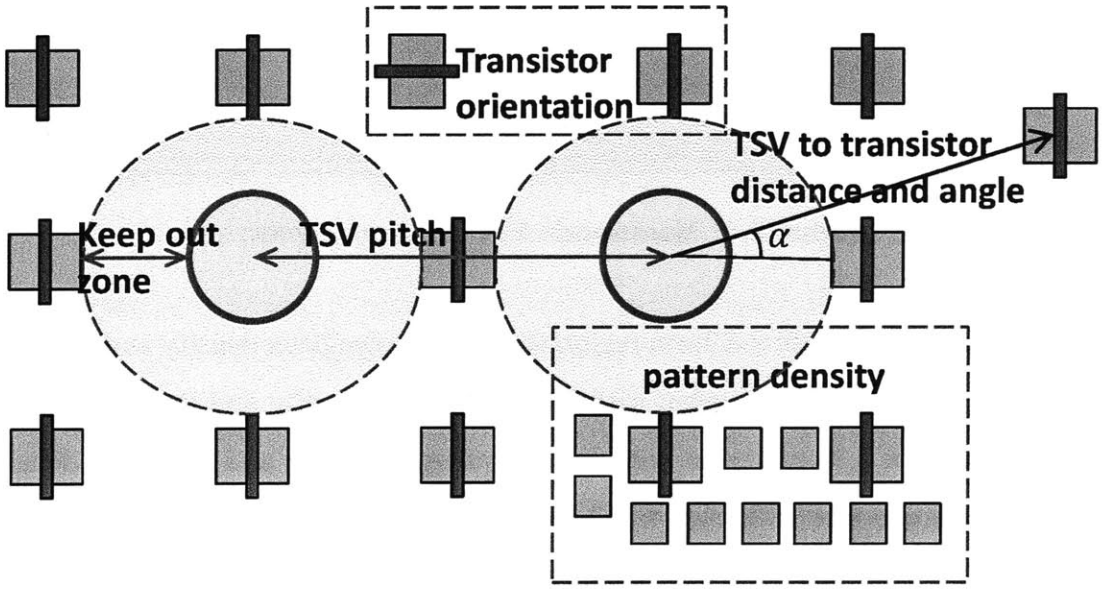

Figure 3-6: Illustration of TSV layout parameters.

The DOE for the single TSV characterization block includes several key layout design parameters: TSV pitch, TSV separation distances from devices, device orientation, TSV keep-out-zone material and width, and transistor geometric parameters (trench widths, active area sizes, transistor width and length, etc.), as well as longer range parameters including pattern densities of polysilicon and STI as summarized in Figure 3-6. Each DUT type consists some particular combination of these layout

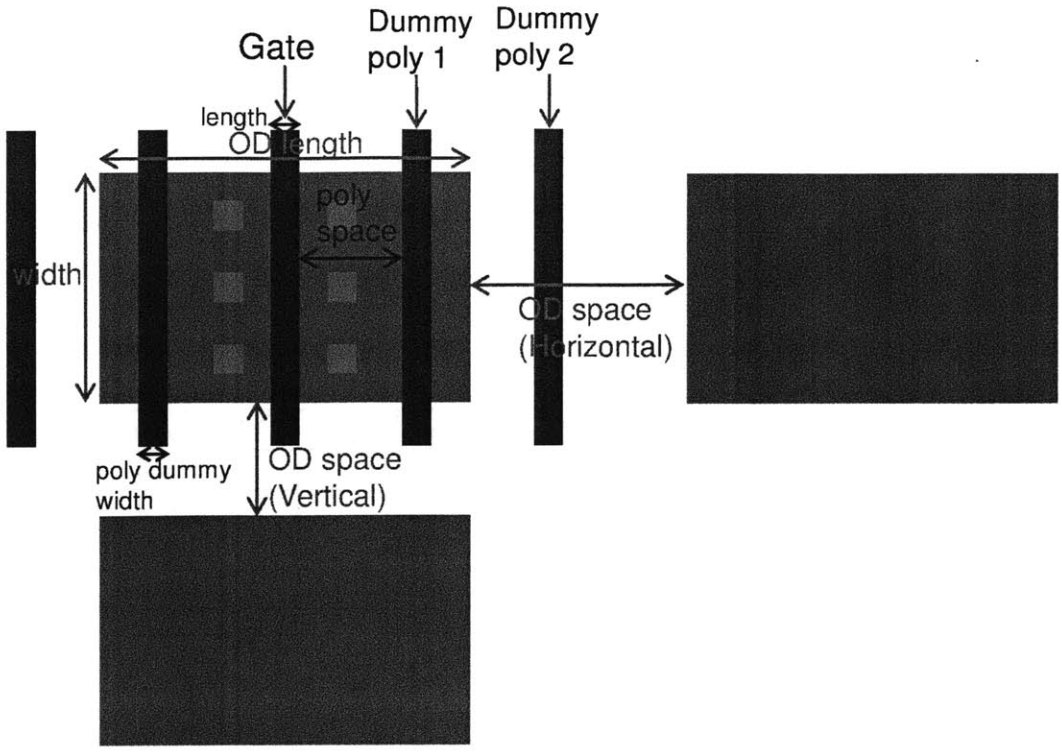

Figure 3-7: Illustration of transistor layout parameters.

design parameters and the entire chip includes a total of 64 types of devices under test, as shown in Table 3.4.

Table 3.4: Single TSV block summary.

Cell Type	Transistor Type	KOZ Material	KOZ Distance	Orien-tation	Pattern Density	Local Spacing	Total cell
Typical with TSV	4	1	1	1	4	1	16
Typical without TSV	1	1	1	1	4	1	4
Stress Relief	1	3	4	1	4	1	28
Orientation	1	1	1	1	4	1	4
Local spacing	1	1	1	1	1	8	8
Density(TSMC style)	1	1	1	1	4	1	4
Summary	4	3	4	2	4	8	64

For the layout dimensions and features of individual transistors, we explore the following geometric variables: transistor width, transistor length, active area (OD) length, vertical OD spacing, horizontal OD spacing, polysilicon spacing, and polysilicon dummy width, as is shown in Figure 3-7. These parameters are related to local spacing effects and stress, which could induce variation on transistors. Therefore our

test structures employ the same group of geometric parameters for different transistor sizes in most cases, as is shown in Table 3.5. DUT type 2 corresponds to the typical transistor size in 40nm technology, while type 1 corresponds to minimum-size in transistor. Type 1, 2 and 3 are all short-channel devices with a $40nm$ gate length and type 4 is a long-channel device with $1\mu m$ gate length.

Table 3.5: Layout design parameter values.

DUT	Length(nm)	Width(nm)	OD length(nm)	Cell length(μm)
1	40	120	620	2×2
2N	40	300	620	2×2
2P	40	600	620	2×2
3	40	1000	620	3×3
4	1000	1000	1520	3×3

To further explore the spacing effect and its interaction with TSV effect, a group of spacing parameters is also explored in the test structure, as shown in Table 3.5. The spacing effect due to different geometric parameters can be examined from combinations of the following groups: (1) DUT groups 1 and 2: exploring the horizontal OD spacing effect; (2) DUT groups 3, 4 and 5: exploring the polysilicon spacing effect; (3) DUT groups 1 and 7: exploring the vertical OD spacing effect; (4) DUT groups 3 and 6: exploring the polysilicon dummy width effect; and (5) DUT groups 1 and 8: exploring the OD length effect.

Table 3.6: Design of experiment: spacing effect (transistor for N and P are all type 2 (typical) with low PO/OD density).

DUT	OD Length (nm)	Vertical OD Spacing(nm)	Horizontal OD Spacing(nm)	Poly Spacing (nm)	Poly dummy Width (nm)
1	620	N:700 P:400	380	140	40
2	620	N:700 P:400	1380	140	40
3	Same as DUT 2 but without dummy poly stripes between two DUT				
4	620	N:700 P:400	1380	160	40
5	620	N:700 P:400	1380	200	40
6	620	N:700 P:400	1380	140	80
7	620	N:1700 P:1400	380	140	40
8	260	N:700 P:400	380	140	40

3.4 Summary

This chapter presented a comprehensive description of our test structure design. We began by explaining the fundamental differences between macro- and micro- test structure design. In the micro-layout section, a detailed discussion of TSV layout design, sampling DUT tiles and pattern density tiles design were provided. A radius sampling scheme specifically designed to characterize TSV-induced transistor variation depending on TSV-to-transistor angles and distances was proposed. After that, different KOZ materials and distances were discussed to explore layout optimization for TSV stress relief. In the macro-layout section, the test structures were designed to explore the interaction between TSV density and other layout pattern densities such as that of polysilicon and shallow trench isolation (STI). Finally, a brief summary on all DOE types and their illustration was provided.

Chapter 4

Design of Test Circuit Architecture

As transistor scaling continues, process variation is becoming increasingly important in both IC design and manufacturing. Therefore, there is an increasing need to design test circuits to characterize this variability. In Chapter 2, we described the introduction of 3D ICs and the variability issues that TSVs bring to transistors and circuits. In Chapter 3, we presented a test structure design to study the impact of stress on device and circuit performance, particularly when induced by single and arrayed TSVs combined with interaction with polysilicon and shallow trench isolation (STI) layout pattern density. In this chapter, we design a test circuit for characterizing TSV-induced variation on devices and circuits. We will motivate the need for a novel test circuit to characterize TSV-induced variation in Section 4.1, describe the test circuit architecture and TSV effects on ring oscillators in Section 4.2, a description of of the test circuit operation in Section 4.3, and end with a summary in Section 4.4.

4.1 Previous Test Circuit Design Related to Variation Characterization

Much work has been done to design test structures that perform measurements to help control, characterize, and model the behavior of transistors. Depending on the purpose of the test structure, the test circuit can either be simple or complex. One of

the most commonly used methods is the probing of individual transistors using four probe pads, one for each terminal of the transistor. Though this method provides I-V data for process monitoring purposes, it can also provide sufficient data to characterize the variation. However, each transistor will need at least four pads and this could result in large amounts of wasted area and thus a limited number of dvices under tests (DUTs) in the test chip.

Gettings et al. proposed an analog-multiplexed test structure which shares the same group of pads for multiple DUTs [6], as shown in Figure 4-1. A scan chain approach was adopted to control the switches that turn the DUT on or off. Though this method greatly increases the number of DUTs when compared to the four probe pads approach, the total number of DUTs is still less than what is required for a TSV test chip and the leakage in unselected DUTs contributes to total current measurement, which will not allow for sub-threshold current measurements.

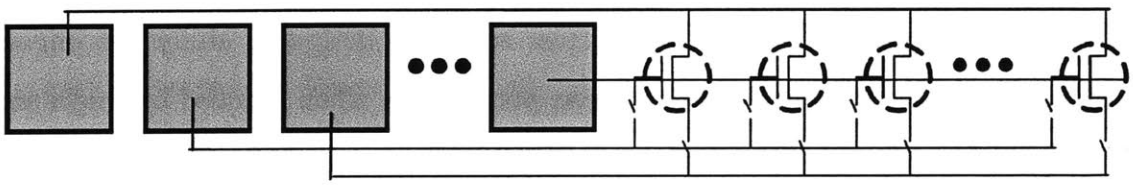

Figure 4-1: Multiplexed test structure to share pads across multiple devices [6].

Drego et al. designed a dedicated test circuit that characterizes threshold-voltage variation [7]. The current measurement is done from the subthreshold regime with small V_{ds} values to separate the variation in V_T from the variation in other parameters, including channel length. A hierarchical access scheme, shown in Figure 4-2, divides the entire die into six sections, each having 90 rows and 127 columns, and allows access to the individual transistor. An on-chip dual-slope ADC is used to perform the current measurement of around $70K$ transistors. An active current subtraction scheme was devised and implemented on-chip to subtract finite leakage current I_{leak} through the row and column access transistors and the "off" DUTs from the measured I_{DS}. However, our test circuit design for TSV induced variability must characterize a full I-V curve rather than just the sub-threshold regime. Moreover, extra transistors

are needed in our design to control the "on" or "off" states of each DUT, which add complexity to satisfy our purpose to control peripheral layout density.

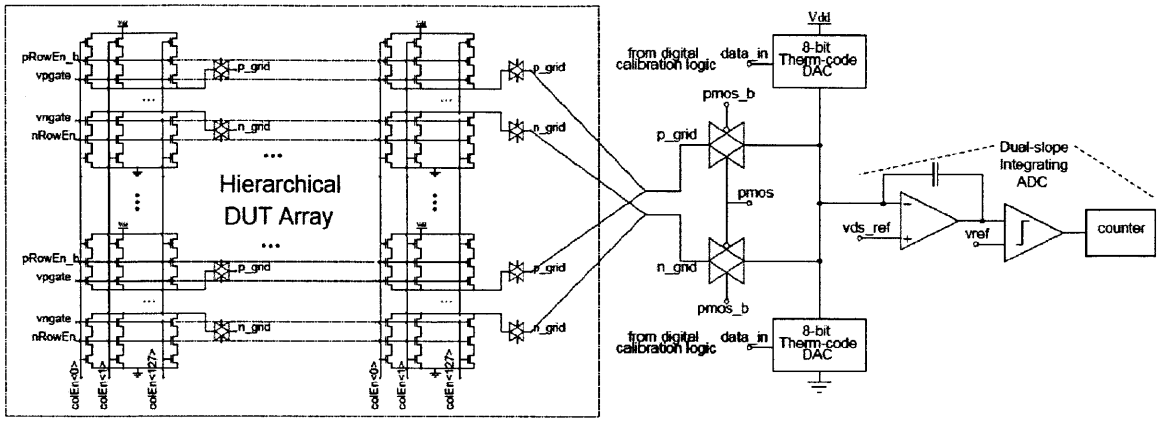

Figure 4-2: Hierarchical access scheme for threshold voltage extraction [7].

Chang et al. proposed a test circuit to investigate the influence of polysilicon density and shallow trench isolation (STI) density pattern on transistor characterizations [8], with a test structure shown in Figure 4-3. The test structure is designed to have more than 260K DUTs with measurement range from subthreshold regime to saturation regime. The test circuits are designed to perform either off-chip wafer probe testing measurement, or on-chip current measurement using an analog-to-digital converter (ADC).

Recently, a few test structures were specifically designed to characterize transistor variation induced by TSV stress. A high resolution DAC based test structure and a MOSFET array based test structure have been proposed to characterize the impact of TSV stress on MOSFET devices [9, 25], as shown in Figure 4-4. Experimental results showed that the variation induced by TSV stress is affected by the particular fabrication process, TSV-to-transistor distance and angle. However, this approach is only valid for long channel devices in saturation regime. Furthermore, the complex interaction between TSV stress effects and pattern density effects is not captured.

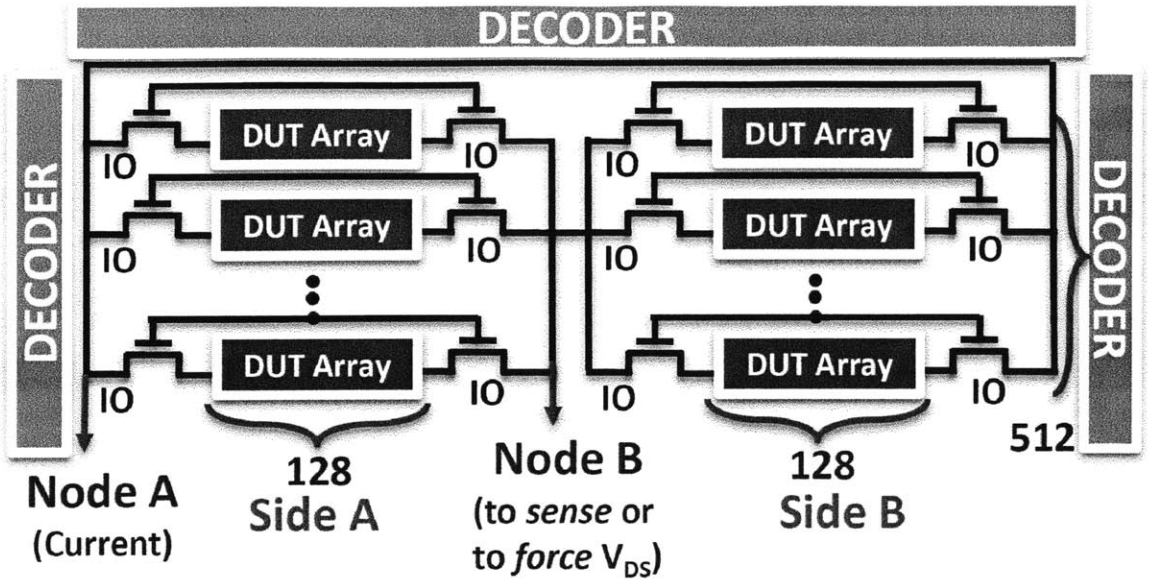

Figure 4-3: Hierarchical accessing scheme analogous to memory design [8]

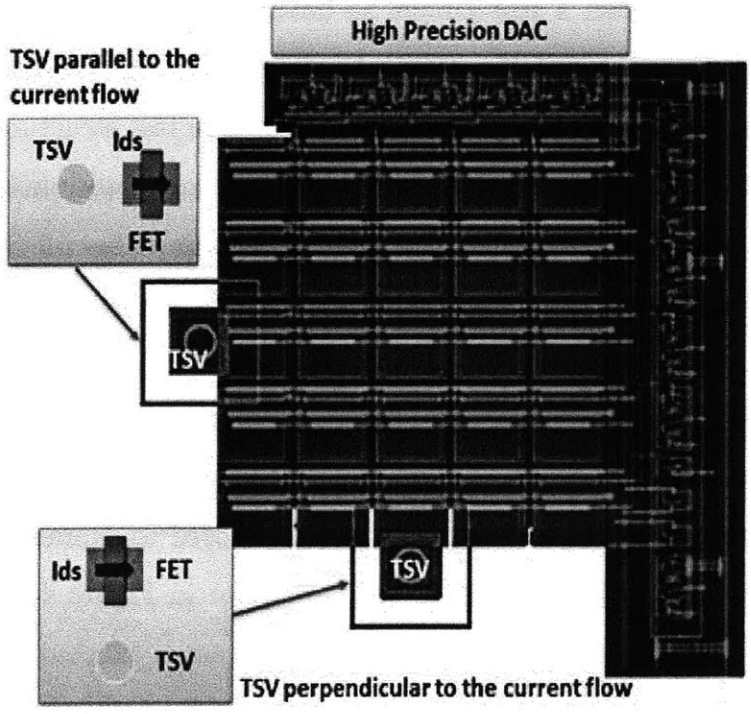

Figure 4-4: A high resolution DAC based test structure [9]

4.2 Test Circuit Architecture

As discussed in Session 4.1, none of the existing test circuits is adequate to comprehensively study TSV-induced variation on transistor and circuit performance. In this work, a comprehensive study to characterize and analyze stress impact on devices and ring oscillator (RO) circuits induced by TSVs and its interaction with polysilicon and shallow trench isolation (STI) is proposed. A test circuit with the capability to access 290K DUTs with full I-V characteristics is designed. An I_{off} measurement technique is implemented which is compatible with off-chip wafer probe testing. Circuit simulations show that the proposed multiplexing approach is very accurate, with an error less than 0.1% in measured current. The test structure is divided in three regions as summarized below.

- Region 1: Two 60× 240 device under test (DUT) transistor arrays with nMOS and pMOS devices respectively are designed to characterize single TSV stress using different KOZ materials and widths.
- Region 2: 512× 512 DUT transistor arrays are designed to characterize pattern density and multiple TSV stress effects. Long-range pattern density effects (STI, polysilicon and TSV pattern density) can also be tested in this region.
- Region 3: Four ring-oscillator (RO) groups with different RO spacings and TSV to transistor angles are designed to characterize single TSV stress effects on digital circuits. In each block, 128 groups of 17-stage ring oscillators with constant STI and poly density are designed to characterize TSV stress effects on circuit speed.

4.2.1 Test Circuit Architecture (I): Transistor Arrays Design

In the case of multiple TSV variation characterization with mixed nMOS and pMOS transistors uses a transistor array with 512 columns and 512 rows, for a total of 262,144 transistor DUTs, as illustrated in Figure 4-5. The multiplexing approach for single TSV variability characterization is a transistor array with 60 columns and 240 rows, a total of 28,800 transistor DUTs, as illustrated in Figure 4-6. For both test

circuits, all DUT gates on each column are connected to "Gon" or "Goff" depending on their on or off states for the gate. For NMOS transistors, the source of all the DUTs is connected to ground, and for PMOS transistors, the source of all the DUTs is connected to the supply voltage. All DUT drain terminals on each row are connected together to two low-leakage switches which are carefully designed to ensure that on and off states of the DUTs are accurate. These switches are input-output (I/O) devices controlled by row-enabling signals.

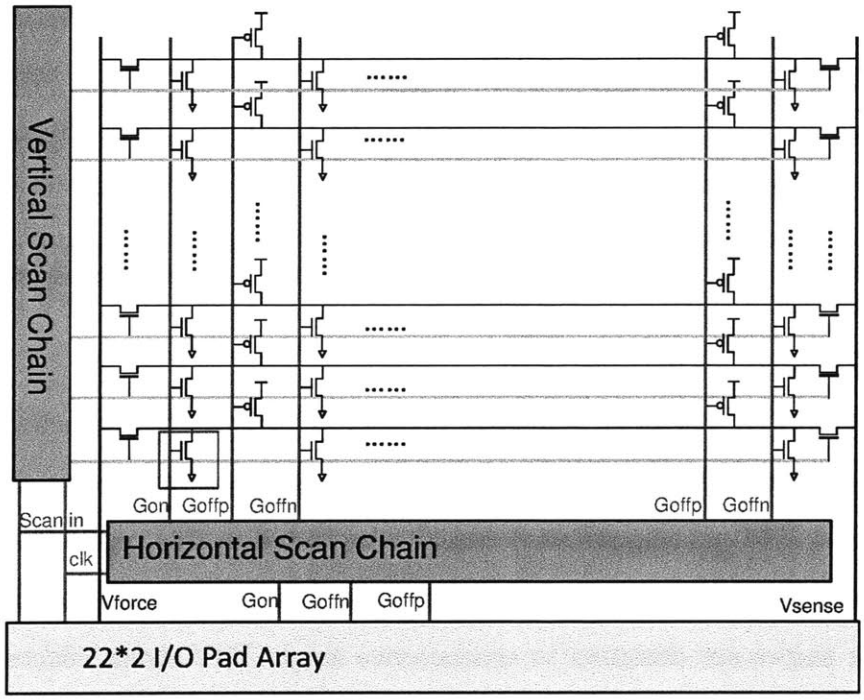

Figure 4-5: Proposed multiple TSV and long rang pattern density induced variation characterization circuit approach for mixed nMOS and pMOS transistor arrays.

A scan chain is employed to generate both row and column enable signals. During each measurement cycle, only one row of I/O devices and one column of gate are enabled, which ensures that the current from only one DUT is measured at shared drain terminal. For the other off-state DUTs, either a negative voltage is applied in the case of NMOS, and an above-supply voltage will be applied in the case of PMOS to minimize leakage. To minimize the effects of IR drops of switches and interconnects, a Kelvin measurement technique is adopted which ensures that the voltage at the DUT drain is equal to the intended voltage.

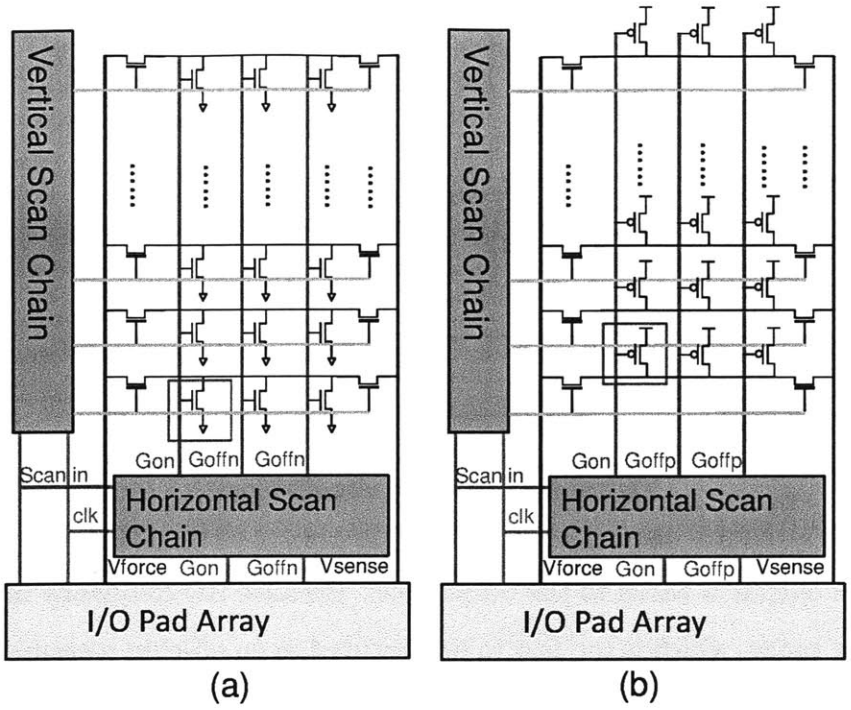

Figure 4-6: Proposed single TSV variation characterization circuit approach for (a) nMOS transistor array or (b) pMOS transistor array.

4.2.2 Test Circuit Architecture (II): Ring Oscillator Design

To further characterize TSV stress effect on circuit performance, 128 groups of 17-stage ring oscillators (RO) are designed with different TSV-to-RO distances and angles. The RO frequency is selected as an indicator of TSV stress because (1) it is a direct circuit-level timing parameter that can be easily measured, (2) it is sensitive to device and interconnect parameters, and (3) random variation in RO chains can be greatly suppressed by the averaging effect.

The 128 groups of ROs are divided into four RO test blocks to increase spatial sampling resolution. The detailed test circuit architecture for each group is shown in Figure 4-7, where each block contains 32 tiles. Each one of the tiles contains a ring oscillator and peripheral control circuitry. A scan chain approach to select the DUT in the analog multiplexing circuit is also employed in this scheme to select an RO under test. For each measurement, only the tile under test is selected and the RO in that tile is enabled. The output of the ring oscillator is connected to the input of a tri-state buffer, whose enable input is connected to the output of the scan chain, and

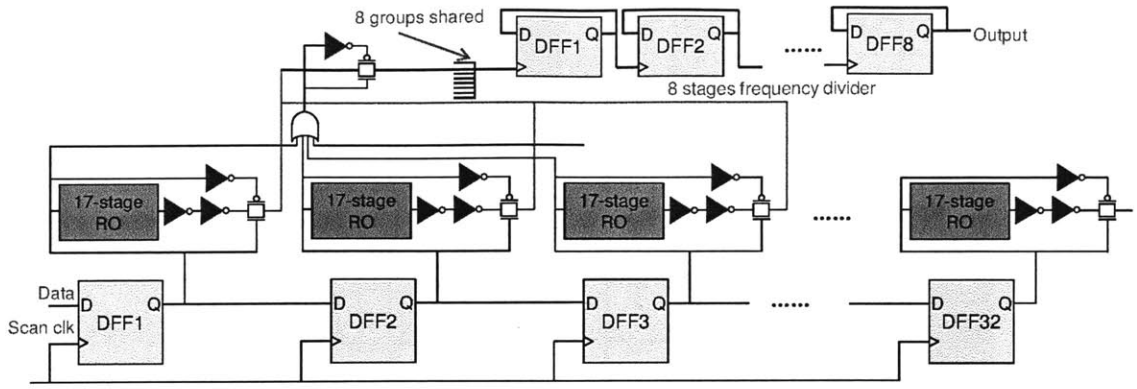

Figure 4-7: RO test circuit block.

the tri-states output is wired to the output bus. Because RO frequency in $40nm$ is in the gigahertz range, which is too fast to be captured in an off-chip measurement, eight frequency dividers follow the output bus to divide the frequency into the megahertz range. The layout for each tile is shown in Figure 4-8, with the size of each tile being $5.22\mu m \times 5.22\mu m$.

4.3 Test Circuit Operation

The test circuit operation ensures that the test circuit measures the exact current through the DUT, which requires taking into account leakage current through other rows and columns. In this section, we will discuss the methods used to achieve that goal including forcing and sensing, leakage mitigation, and a novel I_{off} calibration method. The test circuit schematic is shown in Figure 4-9.

4.3.1 Forcing and Sensing

For each DUT measurement, we apply the desired gate voltage to the DUT through the column enable signal, and we apply the desired drain voltage indirectly by forcing a voltage on node A. All other DUT rows and columns are off except the one containing the DUT to be measured. The voltage at node B is sensed as the desired drain voltage. Because the sensing source monitor unit (SMU) has a high impedance

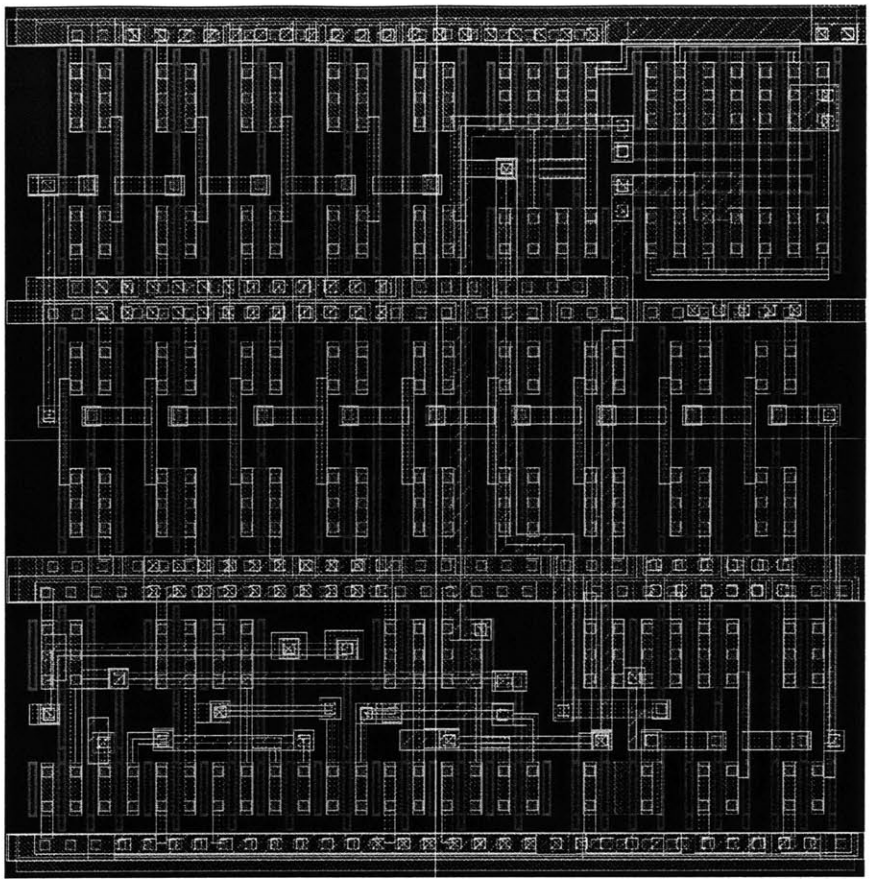

Figure 4-8: RO tile layout.

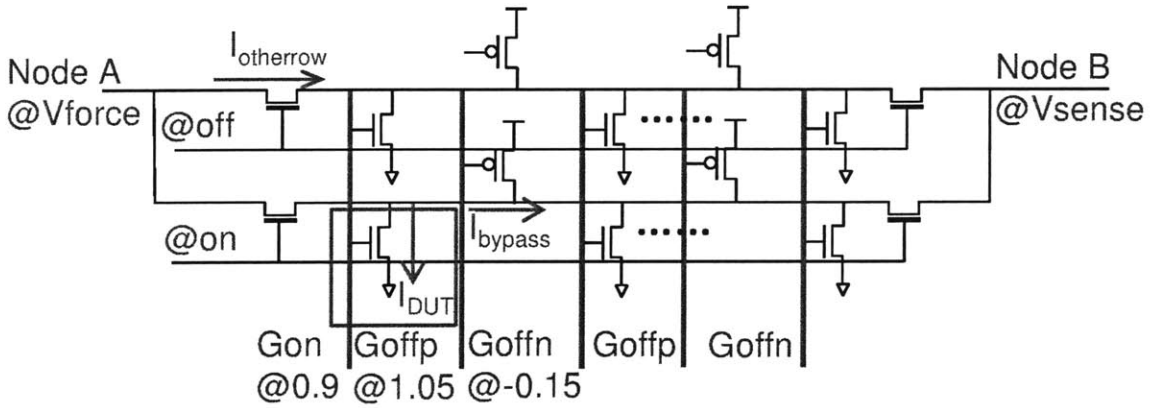

Figure 4-9: Test circuit operation schematics.

and there is very small current coming out of Node B, the IR drop between node B and the DUT drain is negligible. We then measure the current through Node A. Simulation results shows that the voltage difference between node B and drain of each measured DUT is smaller than $0.1mV$.

4.3.2 Leakage Mitigation

While the force-and-sense approach ensures the desired voltages at the four terminals of each measured DUT, the leakage current through bypass columns and rows still cause error in the measurement data. Therefore, it is necessary to make sure that this leakage is not significant compared to the minimum current we want to measure. The criterion for leakage current to judge this importance is set to be 1% of the DUT current. If the leakage current is significant when compared to the total measurement current, an I_{off} calibration method will be employed to calibrate the measurement data. This method will be discussed in Section 4.3.3. Here, we introduce two methods to minimize the leakage current coming from the DUTs in other DUT rows and other DUT columns, respectively.

To minimize the leakage current coming from the DUTs in other rows, we use two I/O devices as the row-enable switches, shown in Figure 4-9. By placing two I/O devices across the DUT array, the leakage is reduced through two mechanisms: (1) the number of transistors contributing leakage reduces from tens or hundreds to one; (2) because of the thicker gate dielectric layer, the I/O device has much higher V_T compared to a normal device, which reduces the leakage current exponentially. The total leakage can be reduced by almost three orders of magnitude by using I/O devices [8].

For the DUTs in the same row as the measured DUT, negative gate biasing will be introduced, which reduces 80% of their leakage current. The negative gate bias is set to -0.15V, which is an optimization point from simulation, as shown in Figure 4-10.

After these two methods, the total leakage of the test circuit is reduced to hundreds of nA for the multiple TSV array and tens of nA for the single TSV array. This is very accurate for above-threshold device characterization. For subthreshold measurements

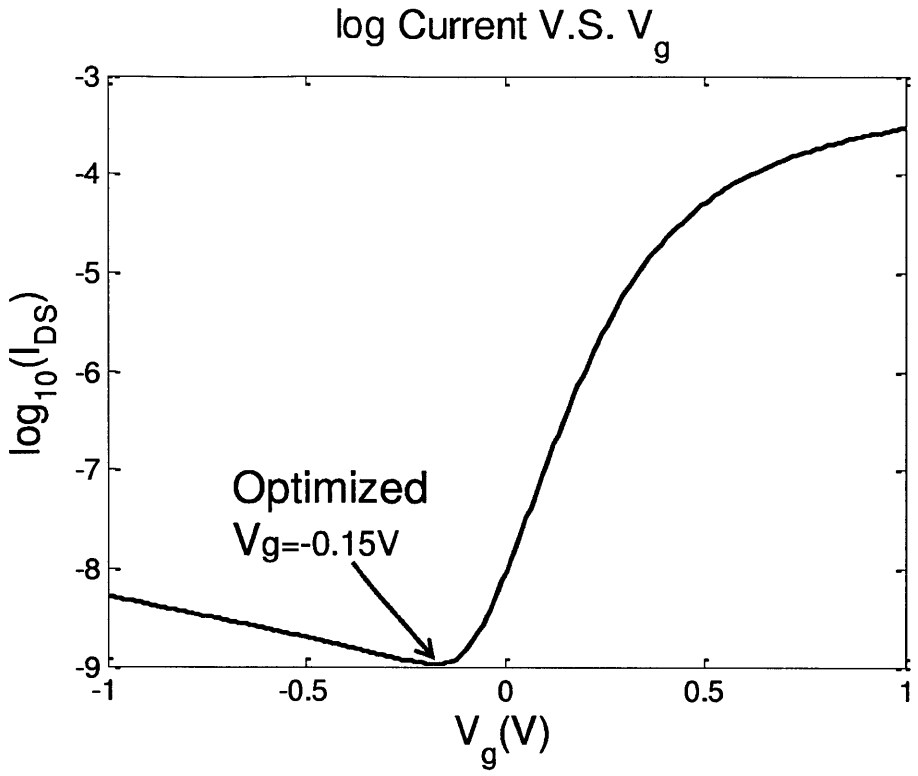

Figure 4-10: Optimal V_{gs} selection to minimize overall leakage.

and I_{off} measurements, a leakage calibration methodology will be introduced in the next section.

4.3.3 I_{off} calibration method

Threshold voltage and leakage current are also affected by TSV stress because strain can cause shifts and splits in both the conduction band and valence band. However, traditional array based test structures cannot perform subthreshold measurement because leakage through other rows and columns will overwhelm the desired current to be measured.

An I_{off} measurement method is proposed in this work to perform full I-V characterization, as shown in Figure 4-11. The required measurement is summarized below where I_i $(i = 1, 2, 3)$ represents for i^{th} total measurement current in Equation 4.1-4.3. (1) I_1 when $G_{on} = -0.15V$ and $G_{off} = -0.15V$; (2) I_2 when $G_{on} = 0V$ and $G_{off} = -0.15V$; and (3) I_3 when $G_{on} = 0V$ and $G_{off} = 0V$.

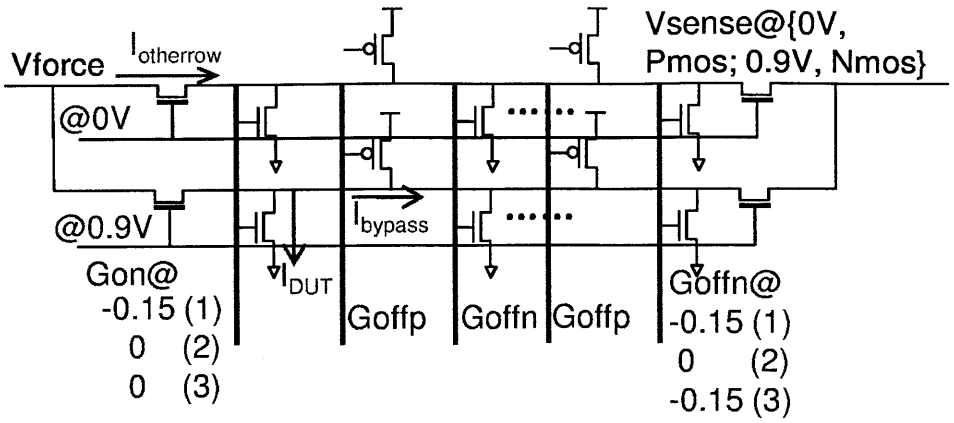

Figure 4-11: I_{off} calibration schematics.

$$I_1 = I_{DUT}(-0.15) + I_{bypass}(-0.15) + I_{otherrow}(-0.15) \tag{4.1}$$

$$I_2 = I_{DUT}(0) + I_{bypass}(0) + I_{otherrow}(0) \tag{4.2}$$

$$I_3 = I_{DUT}(0) + I_{bypass}(-0.15) + I_{otherrow}(-0.15) \tag{4.3}$$

To calculate I_{off}, some assumptions need to be made.

Assumption 1: $I_{pDUT} = 0$ when measuring nMOS DUT and $I_{nDUT} = 0$ when measuring pMOS DUT. This is because $V_{ds} = V_{gs} = 0$ in both cases.

Assumption 2:

$$\begin{aligned} A &= \frac{I_{DUT}(G_{on}=0) - I_{DUT}(G_{on}=-0.15)}{I_{DUT}(G_{on}=0)} \\ &= \frac{I_{bypass}(G_{offn}=0) - I_{bypass}(G_{offn}=-0.15)}{I_{bypass}(G_{offn}=0)} \\ &= \frac{I_{otherrow}(G_{offn}=0) - I_{otherrow}(G_{offn}=-0.15)}{I_{otherrow}(G_{offn}=0)} \end{aligned} \tag{4.4}$$

In Equation 4.4, A is a constant. Assumption 2 is reasonable because device characteristics for the same-sized transistors are similar. From assumptions 1 and 2, we can obtain the following equation:

$$\frac{I_2 - I(1)}{I_2} = A = I_{off} = \frac{I_{DUT}(0) - I_{DUT}(-0.15)}{I_{DUT}(0)} \tag{4.5}$$

$$I_{off} = I_{DUT}(0) = \frac{(I_3 - I_1)I_2}{(I_2 - I_1)} \tag{4.6}$$

Equation 4.6 is the final expression for I_{off}. This method can also be extended to calibrate subthreshold current, where all 0s are replaced by actual voltages in the measurement. The accuracy of this method is verified as shown in Table 1, where $I_{off}(cal)$ and $I_{off}(sim)$ represents the calculated and simulated I_{off}, respectively.

Table 4.1: Calculated and simulated I_{off} comparison

Array	I_1	I_2	I_3	$I_{off}(cal)$	$I_{off}(sim)$
NMOS	63.25nA	420.05nA	70.66nA	8.72nA	8.73nA
PMOS	88.9nA	512.68nA	97.73nA	10.67nA	10.6nA

4.4 Summary

In this chapter, we designed a test circuit for characterizing TSV-induced variation on devices and circuits. After motivating the need for a novel test circuit to characterize TSV-induced variation, we described the test circuit architecture and TSV effects on ring oscillators. A novel test circuit was designed using a scan chain approach combined with low-leakage and low-variation switches and Kelvin sensing connections, which provide access to full I-V characteristics in 290K DUTs. The RO test circuit contains a ring oscillator and peripheral control circuitry in each tile. A scan chain approach to select the DUT using an analog multiplexing circuit is also employed in this scheme to select an RO under test. Finally, detailed description of the test circuit operation was discussed.

Chapter 5

TSV Induced Variation Impact on Transistor Performance

In this chapter, a complete flow to analyze transistor characteristics and circuit performance under the influence of TSV stress is presented. The major contributions of this work are as follows:

- A realistic finite-element method simulation of single TSVs considering effects of the landing pad, SiO_2 liner and stress concentration.
- A linear superposition method to compute the stress profile caused by multiple TSVs on a full-chip scale.
- An accurate analytical model converting TSV stress into mobility and threshold voltage variation for nearby transistors which can then easily feed into post extraction netlists.
- An efficient algorithm for analyzing full chip circuit variation caused by TSV stress.
- Prediction of ring oscillator performance around TSVs at the 40nm node. The interaction between layout and circuit performance is predicted by the new stress models.

5.1 Motivation

5.1.1 Motivation for Characterization for TSV Stress

The process steps and physical presence of TSVs may introduce mechanical stress and further perturb the performance of nearby transistors and associated circuits. The stress in the silicon is introduced by the processing thermal profile due to the mismatch in thermal expansion coefficient (CTE) between the copper TSV (17.7 ppm/°C) and the surrounding silicon (3.05 ppm/°C) [9]. This mechanical stress can be decomposed in two directions, radial tension and tangential compression, as illustrated in Figure 5-1, and affects the carrier mobility and threshold voltage of the adjacent devices. These effects could cause timing violations for digital circuits or current mismatch for analog circuits.

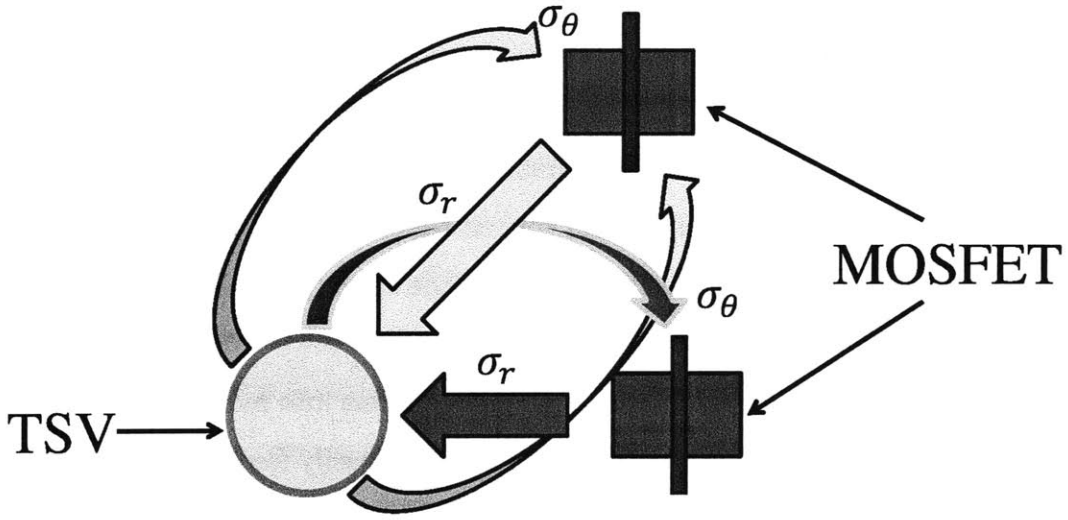

Figure 5-1: Stress pattern from TSV to transistors.

5.1.2 Prior Work

A few papers have reported methods to address TSV stress induced thermo-mechanical reliability or device mobility variation [22, 23, 26, 25]. Ref. [22] provides an analytical formulation for stress distribution around a TSV, referred to as the 2D *Lamé* stress solution. This model was further extended to TSV stress effects on mobility

to deal with timing issues in digital circuits [26]. Even though this model captures the ideal stress distribution in silicon bulk, it fails to consider an irregular shape of landing pad, liner, and effect of stress concentration at the silicon surface where the transistor channel is located. Finite element method (FEM) based device simulations have also been used to numerically analyze the thermo-mechanical stresses and device variation in 3D integrated structures [25]. However, it is often hard to extend this analysis to full chip circuit analysis due to large computing resources required. Recently, the principle of linear superposition of stress tensors against FEA simulations was validated to generate a reliability metric map on a full-chip scale [20]. However, the problem of how to accurately and efficiently characterize TSV stress impact on circuit performance on a full chip scale, especially how to represent this influence for circuit simulation, is still an open question.

5.2 Finite Element Analysis of TSV Structure

In this section, we calculate the single TSV induced stress distribution through FEM simulation and extend to multiple TSV stress analysis through linear superposition. An accurate stress contour is the basis for calculating mobility threshold voltage variation.

5.2.1 Baseline FEM Model for Isolated TSV

To study the thermal stress distribution of an isolated copper TSV with liner and landing pad, a finite element analysis is preformed using the commercial package, COMSOL. An axial symmetric property is assumed in this simulation. The critical process step conditions that we use for simulation of TSV stress are summarized in Table 5.1.

Our baseline TSV process mimics the via middle technology in 3D IC manufacturing. Wafer direction is selected to be (100)/ $\langle 110 \rangle$ and CMOS transistors are located at the silicon surface. TSVs are etched with a depth of $50\mu m$ and a $6\mu m$ diameter.

Table 5.1: Summary of TSV process step conditions.

	Process Step	Temperature($°C$)
1	TEOS liner deposition	400
2	Ta barrier layer deposition	375
3	Cu electroplating	25
4	Annealing	175
5	Cooling	25

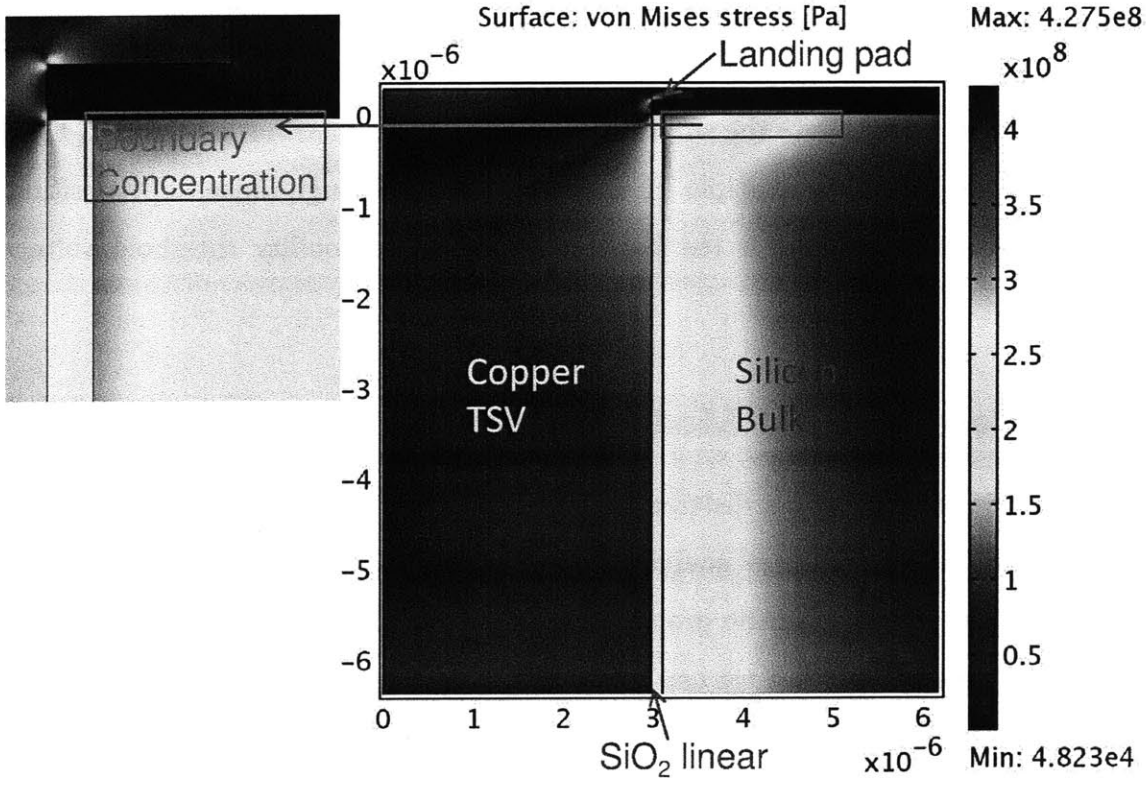

Figure 5-2: Von Mises stress distribution around the TSV.

A $200nm$ thick oxide liner is deposited using TEOS CVD and a $5nm$ Ta barrier is fabricated with PVD Ta. Then the copper TSV is electroplated and annealed subsequently. A CMP process is introduced after a $7\mu m$ landing pad is electroplated. In order to isolate stress contributed by the TSV, both shallow trench isolation (STI) and contact etch stop layer (CESL) structure are not included in this simulation. Material properties used for our experiments are as follows: thermal expansion coefficient ($ppm/°C$): α_{Cu}=17.7, α_{Si}=3.05, and α_{SiO_2}=0.5; Young's modulus (GPa): E_{Cu}=70, E_{Si}= 130, and E_{SiO_2}=70; Poisson ratio: ν_{Cu}=0.34, ν_{Si}= 0.28, and ν_{SiO_2}=0.17.

Figure 5-2 shows the FEA results for von Mises stress distribution around the TSV. We find that the stress concentration can make the stress at the silicon surface larger than in the silicon bulk. Since the TSV structure is axial symmetric and silicon is assumed to be isotropic, we adopt a cylindrical coordinate system in the first step and then convert the tensor matrix into a Cartesian coordinate system. In our simulation, the normal stress σ_r and σ_ϕ are two major components in the stress distribution, as shown in Figure 5-1. We further compare normal stress distribution at silicon surface and silicon bulk, both of which are from FEM result, with 2D *Lamé* solution, as shown Figure 5-3. It shows that while the *Lamé* solution matches well with the silicon bulk case, it does not capture the irregular characteristics of TSV surface stress distribution correctly, especially for the near-TSV region.

5.2.2 Multiple TSV Stress Contour

While FEM gives a very accurate axial symmetric distribution of stress around a single TSV, we cannot perform this kind of "exact" simulation on a full chip scale since FEM is too computationally costly to apply to large areas with complex TSV layout patterns. However, we do have a solution to analyze stress distribution with multiple TSVs in full chip scale because the baseline TSV structure is highly repeatable and the stress tensor is linear superposable within the stress scope generated by TSVs [20]. Before doing this, we need to convert the cylindrical coordinate tensor $\hat{T}_{r\phi z}$ to a Cartesian coordinate system tensor $\hat{T}_{[110]}$ with three axes at [110], [1$\bar{1}$0], and [001], respectively according to transistors channel direction. The method is discussed in

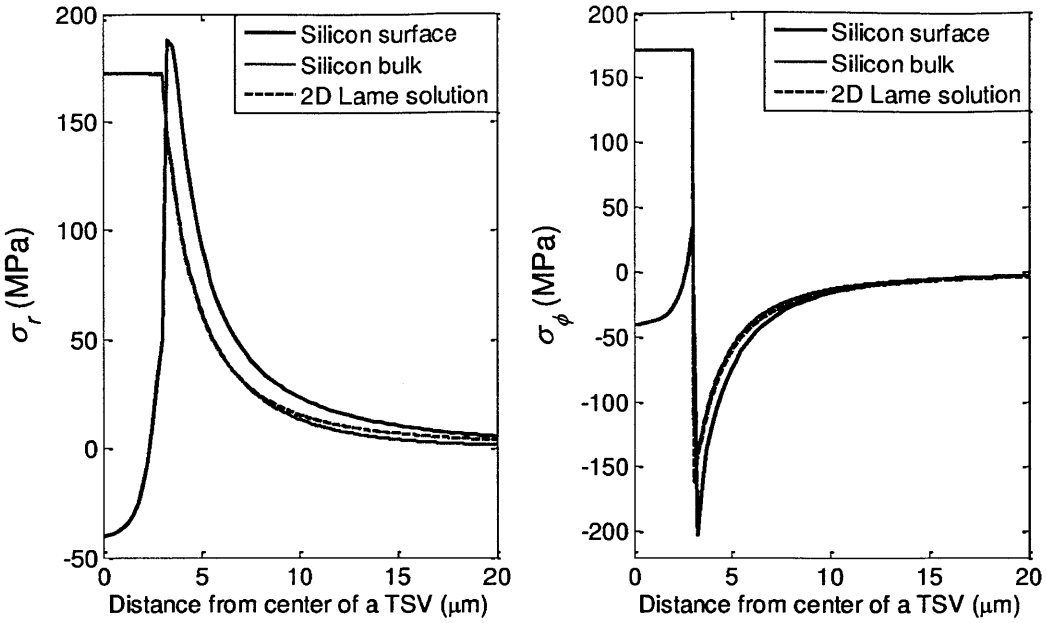

Figure 5-3: TSV stress effect on σ_r and σ_ϕ.

Appendix A where ϕ is the angle between the x-axis and a line from the TSV center to the simulation point and $\theta = 0°$. Figure 5-4 shows a single TSV stress contour for σ_{xx} and σ_{yy} after the coordinate transformation. Then we can puse alinear superposition method at any point needed by adding up the stress tensors of different TSVs within $25\mu m$.

5.3 Mobility and Threshold Voltage Variation Related to TSV Stress

With the FEM simulation result and superposition method, we obtain an accurate channel stress tensor for each transistor. To estimate $\Delta\mu/\mu$ and $\Delta V_{th}/V_{th}$ as a function of stress applied to a MOSFET with respect to its unstressed condition, we will further develop the corresponding variation model combining linear piezoresistance theory and energy calculation. This model is also verified using published device simulation results.

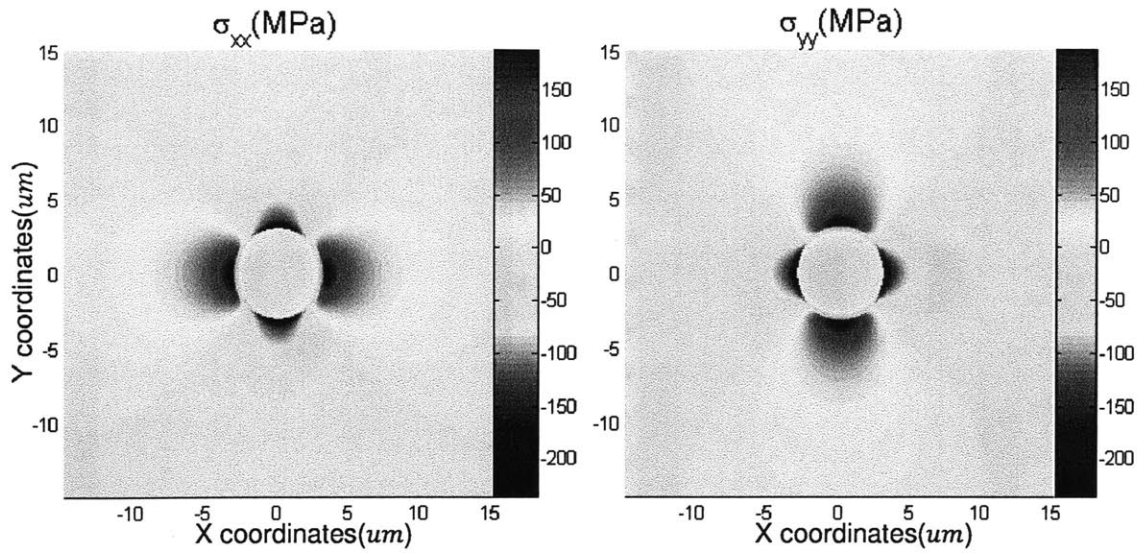

Figure 5-4: σ_{xx} and σ_{yy} contours.

5.3.1 Mobility Variation Modeling

Mobility variation, which corresponds to drive current and transistor speed, is one of the most critical consequences induced by TSV stress. A linear piezoresistance model is the most widely employed model to depict this effect [27]. The validity of the model is verified with coefficients taken either from measurements or from calculations [28]. Although this approach is inaccurate for predicting mobility variation at high levels of stress (normally $\sigma \leq 1$ GPa) [28], it fits well with our purpose to model mobility variation induced by TSVs, which is normally below 200 MPa stress. Since our coordinate system already corresponds with the transistor channels, we use the following equation to express mobility changes:

$$\Delta\mu/\mu = \Pi_L \cdot \sigma_{xx} + \Pi_T \cdot \sigma_{yy} \tag{5.1}$$

Here Π_L and Π_T represent longitudinal and transverse piezoresistance coefficients for (100)/ $\langle 110 \rangle$. Note that these coefficients should take account of effects contributed by channel doping because this would cause quantization splitting and alters the conductivity mass [29].

Simulated mobility contours for nMOS and pMOS transistors are compared in

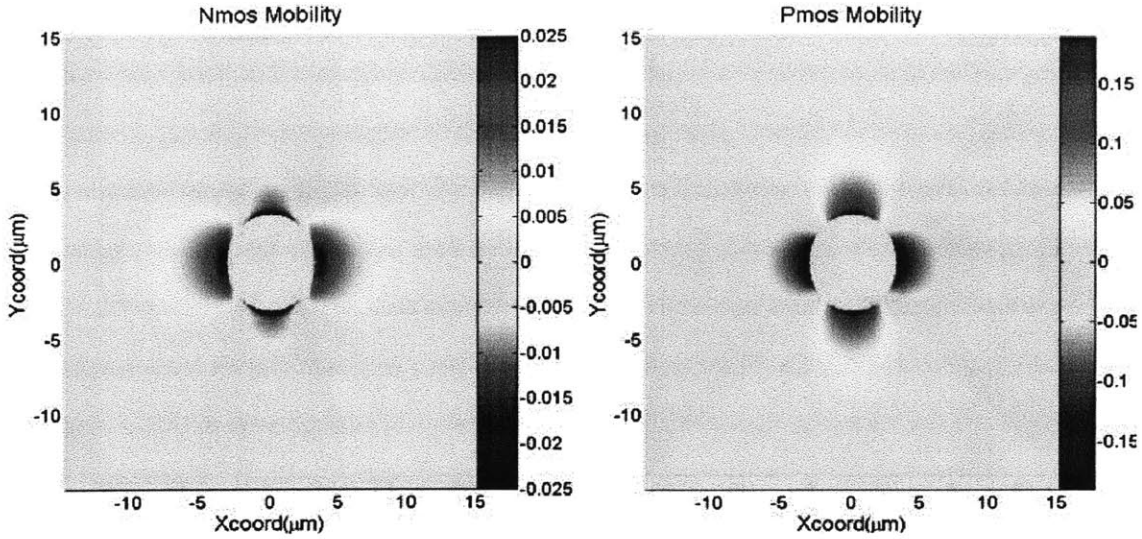

Figure 5-5: Comparison between nMOS and pMOS mobility percentage variation maps.

Figure 5-5. nMOS transistors are almost immune from TSV stress because n-channel piezoresistance coefficient Π_L and Π_T have the same sign and the two items in Equation 5.1 counteract each other. The pMOS transistors, on the other side, suffer more from the different sign of p-channel piezoresistance coefficients Π_L and Π_T, and the two items reinforce. In addition, mobility is immune from TSV stress in the diagonal direction because shear stress does not contributed to mobility change. This property can be further exploited to optimize TSV and transistor layout configurations, as discussed in Section 5.4.2.

The accuracy of FEM based stress and mobility model are validated by 3D FEM device simulation [10], as shown in Figure 5-6. The mobility variation predicted by the 2D *Lamé* solution is also compared in the same figure. Although the *Lamé* solution captures the general trend of mobility variation, it could still cause maximum error of approximately 3% of the total mobility.

5.3.2 Threshold Voltage Variation Modeling

Threshold voltage is also significantly affected by TSV stress because strain can induce shifts and splits in both conduction and valence bands. However, there is no intuitive

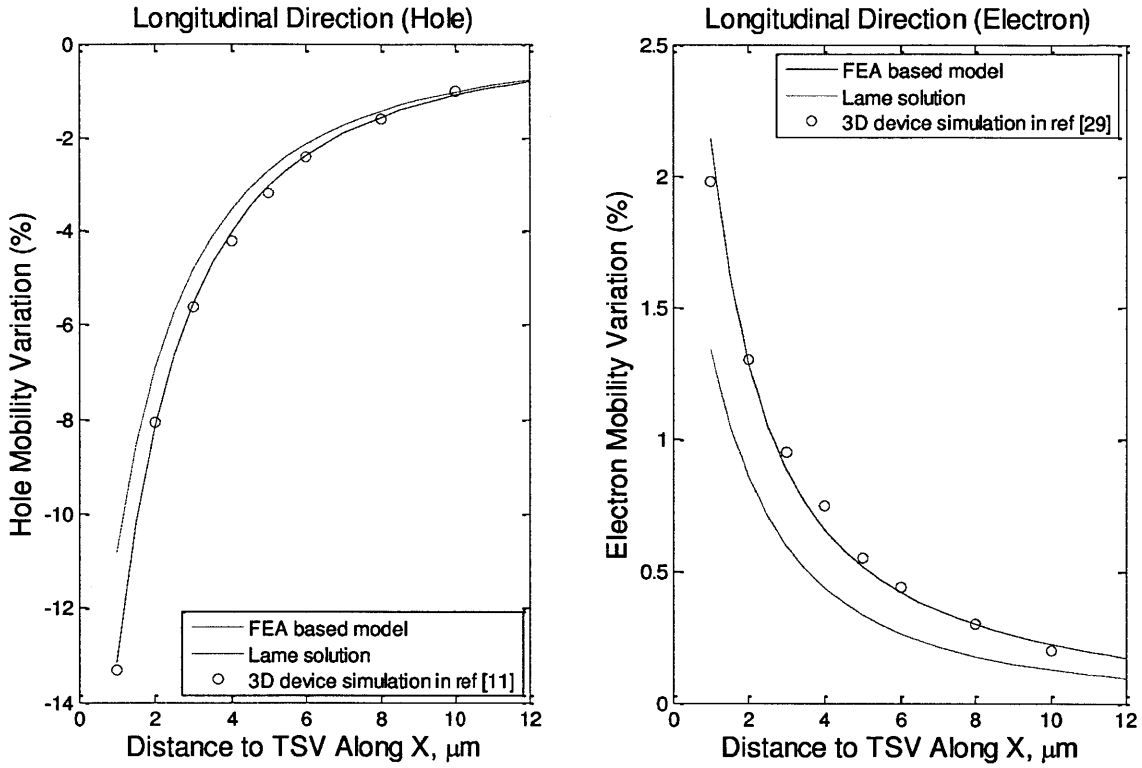

Figure 5-6: Variation of the mobility versus distance to TSV, comparing our FEA based model and the approximate *Lamé* solution to 3D device simulation from [10].

way in piezoresistance theory to depict this effect through coefficients from direct measurement. Therefore we utilize deformation potential theory to calculate the impact of TSV stress on threshold voltage. For the first time, the impact of TSV stress on threshold voltage is estimated.

Since strain is the direct cause of energy splitting, we need to convert stress tensor from current coordinates $\hat{T}_{[110]}$ into crystallographic coordinate tensor $\hat{T}$ using the method discussed in Appendix A, where $\phi = 45°$ and $\theta = 0°$. Then stress is transformed into strain according to Appendix B.

After that, the hydrostatic shift and shear splitting of the valence band ΔE_V and conduction band ΔE_C edges can be calculated through the following equations [11]:

$$\Delta E_C^{(i)}(\sigma) = \Xi_d(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + \Xi_u \varepsilon_i \tag{5.2}$$

$$\Delta E_V(\sigma) = a(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + [b^2(\varepsilon_2 - \varepsilon_3)^2 + d^2\varepsilon_6^2/4]^{1/2} \tag{5.3}$$

Table 5.2: Band edge deformation potential constants [11].

	Ξ_d	Ξ_u	a	b	d
Deformation potential constants (eV)	1.13	9.16	2.46	-2.35	-5.08

In Equation 5.2 and 5.3, the hydrostatic term (with parameters Ξ_d and a) takes account of the band edge shift without change in degeneracy, and the shear term (including parameters Ξ_u, b and d) split the valence and conduction band states. The deformation potential constants are summarized in Table 5.2.

With both ΔE_C and ΔE_V, the expression for the strain-induced threshold-voltage shifts becomes [30]:

$$\Delta V_{thn}(\sigma) = -m\Delta E_C + (m-1)\Delta E_V \tag{5.4}$$

$$\Delta V_{thn}(\sigma) = (m-1)\Delta E_C - m\Delta E_V \tag{5.5}$$

where m is the body-effect coefficient.

Simulated threshold voltage variatfion contours for nMOS and pMOS are shown

in Figure 5-7, where x and y axes represent [110], [1$\bar{1}$0], respectively. Because of the biaxial property of TSV stress, the threshold voltage shift is greatly reduced. Therefore the stress effect on threshold voltage is much less than uniaxial stress reported elsewhere [11]. In addition, the ΔV_{th} contour is almost axisymmetric, but the axial direction is more affected because the shear term also contributes to ΔV_{th}. However, considering that the threshold voltage in advanced technology nodes is around 100 mV, the variation induced by TSV stress amounts to 8% of the total threshold voltage, which should not be neglected.

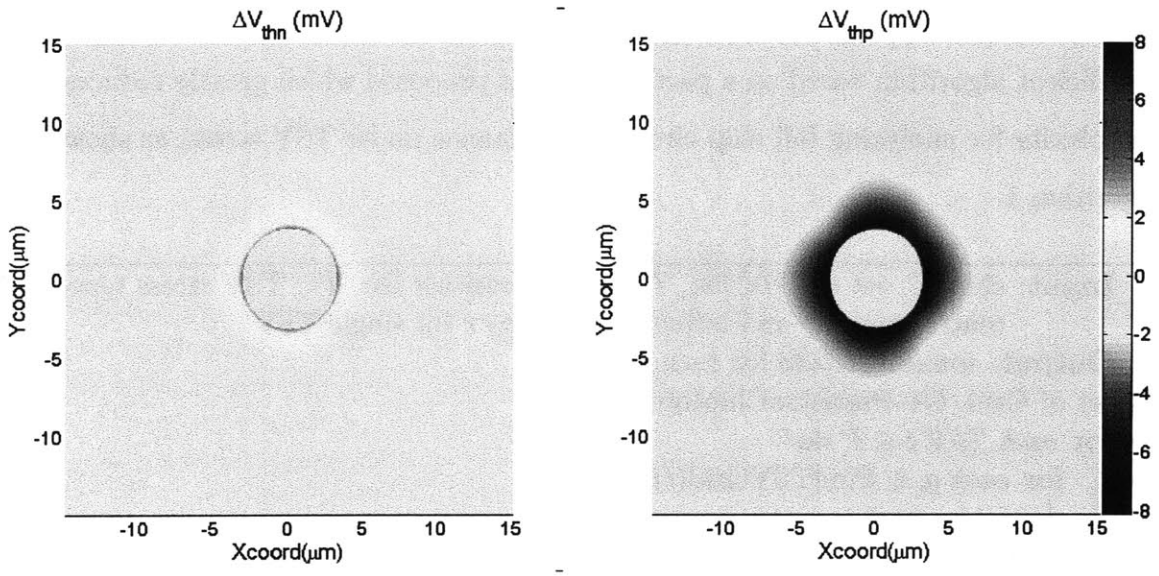

Figure 5-7: Comparison between nMOS and pMOS V_{th} variation maps.

5.4 Analysis and Optimization of Circuit Considering TSV Stress Effects

The changes in transistor characteristics due to TSV stress alters circuit performance around TSVs. While the existing work has focused on timing analysis of digital circuits [26], we propose here a more comprehensive flow to characterize circuit variation in both analog and digital circuits.

5.4.1 Stress Aware Circuit Analysis

As noted above, TSV stress-induced transistor variation is determined by: (1) the separation between the TSV and the transistor, and (2) the angle between the x-axis and a line from the TSV center to the transistor. With LVS extraction results, this information can be obtained and a full chip analysis is possible. Though the author in [20] achieved a full chip stress simulation, the complexity is proportional to the number of full chip simulation points, which requires large memory resources. Because our purpose is to analyze transistor performance under TSV stress, there is no need to generate the stress tensor for each point in the full chip. In this work, an efficient algorithm based on a partition grid is proposed which greatly reduces the complexity for analyzing full chip circuit performance under TSV stress, as shown in algorithm 1.

Input: chip, C; set of TSV list, T; set of transistor list, Tr; TSV stress tensor matrix map M and influence distance r for single TSV
Output: *umulu*0,*delvto* for each $tr \in Tr$

```
1  set of Grid, G←PartitionChipIntoGrid(C);
2  for each TSV t ∈ T do
3  |  for each g_i ∈ FindTSVGrid(t) do
4  |  |  g_i.t ← t
5  |  end
6  end
7  for each transistor tr ∈ Tr do
8  |  g ←FindTransistorGrid(tr);
9  |  for each TSV t' ∈ g do
10 |  |  if Distance(t',tr)< r then
11 |  |  |  tr.stress += FindAvgStressTensor(t', tr, M);
12 |  |  end
13 |  end
14 |  tr.umulu0 += ComputeMuVar(tr.stress);
15 |  tr.strain ← CovertStressToStrain(tr.stress);
16 |  tr.delvto += ComputeVthVar(tr.stress);
17 end
```

Algorithm 1: Full chip stress aware circuit analysis.

This flow: (1) reads the geometrical and coordinate information of transistors and TSVs; (2) partitions the chip into $75\mu m \times 75\mu m$ grids and categorize each TSV

into grids within its influence zone; (3) categorizes each transistor into a particular grid and generates its stress by superposition of TSV stress within the same grid; (4) calculates the amount of variation in transistor characteristics using out TSV stress variation models; and (5) outputs a SPICE netlist reflecting the calculation results. In the SPICE netlist, the characteristic variations are specified with MULU0 and DELVTO. Then the impact of these variations can be considered by performing a SPICE simulation using the SPICE netlist. The complexity of this variation extraction algorithm is $O(n)$, where n is the number of transistors.

5.4.2 TSV Placement Optimization

After a full chip analysis, we are able to further optimize TSV placement and reduce the impact of TSVs on transistors.

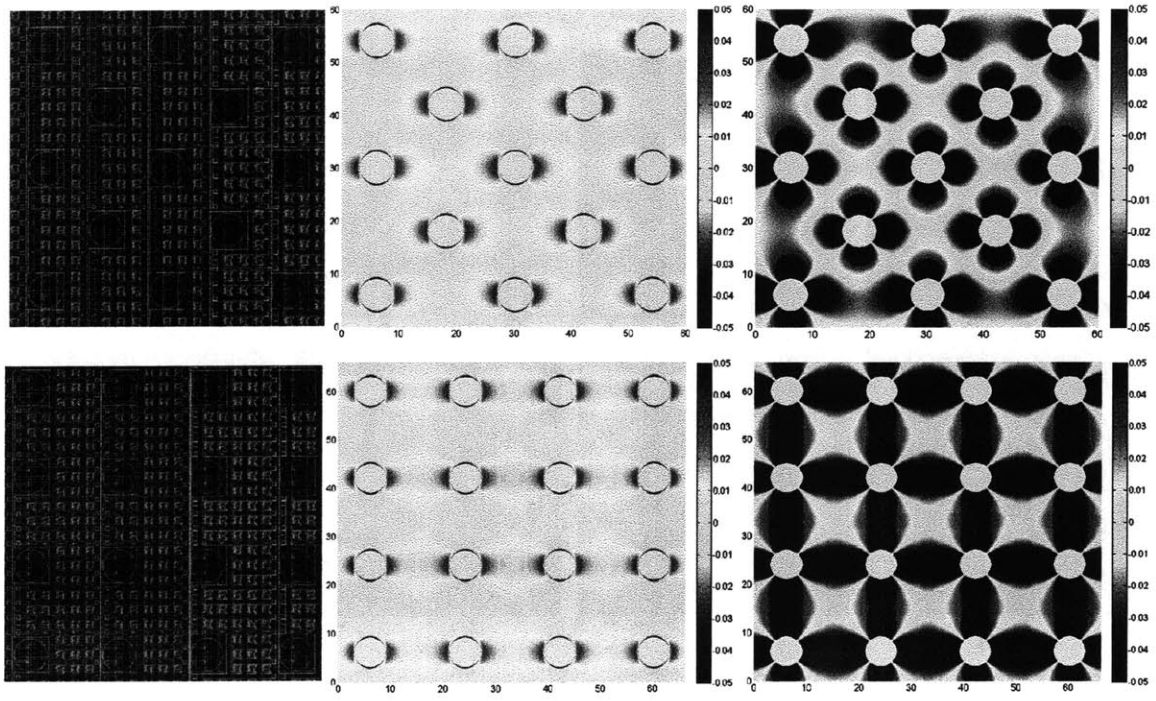

Figure 5-8: Comparison between TSV "diamond" matrix and "square" matrix for realistic layout (left), and the resulting electron (middle) and hole (right) mobility variation contours.

As an example, we first compare mobility variation between "diamond" and "square" TSV layout patterns with the same TSV density, as shown in Fig 5-8.

The TSV pitch (minimum TSV distance) in both TSV configurations are selected to be $18\mu m$, which is a typical distance between TSVs in 3D IC chips. In square configuration, the interaction between neighboring TSV intensifies the mobility variation, while in diamond configuration the interaction between neighboring TSVs cancels the mobility variation. Since TSVs have an almost opposite impact on x and y axis for pMOS transistors, the crossover area is less affected by TSV stress.

To further investigate the effect of TSV layout pattern on nearby circuits, a Keep-Out-Zone (KOZ) is defined as an area where transistor mobility variation is larger than a certain limit. In this example, a criterion for KOZ is set as 0.5% and 5% variation of total mobilities for analog and digital MOSFETs, respectively. Fig 5-9 shows the comparison for analog KOZ and allowable layout area between different TSV patterns and pitches, where green area represents allowable layout area and red area represents the KOZ.

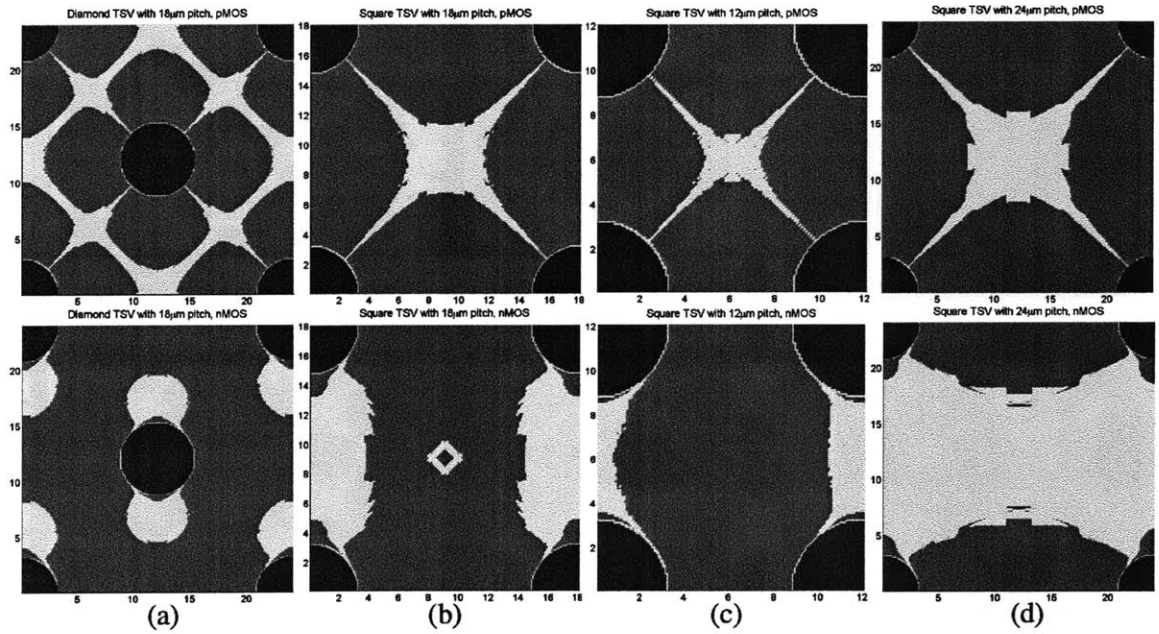

Figure 5-9: nMOS and pMOS "unit cell" comparison for analog KOZ and allowable area between: (a) "diamond" TSV with 18 μm pitch; (b) "square" TSV with 18 μm pitch; (c) "square" TSV with 12 μm pitch; and (d) "square" TSV with 24 μm pitch.

The percentage of allowable layout area for analog and digital circuits with different TSV patterns are summarized in Table 5.3. As discussed earlier, pMOS transistors are significantly affected by TSV stress and nMOS digital transistors are almost im-

Table 5.3: Allowable layout area for digital circuits.

	Analog or Digital	TSV pitch (μm)	TSV pattern	nMOS area	pMOS area
1	Digital	18	Diamond	89.05%	65.61%
2	Digital	18	Square	90.67%	50.49%
3	Digital	12	Square	77.99%	28.38%
4	Digital	24	Square	94.41%	78.21%
5	Analog	18	Diamond	15.22%	17.87%
6	Analog	18	square	25.32%	10.31%
7	Analog	12	square	12.25%	5.99%
8	Analog	24	square	58.45%	15.13%

mune from TSV stress. However, an interesting result appears that analog nMOS transistor are also strongly influenced by TSV arrays. This is mainly because TSV stress has more impact on longitudinal direction than transverse direction, and this effect is increased by parallel TSVs. We may also observe that "diamond" TSV pattern benefits pMOS transistor in both analog and digital with 7.56% and 15.12% more allowable layout area. However, this configuration also greatly reduces digital nMOSFET layout area to 15.22%, which is comparable to pMOS case. In summary, the "diamond" TSV pattern provides more balanced layout area for nMOSFETs and pMOSFETs compared with the "square" pattern.

5.4.3 Circuit Performance Analysis: Ring Oscillators Around a TSV

While the previous case study is about how multiple TSVs affect one transistor, in this part we analyze how a single TSV affects the performance of a circuit that is an aggregate of many transistors. We use realistic 17-stage ring oscillators (ROs) designed in 40 nm CMOS technology to show TSV stress impact on RO frequency using the proposed model. Sixteen groups of RO devices under test (DUTs) around a TSV are designed to characterize the TSV's influence in various locations, as shown in Figure 5-10. The surrounding area around each group of ROs is carefully designed to cancel out other systematic variations.

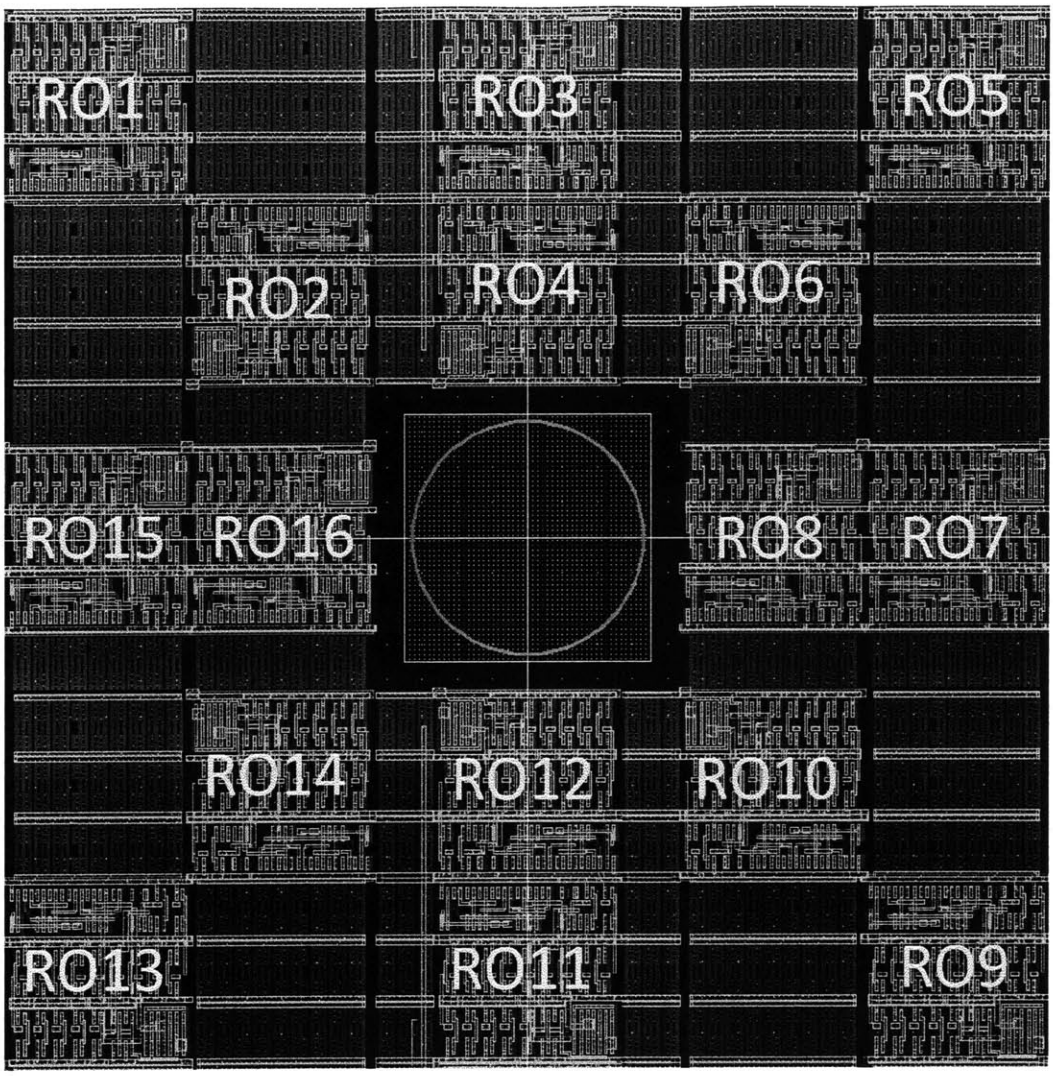

Figure 5-10: Layout of TSV and the sixteen 17-stage ring oscillator groups.

We first generate transient waveforms of all 16 ROs, as shown in Figure 5-11. Because the ratio of carrier velocity change to mobility change $\Delta v/\Delta\mu$ tends to saturate in advanced technologies, the TSV stress does not bring significant change to circuit delay ($\approx 2\%$).

Figure 5-12 further shows how RO frequency changes according to their geometric relation with TSV. While we see that most RO groups in the diagonal direction are not affected, the 4^{th} and 12^{th} RO groups become slower, and the 8^{th} and 16^{th} RO groups become faster. This is because TSV stress on pMOS is more evident than that on nMOS.

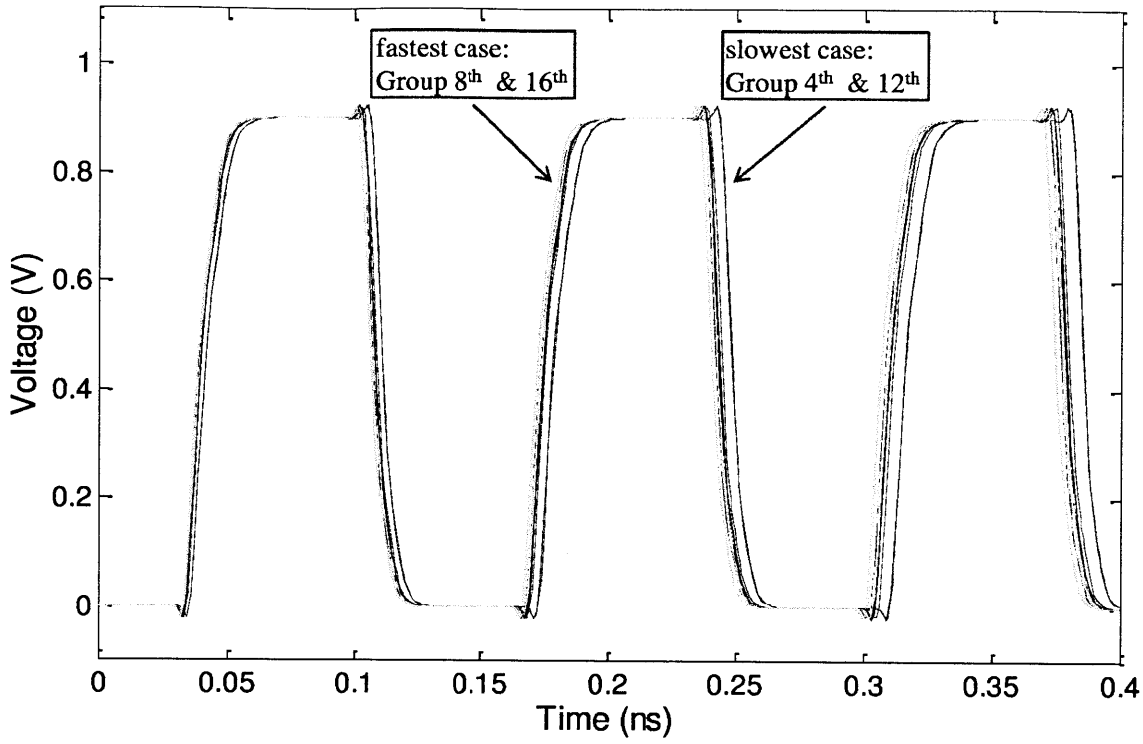

Figure 5-11: RO waveforms for sixteen different 17-stage ring oscillators.

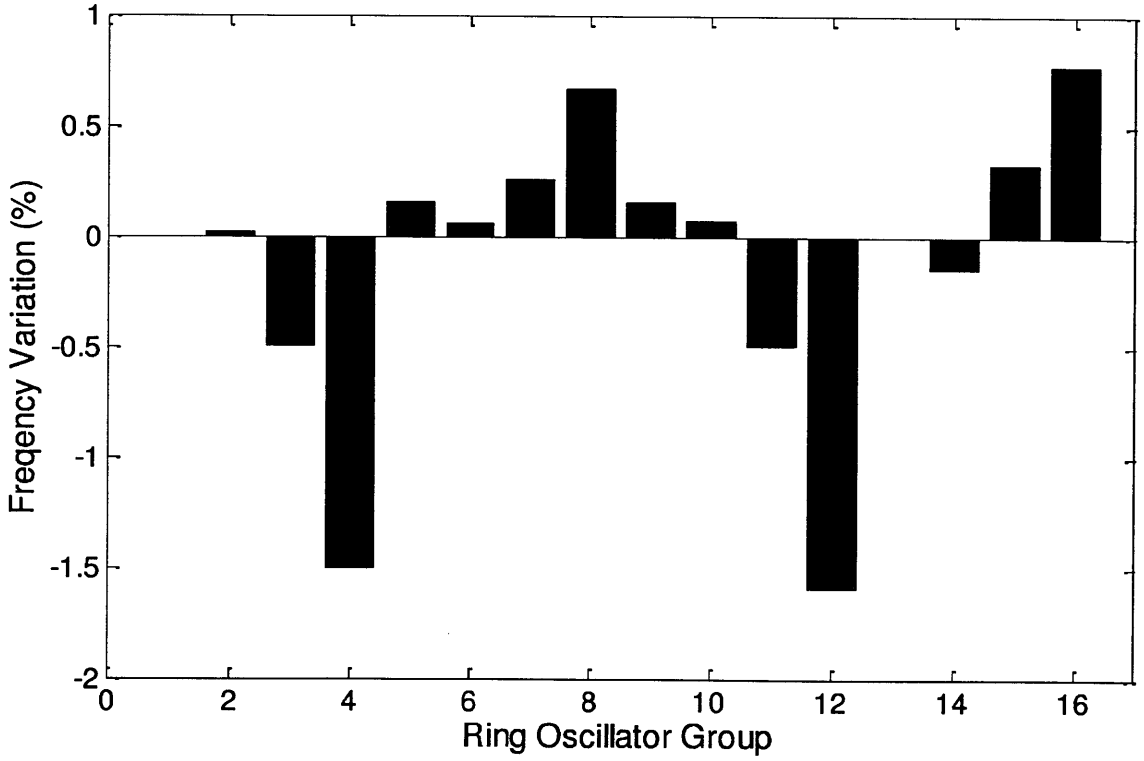

Figure 5-12: Frequency variations of the sixteen ring oscillator groups.

5.5 Summary

In this chapter, a complete flow for analyzing circuit performance under the impact of TSV stress was proposed. At the stress characterization level, we showed how a realistic TSV process and structure affects stress distribution, and showed how to convert the FEM stress model into a stress tensor matrix. At the device modeling level, we proposed a fast and accurate model to capture TSV stress induced variation on mobility and threshold voltage. At the circuit level, we proposed a fast and efficient full chip extraction flow to combine our model with commercial circuit simulation tools. Optimization of TSV layout pattern and a case study of ring oscillators around TSVs was also presented, to illustrate our proposed flow and methodology.

Chapter 6

Thesis Summary and Future Work

This thesis has demonstrated the need for a novel test circuit and an accurate model to study the systematic variation due to TSV induced stress and its interaction with polysilicon and shallow-trench-isolation (STI) layout pattern density. Beginning with the introduction of 3D ICs and TSVs, we were able to show the motivation for studying TSV-induced thermal stress on transistor performance, and the need for a physically-based variation-aware model relating TSVs to devices. A new test structure to explore a range of TSV and device layout choices, and a new test circuit to measure full I-V curves were designed for this purpose. Then we moved to the modeling side to provide a physically based model to characterize TSV induced variation. This concluding chapter summarizes this thesis and presents ideas for future work, since despite the many advances in understanding of TSV induced variation, there is still much room for improvement.

6.1 Thesis Summary

As continued scaling becomes increasingly difficult, 3D integration has emerged as a viable solution to achieve higher bandwidth and power efficiency. A summary of benefits of 3D ICs and key process steps involved in its fabrication, particularly relating to the through silicon vias (TSVs), was discussed in Chapter 2. The process steps and physical presence of TSVs, however, may generate a stress-induced thermal

mismatch between TSVs and the silicon bulk. These effects could further perturb the performance of nearby electronic structures, particularly transistors, diodes, and associated circuits. The central focus of this work is to understand variation induced by TSV stress. We illustrated that though there are published resultsin this area, a comprehensive understanding for TSV stress induced variation is still needed. This includes the need for both carefully designed characterization structures and a realistic model supported by theoretical analysis. Figure 6-1 below summarizes the flow of this thesis.

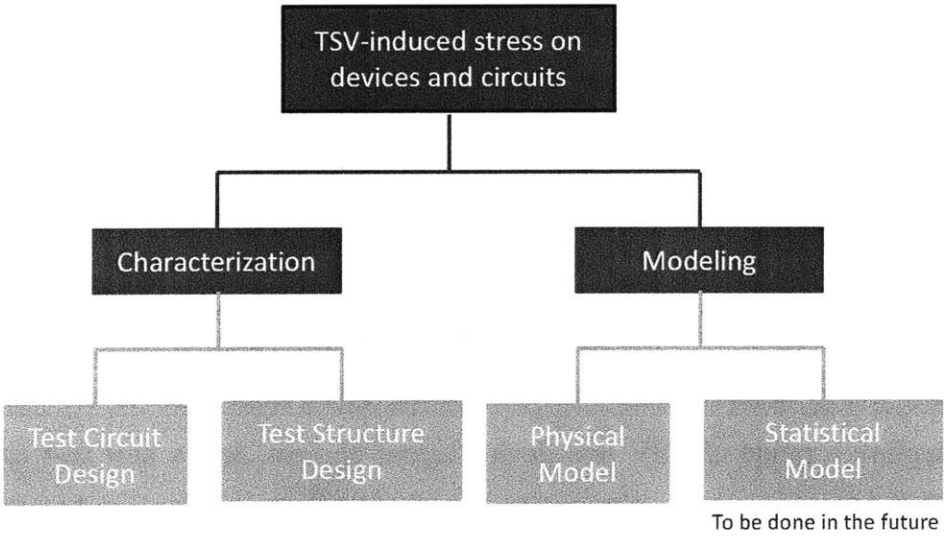

Figure 6-1: Thesis summary.

Our efforts in dealing with TSV-induced variation are divided into two approaches: characterization and modeling. For the characterization approach, both a new test structure and a new test circuit have been designed to feed the need for comprehensively studying the effects of TSV-induced variation on transistor and circuit performance. For the modeling approach, a complete flow and methodology based on a physical stress and device model to analyze transistor characteristics and circuit performance under the influence of TSV stress was proposed. With the flow, we were able to simulate TSV-induced circuit variation accurately and efficiently in standard EDA tools such as HSPICE.

In Chapter 3, test structures which provide measurements of key parameters of

large numbers of devices under test (DUTs) were discussed. These DUTs have layouts whose environments are comprised of a range of TSV and device layout choices with enough variety to enable quantitative understanding of the variation mechanisms and further model them in simulation tools. Specifically, a radius sampling scheme to characterize the transistor variation when TSV-to-transistor distances and angles are different was introduced. In macro-layout design, test structures were designed to explore the interaction between TSV density and other layout pattern densities such as that of polysilicon and shallow trench isolation (STI).

In Chapter 4, we discussed our test circuit design. A test circuit was designed to perform the measurement on the test structure described in the previous chapter. An overview of relevant test circuits which characterize variations was presented. A novel test circuit with the capability to access 290K DUTs with full I-V characteristics was designed. The test circuit uses a scan chain approach combined with low-leakage and low-variation switches and Kelvin sensing connections, which provide access to detailed analog device characteristics in large arrays of test devices. An I_{off} measurement technique is implemented which is compatible with off-chip wafer probe testing. Circuit simulations show that the proposed multiplexing approach is very accurate, with an error less than 0.1% in measured current. Another test circuit based on RO frequency characterization was designed to characterize TSV-induced variation on digital circuits. Each RO tile contains a ring oscillator and peripheral control circuitry. A scan chain approach to select the DUT in analog multiplexing circuit is also employed in this scheme to select an RO under test. A group of frequency dividers follow the output RO bus to divide the frequency into the megahertz range.

In Chapter 5, a complete flow and methodology to analyze transistor characteristics and circuit performance under the influence of TSV stress was presented. The thermal stress contour near the silicon surface with single and multiple TSVs through finite element method (FEM) simulation was analyzed. Realistic TSV structure and processes was adopted. The biaxial stress profile was then converted to mobility and threshold voltage variations depending on transistor type and geometric relation between TSVs and transistors. Next, we proposed an efficient algorithm to calculate full

chip circuit variation corresponding to TSV stress based on a grid partition approach. A TSV pattern optimization strategy and a series of 17-stage ring oscillators using 40 nm CMOS technology was also employed as a test case for the proposed approach.

The future goals of this project, following fabrication of our test chips, are to (1) extract the maximum range TSV affects, (2) develop a statistical model based on the results collected from the test chip, and (3) calibrate the measurement result with the physical model described in Chapter 5.

6.2 Future Work

In addition to measuring the transistors, and extracting the parameter variation upon successful chip fabrication, other future work might help us improve the understanding of TSV induced variation.

6.2.1 Virtual Source Velocity Modeling

In this thesis, we proposed a physically based transistor model to characterize TSV-induced variation. As a result, the characteristic variations are specified with MULU0 and DELVTO, which are changes of mobility and threshold voltage, in the BSIM4 model. While mobility is an accurate indicator for performance of long channel devices, it fails to depict the physical nature of short channel devices. In other words, mobility is more like a fitting parameter rather than a parameter with physical meaning in advanced technologies. Instead, virtual source velocity, the velocity of carriers located in the MOSFET channel at the top of the barrier near the source (virtual source), is a key parameter which could bridge stress to transistor performance. Surprisingly, however, no analysis on the variation of carrier velocity has been reported. For better understanding of TSV induced variation, a detailed virtual source velocity variation model and entire corresponding simulation flow are needed.

6.2.2 TSV Compact Modeling

In this thesis, we analyzed the systematic variation due to thermal mismatch between TSV structures and silicon. The TSV structure itself, however, may also generate parasitics which affect circuit performance. In order to characterize this effect, accurate closed-form models of the TSV impedance which provide an efficient method to characterize the performance of signal paths containing TSVs are needed. These closed-form expressions for the resistance, inductance, and capacitance of TSVs, should account for via length, via diameter, dielectric thickness, and fill material, as well as their variations. To be compatible with SPICE simulators, these models should also be independent of operating frequency. With these models, we would be able to obtain a delay metric incorporating AC parameters, such as parasitic capacitance, resistance and inductance.

Appendix A

Stress Tensor Coordinate Transformation

In this section we summarize how the stress tensor is transformed between different coordinate systems. Consider a generalized direction $[x', y', z']$ in which the stress is applied. The stress in the coordinate system $[x, y, z]$ can be calculated using the transformation matrix U

$$U(\theta, \phi) = \begin{bmatrix} \cos\theta\cos\phi & \cos\theta\sin\phi & -\sin\theta \\ -\sin\phi & \cos\phi & 0 \\ \sin\theta\cos\phi & \sin\theta\sin\phi & \cos\theta \end{bmatrix} \tag{A.1}$$

Here θ denotes the polar and ϕ the azimuthal angle of the stress direction relative to the new coordinate system. The stress in the new coordinate system is then given by

$$\hat{T}^{new} = U \cdot \hat{T} \cdot U^T \tag{A.2}$$

Appendix B

Stress-Strain Relationship

Here we summarize the transformation between stress and strain.

$$\begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{12} & 0 & 0 & 0 \\ s_{12} & s_{11} & s_{12} & 0 & 0 & 0 \\ s_{12} & s_{12} & s_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{44} \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} \tag{B.1}$$

In Equation B.1, the transformation matrix is the tensor of elastic stiffness for silicon. Here $\varepsilon_i (i = 1, 2, 3)$ is normal strain component and $\varepsilon_i (i = 4, 5, 6)$ is shear strain component. $\sigma_i (i = xx, yy, zz)$ is normal stress component and $\sigma_i (i = xy, yz, zx)$ is shear stress component. $s_i (i = 11, 12, 44)$ are parameters in transformation matrix.

Bibliography

[1] M. Scannell, "3d activities and roadmap," in *EMC-3D European Technical Symposium*, 2007.

[2] D. M. Jang, C. Ryu, K. Y. Lee, B. H. Cho, J. Kim, T. S. Oh, W. J. Lee, and J. Yu, "Development and evaluation of [3-d sip."

[3] J. Yannou, "3DIC and TSV interconnects 2010," Yole Development, Tech. Rep., 2010.

[4] D. Chen, W. Chiou, M. Chen, T. Wang, K. Ching, H. Tu, W. Wu, C. Yu, K. Yang, H. Chang, M. Tseng, C. Hsiao, Y. Lu, H. Hu, Y. Lin, C. Hsu, W. Shue, and C. Yu, "Enabling 3D-IC foundry technologies for 28 nm node and beyond: through-silicon-via integration with high throughput die-to-wafer stacking," in *IEEE International Electron Devices Meeting*, Dec. 2009, pp. 14.3.1–14.3.4.

[5] J. Kawa, "TSV stress management," tutorial at *Design Automation and Test in Europe*, 2010.

[6] K. Gettings and D. Boning, "Study of CMOS process variation by multiplexing analog characteristics," *IEEE Transactions on Semiconductor Manufacturing*, vol. 21, no. 4, pp. 513–525, 2008.

[7] N. Drego, A. Chandrakasan, and D. Boning, "Lack of spatial correlation in MOSFET threshold voltage variation and implications for voltage scaling," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, no. 2, pp. 245–255, May 2009.

[8] A. Chang, "A test structure for the measurement and characterization of layout-induced transistor variation," Master's thesis, Massachusetts Institute of Technology, 2009.

[9] A. Mercha, A. Redolfi, M. Stucchi, N. Minas, J. Van Olmen, S. Thangaraju, D. Velenis, S. Domae, Y. Yang, G. Katti, R. Labie, C. Okoro, M. Zhao, P. Asimakopoulos, I. De Wolf, T. Chiarella, T. Schram, E. Rohr, A. Van Ammel, A. Jourdain, W. Ruythooren, S. Armini, A. Radisic, H. Philipsen, N. Heylen, M. Kostermans, P. Jaenen, E. Sleeckx, D. Sabuncuoglu Tezcan, I. Debusschere, P. Soussan, D. Perry, G. Van der Plas, J. Cho, P. Marchal, Y. Travaly, E. Beyne,

S. Biesemans, and B. Swinnen, "Impact of thinning and through silicon via proximity on high-k / metal gate first CMOS performance," *IEEE VLSI Technology Symposium*, pp. 109–110, 2010.

[10] V. Moroz, "The impact of TSV arrays on transistor performance," *IEEE Workshop on Variability Modeling and Characterization*, 2010.

[11] J.-S. Lim, S. Thompson, and J. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 11, pp. 731–733, 2004.

[12] G. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 2, pp. 82–85, Jan. 1998.

[13] N. Magen and A. Kolodny, "Interconnect-power dissipation in a microprocessor," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, pp. 7–13, 2004.

[14] S. Gu, P. Marchal, M. Facchini, F. Wang, M. Suh, D. Lisk, and M. Nowak, "Stackable memory of 3D chip integration for mobile applications," *IEEE International Electron Devices Meeting*, pp. 33.4.1–33.4.4, 2008.

[15] P. Leduc, "What is 3D IC integration and what metrology is needed," in *Conference on Frontiers of Characterization and Metrology for Nanoelectronics*, Mar. 2007.

[16] S. Das, A. Chandrakasan, and R. Reif, "Timing, energy, and thermal performance of three-dimensional integrated circuits," in *Proc. Great Lakes Symposum on VLSI*, 2004, pp. 338–343.

[17] H. Hofstee, "Future microprocessors and off-chip SOP interconnect," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 301–303, May 2004.

[18] P. Andry, C. Tsang, E. Sprogis, C. Patel, S. Wright, B. Webb, L. Buchwalter, D. Manzer, R. Horton, R. Polastre, and J. Knickerbocker, "A CMOS-compatible process for fabricating electrical through-vias in silicon," pp. 831–837, July 2006.

[19] C. Patel, C. Tsang, C. Schuster, F. Doany, H. Nyikal, C. Baks, R. Budd, L. Buchwalter, P. Andry, D. Canaperi, D. Edelstein, R. Horton, J. Knickerbocker, T. Krywanczyk, Y. Kwark, K. Kwietniak, J. Magerlein, J. Rosner, and E. Sprogis, "Silicon carrier with deep through-vias, fine pitch wiring and through cavity for parallel optical transceiver," in *Electronic Components and Technology Conference*, June 2005, pp. 1318–1324.

[20] M. Jung, J. Mitra, D. Pan, , and S. K. Lim, "TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC (preprint)," *48th ACM/IEEE Design Automation Conference*, pp. 803–806, 2011.

[21] X. Liu, Q. Chen, P. Dixit, R. Chatterjee, R. Tummala, and S. Sitaraman, "Failure mechanisms and optimum design for electroplated copper through-silicon vias (TSV)," in *Electronic Components and Technology Conference*, May 2009, pp. 624 –629.

[22] K. Lu, X. Zhang, S.-K. Ryu, J. Im, R. Huang, and P. Ho, "Thermo-mechanical reliability of 3-D ICs containing through silicon vias," *Electronic Components and Technology Conference*, pp. 630 –634, May 2009.

[23] S. Ryu, K. Lu, X. Zhang, J. Im, P. Ho, and R. Huang, "Impact of near-surface thermal stresses on interfacial reliability of through-silicon-vias for 3-D interconnects," *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 1, pp. 35–43, Mar. 2011.

[24] N. Tanaka, M. Kawashita, Y. Yoshimura, T. Uematsu, M. Fujisawa, H. Shimokawa, N. Kinoshita, T. Naito, T. Kikuchi, and T. Akazawa, "Characterization of MOS transistors after TSV fabrication and 3D-assembly," pp. 131 –134, Sep. 2008.

[25] A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, S. Domae, D. Perry, M. Choi, A. Redolfi, C. Okoro, Y. Yang, J. Van Olmen, S. Thangaraju, D. Tezcan, P. Soussan, J. Cho, A. Yakovlev, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k / metal gate cmos performance," *IEEE International Electron Devices Meeting*, pp. 2.2.1–2.2.4, 2010.

[26] J.-S. Yang, K. Athikulwongse, Y.-J. Lee, S. K. Lim, and D. Pan, "Tsv stress aware timing analysis with applications to 3D-IC layout optimization," *47th ACM/IEEE Design Automation Conference*, pp. 803–806, 2010.

[27] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr 1954.

[28] F. Bufler, A. Erlebach, and M. Oulmane, "Hole mobility model with silicon inversion layer symmetry and stress-dependent piezoconductance coefficients," *IEEE Electron Device Letters*, vol. 30, no. 9, pp. 996–998, 2009.

[29] S. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-si: extending the cmos roadmap," *IEEE Transactions on Electron Devices*, vol. 53, no. 5, pp. 1010–1020, May 2006.

[30] W. Zhang and J. Fossum, "On the threshold voltage of strained-Si-$Si_{1-x}Ge_x$ MOSFETs," *IEEE Transactions on Electron Devices*, vol. 52, no. 2, pp. 263–268, 2005.