Architecture for Ultra-low Power Multi-channel Transmitters for Body Area Networks using RF Resonators

by

Arun Paidimarri

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Author . . . .
Department of Electrical Engineering and Computer Science
May 20, 2011

Certified by . . . .
Anantha P. Chandrakasan
Joseph F. and Nancy P. Keithley Professor of Electrical Engineering
Thesis Supervisor

Accepted by . . . .
Leslie A. Kolodziejski
Chairman, Department Committee on Graduate Theses

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Abstract

Body Area Networks (BANs) are gaining prominence for their use in medical and sports monitoring. This thesis develops the specifications of a ultra-low power 2.4GHz transmitter for use in a Body Area Networks, taking advantage of the asymmetric energy constraints on the sensor node and the basestation. The specifications include low transmit output powers, around -10dBm, low startup time, simple modulation schemes of OOK, FSK and BPSK and high datarates of 1Mbps.

An architecture that is suited for the unique requirements of transmitters in these BANs is developed. RF Resonators, and in particular Film Bulk Acoustic Wave Resonators (FBARs) are explored as carrier frequency generators since they provide stable frequencies without the need for PLLs. The frequency of oscillation is directly modulated to generate FSK. Since these oscillators have low tuning range, the architecture uses multiple resonators to define the center frequencies of the multiple channels. A scalable scheme that uses a resonant buffer is developed to multiplex the oscillators' outputs to the Power Amplifier (PA). The buffer is also capable of generating BPSK signals. Finally a PA optimized for efficiently delivering the low output powers required in BANs is developed. A tunable matching network in the PA also enables pulse-shaping for spectrally efficient modulation.

A prototype transmitter supporting 3 FBAR-oscillator channels in the 2.4GHz ISM band was designed in a 65nm CMOS process. It operates from a 0.7V supply for the RF portion and 1V for the digital section. The transmitter achieves 1Mbps FSK, up to 10Mbps for OOK and BPSK without pulse shaping and 1Mbps for OOK and BPSK with pulse shaping. The power amplifier has an efficiency of up to 43% and outputs between -15dBm and -7.5dBm onto a 50Ω antenna. Overall, the transmitter achieves an efficiency of upto 26% and energy per bit of $483pJ/bit$ at 1Mbps.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Joseph F. and Nancy P. Keithley Professor of Electrical Engineering

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Chapter 1

Introduction

1.1 Background and Motivation

Communication systems are ubiquitous, and low-power wireless communication in particular has been a major contributor to this. In the United States, a look at the FCC frequency allocation tables [3] shows the many varied applications for which wireless communication is being used. There is a constant push to use the spectrum more efficiently, increase its utility, and to expand its applications.

A look at the history of wireless communication gives a sense of its usage in daily life [1]. Wireless communication started with telegraphy and broadcast radio as the main applications. Point-to-point communication grew rapidly with the advent of cellular service. Initially,wireless communications were used only for voice communication, soon data was added, and today we have very complex, high data rate internet services provided directly on cellular networks. Most of these systems are large networks covering long distances. With the growth of the Internet, consumer electronics and sensor networks, Wireless Local Area Networks (WLAN), Bluetooth and Zigbee based Wireless Personal Area Networks (WPAN) have also grown. Each of these cater to different data rates and distance specifications.

Table 1.1 summarizes the these standards and some of their specifications. One

theme that is visible here is that continued research and development in CMOS integration, and low-power radio design has shrunk the devices for use in progressively smaller sized networks.

The current focus is the development of Wireless Body Area Networks (WBAN). Targeting very short distances of about 1-2m, WBANs aim to build a network of sensor nodes around the human body. Each of these nodes could be monitoring various vital signs and help in medical monitoring or sports training. This thesis aims to develop a ultra-low power transmitter optimized for use in these WBAN networks. A new standard, called the Medical Body Area Network Standard is being developed, and will be discussed in Section 1.2.

Standard	Year	Frequency	Data rate	Distance	Typ. P_{Out}
GSM	1991	900MHz/1.8GHz	270kbps	<10km	0.5W
802.11b	1999	2.4GHz	54Mbps	<100m	32mW
Bluetooth	1998	2.4GHz	2.1Mbps	10m	2.5mW
Zigbee	2004	2.4GHz	250kbps	10-75m	1mW
MICS	2003	400MHz	200kbps	1-2m	25μW
Bluetooth LE	2010	2.4GHz	200kbps	50m	1mW
MBAN	-	2.4GHz	1Mbps	1-2m	100μW

Table 1.1: Current Specifications of some Wireless Standards [1, 2]

Typical biomedical systems that will be used in BANs will have an analog front-end, ADCs, digital processors and the radios to finally transmit the data. [4] shows that even after significant processing, the radio power is quite significant. [5] shows how clever digital design can lead to large energy savings when processing biomedical information. Since radios are a major energy consumer in these biomedical systems, improvements here can lead directly to significant energy savings for the system.

Wireline communications using e-textiles are a very attractive option for designing BANs because of their really low power [6]. But wireless circuits are more ergonomic and can be more easily used in places like the head and ear and can have more widespread applications. So, this thesis aims to develop a wireless transmitter optimized for use in BANs.

1.2 Medical Body Area Networks Standard

The IEEE P802.15 working group for Wireless Personal Area Networks(WPANs) is in the process of creating a new standard for Body Area Networks, called IEEE 802.15.6 [2]. It is aimed at addressing requirements for BANs, such as power consumption and the short distance nature of the communication. The BAN network topology, as shown in Figure 1-1 is of the star-type, with a main hub or basestation coordinating the network and the sensors as nodes. The basestation is a cellphone type device and can be assumed to be relatively energy unconstrained. The sensor nodes are much smaller and are required to have much longer battery life and are thus energy-constrained.
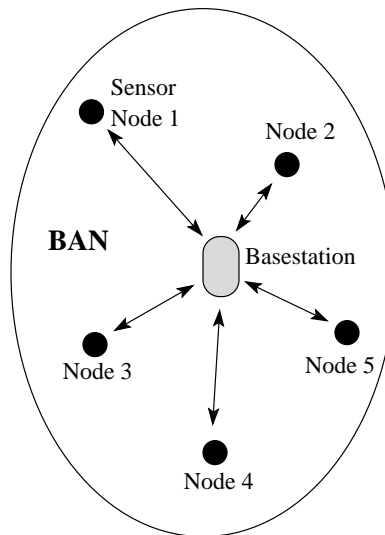
Figure 1-1: Network topology of a BAN

The standard proposes 3 PHY layer standards, Narrowband(NB), Ultra Wideband (UWB) and Human Body Communications(HBC). UWB transmitters have been shown to have excellent performance in terms of energy/bit [7]. But, UWB has also been shown to be susceptible to narrowband interferers. HBC transceivers use the human body as a communication channel. They transmit in the 10s of megahertz frequency, and like the e-textile communication, have localization of signal. Low energy per bit has been achieved in the literature [8], but this scheme relies on good

electrode contacts for minimal path loss and the channel is not well understood.

The NB specification of the proposed standard allows operation in multiple bands, as shown in Table 1.2. The 2.36-2.4 GHz Medical Body Area Networks band is a newly proposed band for used in BAN applications and the 2.4-2.483.5 GHz ISM band is available internationally. These frequency bands are considered in this thesis. As can be seen from the table, a practical radio must be capable of functioning in multiple channels to mitigate fading and interference in the unregulated ISM bands. This thesis focuses on architectures for NB transmitters that are optimized for BANs, especially for the energy-constrained sensor nodes in the network. The PHY specifications for the prototype are inspired from the standard, though some modifications are made to optimize power consumption. The specifications are discussed in Section 1.4

Frequency (MHz)	Channel BW (MHz)	No. of Channels
402-450	0.3	10
420-450	0.5	12
863-870	0.4	14
902-928	0.5	48
950-956	0.4	12
2360-2400	1	38
2400-2483.5	1	79

Table 1.2: The proposed 802.15.6 Frequency Plan [2]

1.3   Body Area Network Channel Characteristics

The distance between nodes on a BAN is only about 1-2m. The Friis free-space path loss equation [9] is:

$$\text{Path Loss} = \frac{P_{\text{r}}}{P_{\text{t}}} = G_r G_t \left(\frac{\lambda}{4\pi d}\right)^2 \tag{1.1}$$

Assuming the antenna gains G_r and G_t to be $0dBi$, then for $2.5GHz$, 1-2m distance implies a path loss of $40dB$ to $46dB$.

But, the path is not free-space, and the environment creates a lot of multipath

effects, which degrades the path quite significantly. Also, there is usually no direct path from the transmitter to the receiver due to conductive nature of the human body. For example, if the transmitter is at the back of the body and the receiver is at the front of the body, the signal reaches the receiver through surface waves that propagate along the human body. These are highly lossy. [10] simulates these surface waves through a finite element method. They show the path loss of these surface waves to be even as high as $100dB$ when the transmitter and receiver are diagonally opposite to each other.

But this high path loss is not realistic. [11, 12] perform measurements of the path loss in real-life environments like an "office". These show the path loss to be actually much lower, around $60 - 70dB$ and approaching at the most $80dB$ is some cases. These measurements and path loss characteristics was verified by Prof. Dina Katabi's group at MIT(A sample measurement is shown in Figure 1-2). This shows that other propagation modes, for example through multiple reflections off the walls, floor or roof, are the dominant modes. So, a BAN network must be designed to meet this path loss constraint.
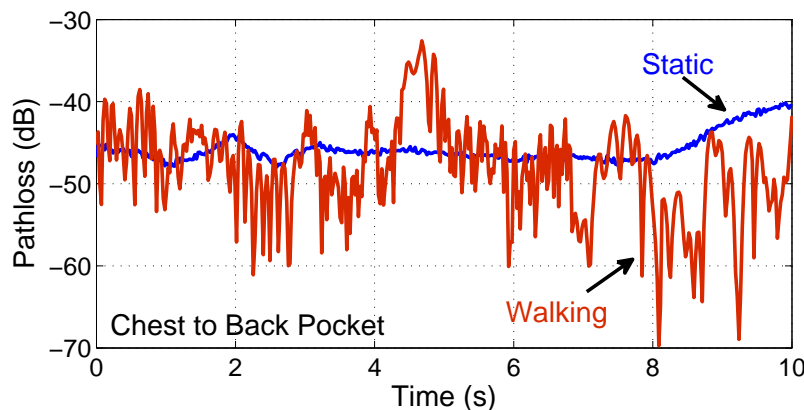
Figure 1-2: Path loss in a BAN measured in office environment, courtesy of H. Hassanieh, D. Katabi, MIT, who performed the experiments.

1.4   BAN Transmitter Specifications

Radios modulate a carrier frequency with baseband data and then transmit the information through an antenna using a power amplifier. These blocks and the other specification of a BAN transmitter are considered further.

Carrier frequency is the center frequency of transmission. Standards usually allocate channels with higher bandwidths at higher frequencies. Higher bandwidths imply a higher datarate for a given modulation scheme. The $2.4GHz$ ISM band is universally available. Also, the the $2.36 - 2.4GHz$ MBANs band is newly proposed for use in BANs and will have lesser interference as compared to the ISM band. So, the center frequency is chosen to be in this range of frequencies.

Power Output of the transmitter must be high enough for the receiver to reliably decode the information after accounting for the path loss. As was shown in the previous section, the maximum path loss in a BAN scenario is at most 80dB, at 2.5GHz. Because of this energy asymmetry of a star-network BAN (Section 1.2), specifications of the transmitter can be relaxed. The receiver on the basestation could be like a standard Bluetooth receiver[1]. Sensitivities of $-90dBm$ are easily achieved [13, 14]. Now, looking at the link budget for the transmitter:

$$P_{TX,max} = \text{Sensitivity} + \text{Path Loss}_{Max} = -90\text{dBm} + 80\text{dB} = -10\text{dBm} \quad (1.2)$$

Hence, the transmit power of the sensor node needs to be around -10dBm. Typically, power amplifiers are designed to operate at much higher power levels and when backed off to power levels like -10dBm, the efficiency is drastically reduced [15]. So, it is important to investigate PA topologies that are optimized for the low transmit powers.

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[1]The frequency, data rate and modulation of the transmitter are quite similar to Bluetooth, so, this assumption is a valid one

Channels : A transmitter needs to be able to operate in multiple channels so as to coexist in a Frequency Division Multiplexing (FDM) scenario and also to avoid interferers in a unlicensed band like the ISM band. So, the transmitter must support multiple channels of operation.

Data rate is another important specification. The intrinsic datarate of the sensor is usually quite low, but it is more efficient to buffer the data and send it in bursts at higher transmission data rates [16]. This data rate determines the energy per transmitted bit that is consumed by the transmitter.

$$\text{E/bit} = \frac{\text{Power}}{\text{Data Rate}} \tag{1.3}$$

Data rate is a function of the modulation scheme, bandwidth and baseband filtering scheme used. Higher order modulation schemes allow transmission of a higher datarate for a given bandwidth. Also, filtering allows a greater symbol rate for a given bandwidth because it reduces the amplitude of sidelobes[2].

Baseband filtering usually implies that linear mixers and Power Amplifiers must be used, which result in higher power consumption. Circuit architectures that can provide filtered outputs and yet be efficient can transmit at higher datarates and get very low energy-per-bit are required. A datarate of 1Mbps is targeted for the transmitter designed in this thesis.

Modulation of the carrier with baseband data is done with a mixer. The modulation scheme determines the specifications like linearity, and thus its power consumption. It also puts constraints on the linearity of the PA. Higher modulation schemes like 4-QPSK consume more power, but also transmit more bits per symbol. Simple modulation schemes like OOK and BPSK can even use

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[2]This is a function of the spectral mask used. For example, the proposed MBANs standard specifies that the side lobe should be 20dB lower than the main lobe. Even for such a relaxed specification, some pulse shaping is required, as shown in Chap 4.

passive mixers which consume no power. In addition, 2-FSK does not even require a mixer. [17] studies sensor networks based on "Energy Per Useful Bit", and concludes that simple modulation schemes like OOK are the most efficient because they minimizes the synchronization overhead.

Transmitter Efficiency is another important metric to consider. It is defined as the ratio between the transmit output power and total power consumed.

$$\eta_{\text{TX}} = \frac{P_{\text{out}}}{P_{\text{total}}} \tag{1.4}$$

When transmitting very low powers like $-10dBm$, the transmitter efficiency is highly degraded if complex modulations schemes requiring power hungry mixers are used. For this reason, only simple binary modulation schemes of OOK, 2-FSK and BPSK are considered in this work.

Startup Time is the time it takes for various blocks in the transmitter to be ready to accept data. The energy spent in startup is wasted and increases the effective energy per bit of the system [16]. Also, long packet sizes must be used to amortize the startup energy. So, it is important to design circuits with low startup time, of the order of a few bit periods. A startup time $< 10\mu s$ is targeted.

Supply Voltage is an important design specification. This must be decided in consideration of all the components of the system. For example, higher V_{DD} implies higher voltage swings are possible. So, one would like to have high amplitudes driving the PA to improve its efficiency. But, generating low output powers like -10dBm from high supply voltages is difficult (Section 3.4), requiring lower V_{DD} operation. For this design, a supply of 0.7V is chosen. and is justified for the various blocks of the system in their respective design sections in Chapter 3

A summary of the specifications of the transmitter are in Table 1.3

	Target Specifications
Voltage	0.7
Frequency Band	2.4GHz MBAN & ISM bands
Channels	> 1
Bandwidth	1MHz
Modulation Scheme	BPSK, OOK, 2-FSK
Data Rate	1Mbps
PA Output Power	-10dBm
Start-up Time	$< 10\mu$s
Energy/bit	500pJ

Table 1.3: Specifications of the prototype BAN transmitter

1.5 Thesis Contributions

1. This thesis develops an architecture for a transmitter than uses multiple RF resonators to generate the center frequencies. A prototype transmitter that multiplexes three FBAR-based oscillators is demonstrated at 2.4-2.5 GHz.

2. A power amplifier that is optimized for low output powers of near -10dBm is developed. It achieves an efficiency of 35% at -10dBm and reaches 43% at -7.5dBm. The PA is also capable of performing pulse shaping efficiecntly through the use of a tunable matching network.

3. An efficient and scalable multiplexing scheme is developed so that the architecture can scale to many more resonators than the three demonstrated. This is achieved by usging a resonant buffer to buffer the signal from the oscillators to the PA.

4. The architecture supports three modulations schemes, OOK, BPSK and FSK. FSK is implemented upto as datarate of 1Mbps, OOK and BPSK can go up to 1Mbps with pulse shaping and 10Mbps without pulse shaping.

5. The circuit is designed to operate at 0.7V and consumes 483pJ/bit for 1Mbps OOK modulation.

1.6   Thesis Outline

This thesis describes the design and measurement of a low power transmitter that is optimized for use in a Body Area Network. The specifications of such a transmitter have been discussed in Section 1.4. Chapter 2 surveys previous work in this space and develops an architecture that meets the specifications set out in Table 1.3. Chapter 3 discusses in detail the design of each of the various blocks, including the oscillators, multiplexer, buffer and the power amplifier. Chapter 4 presents the measured results of the chip. Finally, Chapter 5 presents some conclusions from the work and suggests further improvements to this design.

Chapter 2

Transmitter Architecture

This chapter discusses previous work in low power transmitter designs and builds an architecture that can meet the specifications set out in Section 1.4.

2.1 Some Previous Low-power Transmitters

The literature on radios for Wireless Sensor Networks (WSN), Medical Implant Communications Service (MICS) and recently, Body Area Networks (BAN) is extremely rich, with many architectures and circuit techniques developed to reduce power consumption. WSN radios are quite close in their specifications as BAN radios. But, they are usually designed for slightly longer distances, and target $P_{\text{Out}} \approx 0dBm$. Also, some of these radios are designed for very low raw data rate applications (sometimes as low as 10kbps, which is reasonable in WSNs). This is not true for BANs, where some applications might require large data rates. In addition, since multiple independent BAN networks can coexist in a small region (like multiple people inside a room), higher datarates and multi-channel capability can reduce the amount of packet collisions.

Table 2.1 summarizes some previous WSN, BAN and MICS transmitters.

This table shows that OOK and FSK are the predominant modulations schemes

Ref	Frequency (MHz)	Modulation	Data Rate (Mbps)	P_Out (dBm)	Energy/bit (nJ)	η_{TX} %	Notes
				LC Tank or Ring Oscillator based Transmitters			
[18]	400	MSK	0.12	-16	2.9	7.1	Basestation based frequency correction loop to 3ppm accuracy
[19]	900	FSK	0.02	-6	65	19	FLL and current reuse
[20]	2400	OOK	1	0	2.53	24	Duty cycled PLL
[21]	400	MSK	0.2	-17	0.45	22	Injection locked ring oscillator and edge combining
[22]	2400	FSK	0.5	-8.5	1.4	24	400mV operation, uses LC oscillator without PLL
[23]	900	FSK	0.05	-10	46	4.3	BAN SOC
[24]	400	4-FSK	0.8	-4.5	< 14.4	3.1	
[25]	900	FSK	5	-10	0.14	14.2	LC oscillator, basestation based frequency calibration
				RF Resonator based Transmitters			
[26]	900	OOK	1	-11.4	3.8	2	SAW stabilized oscillator, single channel
[27]	1900	OOK	0.33	0.8	4.05	46	FBAR based, 2 channels
[28]	1900	OOK	0.005	-4.5	320	22	FBAR based, 1 channel operation
[29]	2110	FSK	0.05	1	120	21	Single channel BAW based design
[30]	433	OOK	3/10	-12.7	0.187/0.052	9.6	Single channel BAW based
[31]	1900	OOK	0.04	1.6	200	16.5	Two channels by replicating the whole transmit chain
[32]	2400	GFSK	1	-4	30	1	BAW oscillator and heterodyne architecture
This Work	2400	OOK,BPSK and FSK	1/10	-10	483/48	18	FBAR multi-channel architecture

Table 2.1: Some previous ultra-low power WSN, BAN and MICS transmitters and their specifications compared with the measured results of this work

of transmitters that achieve the lowest power consumption. Also, the energy/bit
of transmitters is greatly dependent on the data rate. Some transmit at very high
datarates like 5-10Mbps, but this is impractical, in general, because with binary mod-
ulation schemes, the bandwidth is very high (10-20MHz). Since these are operating in
unlicensed bands like the ISM bands, it is very difficult to find a slot this wide with-
out interference. So, bandwidths of about 1-2MHz are more practical, which leads to
datarates of around 1Mbps. Another important feature is the output power. It can
be seen that at higher output powers, the transmitter efficiency is higher because the
PA dominates the power consumption. Another notable fact is the performance of RF
resonator based transmitters. They have excellent power consumption, but most are
1 channel and those that operate on 2 channels do not have a scalable architecture.

2.2 System Power Considerations

Figure 2-1 shows a generic transmitter, with a Local Oscillator(LO), a modulation
block and the power amplifier. Since $P_{\mathrm{Out}} \approx -10$dBm, which is $100\mu W$, with $\approx 35\%$
efficiency, the PA will consume $\approx 285\mu W$[1]. So, the power consumption of the other
blocks is very critical to the power consumption of the circuit. This is in contrast to
the circuits for cellular or even Bluetooth transmitters, where the PA is the dominant
power consumer.
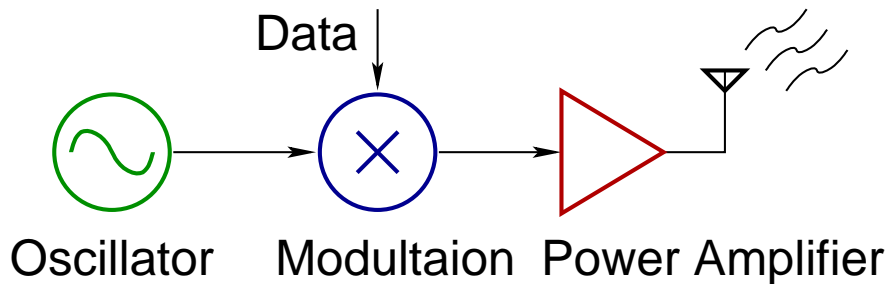
Figure 2-1: Generic Transmitter Architecture

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[1]These numbers are achieved with the PA designed in Section 3.4

The choice of modulation schemes helps in this, because OOK, FSK and BPSK can be achieved with essentially zero power as was discussed in Section 1.4.

For LO generation, a Phase Locked Loop(PLL) is usually used to convert a low frequency crystal reference to the RF frequencies. These PLLs consume a large power because of the frequency dividers, precision phase detectors and charge pumps used. Also, these circuits have a long startup time because the bandwidths of the PLLs dictate their locking time. So, it is good to avoid a PLL in the generation of LO if possible. But, the main advantage of a PLL-based LO generation is frequency stability[2] and tunability. In the absence of a PLL, Table 2.2 summarizes the properties of some individual RF oscillator types.

Oscillator Type	Advantages	Disadvantages
Ring Oscillator	- Ultra low power - Low startup time - Very wide tuning range	- Susceptible to PVT - Frequency instability - Poor phase noise
LC tank Oscillators	- Moderate power - Low startup time - Moderate tuning range	- Frequency instability - Moderate phase noise
RF Resonator based Oscillators	- Low power - Low phase noise - Moderate startup time - Frequency stable	- Low tuning range - Single channel operation

Table 2.2: A summary of individual RF oscillator types

This shows that RF resonator-based oscillators are good choices because they eliminate the need for a PLL. The low tuning range and single channel operation must be addressed however to make it practical. Section 2.4 discusses this further.

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[2]The stability is dictated by the stability of the reference frequency, which is usually a quartz crystal

2.3   RF Resonators for Low Power LO Generation

RF resonators are used extensively in front-end filters for cellphones. These filters are required to have sharp cutoffs, low in-band insertion loss and high out-of-band rejection. This is typically achieved using a ladder topology with very high-Q resonators. The Q specifies how sharp the cut-off is. Surface Acoustic Wave (SAW) filters, thin-film Bulk Acoustic Wave (BAW) resonators are two widely used technologies. These devices use piezoelectric materials. Silicon MEMS is also a very attractive technology currently in development which may one day be fully integrated with standard CMOS

Figure 2-2 shows the characteristics of a resonator, in this case an FBAR. It has the following features:

1. The impedance is resistive and low at the series resonant frequency.

2. The impedance is very high and resistive at a slightly higher frequency called the parallel resonance frequency.

3. The coupling coefficient is defined as $k_t^2 = \left(\frac{f_p}{f_s}\right)^2 - 1$ and indicates the amount of tuning available in the resonator.

4. At frequencies far away from resonance, the impedance is capacitive

5. Between the two resonant frequencies, the impedance is inductive.

The resonators are typically modeled with the modified Butterworth Van Dyke (m-BVD) model shown in figure 2-3(b) [33]. This is a modification of the BVD model shown in Figure 2-3(a) and captures all the characteristics. The BVD model is much simpler and can capture only some of the features. For example, it can be made to capture the parallel resonance better while ignoring the series resonance impedance. This can be useful for analysis of parallel resonance oscillators because it simplifies it. This is used in Section 3.1.
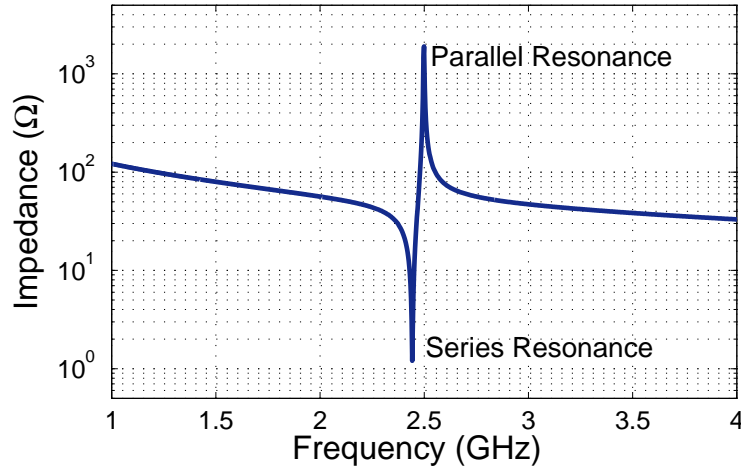
Figure 2-2: Impedance characteristics of a RF Resonator

(a) Butterworth Van Dyke model

(b) Modified- Butterworth Van Dyke model
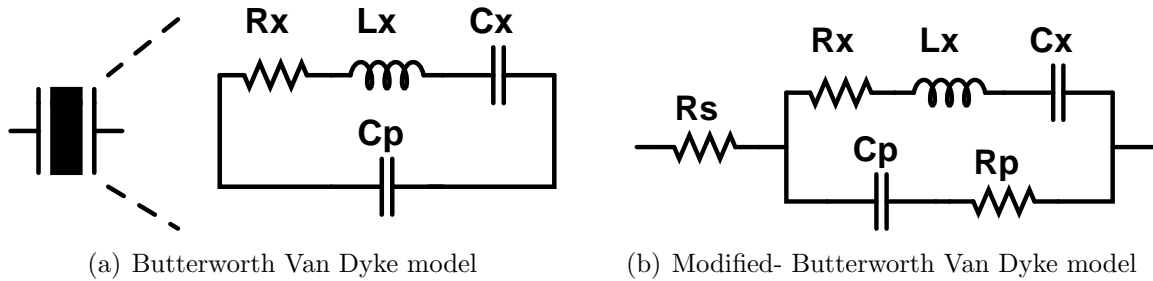
Figure 2-3: FBAR Models

2.3.1   Film Bulk Acoustic Resonators (FBAR)

[34, 35] show that Film Bulk Acoustic Resonators (FBARs) can be used in low-power oscillators to create stable, low phase-noise center frequencies which can be used in radios. FBARs are high-Q (Quality Factor) resonators which lead to the stability in the frequency and the low power. FBARs are used as the resonators in this thesis. FBARs from three different wafer types are used. The BVD model parameters for some of the FBARs used is this project are given in Table 2.3[3]

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[3]BVD model fit for parallel resonance

FBAR Type	R_x	L_x	C_x	C_p	Q	R_p
1	1.15	74.7	55.1	1.23	1000	2.16
2	0.61	58.1	75.9	1.52	1400	2.97
3	1.05	107.2	38.99	1.292	1600	2.26

Table 2.3: Representative BVD model parameters of the FBARs used in the design

2.3.2 RF Silicon MEMS

[36, 37] shows that silicon-based resonators have a very high-Q. These silicon resonators (as opposed to FBARS) have a great scope for integration into CMOS processes and thus present a very attractive option for low-power radios. The challenge in creating oscillators that use these silicon-MEMS resonators is their low coupling coefficient and high motional impedance. Oscillators that use such resonators have been shown to be possible [38], but they consume large currents to compensate for the low k_t^2 and high R_x. So, this is not an option for this design.

2.4 Multiple Channel Operation

Since these oscillators are high-Q and have very low tuning range, transmitters that use these can only transmit in one channel. It is important to have more channels to improve the net throughput of the network and to avoid interferes. [31] has two channels of operation by replicating the full transmit chain, using two resonators, but this method is not scalable. So, an architecture that can use these high-Q resonators and yet have multi-channel operation is required. Some methods are discussed below:

1. One way would be to switch in/out the resonators using a matrix of switches. But, since the resonators are high-Q, the switch resistance must be low to not degrade performance. Also, the excess capacitance of the switches will load the oscillators.

2. [39] develops a method of using a tunable "negative capacitance" across the resonator to extend its frequency tuning range. This helps create oscillations

at frequencies above the intrinsic f_p of the resonator. Good phase noise perfor-
mance is also achieved, but the power consumption is quite high and so, cannot
be ported in a low power radio.

3. Replicate the oscillator structure and select one of the oscillators to drive the
Power Amplifier. This way, each high-Q resonator can provide the center fre-
quency for each channel of operation. Each oscillator topology should be small
in area for this scheme to scale. This is the method chosen in this design. The
exact multiplexing scheme is discussed in detail in Section 3.2 where the need
for a buffer between the multiplexer and the power amplifier is motivated. This
buffer is made resonant to reduce power consumption, as will be discussed in
Sec 3.3

2.5   System Architecture and Salient Features

Figure 2-4 shows the full system architecture.
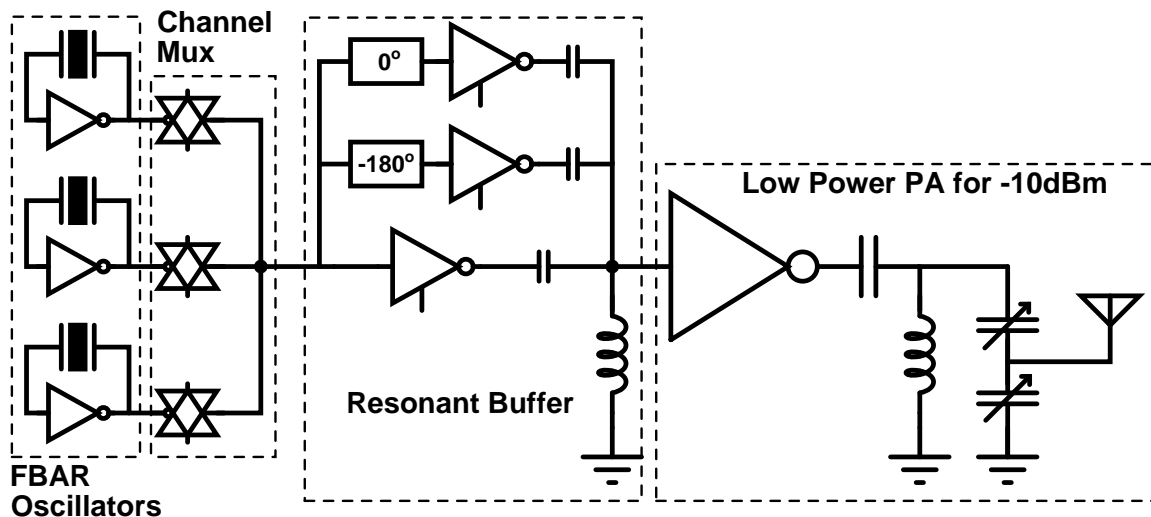
Figure 2-4: Full System Architecture for the Transmitter

1. The 3 channels are defined by the 3 FBAR based oscillators.

2. FSK is achieved by switching capacitive load of the oscillator.

3. A multiplexing scheme selects the currently used channel.

4. A resonant buffer the oscillator signal and drives the Power Amplifier.

5. A calibrated delay in the buffer is used to change the phase of the waveform that drives the PA. This is used to provide BPSK.

6. An efficient PA optimized for $-10dBm$ output power is designed.

7. The PA is turned on/off for OOK modulation. The buffer can also be turned off to reduce power consumption when data is '0'.

8. The PA is designed to also provide efficient pulse shaping to reduce spectral usage. This is done with a tunable matching network.

Thus, an architecture that supports multiple channels, has an output power of $-10dBm$, has a low power and stable LO through the use of high-Q resonators, and supports 3 simple modulation schemes of OOK, FSK and BPSK is developed. Chapter 3 discusses the detailed design of each of these blocks.

Chapter 3

Transmitter Design and Implementation

The previous chapters discussed the specifications of a transmitter for use in body area networks and proposed an architecture that takes advantage of the unique characteristics of the system. In this chapter, the design and implementation of the individual circuits blocks is presented. The design options, specific design choices and trade-offs are discussed.

3.1 FBAR-based Oscillators

Section 2.3.1 presented the characteristics of a Film Bulk Acoustic Resonator (FBAR). It is modeled by a modified-Butterworth Van Dyke (m-BVD) model as shown in figure 2-3(b). The model is the same as that of a crystal, except for the fact that the resonance frequency is at RF. Thus, the vast knowledge of design of crystal oscillators can be applied almost directly for the design of RF resonator-based oscillators, including FBAR oscillators. All the topologies invented for crystal oscillators can also be ported for use with the FBARs. [34, 35, 26, 40] are a few examples of oscillators designed using FBARs. In the following subsection, some of the common oscillators

topologies and their characteristics are explained.

3.1.1 Common Oscillator Topologies

Figures 3-1, 3-2 and 3-3 show 4 common topologies, 2 Pierce oscillators, a single-ended Colpitts oscillator and a differential Colpitts oscillator that use FBARs. These are borrowed from [26, 40, 34, 35].

Single-ended Colpitts Oscillator [26]

This oscillator, shown in Figure 3-1 is a standard LC Colpitts oscillator, with frequency stabilization provided by the FBAR (or SAW as in [26]). The FBAR is a short only at the series resonant frequency, and thus allows the Colpitts oscillator to only oscillate at that frequency. In other words, the loop gain is maximum at the f_s of the FBAR. Since the LC tank is usually low-Q, it has a wide bandwidth, and doesn't dictate the frequency. This oscillator can function at very low voltages and still provide good amplitudes because the inductor allows the drain voltage to swing up to $2V_{DD}$. Some care is required in the design of the oscillator with regard to parasitic oscillations. The FBAR also provides a low impedance at frequencies higher than f_p because of the parallel plate capacitance C_p. If the LC tank in the oscillator provides loop gain > 1 at these higher frequencies, the parasitic oscillations can occur.

This oscillator, though, provides only a single nominal frequency, and cannot be tuned, since the series resonance is intrinsic to the device itself. This feature can be advantageous in some cases, but the center frequency of a transmitter should be tunable to account for process variations in the FBAR and to center the frequency to the center of the channel. Also, without tuning, FSK cannot be used as a modulation scheme in the system.
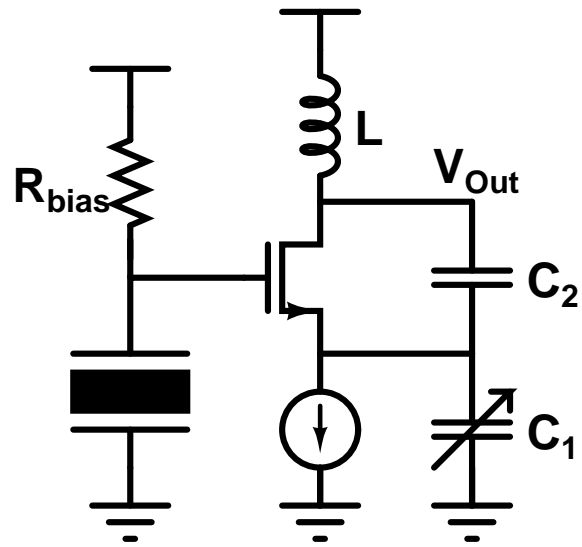
Figure 3-1: Single-ended Colpitts Oscillator
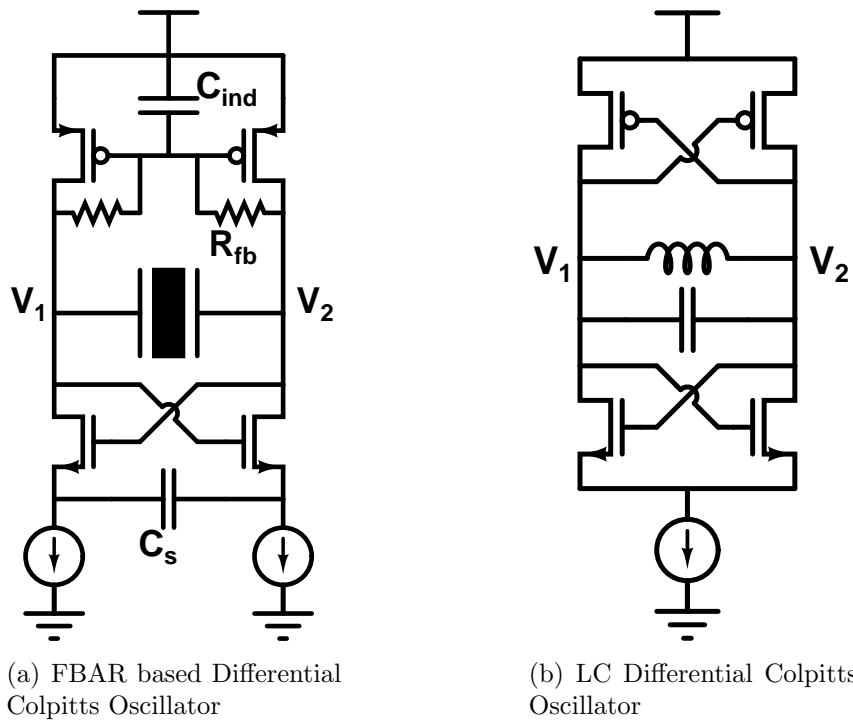
(a) FBAR based Differential
Colpitts Oscillator

(b) LC Differential Colpitts
Oscillator

Figure 3-2: Differential Colpitts Oscillator with and without FBARs

(a) Pierce Oscillator

(b) Inverter-based Pierce Oscillator
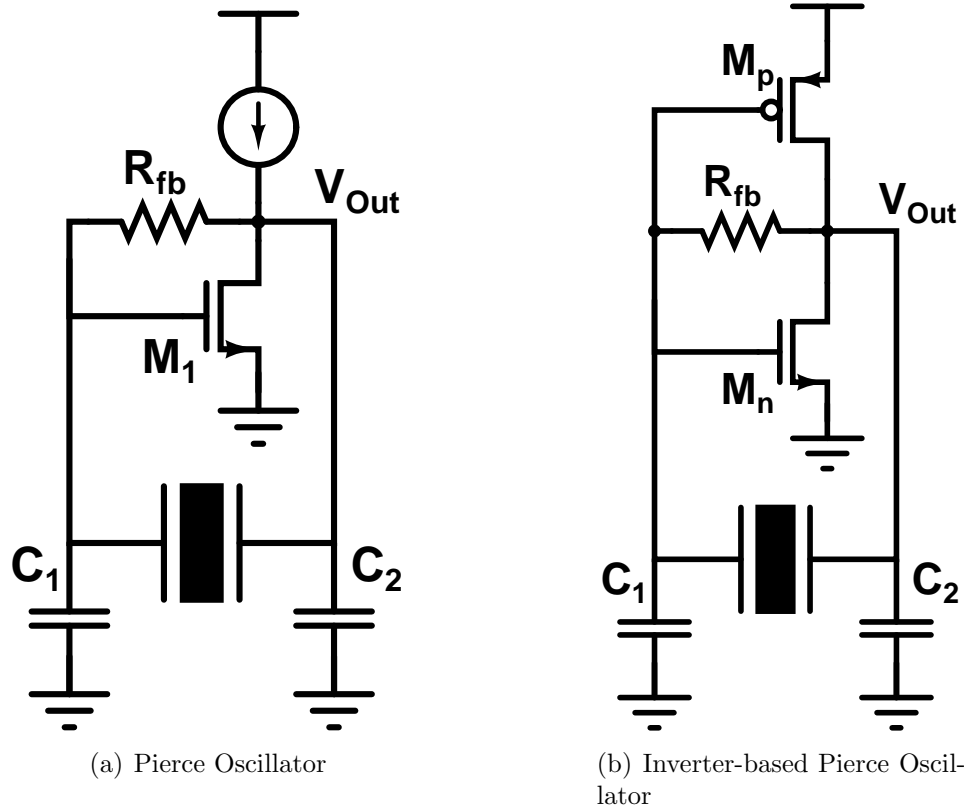
Figure 3-3: Two Pierce Oscillator Topologies

Differential Colpitts Oscillator [40]

A differential Colpitts oscillator with FBARs, shown in Figure 3-2(a) has the advantage of providing differential outputs, which could be used for BPSK modulation, or in a differential PA, if required. Also, due to the matched currents on the two branches, the power supply current is constant and causes lower power supply bounce.

The FBAR behaves like an inductor at frequencies between f_s and f_p and this inductor resonates with the device capacitance to provide an oscillation. Thus, the oscillation occurs at an effective parallel resonance and can be tuned with explicit capacitor banks.

An inductor-based differential Colpitts oscillator, shown in Figure 3-2(b) is easy to bias. Because the inductor is a short at DC, it can set the DC bias voltage of the transistors. But, at DC, the FBAR is an open-circuit (or capacitive) and the bias of

the oscillator must be set with special circuits. For example, if the inductor is simply replaced with an FBAR in Figure 3-2(b), the bias point where $V_1 = V_2$ is unstable and settles to $V1 = 0, V_2 = V_{DD}$ or $V_1 = V_{DD}, V_2 = 0$. The current will be 0 and no oscillations occur.

Figure 3-2(a) shows a biasing scheme that works for a differential Colpitts oscillator using FBARs. The active-inductors are used to present a low-impedance at DC and high-impedance at high frequencies [40]. Also, capacitive degeneration and two separate current sources are required to make the circuit DC-stable.

Due to the DC biasing problem, this circuit requires larger supply voltages. This prevents its use in the current design because low supply voltages are required for low output power PAs as will be seen in Section 3.4

Pierce Oscillator [34]

This oscillator, shown in Figure 3-3(a) uses a fixed current source provides current to the active transistor M1. The resistor R_{fb} provides DC biasing by setting the gate voltage. The FBAR behaves like a inductor at frequencies between its series and parallel resonance. This inductance resonates with the gate, drain and other parasitic capacitors at the effective parallel resonant frequency. The active transistor M1 sees a high impedance at this frequency. Under some approximations, the DC loop-gain of this circuit at the resonant frequency is

$$Gain \propto g_m \cdot R_p \tag{3.1}$$

where R_p is the FBAR impedance at parallel resonance. Thus, the circuit oscillates when designed at sufficient g_m[1]. The oscillator settles to a final amplitude based on the non-linearities and by the power supply voltage. The current can be chosen/adjusted to get the desired amplitude.

---

[1]There are a lot of caveats involved in this very simplified analysis and the full design equations will be explored in detail in Section 3.1.2

The oscillation frequency can be tuned to a certain extent by adding explicit capacitor banks at the drain or gate of the oscillator. Since there are only 2 transistors stacked, this topology is amenable to low supply voltage designs.

Inverter-based Pierce Oscillator [35]

The inverter-based pierce oscillator, shown in Figure 3-3(b) is similar in terms of operation to the one in the previous section but it has certain advantages in practice. The g_m of both the transistors add up and this current-reuse reduces power consumption for the same loop-gain. Also, the circuit is self-biased and does not need any current mirrors or current references. This circuit also provides rail-to-rail oscillation. This is because the current is not controlled by any current source. As the amplitude of gate voltage increases, the current increases above the DC bias current. So,the loop-gain increases for a while, before non-linearities and the rail voltages limit the oscillation amplitude. So, in cases where high amplitudes are required, this inverter-based pierce oscillator performs better. In a transmitter, high amplitudes are required at the PA, and a good amplitude of oscillation from the oscillator is preferred since it eliminates the need for any extra gain stages.

This circuit is also amenable to low-voltage design. In-fact, a higher V_{dd} can be detrimental because large shoot-through currents will make the circuit inefficient. It would be better to create higher amplitudes by using an extra amplifier stage.

Due to the advantages of current-reuse, high amplitudes of oscillation, low-power, low voltage operation, self-biasing and tunability, the inverter-based Pierce oscillator is chosen in this design. The detailed design and analysis of this inverter-based pierce oscillator is presented in the next subsection.

3.1.2   Detailed Design of the Inverter-based Pierce Oscillator

A circuit/system oscillates if it has poles in the right-half plane. This is the fundamental requirement and is fool-proof, because it relies on the actual full-system dynamics

to determine its properties. In this light, root locus analysis or nyquist analysis are the most reliable methods of analyzing oscillator circuits. All other methods, like the Barkhausen's criteria or Bode analysis with gain margin/phase margin are valid only under some assumptions [41].

[42] presents the theory of crystal oscillators. This analyzes the circuit as a negative resistance generator canceling the losses in the crystal itself. Though it is applied to low frequency crystal oscillator circuits, it translates well to the high frequency FBAR oscillators. The analysis, though not as general as looking at poles and zeros the closed loop system, is very useful because of the design insights and trade-offs it brings to the fore. This negative-resistance analysis and the root-locus method are both presented below.

Negative Resistance Oscillator analysis of Pierce Oscillator adapted from [42]

This analysis used the simpler BVD model of Figure 2-3(a), discussed in Section 2.3. Figure 3-4 shows the circuit of a Pierce oscillator with the circuit divided into two parts, a high-Q RLC network that represents the series resonant branch of the FBAR, and the rest of the circuit that includes the transistors, the parallel plate capacitance of the FBAR and circuit parasitics. The rest of the circuit is a low-Q system and its characteristics remain constant with frequency around the region of interest, i.e, around the resonant frequency of the RLC branch.

We now analyze the impedance presented by the rest of the circuit to the RLC branch. Figure 3-4 shows the simplified circuit model used. The parasitic resistances in the mosfet r_{ds}, r_g are ignored and R_{fb} is assumed to be large. The series resistance if the FBAR C_p is also ignored. C_1 represents the device gate capacitance, the associated routing, pad and any explicit capacitance at the gate of the inverter. C_2 similarly represents the capacitance of the drain, routing, input capacitance of the load and pads. C_3 lumps the device C_{gd} with the FBAR C_p. g_m is the sum of the
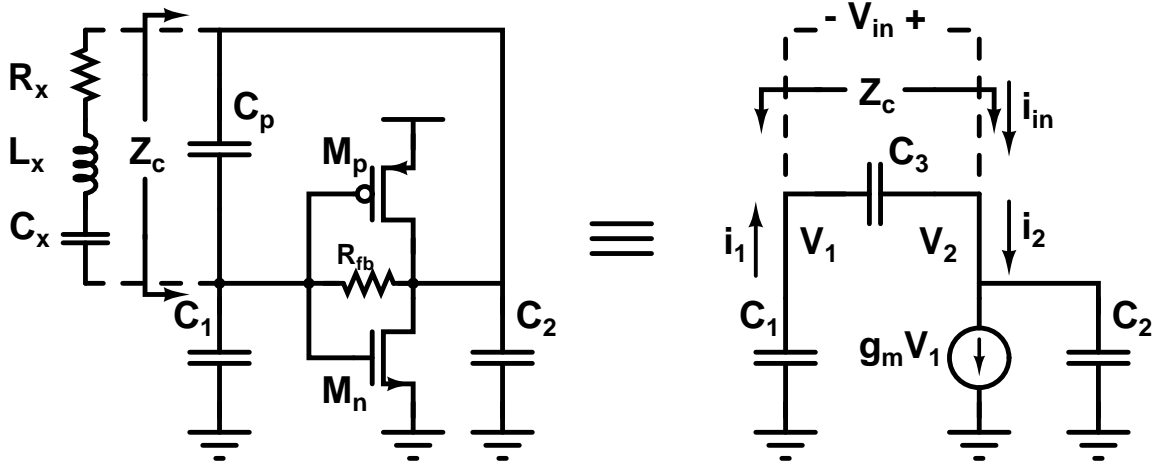
Figure 3-4: Inverter-based Pierce Oscillator: Circuit for Analysis

transconductances of the two transistors $M1$ and $M2$, ie. $g_m = g_{m1} + g_{m2}$. V_{in} is a dummy voltage source used to calculate the impedance of the circuit.

i_1 is the current through C_1. This is also equal to i_2, the sum of currents through $C2$ and the g_m dependent current source. This is given by

$$i_1 = -V_1 \cdot sC_1 \quad = \quad g_m \cdot V1 + V_2 \cdot sC_2 = i_2 \tag{3.2}$$

$$\therefore V_2 \quad = \quad -V_1 \frac{g_m + sC_1}{sC_2} \tag{3.3}$$

$$\therefore V_{in} = V_2 - V_1 \quad = \quad -V_1 \frac{g_m + sC_1 + sC_2}{sC_2} \tag{3.4}$$

$$\therefore i_1 = i_2 \quad = \quad V_{in} \frac{sC_1 \cdot sC_2}{g_m + sC_1 + sC_2} \tag{3.5}$$

The current through the voltage source, i_{in}, is

$$i_{in} = i_1 + V_{in} \cdot sC_3 \quad = \quad V_{in} \frac{g_m sC_3 + s^2 \left(C_1 C_2 + C_2 C_3 + C_3 C_1\right)}{g_m + sC_1 + sC_2} \tag{3.6}$$

$$\therefore Z_c = \frac{V_{in}}{i_{in}} \quad = \quad \frac{g_m + sC_1 + sC_2}{g_m sC_3 + s^2 \left(C_1 C_2 + C_2 C_3 + C_3 C_1\right)} \tag{3.7}$$

Evaluating the real and imaginary components of Z_c at a frequency ω,

$$R_{\text{circuit}} = \mathcal{R}(Z_c) = -\frac{g_m C_1 C_2}{(g_m C_3)^2 + \omega^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2} \tag{3.8}$$

$$\mathcal{I}(Z_c) = -\frac{g_m^2 C_3 + \omega^2 (C_1 + C_2)(C_1 C_2 + C_2 C_3 + C_3 C_1)}{\omega((g_m C_3)^2 + \omega^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2)} \tag{3.9}$$

Both the real and imaginary parts of the impedance are negative. So, the circuit presents a negative resistance in series with a capacitance to the RLC series branch of the resonator. Figure 3-5 shows the reduced model, with a voltage source added, to represent noise[2]. $C_{\text{eff}} = C_x || C_{circuit}$ and $R_{\text{eff}} = R_x + R_{circuit}$
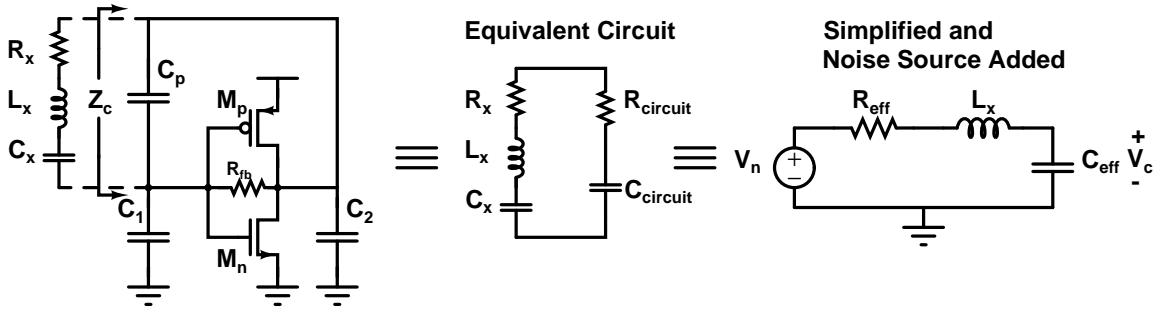
Figure 3-5: Equivalent circuit to calculate impulse response of Pierce oscillator

Oscillation Frequency: The transfer function of the capacitor voltage from the input in the effective circuit, shown in Figure 3-5 is

$$\frac{V_c(s)}{V_n(s)} = \frac{\frac{1}{sC_{\text{eff}}}}{sL_x + \frac{1}{sC_{\text{eff}} + R_{\text{eff}}}} \tag{3.10}$$

$$= \frac{1}{s^2 L_x C_{\text{eff}} + sC_{\text{eff}} R_{\text{eff}} + 1} \tag{3.11}$$

$$= \frac{1}{L_x C_{\text{eff}}} \frac{1}{\left(s + \frac{R_{\text{eff}}}{2L_x}\right)^2 + \left(\frac{1}{L_x C_{\text{eff}}} - \left(\frac{R_{\text{eff}}}{2L_x}\right)^2\right)} \tag{3.12}$$

---

[2]In reality, the noise of the circuit is what starts the oscillation, but for the sake of analysis, the impulse response is considered in this analysis.

The impulse response of the circuit is thus

$$V_c(t) \propto \exp\left(-\frac{R_{\text{eff}}}{2L_x}t\right) \sin\left(\sqrt{\frac{1}{L_x C_{\text{eff}}} - \left(\frac{R_{\text{eff}}}{2L_x}\right)^2}\, t\right) \tag{3.13}$$

So, for $R_{\text{eff}} < 0$ or $R_{\text{circuit}} < -R_x$, the circuit creates exponentially growing oscillations even in the presence of small disturbances like noise. The frequency is set by L_x and C_{eff} and is effected only slightly by R_{eff}.[3] The frequency of oscillation is thus given by

$$\omega_{\text{osc}}^2 \approx \frac{1}{L_x C_{\text{eff}}} = \frac{1}{L_x}\left(\frac{1}{C_x} + \frac{1}{C_{\text{circuit}}}\right) = \frac{1}{L_x C_x}\left(1 + \frac{C_x}{C_{\text{circuit}}}\right) \tag{3.14}$$

$$\therefore \omega_{\text{osc}} \approx \omega_s \sqrt{1 + \frac{C_x}{C_{\text{circuit}}}} \tag{3.15}$$

where ω_s is the series resonant frequency of the resonator. $C_{\text{circuit}} > C_p$, hence, it can be seen that the oscillation frequency is lower than the parallel resonance frequency of the resonator itself.

Startup Time: Also, the startup time of the oscillator is proportional to the time constant of the exponential envelope.

$$t_{\text{startup}} \quad \propto \quad \frac{L_x}{-(R_{\text{circuit}} + R_x)} = \frac{t_{\text{osc}}}{2\pi}\frac{\omega_{\text{osc}}L_x}{R_x}\frac{R_x}{-(R_{\text{circuit}} + R_x)} \tag{3.16}$$

$$\propto \quad t_{\text{osc}} \cdot Q \cdot \frac{R_x}{-(R_{\text{circuit}} + R_x)} \tag{3.17}$$

where t_{osc} is the time period of oscillation and Q is the quality factor of resonance in the resonator. The relation to Q is correct because it represents the amount of energy stored in the resonator as compared to the amount of energy dissipated. So,

---

[3]Since it is still a high-Q system, this is a valid assumption. In fact, R_{eff} affects only the oscillation frequency during startup. As will be shown shortly, R_{eff} becomes 0 when the oscillations settle down, at which point, frequency will be precisely determined by Eqn 3.15

greater the stored energy, the longer it takes to be charged up, which is the startup time. The third term in the equation, $\frac{R_x}{-(R_{\text{circuit}}+R_x)}$, represents the approximate speed or storing the energy in the resonator. R_{circuit}, which is a negative resistance specifies how much energy it is supplying to the resonator and R specifies the amount of energy dissipated. Thus, $\frac{R_x}{-(R_{\text{circuit}}+R_x)}$ represents the ratio of energy dissipated per cycle to the amount of extra energy supplied to the resonator per cycle.

So, in this analysis, the term $\frac{-(R_{\text{circuit}}+R_x)}{R_x}$ can be looked at as a proxy for loopgain of the oscillator. The more negative the R_{circuit}, the faster the circuit will startup and the greater will be the oscillation amplitude. So, the design of the Pierce oscillator is to make R_{circuit} as negative as possible under the constraint of power consumption.

Designing Z_c: Figure 3-6 shows the value of R_{circuit}, given by Eqn 3.8 as a function of g_m for representative values of C_1 ,C_2, C_3 at $2.5GHz$. The locus of Z_c, given by Eqns 3.8, 3.9 is also plotted on a complex plane. The line of $-R_x$ is also plotted so that the region of operation at which oscillations occur is clear. What this shows is that g_m cannot be increased indefinitely. Beyond a point, increasing g_m can be counterproductive and at very large values, can lead to no oscillations at all.

Maximizing $-\mathcal{R}(Z_c)$ as a function of g_m, we get the optimal value of g_m, given by:

$$g_{m,opt} = \omega \left(C_1 + C_2 + \frac{C_1 C_2}{C_3} \right) \tag{3.18}$$

For the FBARs that the circuit is designed for, $C_3 \approx 1.3pF$. From simulations, the capacitors C_1 and $C2$ are much smaller, around $500fF$, including pad capacitances. In this case, $g_{m,opt} = 18mS$, which would result in a very large power consumption, as shown in Figure 3-7.

On the other hand, the critical value of g_m to ensure oscillations occur is given by
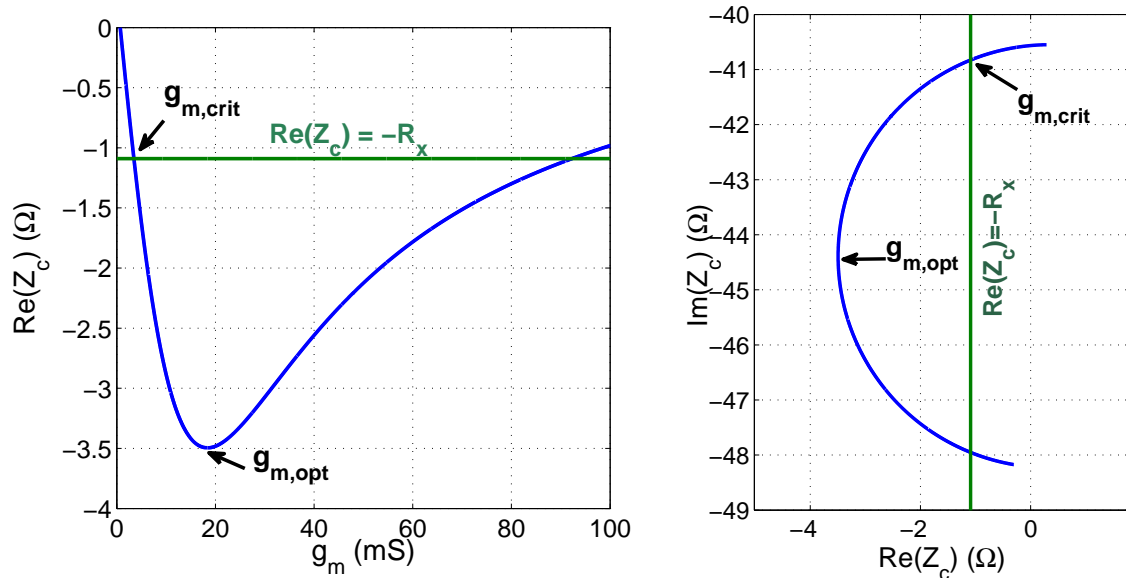
Figure 3-6: Plots showing Z_c as g_m is varied
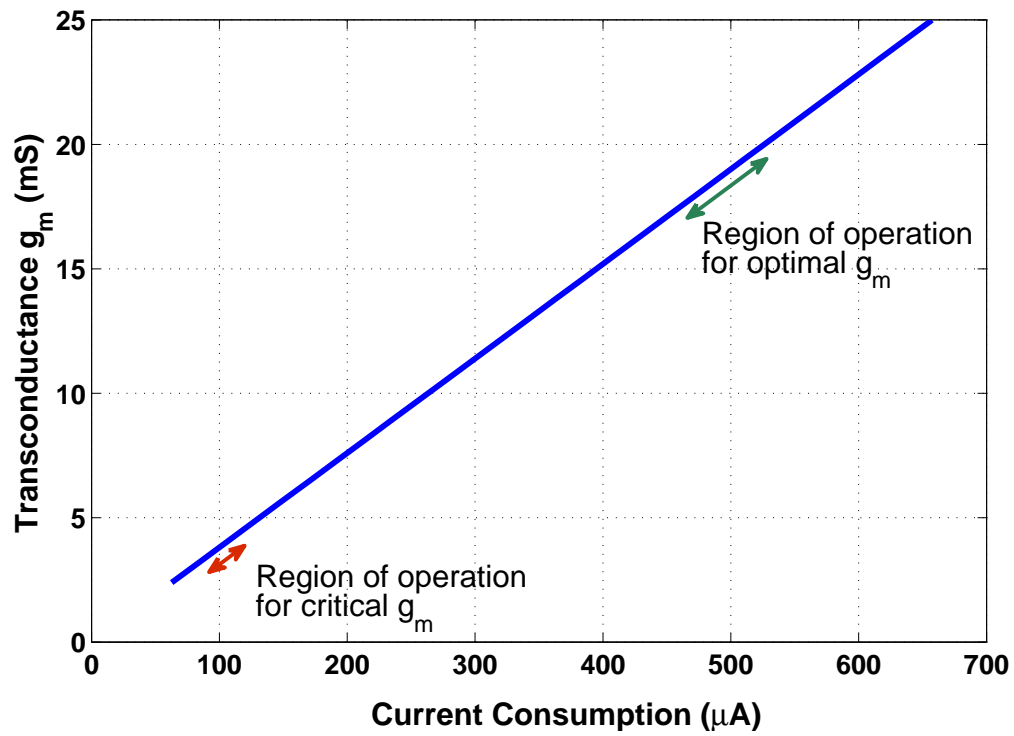
Figure 3-7: Bias current versus g_m

the following equation.

$$g_{m,crit} = \frac{C_1 C_2}{2 C_3^2 R_x} - \sqrt{\left(\frac{C_1 C_2}{2 C_3^2 R_x}\right)^2 - \frac{\omega^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2}{C_3^2}} \qquad (3.19)$$

For typical FBAR parameters, the critical transconductance $g_{m,crit}$ is around $3mS$. The current consumption is more reasonable in this region of operation. So, it is better to design closer to the critical transconductance than to the optimal transconductance when power consumption is critical.

Oscillation Amplitude: The oscillations will not keep on increasing forever. There are multiple effects that limit the oscillation amplitude:

1. Initially, when the amplitude of the oscillation increases, the gate drive on the transistors increases while the transistor is still in saturation. Since there is no current source limiting the amount of current being consumed, the current consumption increases. This causes the g_m to increase and aid in the oscillation buildup.

2. But, as the oscillation amplitude increases further, since the gate and drain are out of phase, $V_g - V_d$ will become lower than V_T and the transistors can go out of saturation. This causes the current consumption to reduce a little and eventually stabilize when the amplitude stabilizes. The output resistance of the transistors reduces. This adds to the losses in the system which, when sufficiently high, can cancel out the energy supplied by the circuit.

3. When the amplitude of oscillation of the gate voltage increases, the effective g_m of the transistors decreases. This large signal G_m is usually computed via simulations. By using describing function analysis [1],

$$G_m \approx \frac{4 I_{DC}}{V_{g,1}} \qquad (3.20)$$

where I_{DC} is the DC bias current and $V_{g,1}$ is the amplitude of the 1st harmonic of gate oscillation. So, the R_{circuit} changes as the amplitude increases as specified in Eqn 3.8. The oscillations stabilize when $R_{\text{circuit,large signal}} + R_x = 0$

Figure 3-8 shows the profile of the current consumption as the oscillation amplitude increases. Initially, the current rises sharply and then stabilizes.
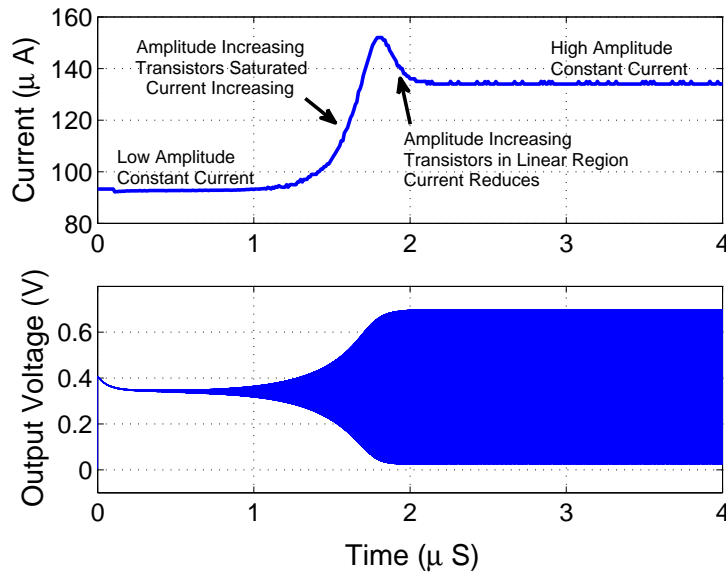
Figure 3-8: Oscillator startup current consumption profile

Because the current consumption in the circuit increases from the startup point and aids in oscillation buildup, the oscillator only needs to be biased close to $g_{m,crit}$ to begin with. The g_m increases initially to aid the oscillation buildup and eventually reduce again to the $g_{m,crit}$. This nature of the inverter-based Pierce oscillator enables the oscillations to usually build up almost rail-to-rail, even without fine-tuning the bias currents. The circuit starts off at a current close to the minimum required value, and increases such that the amplitude is also close to the maximum possible.

This optimization to reduce power consumption means that startup time is not the lowest possible. But, since the startup time is within the desired specifications, reducing power is more critical.

3.1.3 Loop Gain Analysis

A couple more insights can be gained from a loop-gain analysis for the oscillator. Also, it enables the use of a more complete model for the FBAR (the m-BVD model) and other circuit parasitics. Breaking the loop as shown in Figure 3-9, the loopgain is given by

$$\text{Loop Gain} \quad = \quad \frac{-g_m}{sC_1 + sC_2 + Z_{FB} \cdot sC_1 \cdot sC_2} \tag{3.21}$$

where Z_{FB} includes the actual FBAR impedance Z_{FBAR} and any bondwire inductances in the circuit.
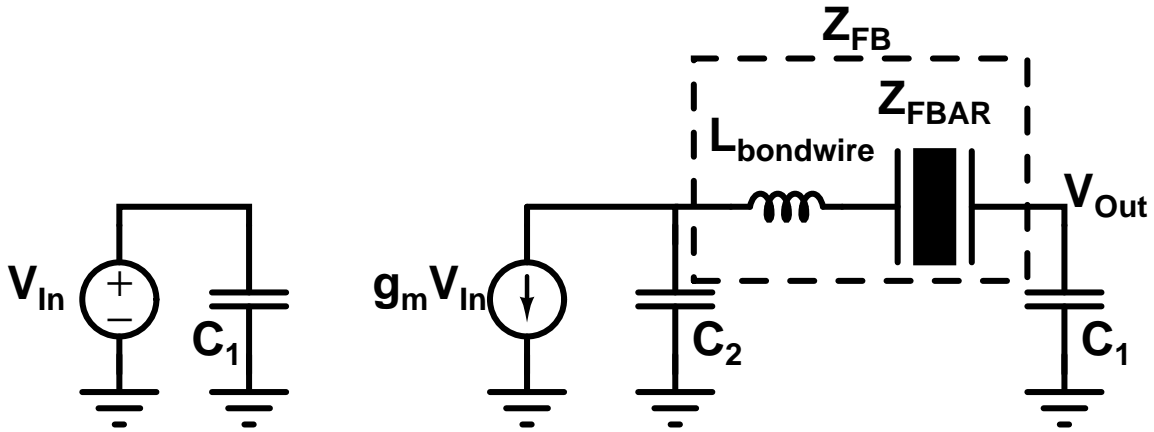
Figure 3-9: Circuit for loop gain analysis of Pierce oscillator

Assuming no bondwire inductance, the root locus is shown in Figure 3-10(a). This also shows that a critical g_m of around $3mS$ puts the poles of the circuit in the right half plane and thus lead to oscillations. But, in addition, it is useful to evaluate the effect of circuit parasitics. The most important of these is the effect of bondwire inductances. The root-locus of the pierce oscillator with a bondwire inductance of $0.3nH$ in series with the FBAR, in Figure 3-10(b) shows that with sufficient g_m, parasitic right-half plane poles can be created, which can cause undesired multi-mode oscillations, or even be the dominant oscillation [41].
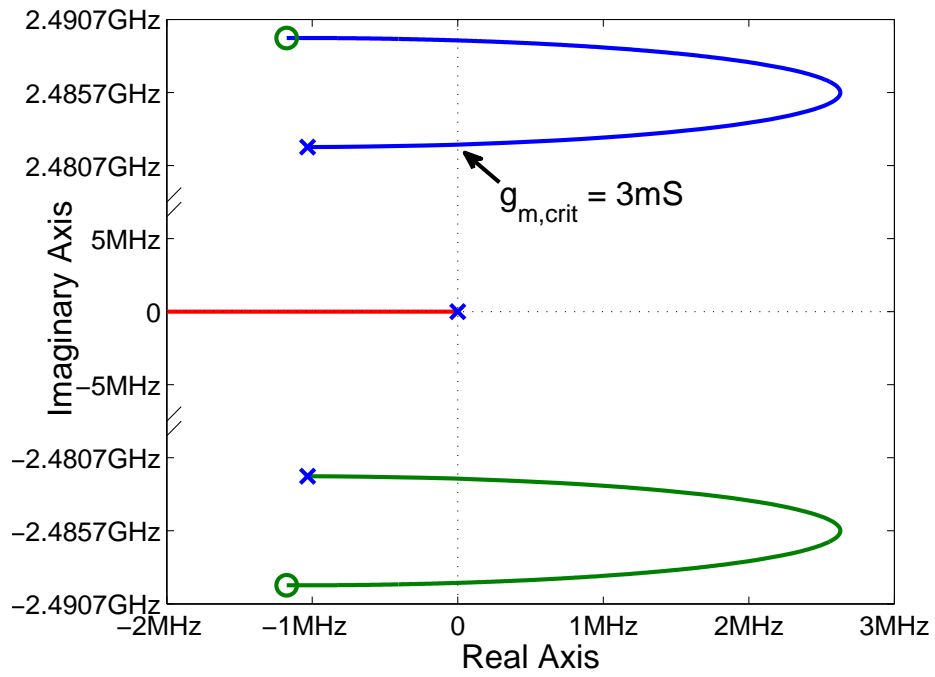
(a) Ideal Case: No bondwire inductance
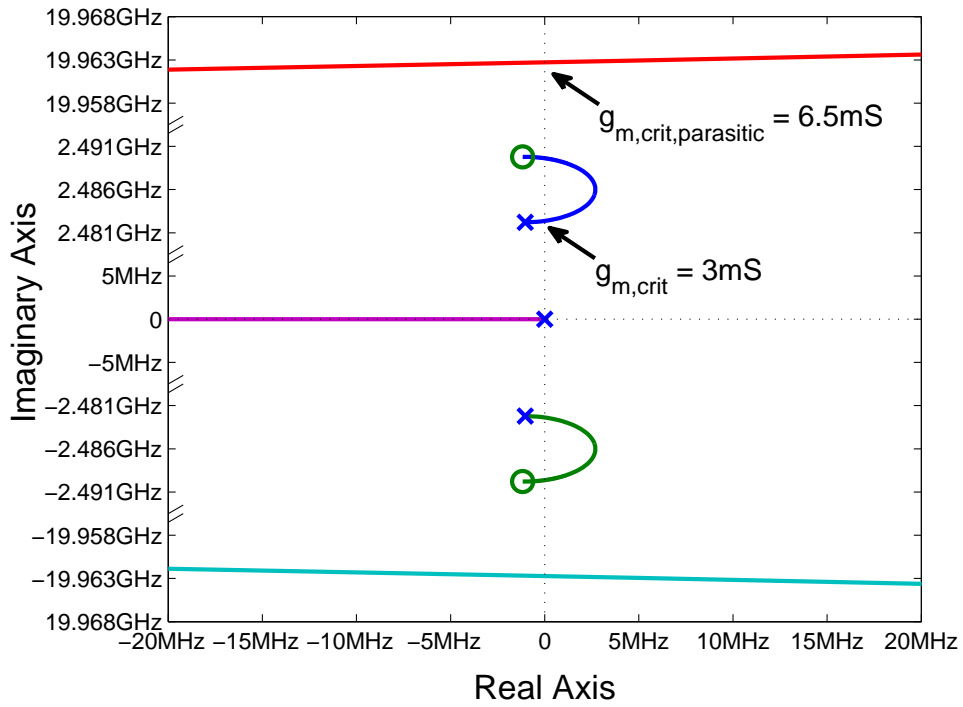
(b) With small bondwire $0.3nH$

Figure 3-10: Root Locus Analysis of Pierce Oscillator

In reality, the value of the bondwire resistance increases with frequency due to the skin-effect, and make the required g_m higher than is shown in the root-locus, which uses the resistance value for $2.5GHz$. But it is good to design the circuit with a better margin to prevent these oscillations.

A spectre simulation of the circuit, with a specific bondwire value[4], is shown in Figure 3-11. The value of the inductor is such that the parasitic oscillations start off faster due to the lower Q of the bondwire, but eventually the FBAR dominates and the final oscillation is only that of the $2.5GHz$ FBAR oscillations. The $g_{m,crit,parasitic}$ for the bondwire oscillations is higher than that of the FBAR oscillations. The startup g_m of the oscillator is chosen to be larger than $g_{m,crit,parasitic}$. In steady state, the large signal G_m is smaller than the $g_{m,crit,parasitic}$ of the bondwire oscillations, and they die out, leaving just the FBAR oscillations. The actual startup time of the FBAR oscillation in this case is much higher than usual because most of the energy provided by the oscillator is used up in sustaining the bondwire oscillations, and only a little energy is contributed to growing the energy in the FBAR. [41] also presents a good analysis of parasitic oscillations and 2-mode oscillations.

This shows that the bondwire inductance has to be made as small as possible, using either double bondwires, or thick bondwires, or use packaging techniques like flip-chip to mitigate the issue.

3.1.4   Final Design of the Pierce Oscillator

Choice of $V_{\mathbf{DD}}$:   The system $V_{\mathbf{DD}}$ of 0.7V is chosen mainly for the design of an efficient PA. But, this is also a good operating point for the oscillator as well.

1. The transistors are biased at $V_{DD}/2$, which is close to the V_T of the transistors. So, since they operate close to the subthreshold region, the trade-off of g_m versus current consumption is close to optimal.

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[4]Chosen to accentuate the effect, for the particular FBAR used in the simulation
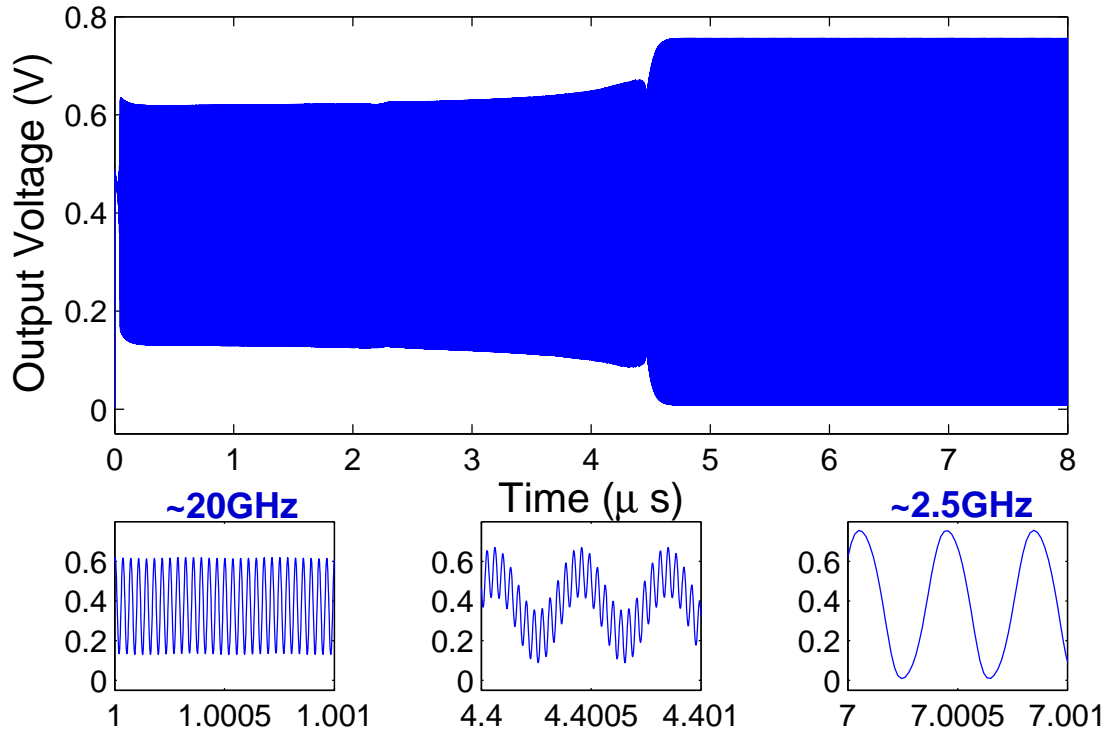
Figure 3-11: Transient simulation showing the effect of bondwire inductance

2. At lower V_{DD}s, this circuit can have a better g_m efficiency, but the signal swing is lowered. Since a common V_{DD} is desired for all blocks, this would mean lower swings for the PA, which affects its efficiency.

3. Higher V_{DD} would imply less g_m efficiency in the oscillator and also more difficult PA design for -10dBm (Section 3.4)

Transistor Sizing: The transistors are sized to be twice the nominal length to get a good output resistance and not add to the losses in the circuit. Also, for the V_{DD} of $0.7V$, the transistors are sized to provide a startup g_m of about $4mS$, which was sufficient to startup oscillations for the FBARs being designed for (as seen in the previous section, the $g_{m,crit}$ was 3mS), and provide near rail-to-rail oscillation. The sizing is such that $g_m > g_{m,crit}$ across corners. The exact value of the g_m is not

important. As long as it is greater than the $g_{m,crit}$, oscillations occur, and occur at the correct frequency. So, this design is robust to process variations.

The drain of the Pierce oscillator has the maximum amplitude since there is a voltage division from the drain to the gate. So, the drain voltage is used as the output of the circuit. This already loads the circuit and so, capacitance for frequency tuning of the oscillator is done with a capacitor bank at the gate of the oscillator.

Frequency Tuning and FSK Modulation: The oscillation frequency is given by Eqn 3.15, and it can be tuned by changing C_{circuit}. By adding a capacitor bank at the gate, C_1 is changed. A change in C_1 leads to change in C_{circuit} given by Eqn 3.9.

The bigger the size of the capacitor bank, the bigger the range of frequencies covered by the oscillator. Section 3.4.4 discusses the design of a capacitor bank. This shows that getting good Q for switched capacitors is difficult. This low-Q of the capacitor appears as a resistive load $R_p = \frac{Q}{\omega C}$ in the oscillator and increases the $g_{m,crit}$. So, the capacitor bank cannot be made too large without increasing power consumption significantly. The frequency tuning range must at least be such that FSK modulation is supported. In FSK modulation, the data is represented by the actual instantaneous frequency of the signal. The frequency deviation required is set by the datarate. The minimum required frequency shift to ensure orthogonality of the '1' and '0' waveforms, used in a specific form of FSK called Minimum Shift Keying(MSK), is 0.5 times the data rate [1]. So, the two frequencies required are

$$f_0 = f_{\text{center}} - \frac{\text{Data Rate}}{2} \tag{3.22}$$

$$f_1 = f_{\text{center}} + \frac{\text{Data Rate}}{2} \tag{3.23}$$

So, for supporting a Data rate of $1Mbps$, a tuning range of $> 500kHz$ would be required. Based on simulations of oscillators using the FBARs of this design, a capacitance bank of $150fF$ would be required. Gaussian pulse shaped MSK can

also be done with such a capacitor bank, as the bank settings can be changed at a up-sampled rate like 10MHz. This helps improve the spectral usage.

A 6-bit capacitor bank would require a step size of $2.3fF/step$. Getting a step-size lower than this with binary weighted capacitors is very difficult due to matching issues. This would provide a tuning accuracy of about $8kHz/step$. The main capacitor bank is designed as a binary weighted capacitor bank in a way similar to the banks used in the PA, as described in Section 3.4.4. Smaller capacitance steps are obtained by adding an additional 3-bit capacitor bank in series with a fixed 10fF capacitor. Because this is nonlinear, a thermometric coded capacitor bank is used here, designed similar to [18].

Figure 3-12 shows the full design of the capacitor bank.
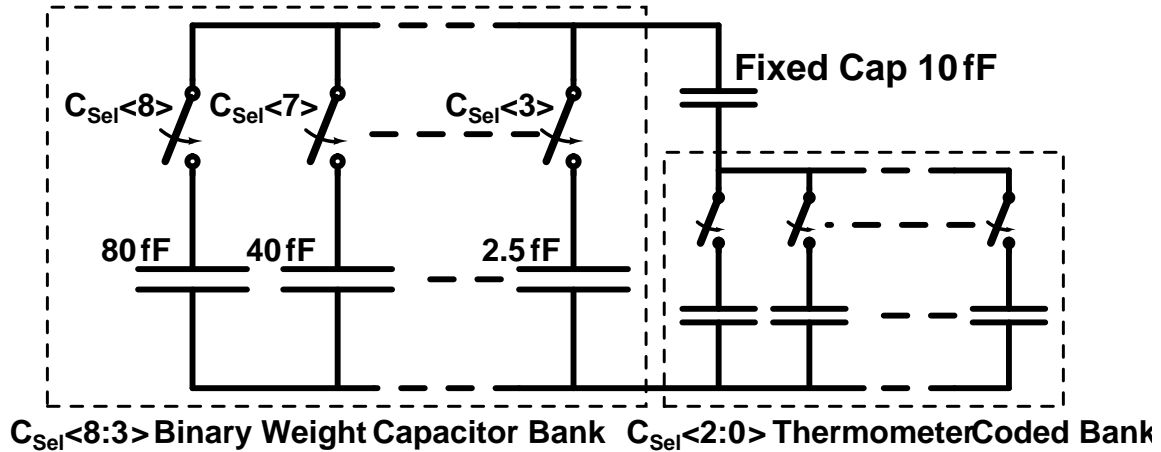
Figure 3-12: Capacitor Bank for oscillator tuning

Full Circuit   Figure 3-13 shows the full design of the oscillators. There are 3 oscillators that use 3 FBARs to define 3 different channel center frequencies and the FSK modulation of each. For each oscillator, when $Enable = 1$, the feedback resistor R_{fb} biases the oscillator and the oscillations begin. When $Enable = 0$, the biasing is disabled, and the gate is pulled up to V_{DD}.

In addition, a Resistor bank is used to do power control. If the FBAR is of a very
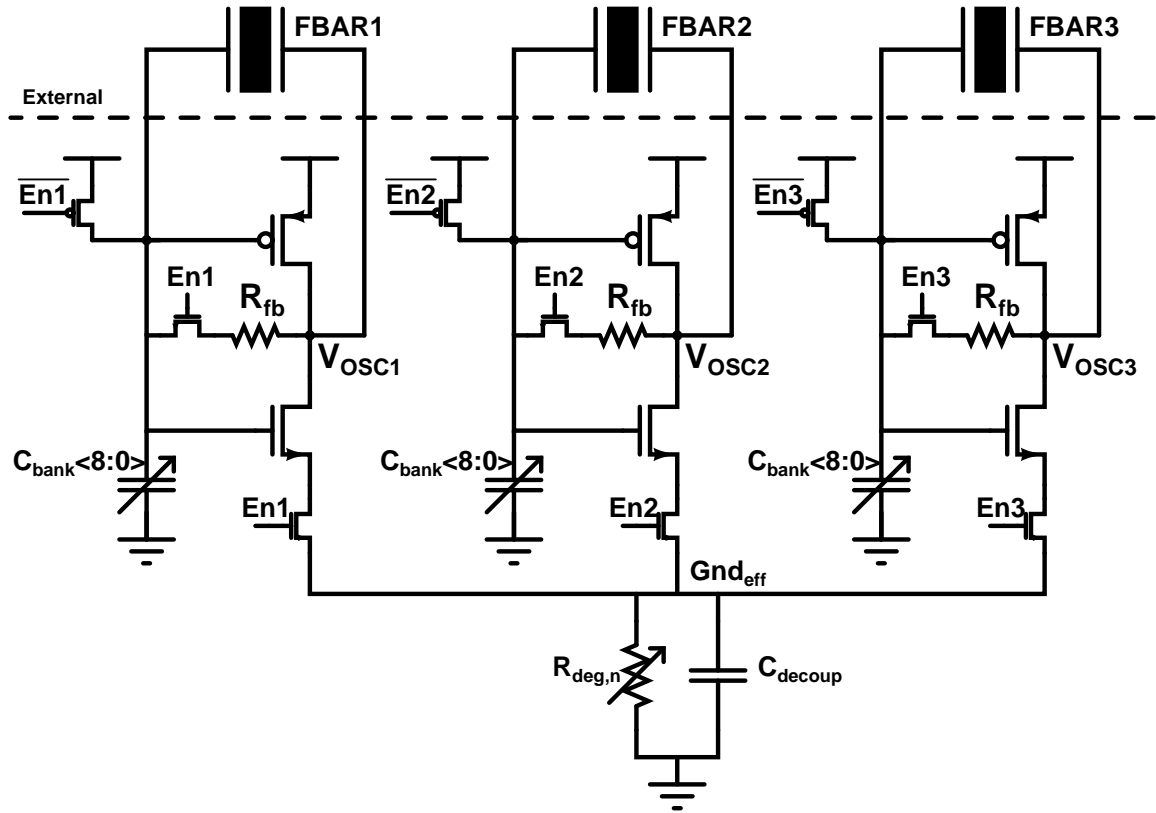
Figure 3-13: Full Implementation of the Oscillators

high Q, g_m can be reduced. So, increasing R_{deg} increases the effective Gnd_{eff} voltage seen by the oscillator and reduces the current consumption, and hence the g_m. The decoupling capacitor prevents the oscillator from seeing any ac resistive degeneration, which would reduce the g_m drastically. The resistor bank and decoupling capacitor is shared by all 3 oscillator channels in the design. Since only one oscillator is turned on at any given time, this is sufficient and reduces area consumption.

Phase Noise Performance

Due to the high Q of the FBAR, the phase noise performance of FBAR based oscillators is excellent. Typical phase noise performance of $-140dBc/Hz$ and $-138dBc/Hz$ at a $1MHz$ offset are reported in [34, 35] with very low power consumption. Also, since the modulation schemes being used are relatively simple, extreme phase noise

performance is not required. So, the design of oscillator is done only with ultra-low power consumption in mind and not to optimize phase noise performance. In spite of this, simulated phase noise of the oscillator is around $-145dBc/Hz$ at $1MHz$ offset.

3.2   Multiplexing and Channel Selection

The previous section discussed the design of the FBAR based oscillators used to generate the center frequencies for each channel. These signals have to be multiplexed before going to the Power Amplifier discussed in Section 3.4. [31] replicates the whole transmit chain to generate 2 channels of operation, but this method is not scalable. In the following, two methods of multiplexing are discussed. The trade-offs are discussed for this particular design, where the PA input capacitance is $200fF$.

3.2.1   Direct Multiplexing to the PA

Figure 3-14 shows a method to directly multiplex the oscillator outputs onto the PA. Transmission gate stitches are used because they present approximately a constant resistance at all input voltages [43] and because the input signals are large amplitude. The pros and cons of this method are discussed below
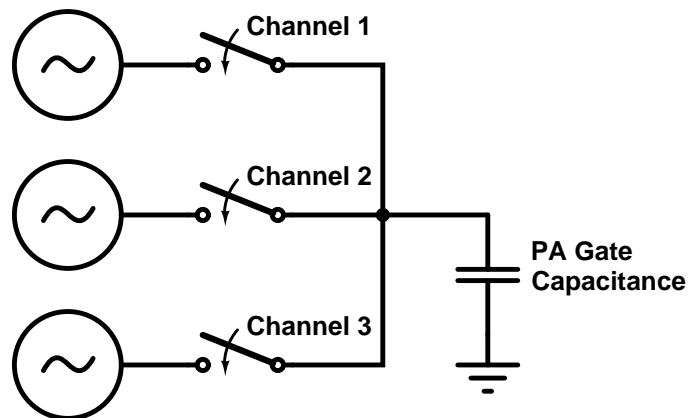

Figure 3-14: Direct multiplexing of Oscillators to PA

1. Given an ideal switch, the PA gate capacitance is in resonance with the oscillator, without any additional loss. The increased capacitance on the oscillator increases the g_m required to sustain oscillations, but the power overhead of multiplexing is quite low.

2. Using a real switch, there is a resistive loading on the oscillator as well, which will further degrade oscillator performance. Transforming the series R_{sw}-C_{PA} circuit into a parallel $R_{p,load}$-C_{PA} at the operating frequency [1], the resistive loading of the oscillator is given by

$$R_{\text{p,load}} \approx Q \cdot \frac{1}{\omega C_{PA}} = \frac{1}{\omega R_{SW} C_{PA}} \cdot \frac{1}{\omega C_{PA}} \qquad (3.24)$$

For the $200fF$ PA input capacitance, to get an effective R_{Load} of $5 - 10k\Omega^5$, would require a $Q \approx 20 - 30$. This would imply a switch resistance $R_{SW} \approx 10 - 20\Omega$. Getting such a low switch resistance is not possible without adding a significant additional capacitance from the switches. This in turn required smaller R_{SW} to maintain the R_{Load}. This scheme is thus limited by the self-loading of the switches. In the 65nm process used for this design, the drain capacitance of a 10Ω transmission gate switch is ≈ 60 fF which appears in parallel with the PA input capacitance. So, for three channels, the parasitic drain capacitance from the three switches is 180 fF, which is the same as the PA capacitance. So, this is not a viable method.

3. The input capacitance of the PA has a component from the C_{gd} of the transistors, which has miller multiplication. Thus, the capacitive load on the oscillator is variable and can cause the frequency to vary. This is not acceptable, and some isolation is required between the oscillator and the PA.

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[5]This resistance should be larger than the R_p of the FBAR itself so as to not affect the oscillations

3.2.2   Multiplexing with a Buffer

Figure 3-15 shows a circuit where the oscillator outputs are multiplexed onto a buffer which has a low input capacitance. The buffer then drives the high-capacitance PA.
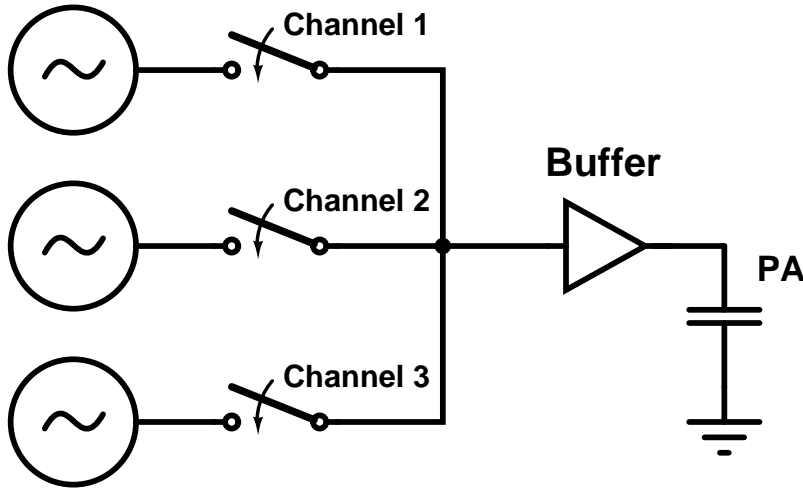
Figure 3-15: Multiplexing of Oscillators to PA with a Buffer

1. The switches in the Transmission gate can be quite small and, without any self-loading, provide a high R_{Load} to the oscillator

2. The oscillator sees a fixed load and is isolated from the PA

3. There is a power overhead involved in this method though, in the buffer.

Inverter Chain Buffer

If the buffer is implemented as an inverter chain buffer, the power consumption of this is

$$P_{\text{Inv Buffer}} > C_{PA} V_{DD}^2 f_c \tag{3.25}$$

which is just the switching loss of the load capacitance. This is $250 \mu W$ for the $200 fF$ PA with $V_{DD} = 0.7V$ and $f_c = 2.5 GHz$. In addition, there is a short circuit current through the inverters. So, the multiplexing problem is solved, but the buffer consumes a lot of power. This is addressed in the next section, by the use of a Resonant Buffer.

3.3 Resonant Buffer

The power consumption problem of the Inverter chain buffer is solved by using a resonant buffer, shown in Figure 3-16. The capacitor $C+\text{PA}$ is the input capacitance of the PA and C_{PAR} is the parasitic capacitance on the node, from routing. This resonant buffer circuit has the following advantages
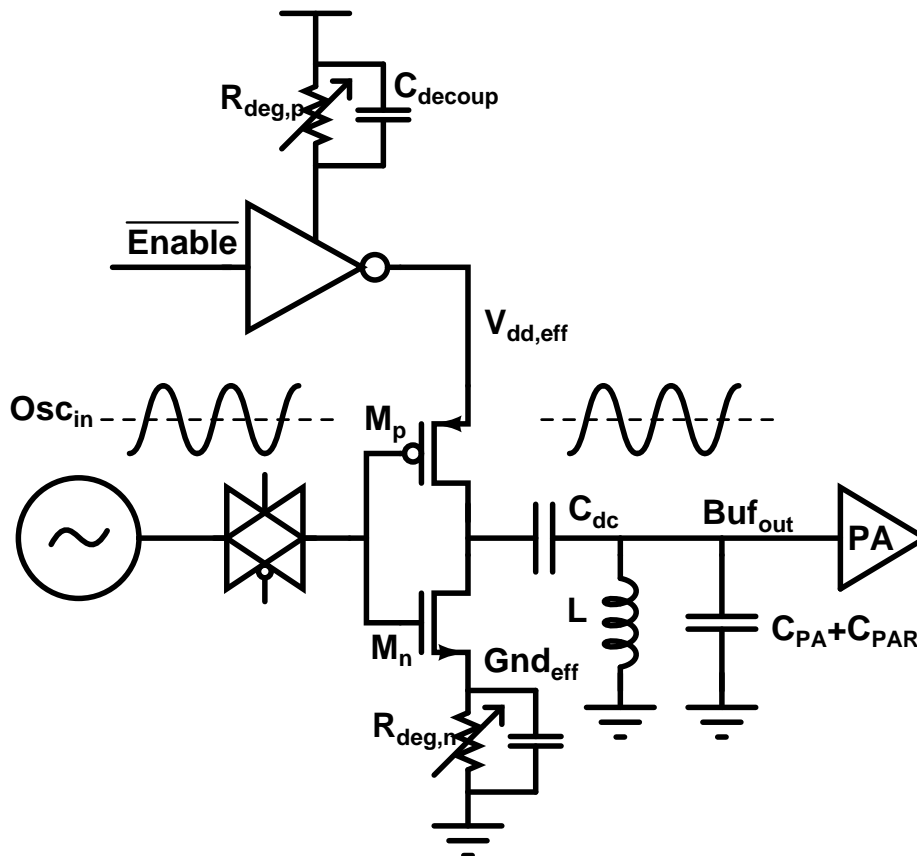
Figure 3-16: Resonant Buffer used in multiplexing Oscillators to the PA

1. Transistors M_n and M_p are the main buffer transistors. They form an inverter with the rail voltages of $C_{\text{dd,eff}}$ and Gnd_{eff}. The inverter doesn't need any biasing circuits. It relies on the fact that the oscillator output is centered at $V_{DD}/2$ to bias it. This also implies that the drain voltage is at $V_{\text{DD}}/2$.

2. The dc blocking capacitor C_{dc} is required because the drain of the inverter is at

$V_{DD}/2$ while the output is at 0V DC (due to the inductor).

3. Current-reuse helps reduce power consumption for a given g_m required.

$$g_{m,tot} = g_{m,n} + g_{m,p} \tag{3.26}$$

4. The load is a resonant load. The resonance occurs between the capacitance $C_{\mathrm{PA}+C_{\mathrm{PAR}}}$ and a inductor L. At resonance, the impedances of the L and C cancel and only the parasitic resistance of the inductor $R_{\mathrm{p,ind}}$ remains. So, the circuit doesn't need to provide any CV^2f power to the PA gate capacitance. It only needs to supply the energy dissipated in $R_{\mathrm{p,ind}}$, i.e, the energy dissipated in the resonant tank, .

$$P_{\mathrm{Buf}} = V_{\mathrm{DD}}I_{\mathrm{Short\ Circuit}} + \frac{V_{\mathrm{DD}}^2}{8R_{\mathrm{p,ind}}} \tag{3.27}$$

The short circuit current can be further reduced by biasing the two transistors at $V_{T,n}$ and $V_{DD} + V_{T,p}$ like it is done in the PA (Section 3.4), but in this case, the savings are only marginal and so is not implemented.

5. Since the load of the inverter is the large $R_{\mathrm{p,ind}}$, the size of the transistors M_n and M_p is very small. This leads to low power consumption in the circuit

6. A single stage of buffering reduces the input capacitance significantly. A sizing of 1:10 is done with respect to the PA transistors. The 20fF capacitance of the Buffer is easily interfaced with the multiplexer without loading the oscillators.

7. Power/Gain control is done using the resistors $R_{deg,n}$ and $R_{deg,p}$ and the decoupling capacitors. They reduce the effective V_{DD} seen by the Buffer. This is useful when the input amplitude from the oscillator is very high and low gain is sufficient in the buffer.

8. The buffer can be tristated by the $\overline{\text{enable}}$ signal.

Simulation Results

The buffer consumes $90\mu W$ from a $0.7V$ supply to buffer an input $260mV$ oscillation to $300mV$ output to the PA. This is $> 2.5x$ better than the inverter buffer.

3.3.1 Resonant Buffer with BPSK capability

[44, 7] describe a method of generating differential signals from a single ended oscillator output, for use in BPSK modulation. This circuit is implemented in the design as shown in Figure 3-17. The circuit uses 2 matched delay paths, a transmission gate and a inverter, to provide the two opposite phased outputs. The final stage of the circuit is a resonant buffer which can be tristated. The 2 resonant buffers in this circuit and the single stage resonant buffer of Figure 3-16 share the same inductor and drive the PA input. Since all three paths can be tristated, and the output is resonant, there is no power overhead to doing this. The Resonant Buffer stages of this circuit also have power/gain control like in Figure 3-16.
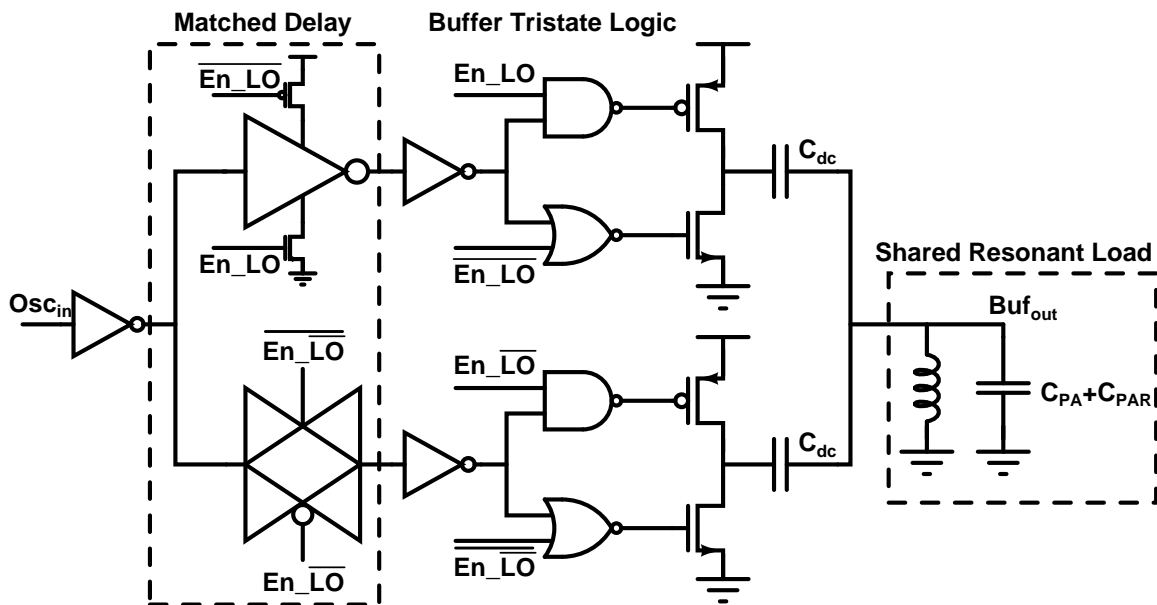
Figure 3-17: Resonant Buffer with capability to generate LO and $\overline{LO}$ for BPSK modulation

When $En\_LO = 1$, the path with the inverter is enabled. When $En\_\overline{LO} = 1$, the path with the transmission gate is enabled. Both paths can be turned off when no output is required, or when the other resonant buffer path (from Figure 3-16) is enabled. Both paths must not be turned on at the same time. The sizing of the inverter and transmission gate is done to get equal delay. The capacitive load of both paths is equal. So, the sizing must be such that the resistance is equal, to get equal rise and fall times.

$$R_{\text{TXGate}} = R_{\text{Inv,nmos}} = R_{\text{Inv,pmos}} \qquad (3.28)$$
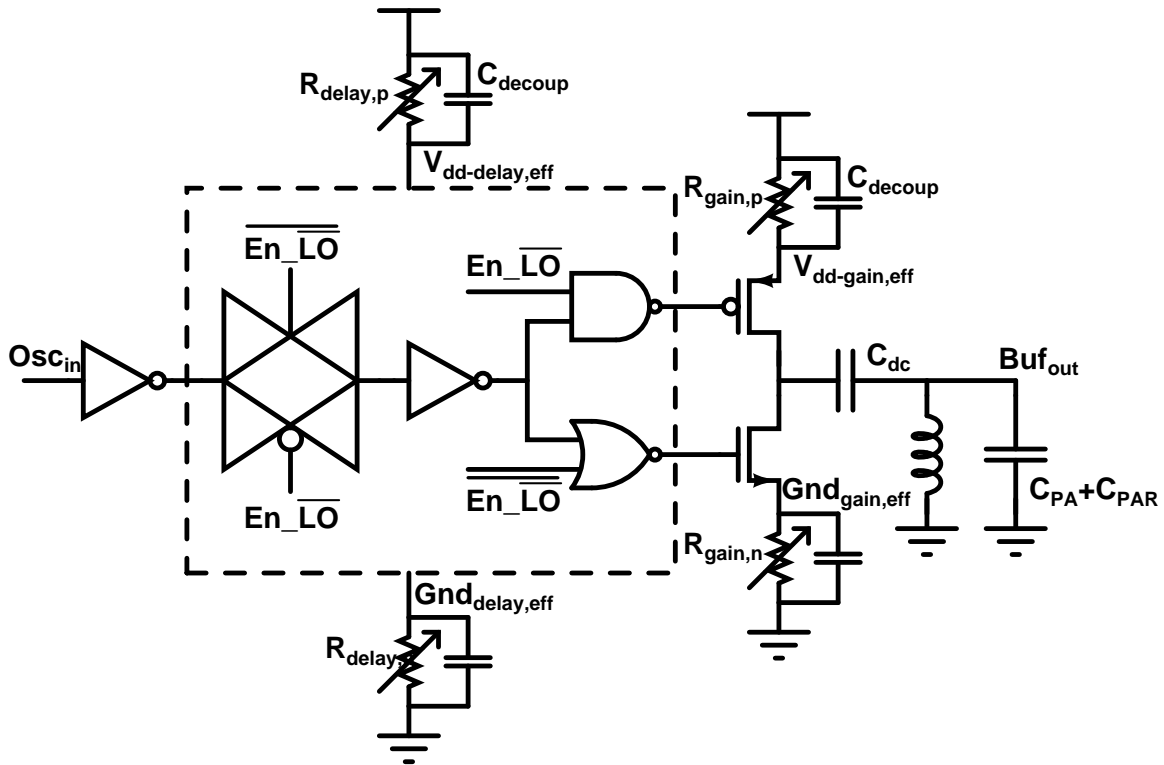
Figure 3-18: The circuit path for $\overline{LO}$ generation in Figure 3-17 expanded. It shows the scheme used to fine tune delay of $\overline{LO}$ by changing $V_{\text{DD-delay,eff}}$ and $Gnd_{\text{delay,eff}}$

The circuit also has some phase delay correction through the use of the resistive degeneration. This scheme is shown for the $\overline{LO}$ case in Figure 3-18. The same scheme is repeated for LO. These resistors reduce the effective V_{DD} seen by each inverter and hence change the delay of the circuit. The delay of any gate is given approximately

by [43]

$$t_{\text{delay}} \approx \frac{C\Delta V}{i_{\text{ds}}} \tag{3.29}$$

$$\text{Assuming Velocity Saturation} \approx \frac{CV_{DD}/2}{\nu_{sat}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{DD} - V_T - \frac{V_{DSAT}}{2}\right)} \tag{3.30}$$

$$= \frac{CV_{DD}}{2K\left(V_{DD} - \left(V_T + \frac{V_{DSAT}}{2}\right)\right)} \tag{3.31}$$

where $K = \nu_{sat}\mu_n C_{ox}$. Now, if V_{DD} changes by ΔV_{DD}, the gate delay changes by:

$$\Delta t_{\text{delay}} \approx \frac{C\Delta V_{DD}}{2K\left(V_{DD} - \left(V_T + \frac{V_{DSAT}}{2}\right)\right)} - \frac{CV_{DD}\Delta V_{DD}}{2K\left(V_{DD} - \left(V_T + \frac{V_{DSAT}}{2}\right)\right)^2} \tag{3.32}$$

$$\therefore \frac{\Delta t_{\text{delay}}}{t_{\text{delay}}} \approx \frac{\Delta V_{DD}}{V_{DD}} - \frac{\Delta V_{DD}}{V_{DD} - \left(V_T + \frac{V_{DSAT}}{2}\right)} \tag{3.33}$$

Let us define $\left(V_T + \frac{V_{DSAT}}{2}\right) = \alpha V_{DD}$. Then,

$$\frac{\Delta t_{\text{delay}}}{t_{\text{delay}}} \approx \frac{\Delta V_{DD}}{V_{DD}} - \frac{\Delta V_{DD}}{V_{DD}(1 - \alpha)} = -\frac{\alpha}{1 - \alpha}\frac{\Delta V_{DD}}{V_{DD}} \tag{3.34}$$

The total change in the delay through a circut with a series of gates is thus given by

$$\Delta t_{\text{delay,circuit}} \approx -\frac{\alpha}{1 - \alpha}\frac{\Delta V_{DD}}{V_{DD}}\sum t_{\text{delay,gate i}} \tag{3.35}$$

As can be seen from this, the shorter the delay of the stage, the less effect changes in V_{DD} has on the total delay. Also, delay in each stage is inversely proportional to the current consumed by the stage. So, the change in V_{DD} of the final resonant stage doesn't affect delay since it consumes the highest current. So, the final resonant stage's ΔV_{DD} is used only for power/gain control.

The $\overline{LO}$ path with transmission gate has only 2 gates and hence has low phase tuning, while the LO path has 3 gates and hence has more tuning range. For the implemented circuit, with tunable resistive degeneration of up to $2k\Omega$, a total tuning of 24° is achieved. Figure 3-19 shows the variation of delay between the two paths

when the resistive degeneration in tuned. This is sufficient to adjust for process variations.
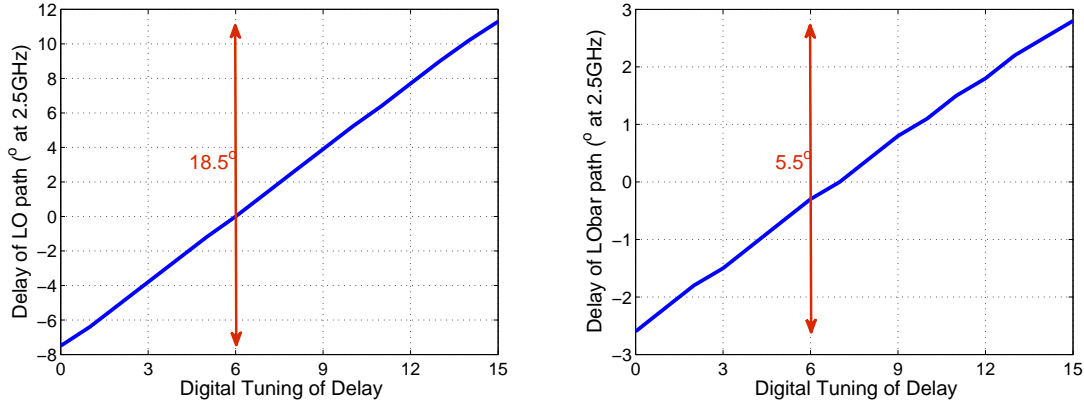
Figure 3-19: Delay tuning in (a)LO and (b)$\overline{LO}$ generation around nominal settings

In addition, for fixed delay settings (i.e, the nominal ΔV_{DD} settings), a Monte Carlo process variation simulation is performed to calculate the delay variations. A standard deviation of 2° is observed (See Figure 3-20), which is good enough by itself for BPSK modulation[6], and can be easily adjusted by the tuning bits.
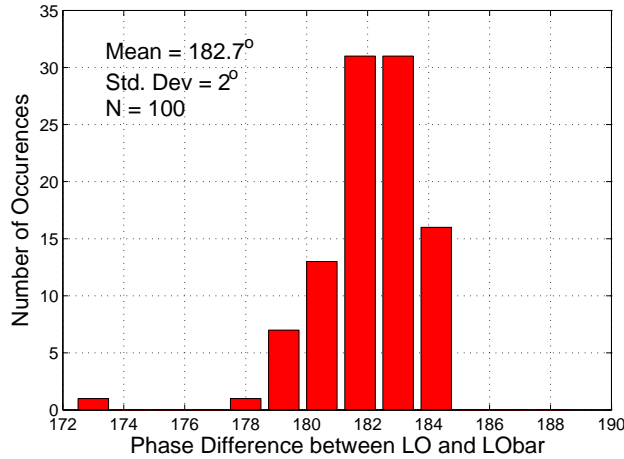
Figure 3-20: Monte Carlo process variation simulation result for the phase difference between LO and $\overline{LO}$

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[6]The IEEE802.15.6 Draft [2] proposes a EVM error of 20% for $\pi/2$ DBPSK which corresponds to a phase error of upto 11°

3.4 Power Amplifier

RF Power Amplifiers (PA) have the job of amplifying the RF signal so as to be transmitted onto an antenna. The PAs should ideally be 100% efficient and transfer all the energy it takes from a power supply, onto the antenna.

Antennas usually have an impedance of 50Ω, and for a particular output power level, the amplitude of the voltage on the antenna is specified. As was discussed in Section 1.4, in Body Area Networks, for the 1-2m communication, a transmit power level of $-10dBm$ is sufficient. Typically, PAs designed for cell phones need to support power levels of $20dBm - 30dBm$, and even bluetooth transceivers usually support a power of up to $4dBm$. So, power amplifier topologies have been developed and optimized to deliver these high power levels. So, when these PAs operate at low output powers like $-10dBm$, they operate in back-off, and are inefficient [15].

[22, 45, 19, 20] have PAs for wireless sensor networks and target a higher power level than is targeted in this design for a BAN. [30, 25] use output powers of -10dBm, but the efficiency is low, at around $< 30\%$. So, PAs that are very efficient and yet transmit low output power of -10dBm are explored.

3.4.1 Survey of PA Topologies

[15, 1] present an excellent review of PA design. Adapting the designs to operate optimally at $-10dBm$, a few insights can be gained. Firstly, on a 50Ω antenna, the output is an amplitude of $100mV$. Another point to note is that the peak output power of a PA is

$$P_{\text{out,max}} \propto \frac{V_{DD}^2}{R_L} \tag{3.36}$$

where R_L is the effective impedance seen by the PA. Also, all PA topologies are most efficient when operating at their peak power, which means that the PA must be optimal for $-10dBm$. This shows that either the V_{DD} has to be made really low, or R_L must be made very high.

Impedance Transformation

Use of matching networks to perform impedance transformation is a trick that is very useful in narrowband RF design. Matching networks have the property of transforming a real impedance to a different real impedance at a fixed frequency[7] [1]. This allows the transformation of to the 50Ω antenna to look like any desired impedance R_L at the frequency of interest.

From Eqn 3.36, we see that the peak output power of a PA is inversely proportional to the load resistance R_L. So. usually, when high output power is required, the 50Ω impedance is transformed to a lower impedance, but in the current design, since we want low output power, the impedance must be transformed higher. The following are some points to note in this case.

1. The higher the ratio of transformation of impedance, the higher is the Q of the transformation. For a higher Q transformation, the intrinsic quality factor of the inductors and capacitors in the network must be higher to get minimize the loss in the network itself. Also, the greater the Q of transformation, the narrower is the band of frequencies over which the match is good.

2. When the transformation ratio is very high, it is sometimes better to do the transformation in multiple steps, but this also degrades efficiency of the network, and leads to more area.

3. For transformation to high impedances, off-chip networks is not a good option, as will be shown in the next section, in spite of the better quality of passives available. This is because of the package parasitics.

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[7]It is a real impedance exactly at one frequency alone, but is approximately real over a narrow frequencies around this.

Effects of Package Parasitics

Figure 3-21 shows the equivalent circuit model for a QFN package, which is a popular package for high frequency designs because of lowparasitics. This is the package considered for the current design. The values of the parasitics are taken from [46] ($C_{\mathrm{pkg}} = 350\ fF$, $L_{\mathrm{pkg}} = 1.1\ nH$). For these values, and with a bondwire inductance of $1nH$, which is reasonable to expect, the effective impedance presented to the chip, as the off-chip R_{ext} varies, is also shown.

(a) Model of package parasitics (b) Impedance seen by circuit at 2.5GHz as R_{ext} varies
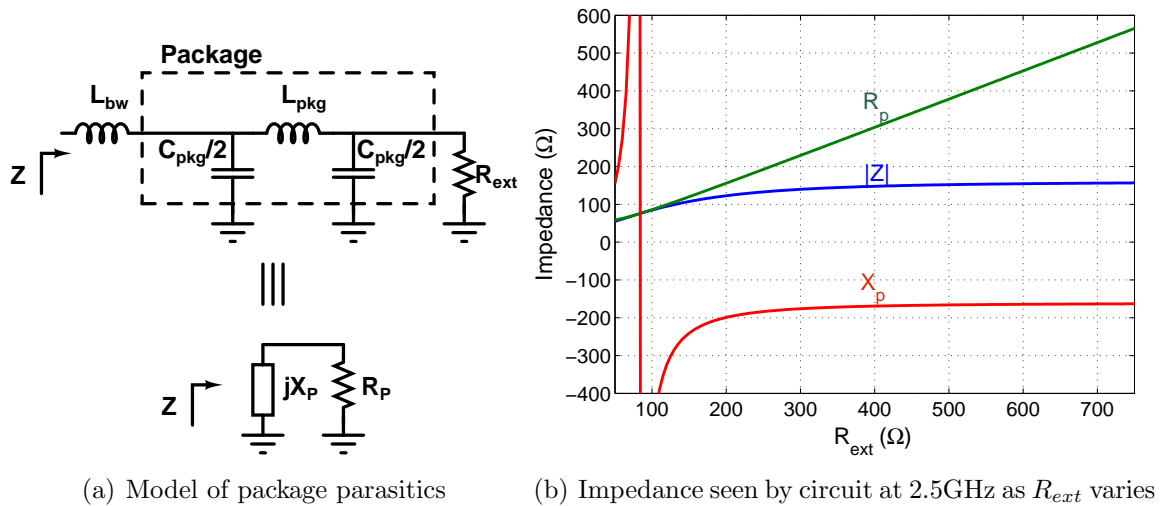
Figure 3-21: Effect of Package parasitics

What this shows is that the package parasitics highly degrade high impedances and pass low impedances (around 50Ω) without much change. Also, the lower impedances see an inductive component, while the high impedances see a capacitive component. On-chip capacitors can be easily used to tune out an inductance, but adding an on-chip inductor to cancel the effective capacitance would defeat the purpose of transforming impedance off-chip.

So, for circuits requiring transformation of 50Ω antenna impedance to a higher impedance, it is better to do it on-chip. Also, it is better to choose topologies that do not require very large impedance conversion.

Classic Linear PAs

Figure 3-22 shows the circuit for a Classic Linear PA, operating in either Classes A, B, AB or C. In this circuit, the drain of the PA swings from 0 to $2V_{DD}$ because of the choke inductor. The drain voltage waveform is also sinusoidal because of the filtering by the matching network. So, The peak output power is given by
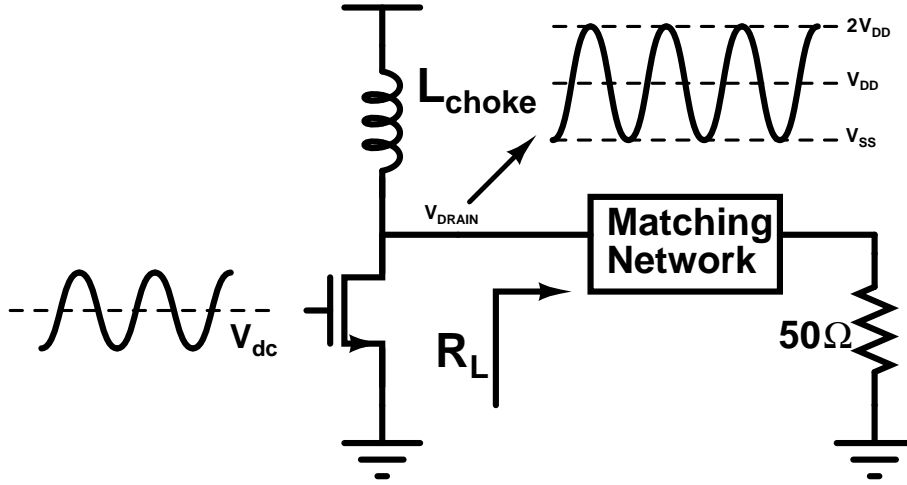
Figure 3-22: Class A, B, AB, or C Power Amplifier

$$P_{\text{out,max}} = \frac{V_{DD}^2}{2R_L} \tag{3.37}$$

For a $-10dBm$ output and a V_{DD} of $0.7V$, $R_L = 2.45k\Omega$. Transformation ratio required is around 50, which is very high and not practical. Also, for the choke inductor to work like a choke, i.e, carry only DC current and bypass all the AC current into the load, $\omega L_{\text{choke}} >> R_L$ with a ratio of about 10 that works well [1]. This would require L_{choke} of $1.5\mu H$ which is impractical at $2.5GHz$ even using off-chip components.

If a lower V_{DD} like 0.35V is used for the PA, $R_L = 612\Omega$ which is more manageable. Even here, $L_{\text{choke}} \approx 390nH$ which is still too high. So, these topologies do not work. In addition, if a fixed V_{DD} is to be used for the whole design, circuits driving the PA will not be strong and hence efficiency of the PA is degraded.

Similarly, Class E, F, etc PAs suffer from similar issues with values of the choke inductor, or extremely large transformation ratios.

Series LC Filters

Series LC filters are often used is PAs to reduce the loss of power in higher harmonics. Figure 3-23(a) shows its use in a Class A PA. It provides DC blocking, and since it is tuned at the frequency of operation, it presents a low impedance path to the load. At higher harmonics, the filter is of a high impedance, and doesn't pass any current to the load. This reduces harmonic content of the output and also improves efficiency of the circuit.

(a) Series LC filter in a ideal -10dBm Class A PA   (b) Parasitics of Series LC filters
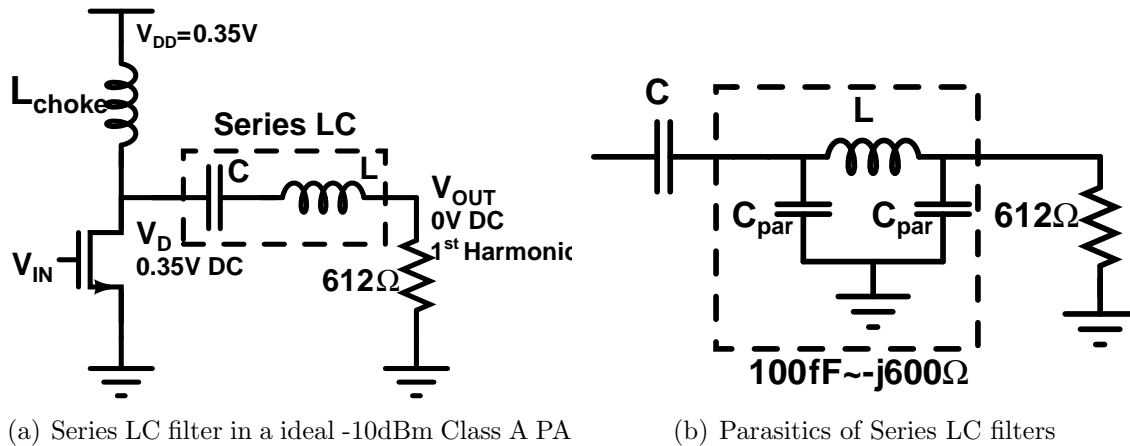
Figure 3-23: Series LC Filters do not work for high R_L due to inductor parasitics

But, Figure 3-23(b) shows the parasitics in the circuit. In particular, on-chip inductors have large capacitors to ground. Since a large impedance R_L is the load, the parasitic capacitor presents a lower impedance path and reduces efficiency drastically. For example, $100fF$ parasitic capacitance is $-j600\Omega$ at $2.5GHz$, which is of around the same value as the 612Ω R_L load. This is not an issue for high power PAs because R_L is low and the impedance of the parasitic capacitor doesn't effect performance.

This implies that series LC filters cannot be used in design of efficient $-10dBm$ PAs. This also eliminates the use of PA topologies like Class-F [1] which rely on such

filters to provide the high efficiencies.

Push Pull PAs

In contrast to the other topologies, Push Pull PAs are much more amenable to design of low power PAs. Figure 3-24 shows such a circuit. The drain node swings only from $0V$ to V_{DD}. If the input drive is strong with square wave or high amplitude sinusoids, the PA operates as a Class-D PA, offering very high efficiency. If the drive is relatively weak, with sinusoidal input, it operates as a Push Pull Class B amplifier.
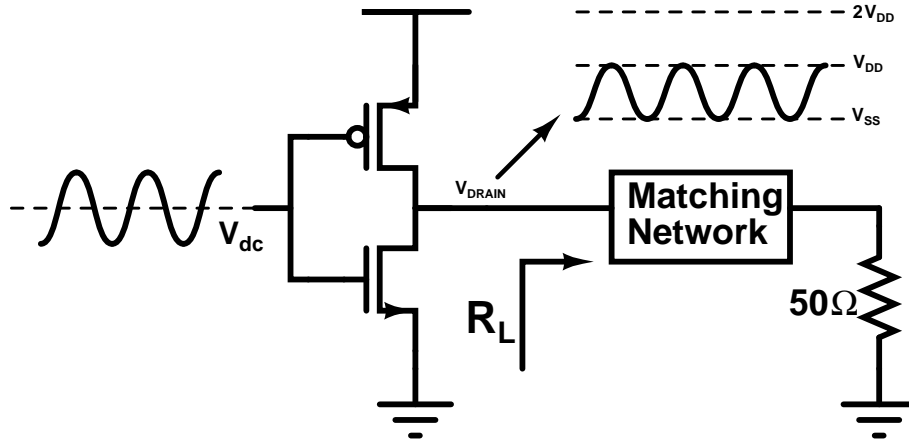
Figure 3-24: Push Pull Power Amplifier¡

Since the buffer is resonant (Section 3.3), the input to the PA is sinusoidal, and so, square wave input is not an option. High amplitude sinusoidal drive can also give class-D operation. But, since a series LC filter cannot be used to filter out the higher harmonics, Class-D operation is not preferred.

So, Class-B operation for the Push Pull PA is considered for further analysis. The drain voltage is a sinusoid of amplitude $0 - V_{DD}$ at peak efficiency operation. The output power is given by

$$P_{\text{out,max}} = \frac{V_{DD}^2}{8R_L} \tag{3.38}$$

For the same V_{DD}, a much lower output power is provided. For 0.7V supply, a $-10dBm$ output requires $R_L = 612\Omega$. Operation at 0.7V is quite attractive because

now, the whole system can be run at the same voltage, and be efficient everywhere. [19] uses a power amplifier with 4 transistors in series to provide similar benefits for low output power generation, but it was done for a high supply voltage operation, and such stacking will be inefficient at supplies like 0.7V.

The Class-B Push Pull PA is thus chosen as the topology for this design.

3.4.2   Pulse Shaping

Pulse shaping is used to improve the spectral usage of transmitters. Standards usually specify the amount of adjacent channel spectral content. So, for a given channel bandwidth, using pulse shaping, the maximum datarate of transmission can be increased. This is useful, since it improves the energy per bit transmitted. For MSK data, Gaussian pulse shaping is often used, yielding GMSK. GMSK still maintains the constant envelope and hence, non-linear PAs can be used.

For OOK data, Gaussian pulse shaping can again be used. But here, the envelope of the waveform is not constant (when ON) and hence requires a PA with good linearity. This also means that the PA operates at lower than $P_{\text{out,max}}$ for a large time and the effective efficiency is deteriorated.

Similarly, for BPSK, Square Root Raised Cosine (SRRC) pulse shaping is usually used. Again, the envelope is not constant and the PA can be quite inefficient.

When using the linear PAs for pulse shaped output, another problem is that a linear mixer is required to provide the pulse shaped signal to the PA. An active mixer would be required, which would lead to increased power consumption.

There are a few ways that this problem has been solved in the literature. [15, 1] discuss these techniques. Doherty technique extends the region of good efficiency by adding in a second PA when high power levels are required. Chireix outphasing combines the power output of 2 PAs running in parallel and controls the total output power by controlling the phase of the outputs of the PAs. This effectively modulates the impedance seen by each PA. This method is effective, but at low power levels,

the individual PAs must be of even lower power. This will result in higher impedance transformations and/or lower V_{DD} operation which are undesirable.

Kahn technique or Envelope Elimination and Restoration (EER) is a technique that is used to improve efficiency. A non-linear PA is used. It is given a input that is only phase modulated. The envelope information is fed into a power supply modulator that modulates the supply voltage of the PA. Thus, the PA always operates at its peak efficiency and the output has all the amplitude information required.

The supply voltage has a squared dependence on the output power and is thus a very effective technique of modulating output power. The supply voltage modulator needs to operate at relatively low frequencies and hence requires large passive components (which need to be off-chip) and the overall efficiency is the product of the efficiencies of the intrinsic PA and the supply modulator. This can be degraded by nonidealities in the supply modulation. Also, at low output power levels, the power overhead of controlling the supply modulator can be significant. So, the Kahn technique is not a preferred solution in the current design.

3.4.3 Pulse Shaping and Power Control Using a Tunable Matching Network

The Push Pull PA is most efficient when operating at its peak output power, which is when the input amplitude is large enough. The output power is determined by R_L through Equation 3.38. The output power can thus be controlled by controlling the R_L presented to the PA explicitly. This can be done by changing the matching network to transform the 50Ω antenna to varying impedances. For example, if the impedance is changed in an analog way, the envelope waveform can be directly sent to the tunable matching network. On the other hand, if R_L can only be changed in steps, a scheme like the one shown in Figure 3-25 can be used.

For a L-match, once the value of the inductor is fixed, the impedance transformation ratio is fixed. Since tunable inductors on-chip are not practical, this matching
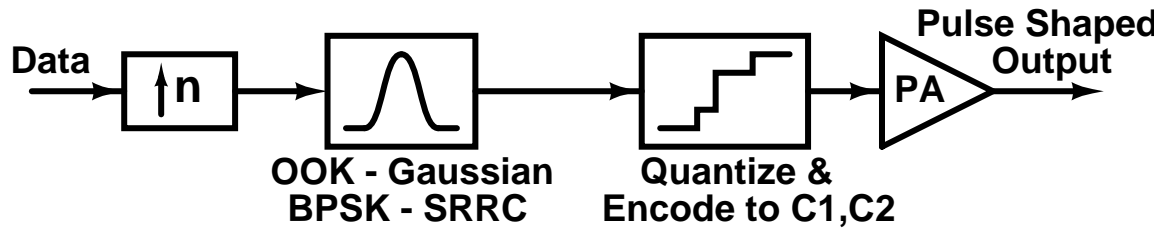
Figure 3-25: Method of pulse shaping for a PA with discrete output power levels

network cannot be used. A matching network with more degrees of freedom is required. Figure 3-26 show two such matching networks, the tapped capacitor match and π-match. Only these are considered because they can absorb the pad capacitance into the matching network without additional impedance conversion steps. These are compared below.

(a) Tapped Capacitor Match

(b) π-Match
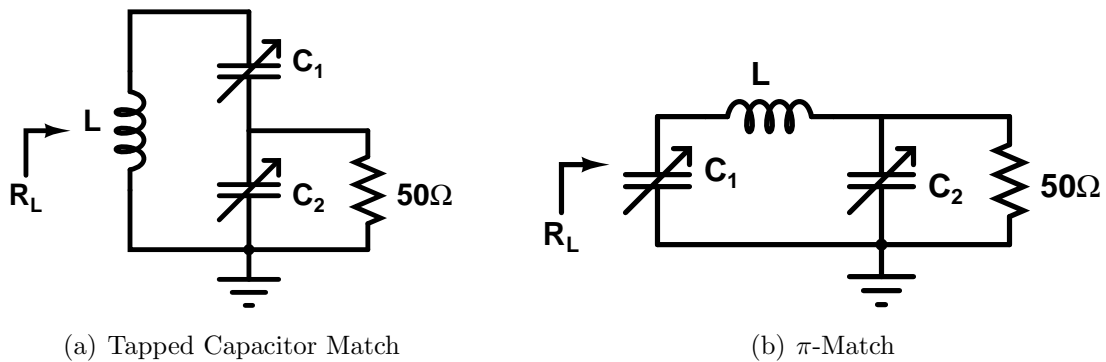
Figure 3-26: Tapped capacitor match and π-match, two matching networks with extra degrees of freedom

For the **Tapped-Capacitor Match**, with a fixed inductance L, the following design equations are derived for narrowband operation using series-to-parallel and

parallel-to-series impedance transformation formulae from [1]:

$$Q_2 \;=\; \omega \cdot C_2 \cdot 50 \tag{3.39}$$

$$C_{2,s} = C_2 \cdot (Q_2^2 + 1) \quad , \quad R_s = \frac{50}{Q_2^2 + 1} \tag{3.40}$$

$$C_{s,\text{eff}} \;=\; \frac{C_1 C_{2,s}}{C_1 + C_{2,s}} \tag{3.41}$$

$$Q \;=\; \frac{1}{\omega \cdot C_{s,\text{eff}} \cdot R_s} \tag{3.42}$$

$$C_{\text{eff}} = \frac{C_{s,\text{eff}}}{Q^2 + 1} \quad , \quad R_L = R_p = R_s \cdot (Q^2 + 1) \tag{3.43}$$

$$\omega^2 \;=\; \frac{1}{L C_{\text{eff}}} \tag{3.44}$$

$$\text{From above, } R_s \approx \frac{(\omega L)^2}{R_p} \tag{3.45}$$

For any required R_L, the values of the capacitors C_1 and C_2 can be calculated from the equations above. The parasitics in this circuit are the parallel resistance of L and resistance of the switches used in capacitor banks for C_1 and C_2. L must be chosen to have the largest parallel resistance because it degrades the efficiency of the circuit by a factor of $\frac{R_{p,ind}}{R_{p,ind}+R_L}$. $R_{p,ind} = Q_{ind} \cdot \omega L$, so, higher inductances are in general better. At the same time, $R_s < 50$, hence, from Eqn 3.45 L cannot be made very large. Also, resistance of C_1 and C_2 must be made much smaller than R_s to maintain efficiency. In this design, a $L = 6.44nH$ was chosen as a trade-off between high $R_{p,ind}$ and tuning range. Table 3.1 lists the values of C_1 and C_2 for conversion of 50Ω to various impedances. The range of impedances is chosen from 300Ω to $1.2k\Omega$ to get a range of output powers around the nominal $-10dBm$ (600Ω)

For the π-**Match** again, with a fixed inductance L, C_1 and C_2 must be chosen. Similar design equations can again be written. Table 3.2 shows the required values of C_1 and C_2 for the same range of impedances of 300Ω to $1.2k\Omega$.

The values of capacitors required in the design for both type of matching networks are similar. Also, both circuits require a input with a DC value of 0V, so, a DC

$L(nH)$	$C_1(fF)$	$C_2(fF)$	$R_L(\Omega)$
	958	1012	300
	890	1460	450
6.44	851	1807	600
	805	2366	900
	779	2820	1200

Table 3.1: Design of Tapped Capacitor Match for Variable Impedances, at 2.5GHz

$L(nH)$	$C_1(fF)$	$C_2(fF)$	$R_L(\Omega)$
	774	1498	300
	784	2024	450
6.44	777	2399	600
	760	2977	900
	746	3438	1200

Table 3.2: Design of π-Capacitor Match for Variable Impedances, at 2.5GHz

blocking capacitor is required between the Push-Pull amplifier and this matching network. Because it goes to GND, the inductor in a tapped-capacitor match can be easily implemented using high-Q bondwire inductors, even though it is not used in this design because of its variability. In simulations, the π-match network had a poorer performance in terms of losses in the network. More importantly, the phase of the voltage at the output with respect to the phase of voltage at the input behaved quite differently between the two networks. Figure 3-27 shows this angle as R_L varies for the two networks. The tapped capacitor match has an angle variation of about 13° while the π-match has a variation of about 30°.

For OOK Modulated data, even if the phase changes during the pulse shaping, the receiver does not get affected since it only cares for the total energy in the bit, but for BPSK, large phase changes will result in poor EVMs and degrade performance of the link. For this reason, the Tapped-capacitor match is chosen in this design.

Note on power overhead: Ideally, if the tunable matching network has no loss, the only power overhead of the circuit is for driving the switches in the capacitor bank on/off. Since this occurs at a very low frequency ($\approx 10 \cdot$ Data Rate), the power
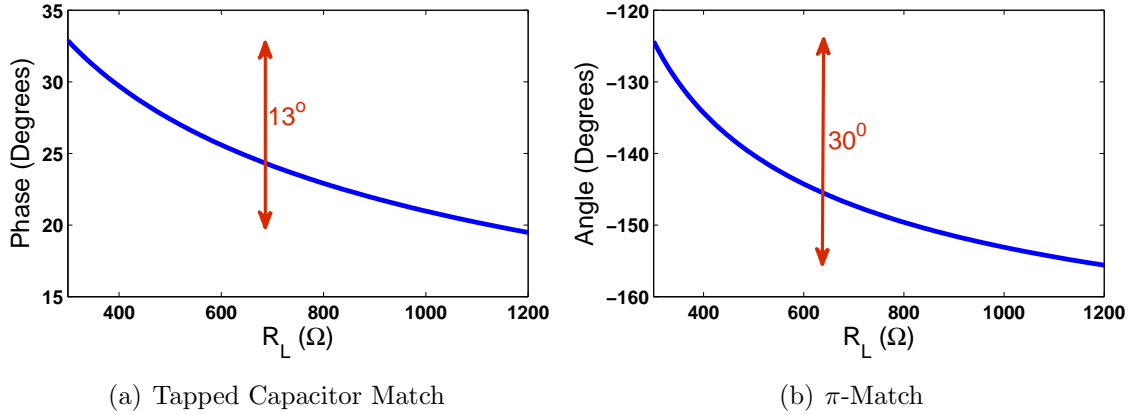
(a) Tapped Capacitor Match   (b) π-Match

Figure 3-27: Variation of phase of output with changing impedance settings for tapped capacitor match and π-match

is negligible. In reality, the presence of the switches in the matching network leads to degradation of the Q of the capacitors, which degrades the PA efficiency. So, care has to be taken in designing the capacitor banks in the tunable matching network, to maintain their Q.

3.4.4 Design of Capacitor Banks

The capacitors C_1 and C_2 of the tapped capacitor matching network are designed as digitally controlled banks. The goal is to make each capacitor of the highest Q possible. Each capacitor has a fixed capacitance in parallel with a binary weighted bank of capacitors. A 5-bit capacitor bank is designed for C_1. C_2 is designed with 7 bits because of the larger range of values.

Figure 3-28 shows a capacitor with a switch and its parasitics. $C_{\mathrm{par}} = C_{\mathrm{bottom\ plate}} + C_{\mathrm{ds}} + C_{\mathrm{routing}}$, of which $C_{\mathrm{bottom\ plate}}$ and C_{ds} scale with the capacitor value and switch size respectively.

$$C_{\text{Switch ON}} \approx C + C_{\text{par2}} \quad , \quad Q_{\text{Switch ON}} \approx \frac{1}{\omega R_{Switch} C} \tag{3.46}$$

$$C_{\text{Switch OFF}} \approx C_{\text{par}} + C_{\text{par2}} \quad , \quad Q_{\text{Switch OFF}} \approx \infty \tag{3.47}$$
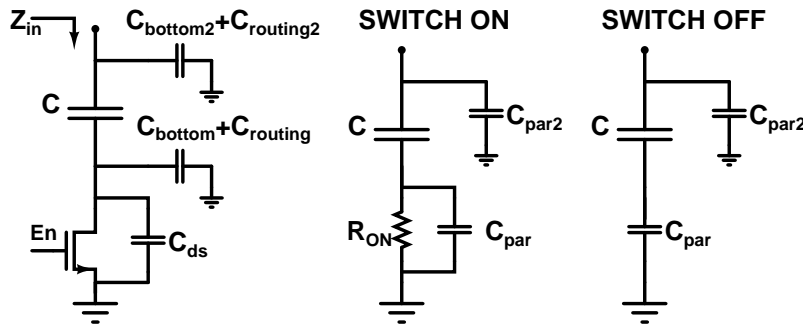
$$C_{\text{Step}} = C - C_{\text{par}} \tag{3.48}$$

Figure 3-28: Design of Capacitor Bank

So, to get a linear capacitor bank, C_{par} must scale with C. The C_{ds} part of this will scale with C if the switch size is scaled along with it. This also leads to a constant-Q switched capacitor. The off-state capacitance is C_{par} and adds to the explicit fixed capacitor. The effective Q of the capacitor bank is thus highest at small digital codes and degrades at higher digital codes.

To minimize C_{ds} for a given switch resistance R_{switch}, a boosted voltage of 1V is used to drive the the switches. The power consumed by this boosted supply is only due to low frequency (upto 10MHz pulse shaping frequencies) charging and discharging of the gate capacitance of the switches. This is very small. For example, a $1pF$ capacitance switching at 10MHz requires only $10\mu W$ at 1V. In this implementation, the 1V supply is provided off-chip, but can easily be implemented using charge pump circuits. Figure 3-29 shows the simulated capacitance values and Q for C_1, with C_2 being quite similar.
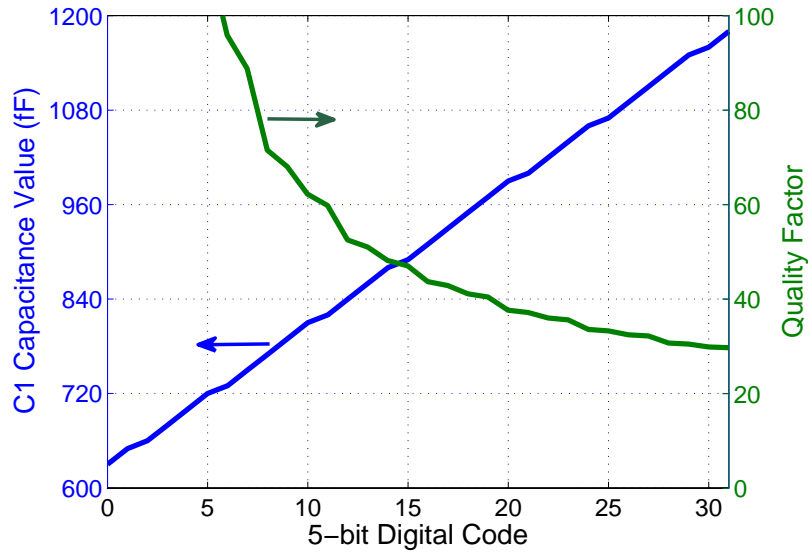
Figure 3-29: Characteristics of Capacitor Bank C1

3.4.5   Final Design of the Power Amplifier

Putting together all the principles discussed in the previous subsections, Figure 3-30 shows the full design of the PA.

1. The gates of the PMOS and NMOS are biased by separate resistive divider DACs through R_{bias}. This is set at the respective V_Ts to minimize the shoot-through currents.

2. The RF input from the buffer is ac-coupled through capacitors to the gates of the PA.

3. The PA can be both turned off by biasing the transistors at V_{DD} and GND respectively. This is used for OOK modulation. To support 1Mbps datarates, the time constant of turning on/off the bias must be around $100ns$. Small R_{bias} will result in a low-Q capacitive load to the buffer and increase its power consumption. A small coupling capacitor will result in capacitive voltage division with the gate capacitance of the PA. The sizing is done taking this trade-off into account.
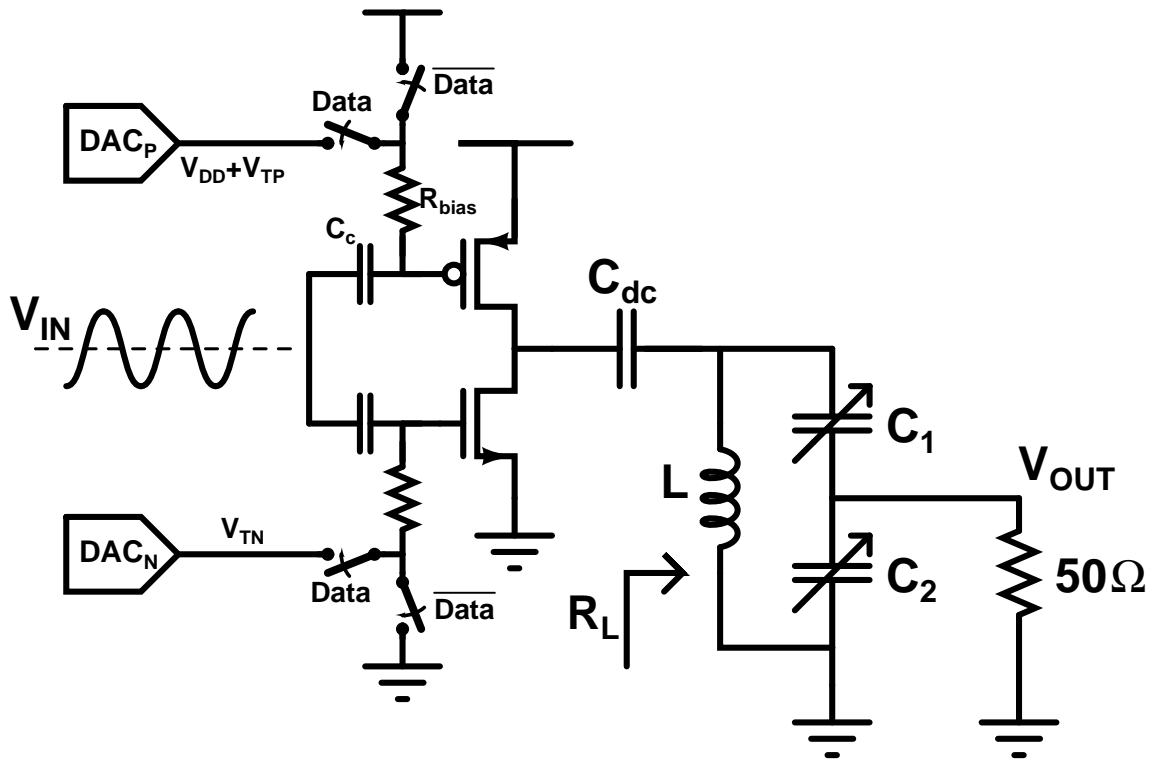
Figure 3-30: Full Design of the -10dBm Power Amplifier

4. The actual transistors in the PA are sized as a trade-off between on-resistance, output resistance r_{ds}(which is a loss), and so as to operate with the the various load resistances R_L presented by the matching network.

5. Only a dc-blocking capacitor is used to interface the PA to the matching network rather than a series-LC filter as was discussed in Section 3.4.1. This is sized to provide minimal capacitive dividing at the fundamental harmonic while keeping the bottom-plate capacitance low.

6. The tapped-capacitor matching network is designed to present impedances from 300Ω to $1.2k\Omega$ to the PA. This provides a 6-dB output power range just from the matching network, which is sufficient to generate pulse-shaped OOK and BPSK outputs.

3.5   Layout and Floor-planning

Because the circuit has to interface with FBARs, floor-planning is very important. Figure 3-31 shows the layout of the RF Core circuits of the transmitter. The three oscillators are placed along the perimeter of the chip on the left. Since the outputs of the oscillators are resonant, they are routed along relatively long traces to the multiplexer and buffer. These circuits are laid out with care to minimize parasitics, especially for the circuits used to generate the BPSK signals[8], (Section 3.3.1). The buffer output is again resonant and is routed along a relatively long path to the PA input. The PA, along with the tapped-capacitor match is laid out to minimize parasitics. The PA output is close to the edge of the chip so that the output trace is short.
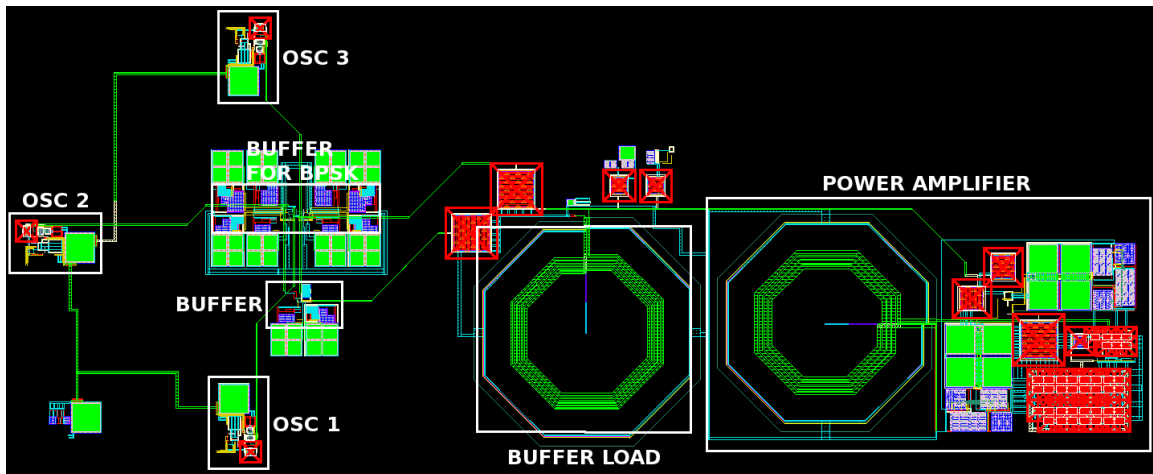

Figure 3-31: Layout of the RF core circuits

Wherever there is a long resonant trace, a return ground path is provided on the lowest metal line to minimize losses. This is explained using Figure 3-32. If no ground trace is placed on the lower metal, the substrate resistance and substrate capacitance are in series with the C_{trace}. These are highly dependent on the layout and location of the closest substrate tap, and are difficult to model without EM simulations. So, the

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[8]Some of these nodes are not resonant

Q of C_{trace} is unknown and could cause losses in the resonance. On the other hand, if a ground trace is drawn on the lowest metal, the capacitance is slightly higher, but the Q of the capacitor is high and losses are minimized. This is similar to the use of patterned ground shields in inductor design [1].
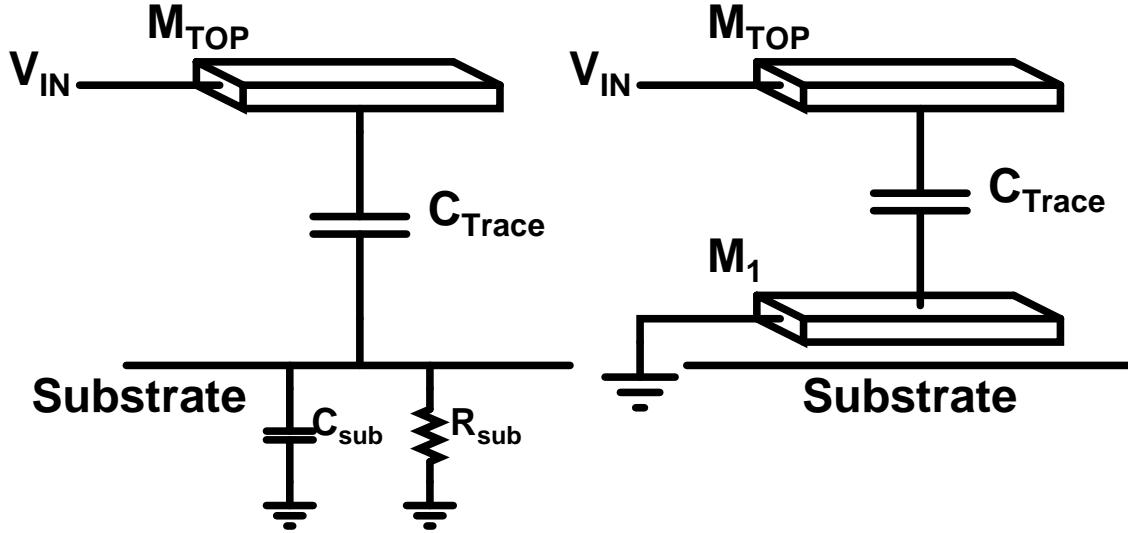

Figure 3-32: Need for return ground path on long resonant paths

Post-layout extraction results in a lot of parasitic capacitances on the resonant nodes, especially the buffer output and the PA. The inductor values are adjusted to recenter the resonance in the frequency of operation. This is critical since resonance is what leads to the low power operation of the circuits.

$$j\omega L_{\text{pre-extraction}} = \frac{j\omega L_{\text{adjusted}}}{1 - \omega^2 L_{\text{adjusted}} C_{\text{extracted parasitic}}} \tag{3.49}$$

$$\therefore L_{\text{adjusted}} = \frac{1}{\frac{1}{L_{\text{pre-extraction}}} + \omega^2 C_{\text{extracted parasitic}}} \tag{3.50}$$

3.6 Auxiliary Circuits

This section lists the auxiliary circuits designed to complete the design.

1. A 68-bit shift register is used to set the static settings of the chip, including the channel of operation, oscillator strength, buffer strength, PA biasing DACs etc. This was designed the same way as described in [47]

2. A 16-bit parallel data interface is used to control the modulation and pulse shaping. They control the oscillator capacitor bank settings for setting the center frequency and for FSK modulation. They also control the PA and the capacitor banks in the tapped capacitor match to perform pulse shaping and OOK modulation. The phase shifting circuit is also controlled through this interface for BPSK modulation.

3. A envelope detector is designed to measure the amplitude of the buffered signal feeding the PA. This is important to know, since it determines the efficiency of the PA. The circuit is a source follower envelope detector circuit similar to the one in [47]. It is designed to measure the amplitudes of interest, between $200mV$ and $350mV$

Chapter 4

Measurement Results

4.1   Die Photo and Test Setup

The transmitter was fabricated in a 65nm process from TSMC with ultra-thick top metal option. The entire chip has an area of 2mmx1mm. It was packaged with 3 resonators in a 40-pin QFN package. Ground pads were down-bonded to the die-attach of the package. This reduces the package pin-count and also provides a more stable ground due to shorter bondwires. Figure 4-1(a) shows a die micrograph of the transmitter and Figure 4-1(b) shows the photograph of the packaged transmitter with 3 resonators. Resonators of three different types were used to measure their performance.

A 4-layer Printed Circuit Board (PCB) was designed to test the TX chip. It consists of a small daughter board that only has the TX chip and RF connectors. It connects to a main board that has voltage regulators, connections to power supplies, a connection to an FPGA board, digital level converters to interface the TX to the FPGA. This setup is useful when testing multiple chips because a socket cannot be used for RF measurements. The test setup is shown in Figure 4-2.

The FPGA board used is from Opal Kelly and uses a Xilinx Spartan 3 FPGA. This FPGA is used to program the shift register, send modulation data to the TX,

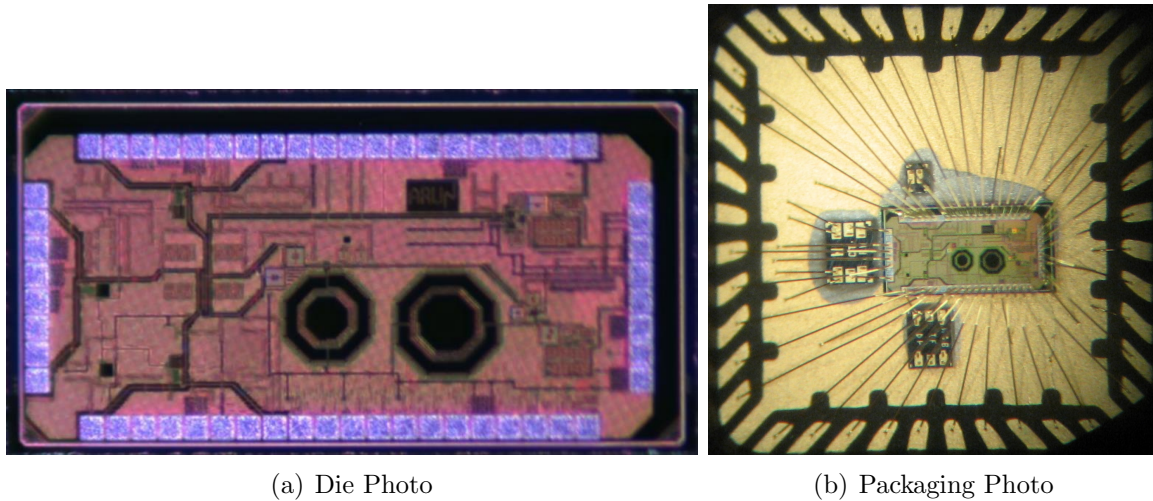(a) Die Photo   (b) Packaging Photo

Figure 4-1: Die Photo of TX and the Packaged chip with 3 FBARs

and perform pulse shaping. The pulse shaping is performed by implementing the algorithm of Figure 3-25. The FPGA itself is controlled through a computer via MATLAB.

All the measurements are done using a Agilent MXA N9020A Spectrum Analyzer and a Agilent DSO90254A Digital Storage Oscilloscope.

4.2   FBAR Oscillator

Figure 4-3 shows the startup transient of the transmitter. The output of the PA is measured after the system is enabled[1]. This shows that the startup time is $< 4\mu s$, which allows the use of very short packets as well.

Figure 4-4(a) shows the three oscillator frequencies of one of the chips. It shows the operation of all three channels in the design. Figure 4-4(b) shows the frequency as a function of the tuning bits of the oscillator. The oscillators on channels 2 and 3 have $> 500kHz$ tuning range which is sufficient for 1Mbps MSK modulation, but Oscillator 1 falls a bit short at $480kHz$. This is presumably because of the lower k_t^2

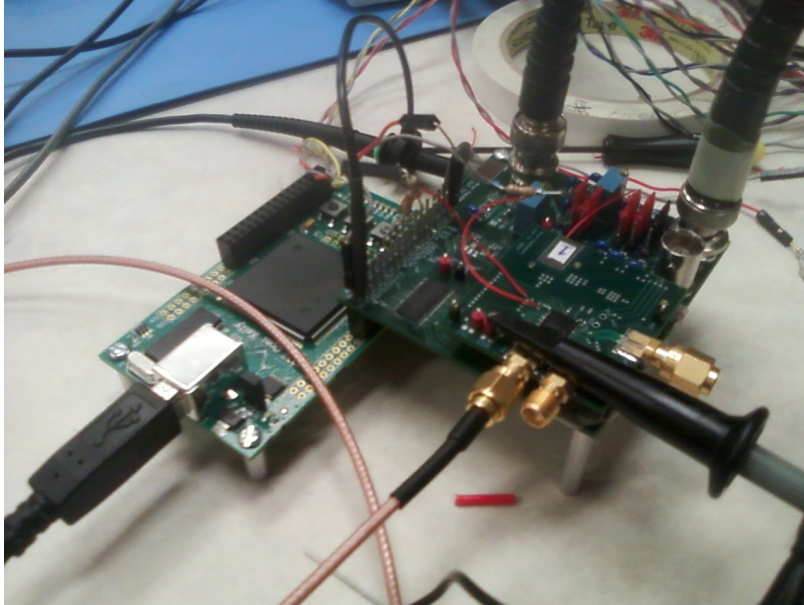[1]The signal that loads the shift register configuration into the design is used as the trigger

Figure 4-2: Test boards showing the daughter board, main board and the Opal Kelly FPGA board
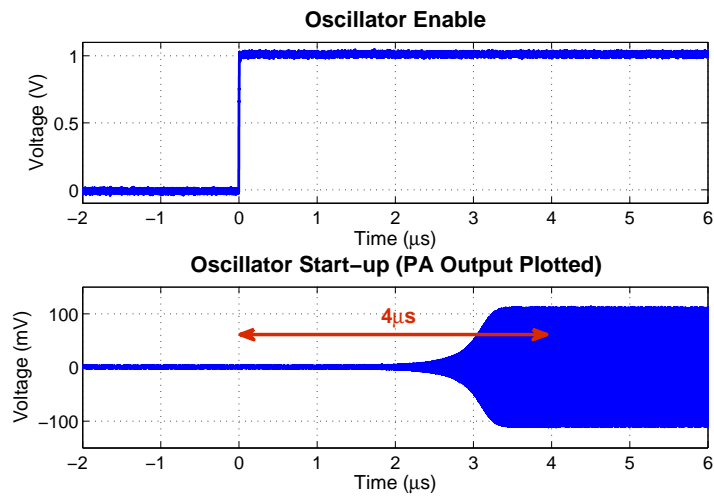

Figure 4-3: FBAR Oscillator Startup as viewed at the output of the PA

of this particular resonator.

Figure 4-5 shows the phase noise of the oscillator. This is again measured at the output of the PA. So, the signal passes through a buffer and a PA before being measured. The phase noise is $-132dBc/Hz$ at a $1MHz$ offset. The phase noise degrades to $-128dBc/Hz$ at $1MHz$ offset when the buffer with BPSK capability is used. This is because the signal passes through more stages of inverters which each add noise.

Table 4.1 shows the effect of power control of the oscillator-3. The oscillator current is controlled by tuning $R_{deg,n}$ as discussed in Section 3.1.4. This shows that the FBAR oscillator is functional down to $89\mu W$ from a 0.7V supply. This reduces further to $65\mu W$ at 0.6V supply.

Osc Power Setting	Osc Power Consumption (μW)
31	151
23	137
15	122
7	108
3	98
0	89

Table 4.1: Power control of Oscillator

4.3   Buffers

The tunable capacitor in the resonant load of the buffer is tuned to the resonance by adjusting it to obtain the peak amplitude (measured with the envelope detector). Unfortunately, in spite of the post-layout extracted simulations, the capacitance at the node was more than expected and the capacitor bank was configured to the minimum value. This is attributed to the capacitance from the metal fill, which was not extracted in the simulations. The effect of this was a slightly degraded output amplitude and slightly increased power consumption due to lack of resonance.

(a) Spectra of 3 oscillators overlaid

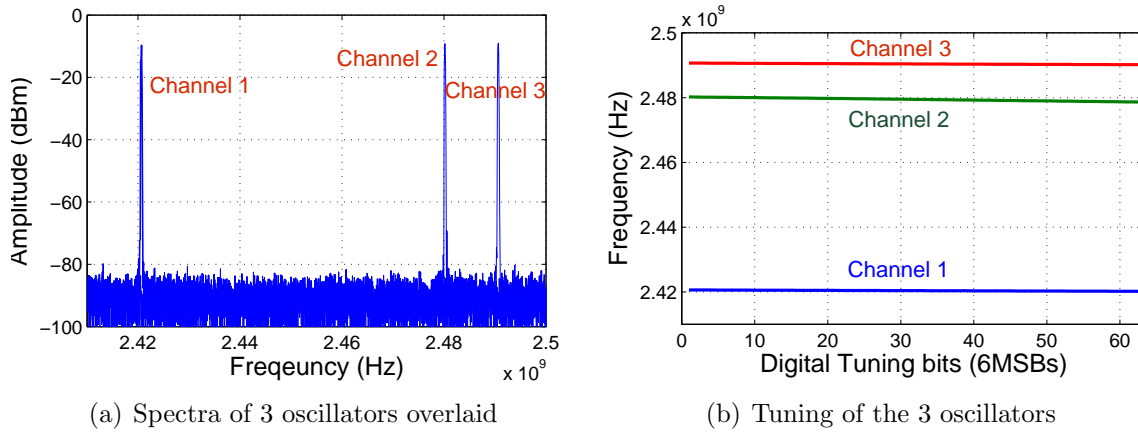(b) Tuning of the 3 oscillators

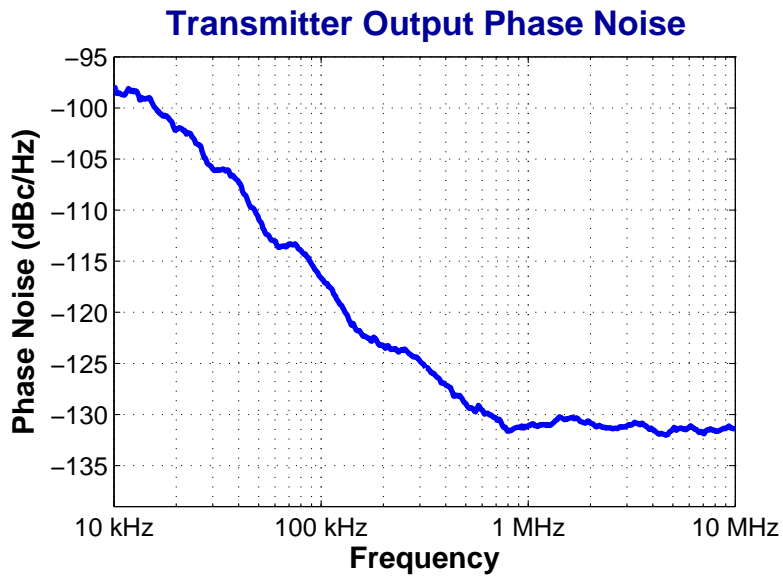Figure 4-4: Spectrum and tuning of the three Oscillators

Figure 4-5: FBAR Oscillator Phase Noise as seen at the output of the PA

But the amplitude reaches approximately $260 - 300mV$ which is within the designed amplitudes for the PA.

4.4   Power Amplifier

Figure 4-6 summarizes the performance of the Power Amplifier. This shows that the PA achieves a peak efficiency of about 43% and $\approx$ 34% at -10dBm. Because of the low power oscillator and buffer, the peak transmitter efficiency is 26%. The PA was originally designed to be more efficient reaching around 40% at -10dBm. One reason for this reduction is the lower amplitude of the buffer output. Another reason is parasitics on the board, which results in a non 50Ω load to the PA.
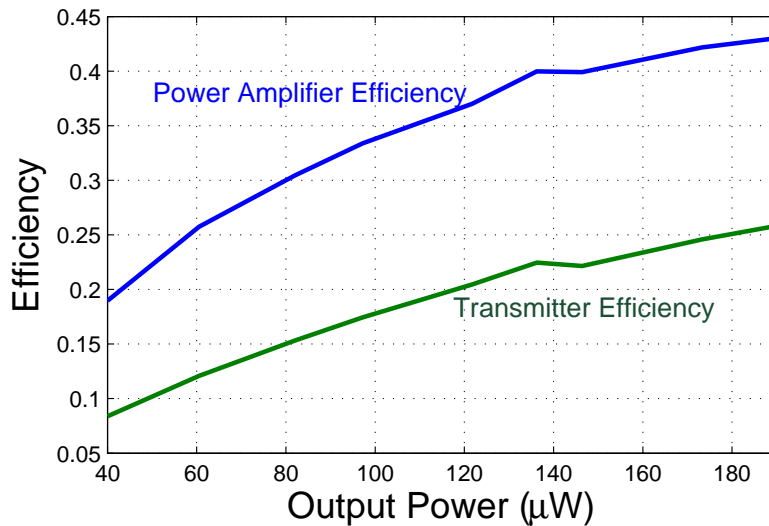

Figure 4-6: Efficiency of the PA and the Transmitter as a whole, as a function of output power

4.5 Modulation and Pulse Shaping

MSK

Figure 4-7 shows the spectrum for $1Mbps$ MSK modulation. The first sidelobe is $-22dB$ which is within a dB of the theoretical value. Also, the absence of any spurs shows that the deviation frequency is correct. The small discrepancy in the spectrum, from theory, is because of the finite time taken by the oscillator to change frequency. This time constant is also dependent on the Q of the resonator, with a higher Q implying longer time constants.
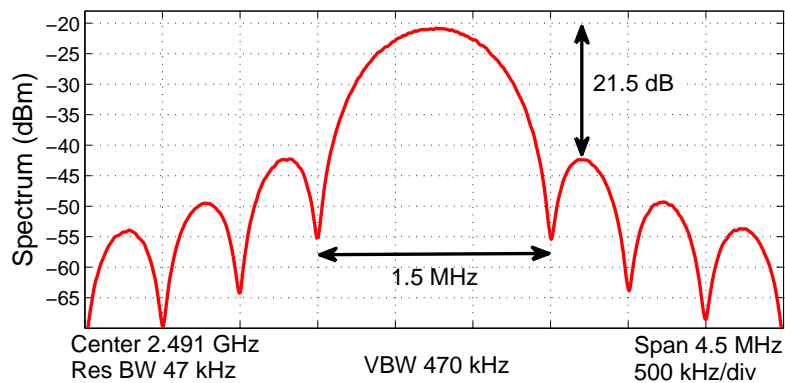
Figure 4-7: Spectrum of 1Mbps MSK modulation

BPSK

Figure 4-8(a) shows the spectrum of $1Mbps$ BPSK modulated data, without any pulse shaping. The delays of the paths generating the BPSK signals are adjusted to obtain the best spectrum without spurs. This indicates a phase difference of 180°. If the phase difference is different from this, there is a spur at the center frequency as shown in Figure 4-8(b) when the phase tuning is disturbed purposefully. The circuit works for 10Mbps BPSK modulation as well (though it occupies a large badwidth).

Figure 4-9 shows the spectrum and time-domain waveform for BPSK at $1Mbps$. The pulse shaping occurs at $8Msps$ with a Square Root Raised Cosine (SRRC) filter.

As can be seen, whenever a bit flips, the phase is changed when the amplitude is low. This improves the spectral efficiency. The $-20dB$ bandwidth of the signal reduces from 5MHz to 1.55MHz.

OOK

Figure 4-10(a), 4-10(b) shows the time domain waveforms for 1Mbps and 10Mbps OOK modulation. In the 1Mbps case, both the PA and buffer are turned off in the '0' case. For the 10Mbps case however, the PA is left on, with the bias voltages at V_T, while the buffer is turned off. This is required because the time constant of setting the bias voltage of the PA is around 100ns. At 10Mbps, the bandwidth is very wide and is not useful in practice, but is shown for demonstration.

Figure 4-11 shows the time domain waveform and spectrum of 1Mbps OOK data pulse shaped at $10Msps$ using a Gaussian filter.

4.6   Results Summary

Figure 4.2 shows a summary of the performance of the transmitter. Table 2.1 gives a comparison of this work with respect to previously published ultra-low power transmitters.

(a) 1Mbps BPSK modulation

(b) 1Mbps BPSK without correct phase tuning
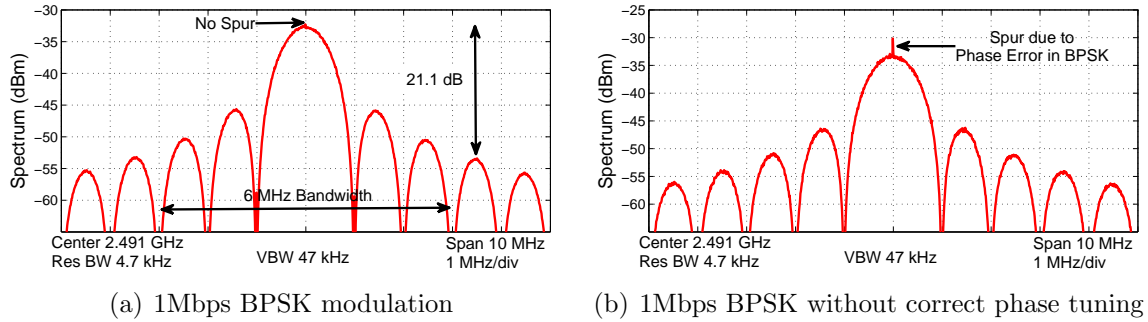
Figure 4-8: 1Mbps BPSK Modulation without pulse shaping

(a) Time waveform

(b) Spectrum with phase of LO and $\overline{LO}$ tuned

(c) Spectrum with phase error between LO and $\overline{LO} tuned$
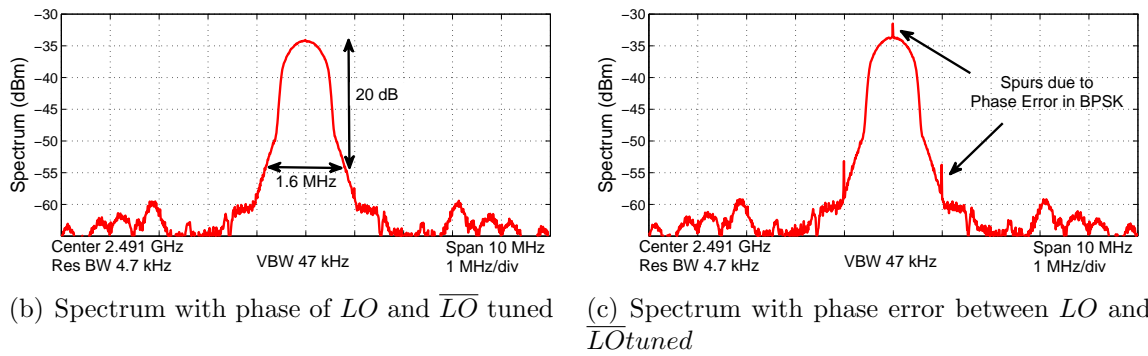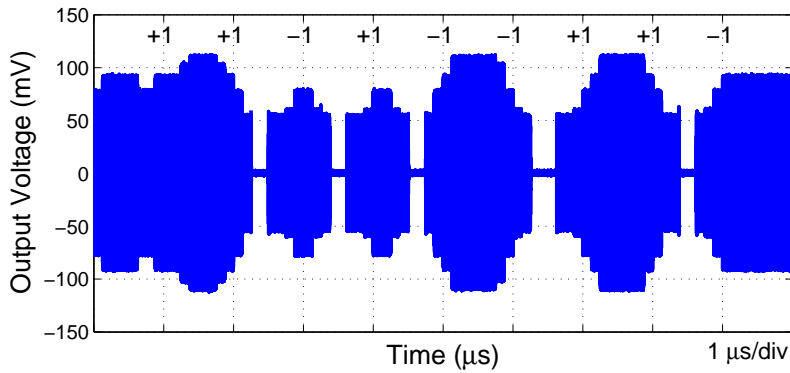
Figure 4-9: 1Mbps BPSK Modulation with SRRC pulse shaping

(a) 1Mbps OOK Waveform

(b) 10Mbps OOK Waveform

(c) 1Mbps OOK Spectrum
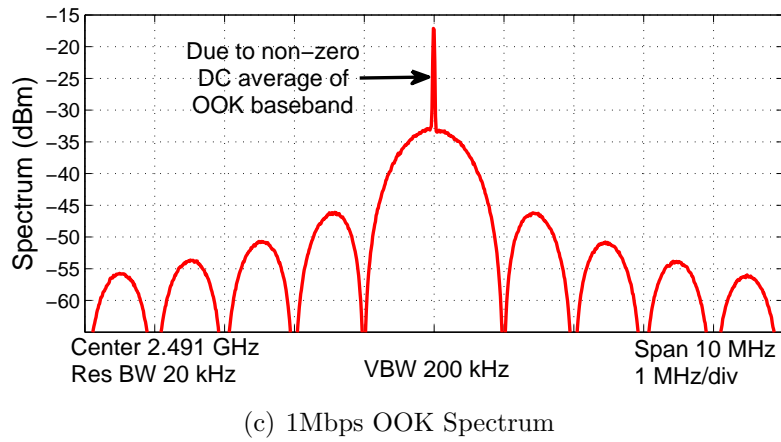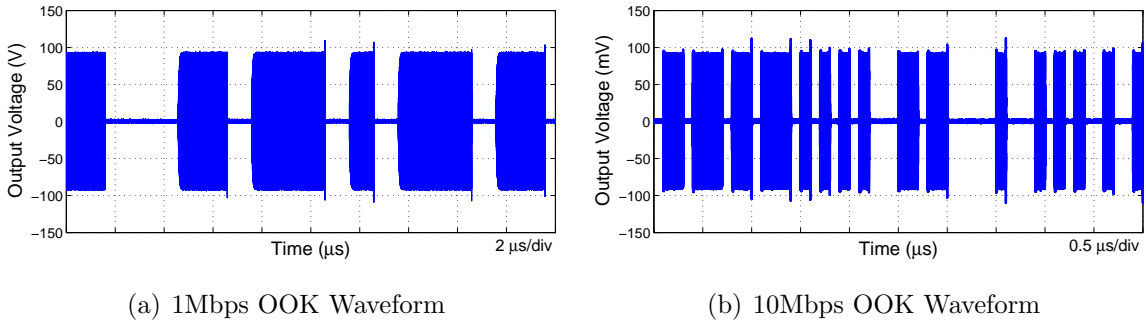
Figure 4-10: OOK Modulated Data
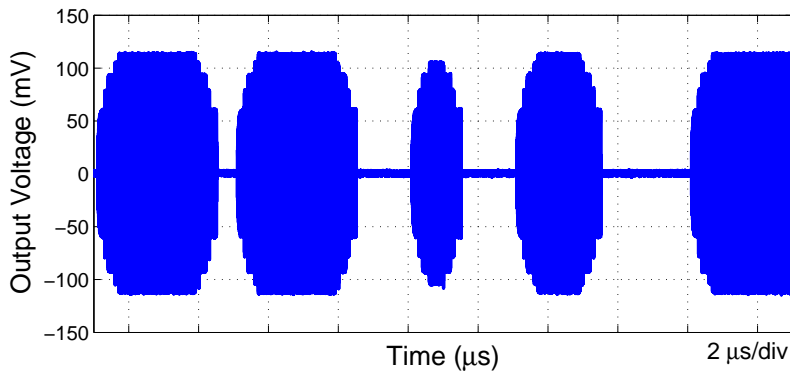
Figure 4-11: 1Mbps Gaussian filtered OOK Data

Specification	Result
Supply	0.7V RF
	1.0V Digital (all switches)
No. of channels	3
Startup time	$< 4\mu s$
Output Phase Noise	$-132 dBc/Hz$ at 1Mhz offset
Modulation	MSK
	OOK with Gaussian pulse shaping
	BPSK with SRRC pulse shape
Data rate	1Mbps (with pulse shaping)
	10Mbps without pulse shaping
PA Efficiency	up to 43%
Power consumption (active)	$480\mu W$ to $740\mu W$
Energy per bit	
OOK (-10.2dBm average) no pulse shaping	483pJ/bit at 1Mbps
	48pJ/bit at 10Mbps
OOK (-12.5dBm average) with pulse shaping	436pJ/bit at 1Mbps
BPSK (-10dBm) no pulse shaping	550pJ/bit at 1Mbps
BPSK (-11dBm average) with pulse shaping	527pJ/bit at 1Mbps
MSK (-10dBm)	550pJ/bit at 1Mbps

Table 4.2: Summary of the Transmitter

Chapter 5

Conclusions

This chapter summarizes the thesis and suggests future directions following this work.

5.1 Thesis Summary

This thesis first developed the specifications of an ultra-low power transmitter for use in a Body Area Network, at 2.4GHz, with asymmetric energy constraints on the sensor node and the basestation. These include low output powers ≈ -10dBm, low startup time, simple modulation schemes of OOK, FSK and BPSK and high datarates ≈ 1Mbps. These specifications motivated an architecture that uses ultra-low power RF resonator-based oscillators (in this case FBAR). These oscillators provide stable frequencies for transmission, without the use of PLLs. Their frequency is changed directly for FSK modulation. Since these oscillators have low tuning range, multi-channel operation, necessary for robustness of the network, was achieved with the use of multiple resonators each tuned to a different frequency. An architecture that uses these multiple oscillators and multiplexes the outputs efficiently onto a PA was developed. A resonant buffer was used to aid in multiplexing efficiently. The buffer stage was also designed to perform BPSK modulation by choosing between an inverting and non-inverting paths. Finally, a Power Amplifier optimized for delivery of low

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output powers was developed. The power amplifier has a tunable matching network that is used to efficiently transmit a wide range of output powers. This was used to provide pulse shaping to the OOK and BPSK modulated signals so that spectral efficiency is increased.

A prototype transmitter supporting 3 FBAR-oscillator channels was designed in 65nm CMOS. It operated from a 0.7V supply for the RF and 1V for the digital section (including the switches used in the design). The transmitter was measured to achieve 1Mbps FSK, up to 10Mbps for OOK and BPSK without pulse shaping and 1Mbps for OOK and BPSK with pulse shaping. The power amplifier was measured to have an efficiency of up to 43% and outputs between -15dBm and -7.5dBm onto a 50Ω antenna. Overall, the transmitter achieved an efficiency of upto 26% and energy per bit of $483pJ/bit$ at 1Mbps.

5.2   Future Work

Digital baseband and on-chip Pulse Shaping Logic: This thesis concentrated on the design of the RF front-end, and concentrated on minimizing the power consumption of the RF front-end. However, the digital baseband is not implemented in this work. With the greatly reduced power consumption of the RF Front-ends, the design of the baseband becomes more challenging, because it will begin to consume a greater portion of the power budget of the transmitter.

The digital baseband should include the Multi Access Controller (MAC), encoding of data for error correction and packet handling. In addition, the pulse shaping logic must be very low power too. This pulse shaping involves a FIR filter and a lookup table to map the output to corresponding PA settings.

Self calibrating test circuits: Self calibration is important in a system to adapt to changes in the environment and to mitigate process variations. For example, antenna characteristics depend on the environment, and clever calibration can

help optimize the PA for various operating conditions. Process variations in the resonators can be adjusted for by measuring the frequency of oscillation and applying the required correction capacitance. Similarly, the buffer can be calibrated to resonance, and the delays generating BPSK signals can be fine-tuned. These circuits can consume power because they are off most of the time.

Integrated Silicon MEMS Resonators: The Resonant Body Transistor [37] has great potential for integration into CMOS. An architecture like the one presented in this thesis can be extended to include many of these resonators as oscillators. The challenge would be to develop a low power oscillator using these resonators and to develop a technique of choosing the correct resonator for the channel of interest. The issue of calibration also becomes important in such designs.

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