Low Temperature Lithographically Patterned Metal Oxide Transistors for Large Area Electronics

by

Annie I. Wang

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Abstract

Optically transparent, wide bandgap metal oxide semiconductors are a promising candidate for large-area electronics technologies that require lightweight, temperature-sensitive flexible substrates. Because these thin films retain relatively high carrier mobilities even in an amorphous state, metal oxide-based field effect transistors (FETs) can be processed at near-room temperatures. Compared to amorphous silicon FETs, which are the dominant technology used in display backplanes, metal oxide FETs have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance. In this thesis we present a low-temperature (~100°C), scalable, fully lithographic process for top-gate, bottom-contact amorphous zinc indium oxide FETs using parylene, a room-temperature-deposited CVD polymer, as gate dielectric. Electrical characteristics were compared for FETs of varying device dimensions (W, L) using a standard set of extracted device parameters. We show in both simulation and experiment that the FET threshold voltage can be modified by varying the channel thickness alone, without requiring the additional complexity of multiple channel materials or different dopings. The baseline lithographic process was further developed to enable the integration of FETs of different channel thicknesses, and hence threshold voltages, on a single substrate. The availability of FETs with different threshold voltages allows the implementation of enhancement-depletion (E/D) logic circuits that have faster speeds and smaller device areas than single-V_T topologies. Using the two-V_T lithographic process, we fabricated integrated E/D inverters that operate at V_{DD} as low as 3V with gains > 20 and symmetric noise margins ~1.2V. Furthermore, we demonstrated integrated 11-stage and 21-stage E/D ring oscillators that operated rail-to-rail at $V_{DD} = 3$V and maintained oscillation for V_{DD} as low as 1.7V. These results demonstrate the potential for low V_{DD} metal oxide-based integrated circuits fabricated in a low temperature budget, fully lithographic process for large-area transparent electronics.

Thesis Supervisor: Akintunde I. Akinwande

Title: Professor

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Chapter 1

Introduction

1.1 Executive summary

The advanced development state of high performance, low-cost silicon-based microelectronics is readily apparent from their ubiquity. However, traditional crystalline silicon (c-Si) devices are less well-suited for a number of proposed applications, particularly large area electronics. Sometimes referred to as "macroelectronics," examples of large area electronics include display backplanes [1, 2], electronic textiles [3], imagers [4], Braille displays [5], and pressure-sensing "skin" [6].

For many of these applications, ultra-fast circuit speed is less crucial than the ability to use inexpensive, flexible substrates. Compared to the rigid silicon substrates on which conventional Si circuits are processed, lightweight, robust flexible substrates offer two major advantages: (a) mechanical flexibility and the ability to withstand repeated bending, and (b) the ability to conform to unconventional non-planar surfaces. These two properties enable the development of new applications, such as rollable displays, conformal skin temperature sensors, or curved wristwatch backplanes, that are not possible with current industry-standard rigid silicon or glass substrates. Another potential benefit of using lightweight substrates such as plastic or paper is a reduction in the total weight of the final product.

Most flexible substrates, particularly polymer substrates, cannot withstand the high temperature processing ($> 400°C$) required for traditional Si device fabrication.

Even the most thermally stable polymer substrates that are commercially available are limited to ~350-400°C; most degrade at much lower temperatures. Overcoming the challenges to using these temperature-sensitive substrates, however, opens up many opportunities for extending microelectronics to new applications. Hence, the development of new materials and device structures that can be processed at low temperatures in a scalable manner is needed to advance the state of the art for large area electronics.

This thesis describes the development of a low-temperature (<100°C), scalable lithographic process for integrated transistor circuits using amorphous metal oxide field effect transistors (FETs). Unlike silicon, metal oxide semiconductors have been demonstrated to retain high carrier mobilities even in the disordered, amorphous phase. The use of room-temperature processable materials for the FETs, namely an amorphous oxide semiconductor, zinc indium oxide, and an organic polymer dielectric, parylene, enables our fabrication process to maintain a low temperature budget compatible with temperature-sensitive substrates. In comparison, most reported lithographic processes require temperatures of at least 200°C or higher, while comparable room-temperature shadow-mask patterning processes cannot be easily scaled for integrated circuits.

By both simulation and experiment, we show that the threshold voltage of metal oxide FETs can be modified simply by changing the semiconductor channel thickness, without requiring the complications of a second material or differential doping. The ability to produce both enhancement and depletion mode transistors allows the implementation of enhancement/depletion (E/D) logic, an improvement over single threshold voltage FET circuits. Using a modified lithographic process capable of integrating devices with different V_Ts, we demonstrate fully integrated E/D inverters and ring oscillators that operate rail-to-rail with supply voltages $\leq$5V. To the author's knowledge, these are the first rail-to-rail ring oscillators demonstrated for metal oxide FETs, with the added benefit of being fabricated in a low temperature scalable lithographic process.

1.2 Need for a low temperature lithographic technology

One of the most widely used fabrication methods for vacuum-deposited semiconductor devices is shadow mask patterning. A relatively simple shadow mask-patterned process can be developed quickly, enabling the rapid exploration of different materials. Because no solvents or etchants are required, shadow masks allows patterning of devices while avoiding interactions except between the materials intrinsic to the device. Yet there are disadvantages to relying on shadow mask patterning. For materials deposited at higher pressures (e.g. sputtering at 10^{-3} Torr versus thermal evaporation at 10^{-6} Torr), the shorter mean free path of atoms and molecules reduces the effectiveness of the shadow mask. A shadow mask must sit flush to the substrate for accurate pattern reproduction; as substrate size increases, so does the likelihood of the mask bowing away from the substrate. In addition, the smallest feature sizes are limited to $\sim 50\mu$m because the metal foils that shadow masks are typically made from cannot be cut into infinitely small patterns. As device layout becomes more complex, shadow masks cannot support arbitrary patterns because each part of the patterned metal foil must be connected. Hence, while it is possible to fabricate FETs by shadow-mask patterning, this method limits the range of feature sizes, accuracy of pattern alignment, and scalability of the process to large substrates.

In contrast, photolithography is a proven scalable process for fabricating complex integrated circuits. Photolithography enables the fabrication of devices with smaller feature sizes and tighter tolerances through subtractive patterning. Fig. 1-1 shows a shadow mask-patterned and a lithographically-patterned FET side-by-side. In addition to shorter channel length and smaller overall geometry, the latter exhibits a much-reduced overlap between the gate and source/drain electrodes. The lithographically-patterned FET thus benefits from lower parasitic capacitances, one important consideration for circuit design.

The trade-off in moving from shadow masks to lithography is increased process complexity. Materials, device layouts, and etchants and etch processes must be com-

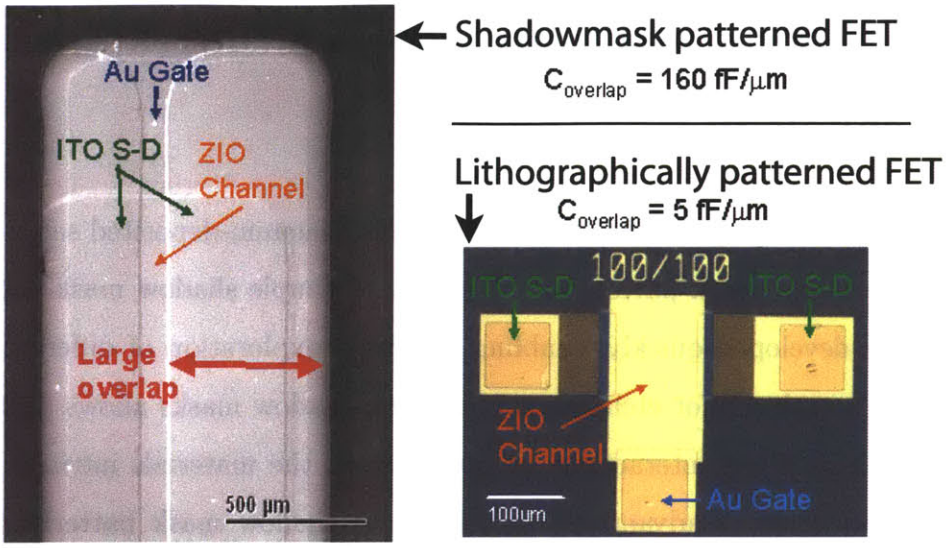

Figure 1-1: Comparison of feature sizes for a shadow mask-patterned FET versus a lithographically patterned FET. The tighter tolerances in lithography enable the design of FETs with much lower overlap capacitances. (Photomicrograph of shadow masked FET (left) courtesy of B. Yaglioglu.)

patible for successful processing. Subtractive patterning by etching requires high etch selectivity between the material being patterned and the underlying materials, otherwise features may be lost. Unlike shadow mask patterning, photolithography uses solvents which may affect the materials or interfaces in the device and these effects must be taken into consideration as well.

The maximum process temperature required for photolithography occurs during photoresist baking. A standard recipe for a widely-used positive resist, Fujifilm OCG-825, calls for baking at 95°C. This temperature falls below the glass transition temperatures (T_g) for a large number of commercially available polymer substrates. For example, the transparent material polyethylene naphthalate (PEN) has a T_g of 120-150° [7]. Above these temperatures the substrate may deform or otherwise degrade. The development of a lithographic process with maximum process temperatures $\leq$100°C would enable the use of these flexible, lightweight polymer substrates for integrated electronic circuits.

1.3 Low temperature processed materials

To achieve the goal of a low temperature, fully lithographic transistor process, all materials in the structure must be processable at <100°C, preferably even at room temperature. A simple thin-film transistor (TFT) structure comprises four layers: gate electrode, source and drain electrodes, gate dielectric, and semiconductor channel. It may also include a passivation or encapsulation layer. While the interactions of all these materials are important, the two main determinants of transistor performance are the semiconductor and the gate dielectric.

1.3.1 Low temperature deposited semiconductors

Currently, for large area electronics such as display backplanes and solar cells, hydrogenated amorphous silicon (a-Si:H) is the industry standard semiconductor material. While the performance of a-Si is much lower than that of crystalline or polycrystalline silicon, it is processed at comparatively lower temperatures, <400°C versus >600°C. Typically deposited by plasma-enhanced chemical vapor deposition (PECVD) at temperatures of 250-350°C, a-Si:H TFTs often utilize PECVD silicon nitride (SiN_x) as gate dielectric. While a-Si has been deposited at temperatures as low as 100°C, the quality of both a-Si:H and SiN_x deteriorate with decreasing deposition temperature [8]. Higher processing temperatures necessitate the use of more heat-tolerant substrates such as glass or steel foils and limit the use of most polymer materials.

In contrast, with the ability to be consistently deposited onto room temperature substrates over large areas, organic semiconductors are a reasonable candidate for flexible electronics. Organic semiconductors have been demonstrated as field effect transistors (FETs) in a variety of large area applications such as imagers, pressure sensors, and temperature sensors [6, 9]. A wide range of organic materials has been explored, from semiconducting polymers such as polythiophene and polyacetylene, to short conjugated oligmers such as pentacene and rubrene [10]. The material properties of an organic semiconductor can be tuned by modifying the chemical structure of the molecule, enabling, for instance, the production of a soluble form of the molecule

that can be ink-jet printed. Despite significant research over the past few decades, however, organic FETs suffer from low mobilities and poor transport that limit their potential uses.

Compared to amorphous silicon or organic semiconductors, metal oxide semiconductors potentially offer higher charge carrier mobilities and, correspondingly, higher current densities and faster response times. Based on heavy post-transition metal cations, these ionic semiconductors were first reported on in detail by the Hosono group at the Tokyo Institute of Technology [11, 12]. Initially interested in transparent conductive oxides (TCOs), they correctly predicted high electron mobilities for amorphous oxides of heavy metal cations, such as ZnO, In_2O_3, and SnO_2. Because amorphous oxide semiconductors (AOSs) can be deposited at low or near-room temperatures, they are amenable to processing on flexible polymer substrates and have even been deposited on paper substrates [13]. In addition, the wide band gaps ($>$ 3eV) result in optically transparent films, opening up a new range of possible technological novelties.

A typical mobility for a-Si FETs is $\approx$0.1-1cm^2/V·s, two to three orders of magnitude lower than mobilities for c-Si devices. The high defect densities in a-Si compared to c-Si limit carrier mobility. Given the tremendous performance hit in going from crystalline to amorphous in silicon, it at first seems surprising that amorphous metal oxides do not suffer the same problem. The reason lies in their different electronic structures. Bonding between the directional sp^3 orbitals in a-Si is highly sensitive to angular disorder. The disordered or strained covalent bonds give rise to localized tail states that impede carrier transport and degrade mobility. In contrast, for the highly ionic metal oxide semiconductors, the conduction band is formed primarily by spherically symmetric metal s orbitals [14, 15]. Hence, the interaction between two s states only depends on the metal-metal distance and not bond angle (Fig. 1-2). In post-transition metal oxides, the metal ion radius is large compared to oxygen and thus packing results in a fairly constant metal-metal distance even in amorphous films [16]. In fact, Takagi, *et al.* found the electronic structure and carrier transport in amorphous indium gallium zinc oxide (IGZO) to be very similar to that in crystalline

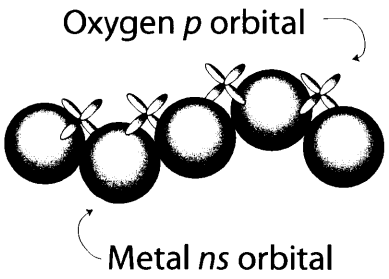

Figure 1-2: Schematic diagram of orbitals in amorphous metal oxide. The overlap of metal *ns* orbitals has no angular dependence. (after K. Nomura, *et al.*, Nature **432**, 488-492, 2004) [14]

IGZO [17].

Most high-mobility metal oxides are n-type. Few stable p-type oxide semiconductors have been demonstrated; Zhang, *et al.* reported that the doping asymmetry in ZnO arises from native defect formation energies which strongly favor n-doping. The n-type conductivity of oxides such as ZnO, In_2O_3, Ga_2O_3, and SnO_2 is attributed to interstitial metal ions and/or oxygen vacancies, which donate electrons [18–20].

Carrier concentration in metal oxide semiconductors can be modified by controlling the oxygen content in the film, either during deposition or by post-annealing in different gas ambients. By changing the oxygen partial pressure, it is possible to produce metal oxide films that range from insulating to semiconducting to conductive [21]. The sensitivity of the film properties to oxygen vacancy concentration offers a wide range of tunability; it also presents a challenge to precise and reproducible control of film properties.

Another method for controlling carrier concentration and mobility is to mix ZnO with other cations to form multicomponent oxides. Pure ZnO tends to form polycrystalline films when deposited at room temperature, and the presence of grain boundaries has been shown to hinder carrier mobility. On the other hand, because of their high crystallization temperatures (>500°C), binary or ternary oxides such as zinc indium oxide (ZIO) and IGZO form stable amorphous films. Compared to poly-

crystalline films, amorphous films offer improved uniformity and decreased surface roughness due to the absence of large grain boundaries. As will be discussed further in Chapter 2, the film composition/stoichiometry of multicomponent oxides can be engineered to improve specific properties, e.g. inhibiting crystallization, increasing or decreasing carrier concentration, or increasing mobility.

The considerable potential of metal oxide semiconductors has generated an actively growing interest, as evidenced by the rapid proliferation of publications on ZnO-based transistors since 2003. Because they retain high carrier mobility in amorphous state and offer wide carrier concentration tunability, metal oxide semiconductors are an attractive choice for a room temperature-deposited FET channel layer in this thesis.

1.3.2 Low temperature deposited dielectrics

FET performance depends on both the semiconductor and the gate dielectric. The success of c-Si technology rests largely on the high quality interface between the Si semiconductor and its thermally-grown SiO_2 dielectric. Grown at temperatures from 800-1200°C, thermal oxide provides a relatively defect-free, low leakage gate dielectric. In fact, oxidized silicon substrates are a popular choice for materials exploration of other semiconductors, including organic and oxide semiconductors. Nevertheless, moving beyond rigid, opaque silicon wafer substrates to glass or polymer substrates requires the development of other gate dielectrics. Particularly for temperature-sensitive substrates, the challenge is to find a low- or room-temperature deposited dielectric with appropriate band alignments and similarly low leakage currents and defect densities.

A number of research groups have utilized SiO_2 or SiN_x (or combinations of both) deposited by PECVD at 200-300°C. While these dielectrics perform well, the quality of the PECVD dielectrics degrades with decreasing deposition temperature, limiting the minimum achievable process temperature. SiO_2 can be deposited at room temperature by sputtering, but the porous films generally exhibit high leakage currents.

Pereira, *et al.* reported similar issues for sputter-deposited HfO_2, though leakage currents were improved by co-sputtering with SiO_2 to form an amorphous HfO_2/SiO_2 film [22].

In contrast to many inorganic dielectrics, organic dielectrics can be deposited at low- or even room-temperatures by solution processing, spin-coating, or chemical vapor deposition. Previously studied as gate dielectrics for organic FETs, pinhole-free polymers such as parylene offer smooth, conformal films with low leakage currents. While the compatibility of organic dielectrics with oxide semiconductors might be cause for concern, a few research groups have shown that they can be successfully integrated in hybrid organic-inorganic FETs [23, 24].

A more detailed discussion on gate dielectrics will be given in Chapter 2.

1.4 Objectives and technical approach

Explorations of new materials, such as organic or metal oxide semiconductors, tend to focus on semiconductor performance as benchmarked by carrier mobility. A field effect transistor is composed of multiple materials (i.e., semiconducting, insulating, and conductive layers), however, and the compatibility and interactions of the disparate materials is a strong determinant of device performance. In the design of any field effect transistor, there are three fundamental issues to consider:

- formation of a channel of charge carriers
- carrier transport through the channel
- carrier injection into the channel from the contacts

These govern device operation and affect parameters such as drive voltages, effective carrier mobility, threshold voltage, and contact resistance. The use of metal oxide FETs as building blocks for integrated logic circuits requires a solid understanding of the underlying device physics. Although their current-voltage and capacitance-voltage characteristics appear similar to crystalline silicon MOSFET curves, the devices do not operate in inversion like c-Si MOSFETs. Instead, as discussed in Chap-

ter 3, the thin-film metal oxide transistors operate in accumulation mode, i.e. carrier transport through the channel is dominated by majority carriers accumulated at the semiconductor-dielectric interface.

The first objective of this thesis is to develop a low temperature, lithographic fabrication process for metal oxide FETs. This baseline process can then serve as a platform to study the basic device operation, particularly channel formation in the device.

Channel characteristics can be described by threshold (V_T) or flatband voltage (V_{FB}), channel charge (Q_n), and interface/trap charge (Q_{it}). These parameters depend on the gate dielectric, i.e. the quality of the interface between semiconductor and dielectric and the band offsets between dielectric material and semiconductor. Band offsets of >1eV are needed to prevent carrier injection into the dielectric bands [25] and inhibit gate leakage. The low temperature budget imposed on the process constrains our choice of materials and allowable process steps.

Carrier transport through the channel is governed by the number of carriers present (n) and their mobility (μ). These two parameters are the most often addressed in current literature. Because materials exploration is not the focus of this thesis, we will not deal with improving channel transport.

Carriers injection into the channel is dependent on the contacts. Source and drain electrodes can be formed from metals, such as Al or Au, or from heavily-doped semiconductors such as indium tin oxide (ITO). Ideally, the source/drain electrodes function as ohmic contacts, i.e., carriers are free to flow in or out of the semiconductor and there is negligible contact resistance. In other words, the Schottky barrier height ϕ_B between 'metal' and semiconductor is zero or negative.

Since the ZnO-based oxides are n-type semiconductors, in a simplistic, ideal Schottky barrier view, the metal workfunction ϕ_m should be less than the electron affinity of the semiconductor χ_s [26]. The presence of interface states results in a non-ideal Schottky barrier, however, which the simple expression $q\phi_{Bn} = q(\phi_m - \chi)$ does not account for. In the non-ideal Schottky barrier model, in addition to a macroscopic dipole

between metal and semiconductor due to misalignment of Fermi levels, a microscopic dipole is formed due to the difference between metal Fermi level and semiconductor CNL. Wager applied these models to ITO-ZnO and ITO-SnO_2 interfaces and found both to function as injecting contacts, as expected from experiment [27].

Based on the work of Wager and others, for this work we chose to use ITO for source/drain contacts to the oxide semiconductor. Though other materials than ITO have been explored for contacts, including Mo, Ti/Au, Al, and doped ZnO, we will not deal specifically with improving carrier injection.

The second major objective is to use a combination of modeling simulations and experimental work (using the baseline lithographic process) to understand channel formation and threshold voltage. The effect of varying material and process parameters can be examined by comparing a standard set of device parameters extracted from FET electrical characteristics. The ability to modify threshold voltage enables the fabrication of both enhancement and depletion mode transistors.

The third major objective is to apply this knowledge to demonstrate simple enhancement/depletion (E/D) logic circuits fabricated in an integrated process. As will be shown, dual V_T E/D logic offers improved gain, noise margins, and rail-to-rail operation compared to unipolar enhancement-enhancement or depletion-depletion logic. The previously developed baseline process serves as a starting point for the development of a fully lithographic two-V_T process used to fabricate E/D inverters and ring oscillators.

1.5 Organization of thesis

Amorphous metal oxide semiconductors potentially offer higher performance than other candidate materials (e.g. a-Si or organic semiconductors) for near-room-temperature processing compatible with lightweight, flexible substrates. By understanding the fundamental issues for device operation in metal oxide FETs, we can improve device design for better performance in metal oxide FET circuits.

Chapter 2 describes the development of a low temperature, fully lithographic process for fabricating metal oxide FETs. Key considerations for material selection, deposition and etch processes, and device structure are discussed. The challenges and advantages of combining an inorganic oxide semiconductor and organic polymer dielectric are demonstrated.

Chapter 3 focuses on characterization and modeling of FETs produced in the low temperature process. A brief description of device operation is given. Device performance is quantified and compared through the extraction of a standard set of relevant device parameters. Silvaco ATLAS simulations of a single FET show the effect of interface traps on I-V characteristics. Further simulations are performed to gain insight into device operation. We show by both simulation and experiment that turn-off and threshold voltages can be modified simply by changing FET channel layer thickness, without requiring a second material or different doping.

In Chapter 4, we describe a modified lithographic process capable of integrating devices with different V_Ts for enhancement/depletion circuits. Using this process, we fabricated E/D inverters operating at $V_{DD} = 3V$ with gains > 20 and noise margins $\sim$1.2V. We further demonstrated rail-to-rail 11-stage and 21-stage ring oscillators fabricated in the low temperature, scalable lithographic process.

Chapter 5 concludes with a summary of contributions and suggestions for future work.

Chapter 2

Development of low temperature lithographic process

The use of metal oxide semiconductors for complex circuits requires a precise, scalable fabrication process capable of integrating many devices on a single substrate. Shadow mask patterning is a simple, straightforward technique but suffers from limitations in feature size, alignment accuracy, and scalability. As an additive process, inkjet printing offers the possibilities of high throughput and minimal waste, but often requires high annealing temperatures and is not yet mature for integrated circuit processing. In contrast, photolithography is a proven process for fabricating complex integrated circuits.

Although the starting point for technology development is the fabrication of single field-effect transistors, these individual devices are the building blocks for integrated metal oxide logic circuits. With the "big picture" goal of large area, flexible electronics in mind, our guiding philosophies for process development were (a) maintaining low process temperatures (<100-120°C) to enable the use of flexible polymer substrates in the future, and (b) patterning of materials by lithography, a proven scalable process. These two guidelines constrained our choice of semiconductor and dielectric materials, device structure and layout, and deposition and patterning processes during fabrication. Although the baseline process was developed for a specific material set, it could be extended to other oxide semiconductors with similar deposition and etch

characteristics.

The remainder of this chapter is organized into five major sections. The first three describe the initial stages of process development: (a) exploration of semiconductor materials (Section 2.1); (b) selection of gate dielectric material (Section 2.2); and (c) choice of FET device structure (Section 2.3). We used the results of this work to set our baseline FET materials and device structure, i.e. a top-gate, bottom-contact FET with zinc indium oxide channel and parylene gate dielectric.

In the fourth section (Section 2.4), baseline FET devices were patterned by shadow mask to verify that the chosen configuration demonstrated transistor behavior. Patterning by shadow mask served as a relatively quick, simple test before we moved on to develop the fully lithographic FET process. The fifth section (Section 2.5) describes the baseline lithographic process flow as well as issues faced in integrating the organic dielectric and inorganic channel.

2.1 Semiconductor material exploration

In Chapter 1 we discussed the advantages of metal oxide semiconductors over other candidates for large area flexible electronics. Even without annealing, oxide semiconductors offer higher mobilities than obtainable from amorphous silicon or organic semiconductors. Their properties can be drastically modified by altering deposition conditions or material composition. In this section we focus on the selection of a suitable oxide composition and deposition method for our low temperature-budget process.

2.1.1 Background

Initially, researchers focused on zinc oxide as a channel material for FETs [19, 28–31]. ZnO generally forms polycrystalline thin films at low deposition temperatures. In 2004, Fortunato, *et al.* reported mobilities as high as $\mu_{FE} = 27\text{cm}^2/\text{Vs}$ in ZnO FETs sputtered at room temperature [19]. Though the ZnO FETs demonstrated by some other research groups required annealing to show transistor behavior, the room

temperature-processed results by Fortunato, *et al.* and Carcia, *et al.* helped establish the potential for low temperature ZnO processing [29].

ZnO-based thin films have been prepared by a variety of methods, including pulsed laser deposition, atomic layer deposition, reactive DC sputtering, plasma-enhanced chemical vapor deposition, ion beam assisted deposition, chemical bath deposition, inkjet-printing and sol gels. One method in particular, RF sputtering, is a widely demonstrated process for metal oxide FETs. One advantage of sputtering is the ability to deposit films at low or room temperatures. Material properties such as stoichiometry and microstructure (and hence electrical and optical properties) can be adjusted by varying deposition conditions.

The effects of chamber pressure, oxygen partial pressure, RF power, and deposition/annealing temperatures have been frequently explored in the literature [18, 32–36]. Carcia, *et al.* were among the first to show that increasing oxygen partial pressures during deposition yielded higher resistivity ZnO films [18]. Similar results are obtained for mixed oxide films (i.e., ZnO mixed with other metal oxides). For instance, by controlling the partial pressure of oxygen during deposition, Suresh, *et al.* produced indium gallium zinc oxide films with carrier concentrations varying from insulating to 10^{19}cm^{-3} and Hall mobilities as high as 16cm/V·s [34], unannealed.

Carrier concentration and mobility can also be modified by forming multicomponent oxides. Iwasaki, *et al.* presented a combinatorial approach for AOSs and a fairly comprehensive set of experimental data on the In-Ga-Zn-O system [37]. By varying the compositional ratio of In:Ga:Zn, they observed that the In concentration largely influenced carrier concentration and mobility, the addition of Ga at higher pO_2 helped suppress oxygen vacancy formation, and an increase in Zn concentration improved subthreshold characteristics. In addition, they examined the influence on threshold voltage of varying compositions of binary and ternary oxides and their corresponding carrier concentrations. Other research groups have explored various multicomponent ZnO-based oxides as well, adding elements such as Hf, In, Ga, Sn, Cu, Mg, and Si [38–45] with the goals of inhibiting crystallization, increasing (or

decreasing) carrier concentrations, increasing carrier mobility, or improving stability. The many options for multicomponent oxides offer the possibility of being able to tailor an oxide semiconductor for specific desired properties in a given application.

Beyond optimizing oxide composition and deposition conditions, post-annealing is another possible method for improving semiconductor performance. Mobilities in pure ZnO have been improved by high temperature annealing (~200-600°C) which increases grain size and crystallinity. Unlike ZnO thin films which are polycrystalline as-deposited, however, mixed oxides tend to form amorphous films. Yaglioglu showed that a mixed oxide, $ZnO:In_2O_3$, remained amorphous until 500°C [46]. Nevertheless, despite the absence of discernible structural changes, annealing has been shown to improve mobilities in mixed oxide semiconductors. It is possible that annealing causes very short-range reordering that bulk measurement techniques like x-ray diffraction (XRD) cannot capture; also, some of the post-annealed FET improvements likely come from an improved semiconductor-source/drain interface rather than simply the semiconductor itself [47].

Our approach

Even without annealing, Fortunato, *et al.* demonstrated that ZnO FETs could be fabricated at room temperature and still yield high performance transistors. Based on those results, we chose to start with ZnO as an FET channel material and then adjust material composition and/or deposition conditions to obtain a suitable semiconductor. Patterning by shadow masks was utilized as a fast, simple way to evaluate materials and optimize deposition conditions for the channel layer prior to developing the full lithographic process.

The sensitivity of oxide thin films to the deposition conditions during sputtering offers wide tunability of their electrical properties but, at the same time, requires tight control over the process to replicate results. While many researchers have reported their deposition conditions for zinc oxide films, many of these optimized parameters are highly dependent on the specific deposition tool and its history. In this rest of

this section we describe the characterization and processing of sputtered zinc oxide and zinc indium oxide FET channel layers in our laboratory.

2.1.2 Shadow mask-patterned ZnO FET results

Initially, ZnO was investigated as channel layer, with the goal of reproducing the results reported by Fortunato, *et al.* for room temperature-deposited ZnO FETs [19].

RF sputtering was performed in the PVD Products sputterer in the Laboratory for Organic Optics and Electronics (now Organic and Nanostructured Electronics Laboratory, ONELab). Substrates are mounted over the 3" targets at a distance of ~5-6 inches. Three targets can be loaded in the chamber simultaneously for sequential deposition of different materials without breaking vacuum. The substrate holders accommodate wafers up to 4" in diameter, although film thickness drops off at the edges of large substrates. For the 2cm x 2cm substrates used for shadow mask patterning, uniformity in film thickness across the substrate was not an issue with substrate rotation during deposition.

In addition to simplifying initial material selection by shadow mask patterning, we also started out with silicon substrates with 100nm-thick thermal oxide to serve as gate and gate dielectric. Although neither flexible nor low temperature, Si/SiO_2 is a well-known system that allowed us to focus on the oxide semiconductor channel layer. An Al_2O_3 interface layer was sputtered immediately prior to ZnO deposition, so that the semiconductor-dielectric interface was formed without breaking vacuum. After deposition of the channel layer (discussed below), indium tin oxide (ITO) source and drain electrodes were deposited through shadow masks in the same sputter-deposition system. The resulting bottom-gate FET structure is shown in Fig. 2-1; a photomicrograph of an actual FET (W/L = 1250μm/100μm) is shown on the left.

The 50nm-thick ZnO thin films were deposited from a 3" ceramic target at a working pressure of either 3mTorr or 5mTorr. The effects of oxygen partial pressure, RF power and post-deposition annealing temperature on FET electrical characteristics were explored.

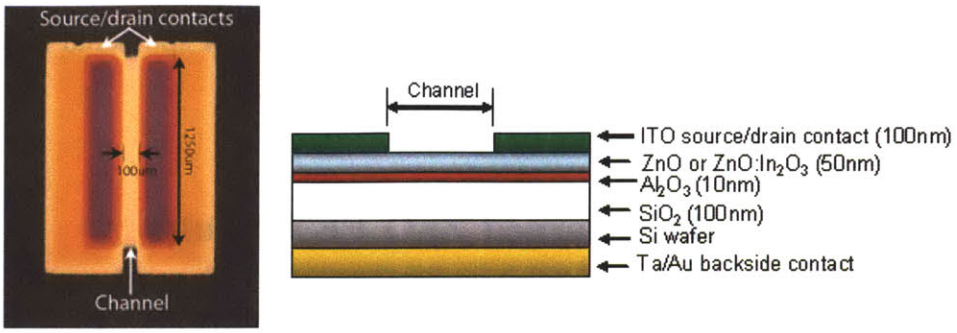

Figure 2-1: Shadow mask-patterned ZnO FET on an oxidized silicon substrate. The photomicrograph (left) shows a top view of a W/L = 1250μm/100μm device. A schematic cross-section of the device is shown on the right.

For room-temperature-deposited ZnO, deposition at lower RF powers (100W, 130W, 175W) or in Ar:O_2 gas mixtures (5% O_2, 15% O_2) resulted in insulating films. Only films deposited at higher RF powers in Ar-only ambients yielded transistor-like current-voltage (I-V) characteristics. Fig. 2-2 shows a comparison between the output I-V characteristics for ZnO FETs sputtered at 3mTorr at 250W and 375W. The low drain current in the 250W device reflects poor carrier mobility ($<10^{-3}$cm^2/Vs) compared to that in the 375W device ($\sim$1cm^2/Vs). (These mobility values were calculated from the I-V characteristics using the conventional long-channel silicon MOSFET equations; while these values suffice for comparison purposes here, please see Chapter 3.2.2 for a fuller discussion of mobility extraction for metal oxide FETs.)

A possible explanation for the increase in drain current and mobility with RF power is unintentional substrate heating. Because the substrate is not actively cooled during sputtering, the higher power densities likely resulted in increasing substrate temperatures during deposition. Elevated substrate temperatures are expected to improve film quality and hence carrier transport.

Fig. 2-3 shows the same trend for ZnO FETs sputtered at 300W, 350W, and 375W at a higher working pressure of 5mTorr. Larger drain currents were observed from the 5mTorr-sputtered device in Fig 2-3(c) compared to 3mTorr-sputtered device in Fig. 2-2(b), despite their deposition at the same power density. This difference might be attributable to the lower deposition rates at higher working pressure, which result

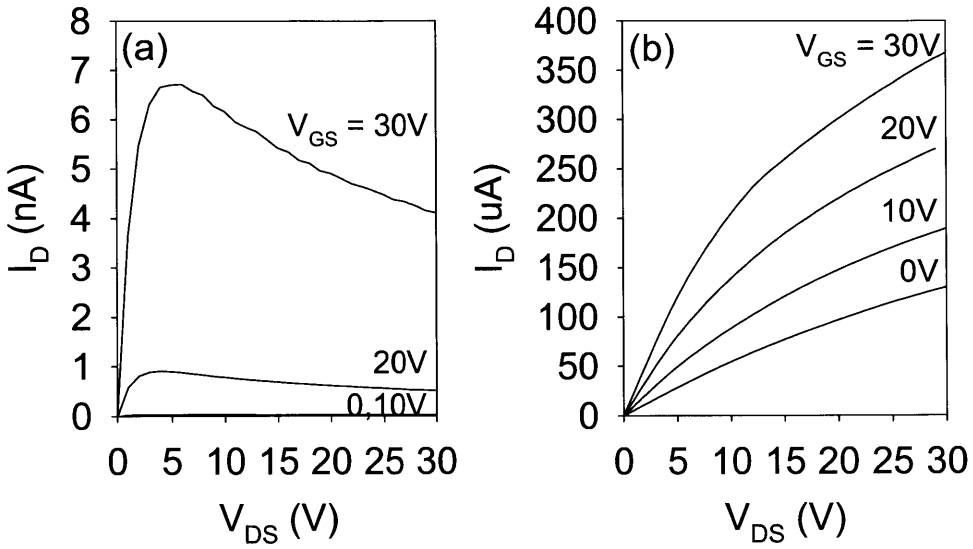

Figure 2-2: Output I-V characteristics for shadow-masked FETs with ZnO channel sputtered at (a) 250W and (b) 375W in Ar-only ambient at a working pressure of 3mTorr. Device dimensions were W/L = 1250μm/50μm.

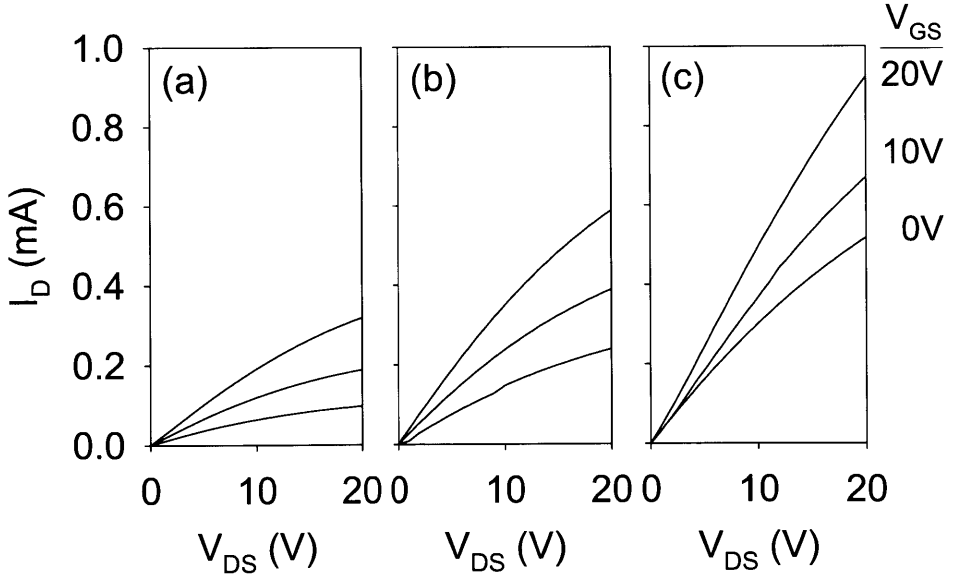

Figure 2-3: Output I-V characteristics for shadow-masked FETs with ZnO channel sputtered at (a) 300W, (b) 350W, and (c) 375W in Ar-only ambient at a working pressure of 5mTorr. Device dimensions were W/L = 1250μm/200μm.

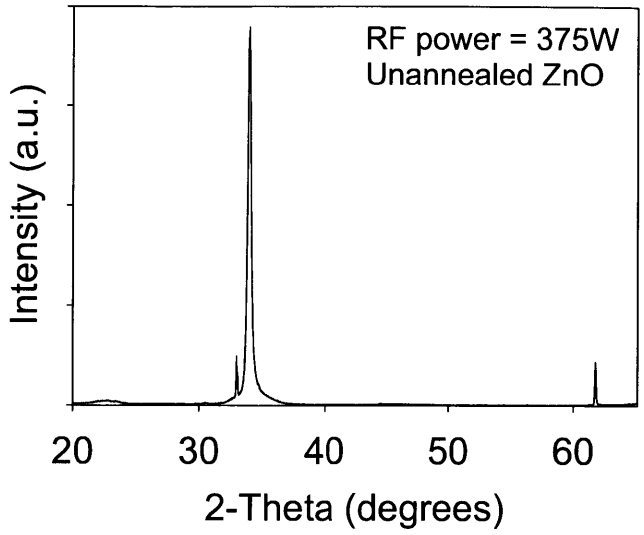

Figure 2-4: X-ray diffraction pattern for an unannealed ZnO thin film sputtered at 375W in Ar. The sharp peaks indicate that the film is polycrystalline instead of amorphous. (The main peak at 34° is ZnO; the smaller peaks at 33° and 62° are an artifact of the Si/SiO_2 substrate.)

in longer total deposition time and more substrate heating.

To verify the polycrstalline nature of the deposited ZnO, the microstructure of the as-deposited films was examined by X-ray diffraction (XRD) on a Rigaku 185mm Bragg-Brentano Diffractometer. A representative XRD spectra is shown in Fig. 2-4. The sharp peaks indicate the film is not amorphous, but rather polycrystalline. (The main peak at 34° is ZnO; the smaller peaks at 33° and 62° are an artifact of the Si/SiO_2 substrate.)

Transport in polycrystalline films is adversely affected by the presence of grain boundaries. Defect states in the grain boundaries form barriers to carrier transport, and hence limit mobility [48]. Consequently, annealing the ZnO films is expected to improve FET performance.

Because of poor and/or inconsistent performance of the as-deposited FET structures, we investigated post-deposition annealing as a possible solution. Devices were annealed for 1 hr on a hotplate at 100°C, 200°C, 300°C, and 400°C; only 300°C- and 400°C-annealed devices showed significant improvement. Fig. 2-5 compares the

unannealed and 300°C-annealed output I-V curves for the 250W device deposited at 3mTorr. Gate and drain voltages were swept from 0 to 30V. Drain current was improved by 3 orders of magnitude by annealing.

Similar I-V curves are plotted in Fig. 2-6 for devices annealed at (a) 200°C, (b) 300°C, and (c) 400°C. Gate and drain were swept from 0 to 40V. For the devices shown in Fig. 2-6, mobility increased from (a) negligible to (b) $\sim$0.3cm^2/Vs to (c) $\sim$1.2cm^2/Vs at V_{GS} = 40V. No improvement in output characteristics was observed for annealing temperatures <300°C, after which drain current monotonically increased with annealing temperature.

Fig. 2-7 shows the corresponding transfer current-voltage and capacitance-voltage curves for the 300°C- and 400°C-annealed devices. Both sets of curves show that the threshold and flatband voltages shift more negative with annealing temperature. In addition, the hysteresis in the I-V and C-V curves decreased with the higher temperature anneal. This improvement might be attributed to a reduction in defects and associated trap states. Hiramatsu, *et al.* observed that post-deposition annealing at temperatures above 250°C caused oxygen desorption and ZnO crystallization in films sputtered at low pressures [32]. An increase in oxygen vacancies would result in higher carrier concentrations in the ZnO channel, thereby causing the shift from enhancement to depletion mode after annealing.

While the previously-described devices became depletion mode after annealing, the device shown in Fig. 2-8(a) appears strongly depletion mode as deposited (375W, 5mTorr). Sputtering at high power potentially causes damage to the growing film from energetic ion bombardment [18, 32]. Defects in the polycrystalline ZnO film could contribute to leakage paths across the channel in this case. A large gate voltage bias is required to fully deplete the channel and turn the transistor off.

As shown in Fig. 2-8(b), annealing at 300°C resulted in improved gate control while drain current remained at the same order of magnitude. This improvement might be attributed to a number of reasons: elimination of excess unoxidized metal Zn, decrease of interface states, or reduction of grain boundaries [32]. Given that the ZnO films varied significantly from one deposition run to the next, it was difficult to predict

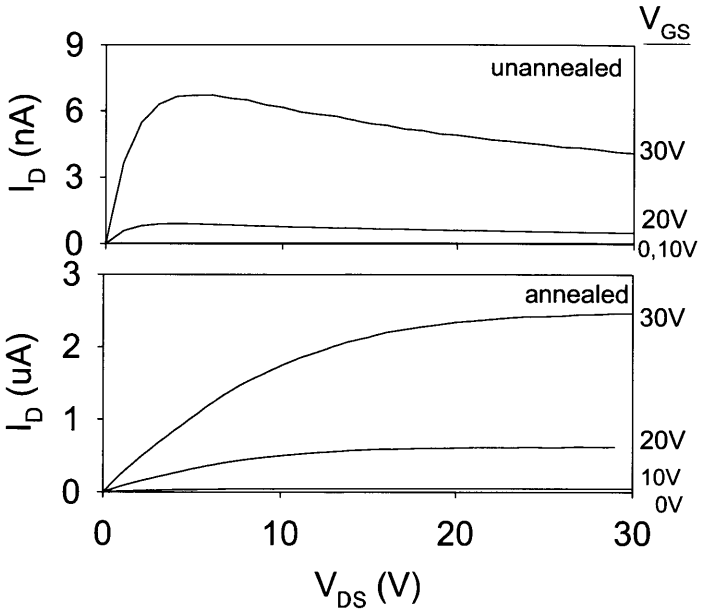

Figure 2-5: Comparison of output I-V characteristics before and after annealing at 300°C for 1 hour. Drain current increases by 3 orders of magnitude after annealing compared to as-deposited state. The ZnO channel was deposited at 250W at a working pressure of 3mTorr.

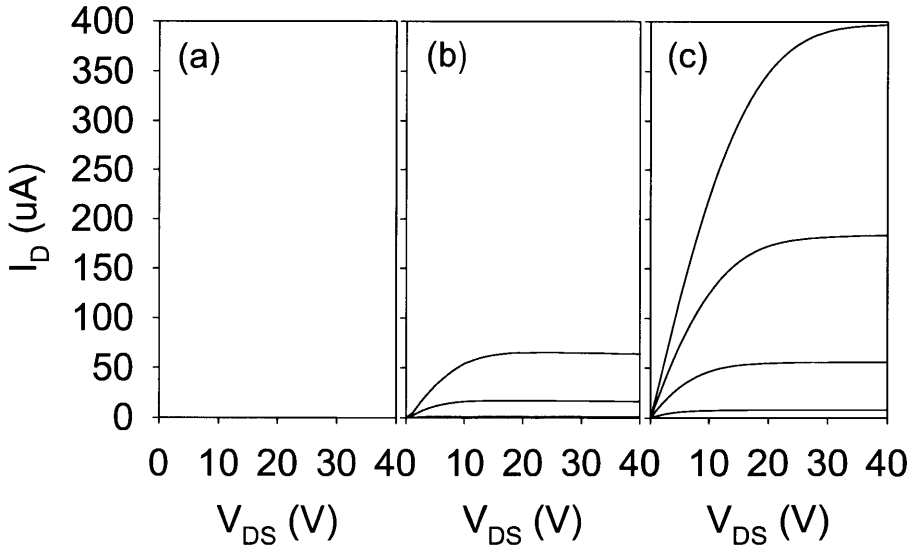

Figure 2-6: Output I-V characteristics for ZnO FET annealed at (a) 200°C, (b) 300°C, and (c) 400°C. No improvement was observed for annealing temperatures <300°C, after which drain current monotonically increases with annealing temperature. The ZnO channel was deposited at 375W at a working pressure of 3mTorr.

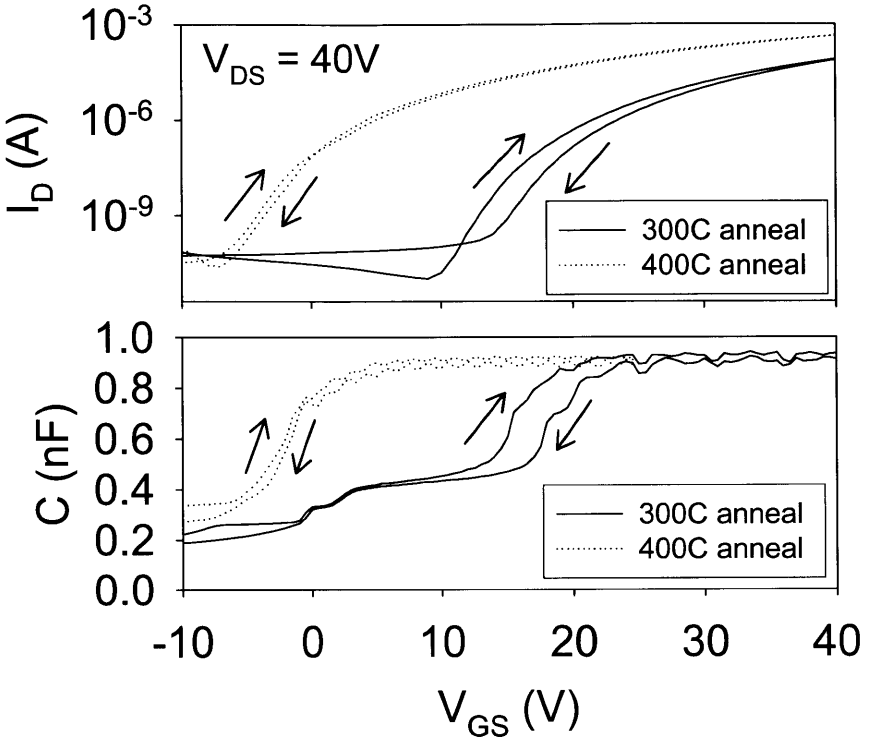

Figure 2-7: The saturation region transfer I-V characteristic (top) shows that threshold voltage shifts more negative with increasing annealing temperature. The corresponding quasi-static C-V characteristic (bottom) shows that flatband voltage also shifts more negative with increasing annealing temperature. Hysteresis in both the I-V and C-V curves is decreased after the higher temperature anneal. The ZnO channel was deposited at 375W at a working pressure of 3mTorr.

the properties of the as-deposited films and the effect of annealing. Hiramatsu, *et al.* offer a comprehensive study of the effect of post-deposition annealing on sputtered ZnO films [32]. They note that different mechanisms dominate the annealing process depending on the exact deposition conditions of the sputtered film.

While we demonstrated the ability to produce ZnO channel field effect transistors by RF sputtering, we were not able to reproduce the room temperature-processed ZnO FETs reported by Fortunato, *et al.*, nor were we able to obtain consistent results at nominally identical deposition conditions. Because the sputter deposition system is shared by many users and different sputter targets are frequently rotated in and out of the system, it is likely that the process was not sufficiently well-controlled. In any

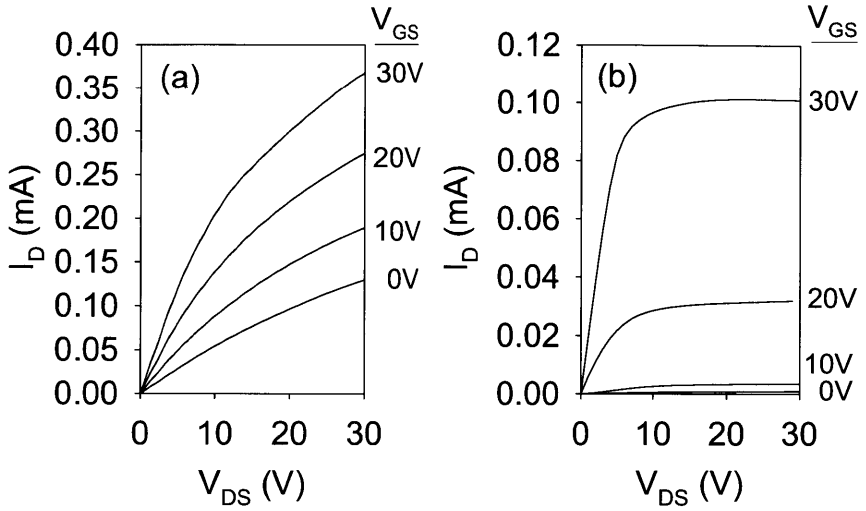

Figure 2-8: Output I-V characteristics for as-deposited and 300°C annealed ZnO FET. The ZnO channel was deposited at 375W and a working pressure of 5mTorr. Unlike previous ZnO FETs deposited at 3mTorr, the 5mTorr-deposited FET operated in depletion mode as-deposited. Gate control is improved after annealing at 300°C for 1 hour.

case, since high power densities and high post-deposition annealing temperatures were required to obtain transistor behavior, we determined the sputter-deposited ZnO to be unsuitable as a channel material for a low temperature process.

2.1.3 Shadow mask-patterned ZIO FET results

In order to obtain a semiconductor that could be deposited at lower power densities without requiring higher temperature annealing, we shifted to a multicomponent oxide target. The addition of indium oxide (In_2O_3) to zinc oxide has been shown to increase carrier concentration and mobility [37]. Robertson explains that In forms a shallow donor state in ZnO, and dopes ZnO without introducing localized states at the conduction band edge [16]. For this reason, zinc indium oxide was chosen for evaluation.

Another result of mixing ZnO and In_2O_3 is that the film does not form grains but is stably amorphous. Yaglioglu, *et al.* reported that zinc indium oxide films remain amorphous up to annealing temperatures of 500°C [49]. Hence, unlike in the case of

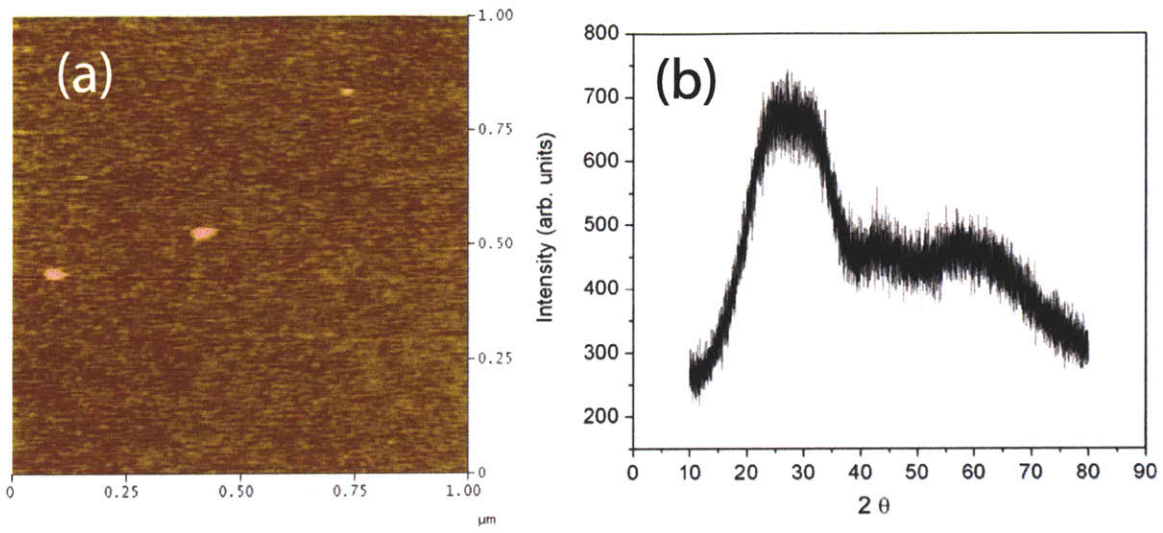

Figure 2-9: (a) AFM topology scan of a 30nm-thick zinc indium oxide film on silicon. The 1μm x 1μm scan shows an average roughness of 0.2-0.3nm; no grain boundaries are visible. (AFM data courtesy of N. Zhao) (b) X-ray diffraction spectra of a 50nm-thick zinc indium oxide film on glass. The absence of sharp diffraction peaks confirms that the film is fully amorphous. (XRD data courtesy of B. Yaglioglu)

ZnO, grain boundaries are not expected to be a limiting factor in carrier transport through a zinc indium oxide channel.

The mixture of ZnO and In_2O_3 results in an smooth amorphous film, as shown in Fig. 2-9(a). The 1μm x 1μm AFM scan of a ZnO:In_2O_3 (1:1) film shows an average roughness of 0.2-0.3nm. The x-ray diffraction (XRD) spectra in Fig. 2-9(b) confirms that the films are not polycrystalline. XRD data were obtained by using a PANanalytical X'Pert Pro Diffractometer (CuKα radiation) equipped with a high speed detector (X'celerator). Intensity versus diffraction angle 2θ from 10° to 80° was collected in steps of $\Delta(2\theta) = 0.01°$. The absence of sharp diffraction peaks in the XRD profile collected from a 50nm-thick ZIO film on glass substrate indicates that the film is fully amorphous.

We found that zinc indium oxide (ZIO) films could be sputtered at much lower RF power densities (100W-200W vs. 375W) than those required by ZnO for comparable deposition rates. However, ZIO films deposited in Ar-only atmospheres were too conductive for use as FET channel layer. The high carrier concentration and conductivity

is not surprising; indium zinc oxide has also been explored as a potential replacement for ITO as transparent conductor [46, 50]. In order to produce semiconducting films, we sputtered ZIO films in an Ar:O_2 (10% O_2) gas mixture. Because it was difficult to maintain a 3mTorr working pressure at the gas flow rates needed for 10% O_2, all films were deposited at 5mTorr.

FETs with a ZIO channel layer were deposited and patterned with the same shadow masks used in the previous ZnO FET experiments. Fig. 2-10 shows electrical characteristics for a ZIO FET sputtered in 10% O_2 and annealed at 100°C in air for an hour. Despite some hysteresis in the doubleswept curves, the linear and saturation region transfer I-V characteristics show that the transistor turns on near $V_{GS} = 0V$. Compared to the previously-described ZnO FETs, the output I-V curves for the ZIO FETs reach saturation at lower V_{DS}. Overall, lower gate and drain biases are needed, reducing the supply voltage and power requirements for ZIO FET-based logic.

Patterning considerations

From a practical fabrication standpoint, electronic properties are not the only considerations in materials selection. Beyond film deposition, another point to consider is pattern definition. As noted in Chapter 1, shadow masking is a straightforward process that generally does not disturb previously deposited layers, but limits feature size and alignment accuracy compared to photolithography. Photolithography allows subtractive patterning by liftoff or by etching, but liftoff is generally considered less desirable for sputtered films because of increased edge roughness and wing formation due to step coverage. If etching is used, the materials, etchants, and layout/structure selected must be compatible for successful processing.

Like ZnO, ZIO can be etched by weak acids such as dilute HCl and hence is easy to selectively wet-etch against other materials (e.g., ITO) in the FET structure [51]. This property, combined with its excellent electronic properties even when processed at temperatures $\leq$100°C, makes ZIO a good choice for our semiconductor channel material.

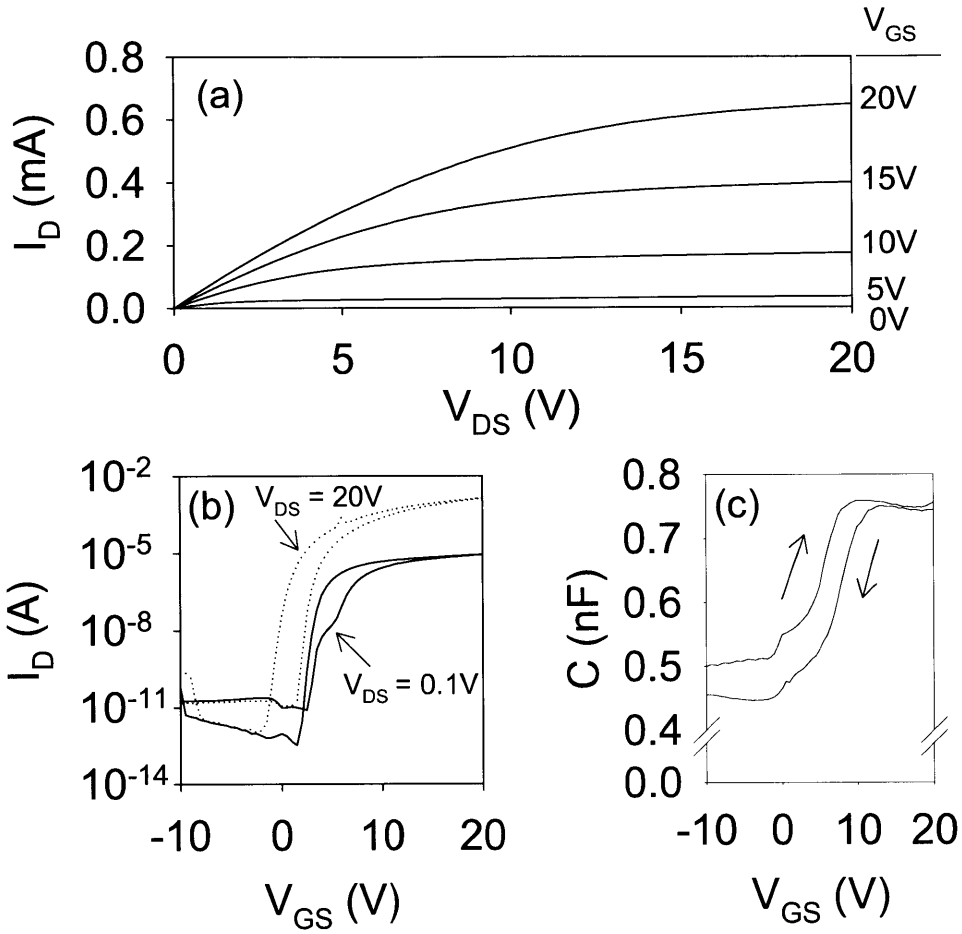

Figure 2-10: Electrical characteristics for shadow mask-patterned ZIO FET on an oxidized Si substrate after annealing for 1 hour at 100°C. (a) Output I-V curves, (b) linear region and saturation region transfer I-V curves, and (c) quasistatic C-V curves are plotted. The transfer I-V and quasistatic C-V doublesweeps are measured from V_{GS} = -10V to +20V and back. The device dimensions are W/L = 1250μm/150μm. In addition to a lower annealing temperature, much lower bias voltages are required to achieve similar performance to the previously-described ZnO FETs.

2.2 Gate dielectric material selection

To simplify material evaluation in the previous section, thermally grown silicon diode was used as gate dielectric. As previously noted, however, the use of thermal oxide is incompatible with a fully low temperature FET fabrication process. Thus, a different dielectric material is needed. In this section we give an overview of gate dielectrics for metal oxide FETs and describe the dielectric chosen for our low temperature process.

While carrier transport in FETs is partly determined by the semiconductor material properties, it is also heavily dependent on the semiconductor-dielectric interface. In metal oxide FETs the channel is formed by the accumulation of charge carriers at this interface under gate bias. A highly defective interface will impede carrier mobility and channel transport. A poor quality, leaky gate dielectric will also degrade carrier confinement to the interface and overall FET performance. Hence, the selection of an appropriate gate dielectric material is critical.

A wide variety of gate dielectrics have been explored for use in metal oxide FETs, fabricated by various methods such as thermal oxidation, plasma-enhanced chemical vapor deposition (CVD), atomic layer deposition (ALD), and solution processing. While a few organic-based dielectrics have been demonstrated for metal oxide FETs, by far most of the literature has reported FETs based on inorganic dielectrics, especially SiO_2. The advantages and disadvantages of several dielectrics, both inorganic and organic, are discussed below.

2.2.1 Inorganic dielectrics

As Robertson notes, the band offset between gate dielectric and semiconductor should be at least 1eV to prevent injection of carriers into the dielectric [16]. With a predicted band offset of 3.7eV for ZnO [16], SiO_2 appears a reasonable dielectric choice, although it seems more often chosen for processing convenience than any particular intrinsic material compatibility. Thermally oxidized silicon substrates, often used in exploratory work (as in the previous section), serve as a convenient starting plat-

form [29,31]. Relying on thermal oxide limits possible applications, however, because of the rigid silicon substrates and high process temperatures required.

Borrowing from amorphous silicon technology [52], several groups have utilized PECVD silicon dioxide, silicon nitride, or multi-layered SiO_x/SiN_y as gate dielectrics [1, 30, 53, 54]. Deposition is typically carried out at 200-300°C. Carcia, *et al.* found that devices on SiN_x showed higher mobility and lower threshold voltages than devices on SiO_2 and attributed the difference to modification of ZnO defect chemistry on SiN_x vs. SiO_2 [53]. Interestingly, Cross, *et al.* also reported higher mobility and drain current in ZnO on an SiO_2/SiN dielectric but higher threshold voltages than devices on SiO_2 of the same total thickness [54]. Higher drain currents can be partly explained by the larger dielectric constant of silicon nitride but the disagreement over the threshold voltage trend suggests a sensitivity of the semiconductor-dielectric interface to preparation as opposed to intrinsic properties of using SiN vs. SiO_2.

To further take advantage of the improved performance offered by metal oxides compared to a-Si, many research groups have explored the use of high-k dielectrics to reduce operating voltage and increase on-current. Al_2O_3 ($k \sim 9$) and HfO_2 ($k \sim 25$) are two such dielectrics frequently used for metal oxide FETs [22, 55–57]. Less commonly reported are other high-k materials such as Y_2O_3 ($k \sim 15$) [14], Ta_2O_5 ($k \sim 22$) [58], and bismuth zinc niobate [BZN] ($k \sim 55$) [59]. Although most high-k dielectric materials reported in the literature are deposited by atomic layer deposition (ALD) or physical vapor deposition methods such as sputtering or pulsed laser deposition (PLD), other deposition methods have been suggested for manufacturing. Ohya, *et al.* showed ZnO thin film transistors with ZrO_2 ($k \sim 25$) gate dielectric by sol gel method [60]. Anderson, *et al.* demonstrated a solution-based process for depositing $HfSO_x$ and $ZrSO_x$ dielectrics that could be adapted for inkjet printing [61].

One of the drawbacks of many high-k dielectrics is higher gate leakage currents due to the narrower band gaps and correspondingly lower band offsets [62]. Kim, *et al.* showed ZnO FET operation at bias voltages <4V, but found that leakage current increased significantly above $V_{GS} = 4V$ [59]. Structural defects, such as pinholes or voids, also contribute to high gate leakage currents. These can be mitigated by

annealing (T > 200°) or, alternatively, by utilizing a multi-layered dielectric such as the superlattice Al_2O_3/TiO_2 (ATO) structure used by Fortunato, *et al.* [19].

2.2.2 Organic and hybrid dielectrics

Hybrid inorganic-organic dielectrics offer a possible solution to high gate leakage currents due to structural defects in the inorganic dielectric. Noh, *et al.* combined a high-k dielectric with organic polymer for a double-layer dielectric where the polymer served to suppress gate current leakage through the polycrystalline SiO_2-CeO_2 dielectric [63]. In a slightly different approach, Oh, *et al.* employed AlO_x-self-assembled-monolayer units to form a 12nm-thick inorganic/organic hybrid dielectric layer with fewer defects than their previous all-inorganic Al_2O_3 film [64].

Purely organic dielectrics are a nonintuitive choice for inorganic semiconductor FETs, but Wang, *et al.* have demonstrated a hybrid inorganic/organic FET using either nanoscopic self-assembled or cross-linked polymer blend organic dielectrics [23]. Originally developed for organic semiconductor FETs, the low temperature-processed spin-coated or self-assembled dielectrics form smooth, conformal films. Although weak adhesion is often expected between inorganic and organic interfaces, they found strong interfacial adhesion between the organic dielectric and inorganic In_2O_3 semiconductor films, and the hybrid FETs exhibited high mobilities and on-off current ratios with V_Ts near 0V.

Other organic polymers, such as poly-4-vinylphenol (PVP) and polyimide, have also been demonstrated as gate dielectrics in metal oxide FETs [24, 65, 66]. After spin-coating, the polymers are cross-linked by annealing at 160-200°C. Compared to the >200-300°C process temperatures often required for high quality, low leakage inorganic dielectrics, these organic polymers offer low process temperatures.

The disadvantage to such solution-processed or spin-coated dielectrics is the possibility that leftover reactive reagents may not be fully removed from the film even after annealing. For this reason, parylene, a CVD polymer which does not require solvents or catalysts, is an attractive choice. Moreover, parylene is deposited at room-temperature and does not require post-annealing. Parylene turns out to offer a

number of advantages for our low temperature process, as the following sections will describe.

2.2.3 Parylene-C

Parylene (poly-*para*-xylylene) is a conformal, pinhole-free polymer formed by vapor deposition polymerization [67]. First reported in 1947 by Szwarc, the chemically inert, transparent films are deposited on substrates at room temperature [68].

More than one type of parylene dimer is commercially available; the chemical structures of the two most common, parylene N and parylene C, are drawn in Fig. 2-11. The substitution of a Cl atom for one of the aromatic H atoms in parylene-C results in a denser film with a higher dielectric constant. Table 2.1 gives a comparison of selected properties. For films $<5\mu$m thick, parylene C offers higher breakdown voltages than parylene N [69]. For this work, parylene-C was chosen as the dielectric material and all references hereafter to "parylene" refer to parylene-C.

Parylene is deposited from solid dimer form in the Gorham process [67]. As shown in Fig. 2-13, the dimer is loaded into the vaporization chamber where it is heated (90°C-180°C). The dimer vapor passes through the pyrolysis chamber (690°C-750°C) to be cracked into monomer units. These monomer units then diffuse into the room temperature deposition chamber where they adsorb and polymerize. The entire process takes place in low vacuum (~mTorr) and the resulting film is smooth and conformal. Fig. 2-12 shows an AFM image of a 100nm-thick parylene-C film deposited in a homemade deposition system in ONELab. The average roughness of the transparent polymer film is <2nm.

Except for oxidizing agents such as undiluted nitric acid, parylene is barely etched by most acids and bases. Its excellent solvent resistance and barrier properties have been exploited for use as an encapsulant for circuit boards, biomedical devices, and other barrier coatings. Parylene's solvent resistance also means that it is compatible for use with standard photoresists. In addition, since it can be patterned easily by etching in oxygen plasma [70], parylene is suitable for use in our low temperature photolithographic process.

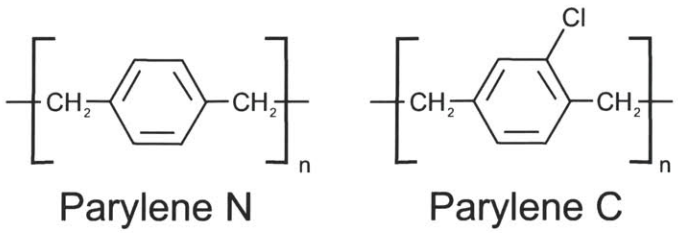

Figure 2-11: Chemical structure of parylene N (left) and parylene C (right). Parylene C differs from parylene N in the substitution of a Cl atom for one of the H atoms on the benzene ring.

Property	Parylene N	Parylene C
Density (g/cm^3)	1.110	1.289
Refractive index	1.661	1.639
Dielectric constant (60Hz)	2.65	3.15

Table 2.1: Comparison of selected parylene properties. [67]

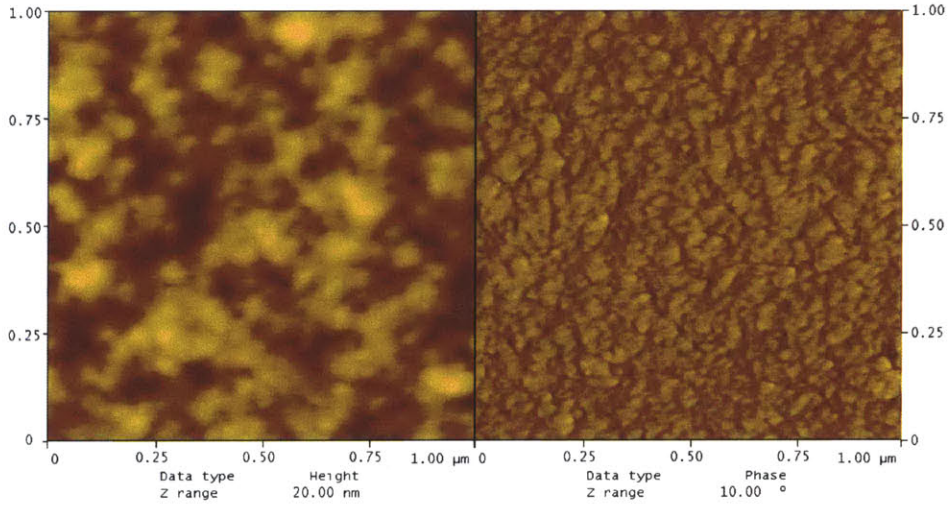

Figure 2-12: AFM topology scan (1μm$\times 1\mu$m) of a 100nm-thick parylene-C film on glass. The left half shows a height image; the right half is the corresponding phase image. The average roughness is <2nm.

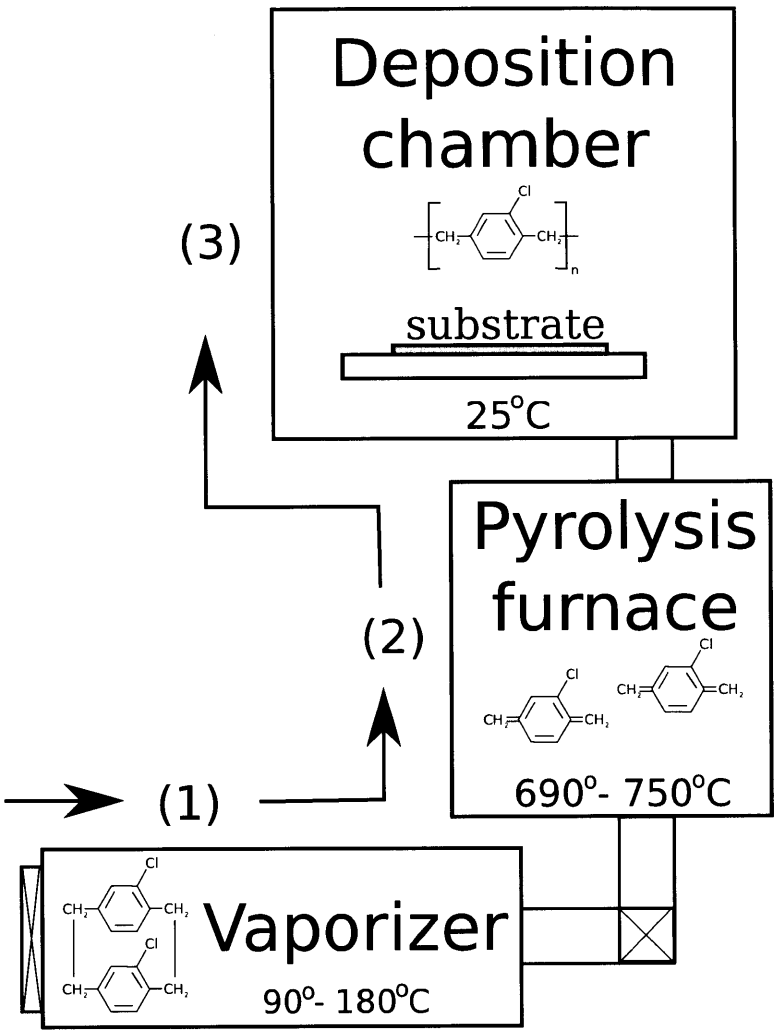

Figure 2-13: A schematic of the parylene deposition process. Parylene dimer is first vaporized at 90°-180°C in the vaporization furnace before being cracked into monomer units in the pyrolysis furnace. The stable monomer units flow into the deposition chamber where they adsorb and polymerize on all surfaces. The substrate remains at room temperature in the deposition chamber during the entire deposition process.

2.3 Device structure considerations

Given the importance of the semiconductor-dielectric interface for charge transport in FETs, the device structure is an important consideration. The quality of the interface depends not only on intrinsic materials properties (e.g., band alignments) but also on device fabrication methods. For example, the dielectric surface could be degraded by exposure to solvents or etchants prior to semiconductor deposition. One way to avoid this problem might be to deposit dielectric and semiconductor without any steps in between to avoid contamination; this then constrains the FET device structure to one in which the electrodes are patterned either before or after the semiconductor-dielectric stack.

Another practical concern is the compatibility of materials and etchants, especially for subtractive patterning processes. Potential damage to underlying layers during etching could be mitigated by reversing the structure to put less-easily etched layers on the bottom. In this section, we briefly discuss such device structure considerations in the context of lithographic fabrication process development.

2.3.1 Top-gate vs. bottom-gate FET structures

Four possible configurations for a simple 4-layer structure (gate electrode, source and drain contacts, semiconductor, and dielectric) are drawn schematically in Fig. 2-14. We find that most ZnO-based TFTs in the literature are bottom-gate structures, i.e. the gate dielectric is deposited before the semiconductor layer. In some cases a top-gate configuration is impossible, such as when oxidized silicon substrates are used as gate and dielectric. For structures in which all layers are deposited as thin films on arbitrary substrates, the main reason top-gate configurations are avoided is to prevent damage to the active layer from dielectric deposition and patterning. For example, sputtering an oxide dielectric over the semiconductor can damage the semiconductor surface, degrading the channel interface and hence, FET performance.

Most of the top-gate FETs reported in the literature utilize dielectrics deposited by less-damaging methods. Spin-coated organic dielectrics are one option since there

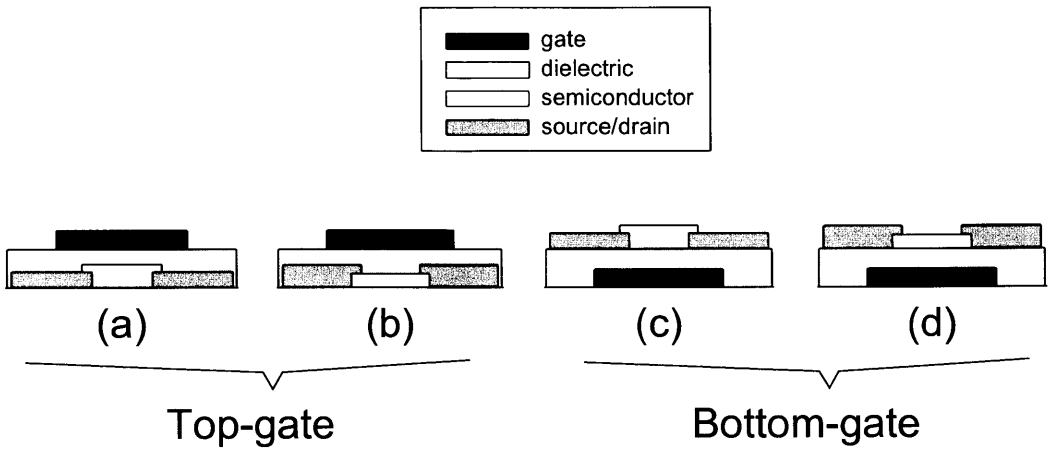

Figure 2-14: Four possible configurations for a 4-layer TFT: (a) top-gate, bottom-contact [staggered]; (b) top-gate, top-contact [coplanar]; (c) bottom-gate, bottom-contact [coplanar]; and (d) bottom-gate, top-contact [staggered] structures.

is no ion bombardment to damage the underlying semiconductor [65, 66, 71]. The disadvantage to using a solution-processed dielectric is the possibility of incomplete removal of reactants and/or solvents after annealing. More popular are inorganic dielectrics grown by atomic/molecular layer deposition [57,72–74], processes that yield high-quality thin films but suffer from low throughput. Alternately, PECVD [1, 75] or PLD [76] have also been employed to deposit oxide dielectrics.

Similarly, the same concerns hold for the deposition of passivation layers for bottom-gate FETs, i.e. where a dielectric is deposited over the exposed active layer. Not surprisingly, most passivation layers are deposited by spin-coating, ALD, or PECVD [77–80]. All of these methods typically require elevated temperatures, whether for post-annealing or during the deposition process itself. On the other hand, CVD deposition of the previously-described polymer, parylene, occurs at room temperature. The non-damaging process yields a dielectric with excellent properties that is suitable both as a dielectric for top-gate FETs and as an encapsulant.

2.3.2 Etch chemistry compatibility

Another consideration in designing a lithographic process is the compatibility of materials, etchants, and device structure. As with the deposition processes listed in the previous section, ideally the optimized patterning processes for each layer do not affect the underlying layers.

Ion bombardment during plasma processes can damage the semiconductor, breaking bonds and changing the stoichiometry of the affected layer. This defect generation can be purposely exploited to modify an amorphous oxide from semiconducting to conducting, as shown by a group at Samsung AIT for fabricating self-aligned electrodes [75, 81]. However, in general the damage caused by plasma processes is undesirable and may not be controllable or reproducible.

One approach to avoid damage during dry etching of top-contact source/drain electrodes is to cover the exposed semiconductor channel. M. Kim, *et al.* deposited a PECVD SiO_x etch stop layer [82] to protect the IGZO semiconductor, while S. Kim *et al.* incorporated a CuGIZO buffer layer over the GIZO channel [43]. Another strategy is to remove the dry-etch-damaged semiconductor layer by a timed wet etch [83]. Both of these methods increase process complexity by requiring additional steps.

Wet etching avoids the issue of plasma damage, but still requires using a chemical etchant with high selectivity for the material being patterned. This can pose a problem when a partially or completely exposed underlying material is easily etched by the subtractive patterning process for subsequent layers. For instance, the etching processes for ITO will also remove ZnO or ZIO, both of which are easily etched in weak acids such as dilute HCl. As a result, FET structures with top-contact ITO electrodes (Fig. 2-14b,d) cannot be prepared by straightforward subtractive etching.

Top-contact ITO electrodes can be patterned by liftoff rather than etching, but liftoff is generally considered less desirable for sputtered films because of increased step coverage. ITO electrodes can be prepared by wet etching if a bottom-contact configuration (Fig. 2-14a,c) is used instead, since the dilute HCl solutions used to etch ZIO barely etch ITO. As this example demonstrates, some process concerns can

be mitigated by changing the device structure.

2.4 Baseline FET structure, shadow mask results

Putting together the material and device structure considerations discussed in this chapter, a top-gate, bottom-contact FET structure with ZIO channel and parylene gate dielectric was selected as the baseline FET structure. This configuration combines:

- zinc indium oxide (ZIO), an oxide semiconductor that:
  - can be sputtered at room temperature
  - offers high mobility without high temperature post-annealing
  - can be selectively wet-etched in dilute HCl without damaging underlying ITO electrodes
- with parylene, a polymer gate dielectric that:
  - is deposited on substrates at room temperature
  - forms a conformal, pinhole-free film with low leakage currents
  - is resistant to solvents and most acids/bases including dilute HCl
  - is compatible with standard photoresist and etchable by oxygen plasma

and potentially offers excellent transistor performance while remaining within the desired temperature-budget for a low temperature, lithographic FET process.

To test the FET performance of this configuration, we first fabricated shadow mask-patterned ZIO/parylene FETs on 2cm×2cm clean glass substrates. After the sputter-deposition of 100nm-thick ITO source/drain electrodes, a 50nm-thick ZIO channel layer was sputtered in 10% oxgyen ambient. The substrates were then transferred in air to a parylene CVD system (Specialty Coating Systems Labcoter2) to deposit the polymer dielectric. Finally, Au gate electrodes were e-beam evaporated to complete the top-gate FETs.

A schematic cross-section of the FET is shown in Fig. 2-15(a). An actual device is shown in Fig. 2-15(b); the microscope image is lighted from below to show the

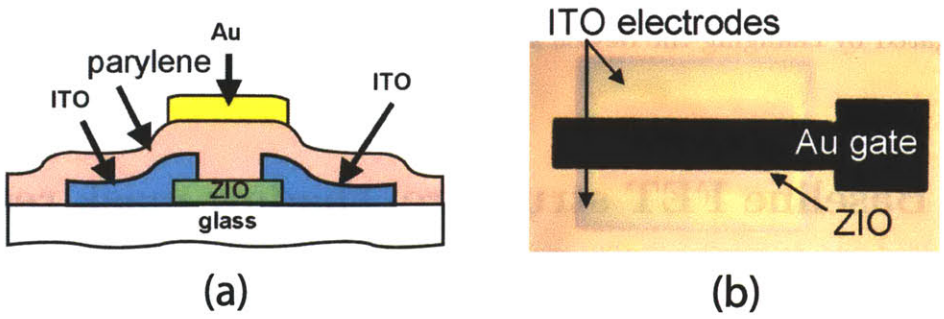

Figure 2-15: (a) Schematic cross-section of top-gate, bottom-contact ZIO FET with parylene gate dielectric. (b) Top-view photomicrograph of an actual device. The image is lighted from below to show the transparency of the ITO and ZIO layers; the Au gate layer is opaque.

transparency of the ITO and ZIO layers. The shadow mask-patterned devices are relatively large, with a channel width of 1250μm and channel lengths ranging from 50μm to 200μm.

Fig. 2-16(top) shows the output I-V characteristics for a top-gate FET with W/L = 1250μm/200μm. The corresponding transfer I-V and quasi-static C-V curves are shown in Fig. 2-16(bottom). The efficacy of parylene as a gate dielectric is demonstrated by the low gate leakage current (<10pA) and high on/off current ratio >10^7. The minimal off-state currents indicate that (a) the channel can be fully depleted of mobile carriers for $V_{GS} < 10$V, and (b) there is no significant contribution from leakage through the gate dielectric, despite the large device area. High on-state currents reflect the much higher carrier mobilities in ZIO compared to ZnO. Even without annealing, the calculated mobility is 20cm^2/Vs at $V_{GS} = 20$V.

Because of the 50μm gate-source/drain overlaps on each side (as-drawn on the shadow mask) to accommodate alignment errors, the overlap capacitance is very large. In addition, the millitorr-range pressures during sputter deposition reduce the effectiveness of shadow masks; even with the shadow mask nearly flush with the substrate surface, some material is deposited under the mask edges and pattern fidelity is degraded. These issues are solved by the lithographic process developed in the next section.

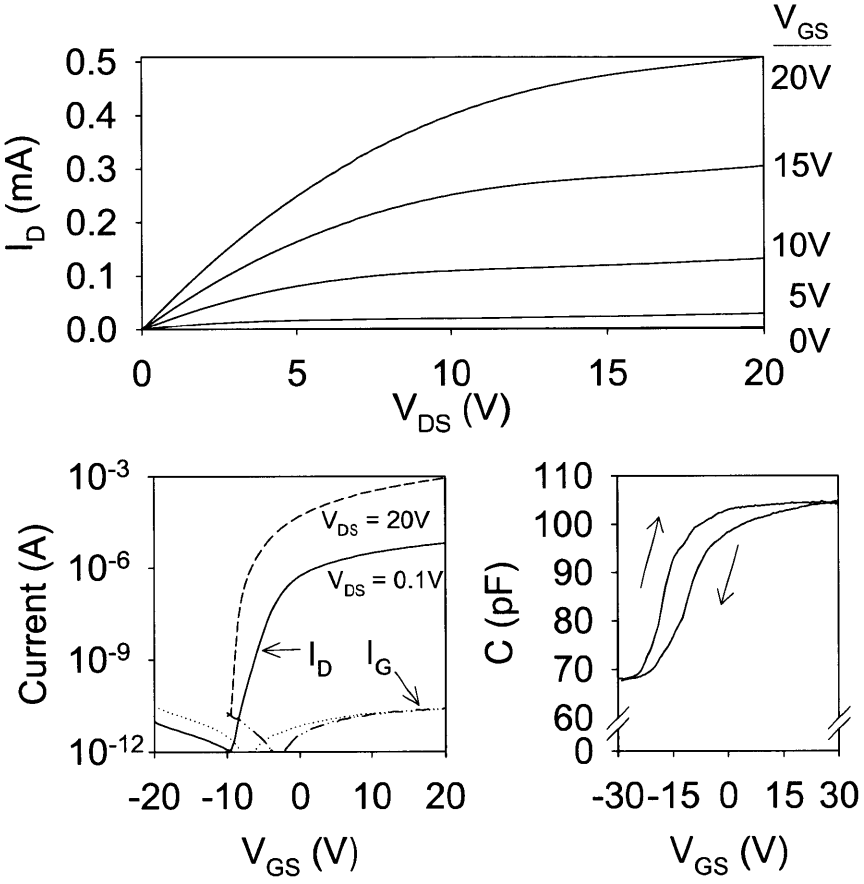

Figure 2-16: Electrical characteristics for shadow mask-patterned top-gate ZIO FET with parylene gate dielectric. Output I-V curves (top), linear and saturation region transfer I-V curves (bottom left), and quasi-static C-V curves (bottom right) are plotted. The doubleswept C-V curve was measured from V_{GS} = -30V to +30V and back and shows noticeable hysteresis. The device dimensions are W/L = 1250μm/200μm. Gate leakage current I_G through the parylene dielectric is < 10pA.

2.5 Baseline lithographic process

Most photolithographically-patterned FETs reported in the literature utilize liftoff rather than etching to avoid dealing with etch selectivity issues. However, in this process we chose to wet etch the sputtered films for more reliable pattern definition. Hirao, *et al.* and Hsieh, *et al.* have also successfully demonstrated fully lithographic oxide FET processes using subtractive etching [1,84]. Because both used SiN_x dielectrics deposited by PECVD, their maximum process temperatures reached 200-250°C. In contrast, the maximum process temperatures in our process (~100°C) are dictated by photoresist baking steps. No intentional annealing of the electrode, semiconductor, or dielectric layers is performed.

A schematic illustration of the lithographic process flow for fabricating ZIO/parylene FETs is shown in Fig. 2-17. The process is run on 100mm borosilicate glass wafers, which are cleaned in a piranha bath (3:1 H_2SO_4:H_2O_2) before starting device fabrication.

2.5.1 Source/Drain Layer

After piranha cleaning, a 100nm-thick layer of indium tin oxide (ITO) is sputter-deposited at room temperature in Ar onto the substrates. During deposition, the chamber pressure is kept at 4mTorr and the unheated substrate holder rotated for uniformity in thickness of the deposited films. (Because of some shadowing from the raised edges of the substrate holder, the sputtered film thickness drops off at the wafer edges.) After photolithography, the source/drain electrodes are then dry-etched in a $CH_4/H_2/Ar$ mixture (1.7:3:4 ratio) at 80°C in a reactive ion etching system. A scanning electron microscope image of cleanly etched ITO after photoresist removal is shown in Fig. 2-18.

2.5.2 Semiconductor Layer

After patterning of the source/drain contacts, the substrates are returned to the sputtering chamber for semiconductor deposition. A 10nm-thick layer of ZIO is RF

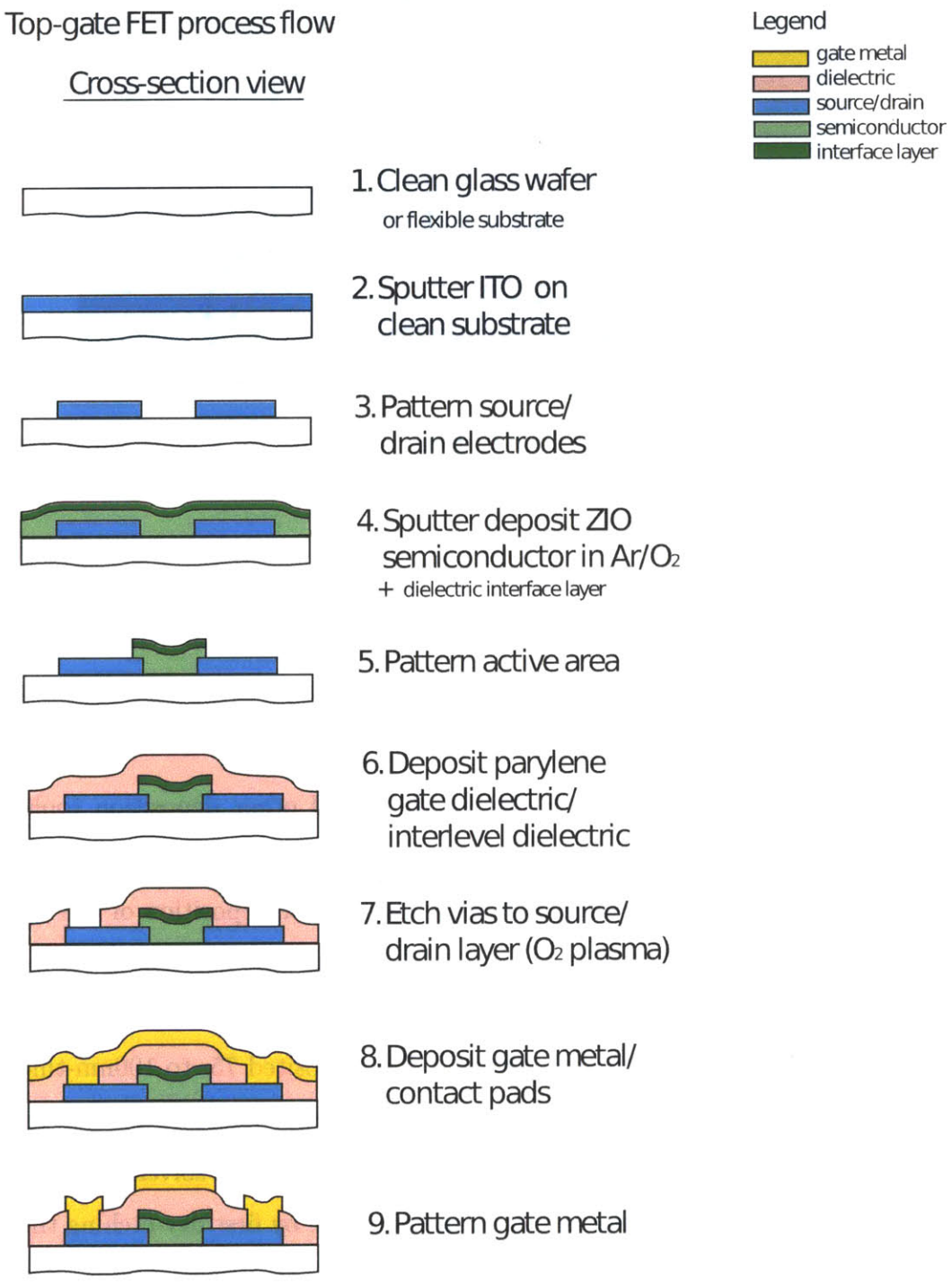

Figure 2-17: The lithographic process flow for fabricating a single ZIO/parylene FET with vias to gate/source-drain layer is illustrated in schematic cross-section views.

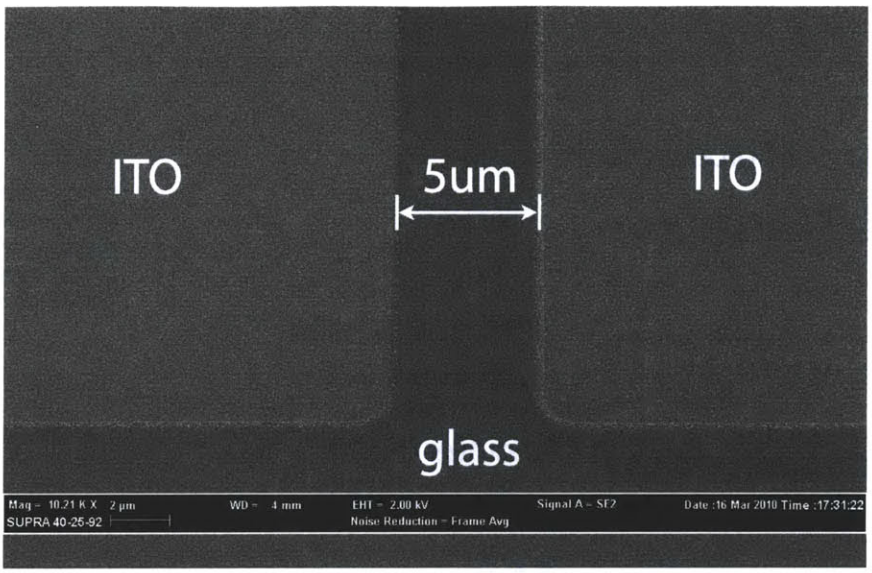

Figure 2-18: SEM image of ITO source/drain electrodes on a glass substrate after patterning by dry etch in $CH_4/H_2/Ar$ and photoresist removal.

sputtered from a 3" mixed oxide target (2:1 $ZnO:In_2O_3$) at room temperature in 10% oxygen. The deposition pressure and power are set at 5mTorr and 50W, respectively. Typical deposition rates ranged from 0.11A/s to 0.14A/s as measured on a quartz crystal monitor.

The sputterer in ONELab is connected to several other deposition tools via a transfer line, which allows substrates to be transferred from one deposition system to another without breaking vacuum. Following the sputter-deposition of the semiconductor, the wafer is transferred in vacuum to the homemade parylene CVD chamber for adhesion promoter treatment and parylene coating. (Details of adhesion promoter treatment are described in the next section.) The deposited 75- to 100nm-thick protective parylene layer forms the semiconductor-dielectric interface for the top-gate FETs. This layer protects the semiconductor from etchants and solvents during photo and patterning. The active area is defined in two steps, by first dry-etching the parylene layer in an oxygen plasma and then wet etching the semiconductor. Although parylene etches at virtually the same rate as photoresist, the parylene layer to be etched is much thinner than the 1μm resist used.

Since ZIO is easily wet-etched compared to ITO, patterning of the semiconductor

is performed in a very dilute hydrochloric acid solution (400:1 H_2O:HCl). Patterning the semiconductor is desirable to isolate the devices from each other, thereby avoiding current leakage between transistors and other circuit elements. We found that the ZIO etch had a negligible effect on the underlying ITO electrodes, which is not surprising given that ITO is typically wet-etched in much stronger acid solutions such as aqua regia [85].

2.5.3 Dielectric/Via Layer

It is known that parylene does not adhere readily on inorganic substrates [86]. In a lithographic process, multiple patterning steps may follow parylene deposition. Avoiding parylene delamination is crucial for repeatable fabrication of the integrated circuits. Thus, an adhesion promoter treatment immediately prior to parylene deposition was added to the process. Initially, a fast-reacting vapor-phase adhesion promoter, vinyltrichlorosilane, was tested. A five-minute exposure to vinyltrichlorosilane vapor in an evacuated chamber is sufficient to fully coat the substrate. However, the reaction evolves HCl which etches the ZIO semiconductor; in fact, in our test the 50nm-thick ZIO layer was removed completely. Instead, a slower-reacting but non-etching adhesion promoter, vinyltrimethoxysilane, was substituted. The chemical structure of vinyltrimethoxysilane is drawn in Fig. 2-19. The silane groups attach to the glass substrate, while the vinyl groups on the other end react with parylene to anchor the polymer to the substrate. The addition of the adhesion promoter mitigates the delamination of patterned parylene islands, as shown in Fig. 2-20.

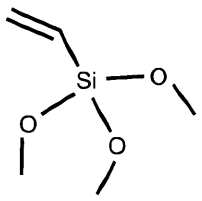

Figure 2-19: Chemical structure of vinyltrimethoxysilane molecule, used as an adhesion promoter for parylene. The silane groups on one side attach to the glass substrate while the vinyl groups on the other react with parylene to anchor the polymer to the substrate.

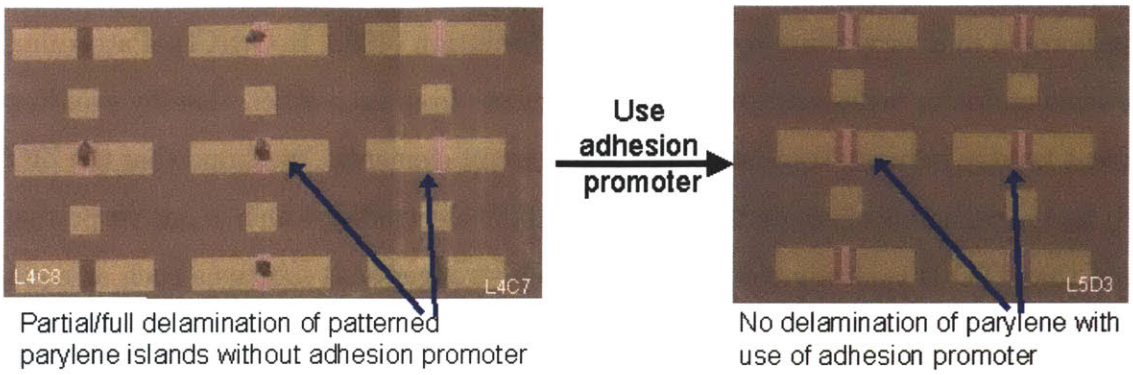

Figure 2-20: While parylene can be deposited and patterned without the use of an adhesion promoter, smaller parylene islands are susceptible to delamination during subsequent wet processing (left). An adhesion promoter such as vinyltrimethoxysilane bonds the parylene polymer to the substrate, preventing delamination during wet processing and ultrasonication (right).

Coverage of the substrate can be estimated from contact angle measurements of the surface. Bare cleaned glass is strongly hydrophilic and has a contact angle of $\sim 0°$. On the other hand, the vinyl groups on the vinyltrimethoxysilane molecule are more hydrophobic and have a higher contact angle. As the first monolayer of vinyltrimethoxysilane adheres to the surface, the contact angle rises rapidly and then saturates. The reaction does not terminate at a single monolayer, however, and continued vapor exposure will build additional layers. Fig. 2-21 plots measured contact angle as a function of treatment time. From this plot, a vapor treatment time of 30 minutes was selected to try to ensure full surface coverage without building more than a monolayer.

After the active area is patterned, the adhesion promoter vapor treatment is applied to the substrate immediately prior to parylene deposition. A valved attachment to the parylene deposition chamber allows the introduction of vinyltrimethoxysilane vapor directly to the chamber; at the end of the treatment time, the valve is closed off and the chamber flushed with nitrogen to remove residual solvent before beginning parylene deposition.

Following adhesion promoter treatment, a 120- to 150nm-thick parylene layer is deposited by CVD (diX-C dimer, Daisan Kasei Co.) to form the gate/interlevel dielectric. During the deposition process, the substrate itself remains at room tem-

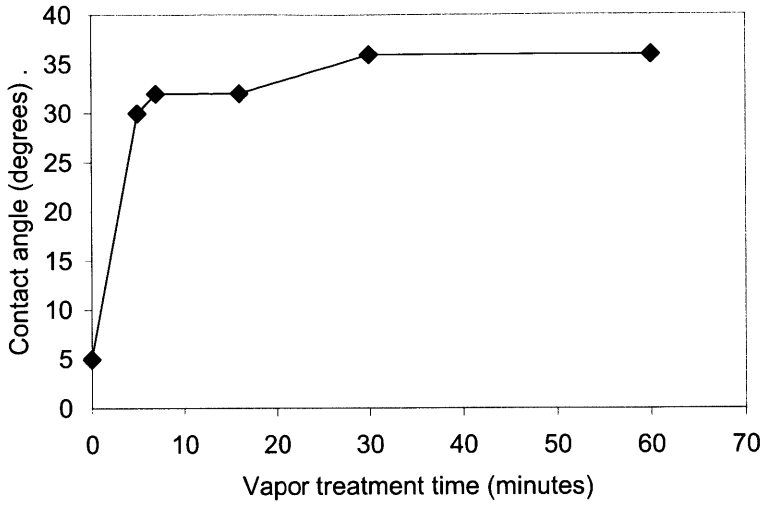

Figure 2-21: Plot of contact angle versus vinyltrimethoxysilane vapor treatment time on a cleaned glass substrate. Contact angle saturates after the surface is covered by a complete monolayer, but the reaction is not self-terminating and continued vapor exposure will build additional layers.

perature. Vias are then opened through the parylene using an oxygen reactive ion etch, following the basic process outlined by Kymissis *et al.* [87]. Parylene's relative insolubility allows for use of standard photolithography solvents.

2.5.4 Gate Layer

Following via definition, a chromium/gold (Cr/Au) thin film is e-beam evaporated onto the substrates for gate electrodes and probe pads. The 10nm-thick Cr layer serves as adhesion layer for the 100nm-thick Au film. The two metal layers are then wet-etched in two steps, first a potassium-iodide-based etch (Transene TFA) to pattern the gold, then Cr-7 chromium etchant (Cyantek) to remove the exposed chromium.

Fig. 2-22 shows a completed array of single transistors of varying channel lengths. The inset shows a magnified view of a single FET (W/L = 100μm / 100μm).

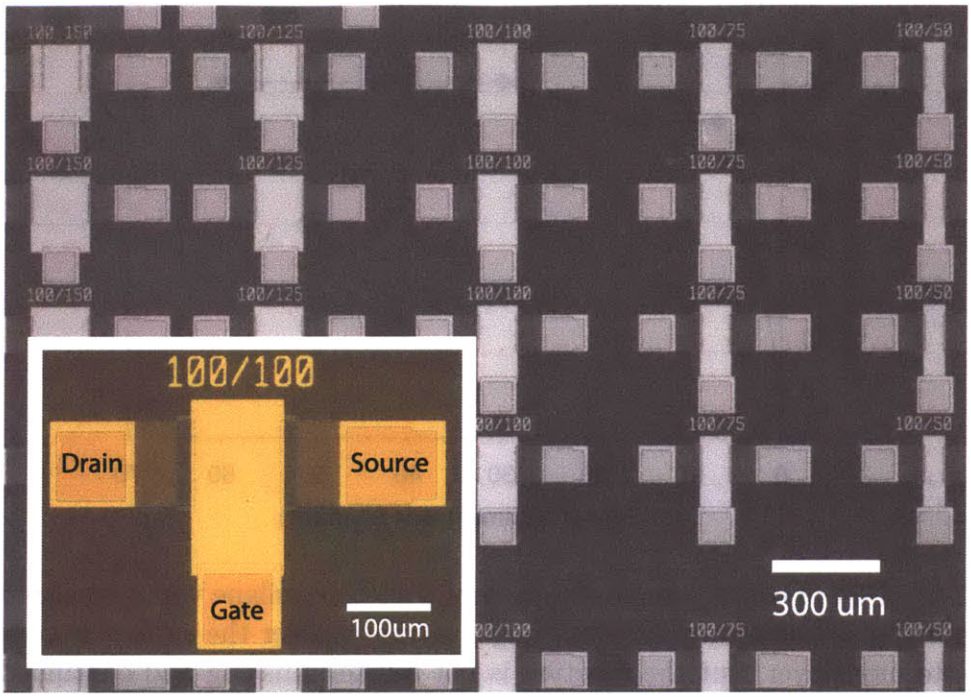

Figure 2-22: Micrograph of a fabricated array of single devices with varying channel lengths. The inset gives a larger view of a single field effect transistor (W/L = 100μm / 100μm).

2.5.5 Variations from the baseline process

The baseline process described in this section serves as a platform for study, allowing comparisons between devices fabricated on the same wafer, on different wafers with nominally the same process conditions, and on wafers with variations in the process parameters. (A fully detailed process flow including deposition conditions, etch times, photoresists used, etc. is given in Appendix A.)

An earlier version of the process used 15% O_2 during ZIO sputter of a 50nm-thick film and lacked the protective parylene layer [88]. With the exception of Chapter 3.2 which uses data collected from an early-process wafer, the results described in the following chapters were obtained from wafers fabricated using the baseline process and variations on the baseline process as noted.

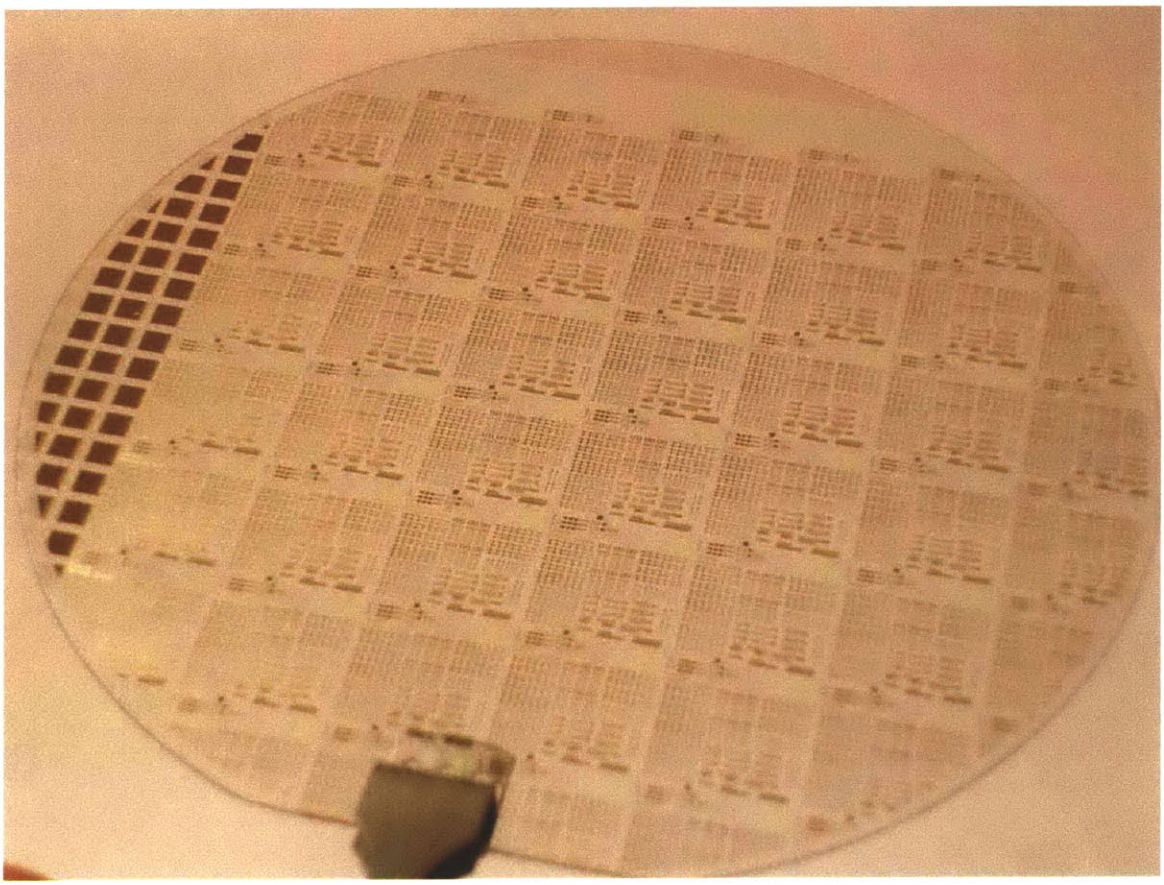

Figure 2-23: Photograph of a completed 100mm wafer. Each of the repeating die contains the same transistor arrays, test structures, and alignment marks. With the exception of the Cr/Au gate metal, all layers on the glass substrate are transparent.

Chapter 3

Device characterization and modeling

Unlike bulk crystalline silicon MOSFETs, amorphous oxide TFTs operate in accumulation. In the ZnO-based n-type oxide semiconductors, hole carrier concentrations and mobilities are so low that the channel does not invert. Instead, the charge carrier channel is formed when a gate bias is applied that causes electrons, the majority carriers, to accumulate at the semiconductor-dielectric interface.

Although the device is operated in accumulation rather than inversion, the resulting current-voltage (I-V) and capacitance-voltage (C-V) characteristics appear much like traditional silicon MOSFET curves. This similarity allows us to quantify device performance using nearly identical parameters.

This chapter discusses electrical characterization and modeling of the low temperature, lithographically-fabricated FETs. The first section (3.1) describes the transistor operation and discusses the underlying device physics. The second section (3.2) defines a standard set of parameters used to quantify device performance. In the third section (3.3), these extracted device parameters are used to compare transistor performance for fabricated FETs of varying channel lengths and channel widths. Shifting to simulation using Silvaco ATLAS, the fourth section (3.4) examines the effect of interface traps on I-V characteristics while the fifth (3.5) explores the effects of varying material and process parameters in order to guide device design. Finally, in the last

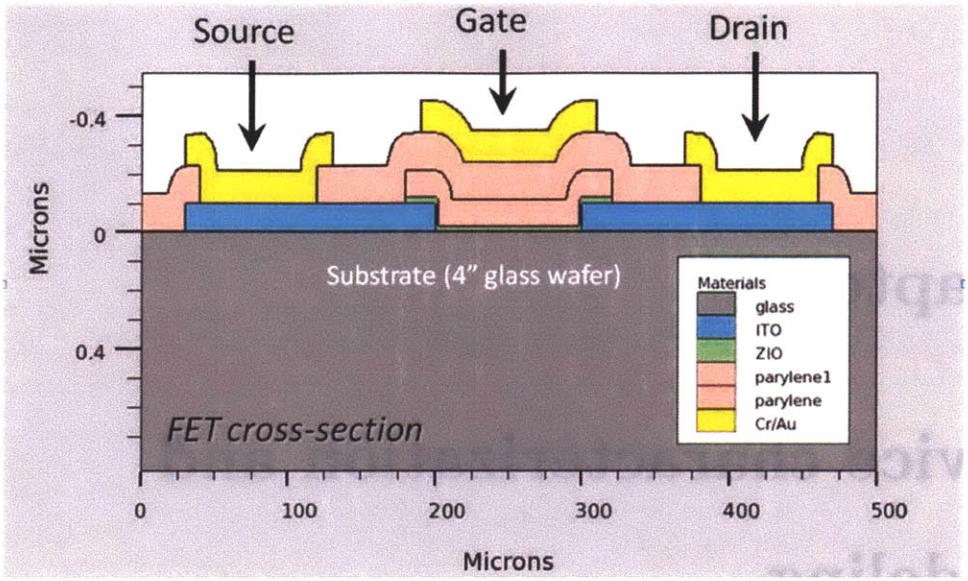

Figure 3-1: Cross-section of FET, drawn to scale using Silvaco ATHENA process simulation software and annotated with a graphics editor. Note that the horizontal axis spacings are much larger than the vertical axis spacings. In our fabricated top-gate, bottom-contact FET structure, the ZIO semiconductor layer is very thin (~10nm) compared to the parylene gate dielectric (~200-250nm), ITO source/drain contacts (100nm), and Cr/Au gate metal and contact pads (110nm). (See also Fig. 3-18.)

chapter section (3.6) the predicted effect of channel thickness on threshold voltage is verified by fabricating and characterizing FETs with varying channel thicknesses.

3.1 Device operation

Fig. 3-1 shows the cross-section of a metal oxide FET whose fabrication was described in the previous chapter. As shown by the axes in the figure, the horizontal dimensions are much larger than the vertical dimensions. These FETs can also be called thin-film transistors (TFTs); all layers are deposited as thin films on the substrate.

As stated in Chapter 1.4, the device operates in accumulation, i.e. carrier transport through the channel is dominated by majority carriers accumulated at the semiconductor-dielectric interface. Because the total drain current also includes a parallel contribution from mobile carriers in an undepleted "bulk," minimizing the semiconductor thickness is preferable in order to obtain threshold voltages close to zero. The effects of channel thickness and doping on threshold voltage, V_T, are dis-

cussed further in Sections 3.5 and 3.6.

The metal oxide FET in Fig. 3-1 is essentially a metal-insulator-semiconductor (MIS) capacitor with two contacts placed at either end of the semiconductor layer. The applied gate voltage bias, V_{GS}, controls the formation of a conducting channel which is accessed by the source and drain contacts. When a drain-to-source voltage, V_{DS}, is applied across the contacts, mobile carriers in the channel flow from source to drain to produce the drain current, I_D. An example current-voltage transfer characteristic is shown in Fig. 3-3. (Each of the parameters drawn on the plot is defined more specifically in Section 3.2.) The regions of operation are described below.

Cut-off

When V_{GS} is less than the turn-off voltage, V_{off}, the channel is fully depleted of carriers and no current flows through the channel regardless of V_{DS}. This situation is analogous to pinch-off in a junction-FET (JFET). The measured I_D is simply equal to the gate leakage current, I_G.

Subthreshold

As the applied V_{GS} becomes more positive, the semiconductor begins to come out of depletion and the carrier concentration in the channel rises exponentially with gate voltage [26]. The depletion width eventually shrinks to zero as V_{GS} approaches the flatband voltage, V_{FB}. For $V_{off} < V_{GS} < V_T$, the drain current is dominated by diffusion and $I_D \propto e^{qV_{GS}/nkT}$, where q is the electronic charge, n is the ideality factor, k is Boltzmann's constant, and T is the temperature in Kelvin. On a semi-log plot of the I_D-V_{GS} transfer characteristics, $\log(I_D)$ appears linear in this region.

Above Threshold

In a MIS capacitor, the onset of majority carrier accumulation at the semiconductor-dielectric interface occurs at the flatband voltage, V_{FB}. For $V_{GS} > V_{FB}$, the carrier concentration in the channel increases linearly with increasing V_{GS}. In an ideal accumulation mode FET, $V_T = V_{FB}$; this differs from the definition of V_T as the

onset of inversion in bulk c-Si MOSFETs. Nevertheless, the accumulated sheet charge of majority carriers functions in the same way as the inversion sheet charge in a c-Si MOSFET.

For $V_{GS} > V_T$, the drain current shifts from being dominated by diffusion current to drift current. At low V_{DS} biases (where $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$) the lateral electric field is small and the carrier density from source to drain is approximately constant. In this linear, or triode, region, the channel can be modeled as a resistor and I_D increases linearly with V_{DS}.

As V_{DS} increases, the transistor moves from the linear region into saturation (where $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$). The conducting charge layer at the interface becomes pinched-off at the drain end, and the slope of the I_D-V_{DS} characteristic decreases until I_D becomes nearly constant.

This c-Si MOSFET-like behavior above threshold can be observed from the output I-V characteristics, though as previously mentioned, the total I_D in an accumulation mode device includes an additional contribution from the undepleted "bulk" channel.

3.2 Quantified device performance

To explain the parameters used to quantify device performance, we use as an example the electrical characteristics from an early-process wafer, shown in Fig. 3-2. (Unlike the later "baseline" process wafers, the ZIO semiconductor for this wafer was sputtered in 15% O_2 for a 50nm-thick film and lacked the protective parylene layer.) The device dimensions are W/L = 100μm/100μm. Gate and drain bias voltages were swept from 0V to 20V for the output I-V curves in Fig. 3-2(a). The double-swept quasi-static C-V (Fig. 3-2(b)) was measured by holding source and drain at 0V while sweeping V_{GS} from -10V to 20V and back. Similarly, linear and saturation transfer I-V curves (Fig. 3-2(c)) were taken by holding V_{DS} fixed and sweeping V_{GS} from -10V to 20V and back.

Performing doublesweeps (i.e. sweeping the gate bias voltage forward and then back) serves as a method to identify hysteresis in the device. Possible causes of

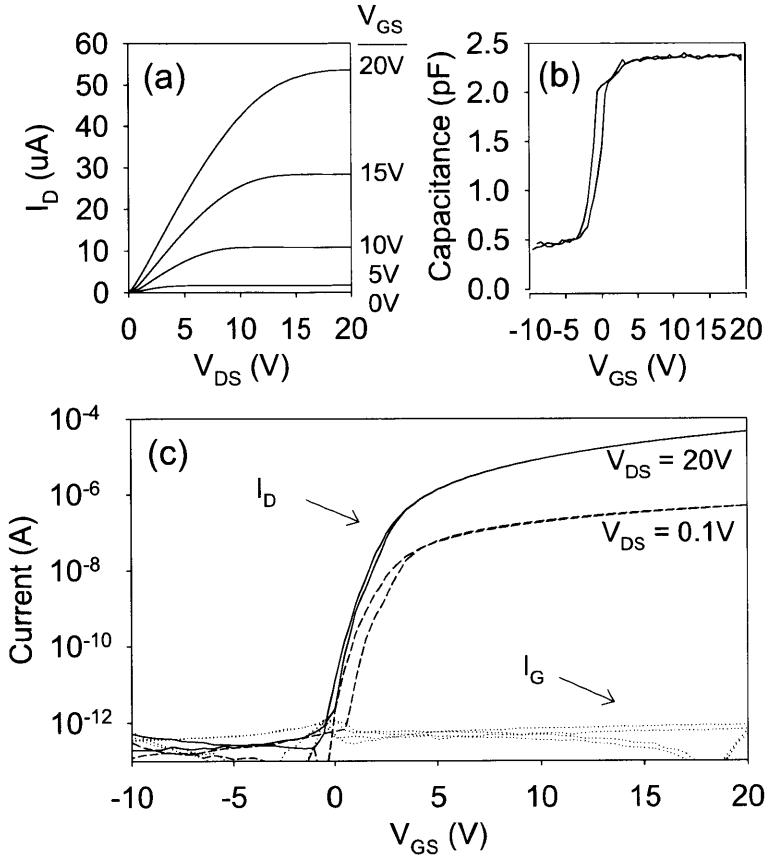

Figure 3-2: (a) Output I-V, (b) transfer I-V, and (c) quasi-static C-V curves for an early lithographic process wafer.

hysteresis include trap states in the semiconductor, charge injection into the dielectric, or slow relaxation of the gate dielectric [89]. Since measurement speed and voltage bias range will affect the observed hysteresis, a consistent set of measurement parameters is needed for meaningful comparisons between different devices.

Qualitatively, the output I-V in Fig. 3-2 looks like an ideal MISFET output curve with hard saturation for $V_{DS} \gg V_{GS}$ - V_T. To advance from single proof-of-concept FETs to being able to use the devices as circuit building blocks, however, requires more quantitative analysis. Plotting the full I-V and C-V characteristics of an FET gives us a detailed picture of device operation but for the purpose of circuit design, the extraction of a few relevant parameters is more useful. Some of these device parameters can be extracted from a single FET's characteristics, while others require analysis of multiple FET curves.

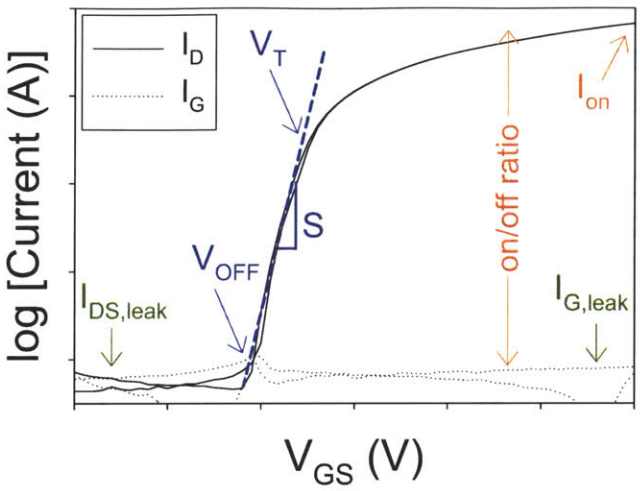

Figure 3-3: An example transfer I-V characteristic with relevant device parameters indicated on the plot.

An explanation of each parameter follows in the rest of this section.

3.2.1 Device parameter extraction

A number of relevant device parameters can be calculated from transfer characteristics alone. The definitions of several are pointed out in Fig. 3-3.

There are two components of leakage current in the device: gate leakage current, $I_{G,leak}$, and channel leakage current, $I_{DS,leak}$. The former, $I_{G,leak}$, is a measure of the leakage current through the gate dielectric and is determined by the quality and thickness of the dielectric. The latter, $I_{DS,leak}$, is a measure of how well the device can be turned off, i.e. that the channel can be depleted of carriers for negative gate voltage biases. Both should be minimized for optimal device performance. The turn-off voltage, V_{off}, is defined here as the voltage at which the drain current, I_D, falls below the gate leakage current $I_{G,leak}$.

The subthreshold swing, S, is the gate voltage needed to change the drain current by one decade when $V_{DS} < V_T$. It can be expressed by the equation $S = n\frac{kT}{q} \ln 10$ where n is the ideality factor, k is Boltzmann's constant, T is the temperature in Kelvin, and q is the electronic charge [26]. The parameter S is extracted from transfer I-V curves by taking the inverse of the slope of $\log(I_D)$ versus V_{GS} in the region below

threshold where I_D rises exponentially. A steep subthreshold slope is desirable; in the best case, n = 1 and S = 60mV/dec at room temperature [26]. In practice, typical reported values for S in metal oxide transistors currently range from 0.2V to >1V. Kawamura suggests that subthreshold slope in metal oxide FETs can be minimized by thinning the channel layer to obtain fully-depleted TFTs (similar to fully-depleted silicon-on-insulator transistors) and increasing the insulator capacitance for improved gate control [90]. The subthreshold characteristics can be degraded by the existence of interface or bulk traps, which will also affect threshold voltage.

In an ideal accumulation MISFET, the threshold voltage should correspond to the flatband voltage, i.e. the onset of carrier accumulation, which can be measured by C-V. Here, threshold voltage, V_T, is defined as the gate bias voltage at which I_D pulls away from linear dependence on V_{GS} in a semi-log I_D versus V_G plot.

Additional useful parameters are the on-current, I_{on}, at a given bias voltage and the on/off ratio. Unless otherwise specified, the I_{on} values in this work are measured at V_{GS} = 10V, V_{DS} = 10V. The on-current is affected by mobility, channel length, and contact resistance, and affects how fast a circuit can be operated or how much current it can supply. The current on/off ratio is a measure of the difference between the on-state and off-state of the transistor. An FET with a large on/off ratio potentially offers high on-state drive currents combined with low off-state power requirements.

From the quasi-static C-V plot the gate-source/drain overlap capacitance, $C_{overlap}$, can be found. This parasitic capacitance can be reduced by designing a device with layout that minimizes gate and source/drain electrode overlaps. The device moves from depletion into accumulation as the gate bias becomes more positive. In accumulation, the channel capacitance becomes equivalent to the gate dielectric insulator capacitance, C_{ins}.

Fig. 3-4 shows a doublesweep C-V curve with hysteresis. The interface and/or bulk traps that degrade subthreshold swing may also lead to hysteresis of the measured curves. The parallel shift in the C-V plot can be measured by the parameter V_{shift}. Because the amount of hysteresis depend on the speed of the measurement itself, comparisons between different transistor curves should ensure that the same

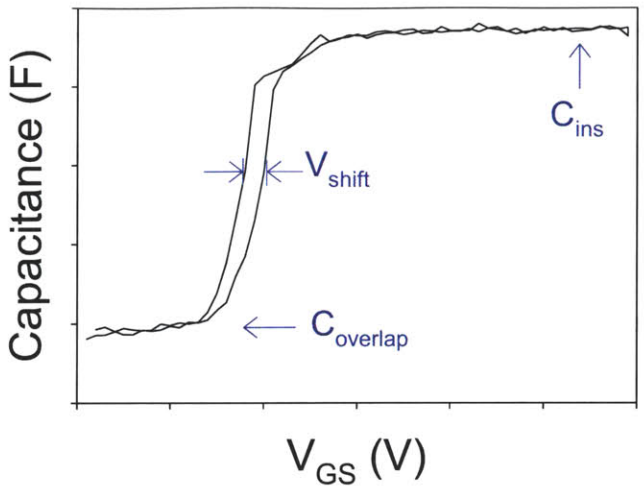

Figure 3-4: An example quasi-static C-V characteristic with relevant device parameters indicated on the plot.

measurement conditions were used.

Returning to the FET characterized in Fig. 3-2, we can condense the relevant information into the table shown (Table 3.1). Device performance quantified thus is much easier to compare across devices. Except for the last two lines, all the parameters extracted from a single curve. We now discuss mobility and contact resistance, which require analysis of multiple curves.

3.2.2 Mobility

Mobility is perhaps the most often cited figure of merit for oxide semiconductors, although it is not always defined the same way. Several methods for extracting effective carrier mobility in amorphous semiconductor FETs have been reported in literature. It is common to report mobility values calculated from saturation region transfer characteristics, borrowing the definition of saturation mobility from crystalline Si models. However, as noted by Hoffman [91] for oxide FETs and by Ryu *et al.* [92] for organic FETs, the assumptions of the ideal crystalline Si conduction models may not hold true for disordered semiconductors.

The mobility extraction method developed by Hoffman calculates an average mo-

Parameter	Value	Units
$I_{G,leak}$*	$<9x10^{-8}$	A/cm^2
$I_{DS,leak}$	2.4	$fA/\mu m$
S	0.7V	V/dec
V_{off}	~0V	V
V_T	2.0	V
on/off ratio	$\sim 10^8$	–
I_{on}*	450	$nA/\mu m$
$C_{overlap}$	<5	$fF/\mu m$
C_{ins}	19	nF/cm^2
V_{shift}	1.5	V
μ	12±0.8	cm^2/Vs
$R_{contact}$	~3	$M\Omega$-μm

* at V_{GS} = 20V

Table 3.1: Summary of device parameters calculated from an early-process wafer.

bility, μ_{avg}, from the channel conductance assuming drift-dominated charge transport. Noting the difficulty in estimating the induced charge in the channel, Q_{ind}, from a frequency-dependent measured capacitance, this derivation calculates Q_{ind} from simple electrostatics to be $Q_{ind} = C_{ins}[V_{GS} - V_{on,H}]$, where C_{ins} is the insulator capacitance and V_{GS} the gate-to-source bias. The parameter $V_{on,H}$ is defined as the gate voltage at which drain current begins to increase exponentially from the off-state; it is equivalent to the parameter V_{off} in Fig. 3-3. (An 'H' subscript was added to V_{on} to differentiate the parameter 'V_{on}' defined by Hoffman from that defined by Ryu, *et al.* Note that when gate leakage current is sufficiently low, $V_{on,H}$ is the same as the previously defined V_{off}.) Combining expressions for channel conductance and induced channel charge yields the following equation for average mobility at low drain-to-source bias ($V_{DS} \rightarrow 0$):

$$\mu_{avg} = \frac{G_{ch}(V_{GS})}{\frac{W}{L} C_{ins}[V_{GS} - V_{on,H}]} \tag{3.1}$$

where G_{ch} is the channel conductance as a function of V_{GS}.

As Hoffman notes, this expression appears almost the same as that for Si MOSFET mobility in the linear regime, μ_{eff}, except that threshold voltage, $V_{T,lin}$, is replaced here by $V_{on,H}$. Fig. 3-5 plots the linear region transfer characteristic for a

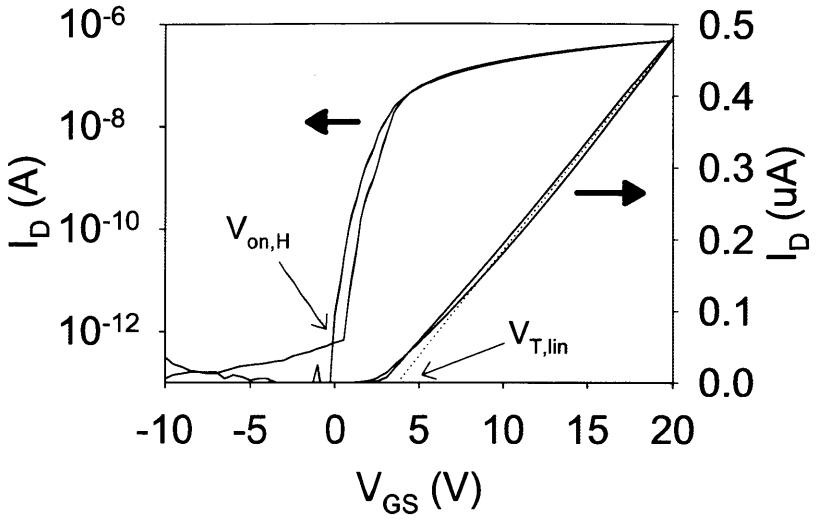

Figure 3-5: Transfer current-voltage (I-V) characteristics for a W/L = 100μm/100μm zinc indium oxide FET at V_{DS} = 1V. The same curve is plotted on both log and linear scales, and $V_{on,H}$ and $V_{T,lin}$ are pointed out for comparison. The 3.8V difference between $V_{on,H}$, the gate voltage at which drain current beings to increase exponentially from the off-state, and $V_{T,lin}$, as commonly found by linear extrapolation method, leads to a discrepancy in the calculated channel charge used in mobility calculations.

100μm x 100μm FET on both log and linear scales and compares $V_{T,lin}$, found by the commonly-used linear extrapolation method, with $V_{on,H}$. As shown, $V_{on,H}$ = 0V is several volts lower than $V_{T,lin}$ = 3.8V. The higher calculated value of μ_{eff} = 15cm^{2}V^{-1}s^{-1} compared to μ_{avg} = 12cm^{2}V^{-1}s^{-1} results from an underestimation of induced channel charge, which must be accurately determined for mobility calculations.

The method proposed by Ryu *et al.* [92] also starts from simple electrostatics but calculates the total sheet charge density by integrating over the quasi-static capacitance-voltage curve, $Q = \int_{-\infty}^{V_{GS}} \left(\frac{C_{ch}}{WL}\right) dV$, where the channel capacitance, C_{ch}, is the capacitance due to charge induced in the semiconductor. In this derivation, the model parameter $V_{on,R}$ can be defined from the C-V characteristic such that the total integrated charge $Q = -\frac{C_{ch,accumulated}}{WL}(V_{GS} - V_{on,R})$. (An 'R' subscript was added to V_{on} to differentiate the parameter 'V_{on}' defined by Ryu, *et al.* from that defined by

	Charge mobility ($cm^2V^{-1}s^{-1}$)	
L (μm)	Hoffman (μ_{avg})	Ryu, *et al.* (μ)
50	13.1	12.7
100	11.8	11.4
150	11.2	11.2
200	11.2	10.8

Figure 3-6: The table summarizes mobility values calculated in the linear region (V_{DS} = 100mV) with V_{GS} = 20V for 50, 100, 150, and 200μm channel length FETs. Two methods used to calculate mobility (following Hoffman [91] and Ryu, *et al.* [92]) are compared. The channel width for all devices was 100μm.

Hoffman.)The calculated channel mobility, μ, is given by

$$\mu = \frac{I_D}{W \int_{-\infty}^{V_{GS}} \left(\frac{C_{ch}}{WL}\right) dV} \left(\frac{L}{V_{DS}}\right) \tag{3.2}$$

The calculated channel mobility is then an average mobility over the total gate-bias induced charge, which includes free and trapped charges.

A comparison of the mobility values obtained using each of these methods is shown in Fig. 3-6. The table lists values for devices with channel width of 100μm and four different channel lengths (50μm, 100μm, 150μm, 200μm); the reported values were taken near V_{GS} = 20V when V_{DS} = 100mV. For all channel length devices, both the Hoffman (μ_{avg}) and Ryu, *et al.* (μ) methods give similar values. The slightly lower μ values suggest that not all the channel charge is accounted for in μ_{avg}, but for $V_{GS} \gg V_{on}$ the difference does not appear significant. Overall, the calculated mobility values are very similar for transistors of different channel lengths. Both μ_{avg} and μ are (12$\pm$0.8) $cm^2V^{-1}s^{-1}$ across the four different channel length transistors shown in Fig. 3-6.

We prefer the Ryu method for mobility calculations because the Hoffman estimation of induced channel charge may not be accurate for FETs whose transfer curves are non-ideal. Further comments on parameter extraction for non-ideal electrical characteristics are given in Section 3.2.4.

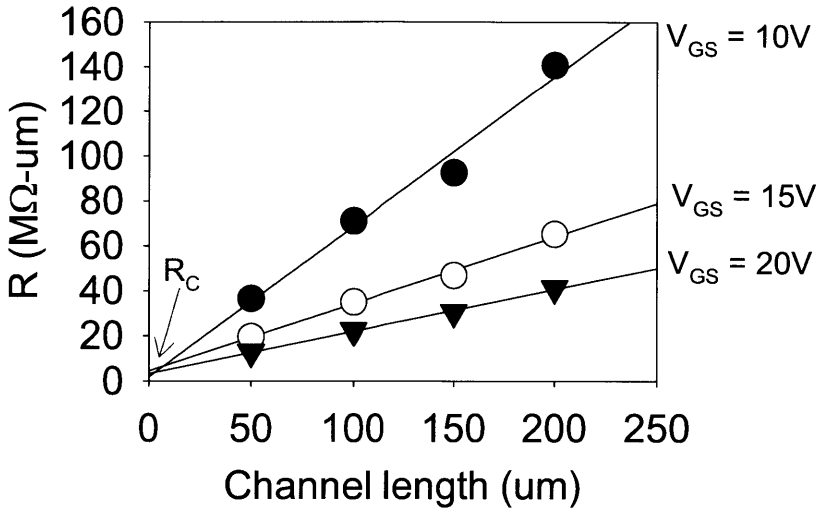

Figure 3-7: Contact resistance is calculated using the transfer length method. Total resistance for four devices with different channel lengths is plotted and extrapolated to L = 0.

3.2.3 Contact resistance

Ideally, carrier injection to the channel is unimpeded by potential barriers between the semiconductor channel and the metal contacts; this is rarely the case. Contact resistance, R_c, can be calculated using the transfer length method [93]. Fig. 3-7 plots measured resistance ($R_m = V_{DS}/I_D$) for four different channel length devices at V_{DS} = 1V and V_{GS} = 10V, 15V, and 20V. The measured resistance R_m is a linear combination of the channel resistance and the source and drain contact resistances, and depends on the applied gate voltage. The contact resistance is found by extrapolating to L = 0, as shown in Fig. 3-7.

High contact resistances can sometimes be seen in output curves as a "bird's beak," i.e. at low V_{DS} the drain current I_D does not rise linearly. When R_c is large, the effective voltage bias across the channel will be less than the bias applied at the contacts, which can affect parameters extracted from current-voltage sweeps such as mobility. Ryu has shown in pentacene FETs that channel-length dependence in calculated mobility values reflects the effects of high contact resistance rather than actual effective carrier mobility, an effect that vanishes when contact resistance is accounted for [94].

3.2.4 Validity of parameter extraction

To handle data from multiple devices, die, and wafers, we wrote an Excel VBA program to automate data plotting and parameter extraction. Automation allows rapid and consistent handling of data, but it is important to sanity check the output values for outliers and non-idealities. For example, the device in Fig. 3-8 does not show the smooth exponential rise expected for a transfer I-V curve. The standard parameters (S, V_T) cannot fully describe the hump that appears in the I-V curve. For electrical characteristics that do not match the model in Fig. 3-3, the meaning of extracted device parameters becomes ambiguous.

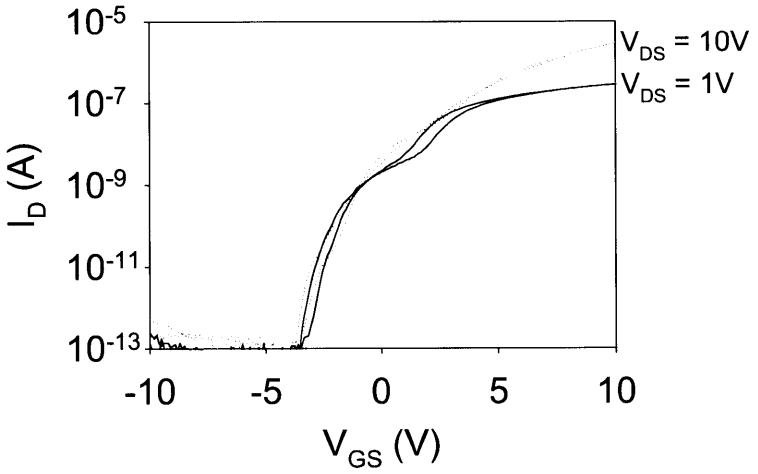

Figure 3-8: Non-idealities in measured electrical characteristics cause ambiguity in device parameter extraction. The saturation and linear region transfer I-V characteristics in the above plot show a hump that cannot be described by the standard model parameters in Fig. 3-3.

A different concern arises for the calculation of R_c, which requires plotting data from multiple FETs. In some cases, non-uniformities between devices (e.g., different V_T or R_c) result in a scatterplot for R_m vs. L from which R_c cannot be extracted. For data sets where a value for R_c cannot be found, mobility calculations will not be significantly affected when contact resistance is small, but for high contact resistances the uncorrected calculated mobility will be lower than actual.

With these caveats in mind, we will discuss device performance of FETs fabricated in the baseline lithographic process.

3.3 Baseline lithographic FET characterization

Devices fabricated in the baseline lithographic process (described in Chapter 2) were characterized in the dark using an Agilent 4156C Semiconductor Parameter Analyzer. To confirm that the devices functioned as transistors, the output I-V curves were measured by sweeping V_{DS} from 0V to 10V for fixed V_{GS} values, which were stepped in 2V increments from 0V to 10V. Linear and saturation transfer I-V curves were then measured by holding V_{DS} fixed and double-sweeping V_{GS} from -10V to 10V and back. The doubleswept quasi-static C-V curves were measured by holding source and drain at 0V while sweeping V_{GS} from -10V to 10V and back.

To allow meaningful comparisons of the collected data for different devices, settings for step voltage, hold and delay times, integration time, etc. were kept uniform. Although the 4156C can be directly controlled from the front panel, we designed a LabView program to control the 4156C and simplify the process of programming measurement settings and saving the data.

This section compares the results from a number of devices characterized using this standardized procedure.

3.3.1 Comparison of varying channel length FETs

As shown previously in a photomicrograph (Fig. 2-22) arrays of FETs with varying channel lengths were fabricated in repeating die across each 100mm wafer. This allows us to compare not only FETs of the same W/L but also the characteristics of FETs with different geometries for additional insights.

The electrical characteristics for a set of devices in the same die are shown in this section. Fig. 3-9 plots the transfer curves for FETs of different channel lengths at V_{DS} = 1V; Fig. 3-10 shows the transfer curves for the same devices at V_{DS} = 10V. Fig. 3-11 plots the corresponding quasi-static C-V characteristics. Note that capacitance scales with channel length (L = 200, 150, 100, 50, and 25 μm) because the channel width is 100μm for all devices (i.e. channel area is proportional to channel length). From this data, we can extract all the device parameters described in the previous

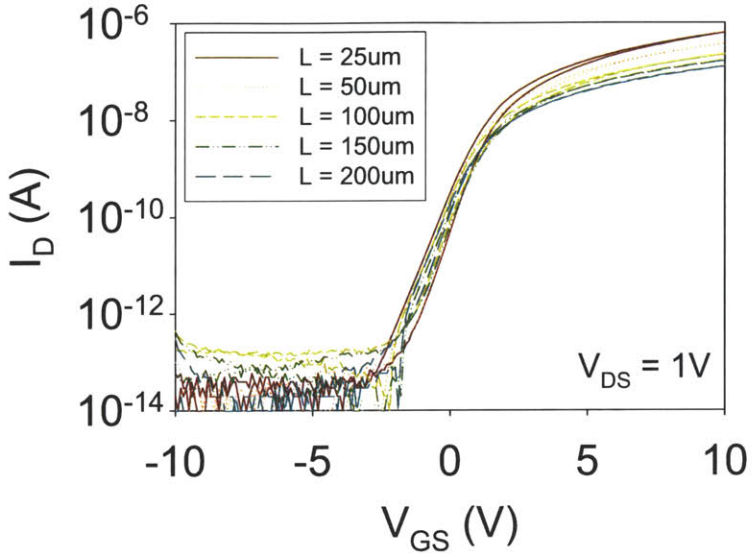

Figure 3-9: Overlay plot of linear region transfer I-V characteristics for FETs with W = 100μm and varying L. Each doubleswept curve is measured at V_{DS} = 1V and swept from V_{GS} = -10V to 10V and back.

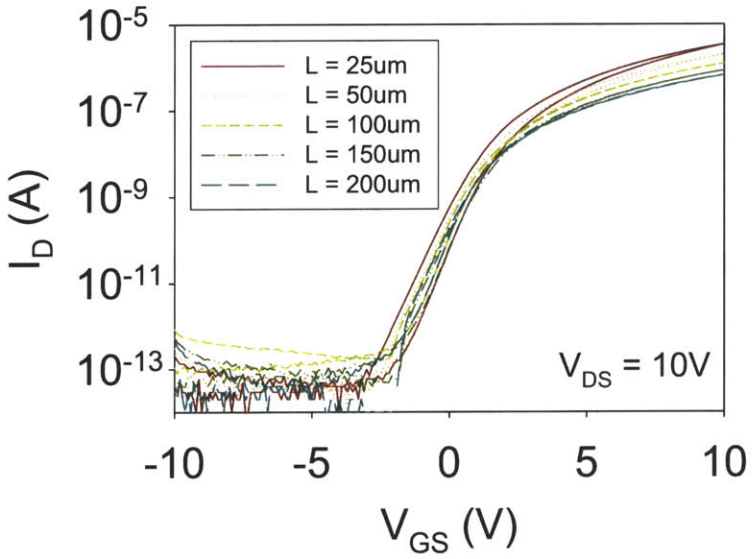

Figure 3-10: Overlay plot of saturation region transfer I-V characteristics for FETs with W = 100μm and varying L. Each doubleswept curve is measured at V_{DS} = 10V and swept from V_{GS} = -10V to 10V and back.

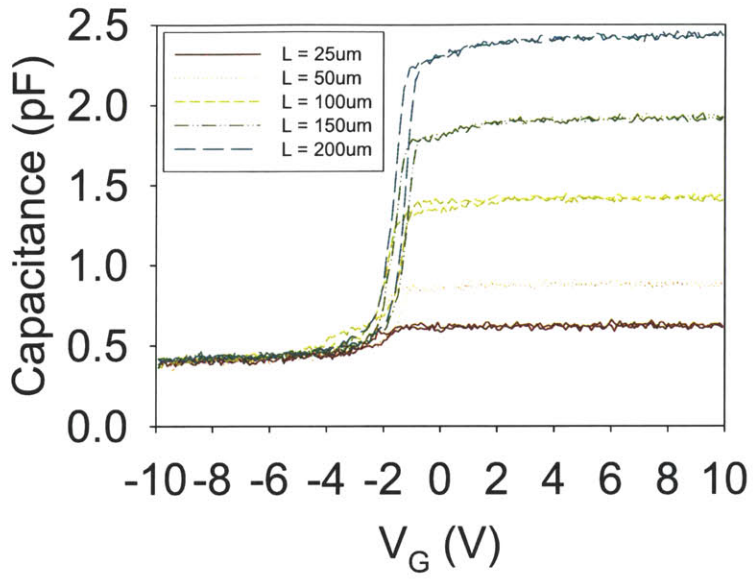

Figure 3-11: Overlay plot of quasi-static C-V characteristics for FETs with W = 100μm and varying L. Accumulation capacitances scales with channel length, but overlap capacitance remains constant. Each doubleswept curve is measured from V_{GS} = -10V to 10V and back.

L	200	150	100	50	25	μm
W	100	100	100	100	100	μm
$I_{G,leak}$ **	1.20	2.20	5.10	1.30	1.10	fA/μm
$I_{DS,leak}$	0.10	0.30	1.60	0.10	0.10	fA/μm
S	0.77	0.76	0.75	0.75	0.74	V/dec
V_{off}	-2.7	-2.3	-2.1	-2.7	-2.9	V
V_T	0.9	1.2	1.0	1.0	0.7	V
on/off	$3x10^6$	$4x10^6$	$6x10^6$	$5x10^7$	$8x10^7$	–
I_{on} **	6.7	8.7	12.6	21.0	35.5	nA/μm
$C_{overlap}$	4.2	4.1	3.9	3.9	3.9	fF/μm
C_{ins}	10.1	10.0	10.2	9.8	9.1	nF/cm_2
V_{shift}	0.5	0.5	0.5	0.8	0.8	V
mobility **	2.5	2.6	2.2	2.4	2.9	cm^2/Vs

** at V_{GS} = 10V

Table 3.2: A summary of device parameters extracted from FETs of varying channel lengths and W = 100μm. Values are normalized per micron channel width or per square cm channel area as appropriate.

section.

Table 3.2 summarizes the extracted FET device parameters, normalized per micron channel width or per square centimeter area as appropriate. Displaying the data in this form enables easy comparisons of device performance. While some variations is expected due to process non-uniformities, there are some clear differences between the different channel length devices.

Certain parameters are expected to remain invariant to channel length. Overlap capacitance depends on the overlap between source/drain and gate electrodes and is determined by channel width, not length. In addition, the normalized insulator capacitance depends only on dielectric thickness. For this set of devices, $C_{overlap}$ = 4.0±0.1fF/μm and C_{ins} = 9.8±0.4 x10^{-9}F/cm^2. Similarly, the normalized leakage currents, $I_{DS,leak}$ and $I_{G,leak}$, do not show channel length dependence.

The gate leakage currents of $\sim 10^{-9}$A/cm^2 (at V_{GS} = 10V, or applied field $\approx$ 0.5MV/cm) through parylene are competitive with other dielectrics in the literature. Pereira, *et al.* reported leakage currents of 10^{-9}A/cm^{-2} at 10V through optimized HfO_2 and HfO_2/SiO_2 films 180nm thick [22]. In comparison, Choi, *et al.* reported leakage current densities of 10^{-9}A/cm^2 for 300nm-thick thermal oxide and 10^{-8}A/cm^2 for 350nm-thick PVP, both at an applied electric field of 1.5MV/cm [66].

The low gate leakage currents contribute to the high on/off ratios $>10^6$ across all devices. As can also be seen qualitatively on the transfer I-V plots, subthreshold slope (0.76V±0.1V/dec)is uniform across all channel lengths. This subthreshold slope is lower than previously reported ZIO FETs with RT-deposited gate dielectrics [95, 96] though poorer than other reported ZIO FETs [97].

The calculated mobility, μ=2.5±0.3cm^2/Vs, is an order of magnitude lower than the highest values reported in the literature, but it is notable that our values are for an unoptimized and unannealed material. Mobility could be improved by material optimization; however, that is not the focus of this thesis.

The slight variation in V_{off} and V_T values in Table 3.2 reflect both device variation and some subjectivity in defining the exact values. There is not a clear trend with channel length for either V_{off} or V_T; on the other hand, the on-current I_{on} measured

at $V_{GS} = 10V$ clearly increases with decreasing channel length. These results follow our expectations, as described below.

If we think of the transistor channel fundamentally as a resistor whose carrier concentration, n, and hence resistivy, ρ, are controlled by the gate, we expect the gate bias at which current begins to flow through the device to be independent of channel length. Table 3.2 indeed shows no channel length dependence for V_{off} and V_T. On the other hand, if we combine the equation for the resistance of a bulk semiconductor

$$R_{channel} = \frac{\rho \times L}{Wt}$$

where L is the length, W is the width, and t is the thickness [98], with Ohm's Law

$$I_{on} = \frac{V_{DS}}{R_{channel}} = \frac{V_{DS}Wt}{\rho \times L}$$

we see that the on-current I_{on} does depend inversely on channel length. In this simplified analysis, we assume that the resistivity of the channel is dominated by the accumulated carriers at the semiconductor-dielectric interface and hence t should be thought of as the thickness of the accumulation layer rather than the entire semiconductor material thickness. Note that I_{on} is measured at high V_{GS} when the channel is strongly accumulated. If the total resistance is dominated by the channel rather than source/drain or contact resistances, then $I_{on} \times L$ will be constant. Fig. 3-12 shows that $I_{on} \times L$ is approximately constant. The decrease in $I_{on} \times L$ at shorter channel lengths can be attributed the fact that we have neglected to account for contact resistance, which can be modeled as an additional series resistance. As the channel length is reduced and channel resistance decreases, the contribution of contact resistance to the total resistance becomes proportionally larger and the calculated $I_{on} \times L$ through the device is diminished.

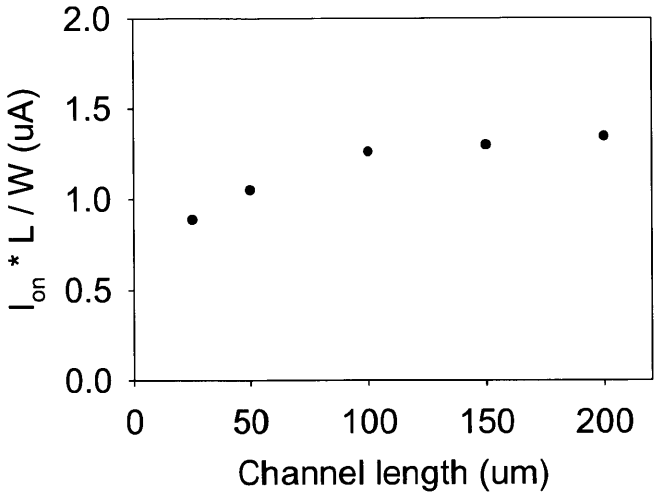

Figure 3-12: Plot of normalized $I_{on} \times L$ for FETs with W = 100μm and varying L. The values are approximately constant with channel length; the slightly lower $I_{on} \times L$ at shorter channel lengths can be attributed to contact resistance, which was not accounted for and becomes proportionally more significant as channel length and hence channel resistance decrease.

3.3.2 Comparison of varying channel width FETs

Although the original mask set only included arrays of FETs with varying lengths, we added arrays of FETs with uniform L and varying W to each die in a later mask design. For the devices shown in this section, L is fixed at 25μm and W = 25, 50, 100, 125, 250, and 500μm to yield W/L ratios of 1, 2, 4, 5, 10, and 20. Because channel length is fixed, we expect all device parameters to share the same values after scaling for width.

Following the same procedure as in the previous section, the characterized devices are all located in the same die (though from a different wafer from the previous section). Transfer I-V characteristics at V_{DS} = 1V and V_{DS} = 10V are plotted on both linear and log scales in Figs. 3-13 and 3-14, respectively. Qualitatively, on a linear scale all transfer I-Vs appear similar to the ideal silicon MOSFET model: in the triode region (Fig. 3-13, left) the I-V curves rise linearly above $V_T \sim$ 0V, and in the saturation region (Fig. 3-14, left) the I-V curves are nearly square-law. The low leakage currents contribute to high on/off current ratios, which are summarized together with other device parameters in Table 3.3.

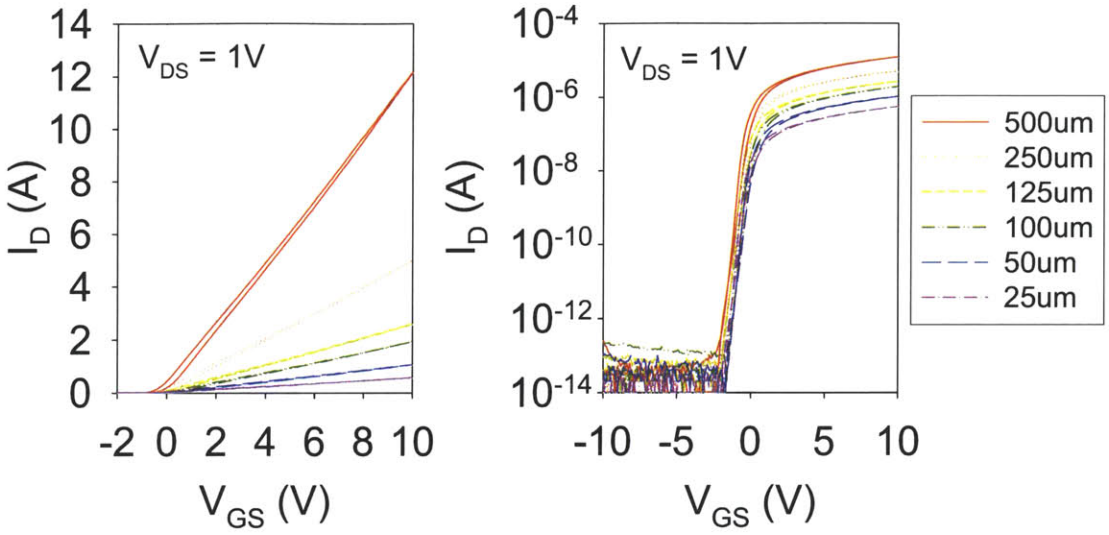

Figure 3-13: Linear region transfer I-V characteristics for FETs with varying channel widths are plotted on linear scale (left) and semi-log scale (right). The doublesweeps are measured at V_{DS} = 1V and show linear behavior for $V_{GS} > V_T$. The device dimensions are L = 25μm and W = 25, 50, 100, 125, 250, and 500μm.

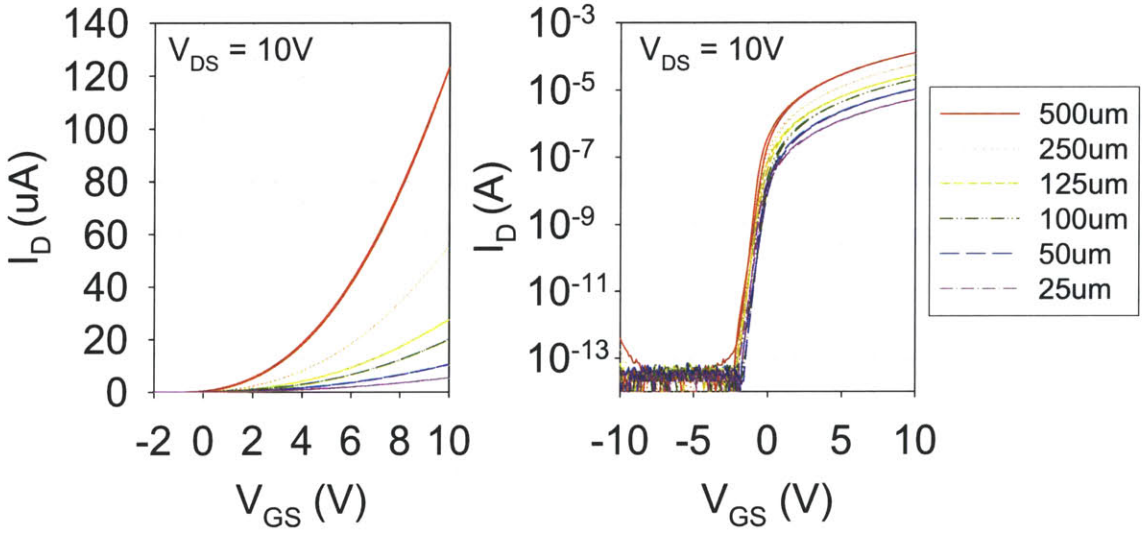

Figure 3-14: Saturation region transfer I-V characteristics for FETs with varying channel widths are plotted on linear scale (left) and semi-log scale (right). Measured at V_{DS} = 10V, the doublesweeps show sharp subthreshold slopes of 0.33V/dec and square-law behavior for $V_{GS} > V_T$. The device dimensions are L = 25μm and W = 25, 50, 100, 125, 250, and 500μm.

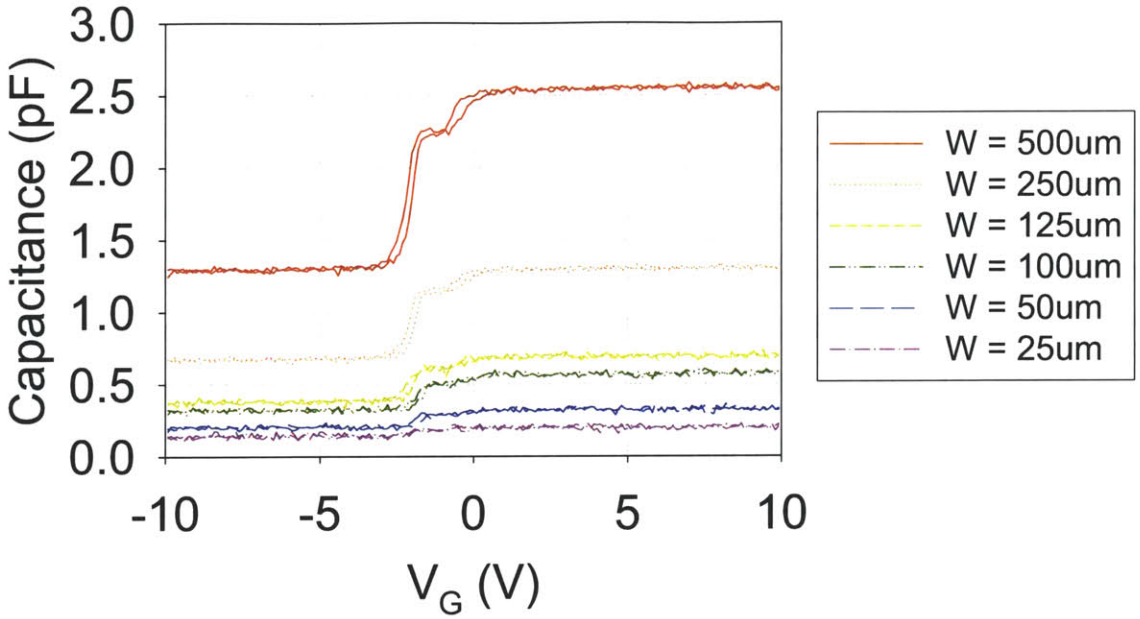

Figure 3-15: Overlay plot of quasi-static C-V characteristics for FETs with L = 25μm and W = 25, 50, 100, 125, 250, and 500μm. Both accumulation and overlap capacitances scale with channel width. Each doubleswept curve is measured from V_{GS} = -10V to 10V and back.

L	25	25	25	25	25	25	μm
W	25	50	100	125	250	500	μm
$I_{G,leak}$ **	1.20	0.40	0.30	0.24	0.16	0.38	fA/μm
$I_{DS,leak}$	0.40	0.20	0.10	0.08	0.04	0.02	fA/μm
S	0.33	0.33	0.33	0.34	0.32	0.34	V/dec
V_{off}	-2.1	-1.9	-1.8	-2.3	-2.2	-2.5	V
V_T	-0.2	0.0	0.1	-0.2	-0.2	-0.2	V
on/off	2x10^8	3x10^8	6x10^8	8x10^8	1x10^9	2x10^9	–
I_{on} **	208	204	197	220	221	246	nA/μm
$C_{overlap}$	5.5	4.1	3.2	3.0	2.7	2.6	fF/μm
C_{ins}	11.2	10.2	10.2	10.2	10.1	10.1	nF/cm$_2$
V_{shift}	0.5	0.4	0.3	0.3	0.3	0.2	V
mobility **	4.1	4.7	4.2	4.3	4.3	5.1	cm^2/Vs

** at V_{GS} = 10V

Table 3.3: Summary of extracted device parameters for FETs with fixed channel length (L = 25μm) and varying channel widths. Values are normalized per micron channel width or per square cm channel area as appropriate. All devices are located in the same wafer die.

Fig. 3-15 shows the corresponding quasi-static C-V characteristics. Similarly to Fig. 3-11 in the previous section, the accumulation capacitance scales with increasing device area. However, since in this case device area scales with width, not length, the total gate-source/drain overlap capacitance also increases with the device area. The normalized values in Table 3.3 verify that capacitance scales with device size. For the set of devices in Fig. 3-15, C_{ins} = 10.3±0.4 x10^{-9}F/cm^2 and $C_{overlap}$ = 3.5±1.1fF/μm. The apparent slight width dependence in $C_{overlap}$ is likely caused by greater sensitivity to measurement error and fringing capacitances as the device area decreases by 20x.

The ideal silicon MOSFET model predicts that drain current scales proportionally with W/L ratio. Previously, Hsieh, *et al.* demonstrated drain current scaling with W/L for ZnO FETs with a Al_2O_3/HfO_2 dielectric and L $\geq$ 5μm [99]. A comparison of the values in Table 3.3 shows that our lithographically patterned ZIO FETs follow expected channel width scaling behavior as well. Fig. 3-16 shows the linear relationship between I_{on} and L. At V_{GS} = V_{DS} = 10V, the width-normalized I_{on} = 220±17 nA/μm for all devices from W = 25μm to 500μm. Furthermore, device parameters expected to be invariant to channel width are shown to be nearly uniform across all devices: S = 0.33±0.007V/dec, V_{off} = -2.1±0.26V, V_T = -0.1±0.1V, μ = 4.4±0.38cm^2/Vs.

We found that subthreshold slope varied from wafer-to-wafer, likely due to process variations that affected the semiconductor-dielectric interface. The data in Tables 3.2 and 3.3 were extracted from two different wafers. While subthreshold slope is uniform for all devices in each table, in the former S $\sim$ 0.75V/dec while in the latter S $\sim$ 0.33V/dec. On most of the wafers we fabricated and characterized over the course of this project, subthreshold slopes generally fell in this range. In Section 3.4.2 we speculate on possible reasons for non-ideal subthreshold slope in these devices.

3.3.3 Comparison across wafer lots

In addition to comparing devices in a single die, a standard set of extracted FET device parameters can be used to quickly compare devices across a wafer. Device

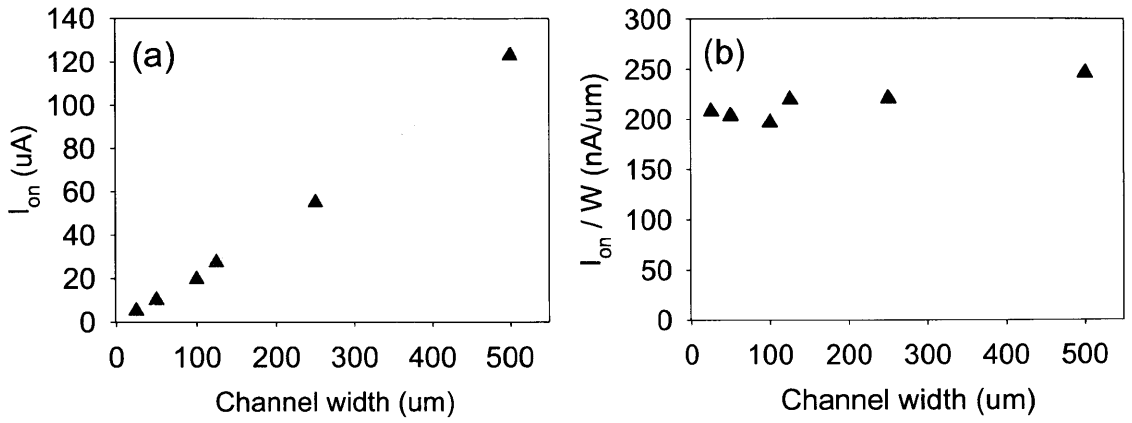

Figure 3-16: Plot of I_{on} versus W for FETs with L = 25μm, demonstrating (a) the linear relationship between I_{on} and channel width, and (b) that normalized for width, I_{on}/W is approximately constant.

performance can also be monitored across wafer lots. Comparison of tables is much easier, quicker and more meaningful than trying to compare line plots qualitatively.

Plotted in Fig. 3-17 are the I-V and C-V curves for devices in two different wafer lots fabricated months apart (one in March 2009, the other in December 2009) using the baseline process. All process parameters are nominally the same, and the device dimensions are W/L = 100μm/100μm. Qualitatively, the electrical characteristics for both devices look similar; a more quantitative comparison is given in Table 3.4 which summarizes relevant device parameters. The minor differences between the two devices help confirm that device performance is comparable despite the gap in process times.

From a processing standpoint, wafer summary tables are also useful for diagnosing problem/trends arising from process drift. Machine conditions, sputter targets, source materials change over time and usage, and process variations strongly affect the device performance. In one case, we noticed a gradual increase in gate leakage currents over several wafer lots. This issue indicated a possible problem with the parylene dimer source material that was resolved when the dimer was replaced.

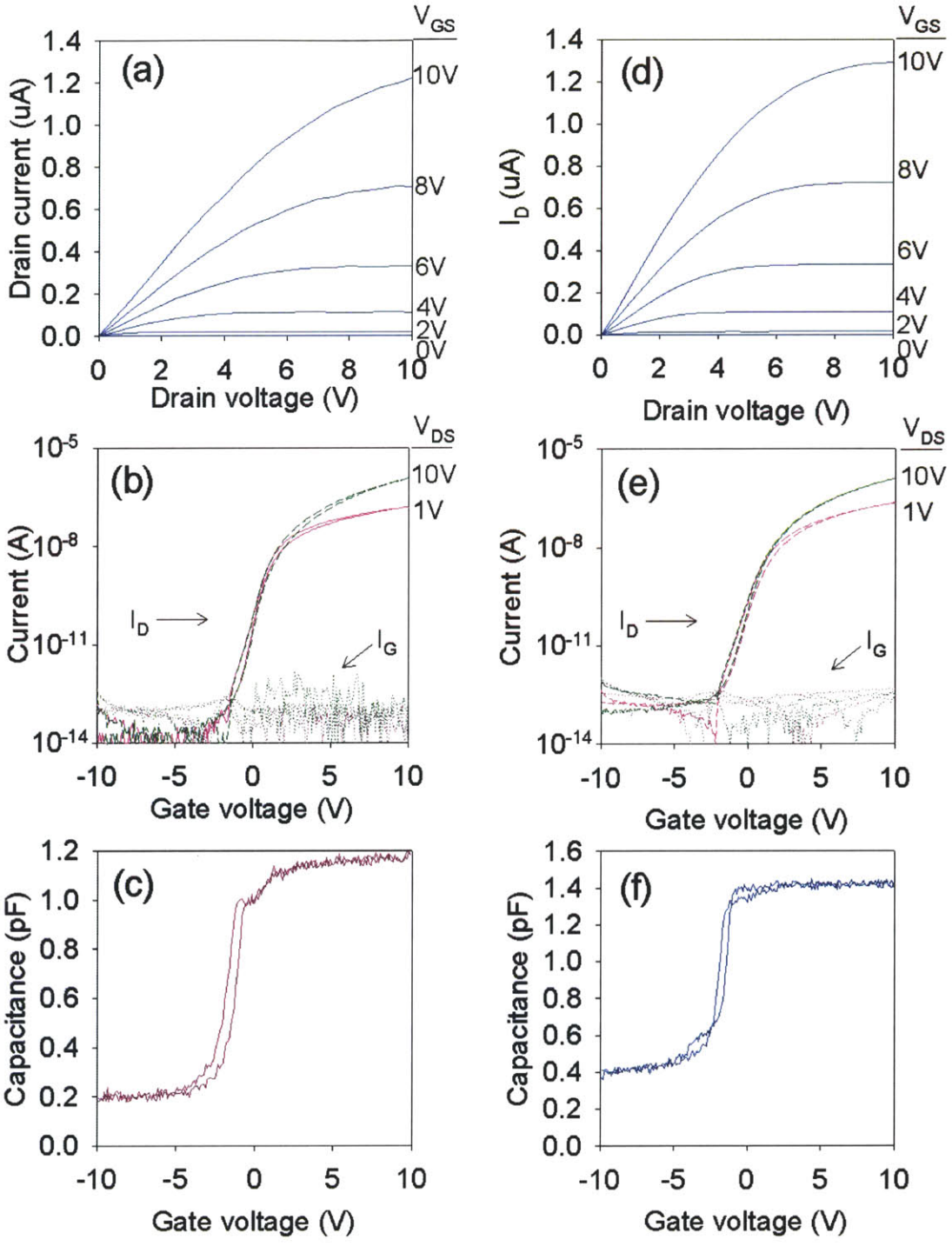

Figure 3-17: Comparison of electrical characteristics for devices in two separate wafer lots fabricated using the baseline process. Output I-V, transfer I-V, and quasi-static C-V curves for an FET on wafer MO11Q2 are shown in (a-c); the same for wafer MO11U5 are shown in (d-f). The device dimensions for both FETs are W/L = 100μm/100μm.

	MO11Q2	MO11U5	
L	100	100	μm
W	100	100	μm
$I_{G,leak}$ **	0.10	5.10	fA/μm
$I_{DS,leak}$	0.10	1.60	fA/μm
S	0.59	0.75	V/dec
V_{off}	-2.0	-2.1	V
V_T	1.1	1.0	V
on/off	$2x10^7$	$6x10^6$	–
I_{on} **	11.7	12.6	nA/μm
$C_{overlap}$	2.0	3.9	fF/μm
C_{ins}	9.7	10.2	nF/cm^2
V_{shift}	0.7	0.5	V
mobility **	1.4	2.2	cm^2/Vs
$R_{contact}$	–	10^2	MΩ-μm

** at V_{GS} = 10V

Table 3.4: Summary of extracted device parameters for FETs from two wafer lots. The parameter values are extracted from the I-V and C-V plots shown in Fig. 3-17.

3.4 Modeling of fabricated FETs

Simulation is a useful complement to experimental work for studying FET behavior. Although the actual device physics may be very complex, further insights may be gained by using a model that accurately reproduces the experimental I-V characteristics with a minimal set of parameters. We briefly overview several models that have been used to fit oxide-based FETs before discussing our approach and simulation results.

3.4.1 Background and approach

There are a number of models used in the literature to model amorphous oxide FETs. It is common to simply use the crystalline silicon model, as is often the case for mobility calculations. Despite the questionability of whether its underlying assumptions apply to oxide semiconductors, the advantage is that it is a simple, well-known ana-

lytical model that appears to fit experimentally.

Hong, *et al.* suggested several refinements to the square law model in order to account for oxide TFT non-idealities [100]. While retaining fairly simple analytical models, they consider the effects of series resistance at the source and/or drain, the presence of an undepleted "bulk" layer, varying channel mobility, and a discrete electron trap. Using these models, they demonstrated good agreement with experimental data for a SnO_2 TFT for a wide range of applied V_{GS}. While offering useful insight to the effect of discrete traps, however, the models do not accurately reproduce the experimental data in the subthreshold region.

Another approach is to borrow the models of another disordered semiconductor, amorphous silicon. Like oxide FETs, a-Si TFTs operate in accumulation mode. The a-Si models have been fairly well developed [101, 102], and a number of simulation tools for a-Si TFTs commercially available. Several research groups have applied these tools and models to oxide FETs [103–105]. However, in some cases, as noted in a paper by Fung, *et al.*, numerical simulations result in a good fit for experimental I-V curves but do not include a solid physical justification for the fitting parameters [106].

One issue with using a-Si models is that the amorphous oxide semiconductors are not a-Si. Hoffman notes that the sophisticated models for a-Si TFTs are tailored to the specific material system and include non-idealities that are not generally applicable to all non-ideal TFTs [107]. The effects of bond angle disorder that plague a-Si TFTs are not applicable to oxide FETs, whose conduction bands are primarily composed of spherically symmetric *s*-orbitals [108]. In addition, Robertson points out that for oxide semiconductors high doping or oxygen vacancy concentrations can raise the Fermi level, E_F, above the conduction band edge. In contrast, E_F in a-Si will be pinned below the donor level by auto-compensation and the formation of Si dangling bonds, preventing the formation of metallic a-Si [109, 110].

Unlike a-Si, the chemical bonding in amorphous oxides is strongly ionic rather than covalent [111]. Hosono argues that conduction is band-like, rather than by hopping [12]. This suggests that for the purpose of modeling electrical characteristics, it is possible to treat amorphous oxides similarly to c-Si. In fact, Takechi *et al.* evaluated

silicon-on-insulator (SOI) and a-Si models for IGZO TFTs and found IGZO TFTs to be more comparable to SOI than a-Si [112].

Following the arguments of Robertson and Takechi, in our simulations we treated the amorphous oxide channel as a non-defective semiconductor similar to that in SOI devices. This approach allows us to draw physical insights without getting mired in the complexity of the many numerical parameters in a-Si TFT models.

3.4.2 Modeling FETs in Silvaco

We modeled FETs using the Silvaco simulation suite, first constructing the device structure in the ATHENA process simulator and then loading the structure into ATLAS, a 2D device simulator. The simulated top-gate structure is shown in Fig. 3-18. Metal, semiconductor, and insulator thicknesses are defined to match the dimensions of the actual fabricated device, and the channel length is set to L = 100μm. Since ATLAS is a 2-D simulator, it sets the third dimension (W) to 1μm and hence, to compare the simulation results with our data in the following plots, the ATLAS-simulated drain currents are multiplied by 100 to match the actual devices' 100μm channel width.

ATLAS supplies a fixed set of materials for simulation and does not directly support user-defined materials. However, new materials may be defined by overriding the default values for the material parameters of an existing material. By specifying the band gap, dielectric permittivity, carrier mobilities, etc., we re-defined "Si" to match the material parameters of ZIO. Similarly, the dielectric and source/drain electrode materials were redefined to match parylene and ITO, respectively.

Comparing simulation to data

To evaluate how well simulation matches experimental data, the simulated I-V curves are plotted against the measured I-V characteristics. The simulated devices has a channel thickness of 10nm and dielectric thickness of 266nm in order to match the actual device ("MO11U5" in Fig. 3-17). A doping concentration of 10^{17}cm^{-3} was calculated from C-V measurements of a 300μm x 300μm MIS capacitor in the same

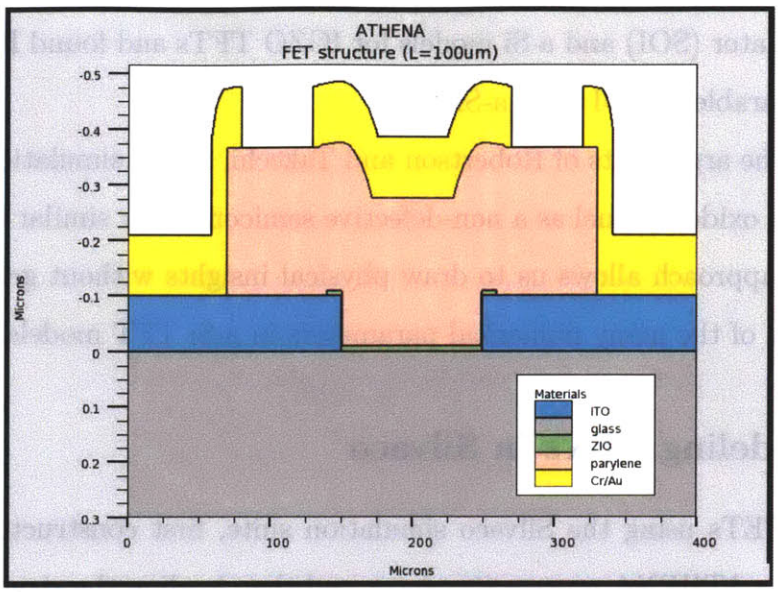

Figure 3-18: Cross-section of the FET device structure constructed in ATHENA and loaded into ATLAS for simulation. Channel length is 100μm, and the metal, semiconductor, and dielectric thicknesses are defined to match the actual device dimensions. (Note that the horizontal dimensions actually much larger than the vertical dimensions; to show more detail, different x- and y-scales were chosen for the above image.)

die. (Details of the doping calculation are given in Appendix B.)

Initially, no interface traps are specified. Fig. 3-20 compares simulated transfer I-V curves (red circles) with the measured I-V curves (green diamonds) from MO11U5 at $V_{DS} = 1V$. The I-V curves are plotted on semi-log scale on the left and linear scale on the right. The discrepancy in threshold voltages is clear from the linear plot. The semi-log plot shows that although V_{off} for both simulation and data is $\sim$ -2V, the simulated curve has much steeper subthreshold slope.

Subthreshold slope is generally degraded by the presence of traps, either in the semiconductor, dielectric, or the interface between the two [26, 101]. Shur and Hack showed that localized states impede carrier transport and reduce the field effect mobility in a-Si [101]. Since not all the induced charge is mobile, the observed drain current is decreased. Interface trapped charges also cause stretch-out in capacitance-voltage curves [26]. Schroder describes a number of methods for measuring trap densities [93].

Given the fact the device has an active organic/inorganic interface, it is reasonable to expect the presence of traps at the semiconductor-dielectric interface. As Fig. 3-19

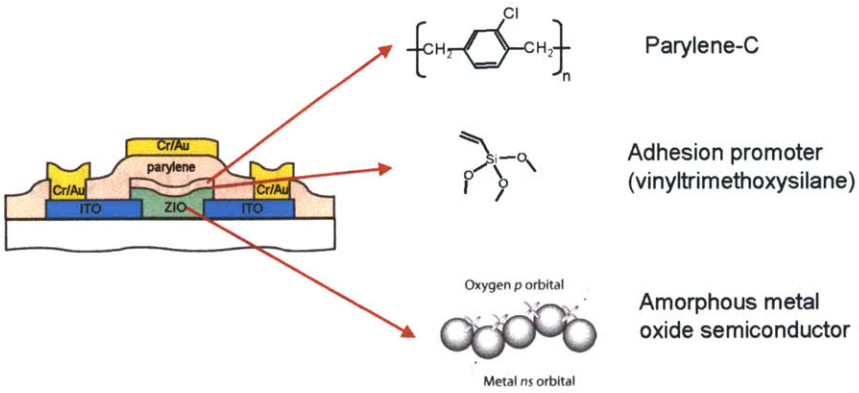

Figure 3-19: Schematic diagram of the various layers at the semiconductor-dielectric interface in a ZIO-parylene FET. Trap states at the interface will affect FET performance.

shows, the carrier channel is formed at an interface between organic and inorganic layers. Although the adhesion promoter molecule sandwiched between should only be a monolayer thick, the process is not perfectly controlled. The parylene dielectric itself might be responsible for charge-trapping, as Ryu suggested for pentacene organic FETs using a parylene dielectric [94].

In addition, dangling ZIO bonds or oxygen vacancies at the interface could also give rise to interface traps. Several researchers have performed calculations that show that oxygen vacancies form states at different energy levels in the band gap [20, 106, 110]. Chen, *et al.* investigated the stress and recovery of positively gate-bias stressed IGZO TFTs and found electron trapping and detrapping energies of 0.38eV and 0.23eV, respectively [113]. We use these values in the simulations below.

Introducing interface traps to simulation

To examine the effect of interface traps on the simulated I-V characteristics, we introduced acceptor-type interface trap levels at different energies below the conduction band energy E_c. Fig. 3-21 plots the simulated transfer curve for an FET with a single interface trap at 0.23eV below E_c with a density of 10^{11}cm^{-2}. The fit is improved compared to Fig. 3-20 but still fails to reproduce the measured I-V data near V_{off}.

Fig. 3-22 plots the effect of a single interface trap at 0.38eV below E_c instead. On a linear scale, both trap levels appear to have a similar effect, but the semi-log plot

shows their different behaviors. For this deeper interface trap, the simulation matches for V_{GS} near V_{off} but fits poorly for V_{GS} near V_T. Clearly, a single interface trap cannot account for the measured I-V data.

The effect of two interface traps, one at 0.23eV and one at 0.38eV, on the transfer characteristic is shown in Fig. 3-23. Measured data is plotted in green (diamonds) and overlaid with the simulated I-V curve in red (circles). The plot shows that simulating with two discrete traps reproduces the measured I-V characteristic fairly well on both linear and semi-log scales. V_{off}, S, and V_T values extracted from the simulated curve match the measured values in Table 3.4.

Applying the same interface trap parameters, we simulated the I-V characteristics for a second data set ("MO11Q2" in Fig. 3-17). Note that calculated mobility is slightly lower for this device, resulting in the slightly lower I_{on} at $V_{GS} = 10V$ shown in the linear plot in Fig. 3-24 (right). The dark and light blue curves (circles) correspond to the measured and simulated I-V curves, respectively, for MO11U5; the dark and light green curves (triangles) correspond to the same for MO11Q2. Although the actual devices likely have a continuous distribution of interface trap states, the discrete two-trap-model again reproduces the transfer characteristic fairly well using the same trap depths and densities. This minimal set of parameters is useful to gain insight to the effect of traps on FET performance.

Model sensitivity

One question to ask is how sensitive the model is to perturbations in trap energy E_t and trap density N_t. We varied the energy levels by $\pm kT = 0.026eV$ and plotted the simulated I-V characteristics together with the measured data in Fig. 3-25. The red (circle) and green (triangle) lines show I-V curves for a simulated device with a set of traps at 0.23eV$\pm$kT and 0.38eV; the orange (rectangle) and blue (circle) lines show I-V curves for a simulated device with traps at 0.23eV and 0.38eV$\pm$kT. All the simulated curves remain close to the actual I-V curves (shown as dark green diamonds).

In contrast, when trap depth varies by more than kT, the resulting I-V curves

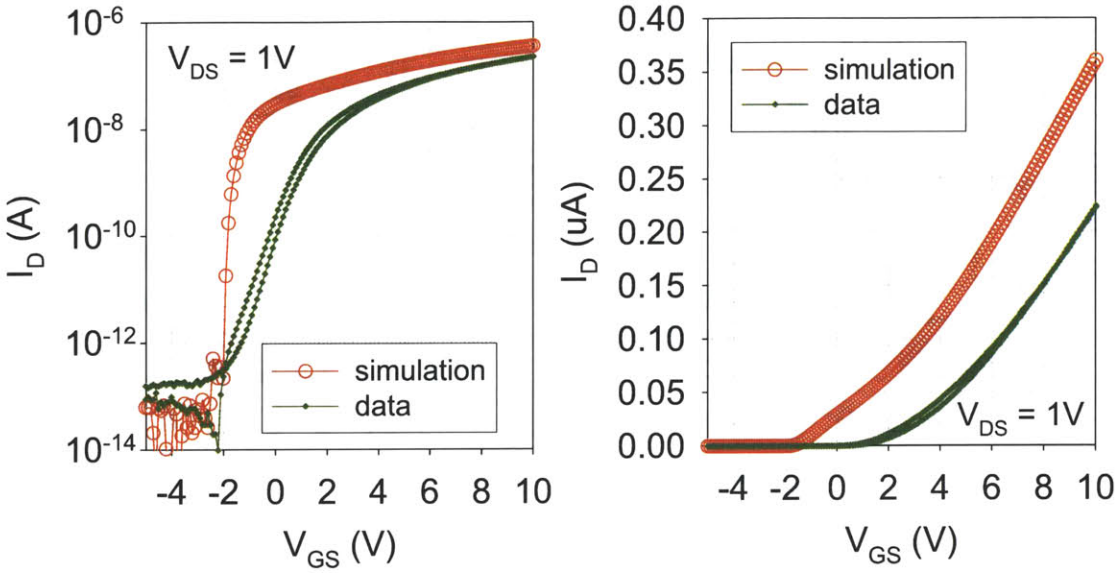

Figure 3-20: Simulated and measured transfer I-V curves at $V_{DS} = 1V$. No interface traps are included in the simulation.

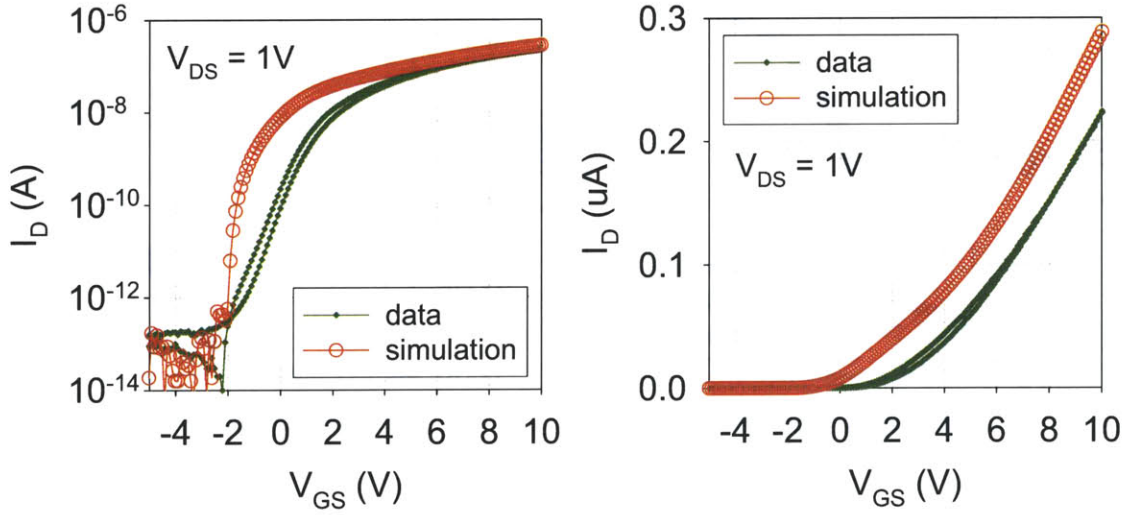

Figure 3-21: Simulated and measured transfer I-V curves at $V_{DS} = 1V$. A single interface trap at 0.23eV below E_c is included in the simulation.

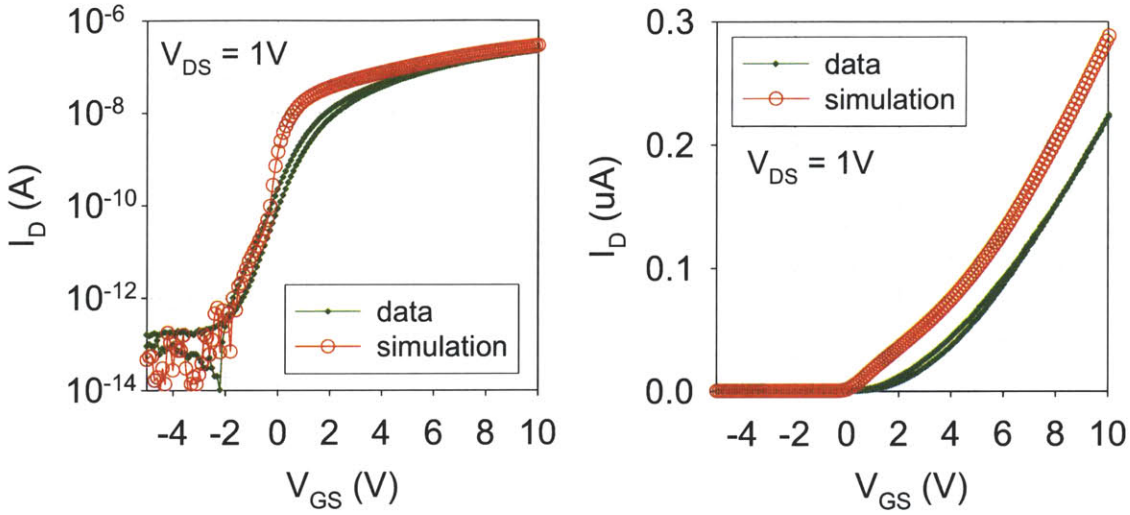

Figure 3-22: Simulated and measured transfer I-V curves at V_{DS} = 1V. A single interface trap at 0.38eV below E_c is included in the simulation.

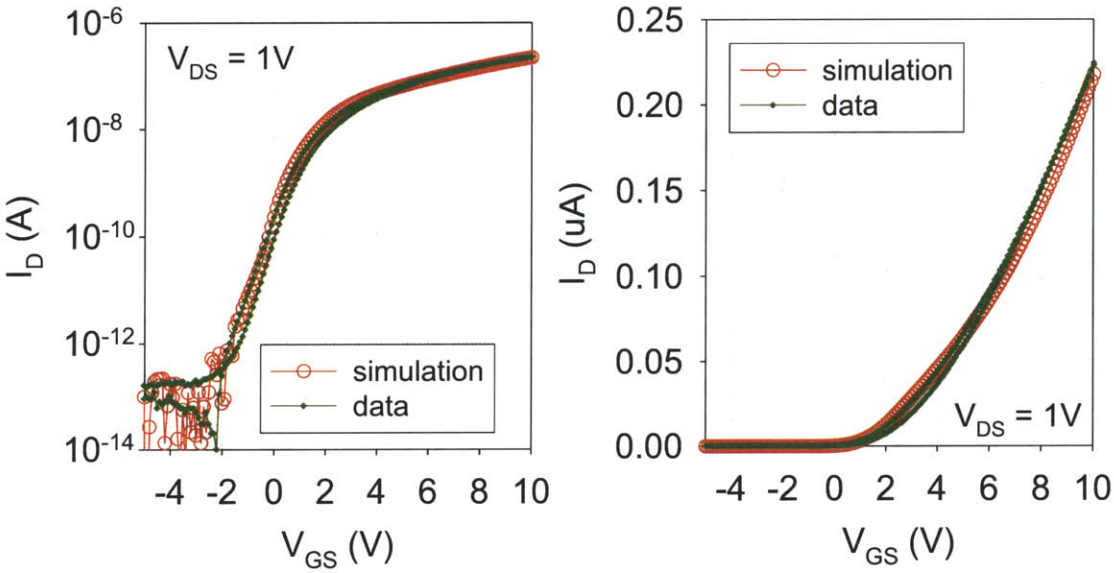

Figure 3-23: Simulated and measured transfer I-V curves at V_{DS} = 1V. Two interface traps at 0.23eV and 0.38eV below E_c are included in the simulation.

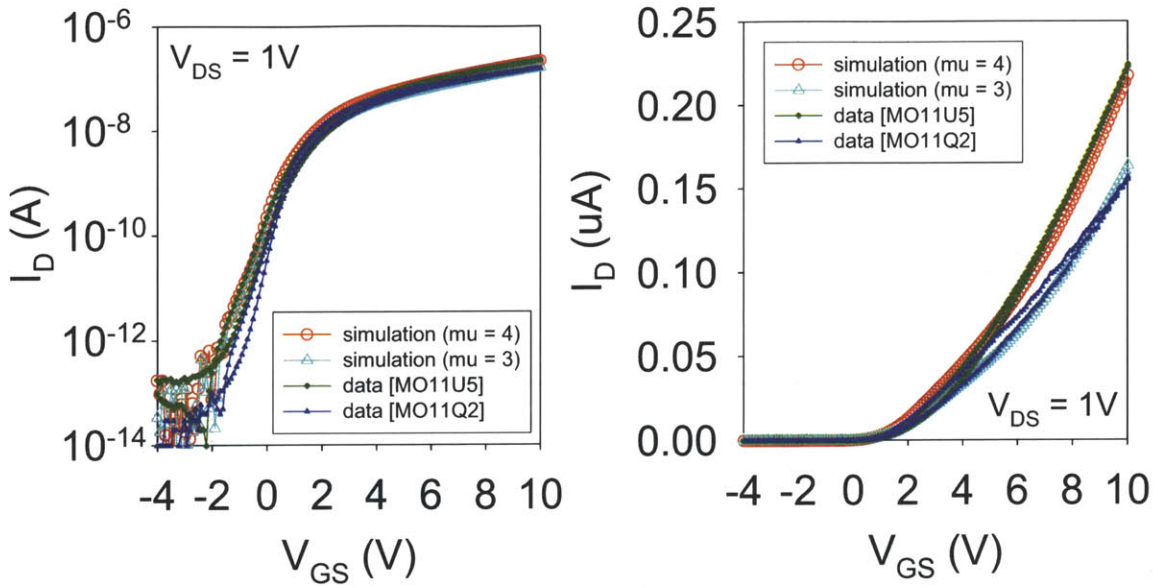

Figure 3-24: Measured I-V characteristics at $V_{DS} = 1V$ from Fig. 3-17(b),(e) are overlaid with simulated I-V curves. The dark and light blue curves (circles) correspond to the measured and simulated I-V curves, respectively, for MO11U5-8B100A; the dark and light green curves (triangles) correspond to the same for MO11Q2-12B100A. Both simulated device curves include the effects of two interface traps at 0.23eV and 0.38eV below E_c and only differ in the mobility values used.

differ noticeably from the measured data. Fig. 3-26 shows the I-V curves for simpled devices with trap depths varied by ±2kT. The pink (circle) and green (triangle) lines plot I-V curves for a device with traps at 0.23eV±2kT and 0.38eV; the orange (rectangle) and cyan (circle) lines plot I-V curves for a device with traps at 0.23eV and 0.38eV±2kT. The poorer fit to the measured data (dark green diamonds) demonstrates the sensitivity of this model to interface trap depth.

Similarly, the simulated I-V curves are sensitive to the density of traps. In the previous simulations, trap density was fixed at $10^{11}cm^{-2}$ for each trap level. In Fig. 3-27 we set the two discrete trap levels to 0.23eV and 0.38eV and varied their densities from $10^{10}cm^{-2}$ to $10^{12}cm^{-2}$. Although V_{off} is barely affected by trap density, the subthreshold slope increases drastically from 0.12V at $N_t = 10^{10}cm^{-2}$ to 2.2V at $N_t = 10^{12}cm^{-2}$.

If we reduce the change in N_t from a factor of 10 to a factor of 2 instead, a comparison of the $5.0x10^{10}cm^{-2}$ (red) and $2.0x10^{11}cm^{-2}$ (blue) curves in Fig. 3-27

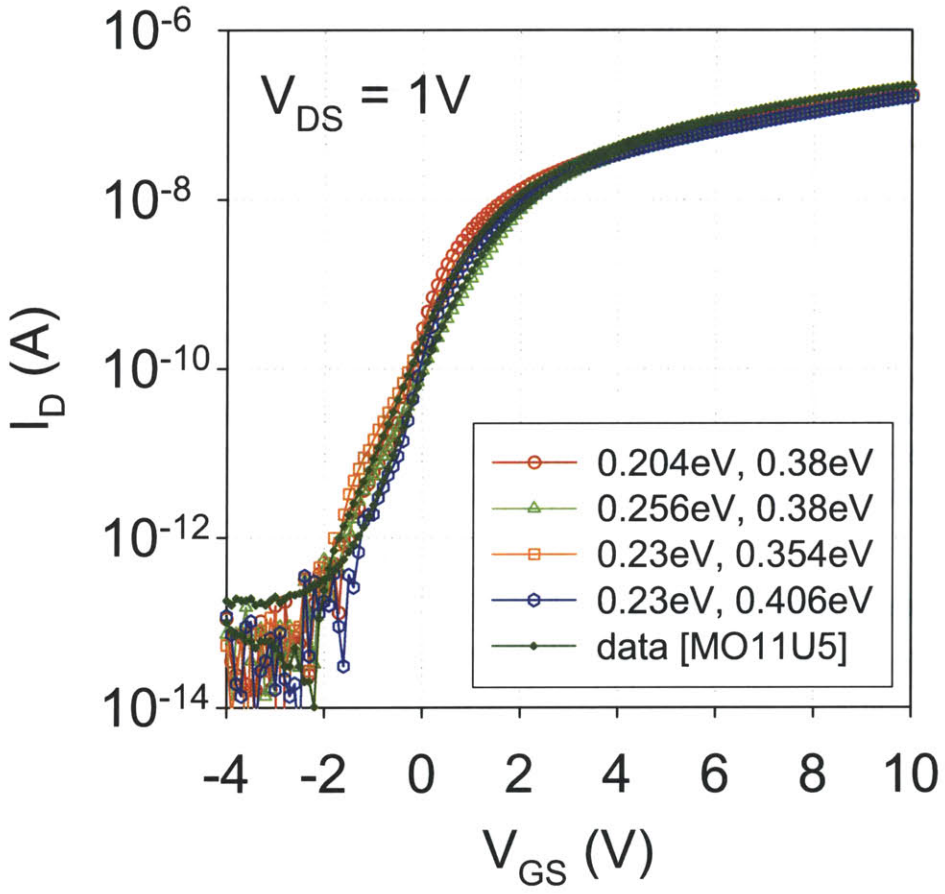

Figure 3-25: Simulated and measured transfer I-V curves at V_{DS} = 1V. The trap depths of the two interface traps previously simulated in Fig. 3-23 are varied by ±kT.

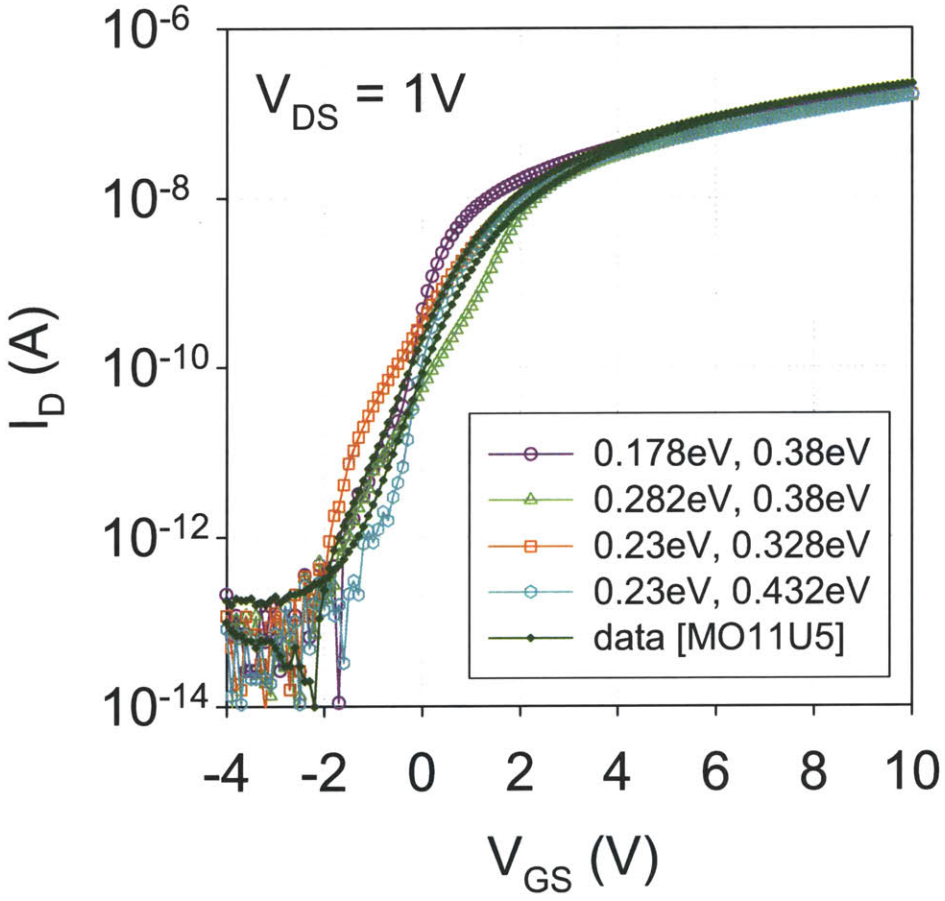

Figure 3-26: Simulated and measured transfer I-V curves at V_{DS} = 1V. The trap depths of the two interface traps previously simulated in Fig. 3-23 are varied by ±2kT.

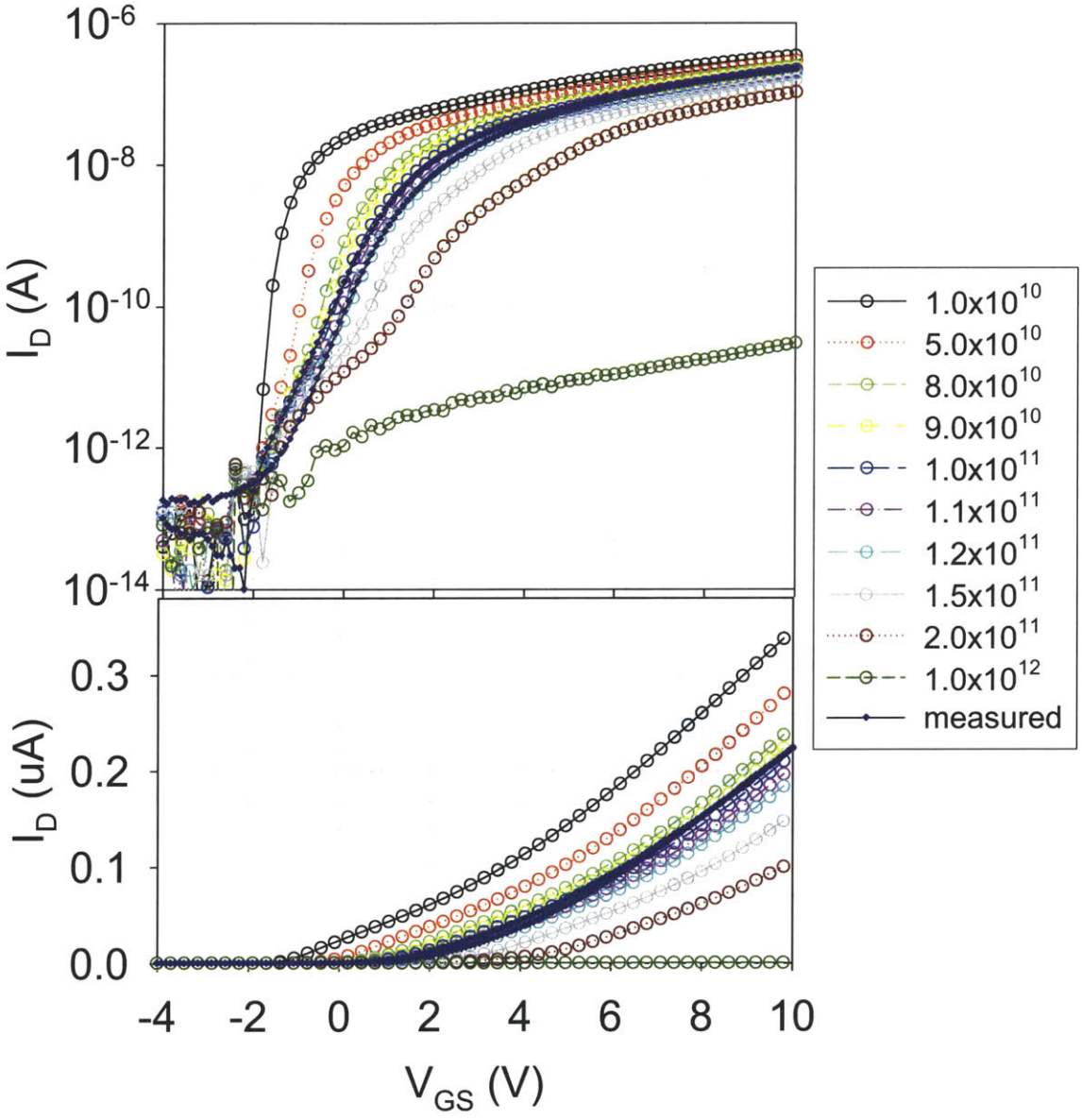

Figure 3-27: Simulated and measured transfer I-V curves at $V_{DS} = 1V$. Trap densities of the two interface traps previously simulated in Fig. 3-23 are varied over two orders of magnitude from $10^{10}cm^{-2}$ to $10^{12}cm^{-2}$.

(top) to the measured I-V characteristic (dark blue) shows that both simulated I-V curves are approximately an order of magnitude off in the subthreshold region. A closer examination of the simulated characteristics plotted in Fig. 3-27 reveals that the measured I-V characteristics are satisfactorily reproduced for trap densities that deviate no more than 10% from $N_t = 10^{11}cm^{-2}$.

3.5 Using simulation to guide device design

In addition to providing insight to the device physics of fabricated devices, simulation is a useful tool for predicting the effects of varying material and process parameters. It can provide a physical understanding for expected trends not always as clear from experimental data alone, especially since such trends may be obscured by wafer-to-wafer variation. These insights help guide our device design.

For the following simulations, we start with the base case plotted in Fig. 3-20 (i.e., no interface traps). Drain current is given in units of A/μm since ATLAS defaults to W = 1μm.

3.5.1 Simulated effects of material-dependent parameters

In the previous section, we simulated a model device with two interface trap levels and investigated its sensitivity to variations in the interface trap energies and densities. To examine the effect of trap depth more generally, we simplified the simulation back to a single interface trap level. Fig. 3-28 plots a series of I-V curves for devices with different interface trap depths ($N_t = 10^{11}cm^{-2}$). A shallow interface trap (E_t = 0.15eV) barely affects the subthreshold region, while a deeper trap (E_t = 0.30eV) severely degrades the subthreshold slope and gives rise to a "hump" in the I-V characteristic. Neither of these traps change the turn-off voltage, but the deepest trap plotted (E_t = 0.60eV) causes a linear shift in the transfer curve, shifting V_{off} without significantly affecting S. Because of their location below the Fermi level, deep traps are likely to be always filled and hence, act as fixed charges.

As previously noted, the carrier concentration in metal oxides can be varied over a wide range by controlling the film stoichiometry. Doping, attributed to the presence of oxygen vacancies and/or metal interstitials, partly determines FET characteristics such as V_{off} and V_T. We simulated two model devices, one with a 10nm-thick channel (Fig. 3-29(a)) and one with a 50nm-thick channel (Fig. 3-29(b)) with different doping concentrations (N_d). For $N_d \leq 10^{16}cm^{-3}$, V_{off} is close to 0V but as doping increases, V_{off} shifts more negative and larger voltage biases are required to deplete the channel. This effect is more noticeable for the thicker film, which has a larger "bulk" to deplete through to completely shut off the channel. For large N_d, the film becomes conductive for all gate biases – a useful property for forming contact electrodes but undesirable for a controllable FET channel.

Both of the properties simulated in this section are difficult to control precisely in our current lithographic process. While we have drawn on the work of others, due to the fact that the material properties adjustable by deposition conditions are often highly dependent on the specific deposition tool and its history, we found it difficult to precisely replicate their results. Since materials optimization is not the focus of this thesis, we chose to simulate instead the effects of easily process-controllable parameters.

3.5.2 Simulated effects of process-controlled parameters

While technically material properties such as oxygen vacancy doping are process-controllable, in this section we refer specifically to device dimensions, i.e. the thicknesses of the dielectric and semiconductor layers. These parameters are more easily manipulated with precision during the deposition process.

Gate dielectric thickness

Fig. 3-30 plots the effect of varying the gate dielectric thickness from 50nm to 300nm for a device with 10nm-thick channel (left) and a 50nm-thick channel (right). Doping is fixed at $10^{17}cm^{-3}$. As expected, the thicker dielectric results in poorer gate control since the effective field in the channel is lower at a given gate bias voltage. Larger

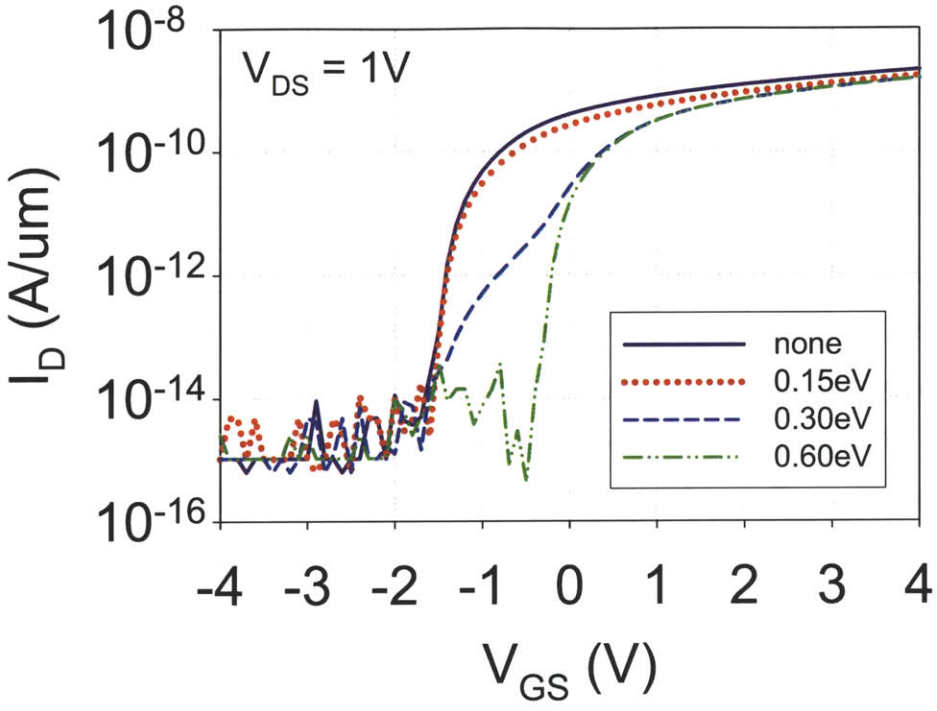

Figure 3-28: Simulated transfer I-V curves at $V_{DS} = 1V$ as a function of trap depth. (For simplicity, only a single interface trap level is simulated.)

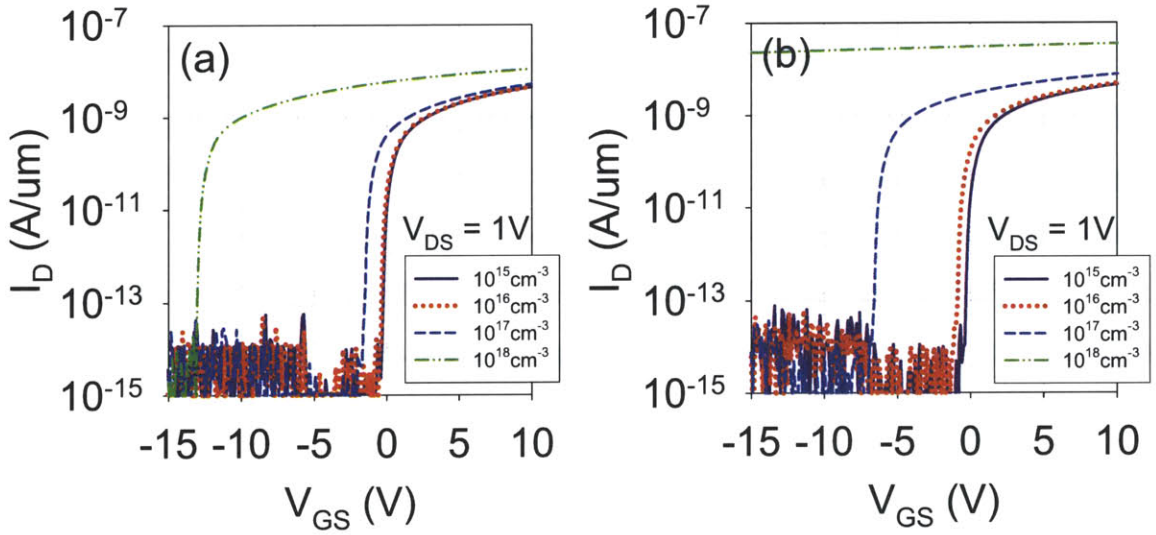

Figure 3-29: Simulated transfer I-V curves at $V_{DS} = 1V$ for (a) 10nm-thick channel and (b) 50nm-thick channel FETs. As doping level increases the device is more difficult to turn off, i.e., V_{off} shifts more negative. The effect is more pronounced for the 50nm device since it has a larger "bulk" to deplete through in order to turn off the channel.

gate biases are required to turn off the device (i.e., V_{off} becomes more negative), and I_{on} is lower at the same V_{GS}. This effect is more obvious for the thicker channel device. In both cases, threshold voltage approaches $V_{GS} = 0V$ and I_{on} increases as the dielectric thickness decreases which suggests that the parylene layer should be thinned to a minimum.

Though an arbitrarily thin dielectric layer is feasible in simulation, in reality parylene layers less than 100nm-thick suffer from high leakage currents. The Au top electrodes can penetrate into the insulator and cause shorting when bias is applied. To overcome this limitation we could switch to a different material that can be thinned further without suffering from high leakage currents; switch to a higher dielectric constant material to retain the same thickness while increasing the effective field in the channel; or otherwise modify the dielectric to an optimized stack of materials. The basic idea is the same in any case.

Channel thickness

The 50nm-thick channel device plotted in Fig. 3-30 (right) has a more negative V_{off} than the 10nm-thick device (left) at the same dielectric thickness. To further explore the effect of varying channel thickness, we simulated devices with a 200nm-thick dielectric, $N_d = 10^{17}cm^{-3}$, and channel thicknesses ranging from 10nm to 120nm. Fig. 3-31 shows that the I-V curves shift in a parallel manner without significant change to the subthreshold slope, similar to the results presented by Takechi, *et al.* [112]. Park, *et al.* also showed that threshold voltage could be modulated by adjusting the channel thickness without significantly affecting channel mobility or subthreshold slope [114]. To obtain $V_T \sim 0V$, the simulation results in Fig. 3-31 suggest thinning down the channel as much as possible.

One caveat is that since mobility is specified at a fixed value, the present simulation does not capture the possibility of degraded mobilities for very thin channels due to interface roughness. Oh, *et al.* found that their thinnest ZnO-channel FETs did not turn on, likely because of high resistivity due to small grain sizes [115]. While grain size is not measurable for amorphous oxides, bulk measurement techniques like x-ray

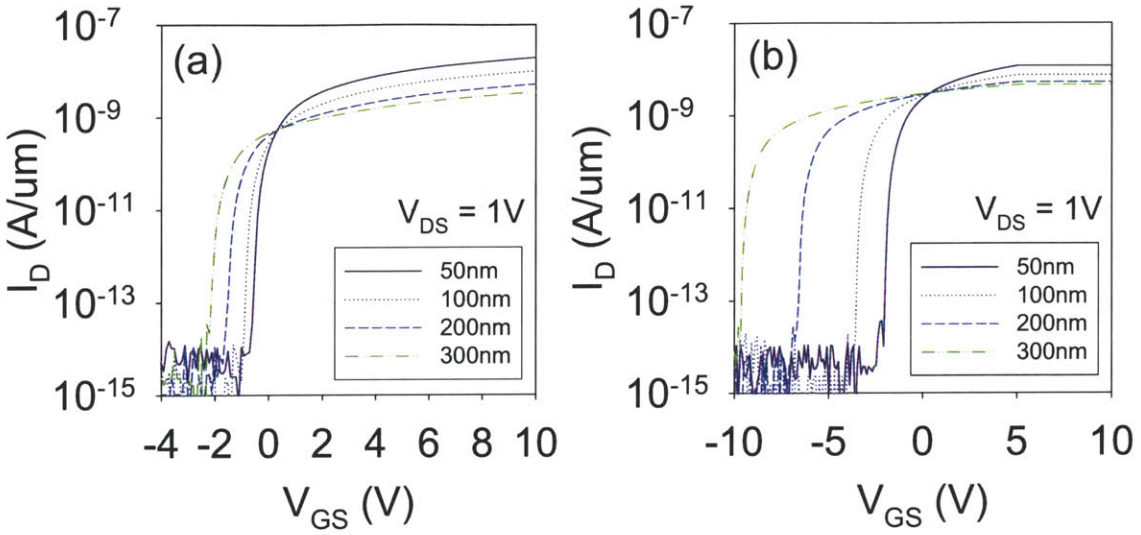

Figure 3-30: Simulated transfer I-V curves as a function of gate dielectric thickness for (a) 10nm-thick channel and (b) 50-nm thick channel FETs. Four gate dielectric thicknesses are simulated: 50nm, 100nm, 200nm, and 300nm. (V_{DS} = 1V.) The turn-off voltage V_{off} shifts more negative as gate dielectric thickness increases; the effect is more pronounced for the thicker channel device.

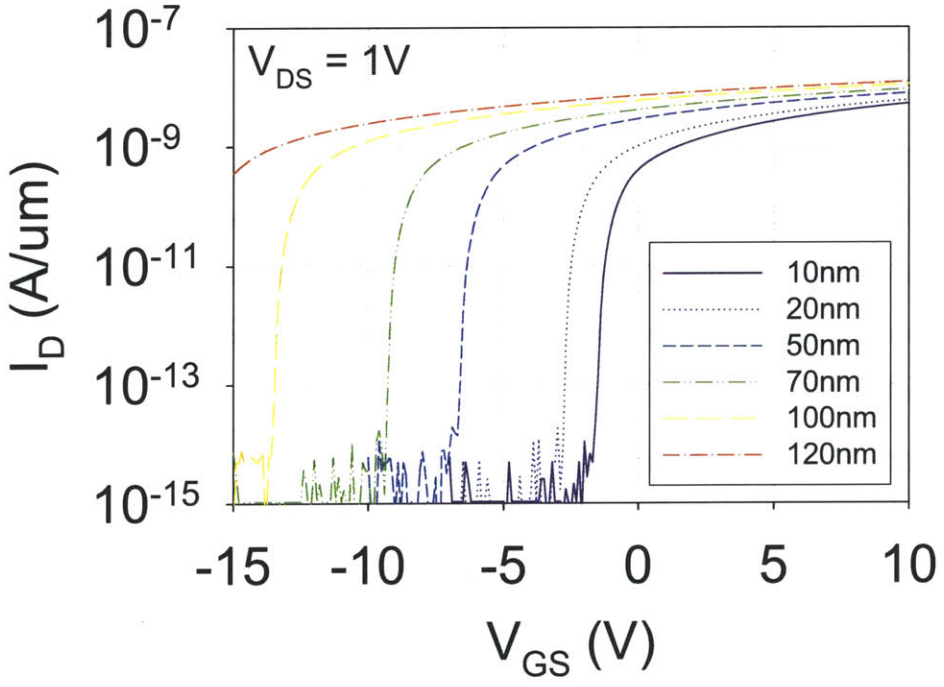

Figure 3-31: Simulated transfer I-V curves at V_{DS} = 1V for six different semiconductor channel thicknesses from 10nm to 120nm. Increasing channel thickness results in a parallel shift of the I-V curves without a change in subthreshold slope.

diffraction (XRD) cannot capture very short-range ordering that may change in the absence of discernible structure changes. In addition, very thin film depositions may result in an incomplete channel layer.

In general, enhancement mode devices ($V_T \geq 0V$) are preferable since the transistor is in the off-state when no bias is applied. A depletion mode transistor ($V_T < 0V$) is always on at $V_{GS} = 0V$ and hence dissipates power for zero gate bias. Most oxide FET circuits reported in the literature are designed to accommodate the constraints of using only enhancement mode (or only depletion mode) transistors with uniform threshold voltage. As will be described in Chapter 4, however, the availability of FETs of different V_Ts is useful for improving circuit designs. The simulations in Fig. 3-31 suggest a straightforward way to obtain FETs with different threshold voltages.

3.6 Simulation to experiment: channel thickness

Based on the simulation results in the previous section, we expect V_T and V_{off} to shift negative and I_{on} to increase with increasing channel thickness. As previously noted, this offers a possible method for producing FETs with different theshold voltages. To verify the simulated trend, we fabricated and characterized ZIO FETs with different channel thicknesses.

Fig. 3-32 offers a simple physical picture of the effect of a thicker channel layer. For a thin channel layer, the total drain current is dominated by carriers in the accumulation channel at the semiconductor-dielectric interface. As the channel thickness increases, the undepleted "bulk" contributes additional mobile carriers to the overall drain current. In addition, the thicker the semiconductor layer is the lower the gate bias at which the channel comes out of depletion, pushing the turn-off voltage more negative.

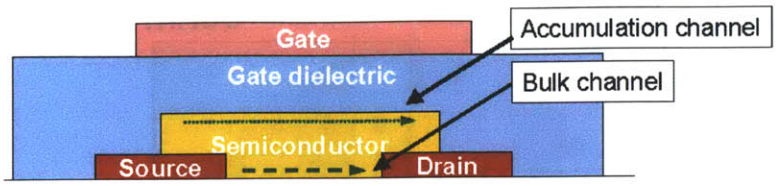

Figure 3-32: Schematic cross-section of possible conduction paths through a thin-film transistor. In this simple physical picture, the total drain current is dominated by carriers accumulated at the semiconductor-dielectric interface for a thin channel layer, with increasing contributions from a "bulk" back channel as channel thickness increases.

3.6.1 Partially shadow masked fabrication process

To avoid issues from water-to-wafer variation, FETs with different channel thickness were fabricated all on the same 100mm borosilicate glass wafer. The fabrication process was almost identical to the baseline process described in Section 2.5 except for a modification during the ZIO deposition step. A simple rectangular mask was employed to cover half the wafer during sputter deposition of a 10nm-thick ZIO layer. The deposition was then paused to rotate the mask before sputtering another 40nm of ZIO. Because the cluster tool in ONELab allows in-situ mask changes, the entire deposition was performed without breaking vacuum. The partial masking generates a wafer with 4 quadrants, as shown in Fig. 3-33.

Following the ZIO deposition, the FETs were completed following the baseline lithographic process to form 10nm-, 40nm-, and 50nm-thick ZIO FETs on a single substrate. The total parylene gate dielectric thickness was 280nm.

3.6.2 Device characterization

Output I-V characteristics for (a) 10nm-thick channel, (b) 40nm-thick channel, and (c) 50nm-thick ZIO channel FETs are compared in Fig. 3-34. For each device, V_{DS} was swept from 0V to 10V and V_{GS} was stepped in 2V increments from 0V to 10V. Since all devices are sized the same (W/L = 100μm/100μm), the plot clearly shows that I_D increases with channel thickness. While an improvement in I_{on} at any given bias could be explained by higher carrier mobility, the main contributor is a shift in V_T. In Fig. 3-34(c) the output curve for the 50nm-thick channel at $V_{GS} = 0$V is visibly

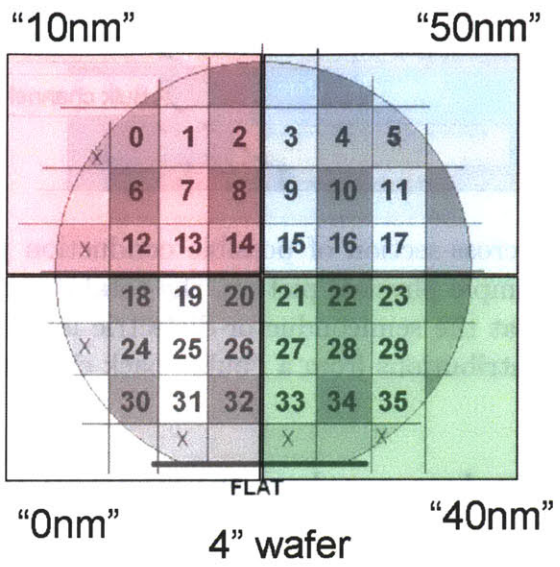

Figure 3-33: Multiple semiconductor channel thicknesses were deposited on a single wafer by a simple shadow masking technique. By masking off half the wafer and rotating the half-wafer mask 90° partway during deposition, different thickness ZIO layers are deposited in each of the four quadrants.

greater than 0μA indicating that $V_T < 0$V. Hence, a gate bias of 10V corresponds to a larger overdrive (V_{GS} - V_T) for the thicker channel device and higher drain current is expected.

The shift in V_T is clear from transfer I-V characteristics. Fig. 3-35 plots the corresponding transfer curves at V_{DS} = 1V on (a) linear scale and (b) log scale. Similarly, saturation transfer I-V curves are shown in Fig. 3-36. The double-swept curves from V_{GS} = -10V to +10V show minimal hysteresis, and low gate leakage currents of <1pA contribute to high on/off ratios $>10^7$. The key feature to note is the shift in V_{off} and V_T with channel thickness: V_{off} shifts from -2V to -4V to -7V for the 10nm, 40nm, and 50nm devices, respectively. Similarly, V_T shifts from 1.1V to 0.7V to -3.4V. As predicted from simulation, they become more negative for increasing channel thickness.

While the trend is correct, the experimental results do not perfectly match the simulation. The ideal ATLAS-generated I-V curves in Fig. 3-30 assumed a constant mobility and the absence of any traps. The experimental data in Fig. 3-36 show not only that subthreshold slope deviates from the ideal case but also that it increases,

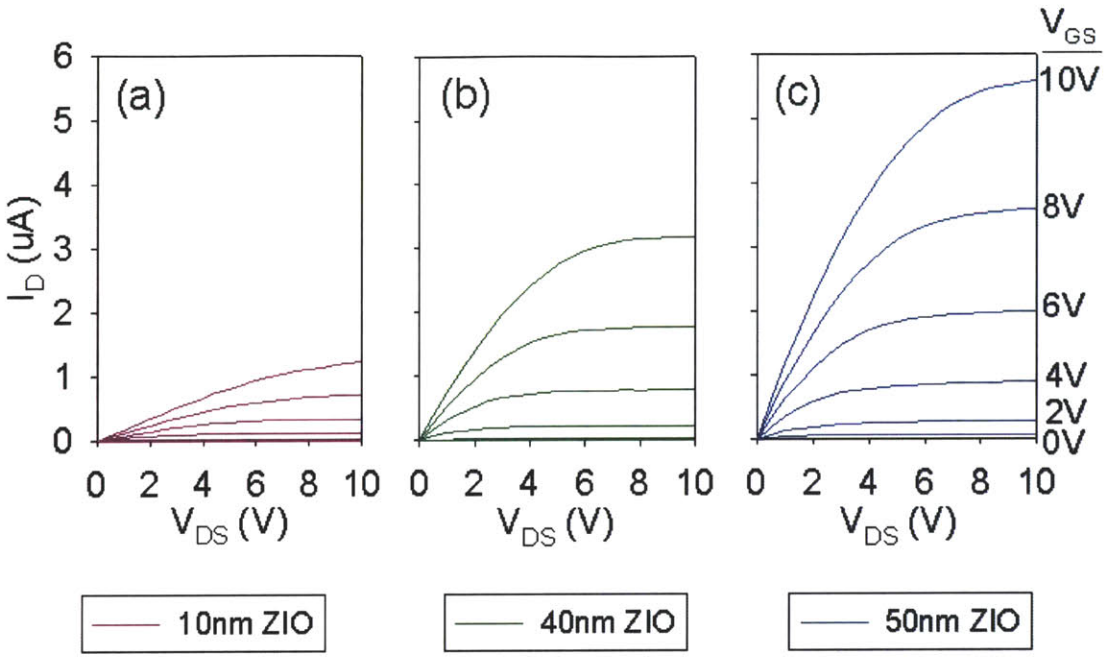

Figure 3-34: Output I-V characteristics for (a) 10nm- (b) 40nm- and (c) 50nm-thick ZIO channel FETs. For each device, W/L = 100μm/100μm. As channel thickness increases, V_T shifts negative and I_D increases since the overdrive (V_{GS} - V_T) is larger for a given gate bias.

from 0.6V/dec for the 10nm device to 1.0V/dec for the 40nm and 50nm devices. Also, while I_D in the 10nm device is linear for $V_{GS} > 0$V, the 40nm and 50nm devices show a break in slope at 4V and 3.5V, respectively. This change in slope points to a change in carrier mobility, which increases from 1.4 $cm^2V^{-1}s^{-1}$ for the 10nm device to 5.5-7.0 $cm^2V^{-1}s^{-1}$ at V_{GS} = 10V for the thicker channels. We speculate that mobility in the thin channel device is dominated by carriers hindered by defects at the semiconductor-dielectric interface, whereas the higher mobility in the thicker semiconductor films is partly due to carriers located in the undepleted back channel.

Nevertheless, we have successfully demonstrated the ability to fabricate ZIO FETs with different threshold voltages on the same substrate simply by modifying the channel thickness. This capability will be further developed in Chapter 4 and exploited for the design of FET circuits.

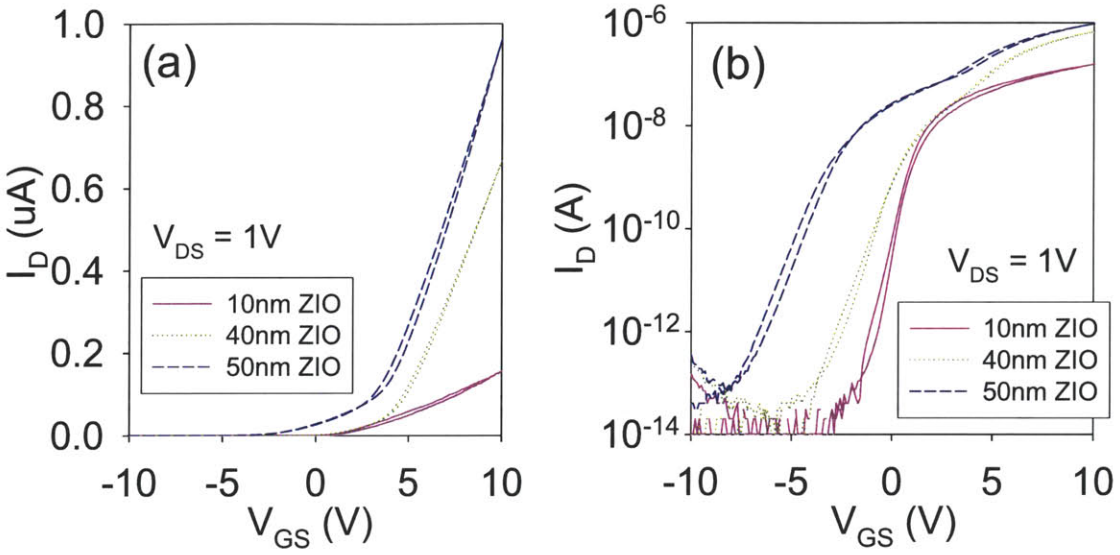

Figure 3-35: Transfer current-voltage characteristics for FETs with different ZIO channel thicknesses at V_{DS} = 1V on linear scale (left) and log scale (right). The thicker channel layers result in an undepleted back channel that affects FET mobility, subthreshold slope, and threshold voltage.

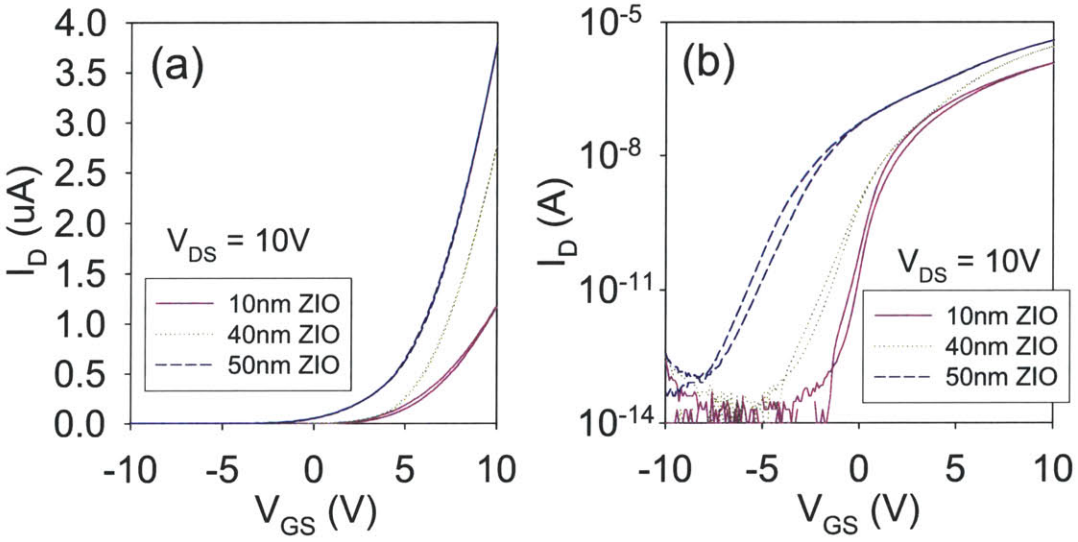

Figure 3-36: Saturation region transfer current-voltage characteristics for FETs with different ZIO channel thicknesses at V_{DS} = 10V on linear scale (left) and log scale (right). Turn-off voltage becomes more negative and subthreshold slope increases with channel thickness.

Chapter 4

Applications to circuits

Thus far, we have focused on the fabrication and characterization of individual FETs. With the insights gained for FET device design and operation, we can now use the metal oxide FET as a building block for circuits. In this chapter, we begin by describing the most basic digital circuit, the inverter, and several ways that it can be implemented: CMOS, enhancement-enhancement, or enhancement-depletion (Section 4.1). To enable the fabrication of enhancement-depletion logic using metal oxide FETs, a modified version of the lithographic process from Chapter 2 was developed to integrate FETs with different threshold voltages (Section 4.2). Using this modified process, we then demonstrate low temperature-processed enhancement-depletion inverters and ring oscillators in Sections 4.3 and 4.4.

4.1 Background

4.1.1 Inverter characteristics

Despite its simplicity, the inverter is a fundamental building block for more complex logic circuits. The logic function of an inverter is to take a voltage input V_{in} and invert the signal to an output voltage V_{out}. The switching point of the inverter, V_m, is defined as the point at which $V_{in} = V_{out}$. Roughly speaking, when V_{in} is greater than the switching voltage V_m (i.e., V_{in} is "high," or a positive logic value of "1"),

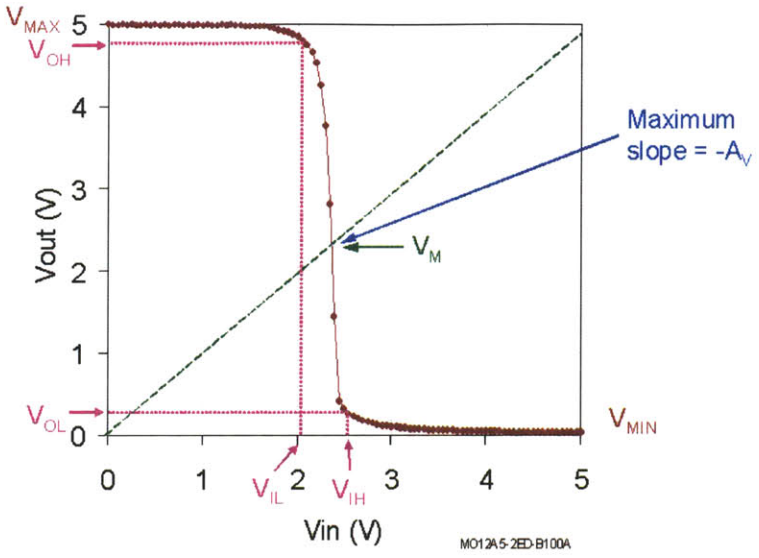

Figure 4-1: Example inverter transfer characteristic with key voltage parameters defined. The supply voltage, V_{DD}, is 5V. [98]

V_{out} will be "low," or a positive logic value of "0." Conversely, when V_{in} is "0," V_{out} will be "1." The inverter "high" and "low" voltage levels are defined below.

Inverter performance can be quantified by the parameters pointed out on the example DC inverter transfer function plotted in Fig. 4-1. When V_{in} is at 0V, V_{out} = V_{max}, or the maximum output voltage. When V_{in} is at V_{DD}, V_{out} = V_{min}, or the minimum output voltage. For a full-swing inverter, V_{max} = V_{DD} and V_{min} = 0V.

The input high voltage, V_{IH}, is the minimum input voltage required to output a logic "0." The input low voltage, V_{IL}, is the maximum input voltage for the inverter to output a logic "1." These voltages are defined at the points where the slope of the transfer function = -1V/V. At the points on the transfer curve where the magnitude of the slope is greater than 1, the inverter will begin to switch; the maximum slope, A_V, is considered the inverter gain.

In a paper on defining noise margins for digital logic circuits, Hauser notes that output logic high (V_{OH}) and output low (V_{OL}) values are defined slightly differently by different textbook authors [116]. One typical method uses a bistable inverter pair to define V_{OH} and V_{OL} (or V_{HI} and V_{LO}, respectively), as in [117]. The high

and low voltages can be found graphically by plotting the transfer function and its mirror (i.e. with input and output axes switched) to determine the intersection points, which represent the stable states of a cross-coupled inverter pair or an infinite chain of inverters. The other method uses the -1 slope points on the transfer function to define V_{OH} and V_{OL}, as in [98]. V_{OH} is then the minimum output voltage that can be interpreted as a logic "1" (e.g., as an input to a second inverter), and V_{OL} is the maximum output voltage that can be interpreted as a logic "0." We follow this latter approach in this work.

The output/input high/low voltages (V_{OH}, V_{OL}, V_{IH}, V_{IL}) determine the noise margins, or how far an input voltage may deviate from a "high" or "low" signal and still result in the correct logical "0" or "1" output. The noise margin high (NM_H) and noise margin low (NM_L) can be defined as follows [98]:

$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

In an ideal inverter, the inverter gain $A_V = \infty$, $V_m = V_{DD}/2$, and the noise margins on each side = $V_{DD}/2$.

Fig. 4-2 shows a basic design for an inverter with an n-channel FET driver, or pull-down, and an unspecified load, or pull-up; the inverter is connected to a load capacitance C_L. When the input voltage is high, the driver FET turns on to discharge C_L and pull the output voltage low. When the input voltage is low, the driver FET turns off and the load sources current to charge up C_L and pull up the output voltage.

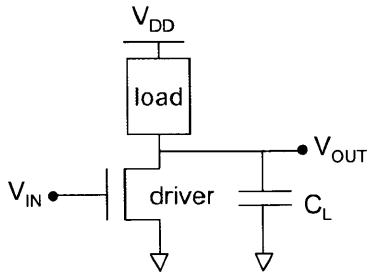

Figure 4-2: Schematic for an inverter

The inverter load can be implemented in a number of ways. A resistor R can be used as the load, but increasing inverter gain requires a larger R which degrades the transient response. A better solution is to use a current source pull-up, which can be implemented using another FET. Three possible configurations for inverters with FET loads are shown in Fig. 4-3. We discuss the advantages and disadvantages of each of these implementations below.

4.1.2 Complementary logic

Fig. 4-3(a) shows the circuit schematic for a CMOS inverter. Silicon complementary metal-oxide-semiconductor (CMOS) is the predominant technology in digital integrated circuits because of its low static power dissipation and high noise immunity. CMOS architectures require both p-channel and n-channel devices. When the input voltage is applied to both the gates of the p- and n-channel devices, the different threshold voltages mean that only one transistor will turn on, thereby pulling the output high (pFET on) or low (nFET on). Hence, power is only dissipated during switching.

Several research groups have published complementary ZnO-based inverter circuits using organic FETs as the p-FET load [118–120]. These are hybrid oxide-organic semiconductor implementations because of the difficulty in producing stable p-type oxide semiconductors, particularly those based on ZnO [20, 121, 122]. On the other hand, most organic semiconductors are be p-type materials. Combining oxide and organic semiconductors, Oh, *et al.* demonstrated a shadow mask-patterned ZnO-pentacene hybrid complementary inverter with maximum gain of 100 at a V_{DD} of 7V [123]; the supply voltage could be reduced as low as $V_{DD} = 2V$ and still yield inverting behavior. The average gate delay of these hybrid inverters was relatively long at ~20ms.

Despite their excellent gain and noise margins, the disadvantage of hybrid complementary inverters is the need for two different materials to form the p-channel and n-channel transistors. Pentacene, one of the best-performing organic semiconductors, has been reported with mobilities as high as 1-2 cm^2/Vs [124, 125], but typical values

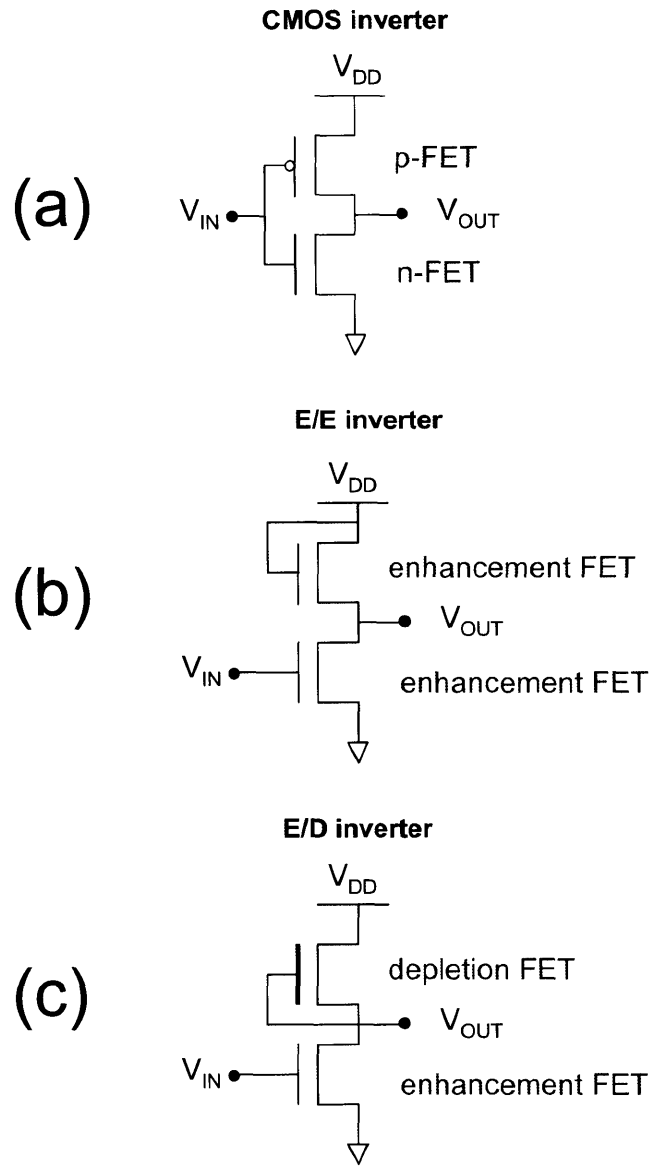

Figure 4-3: Circuit schematics for 3 types of inverters: (a) CMOS inverter with n-channel driver and p-channel load; (b) n-channel enhancement/enhancement inverter with diode-connected load; (c) n-channel enhancement/depletion inverter with depletion-mode load.

are an order of magnitude or two lower. This is far lower than possible in ZnO-based semiconductors, which holds back the potential maximum currents and speed performance for oxide-organic hybrid inverters. The mobility mismatch requires that the organic p-channel FET be sized much wider, increasing total device area and load capacitance. In addition, the integration of two types of materials requires careful consideration for process compatibility. The shadow mask-patterning approach utilized by Oh, *et al.* is not easily scalable to more complex circuits, unlike the lithographic processes demonstrated for oxide FETs.

4.1.3 Unipolar n-channel logic

If we are constrained to n-channel devices only, a current source pull-up can be implemented using an n-channel FET with its gate tied to a fixed bias voltage V_B, as shown in Fig. 4-4. Circuits composed of FETs with $V_T > 0$ are referred to as enhancement/enhancement (E/E) logic; conversely, circuits composed of FETs with $V_T < 0$ are referred to as depletion/depletion (D/D) logic.

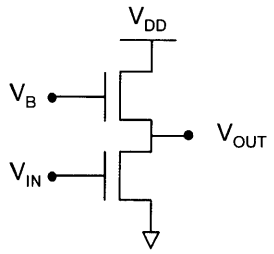

Figure 4-4: Circuit schematic for E/E inverter with separate load bias voltage, V_B.

Fig. 4-3(b) shows the circuit schematic for an inverter where both driver and load are n-channel FETs with the same threshold voltage. In this case, the top FET has its gate tied to V_{DD}, forming a diode-connected load. The diode-connected FET acts as a current source pull-up with small signal output resistance $\sim 1/g_m$, where the transconductance $g_m = \Delta I_D/\Delta V_{GS}$. For this configuration, inverter gain depends on

the relative transconductances g_m of the driver and load FETs [126]:

$$A_V = -g_{m,driver} \times \left[\frac{1}{g_{m,load}} \,||\, r_{o,driver} \right] \Bigg|_{V_M} \tag{4.1}$$

$$\approx - \frac{g_{m,driver}}{g_{m,load}} \Bigg|_{V_M} \tag{4.2}$$

Typically, the driver FET is sized larger than the load FET to obtain $|A_V| > 1$; the ratio between the two is referred to as the geometrical factor β, where $\beta = \left(\frac{W}{L}\right)_{drive} / \left(\frac{W}{L}\right)_{load}$. At first glance, one might choose to make β very large in order to increase A_V and improve noise margins. However, because increasing β also shifts V_M towards V_{DD}, the circuit designer must trade off inverter gain and noise margins when choosing β.

Several research groups have demonstrated n-channel-only oxide FET logic circuits [21,127–130]. Ofuji, *et al.* demonstrated an IGZO inverter designed with W_{drive}/W_{load} = 100μm/40μm that operated at V_{DD} = 18V with a gain of 1.7 [127]. Since they set $V_B = V_{DD}$, their E/E inverter essentially had a diode-connected load. In contrast, the ZnO FET reported by Sun, *et al.* used two power supplies to bias the inverter (V_{DD} = 10V, V_B = 15V) [128]. With a larger β (β=30) they obtained a slightly higher gain of ~5, though unlike the inverter in [127] in this case $V_{OH} < V_{DD}$ by several volts. In both cases, the DC transfer characteristics show that the inverters fully switch from 'high' (V_{OH}) to 'low' (V_{OL}) when the input voltage is swept from 0V to V_{DD}, but the low gains resulted in poor noise margins.

An additional complication arises for D/D inverters, which require input voltages $V_{in} < 0$V to reach the maximum 'high' output voltage level, V_{OH}. Hence, the addition of level shifters are required to use the output from one inverter as an input to the next stage. Hirouchi, *et al.* demonstrated a four-FET circuit that combines an inverter with level shifter [129]. In addition to increasing the number of devices needed, this configuration also necessitates the use of two supply voltages, V_{DD} and V_{SS} = -V_{DD}, plus the fixed voltage bias V_B. Like the previous examples, the inverter transfer characteristic shows that gain is low (1.8) and the output is not rail-to-rail, i.e. it does not sweep from V_{DD} to 0V.

4.1.4 Approaches to improving unipolar n-channel logic

The inverters in the previous section comprised transistors with identical device characteristics and only the device geometry (W, L) modified to change FET transconductance. Improvement of n-channel FET logic circuits is possible by differentiating the performance (i.e., output drive currents) of the load and driver transistors. Drain current is a function not only of device geometry (W/L) but also carrier mobility, dielectric capacitance, and threshold voltage. In this subsection we describe several approaches in the literature for improving unipolar n-channel inverters.

For the inverters cited below, the current source pull-up is implemented by tying the gate of the load FET to its source, rather than to a fixed bias as before. A representative circuit diagram with $V_{GS,load}$ = 0V is shown in Fig. 4-3(c). This topology offers a current source load with higher output resistance. (It is not generally used if limited to transistors with identical device characteristics, since it would require a prohibitively large load device to obtain a functional inverter.)

Mobility

Instead of increasing W/L, performance can be improved by designing a load FET with higher mobility than the driver FET. Oh, *et al.* found that shadow mask-patterned bottom-gate and top-gate ZnO FETs with the same W/L ratio had similar V_T and S but mobilities that differed by more than an order of magnitude [131]. They attributed the higher mobility in bottom-gate FETs to decreased surface roughness. Connecting a bottom-gate FET (load) and top-gate FET (driver) to form an inverter, they obtained a rail-to-rail transfer characteristic with A_V = -41 at V_{DD} = 5V.

Given that ZnO tends to form polycrystalline thin films, increased surface roughness in the top-gate FETs could be caused by grain growth during the 200°C ALD dielectric deposition. Since the mixed oxides have been shown to remain amorphous even for fairly high process temperatures, this strategy for modifying mobility may not be as effective for the amorphous oxide semiconductors.

Doping and stoichiometry

Another approach to improving performance involves modifying semiconductor carrier concentrations to form both enhancement- and depletion-mode FETs. Since at V_{GS} = 0V the channel is always on, depletion mode FETs offer better performance as current source loads in the circuit shown in Fig. 4-3(c). Heineck, *et al.* demonstrated a lithographically-patterned enhancement-depletion (E/D) inverter with a gain of $|A_V| > 10$ at V_{DD} = 10V [132]. Using a single channel material for the bottom-gate FETs, E- and D-mode FETs were fabricated by altering the oxygen vacancy doping levels. The first zinc tin oxide (ZTO) channel layer was sputtered in 10% O_2 ambient to form the active layer for enhancement mode driver FETs. The depletion mode load FETs were completed by sputtering a second ZTO channel layer over the first layer in an Ar-only ambient. The decrease in oxygen partial pressure results in higher carrier concentrations in the load FETs and shifts V_T negative without affecting mobility and S significantly. This approach requires strict control over oxygen vacancies in the device, which are affected by the sputtering ambient as well as post-deposition processes such as annealing.

Similarly, Yin *et al.* produced an E/D inverter by integrating single channel layer E-mode FETs and bi-layer channel D-mode FETs [133]. Instead of modifying oxygen partial pressure, they utilized two different channel film compositions, IZO/GIZO and GIZO. The higher carrier concentrations in the IZO/GIZO channel resulted in D-mode operation while the GIZO channel operates in E-mode. The reported inverter operated at V_{DD} = 5V with $|A_V| > 15$. Although this strategy (modifying film composition versus oxygen partial pressure) is probably less sensitive to processing conditions, it does add complexity by requiring two semiconductors instead of one.

Threshold voltage

Both of the above approaches can also be considered methods to adjust the threshold voltage. The availability of FETs with different threshold voltages allows the design of enhancement-depletion logic circuits with faster speeds and smaller device areas. As previously noted, a load FET with a depletion-mode threshold voltage (i.e., $V_{T,load} < V_{T,driver}$) can source more current than an enhancement-mode FET of the

same width at $V_{GS} = 0V$.

Besides doping and film stoichiometry, other methods for modifying V_T have also been explored. Park and Im fabricated a dual gate ZnO TFT whose V_T could be controlled from 0.5V to 2.0V by applying a bias to the back-gate [134]. While this technique allows V_T shifting, the need for an additional power supply for the back-gate voltage bias is undesirable for circuits. In contrast, Nausieda, *et al.* utilized two gate metals with different workfunctions to fabricate pentacene transistors with different threshold voltages [135]. While they successfully demonstrated improved circuits using the dual-V_T transistors, this technique for shifting V_T is limited by the available gate metals and sensitive to issues such as oxidation of the gate metal interfaces.

Though most studies of the effect of channel thickness on V_T focus on bringing V_T as close to 0V as possible, in fact channel thickness can be engineered to produce FETs with different V_Ts. Lee, *et al.* demonstrated a full-swing E/D inverter using 200nm-thick and 20nm-thick IGZO channels for the load and driver FETs, respectively [136]. At $V_{DD} = 20V$, the inverter achieved a high gain of $|A_V| > 37$ and nearly equal noise margins. These results significantly outperform all previously cited single-V_T inverters.

Approach pursued

While the reported inverter was fabricated using shadow mask-patterned IGZO FETs on thermally-oxidized silicon wafers, the channel thickness-V_T approach can be applied more generally. In Chapter 3.6 we fabricated and characterized FETs of different channel thicknesses and hence, threshold voltages. Exploiting the differences in V_T, two FETs on the previously characterized substrate (see Figs. 3-35, 3-36) were probed and connected externally to form an enhancement-depletion inverter (Fig. 4-5). The W/L ratio for both the 50nm depletion load device ($V_T \sim$ -3.4V) and the 10nm enhancement driver ($V_T \sim 1.1V$) is 100μm/100μm. Using a supply voltage of $V_{DD} =$ 5V, the resulting inverter has a gain of -20 at the voltage midpoint, $V_M = 2.5V$. From the inverter characteristic in Fig. 4-5, the calculated noise margins are $NM_H = 1.5V$

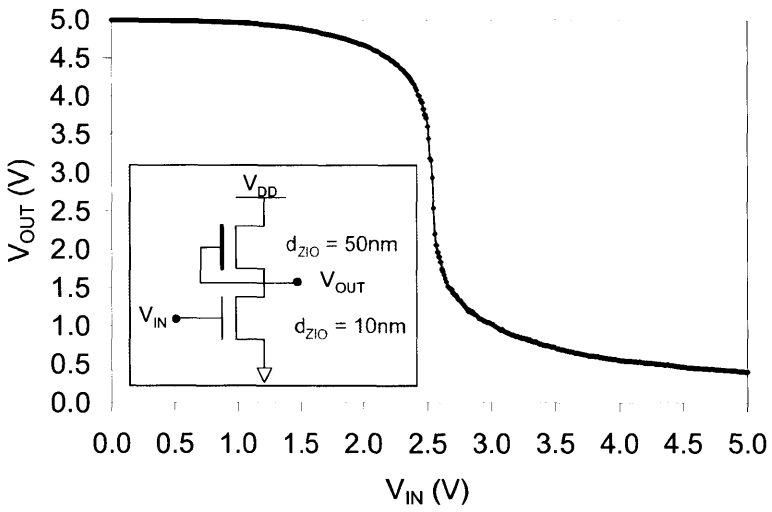

Figure 4-5: Inverter characteristic for dual threshold voltage FET circuit with V_{DD} = 5V and gain of -20 at V_M = 2.5V. Both the 10nm driver and 50nm depletion load ZIO FETs have W/L = 100μm/100μm; their V_Ts were 1.1V and -3.4V, respectively. The individual devices were contacted with microprobes and connected externally.

and NM_L = 1.1V.

These results compare favorably to the literature; however, the inverter in Fig. 4-5 is not an integrated circuit. Although we could take a similar approach to Lee, *et al.* and use shadow masks to pattern two different channel layers for an integrated inverter, a fully lithographic fabrication process offers the ability to design more complex circuits beyond simple inverters. The development and application of such a process is described in the rest of the chapter.

4.2 Fully lithographic two V_T FETs

In the previous section we demonstrated high gain and nearly rail-to-rail output in a two-V_T inverter, but it required cumbersome external connections. While an integrated inverter could be produced by using a more specially-designed shadow mask during ZIO deposition, this approach still limits the range of feature sizes and process scalability. To enable the development of arbitrarily complex patterns for integrated two-V_T FET circuits, a fully lithographic process capable of producing FETs with different threshold voltages side by side is needed.

In this section we show that the baseline lithographic process from Chapter 2 can be expanded to integrate multiple channel thicknesses on a single substrate. Electrical characterization verifies that FETs with different threshold voltages can be produced using the modified process.

4.2.1 Modified lithographic process

The key change to the fabrication process is adding the ability to pattern multiple semiconductor layers instead of only a single channel thickness. As highlighted in green in Fig. 4-6, the only change to baseline process required is the active layer patterning step; all other layers can be processed as previously described in Chapter 2.

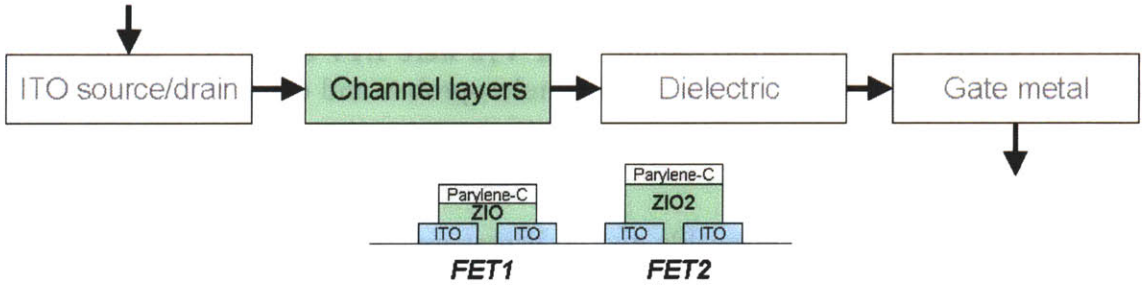

Figure 4-6: Schematic diagram of the general FET process flow. The modified process to generate FETs with different channel thicknesses on the same substrate (bottom) only requires changes to the channel layer processing step.

Our modified approach to patterning the channel layers is drawn schematically in Fig. 4-7. In part A, the first channel thickness for the FET on the left (FET1) is deposited and patterned with photoresist as before. Note that the deposited semiconductor/protective parylene stack 1 is completely removed from the region occupied by the second FET on the right (FET2). In part B, a second active area stack is deposited over the wafer and this time, the photoresist is exposed to pattern FET2. During the oxygen plasma etch of the parylene 2 layer, the original protective parylene over FET1 is protected by the second oxide layer (ZIO2). We found that a layer of ZIO $\geq$ 10nm is sufficient to protect the parylene underlayer. After this dry etch, the semiconductor (ZIO2) is wet-etched in dilute HCl to complete the active area patterning for FET2. During the second wet etch, the first ZIO layer is protected by its

protective parylene cap. The use of two disparate materials (an oxide semiconductor and an organic dielectric) allows them to serve as etch stops for each other.

Although the schematic depicts the patterning of two channel thicknesses, the process could be iterated to define more than two channel thicknesses on the same substrate with the appropriate masks. We found that 10–50nm-thick ZIO films sputtered on top of 100nm-thick parylene were smooth with no evidence of cracking and/or delamination even after wet processing and photoresist baking.

Mask redesign and process efficacy

To take advantage of the new process, we designed a new mask with simple integrated FET circuits as well as individual FET arrays, MIM and MIS capacitors, and process test structures. Identical die were repeated across the entire wafer. The placement of FETs with different V_Ts side by side in each die minimizes the effects of variation across the wafer when comparing FET performance.

In-process photomicrographs for a wafer with two semiconductor channel thicknesses are shown in Figs. 4-8 and 4-9. All layers except the gate electrode were already completed. For this wafer, the 10nm-thick ZIO (A1) was deposited and patterned before subsequent patterning of a 30nm-thick ZIO layer (A2). Fig. 4-8(a) shows part of an array of individual FETs where rows of devices with 10nm-thick ZIO (A1) alternate with rows with 30nm-thick ZIO (A2). Fig. 4-8 shows two rows of three different 150μm x 150μm square capacitor structures. The leftmost structure contains no ZIO (M) in order to form an MIM capacitor; the center and middle structures contain 10nm ZIO (A1) and 30nm ZIO (A2), respectively, to form MIS capacitors. The two thicknesses of the transparent ZIO appear as different colors underneath the parylene gate/interlevel dielectric layers.

Three types of two-FET inverters from the same wafer are photographed in Fig. 4-9. The inverters in Fig. 4-9(a) and (b) are designed to have both load and driver FETs with the same channel thickness (A1 or A2). The inverters in Fig. 4-9(c) integrate load and driver FETs with different channel thicknesses to form dual-V_T inverters. The two layers are visible in the color photographs, confirming that we can successfully

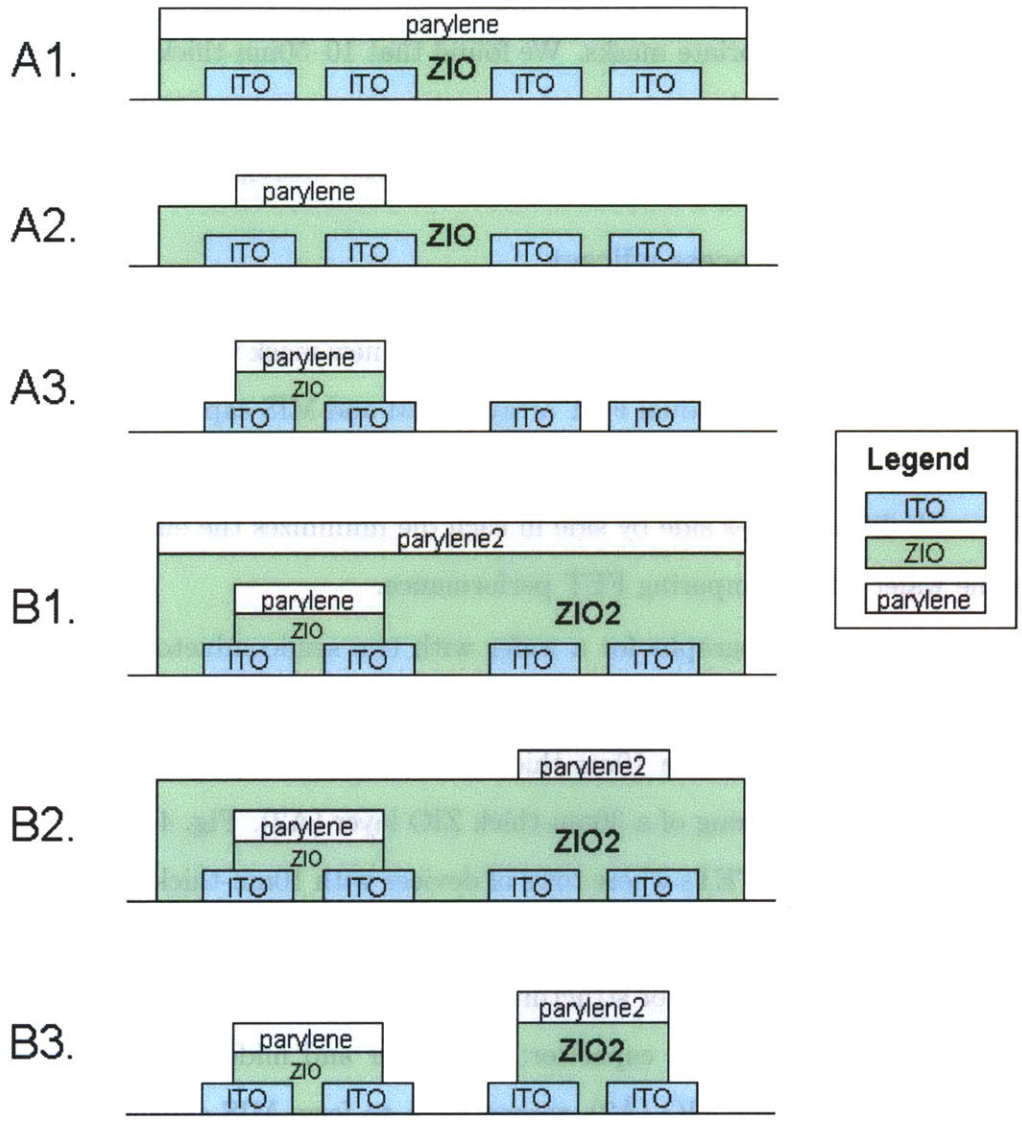

Figure 4-7: Expanded view of modified channel layer patterning sub-process. Steps A1-A3 pattern the first channel layer; steps B1-B3 form the second channel layer. This sub-process takes advantage of the wet-etch resistance of parylene and dry-etch resistance of the oxide to use each as an etch stop for the other.

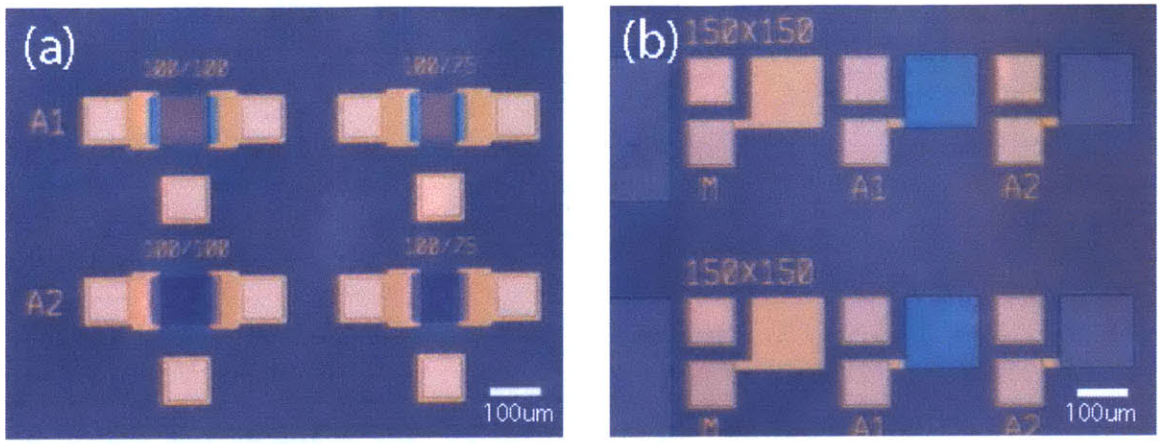

Figure 4-8: Photomicrographs from an in-process wafer prior to gate electrode deposition. Vias through the interlevel dielectric have already been etched. (a) Individual FET structures with 10nm ZIO (row A1) and 30nm ZIO (row A2) layers. (b) Square capacitor structures with no ZIO (M), 10nm ZIO (A1), and 30nm ZIO (A2). The two thicknesses of the transparent ZIO layers appear as different colors.

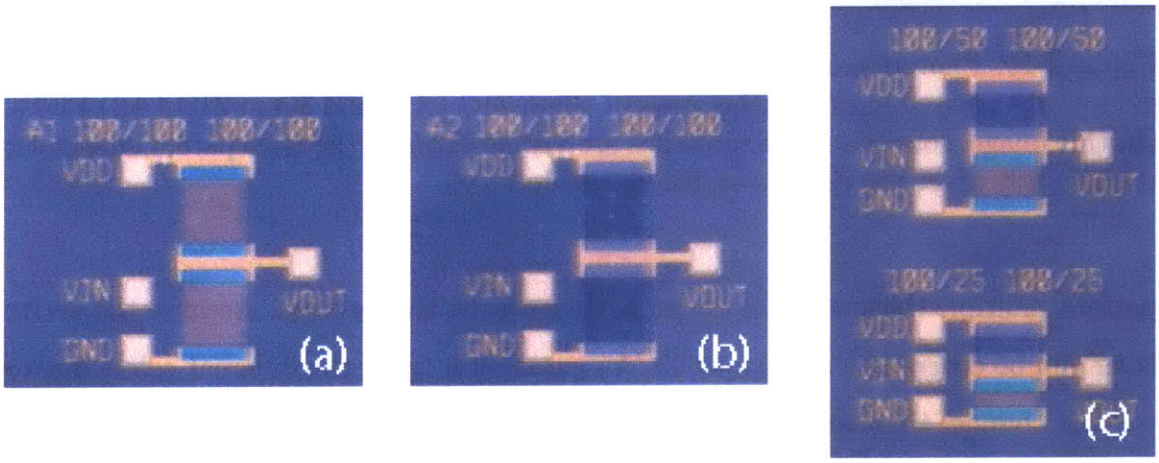

Figure 4-9: Photomicrographs from an in-process wafer prior to gate electrode deposition. Vias through the interlevel dielectric have already been etched. (a) Inverter with W/L = 100μm/100μm for both load and driver FET; the channel layer (A1) is 10nm-thick. (b) Inverter with W/L = 100μm/100μm for both load and driver FET; the channel layer (A2) is 30nm-thick. (c) Inverters with equally sized load and driver FETs; the driver FET has a 10nm-thick ZIO layer (A1) and the load FET has a 30nm-thick ZIO layer (A2). The two thicknesses of the transparent ZIO layers appear as different colors.

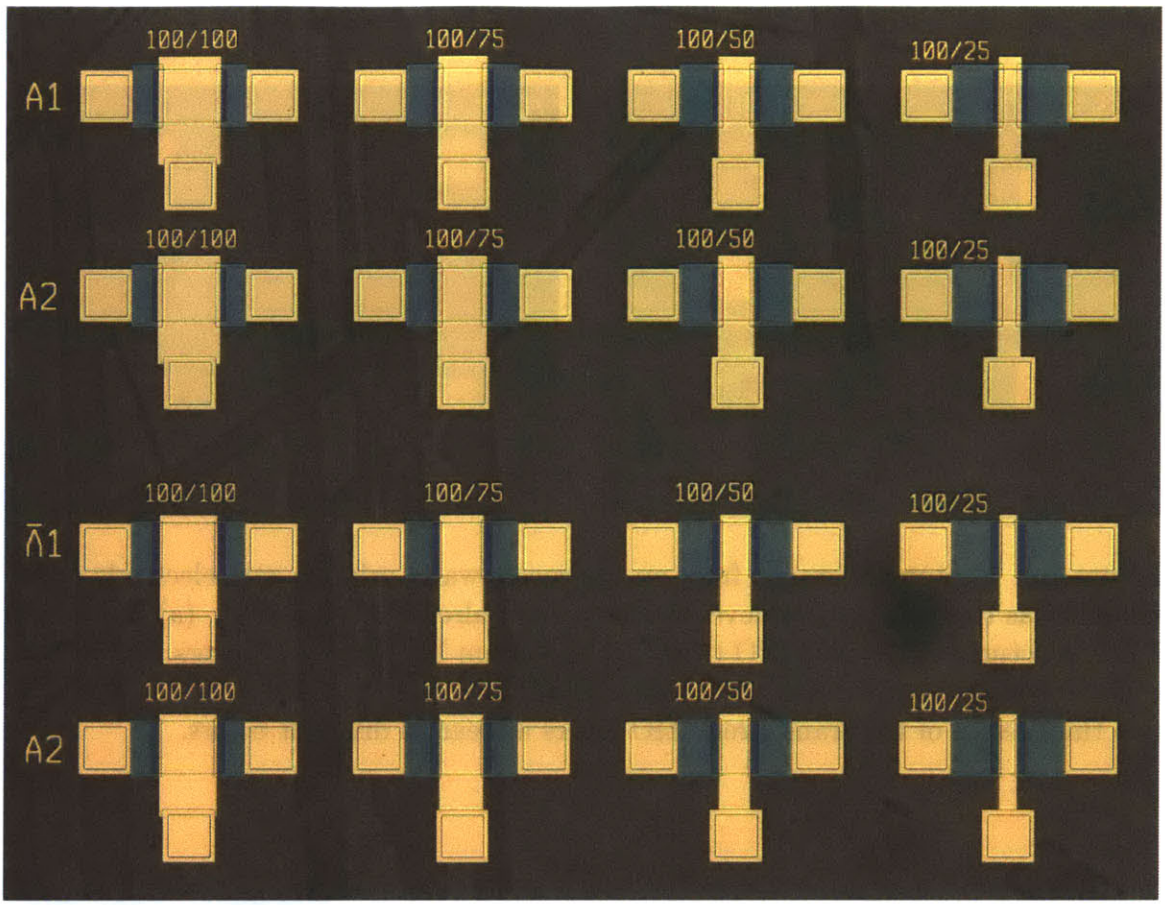

Figure 4-10: Photomicrograph of completed individual FETs. Varying channel length devices are arrayed in alternating rows of 10nm ZIO (*A1*) and 30nm ZIO (*A2*) FETs. (In this image, some backside scratches are visible through the transparent substrate; they do not affect the devices on the frontside.)

pattern multiple thicknesses of the active layer using this process. Because the active layer will be covered by an opaque Cr/Au gate metal layer, the different colors due to varying channel thicknesses are not visible after fabrication is completed. Fig. 4-10 shows a photomicrograph of an FET array on the finished wafer.

Though we successfully demonstrated the ability to integrate multiple ZIO thicknesses on a single substrate by lithographic patterning, one concern is the quality of the channel interfaces. As shown in the simulations in Section 3.4.2, the presence of interface traps significantly affects FET performance. We previously noted the difficulty in precisely controlling stoichiometry and interface traps in our unoptimized material deposition processes. The partially shadow-masked process used in

Section 3.6 sidestepped this issue by sputtering all semiconductor thicknesses in a single deposition on a single substrate so that the material properties and interfaces would be as uniform as possible for comparison purposes.

In contrast, in the fully lithographic process the different thickness active layer stacks are deposited in completely separate runs. This process requires selective removal of the previously deposited channel material prior to the deposition and patterning of subsequent channel layers. It is reasonable then to question whether the different threshold voltages observed in FETs fabricated in the fully lithographic process depend on the active layer patterning order, not semiconductor thickness. In the next section, we reproduce the V_T-channel thickness trend seen in the partially shadow-mask processed wafers and show that the trend holds whether the thicker ZIO channel or thinner ZIO channel is patterned first.

4.2.2 Device characterization: two V_Ts on one substrate

Because of issues with significant wafer-to-wafer variation as well as noticeable die-to-die non-uniformity, the most meaningful comparisons are between FETs situated close to each other on the same wafer. For this reason, the mask was purposely designed to intersperse individual devices with different channel thicknesses in addition to adding the integrated circuits. We show three sets of data from different wafers to verify that the V_T-channel thickness trend holds true for the fully lithographic process.

10nm ZIO versus 40nm ZIO

For the first data set shown, a thin ZIO channel layer (10nm) was deposited and patterned before the thicker ZIO layer (40nm). Both channels were deposited in 15% O_2 sputtering ambient; all other fabrication details followed the modified baseline process. Fig. 4-11 plots the linear and saturation transfer I-V characteristics for both 10nm (green curves) and 40nm (blue curves) devices.

Compared to the partially shadow mask-patterned devices shown in Chapter 3.6, these FETs had very slightly higher gate leakage, $I_g \sim 6\text{x}10^{-9}\text{A/cm}^2$. This difference we attribute to a thinner gate dielectric (200nm versus 280nm) rather than any effects

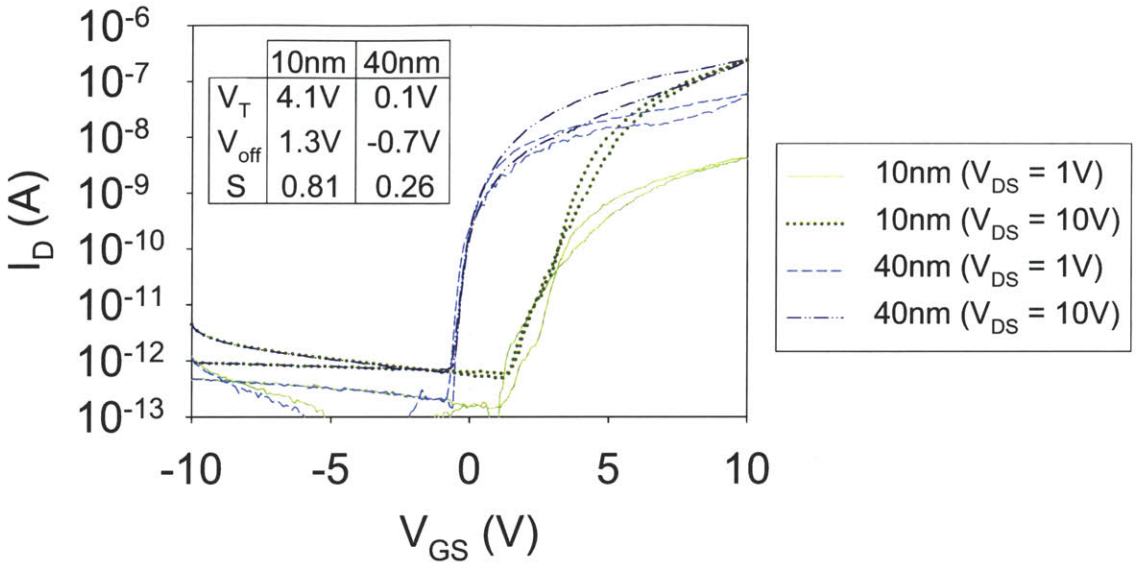

Figure 4-11: Comparison of 10nm-thick and 40nm-thick ZIO FETs fabricated on the same wafer in the two-channel FET process. Transfer I-V characteristics at V_{DS} = 1V and V_{DS} = 10V for the thin ZIO channel (10nm, green) and the thick ZIO channel (40nm, blue) are overlaid to show that V_{off} and V_T shift more negative for the thicker channel. Values for V_T and V_{off} are shown in the inset table.

from the fully lithographic process. On the other hand, the different subthreshold slopes in the transfer curves in Fig. 4-11 are likely caused by the new process, since the two separate semiconductor and protective parylene stacks are subject to process variations, particularly in material deposition.

Nevertheless, as expected V_{off} and V_T are more negative for the thicker ZIO channel FET. The inset table in Fig. 4-11 lists the values of V_{off} and V_T, which show shifts of 2V and 4V, respectively for 10nm versus 40nm devices.

30nm ZIO versus 10nm ZIO

For the second data set, the thick ZIO channel layer (30nm) was deposited and patterned before the thin ZIO layer (10nm). Following the modified baseline process, both layers were sputtered in 10% O_2 in separate deposition runs. Fig. 4-12 compares the linear and saturation transfer I-V characteristics of the 10nm (green curves) and 30nm (blue curves) device.

Despite the reversed patterning order the thicker channel FET still shows more

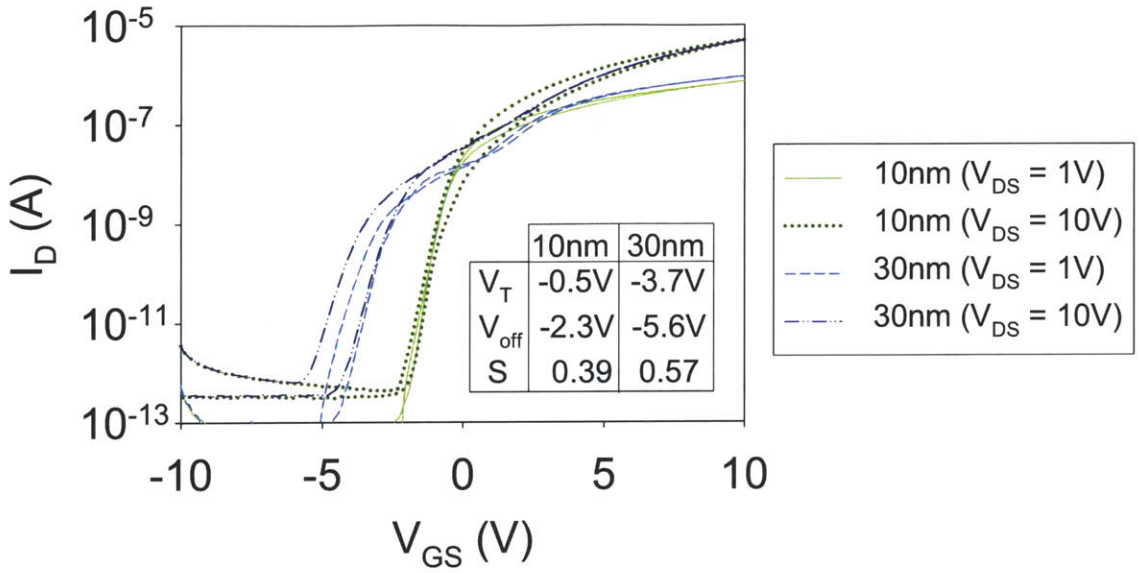

Figure 4-12: Comparison of 30nm-thick and 10nm-thick ZIO FETs fabricated on the same wafer in the two-channel FET process. For this wafer, the thicker channel was patterned first. Transfer I-V characteristics at V_{DS} = 1V and V_{DS} = 10V for the thin ZIO channel (10nm, green) and the thick ZIO channel (30nm, blue) are plotted together. As shown in the plot and the inset table, V_{off} and V_T shift more negative for the thicker channel.

negative threshold and turn-off voltages, confirming the V_T-channel thickness trend. As the inset table shows, V_{off} and V_T in the 30nm channel are shifted by ~3V compared to the 10nm devices.

10nm ZIO versus 30nm ZIO

For the third data set, a thin ZIO channel layer (10nm) was deposited and patterned before the thick ZIO layer (30nm). With the exception of active layer patterning order, this wafer was fabricated with nominally all the same process parameters as the second data set wafer. Fig. 4-13 compares the linear and saturation transfer I-V characteristics of the 10nm (green curves) and 30nm (blue curves) device.

Compared to the previous data set, the difference in transfer I-V characteristics is a reflection of the imprecise control in our unoptimized material deposition processes. Nevertheless, despite the difference in the absolute values of V_{off} and V_T from previous wafers, the V_T-channel thickness trend still holds. As shown in Fig. 4-13, V_{off}

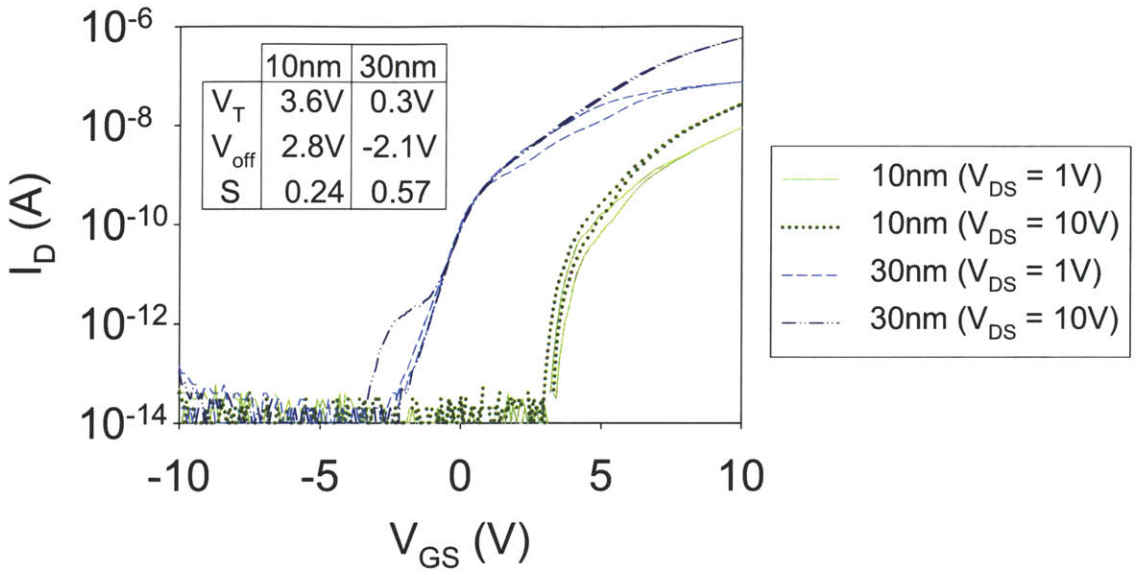

Figure 4-13: Comparison of 10nm-thick and 30nm-thick ZIO FETs fabricated on the same wafer in the two-channel FET process. For this wafer, the thinner channel was patterned first. Transfer I-V characteristics at V_{DS} = 1V and V_{DS} = 10V for the thin ZIO channel (10nm, green) and the thick ZIO channel (30nm, blue) are plotted together. As shown in the plot and the inset table, V_{off} and V_T shift more negative for the thicker channel.

shifts from -2.1V in the 30nm device to +2.8V in the 10nm device.

These three data sets demonstrate that the fully lithographic process can be used to integrate multiple channel thicknesses on a single substrate to produce FETs with different threshold voltages. This capability enables the fabrication of enhancement-depletion inverters and ring oscillators, as demonstrated later in this chapter.

4.3 Enhancement/depletion inverters

The availability of FETs with different threshold voltages allows the implementation of enhancement-depletion (E/D) inverters that have higher gains and larger noise margins than single-V_T inverters. In this section we discuss the performance of E/D inverters fabricated in the two-V_T lithographic process.

4.3.1 Load line analysis: calculated transfer curves

Using the electrical characterization data of the individual FETs from the previous section, we can predict the integrated inverter transfer curves using load line analysis. For comparison, both a single V_T inverter (E/E) using a diode-connected load and a dual V_T (E/D) inverter with depletion load are simulated. For all devices, W = L = 100μm. We set the power supply to V_{DD} = 5V.

To calculate the transfer curve for an E/E inverter, Fig. 4-14 (left) overlays the output characteristics for driver FET and diode-connected load FET. The operating points are replotted as the voltage transfer characteristic on the right. Note that this "inverter" does not successfully invert the voltage signal; maximum gain is A_V = -1 and noise margins are negative. This poor performance is partly due to the sizing of the FETs, as in reality no optimized circuit design would set the driver:load ratio as low as 1:1 in this configuration. In contrast, the enhancement/depletion inverter simulated in Fig. 4-15 performs well with two FETs of the same size.

Fig. 4-15 (left) overlays output characteristics for an enhancement mode driver FET and depletion mode load FET to extract the expected inverter transfer characteristic. The inset in Fig. 4-15 (right) is a zoomed-in view of the output curves, which show the desirable high output resistance of the load FET. Because of high contact resistance, the driver FET's output curves are not ideal. Nevertheless, the simulated E/D inverter characteristic shows rail-to-rail operation with A_V = -11 and noise margins >1V on each side.

4.3.2 Comparison of fabricated E/E and E/D inverters

Since both discrete FETs and integrated inverters were fabricated on the same wafer, we can compare directly the simulated transfer curves to the actual circuits. Fully integrated inverters similar to those photographed in Fig. 4-9 were characterized using an Agilent 4156C in sweep mode. The experimental inverter transfer characteristics are quite similar to the calculated transfer curves, as can be seen by comparing Fig. 4-16 and Figs. 4-14, 4-15.

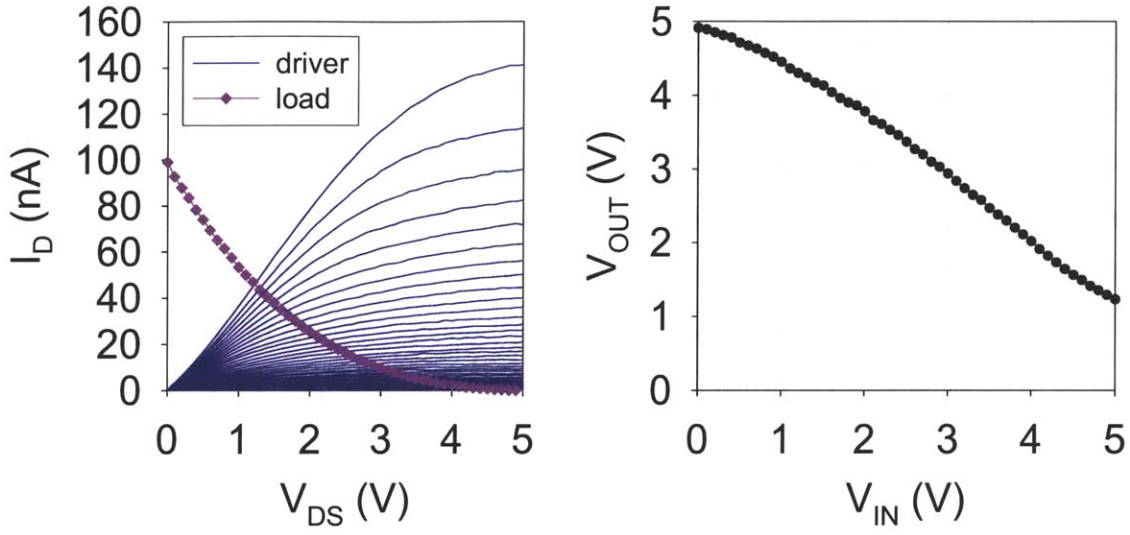

Figure 4-14: Load line analysis for E/E inverter based on W/L = 100μm/100μm enhancement mode FETs (Fig. 4-13, 10nm). The simulated transfer characteristic shows poor performance with A_V = -1 and negative noise margins.

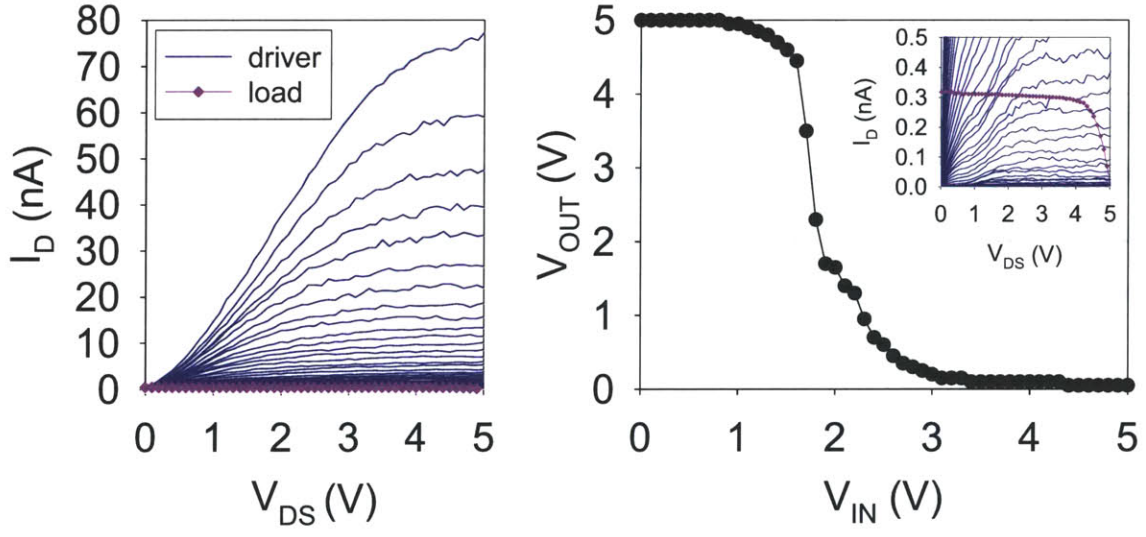

Figure 4-15: Load line analysis for E/D inverter based on W/L = 100μm/100μm enhancement and depletion mode FETs (Fig. 4-13, 10nm and 30nm). The simulated transfer characteristic shows excellent performance with A_V = -11 and NM_L = 1.15V and NM_H = 1.9V.

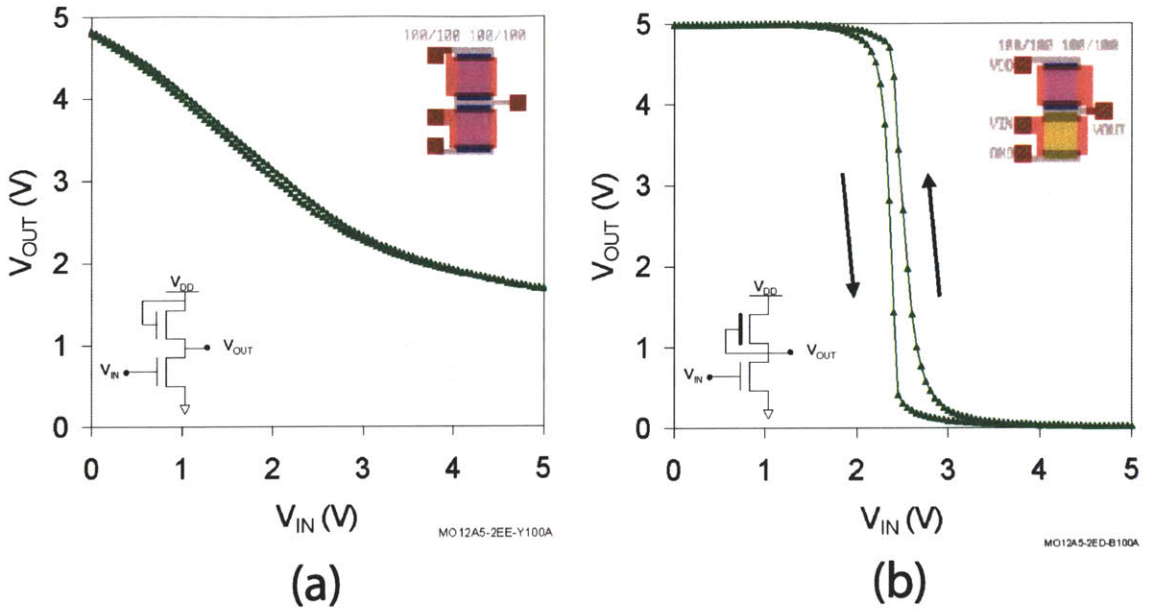

Figure 4-16: Measured transfer characteristics for (a) E/E inverter and (b) E/D inverter at V_{DD} = 5V. The sizing for all FETs is W/L = 100μm/100μm. Both inverters were fabricated on the same wafer together with the FETs shown in Fig. 4-13. The depletion load yields superior performance in the E/D inverter, with A_V = -23 and noise margins > 2V on each side.

The fabricated E/D inverter performs far better than the E/E "inverter," which shows a gain < 1 and negative noise margins. Conversely, the E/D inverter achieves A_V = -23 with a switching point near $V_{DD}/2$ and excellent noise margins > 2V. With the exception of the hybrid CMOS ZnO-pentacene inverters, these results outperform metal oxide-FET inverters reported in the literature at a lower or equal supply voltage V_{DD}.

4.3.3 Inverter hysteresis

The double-swept inverter characteristic in Fig. 4-16 (right) shows hysteretic behavior, with the return sweep from V_{IN} = 5V to 0V displaying a more positive V_M than the initial sweep. The amount of voltage shift is related to sweep speed. As shown in Table 4.1, increasing the delay time between the measurement of each data point and hence, the total sweep time, results in larger hysteresis. (Note that a delay time of 0s does not mean the sweep occurs instantaneously, since the Agilent 4156C

Delay time (s)	V_{shift} (V)
0	0.05
0.1	0.18
0.2	0.25
0.5	0.29
1.0	0.39

Table 4.1: Inverter hysteresis as a function of delay time between each data point measurement, as calculated from the shift in V_{in} at $V_{out} = V_{DD}/2 = 2.5V$ for each double sweep. The longer the delay time (i.e. the longer the total sweep time), the more hysteresis is observed.

still requires a finite amount of time to measure at each voltage step. Delay time is controlled by the operator to force the machine to wait the specified time before taking a measurement, but the total sweep time is longer than delay time $\times$ number of data points.) For each doublesweep, V_{in} is measured in 0V to 5V and back in 50mV increments for a total of 202 points.

We speculate that the voltage shift is caused by gate bias stressing of the FETs which causes the threshold voltage to shift. Qualitatively, we have observed that voltage shifts due to continuous gate bias stressing do not increase linearly but eventually saturate. In addition, the shift is not permanent and recovery begins as soon as gate bias is removed.

Similar results have been reported more quantitatively in various studies in the literature on bias stress stability in metal oxide FETs. It has been shown that FET stability can be improved by optimizing material composition and preparation. Such improvements are beyond the scope of this thesis, but could be easily applied in the framework presented here.

4.3.4 Reducing inverter area

One of the advantages of photolithography is the ability to pattern small features with tight tolerances. The previously demonstrated inverters used FETs with L = 100μm, but total inverter area could be significantly reduced by shrinking down FET dimensions. Keeping W = 100μm, we fabricated inverters with shorter channel

	V_{DD} = 5V				V_{DD} = 3V			
L (μm)	A_V	V_M	NM_L	NM_H	A_V	V_M	NM_L	NM_H
100	-23	2.4V	2.3V	2.4V	-28	1.3V	1.1V	1.4V
50	-31	1.9V	1.6V	2.9V	-34	1.4V	1.1V	1.4V
25	-25	1.5V	1.0V	3.3V	-24	1.6V	1.2V	1.2V

Table 4.2: Performance summary of lithographically patterned E/D inverters where the sizing ratio of load and driver FETs = 1:1. For all FETs, W = 100μm and L = 100μm, 50μm, or 25μm. Each inverter was tested at V_{DD} = 5V and V_{DD} = 3V.

lengths and similar or better performance.

Fig. 4-17 shows the transfer characteristic for an E/D inverter composed of FETs with half the channel length, i.e. W/L = 100μ/50μm. A photomicrograph of the inverter is shown in the inset on the upper right. Instead of V_{DD} = 5V, the supply voltage was reduced to V_{DD} = 3V while maintaining nearly rail-to-rail operation ($V_{OH} \sim V_{DD}$, $V_{OL} \sim$ 0.1V) and $|A_V| > 20$. The high gain results in wide noise margins of 1.1V and 1.4V on either side.

Reducing channel length by half again, we fabricated and characterized inverters with W/L = 100μ/25μm. Fig. 4-18 plots the voltage transfer characteristic for such an inverter, with a photomicrograph of the actual inverter inset. At V_{DD} = 3V, the inverter operates nearly rail-to-rail ($V_{OH} \sim V_{DD}$, $V_{OL} \sim$ 0.15V) with A_V = -24 and noise margins of $\sim$ 1.2V on either side.

Table 4.2 summarizes the performance of the 3 different E/D inverters at both V_{DD} = 5V and at V_{DD} = 3V. As previously indicated, for all inverters the ratio between load and driver FETs is 1:1. For simplicity, we will refer to each inverter by the channel length of its constituent FETs: 100μm, 50μm, or 25μm.

While all inverters perform well at V_{DD} = 5V, the 100μm inverter offers V_M closest to $V_{DD}/2$ = 2.5V and nearly equal noise margins. These results are competitive with the best unipolar n-channel oxide inverters demonstrated in the literature by Oh, *et al.* and Yin, *et al.* [131, 133]. While Oh, *et al.* reported a ZnO inverter with twice the inverter gain at V_{DD} = 5V, the switching voltage was at 1.45V rather than 2.5V. More significantly, their fabrication process required shadow masking to form

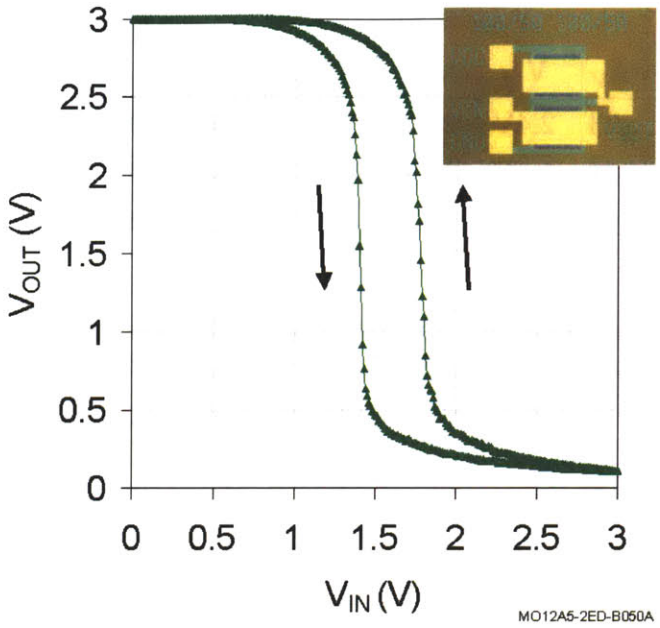

Figure 4-17: Voltage transfer characteristic for E/D inverter where W/L = 100μm/50μm for both enhancement driver and depletion load FETs. With V_{DD} = 3V, $|A_V| > 20$ and noise margins are 1.1V and 1.4V on either side. The inset shows a photomicrograph of the actual inverter.

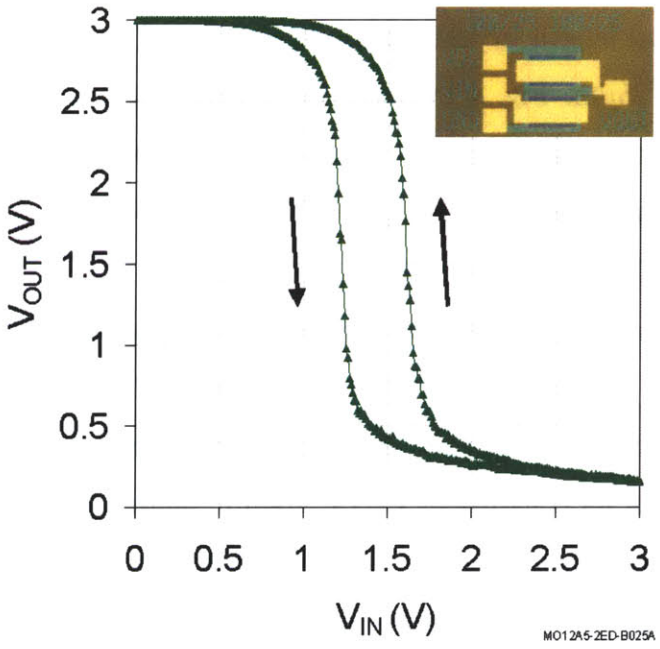

Figure 4-18: Voltage transfer characteristic for E/D inverter where W/L = 100μm/25μm for both enhancement driver and depletion load FETs. With V_{DD} = 3V, A_V = -24 and noise margins are ~1.2V on either side. The inset shows a photomicrograph of the actual inverter.

the electrodes for the top- and bottom-gate FETs while the inverters presented here were patterned in a fully lithographic process. In comparison, the lithographically patterned GIZO/IZO inverters demonstrated by Yin, *et al.* have a lower gain ($A_V \sim$ -15) with similarly asymmetrical noise margins.

Reducing the power supply voltage is desirable for improving circuit power consumption but may also degrade performance, particularly if the inverter is no longer able to fully switch. Currently, most E/E and E/D metal oxide inverters demonstrated in the literature require $V_{DD} \geq 10V$. The lowest power supply voltage for a fully lithographically processed integrated oxide inverter ($V_{DD} = 5V$) was reported by Yin, *et al.* In this work however, we have successfully demonstrated fully lithographic E/D inverters operating at an even lower voltage. As shown in the right half of Table 4.2, reducing the supply voltage to $V_{DD} = 3V$ does not degrade inverter performance and the inverter gains remain high. All inverters show $V_M \approx V_{DD}/2 =$ 1.5V and balanced noise margins.

While all the inverters in Table 4.2 share very similar characteristics in static analysis, the shorter channel length devices produce larger drain currents and hence, faster switching times. By chaining multiple inverters together to form ring oscillators, inverter propagation delay can be measured.

4.4 Enhancement/depletion ring oscillators

4.4.1 Background

Ring oscillators (ROs) are often implemented to demonstrate new materials technologies. They are also subsequently included in wafer manufacturing as on-die test circuits to verify device performance specifications. As shown in Fig. 4-19, a ring oscillator is constructed by cascading an odd number of inverters, and the output of the last inverter is fed back to the input of the first. When a sufficiently high supply voltage is applied, after an initial transient the RO output spontaneously oscillates. A multistage output buffer can be included to avoid loading the ring oscillator and

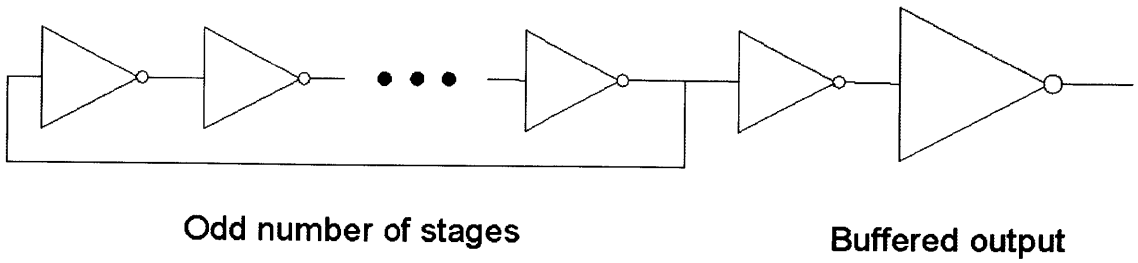

Figure 4-19: Schematic of ring oscillator with multistage output buffer. Oscillation frequency depends on the number of stages and can be used to calculate inverter propagation delay.

changing its oscillation frequency.

While a simple inverter-based RO can be used to generate clock signals, the oscillation frequency in this topology tends to be undesirably sensitive to temperature and voltage supply fluctuations. In practice, the ring oscillator is typically used as a benchmark for the speed performance of a digital circuit technology. The oscillation frequency is determined by the number of stages and the inverter delay per stage, which in turn depends on the charging and discharging currents supplied by each inverter in the chain to its load. Inverter propagation delay, or the time it takes the inverter to switch, can be calculated from the RO oscillation frequency:

$$\tau_d = \frac{1}{2nf} \tag{4.3}$$

where τ_d = inverter propagation delay, n = (odd) number of stages, and f = RO oscillation frequency.

For each inverter in the chain, switching begins as soon as the previous inverter output reaches V_M. Thus, a RO can show oscillation without its output voltage transient reaching V_{OH} and V_{OL} (the minimum and maximum output voltages that indicate a logic "1" and "0", respectively). However, the τ_d values calculated from such non-saturated RO output transients may not accurately reflect the actual inverter delay. Failure to exhibit saturated (ideally, rail-to-rail) output is more likely for ROs with an inadequate number of stages.

4.4.2 State of the art

Table 4.3 gives a brief comparison of oxide semiconductor-based ring oscillators reported in the literature. Although it is typical to report RO oscillation frequency, for more accurate comparisons between ROs with different numbers of stages we have listed the corresponding calculated inverter propagation delay τ_d for each reference instead.

The first ROs were demonstrated by Presley, *et al.* at Oregon State University in 2006. Integrating IGO channel FETs annealed at 500°C, the 5-stage RO operated at V_{DD} = 30V [137]. Ofuji, *et al.* reported a much higher performance 5-stage RO in 2007 based on sputtered IGZO FETs [127]. Despite a lower supply voltage of V_{DD} = 18V, the peak-to-peak output voltage, $V_{out,pp}$, was close to that of the previously reported RO. The authors attributed the faster speed to higher FET mobilities and tighter design rules (gate-source/drain overlap lengths of 5μm versus 200μm) that greatly reduced overlap capacitances.

To further reduce gate-drain overlap capacitances, Mourey, *et al.* utilized a gate-self-aligned process to form a 7-stage RO with gate-source/drain overlaps of 0.3μm [140]. Instead of sputtered IGZO, the channel material was ZnO deposited at 200°C by plasma-enhanced ALD for the bottom-gate FETs. Because of the opaque Cr gate layer used for the backside exposure process, the circuit is not completely transparent. This self-alignment technique cannot be used with a transparent gate layer; however, for some applications an optically transparent circuit may be preferable. To meet this goal, Suresh, *et al.* presented a fully visible-transparent 7-stage RO using IGZO channels deposited by PLD at room temperature and Al_2O_3 dielectric deposited by ALD at 200°C [142].

With the exception of the circuits presented by Yin, *et al.* from Samsung AIT, the oxide semiconductor ROs in the literature are based on E/E inverters. As previously shown, E/E inverters tend to suffer from low gain and less than rail-to-rail output voltage ranges. Of all the ROs listed in Table 4.3, the E/D RO demonstrated

	RO Topology	τ_{PD}	V_{DD}	$V_{out,pp}$	Rail-to-rail?
Wager group, Oregon State University [137]					
(2006)	5-stage E/E, transparent, IGO Max process temp ~ 500°C	45μs	30V	8V	×
Hosono group, Tokyo Institute of Technology [127]					
(2007)	5-stage E/E, IGZO Max process temp ~ NR	240ns	18V	7.5V	×
Jackson group, Penn State University [138–140]					
(2008)	7-stage E/E, ZnO Max process temp ~ 200°C	31ns	25V	~3V	×
(2010)	15-stage E/E, ZnO Max process temp ~ 200°C	22ns	16V	NR	?
(2010)	7-stage E/E, self aligned, ZnO Max process temp ~ 200°C	9.8ns	18V	NR	?
Shin, *et al.*, Gwangju Institute of Science and Technology [141]					
(2009)	5-stage E/E, ZnO Max process temp ~ 350°C	28μs	50V	~5V	×
Muth group, North Carolina State University [142]					
(2010)	5-stage E/E, transparent, IGZO Max process temp ~ 200°C	48ns	25V	~0.1V	×
Samsung Advanced Institute of Technology [133, 143]					
(2008)	5-stage bootstrapped, IGZO Max process temp ~ 300°C	<1ns	9V	<0.5V	×
(2009)	7-stage E/D, IZO/GIZO	4ns	5V	3.8V	closest

NR = not reported

Table 4.3: Performance comparison of oxide semiconductor-based ring oscillators in the literature. While fast inverter propagation delays (τ_d) in the nanoseconds are reported, these values are calculated from output transients with peak-to-peak voltage swings ($V_{out,pp}$) that are a fraction of the supply voltage V_{DD}. More reliable values are obtained when rail-to-rail output swing is demonstrated.

by Yin, *et al.* operates at the lowest supply voltage V_{DD} and achieves the largest $V_{out,pp}$ relative to V_{DD} [133]. Their circuit integrates uni-layer GIZO enhancement mode FETs and bi-layer GIZO/IZO depletion mode FETs. As standalone inverters, the E/D design successfully operates rail-to-rail at V_{DD} = 5V; however, the output transient of the 7-stage E/D RO reaches only $3.8V_{pp}$.

To date, none of the reported oxide semiconductor-based ROs have demonstrated rail-to-rail output transients. The failure to reach maximum peak-to-peak output voltages may be partly due to circuit designs with too few stages to ensure saturated logic swing. As previously noted, in a RO with a small number of stages the individual inverters may not switch completely before their input reverses. For this reason, the τ_d values calculated from the measured oscillation frequency in Table 4.3 probably underestimate the actual inverter propagation delays.

4.4.3 Predicted and actual performance

The inverter propagation delay can be roughly estimated knowing the device layout, dielectric capacitance, and current drive. For each inverter in a ring oscillator, the load capacitance is simply the input capacitance to the next inverter in the chain. The time to switch can be estimated using the following simple equation:

$$\Delta t = \frac{C_L \Delta V}{i} \tag{4.4}$$

where C_L is the load capacitance, V is the voltage, and i is the charging current, or the current supplied by the inverter. The input capacitance for each input driver FET can be estimated by summing the gate capacitance and parasitic gate-source/drain overlap capacitances:

$$C_L \approx C_{gate} + C_{overlap} \tag{4.5}$$

$$= C_{ins} * [WL + 2W_{overlap}L_{overlap}] \tag{4.6}$$

Assuming a constant current $I_{D,load}$, the propagation delay from output low to high (t_{PLH}) for a rail-to-rail E/D inverter can be estimated as

$$t_{PLH} \approx \frac{C_{ins} * [WL + 2W_{overlap}L_{overlap}] * V_{DD}/2}{I_{D,load}} \tag{4.7}$$

Similarly, the propagation delay from output high to low (t_{PHL}) can be estimated as

$$t_{PHL} \approx \frac{C_{ins} * [WL + 2W_{overlap}L_{overlap}] * V_{DD}/2}{I_{D,driver} - I_{D,load}} \tag{4.8}$$

The overall inverter propagation delay τ_{PD} is then an average of t_{PLH} and t_{PHL}.

Fig. 4-20 plots the voltage transfer characteristic for a 25μm inverter and its corresponding static current for a supply voltage of V_{DD} = 3V. When the input is 'low,' the driver FET is off and only a small static leakage current of 1.1pA flows through the device. When the input is 'high,' both FETs are on and the static current is 3.3nA, i.e., the driver sinks all the current supplied by the load FET to bring the output 'low.' During switching, current from either the driver ('high' to 'low') or load ('low' to 'high') FET drives the output to its final value.

For these E/D inverters, we expect $t_{PLH} > t_{PHL}$ because the depletion load FET supplies a smaller, fixed current compared to the enhancement driver FET. Using the values in Table 4.4 and output I-V characteristics for L = 50μm and L = 25μm FETs, we calculated estimates for inverter propagation delay. Table 4.5 summarizes the calculated values for t_{PLH}, t_{PHL}, and τ_{PD} at both V_{DD} = 3V and V_{DD} = 5V. The overall inverter propagation delays are slightly shorter for the lower supply voltage. Because not all parasitic capacitances are included (wiring, etc.) these values are expected to underestimate the actual propagation delay measured from the fabricated ROs.

Fabrication of E/D ring oscillators

Integrated enhancement/depletion ring oscillators were fabricated in the two-channel lithographic process together on the same wafer as the inverters characterized

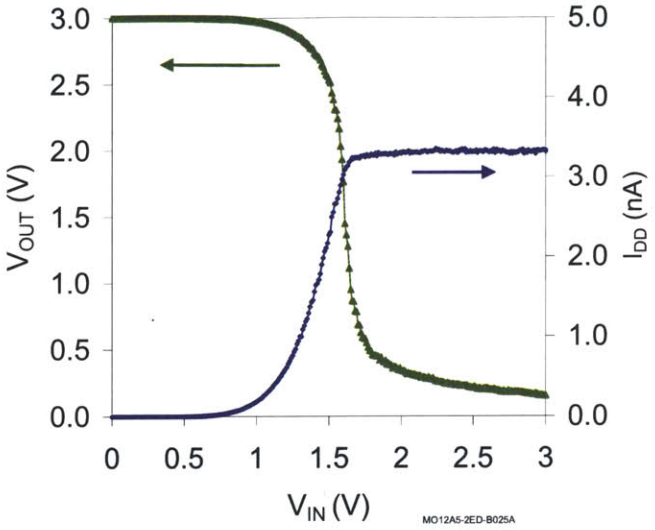

Figure 4-20: Plot of E/D inverter characteristics. The voltage transfer function is plotted on the left axis; the corresponding current through the inverter, I_{DD}, is plotted on the right axis. The inverter draws a static current of 1.1pA when V_{in} = 0V (V_{out} = 'high') and 3.3nA when V_{in} = 5V (V_{out} = 'low'). The enhancement driver FET channel is 10nm thick; the depletion load FET channel is 30nm thick. Device dimensions for both FETs are W/L = 100μm/25μm.

Geometric parameters (for all devices):			
W	$W_{overlap}$	$L_{overlap}$	C_{ins}
100μm	120μm	10μm	9.0x10^{-9}F/cm^2

Table 4.4: Parameter values for inverter propagation delay calculation

Channel length	V_{DD} = 5V			V_{DD} = 3V		
	τ_{PLH} (ms)	τ_{PHL} (ms)	τ_{PD} (ms)	τ_{PLH} (ms)	τ_{PHL} (ms)	τ_{PD} (ms)
L = 50μm	1.10	0.011	0.56	0.67	0.069	0.37
L = 25μm	0.35	0.005	0.17	0.21	0.029	0.12

Table 4.5: Estimated propagation delays for 50μm and 25μm inverters at two different supply voltages, V_{DD} = 3V and V_{DD} = 5V.

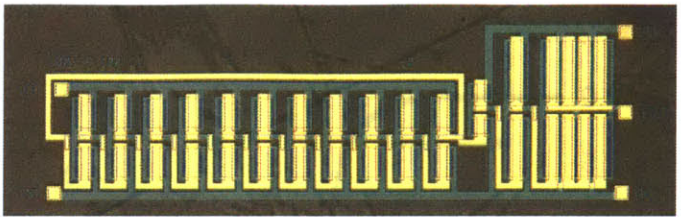

Figure 4-21: Photomicrograph of 11-stage E/D ring oscillator with three-stage output buffer. The ZIO channel is 10nm-thick for the enhancement driver FETs and 30nm-thick for depletion load FETs. Device dimensions for all FETs in the RO are W/L = 100μm/25μm.

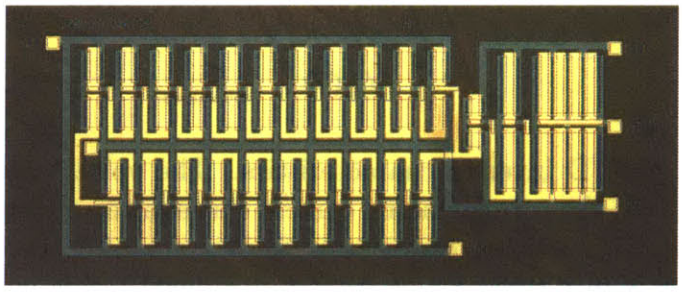

Figure 4-22: Photomicrograph of 21-stage E/D ring oscillator with three-stage output buffer. The ZIO channel is 10nm-thick for the enhancement driver FETs and 30nm-thick for depletion load FETs. Device dimensions for all FETs in the RO are W/L = 100μm/25μm.

in Section 4.3. Each RO was implemented with a three-stage output buffer to minimize loading during measurement of the oscillation frequency. Fig. 4-21 shows a photomicrograph of an 11-stage E/D ring oscillator implemented with 25μm channel length FETs. Device dimensions for both enhancement mode driver and depletion mode load FETs are W/L = 100μm/25μm. A ring oscillator with twice as many stages (21-stage) is shown in Fig. 4-22 and integrates a total of 48 individual FETs.

We expect the extracted inverter propagation delay to be the same for both ROs since the component inverters share identical dimensions (L = 25μm). A second 21-stage RO composed of 50μm channel length FETs (not pictured) should exhibit longer propagation delays due to lower drive currents and larger device areas and hence capacitance.

Characterization of fabricated ring oscillators

Initially, we measured the RO output transients using an Agilent 4156C in sampling mode. While rail-to-rail voltage output was observed, the data contained too few points to accurately measure oscillation frequency. Instead, RO output transients were measured using an Agilent DSO6034A digital storage oscilloscope. Because of the large input impedance of the scope probes, the RO output voltage signal was buffered by using a LMC6062 precision op amp in unity gain configuration.

Fig. 4-23 plots the output transients for 3 ring oscillators: (a) 21-stage, 50μm channel length (top); (b) 21-stage, 25μm channel length (middle); (c) 11-stage, 25μm channel length (bottom). All are plotted on the same time scale for comparison. The supply voltage (V_{DD} = 5V) is the same as that used by Yin, *et al.* for uni/bi-layer E/D ring oscillator [133] but these ROs demonstrate a larger $V_{out,pp}$.

The 50μm RO oscillates more slowly than the 25μm RO with the same number of stages due to lower on-currents in the longer channel length devices. On the other hand, the 25μm RO with half as many stages (11-stages vs. 21-stages) operates at twice the frequency of the corresponding RO built from FETs with the same channel length. Since the propagation delay for all 25μm inverters should be the same, these results follow expectation.

The same ring oscillators can also be operated at a lower supply voltage of V_{DD} = 3V, as shown in Fig. 4-24. Again, all three are plotted on the same time scales for comparison. Even at the lower supply voltage, the ROs demonstrate rail-to-rail operation.

Using the data in Figs. 4-23 and 4-24 and Eqn. 4.3, we extracted the inverter propagation delays for each RO. As shown in Table 4.6, τ_{PD} is longer for the 50μm RO and the same for both 25μm ROs. Compared to the estimated values in Table 4.5, these values are slightly larger since the actual devices include parasitic capacitances not accounted for in hand calculations.

Relative to ROs reported in the literature, these circuits appear quite slow. One cause for the long propagation delays is the large device areas and gate-source/drain

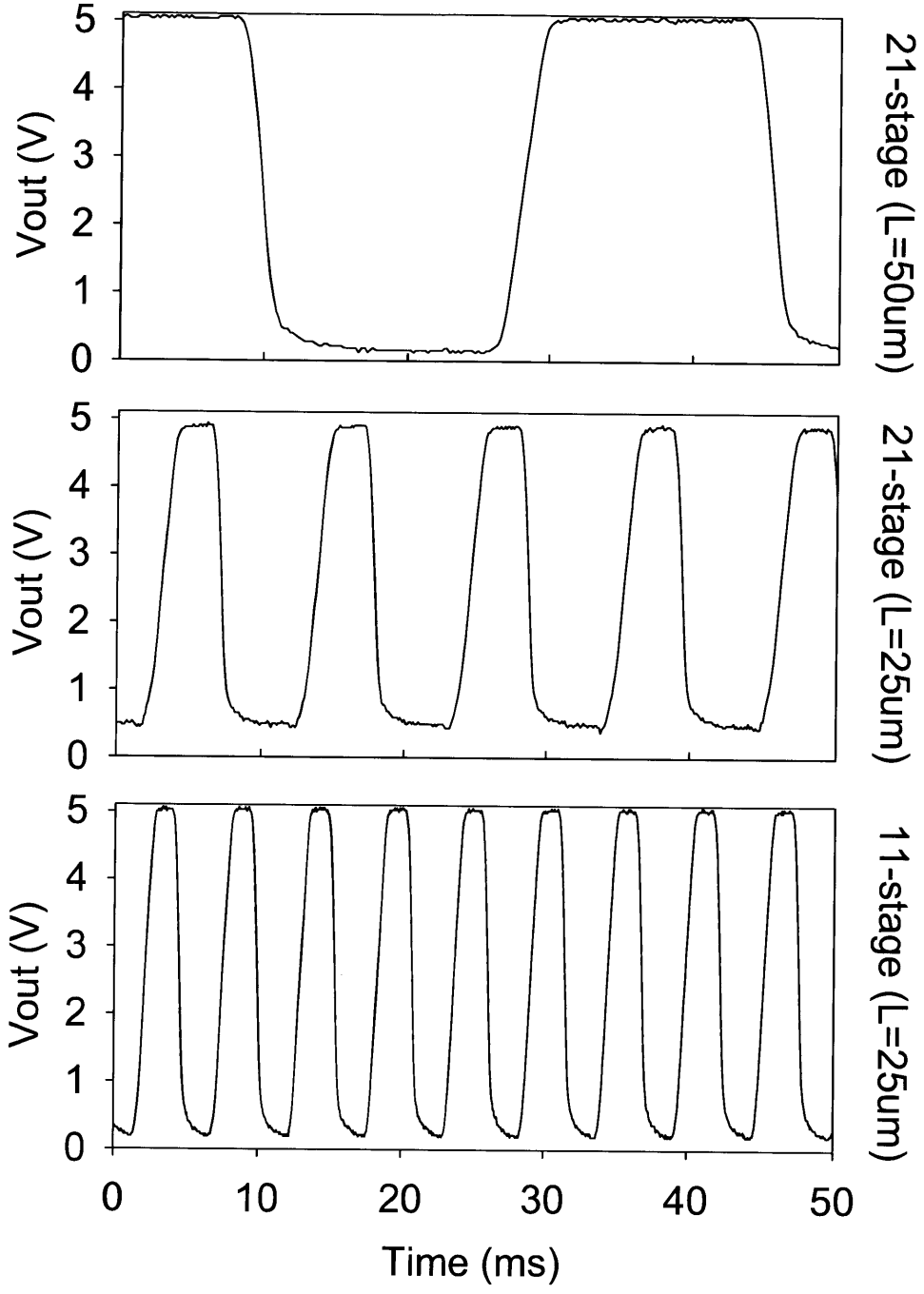

Figure 4-23: Ring oscillator output transients for a 21-stage, 50μm channel length RO (top); 21-stage, 25μm channel length RO (middle); and 11-stage, 25μm channel length RO (bottom) operating with V_{DD} = 5V. All show rail-to-rail behavior.

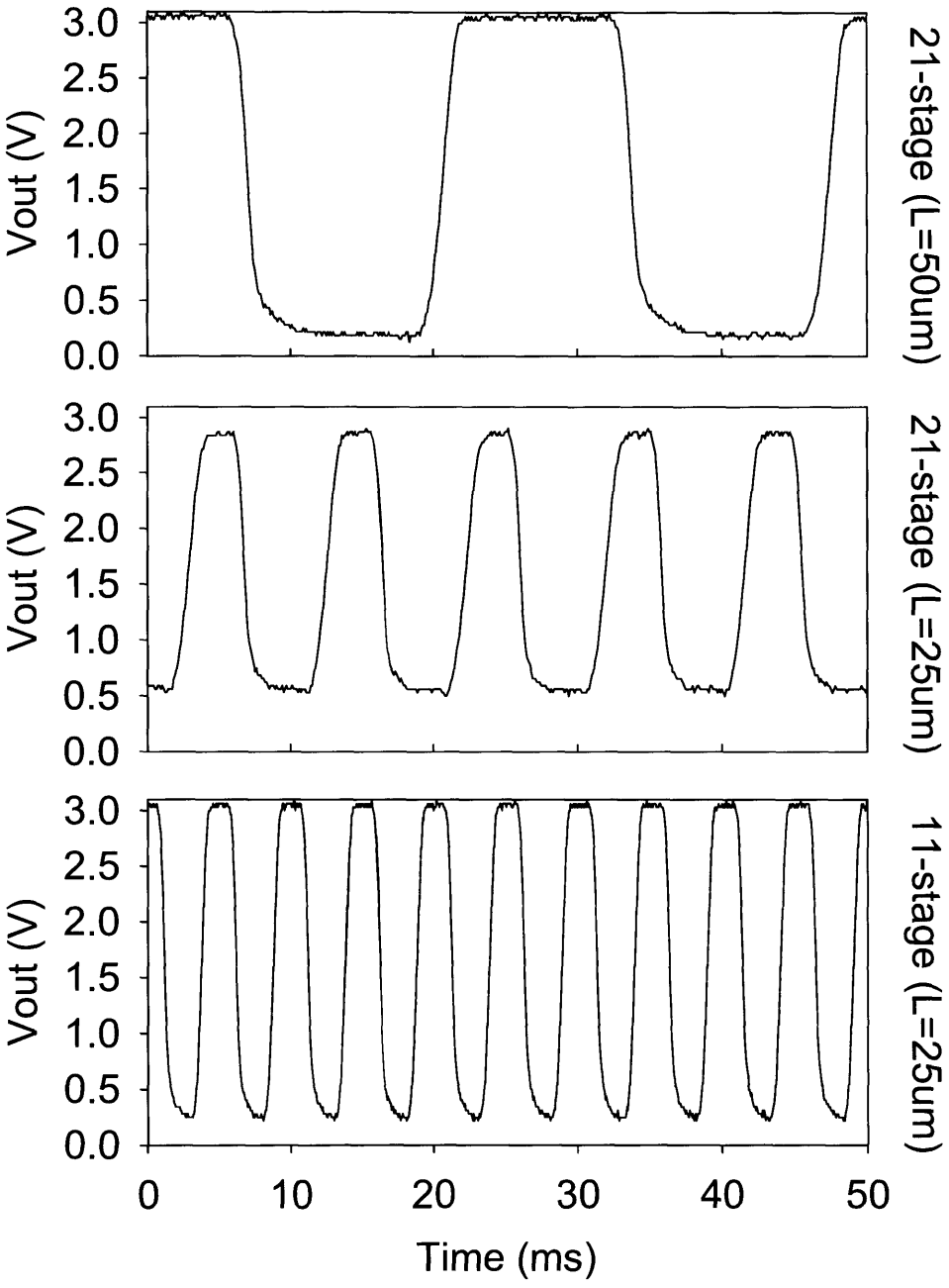

Figure 4-24: Ring oscillator output transients for a 21-stage, 50μm channel length RO (top); 21-stage, 25μm channel length RO (middle); and 11-stage, 25μm channel length RO (bottom) operating with V_{DD} = 3V. All show rail-to-rail behavior.

RO topology	Measured		Estimated	
	V_{DD} = 5V τ_{PD} (ms)	V_{DD} = 3V τ_{PD} (ms)	V_{DD} = 5V τ_{PD} (ms)	V_{DD} = 3V τ_{PD} (ms)
L = 50μm, 21-stage	0.85	0.64	0.56	0.37
L = 25μm, 21-stage	0.26	0.23	0.17	0.12
L = 25μm, 11-stage	0.24	0.23	0.17	0.12

Table 4.6: Summary of measured inverter propagation delays from the ring oscillators in Figs. 4-24, 4-23. The measured values are slightly larger than the calculated values (repeated here from Table 4.5) since the actual devices include parasitic capacitances not accounted for in hand calculations.

overlaps. In the case of the L = 25μm FETs, the overlap area (2400μm^2) is nearly equal to the channel area (2500μm^2). In contrast, Yin, *et al.* utilized FETs with W/L = 50μm/0.5μm [133] which have much smaller overall device area than the FETs in this work. In addition, their shorter channel lengths and larger W/L ratios enable larger on-currents which speed up inverter switching. By optimizing the device layout with tighter design rules, performance could be improved.

In addition, the devices and circuits in this work are fabricated at low temperature, i.e. the semiconductor channel is not annealed. Annealing has been shown to improve mobility and hence, current drive. Despite this disadvantage, we have successfully demonstrated rail-to-rail enhancement/depletion ring oscillators that operate at low power supply voltages.

The minimum supply voltage at which the RO still functions is V_{DD} = 1.7V. Fig. 4-25 shows the output transient which, although no longer rail-to-rail, clearly demonstrates oscillation with $V_{out,pp}$ = 0.9V, or approximately $V_{DD}/2$. This supply voltage is lower than any other amorphous oxide semiconductor-based RO in the literature.

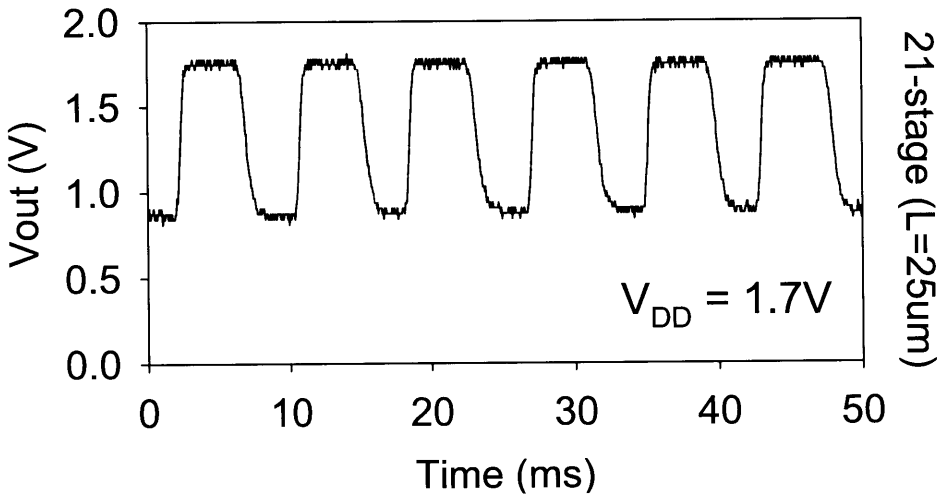

Figure 4-25: Ring oscillator output transient for a 21-stage, 25μm channel length RO (bottom) operating at V_{DD} = 1.7V. The output swing is 0.9V. Although the output voltage is no longer rail-to-rail, the supply voltage is lower than any other AOS ring oscillator in the literature.

Chapter 5

Conclusion

5.1 Summary

Amorphous metal oxide semiconductors offer the potential for higher FET performance at lower processing temperatures than amorphous silicon, the established technology for large area applications. Their room temperature deposition enables the use of unconventional temperature-sensitive substrates such as lightweight, flexible polymers and even paper, but capitalizing on this advantage requires the development of fully low temperature processes for scalable device fabrication. In this thesis we have presented a lithographic process for metal oxide FETs whose maximum temperature of ~100°C fulfills these requirements and enables the development of large area flexible applications.

Development of a new technology starts from understanding the materials. Exploratory experiments used shadow mask patterning to characterize ZnO and ZIO FETs sputtered and annealed at various conditions. Because the ZnO FETs required high annealing temperatures (300-400°C) compared to ZIO (as-deposited - 100°C), ZIO was selected as the semiconductor channel material. The mixture of indium oxide with zinc oxide produces thin films with higher mobilities without annealing which is ideal for a low temperature process. For gate dielectric we chose to use parylene, a conformal CVD polymer compatible, for its pinhole-free, low leakage films; room-temperature deposition; and compatibility with photolithographic processing. Using

the lithographic process we developed, we

- Demonstrated a hybrid inorganic-organic FET consisting of all room-temperature-deposited materials with mobilities as high as $12cm^2/Vs$, comprising
  - an amorphous oxide semiconductor (zinc indium oxide) and
  - polymer dielectric (parylene)

Electrical characterization results for the top-gate, bottom-contact FETs fabricated in the baseline lithographic process were compared for devices of varying channel lengths and widths. We found that drain current scaling with channel width and length approximately followed the conventional design rules which predict that I_D scales proportionally with W/L. Using the Silvaco simulation suite, we modeled a $100\mu m \times 100\mu m$ baseline FET by treating the amorphous oxide channel as a non-defective semiconductor. We showed that the measured I-V characteristics could be reasonably reproduced by simulating an FET with two interface trap levels with a density of $10^{11}cm^{-2}$ each. These results emphasize the importance of interface states on FET behavior.

To aid device design, we simulated the effects of several material- and process-controlled parameters. One of the most important parameters for FET circuit design is threshold voltage. To verify the trend shown in simulation, we fabricated devices with varying channel thicknesses by using partial shadow masking and

- Showed by simulation and experiment that threshold voltage can be modified by changing FET channel layer thickness i.e., without needing a second material or different doping

The availability of FETs with different threshold voltages allows the implementation of enhancement-depletion (E/D) logic circuits that have faster speeds and smaller device areas than single-V_T topologies. Our first approach to putting FETs with

different V_Ts on a single substrate, i.e., shadow masking during semiconductor deposition, limited integration and scalability. To enable the fabrication of arbitrarily complex patterns for integrated two-V_T circuits, we

- Developed a low temperature, scalable lithographic process for integrated circuits using ZIO/parylene FETs capable of integrating devices with different V_Ts for enhancement/depletion circuits

Individual FETs are the building blocks for integrated metal oxide circuits. The most basic digital circuit is an inverter, which can be implemented with two FETs. Multiple inverters can be chained together to form ring oscillators, which are often used to benchmark new materials technologies. Using the two-V_T process we developed, we

- Demonstrated E/D inverters operating at $V_{DD} = 3V$ with $A_V > 20$ and noise margins $\sim$1.2V
- Further demonstrated the first 11-stage and 21-stage E/D ring oscillators fabricated in a low temperature, fully lithographic process that operate rail-to-rail at $V_{DD} = 3V$ and maintain oscillation for V_{DD} as low as 1.7V

These results demonstrate the potential for low V_{DD} metal oxide-based integrated circuits fabricated in a low temperature budget, integrated lithographic process for large-area flexible electronics.

5.2 Suggestions for future work

A straightforward improvement for the circuits in this work would be to optimize device layout to reduce gate-source/drain overlaps and overall device size, as suggested in Chapter 4.4. In the author's opinion, however, the most pressing issues for oxide semiconductor circuits are materials-related rather than simple circuit optimizations.

Experimentally, we have observed that the electrical characteristics of our ZIO films depend primarily on the oxygen partial pressure during sputtering but also

show sensitivity to the history of the sputter target. For instance, a ZIO film sputtered in 10% O_2 following a previous deposition in 5% O_2 will show higher carrier concentrations than a ZIO film sputtered subsequently at the same oxygen concentration. While we have not performed systematic studies on the material deposition, this effect appeared to last through multiple deposition runs despite attempts to condition the target at the desired oxygen partial pressure. Is this sensitivity related to target preparation, due to inadequate control over the deposition conditions, or somehow intrinsic to sputtered oxides? As shown by phase diagrams of the In_2O_3-ZnO system, sintering temperature during sputter target preparation determines the exact compounds and crystal phases in the target. Different sintering temperatures might negatively affect the thin films deposited from the sputter target. If reproducibility is primarily hampered by inadequate control over the deposition conditions, it might be worthwhile to invest in a dedicated deposition system not shared with other materials that enables more precise control over the sputtering environment. A better understanding is needed to mitigate these issues for the reproducible fabrication of oxide FETs.

Another particular area of concern is the semiconductor-dielectric interface. In this thesis we presented FETs with an inorganic/organic active interface. Organic and inorganic materials are commonly regarded to form poor interfaces, but our work and that of a few groups using other polymer dielectrics have demonstrated that it is possible to obtain transistor behavior with these interfaces. We speculate that these results are achievable because the constituent molecules have polar groups that bind to the oxide semiconductor. Parylene-C contains chlorine atoms, which are strongly electronegative; the self-assembled nanodielectrics presented in [23] contain highly polarizable groups. In contrast, in a brief experiment to try parylene-N instead of parylene-C for ZIO FETs, we found that using the non-chlorinated version of parylene resulted in low gate leakage currents but a poor semiconductor-dielectric interface with drain-to-source currents that could not be gate-controlled.

One possible route to further exploring the impact of dielectric interface is to insert a thin oxide dielectric between the ZIO semiconductor and the parylene dielectric.

The use of parylene as the main dielectric gives greater flexibility in selecting an oxide interface layer, since the conformal polymer can fill in pinholes/voids and prevent gate current leakage. The oxide dielectric can then be chosen for its band gap offset and expected charge- or dipole-formation at the semiconductor surface. If the same trap levels appear in FETs with different dielectrics, it might also be the case that these traps states arise from dangling bonds at the surface of the oxide semiconductor itself regardless of the dielectric. Understanding and controlling the presence of interface states was an indisputably important step in the development of silicon technology, and the same is needed for metal oxide semiconductor technology.

Reproducibility is key to circuit design, which is predicated on knowing the relevant device parameter values for individual FETs fabricated in a given process. A closely related concern is FET stability and the effects of bias stress, ambient, and light. Though shifts in device performance caused by gas ambient or light can be exploited to fabricate sensors, generally such shifts are detrimental to circuit performance. For example, gate bias stress could cause threshold voltage to shift out of the designed-for range and render the circuit inoperable. This thesis does not directly address device stability, but stability is already an active area of research and researchers have suggested way to improve device stability such as encapsulation/passivation, annealing the semiconductor, or modifying film stoichiometry and/or composition.

The semiconductor is a vital component of metal oxide technology. Interactions at the semiconductor-dielectric interface determine FET performance. Future applications of the approach presented in this thesis for building oxide semiconductor-based E/D logic circuits in a low temperature, lithographic process would certainly benefit from a stronger materials understanding.

Appendix A

Detailed lithographic process flows

The following processes were run on 100mm Corning Eagle 2000 alkali-free glass wafers. Metal oxide semiconductor sputter-deposition and parylene CVD were performed in the ONELab laboratory. All other processing was performed in MTL's Technology Research Laboratory, a Class 100 fabrication facility.

A.1 Baseline lithographic process

Step	Tool	Process Parameters
CLEAN WAFERS		
Piranha clean	acidhood	Immerse in 3:1 H_2SO_4 to H_2O_2 for 10 minutes. Rinse in DI water and SRD.
SOURCE/DRAIN ELECTRODES		
Deposit ITO	sputterer (onelab)	Sputter 1000Å ITO at 50W, 4mTorr, Ar-only ambient with rotation at RT.
Photolith pattern Mask MO11-SD	coater	Spincoat 1μm Fujifilm OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm).
	prebake oven	Prebake 20min at 95°C.
	EV1 aligner	Expose 2s with mask.
	photowet-r	Develop 90s in Fujifilm OCG-934.

Etch ITO	plasmaquest	Dry etch in $CH_4/H_2/Ar$ mixture (1.7:3:4 ratio) at 80°C in 45s/60s etch/cool cycles to avoid burning resist.
Strip resist	solvent-Au	Soak in heated Microstrip (75°C) for 30min. Rinse in DI water and SRD. (Opt'l: soak in Nanostrip 2-3min, immediately prior to next step. Rinse, SRD.)
SEMICONDUCTOR		
Sputter ZIO	sputterer (onelab)	Sputter 100Å ZIO at 50W, 5mTorr, 10% O_2/Ar with rotation at RT.
Deposit parylene	parylene (onelab)	30min vapor treatment, vinyltrimethoxysilane adhesion promoter. Deposit 1000Å parylene.
Photolith pattern Mask MO11-ACT	coater prebake oven EV1 aligner photowet-r	Spincoat OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm). Prebake 20min at 95°C. Expose 2s with mask. Develop 90s in OCG-934 developer.
Etch parylene	plasmaquest	Dry etch in O_2 plasma at 25°C.
Etch ZIO	acidhood	Wet etch in 400:1 DI H_2O:HCl, 20s at RT.
Strip resist	solvent-Au	Sonicate in unheated Microstrip for 3min, soak for additional 7min. Rinse in DI water and SRD.
VIAS		
Deposit parylene	parylene (onelab)	30min vapor treatment, vinyltrimethoxysilane adhesion promoter. Deposit 1000Å parylene.

Photolith pattern Mask MO11-VIA	coater	Spincoat AZ5214 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm).
	prebake oven	Prebake 20min at 95°C.
	EV1 aligner	Expose 2s with mask.
	postbake	Bake on hotplate in oven 90s at 120°C.
	EV1 aligner	Flood expose 60s.
	photowet-r	Develop 2min in AZ422 developer.
Etch vias	plasmaquest	Dry etch parylene in O_2 plasma at 25°C.
Strip resist	solvent-Au	Sonicate in unheated Microstrip for 3min, soak for additional 7min. Rinse in DI water and SRD.
GATE METAL		
E-beam Cr/Au	ebeam-Au	Deposit 100Å Cr / 1000Å Au.
Photolith pattern Mask MO11-G	coater	Spincoat OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm).
	prebake oven	Prebake 20min at 95°C.
	EV1 aligner	Expose 2s with mask.
	photowet-r	Develop 90s in OCG-934 developer.
Etch Au	acidhood	Wet etch in 5:1 DI H_2O to Transene TFA Au etchant for ~3min.
Etch Cr	acidhood	Wet etch in 1:1 DI H_2O to CR-7 Cr etchant for ~30s. Rinse in DI water and SRD.
Strip resist	solvent-Au	Soak in unheated Microstrip for 10min. Rinse in DI water and SRD.

A.2 Two-V_T lithographic process

Though 10nm- and 30nm-thick semiconductor layers are specified in the table, other values may be substituted.

Step	Tool	Process Parameters
CLEAN WAFERS		
Piranha clean	acidhood	Immerse in 3:1 H_2SO_4 to H_2O_2 for 10 minutes. Rinse in DI water and SRD.
SOURCE/DRAIN ELECTRODES		
Deposit ITO	sputterer (onelab)	Sputter 1000Å ITO at 50W, 4mTorr, Ar-only ambient with rotation at RT.
Photolith pattern Mask MO12-SD	coater prebake oven EV1 aligner photowet-r	Spincoat 1μm OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm). Prebake 20min at 95°C. Expose 2s with mask. Develop 90s in OCG-934 developer.
Etch ITO	plasmaquest	Dry etch in $CH_4/H_2/Ar$ mixture (1.7:3:4 ratio) at 80°C in 45s/60s etch/cool cycles to avoid burning resist.
Strip resist	solvent-Au	Soak in heated Microstrip (75°C) for 30min. Rinse in DI water and SRD. (Opt'l: soak in Nanostrip 2-3min, immediately prior to next step. Rinse, SRD.)
ACTIVE LAYER 1		
Sputter ZIO	sputterer (onelab)	Sputter 100Å ZIO at 50W, 5mTorr, 10% O_2/Ar with rotation at RT.
Deposit parylene	parylene (onelab)	30min vapor treatment, vinyltrimethoxysilane adhesion promoter. Deposit 1000Å parylene.

Photolith pattern Mask MO12-ACT1	coater prebake oven EV1 aligner photowet-r	Spin OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm). Prebake 20min at 95°C. Expose 2s with mask. Develop 90s in OCG-934 developer.
Etch parylene	plasmaquest	Dry etch in O_2 plasma at 25°C.
Etch ZIO	acidhood	Wet etch in 400:1 DI H_2O:HCl, 20s at RT.
Strip resist	solvent-Au	Sonicate in unheated Microstrip for 3min, soak for additional 7min. Rinse in DI water and SRD.
ACTIVE LAYER 2		
Sputter ZIO	sputterer (onelab)	Sputter 300Å ZIO at 50W, 5mTorr, 10% O_2/Ar with rotation at RT.
Deposit parylene	parylene (onelab)	30min vapor treatment, vinyltrimethoxysilane adhesion promoter. Deposit 1000Å parylene.
Photolith pattern Mask MO12-ACT2	coater prebake oven EV1 aligner photowet-r	Spin OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm). Prebake 20min at 95°C. Expose 2s with mask. Develop 90s in OCG-934 developer.
Etch parylene	plasmaquest	Dry etch in O_2 plasma at 25°C.
Etch ZIO	acidhood	Wet etch in 400:1 DI H_2O:HCl, 20s at RT.
Strip resist	solvent-Au	Sonicate in unheated Microstrip for 3min, soak for additional 7min. Rinse in DI water and SRD.
VIAS		
Deposit parylene	parylene (onelab)	30min vapor treatment, vinyltrimethoxysilane adhesion promoter Deposit 1000Å parylene.

Photolith pattern Mask MO12-VIA	coater	Spin AZ5214 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm).
	prebake oven	Prebake 20min at 95°C.
	EV1 aligner	Expose 2s with mask.
	postbake	Bake on hotplate in oven 90s at 120°C.
	EV1 aligner	Flood expose 60s.
	photowet-r	Develop 2min in AZ422 developer.
Etch vias	plasmaquest	Dry etch parylene in O_2 plasma at 25°C.
Strip resist	solvent-Au	Sonicate in unheated Microstrip for 3min, soak for additional 7min. Rinse in DI water and SRD.
GATE METAL		
E-beam Cr/Au	ebeam-Au	Deposit 100Å Cr / 1000Å Au.
Photolith pattern Mask MO12-G	coater	Spincoat OCG-825 resist (6s spread, 500rpm; 6s, 750rpm; 30s final spin, 3000rpm).
	prebake oven	Prebake 20min at 95°C.
	EV1 aligner	Expose 2s with mask.
	photowet-r	Develop 90s in OCG-934 developer.
	bench	
Etch Au	acidhood	Wet etch in 5:1 DI H_2O to Transene TFA Au etchant for ~3min.
Etch Cr	acidhood	Wet etch in 1:1 DI H_2O to CR-7 Cr etchant for ~30s. Rinse in DI water and SRD.
Strip resist	solvent-Au	Soak in unheated Microstrip for 10min. Rinse in DI water and SRD.

Appendix B

Doping calculation from C-V

Semiconductor doping levels (N_d) can be extracted from capacitance-voltage (C-V) measurements of metal-insulator-semiconductor (MIS) capacitors. An example C-V curve for a 300μm x 300μm ZIO MIS capacitor (Fig. B-1) shows the shift from accumulation to depletion as the applied gate voltage changes from positive to negative. Since depletion width depends on doping, the C-V measurement can be used to extract N_d. For an n-type semiconductor, the depletion width x_d can be expressed as follows [98]:

$$x_d\left(V_{GB}\right) = \frac{\epsilon_s}{C_{ins}}\left[\sqrt{1+\frac{2C_{ins}^2\left(V_{FB}-V_{GB}\right)}{\epsilon_s q N_d}}-1\right]$$

where C_{ins} is the insulator capacitance ($C_{ins} = \frac{\epsilon_{ins}}{t_{ins}}$), C_s is the semiconductor capacitance ($C_s = \frac{\epsilon_s}{t_s}$), q is the electronic charge (q = 1.6x10^{-19}C), V_{GB} is the applied gate voltage, V_{FB} is the flatband voltage, ϵ_s and ϵ_{ins} are the dielectric constants of the semiconductor and insulator, respectively. With a bit of algebraic manipulation, we

can obtain a more useful expression in terms of C:

$$\frac{x_d}{\epsilon_s} = \frac{1}{C_s} = \frac{1}{C_{ins}}\left[\sqrt{1+\frac{2C_{ins}^2\left(V_{FB}-V_{GB}\right)}{\epsilon_s q N_d}}-1\right]$$

$$\frac{1}{C_s}+\frac{1}{C_{ins}} = \frac{1}{C} = \frac{1}{C_{ins}}\left[\sqrt{1+\frac{2C_{ins}^2\left(V_{FB}-V_{GB}\right)}{\epsilon_s q N_d}}-1\right]$$

Squaring this result:

$$\begin{aligned}\frac{1}{C^2} &= \frac{1}{C_{ins}}\left(1+\frac{2C_{ins}^2\left(V_{FB}-V_{GB}\right)}{\epsilon_s q N_d}\right)\\ &= \left[\frac{1}{C_{ins}^2}+\frac{2V_{FB}}{\epsilon_s q N_d}\right]-\left[\frac{2}{\epsilon_s q N_d}\right]V_{GB}\\ &= [intercept]-[slope]*V_{GB}\end{aligned}$$

with the result that N_d can be calculated as:

$$N_d = \frac{2}{\epsilon_s q[slope]}$$

Fig. B-2 shows the C-V data re-plotted as $1/C^2$ versus V_{GB}; a linear fit in the depletion region is drawn on the graph. From this data, we extracted $N_d \approx 10^{17}\text{cm}^{-3}$; this value is used for the FET simulations in Chapter 3.4.

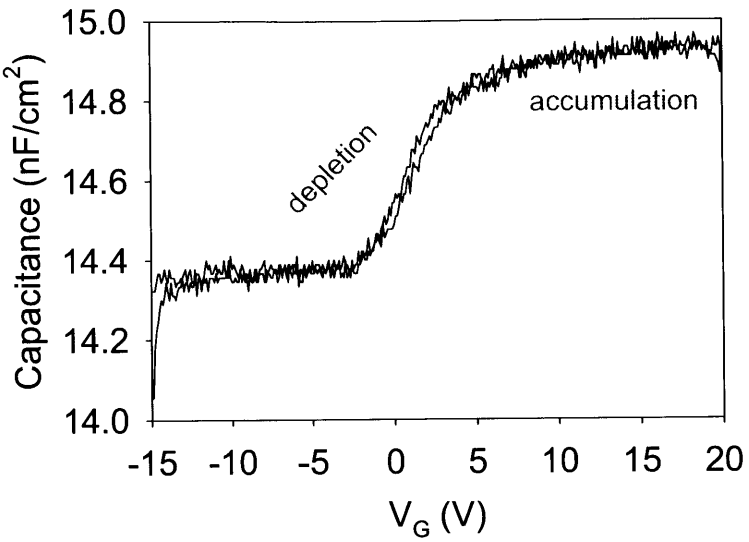

Figure B-1: Quasi-static C-V characteristic for a 300μm x 300μm MIS capacitor. The gate bias was swept from -15V to +20V and back for a doublesweep. The ZIO semiconductor was 500Åthick and the parylene dielectric ~1770Åthick.

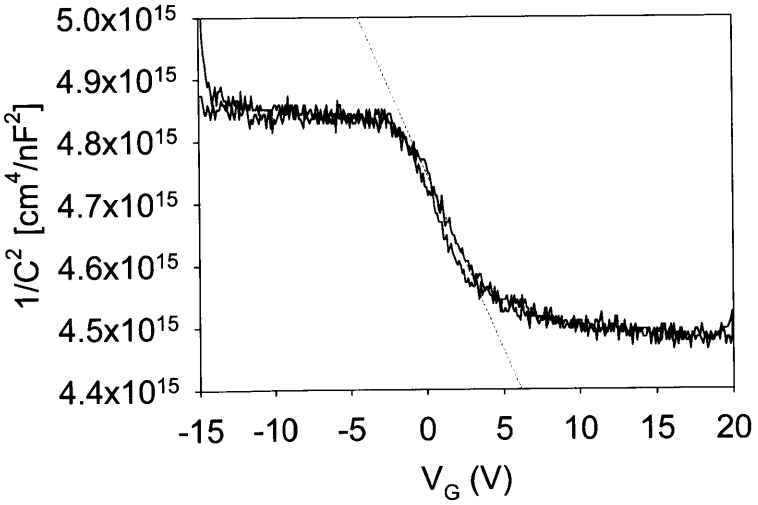

Figure B-2: The data in Fig. B-1 is re-plotted as $1/C^2$ vs V_G in order to extract the doping level, N_d.

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