Development of Gallium Nitride Power Transistors

by

Daniel Piedra

S.B., Electrical Engineering M.I.T., 2009

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

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ABSTRACT

GaN-based high-voltage transistors have outstanding properties for the development of ultra-high efficiency and compact power electronics. This thesis describes a new process technology for the fabrication of GaN power devices optimized for their use in efficient power distribution systems in computer micro-processors. An existing process flow was used to fabricate the baseline single-finger transistors and additional process steps were developed and optimized to fabricate multi-finger devices with total gate widths up to 12mm. These transistors offer the current and on-resistance levels required by future GaN-based power converters. Transistors with various gate widths were fabricated and characterized by DC and capacitance-voltage measurements to study how the main transistor metrics scale with gate width.

Acknowledgements

I would like to thank my advisor Professor Tomás Palacios for all of his help and guidance over the course of this MEng thesis and further back to my days as a UROP. I am very grateful for all of his advice and his assistance in striving to be a great researcher.

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I would like to thank the MTL staff for training and assistance with the clean room tools.

None of this would have been possible without the support of my family, for which I am very grateful.

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Chapter 1: Introduction

Section 1.1: Introduction to Power Electronics

Power electronics have become a substantial part of the semiconductor business. About ten percent of the semiconductor industry's 200 billion dollars of revenue come from power integrated circuits and power semiconductor devices. An estimated 50% of the electricity used in the world is controlled by power devices [1]. Since they have become such an integral component of the modern world, it is very important that the power semiconductor devices are very efficient. The performance of the device ultimately dictates the efficiency of the system. Furthermore, size and cost will determine the success of future power systems, so it is important to develop compact, economical solutions.

Power electronics is concerned with the control and conversion of electrical power using semiconductor switches. Applications of power electronics are widespread and encompass systems operating over a broad range of power levels, frequencies, voltage ratings and current ratings as shown in figures 1 and 2. In homes and offices, 60 Hz alternating current is converted to direct current for use in electronics such as computers and televisions [2]. Hybrid vehicles require conversion from DC from their batteries to AC to run their motors [3]. Solid state lighting requires power electronic down converters to reduce the 110V supplied voltage to the much lower voltage required by the light emitting diodes (LEDs). On the very high end of the voltage spectrum, voltages greater than 10kV are used in grid applications. Large transformers are used to step down voltages from hundreds of thousands of volts on the transmission grid to thousands of volts on the distribution grid.

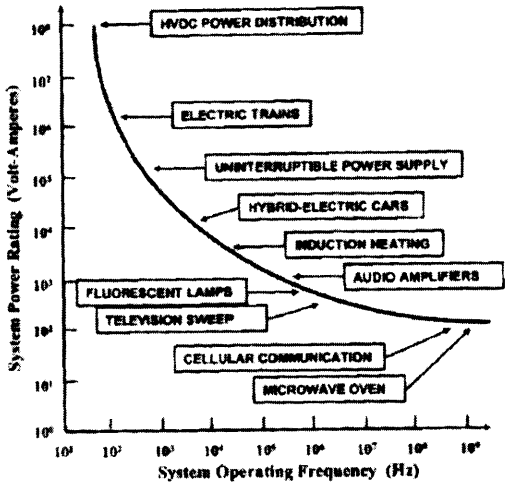


Figure 1. Applications for Power Electronics [1]

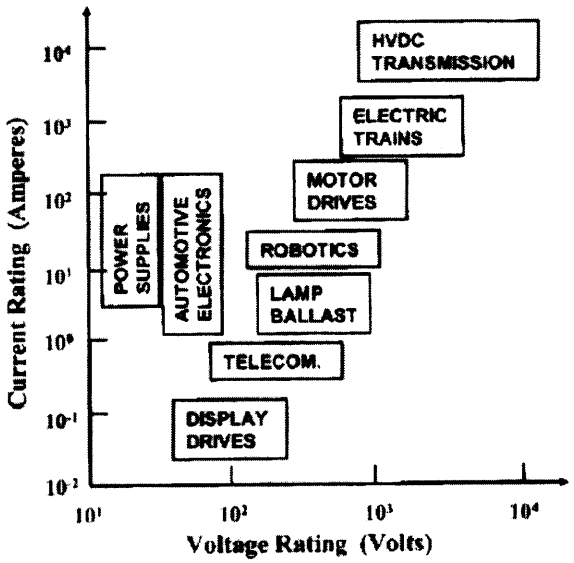


Figure 2. Voltage and Current ratings for power electronic systems [1]

One fundamental application of power electronics is DC to DC down conversion, where the output voltage is a fraction of the input voltage. This conversion scheme is widely used in electronic systems such as cellular phones, hybrid automobiles, and laptop computers which are comprised of several circuits that have lower voltage requirements than the battery supplies. For

this task, a circuit such as the one shown in figure 3 is used [4]. By controlling the switches in a periodic fashion (periodic waveform shown in figure 4), the output voltage can be "stepped down" to a fraction of the input voltage.

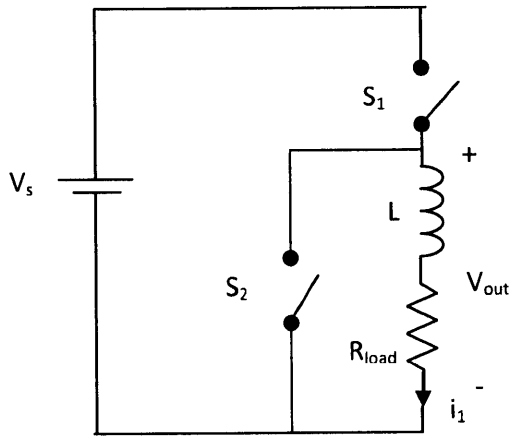


Figure 3. Basic step-down DC-DC converter.

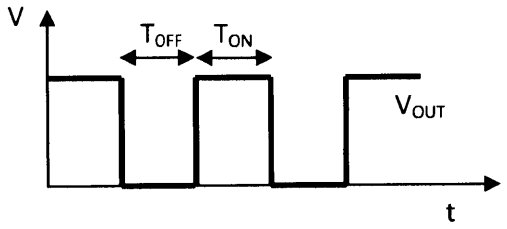


Figure 4. Load voltage waveform

During the time period T_{ON}, the switch S_1 is closed and the switch S_2 is open, thus giving the following expression for the voltage in the circuit:

$$V_S = Ri_1(t) + L\frac{di_1(t)}{dt}$$

During the time period T_{OFF}, the switch S_1 is open and S_2 is closed, causing the load voltage to become zero:

$$0 = Ri_1(t) + L\frac{di_1(t)}{dt}$$

At the completion of T_{OFF}, S_1 is closed and the cycle begins again. Thus the cycle time (and inverse fundamental frequency) is:

$$T = T_{ON} + T_{OFF} = \frac{1}{f}$$

The average voltage at the output is

$$V_{out} = \frac{1}{T}\left[\int_0^{T_{ON}} V_s\, dt + \int_{T_{ON}}^{T} 0\, dt\right] = V_s \frac{T_{ON}}{T} = V_s T_{ON} f = V_s \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_s \frac{T_{ON}}{T}$$

It is shown that by controlling the ratio $\frac{T_{ON}}{T}$, called the duty ratio D, the output voltage can be "stepped down" to a specific fraction of the input voltage. This is the basic concept employed by down converters. Operation of the circuit and thus control of the output voltage is ultimately dependent on the switches S_1 and S_2. In the early part of the 20th century, these switches were vacuum tubes, but have since then have been replaced by solid-state devices.

Section 1.2: Gallium Nitride for Power Devices

After the replacement of vacuum tubes by solid-state devices, silicon based semiconductor power devices have been dominant [1]. Considering the wide use of the switching devices, improvements are being sought. The relatively low breakdown voltage of silicon, low operating temperatures, and its high resistance open the door for a viable replacement material. A new switching technology that would improve the switching frequency, on-resistance, and maximum temperature is desirable, since these are important metrics of the switch.

Nitride semiconductors have the material characteristics to fabricate devices that would make an improved switching technology possible. The nitride family of semiconductors span a

very large bandgap range, from 0.6eV in InN to 3.4eV in GaN to 6.2eV in AlN and are well suited for many applications. In particular, gallium nitride has outstanding properties for power electronics. Originally used in optoelectronic devices, GaN has a wide bandgap, giving it a high breakdown voltage. GaN and other wide band semiconductors have the characteristic of small lattice constants, so the distance between unit cells in the crystal lattice of the material is smaller than in Si. The small lattice constant results in a strong atomic bond and thus high stability with almost 10 times improvement in critical electric field [5]. Furthermore, GaN can form heterojunctions (interfaces between materials with different bandgaps), so this semiconductor can be used in the fabrication of high electron mobility transistors (HEMTs). In HEMTs, there is a thin layer of highly mobile electrons in the channel, known as the two-dimensional electron gas (2-DEG). HEMTs have higher carrier concentrations and electron mobility than traditional transistors and are thus desirable for many applications, including power electronics (Table 1).

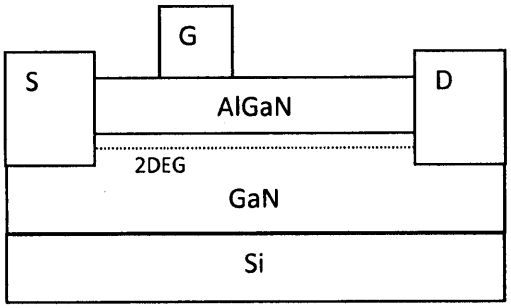


Figure 5. Diagram of an AlGaN/GaN HEMT (High Electron Mobility Transistor)

Table 1. Comparison of material properties of Si, GaN, and SiC [6]

	Si	GaN	4H-SiC
Band Gap E_g (eV)	1.1	3.39	3.26
Breakdown Electric Field E_{br} (MV/cm)	0.3	3.3	3.0
Peak drift velocity v_{sat} (10^7 cm/s)	1.0	2.5	2.0
Electron mobility μ_n (cm^2/Vs)	1350	2000 (2 dimensional electron gas)	700
Relative dielectric constant ε	11.8	9.0	10
Johnson Figure of Merit ($E_{br}\, v_{sat}/2\pi$)	1	27.5	20
Baliga's Figure of Merit ($\varepsilon\mu E_C^3$)	1	1507	548

Low on-resistance is an important characteristic for transistors used in power applications, because this will determine the power dissipated. This dissipated power is comprised of conductive power loss and switching power loss. The switching waveform shown in figure 4 exists only for ideal power switches that have on state resistance of zero. For such a device, there is no power dissipation in the transition states from on to off. Unfortunately, real power switches have some on-resistance, so the transition from on to off is not instantaneous, resulting in the waveform shown in figure 5. Devices with large on-resistance deviate greatly from the ideal power switching device and thus have more dissipated power.

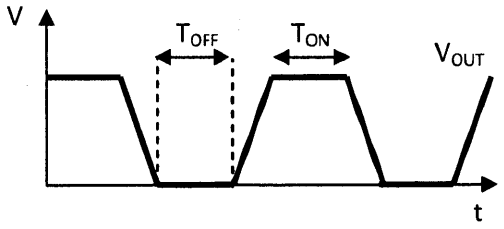


Figure 6. Typical Load voltage waveform

In general, the on-resistance in transistor devices is given by [1]:

$$R_{on} = \frac{4V_b^2}{\varepsilon_s \mu_n E_{br}^3}$$

The inverse dependence on mobility and breakdown field favors a semiconductor with high electron mobility and high breakdown field to minimize on-resistance. As seen in table 1, GaN is superior to silicon in both these respects. Figure 7 shows on-resistance as a function of breakdown voltage for GaN, Si, and SiC.

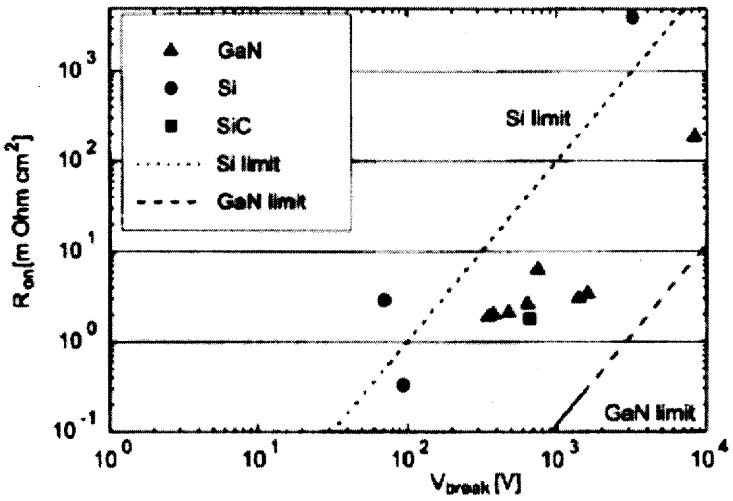


Figure 7. On-resistance as a function of breakdown voltage for switching applications [9]

Currently, GaN is grown on substrates of Si, SiC, or sapphire, as there is not yet an inexpensive method to make GaN substrates. Factors such as crystal lattice uniformity, heat conduction and cost are important in the selection of the substrate. Gallium nitride grown on silicon carbide has shown good performance due to the fact that the two compounds are well crystal lattice matched. However, GaN on SiC is very expensive, with a 100mm wafer costing up to $10,000 [3]. A more cost appealing alternative is GaN grown on Si, so this thesis is

focused on this method. Advancement of this technology is important, since gallium nitride power switches are being pursued for use in hybrid vehicles, power adapters, and power regulation systems in microprocessors.

Section 1.3: Application: Power regulation and distribution in microprocessors

In current microprocessors, low voltages are needed to reduce the energy consumption during switching. However, the low voltages at which the power is distributed limit the circuit performance and significantly increase power dissipation due to ohmic losses.

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{IV_{out}}{IV_{in}} = \frac{V_{in} - IR}{V_{in}} = 1 - \frac{IR}{V_{in}}$$

Thus, high efficiency power transmission requires high V_{in} and low current. Such a power transmission method is employed in power lines. Power is transmitted at a high voltage, low current to maximize efficiency and then the voltage is stepped down to the necessary voltage levels when needed. However, this is difficult with conventional silicon devices, which cannot simultaneously take high V_{in} and high switching frequencies due to their relatively low critical electric field. Off chip regulators are needed in this case. This causes a waste of space and input lines into the microprocessor to introduce current at the stepped down voltage. It would be more efficient to have on chip regulators. Such devices must have low on-resistance and operate at a high switching frequency and high voltage. Furthermore, the devices must be integrated with silicon chips to take advantage of the existing silicon processing infrastructure. The high switching capabilities of GaN power transistors enable the possibility of on chip converters for local conversion from 12V to low voltage (approximately 1V).

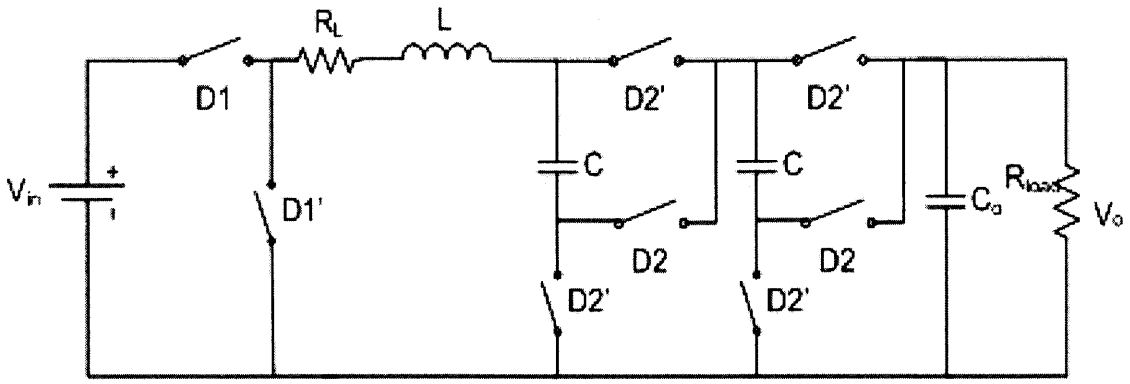


Figure 8. Step down DC to DC converter in integrated GaN/Si system. D1 and D1' are GaN transistors. D2 and D2' are Si transistors.

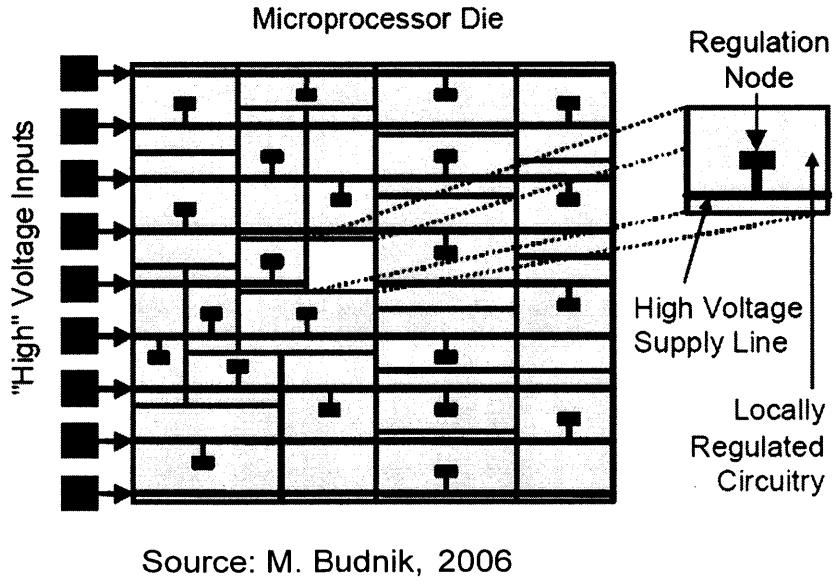


Figure 9. Proposed power distribution system in microprocessor[7]

Section 1.4: Project Goals

Power switches need to have low on-resistance to minimize dissipated power losses. At the same time, the switches need to have high breakdown voltage so that they can withstand unexpected voltage spikes and a low gate capacitance for high switching operation, which requires a small transistor footprint. The goal of this project is to develop a fabrication technology for GaN power switches that will meet these requirements. Furthermore, this project will investigate how important transistor metrics scale with device dimensions. Specifically, the multi-finger process technology developed in this project will be used to fabricate transistors with very long gate widths to examine how maximum drain current, gate leakage current, on-resistance, and gate capacitance scale with increasing gate width.

Chapter 2: Fabrication of Multi-finger Transistors

Section 2.1: Motivation for Multi-finger Technology

Large amounts of current flow through the power devices required in computer power supplies, the main application space in this thesis. To accommodate such a high current level, large transistors with very long gate widths (on the order of tens to hundreds of millimeters) are necessary.

However, transistors of such a large size, while ideal for high voltage situations, represent an obvious departure from the typical dimensions used in GaN transistors for RF amplifier applications. Circuits composed of several of these twenty-millimeter gate width transistors would be massive compared to circuits built with the 150-micron gate width counterparts. Furthermore, the gate resistance present in such a large transistor would degrade the frequency performance of the device. The ideal power transistor would combine the best of both worlds and fit a large gate width into a microscopic package. Multi-finger transistor technology could be used to fabricate micron scale gallium nitride transistors that have the advantages of long gate widths. The essence of the idea is to fabricate a linear structure with alternating separate source/drain pads. A single gate is intertwined between the separate source and drain pads, giving a structure resembling traditional transistors. This approach provides the long gate width required for power electronics, but since the gate is intertwined between the separate sources and drains (rather than laid out in a single straight line), space will be conserved. The completed multi-finger devices will have the equivalent gate width of much larger devices, but occupy a smaller area, as seen in figure 10.

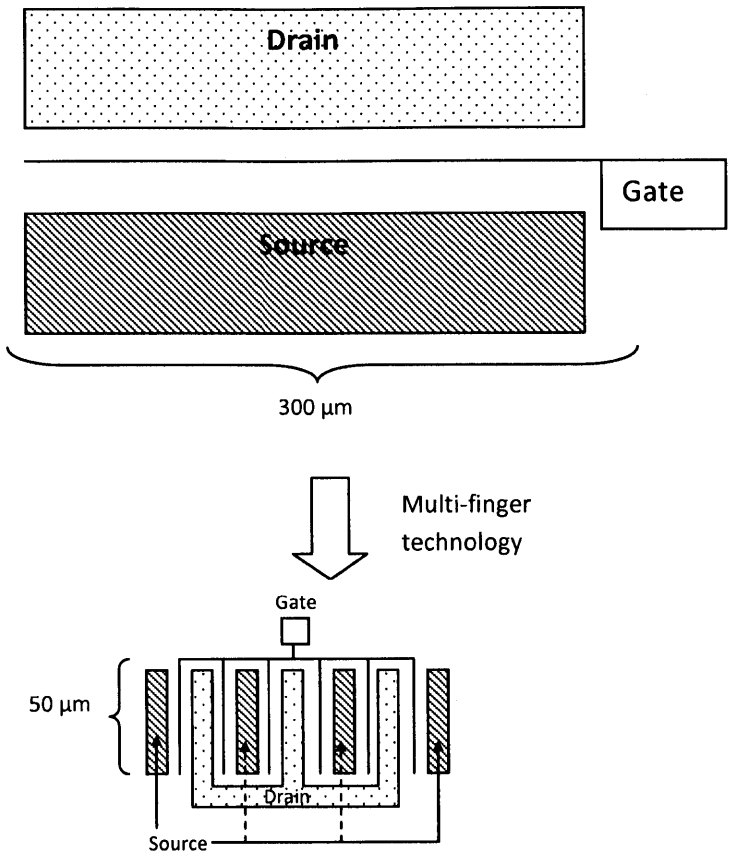


Figure 10. The Advantage of Multi-finger devices. In the figure above, the transistors have the same gate width, but the multi-finger device is more compact (6 fingers of 50µm each)

Section 2.2: Design of GaN Power Devices

To fabricate the GaN power transistors, a new photolithography mask design was developed. The new mask had conventional single-finger devices, as seen in figure 11. Single-finger devices were included in the mask to test device quality prior to any multi-finger specific processing steps. Furthermore, the transistor metrics of these devices with a W_g of only 100µm were compared against the multi-finger devices with larger gate width to examine the effects of increasing gate width.

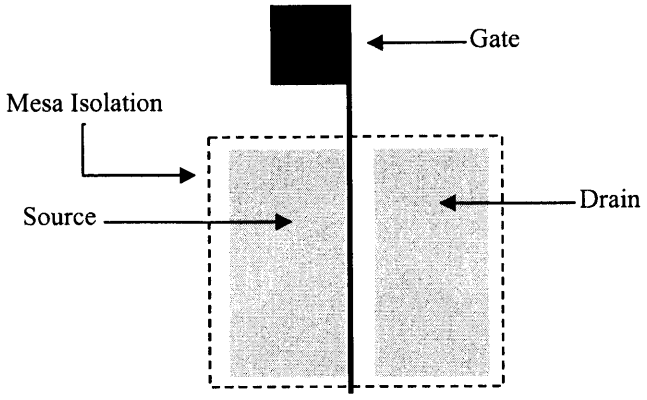


Figure 11. Single-finger transistor. W_g=100μm, L_{gd}=10 μm, L_{gs}= 1.5 μm, L_g=2 μm

Additionally, the mask included multi-finger devices. A multi-finger device on this mask is comprised of several W_g=300 μm single-finger devices with shared source, drain, and gate contacts. The total gate width of the multi-finger device can vary depending on how many single-finger devices are tied together. Figures 12 and 13 illustrate how the complete W_g=12 mm device is composed of smaller two W_g=6 mm devices, which are each composed of twenty W_g=300 μm devices. Prior to any multi-finger processing, individual W_g=300 μm devices can be measured. A dielectric is deposited and openings are etched to give access to the source contact. A metal stack is deposited across the opening to connect each single-finger device. Connecting the devices on the top half (but keeping them isolated from the bottom half) give a W_g=6 mm device. Finally connecting the top and bottom half give the complete W_g=12 mm device.

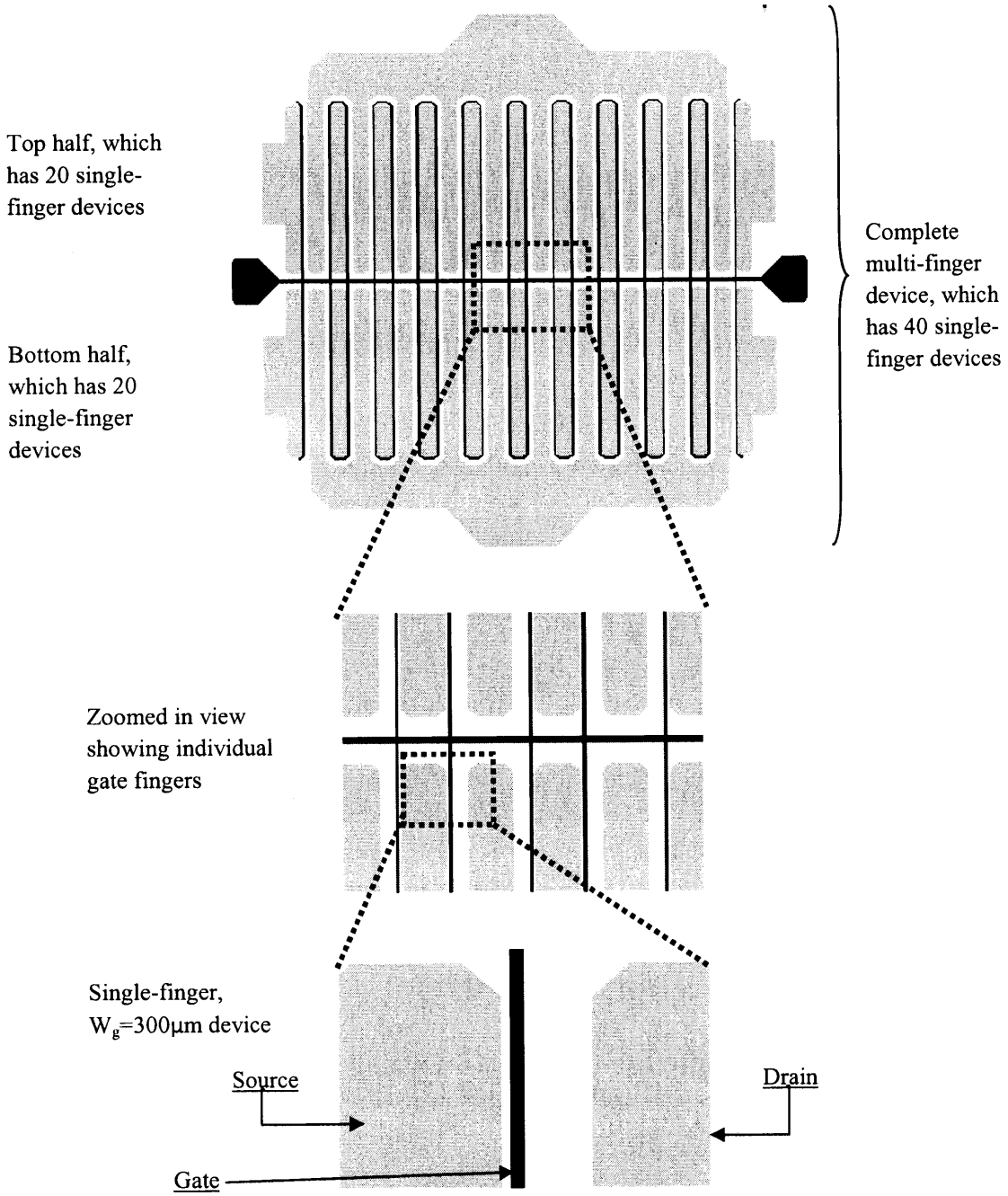


Figure 12. Prior to any multi-finger processing steps, this structure is 40 individual single-finger transistors

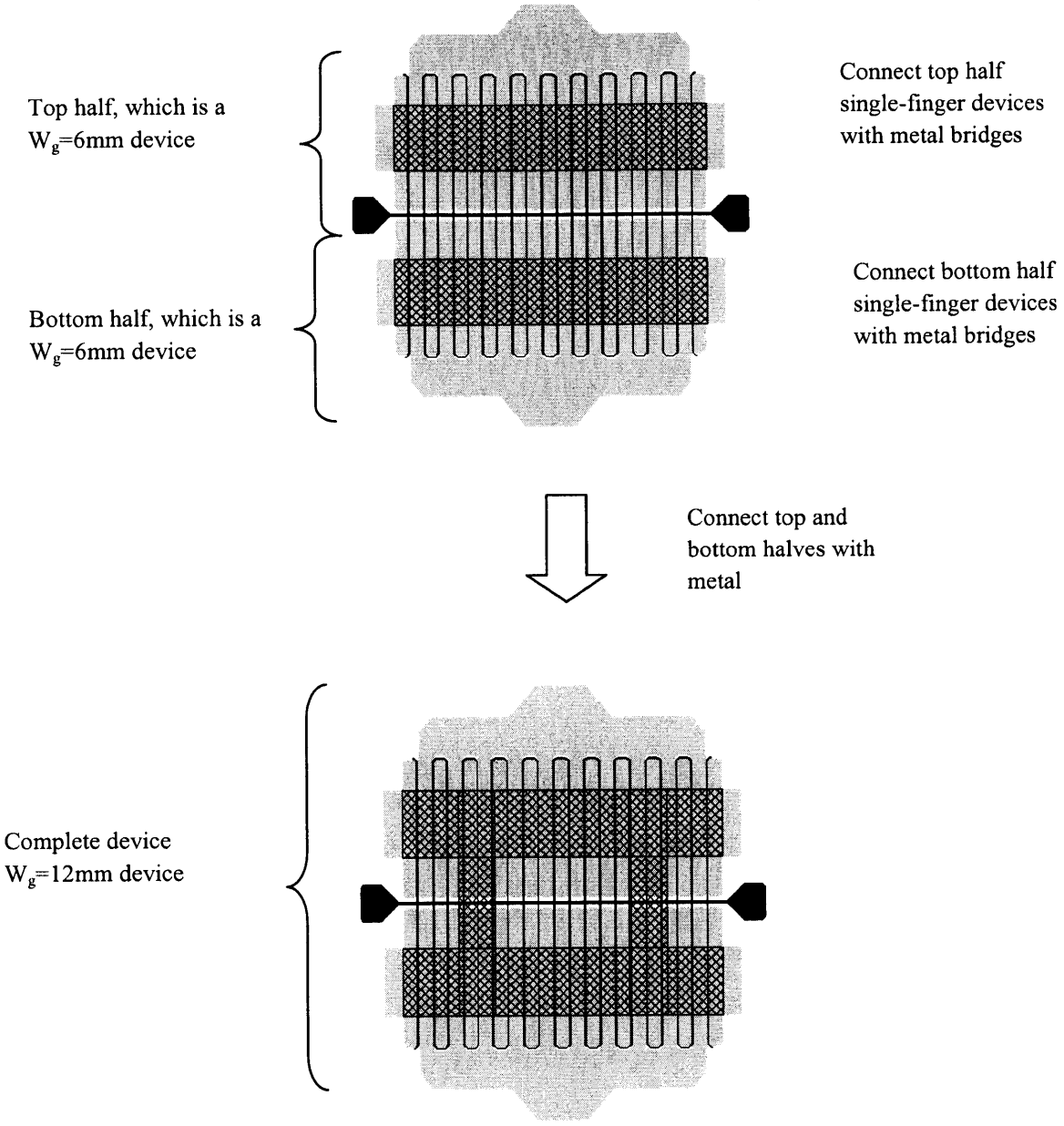


Figure 13. The complete W_g=12mm multi-finger device is composed of two W_g=6mm, which are each composed of twenty W_g=300μm devices

Section 2.3: Standard GaN High Electron Mobility Transistor (HEMT)

This chapter describes the process used to fabricate multifinger GaN High Electron Mobility Transistors. The devices were fabricated on AlGaN/GaN structures grown on Si (111) by Metalorganic Chemical Vapor Deposition (MOCVD). The AlGaN layer had an Al composition of 26% and a thickness of 17nm. The sheet resistance of the material was 439Ω/sq, as determined by TLM characterization.

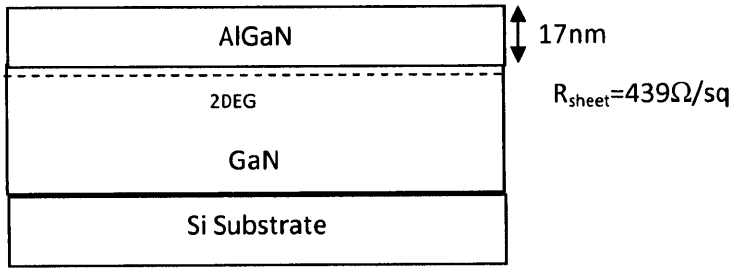


Figure 14. AlGaN/GaN on Si wafer. The AlGaN/GaN heterostructure causes 2-dimensional electron gas.

In preparation for processing, the piece was cleaned with acetone, isopropyl alcohol, and deionized water and baked on a hot plate at 130° C to evaporate all solvents.

First, mesa isolation was performed by electron cyclotron resonance (ECR) etching to electrically segregate the devices from one another. The principle is to etch away the AlGaN layer to the GaN layers, so that the heterojunction (where 2-dimensional electron gas exists) is removed and there is not unwanted current between devices. The mesa pattern was defined by spinning on OCG-825 photoresist, prebaking to cure the resist, exposing in the Karl Suss MA-6 aligner, and developing in OCG934 solution. After patterning, the sample underwent etching with the following parameters:

Table 2: Mesa Isolation Etch Parameters

	Step 1	Step 2	Step3	Step 4	Step 5	Step 6
BCl_3 (sccm)	10	10	10	20	20	20
Cl_2 (sccm)	0	0	0	5	5	5
Pressure (mTorr)	10	10	10	10	10	10
ECR (W)	0	50	100	0	50	100
RF (W)	0	15	15	0	15	25
Time (s)	30	5	60	30	5	400

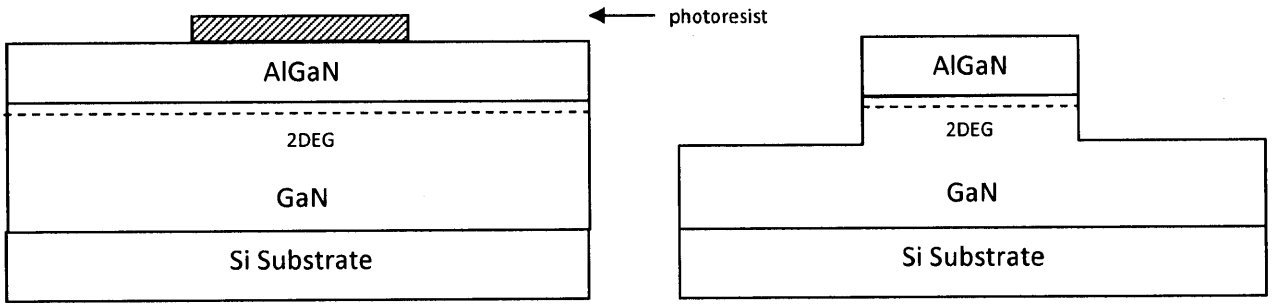


Figure 15. Mesa Isolation. After etching, area not protected by photoresist is etched away creating electrical isolation between devices by cutting off the 2DEG

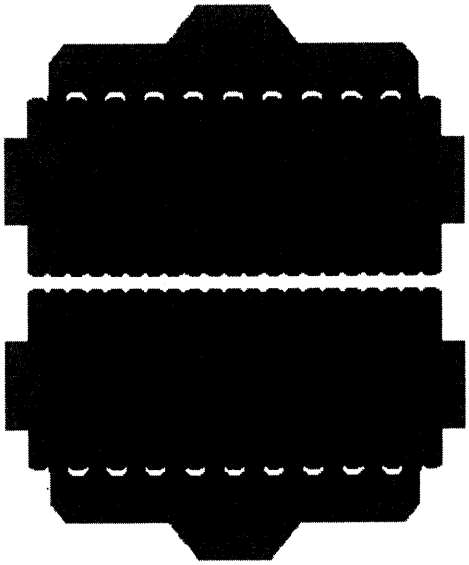


Figure 16. Top view of mesa Isolation pattern in a multi-finger transistor

Mesa isolation was done first to avoid photoresist problems caused by plasma etching. Plasma in the etcher made the OCG-825 resist insoluble to acetone, and thus very difficult to remove. Neither acetone nor heated *N*-Methyl-2-pyrrolidone (NMP) provided a reliable method of removing resist. Exposure to oxygen plasma for 15 minutes successfully removed the photoresist from the sample. However, prolonged time periods in oxygen plasma damaged any metal resulting in poor device performance. Performing mesa isolation first gives the freedom to expose to oxygen plasma since there is not yet any deposited metal on the sample.

The next step in the process was the patterning and deposition of ohmic contacts. The contacts were patterned by spin coating AZ5214 image reversal photoresist on the sample and prebaking at 80°C on a hotplate to cure the resist. An initial 8 second exposure (with the ohmic contacts mask) established the pattern on the sample and a 110° C reversal bake crosslinks the exposed areas of photoresist, making those areas inert to developer. The sample then underwent an 80 second flood exposure (without a mask), which makes all areas that are not crosslinked soluble to developer. The sample was then agitated in AZ422 developer to dissolve all soluble areas of photoresist (where ohmic contact metal will ultimately be). The metal stack of 200Å Ti, 1000 Å Al, 250Å Ni, 500 Å Au was deposited by electron beam evaporation. The sample was then placed in acetone to dissolve the underlying photoresist and liftoff the metal in all areas around the contact areas.

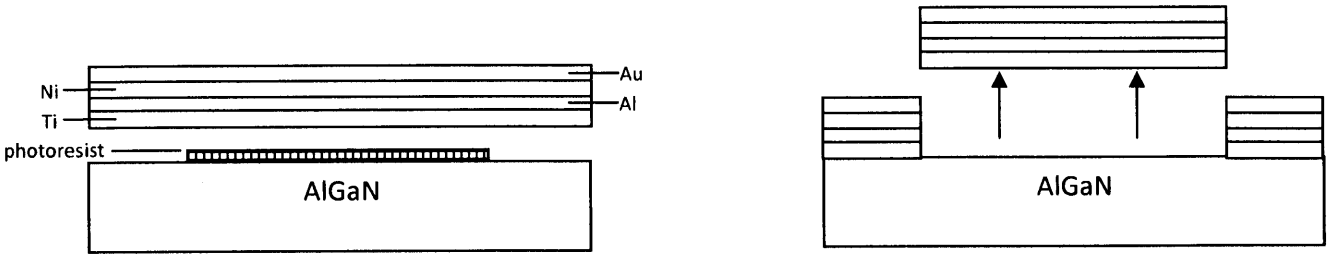


Figure 17. Liftoff of ohmic contact metals. The e-beam evaporation deposits a uniform layer of metal on the entire sample. Photoresist dissolves in acetone, lifting off metals in the regions around the contacts. Figure is not drawn to scale.

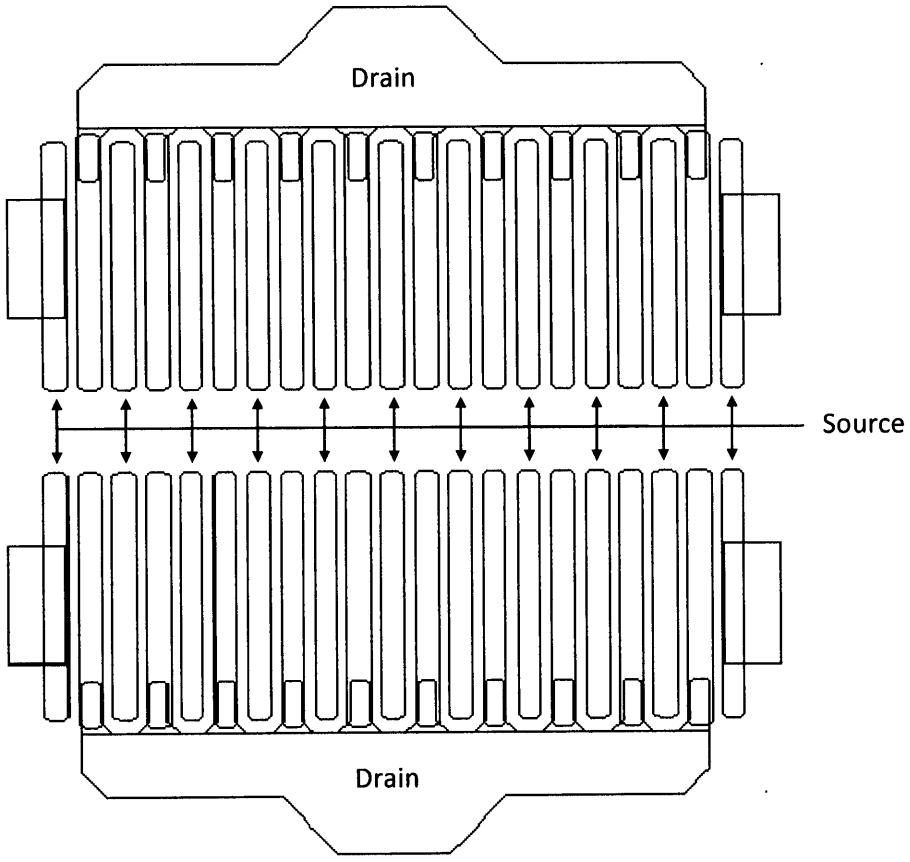


Figure 18.Ohmic contact pattern seen from above view

The sample then underwent a rapid thermal anneal at 870°C for 30 seconds in a nitrogen atmosphere. High temperature annealing caused the metal alloy to vertically diffuse into the

surface. The sample was then cleaned with acetone, isopropyl, deionized water and baked at 130° C to evaporate solvents. The resulting ohmic contacts had a contact resistance of 285Ωmm, as determined by TLM characterization.

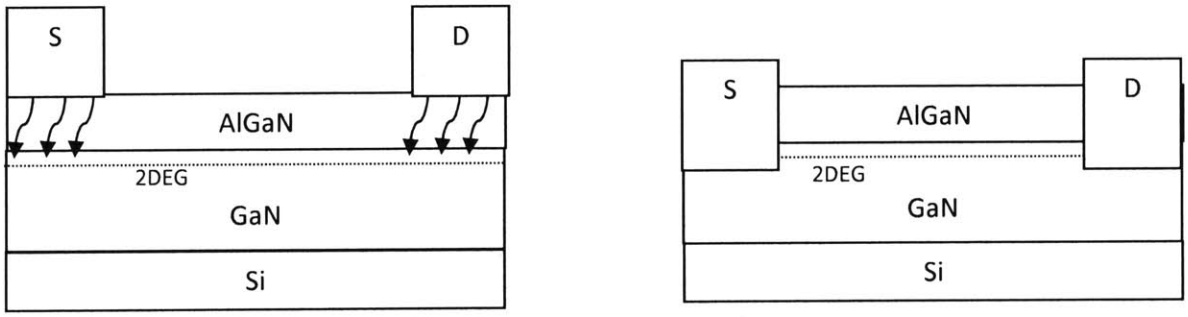


Figure 19. Rapid Thermal Annealing. During annealing, there is diffusion of ohmic metals to make contact with 2-Dimensional electron gas

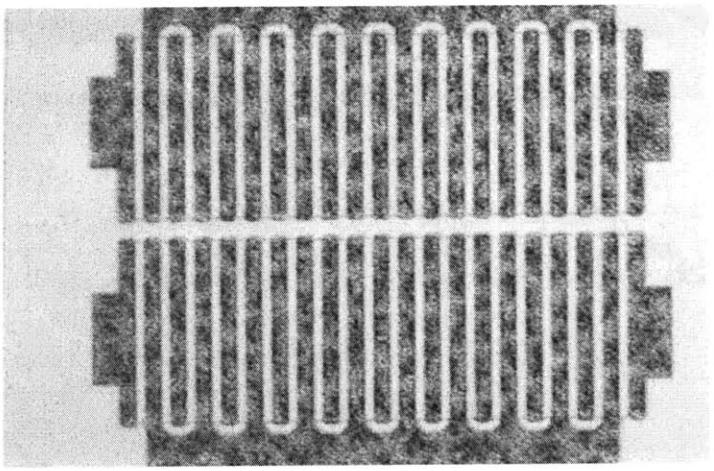


Figure 20. Micrograph of annealed ohmic contacts

Next, a 17nm layer of aluminum oxide was deposited on the sample by atomic layer deposition (ALD) to serve as a gate dielectric to minimize gate leakage current. The aluminum oxide layer also acts as a partial passivation layer. Contact pad openings were patterned using OCG825 photoresist and the aluminum oxide over these openings was etched by a dip in 7:1 buffered oxide etch (BOE) for 20 seconds.

After cleaning with acetone, isopropyl, and deionized water, the sample was ready for gate metal deposition. The same liftoff process described above was used. The gate pattern has much smaller features than the ohmic contact pattern, so it was important that the exposure time and reversal bake time and temperature were exact. Inspection under the fluoroscope was done to insure proper alignment and definition of the gate patterns. The sample was descummed in the oxygen plasma asher for 5 minutes at 1000W. A schottky metal gate stack of 300Å Ni, 2000Å Au, and 500Å Ni was deposited by electron beam evaporation. Agitation in acetone dissolved the underlying photoresist and lifted off the metal in all areas around the gates.

This concludes the process for fabricating standard GaN High Electon Mobility Transistors.

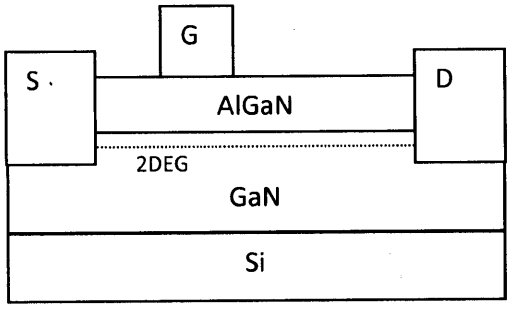


Figure 21.Gate contact

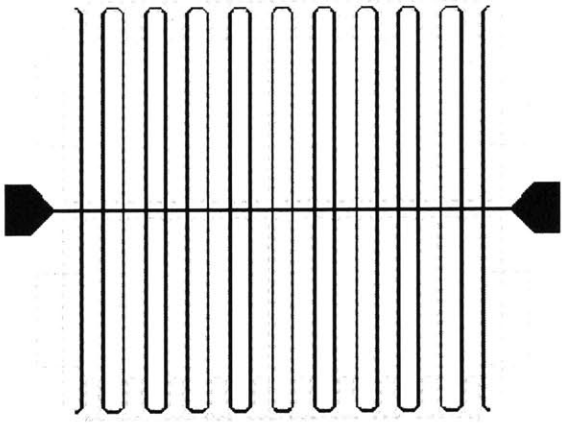


Figure 22.Gate metal pattern seen from above view

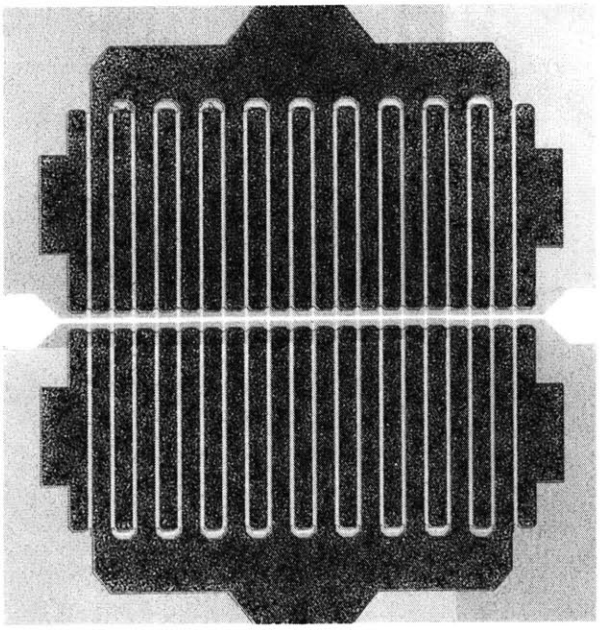


Figure 23. GaN transistors prior to multi-finger processing

Section 2.4: Multi-finger Process

The sample was cleaned with acetone, isopropyl, and deionized water and baked at 130°C to evaporate solvents to prepare the surface for coating. AP3000 solution was spun on the sample at 500rpm for 5 seconds to spread, then 2000rpm for 30 seconds. AP3000 is a silane based adhesion promoter which enhances the interfacial adhesion of BCB to inorganic surfaces, which is otherwise poor [8]. Next, BCB was dispensed on the sample and spun on at 500rpm for 5 seconds to spread, then 1500 rpm for 60 seconds for a target thickness of 2 microns. T1100 rinse solution was lightly swabbed on the backside and edges of the piece to remove excessive BCB. The coated piece was prebaked at 110° C to remove solvents and stabilize the film. The sample was then placed in an oven with nitrogen atmosphere at 250°C for one hour to cure the BCB.

At this point in the process, the entire sample was coated with BCB and openings had to be patterned and etched to access the metal contacts. Two different masking techniques were tested: a chromium hard mask and a photoresist soft mask.

AZ4620 thick photoresist was dispensed and spun at 1500rpm for 9 seconds to spread, 4000rpm for 60 seconds, and 5000rpm for 10 seconds to remove edge bead. The sample was then placed in a pre-bake oven at 95°C for 10 minutes to cure the resist, exposed in the Karl Suss aligner, and developed in AZ400 to remove the photoresist above the areas that needed to be opened. The resist acted as a soft mask (sacrificial layer) in the etching process.

A chromium hard mask was deposited on another sample. A 750Å layer of Cr deposited by electron beam evaporation and patterned by the same liftoff process described above.

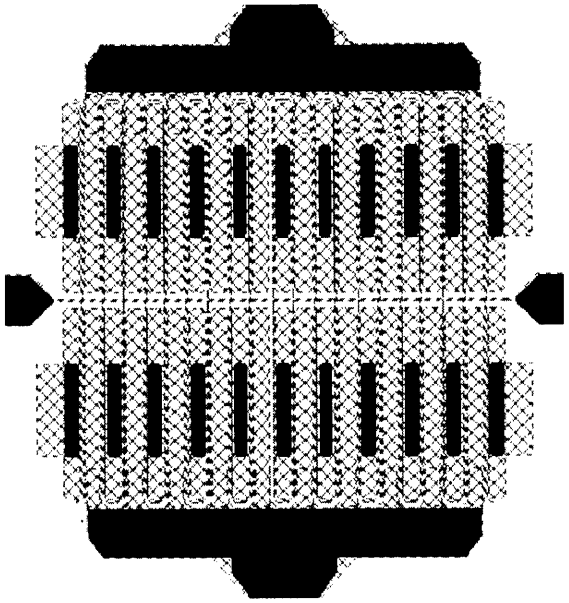


Figure 24. Openings pattern shown in black, with underlying metals shown in cross pattern.

Prior to etching the sample, work was done to determine the etch rate of BCB with a given etch chemistry and power. A dummy silicon piece was prepared by spinning on BCB as described in the preceding paragraph. ECR etching was performed on the silicon dummy piece. The etch conditions are shown in the table below.

Table 3. BCB etch conditions

	Step 1	Step 2	Step3
O_2 (sccm)	40	40	40
CF_4 (sccm)	5	5	5
Pressure (mTorr)	10	10	10
ECR (W)	0	15	100
RF (W)	0	30	30
Time (s)	30	5	vary

The piece was etched for three different times and the thickness of the BCB layer after each etch was measured using a spectroscopic reflectometry tool, the Nanometrics Nanospec. The results are shown in figure 25 below. From this data, the etch rate of BCB in O_2/CF_4 was extrapolated. With this etch rate, it was determined that 21 minutes of etching would remove the approximate 2 micron thick layer of BCB on the sample.

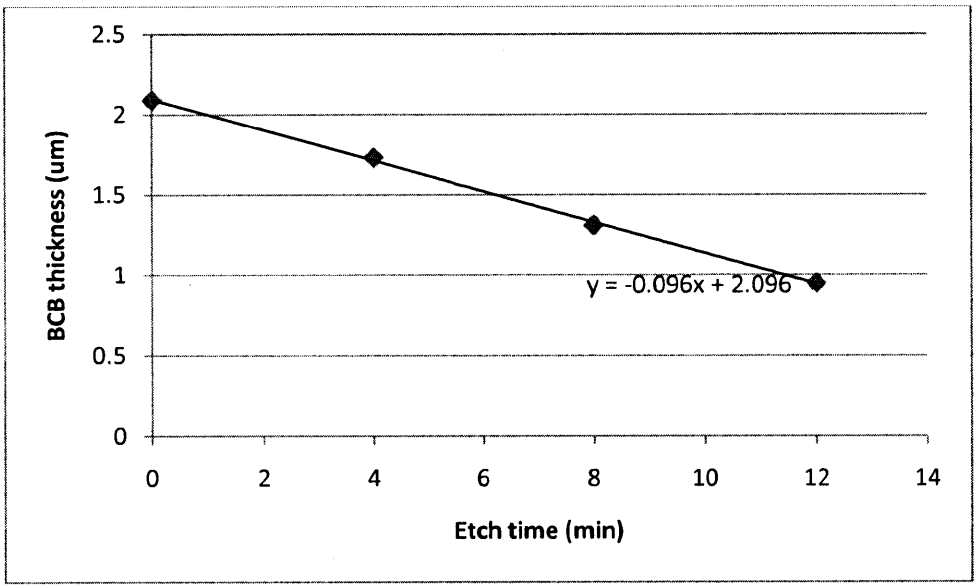


Figure 25. Etch rate of BCB in CF_4/O_2 plasma = 0.096 micron/minute

The GaN samples with transistors were etched for the necessary time to remove the BCB not shielded by a masking material, thus creating openings to the metal contacts. Agitation in acetone removed the remaining photoresist on the sample with the soft mask, and a 30 second immersion in Cr etchant removed the remaining chromium on the sample with the hard mask.

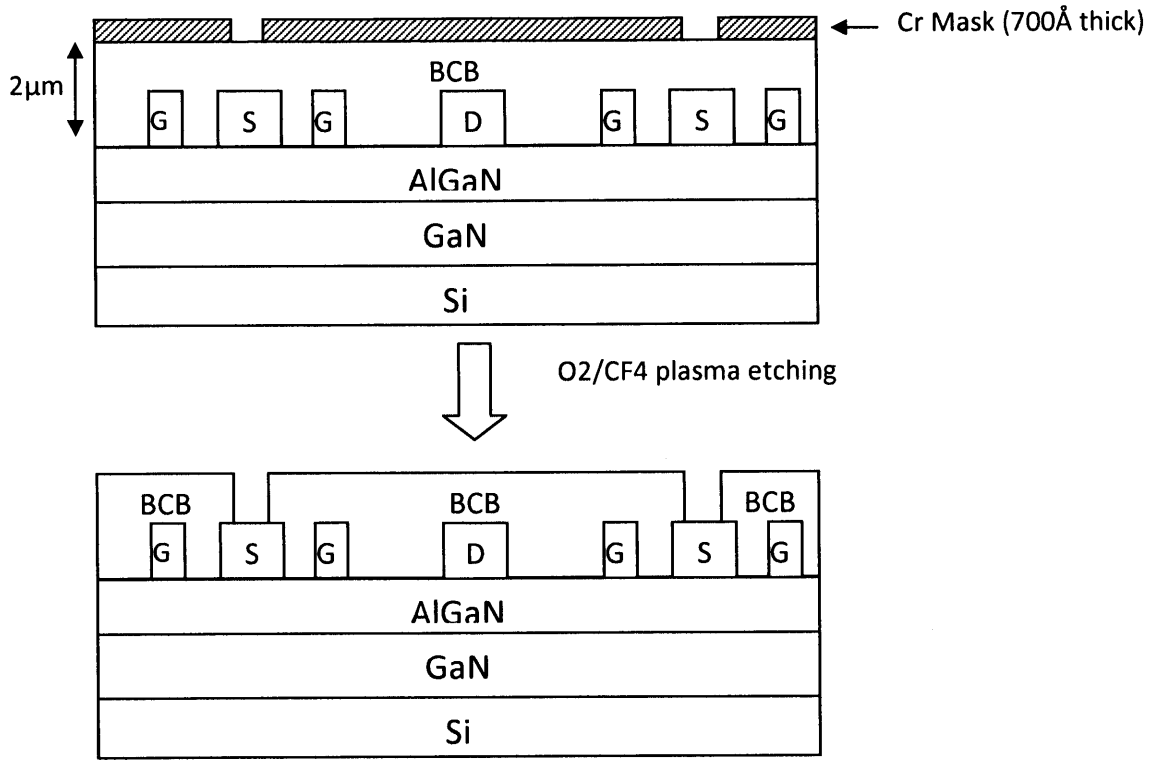


Figure 26. BCB Etching. Areas above the source contacts not covered by masking material are etched.

Different results occurred from the different masks. Figures 27 and 28 below illustrate the differences. In these micrographs the source openings have been coated with gold (as required to connect the separate sources). The openings etched with photoresist mask had poor definition and uniformity. As seen in figure 27, the openings have a round shape and the features on the left of the figure are much more etch than the features on the right.

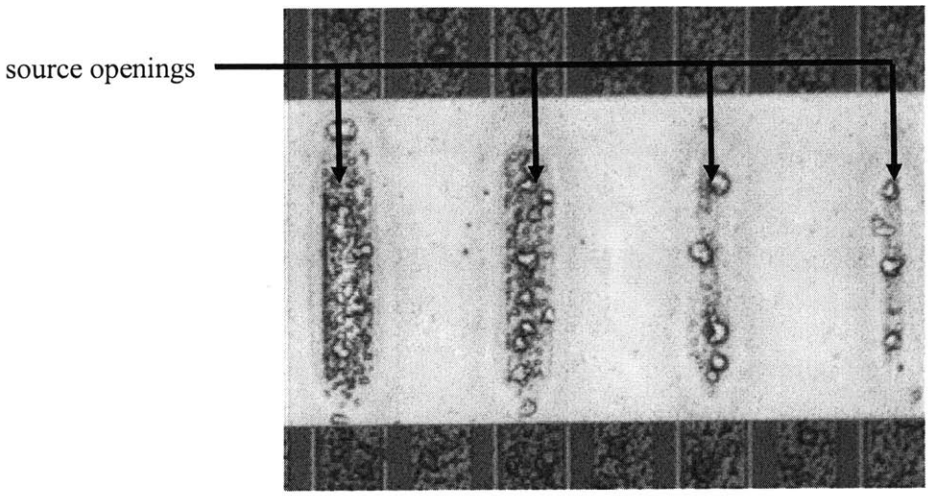


Figure 27. Etched source openings with photoresist mask.

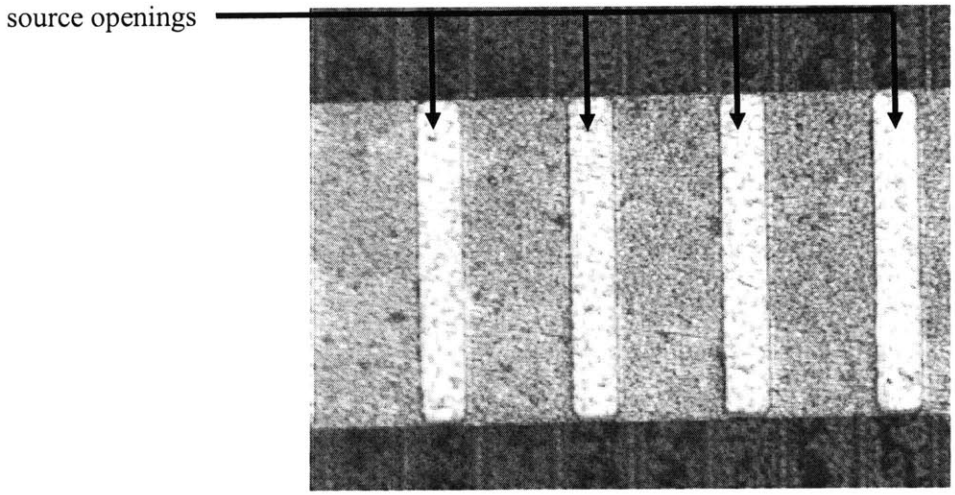


Figure 28. Etched source openings with Cr mask.

The differences in quality of etch definition of the openings can be explained by a fabrication effect called the aspect ratio dependent etching (ARDE) lag. Variations in the size of the pattern opening will cause variations in the etch rate of the specific material. Specifically, larger features (having smaller depth to width aspect ratios) will etch faster than smaller features (having larger depth to width aspect ratios).

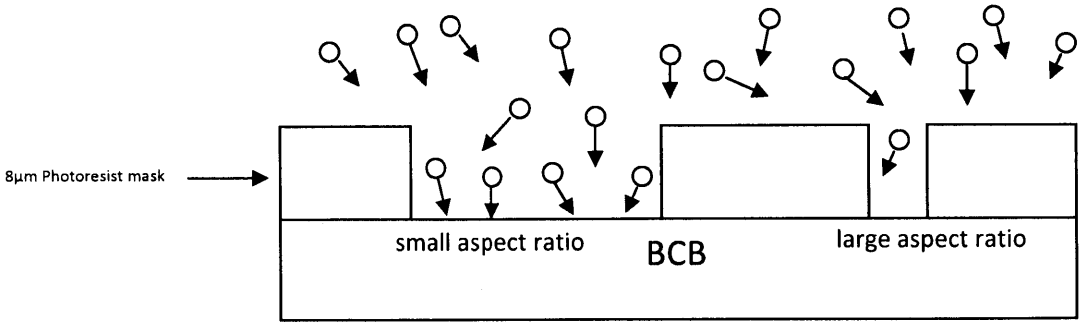


Figure 29. Thicker masking layer results in blocking of etching species in the smaller openings. This results in a non-uniform etch

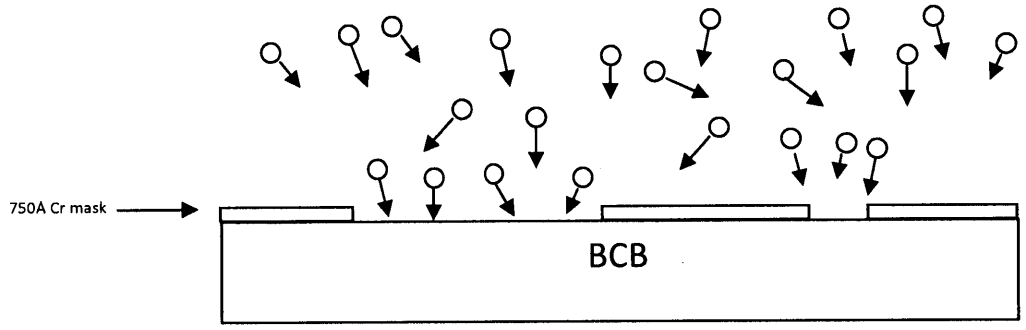


Figure 30. Thinner masking layer results in less blocking of etching species in the smaller openings. There is a small aspect ratio for all features, resulting in a uniform etch.

Etch resistance of Cr in BCB etch chemistry is much better and thus a thinner layer will suffice and there ARDE lag will not be as drastic, meaning that the piece can be etched more uniformly. It was thus decided that the thin Cr mask was the better option and subsequent devices were processed using this hard mask.

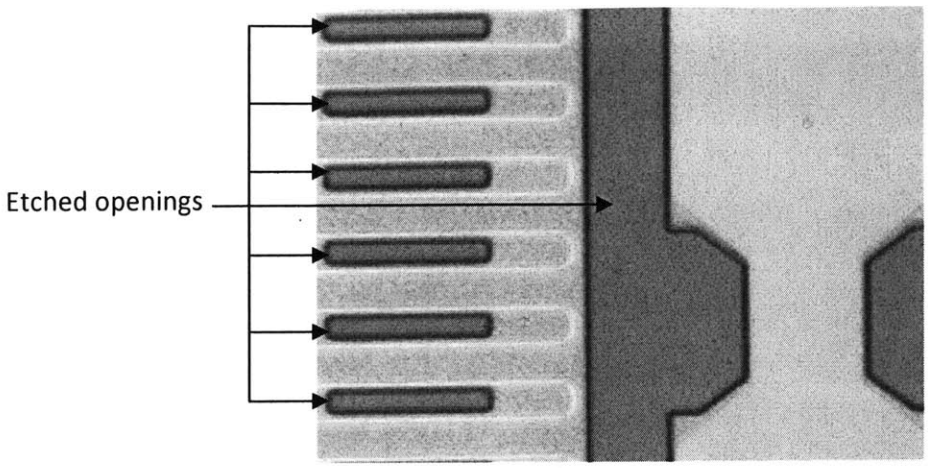


Figure 31. Micrograph of BCB etched piece

The next step in the process was the patterning and deposition of the bridge metals to connect the source contacts. The bridges were patterned by spin coating AZ5214 image reversal photoresist on the sample and prebaking at 80°C on a hotplate to cure the resist. The sample underwent an initial 8 second exposure (with mask) and was then baked at 110° C. The sample then underwent an 80 second flood exposure (without a mask) and was agitated in AZ422 developer. The metal stack of 500Å Ti, 5000 Å Au, 550Å Ni was deposited by electron beam evaporation. The sample was then placed in acetone to dissolve the underlying photoresist and liftoff the metal in all areas around the contact areas.

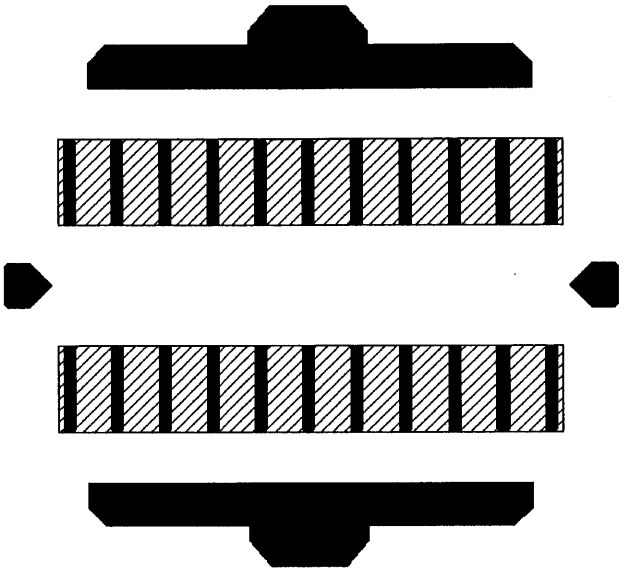


Figure 32. Deposited metal shown in the diagonal lined pattern and the openings to BCB shown in black.

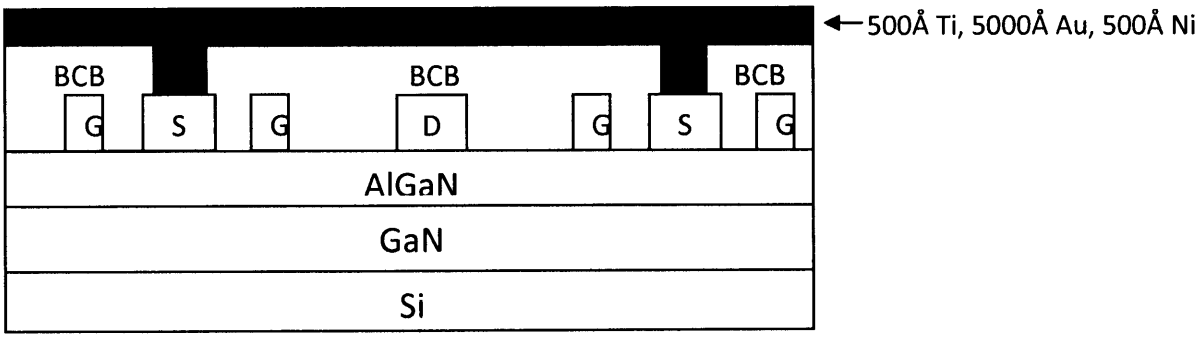


Figure 33. Metallization to connect the source pads

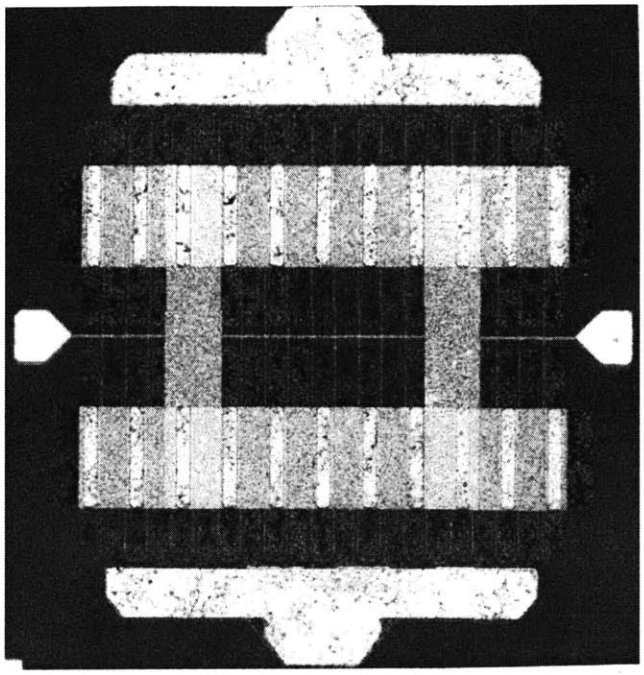


Figure 34. Multi-finger transistor.

Devices fabricated up to this step underwent initial IV characterization, but the transistors exhibited a problem at drain voltages of about 9V-10V and drain currents approaching 1A. Dark spots appeared in the drain contact (as seen in figure 35) and the drain current was greatly reduced. To correct this problem, associated with the high resistance of a relatively thin metal layer, an additional layer of metal (200Å Ti, 1kÅ Au) was deposited on the contact pads and patterned by the liftoff technique described above.

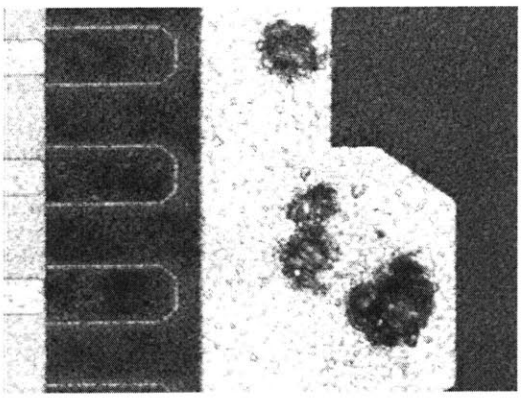


Figure 35. Damaged drain contact pad

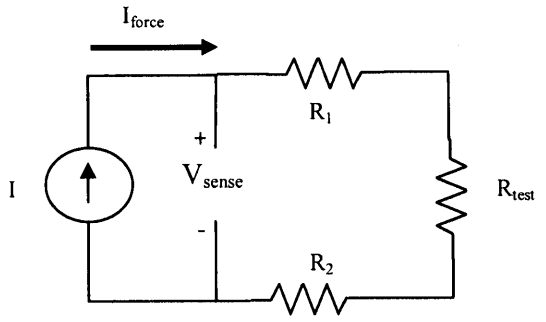
Chapter 3: Device Characterization

This chapter describes the device characterization procedures and results from the fabricated devices described above. Direct current-voltage (IV) and capacitance measurements were taken from several devices varying in gate width (other dimensions constant) to study how several device parameters scale.

Section 3.1: Direct Current IV Measurements

Measurements of I_{ds}-V_{ds} characteristics were taken using an Agilent 4155C Semiconductor Parameter Analyzer. This parameter analyzer is constrained by a built-in current compliance limit of 100mA, so it was used in conjunction with the Agilent 41501B SMU and Pulse Generator Expander to get the current compliance limit up to 1A.

For the large current anticipated from these devices, it was expected that the probe resistances would not be negligible. To limit the effect of the probe resistances, the 4-probe Kelvin measurement technique was used [10]. For this type of measurement, two of the probes are dedicated to source and sink current, while the other two are used to measure voltage. The probes being used to measure voltage draw no current and thus there is no resistive voltage drop in the measurement lines to invalidate the voltage measurement. Figure 37 illustrates this concept.

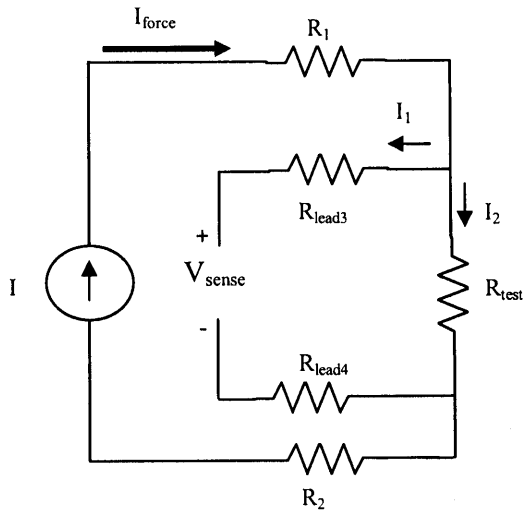


$R_1=R_{lead1}+R_{contact1}$

$R_2=R_{lead2}+R_{contact2}$

$V_{sense}=I_{force}*(R_1+R_2+R_{test})$

Figure 36. 2 probe measurement. The measured voltage V_{sense} is not accurate as it is influenced by the lead and contact resistances



$R_1=R_{lead1}+R_{contact1}$

$R_2=R_{lead2}+R_{contact2}$

$V_{sense}=I_1 R_{lead3}+ I_1R_{lead3}+I_2R_{test}$

$I_1 = 0$, $I_{force}=I_2$,

so that $V_{sense}=I_{force}*R_{test}$

Figure 37. 4 probe Kelvin measurement. A much more accurate measurement as the V_{sense} should only measure voltage across the test structure.

Figure 38 is an optical micrograph showing how the 4-probe Kelvin measurement method was used on the multi-finger GaN devices fabricated in this thesis.

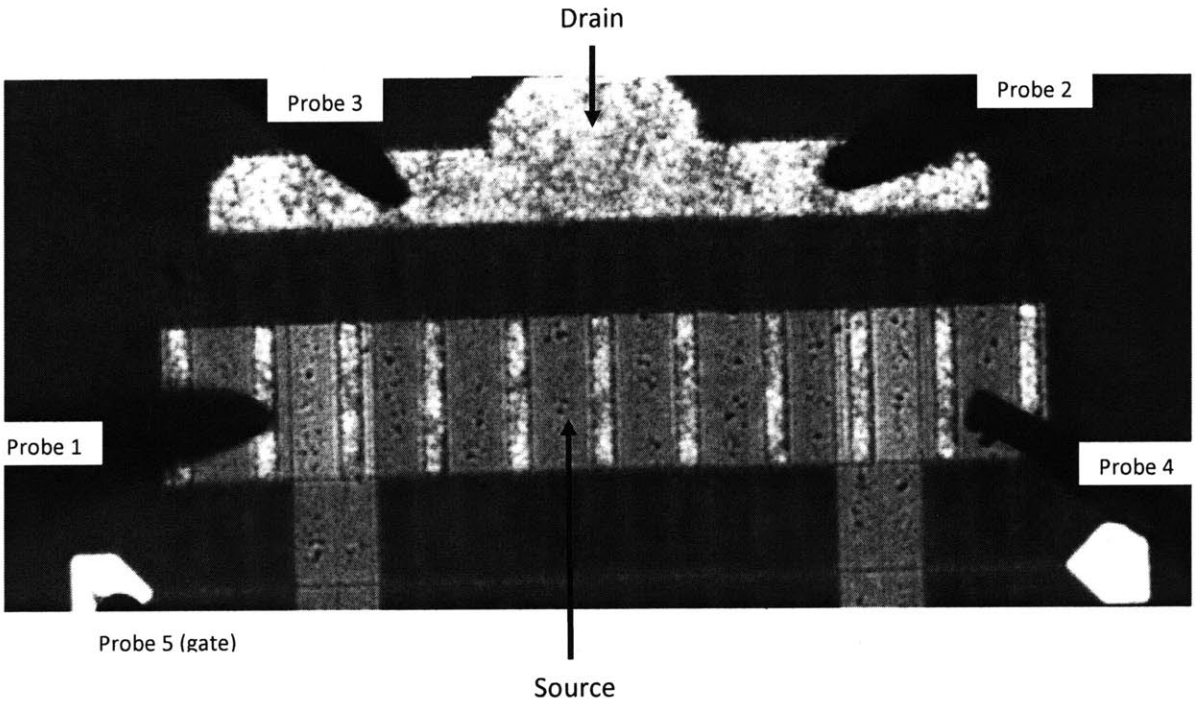


Figure 38. Probe 1 was set to ground, probe 2 was set to have variable voltage, and Id was I_2. Defined Vds as V_3-V_4, so probes 3 and 4 drive no current, they only measure the voltage difference

Using the 4-probe Kelvin measurement, the following IV measurements were taken:

W_g=100μm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

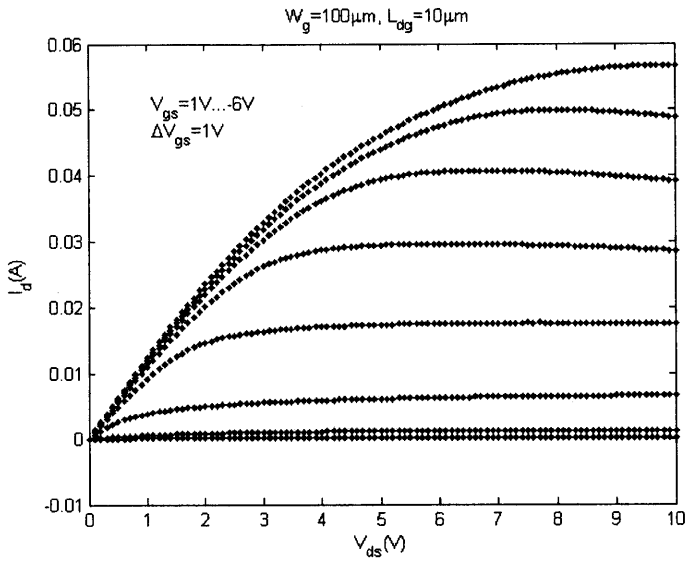


Figure 39. Id-Vds characteristics of device with gate width of 100μm. I_{dmax} = .056A

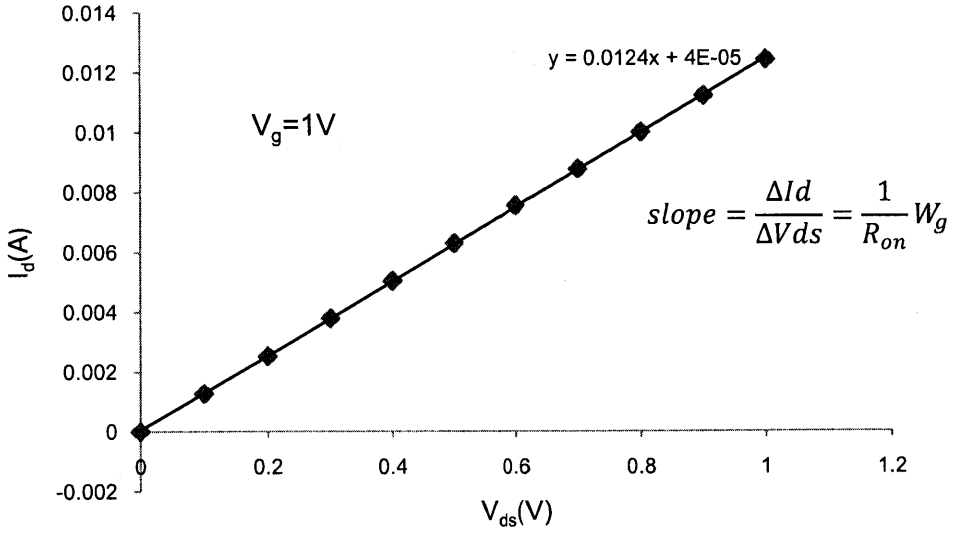


Figure 40. Close up segment of Id-Vds curve, illustrating the on-resistance, slope=0.0124A/V

The slope of the line in figure 40 represents the change in I_d over the change in V_{ds} in the linear (triode) region. This slope is the inverse of the on-resistance times the gate width. Thus, the on-resistance, R_{on}, is calculated by taking the inverse of the slope of the line times the gate width

$$R_{on} = \frac{1}{slope} * W_g = \frac{1}{0.0124A/V} * .100mm = 80.6\Omega * .100mm = 8.06\Omega mm$$

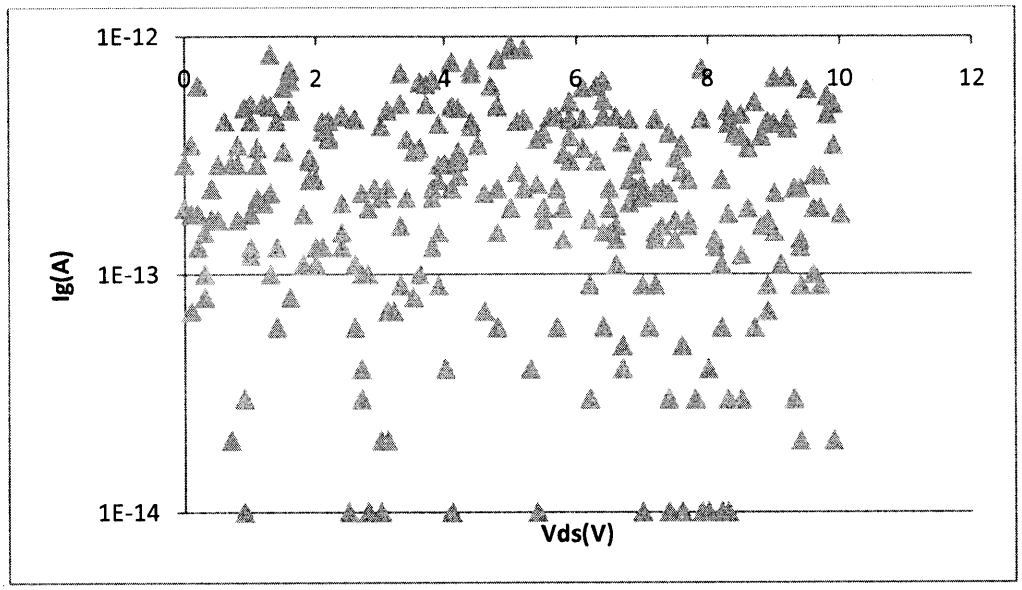


Figure 41.Ig-Vds (gate leakage current) measurements (Vg=1V to -6).
I_{gmax}=9.1x10^{-13}A

Wg=300μm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

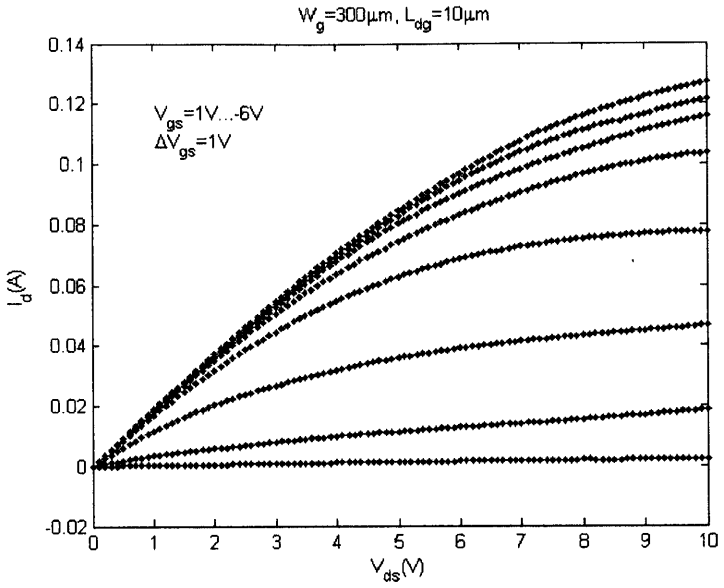


Figure 42. Id-Vds characteristics of device with gate width of 300μm. I_{dmax} =.127A

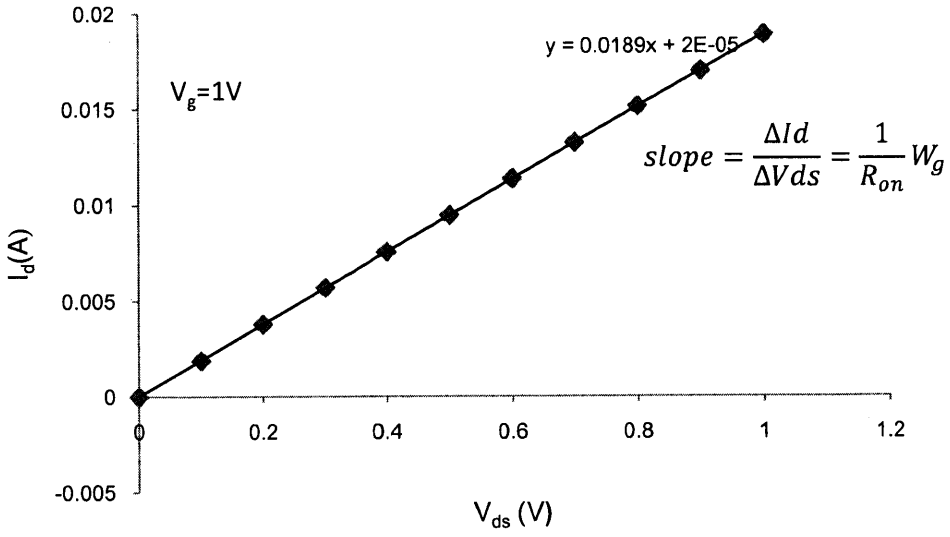


Figure 43. Close up segment of Id-Vds curve, illustrating the on-resistance, slope=.0189A/V

$$R_{on} = \frac{1}{slope} * W_g = \frac{1}{0.0189A/V} * .300mm = 52.9\Omega * .300mm = 15.87\Omega mm$$

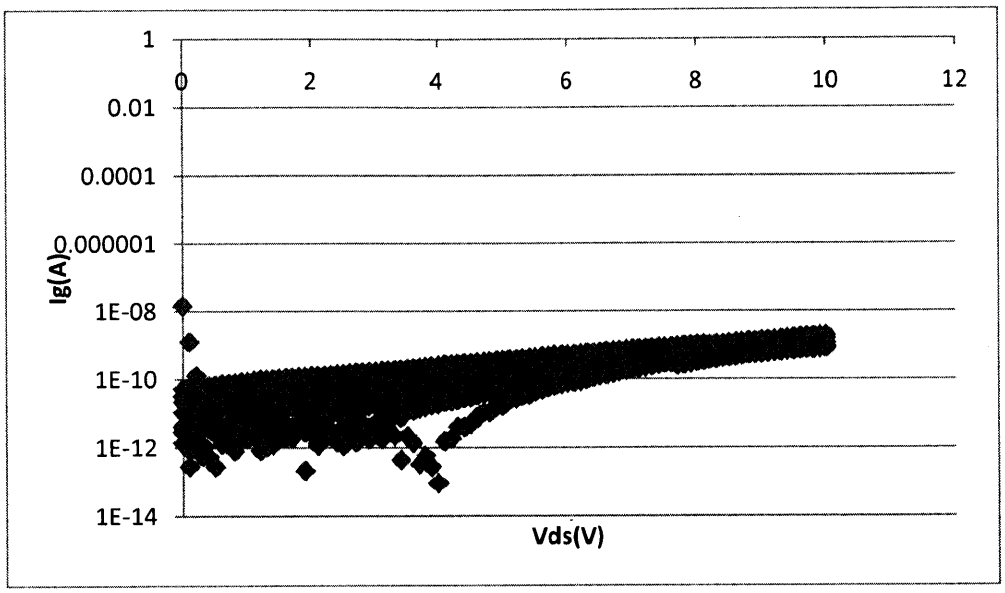


Figure 44. Ig-Vds (gate leakage current) measurements (Vg=1V to -6). Igmax=1.48x10^{-8}A

Wg=600micron, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

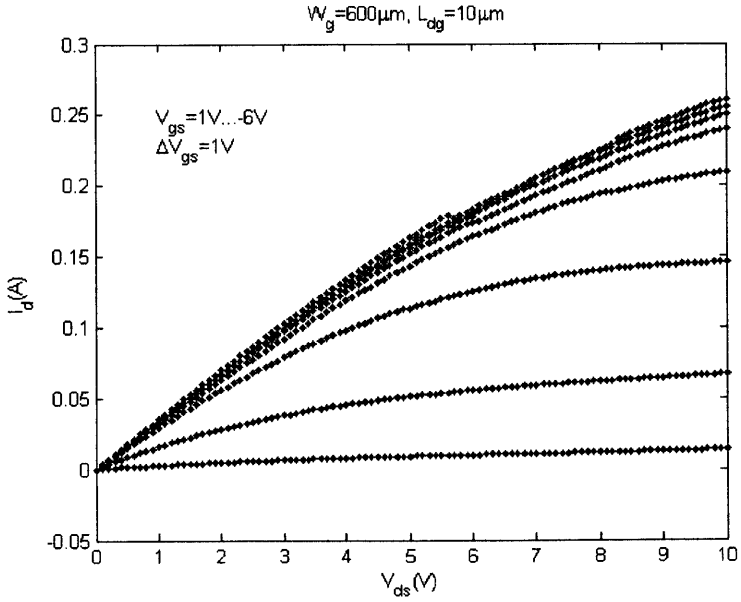


Figure 45. Id-Vds characteristics of device with gate width of 600μm. I_{dmax}=.260A

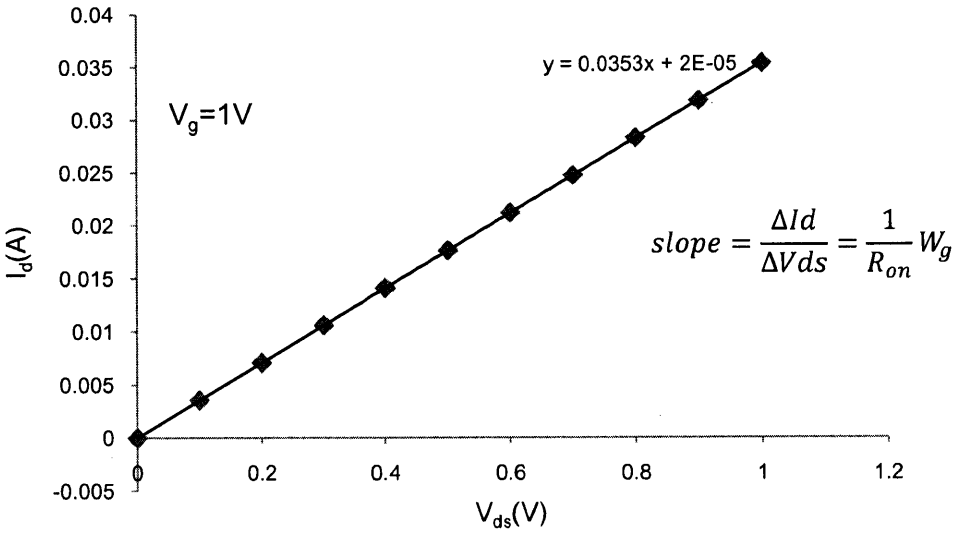


Figure 46. Close up segment of Id-Vds curve, illustrating the on-resistance, slope=0.0353A/V

$$R_{on} = \frac{1}{slope} * W_g = \frac{1}{0.0353A/V} * .600mm = 28.32\Omega * .600mm = 16.99\Omega mm$$

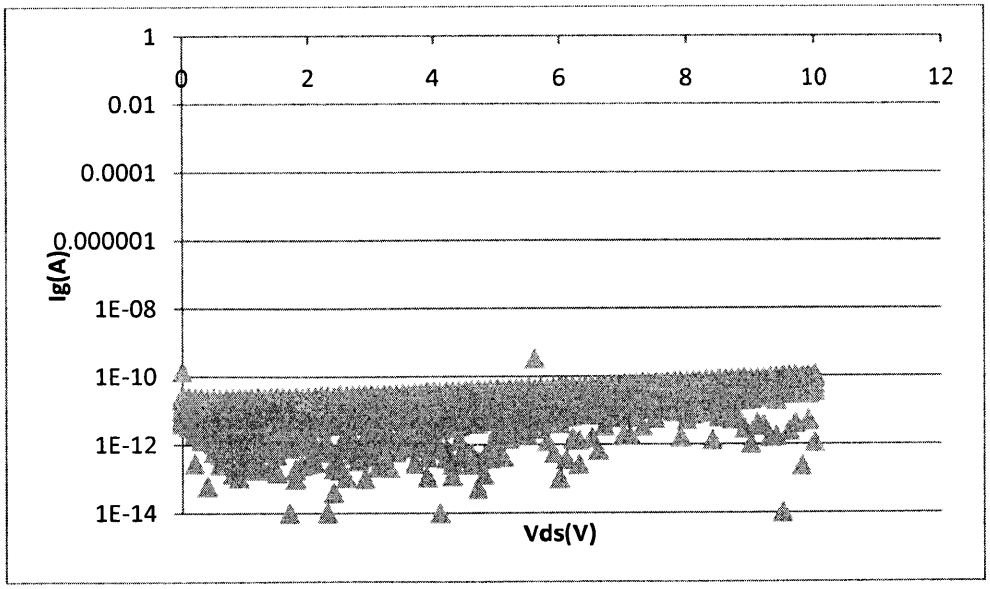


Figure 47. Ig-Vds (gate leakage current) measurements (Vg=1V to -6). Igmax=3.349×10^{-10}

W_g=6mm , L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

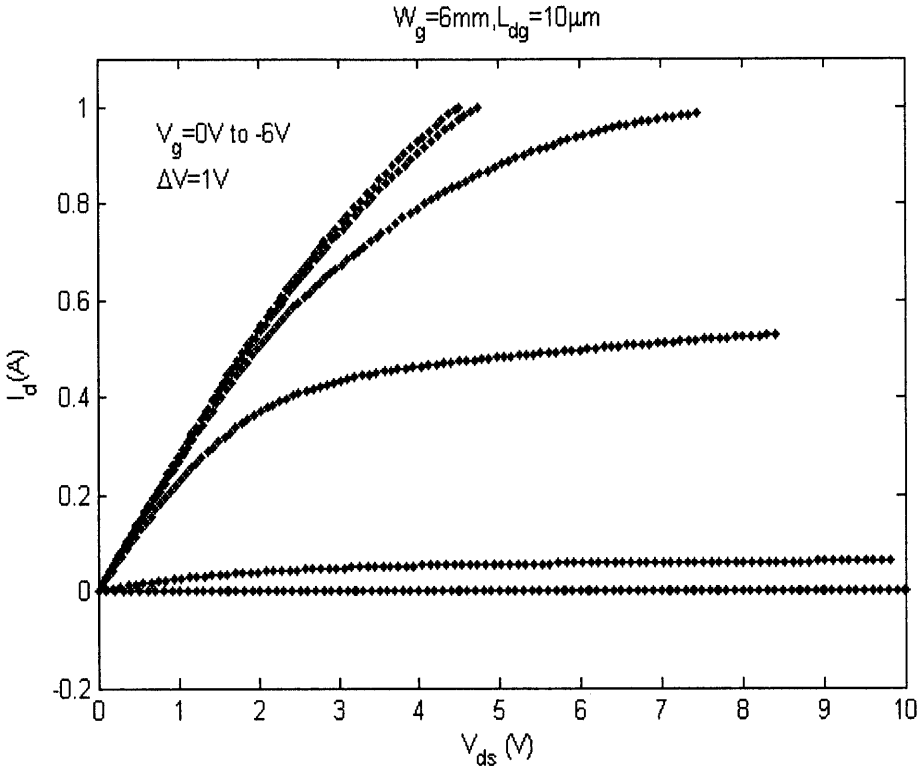


Figure 48. Id-Vds characteristics of device with gate width of 6mm

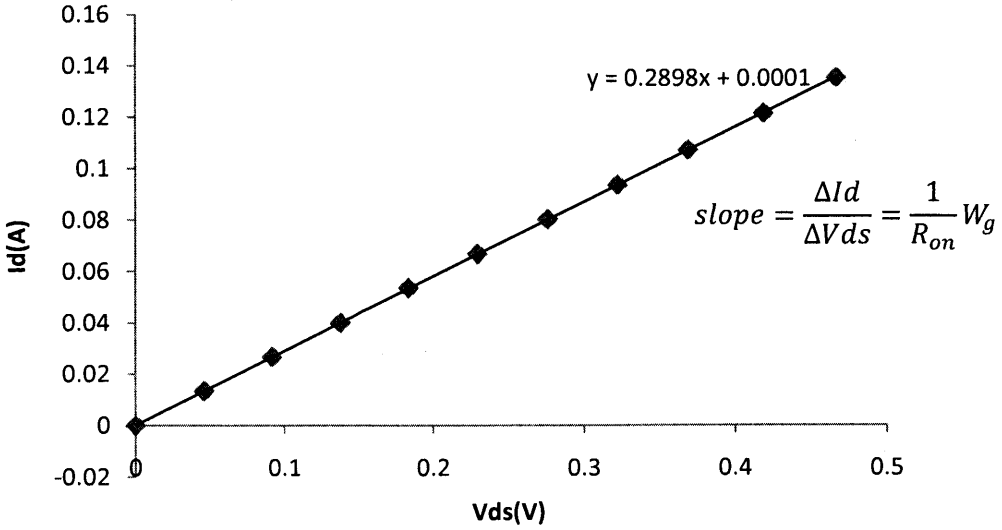


Figure 49. Close up segment of Id-Vds curve, illustrating the on-resistance, slope=0.2898A/V

$$R_{on} = \frac{1}{slope} * W_g = \frac{1}{0.2898A/V} * 6mm = 3.45\Omega * 6mm = 20.70\Omega mm$$

As can be seen in Figure 48, the maximum drain current is above the 1A compliance limit of the Agilent 41501B SMU and Pulse Generator Expander, so the Tektronix Type 576 Curve Tracer was used to measure the current beyond 1A.

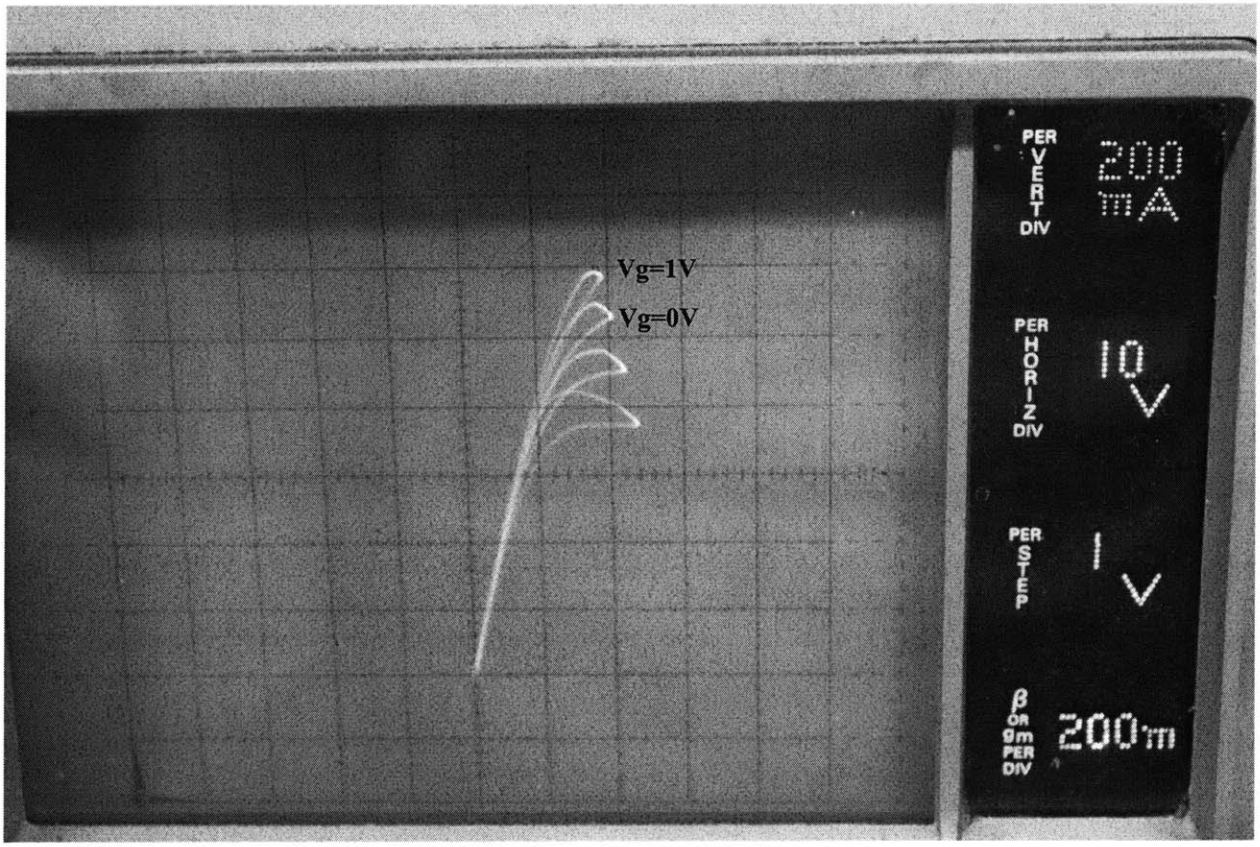


Figure 50. Id-Vds measurement of device with gate width of 6mm. I_{dmax}=1.2A

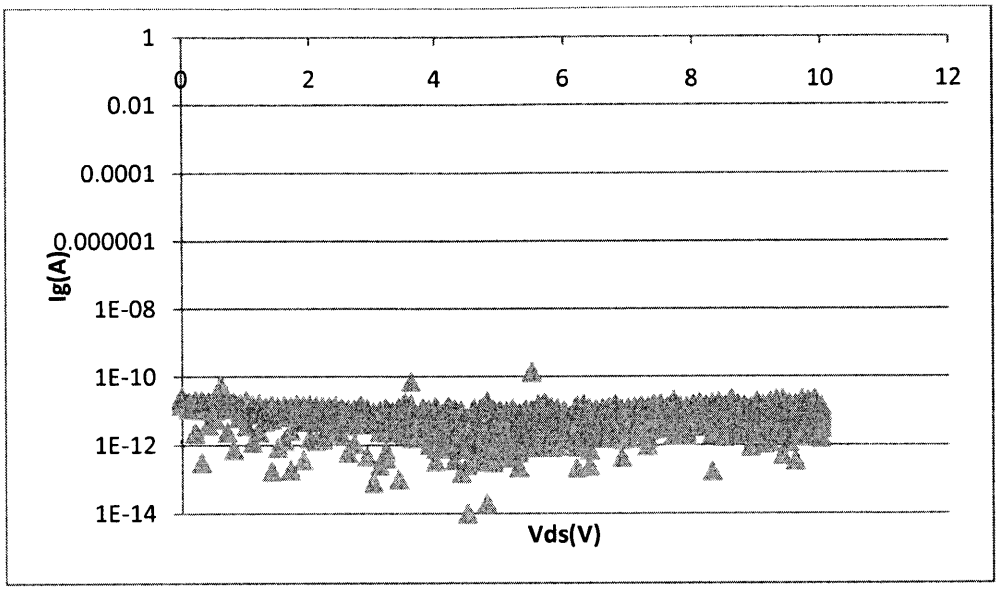


Figure 51. Ig-Vds (gate leakage current) measurements (Vg=1V to -6). $I_{gmax}=1.36x10^{-10}A$

W_g=12mm , L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

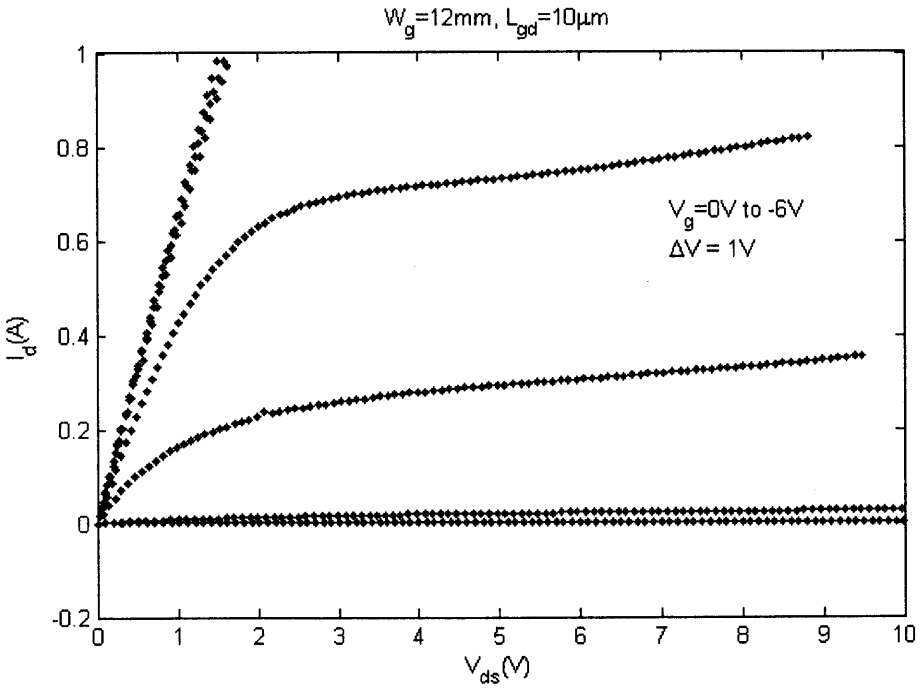


Figure 52. Id-Vds characteristics of device with gate width of 12mm

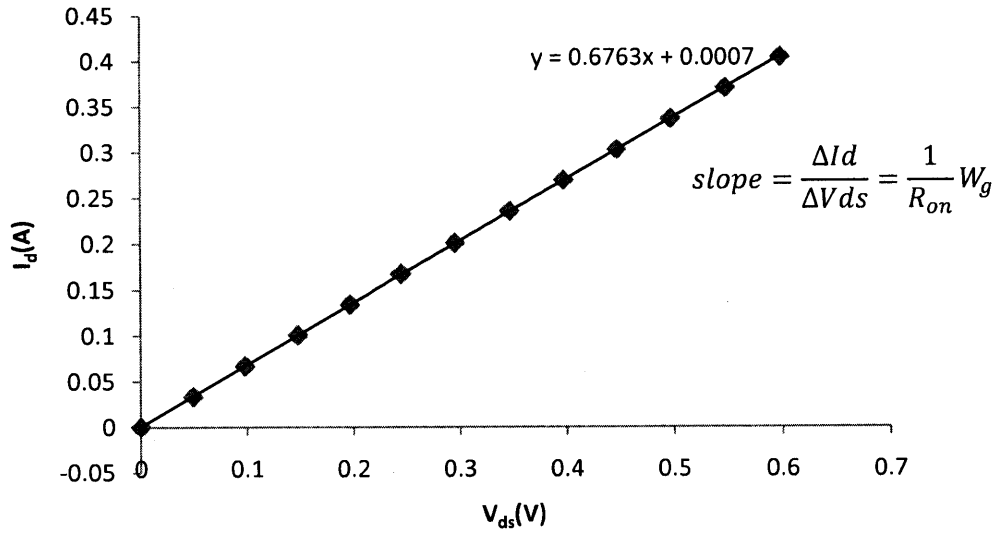


Figure 53. Close up segment of Id-Vds curve,
illustrating the on-resistance, slope=0.676A/V

$$R_{on} = \frac{1}{slope} * W_g = \frac{1}{0.676A/V} * 12mm = 1.48\Omega * 12mm = 17.76\Omega mm$$

As seen in the case of the device with 6mm gate periphery, the maximum drain current is above the 1A compliance limit of the Agilent 41501B SMU and Pulse Generator Expander, so the Tektronix Type 576 Curve Tracer was used to measure the current beyond 1A.

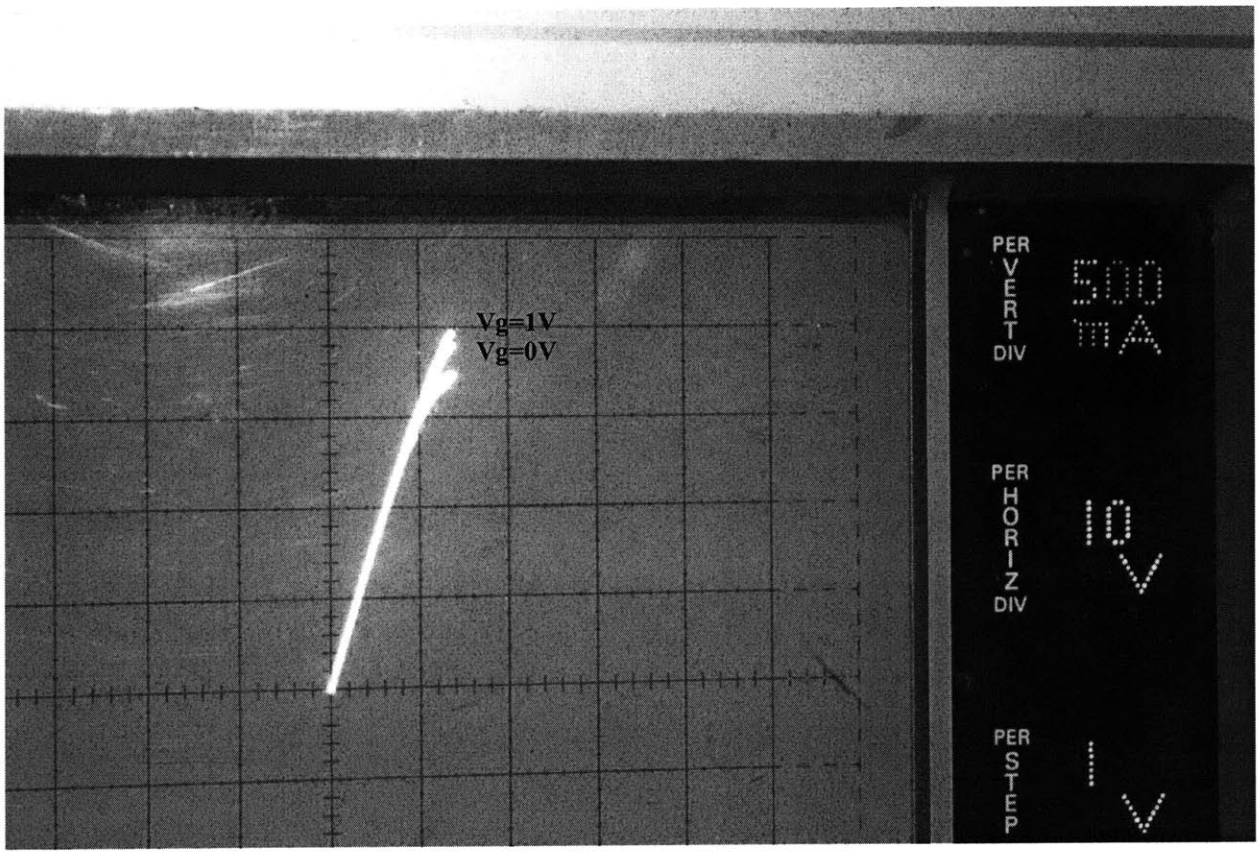


Figure 54. Id-Vds measurement of device with gate width of 12mm. I_{dmax}=2.0A

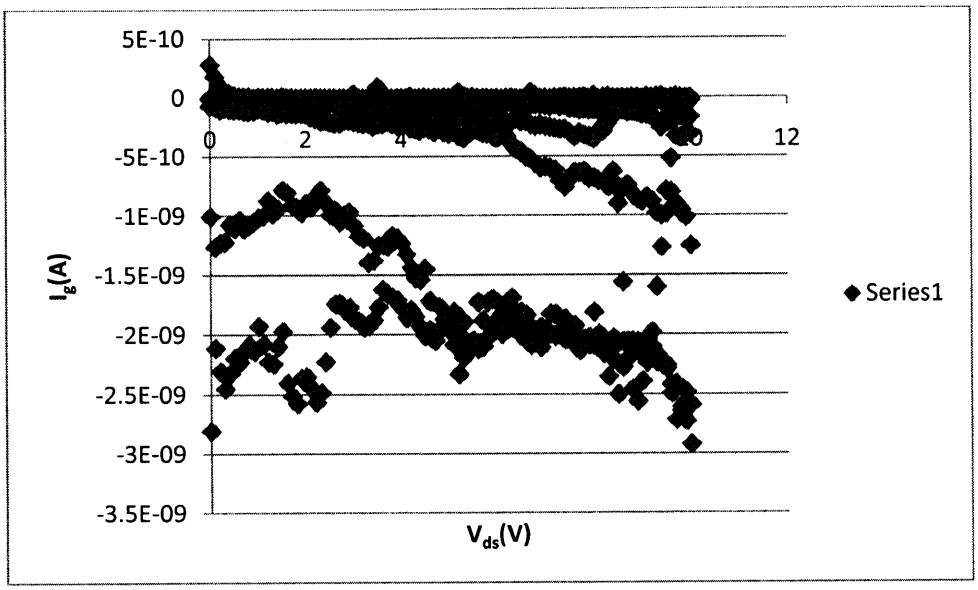


Figure 55. Ig-Vds (gate leakage current) measurements. $I_{gmax}=2.92x10^{-9}A$

Section 3.2: Capacitance Measurements

The gate capacitance is a very important parameter in power switches as it is responsible for the switching losses of these devices. Measurements of the gate capacitance were taken using the Agilent 4294A Precision Impedance Analyzer. For these measurements, the oscillation level was set to 100mV and the oscillation frequency to 1MHz. The DC bias was swept from -8 V to 1V. Altering the oscillation frequency (from 1MHz to 100kHz) and the illumination conditions did not change the results.

W_g=100μm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

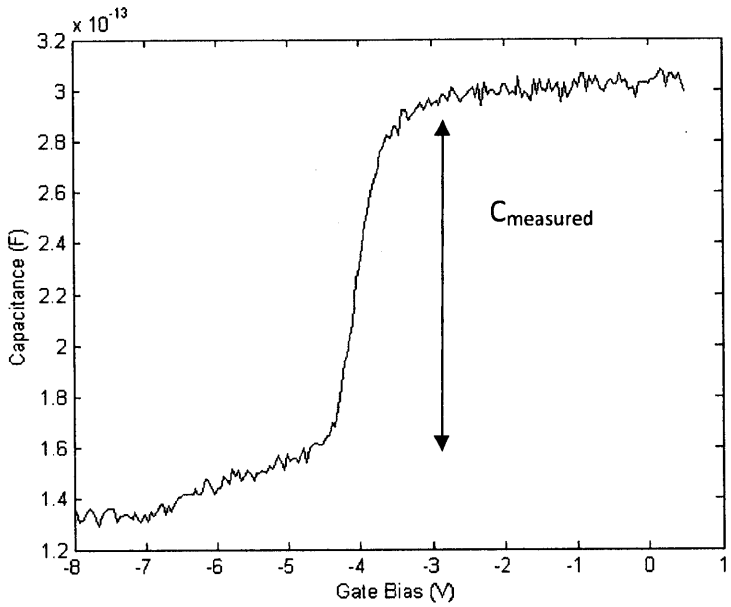


Figure 56. Capacitance-Voltage measurement of device with gate width of 100μm

Wg=300μm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

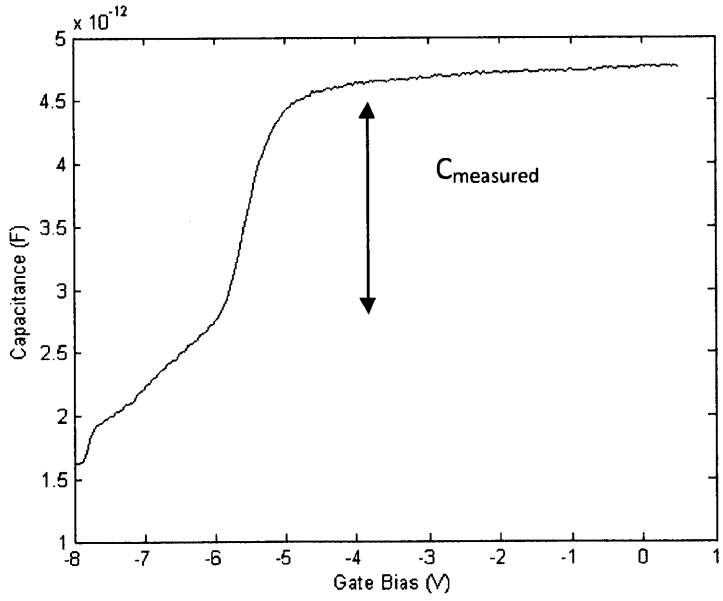


Figure 57. Capacitance-Voltage measurement of device with gate width of 300μm

Wg=600μm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

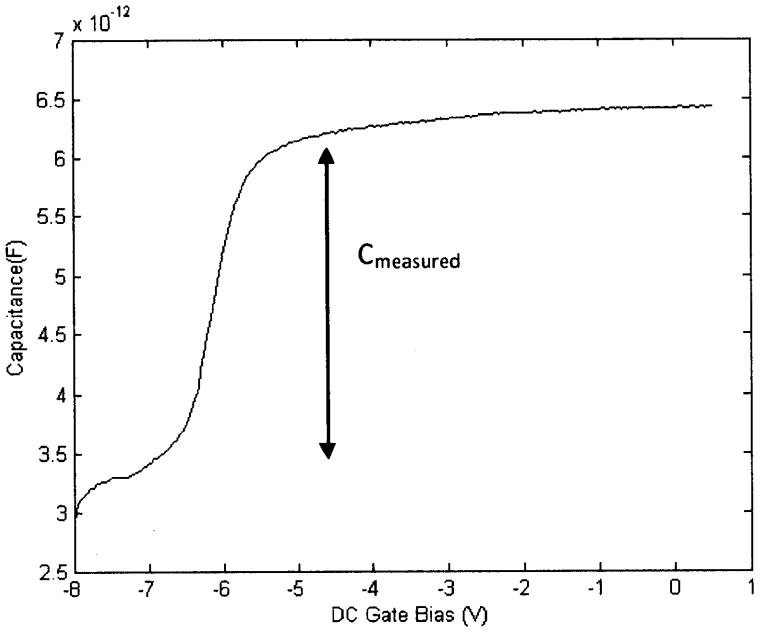


Figure 58. Capacitance-Voltage measurement of device with gate width of 600μm

Wg=6mm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

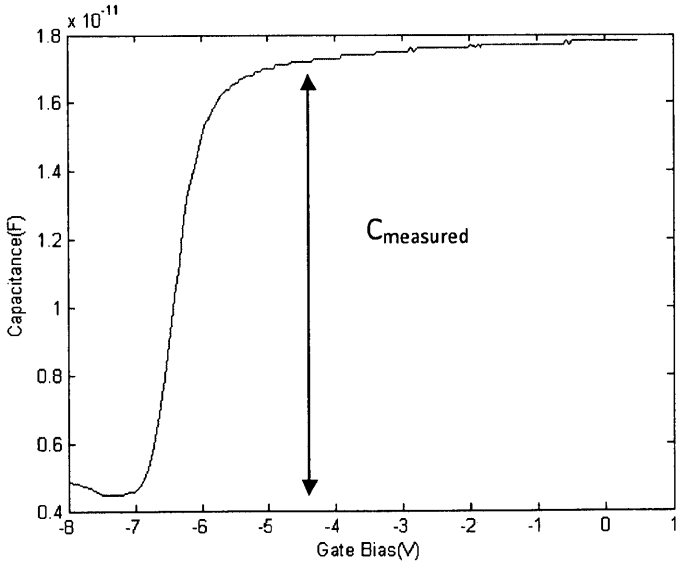


Figure 59. Capacitance-Voltage measurement of device with gate width of 6mm

Wg=12mm, L_g=2μm, L_{dg}=10μm, L_{sg}=1.5μm

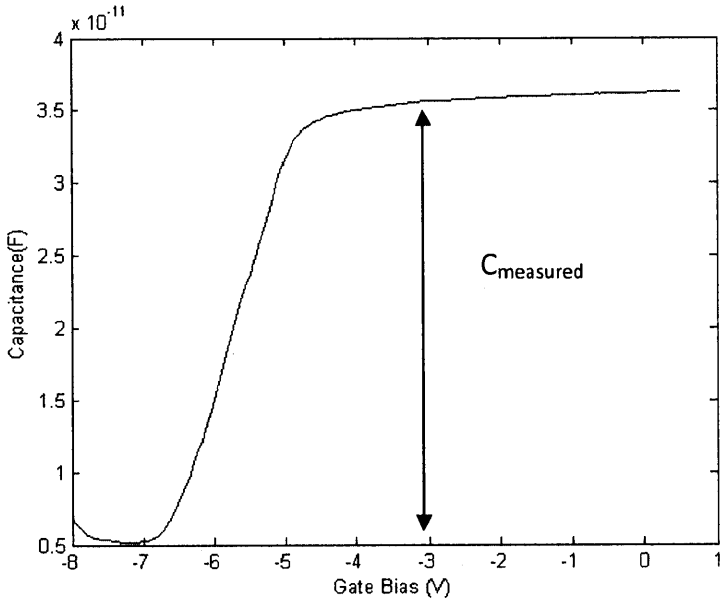


Figure 60. Capacitance-Voltage measurement of device with gate width of 12mm

Section 3.3: Theoretical Parameter Calculations

As a comparison to the theory, the calculations for the expected gate capacitance and on-resistance based on device geometry are included below.

Capacitance Calculations

Area of circular capacitor used as a reference = $\pi*(90\mu m)^2=25446.9\mu m^2$

Measured capacitance in circular capacitor =70pF

Cap per area = 70pF/25446.9μm2=$2.75x10^{-3}pF/\mu m^2$

W_g=12mm

$C_{g\text{-}2DEG}$=
Area of overlap between gate and mesa*capacitance per area=
(300μm*2μm*40fingers)*$2.75x10^{-3}pF/\mu m^2$=66pF

$C_{g\text{-}bridges}$=
dielectric constant of BCB*(Area of overlap between gate and bridge)/d=
(2.7*8.85x10^{-6}pF/μm)*(150μm*2μm*40fingers)/2 μm=.143 pF

$C_{g\text{-}substrate}$=
dielectric constant of GaN *(Area of gate)/d=
(10.4*8.85x10^{-6}pF/μm)*(300μm*2μm*40fingers+4μm*890μm+50μm*80μm*2pads)/2μm=1.6pF

$C_{s\text{-}substrate}$=
dielectric constant of GaN *(Area of source)/d=
(10.4*8.85x10^{-6}pF/μm)*(28μm*300μm*22pads)/2μm=8.5pF

C_{gs}=
$C_{g\text{-}2DEG}+C_{g\text{-}bridges}+(C_{g\text{-}substrate}$ in series with $C_{s\text{-}substrate})=C_{g\text{-}2DEG}+C_{g\text{-}bridges}+$
$(C_{g\text{-}substrate}*C_{s\text{-}substrate})/(C_{g\text{-}substrate}+C_{s\text{-}substrate})=$
66pF+.143pF+(1.6pF*8.5pF)/(1.6pF+8.5pF)=67.5pF

W_g=6mm

$C_{g\text{-}2DEG}$=
Area of overlap between gate and mesa*capacitance per area=
(300μm*2μm*20)*$2.75x10^{-3}pF/\mu m^2$=33pF

$C_{g\text{-}bridges}$=
dielectric constant of BCB*(Area of overlap between gate and bridge)/d=
(2.7*8.85x10^{-6}pF/μm)*(150μm*2μm*20)/2 μm=.072pF

$C_{g\text{-}substrate}$=
dielectric constant of GaN *(Area of gate)/d=
(10.4*8.85x10^{-6}pF/μm)*(2*300μm*20fingers+890μm*4μm+50μm*80μm*2pads)/2μm=1.08pF

$C_{s\text{-}substrate}$=
dielectric constant of GaN *(Area of source)/d=
(10.4*8.85x10^{-6}pF/μm)*(28μm*300μm*11pads)/2μm=4.25pF

C_{gs}=
$C_{g\text{-}2DEG}+C_{g\text{-}bridges}+(C_{g\text{-}substrate}$ in series with $C_{s\text{-}substrate})=C_{g\text{-}2DEG}+C_{g\text{-}bridges}+$
$(C_{g\text{-}substrate}*C_{s\text{-}substrate})/(C_{g\text{-}substrate}+C_{s\text{-}substrate})=$
33pF+.072pF+(1.06pF*4.25pF)/(1.06pF+4.25pF)=33.92pF

W_g=600μm

$C_{g\text{-}2DEG}$=
Area of overlap between gate and mesa*capacitance per area=
(300μm*2μm*2fingers)*2.75x10^{-3}pF/μm^2=3.3pF

$C_{g\text{-}bridges}$=
dielectric constant of BCB*(Area of overlap between gate and bridge)/d=
(2.7*8.85x10^{-6}pF/μm)*(150μm*2μm*2fingers)/2 μm=.0072pF

$C_{g\text{-}substrate}$=
dielectric constant of GaN *(Area of gate)/d=
(10.4*8.85x10^{-6}pF/μm)*(50μm*80μm*1pad+2μm*300μm*2)/2μm=.24pF

$C_{s\text{-}substrate}$=
dielectric constant of GaN *(Area of source)/d=
(10.4*8.85x10^{-6}pF/μm)*(28μm*300μm*2)/2μm=.77pF

C_{gs}=
$C_{g\text{-}2DEG}+C_{g\text{-}bridges}+(C_{g\text{-}substrate}$ in series with $C_{s\text{-}substrate})=C_{g\text{-}2DEG}+C_{g\text{-}bridges}+$
$(C_{g\text{-}substrate}*C_{s\text{-}substrate})/(C_{g\text{-}substrate}+C_{s\text{-}substrate})=$
3.3pF+.0072pF+(.24pF*.77pF)/(.24pF+.77pF)=3.49pF

W_g=300μm

$C_{g\text{-}2DEG}$=
Area of overlap between gate and mesa*capacitance per area=
(300μm*2μm*1finger)*2.75x10^{-3}pF/μm^2=1.65pF

$C_{g\text{-}bridges}$=0 (no bridges)

$C_{g\text{-}substrate}$=
dielectric constant of GaN *(Area of gate)/d=
(10.4*8.85x10^{-6}pF/μm)*(50μm*80μm*1pad+2μm*300μm*1)/2μm=.21pF

$C_{s\text{-}substrate}$=
dielectric constant of GaN *(Area of source)/d=
(10.4*8.85x10^{-6}pF/μm)*(28μm*300μm*1pad)/2μm=.39pF

C_{gs}=
$C_{g\text{-}2DEG}+C_{g\text{-}bridges}+(C_{g\text{-}substrate}$ in series with $C_{s\text{-}substrate})=C_{g\text{-}2DEG}+C_{g\text{-}bridges}+$
$(C_{g\text{-}substrate}*C_{s\text{-}substrate})/(C_{g\text{-}substrate}+C_{s\text{-}substrate})=$
1.65pF+0pF+(.21pF*.39pF)/(.21pF+.39pF)=1.79pF

W_g=100μm

$C_{g\text{-}2DEG}$=
Area of overlap between gate and mesa*capacitance per area=
(100μm*2μm*1finger)*2.75x10^{-3}pF/μm^2=.55pF

$C_{g\text{-}bridges}$=0 (no bridges)

$C_{g\text{-}substrate}$=
dielectric constant of GaN *(Area of gate)/d=
(10.4*8.85x10^{-6}pF/μm)*(35μm*35μm*1pad+2μm*100μm*1finger)/2μm=.066pF
$C_{s\text{-}substrate}$=
dielectric constant of GaN *(Area of source)/d=

$(10.4*8.85x10^{-6}pF/\mu m)*(50\mu m*100\mu m*1pad)/2\mu m=.23pF$

$C_{gs}=$
$C_{g\text{-}2DEG}+C_{g\text{-}bridges}+(C_{g\text{-}substrate}$ in series with $C_{s\text{-}substrate})=C_{g\text{-}2DEG}+C_{g\text{-}bridges}+$
$(C_{g\text{-}substrate}*C_{s\text{-}substrate})/(C_{g\text{-}substrate}+C_{s\text{-}substrate})=$
$.55pF+0pF+(.066pF*.23pF)/(.066pF+.23pF)=0.60pF$

On-resistance Calculation

The on-resistance is composed of contact resistance (R_C), characteristic of the metal contacting the substrate, and the sheet resistance (R_{sheet}), characteristic of the semiconductor substrate itself. Figure 61 shows a general case of how these component resistances make up the total on-resistance. Figure 62 illustrates the on-resistance calculation parameters for the fabricated GaN devices.

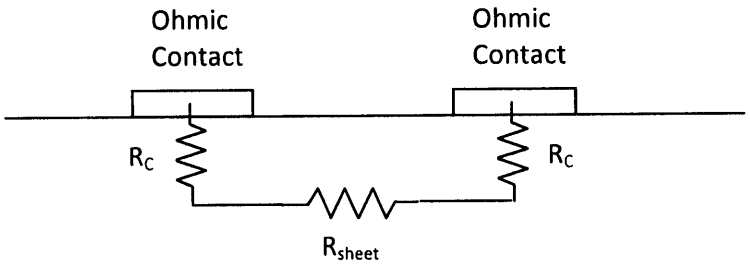


Fig. 61: $R_{ON} = R_C + R_C + R_{sheet}$*(length of channel)

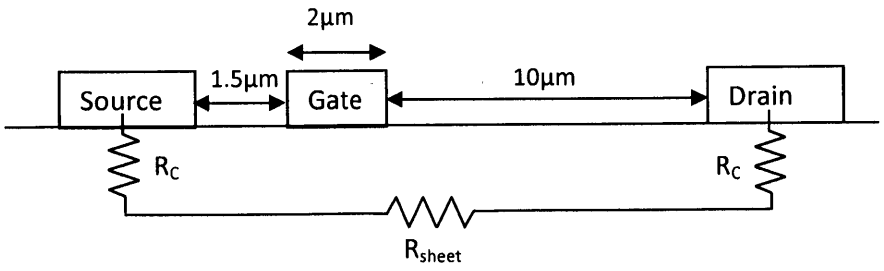


Fig.62: On-resistance parameters for fabricated devices.

Based on Transmission Line Method (TLM) measurements performed on the sample, R_C=.285Ωmm and R_{sheet}=439Ω. Thus, the theoretical on-resistance R_{ON} is:

$$R_{ON} = .285\Omega mm + .285\Omega mm + 439\Omega*(0.0015mm+.002mm+.010mm)=6.49\ \Omega mm$$

Section 3.4: Summary of Device Metrics

Table 4 and Figures 63-67 show a summary of how the different parameters studied in this thesis change with gate width.

Table 4. Summary of Device Metrics for different gate width

	Max drain current I_{dmax}(A)	Max gate leakage, I_{gmax} (A)	On-resistance R_{on} (Ωmm)	Expected R_{on} (Ωmm)	Unscaled Expected R_{on} (Ω)	Unscaled R_{on} (Ω)	Gate Capacitance C_g (pF)	Expected C_g (pF)
W_g=100μm	0.056	$9.1x10^{-13}$	8.06	6.49	64.9	80.6	.13	0.60
W_g=300μm	0.127	$1.48x10^{-8}$	15.87	6.49	21.6	52.9	1.75	1.79
W_g=600μm	0.260	$3.3x10^{-10}$	16.99	6.49	10.8	28.32	3.0	3.49
W_g=6mm	1.2	$1.36x10^{-10}$	20.70	6.49	1.1	3.45	12.8	33.92
W_g=12mm	2.0	$2.92x10^{-9}$	17.76	6.49	.54	1.48	30	67.5

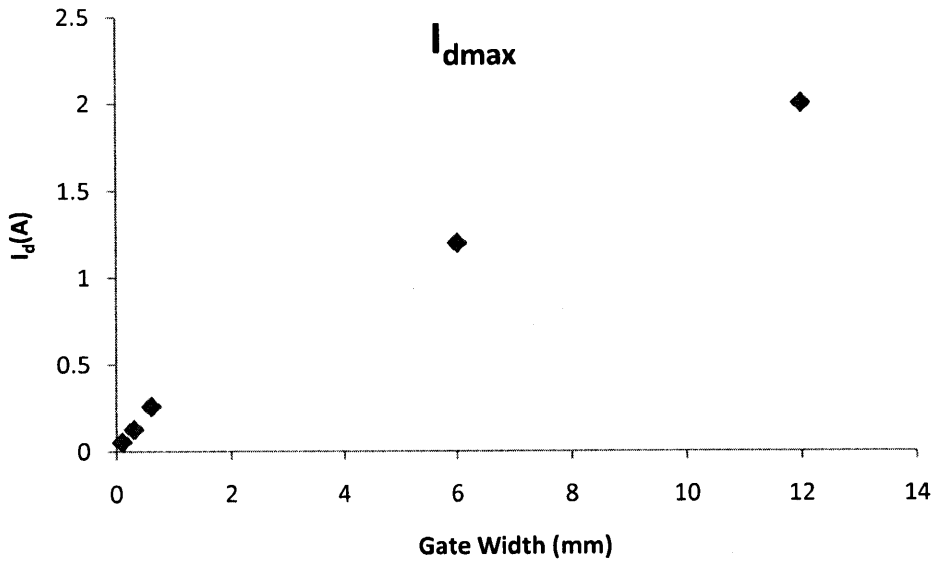


Figure 63. Maximum drain current scaling with gate width

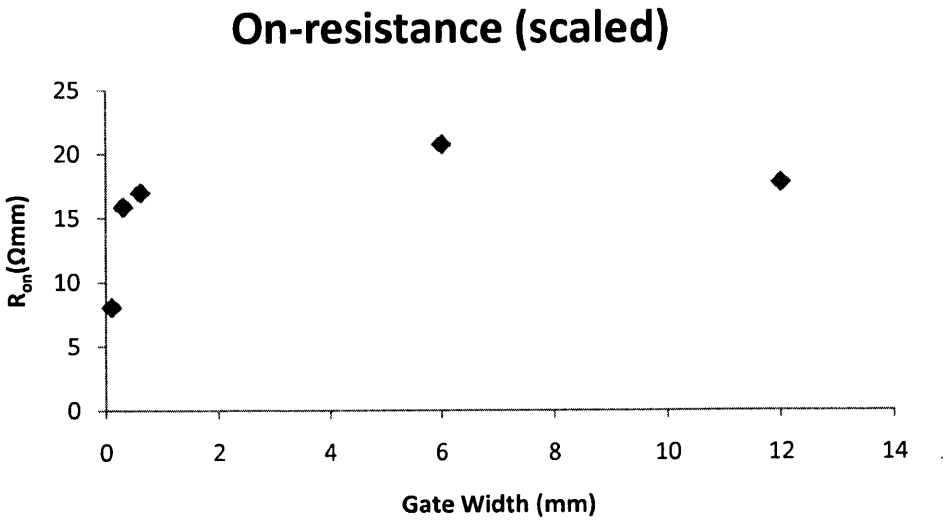


Figure 64. On-resistance scaling with gate width

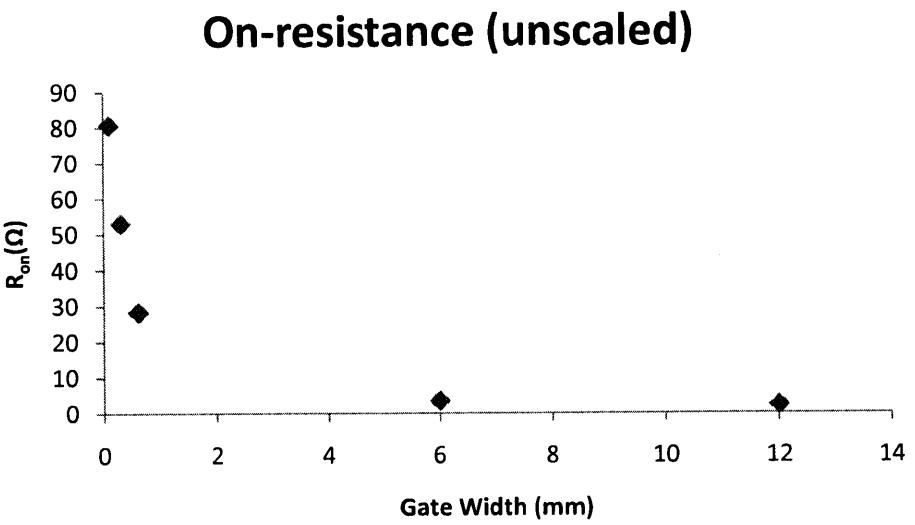


Figure 65. On-resistance scaling with gate width

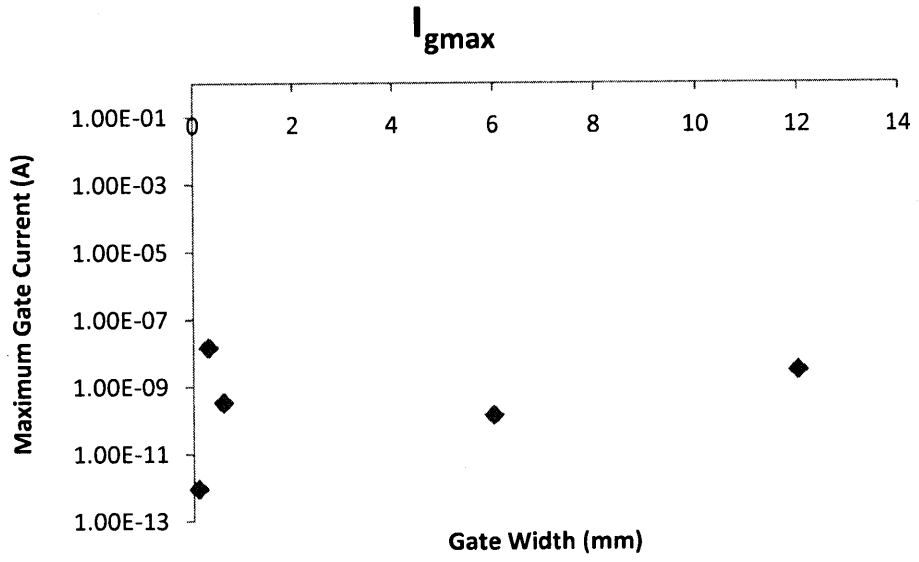


Figure 66. Maximum gate leakage scaling with gate width (V_{gs}=1V)

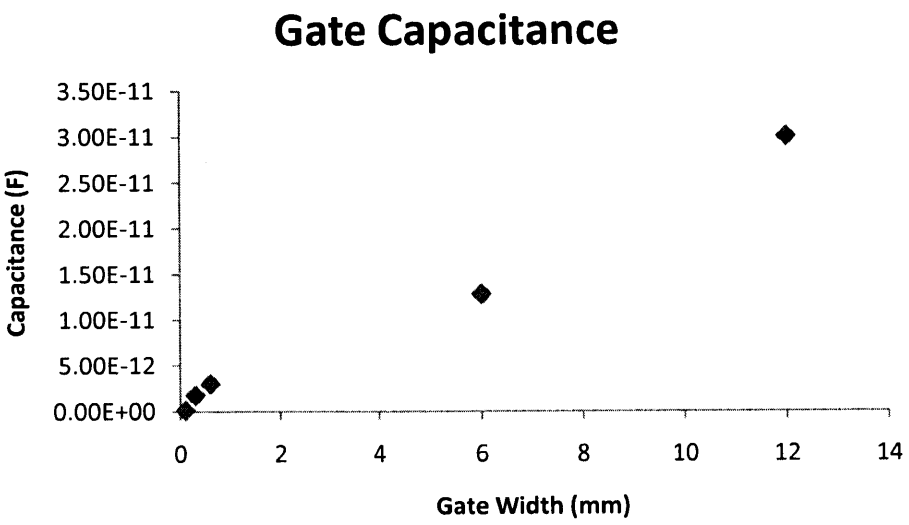


Figure 67. Gate capacitance scaling with gate width

Chapter 4: Conclusion and Future Work

In this thesis, a new process to fabricate GaN power transistors was developed. Specifically, a new technology to fabricate multi-finger devices was designed and the fabrication process for these devices was optimized. Direct current-voltage and capacitance measurements were taken from several devices varying in gate width (other dimensions constant) to study how several device parameters scale and how the experimental results compares with calculated theoretical data.

The measurements showed that maximum drain current, on-resistance, maximum gate leakage current, and gate capacitance all increase with increasing gate width. The calculated and measured gate capacitances show good agreement with some small differences possibly due to the fact that the actual dimensions of the contact pads were not exactly the expected size. Although, the BCB was spun at the same speed for the same amount of time on each run, there may have been slight variations in BCB thickness, leading to differences in the calculated and measure capacitance.

Assuming a certain set maximum current density (maximum drain current per unit gate width), it was expected that the I_{dmax} should scale linearly with W_g. This trend is seen in the smaller devices with gate width 100μm, 300μm, and 600μm (as seen in figure 68), but does not hold for the larger devices. The maximum drain currents for the W_g=6mm and W_g=12mm devices were not as high as expected (as seen in figure 69). Although steps were taken to minimize the effect of probe and contact resistance, these resistances still appear to reduce the maximum current. In the same way, the on-resistance was expected to stay somewhat constant across multiple gate widths. However, scaled R_{on} [Ω/mm] increases with increasing gate width,

which supports the hypothesis that there is some undesired probe and contact resistance in the measurement setup.

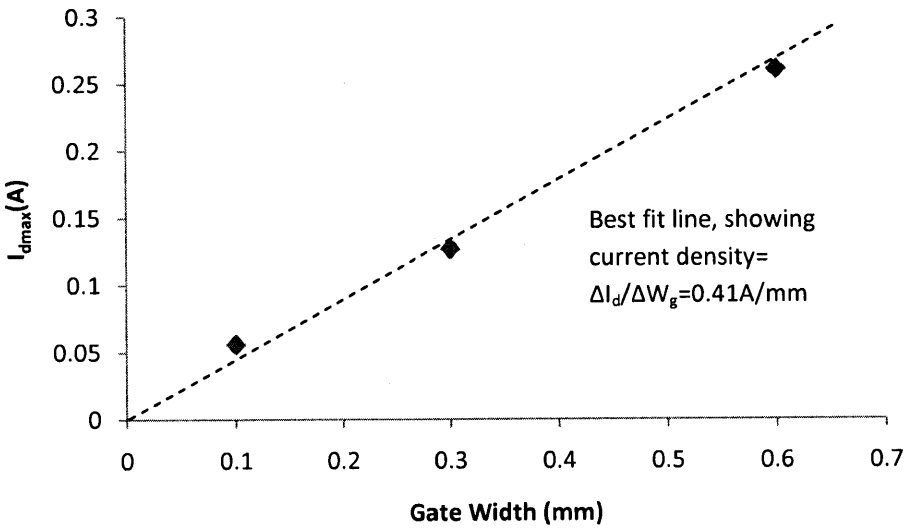


Fig. 68: Measured I_{dmax} values for W_g=100μm, 300μm and 600μm. The measured data points fall very close to the best fit line, showing that I_{dmax} scales linearly with gate width for these devices.

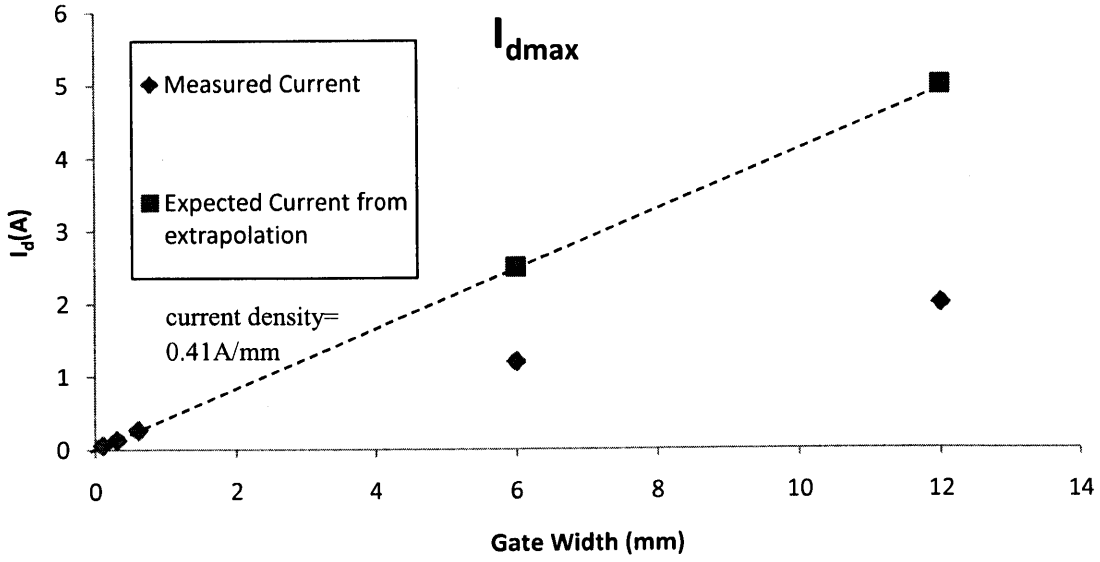


Fig. 69: Expected I_{dmax} of Wg=6mm and Wg=12mm devices based on extrapolated I_{dmax} from of smaller devices

To gain insight into the resistance in the large drain and source contact pads, the 4-probe Kelvin measurement method was used to apply a voltage difference across the pads and measure the current to derive the resistance. The results of the measurements are shown in figures 70 and 71.

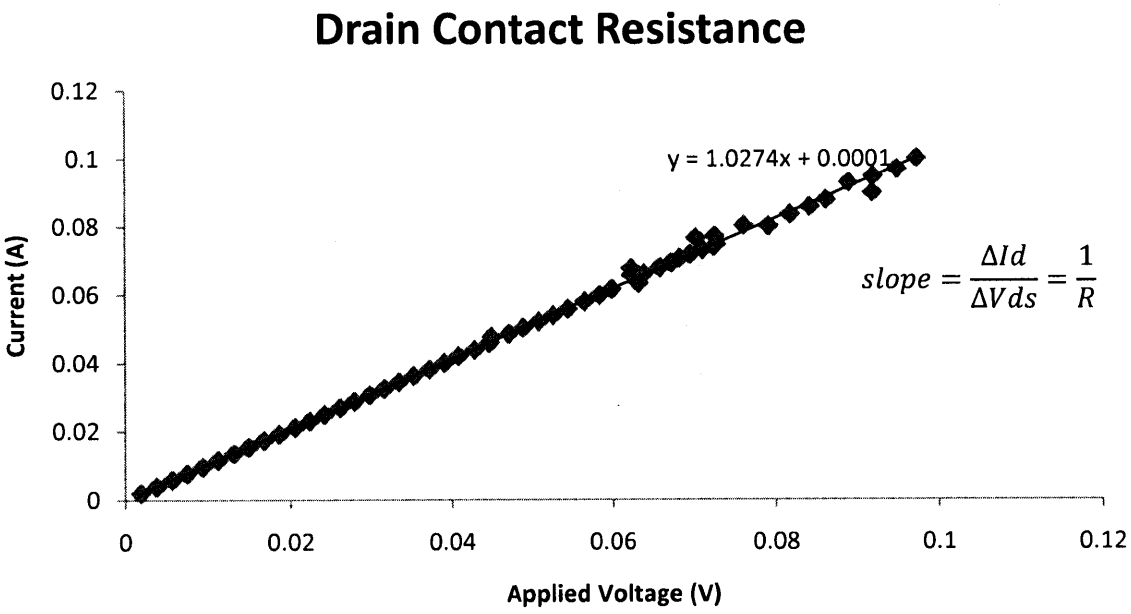


Fig. 70: Resistance of the drain contact on the W_g=12mm device. R=0.97Ω

$$R_{drain} = \frac{1}{slope} = \frac{1}{1.027A/V} = 0.97\Omega$$

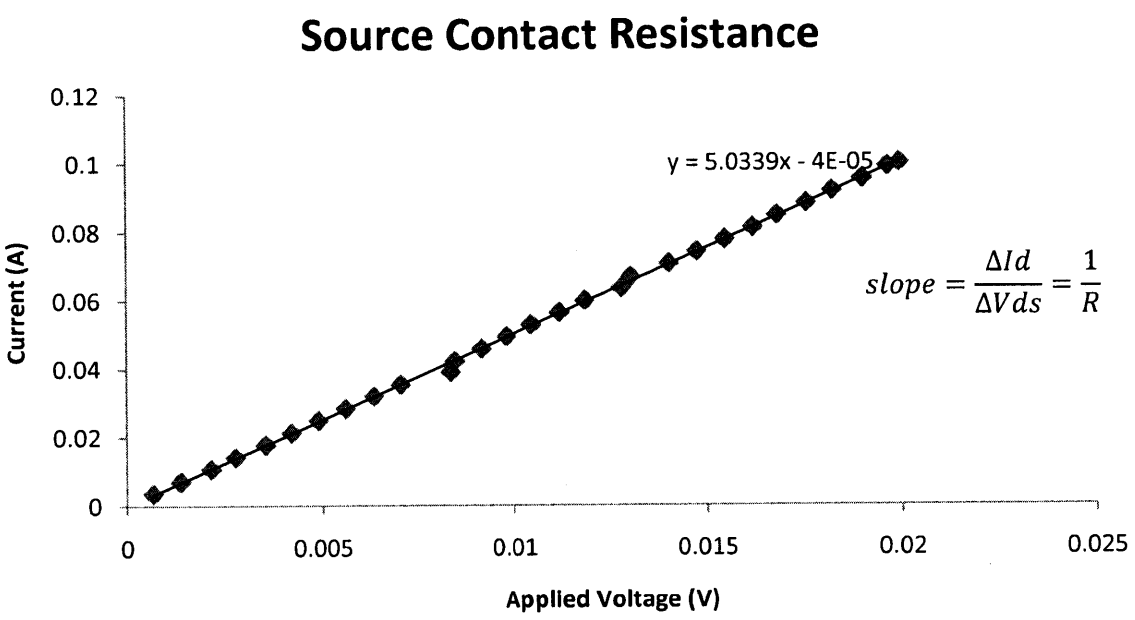


Fig. 71: Resistance of the source contact on the W_g=12mm device.
R=.199Ω

$$R_{source} = \frac{1}{slope} = \frac{1}{5.0339A/V} = .199\Omega$$

The resistances of the metal drain contact (0.97Ω) and source contact (.199Ω), as derived from the above calculations, constitute a large part of the total on-resistance.

The effect of temperature on the on-resistance was also investigated. The on-resistance was measured in a LakeShore cryogenic probe station at a reduced temperature of -50°C and compared with room temperature measurement of the R_{on} (shown in figure 72).

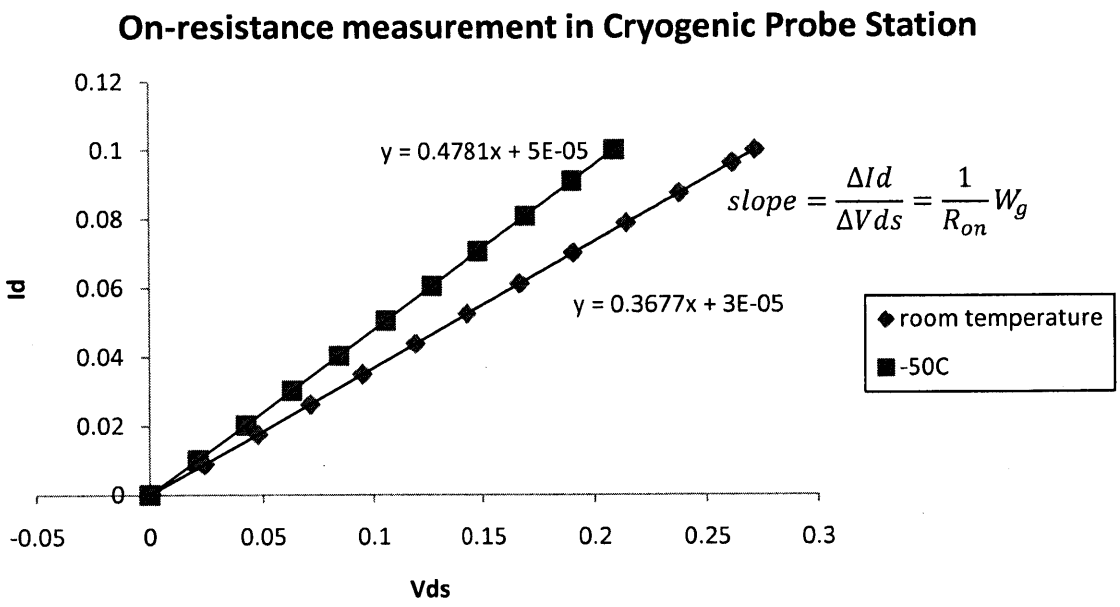


Fig. 72: On-resistance measure in the cryogenic probe station room temperature and at -50°C

$$R_{on,room\ temp.} = \frac{1}{slope} = \frac{1}{0.367A/V} = 2.72\Omega$$

$$R_{on,-50°C} = \frac{1}{slope} = \frac{1}{0.478A/V} = 2.09\Omega$$

This shows that reducing the temperature from room temperature (300K) to -50°C (223.15 K) results in a 23.2% decrease in on-resistance, which is in fairly good agreement with results from literature that show a decrease in sheet resistance of 27% in going from room temperature (300K) to -50°C (223.15 K) [11]. This decrease in on-resistance can be attributed to an increase in mobility at reduced temperatures.

One explanation for the low drain currents could be self-heating effects of the transistor. This might explain why the high on-resistance and the failure of I_{dmax} to scale linearly with W_g are more pronounced in the W_g=6mm and W_g =12mm devices. These larger devices support

higher currents which in turn produce more heat. R. Gaska et al. have shown that source-drain current in GaN devices grown on sapphire is significantly reduced by thermal heating compared to GaN devices grown on SiC, since the thermal conductivity of sapphire (0.25-0.5 $Wcm^{-1}K^{-1}$) is lower than that of SiC (5 $Wcm^{-1}K^{-1}$) [12]. The GaN devices processed in this thesis were grown on Si, which also has a lower thermal conductivity than SiC (1.5 $Wcm^{-1}K^{-1}$ for Si), so it is reasonable to believe that the relatively large amount of self-heating in the devices will lead to reduced drain current.

Future work should be focused on investigating the origin of the unwanted resistances in the measurement setup. With the elimination of these resistances via adequate packaging, for example, the on-resistance should decrease and the maximum drain current should increase. We are also working to use these devices in actual power electronic circuits that can take advantage of the large currents available in these new multi-finger devices.

Appendix A: Multi-finger Process Flow

Process and process number	Process steps	Tool
1) Wafer cleaning	Wash with Acetone from squirt bottle	Photo-wet-r
	Wash with Isopropanol from squirt bottle	Photo-wet-r
	Wash with DI water	Photo-wet-r
	Bake hotplate 5 min at 130C in order to dehydrate sample	Hot plate
	3 min cool down	
2) Lithography for Mesa isolation	Spin on OCG 825 with the following settings: Static dispense with pipette Spread for 2 sec at 750 rpm Spin for 30 sec at 3000 rpm	Coater
	Bake at Hotplate 2 or Hotplate 1 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate2 or Hotplate 1
	Exposure for 11.7 sec. Use low vac mode but hard contact also works	MA-6
	Develop in OCG 934 (1:1). The resist develops away in 30s – 1 min	Photo-wet-r
	DI-H_2O rinse 1 min	Photo-wet-r
3) Mesa etch	Run ETCHCLN.RCP for 10 min w/o sample in order to clean the chamber. Your ECR reflected power should not exceed 5W Then run GANETCH.RCP w/o sample in order to prepare the chamber. The reflected power should not exceed 1 W	PlasmaQuest
	Run GANETCH.RCP with the sample. Here is the recipe for GANETCH.RCP. Chuck temperature is 15	PlasmaQuest

	C (change on chiller). step 1: BCL3 10sccm / 10mtorr / 30s Step 2: BCL3 10sccm / 10mtorr / ECR = 50W/ RF = 15 W/ 5 s step 3: BCL3 10sccm / 10mtorr / ECR=100W / RF=15W / 60s step 4: BCL3 20sccm / CL2 5sccm / 10mtorr / 30s step 5: BCL3 20sccm / CL2 5sccm / 10mtorr / ECR=50W / RF=15W / 5s step 6: BCL3 20sccm / CL2 5sccm / 10mtorr / ECR=100W / RF=15W / 400s for around 150 nm etch.	
4) Wafer cleaning after mesa	Acetone with ultrasonic 5 min at power level 3-5. Glass beakers are more effective It is important to make sure that the sample is agitated (i.e. does not just sit in a corner) in order to get rid of the resist	Photo-wet-Au
	Isopropanol with ultrasonic 2 min at power level 3	Photo-wet-Au
	Running DI-H_2O 3 min	Photo-wet-r
	10 min descum in the asher at a 1000W. This ensures that all the photo-resist is gone. This is very important if your sample is going to go through a second anneal step of some sort.	Asher
	Inspect in fluoroscope. In the fluoroscope, all organic materials appear as red. Therefore, the pattern should look black (all the resist is gone).	Fluoroscope
	Once the fluoroscope inspection looks good, inspect under an optical microscope. Basically, if you can see colored fringes where the resist was supposed to be gone, then you still have resist. There have been cases where the sample looked OK in the fluoroscope but there was this residue in the sample	Optical Microscope
5) Lithography for ohmic contacts	Resist coat (AZ 5214). Dispense AZ 5214 in Al tray. Use pipette to put resist on stationary piece. Then Spread at 750 rpm for 5 s Spin at **3000** rpm for 30s.	Coater

	Bake at Hotplate 2 or Hotplate 1 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	hotplate
	Exposure for 10 sec. The exposure mode is low vacuum contact. The vacuum pressure should be -11psi. and the WEC should be 0.05 bar.	MA-6
	Post Exposure Bake. Hotplate 2 at 105C for 1min 5s, or Hotplate 1 at 110 C for 1 min.	hotplate
	Flood exposure for 100s. No clear mask necessary.	MA-6
	Develop in AZ 422 for 2 min. Make sure to agitate sample. Agitation is also VERY important to get good results	
	DI-H_2O rinse 1 min	
	Inspect in fluoroscope. In the fluoroscope, all organic materials appear as red. Therefore, the pattern should look black (all the resist is gone)	Fluoroscope
	Once the fluoroscope inspection looks good, inspect under an optical microscope. Basically, if you can see colored fringes where the resist was supposed to be gone, then you still have resist. There have been cases where the sample looked OK in the fluoroscope but there was this residue in the sample	Optical microscop
	Descum for 5 minutes at 1000W. The descum will create a thin layer of gallium oxide that will be stripped away	Asher
6) Oxide strip	DI-H_2O dip 1 min	Acid-hood
	HCl:H_2O (1:3) 1 min. When transferring the sample from the water to the acid, make sure that the sample still has water on top. This will allow for the acid to wet the surface.	Acid-hood
	DI-H_2O dip 1 min	Acid-hood
7) Ohmic contact	The sample should be placed in vacuum as soon as	EbeamAu or

metal deposition	possible after the oxide strip so please time yourself accordingly Ti (200 Å)/ Al (1000 Å) / Ni (250 Å) /Au (500 Å) For the EbeamFP, set the rotation speed to 0 rpm in order to ensure an easier liftoff. Don't forget to set rotation speed to 15 after use.	EbeamFP
8) Lift off	Place in Acetone.	Photo-wet-Au
	After the liftoff wait, use a pipette in order to squirt away as much of the metal as possible. Then, place the sample in a **new** beaker with acetone and agitate for 1-2 min at power level 3 in the ultrasonic bath	Photo-wet-Au
	Agitate in isopropanol for 2 min at power level 3 in ultrasonic bath	Photo-wet-Au
	Rinse in DI water and dry off with N2 gun	Photo-wet-Au
9) RTA	The RTA recipe is called GaN870. First, run the recipe w/o your sample in order to make sure that the tool is working correctly. Then, open the chamber and place sample. Wait for 5 min in order to ensure a pure N_2 atmosphere. Then, execute GaN870: Ramp in 40 s to 800C Hold 7s Ramp 870C Hold 30s (870C) Cool down 3m40s Wait until the temperature is below 100C before opening. This is to ensure that the sample does not react with oxygen present in the room	Rta35
10) Wafer cleaning	Wash with Acetone from squirt bottle	Photo-wet-r
	Wash with Isopropanol from squirt bottle	Photo-wet-r

	Wash with DI water	Photo-wet-r
	Bake hotplate 5 min at 130C in order to dehydrate sample	Hot plate
11) Gate dielectric deposition	Deposit 17nm Al_2O_3 by ALD	Cambridge Nanotec ALD
	Rapid thermal anneal	RTA
12) Pattern openings in dielectric ("opens" mask)	HMDS recipe #5 (adhesion promoter for resist in BOE dip)	HMDS
	Spin on OCG 825 with the following settings. Static dispense with pipette Spread for 2 sec at 750 rpm Spin for 30 sec at 3000 rpm	Coater
	Bake at Hotplate 2 or Hotplate 1 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate2 or Hotplate 1
	Exposure for 11.7 sec. Use low vac mode but hard contact also works	MA-6
	Develop in OCG 934 (1:1). The resist develops away in 30s – 1 min	Photo-wet-r
	DI-H_2O rinse 1 min	Photo-wet-r
13) Open dielectric for access to contacts	DI-H_2O dip 1 min	Acid-hood
	Buffered Oxide Etch for 20 seconds (bottle is labeled 7:1 BOE). When transferring the sample from the water to the acid, make sure that the sample still have water on top. This will allow for the acid to wet the surface.	Acid-hood
	DI-H_2O dip 1 min	Acid-hood

14) Lithography for Gate contact	Resist coat (AZ 5214). Dispense AZ 5214 in Al tray. Use pipette to put resist on stationary piece. Then Spread at 750 rpm for 5 s Spin at **4000** rpm for 30s. (Note: Omair has also got gate lithography to work with 3000 rpm)	Coater
	Bake at Hotplate 2 or Hotplate 1 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate
	Exposure for 10 sec. The exposure mode is low vacuum contact. The vacuum pressure should be -11psi. and the WEC should be 0.05 bar.	MA-6
	Post Exposure Bake. Hotplate 2 at 105C for 1min 5s, or Hotplate 1 at 110 C for 1 min.	Hot plate
	Flood exposure for 100s. No clear mask necessary.	MA-6
	Develop in AZ 422 for 2 min. Make sure to agitate sample. Agitation is also VERY important to get good gate lithography	Photo-wet-r
	DI-H_2O rinse 1 min	Photo-wet-r
	Inspect in fluoroscope. In the fluoroscope, all organic materials appear as red. Therefore, the pattern should look black (all the resist is gone)	Fluoroscope
	Once the fluoroscope inspection looks good, inspect under an optical microscope. Basically, if you can see colored fringes where the resist was supposed to be gone, then you still have resist. There have been cases where the sample looked OK in the fluoroscope but there was this residue in the sample	Optical Microscope
15) Deposition of gate metals	Ni (300Å)/Au(2000 Å)/Ni(500 Å) For the EbeamFP, set the rotation speed to 0 rpm in order to ensure an easier liftoff.	EbeamAu or EbeamFP
16) Lift off of gate	Place in Acetone.	Photo-wet-Au

metal		
	After the liftoff wait, use a pipette in order to squirt away as much of the metal as possible. Then, place the sample in a **new** beaker with acetone and agitate for 1-2 min at power level 3 in the ultrasonic bath	Photo-wet-Au
	Agitate in isopropanol for 2 min at power level 3 in ultrasonic bath	Photo-wet-Au
	Rinse in DI water and dry off with N2 gun	Photo-wet-Au
17) Wafer cleaning	Wash with Acetone from squirt bottle	Photo-wet-r
	Wash with Isopropanol from squirt bottle	Photo-wet-r
	Wash with DI water	Photo-wet-r
18) Lithography for etch protection layer ("opens" mask)	Spin on OCG 825 with the following settings. Static dispense with pipette Spread for 2 sec at 750 rpm Spin for 30 sec at 3000 rpm	Coater
	Bake at Hotplate 2 or Hotplate 1 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate2 or Hotplate 1
	Exposure for 11.7 sec. Use low vac mode but hard contact also works	MA-6
	Develop in OCG 934 (1:1). The resist develops away in 30s – 1 min	Photo-wet-r
	DI-H_2O rinse 1 min	Photo-wet-r
19)Deposition of etch protection layer	Deposit 400 Å Ni Liftoff in acetone	EbeamFP or EbeamAu
20) Coating adhesion promoter	Dispense AP3000 Spread for 2s@500rpm	Coater

<table>
<tr><td></td><td>Spin for 30s@2000rpm</td><td></td></tr>
<tr><td>21) BCB coating</td><td>Dispense Dow Corning Cyclotene 3022-35

Spread for 5s@500rpm

Spin for 60s@1500rpm</td><td>Coater</td></tr>
<tr><td></td><td>Bake at 250C for 1 hour</td><td>varTemp oven</td></tr>
<tr><td>22) Lithography for Cr Mask ("opens" mask)</td><td>Resist coat-AZ5214 spun at 750rpm for 5s, then 3000rpm for 30s</td><td>Coater</td></tr>
<tr><td></td><td>Bake for 5 min at 80C</td><td>Hotplate</td></tr>
<tr><td></td><td>Expose for 10s</td><td>MA-6</td></tr>
<tr><td></td><td>Post Exposure Bake. Hotplate 2 at 105C for 1min 5s, or Hotplate 1 at 110 C for 1 min.</td><td>hotplate</td></tr>
<tr><td></td><td>Flood exposure for 100s. No clear mask necessary.</td><td>MA-6</td></tr>
<tr><td></td><td>Develop in AZ422 for 2min (make sure to agitate sample)</td><td>Photo-wet-r</td></tr>
<tr><td></td><td>DI-H2O rinse 1 min</td><td>Photo-wet-r</td></tr>
<tr><td>22) Deposition of Cr mask</td><td>Deposit 700 Å Cr in ebeamAu, deposition rate 1Å/s, no rotation

liftoff in acetone</td><td>EbeamAu</td></tr>
<tr><td>23) BCB Openings Etch</td><td>BCBETCH.rcp
<table><tr><td>O2 (sccm)</td><td>40</td><td>40</td><td>40</td></tr><tr><td>CF4 (sccm)</td><td>5</td><td>5</td><td>5</td></tr><tr><td>Process. Pressure (mTorr)</td><td>10</td><td>10</td><td>10</td></tr><tr><td>ECR system (Watts)</td><td>0</td><td>15</td><td>125</td></tr></table></td><td>Plasmaquest</td></tr>
</table>

<table>
<tr><td></td><td><table>
<tr><td>RF system (Watts)</td><td>0</td><td>30</td><td>30</td></tr>
<tr><td>Step time(s)</td><td>30</td><td>5</td><td>740</td></tr>
</table></td><td></td></tr>
<tr><td>24) Lithography for Cr Mask ("opens" mask)</td><td>The first BCB etch etches away the first Cr mask, so a second Cr mask must be deposited

Resist coat-AZ5214 spun at 750rpm for 5s, the 3000rpm for 30s</td><td>Coater</td></tr>
<tr><td></td><td>Bake for 5 min at 80C</td><td>Hotplate</td></tr>
<tr><td></td><td>Expose for 10s</td><td>MA-6</td></tr>
<tr><td></td><td>Post Exposure Bake. Hotplate 2 at 105C for 1min 5s, or Hotplate 1 at 110 C for 1 min.</td><td>hotplate</td></tr>
<tr><td></td><td>Flood exposure for 100s. No clear mask necessary.</td><td>MA-6</td></tr>
<tr><td></td><td>Develop in AZ422 for 2min (make sure to agitate sample)</td><td>Photo-wet-r</td></tr>
<tr><td></td><td>DI-H2O rinse 1 min</td><td>Photo-wet-r</td></tr>
<tr><td>25) Deposition of Cr mask</td><td>Deposit 700 Å Cr in ebeamAu, deposition rate 1Å/s, no rotation

liftoff in acetone</td><td>EbeamAu</td></tr>
<tr><td>26) BCB Openings Etch</td><td>BCBETCH.rcp<table>
<tr><td>O2 (sccm)</td><td>40</td><td>40</td><td>40</td></tr>
<tr><td>CF4 (sccm)</td><td>5</td><td>5</td><td>5</td></tr>
<tr><td>Process. Pressure (mTorr)</td><td>10</td><td>10</td><td>10</td></tr>
<tr><td>ECR system (Watts)</td><td>0</td><td>15</td><td>125</td></tr>
</table></td><td>Plasmaquest</td></tr>
</table>

	RF system (Watts)	0	30	30	
	Step time(s)	30	5	540	
27) Cr mask removal	Dip in CR-7 chromium etchant for 20s, or until entire Cr mask is removed				Acidhood
28) Wafer cleaning after etch	Acetone with ultrasonic 5 min at power level 5. It is important to make sure that the sample is agitated (i.e. does not just sit in a corner) in order to get rid of the resist				Photo-wet-Au
	Isopropanol with ultrasonic 2 min at power level 3				Photo-wet-Au
	Running DI-H_2O 3 min				Photo-wet-r
29) Lithography for source bridges ("pads1" mask)	Resist coat-AZ5214 spun at 750rpm for 5s, the 3000rpm for 30s				Coater
	Bake at Hotplate 2 or Hotplate 300 at 80C for 5 min. This step cures the resist by evaporating the solvent away.				Hot plate
	Exposure for 10 sec				MA-6
	Post Exposure Bake. Hotplate 2 at 105C, Hotplate 300 at 110 C for 2 min. Note: Hotplate 2 is 5 C hotter than Hotplate 300, which is why the temperatures are different				Hot plate
	Flood exposure for 100 s with clear mask				MA-6
	Develop in AZ 422 for 2 min. Make sure to agitate sample.				Photo-wet-r
	DI-H_2O rinse 1 min				Photo-wet-r
30) Source Bridge Metal deposition	0.05μm Ti + 0.6μm Au, rotation on (takes about 2.5 hrs in ebeamfp) Liftoff in acetone				EbeamFP
31) Lithography for	Spin on OCG 825 with the following settings.				Coater

contact metal thickening ("Opens" mask)	Static dispense with pipette Spread for 2 sec at 750 rpm Spin for 30 sec at 3000 rpm	
	Bake at Hotplate 2 or Hotplate 1 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate2 or Hotplate 1
	Exposure for 11.7 sec. Use low vac mode but hard contact also works	MA-6
	Develop in OCG 934 (1:1). The resist develops away in 30s – 1 min	Photo-wet-r
	DI-H_2O rinse 1 min	Photo-wet-r
32) Contact metal thickening	200 Å Ti+1.5k Å Au Liftoff in acetone	EbeamFP
33)Lithography for source bridge connections ("pad2" mask)	Resist coat-AZ5214 spun at 750rpm for 5s, the 3000rpm for 30s	Coater
	Bake at Hotplate 2 or Hotplate 300 at 80C for 5 min. This step cures the resist by evaporating the solvent away.	Hot plate
	Exposure for 10 sec	MA-6
	Post Exposure Bake. Hotplate 2 at 105C, Hotplate 300 at 110 C for 2 min. Note: Hotplate 2 is 5 C hotter than Hotplate 300, which is why the temperatures are different	Hot plate
	Flood exposure for 100 s with clear mask	MA-6
	Develop in AZ 422 for 2 min. Make sure to agitate sample.	Photo-wet-r
	DI-H_2O rinse 1 min	Photo-wet-r
34) Deposit Source	0.05μm Ti + 0.6μm Au, rotation on (takes about 2.5	EbeamFP

Bridge connections	hrs in ebeamfp) Liftoff in acetone	

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