Low Power Circuits and Systems for Wireless Neural Stimulation

by

Scott Kenneth Arfin

Bachelor of Science in Electrical Engineering
Columbia University, 2004

Master of Science in Electrical Engineering
Massachusetts Institute of Technology, 2006

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2011

Author .....
Department of Electrical Engineering and Computer Science
May 16, 2011

Certified by .....
Rahul Sarpeshkar
Associate Professor of Electrical Engineering
Thesis Supervisor

Accepted by .....
Leslie Kolodziejski
Chair, Committee on Graduate Students
Professor of Electrical Engineering

Low Power Circuits and Systems for Wireless Neural Stimulation

by

Scott Kenneth Arfin

Submitted to the Department of Electrical Engineering and Computer Science
on May 16, 2011 in partial fulfillment of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

Abstract

Electrical stimulation of tissues is an increasingly valuable tool for treating a variety of disorders, with applications including cardiac pacemakers, cochlear implants, visual prostheses, deep brain stimulators, spinal cord stimulators, and muscle stimulators. Brain implants for paralysis treatments are increasingly providing sensory feedback via neural stimulation. Within the field of neuroscience, the perturbation of neuronal circuits wirelessly in untethered, freely-behaving animals is of particular importance. In implantable systems, power consumption is often the limiting factor in determining battery or power coil size, cost, and level of tissue heating, with stimulation circuitry typically dominating the power budget of the entire implant. Thus, there is strong motivation to improve the energy efficiency of implantable electrical stimulators.

In this thesis, I present two examples of low-power tissue stimulators. The first type is a wireless, low-power neural stimulation system for use in freely behaving animals. The system consists of an external transmitter and a miniature, implantable wireless receiver-and-stimulator utilizing a custom integrated chip built in a standard 0.5 μm CMOS process. Low power design permits 12 days of continuous experimentation from a 5 mAh battery, extended by an automatic sleep mode that reduces standby power consumption by 2.5x. To test this device, bipolar stimulating electrodes were implanted into the songbird motor nucleus HVC of zebra finches. Single-neuron recordings revealed that wireless stimulation of HVC led to a strong increase of spiking activity in its downstream target, the robust nucleus of the arcopallium (RA). When this device was used to deliver biphasic pulses of current randomly during singing, singing activity was prematurely terminated in all birds tested.

The second stimulator I present is a novel, energy-efficient electrode stimulator with feedback current regulation. This stimulator uses inductive storage and recycling of energy based on a dynamic power supply to drive an electrode in an adiabatic fashion such that energy consumption is minimized. Since there are no explicit current sources or current limiters, wasteful energy dissipation across such elements is naturally avoided. The stimulator also utilizes a shunt current-sensor to monitor and regulate the current through the electrode via feedback, thus enabling flexible and safe stimulation. The dynamic power supply allows efficient transfer of energy both to and from the electrode, and is based on a DC-DC converter topology that is used in a bidirectional fashion. In an exemplary electrode implementation, I show how the stimulator combines the efficiency of voltage control and the safety and accuracy of current control in a single low-power integrated-circuit built in a standard 0.35 μm CMOS process. I also perform a theoretical analysis of the energy efficiency that is in accord with experimental measurements. In its current proof-of-concept implementation, this stimulator achieves a 2x-3x reduction in energy consumption as compared to a conventional current-source-based stimulator operating from a fixed power supply.

Thesis Supervisor: Rahul Sarpeshkar
Title: Associate Professor of Electrical Engineering

Acknowledgments

There are many people whom I would like to thank for supporting me while I did the research for this thesis.

I would like to thank my adviser, Professor Rahul Sarpeshkar for his thoughtful advice and inspirational teaching. I have learned an enormous amount of circuit design, especially feedback circuit design, and how to think both critically and imaginatively from him. I would also like to thank the members of my thesis committee for their comments, suggestions and guidance which helped improve the quality of this thesis: Professors Michale Fee, Edward Boyden, and Clifton Fonstad.

I would also like to thank all family & friends. The support especially of my Mom, Dad, brother Dan, and close friends Seth and David, has been immeasurably important in helping me to conquer the challenges of graduate school and to make it across the finish line. Thank you so much. You are the best.

Special thanks to thank the many members of the Analog VLSI & Biological Systems Group with whom I have had the pleasure of working with over my time in the lab. I would especially like to thank Soumyajit Mandal, my first TA and graduate student mentor at MIT, and Serhii Zhak for sharing an office with me for several years and for many helpful discussions. I also would like to thank Woradorn Wattanapantich, my officemate in my final year of graduate school for his expertise and for proofreading parts of this dissertation. Ben Rapoport and Lorenzo Turicchia have also been close associates who have advised, encouraged and helped ensure the success of this work.

A special acknowledgement goes to Dr. Michael Long, master surgeon extraordinaire, Met fan, and friend. Thank you Michael for enriching my graduate school experience with neuroscience.

Finally, I would like to acknowledge the various funding sources that made my research possible: the National Institutes of Health, the Office of Naval Research, and the McGovern Institute Neurotechnology program at MIT.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background of Neural Stimulation

Perhaps the oldest example of implantable electrical tissue stimulators is the artificial cardiac pacemaker, with the first battery powered, fully implanted example appearing in 1958. Since then, approximately 3 million people worldwide now have artificial pacemakers. An example of an implantable artificial pacemaker is shown in Figure 1-1a.

With the success of the pacemaker, the number of stimulation applications has since exploded. For example, cochlear implants now enable hearing for approximately 180,000 profoundly deaf individuals worldwide. A patient is a candidate for a cochlear implant if they have greater than 70-80dB of hearing loss. At these levels of loss, a hearing aid is of little value. In a cochlear implant, a microphone collects sound which is fed to a processor translating this incoming sound into patterns for driving the stimulating electrodes. The cochlea contains approximately 25,000 nerve fibers, yet remarkably the 16 stimulating electrodes found in the typical cochlear implant is sufficient for reproducing intelligible speech in the profoundly deaf patient. An example of a cochlear implant processor is shown in Figure 1-1b. The astounding success of the cochlear implant has helped pave the way for even more ambitious stimulator applications.

Restoring sight to the blind is one such highly ambitious application which has yet to achieve widespread clinical use. Figure 1-1c shows the concept of one such visual prosthesis based on stimulation of the retina. In this design, a camera collects images and a signal processor generates patterns to drive an array of electrodes implanted in the retina, resulting in the perception of vision. Visual prostheses are currently under research and development, and advances in signal processing, stimulator design and electrode fabrication technology could achieve the high spatial and temporal

resolution that is necessary for producing useful images via stimulation.

One rapidly developing stimulator technology is deep brain stimulation (DBS). DBS is presently being used to treat a growing number of neurological disorders, such as essential tremor and Parkinson disease in patients who do not respond to medication or physical therapy. Currently, approximately 70,000 patients have received DBS implants for Parkinson's disease with uncanny success; the mechanisms of DBS and the underlying neurological disorders it treats remain poorly understood. DBS has also shown potential for treating a variety of other disorders such as Tourette syndrome, pain, depression, and obsessive compulsive disorder. Brain implants for paralysis treatments are increasingly providing sensory feedback via neural stimulation. An x-ray image of implanted DBS electrodes is shown in Figure 1-1d. With a DBS-style arrangement implanted in the spinal cord, the treatment of severe chronic back pain is also possible, as shown in Figure 1-2a.

Individuals suffering from tetraplegia or paraplegia may also benefit from functional electrical stimulation, an example system of which is shown in Figure 1-2b. Actuation of paralyzed limbs is achieved through stimulation of muscles based on control inputs, which may be derived from a variety of methods including shoulder or head movement, voice control, electroencephalogram (EEG), or other brain-computer and brain-machine interfaces.

Finally, within the field of neuroscience, the perturbation of neuronal circuits wirelessly in untethered, freely-behaving animals is of particular importance. A rat with a head stage for recording and stimulation of neurons is shown Figure 1-2c.

In implantable systems, power consumption is often the limiting factor in determining battery or power coil size, cost, and level of tissue heating, with stimulation circuitry typically dominating the power budget of the entire implant. For example, state-of-the-art cochlear implants spend only a small fraction of their power budget on the microphone front end and signal processing, with the majority of power going to the stimulator. Deep brain stimulators perform essentially no signal processing to speak of, so all of the power consumed in a DBS system is due to the stimulators themselves. Other emerging technologies such as retinal stimulators are likely to be dominated by stimulator power consumption due to the large arrays of stimulating electrodes. Thus, there is strong motivation to improve the energy efficiency of implantable electrical stimulators. Improvements in stimulator energy efficiency lead directly to reductions in battery or coil size, increases in battery lifetime, and reductions in tissue heating. Patient safety and comfort are increased, and medical costs are reduced if the size of the implant can be decreased.

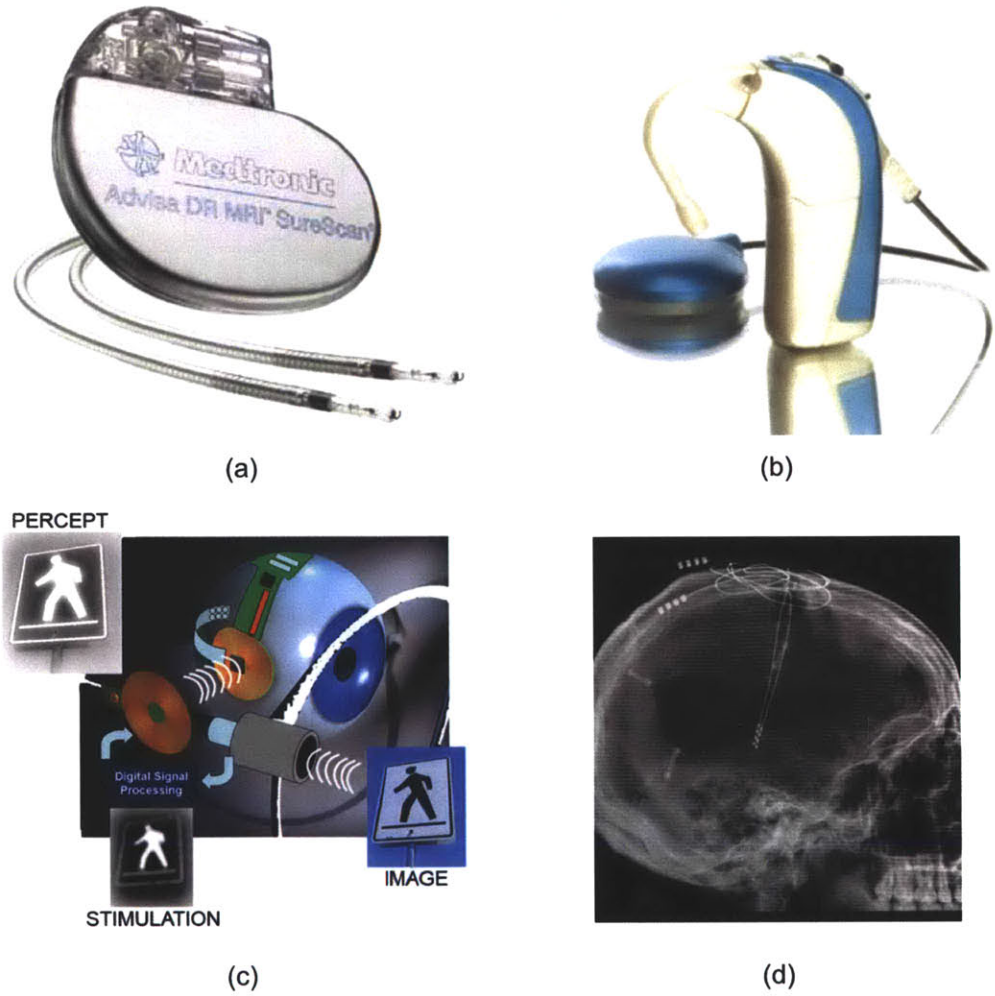


Figure 1-1: Stimulator applications examples. (a) Artificial pacemaker. Figure courtesy Medtronic. (b) Cochlear implant processor. Figure courtesy Advanced Bionics. (c) Retinal implant. Figure courtesy Boston Retinal Implant Group. (d) X-ray image of implanted DBS electrodes. Figure courtesy Cleveland Clinic.

1.2 Existing Methods of Low Power Stimulation

Stimulators typically use current sources to control total charge and charge density precisely. By controlling charge, it is possible to achieve charge-balance, required for safety of stimulation. By controlling charge density, we can be assured that the electrode will not become polarized at any point during the stimulation, thereby causing potentially irreversible and harmful redox reactions. The primary disadvantage of current-source-based stimulation is energy efficiency. As will be described in great detail in Chapter 4, the energy efficiency of a current source stimulator can be improved upon several times by using a voltage-based stimulator with appropriate feedback controls.

Voltage-based stimulators are occasionally used, and may possibly be used in some commercial

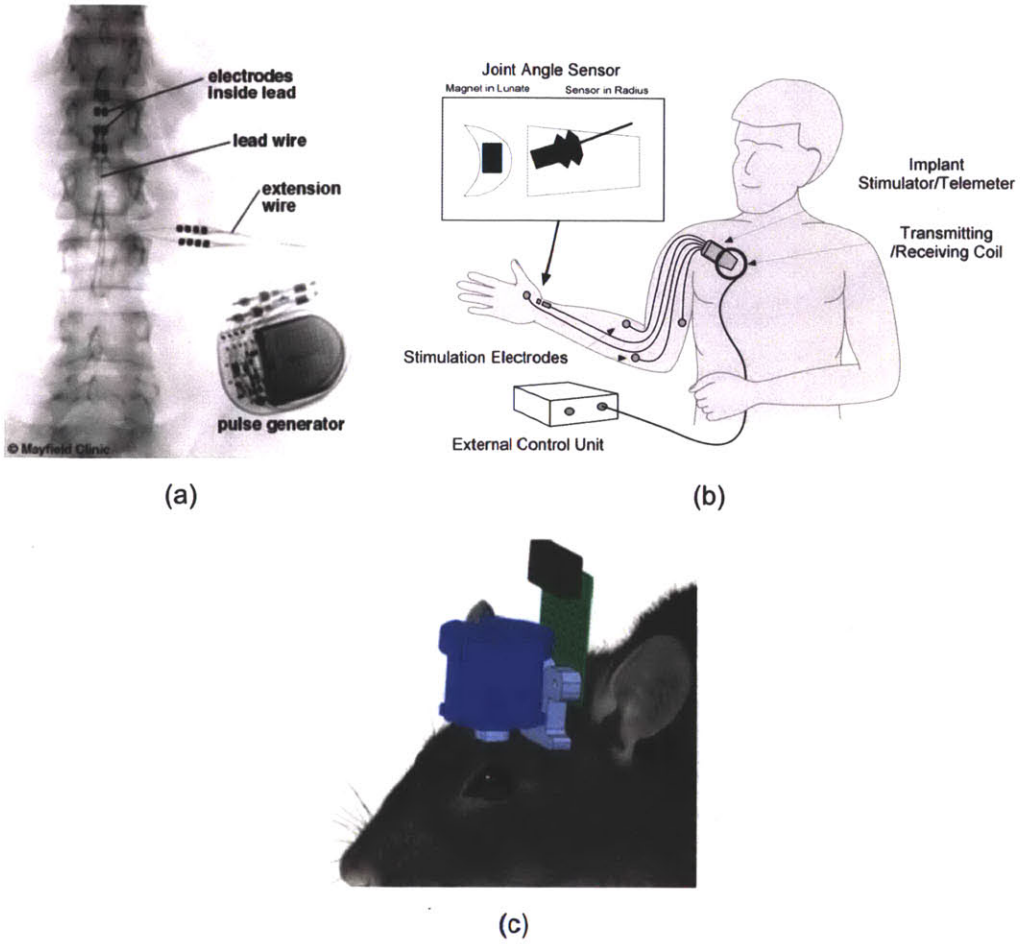


Figure 1-2: Additional stimulator applications examples. (a) Recording/stimulating headstage for experimental neuroscience. Figure courtesy Plexon. (b) Spinal cord stimulator. Figure courtesy Mayfield Clinic. (c) Example FES hand grasp system. Figure courtesy United States Department of Veterans Affairs.

implementations (the details of which are generally not available), with appropriate charge-monitoring and/or cancellation circuitry. The primary advantage of voltage based-stimulation is energy efficiency. However, charge monitoring and control becomes more complicated in voltage-based stimulators. In addition, the full potential of voltage-based stimulation is only realized if the voltage source is designed to actively *track* the voltage of the electrode itself. In my own research and experimentation with commercially available models, there is no evidence that any commercial stimulator behaves in this way.

Figure 1-3 shows an example of a typical electrode voltage resulting from a charge-balanced, biphasic current stimulation pulse. The most efficient possible stimulator operates simultaneously as a voltage source and current source, applying the desired electrode current and the desired electrode voltage at the same time, thereby tracking the anticipated electrode voltage waveform that would

have resulted from the desired stimulation if it were applied as a charge-balanced, biphasic pulse of current.

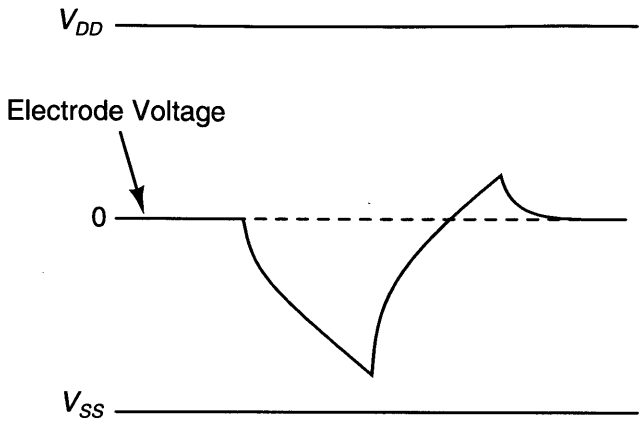


Figure 1-3: Example of a typical electrode voltage resulting from a charge-balanced, biphasic current stimulation pulse.

One example of a voltage based stimulator designed to *adiabatically* track electrode voltages is due to Kelly (Kelly and Wyatt, 2011), and shown in Figure 1-4. In this design, the input to the system is not a DC voltage, but an AC voltage V_s. Synchronous rectifiers tuned to particular voltages pluck away energy from the input waveform and charge the capacitor bank (seen as 3 capacitors $C_1 - C_3$) to a set of specific voltages. Once the capacitors are charged, the electrode is driven by connecting the electrode to the various capacitors in sequence over time, resulting in a step-like voltage waveform. The synchronous rectifiers are always operating, keeping the capacitor bank topped off as energy is taken from them by the electrode.

If the electrode impedance was as predicted, the electrode current will be correct. If the electrode impedance varies in any way, the resulting current will be different from what was desired. This will lead to inefficiencies and could also result in ineffective stimulation and tissue damage. Since each capacitor stores only a single voltage, and many voltages are required to produce an accurate stimulation waveform, many capacitors are required per stimulating electrode, a clear disadvantage of this design in terms of size and cost.

It is possible to improve the accuracy of the current delivered by the capacitor bank design by designing each step voltage to be somewhat larger than needed, and using a series current limiter to restrict the current to the desired value. This is more energy efficient than using current limiters connected to large DC power supplies, as in the conventional stimulator, but is less efficient than simply applying the correct electrode voltage in the first place.

This thesis describes an energy-efficient stimulation system which seeks to improve upon the limitations of previous voltage-based stimulators. In particular, this improved stimulator will not require a capacitor bank, but will rely on a single LC circuit to create a continuum possible electrode voltages, and will utilize current feedback to establish and control the electrode current accurately without the need for series current limiters.

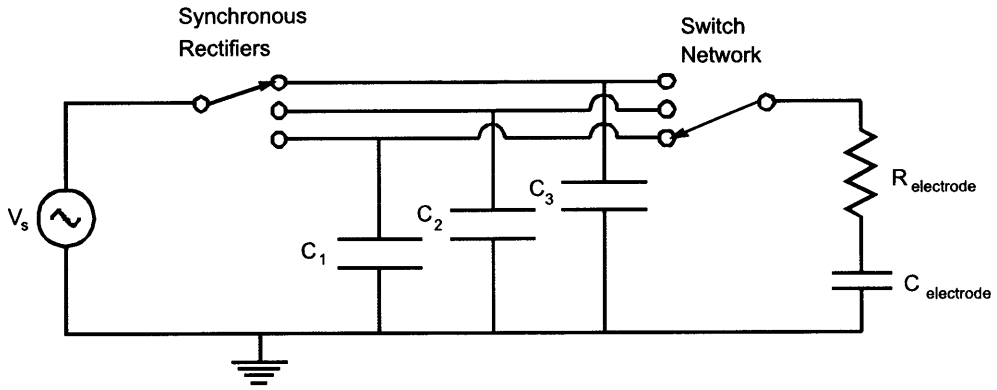


Figure 1-4: Efficient stimulation system based on stepped voltages. Figure credit: Shawn Kelly

1.3 Organization of Thesis

This thesis is primarily the compilation of two papers on two different types of tissue stimulators, one published, the other under review. They are:

- Arfin SK, Long MA, Fee MS, Sarpeshkar R (2009) Wireless Neural Stimulation in Freely Behaving Small Animals. *J Neurophysiol* 102:598–605.
- Arfin SK, Sarpeshkar R. An Energy-Efficient, Adiabatic Electrode Stimulator with Inductive Energy Recycling and Feedback Current Regulation. *IEEE T Biomed Circ Syst*, under review.

I will briefly describe each chapter of this thesis. Chapter 2 is a reproduction of the paper, *Wireless Neural Stimulation in Freely Behaving Small Animals*. The paper describes a miniature, lightweight (1.3 g), and low-power wireless neural stimulation system which I designed and built, and the results obtained from an experiment involving the modulation of the song of zebra finches using the wireless neural stimulator. Dr. Michael Long performed the surgeries on the zebra finches. Professors Michale Fee and Rahul Sarpeshkar were advisers on the project.

In Chapter 3, I introduce the concept of an adiabatic neural stimulator. I begin by first reviewing essential principles of electrodes and then describe how these principles may be applied to the design

of an adiabatic stimulator. In Chapter 4, I describe the design and measurement of an integrated circuit that implements an adiabatic neural stimulator. The text of this chapter is from the paper entitled *An Energy-Efficient, Adiabatic Electrode Stimulator with Inductive Energy Recycling and Feedback Current Regulation.* The manuscript is currently under review with the IEEE Transactions on Biomedical Circuits and Systems.

In Chapter 5, I provide additional measurements and discussion of the energy-efficient, adiabatic electrode stimulator. In Chapter 6, I describe future work and conclude the thesis.

I have also spent considerable time studying analog filters, particularly low-power $G_m - C$ filters. In Appendix A, I have summarized some of my findings.

1.4 Contributions of Thesis

This thesis contributes in two major areas: In the area of experimental neuroscience, I have:

1. Developed a miniature, implantable, wireless neural stimulator for use in freely behaving small animals.

2. Developed a sleep mode and wireless wake up circuit achieving a 2.5x reduction in static power consumption.

3. Applied techniques of low power circuit design to create a device that occupies a footprint of just 1.7 cm^2 and weighs just 1.3 g including batteries which can operate for up to 12 days of continuous experimentation on a 5 mAh battery without recharging.

The second area this thesis contributes towards concerns improvements in the efficiency of electrode stimulators themselves. I have:

1. Developed a dynamic power supply based on inductive energy recycling to efficiently charge or discharge an electrode.

2. Developed an algorithm for feedback current regulation of a programmable stimulation current.

3. Developed a dual-loop control strategy comprising a fast inner voltage control loop and an outer slow current control loop that monitors the electrode current and adjusts the electrode set voltage adiabatically to maintain a constant current through the electrode independent of electrode impedance.

4. Developed a current sensing circuit that operates in shunt with the electrode. The current sensing circuit draws essentially no current from the electrode and naturally contributes no energy dissipation or reduction of electrode voltage headroom.

5. Identified the fundamental physical limits of energy efficiency and matched theory to experiment in an *in-vitro* electrode stimulator.

6. Demonstrated the first voltage-based stimulator which controls current without the use of current limiters, and is thus able to approach theoretical limits for electrode energy efficiency.

7. Demonstrated a practical implementation of these ideas in a micropower integrated circuit stimulator that improves energy efficiency by 2x-3x over traditional current source stimulators.

Chapter 2

Wireless Neural Stimulation in Freely Behaving Small Animals

2.1 Abstract

We introduce a novel wireless, low-power neural stimulation system for use in freely behaving animals. The system consists of an external transmitter and a miniature, implantable wireless receiver-and-stimulator. The implant uses a custom integrated chip to deliver biphasic current pulses to 4 addressable bipolar electrodes at 32 selectable current levels (10 μA to 1 mA). To achieve maximal battery life, the chip enters a sleep mode when not needed and can be woken up remotely when required. To test our device, we implanted bipolar stimulating electrodes into the songbird motor nucleus HVC (formerly called the high vocal center) of zebra finches. Single-neuron recordings revealed that wireless stimulation of HVC led to a strong increase of spiking activity in its downstream target, the robust nucleus of the arcopallium (RA). When we used this device to deliver biphasic pulses of current randomly during singing, singing activity was prematurely terminated in all birds tested. Thus, our device is highly effective for remotely modulating a neural circuit and its corresponding behavior in an untethered, freely behaving animal.

2.2 Introduction

The stimulation of neuronal circuits with electrical current is a highly valuable tool within the field of neuroscience. Electrical stimulation has previously been used to probe connectivity (Hahnloser et al., 2002; Swadlow, 1998), to elicit (Berg and Kleinfeld, 2003; Jasper and Penfield, 1954) or

modify (Talwar et al., 2002), certain behaviors, to bias sensory perception (Houweling and Brecht, 2008; Salzman et al., 1990), or to treat a range of neurological conditions (Bittar et al., 2005; Krack et al., 2003; Moritz et al., 2008; Tarsy et al., 2008).

Standard stimulation experiments require that the subject be physically tethered to a stimulator with a bundle of electrical wires, an arrangement which has a number of practical disadvantages. For instance, the tether limits the full range of motion of the animal and can become tangled or twisted over long periods of time (Fee and Leonardo, 2001). Furthermore, the tether can also cause undue stress to the animal, potentially restricting spontaneous behaviors. To avoid these issues, we designed a wireless neural stimulation system for use with freely behaving animals. A number of major technical challenges had to be met in order to develop a wireless stimulator. Since the vast majority of behavioral research is conducted on small laboratory animals such as mice (30-35 g), the device has to be light enough to be easily carried. Without a wire available to provide power, an independent power source, such as a battery, must be used. Unfortunately, a battery contributes a significant amount of weight, all of which must be borne by the animal. The power consumption of the implantable device must be as low as possible to minimize the size of the battery. Furthermore, removing the animal from the experiment for frequent battery changes is often not desirable. Existing wireless stimulating devices that were assembled from commercial, off-the-shelf (COTS) components were either too bulky or heavy for use with small animals, or they required more power than was available from a practically sized battery (Mavoori et al., 2005; Peng et al., 2004315). Other designs used application specific integrated circuits (ASIC), which helped reduce size. However, these devices often employ a transcutaneous wireless inductive power source rather than a battery (Coulombe et al., 2007; Ghovanloo and Najafi, 2007; Sarpeshkar et al., 2008; Theogarajan, 2008), which has a limited range (1-10mm) that is far too small for use with freely behaving animals (Baker and Sarpeshkar, 2007). In addition, the power requirements of these designs are too high for use with a battery size that is practical on small animals. Therefore, we chose to explore a compact, ultra-low-power, ASIC-based implementation that could function on a tiny battery. We also designed the device to automatically enter a low-power sleep mode when not being used. Our device is simultaneously small in size, weight, and low in power. We will describe how we achieved these specifications, and show the performance of the device in manipulating neural circuit dynamics and behavior in a freely moving small animal.

2.3 Methods

2.3.1 General Overview of the System Design

The wireless stimulator consists of two parts: an external transmitter, controllable through a computer interface, and a miniature, implantable wireless receiver-and-stimulator (Figure 2-1). A block diagram of the wireless neural stimulation system illustrates the division between external and implantable components (Figure 2-2). The implantable device is assembled on a miniature printed circuit board (PCB), and contains an off-chip receiver coil, a custom integrated circuit for data demodulation and neural stimulation, and batteries. The chip is capable of delivering biphasic current pulses to 4 addressable electrode sites at 32 selectable current levels ranging from 10 μA to 1 mA. To achieve a long operating time from minimally sized batteries, an automatic standby mode decreases static power consumption during periods of inactivity. Table 2.1 lists the detailed specifications of the device including size, weight, power, stimulus capabilities, and lifetime.

Table 2.1: Wireless Neural Stimulator Specifications

Board Dimensions	1.3 cm × 1.3 cm
Mass with batteries	1.3 g
Stimulation Sites	4, bipolar
Stimulation Range	0.01 - 1 mA in 32 steps
Stimulation Duration	180 μs / phase, biphasic
Maximum Stimulation Rate	1400 Hz
Electrode Voltage Compliance	5 V
Power Consumption, standby	20 μW
Power Consumption, awake	50 μW
Power-up time	approximately 30 μs
Operating Time	approximately 12 days on standby (typical conditions)
Transmitter Range (16 V power supply, 272 mW power consumption)	20 cm (typical)
Transmitter Coil Diameter	17 cm
Bird Cage Interior Dimensions	18 cm width, 18.7 cm depth, 15 cm height
Chip Fabrication Process	AMI 0.5 μm CMOS

2.3.2 Data Transmission using Magnetic Near-Field RF Telemetry

Data are transmitted via a near-field, magnetic link. The transmitter coil is a part of a resonant Colpitts oscillator transmitter circuit (Figure 2-3). The transmitter is positioned externally, just

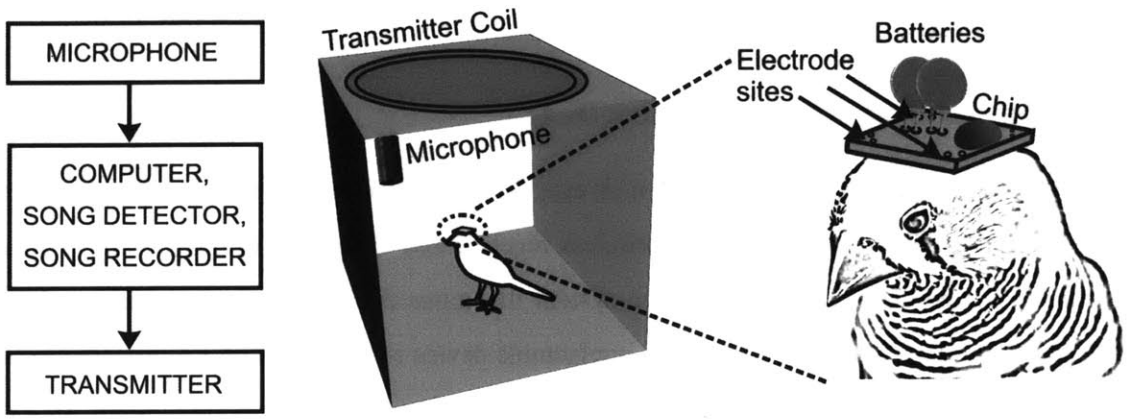


Figure 2-1: A broad overview of the wireless neural stimulation system showing the bird cage, external transmitter, and bird with implantable device. In behavioral experiments, the system was used with a microphone and a song detector to automatically operate the stimulation device during singing. Also shown is a close-up of the implanted stimulation device mounted atop the head of a zebra finch with the chip, batteries, and electrode sites (4 sites total, 1 per corner).

outside the animal's cage (Figure 2-1).

The receiver is only able to pick up a small fraction of the total magnetic flux generated by the transmitter. A preamplifier (Figure 2-4), which provides both passive and active gain, amplifies the received signal to suitable levels. The output of the preamplifier is used to drive the input of a peak detector (not shown), which recovers the modulation input used at the transmitter. A comparator (not shown) is used to restore the peak detected waveform to a full-scale digital signal (V_{comp}).

Data are encoded in two layers. First, a digital data sequence is pulse-width modulated (PWM), a self-clocking return-to-zero coding scheme. The PWM signal is then fed to the transmitter, which on/off keys a sinusoidal carrier. Although PWM consumes additional bandwidth through return-to-zero modulation, it is advantageous in a low-power system because complicated clock recovery circuits are unnecessary. The choice of near-field coupling is important for saving power because low carrier frequencies (13.5 MHz) can be used. Although low carrier frequencies can restrict bandwidth, the bandwidth requirements for this neural stimulation application are low because only a limited set of stimulation commands need to be transmitted infrequently. With a data rate of 25 kbps, a stimulation triggered on 16 bits of data requires a latency of about 700 μs.

It should be noted that near field magnetic coupling is directional. However, there are no blind spots in the cage for reasonable orientations of the headstage. We tested the device for the maximum possible range (vertical distance from the transmitter) at three possible tilt angles (0, 45, and 60°), and two possible horizontal positions (0 cm (on-axis with the center of the transmitter coil), and 8.5 cm (the edge of the transmitter coil)). The results indicate a maximum range of 24 cm, and

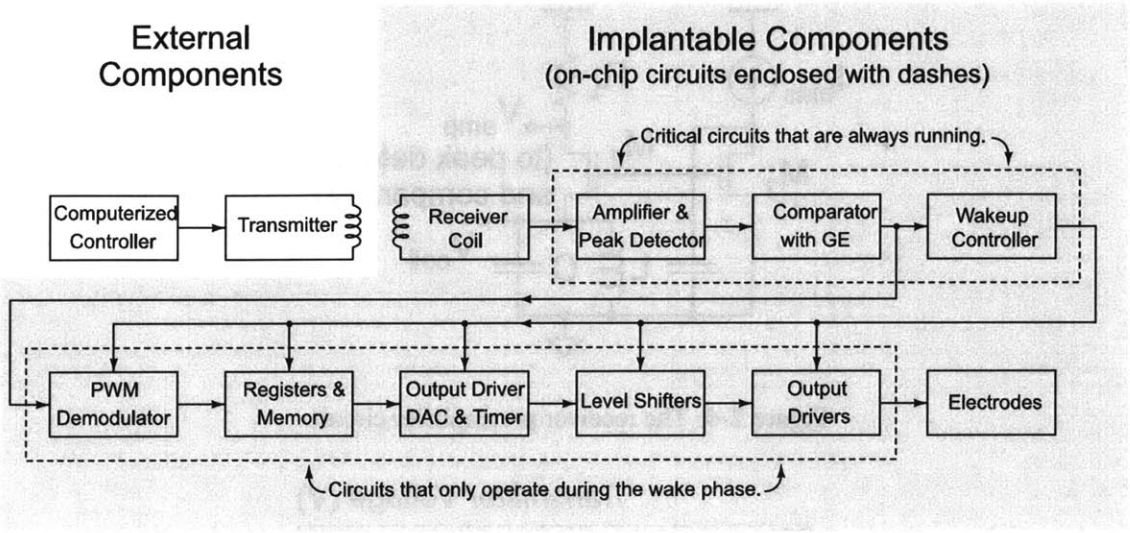


Figure 2-2: A complete block diagram of the wireless neural stimulation system.

a range of 14.5 cm at a horizontal displacement of 8.5 cm and a tilt angle of 60°, a considerably awkward and unlikely position for the bird. Thus, even under extreme conditions, the stimulation device still has 14.5 cm of vertical range. For typical conditions, the range of the transmitter and receiver is about 20 cm.

The circuit topologies are also robust to large signals. For example, should the bird closely approach the transmitter coil, the received signal may become so large that preamplification is no longer necessary. However, the circuit topology can handle large signals easily because the output of the preamplifier stage will simply saturate at the power supply level if the input is large. The subsequent peak detected levels are therefore limited as well.

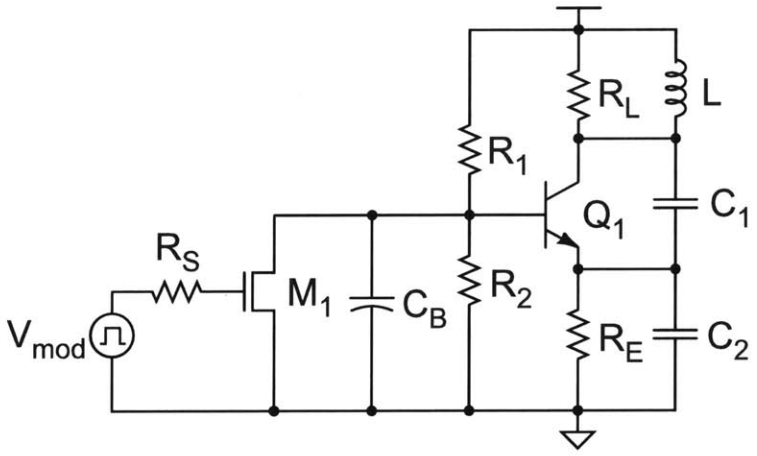


Figure 2-3: The Colpitts oscillator-transmitter circuit.

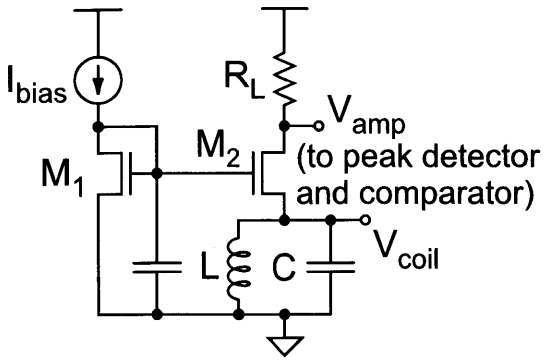


Figure 2-4: The receiver preamplifier circuit.

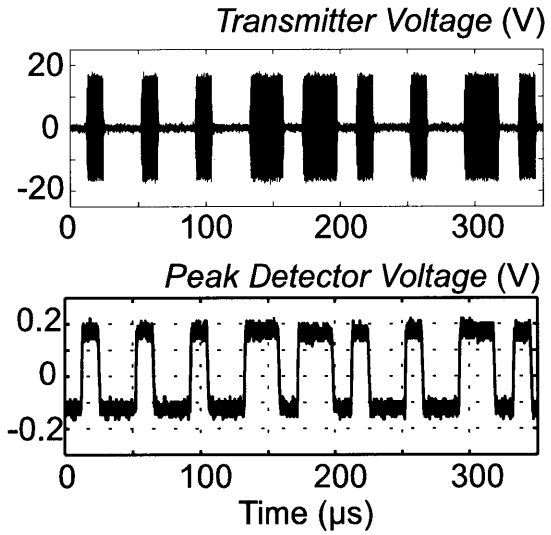


Figure 2-5: *Top*, Modulated voltage at the output of the RF transmitter. *Bottom*, the output of the peak detector, showing the recovered amplitude modulation signal of the carrier.

2.3.3 Low-power sleep mode

To conserve power when stimulation is not needed, the receiver chip automatically enters into a low-power sleep mode where all circuits are shut down except for the preamplifier, peak detector, and comparator, which run continuously, awaiting any RF signal from the transmitter. The wakeup controller with glitch eliminator (GE) (Figure 2-6) continuously monitors the comparator output, checking for level transitions. When a transition is detected, a digital timer is reset to its highest value and all the remaining circuitry on the chip is powered up. The timer is constantly reset with every level transition of the incoming data. If no data is received for 1 second, the timer expires and the chip powers down. This circuit allows the chip to wake up remotely and immediately on the first data bit.

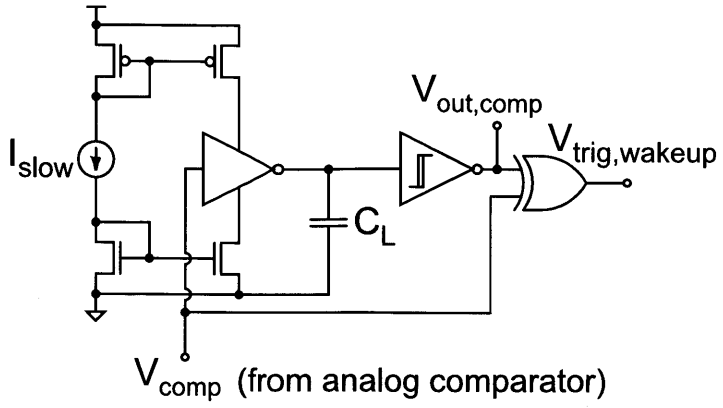


Figure 2-6: The XOR-based "wakeup" detector circuit with glitch eliminator.

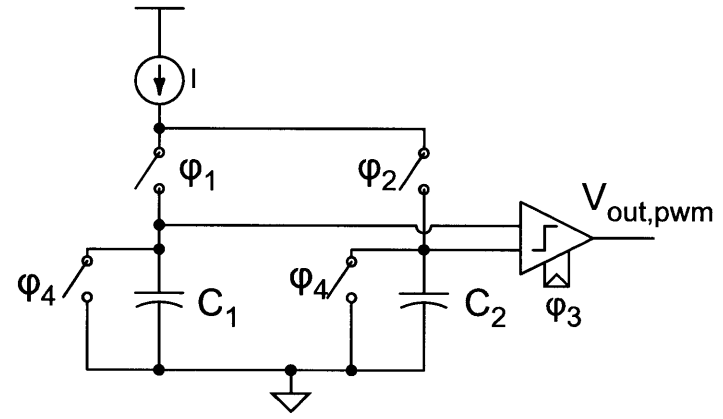


Figure 2-7: The simplified PWM demodulator.

We have operated the implanted device on a single battery charge for up to 8 days without completely discharging the batteries. The device can be used theoretically up to 15 days on standby based on battery-capacity and power-consumption figures. For experiments with frequent stimulation (e.g., 100 μA stimuli of 5 pulses each to 4 electrodes, 5000 times per day, 1000 sleep/wake cycles), power consumed by the output stage reduces running time by about 15% from the standby time alone. The additional power consumed comes from the bias current for the output driver circuits as well as the stimuli themselves. In the worst case with 1 mA pulses, running time may be reduced by about 60%.

2.3.4 Data demodulation and decoding

The receiver chip is equipped with a PWM demodulation circuit (Figure 2-7). The circuit determines in a given bit period whether $V_{out,comp}$ was logical high for greater than or less than half of the period

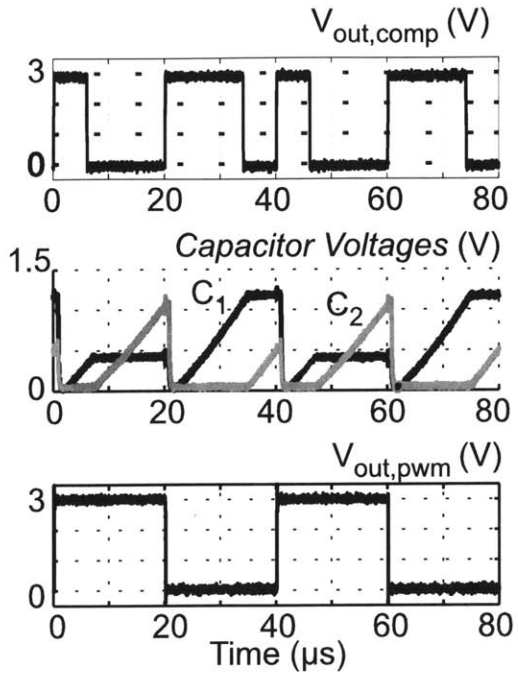


Figure 2-8: Example of the PWM demodulator operating. V_{comp} is a thresholded version of the peak detector voltage (2-5). $V_{out,comp}$ is the same as V_{comp}, but with glitches removed (2-6). The PWM demodulator converts the timing of $V_{out,comp}$ into analog voltages stored on capacitors C_1 and C_2. Comparison of the two capacitor voltages at the end of each period determines $V_{out,pwm}$, which always lags $V_{out,comp}$ by a full data period.

(Figure 2-8). A bit period starts with a rising edge of $V_{out,comp}$ and ends on a subsequent rising edge of $V_{out,comp}$. Hence, the demodulated data ($V_{out,pwm}$) contains half of the number of transitions as $V_{out,comp}$, and every falling edge of $V_{out,comp}$ occurs only after $V_{out,pwm}$ has reached a stable value. For this reason, falling edges of $V_{out,comp}$ are used to subsequently "clock" $V_{out,pwm}$ into a shift register. The shift register converts serial data into parallel words. These words configure a DAC (digital-to-analog converter) which sets the stimulation current level, selects a specific output driver, and triggers a timer circuit, initiating a biphasic current pulse on the desired electrode pair at the chosen current level.

2.3.5 Electrical Stimulation

There are four output driver cells on the chip - one for each pair of electrodes. The output driver circuit implements a floating bipolar current source (McDermott, 1989). The chip has one central DAC circuit which sets a reference current used to generate the actual stimulation current. A set of current mirrors copy the DAC current to the appropriate output driver transistors. Although only one output driver can be active at a time, new data can be transmitted to the chip while simultaneously

delivering a stimulation charge, making it possible to stimulate multiple times in rapid succession at either the same or different sites. Off-chip series DC (low frequency) blocking capacitors are installed on the circuit board between the electrode drivers and the electrodes to prevent tissue damage (Brummer and Turner, 1977).

It should be noted that data transmission is asynchronous and not continuous, meaning that data is only transmitted when stimulation is required. Further, the receiver circuit has no knowledge of when a transmission will begin. For this reason, a unique recognition sequence is used at the start of every transmission to allow the receiver to determine which bits are valid and when. A parity check also detects errors and ignores stimulation requests that contain errors. Errors are rare but become more common as the receiver moves out of range of the transmitter. In addition, spacer bits must be transmitted to prevent intended data from mimicking the recognition sequence.

Because there is no back-telemetry from the chip to the transmitter, it is not possible to tell directly whether or not the stimulus was applied. To address this issue, we connected a light emitting diode (LED) to one of the unused stimulation channels, effectively reducing the number of channels from 4 to 3. To confirm that the device was working, we used the stimulator to turn on the LED remotely, thus giving visual confirmation that the signal was correctly received. Although this method cannot easily confirm that every individual stimulation command was correctly received, this is a useful way to allow one to periodically "check" the device to make sure it is still working.

2.3.6 Detailed Circuit Operation

Colpitts Oscillator/Transmitter (Circuit: Figure 2-3, Operation: 2-5): To turn the oscillator on and off, M_1 is operated as a switch by the PWM data, referred to here as V_{mod}. If V_{mod} is low, M_1 behaves as an open circuit and can be ignored. If V_{mod} is high, M_1 turns on and creates a low impedance path to ground, rapidly discharging C_B. As the base of Q_1 is brought to ground, the oscillation quickly dies. When M_1 is opened, C_B begins to charge through R_1 and R_2. As Q_1's base returns to its normal operating point, the oscillation restarts. The inductor L functions both as the transmitter coil and to set the resonant frequency of the oscillation, along with capacitors C_1 and C_2. A list of parts and component values is provided in Table 2.2. Supplementary Figure S13 (Section 2.6) provides additional information on the creation of the PWM signals and the organization of the data packet.

The transmitter typically operates from a relatively large power supply voltage of about 16 V. This high supply voltage is necessary to maintain a wide communication range with the stimulation device. Power consumption in the transmitter is about 270 mW, which can be supplied by wall power.

Table 2.2: Transmitter Parts List

Q_1	2N2222
M_1	NDS351AN
R_1 and R_2	10 kΩ
C_b	1 nF
R_L	Not used (replace by open circuit)
L	700 nH
C_1	220 pF, tunable
C_2	680 pF
R_S	Not used (replace by short circuit)

Receiver Preamplifier (Circuit: Figure 2-4): The LC circuit at the source of M_2 is formed by the printed coil on the PCB as well as a surface-mount capacitor. As flux is picked up by the coil, the LC circuit resonates, providing a passive voltage gain of Q at V_{coil}, where Q is the quality factor of the tuned circuit, approximately 25. The signal at V_{coil} is then amplified by M_2 functioning as a common-gate amplifier with output V_{amp}. The amplifier is biased by the current mirror $M_1 - M_2$, as the inductor L is a short circuit at DC. The bandwidth of the amplifier is set by parasitic capacitance at the output of the amplifier and R_L. In this design, R_L is 80 kΩ, the bias current of M_2 is 5 μA, the overall voltage gain is 10, and the bandwidth was simulated at 30 MHz. The amplifier operates close to the MOSFET (metal-oxide-semiconductor field-effect transistor) weak inversion region, providing power-efficient voltage gain (Comer and Comer, 2004; Tsividis, 1999).

Peak Detector (Operation: Figure 2-5) and Comparator: The peak detector circuit is similar to a source-follower, but with an intentionally small bias current and large load capacitor, forming a slow time constant. When driven with high frequency signals beyond the linear range of the input transistor, rectification occurs. A comparator restores the peak detected waveform to a full-scale digital signal.

Wakeup detector and glitch eliminator (Figure 2-6): First, any brief, spurious transitions (glitches) in the comparator output V_{comp} are removed by passing the signal through an inverter with an intentionally slow transition time. Thus, brief signals are not passed by the inverter. For valid signals that do pass, the slow edges are sped up by a Schmitt trigger before entering the XOR gate. In addition to removing glitches, the GE also introduces a delay into the comparator signal, which is necessary for the wakeup detector to work. The comparator output, along with a slightly delayed copy of itself, $V_{out,comp}$ is fed to an XOR gate. Whenever a transition in V_{comp} occurs, $V_{out,comp}$ temporarily differs, causing $V_{trig,wakeup}$ to enter the high state. This signal triggers the wakeup timer

and powers up the rest of the chip if needed.

PWM Demodulator (Circuit: Figures 2-7, Operation: 2-8): Assume that initially, all switches are open. The voltages on C_1 and C_2 are assumed to be zero. When the modulated data level ($V_{out,comp}$) goes high, switch ϕ_1 closes and charges C_1 with current I. When $V_{out,comp}$ changes from high to low, switch ϕ_1 opens and ϕ_2 closes, charging C_2 with I. At the end of the bit period, switch ϕ_2 opens and ϕ_3 momentarily goes high to latch the output of the comparator and update $V_{out,pwm}$. After $V_{out,pwm}$ has been latched, ϕ_4 briefly closes the two reset switches to return the voltages on C_1 and C_2 to zero. The PWM modulator effectively converts durations into voltages, and reports an output corresponding to whether the input signal ($V_{out,comp}$) was predominantly high or low during a given bit period.

Additional circuitry (Figure 2-2) employed includes shift registers and memory, an output driver DAC and timer, level shifters, and output drivers. The shift registers for receiving incoming data and memory for storing this data are designed from a digital standard cell library (Tanner Research). The output driver DAC is a digitally controllable current source consisting of a set of binary weighted current sources, which are switched on or off and then combined in accordance with the stimulation parameters.

The stimulator chip requires a dual power supply. A single battery (Panasonic ML621) powers all the integrated circuits except for the output drivers, which require a larger power supply for wider voltage compliance. The dual power supply is achieved by adding an additional battery (Panasonic ML614) in series with the first battery to double the power supply. A set of level shifters amplify the output driver control signals running at the lower supply up to the level required for the higher supply.

For complete schematics of the entire custom integrated circuit, see the Supplementary Materials, Figures S1-S11, located in Section 2.6.

2.3.7 ASIC and PCB Fabrication

The ASIC was fabricated in a 0.5 μm CMOS (complementary metal-oxide-semiconductor) process (AMI Semiconductor). The PCB for the stimulator chip, including receiver coil, was fabricated by Advanced Circuits. Advanced Circuits also fabricated the PCB for the transmitter circuit. Supplementary Figure S12 (see Appendix **??**) provides the layout and required components for the PCB.

2.3.8 Animals and surgery

Adult (> 100 days post hatch) male zebra finches (Taeniopygia guttata) were obtained from our breeding colony or from a commercial breeder. Birds were housed under constant 12 h light/dark conditions and given unlimited food and water. All procedures described here were approved by an institutional animal care and use committee at the Massachusetts Institute of Technology.

Prior to surgery, birds were anesthetized with 1-2% isofluorane in oxygen and placed in a stereotaxic apparatus. Craniotomies were made bilaterally above HVC (1.9 to 2.7 mm lateral; 0 to 0.5 mm anterior to the bifurcation of the midsagittal sinus). Two stimulating electrode pairs (600 μm separation), constructed from 50 μm teflon coated stainless steel wire (California Fine Wire Company) were stripped 300 μm at the tips and implanted to a depth of 500 μm in each HVC. Once the electrodes were in place, the device was secured to the bird's skull with dental acrylic. After surgery, birds were placed inside sound isolation chambers and allowed to recover and acclimate to the chamber.

2.3.9 Acoustic recording and automatic electrical microstimulation

An adult male zebra finch was placed inside a sound isolation chamber, and a microphone (Audio Technica AT803B) was placed inside the chamber external to the cage. Stimulation parameters were set in advance on a computer which would generate the pulse-width modulated data sequence and transfer it to the memory of an arbitrary waveform generator (Agilent 33250). The PWM data could be recalled on command and sent to the transmitter. The data transmission specifies stimulation sites, number of pulses, and pulse intensity. The neural stimulation device receives and decodes the data stream and provides the desired neural stimulation.

Sound inside the chamber was continuously monitored with Sound Analysis Pro software. When the software detected spontaneous birdsong, the sound was recorded to disk. Simultaneously, the microphone signal was sent to an external electronic circuit to also detect birdsong and trigger the wireless transmitter after a random delay (Figure 2-9). The random delay was achieved by gating the song detector output with an independent oscillator. Since singing in isolation occurs spontaneously and randomly, the bird's song will also fall into phase with the delay oscillator at random. The objective was to apply electrical stimuli to HVC approximately once per motif, at a random time within the motif. The motif is a repeated unit of song substructure approximately 0.5-1.0 s in duration. The time of the neural stimulation was also marked onto the audio recording with an out-of-band

tone so it could be identified later during analysis of the obtained recordings.

Motifs were recorded in this manner on 4 birds. For 3 of the 4 birds, stimuli were a train of 5 bipolar, biphasic (0.18 ms/phase) pulses per hemisphere at 10, 40, 70, or 100 μA. The fourth bird was tested at only a single current level. Approximately 150 motifs were collected per bird, per level of stimulation. Motifs were analyzed using in-house computer software which computed spectral and envelope information from the sound recordings. A consistent threshold for each bird was used to segment the audio into syllables and determine their duration. Syllables were classified by hand.

Typical electrode voltages during stimulation were measured by probing the electrode attachment points on the stimulator device and captured on a Tektronix TDS3014 digital oscilloscope. In anesthetized birds, stimuli were also applied unilaterally to HVC at 1 second intervals and responses were recorded from single neurons in RA with a carbon fiber electrode (Carbostar-1, Kation Scientific, Inc.).

2.3.10 Histology

Birds were deeply anesthetized with urethane and perfused with phosphate buffered saline and paraformaldehyde. 100 μm sections were cut parasagittally with a vibrating microtome (Vibratome 1000) for verification of forebrain electrode placement. The tissue slices were imaged using dark-field microscopy (Zeiss Axioplan 2).

2.3.11 Electrophysiology

Single-unit electrophysiology in RA was carried out in a manner similar to that described previously (Hahnloser et al., 2006), except these recordings were performed in anesthetized (1.0-1.5% isoflurane) zebra finches. Briefly, glass microelectrodes were fabricated on a vertical puller (Narishige PE-21) and filled with 2 M sodium acetate. Electrode tips were broken to achieve a final resistance of 10-15 MΩ. Signals were amplified using an Axoclamp 2B (Axon Instruments).

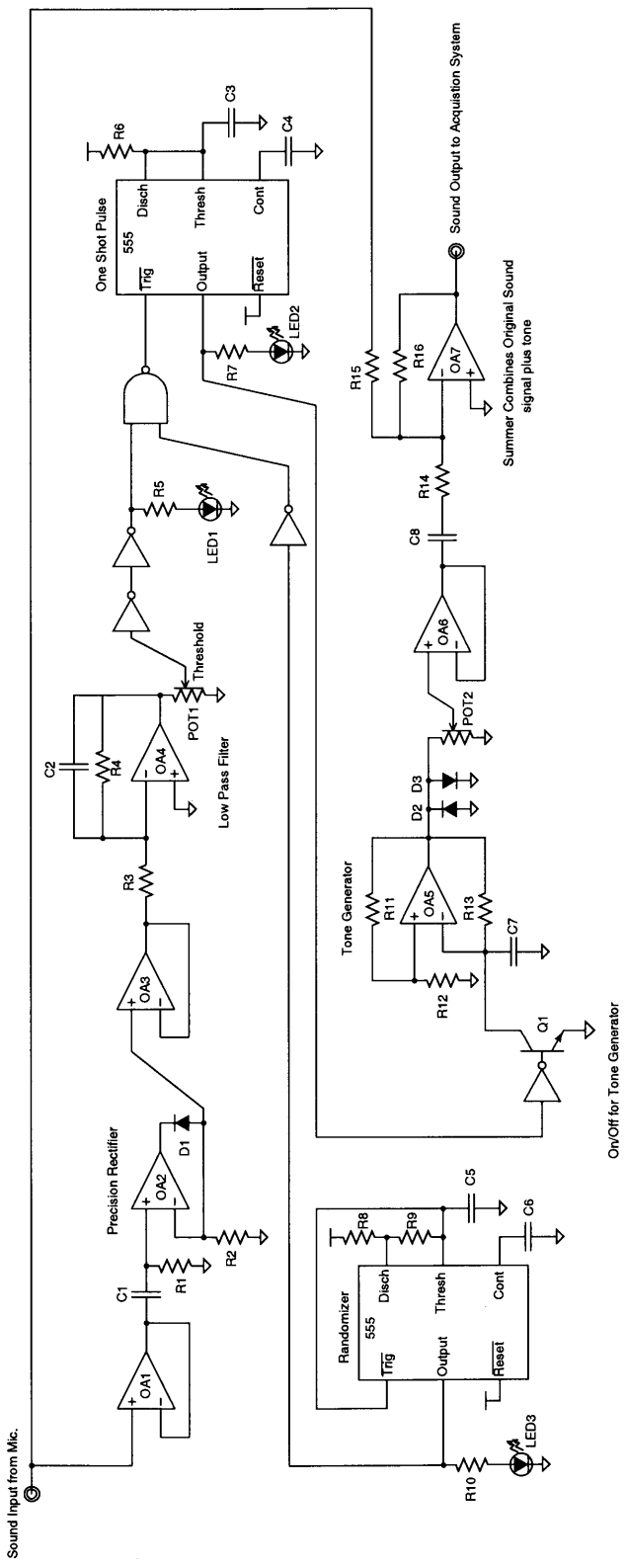


Figure 2-9: Song Detector Circuit Schematic.

2.4 Results

2.4.1 *In vivo* implementation of wireless stimulator

To test the viability of our stimulator, we used the zebra finch as our model system. The zebra finch generates a well-documented behavior (singing) that is mediated by a set of dedicated song control nuclei (Figure 2-10). Included in this motor pathway is nucleus HVC (formerly known as the high vocal center), which is a forebrain region that is critically involved in song production and timing (Fee et al., 2004; Hahnloser et al., 2002; Long and Fee, 2008; Nottebohm et al., 1976; Yu and Margoliash, 1996), which projects to the robust nucleus of the arcopallium (RA). Previous studies have demonstrated that electrical stimuli applied to HVC have resulted in premature truncation of singing behavior (Ashmore et al., 2005; Vu et al., 1994; Wang et al., 2008). We attempted to recreate this behavioral response in order to test the viability of our wireless device. The device was prepared with pairs of bipolar stimulating electrodes (Figure 2-11) and implanted bilaterally into HVC (Figure 2-10). In all four birds used in behavioral experiments, electrodes were histologically confirmed to be within HVC (Figure 2-12).

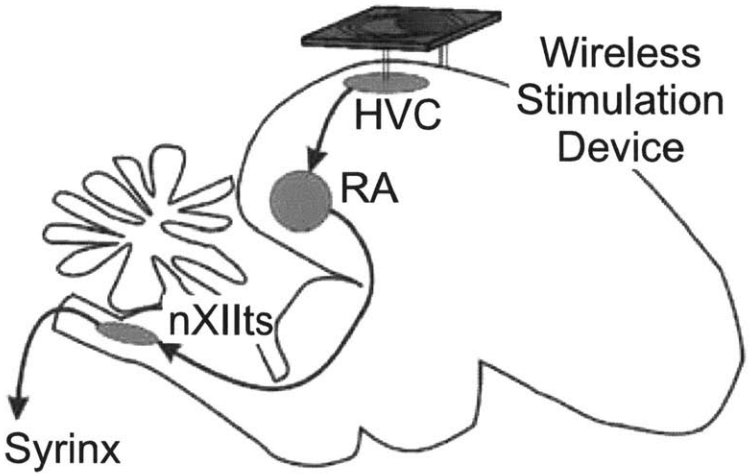


Figure 2-10: Schematic showing the stimulation device and relevant parts of the song production pathway.

2.4.2 Current Source Characterization and Programmability

Electrode voltage was measured in anesthetized zebra finches at the completion of the chronic trials to characterize electrode impedance (Figure 2-13). Biphasic constant current pulses were applied to HVC, and the differential electrode voltage was recorded. As current was increased, electrode

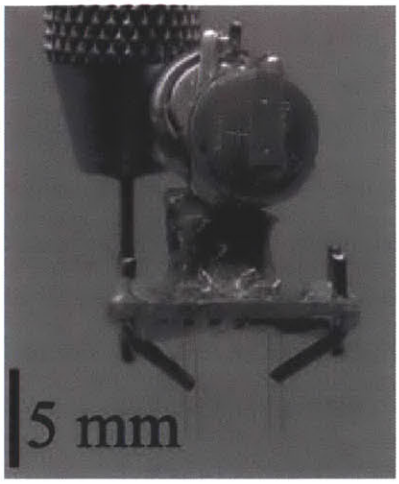


Figure 2-11: The device ready for implantation, showing two pairs of stimulating electrodes, batteries, and structural legs.

voltage also rose, indicating that raising the current level increases the intensity of the stimulation. However, current settings greater than 190 μA caused the electrode back voltage to build quickly and reach the power supply voltage within the duration of the stimulation. As the measured voltage approaches the power supply, the current source transistors are no longer able to supply the desired current, causing the current to decrease. This loss of current control is unavoidable; however, series DC blocking capacitors in the current path guarantee that stimulations were always charge-balanced on average. Increasing the power supply voltage or decreasing electrode impedance could restore function at higher current levels.

The peak voltage deflection as a function of current using 4 separate electrode pairs (Figure 2-14) shows the range of achievable currents in the implanted device. If the current level is set beyond 130 μA, the current becomes unsustainable for the duration of the simulation because of the power supply constraint. Thus, the electrode impedance can limit the range of current control in the stimulation device. To characterize the mapping from the current level setting to achieved current for ideal low-impedance electrodes, a small resistor was used as the load on the stimulation device. In this case, the current is controllable in linear steps and the positive and negative simulation phases are closely matched (Figure 2-15).

2.4.3 Wireless stimulation drives spiking activity in identified single neurons

We demonstrated the operation of the wireless neural stimulation system on single-neuron spiking responses in the zebra finch motor pathway. Electrical stimulation applied unilaterally to HVC

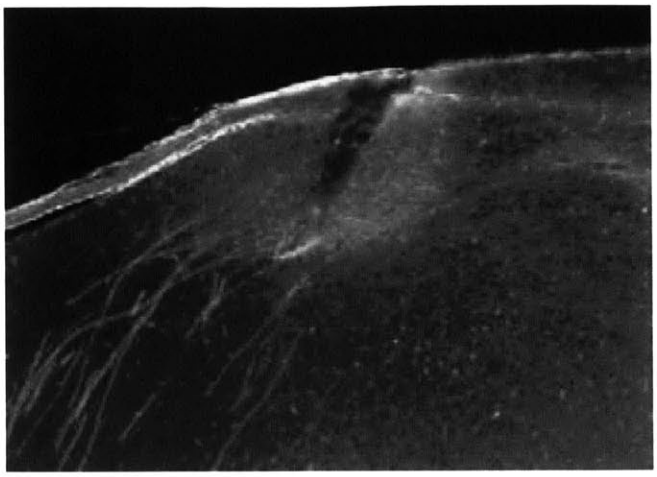


Figure 2-12: Dark-field microphotograph of a 100 μm parasagittal slice of finch forebrain showing HVC, a stimulating electrode track penetrating into that nucleus, and RA projecting nerve fibers (at left).

resulted in time-locked spiking activity in downstream RA neurons in all cases (n = 4 birds). Recordings were made from 12 RA cells at stimulation current levels of 10, 40, 70, and 100 μA (Figures 2-16, 2-17). These current levels are identical to those used in our behavioral experiments (see below).

2.4.4 Wireless stimulation drives behavioral changes in the freely behaving zebra finch

Adult male zebra finch song is composed of motifs approximately 0.5-1.0 s in duration, which may be repeated a variable number of times (Konishi, 1985). These motifs are composed of syllables (periods of continuous acoustic output) approximately 100 ms in length. Both the individual syllable structure and the sequence of syllables comprising a motif are highly stereotyped, meaning that the zebra finch sings each motif nearly identically (Cooper and Goller, 2006; Glaze and Troyer, 2006). Singing may occur in the presence of a female zebra finch or spontaneously in isolation without any external stimulus (Sossinka and Böhner, 1980). We exclusively studied the latter type, known as undirected singing.

Three adult male zebra finches (12-15 g) were implanted with the stimulation device bilaterally in HVC and subject to random electrical microstimulation triggered by singing (5 biphasic pulses per hemisphere, 180 μs per phase). Sufficiently large stimuli applied bilaterally to HVC during singing caused truncation of the ongoing motif (Figure 2-18) (Ashmore et al., 2005; Vu et al., 1994;

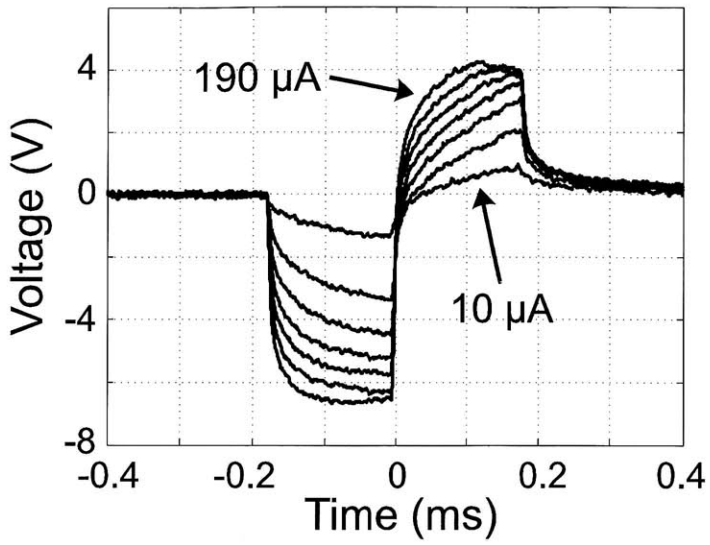


Figure 2-13: Single examples of measured electrode voltages due to unilateral stimulation of HVC. Stimulation currents ranged from 10-190 μA in steps of 30 μA, with larger voltage deflections corresponding to increasing current, as shown. As stimulation current increases, the maximum electrode voltage also increases until the voltage becomes saturated at the power supply voltage. Increasing stimulation current further than shown has no significant effect on the measured electrode voltage.

Wang et al., 2008). On some trials, the song would start again after a brief pause (not shown).

Wireless stimulation led to current-dependent motif truncation in all birds tested (Figure 2-20). The fraction of motifs that were truncated compared to unperturbed motifs increased with increasing simulation intensity, approaching nearly 100% of motifs being truncated for stimulation intensities of 70 μA and greater (Figure 2-19). At this intensity, the mean time to truncation across all Birds 1-3 ranged from 49.5 ms to 60.9 ms. A fourth bird was also implanted bilaterally in HVC, but tested at only a single stimulation intensity by setting the device at the maximum current level (1 mA), which resulted in 96% of motifs being truncated by the stimulation. The stimulation current was not measured and was most likely limited to values much below 1 mA due to power supply saturation (Figures 2-13, 2-14).

2.5 Discussion

The design of a low-power, miniature, implantable wireless neural stimulator for chronic use in small, freely behaving animals has been presented and tested in zebra finches. We have shown that stimulation current level can be modulated remotely. Stimulation using this wireless device led to

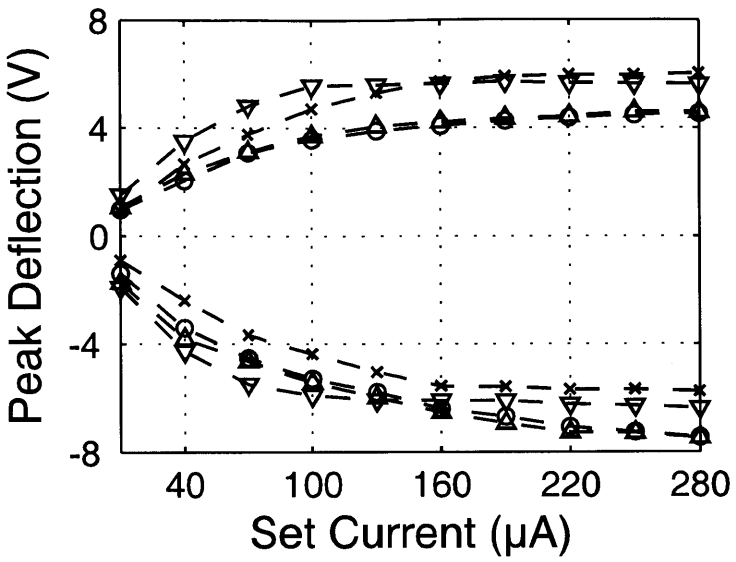


Figure 2-14: The maximum measured electrode voltage during a stimulation, as a function of current. Measurements were made for both the positive and negative phases of the same stimulation, with corresponding peaks shown with like symbols.

larger electrode voltage deflections with increasing current level, increases in spiking activity within the motor pathway, and a greater incidence of motif truncation.

The small size and weight of the device are essential to its success. Small batteries, enabled by a power-conserving wakeup system, helped limit the weight. The device with batteries weighs only 1.3 g, suitable for use in rats and mice as well as zebra finches. We expect that this device will be useful in wireless stimulation experiments applicable to a large body of research animals.

The introduction of this wireless stimulation device to the field of neuroscience opens up vast possibilities for behavioral experiments. For example, experiments where multiple freely behaving animals interact naturally are only feasible with a wireless system because any tethers would become entangled. Experiments that involve an animal passing freely through small openings, such as a boundary between a light and dark area, or between sections of a maze, would be limited by tethers.

The device could also be modified to suit a range of applications. For example, by adjusting the stimulus protocol, revising the circuitry to support higher current levels, and replacing the stimulating electrodes with light emitting diodes connected to optical fibers, the device can provide optical stimulation of neurons (Boyden et al., 2005). The higher power levels currently required for optical stimulation may result in reduced battery life. In this case, experiments using optical stimulation could be performed on a shorter time scale, or the device could be used with larger batteries on

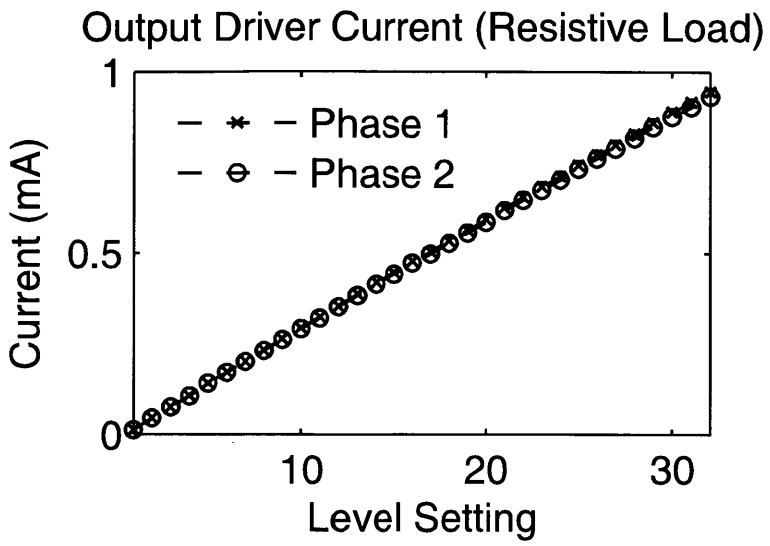


Figure 2-15: The behavior of the stimulator when driving a dummy low-impedance resistive load. The current control is linear, ranging from approximately 10 - 940 μA in steps of 30 μA. The positive and negative phases (Phase 1 and Phase 2) are symmetric.

animals larger than birds. Another possibility is to incorporate a scheme for wireless recharging of the batteries to extend their lifetime.

The device is also small enough that it could be chronically implanted in humans to perform deep brain stimulation (DBS). Deep brain stimulation has been shown to be effective in treating movement disorders such as Parkinson's disease and non-movement disorders such as depression (Kringelbach et al., 2007). However, the mechanisms of DBS are not well understood. Pairing the device with simultaneous wireless micropower neural recording (Wattanapanitch et al., 2007) would make the tool even more valuable in experimental and clinical neuroscience. Further reductions in size through the use of high-precision blocking-capacitor-free stimulation (Sit and Sarpeshkar, 2007a) could enable scaling to applications that need large numbers of electrodes or that need to be even smaller.

2.6 Supplementary Figures

Figures S1-S14 include detailed circuit schematics for each part of the integrated circuit. Also included is layout for creating the miniature stimulator circuit board and control signals for operating the stimulator chip.

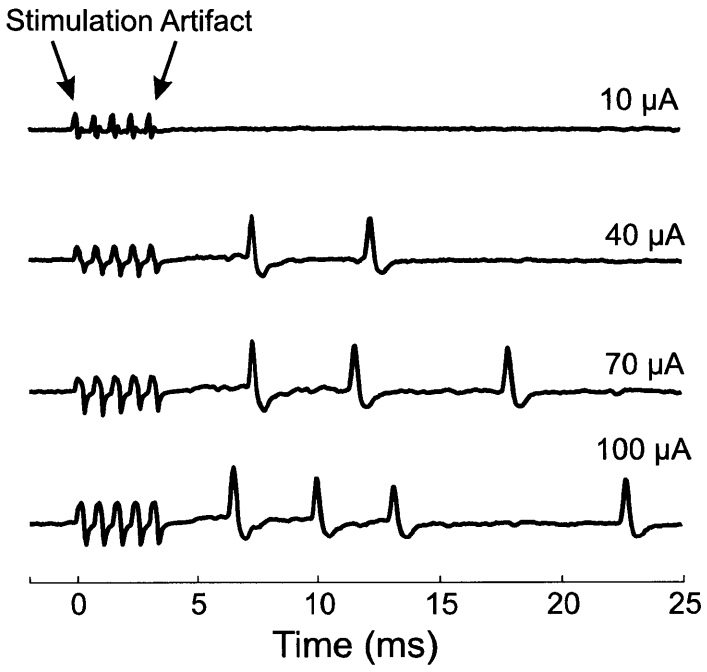


Figure 2-16: Example extracellular responses of an isolated RA neuron to stimulation in HVC at four different current levels. The stimulation artifacts have been artificially reduced in software to increase the resolution of the vertical scale.

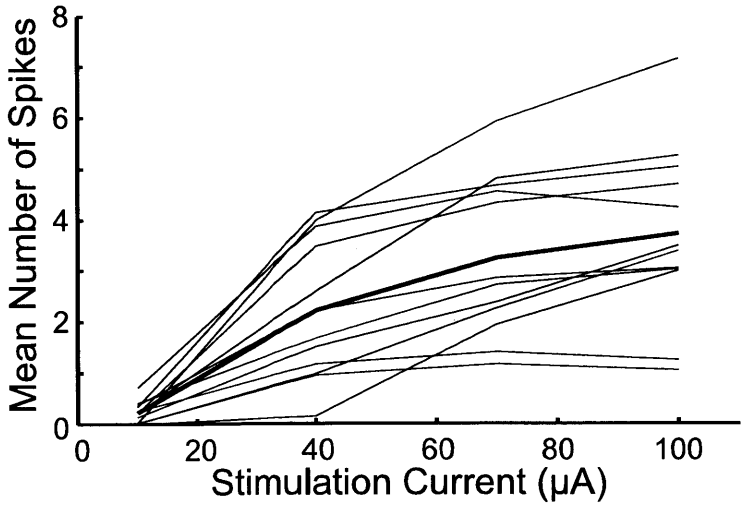


Figure 2-17: Average number of spikes per response as a function of the stimulation current. Averages for 12 neurons are shown. The thick line represents the average of all neurons.

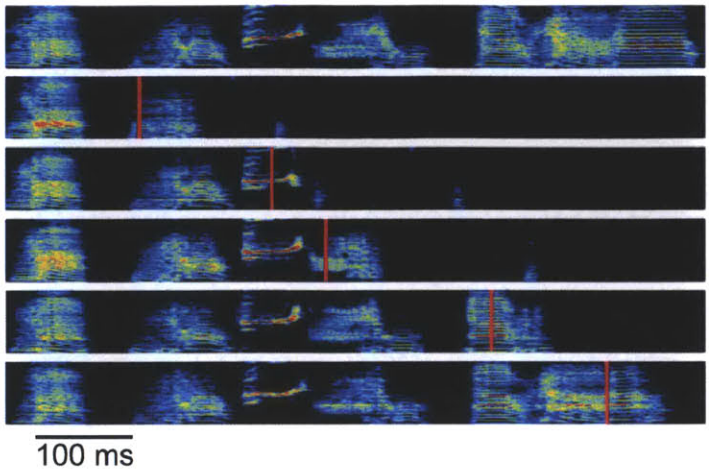


Figure 2-18: A sonogram of an unperturbed, reference motif is shown (top) followed by sonograms of five motifs truncated by stimulation at various points within the motif. The vertical red lines signify the time of stimulation.

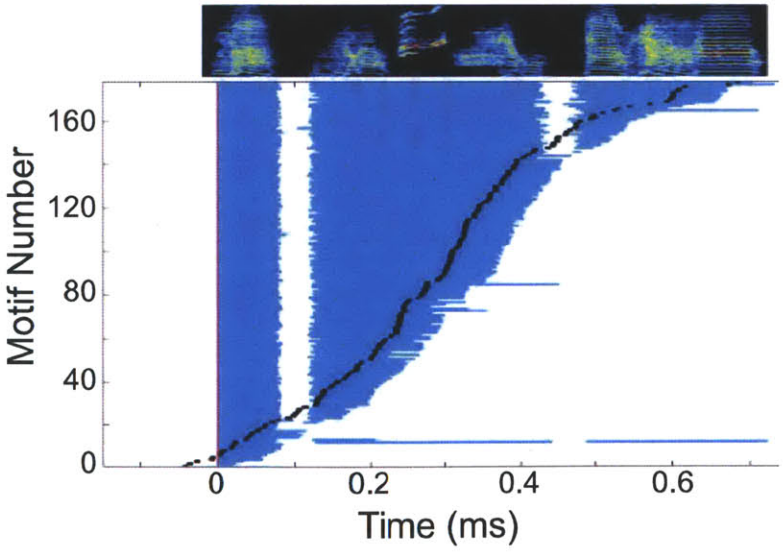


Figure 2-19: A raster plot showing all stimulation trials for a single bird at a current level of 100 μA. Sound is represented by horizontal blue bars. The time of stimulation is marked (black dash), and song truncation follows after a brief delay in nearly every case.

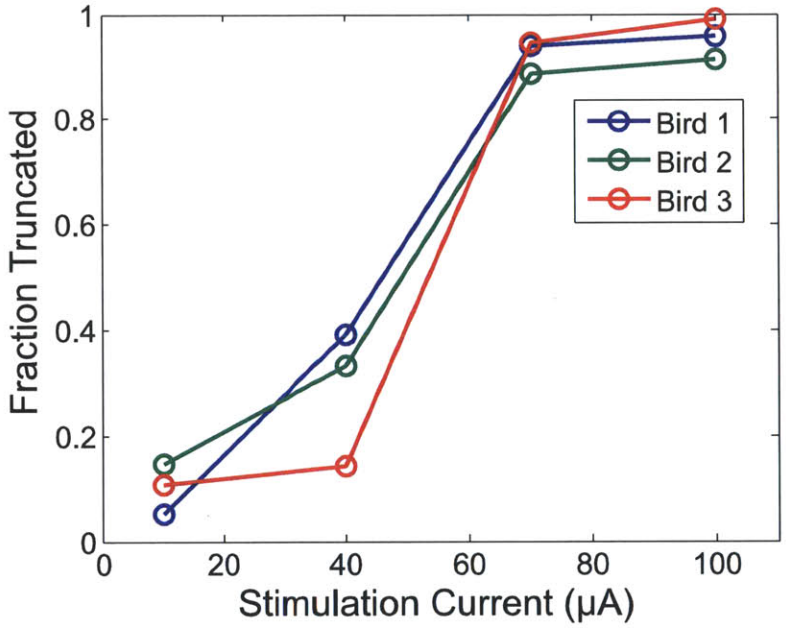


Figure 2-20: The fraction of motifs that were truncated by stimulation is shown as a function of stimulation current level (n = 3 birds).

Figures S1-S11 present the complete schematics for the custom integrated circuit used in the wireless neural stimulation device. Each schematic shows a portion of the overall circuit and gives a summary of its inputs and outputs as a block. Also included are all MOSFET length and widths, resistor, capacitor, and bias current values.

FIGURE LEGENDS

Figure S1. Signal pre-amplification and peak detection. Schematics are given in detail for the receiver preamplifier, peak detector, bandpass filter, comparator (Figure S4), and glitch eliminator. The bandpass filter conditions the peak detector waveform by removing any high frequency ripple due to the RF carrier and AC-couples the signal to the comparator. The glitch eliminator uses a current-limited inverter to reject any digital pulses that are too narrow in width (as determined by the load capacitor and limiting current). A Schmitt trigger (Figure S4) ensures that the edges of $V_{out,comp}$ are fast. The glitch eliminator also produces the delayed copy of the comparator signal needed to produce $V_{trig,wakeup}$ every time a transition in the comparator signal is detected.

Figure S2. Wakeup controller, with ring oscillator and standby counter. The circuit schematic of the wakeup controller is given in detail. When the signal $V_{trig,wakeup}$ is received, the standby counter (constructed using a ripple cascade of flip-flops) is preset such that all state variables are 1. The wakeup trigger also turns on a ring oscillator which clocks the standby counter, decreasing its stored value by 1 each clock cycle. The output of the final flip-flop in the counter determines the value of *wakeup*. If the chip is receiving a stream of data, $V_{trig,wakeup}$ is received repeatedly which keeps resetting the counter to the maximum value. If the counter reaches zero before another $V_{trig,wakeup}$ trigger pulse is received, the chip will go to sleep. The duration of the timeout is set by the size of the counter and the frequency of the ring oscillator. In this design, a 10-bit counter encoding 1024 values is designed to run down in about 1 second.

Figure S3. Pulse-width demodulator. This schematic is a more detailed version of that given in Figure 2C. This circuit and all subsequent circuits are inactivated when *wakeup* is low. A set of current-limited inverters produce delayed copies of the input signal, $V_{out,comp}$. Combinations of the input and delayed copies of itself are used to produce the four timing phases needed for the pulse-width demodulator.

Figure S4. Comparator and Schmitt trigger. Full schematics provided.

Figure S5. Data decoding and stimulus control. The data recovered by the PWM demodulator is passed into a Data Processing Unit (Figure S6). Once the data is decoded, a digital-to-analog converter (DAC) (Figure S9) is configured and the appropriate output driver is selected (Figure S10). A timer circuit (Figure S8) controls the timing of the stimulus. A set of level shifters (Figure S9) convert the control signals from the low-voltage power supply (2.5 V) to the high-voltage power supply (5.0 V). The stimulus itself is supplied by the output driver circuit (Figure S10).

Figure S6. Data processing unit. The data processing unit (DPU) receives demodulated data from the PWM demodulator. These data are fed into a shift register (Figure S7). The DPU looks at the data in the shift register in parallel and checks for a recognition sequence of all 1's in bit positions 0-3. It also checks that bit positions 4, 8, and 12 contain 0's. This is required so that is impossible for other data, when transmitted correctly, to mimic the recognition sequence. Additionally, it also calculates a parity bit (Figure S7) for the actual stimulation parameters (bits 5-7, 9-11, 13-14) and compares that to the parity bit transmitted (bit 15). If all checks pass, the stimulation parameters are transferred from the shift register into another set of memory registers (Figure S7). Once the stimulus parameters are stored in memory, a trigger pulse is generated to initiate the stimulus. Because the stimulation parameters are now stored in memory, new data can be transmitted and loaded into the shift registers.

Figure S7. Data shift register, data memory, and parity check. The data shift register and data memory registers use ordinary flip-flops. Any general purpose flip-flop design should be acceptable. The parity bit is calculated by a simple XOR applied to all inputs simultaneously.

Figure S8. Output driver timer and output driver selection logic. The output driver timer is based on a one-shot topology, where a current charges a capacitor to a threshold. This times the first pulse. Once the threshold is reached, a current charges a second capacitor to the same threshold. Once both thresholds are reached, the voltage on both capacitors is reset to zero. This results in a stimulus consisting of two identical pulses. The output driver selection logic works by taking the stimulus timing and passing it to the correct output driver using a set of combinational and multiplexer based logic. Only the selected output driver receives the timing pulse.

Figure S9. Output driver DAC, OTA, and level shifter. The DAC provides a reference voltage to the output drivers. Based upon the stimulation parameters selected by the user, the DAC generates a scaled copy of the intended stimulation current using a combination of binary-weighted current sources. The DAC outputs this current as a transistor gate voltage for both NMOS and PMOS transistor types. Because the PMOS voltage must be reference to the higher 5 V power supply, a regulated cascode implemented using an operational transconductance amplifier (OTA) is used to make a more accurate current mirror.

Figure S10. Output driver. The output driver circuit is essentially a current-mirror which accepts the voltages *Vn* and *Vp* generated by the DAC to generate a reference current which is scaled up by 10x before being sent to the output. Enable switches controlled by the timer circuit and driver selection circuitry turn the output current on and off. The driver is said to be "floating" because the current source has two outputs, labeled *elec1* and *elec2*, neither which need to be connected to ground.

Figure S11. Current reference. The current reference produces a constant output independent of the supply voltage. This current is automatically generated by the chip

and then scaled using a series of current mirrors to provide the bias currents to all circuits on the chip. See Mandal, S. Arfin, S. Sarpeshkar, R., "Fast startup CMOS current references," *Proceedings of the IEEE Symposium on Circuits and Systems (ISCAS 2006),* pp. 2845-2848.

Figure S12. PCB Layout.

Parts Table

Capacitor	Value	Digikey Part Number
C1	270 pF	PCC1714CT-ND
C2	0.22 μF	PCC2272CT-ND
C3	1 μF	PCC2189CT-ND

C_1 is the resonant capacitor in parallel with the receiver coil. C_2 are the DC blocking capacitors in series with every electrode output. C_3 are power supply bypass capacitors, placed in parallel with the batteries. The chip is placed on the die attach paddle and wirebonded to the board and covered in epoxy encapsulation. The only electrical connections required are for the batteries, the input from the coil, and the 8 outputs corresponding to the 4 electrode pairs.

Figure S13. Data packet organization.

Figure S14. Glossary of symbols.

Figure S1

Signal Pre-amplifcation and Peak Detection

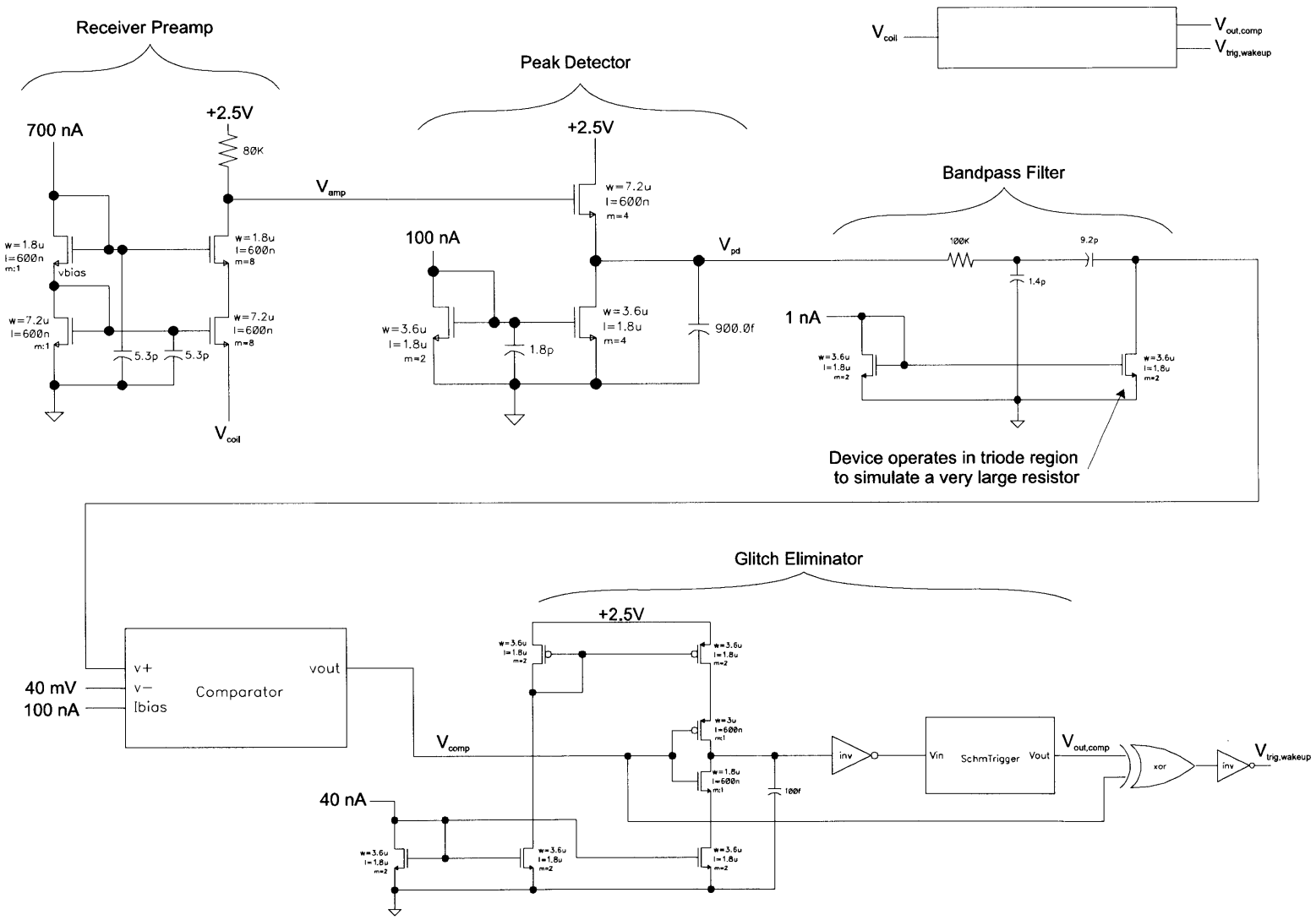
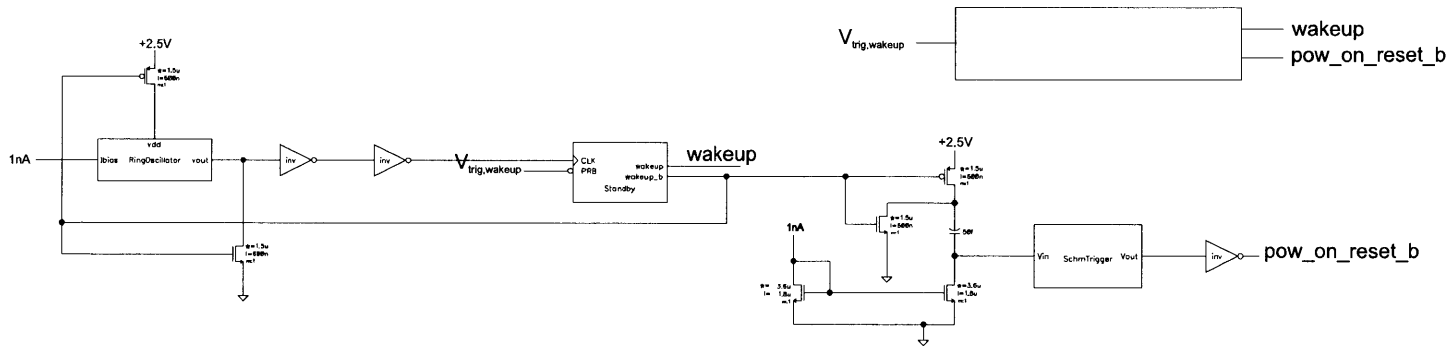
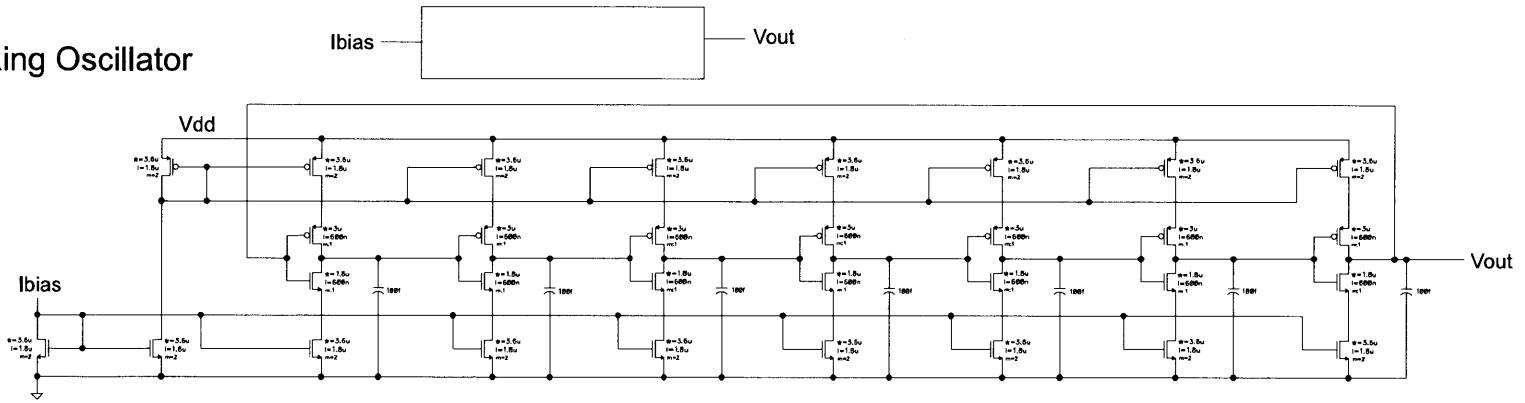


Figure S2

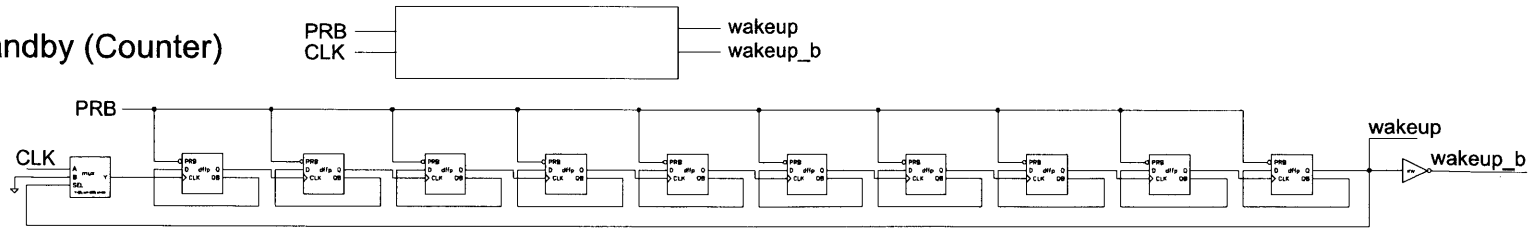
Wakeup Controller (including power-on reset)



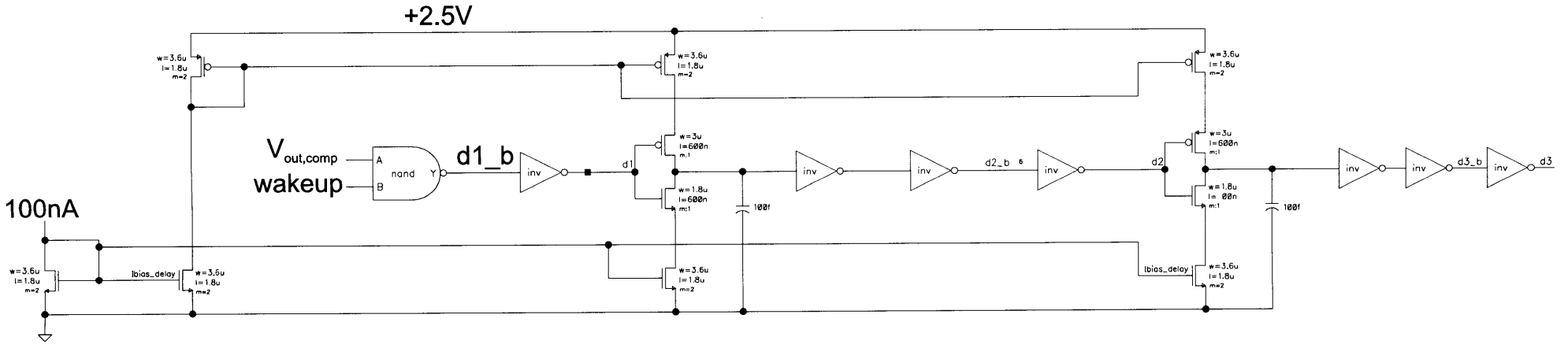
Ring Oscillator

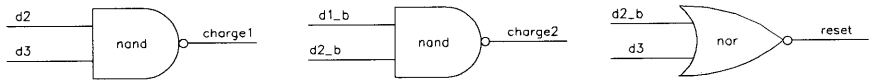


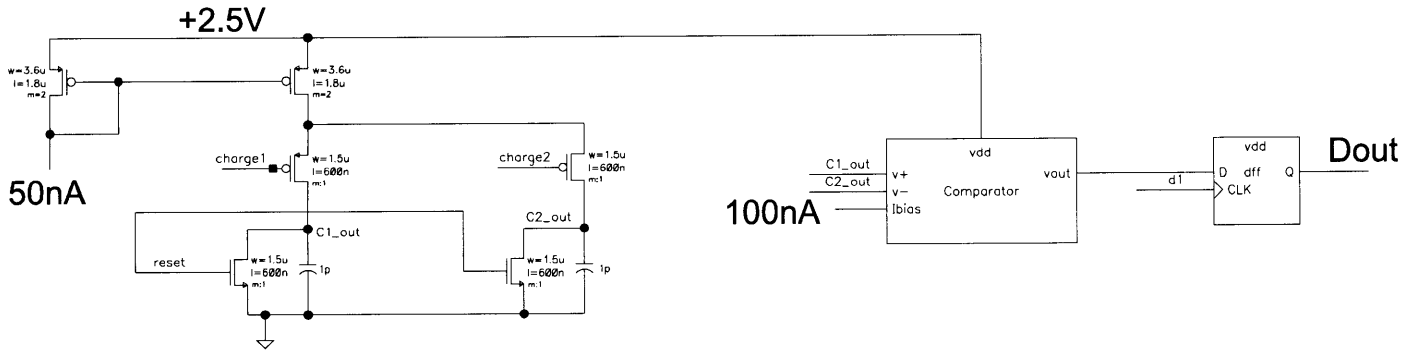
Standby (Counter)

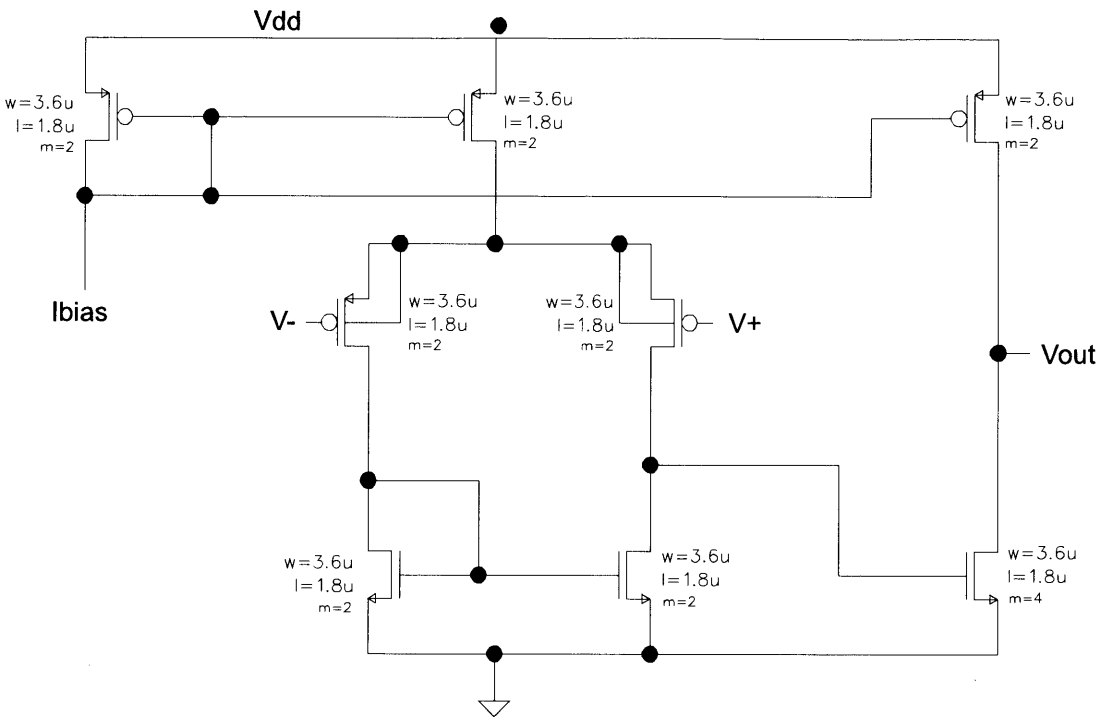


Pulse-Width Demodulator









Schmitt Trigger

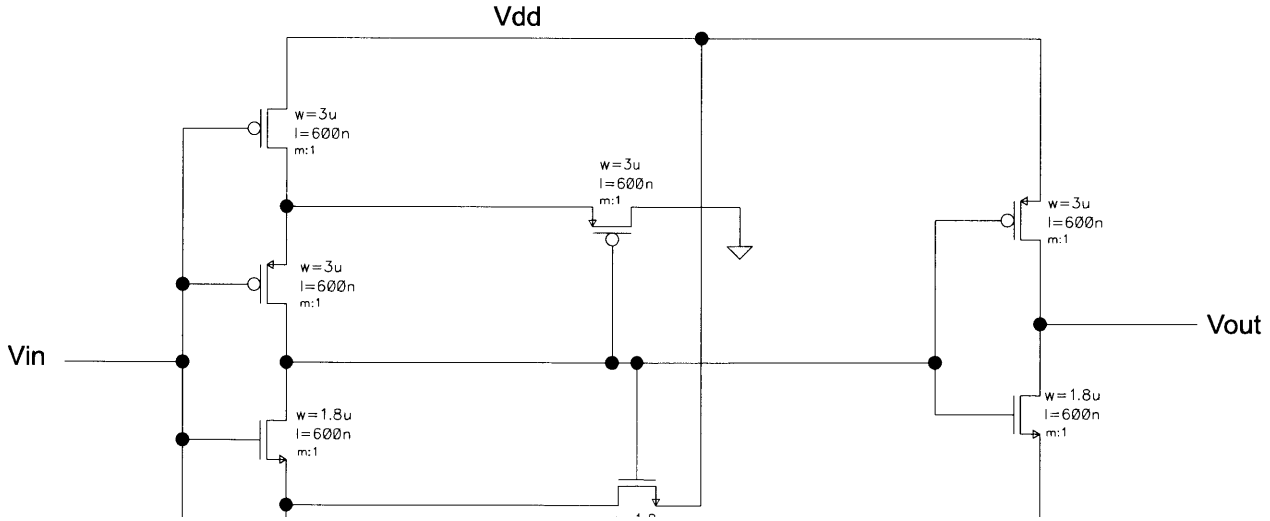


Figure S5

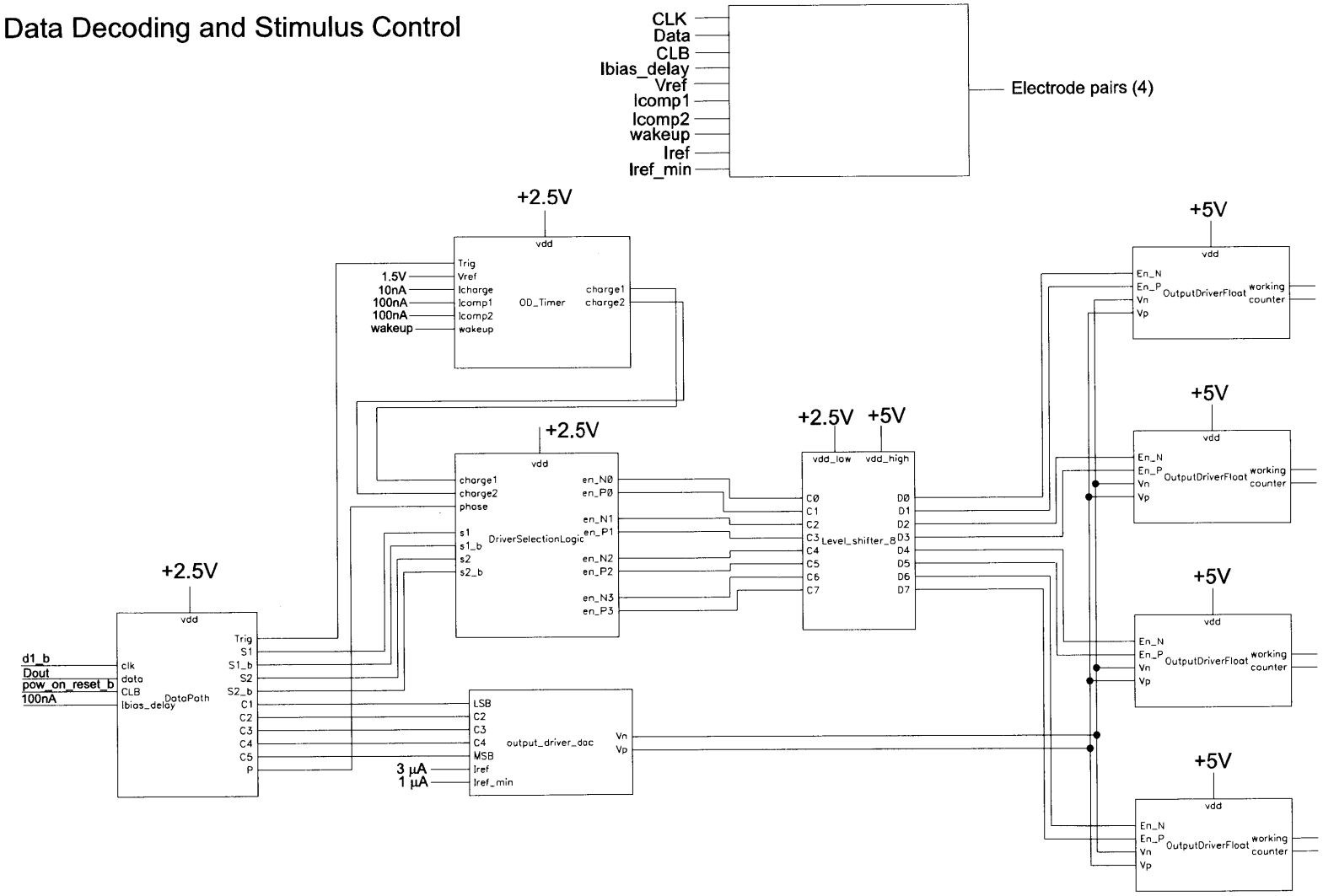
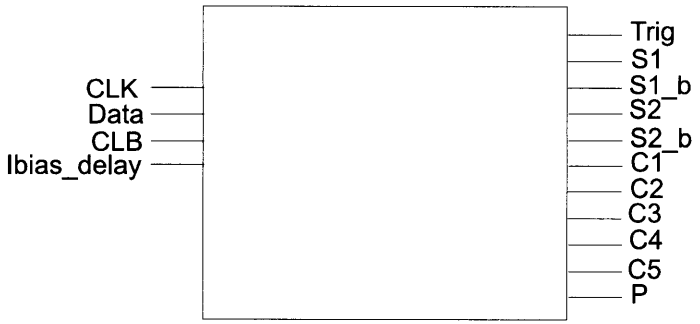
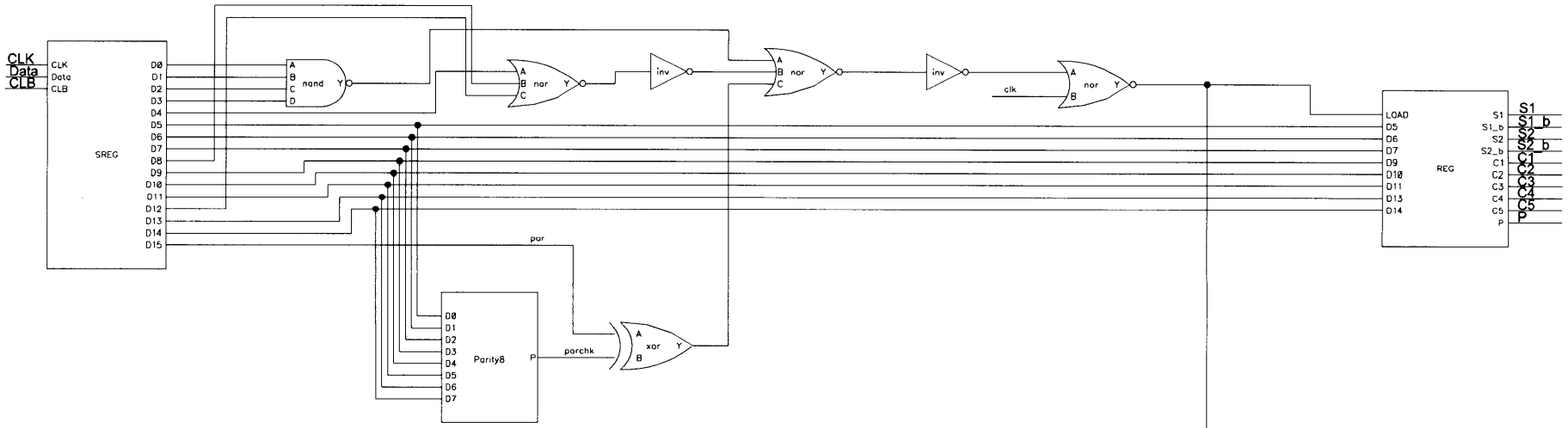

Data Decoding and Stimulus Control
CLK
Data
CLB
Ibias_delay
Vref
Icomp1
Icomp2
wakeup
Iref
Iref_min
Electrode pairs (4)
+2.5V
vdd
Trig
Vref
Icharge
Icomp1
Icomp2
wakeup
1.5V
10nA
100nA
100nA
wakeup
OD_Timer
charge1
charge2
+2.5V
vdd
charge1
charge2
phase
s1
s1_b
s2
s2_b
DriverSelectionLogic
en_N0
en_P0
en_N1
en_P1
en_N2
en_P2
en_N3
en_P3
+2.5V
+5V
vdd_low
vdd_high
C0
C1
C2
C3
C4
C5
C6
C7
Level_shifter_8
D0
D1
D2
D3
D4
D5
D6
D7
+2.5V
vdd
d1_b
Dout
pow_on_reset_b
100nA
clk
data
CLB
Ibias_delay
DataPath
Trig
S1
S1_b
S2
S2_b
C1
C2
C3
C4
C5
P
LSB
C2
C3
C4
MSB
Iref
Iref_min
output_driver_dac
Vn
Vp
3 µA
1 µA
+5V
vdd
En_N
En_P
Vn
Vp
OutputDriverFloat
working
counter
+5V
vdd
En_N
En_P
Vn
Vp
OutputDriverFloat
working
counter
+5V
vdd
En_N
En_P
Vn
Vp
OutputDriverFloat
working
counter
+5V
vdd
En_N
En_P
Vn
Vp
OutputDriverFloat
working
counter

Figure S6

Data Processing Unit





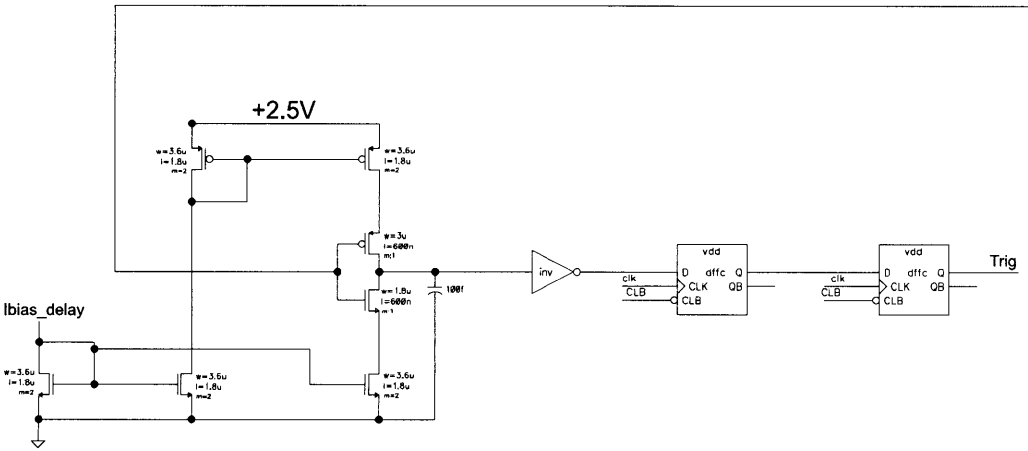
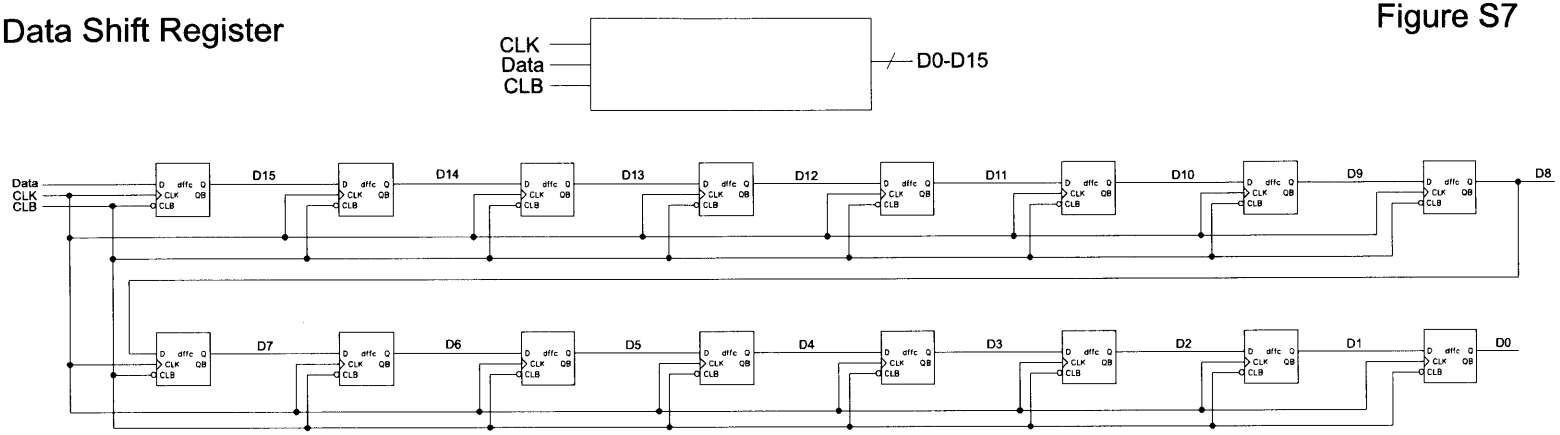
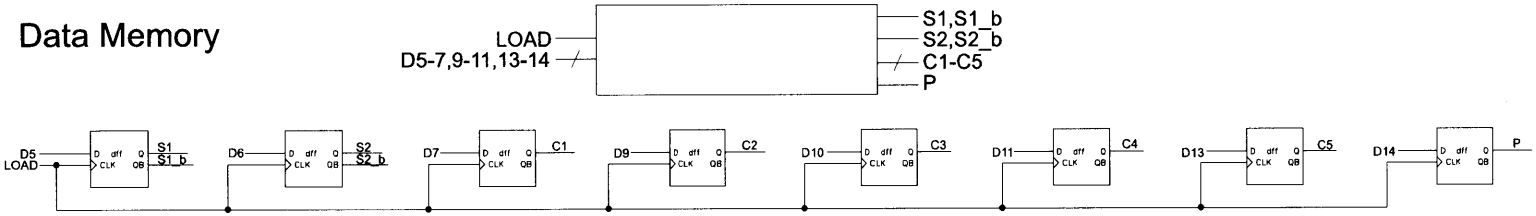


Figure S7

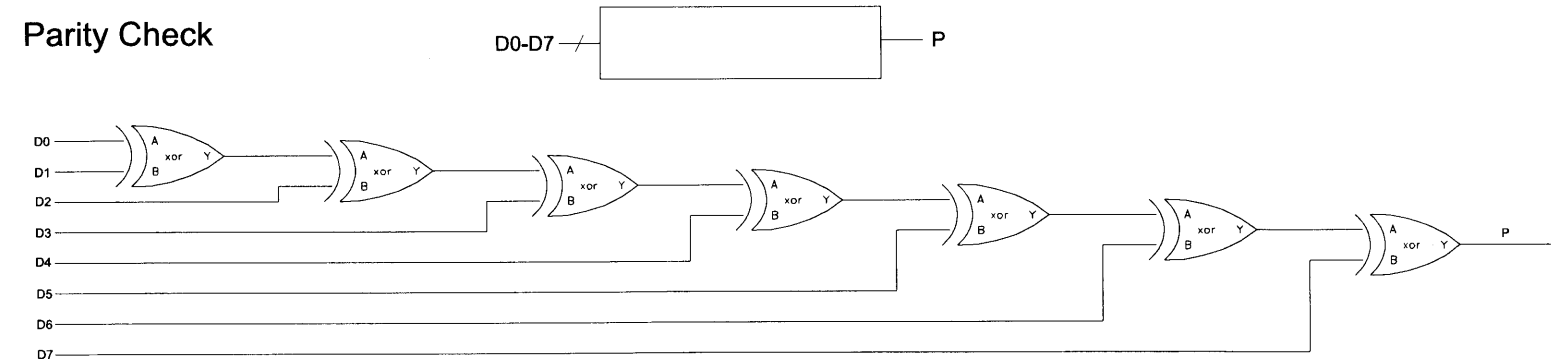
Data Shift Register



Data Memory

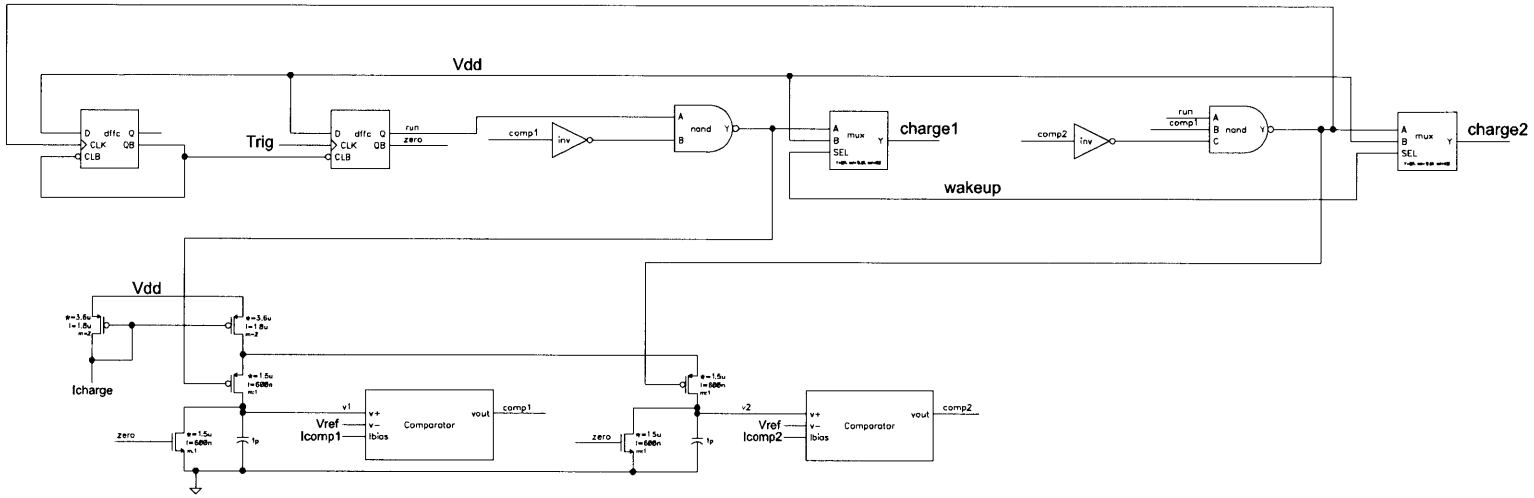


Parity Check



Output Driver Timer

Figure S8



Output Driver Selection Logic

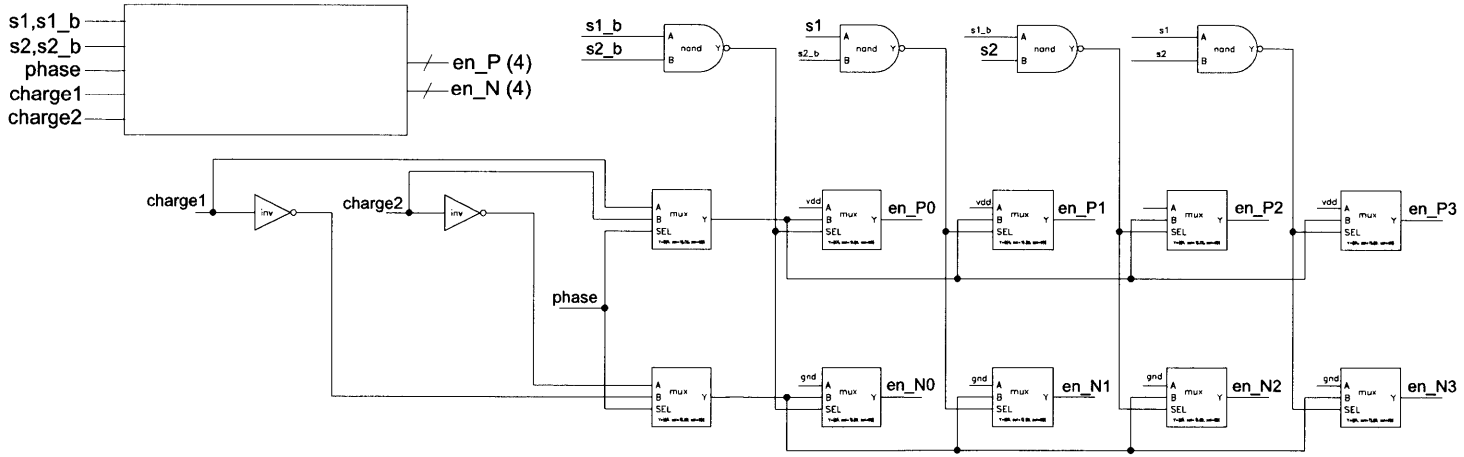
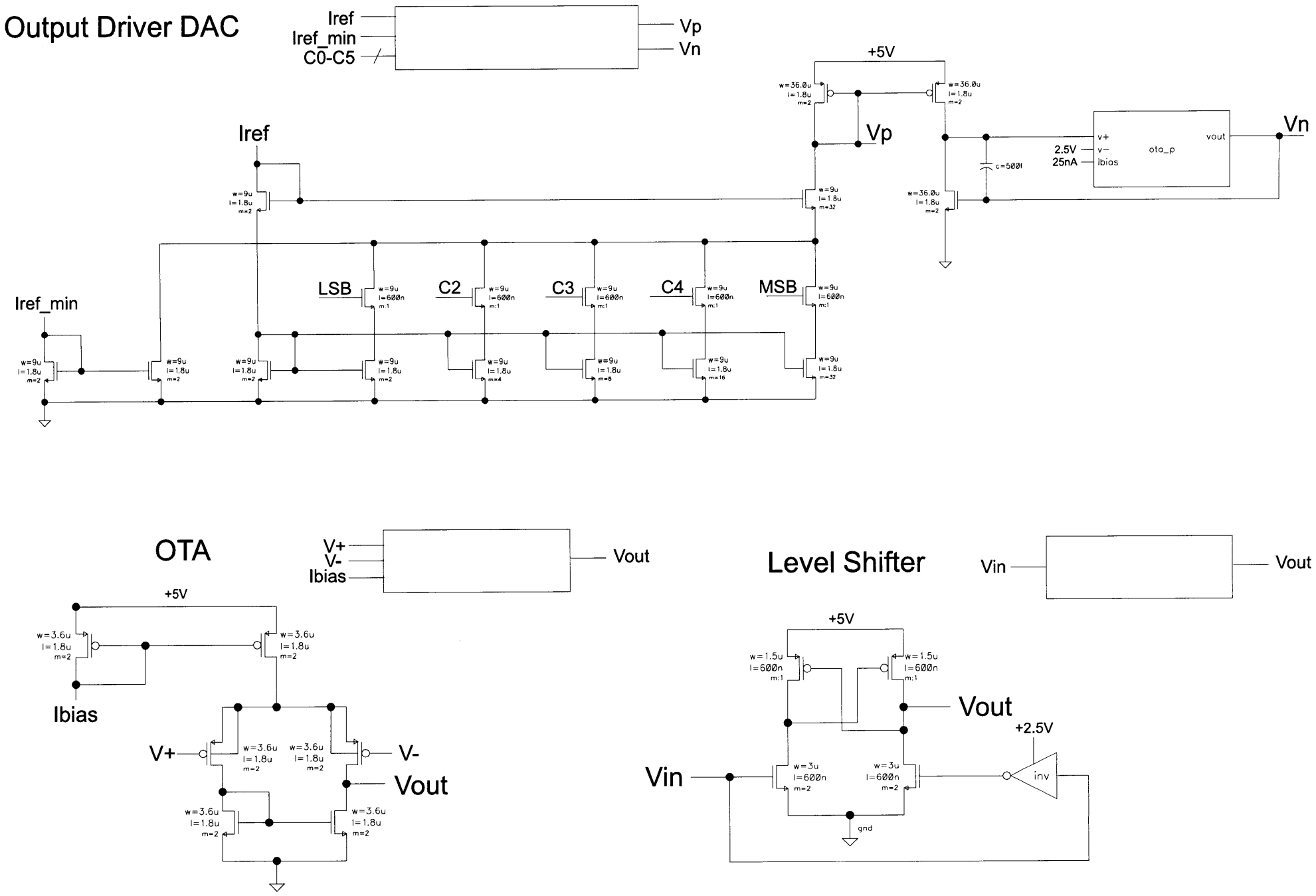


Figure S9


Output Driver DAC
Iref
Iref_min
C0-C5
Vp
Vn
+5V
Iref
Vp
Vn
2.5V
25nA
v+
v−
Ibias
ota_p
vout
c=500f
Iref_min
LSB
C2
C3
C4
MSB
OTA
V+
V-
Ibias
Vout
+5V
Ibias
V+
V-
Vout
Level Shifter
Vin
Vout
+5V
Vout
+2.5V
Vin
inv
gnd

Output Driver (x4)

Supplementary Figure 10

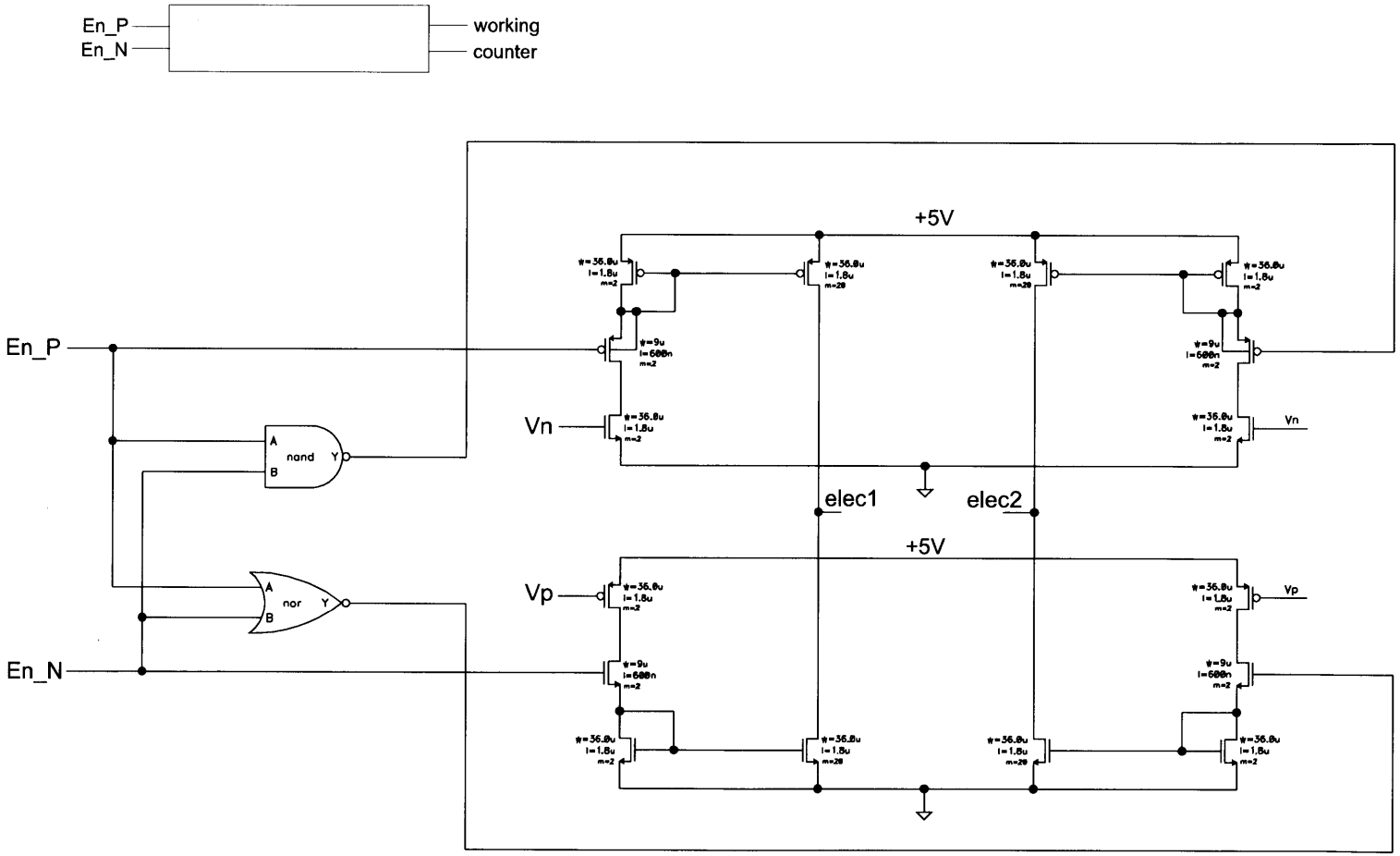


Figure S11

Current Reference

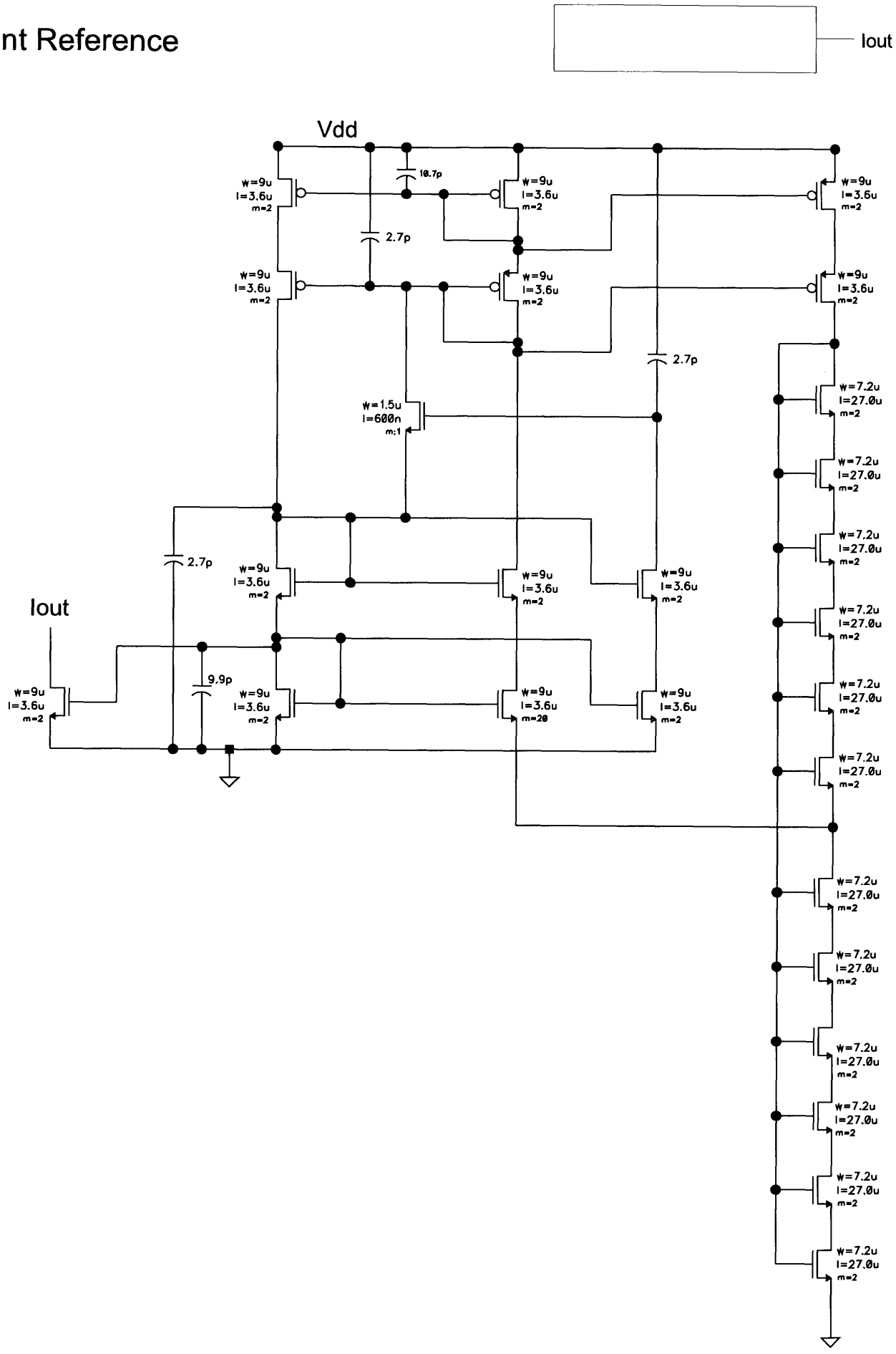
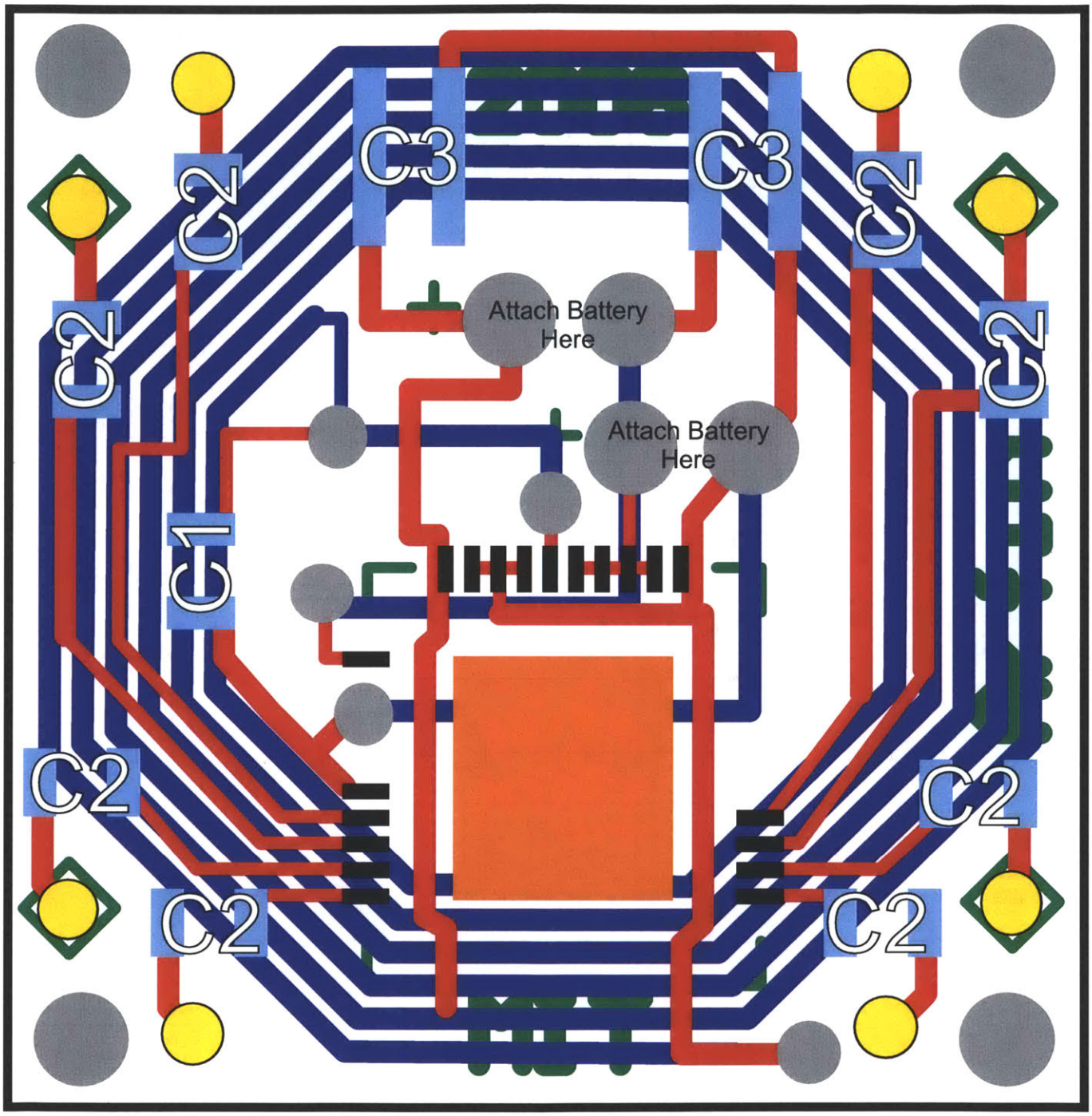


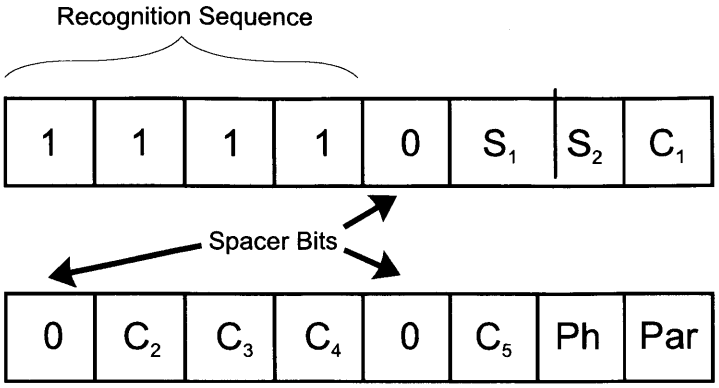
Figure S12



Top Metal
Bottom Metal
Silkscreen
Drill/Via
Capacitor Pad (top metal)
Chip Wirebonding Pad (top metal)
Die attach paddle (top metal)
Electrode wire connection point (via)

10 mil

Figure S13



S_1-S_2: Output driver selector bits
C_1-C_5: Current level selector bits
Ph: Phase selector bit
Par: Parity check bit

Encoding data with PWM

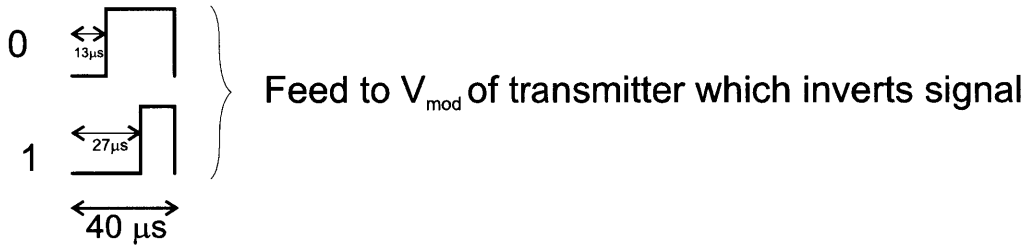
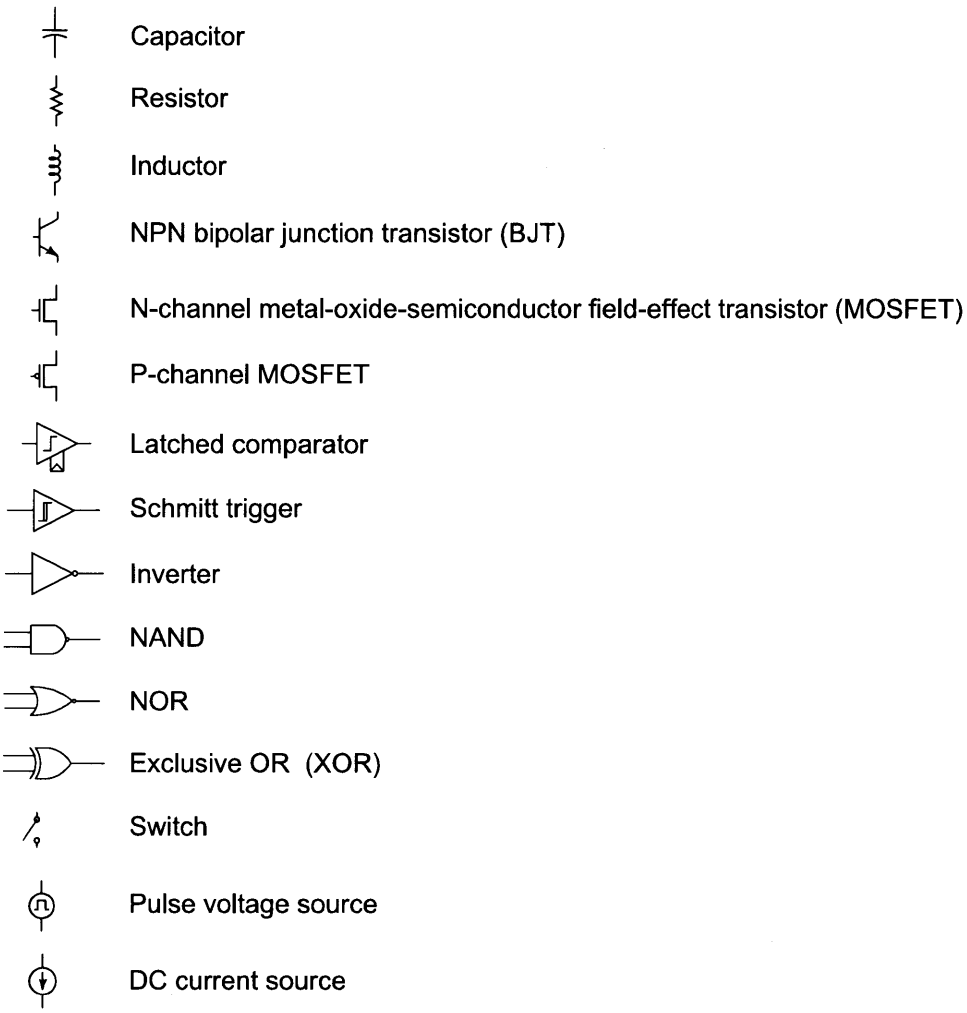


Figure S14

Glossary of Symbols



Chapter 3

Adiabatic Electrode Stimulation: Introduction and Theory

3.1 Introduction to Electrodes

Electrodes provide the interface between the electrical and chemical domains. In neural stimulation, the purpose of the electrode is to interface the stimulator circuitry with the neural tissue. Conventionally, neural stimulation uses charge balanced, biphasic pulses of current to artificially induce neurons near the electrode to fire. Thus, the design of neural stimulators is influenced by the electrical properties of the electrodes. In particular, we would like to know what impedance the electrode will present to the stimulator.

Electrochemical cells always consist of at least two electrodes. In experiments, the electrode under observation is termed the working electrode, and the secondary electrode for carrying the return current is called the counter electrode. Sometimes a third reference electrode is used as well. Implanted neural stimulation electrodes may be modeled by an electrochemical cell consisting of the stimulating (working) and return (counter) electrodes, and tissue, which may be modeled as a 0.9% NaCl electrolyte (physiological saline). A more detailed treatment of electrodes as they apply to neural stimulation may be found in (Kelly, 2003; Roach, 2003), and a more general reference on electrodes and electrochemistry may be found in (Bard and Faulkner, 2001).

3.1.1 The Randles Model

One commonly used circuit model of an electrode in solution is due to Randles (Randles, 1947). The Randles model is a composition of electrical circuit elements that ideally behave identically to a real electrode in solution. However, this model is limited to small-signal excitations, that is, perturbations about an operating point. Electrode responses to large excitations and behavior at D.C. is not covered by the Randles model. Unfortunately, the voltage and current drives used for neural stimulation do not typically fall into the category of small-signal. Nevertheless, the Randles model is a good starting point for our investigation.

Figure 3-1 shows the general Randles model of the electrode. The model details two current paths, I_c and I_f. I_c is the current that charges the double-layer capacitance, C_{dl}. The other current path, I_f, represents the Faradaic current. Faradaic currents correspond to the oxidation or reduction of chemical species. The flow of Faradaic current is limited by the sum of two impedances, R_{ct} and Z_W. Physically, R_{ct} is the charge transfer resistance, or the impedance opposing an electron trying to transfer from the surface of the electrode into the electrolyte, and vice-versa. The Warburg impedance, Z_W, represents limitations on mass transport by diffusion inside the solution. The Warburg impedance is also frequency dependent. R_s is a general solution resistance, set by the conductivity of the electrolyte itself. Both the Faradaic and charging currents must pass through the solution resistance.

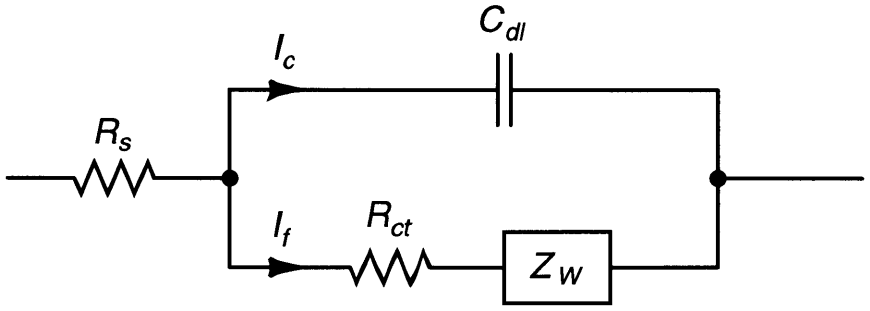


Figure 3-1: Randles electrode model.

3.1.2 The Double-Layer Capacitance

One of the most significant features of electrode impedance is the double-layer capacitance. To get a general idea of how the Faradaic and charging currents interplay, let us once again consider the Randles model of the electrode of Figure 3-1. If a sufficiently large step in potential is applied to the working electrode in an electrochemical cell, initially a large current, I_c, flows to charge

the double-layer capacitance. The charging time constant is set by the product of the double-layer capacitance, C_{dl}, and the series solution resistance, R_s. In fact, the charging of this capacitance is what actually causes polarization of the electrode. Once the capacitance charges appreciably, the Faradaic current due to redox processes, I_f, begins to take over and eventually dominates the total electrode current. After a few RC time constants, the double-layer charging current falls below detectable levels.

Physically, the double-layer capacitance arises due to a diffuse charge region in the electrolyte near the surface of the electrode. The geometry is similar to that of a parallel plate capacitor, where the top plate is the electrode itself, and the bottom plate is formed from charges in solution piling up near the electrode. The separation between the "plates" is on the order of molecular scales; hence the double-layer capacitance can be quite large. The parallel plate view of the double-layer capacitor is known as the Helmholtz model.

Unfortunately, the Helmholtz model is not accurate because it predicts C_{dl} is a constant. It also does not account for the fact that real charge distributions in solution do not take the shape of a parallel plate, but rather are most heavily concentrated near the electrode, and then taper off. One can define the thickness of the diffuse charge region as where the strength of the electrostatic forces fall below that of thermal processes. The Gouy-Chapman capacitance model takes into account the average distance of the separation between charges on the surface of the electrode and charges in solution. This improved model also takes into account the fact that as the electrode becomes more heavily polarized, the double-layer capacitance actually increases. The diffuse charge region shrinks under strong polarization, which results in an increased capacitance. However, the double-layer capacitance does not increase without bound as the applied potential increases because the charge separation cannot become infinitely small. The Stern model improves the Gouy-Chapman model to account for this limit.

For the purposes of estimating the double-layer capacitance of an electrode, we can simply apply the Gouy-Chapman formula in Equation 3.1 with the applied potential, ϕ_0, set to zero. C^* is the bulk concentration of the electrolyte in moles per liter. For simplicity, we can assume tissue is equivalent to a 0.9% NaCl solution, which has a molarity of 0.153. Therefore, we can calculate from Equation 3.1 the double-layer capacitance to be $89\mu F/\text{cm}^2$.

$$C_{dl} = 228zC^{*1/2}\cosh\left(19.5z\phi_0\right)\mu F/\text{cm}^2 \tag{3.1}$$

3.1.3 The Solution Resistance

The solution resistance arises because all the electrode current, both Faradaic and charging, must pass through the solution to the cell's counter electrode. In the case of a monopolar stimulation, the counter electrode will be a remote ground. In a bipolar stimulation, the counter electrode is normally a second electrode identical to the first, placed nearby, usually on cellular scales.

One model for the solution resistance, the hemispherical model, is presented here in Equation 3.2:

$$R_{hemi} = \frac{\rho}{2\pi a_0} \tag{3.2}$$

where ρ is the resistivity of the solution and a_0 is the radius of the working electrode. It is assumed that the counter electrode has a significantly larger radius than the working electrode. A typical value for the resistivity of 0.9% physiological saline is 85Ω·cm. From this equation, we see that the solution resistance scales directly with electrolyte resistivity and inversely with electrode radius.

An alternative model of the solution resistance is the disk model. Instead of the electrode current spreading from a hemisphere, it spreads from a disk. The disk model, given in Equation 3.3 has the same dependencies as the hemispherical model, but is a factor of $\pi/2$ greater.

$$R_{disk} = \frac{\rho}{4a_0} \tag{3.3}$$

3.1.4 The Warburg Impedance

The Warburg impedance is one component of the impedance that sets the Faradaic current. Usually, it dominates the charge transfer resistance, i.e., most chemical reactions are mass transfer limited rather than charge transfer limited. Physically, the Warburg impedance arises from a diffusion current in the cell. As reactants in the cell are either oxidized or reduced, a concentration gradient arises in the cell due to a depletion of reactants near the electrode-electrolyte interface. This gradient is what allows for mass transport. More reactant will diffuse towards the interface to fuel the reaction. The Warburg impedance can be solved for by assuming a small, sinusoidally varying input to a semi-infinite RC transmission line. The Warburg impedance has a $1/\sqrt{\omega}$ dependence on frequency.

3.1.5 Low and High Frequency Limits

At low frequencies, the Warburg impedance and the double-layer capacitance compete to set the impedance of the cell. However, the impedance of C_{dl} rises faster than Z_W as frequency decreases

because of the square root in the Warburg impedance. Therefore, at extremely low frequencies, C_{dl} is effectively an open circuit and can be ignored, and Z_W in series with R_{ct} and R_s determine the total electrode impedance. Eventually, Z_W will also dominate R_{ct} and R_s. Strictly speaking, according to the Randles model, the Warburg impedance should have a constant phase angle of 45°. However, due to a number of simplifications in the Randles model, this is often not the case. For instance, the real and imaginary components to the Warburg impedance would need to be equal at all frequencies to main a constant phase angle of 45°. However, if the real and imaginary components remain in a constant ratio, though not necessarily equal, the Warburg impedance will contribute a constant phase.

At high enough frequencies, the impedance of C_{dl} falls below the impedance of Z_W and effectively shorts out both components of the Faradaic impedance. The electrode impedance then appears as the solution resistance R_s in series with the double-layer capacitance C_{dl}. Figure 3-2 shows the Randles high frequency model. Electrode drive under constant current usually involves biphasic pulses which are quick enough to fall into the high frequency category.

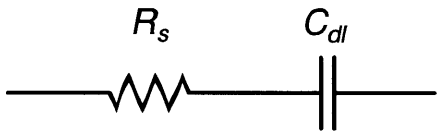


Figure 3-2: Randles high frequency electrode model.

3.1.6 Safe Stimulation Limits

Passing current through the electrode into the tissue initially results in the charging of the double layer capacitance. As the electrode begins to move away from equilibrium, this overpotential leads exponentially to an increase in Faradic reactions. Normally, the oxidation and reduction of ions in solution is safe and reversible. However, at higher potentials, the oxidation or reduction of water becomes possible. This is a particularly dangerous and not easily reversible reaction. Reducing water forms hydrogen gas while oxidizing water forms oxygen. The overpotential limits under which water begins to oxidize or reduce is termed the water window (Merrill et al., 2005). The exact value of the water window depends on the electrode material. Because it is impossible to measure the overpotential directly without sophisticated potentiostats with reference electrodes, an impracticality *in vivo*, conservative safe charge injection limits must be imposed based on the properties of the stimulating electrodes.

It should be noted that when electrode voltages are normally measured, for example, by connect-

ing the electrode directly to an oscilloscope, one sees only the total electrode voltage. That is, one sees the sum of the IR drops across the solution resistance and any overpotential stored on C_{dl}. One cannot distinguish the individual resistive and capacitive voltage drops. In addition, measuring the electrode current reveals only the total current, not the individual Faradaic and capacitive currents, nor what reactions are taking place. Thus, there is no simple way to guarantee that safe limits will not be exceeded. However, adhering to published safe charge density limits and avoiding the buildup of D.C. potentials through active and passive charge cancelation, one can greatly reduce the chance of producing dangerous overpotentials.

3.1.7 Example: Clinical DBS Electrode Impedance

Because stimulation tends to fall into the high-frequency category of electrode modeling, we can almost completely characterize the electrode impedance with just C_{dl} and R_s. Common clinical DBS electrodes, such as the Model 3387 and 3389(Medtronic, Minneapolis, MN (Medtronic, 2008)), have a linear array of four cylindrical electrodes 1.5 mm in length and 1.27 mm in diameter, for a total surface area of 5.98 mm^2. The Gouy-Chapman formula predicts 5.3 μF of double-layer capacitance, a number which far exceeds reality. Measurements *in vitro* and *in vivo* indicate C_{dl} in the range of 1-2 μF for currents up to 1 mA (Wei and Grill, 2009).

To estimate solution resistance using either the disk or hemispherical model, we need to convert the electrode surface area into an equivalent disk shape. The radius of that disk would then be 1.38 mm. The disk and hemispherical models therefore predict R_s to be in the range of 100-150 Ω. This compares favorably to the *in vitro* measurement of 100 Ω, but falls well below the *in vivo* measurement of 500 Ω (Wei and Grill, 2009).

It is apparent that many factors beyond what is described here affect electrode behavior. For example, it should be noted that although the solution resistance is generally regarded as an ohmic resistance set by the conductivity of the electrolyte, even in the absence of any faradaic process, a simple electrode circuit consisting of only R_s and C_{dl} in series will show some effects of frequency dispersion at low electrolyte concentrations. Thus, both R_s and C_{dl} will exhibit frequency dependence. This simplistic view of electrodes is useful only for making order-of-magnitude predictions of actual electrode properties. In fact, this very unpredictable nature of electrodes makes it difficult to design a stimulator which is efficient over a wide range of electrode impedances, and emphasizes the need for feedback in stimulator circuits to reduce or eliminate the effect of variable electrode impedances.

3.2 Adiabatic Processes in Circuits

Generally speaking, an adiabatic process is one which does not dissipate energy. That is, the total energy of the system remains constant throughout the entire procedure. In the context of circuits, this refers to taking energy from the power supply, transferring it to a capacitive circuit element, and then transferring it back, with as little dissipation as possible.

The concept of adiabatic processes in circuits was first introduced for adiabatic computing (Athas et al., 1994; Sarpeshkar, 2010), a modification of CMOS logic circuits where traditional clocks, input, and output waveforms are restricted to slow ramps. In CMOS, loads are typically capacitive. For example, in Figure 3-3(a), an inverter charging a capacitive load C_L with power supply V_{DD} is subject to the customary $C_L V_{DD}^2$ dynamic switching loss. At the end of the charge, the capacitor will hold a charge $C_L V_{DD}$, corresponding to a stored energy of $\frac{1}{2} C_L V_{DD}^2$. However, a total energy of $C_L V_{DD}^2$ was taken from the power supply, an amount which is invariant, no matter the charging profile. The energy stored in the capacitor will be eventually lost when the capacitor is discharged back to ground.

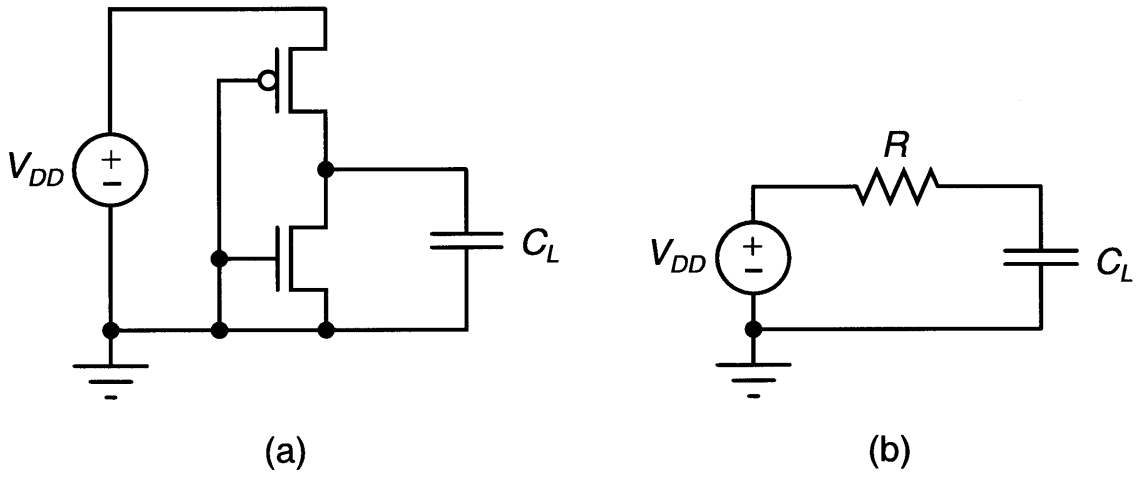


Figure 3-3: (a) An inverter charging a load. (b) Simplified equivalent circuit.

In traditional CMOS, the loss of $\frac{1}{2} C_L V_{DD}^2$ during charging is due to the inverter itself, which dissipates energy when simultaneous voltage and current appear across and within the transistors of the inverter. This loss is more apparent in Figure 3-3(b), where we have replaced the inverter with an equivalent circuit, a simple resistor. If one were to replace V_{DD} with a dynamic supply $V_{DD}(t)$ that followed the voltage on the load capacitor as it charged exactly, then any voltage drop across the charging transistor would be minimized, thus significantly reducing the energy losses in the inverter.

In fact, if we could charge C_L infinitely slowly, that is, truly *adiabatically*, then there would be absolutely no loss at all in the inverter.

Unfortunately, it is not practical to charge a load infinitely slowly. If we have some time limit in which to charge the load, what is, then, the ideal profile for $V_{DD}(t)$? It can be proven relatively simply that the optimal current profile to charge a capacitor with a series resistor in a finite period of time, as in Figure 3-3(b), is with a constant current. One way to observe this is to note that the energy dissipated in the resistor R is $E = \int_0^T i(t)^2 R\, dt$, where $i(t)$ is the charging current and T is the charging period. If we assume that $i(t)$ is a constant, I, the energy dissipated simplifies to I^2RT. To prove informally that anything but a constant current results in higher energy loss, we can suppose that we begin with a constant current I. Since R and T are constants, we can informally call the total energy dissipated I^2. Suppose now we increase the current by a tiny amount, δ, for half the period. In order to keep the total charge transferred constant, this must be countered with a decrease in current by the same amount δ, for the second half of the period. Calculating the energy, we obtain:

$$\begin{aligned} E' &= \frac{1}{2}(I+\delta)^2 + \frac{1}{2}(I-\delta)^2 \\ &= \frac{1}{2}\left(I^2 + 2I\delta + \delta^2 + I^2 - 2I\delta + \delta^2\right) \\ &= I^2 + \delta^2 \end{aligned}$$

which is of course, greater than I^2, for any δ. Thus, given the requirement to deliver a fixed charge in a fixed period of time, a constant charging current for the entire duration minimizes energy losses in a series resistance.

A constant current charging a capacitor results in a ramp of voltage. Therefore, a ramp in $V_{DD}(t)$, so long that the period $T \gg RC_L$, will result in a constant current. This is the principle of adiabatic computing, in which digital circuits are modified to be essentially clock-powered. That is, the conventional square-wave clock is replaced by a slow ramp which also powers the circuit. Thus, any load capacitors which should be in the logic high state are brought up slowly as the power supply ramps up. As we will see shortly, the capacitive properties of electrodes make them similar to the capacitive loads of logic gates.

These principles of electrochemistry and adiabatic computing form the basis for the design presented in Chapter 4, the adiabatic electrode stimulator.

Chapter 4

An Energy-Efficient, Adiabatic Electrode Stimulator with Inductive Energy Recycling and Feedback Current Regulation

4.1 Abstract

In this paper, we present a novel energy-efficient electrode stimulator. Our stimulator uses inductive storage and recycling of energy in a dynamic power supply. This supply drives an electrode in an adiabatic fashion such that energy consumption is minimized. It also utilizes a shunt current-sensor to monitor and regulate the current through the electrode via feedback, thus enabling flexible and safe stimulation. Since there are no explicit current sources or current limiters, wasteful energy dissipation across such elements is naturally avoided. The dynamic power supply allows efficient transfer of energy both to and from the electrode and is based on a DC-DC converter topology that we use in a bidirectional fashion in *forward-buck* or *reverse-boost* modes. In an exemplary electrode implementation intended for neural stimulation, we show how the stimulator combines the efficiency of voltage control and the safety and accuracy of current control in a single low-power integrated-circuit built in a standard 0.35 μm CMOS process. This stimulator achieves a 2x-3x reduction in energy consumption as compared to a conventional current-source-based stimulator operating from a fixed power supply. We perform a theoretical analysis of the energy efficiency

that is in accord with experimental measurements. This theoretical analysis reveals that further improvements in energy efficiency may be achievable with better implementations in the future. Our electrode stimulator could be widely useful for neural, cardiac, retinal, cochlear, muscular and other biomedical implants where low power operation is important.

4.2 Introduction

Electrical stimulation of tissues is an increasingly valuable tool for treating a variety of disorders. For example, the applications of implantable electrical stimulators include cochlear implants for profound hearing loss, visual prostheses for blindness, spinal cord stimulators for severe chronic pain, muscle stimulators for paralysis, cardiac pacemakers, and deep brain stimulators (Loizou, 1999; Normann et al., 1999; Linderoth and Forman, 1999; Smith et al., 1987; Zoll, 1952; Sarpeshkar, 2010). Deep brain stimulation is presently being used to treat a growing number of neurological disorders, such as essential tremor and Parkinson disease, and has also shown potential benefit for a variety of other disorders such as Tourette syndrome, pain, depression, and obsessive compulsive disorder (Perlmutter and Mink, 2006; Tarsy et al., 2008; Collins et al., 2010). Brain implants for paralysis treatments are increasingly providing sensory feedback via neural stimulation (O'Doherty et al., 2009). The electronic hardware for several such applications is discussed in (Sarpeshkar, 2010).

Implantable electrical stimulators must avoid wires through the skin due to risk of infection. As such, these stimulators are often powered by an implanted battery or by an implanted RF coil receiving energy wirelessly. Thus, the energy efficiency of the stimulator is critically important in determining the size of the battery or coil, and improvements in stimulator energy efficiency lead directly to reductions in battery or coil size, increases in battery lifetime, and reductions in tissue heating (Sarpeshkar, 2010). Patient safety and comfort are increased, and medical costs are reduced if the size of the implant can be decreased (Sarpeshkar, 2010). Therefore, there is a strong push to improve the energy efficiency of implantable electrical stimulators, which often consume the lion's share of power in a prosthesis.

Current-source-based stimulators are favored because of their safety (Merrill et al., 2005), established methods of charge balancing (Sooksood et al., 2010; Liu et al., 2008; Sit and Sarpeshkar, 2007b), and overall facility of implementation (Arfin et al., 2009; Ghovanloo and Najafi, 2004; Ghovanloo and Najafi, 2005; Thurgood et al., 2009; Livi et al., 2010; Cheng et al., 2004; Ortmanns

et al., 2007; Lee et al., 2010). However, they are generally inefficient, consuming up to 10x the energy necessary to achieve stimulation of tissue. Voltage-based stimulators are sometimes used as an alternative to current stimulators because of their inherently higher energy efficiency (Simpson and Ghovanloo, 2007). However, they suffer from poor charge and current control and are especially sensitive to changes in electrode impedance. In (Kelly and Wyatt, 2011), the authors described a novel system for efficient neural stimulation through the use of a bank of capacitors precharged to specific voltages. The capacitors were connected directly to the electrode in sequence as a means of keeping the difference between the electrode voltage and capacitor voltage small thus enabling adiabatic improvements in energy efficiency (Sarpeshkar, 2010). However, currents were neither constant nor controlled. In (Vidal and Ghovanloo, 2010), the authors demonstrated a prototype system with off-the-shelf discrete electronic parts, which was also based on a switched-capacitor bank, but that added current limiters in series with the electrode to keep its current relatively constant. Since capacitor banks only allow for coarse discrete adiabatic operation, both implementations are inherently not as energy efficient as continuous voltage-based implementations. The use of explicit current limiters in the latter implementation degrades energy efficiency. Thus, we were motivated to seek alternative solutions.

In this work, we use a dynamic power supply based on inductive energy storage for adiabatically driving the electrode with a continuum of possible voltages instead of just the discrete steps offered by a capacitor bank. Further, the electrode current is sensed and kept at the desired level through feedback adjustment of the dynamic power supply output voltage, even as the electrode voltage is changing. In other words, as the electrode voltage changes from the charging current, the feedback loop adapts and continuously servos the dynamic power supply output voltage to maintain the appropriate current level without dissipative current sources or limiters. This permits our adiabatic stimulator to maintain efficient, precise voltage control over an electrode while also maintaining precise current control. Thus, our dynamic power supply automatically adapts to, or *tracks* the internal electrode voltage. Because our feedback scheme is based on current sensing, the feedback loop's tracking is independent of the electrode impedance.

The organization of this paper is as follows: In Section 4.3, we describe how stimulation with an adiabatic dynamic power supply improves energy efficiency and also describe the general architecture used in this work. In Section 4.4, we describe the operation of the circuits in this stimulator in detail. In Section 4.5, we analyze the stimulator's theoretical performance. Finally, in Section 4.6, we present the results of the stimulator and compare theory with experimental measurements.

4.3 Stimulation with a Dynamic Power Supply

4.3.1 Energy Loss in Current-Source-Based Stimulators

Current-source-based stimulation, though desirable for its precise, safe control, is relatively inefficient. Two current source stimulator configurations are shown in Fig. 4-1. Here we have modeled the electrode as a series combination of resistor R_s and capacitor C_{dl} based on the well known model due to Randles (Randles, 1947). The parameter R_s is the solution resistance, and C_{dl} is the double-layer capacitance. Ideal electrodes have minimal series resistance and high capacitance, enabling effective operation at lower voltages. In Fig. 4-1(a), a switch allows the electrode to be either connected to the positive power supply, V_{DD}, via the current source $I_{CS,P}$, the negative power supply, V_{SS}, via $I_{CS,N}$, or connected to ground to short out any accumulated charge. Both current sources restrict the flow of current, dissipating a large amount of energy due to the voltage difference between the power supply and the electrode appearing across the current sources. Fig. 4-1(b) shows the same circuit, but all voltages have been shifted such that the electrode can now be connected to either V_{DD} or ground via a current source, while the electrode baseline potential is set midway by a second supply, V_{mid}. To keep the circuits of Figs. 4-1(a) and (b) on equal footing, V_{DD} of (b) is set equal to $V_{DD} + |V_{SS}|$ of (a), with V_{mid} halfway between V_{DD} of (b) and ground.

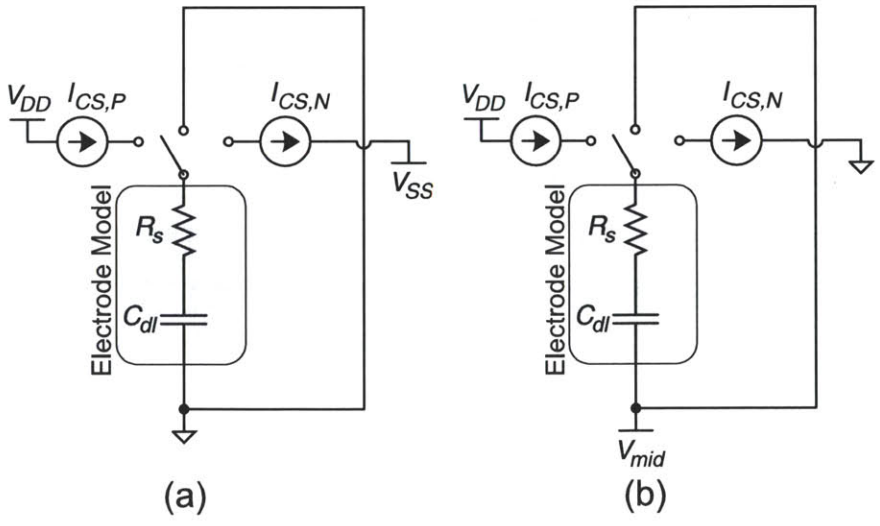


Figure 4-1: (a) Simplified stimulator based upon controlled current sources with dual power supplies. (b) Simplified stimulator based upon controlled current sources with a single power supply plus a midrail power supply V_{mid}.

Fig. 4-2 shows graphically how current sources can waste energy. For example, suppose that C_{dl} is initially uncharged and the electrode is floating. Now suppose that $I_{CS,N}$ is switched on,

connecting the electrode to V_{SS}. Initially, since there is no charge on C_{dl}, most of the energy taken from the power supply is wasted in $I_{CS,N}$. As the stored energy in C_{dl} increases and the voltage magnitude across C_{dl} increases, the voltage drop and hence instantaneous energy dissipated in $I_{CS,N}$ decreases. During the discharge cycle, the electrode is connected to V_{DD} via $I_{CS,P}$. Once again, energy is dissipated in $I_{CS,P}$ as shown in Fig. 4-2. It should be noted that Fig. 4-2 does not depict the energy stored in C_{dl} which is also partly dissipated in R_s. In principle, this energy stored in C_{dl} is recoverable, and our stimulator design will in fact attempt to recover a large fraction of it. Additionally, to dissipate the least possible energy in a current-source-based design, one would need to set the V_{DD} and V_{SS} rails as low as possible given the expected excursions of the electrode voltage. Often, supply rails are designed much higher than necessary to allow for worst-case scenarios. Such design leads to even greater energy dissipation.

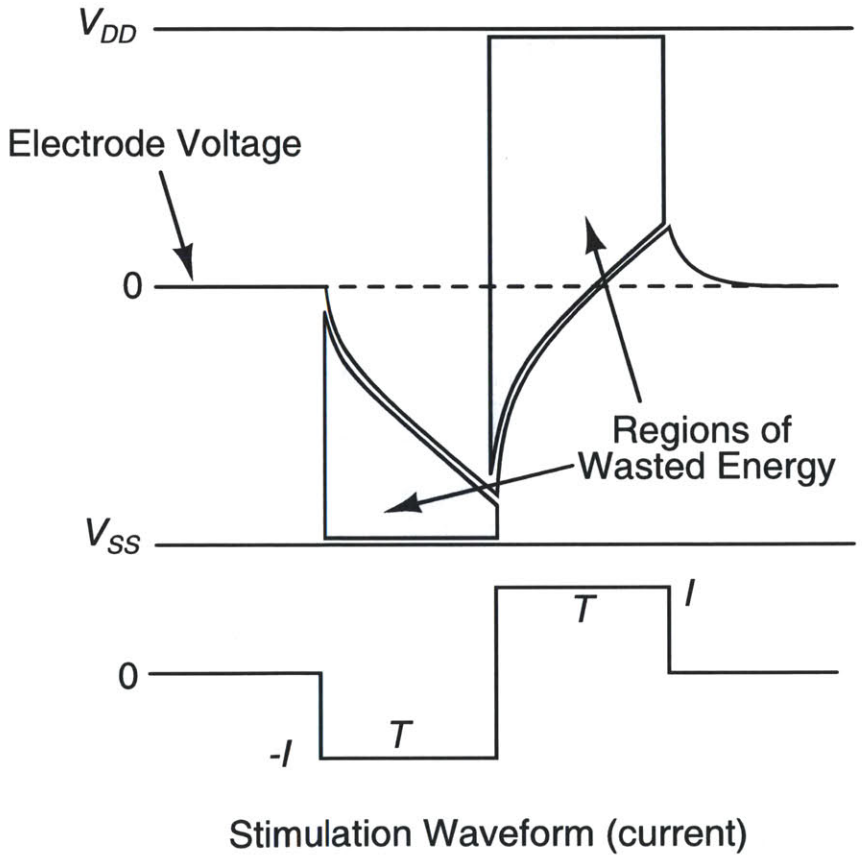


Figure 4-2: A cathodic-first biphasic pulse of current. During the cathodic phase, a current source connects the electrode to V_{SS}. The shaded region indicates the excessive voltage being dropped across the current source. During the anodic phase, the electrode is connected to V_{DD} via a current source. Again, the shaded region shows excessive voltage being dropped across the current source. In both cases, energy is lost in the current sources. Additional energy stored in C_{dl} (not shown), which is recoverable, is also lost.

4.3.2 Dynamic Electrode Power Supply

It can be shown relatively easily that for any given charge-transfer requirement within a given time interval, a constant current spanning the whole interval will minimize the losses in the solution resistance (R_s) (Sarpeshkar, 2010). Current-source-based stimulators achieve this condition naturally, but themselves dissipate power. The currents produced by adiabatic switched-capacitor-based stimulators tend to be exponential in nature because a step change in stimulator voltage leads to an exponential decay in current due to the first order RC circuit created by the electrode's impedance. An adiabatic voltage-based stimulator that also provides a constant, controlled current leads to the highest possible energy efficiency.

Fig. 4-3 shows a block diagram that illustrates the key parts of an adiabatic voltage-based stimulator with current control. The dynamic power supply is implemented as a high-efficiency DC-DC converter that is controlled to maintain V_{elec} at a potential that is near that on C_{dl} and that is consistent with a desired constant electrode stimulation current. The current sensing is done with a shunt topology rather than with a series topology, as we explain later. In our implementation, only a single power supply, V_{DD} is used. With the use of a midrail voltage source, V_{mid}, at the return side of the electrode instead of ground, we avoid extreme conversion ratios or the need for a second converter to provide negative voltages. The only sources of dissipation are the solution resistance intrinsic to the electrodes themselves, and the imperfect efficiency of the dynamic power supply.

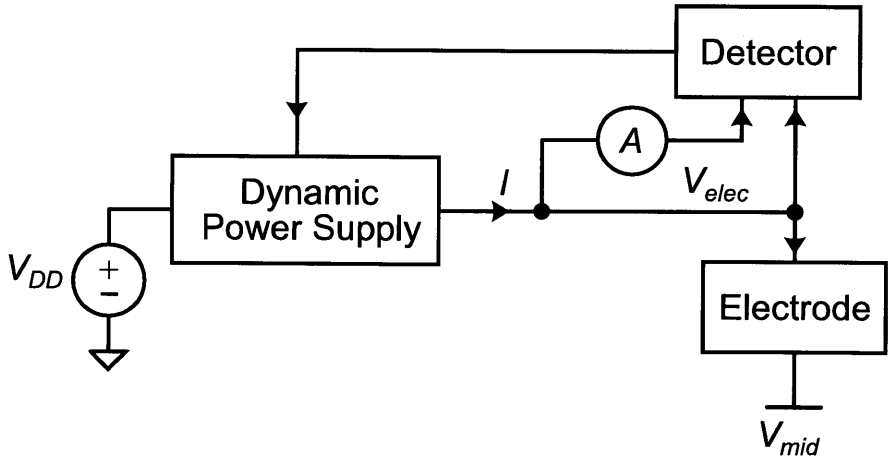


Figure 4-3: The critical parts of a voltage-based stimulator. Both the electrode current and voltage are actively monitored to provide simultaneous current and voltage control.

4.3.3 Dynamic Power Supply Requirements

Electrode stimuli are often in the neighborhood of hundreds of microseconds in duration. Thus, an electrode voltage, starting at rest, will develop anywhere from several hundred millivolts to several volts and back to rest in a brief span of time. In conventional power converter applications, load currents may vary over time, but load voltages are typically fixed or vary only slowly. Thus, a conventional power converter does not usually need a very fast response time or a very wide output voltage range. The design of the converter's load filter and choice of switching frequency dictate a compromise between settling time due to changes in either load or the output voltage, and peak-to-peak ripple of the output voltage. In a stimulation application, voltage ripple is not a serious concern. However, fast settling time to adapt to the quickly changing electrode voltage is required. This is particularly true during transitions from positive to negative electrode current and vice versa where near-instantaneous changes in the IR voltage drop across an electrode's solution resistance are required. A converter which cannot change its output voltage quickly cannot quickly effect changes in electrode current.

Biphasic pulses, required to create charge-balanced waveforms for safe stimulation, require that this power converter be able to both source and sink current. This is a particularly unusual requirement as power converters typically deliver current to a load rather than draw current from a load. However, a single converter able to run in two directions allows us to operate the stimulator from a single power supply, and perform energy recovery during the second, charge balancing phase of stimulation.

4.3.4 General Stimulator Architecture

The general architecture of the stimulator is shown in Fig. 4-4. There are two nested feedback loops for controlling the dynamic power supply. The inner feedback loop is a fast voltage control loop for the dynamic power supply core, a loop which is necessary in any ordinary DC-DC converter. It works by measuring V_{elec} and comparing it to a reference voltage set digitally by the slow outer current control loop. Inside the voltage control loop is a DAC which periodically samples V_{elec}. The set voltage input operates a set of switches inside the DAC, which redistribute the charge that was acquired when V_{elec} was sampled, effectively subtracting V_{elec} from the set voltage. When combined with a comparator, this procedure provides a readout of whether V_{elec} was greater than or less than the set voltage.

Unlike conventional DC-DC converters, the dynamic power supply can operate both forwards and backwards, delivering current to or from the electrode. We term these complementary modes *forward-buck* and *reverse-boost* respectively. In the forward-buck mode, if V_{elec} is below the set point, a pulse generator supplies a pair of control pulses to run the dynamic power supply for one cycle, causing V_{elec} to rise. In the reverse-boost mode, these operations are reversed. If V_{elec} is too high for the set voltage, the pulse generator fires off a pair of control pulses in the opposite order to let the dynamic power supply lower V_{elec}, thereby returning energy to the power supply.

The slow outer loop measures the current in the electrode via a special shunt sensing technique and operates in a symmetric manner for the forward-buck and reverse-boost modes. The output of the current-sensor is a voltage proportional to the electrode current. The desired "set" current is controlled by the voltage input V_{cur}. If the measured current magnitude is too small, a digital counter increments the set voltage magnitude by a fixed number of LSB's denoted D_{attack}. If the measured current magnitude is too large, the counter decrements the set voltage magnitude by a separate fixed number of LSB's denoted $D_{release}$. The state of this counter is used to control a DAC inside the fast voltage control loop which creates the set voltage reference. In both modes, current flow is limited, and set by the electrode's own internal resistance and the output voltage of the dynamic power supply. To assure stability, the slow outer loop allows for the inner voltage loop to settle before it makes any adjustments to the set voltage.

4.4 Circuit Operation

4.4.1 Dynamic Power Supply

The source topology for our dynamic power supply is shown in Fig. 4-5 and is based on a buck converter topology. In normal buck converter operation, $V_{out} < V_{in}$ and energy is transferred from C_{in} to C_{out}. This voltage downconversion is achieved by first turning on M_p to flux up the inductor, and then turning on M_n to release the stored energy in the inductor to the load. Such operation corresponds to our forward-buck mode. For simplicity, the electrode load normally connected to V_{out} and in parallel with C_{out} has been omitted.

In our reverse-boost mode, the switch order is commutated to reverse the flow of energy from the output at a lower voltage to the input at a higher voltage. In this reverse-boost mode, M_n is turned on first, negatively fluxing up the inductor by withdrawing energy from C_{out}. Then, M_p is turned on, which releases the energy stored in the inductor into C_{in}. Because energy recycling is

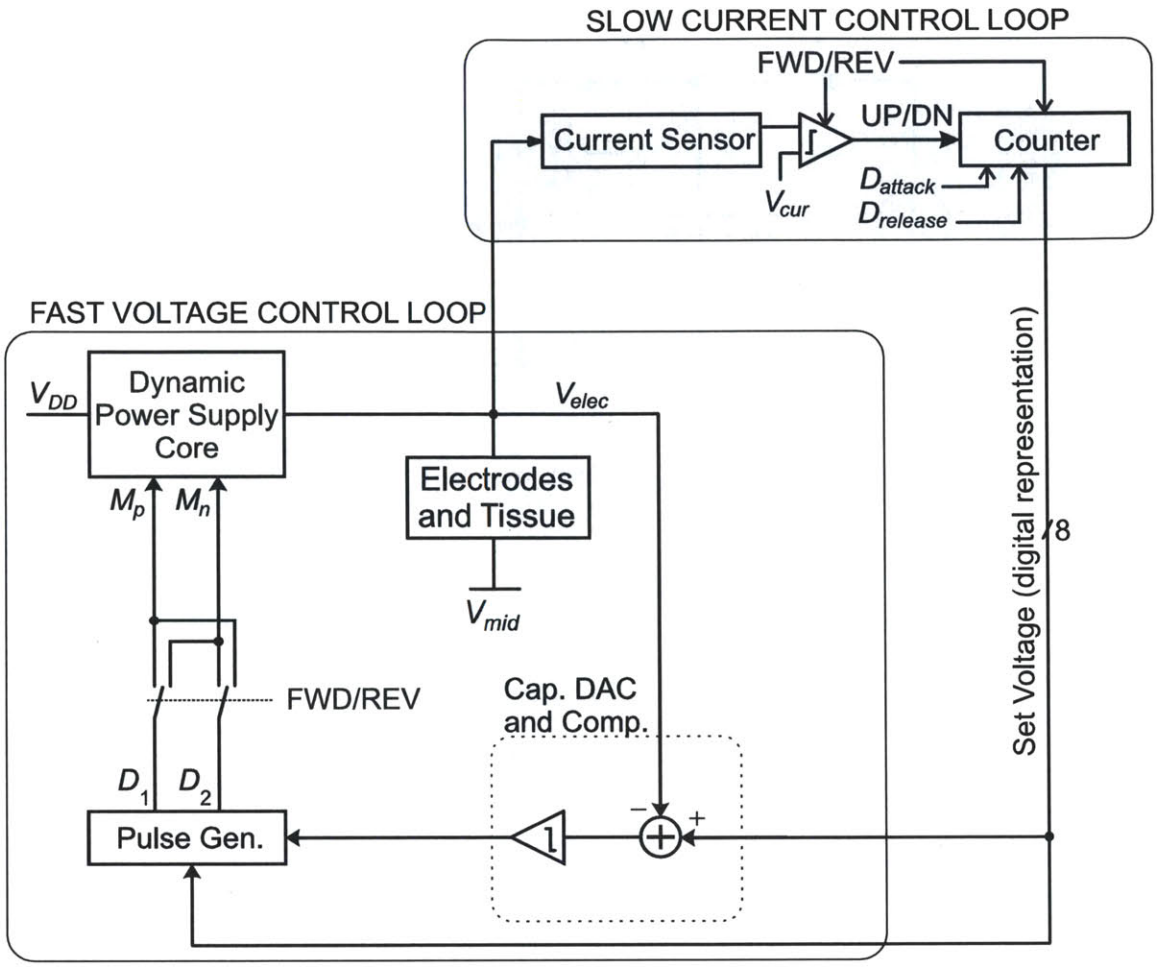


Figure 4-4: Architecture of the Adiabatic Electrode Stimulator

never 100% efficient in practice, and because there is dissipation in the load resistance R_s, C_{in} is periodically "topped-off" by V_{DD} by closing S_1 to replenish charge loss in C_{in} over a cycle. Fig. 4-6 illustrates the range of output voltages and flow of power for our dynamic power supply. In the forward-buck mode, the signals D_1 and D_2 (Fig. 4-4) operate M_p and M_n (Fig. 4-5) respectively. In the reverse-boost mode, D_1 and D_2 operate M_n and M_p respectively.

In our design, a fixed switching frequency of 250 kHz was chosen as a compromise between speed and power consumption, as higher switching frequencies consume greater power in their control circuitry. For instance, a neural stimulation pulse at 1 ms/phase would allow for 250 individual switching cycles/phase. Our sampling choice provides enough resolution to produce a reasonably accurate pulse shape. The components L and C_{out} may be adjusted to meet the power and speed requirements of any individual application.

Since the dynamic power supply must be able to a power a variety of loads, ranging from very

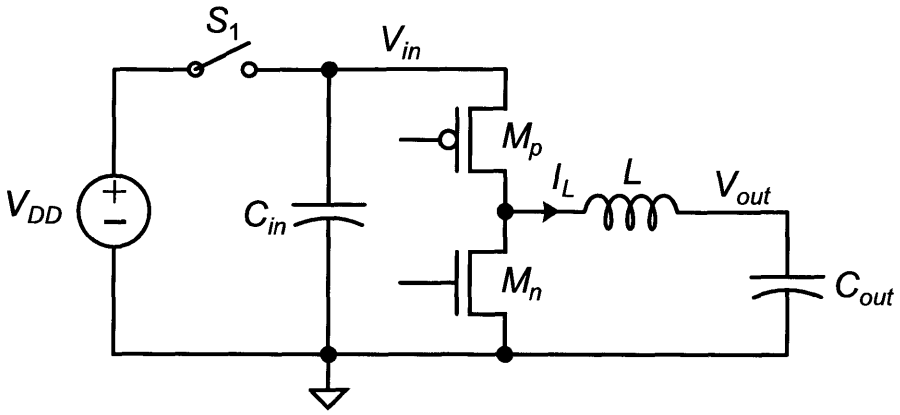


Figure 4-5: Basic forward-buck / reverse-boost converter.

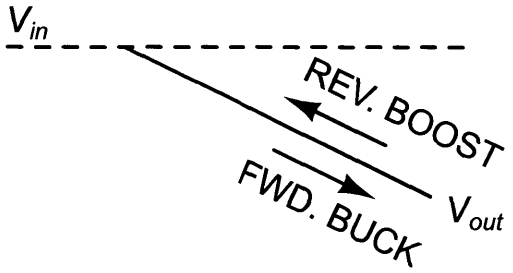


Figure 4-6: The arrows represent the flow of power in the dynamic power supply, with $V_{out} < V_{in}$.

light, to moderate, the discontinuous conduction mode (DCM) and a pulse frequency modulated (PFM) control strategy were chosen (Xiao et al., 2004). Under PFM, the voltage control loop pulses D_1 and D_2 only as necessary, as determined by feedback monitoring of V_{out}. Thus, there will be a maximum possible load current I_{load}^{max} that our dynamic power supply can support, corresponding to a pulsing cycle occurring at every switching interval T. At lighter loads, the power supply will pulse in any given switching interval with probability of activity P_a, resulting in an average apparent switching of interval of $T_{apparent} = T/P_a$. The absolute duration of D_1 and D_2 therefore do not change with load. However, the frequency at which D_1 and D_2 pulse will change with load.

Let us allow D_1 and D_2 to represent the fractions of the nominal switching period T for which each signal enables the corresponding switches M_p or M_n respectively. Thus, any time the power supply pulses in the forward-buck mode, the energy taken from C_{in} is:

$$E_{C_{in}} = \frac{V_{in}\left(V_{in} - V_{out}\right)}{2L} {D_1}^2 T^2 \tag{4.1}$$

However, because the power supply may not be required to pulse at the maximum possible frequency, this energy will be consumed by the load over the interval $T_{apparent}$. The energy consumed by the

load is:

$$E_{load} = V_{out} \times I_{load} \times T/P_a \tag{4.2}$$

Equating $E_{C_{in}}$ and E_{load}, we obtain the following relationship for our dynamic power supply operating in DCM:

$$D_1{}^2 = \frac{2L \times V_{out} \times I_{load}/P_a}{V_{in}(V_{in} - V_{out})T} \tag{4.3}$$

where I_{load} is the average current into the electrode, V_{in} and V_{out} are the input and output voltages respectively, T is the available switching interval, L is the inductance of the inductor, and P_a is the probability that the dynamic power supply actually pulses during any given switching interval. The parameters V_{in}, L, I_{load}, and T are user-settable constants by design. We also assume that the change in V_{out} in a given switching cycle is small such that V_{out} can be considered constant throughout the cycle.

In designing D_1 and D_2, consider the dynamic power supply in forward-buck mode. The signal D_1 closes M_p, placing a voltage $V_{in} - V_{out}$ across the inductor, leading to a steady buildup of current in the inductor. Then, M_p is opened and M_n is closed according to D_2, placing $-V_{out}$ across the inductor. In order to prevent an unlimited buildup of flux in the inductor, the average voltage across the inductor must be zero. This condition leads to the relationship between D_1 and D_2 shown in Equation 4.4.

$$D_2 = \frac{V_{in} - V_{out}}{V_{out}} \times D_1 \tag{4.4}$$

One simple strategy for satisfying Equation 4.4 is to select D_1 to be constant and D_2 variable according to V_{out}. However, if D_1 were fixed in duration, a single pulse would cause a large increase in V_{out} if V_{out} were very low, but only a small increase in V_{out} if V_{out} were already large. This is acceptable if we have a large filtering capacitor, but not for a stimulator which needs to be able to adjust the output voltage quickly and uniformly over a wide range. We would like to find a scheme for D_1 and D_2 that causes the same change in V_{out} per pulse, independent of the present value of V_{out}. If we substitute Equation 4.3 for D_1 in Equation 4.4, we find that, remarkably, the product of D_1 and D_2 is a constant independent of V_{out}.

$$D_1 \times D_2 = \frac{2LI_{load}/P_a}{V_{in}T} \tag{4.5}$$

Thus, as the desired V_{out} changes, we must adjust the ratio of D_1 and D_2 in a feedforward manner to satisfy Equation 4.4 while simultaneously keeping the product of D_1 and D_2 constant to satisfy Equation 4.5. If both conditions are satisfied, whenever the converter pulses, the charge packet delivered per pulse and change in V_{out} immediately following the pulse are invariant with V_{out}. This property guarantees predictable operation of the dynamic power supply, regardless of the value of V_{out}. It should be noted that all these calculations are made assuming forward-buck operation, and apply equally to reverse-boost mode, as the topology and circuitry are identical but with the direction of current flow reversed.

4.4.2 The Midrail Reference

Fig. 4-7 shows the dynamic power supply with a model electrode as the load. Normally, a second electrode is required to complete the circuit. However, the model of this return electrode has been omitted by combining its model with the stimulating electrode into a single electrode model. Thus, the remote end of the electrode model corresponds to the bulk tissue whose potential has been set to V_{mid} by the midrail voltage reference, halfway between V_{DD} and ground. By maintaining the bulk tissue at an intermediate voltage, a single dynamic power supply can drive the stimulating electrode both above and below V_{mid}.

Because all stimuli are designed to be charge neutral on average, it is not necessary for the midrail reference to supply any DC current. Hence, the midrail's role as an actual power supply is very limited. For that reason, we can create V_{mid} using the voltage reference $V_{mid,ref}$ and a large-valued RC filter network consisting of R_{mid} and C_{mid}, as shown in Fig. 4-7. Without this filter, all the instantaneous electrode current would both enter and leave $V_{mid,ref}$, requiring $V_{mid,ref}$ to be a genuine DC supply. With the filter in place, $V_{mid,ref}$ can be a high impedance voltage reference. Thus, R_{mid} can be explicit or implied in the output impedance of $V_{mid,ref}$. During stimulation, C_{mid} will absorb all the charge fluctuations but keep V_{mid} stable. This stability eases the design requirements on $V_{mid,ref}$, which only needs to be strong enough to initially charge up C_{mid}. The resistance R_{mid} also enhances safety by limiting any faulty DC current that may attempt to return to ground through $V_{mid,ref}$.

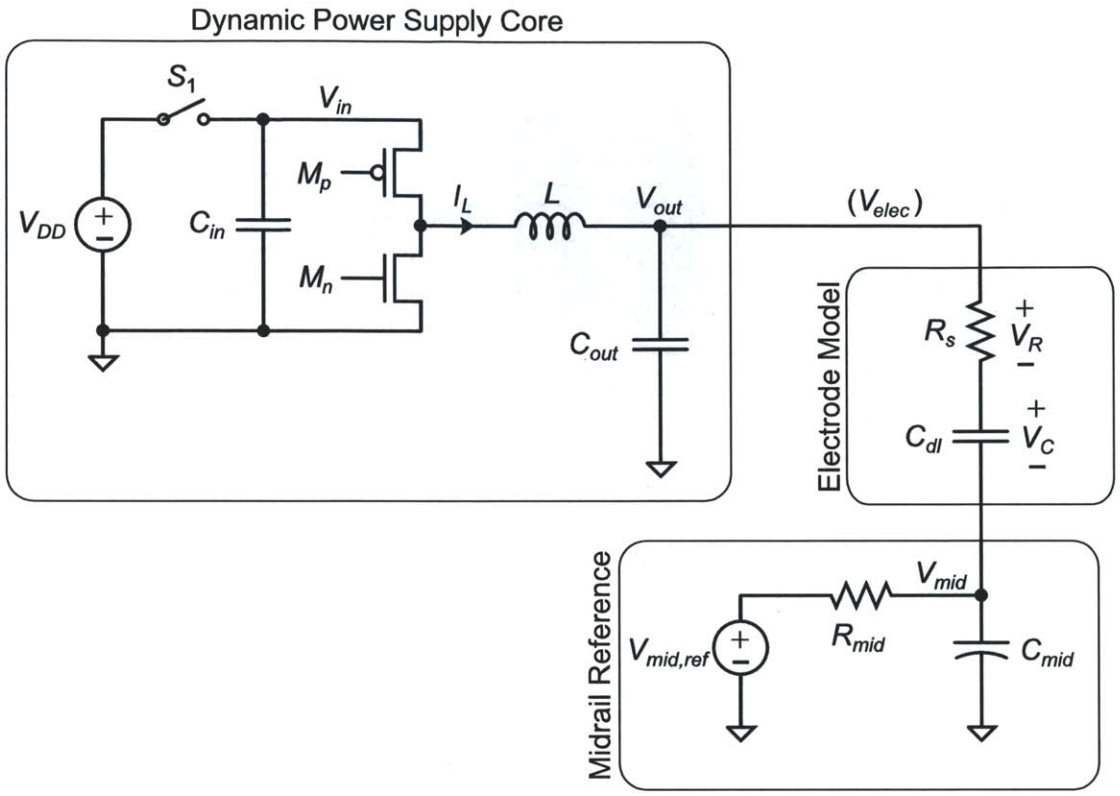


Figure 4-7: Dynamic power supply core with electrode load and midrail reference.

4.4.3 Switch Timing Generation

Generation of the switch timing signals D_1 and D_2 is accomplished through a delay line comprising 20 unit elements as shown in Fig. 4-8. A multiplexer is used to select two outputs from the delay line based on the current set value of V_{out} (the "set voltage" in Fig. 4-4). These two outputs, denoted V_1 and V_2, are used to generate the signals D_1 and D_2. An example is given in Fig. 4-9. Table 4.1 shows the 7 possible timing configurations that are available in this design (two of the 8 configurations are identical). One of these 7 configurations is chosen automatically via a lookup table using a digital representation of the dynamic power supply set voltage, as shown in Fig. 4-4. The tap positions were chosen such that the product of the number of delay units for D_1 and D_2 is constant across all settings (36 in Table 4.1).

4.4.4 Charge Redistribution DAC and Comparator

Our stimulator uses a charge redistribution DAC (Fig. A-23) and comparator (Fig. 4-12) to measure the the electrode voltage V_{elec}, and compare it to a reference voltage set by the bits $D_0 - D_7$. The DAC and comparator combination operate on multiple phases. During ϕ_{samp}, V_{elec} is sampled

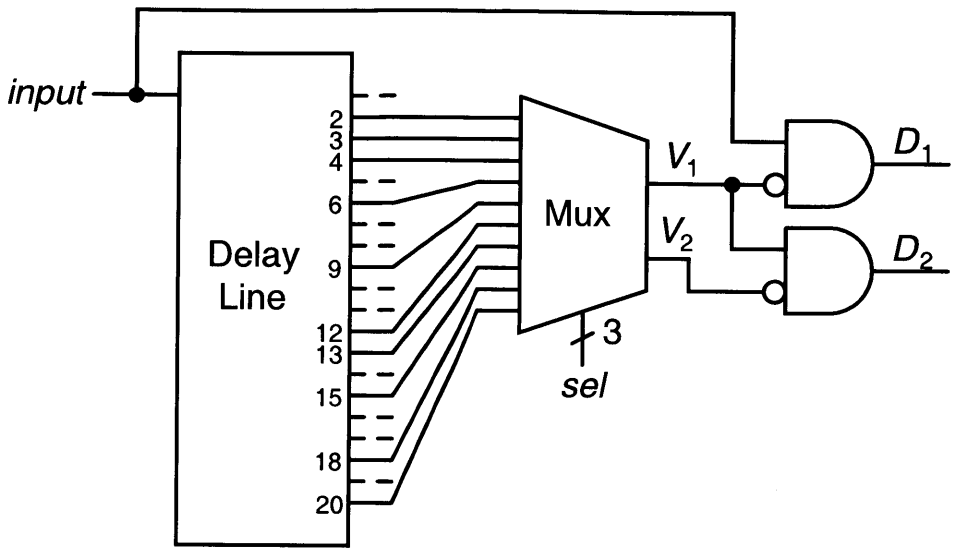


Figure 4-8: Circuit for generating the control pulses D_1 and D_2.

Table 4.1: Timing Selector Table

S_2	S_1	S_0	V_1 tap (D_1 Length)	V_2 tap	D_2 Length	Ratio
0	0	0	2	20	18	2:18
0	0	1	3	15	12	3:12
0	1	0	4	13	9	4:9
0	1	1	6	12	6	6:6
1	0	0	6	12	6	6:6
1	0	1	9	13	4	9:4
1	1	0	12	15	3	12:3
1	1	1	18	20	2	18:2

onto the capacitor array. During ϕ_{redist}, charge is redistributed within the capacitor array based on $D_0 - D_7$. The phases ϕ_{samp} and ϕ_{redist} are non-overlapping. The DAC phases are indicated in parenthesis in Fig. 4-11.

We will now analyze how this DAC works. For simplicity, we will work in normalized charge units, denoted by Q', where we have assumed all unit capacitors to be equal to 1 and unitless. During the sample phase, the switches controlled by ϕ_{samp} close, connecting the top plate of every capacitor to $V_{DD}/2$ and every bottom plate except that of the rightmost capacitor (the MSB capacitor) to V_{elec}. The MSB capacitor is instead connected to ground. Since the weight of the MSB capacitor, 128, is equal to the weights of all the other capacitors combined, this strategy has the effect of sampling half of the electrode voltage onto the capacitor array. Hence the electrode voltage may be rail-to-rail (ground to V_{DD}) while the internal reference voltages of the DAC and comparator can be at $V_{DD}/2$.

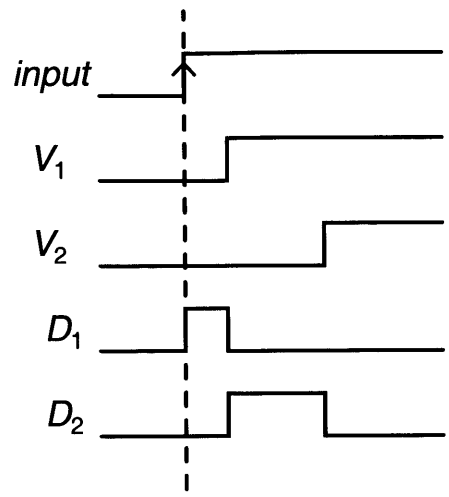


Figure 4-9: The individual voltage waveforms that generate the pulses D_1 and D_2.

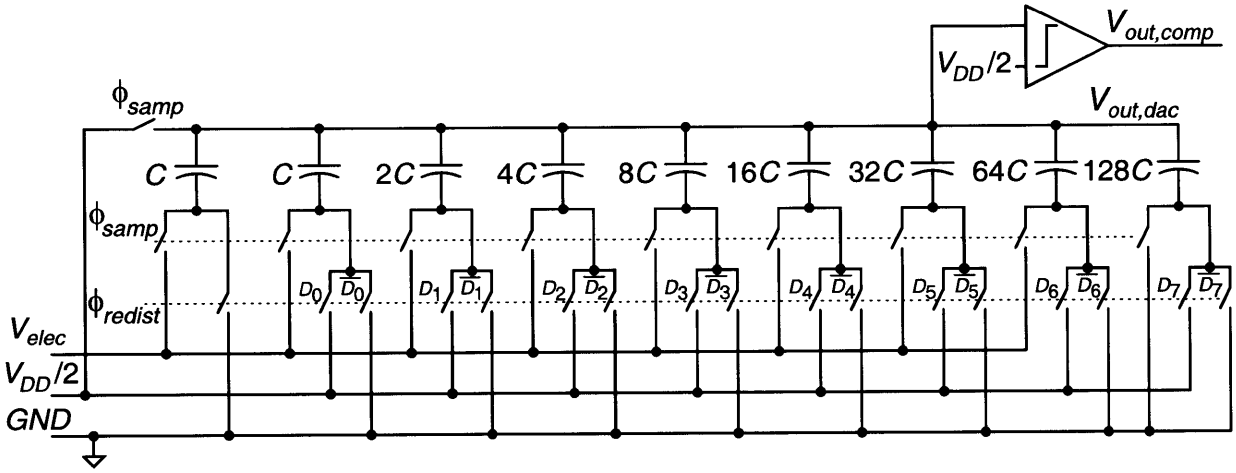


Figure 4-10: The charge redistribution DAC and comparator.

Thus, the normalized charge sampled on to the capacitor array is given by Equation 4.7.

$$Q' = \left(\frac{V_{DD}}{2} - V_{elec}\right) \times 128 + \left(\frac{V_{DD}}{2} - 0\right) \times 128 \tag{4.6}$$

$$= (V_{DD} - V_{elec}) \times 128 \tag{4.7}$$

At the end of ϕ_{samp}, the top plate switch opens, permanently locking in the charge on the capacitor array. A moment later, all the bottom plate sampling switches open. Now, during the redistribution phase, ϕ_{redist}, each capacitor's bottom plate will be connected to either $V_{DD}/2$ or GND, depending on the DAC code represented by individual bits D_i. This scheme is shown in

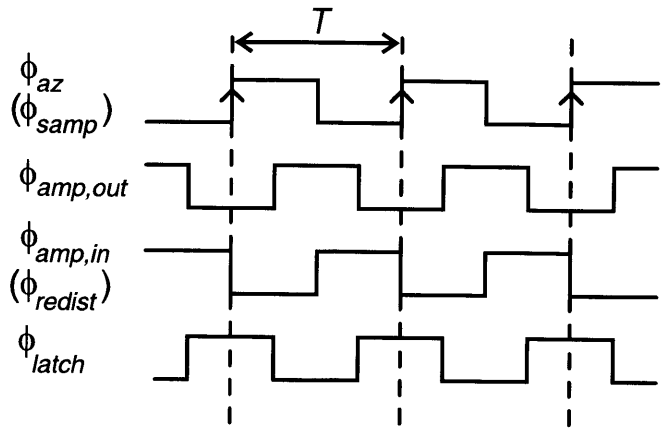


Figure 4-11: Phases of the comparator with the simultaneous phases of the charge redistribution DAC shown in parentheses.

Fig. A-23 as a pair of switches per capacitor, each controlled by ϕ_{redist} and the state of D_i, where i is the i^{th} bit. The code must be an integer between 0 and 255 inclusive.

For the moment, $V_{out,dac}$, the output voltage of the DAC remains unknown. The charge stored by all capacitors whose bit D_i was high is therefore:

$$\left(V_{out,dac} - \frac{V_{DD}}{2}\right) \times code$$

The charge stored by all capacitors whose bit D_i was low, including the leftmost capacitor, which is always connected to GND during the redistribution phase, is;

$$(V_{out,dac} - 0)\,(256 - code)$$

These equations lead to a total charge stored on the entire array, following redistribution:

$$\begin{aligned} Q' &= \left(V_{out,dac} - \frac{V_{DD}}{2}\right) \times code + (V_{out,dac} - 0)\,(256 - code) \\ &= -\frac{V_{DD}}{2} \times code + V_{out,dac} \times 256 \end{aligned} \tag{4.8}$$

Since charge is conserved between the sampling and redistribution phases, we can equate Equations 4.7 and 4.8 to solve for $V_{out,dac}$ after redistribution.

$$-\frac{V_{DD}}{2} \times code + V_{out,dac} \times 256 = (V_{DD} - V_{elec}) \times 128 \tag{4.9}$$

which simplifies to:

$$\boxed{V_{out,dac} = \frac{V_{DD}}{2} - \left(\frac{V_{elec}}{2} - \left(\frac{V_{DD}}{2} \times \frac{code}{256}\right)\right)} \tag{4.10}$$

Thus, we see that $V_{out,dac}$ is equal to $V_{DD}/2$ only if $V_{elec} = V_{DD} \times code/256$. The voltage $V_{out,dac}$ is directly connected to a clocked comparator, the output of which, $V_{out,comp}$, is also shown in Fig. A-23. The circuit for the comparator is given in Fig. 4-12.

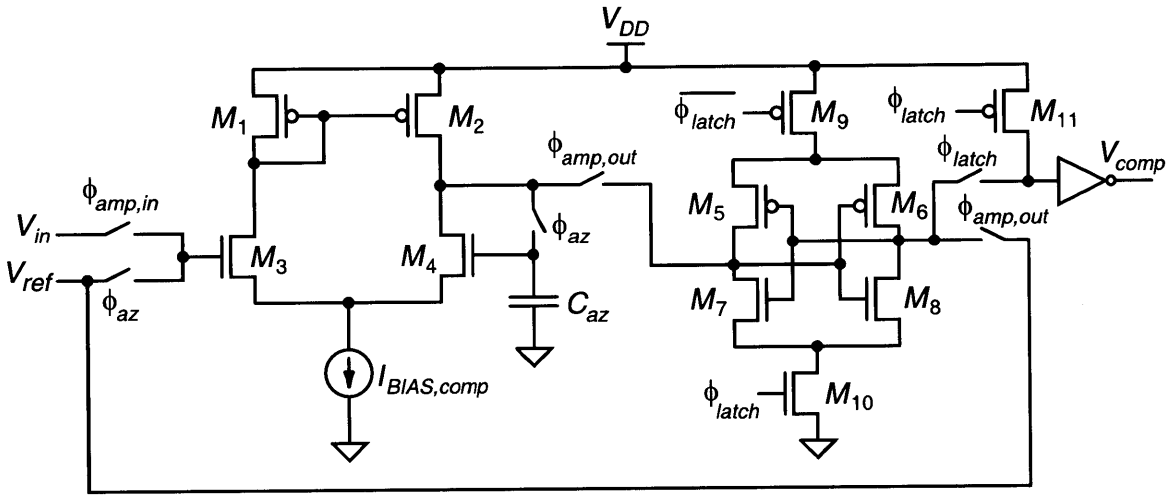


Figure 4-12: Schematic of the comparator circuit.

The comparator works based on a series of four overlapping phases. The order of the phases is shown in Fig. 4-11. These comparator phases also coincide with the sampling and redistribution of the phases of the DAC, as indicated. The comparator is a conventional clocked design, consisting of a preamplifier ($M_1 - M_4$), and a latch ($M_5 - M_8$).

The operation of the comparator is as follows: During ϕ_{az}, the preamplifier is placed in unity-gain. The input to the preamplifier is V_{ref}, equal to $V_{DD}/2$. Thus, because of the unity gain configuration, the output of the preamplifier is also V_{ref}, excluding any offset that may exist within the preamplifier and any errors due to the amplifier's finite DC gain. The overall topology results in the preamplifier being auto-zeroed, with any offset stored on C_{az}. Halfway through ϕ_{az}, the comparator enters $\phi_{amp,out}$, which connects the output of the preamplifier to the output of the latch which is, for the moment, in a high-impedance or "high-Z" state because ϕ_{latch} and $\overline{\phi_{latch}}$ are in an inactivating state for M_{10} and M_9. The complementary output of the latch, also high-Z, is held simply at V_{ref}[1].

[1]If the preamplifier were fully differential, the complementary output of the latch would receive the corresponding complementary output of the differential preamplifier. Making the preamplifier output single-ended simplifies the comparator design

In principle, the output of the preamplifier does not move at all during this transition because the preamplifier input has not changed and the offset value is still held on C_{az}. Halfway through $\phi_{amp,out}$, ϕ_{az} ends and $\phi_{amp,in}$ begins. At the same time, the DAC transitions from the sampling phase (ϕ_{samp}) to the redistribution phase (ϕ_{redist}). The DAC output, which is now valid, is connected to the input of the preamplifier. Any difference between V_{in} and V_{ref} is amplified. Halfway through $\phi_{amp,in}$, $\phi_{amp,out}$ ends, locking the preamplified value in on the latch's own parasitic capacitance. Simultaneously, ϕ_{latch} begins, which causes the latch to regenerate. During ϕ_{latch}, the output V_{comp} is high whenever $V_{in} > V_{ref}$ and low when $V_{in} < V_{ref}$. At other times, V_{comp} is low due to the action of M_{11}.

4.4.5 Current-Sensor Circuit

To regulate the flow of current to and from the electrode, a circuit for sensing the current in the electrode is required. One possible design is to use a small series resistor to convert current into voltage. This method has two primary disadvantages: The use of a series sense resistor reduces valuable voltage headroom, and also consumes power. The larger the sense resistor, the worse each of these two problems become. However, a small sense resistor produces only small voltages, for instance, 1-10 mV for a 10 Ω resistor carrying 100-1000 μA of current. To be useful, these voltages would need to be amplified by an AC coupled or offset-compensated amplifier to avoid large output offsets drowning the small sense signal.

Our alternative design measures changes in the capacitor voltage V_{out} over a fixed time caused by the electrode current discharging the capacitor C_{out}. To ensure that the voltage change is solely caused by the electrode current, the transistors M_p and M_n are to be off during this measurement phase such that all the current to the electrode is supplied from C_{out}. If $C_{dl} \gg C_{out}$, which is often the case, and $R_s C_{out} \gg T$, where T is the dynamic power supply switching period, current leaks off C_{out} at an essentially constant rate, resulting in a linear droop in the voltage on C_{out}. If we measure the change in the electrode voltage ΔV_{elec} during a sense interval T_{sense}, the electrode current I is approximately given by

$$I = C_{out} \frac{\Delta V_{elec}}{T_{sense}} \tag{4.11}$$

Symmetric measurements occur during charging or discharging of C_{out} depending on the sign of the electrode current.

The current-sensor circuit shown in Fig. 4-13 helps us measure ΔV_{elec}. The circuit draws essentially no power from the electrode, and since it is in a shunt configuration with the electrode rather than in series with it, the electrode's voltage headroom is unaffected. The current-sensor circuit operates as a hybrid of a conventional capacitive-feedback amplifier and a track-and-hold circuit. The circuit has 3 primary phases of operation controlled by the states of two switches, themselves controlled by the signals ϕ_1 and ϕ_2. These phases are indicated in Fig. 4-14.

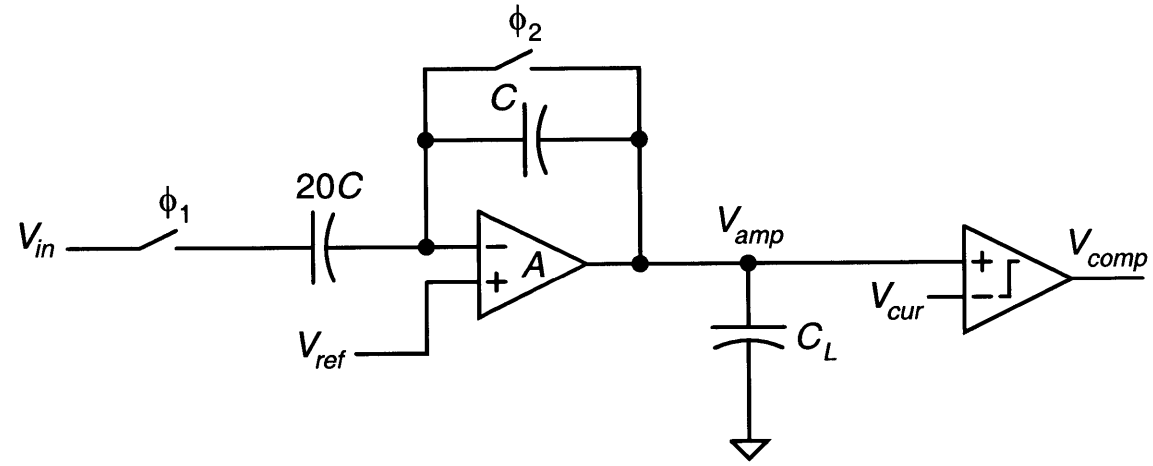


Figure 4-13: The capacitor-based current-sensor circuit with comparator shown at output.

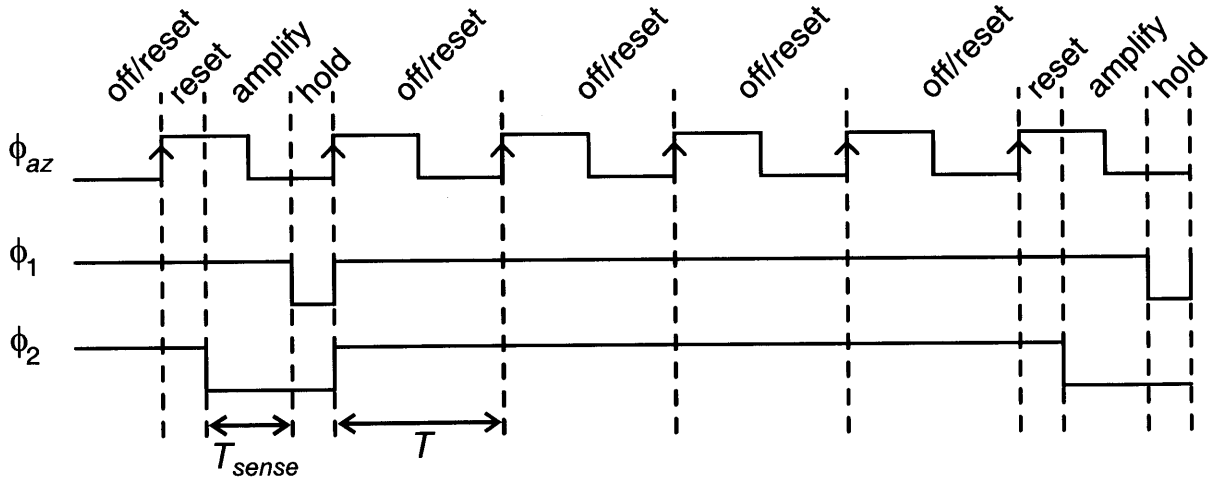


Figure 4-14: The phases of the current-sensor. The current-sensor measures the current on every fifth cycle of the dynamic power supply.

The operation of the current-sensor circuit is as follows: When both ϕ_1 and ϕ_2 are high, both switches in Fig. 4-13 are closed, corresponding to the reset phase. The amplifier runs in unity gain, highpass filtering the input. The DC level of V_{amp} settles to V_{ref}. During this time, and only during this time, M_p and M_n of Fig. 4-5 may be active. After a brief period, the switch controlled by ϕ_2

opens, placing the amplifier into a gain configuration whereby any changes in V_{in} are inverted and amplified by the gain determined by capacitor ratio, i.e., by a gain of -20. Finally, after the interval T_{sense} elapses, the switch controlled by ϕ_1 opens as well. With the input disconnected, V_{amp} is held by the amplifier while V_{amp} is compared to the reference voltage V_{cur}. Thus, the relationship between V_{amp} and V_{cur} indicates whether the measured current was above or below the set value. So far, we have assumed operation in the forward-buck mode. In the reverse-boost mode, ΔV_{elec} has the opposite sign compared to the forward-buck mode because the load powers C_{out}, causing V_{elec} to rise linearly instead of fall. Therefore, in the forward-buck mode, V_{cur} must be greater than V_{ref}. In the reverse-boost mode, V_{cur} must be less than V_{ref}. In both cases, $|V_{cur} - V_{ref}|$ encodes a desired current magnitude in the slow current loop. The signal V_{comp} is used to decide whether the the set voltage for the dynamic power supply should be raised or lowered, as discussed in Section 4.3. This signal is automatically inverted in the reverse-boost mode such that the sign of the Up/Down error correction in the feedback loop shown in Fig. 4-4 is automatically correct.

As can be inferred from the timing diagram (Fig. 4-14), the current-sensor circuit only detects and makes a decision once in every five conversion cycles of the dynamic power supply. This strategy allows ample settling time for the dynamic power supply to reach its new set point and helps ensure stability of V_{out}.

4.5 Theoretical Performance

4.5.1 Figure of Merit

An important figure of merit for stimulators, which can be calculated in all circumstances even if the properties of the electrode are unknown, is the ratio of the energy consumed by the stimulator to the energy that a constant current source stimulator would have used. This ratio is defined to be the Energy Factor relative to a constant Current Source stimulator (EF_{CS}). The minimum possible EF_{CS} is electrode dependent. An EF_{CS} less than 1 indicates a performance improvement with respect to a current source stimulator while an EF_{CS} greater than 1 indicates that a constant current source would be more energy efficient.

4.5.2 Energy Storage in the Midrail Reference

During stimulation, because the electrode's return is at V_{mid} and not at ground, there will be energy stored in C_{mid} during stimulation. It makes no difference whether the midrail reference is generated

as shown in Fig. 4-7 or if an explicit voltage source is used instead. Either way, the voltage V_{mid} is assumed to be constant throughout the duration of a stimulation. This assumption is a good one as long as C_{mid} is large enough and as long as current stimuli are charge-balanced.

From Fig. 4-7, it is apparent that the electrode's resistance R_s and capacitance C_{dl} is in series with C_{mid}, as shown in Fig. 4-15. Thus, when the electrode is charged with a constant current I_{stim} for duration T_{stim}, the energy stored in the electrode capacitance is $E_C = \frac{1}{2}C_{dl}{V_C}^2$. The energy stored in the midrail capacitor C_{mid} is approximately $E_{mid} = V_{mid} \times I_{stim} \times T_{stim}$, where we have assumed that C_{mid} is large enough to behave as a power supply for small signals. Therefore, the total energy stored in both the electrode and in C_{mid} is:

$$E_C{}' = \left(\frac{1}{2}V_C + V_{mid}\right) \times I_{stim} \times T_{stim} \tag{4.12}$$

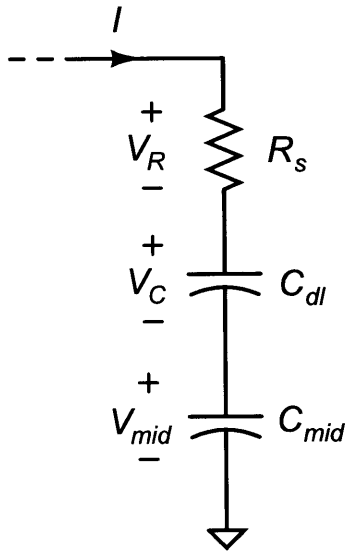


Figure 4-15: In the simplified electrode model, C_{mid} appears in series with R_s and C_{dl}.

If V_{mid} is $V_{DD}/2$ as is typical, the ratio of the energy stored in C_{mid} to the energy stored in the electrode capacitance is V_{DD}/V_C. Thus, during a typical stimulation, the peak energy stored in C_{mid} may be several times that stored in C_{dl}. In principle, the only energy required to be transferred is that which will be stored in C_{dl}, plus any energy dissipated in R_s. A dynamic power supply with perfect efficiency suffers no consequences from transferring energy back and forth. However, transferring extra energy, although it can be recovered during the second, charge-balancing phase of the stimulation, is dissipative because of dynamic power supply losses (no inductors, capacitors, or switches are perfectly lossless).

4.5.3 Comparison to a Conventional Current-Source-Based Stimulator

A current-source-based stimulator always consumes the same amount of energy, given by $E_{CS} = V_{DD} \times I_{stim} \times T_{stim}$, regardless of the electrode impedance. Note that in Fig. 4-1(b), the current source stimulation stores energy in V_{mid} during a charging phase when $I_{CS,P}$ is on, but dissipates that stored energy during a discharging phase when $I_{CS,N}$ is on. The net energy dissipation over both phases is given by:

$$\begin{aligned} &((V_{DD} - V_{mid})\, I_{stim} + V_{mid} \times I_{stim})\, T_{stim} \\ &= V_{DD} \times I_{stim} \times T_{stim} = E_{CS} \end{aligned} \tag{4.13}$$

In both current source stimulators and in our stimulator, if $V_{mid} = V_{DD}/2$, a peak energy $E_{mid,pk} = E_{CS}/2$ is stored on C_{mid} during the transition between charging and discharging phases. To supply $E_{mid,pk}$, an energy $E_{mid,pk}/\eta$ would be taken from V_{DD}, and an amount $E_{mid,pk} \times \eta$ would be returned. Compared to the energy consumed in a constant current source design, $E_{CS} = 2E_{mid,pk}$, we then obtain that:

$$EF_{CS} \geq \frac{1-\eta^2}{2\eta} \tag{4.14}$$

Thus, our stimulator performs at the same level as a constant current source stimulator when $\eta = \sqrt{2} - 1 = 41.4\%$. Efficiencies of at least 75% are routinely achievable, giving our stimulator an expected EF_{CS} of at least 0.29, or a 3.5x improvement over the constant current source stimulator for ideal electrodes. If the dynamic power supply efficiency increases to 90%, improvements of nearly 10x are possible.

In reality, electrode resistance contributes electrode dependent loss. The electrode capacitance also contributes loss because the capacitor must be charged and then discharged (or discharged and then charged) by a non-ideal dynamic power supply with less than 100% efficiency. The shuttling of electrode capacitive energy is subject to the imperfect efficiency of the dynamic power supply, just as is the energy stored in the midrail, E_{mid}.

To calculate EF_{CS} for an electrode with resistance R_s and capacitance C_{dl}, we must know approximately what the voltage drop, V_R, across the electrode resistance will be during the stimulation, and what the peak voltage attained across the electrode capacitor, V_C, will be. It is useful to

express both voltages as a fraction of the midrail voltage. Therefore, let us define α_C and α_R such that $V_C = \alpha_C V_{mid}$, and $V_R = \alpha_R V_{mid}$. For simplicity, we will assume that the electrode receives positive constant current during the first stimulation phase, and negative constant current during the second stimulation phase. However, the calculation has identical results even if the phase order is reversed. Thus, during the first phase of an electrode stimulation, if the energy stored in the midrail supply is E_{mid}, then the energy stored in the electrode capacitance is $(\alpha_C/2)\, E_{mid}$ because the average voltage across C_{dl} during charging is $V_C/2 = (\alpha_C/2)\, V_{mid}$. Finally, the energy dissipated in the resistor is $\alpha_R E_{mid}$. We divide the sum of these three component energies by η to determine the amount of energy that must have been taken from V_{DD}. During the second phase, energy is recovered from both the midrail supply and the electrode capacitor, but is dissipated in the electrode resistor. This energy is subject to the dynamic power supply efficiency, reducing the amount that can be returned to V_{DD}. Referring to the net energy taken from the supply as E_{sup}, the general form of EF_{CS} that includes all losses is given by Equation 4.15:

$$\begin{aligned} EF_{CS} = \frac{E_{sup}}{E_{CS}} &= \frac{\left(E_{mid} + \frac{1}{2}\alpha_C E_{mid} + \alpha_R E_{mid}\right)\frac{1}{\eta}}{2E_{mid}} \\ &\quad - \frac{\left(E_{mid} + \frac{1}{2}\alpha_C E_{mid} - \alpha_R E_{mid}\right)\eta}{2E_{mid}} \\ &= \frac{1-\eta^2}{2\eta}\left[1 + \frac{\alpha_C}{2} + \alpha_R \frac{(1+\eta^2)}{(1-\eta^2)}\right] \end{aligned} \tag{4.15}$$

Note that Equation 4.15 is consistent with the minimum value of EF_{CS} predicted by Equation 4.14 that analyzed EF_{CS} when there is no loss in the electrode.

Fig. 4-16 is a plot of the theoretical EF_{CS} vs. η for various values of α_C and α_R according to Equation 4.15. As expected, higher power supply efficiencies always lead to a lower EF_{CS} since energy recycling is then very efficient such that operation with respect to a constant current source stimulation is highly beneficial. We see that, at 90% power supply efficiencies, a 10x reduction in energy dissipation can result. Fig. 4-16 also shows that as α_C, and especially α_R increase, the EF_{CS} rises because more electrode energy is lost due to imperfect energy recycling in the dynamic power supply. Nevertheless, for almost all practical values of α_R, α_C, and η, EF_{CS} is well below 1, implying that our stimulator is more energy efficient than a current source stimulator.

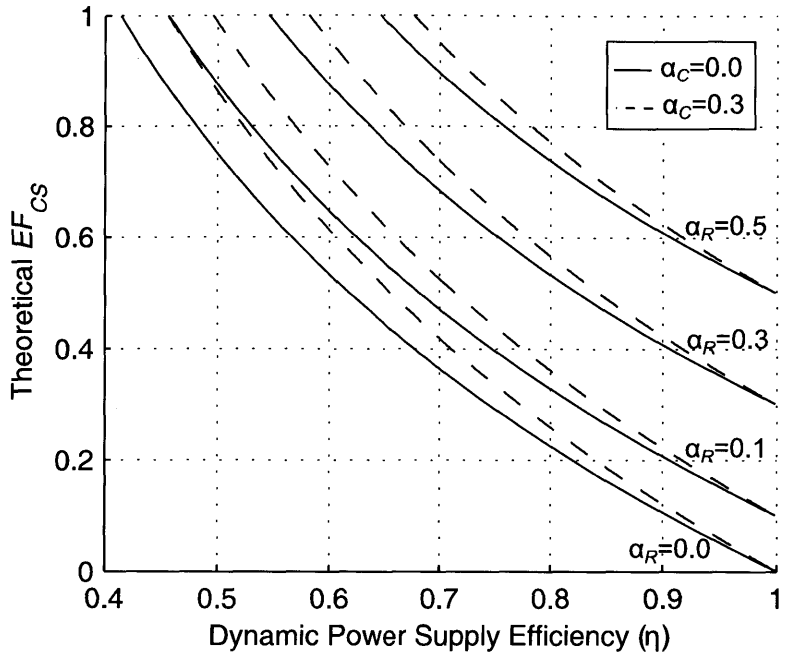


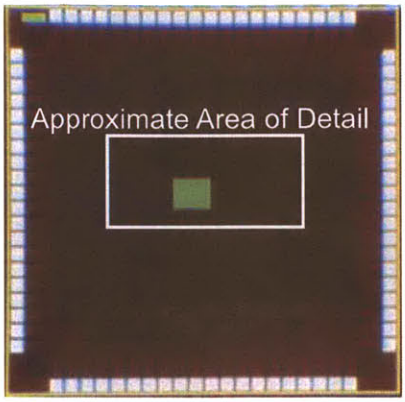
Figure 4-16: Theoretical EF_{CS} curves for different values of α_C and α_R.

4.6 Results

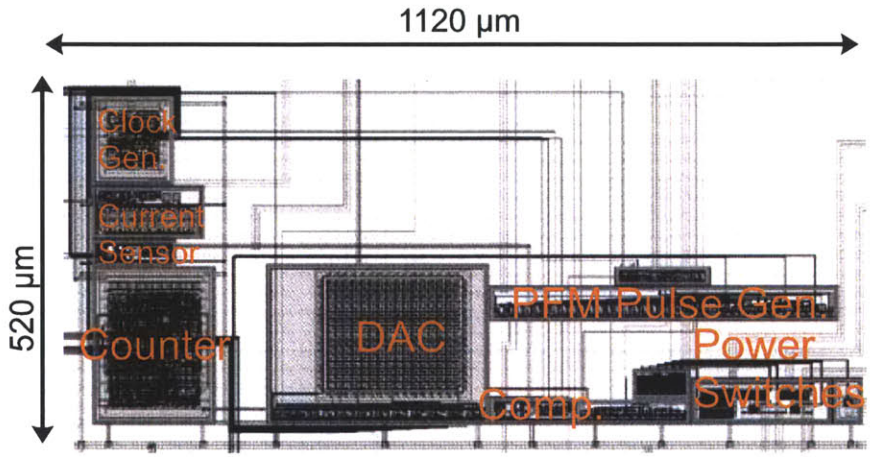
A single stimulator channel was fabricated in the ON Semiconductor (formerly AMI) 0.35 μm CMOS process. A photograph of the die (Fig. 4-17a) and the layout of a single channel with key parts labeled (Fig. 4-17b) are provided. The stimulator was constructed with external components L = 39 μH, C_{out} = 47 nF, and C_{in} = 4.7 μF. The period T for the voltage control was 4 μs, while the current control loop sampled the current at 20 μs intervals.

4.6.1 Dynamic Power Supply Efficiency Measurements

Fig. 4-18 shows the raw efficiency of our dynamic power supply when powering a 300 μA DC load. This efficiency considers only the fundamental transfer of energy to and from V_{DD} and the load via the dynamic power supply core, which effectively operates like a DC-DC converter. For these measurements, a fixed load was supplied by a DC current source (Keithley 2400). The output set voltage in Fig. 4-4 was swept over its entire range and measurements of the current from V_{DD} and the output voltage were taken to obtain the DC-DC converter efficiency. Note that the slow current feedback loop is effectively inactivated during these measurements because the set voltage is fixed externally and not allowed to vary. Although the current control loop was effectively overridden, it was not actually disabled. This procedure was repeated for both the forward and reverse dynamic



(a)



(b)

Figure 4-17: (a) Die microphotograph. (b) Screen capture of layout with major parts labeled.

power supply modes by exchanging the V_{DD} input and V_{elec} output. The output filter capacitor C_{out} was chosen to be 1 μF just for these measurements in order to create a well-smoothed voltage for V_{elec}. The control loop power, which includes all circuitry for electrode voltage and current sensing, set voltage counter, D_1 and D_2 pulse generation, and gate drive for M_p and M_n, was about 40 μW. This control power overhead will reduce the net efficiency of the converter on average by a few per cent. The bias currents for the current-sensor circuitry are still included in this control power. As a result, these measurements should reflect reality even in full dual-loop operation.

Measurements at the extremes of the voltage span (very near ground and V_{DD}) are not shown. The dynamic power supply did not operate well at those extremes. In practice, one should expect to limit the output voltage range to approximately 10-90% of the supply voltage. The transitions between duty-cycle modes in the dynamic power supply are easily seen in Fig. 4-18. At the discontinuities

in these curves, the converter is changing the duty cycles for D_1 and D_2, which are chosen as approximate values to suit a particular output voltage range.

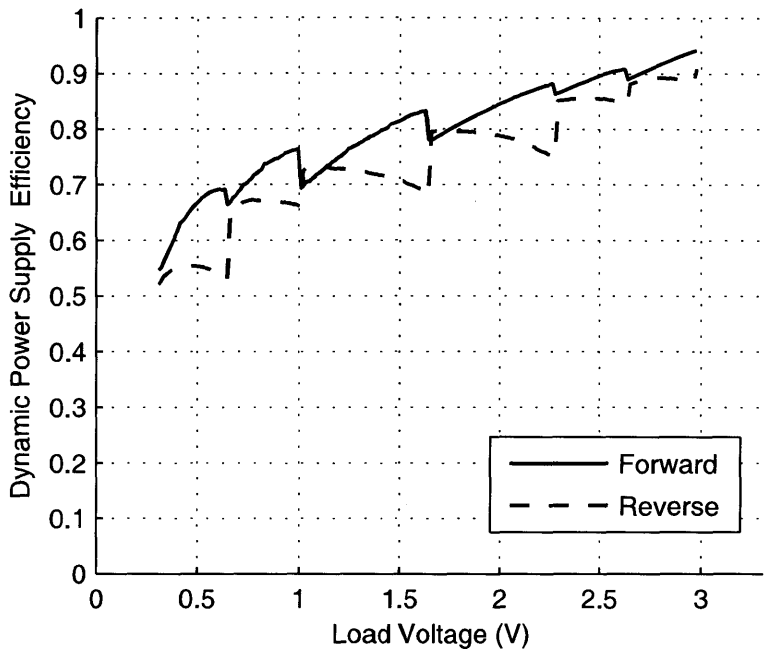


Figure 4-18: Efficiency of the dynamic power supply at DC, excluding control power. Including control power decreases efficiency slightly. The power supply was 3.3 V

4.6.2 Current Control Characterization

As previously described, the current controller works by measuring the droop (forward-buck) or rise (reverse-boost) on C_{out} in one conversion cycle to approximate the current. The rate of droop (or rise) is expected to be approximately invariant with load impedance, depending only on the load current. To characterize the current controller, the dynamic power supply was tested using different purely resistive loads. The data are shown in Fig. 4-19. The control voltage V_{cur} was swept over a range of 0$\pm$300 mV about V_{ref} to obtain data for the forward and reverse modes. As Fig. 4-19 reveals, currents ranged from 0-450 μA with good linearity over the entire range. Fig. 4-19 shows that changes in load do not significantly affect the load current, as expected.

4.6.3 Model Electrode Drive Measurements

The stimulator was tested with several model loads consisting of a series resistor and capacitor. Two values of V_{cur} were used, testing the stimulator at two different current levels. The values of the resistor and capacitor were chosen to be consistent with what is typically encountered with a

Medtronic DBS electrode (Wei and Grill, 2009; Medtronic, 2008). The power supply voltage was 3.3 V. Stimuli were 2 ms in duration, with 1 ms/phase. The energy usage of the stimulator was measured by monitoring the voltage on C_{in} throughout the stimulation. Since energy recycling is not perfect, C_{in} was "topped off" to recharge it back to V_{DD}. The change in the voltage across C_{in} during one stimulation represents the stimulator's energy usage.

Examples of stimulator waveforms for $|V_{cur} - V_{ref}|$ = 300 mV are given in Fig. 4-20. In subpanels (a) and (b), the voltage and current waveforms are shown for anodic-first stimuli. In subpanels (c) and (d), the same stimuli were applied cathodic first. The loads consist of a 0.93 μF capacitor in series with a 500, 1000 or 1500 Ω resistor. As in Fig. 4-19, it can be seen in Fig. 4-20 that variations in load impedance do not significantly affect the load current due to regulation by the current feedback loop, even as the load voltage is continuously changing.

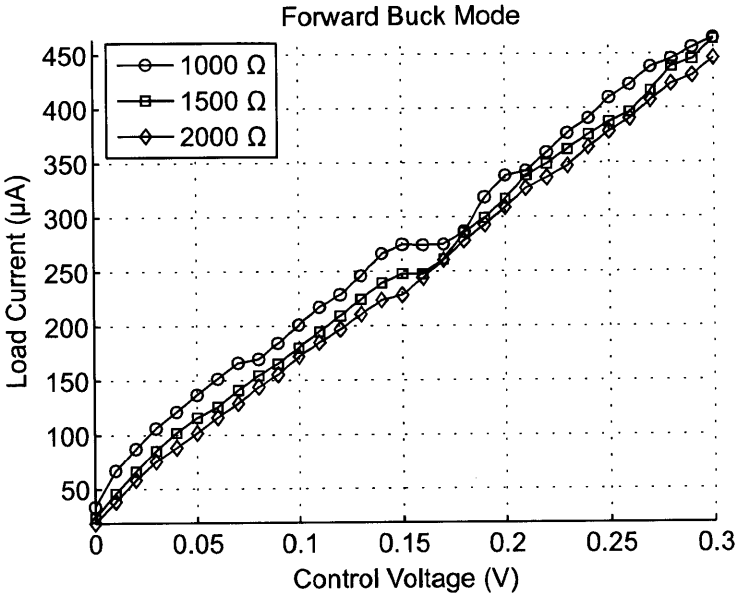
In Fig. 4-21, measured values of EF_{CS} are shown. In subpanel (a), $|V_{cur} - V_{ref}|$ = 200 mV. Since C_{dl} was set constant at 0.93 μF, α_C is always approximately 0.18 since V_{cur} is not varied. However, different values for R_s were selected, thus varying α_R. Each value of EF_{CS} was obtained by aggregating many trials with those particular values of V_{cur}, C_{dl}, and R_s. To see if the theory would agree with the data, the measured values of α_C, α_R, and EF_{CS} were input into Equation 4.15 and a best-fit line was obtained by finding the value of η that minimized the least-squared error. The values of η obtained from the fit were 82% for $|V_{cur} - V_{ref}|$ = 200 mV and 84% for $|V_{cur} - V_{ref}|$ = 300 mV. Both values are quite reasonable considering the measured values of the dynamic power supply efficiency under DC conditions. The theory presented in this paper correctly predicts the rise in EF_{CS} with increasing electrode impedance and also predicts EF_{CS} to within about $\pm$10% using an appropriate value of η. At smaller resistances, the EF_{CS} improves because although the constant current source stimulator continues to burn the same amount of energy regardless of the electrode impedance, our stimulator uses less energy.

It should be noted that these measurements do not include the energy required to run the control loop during the stimulation. However, that penalty is small – approximately 12 μA of current from a 3.3 V supply during the stimulation. In principle, the control loop could be turned off between stimuli, although we did not implement this improvement.

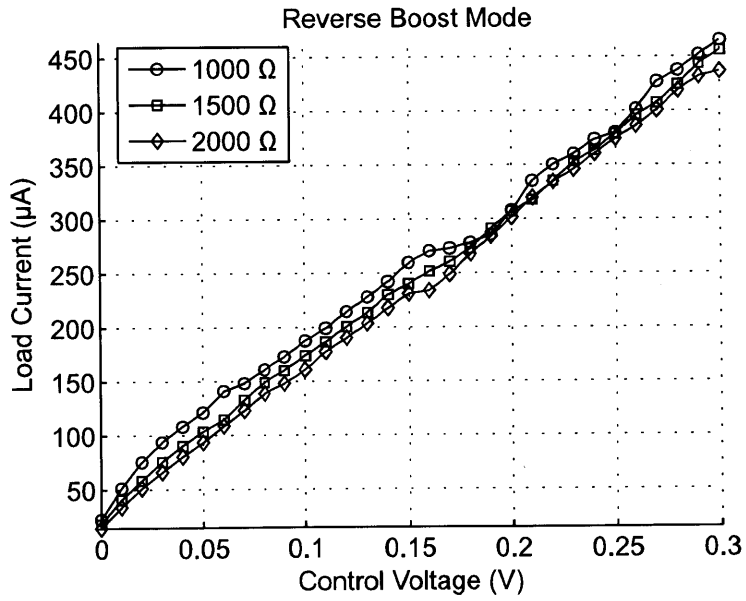
4.7 Conclusion

We have presented the design and measurement of an integrated-circuit adiabatic electrode stimulator which uses a dynamic power supply as a variable voltage source to efficiently drive an electrode with positive or negative current. The stimulator also monitors the current flow into or out of the electrode based upon a shunt current sensing technique, and adjusts the voltage output of the converter to maintain a constant current as selected by the user. This shunt technique operates on micropower and draws essentially no current from the electrode, avoiding the need for series current sense resistors or dissipative current limiters. We have demonstrated both in theory and in practice reductions in energy usage of 2-3x over conventional stimulators based on current sources.

The current sensing circuit makes the current output independent of the electrode impedance, a problem which routinely stymies other voltage-based stimulators due to highly variable electrode impedances. Because this technique is general, it can be used to drive any impedance at all, including LEDs for optical based stimulators (Boyden et al., 2005). When used in implantable medical devices, these energy reductions offered by our stimulator can be used to decrease the size of implanted batteries or coils, thereby reducing device size, increasing battery life time, reducing device costs, reducing heat dissipation, and increasing the quality of life of the patients. Our stimulator may be useful in cardiac, neural, muscular, cochlear, retinal, and other biomedical implants.



(a)



(b)

Figure 4-19: Load Current vs. Control Voltage ($|V_{cur} - V_{ref}|$ as in Fig. 4-13) is illustrated for the forward-buck mode (a), and reverse-boost mode (b) for different resistive loads.

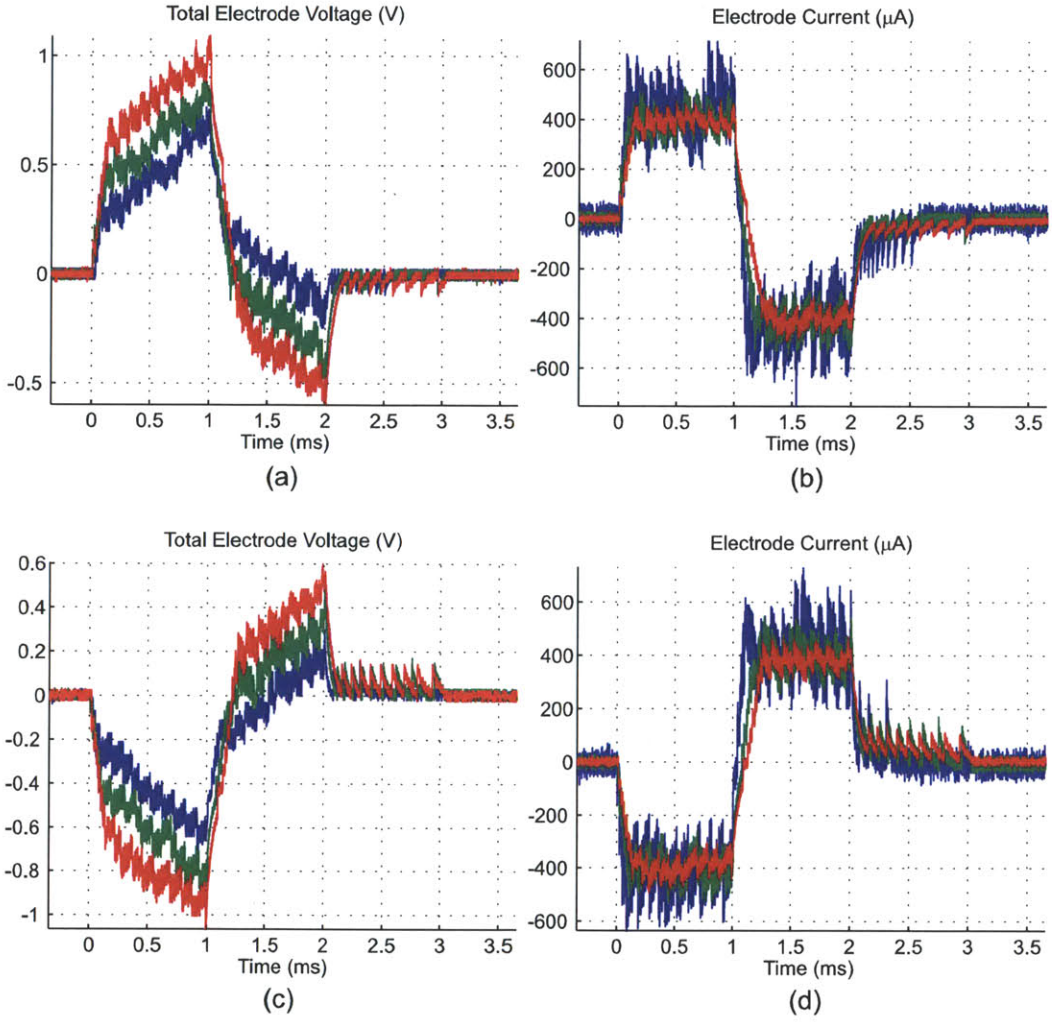


Figure 4-20: Time domain observations of model electrode under simultaneous current and voltage control, where $|V_{cur} - V_{ref}| = 300$ mV. For all experiments, $C_{dl} = 0.93$ μF. R_s varies according to colored curve: Blue (500 Ω), Green (1000 Ω), Red (1500 Ω). (a) Anodic-first electrode voltage. (b) Electrode current corresponding to (a). (c) Cathodic-first electrode voltage. (d) Electrode current corresponding to (c).

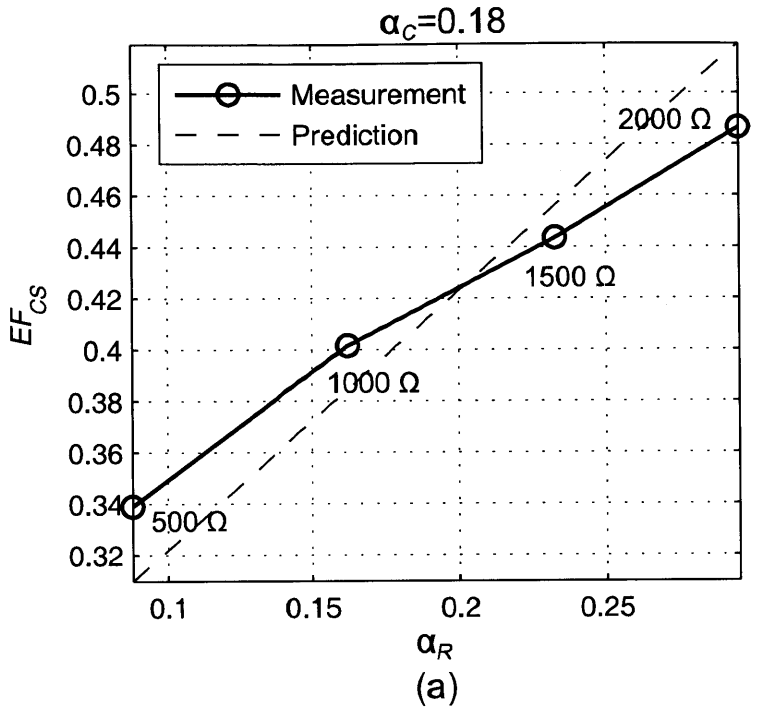


Figure 4-21: (a) Average EF_{CS} measurements where $|V_{cur} - V_{ref}|$ = 200 mV and theoretical prediction. (b) Average EF_{CS} measurements where $|V_{cur} - V_{ref}|$ = 300 mV and theoretical prediction. Both (a) and (b) are shown for a single value of α_C corresponding to C_{dl} = 0.93 μF and various values of α_R corresponding to various resistor values as shown.

Chapter 5

An Energy-Efficient, Adiabatic Electrode Stimulator: Additional Measurements

This chapter provides some additional measurements and discussion of the circuits described in Chapter 4. This chapter is not meant to stand alone and makes frequent references to Chapter 4.

5.1 DAC Characterization

The DAC of Figure A-23 used in the adiabatic electrode stimulator offers 8 bits of resolution. The DNL and INL for this DAC are shown in Figures 5-1(a) and 5-1(b) respectively. Both the DNL and INL are well below the conventional ± 0.5 LSB limit, guaranteeing monotonic operation.

5.1.1 Method of Measurement

The DAC operates by measuring the difference between a digitally coded set voltage in the bits $D_0 - D_7$ and the externally sampled voltage V_{elec}, and reports this difference as $V_{out,dac}$. However, only $V_{out,comp}$ was available externally. To obtain the true output value of the DAC, a probabilistic method was employed as follows: The bits $D_0 - D_7$ were first set externally to a particular value, and then V_{elec} was manually swept through a range of values such that $V_{out,comp}$ tripped. This sweep was repeated many times for a particular DAC value to obtain a probability distribution for whether or not the comparator will trip for a given value of V_{elec} and a given value of $D_0 - D_7$. This entire

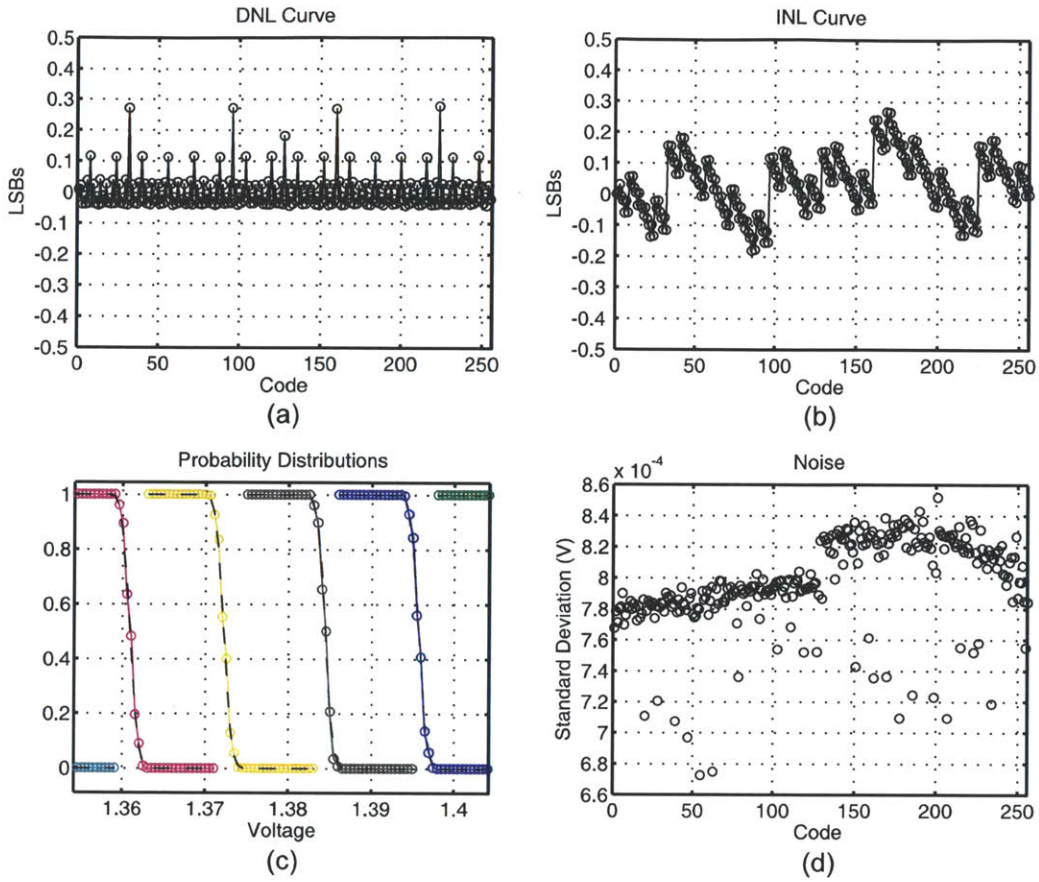


Figure 5-1: DAC characteristics. (a) DNL (b) INL (c) Comparator trip probability (d) Comparator output noise

overall procedure was repeated for all 256 states of $D_0 - D_7$.

An example of these probability distributions is shown in Figure 5-1(c). The point on each curve where the probability is 0.5 is the voltage at which the comparator trips for a given setting of $D_0 - D_7$. By fitting each curve to a Gaussian error function, the mean and variance for each distribution was obtained. The means as a function of the DAC code was used to construct the DAC transfer function and obtain the DNL and INL. The Gaussian curve fitting also obtained the variance, which is shown in Figure 5-1(d) as the RMS noise at the output of the comparator.

5.2 Current-Sensor Circuit Amplifier

The current-sensor circuit of Figure 4-13 contains an amplifier with feedback. The schematic of that amplifier is given in Figure 5-2. The amplifier is a single stage, wide output swing operational transconductance amlifier (OTA).

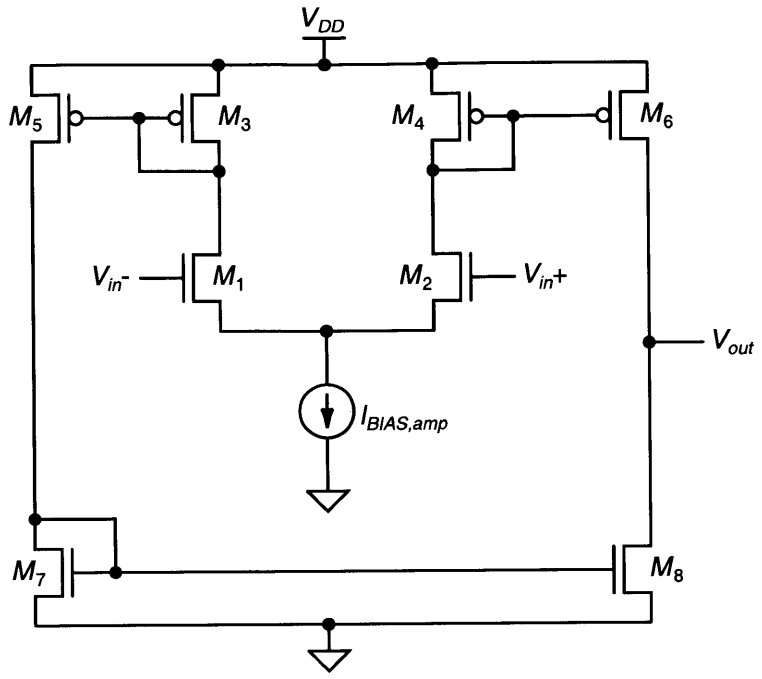


Figure 5-2: Single-Stage, wide output swing OTA used as the current sensor amplifier.

5.3 Active Charge Balancing with Post-Stimulation Correction Pulses

The adiabatic electrode stimulator attempts to maintain charge balance by bringing the electrode voltage back to its resting potential V_{mid} at the end of the stimulation. This method works so long as the faradaic pathway in the electrode is not activated. If the voltage across the capacitive portion of the electrode is kept within the "water window," the faradaic pathway is assumed to be in activated. Thus, any net charge delivered to the electrode should still be stored inside the electrode's C_{dl}. Applying a short across the electrode should eliminate that excess charge.

An alternative option is to actively maintain the electrode at its resting potential. Post stimulation, any residual charge on C_{dl} will bleed out naturally and cause V_{elec} at the output of the dynamic power supply to drift away from V_{mid}. Thus, it is possible to use the dynamic power supply to monitor V_{elec} at intervals and apply correction pulses to move V_{elec} back towards V_{mid} as it drifts to residual charge on C_{dl} bleeding. In fact, we did implement this strategy in our stimulator. In Figure 4-20, additional correction pulses in the electrode voltage and current are visible during the the time interval from 2-3 ms, that is, the millisecond immediately following the stimulation. This correction pulses help ensure charge balance and also enhance energy recovery, if that energy would normally dissipated due to electrode shorting. After the correction pulses phase, conventional electrode shorting was used to hold the electrode at V_{mid} until the next stimulation pulse.

5.4 Performance of Stimulator with Electrode in Saline

The measurements in Chapter 4 were presented for a model electrode composed of a series resistor and capacitor. This allowed us to vary the impedance of the electrode while showing that the feedback current control and monitoring would adapt to the changing electrode impedance or variation in current setting. Figure 5-3 shows acquired data for an electrode in saline. Because it is not possible to know directly the values of R_s and C_{dl} for a real electrode, the corresponding values of α_R and α_C were not calculated. As a result, there was no attempt to match these experimental results with the theory presented in Section 4.5. However, despite this limitation, it is still possible to measure EF_{CS} by measuring the average current through the electrode and therefore know the amount of energy a constant current source stimulator would require.

Figure 5-3(a,d) show the voltage of the power supply capacitor C_{in} during anodic stimulation (a) and cathodic stimulation (d). The energy consumed by the adiabatic neural stimulator was calculated based on the initial and final values of the voltage of C_{in} and the value of its capacitance (4.53 μF) to find the total change in energy.

Figure 5-3(b,e) shows the current through the electrode for anodic and cathodic stimulations respectively. In panels (c,f), we observe the electrode voltage for anodic and cathodic stimulations respectively. In all cases the blue curves correspond to a current control voltage $|V_{cur} - V_{ref}|$ of 200 mV while the green curve corresponds to a current control voltage of 300 mV. Thus, these sets of curves reveal that the stimulation current for a particular electrode can be controlled.

Table 5.1 shows the measured values of EF_{CS} for the electrode in saline. Note that at higher levels of current the efficiency of the adiabatic stimulator relative to a current source falls because the larger electrode voltage results in greater energy dissipation in the resistive component of the electrode.

Table 5.1: Measured EF_{CS} for Electrode in Saline

Direction	$\|V_{cur} - V_{ref}\|$	EF_{CS}
Anodic	200 mV	0.43
Cathodic	200 mV	0.36
Anodic	300 mV	0.52
Cathodic	300 mV	0.47

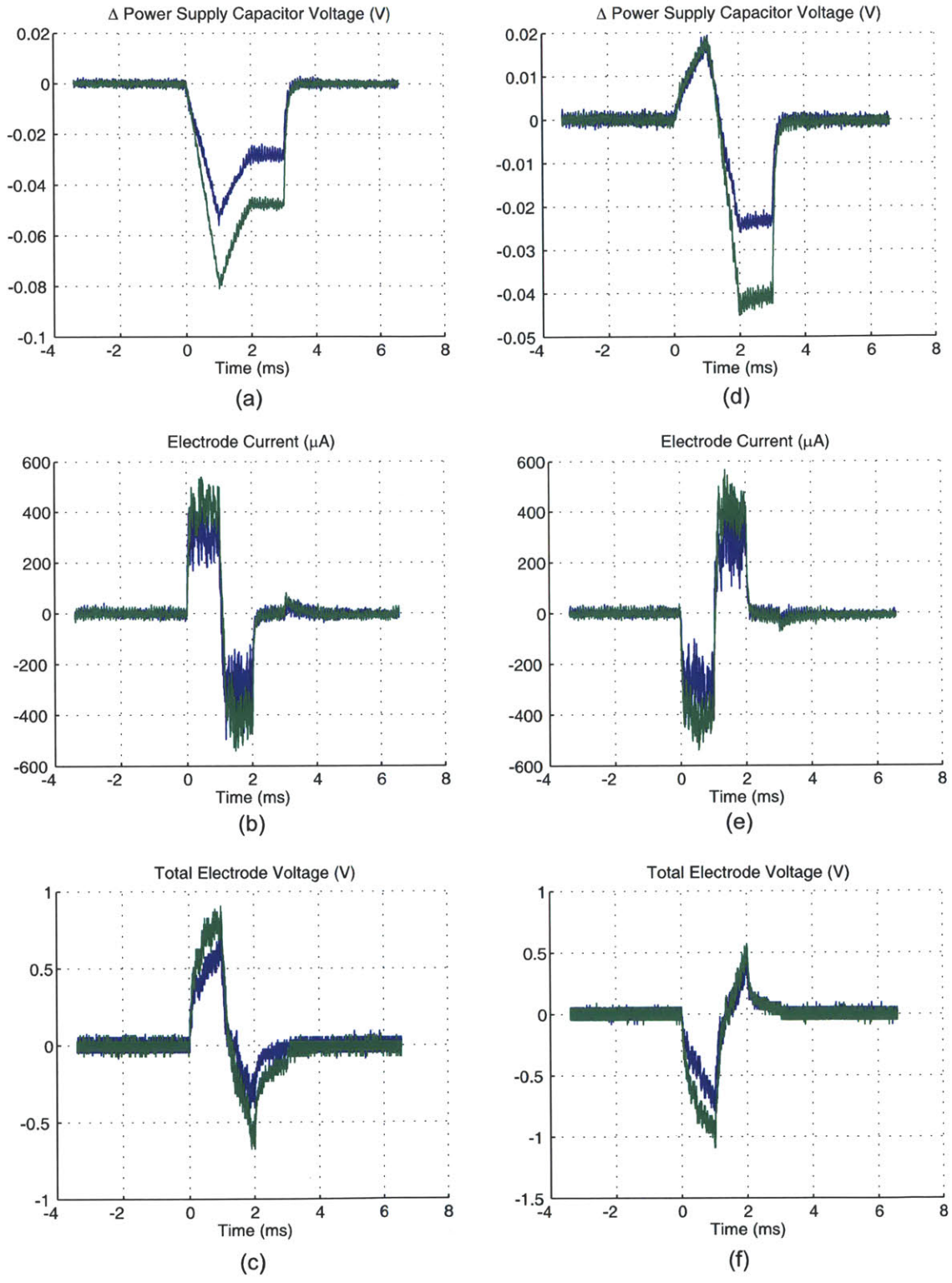


Figure 5-3: Measurements of electrode in saline. (a,d) Power Supply Capacitor Voltage (C_{in}), (b,e) Electrode Current (c,f) Electrode Voltage. (a-c) Anodic stimulation. (d-f) Cathodic stimulation. Blue Curves: $|V_{cur} - V_{ref}|$ = 200 mV. Green Curves: $|V_{cur} - V_{ref}|$ = 300 mV.

Chapter 6

Conclusions and Future Work

6.1 Wireless Neural Stimulator

In this thesis, I have a presented a complete wireless neural stimulator for use in freely behaving small animals. The device uses a miniature printed circuit board and integrated circuit to deliver biphasic current pulses to 4 addressable bipolar electrodes at 32 selectable current levels. The chip enters a sleep mode when not needed and can be woken up remotely when required, thereby reducing standby power consumption by approximately 2.5x. We demonstrated its ability to effectively modulate a neural circuit and its associated behavior in an untethered, freely behaving zebra finch.

The addition of this wireless stimulation device to the field of neuroscience opens up greater possibilities for behavioral experiments. For example, experiments that involve an animal passing freely through small openings, such as a boundary between a light and dark area, or between sections of a maze, only become possible with a wireless system. Experiments where multiple freely behaving animals interact naturally are only feasible with a wireless system because any tethers would become entangled. Wireless neural stimulation systems are also important for the clinical treatment of neurological disorders, where stimulation applications are ubiquitous and ever-increasing, ranging from prostheses for hearing and vision to the treatment of Parkinson's disease and chronic pain.

The stimulator chip could be further improved in a fundamental way. First of all, the sensitivity of the receiver could be improved by increasing the amount of gain on the receiver. Presently, the sensitivity of the wireless receiver is limited by the dead zone of the peak detector circuit and not the thermal noise of the preamplifier. While some dead zone to reject noise is desirable, the output thermal noise of the receiver preamplifier, post gain, is still significantly smaller than the dead zone. The dead zone of the peak detector is approximately ϕ_t/κ, or about 35 mV, while the output referred

noise of the preamplifier is approximately 1 mV. The current preamplifier gain of approximately 10 could be easily increased by another factor 10 at the expense of additional standby power from greater amplifier bias current. Since the wireless neural stimulator circuit was ultimately limited by standby power consumption in the zebra finch truncated-song application, the decision to increase receiver sensitivity and standby power would need to be made on a case-by-case basis.

Other improvements to the wireless neural stimulator circuit include the ability to wirelessly power and/or recharge the device via rectifier or other energy harvesting method. This would serve to increase the lifetime of the device per initial charge, or further lighten the device by reducing the amount of battery required by the stimulator. Still, other improvements to the stimulator include adding a greater number of channels, ability to modulate the duration of the stimulation pulse width, and also ability to simultaneous record and stimulate with wireless telemetry of neural recordings. Such a dual recording/stimulation system would be highly valuable to experimental neuroscience. Further, the recording and stimulation circuitry could also be synchronized in order to suppress the stimulation artifacts that can saturate and temporarily disable AC coupled neural recording amplifiers.

6.2 Adiabatic Electrode Stimulator with Feedback Current Regulation

I have reported the first integrated adiabatic electrode stimulator with simultaneous control of electrode voltage and current. In addition to offering the efficiency of voltage stimulation and the safety and precision of current stimulation, this stimulator is also capable of inductively recycling electrode energy while generating a continuum of electrode voltages. This is in contrast to earlier attempts at adiabatic electrode drivers which relied on switched capacitor banks offering just a limited, discrete number of voltage steps and no current regulation, or simple current regulation based on current limiters rather than true adiabatic electrode drives.

I have also reported in this thesis a quantification of theoretical stimulator efficiency for a given electrode impedance, magnitude of stimulation, and DC power supply voltage. The performance of the stimulator presented in this thesis matches theory well, achieving 2x-3x reductions in stimulator energy as compared to a conventional stimulator based on constant current sources. The adiabatic stimulator utilizes a dynamic power supply, the core efficiency of which limits the stimulator's overall energy efficiency. In this work, the average core efficiency was about 80%. If that were improved to 90%, stimulators that are 2.5x-5x more efficient than current sources may become reality.

One limitation of the adiabatic electrode stimulator in its present version is voltage compliance. Transistors in integrated circuits have low breakdown voltages, especially between the gate and source and gate and drain terminals, and also to a lesser extent between the drain and source terminals, especially if special transistors modified for high voltage are available. In the case of the adiabatic electrode stimulator, the power supply voltage must be limited to about 3.3 V, the breakdown voltage of the standard transistors in the AMI/ON 0.35 μm process. This results in stimulator output voltages being unable to exceed 3.3 V. While this is good enough for many stimulator applications, cochlear implants in particular often require power supplies of 10-15 V. To meet these requirements, it would be necessary to redesign the stimulator circuits to work at these higher voltages, making use of high voltage transistors where needed.

It should be noted that one advantage of the adiabatic stimulator is that performance does not suffer adversely from higher supply voltages. Whereas conventional current source stimulators must set their power supply rails for the worst case electrode, thereby burning the same amount of worse-case energy per stimulation regardless of electrode impedance, the adiabatic electrode stimulator burns only what energy is necessary. In a given distribution of electrodes, some electrodes will show higher impedances than others, or require more current than others to achieve the desired outcome. Although even in the adiabatic stimulator the overall power supply rails are still set for the worst case, the adiabatic stimulator conserves energy on electrodes performing well at lower currents or with less than the worst-case impedance.

Another limitation of the adiabatic electrode stimulator is that the prototype design contains only one channel. Clearly, more channels are necessary for practical devices, and the number of off-chip components may become cumbersome. However, the requirement of one external capacitor per simultaneous channel is not severe due to the availability of extremely tiny surface mount devices. Microwound inductors are also available in miniature surface mount devices, but the requirement of one inductor per simultaneous channel does not scale well. However, because the inductor is operated in discontinuous conduction mode with the inductor current beginning and ending at 0 A with each cycle, it may be possible to share a single inductor across multiple channels. Nevertheless, the adiabatic electrode stimulator presented in this thesis compares favorably with other designs based upon banks of switched capacitors, as a large number of capacitors are required per simultaneous channel in capacitor-bank stimulators, but not the stimulator described in this thesis. For non-simultaneous electrode channels, the same electrode circuitry and off-chip passive devices can be reused via a multiplexer network.

The presence of a magnetic core inductor in the adiabatic electrode stimulator also poses a problem for MRI scans, but this problem is easily remedied by allowing the inductor to be removed for the scan and replaced afterward via a simple surgery. Cochlear implants, which generally have two magnetically aligned components – an external microphone and sound processor unit, and an internal stimulator unit – must also have their alignment magnets removed prior to MRI scans.

The great energy savings offered by the adiabatic stimulation and inductive energy recycling techniques described in this thesis, and the outstanding energy savings that are possible with improvements, make this stimulator an excellent choice for implantable medical device systems that require long battery lifetime or benefit from reduced battery or coil size, cost, tissue heating, and increased patient comfort.

Appendix A

Low Power $G_m - C$ Filters

A.1 Introduction to $G_m - C$ Filters

There are many different types of active electronic filters. Some major classes of filters are RLC ladder filters, opamp-RC filters, switched-capacitor filters, and $G_m - C$ filters. Active filters are often preferred at low to moderate frequencies because of their electronic tunability, isolation, and ability to provide gain.

In conventional filter design, realizing the desired transfer function may be the designer's top priority. However, transfer function is only one measure of a filter's performance. Other important characteristics are the noise and dynamic range of the filter, its linearity, power consumption, and if it is an integrated design, its area. If it is a discrete design, the number and cost of components is of concern.

Power consumption has become of significant importance in recent times with the emergence of portable electronic devices for consumers and other battery operated medical devices such as cochlear implants. Cochlear implants require low power operation out of concern for cost, convenience, and also safety. Fully implanted systems must rely on a limited number of wireless recharge cycles over the patient's lifetime. If the battery is made larger to accommodate a higher power requirement, equipment costs rise. If the battery fails and needs replacement, additional surgery will be necessary, exposing the patient to risk and excessive cost.

$G_m - C$ filters are inherently low power because there is a minimal gain-bandwidth requirement on the components of the filter. In a $G_m - C$ filter, the required bandwidth of any given transconductor is only related to the pole frequency that transconductor helps set. In contrast, an opamp-RC filter must have sufficient gain-bandwidth in order to maintain the virtual ground condition at its inputs over

a wide range of frequencies, including frequencies well beyond the particular pole frequencies of the filter. This in turns results in a large power dissipation compared to a $G_m - C$ filter operating at the same frequency. A similar argument applies to switched-capacitor filters, as they often also employ operational amplifiers. The opamps in switched-capacitor usually have stringent requirements on settling time, which is often specified such as to permit clock frequencies many times the upper frequency limit of the filter. This also demands a high power consumption.

What opamp based filters lose in terms of power they gain back, somewhat, in terms of linearity. Opamp linearity is generally excellent as long as virtual ground is maintained at the input. Linearity in an opamp based filter is often limited by the output swing and in turn the power supply. $G_m - C$ filters do not rely on feedback for linearity. The feedback around individual transconductors in a $G_m - C$ filter is only present at low frequencies and vanishes as the input frequency moves well past the pole frequency related to that particular transconductor. For this reason, output swing is often not a limiting factor in linearity, but the input swing is. Various techniques for transconductor linearization have been proposed in the literature. Distortion performance in a $G_m - C$ filter is therefore often dominated by weak nonlinearities in the V-I transfer characteristic of the constituent transconductors (Sotiriadis et al., 2007).

Applications for ultra low power analog filters include bionic ear processor front ends. Bionic ears generally require 80 dB of sensing dynamic range (30 - 110 dB SPL), compressing to 60 dB internal dynamic range. Shrinking supply voltages mean that the amount of signal swing available for analog filtering is ever decreasing. Designers must pay attention to more than ever the dynamic range that can be achieved with their design.

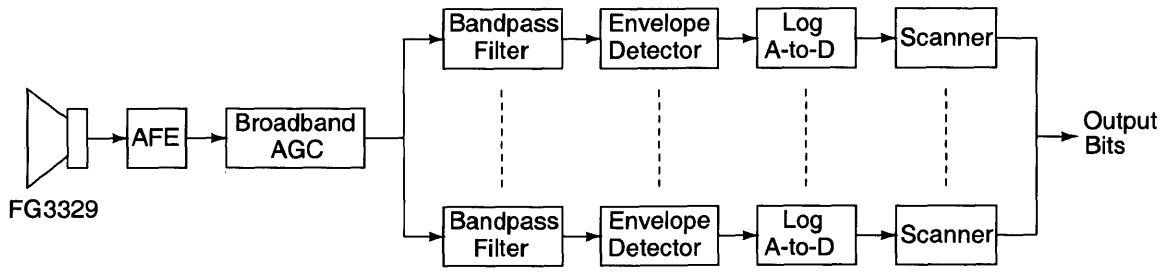


Figure A-1: Architecture of the analog bionic ear processor.

A.2 An Analog Bionic Ear Processor – A filtering Application

Speech recognition and cochlear implant systems often use a bank of bandpass filters to detect the level of sound energy in each of some 8-20 frequency bands. The filters are either linearly or logarithmically spaced, or some combination of the two, such as the mel scale, which is designed to map frequencies onto a "perceptually linear" scale (Picone, 1993). Filter banks based on the mel scale use linearly spaced filter center frequencies up to 1 kHz and logarithmically spaced center frequencies above 1 kHz. A logarithmic measure of the spectral energy in each filter bank channel is used for further processing. In cochlear implant systems, unwanted interactions between stimulations electrodes limit the number of electrodes to approximately 8-20.

Figure A-1 shows the overall architecture of an analog bionic ear processor (Sarpeshkar et al., 2005). Sound is collected by a microphone (Knowles FG3329), amplified by a specialized analog front end (AFE) with wide dynamic range andn excellent power supply rejection (Baker and Sarpeshkar, 2003). A broadband automatic gain control (AGC) compresses the incoming signal with approximately 80 dB dynamic range into 60 dB internal dynamic range for processing (Baker and Sarpeshkar, 2006). Once compressed, the signal is fed to a bank of 16 channels consisting of a bandpass filter (Salthouse and Sarpeshkar, 2003), envelope detector (Zhak et al., 2003), and logarithmic A-to-D (Sit and Sarpeshkar, 2004) to detect the amount of energy in each of 16 bands. The output of each channel is used to set the correct stimulation level for the electrode corresponding to each channel. The center frequency of each filter, its bandwidth, and the stimulation parameters are a matter of preference determined through trial-and-error for each individual cochlear implant patient.

Low-power filtering has many potential biomedical applications. The one we are focusing on here in great detail is a bionic ear processor, where high-Q bandpass filters are needed to isolate frequency information. However, other biomedical or neural prosthetic applications include filtering for heart sounds, electrocardiograms (EKG), electroencephalograms (EEG), and filtering of neural recordings to obtain either single units or local field potential (LFP) activity.

The 16 bandpass filters used in the bionic ear processor are critical components. At 60 dB internal dynamic range and adjustable quality factors, typically about 4 but perhaps as high as 6, they perform a significant computation task. To build a low-power system, all components must be low power with no single component dominating the power consumption. For implantable devices, low power is a critical requirement. An oft cited argument is that low power leads to lower medical costs because a

low power device needs a correspondingly small battery leading to lower overall implant size, easier and less costly surgery, and fewer complications resulting from surgery. Follow-up surgeries, such as battery replacements, if necessary, also become easier and less expensive. The dream of realizing a fully-implantable cochlear implant system where there is no patient-external unit is only possible with ultra low-power design. On sufficiently small power consumption, everything including the microphone, preamplifiers, filtering, and stimulation circuitry can all be fully implanted into a patient such that it would be virtually imperceptible that a patient was using a cochlear implant.

A.3 Filter Design Approaches

Conventional approaches for designing filters include two primary techniques. In this chapter, we will consider both approaches.

- **State-Space**: The designer selects a desired transfer function, and then performs a series of algebraic manipulations to discover convenient implementations. Usually, reducing the transfer function into integrator form is most convenient for efficient filter implementation. This method will work for both opamp-RC filters as well as $G_m - C$ filters.
- **Element Replacement**: The designer selects a passive topology from a filter design book, and then replaces elements with their active equivalents. For example, capacitors remain unchanged, but inductors are replaced by gyrated capacitors. In $G_m - C$ filters, gyrators have simple, convenient implementations.

A.4 Bandpass Filters

Throughout this chapter, we will consider several types of $G_m - C$ bandpass filters. Although lowpass filters are also of great interest, the concepts and techniques presented here can be extended to lowpass filters as well.

A.4.1 Introduction

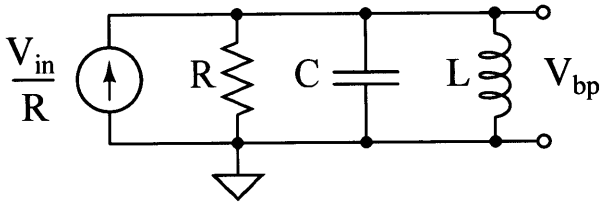
This section reviews various topologies for CMOS $G_m - C$ bandpass filters. Power, center frequency, filter order, dynamic range, and quality factor are all important bandpass filter specifications.

In Section A.4.2 we discuss a low-Q and a high-Q variation of a standard bandpass filter structure. In Section A.8, we review capacitive attenuation as a transconductor linear range extension technique.

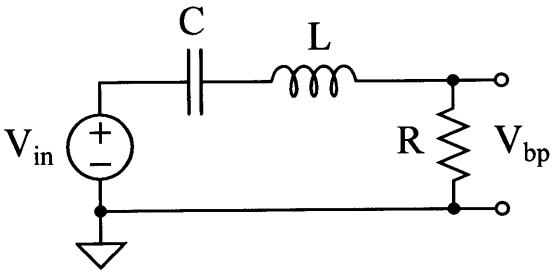
In Section A.5, we consider $G_m - C$ filters synthesized by transformation from prototype ladder filters.

A.4.2 Passive Bandpass Filter Structures

Figure A-2 shows two prototype RLC bandpass filters. The first version, shown in Figure A-2(a), is a parallel resonator. When driven with a current source, the parallel resonator becomes a high impedance at the resonant frequency and a low impedance at frequencies far from the resonance, thus producing a bandpass voltage response. The second version, shown in Figure A-2(b), uses a series resonator driven by a voltage source. The output of the filter is the voltage taken across the resistor. Near the resonant frequency, the series tank looks short and a large current flows through the resistor, developing the output voltage. At other frequencies far from the resonance, the output looks grounded. The parallel version is particularly suitable for transformation to an integrated implementation because all circuit components are grounded. The series resonator can also be implemented in integrated form, but is less flexible than the parallel version and requires some floating components.



(a) Prototype parallel RLC bandpass filter.



(b) Prototype series RLC bandpass filter.

Figure A-2: Prototype RLC bandpass filters.

We can write the transfer function for each the parallel and series resonators. For the parallel resonator in Figure A-2(a), we obtain the transfer function in Equation A.1. For the parallel resonator in Figure A-2(b), we obtain the transfer function in Equation A.2.

$$\frac{V_{bp}}{v_{in}} = \frac{\frac{sL}{R}}{s^2LC + \frac{sL}{R} + 1} \tag{A.1}$$

$$\frac{V_{bp}}{v_{in}} = \frac{sRC}{s^2LC + sRC + 1} \tag{A.2}$$

These transfer functions resemble the canonical second order bandpass transfer function, $H(s)$.

$$H(s) = \frac{\frac{\tau s}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.3}$$

The following relations apply:

$$\begin{aligned} \tau &= \sqrt{LC} \\ Q_{par} &= R/\sqrt{\frac{L}{C}} \\ Q_{ser} &= \sqrt{\frac{L}{C}}/R \end{aligned}$$

The time constant, τ, is the same for both the parallel and series filters. However, the quality factor, denoted Q_{par} and Q_{ser}, is defined differently.

A.4.3 Fundamental Noise Limit of a Bandpass Filter

Figure A-2(a) shows a prototype RLC bandpass filter. This filter achieves the highest dynamic range possible of any 2nd order bandpass filter design for a given power supply voltage. As we will show shortly, the noise of the filter is *independent* of the both the center-frequency and Q of the filter.

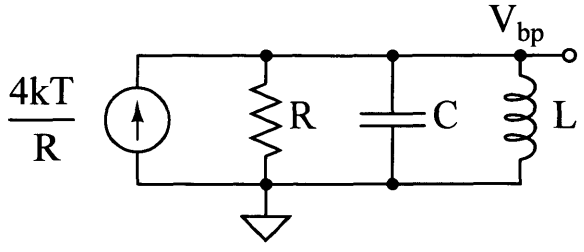


Figure A-3: Parallel RLC bandpass filter showing noise sources.

To calculate the noise of this filter, we replace the input to the filter with the resistor's noise current, $\overline{i_n^2} = \frac{4kT}{R}$. Referring to any input current as i_{in}, we can calculate the filter's impedance

transfer function:

$$\frac{V_{bp}}{i_{in}} = \frac{sL}{s^2LC + \frac{sL}{R} + 1} = \frac{\frac{\tau sR}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.4}$$

We can find the output noise of the filter, $\overline{v_{no}{}^2}$, by solving the following integral:

$$\overline{v_{no}{}^2} = \int_0^\infty \overline{i_n{}^2} \cdot \left| \frac{V_{bp}}{i_{in}} \right|^2 df \tag{A.5}$$

It is convenient to make the following substitutions before proceeding with integrating the noise transfer function (Sarpeshkar, 1997):

$$\begin{aligned} s &= j\omega \\ \omega &= 2\pi f \\ x &= \omega\tau \end{aligned}$$

The last substitution allows us to work in normalized frequency units which is convenient for solving the noise integral. The filter transfer function in normalized units is:

$$H(x) = \frac{\frac{jxR}{Q}}{1 - x^2 + \frac{jx}{Q}} \tag{A.6}$$

The integral of the $|H(x)|^2$ over all x is:

$$\int_0^\infty |H(x)|^2 \, dx = \frac{\pi R^2}{2Q} \tag{A.7}$$

We can now rewrite the noise integral in Equation A.5 as:

$$\begin{aligned} \overline{v_{no}{}^2} &= \frac{1}{2\pi\tau} \frac{4kT}{R} \int_0^\infty |H(x)|^2 \, dx \\ &= \frac{1}{2\pi\tau} \frac{4kT}{R} \frac{\pi R^2}{2Q} \\ &= \frac{kTR}{\tau Q} \qquad \text{(A.8)} \\ &= \frac{kT}{C} \qquad \text{(A.9)} \end{aligned}$$

We see that the total integrated noise power spectral density of any bandpass filter built using the topology in Figure A-2(a), for any choice of L, R, and C, depends only on C. Although this result may sound counterintuitive at first, it actually repeats the result for the noice of an RC lowpass filter. For any RC lowpass filter, one also obtains $\frac{kT}{C}$ for the total integrated noise, independent of R. The reason is the RC product sets the bandwidth of the filter, but the R alone sets the noise power spectral density, equal to $4kTR$ in V^2/Hz. If one increases R, the PSD increases, but the bandwidth decreases by the same fraction, keeping the total integrated noise constant. Likewise, if one decreases R, the noise PSD decreases, but is countered by rising bandwidth. A similar explanation applies to the bandpass filter. Another way of looking at the noise of the bandpass filter is to observe that the filter's bandwidth, $BW \equiv \frac{1}{\tau Q}$. Hence, the noise of the filter can be viewed in voltage squared units as $kTR \cdot BW$ (see Equation A.8). By the definitions for τ and Q, we see that changing L has no effect on the bandwidth, since L affects τ and Q in opposite ways. We also see that changing R affects Q but not τ. Hence, the bandwidth is inversely proportional to R, canceling out the R in Equation A.8. However, changing C inversely affects the filter bandwidth. The result is Equation A.9, independent of R and L.

We can now calculate the dynamic range of this bandpass filter. Let us assume a power supply voltage of 1.5 V. If the maximum swing on the capacitor is equal to the supply voltage, then the upper limit to our dynamic range is 530 mV_{rms}. At the lower limit, the noise voltage is $\sqrt{\frac{kT}{C}}$. If we design for a filter center frequency of 1 kHz, and we choose a 100 μH inductor, then we require a 253 μF capacitor. The noise voltage is therefore 4 nV_{rms}. The overall dynamic range of this filter is 162 dB. This represents the best that one can do. Of course, such inductor and capacitor values are prohibitively large if we are to build large, higher order filter banks using this topology. For this reason, we turn to integrated circuits, knowing well that we cannot achieve anywhere near the dynamic range of the purely passive filter. However, such a wide dynamic range is usually not necessary. Nonetheless, we are concerned with dynamic range because good filter design is usually required to achieve even a modest dynamic range of 60 dB in integrated topologies using reasonable capacitor sizes.

If we want to integrate this filter using the topology shown in Figure A-2(a), we may be limited to capacitor values of 10 pF per capacitor. Suppose that we could implement the necessary inductor by *noiselessly* gyrating a capacitance into an inductance. This is, of course, not possible, but we are making this assumption to try to recalculate a fundamental limit for integrated circuits. We must also assume that the resistance which sets the Q is implemented using a real resistor, or is

implemented actively in a way that does not contribute more noise than the equivalent real resistor.[1] If we again assume a single 1.5 V supply is available and rail-to-rail voltage swings are possible, the theoretically best possible dynamic range is reduced to 88 dB. This is indeed an excellent number for a continuous-time integrated filter, but probably not achievable in practice since this includes just the minimum noise source necessary – the noise from the resistor that sets the Q. In an integrated active filter, it will likely be necessary to set that resistance with an active element that may contribute more than 1 device's worth of noise, and the inductor implemented with a gyrated capacitor will also contribute excess noise.

A.5 Parallel-type $G_m - C$ Bandpass Filters

The $G_m - C$ bandpass filter based upon the parallel RLC ladder filter can be easily realized using either the state-space or element replacement techniques.

A.5.1 Filter Synthesis by State-Space Equations

A method for synthesizing filters, including $G_m - C$ filters, is to use state-space equations. For example, to design a bandpass filter from state-space, one begins with the canonical state-space form of the bandpass filter. The objective is then to manipulate the equation so that it consists only of adders, scalers, and integrators. The state-space equation based upon these operations only can be represented by a feedback block diagram and readily realized as an active filter. The algebraic manipulations required for the state-space realization are shown below, beginning with the canonical form of the bandpass filter in Equation A.10 and ending with the integrator format in Equation A.15.

[1] For a 1 kHz center frequency and Q of 4, if C = 10 pF, L = 2533 H and R = 64 MΩ.

$$\frac{V_{bp}}{V_{in}} = \frac{\frac{\tau s}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.10}$$

$$\left(\tau^2 s^2 + \frac{\tau s}{Q} + 1\right) V_{bp} = V_{in}\frac{\tau s}{Q} \tag{A.11}$$

$$\tau s\left(\tau s + \frac{1}{Q}\right) V_{bp} = V_{in}\frac{\tau s}{Q} - V_{bp} \tag{A.12}$$

$$\left(\tau s + \frac{1}{Q}\right) V_{bp} = \frac{V_{in}}{Q} - \frac{1}{\tau s}V_{bp} \tag{A.13}$$

$$\tau s V_{bp} = \frac{V_{in}}{Q} - \frac{1}{\tau s}V_{bp} - \frac{1}{Q}V_{bp} \tag{A.14}$$

$$V_{bp} = \frac{1}{\tau s}\left(\frac{1}{Q}(V_{in} - V_{bp}) - \frac{1}{\tau s}V_{bp}\right) \tag{A.15}$$

Once we have an integrator state-space representation, it is relatively straightforward to translate that into a block diagram, shown in Figure A-4. From the block diagram, we can create either an opamp-RC implementation (Figure A-5) or a $G_m - C$ implementation(Figure A-6 by inspection. The opamp-RC implementation is also known as the Tow-Thomas biquad. It also turns out there is a lowpass output available with the following transfer function:

$$V_{lp} = V_{bp} \cdot \frac{1}{\tau s} = \frac{\frac{1}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1}$$

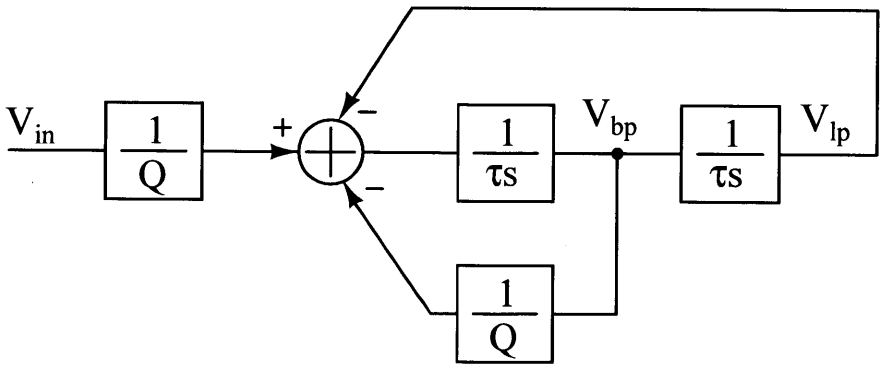


Figure A-4: Block diagram of the bandpass filter.

Figure A-6 shows a $G_m - C$ implementation of the RLC ladder filter of Figure A-2(a). The current source has been replaced with G_{m1} and the resistor with G_{m4}. The capacitor C, now called C_1, is unchanged. The inductor, L, is implemented by gyrating C_2.

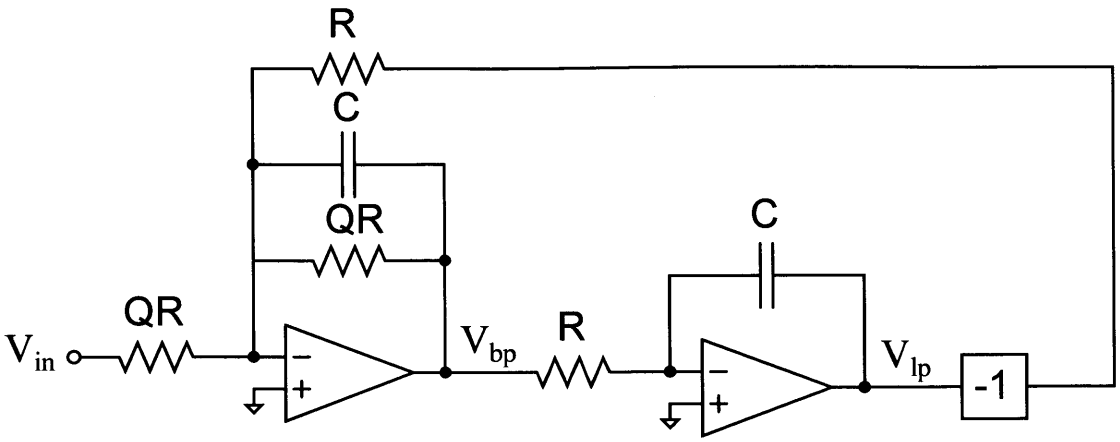


Figure A-5: Generic opamp-RC implementation of the bandpass filter (Tow-Thomas Biquad).

$$\frac{V_{bp}}{V_{in}} = \frac{G_{m1}}{G_{m4}} \left(\frac{\frac{G_{m4}C_2}{G_{m2}G_{m3}} s}{\frac{C_1C_2}{G_{m2}G_{m3}} s^2 + \frac{G_{m4}C_2}{G_{m2}G_{m3}} s + 1} \right) \tag{A.16}$$

The transfer function of the filter is given by Equation A.32. This transfer function can be rewritten in the canonical form of Equation A.3, multiplied by the scaling factor A_{ω_0}. Expressions for A_{ω_0}, τ, and Q are given below:

$$\begin{aligned} A_{\omega_0} &= \frac{G_{m1}}{G_{m4}} \\ \tau &= \sqrt{\frac{C_1C_2}{G_{m2}G_{m3}}} \\ Q &= \sqrt{\frac{C_1}{C_2}} \frac{\sqrt{G_{m2}G_{m3}}}{G_{m4}} \end{aligned}$$

Ordinarily, we choose $C_1 = C_2 = C$, $G_{m2} = G_{m3} = G_\tau$, and $G_{m1} = G_{m4} = \frac{G_\tau}{Q}$. This makes the filter τ and Q very easy to set and also sets the center frequency gain to 1. Reduced expressions for τ and Q are given below.

$$\begin{aligned} \tau &= \frac{C}{G_\tau} \\ Q &= \frac{G_\tau}{G_{m4}} \\ \Longrightarrow G_{m4} &= \frac{G_\tau}{Q} \end{aligned}$$

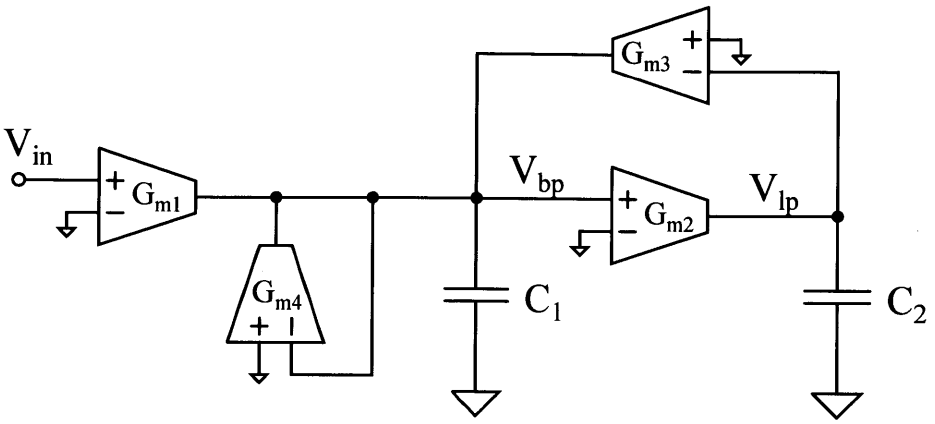


Figure A-6: Parallel-type bandpass filter using four transconductors. The first two transconductors simulate the current source and resistance in Figure A-2(a). The remaining two transconductors gyrate a C into an L.

A.5.2 Filter Synthesis by Element Replacement

An alternative method for synthesizing $G_m - C$ bandpass filters is to begin the design process with prototype RLC ladder filters and replace troublesome elements with active components (Schaumann and Valkenburg, 2001). For example, the next step in the design process is to replace current sources and resistors with transconductors and inductors with gyrated capacitors. Capacitors remain capacitors. After the transformation, the inductors and resistors become electronically controllable through setting of transconductances.

Gyrators

The gyrator is a critical element to building large simulated inductances on chip. Figure A-7 shows a gyrator implemented using two transconductors. This implementation is a simple and compact way to realize an inverse impedance. We find that the input impedance of the gyrator is:

$$Z_{in} = \frac{1}{G_{m1}G_{m2}Z_L} \tag{A.17}$$

If Z_L is a capacitor with an impedance equal to $\frac{1}{sC}$, then the gyrator simulates an inductance of $L = \frac{C}{G_{m1}G_{m2}}$.

It can be seen easily that our prototype parallel RLC bandpass filter of Figure A-2(a) maps directly to the active version with 4 transconductors (Figure A-6). The input current source becomes G_{m1}, the resistor G_{m4}, C_1 remains unchanged, and G_{m2} and G_{m3} gyrate C_2 into an equivalent

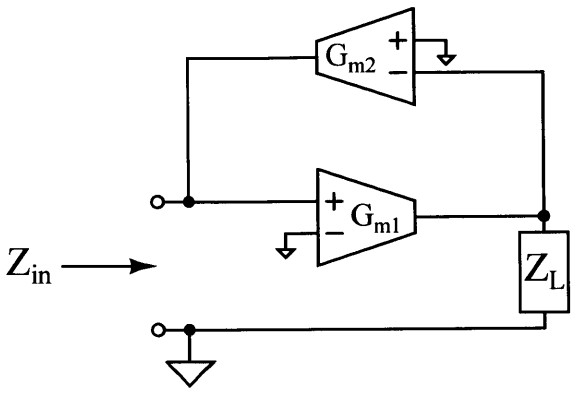


Figure A-7: Gyrator using two transconductors.

inductance.

A.5.3 Noise and Dynamic Range Analysis

Figure A-8 shows a feedback block diagram of the parallel-type $G_m - C$ bandpass filter. This diagram is useful for solving the filter's transfer function and calculating its noise. To help solve for the noise, we have added noise sources to the block diagram. The noise current $\overline{i_{n134}{}^2}$ represents the current noise due to transconductors G_{m1}, G_{m3} and G_{m4}. The noise current from G_{m2} adds to a different place in the block diagram, and is denoted by $\overline{i_{n2}{}^2}$.

To solve for the noise, we must first find the noise transfer function to the output for each of the two noise sources. By inspection, we can find the transfer function for $\overline{i_{n134}{}^2}$ to the output:

$$\frac{V_{bp}}{i_{n134}} = \frac{V_{bp}}{V_{in}G_{m1}} \tag{A.18}$$

To determine the noise PSD, $\overline{i_{n134}{}^2}$, we will assume that all transconductors operate in subthreshold at some bias current I_{bias}. Assuming the transconductors are made with differential pairs, then each transistor operates at some nominal bias current of $I_{bias}/2$. Therefore, the total shot noise current for each transconductor is $N2qI_{bias}/2$, where N is the effective number of noise devices. We can also define the linear range of each transconductor, $V_L = \frac{I_{bias}}{G_m}$. We can now rewrite the shot noise current for transconductors 1, 3, and 4 as:

$$\overline{i_{n134}{}^2} = NqV_L\left(G_{m1} + G_{m3} + G_{m4}\right) \tag{A.19}$$

To determine the total noise power at the output, we must solve the integral below:

$$\int_0^\infty \overline{i_{n134}{}^2} \left| \frac{V_{bp}}{V_{in} G_{m1}} \right|^2 df \tag{A.20}$$

After some calculus and algebra, we find the integrated noise power due to transconductors 1, 3, and 4 is:

$$\overline{v_{no134}{}^2} = \frac{NqV_L \left(1 + \frac{G_{m1}}{G_{m4}} + \frac{G_{m3}}{G_{m4}}\right)}{4C_1} \tag{A.21}$$

We must repeat a similar set of calculations for the noise of transconductor G_{m2}. The noise current PSD is $\overline{i_{n2}{}^2} = NqV_L G_{m2}$. We find that the transfer function from the noise current to the output is given in Equation A.22. Performing a similar integration as before to find the total output noise power due to G_{m2}, we obtain the result in Equation A.23.

$$\frac{V_{bp}}{i_{n2}} = \frac{1}{G_{m2}} \cdot \frac{1}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.22}$$

$$\overline{v_{no_2}{}^2} = \frac{NqV_L}{4C_2} \cdot \frac{G_{m3}}{G_{m4}} \tag{A.23}$$

The total integrated voltage squared noise of the filter is:

$$\overline{v_{no}{}^2} = \overline{v_{no134}{}^2} + \overline{v_{no_2}{}^2} = \frac{NqV_L}{4} \left(\frac{\left(1 + \frac{G_{m1}}{G_{m4}} + \frac{G_{m3}}{G_{m4}}\right)}{C_1} + \frac{\frac{G_{m3}}{G_{m4}}}{C_2} \right) \tag{A.24}$$

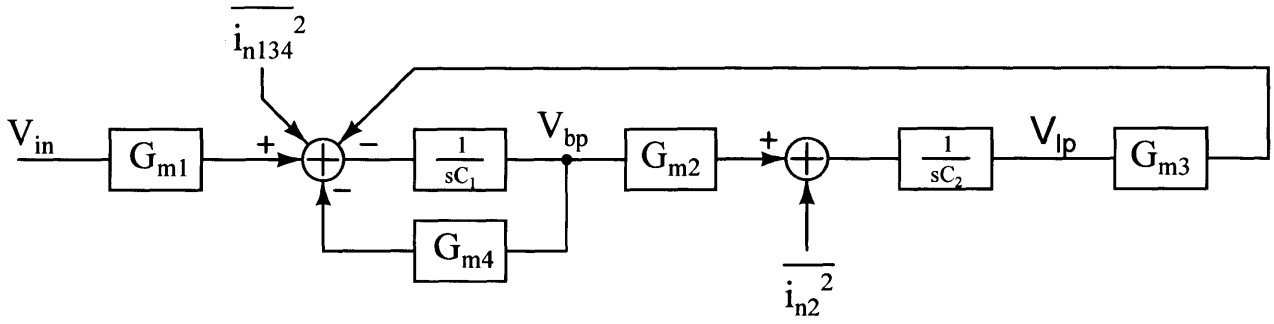


Figure A-8: Block diagram of the gyrator-based bandpass filter.

We can simplify the noise expression by substituting our typical choices for the filter parameters. As stated earlier, we choose $C_1 = C_2 = C$, $G_{m2} = G_{m3} = G_\tau$, and $G_{m1} = G_{m4} = \frac{G_\tau}{Q}$. The total

integrated output voltage noise power of the filter then becomes:

$$\overline{v_{no}^2} = \frac{NqV_L(2Q+2)}{4C} \approx \frac{NqV_LQ}{2C}, Q \gg 1 \tag{A.25}$$

Finally, to calculate dynamic range, we must also determine the largest signal that the filter can handle. We will start by checking the voltage transfer function from the input to each transconductor's differential voltage. Since each transconductor has one input at signal ground, this amounts to finding $\frac{V_1}{V_{in}}$, since $\frac{V_{bp}}{V_{in}}$ is already known.

$$\frac{V_{lp}}{V_{in}} = \frac{V_{bp}}{V_{in}} \cdot \frac{G_{m2}}{sC_2} = \frac{\frac{G_{m1}}{G_{m3}}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.26}$$

The maximum differential voltage magnitudes for each transconductor are given by, in normalized units with $|V_{in}| = 1$:

$$G_{m1} : |V_{in}|_{max} = 1 \tag{A.27}$$

$$G_{m2} : |V_{bp}|_{max} = \frac{G_{m1}}{G_{m4}} = 1 \tag{A.28}$$

$$G_{m3} : |-V_{lp}|_{max} = Q\frac{G_{m1}}{G_{m3}} = 1 \tag{A.29}$$

$$G_{m4} : |-V_{bp}|_{max} = \frac{G_{m1}}{G_{m4}} = 1 \tag{A.30}$$

Since we normally choose to operate with $\frac{G_{m3}}{G_{m1}} = Q$, the maximum swing on G_{m3} is equal to 1. Since all transconductors see a swing of 1 when the input is 1, the swing is optimized, since no one transconductor limits the performance of the circuit at the upper end of the dynamic range.

In a typical filter, one might choose $C_1 = C_2 = 10$ pF, $V_L = 1$ V, and $Q = 4$. A typical value for N might be 4. Under these conditions, the largest useable signal might be 530 mV_{rms}. Under these assumptions, our filter would have a dynamic range of 63 dB.

A.5.4 Alternative Biasing Schemes

The noise analysis was carried out assuming a standard bias arrangement where $G_{m2} = G_{m3} = G_\tau$, and $G_{m1} = G_{m4} = \frac{G_\tau}{Q}$. However, this is not the only biasing arrangement possible. In fact, any combination of G_{m2} and G_{m3} where the product of the two is held constant doesn't alter the filter's

Q, τ or A_{ω_0}. In fact, suppose we chose $G_{m1} = G_{m3} = G_{m4} = G_\tau/Q$ and $G_{m3} = G_\tau \times Q$.

The total integrated output voltage noise power of the filter then becomes:

$$\overline{v_{no}^2} = \frac{NqV_L}{C} \tag{A.31}$$

It appears that we have created a filter with less noise than the original design. The noise is also independent of Q, a property exhibited by the passive version of this filter. However, these improvements have come at a price. Power consumption has gone up, but that is a tradeoff we can accept as long as it is within reason. However, one must also look at the lowpass output of the filter. The bandpass output is clearly unaffected because its gain depends only on G_{m1}/G_{m4}, a ratio which we did not modify, and is still equal to 1. Hence the magnitude of the output never exceeds that of the input. The lowpass output, on the other hand, is specified by:

$$\frac{V_{lp}}{V_{in}} = \frac{G_{m1}}{G_{m3}} \left(\frac{1}{\frac{C_1 C_2}{G_{m2} G_{m3}} s^2 + \frac{G_{m4} C_2}{G_{m2} G_{m3}} s + 1} \right) \tag{A.32}$$

Under the standard biasing arrangement, the factor G_{m1}/G_{m3} is equal to $1/Q$. At low frequencies the output is smaller than the input by a factor of Q, but as the lowpass filter resonates, that factor is canceled out by a gain of Q, so as with the bandpass output, the lowpass output never exceeds the input. Under the new arrangement, the ratio $G_{m1}/G_{m3} = 1$, so when the lowpass filter resonates, its output magnitude reaches Q times the input. This behavior is a major disadvantage as it now limits the maximum input signal to $1/Q$ of the linear range of the transconductors. Although our noise power has gone down by roughly Q, our maximum signal power has gone down by Q^2, degrading our maximum SNR by a factor of Q as well as increasing our power consumptions. It seems that this tradeoff is never acceptable, except perhaps for low values of Q, or if the input signal is going to be small. For example, a filter than can electronically retune itself to lower its noise when appropriate can extend its dynamic range. We explore this possibility and other related possibilities in greater detail in the next chapter.

A.5.5 Modification with 3 transconductors

If one chooses $G_{m1} = G_{m4}$, it is possible to reduce the filter complexity from 4 transconductors to 3. Since each G_{m1} and G_{m4} have opposite unused input terminals and the same transconductance, we can combine their connections by eliminating G_{m4} and connecting G_{m1} in unity feedback as shown

in Figure A-9. The loading on V_{bp} is virtually unchanged by this modification.

The transfer function of the circuit in Figure A-9 is given by:

$$\frac{V_{bp}}{V_{in}} = \frac{\frac{G_{m1}C_2}{G_{m2}G_{m3}}s}{\frac{C_1C_2}{G_{m2}G_{m3}}s^2 + \frac{G_{m1}C_2}{G_{m2}G_{m3}}s + 1} \tag{A.33}$$

In canonical form, the filter's τ and Q are given by:

$$\begin{aligned} \tau &= \sqrt{\frac{C_1C_2}{G_{m2}G_{m3}}} \\ Q &= \frac{\sqrt{G_{m2}G_{m3}}}{G_{m1}} \end{aligned}$$

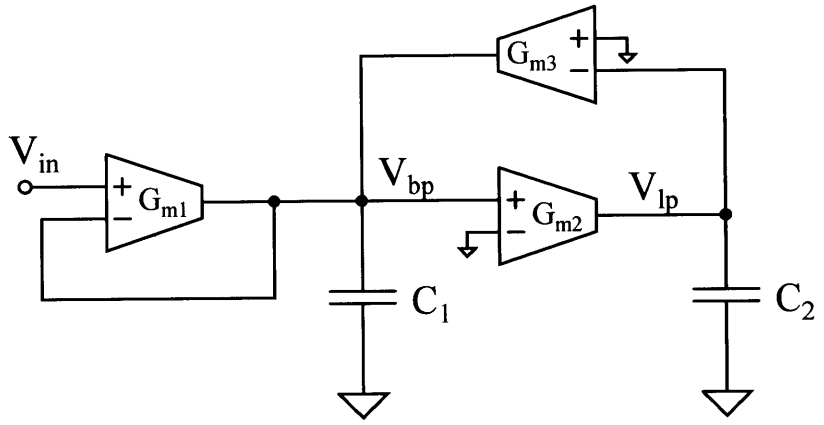


Figure A-9: Modification of the parallel-type $G_m - C$ bandpass filter with 3 transconductors..

Although possible in theory, this type of connection is not recommended in practice. Recall that the Q of the filter is controlled by G_{m4} and completely unaffected by G_{m1}. However, if the transconductors G_{m1} and G_{m4} are combined together, should G_{m1} be saturated by a large input, the transconductance will fall due to compressive nonlinearities and cause the Q of the filter and total harmonic distortion to increase. If G_{m1} and G_{m2} are kept separate, saturating G_{m1} with a large input will not also saturate G_{m4}, hence the Q does not vary significantly with input level. Although the 3 transconductor filter will have slightly less noise and consume slightly less power than the 4 transconductor version, its increased distortion makes this modification an unhelpful tradeoff.

A.6 Series-type $G_m - C$ Bandpass Filters

A.6.1 Filter Synthesis by Element Replacement

Like the parallel-type $G_m - C$ bandpass filter, it is also possible to build a series-type bandpass filter based on the series passive RLC topology of Figure A-2(b). Implementing this topology in $G_m - C$ may be tricky because it requires floating elements. However, the element replacement technique is straightforward. The floating capacitor at the input can remain as floating capacitors are usually available in standard mixed-signal integrated technologies. Once again, we can implement the inductor by gyrating another capacitor. However, implementing a floating inductor directly, while possible, is not necessary. Instead of gyrating a pure capacitance, we can add a resistance in parallel with the capacitance.

The impedance of a resistance and capacitance in parallel is $Z_L = \frac{R}{sRC+1}$. Referring to Equation A.17, we find that the gyrated impedance is:

$$Z_{in} = \frac{RCs+1}{G_{m1}G_{m2}R} = \frac{Cs}{G_{m1}G_{m2}} + \frac{1}{G_{m1}G_{m2}R} \tag{A.34}$$

The gyrated impedance corresponds to an inductor in series with a resistor. Figure A-10 shows the series-type bandpass filter implemented with transconductors. Capacitor C_1 is originally C from the passive filter, and C_2 is gyrated into an inductor. Transconductors G_{m2} and G_{m3} implement the gyrator, and G_{m1} implements a resistance. The output is taken as shown to obtain a bandpass response. The alternate output at V_{hp} provides a combined highpass plus bandpass response. The transfer functions are:

$$\frac{V_{bp}}{V_{in}} = \frac{G_{m2}}{G_{m1}}\left(\frac{\frac{G_{m1}C_1}{G_{m2}G_{m3}}s}{\frac{C_1C_2}{G_{m2}G_{m3}}s^2 + \frac{G_{m1}C_1}{G_{m2}G_{m3}}s + 1}\right) = A_{\omega_0}\left(\frac{\frac{\tau s}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1}\right) \tag{A.35}$$

$$\frac{V_{hp}}{V_{in}} = \frac{\frac{C_1C_2}{G_{m2}G_{m3}}s^2 + \frac{G_{m1}C_1}{G_{m2}G_{m3}}s}{\frac{C_1C_2}{G_{m2}G_{m3}}s^2 + \frac{G_{m1}C_1}{G_{m2}G_{m3}}s + 1} = \frac{\tau^2 s^2 + \frac{\tau s}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.36}$$

$$
\begin{aligned}
A_{\omega_0} &= \frac{G_{m2}}{G_{m1}} \\
\tau &= \sqrt{\frac{C_1 C_2}{G_{m2} G_{m3}}} \\
Q &= \sqrt{\frac{C_2}{C_1}} \frac{\sqrt{G_{m2} G_{m3}}}{G_{m1}}
\end{aligned}
$$

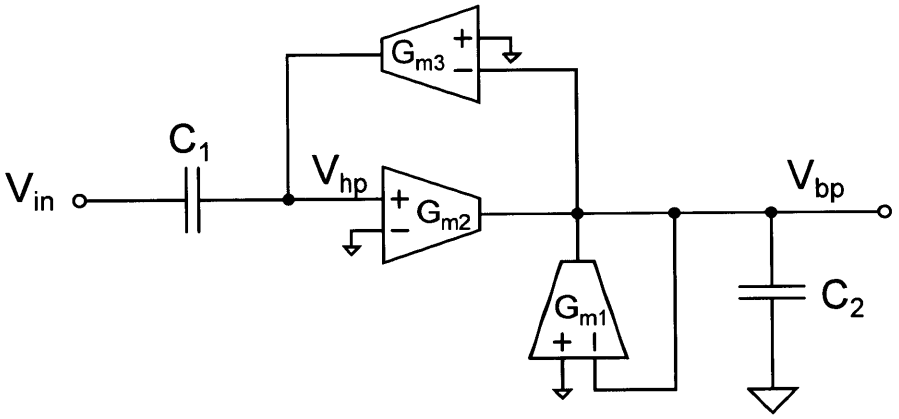


Figure A-10: $G_m - C$ bandpass filter based on the series RLC topology using gyrators.

A.6.2 Filter Synthesis by State-Space Equations

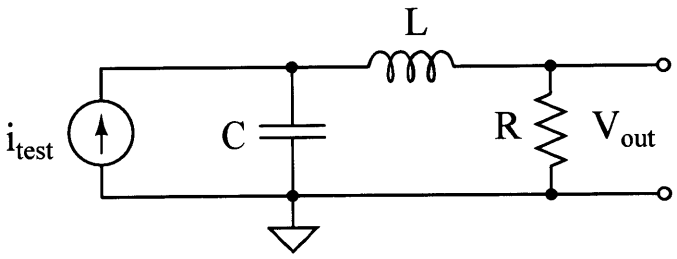


Figure A-11: The prototype series bandpass filter with input capacitor grounded and test current shown.

It is also possible to synthesize this filter from state-space, although not directly. The floating capacitor in the prototype is problematic for the state space approach because one of the state variables in question is the voltage *across* the capacitor, which is difficult to represent directly. It is not correct to simply eliminate the capacitor, work with only the series inductor and resistor, and then replace the capacitor later, as this ignores the interactions between the capacitor and the inductor. The

element replacement method works because in addition to preserving the correct transfer functions of each element, it also preserves the impedances of each element. In order to utilize state-space synthesis on the series bandpass topology, it is helpful to use a superposition whereby the input is removed and grounded. A test current can be injected at the ungrounded side of the capacitor, as shown in Figure A-11. If we assume that $i_{test} = V_{in}/R$, then we can obtain the transfer function to the output:

$$\frac{V_{out}}{i_{test}} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{1}{s^2LC + RCs + 1}$$

which canonically is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{\tau^2 s^2 + \frac{\tau s}{Q} + 1}$$

which is just a lowpass filter. This is not entirely surprising as feeding the input through a capacitor instead of a conductance should add a single differentiator, converting a lowpass into a bandpass. We can now synthesize the circuit via state space based on this lowpass transfer function:

$$\frac{V_{lp}}{V_{in}} = \frac{1}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.37}$$

$$\left(\tau^2 s^2 + \frac{\tau s}{Q} + 1\right) V_{lp} = V_{in} \tag{A.38}$$

$$\tau s \left(\tau s + \frac{1}{Q}\right) V_{lp} = V_{in} - V_{lp} \tag{A.39}$$

$$\left(\tau s + \frac{1}{Q}\right) V_{lp} = \frac{1}{\tau s}\left(V_{in} - V_{lp}\right) \tag{A.40}$$

$$\tau s V_{lp} = \frac{1}{\tau s}\left(V_{in} - V_{lp}\right) - \frac{1}{Q} V_{lp} \tag{A.41}$$

$$V_{lp} = \frac{1}{\tau s}\left(\frac{1}{\tau s}\left(V_{in} - V_{lp}\right) - \frac{1}{Q} V_{lp}\right) \tag{A.42}$$

From Equation A.42 we can create a block diagram for the lowpass filter in $G_m - C$ format. The equivalent block diagram after bandpass conversion is shown in Figure A-12. In the lowpass version, the input block would be a simple G_m, but instead we have replaced that block with sC_1, which corresponds to feeding V_{in} to the bottom plate of C_1. Translating from the block diagram to an actual $G_m - C$ filter, we obtain the same filter topology and corresponding transfer functions as

with the element replacement technique (Figure A-10)

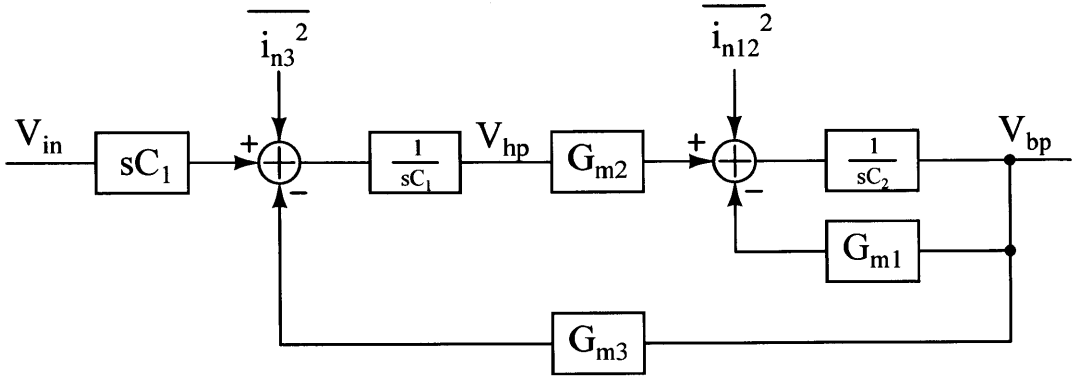


Figure A-12: Block diagram of the series-type gyrator-based bandpass filter.

A.6.3 Noise and Dynamic Range Analysis

The block diagram in Figure A-12 is useful for finding the noise of the filter. We must first find the noise transfer functions from each noise source to the output of the filter.

$$\frac{V_{bp}}{i_{n12}} = \frac{1}{G_{m1}} \cdot \frac{\frac{\tau s}{Q}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.43}$$

$$\frac{V_{bp}}{i_{n3}} = \frac{1}{G_{m3}} \cdot \frac{1}{\tau^2 s^2 + \frac{\tau s}{Q} + 1} \tag{A.44}$$

If we perform the same basic substitutions and integrate as we did for the parallel-type filter case, we obtain the output noise power:

$$v_{no}^2 = \frac{NqV_L}{4C_1}\left(\frac{G_{m2}}{G_{m1}} + \frac{C_2}{C_1}\left(1 + \frac{G_{m2}}{G_{m1}}\right)\right) \tag{A.45}$$

If we make the following substitutions:

$$G_{m2} = G_{m3} = G_\tau \tag{A.46}$$

$$C_1 = C_2 = C \tag{A.47}$$

$$\tau = \frac{C}{G_\tau} \tag{A.48}$$

$$G_{m1} = \frac{G_\tau}{Q} \tag{A.49}$$

The output noise power becomes:

$$v_{no}^2 = \frac{NqV_L}{4C}(2Q+1) \approx \frac{NqV_LQ}{2C}, Q \gg 1 \tag{A.50}$$

This is the same result obtained for the parallel-type $G_m - C$ bandpass filter. The maximum voltages seen by the transconductors in normalized units, and assuming filter parameters are chosen as listed above:

$$G_{m1} : |-V_{bp}| \leq \frac{G_{m2}}{G_{m1}} = Q \tag{A.51}$$

$$G_{m2} : |V_1| = \left| \frac{\frac{j\omega\tau}{Q} - \tau^2\omega^2}{1 - \tau^2\omega^2 + \frac{j\omega\tau}{Q}} \right| \leq Q \tag{A.52}$$

$$G_{m3} : |-V_{bp}| \leq Q \tag{A.53}$$

Under these conditions, both V_1 and V_{bp} see a gain of Q at the filter center frequency. Therefore, the output linear range is maximized since no one transconductor limits the performance. Therefore, one finds that the dynamic range of the series-type filter is the same as the parallel-type filter.

One will note that the highpass node, V_1, always has a gain of approximately Q at the center frequency, no matter how the transcondutors and capacitors are chosen. The bandpass node, V_{bp}, however, has a center-frequency gain of G_{m2}/G_{m1}, no matter what Q is chosen. At first glance, it might seem appropriate to set $G_{m1} = G_{m2}$ to make the center-frequency gain unity. However, the filter's dynamic range is maximized if we chose $G_{m2}/G_{m1} = Q$. This way, all transconductors in the circuit become saturated at the same input level. It then follows to choose $G_{m2} = G_{m3}$ and $C_1 = C_2$, just as we did in the parallel-type filter case.

A.7 Effect of Finite Output Impedance on Filter Performance

Thus far we have assumed ideal transconductors in all of our analyses. In practice, limited linear range and output impedance will limit overall filter performance. We can analyze the effect of finite output impedance by including the output impedance of each transconductor in our calculations. Figure A-13 shows the same filter as Figure A-6 but with R_o included. Repeating our analysis for the bandpass output, we obtain the following:

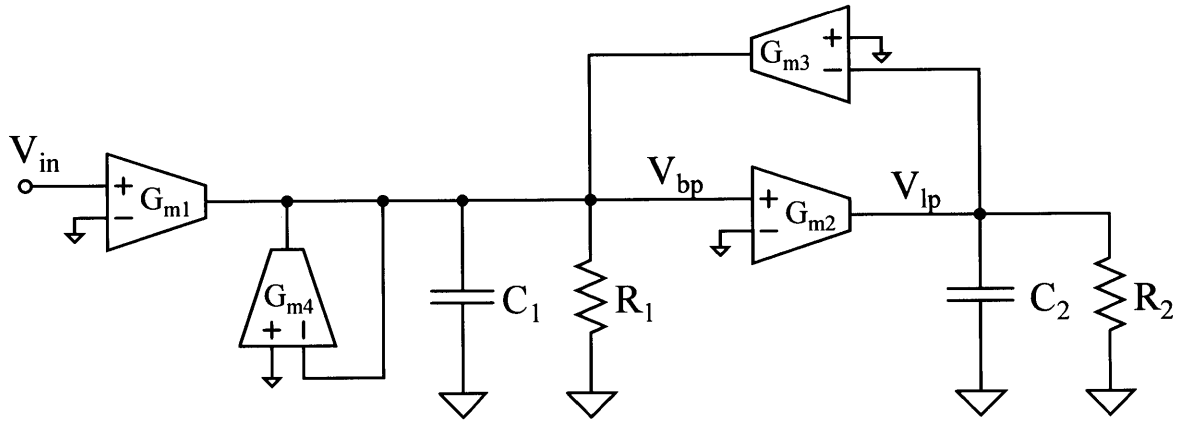


Figure A-13: $G_m - C$ bandpass filter implementation, shown with output impedances for calculating revised transfer functions.

$$\frac{V_{bp}}{V_{in}} = \frac{G_{m1}}{G_{m4}} \cdot \frac{\frac{G_{m4}R_1R_2C_2}{R_1R_2G_{m2}G_{m3}+1}s + \frac{1}{R_1R_2G_{m2}G_{m3}+1}}{\frac{R_1R_2C_1C_2}{R_1R_2G_{m2}G_{m3}+1}s^2 + \frac{G_{m4}R_1R_2C_2 + R_2C_2 + R_1C_1}{R_1R_2G_{m2}G_{m3}+1}s + 1}$$

Attempting to match the terms of Equation A.7 with the canonical form, plus applying some algebraic simplifications, we obtain the following values for Q_{eff}, τ_{eff}, and $A_{\omega_0,eff}$, the effective values of Q, τ, and A_{ω_0}. For simplicity, we have assumed $C_1 = C_2 = C$ and $\sqrt{G_{m2}G_{m3}} = G_\tau$. Q, τ, and A_{ω_0} are the nominal values obtained when R_o is ignored.

$$Q_{eff} \approx Q \times \frac{1}{1 + \frac{Q}{G_\tau \left(\frac{R_1 R_2}{R_1 + R_2} \right)}} \tag{A.54}$$

$$\tau_{eff} = \tau \times \sqrt{\frac{G_\tau^2 R_1 R_2}{1 + G_\tau^2 R_1 R_2}} \tag{A.55}$$

$$A_{\omega_0,eff} \approx A_{\omega 0} \times \frac{1}{1 + \frac{Q}{G_\tau \left(\frac{R_1 R_2}{R_1 + R_2} \right)}} \tag{A.56}$$

We can now evaluate these equations by substituting in values for R_1 and R_2. We can make a simple assumption that a given transconductor has a constant DC gain, or $G_m R_o$ product. If all transconductors operate in weak inversion, this is roughly correct as transconductance is proportional to bias current in weak inversion, and output impedance is inversely proportional to bias current, resulting in a constant product. Let us begin by defining G_τ as the nominal transconductance with a corresponding output impedance of R_o. The table below shows the values for transconductance and output impedance under the standard biasing arrangement:

Table A.1: Transconductance and output impedances under the standard biasing arrangement.

	Transconductance	Output Impedance
G_{m1}	G_τ/Q	QR_o
G_{m2}	G_τ	R_o
G_{m3}	G_τ	R_o
G_{m4}	G_τ/Q	QR_o

Thus, we find the following for R_1 and R_2.

$$\begin{aligned} R_1 &= R_{o1} || R_{o3} || R_{o4} = \frac{Q}{Q+2} R_o \\ R_2 &= R_o \end{aligned}$$

Substituting these values, we find values for τ_{eff}, Q_{eff}, and $A_{\omega_0,eff}$.

$$\tau_{eff} = \tau \times \sqrt{\frac{\left(\frac{Q}{Q+2}\right) G_\tau^2 R_o^2}{\left(\frac{Q}{Q+2}\right) G_\tau^2 R_o^2 + 1}}$$

$$Q_{eff} = \frac{Q}{1 + \left(\frac{2Q+2}{G_\tau R_o}\right)}$$

$$A_{\omega_0,eff} = \frac{1}{1 + \left(\frac{2Q+2}{G_\tau R_o}\right)}$$

If we refer to the alternative biasing arrangement described earlier, the principal advantage was the reduction of filter noise. Among its disadvantages were increased power consumption and also the unexpected increase in gain of the filter's internal lowpass node. We can recalculate the variation of τ, Q, and $A_{\omega,0}$ based on this biasing arrangement:

Table A.2: Transconductance and output impedances under the alternative biasing arrangement.

	Transconductance	Output Impedance
G_{m1}	G_τ/Q	QR_o
G_{m2}	$G_\tau \times Q$	R_o/Q
G_{m3}	G_τ/Q	QR_o
G_{m4}	G_τ/Q	QR_o

The new values for R_1 and R_2 are:

$$R_1 = QR_o/3$$

$$R_2 = R_o/Q$$

$$\tau_{eff} = \tau \times \sqrt{\frac{G_\tau^2 R_o^2/3}{G_\tau^2 R_o^2/3 + 1}}$$

$$Q_{eff} = \frac{Q}{1 + \left(\frac{Q^2+3}{G_\tau R_o}\right)}$$

$$A_{\omega_0,eff} = \frac{1}{1 + \left(\frac{Q^2+3}{G_\tau R_o}\right)}$$

Although this analysis was carried out for the parallel-type bandpass filter, similar relationships can be derived for the series-type version, as well as for other outputs of these filters. The same general concepts apply. It is clear that the standard biasing arrangement is superior to the alternative arrangement when the accuracy of τ and Q are considered. The ability to generate high-Q is severely compromised for transconductors that do not have sufficient output impedance, and the problem is exacerbated in the alternative biasing arrangement because one transconductor has a seriously degraded output impedance due to its high bias current, an effect which is not compensated for by running other transconductors at lower bias current.

Figure A-14 shows expected deviations in A and Q for various transconductor DC gains ($G_\tau R_o$) for both the standard and alternate biasing topologies. Clearly the standard topology is preferred if possible, and high DC gain is important for high Q. If necessary, transconductor outputs can be cascoded to improve output impedance.

The effect of finite R_o on τ was negligible in all cases, so its plot is not shown here. Intuitively, the DC gain of a transconductor is irrelevant in setting τ because it is a high frequency property set by the crossover frequency of individual $G_m - C$ filter subcircuits, and is largely independent of what the gain at DC is. On the other hand, high Q requires extremely low loss, and R_o is enough to cause loss that interferes with obtaining that Q.

A.8 Capacitive Attenuation as a Linearization Technique

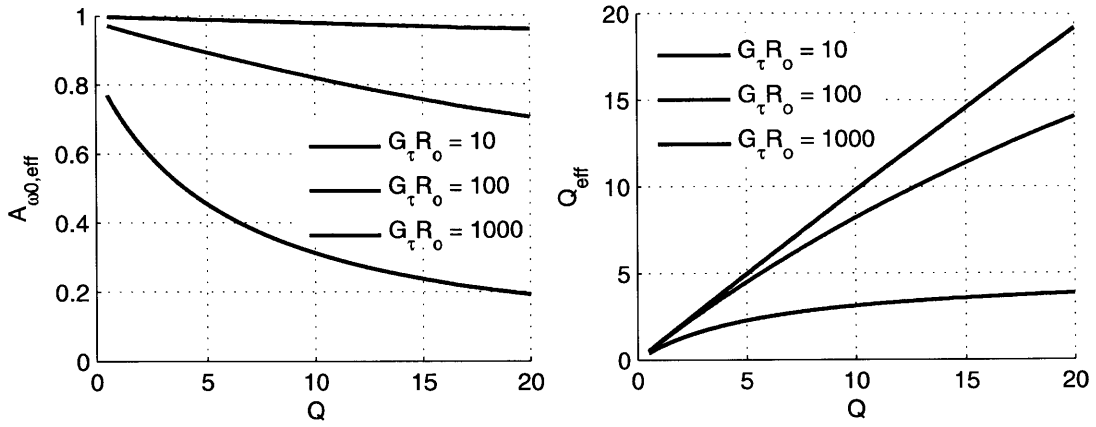
The ability of the bandpass filter to process signals with large input amplitudes without distortion is related to the linear range of the transconductors used to build the filter as well as the Q of the filter.[2] Capacitive attenuation effectively increases the linear range of the transconductors. In integrated technologies, it is possible to set accurate attenuation factors with capacitor ratios. Capacitive attenuation is also desirable since the capacitors consume no power, static or dynamic. However, in some cases, the DC operating point of purely capacitive nodes can be troublesome to set.

A.8.1 Capacitive Attenuation Building Blocks

Highpass Capacitive Attenuator

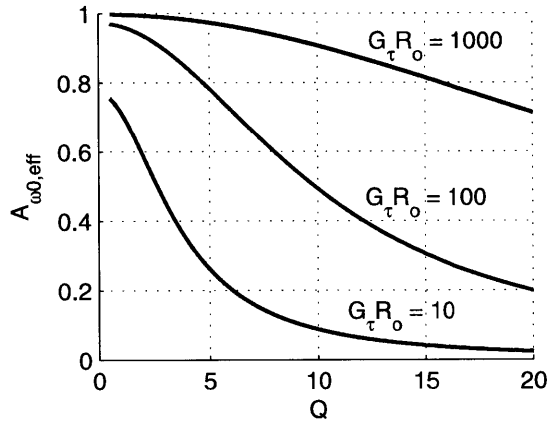
Figure A-15 shows a capacitively attenuated highpass filter.

[2]The overall linearity of the filter can be limited by saturation of *any* transconductor in the filter, not just those at the input or the output. Therefore, transfer functions from the input to the differential voltages across all transconductors must be considered. These transfer function magnitudes at center frequency are often determined in some way by Q.

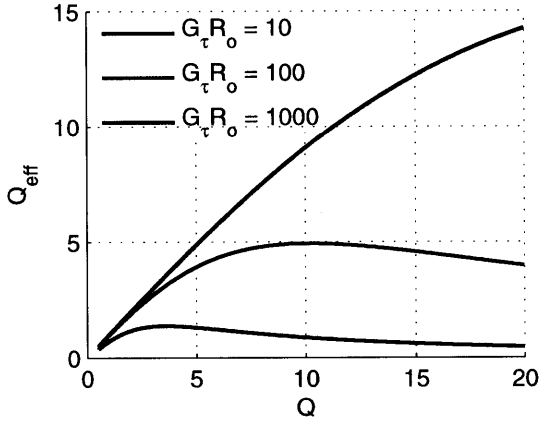


(a) $A_{\omega_0,eff}$ vs. ideal Q with standard biasing.

(b) Q_{eff} vs. ideal Q with standard biasing.



(c) $A_{\omega_0,eff}$ vs. ideal Q with alternate biasing.



(d) Q_{eff} vs. ideal Q with alternate biasing.

Figure A-14: Effect of Finite R_o on A_{ω_0} and Q for the standard and alternate biasing schemes for various transconductor DC gains, i.e., $G_\tau R_o$

The transfer function of this filter is given by:

$$\frac{V_{bp}}{V_{in}} = \frac{\frac{C}{G_m}s}{\frac{(A+1)C}{G_m}s+1} \tag{A.57}$$

The transconductor effectively behaves as a resistor. At low frequencies, the transconductor sets the operating point of V_{bp}, the middle node of the capacitive divider. At high frequencies, the transconductor loses control over V_{bp}, effectively behaving as an open circuit. Hence, V_{bp} is equal to V_{in} attenuated by a factor of $(A+1)$. Also note that the highpass pole is set by the total capacitance, $(A+1)C$.

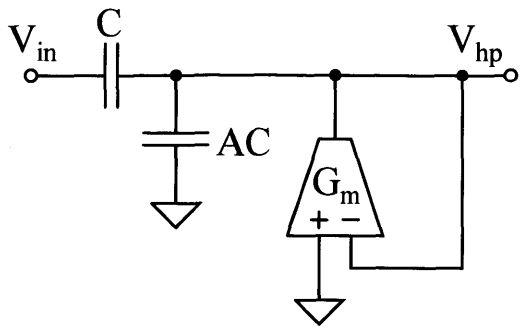


Figure A-15: A capacitive attenuation highpass filter.

Lowpass Capacitive Amplifier

Capacitive attenuation in the feedback path of a lowpass filter results in amplification. Figure A-16 shows a lowpass filter with capacitive attenuation used in the feedback path.

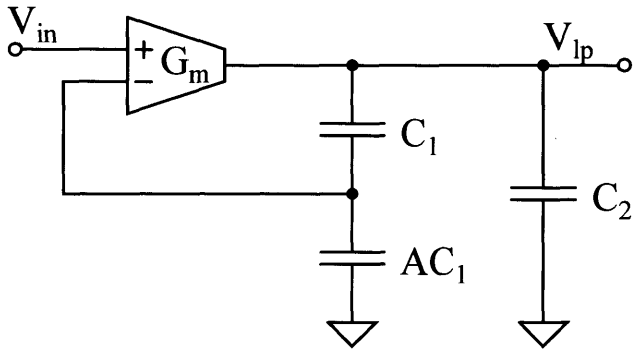


Figure A-16: Lowpass filter with gain provided by capacitive attenuation in the feedback path.

The transfer function for this filter is given by:

$$\frac{V_{bp}}{V_{in}} = \frac{A+1}{\left(\frac{AC_1 + (A+1)C_2}{G_m}\right)s + 1} \tag{A.58}$$

Here, we have added an extra capacitor, C_2, at the load of the transconductor. It does not affect the feedback ratio, but it does affect the overall transfer function. Without C_2, the pole frequency is $s = G_m/AC_1$. This does not perfectly mimic the highpass attenuator of Figure A-15, which has its pole frequency at $s = G_m/(A+1)C$. We can see from Equation A.58 that choosing $C_2 = C_1/(A+1)$ and $C_1 = C$ makes the lowpass and highpass filters precise duals of each other. The addition of C_2 means that when we assemble the bandpass filter from the lowpass and highpass building blocks, the design will be simplified. We will be able to relate all capacitors through constant

values for C and A. The bandpass filter transfer function τ and Q will also be controllable through simple ratios of the transconductances (discussed in Section A.8.2). The resulting modified transfer function for the lowpass filter is:

$$\frac{V_{bp}}{V_{in}} = \frac{A+1}{\frac{(A+1)\,C}{G_m}s+1} \tag{A.59}$$

Intuitively, C_2 is necessary because if we first consider the highpass filter of Figure A-15, we can see that the total capacitance at the output of the transconductor is $(A+1)\,C$. This, along with the G_m sets the highpass cut-in frequency. It is easily verified from the transfer function that this is correct. On the other hand, in the lowpass filter, first ignoring C_2, the transconductor drives a load equal to $A/\,(A+1)\,C_1$. Accounting for the filter's gain of $A+1$ due to the negative feedback path, the effective capacitance is equal to AC_1. To increase the total capacitance to $(A+1)C$ so that it matches the highpass filter, we can simply add an extra capacitor from the output to ground with value $C_1/\,(A+1)$. Assigning $C_1 = C$ and accounting for the filter gain of $A+1$, the extra capacitance effectively looks like an additional C, bringing the total effective load capacitance to $(A+1)\,C$, just as in the highpass case.

This lowpass filter structure with capacitive attenuation allows for large signal swings at V_{bp} while maintaining small differential voltages across the input to the transconductor. Once again, the linear range of the transconductor is effectively increased by a factor of $A+1$. It should be noted, however, that the DC operating point of the feedback node is purely capacitive and must be set through a high impedance path. Intuitively, a reasonable way to do this is to add a resistor across the capacitor C, which effectively puts the transconductor in a unity feedback configuration for DC. This will remove any DC voltage stored on C and set V_{bp} and the capacitive feedback node to the same DC value as V_{in}. However, this additional path introduces a pole-zero pair. The resistance must therefore be considerably large to ensure that it will not affect the passband of the filter. In audio filtering applications, the lowest frequency filter may be centered at 100 Hz, which means that the resistance needs to be on the order of 10 GΩ for integrated filters. Real resistors are not practical at these impedance levels. Additional low-frequency transconductors or adaptive elements could be used instead (Salthouse and Sarpeshkar, 2003).

Figure A-17 shows the capacitive attenuation lowpass filter with the DC biasing path, ignoring any output capacitance (C_2 in Figure A-16). The modified transfer function for this filter is given by Equation A.60. For simplicity, we will generally ignore the effects of this resistor when calculating

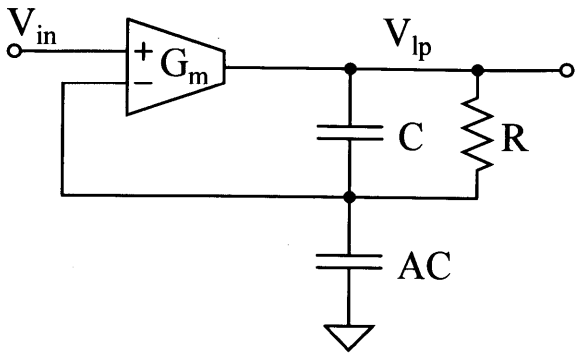


Figure A-17: Lowpass filter with capacitive attenuation showing the DC biasing path.

transfer functions and use the transfer function in Equation A.59 instead. However, the low frequency path must be considered when designing the filter and its effects must be made negligible at frequencies of interest.

$$\frac{V_{bp}}{V_{in}} = \frac{R(A+1)Cs+1}{\left(\frac{AC}{G_m}s+1\right)\left(RCs+1\right)} \tag{A.60}$$

A.8.2 The Capacitive Attenuation Bandpass Filter

Figure A-18 shows the schematic of the capacitive attenuation bandpass filter. Biasing of the feedback node, V_y, is not shown. The transfer function of this filter is:

$$\frac{V_{bp}}{V_{in}} = \frac{\frac{(A+1)C}{G_{m1}}s}{\frac{((A+1)C)^2}{G_{m1}G_{m2}}s^2 + \frac{(A+1)C}{G_{m1}}s+1} \tag{A.61}$$

In canonical form, τ and Q are given by:

$$\begin{aligned} \tau &= \frac{(A+1)C}{\sqrt{G_{m1}G_{m2}}} \\ Q &= \sqrt{\frac{G_{m1}}{G_{m2}}} \end{aligned}$$

In subthreshold, $G_m \propto I$, the bias current of the transconductor. Therefore, to raise τ while holding Q constant, G_{m1} and G_{m2} must be raised and lowered respectively by the same fraction.

This filter leads to similar behavior as the series-type $G_m - C$ bandpass filter with Q times as

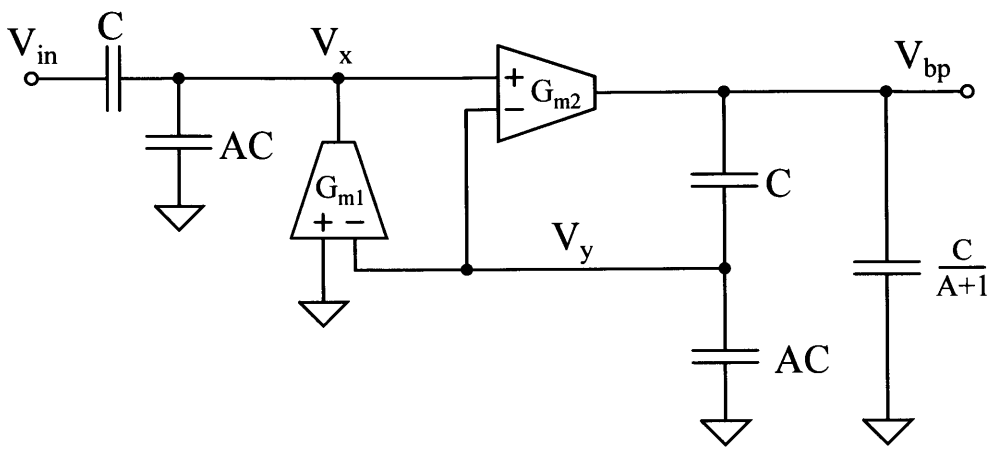


Figure A-18: Capacitive attenuation bandpass filter.

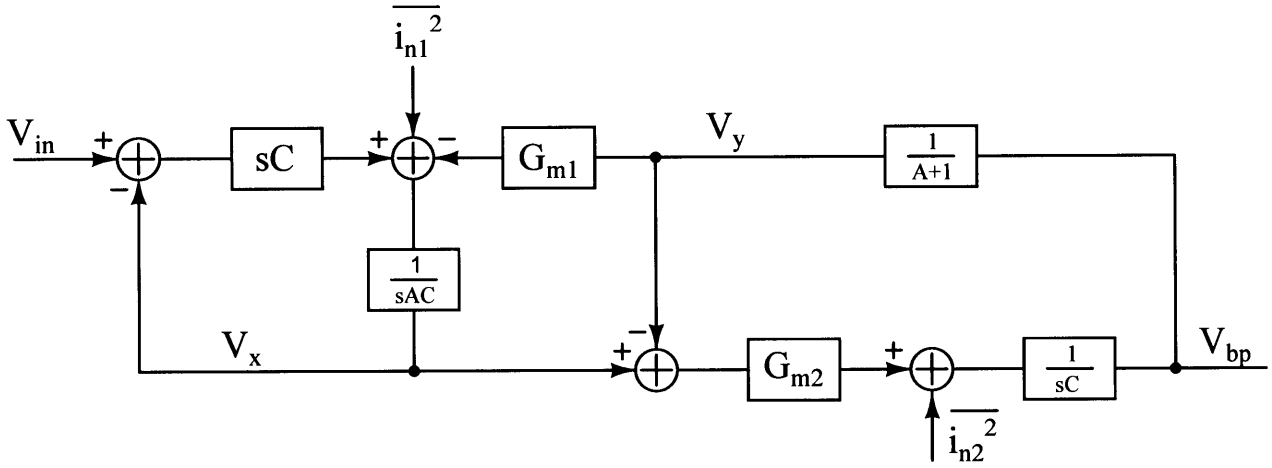


Figure A-19: Block diagram of the integrator-based bandpass filter for finding transfer functions.

much gain to the an internal node as compared to the output. The transconductor differential voltages are:

$$G_{m1} : |-V_y| \leq \frac{1}{A+1} \tag{A.62}$$

$$G_{m2} : |V_x - V_y| \leq \frac{Q}{(A+1)} \tag{A.63}$$

Total integrated output voltage noise power of the filter:

$$\overline{v_{no}^2} = \frac{NqV_L\,(A+1)}{2C} \tag{A.64}$$

As can be seen from Equation A.64, the total integrated output voltage noise of the filter depends on the linear range of the transconductors, the attenuation ratio, $(A+1)$, and the unit capacitance, C. Somewhat counterintuitively, while the total capacitance at each of the filter's nodes does set the filter poles, the attenuation capacitance doesn't filter the noise. In fact, it increases the noise because the factor of $(A+1)$ appears in the numerator, not the denominator of the noise expression. Once this is known, the expression begins to make sense. The capacitive attenuator effectively increases the linear range of the transconductor by a factor of $(A+1)$. The increase in linear range reduces the transconductance, requiring more bias current in the filter to maintain the same pole locations. The attenuator's capacitance has no other effect on the noise. Thus, the noise filtering capacitance is just the unit capacitor, C, and not the total capacitance, $(A+1)\,C$.

A.9 CMOS Implementation of a Capacitive Attenuation Bandpass Filter

The filter of Figure A-18 was fabricated in the United Microelectronics Corporation (UMC) 0.18μm analog CMOS process available via the Europractice service.

The operational transconductance amplifiers (OTA), G_{m1} and G_{m2} were based on the circuit of Figure A-20. This OTA has its linear range extended beyond the normal range of a differential pair, $2\phi_t/\kappa$ to $4\phi_t/\kappa$, where κ is the subthreshold slope factor, normally about 0.6-0.8. M_3 and M_4 form the input differential pair, and M_1 and M_2 act as source-degeneration MOS diodes which essentially provide a voltage division to the input signal as seen by M_3 in the ratio of $g_{m1}/(g_{m1}+g_{m3})$. This reduces to simply $1/2$ if $M_1 - M_4$ operate in the weak inversion region, hence the doubling of the linear range of the OTA. A host of other tricks are available to the designer, as described in (Sarpeshkar et al., 1997). The capacitive divider at the input helps reduce the signal seen by the input of the OTA, so advanced linearization techniques are not required.

As described previously, V_y requires a D.C. operating point. In this design, a D.C. path is provided by the circuit in Figure A-21. M_1 and M_2 behave essentially as zero-biased MOSFETs, provided a very high impedance leakage path to stabilize V_y at low frequencies. However, for A.C. operation, V_{bp} can swing above or below V_y by a large amount. For $V_{bp} > V_y$, M_1 remains firmly shut off, even if M_2 turns on. For $V_{bp} < V_y$, M_1 may turn on, but M_2 will be firmly off, thus preventing V_{bp} from ever shorting to V_y during A.C. operation.

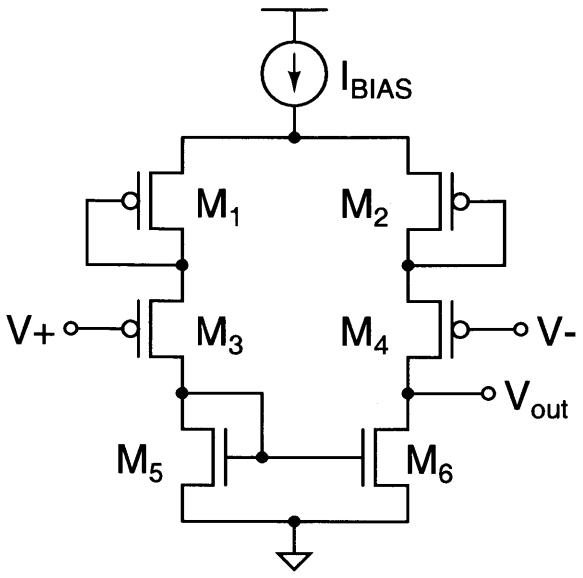


Figure A-20: OTA with linear range extended via source degeneration.

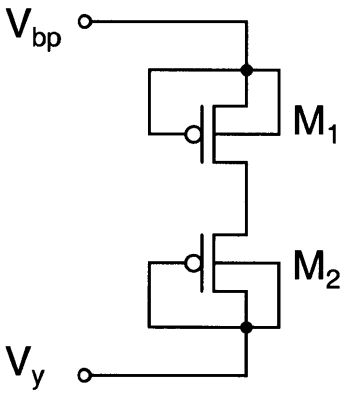


Figure A-21: A MOS resistor to provide the D.C. bias path to V_y.

A.10 Logarithmic Filter Biasing

As a matter of convenience, it is possible to generate bias currents automatically based on a logarithmic distribution. Transconductors operating in weak inversion have intrinsic transconductances and hence center frequencies proportional to their bias currents. Logarithmically spaced filter center frequencies are useful for spectral analysis.

Figure A-22 shows a CMOS circuit for generating logarithmically spaced bias currents. Basic operation is as follows: M_1 is supplied a bias current I_{low}, which is chosen as the lower limit of the logarithmic span. M_3 is fed a bias current of I_{high} at the upper limit of the range.

Now, there is a feedback loop at play in each of these sub-circuits. For the I_{low} loop, V_2 is a high

impedance node due to the output impedance of M_1. Current at the drain of M_1 pulls V_2 low quickly which pulls down the gate of M_2. M_2, loaded by a resistor string and the current source M_4 acts like a source-follower. A drop in V_2 causes V_1 to drop an equal amount, turning on V_1 strongly, enabling M_1 to accept the current I_{low}. As a result of the two-pole loop and high impedance node at V_2, a capacitor at V_2 is needed to stabilize this loop.

A similar feedback loop occurs at $M_3 - M_4$. The I_{high} input again pulls V_4 down strongly because of the high output impedance of M_3. M_4, as M_2, likewise behaves as a source-follower. A drop in V_4 causes a corresponding drop in V_3, turning on M_3 strongly and enabling the flow of I_{high}. C is once again needed at V_4 to stabilize the loop, as it is the high impedance node.

The way this circuit generates logarithmic currents is by first buffering the logarithmically compressed voltages V_1 and V_3, corresponding to I_{low} and I_{high} respectively. A resistor string in between the two, which can contain any number of unit resistors, R, generates a series of equally spaced voltages between V_1 and V_3, essentially a thermometer style DAC. The current through the resistor branch is therefore determined by the total resistance and the difference in V_1 and V_3.

A series of MOS switches, M_{sw}, allow any of the derived voltages to be connected to M_5 which exponentiates the voltage back into logarithmically spaced currents. The only requirement is that M_1, M_3, and M_5 all operate in weak inversion, and that M_1 and M_3 have identical dimensions.

M_2 is a special MOSFET which can carry a substantial current at $V_{GS} = 0$, a zero threshold MOSFET. This device may not be available in all processes, so modification to this circuit might be necessary. A zero V_{GS} for M_2 is needed to keep V_2 from rising too high and forcing M_1 out of saturation.

Figure A-23 shows measurements taken from the logarithmic DAC. As seen in subpanel (a), (c), and (d), the linearity of the resistor string is excellent. This is not surprising since a thermometer coded scale with only 32 levels should show excellent matching. The output current, shown in subpanel (b), ranges approximately from 2 nA to 600 nA. The current axis is logarithmic, so a straight line on this scale would represent perfect log spacing. However, at the higher DAC codes, it is apparent that approaching strong inversion was a problem, which caused the DAC not to fully keep pace. Nonetheless, this problem can be easily solved with using larger W/L MOSFETs.

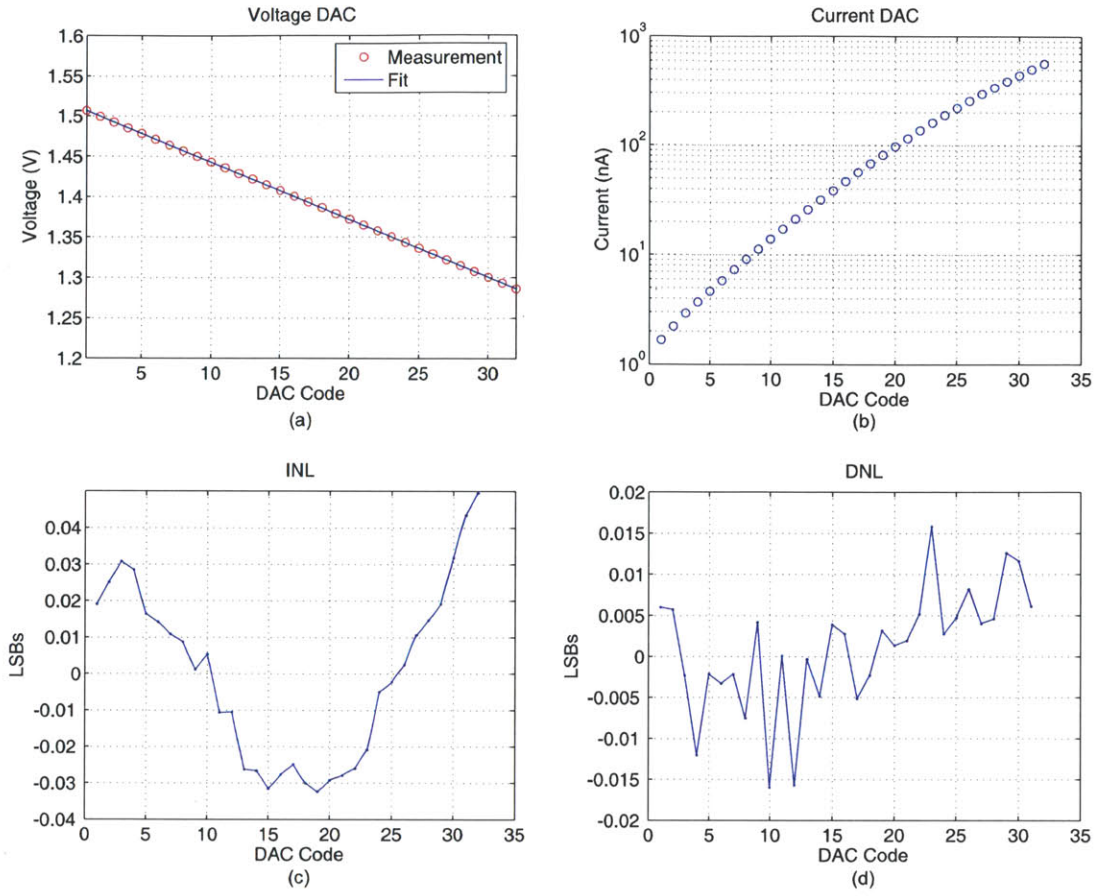


Figure A-23: Log DAC Measurements.

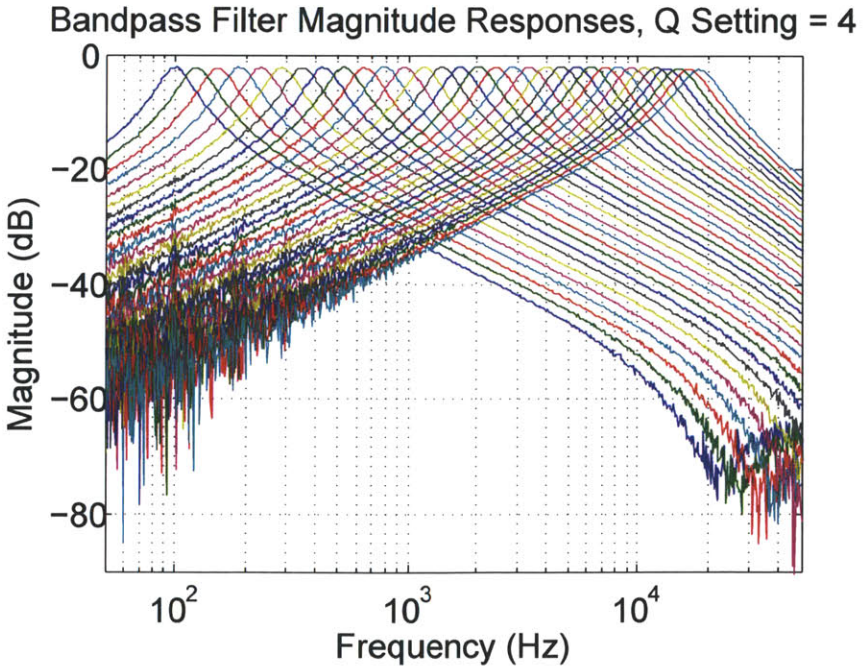


Figure A-24: Normalized frequency responses, Q setting = 4.

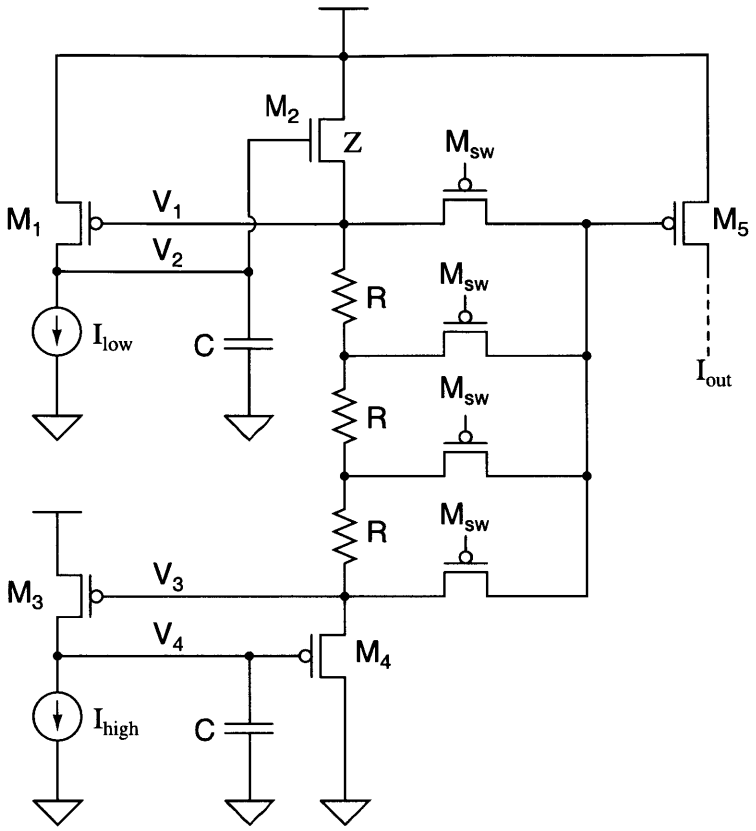


Figure A-22: Log DAC for biasing.

A.11 Bandpass Filter Measurements

Figure A-24 shows the frequency response of the filter at a constant Q setting of 4 over all the bias settings achieved with the logarithmic DAC. In Figure A-25a, the total harmonic distortion (THD) was measured as a function of input amplitude. As expected, the linear range is poor because of the growth of the signal at V_x by an extra factor of Q, which was 4. This result was obtained in Equation A.36 for the series-type bandpass filter. It is unavoidable in this topology because only two transconductors are used, requiring the bias arrangement which results in this unappealing phenomenon. The large signals saturate the transconductors, causing distortion, and also reduce effective transconductance, which has further implication beyond THD, as seen in the shift of the center frequency in Figure A-25b. Clearly, high distortion and center frequency shift are not acceptable for precise filtering applications.

Figure A-26 shows the relative contributions of the first 5 harmonics on the THD. It is apparent that at higher amplitudes, the third harmonic becomes dominant.

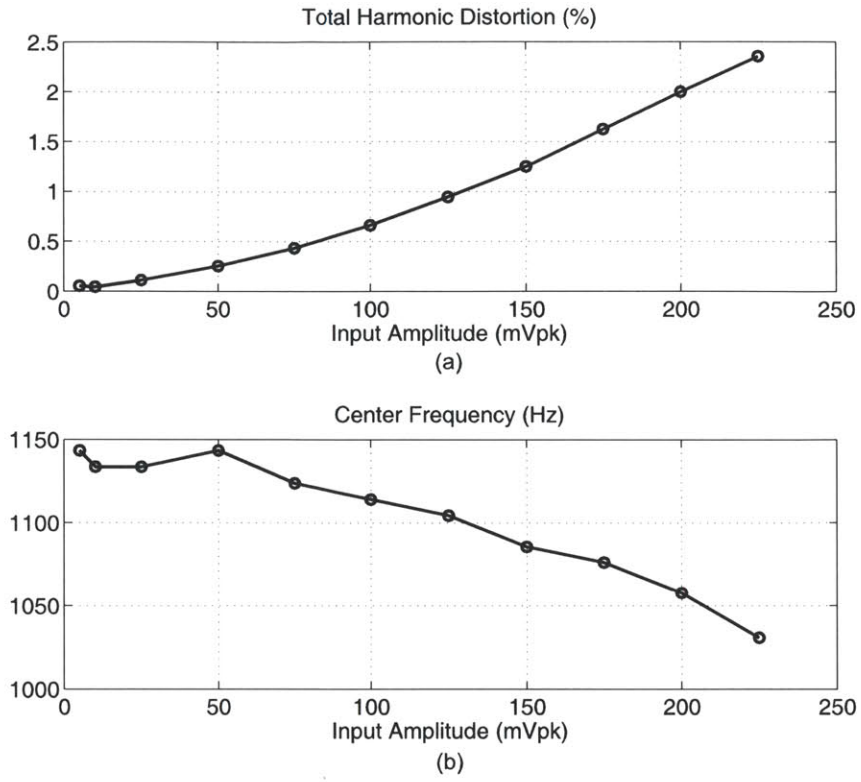


Figure A-25: THD measurements at 1 kHz center frequency.

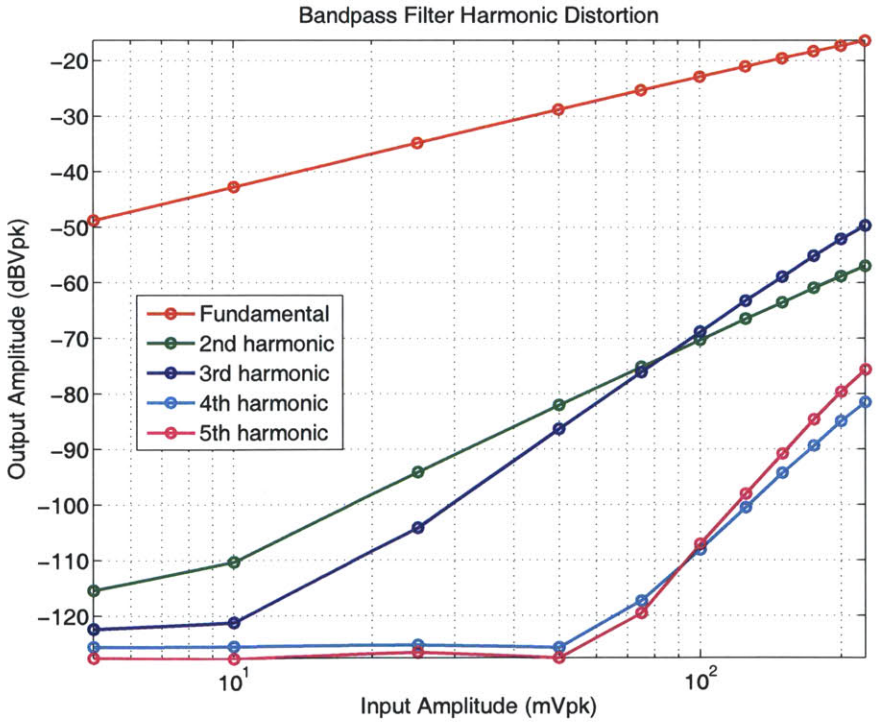


Figure A-26: Harmonic measuremnts.

References

Arfin SK, Long MA, Fee MS, Sarpeshkar R (2009) Wireless neural stimulation in freely behaving small animals. *J Neurophysiol* 102:598–605.

Ashmore RC, Wild JM, Schmidt MF (2005) Brainstem and forebrain contributions to the generation of learned motor behaviors for song. *J Neurosci* 25:8543–54.

Athas W, Svensson L, Koller J, Tzartzanis N, Ying-Chin Chou E (1994) Low-power digital systems based on adiabatic-switching principles. *IEEE T VLSI Syst* 2:398 –407.

Baker M, Sarpeshkar R (2003) A low-power high-psrr current mode microphone preamplifier. *IEEE J Solid-St Circ* 38:1671–1678.

Baker M, Sarpeshkar R (2006) Low-power single loop and dual-loop agcs for bionic ears. *IEEE J Solid-St Circ* 41:1983–1996.

Baker M, Sarpeshkar R (2007) Feedback analysis and design of RF power links for low-power bionic systems. *IEEE T Biomed Circ Syst* 1:28–38.

Bard A, Faulkner L (2001) *Electrochemical Methods: Fundamentals and Applications* John Wiley and Sons, Hoboken, NJ, Second edition.

Berg RW, Kleinfeld D (2003) Rhythmic whisking by rat: retraction as well as protraction of the vibrissae is under active muscular control. *J Neurophysiol* 89:104–17.

Bittar RG, Burn SC, Bain PG, Owen SL, Joint C, Shlugman D, Aziz TZ (2005) Deep brain stimulation for movement disorders and pain. *J Clin Neurosci* 12:457–63.

Boyden ES, Zhang F, Bamberg E, Nagel G, Deisseroth K (2005) Millisecond-timescale, genetically targeted optical control of neural activity. *Nat Neurosci* 8:1263–8.

Brummer SB, Turner MJ (1977) Electrochemical considerations for safe electrical stimulation of the nervous system with platinum electrodes. *IEEE T Biomed Eng* 24:59–63.

Cheng K, Lu Y, Tong KY, Rad A, Chow D, Sutanto D (2004) Development of a circuit for functional electrical stimulation. *IEEE T Neural Syst Rehabil Eng* 12:43 –47.

Collins KL, Lehmann EM, Patil PG (2010) Deep brain stimulation for movement disorders. *Neurobiol Dis* 38:338–345.

Comer D, Comer D (2004) Using the weak inversion region to optimize input stage design of CMOS op-amps. *IEEE T Circuits–II* 51:8–14.

Cooper BG, Goller F (2006) Physiological insights into the social-context-dependent changes in the rhythm of the song motor program. *J Neurophysiol* 95:3798–809.

Coulombe J, Sawan M, Gervais JF (2007) A highly flexible system for microstimulation of the visual cortex: Design and implementation. *IEEE T Biomed Circ Syst* 1:258–269.

Fee MS, Kozhevnikov AA, Hahnloser RH (2004) Neural mechanisms of vocal sequence generation in the songbird. *Ann N Y Acad Sci* 1016:153–70.

Fee MS, Leonardo A (2001) Miniature motorized microdrive and commutator system for chronic neural recording in small animals. *J Neurosci Meth* 112:83–94.

Ghovanloo M, Najafi K (2004) A modular 32-site wireless neural stimulation microsystem. *IEEE J Solid-St Circ* 39:2457 – 2466.

Ghovanloo M, Najafi K (2005) A compact large voltage-compliance high output-impedance programmable current source for implantable microstimulators. *IEEE T Biomed Eng* 52:97 –105.

Ghovanloo M, Najafi K (2007) A wireless implantable multichannel microstimulating system-on-a-chip with modular architecture. *IEEE T Neur Sys Reh* 15:449–457.

Glaze CM, Troyer TW (2006) Temporal structure in zebra finch song: implications for motor coding. *J Neurosci* 26:991–1005.

Hahnloser RH, Kozhevnikov AA, Fee MS (2002) An ultra-sparse code underlies the generation of neural sequences in a songbird. *Nature* 419:65–70.

Hahnloser RH, Kozhevnikov AA, Fee MS (2006) Sleep-related neural activity in a premotor and a basal-ganglia pathway of the songbird. *J Neurophysiol* 96:794–812.

Houweling AR, Brecht M (2008) Behavioural report of single neuron stimulation in somatosensory cortex. *Nature* 451:65–8.

Jasper H, Penfield W (1954) *Epilepsy and the Functional Anatomy of the Human Brain* Little, Brown and Co., 2nd edition.

Kelly SK (2003) A System for Efficient Neural Stimulation with Energy Recovery Ph.D. Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science.

Kelly SK, Wyatt JL (2011) A power-efficient neural tissue stimulator with energy recovery. *IEEE T Biomed Circ Syst* 5:20 –29.

Konishi M (1985) Birdsong: from behavior to neuron. *Ann Rev Neurosci* 8:125–170.

Krack P, Batir A, Van Blercom N, Chabardes S, Fraix V, Ardouin C, Koudsie A, Limousin PD, Benazzouz A, LeBas JF, Benabid AL, Pollak P (2003) Five-year follow-up of bilateral stimulation of the subthalamic nucleus in advanced parkinson's disease. *N Engl J Med* 349:1925–34.

Kringelbach ML, Jenkinson N, Owen SL, Aziz TZ (2007) Translational principles of deep brain stimulation. *Nat Rev Neurosci* 8:623–35.

Lee J, Rhew HG, Kipke D, Flynn M (2010) A 64 channel programmable closed-loop neurostimulator with 8 channel neural amplifier and logarithmic adc. *IEEE J Solid-St Circ* 45:1935 –1945.

Linderoth B, Forman RD (1999) Physiology of spinal cord stimulation: review and update. *Neuromodulation* 2:150–164.

Liu X, Demosthenous A, Donaldson N (2008) An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors. *IEEE T Biomed Circ Syst* 2:231 –244.

Livi P, Heer F, Frey U, Bakkum DJ, Hierlemann A (2010) Compact voltage and current stimulation buffer for high-density microelectrode arrays. *IEEE T Biomed Circ Syst* 4:372 –378.

Loizou P (1999) Introduction to cochlear implants. *IEEE Eng Med Biol Mag* 18:32 –42.

Long MA, Fee MS (2008) Using temperature to analyse temporal dynamics in the songbird motor pathway. *Nature* 456:189–94.

Mavoori J, Jackson A, Diorio C, Fetz E (2005) An autonomous implantable computer for neural recording and stimulation in unrestrained primates. *J Neurosci Methods* 148:71–7.

McDermott H (1989) An advanced multiple channel cochlear implant. *IEEE T Biomed Eng* 36:789–797.

Medtronic (2008) *DBS 3387, 3389 Lead Kit for Deep Brain Stimulation* Medtronic, Minneapolis, MN.

Merrill DR, Bikson M, Jefferys JG (2005) Electrical stimulation of excitable tissue: design of efficacious and safe protocols. *J Neurosci Meth* 141:171–198.

Moritz CT, Perlmutter SI, Fetz EE (2008) Direct control of paralysed muscles by cortical neurons. *Nature* 456:639–42.

Normann RA, Maynard EM, Rousche PJ, Warren DJ (1999) A neural interface for a cortical vision prosthesis. *Vision Res* 39:2577 – 2587.

Nottebohm F, Stokes TM, Leonard CM (1976) Central control of song in the canary, *Serinus canarius*. *J Comp Neurol* 165:457–486.

O'Doherty JE, Lebedev MA, Hanson TL, Fitzsimmons NA, Nicolelis MA (2009) A brain-machine interface instructed by direct intracortical microstimulation. *Front Integr Neurosci* 3:20.

Ortmanns M, Rocke A, Gehrke M, Tiedtke HJ (2007) A 232-channel epiretinal stimulator asic. *IEEE J Solid-St Circ* 42:2946 –2959.

Peng CW, Chen JJJ, Lin CCK, Poon PWF, Liang CK, Lin KP (2004/3/15) High frequency block of selected axons using an implantable microstimulator. *J Neurosci Meth* 134:81–90.

Perlmutter JS, Mink JW (2006) Deep brain stimulation. *Annu Rev Neurosci* 29:229–257.

Picone JW (1993) Signal Modeling Techniques in Speech Recognition. *Proc IEEE* 81:1215–1247.

Randles JEB (1947) Kinetics of rapid electrode reactions. *Disc Faraday Soc* 1:11–19.

Roach KL (2003) Electrochemical Models for Electrode Behavior in Retinal Prostheses M. Eng. Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science.

Salthouse CD, Sarpeshkar R (2003) A Practical Micropower Programmable Bandpass Filter for Use in Bionic Ears. *IEEE J Solid-St Circ* 38:63–70.

Salzman CD, Britten KH, Newsome WT (1990) Cortical microstimulation influences perceptual judgements of motion direction. *Nature* 346:174–7.

Sarpeshkar R (1997) Efficient Precise Computation with Noisy Components: Extrapolating From an Electronic Cochlea to the Brain Ph.D. Thesis, California Institute of Technology, Pasadena, California.

Sarpeshkar R, Lyon R, Mead CA (1997) A low-power wide-linear-range transconductance amplifier. *Analog Integr Circ S* 13:123–151.

Sarpeshkar R, Salthouse C, Sit JJ, Baker MW, Zhak SM, Lu TKT, Turicchia L, Balster S (2005) An Ultra-Low-Power Programmable Analog Bionic Ear Processor. *IEEE T Biomed Eng* 52:711–727.

Sarpeshkar R, Wattanapanitch W, Arfin SK, Rapoport BI, Mandal S, Baker MW, Fee MS, Musallam S, Andersen RA (2008) Low-power circuits for brain-machine interfaces. *IEEE T Biomed Circ Syst* 2:173–183.

Sarpeshkar R (2010) *Ultra Low Power Bioelectronics* Cambridge University Press, Cambridge, UK.

Schaumann R, Valkenburg MEV (2001) *Design of Analog Filters* Oxford University Press, New York.

Simpson J, Ghovanloo M (2007) An experimental study of voltage, current, and charge controlled stimulation front-end circuitry In *ISCAS*, pp. 325 –328.

Sit JJ, Sarpeshkar R (2004) A micropower logarithmic a/d with offset and temperature compensation. *IEEE J Solid-St Circ* 39:308–319.

Sit JJ, Sarpeshkar R (2007a) A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 na dc error for 1-ma full-scale stimulation. *BIEEE T Biomed Circ Syst* 1:172–183.

Sit JJ, Sarpeshkar R (2007b) A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 na dc error for 1-ma full-scale stimulation. *IEEE T Biomed Circ Syst* 1:172 –183.

Smith B, Peckham PH, Keith MW, Roscoe DD (1987) An externally powered, multichannel, implantable stimulator for versatile control of paralyzed muscle. *IEEE T Biomed Eng* BME-34:499 –508.

Sooksood K, Stieglitz T, Ortmanns M (2010) An active approach for charge balancing in functional electrical stimulation. *IEEE T Biomed Circ Syst* 4:162 –170.

Sossinka R, Böhner J (1980) Song types in the zebra finch (poephila guttata castanotis). *Z Tierpsychol* 53:123–132.

Sotiriadis PP, Çelik A, Loizos D, Zhang Z (2007) Fast State-Space Harmonic-Distortion Estimation in Weakly Nonlinear $G_m - C$ Filters. *IEEE T Circuits–I* 54:218–228.

Swadlow HA (1998) Neocortical efferent neurons with very slowly conducting axons: strategies for reliable antidromic identification. *J Neurosci Methods* 79:131–41.

Talwar SK, Xu S, Hawley ES, Weiss SA, Moxon KA, Chapin JK (2002) Rat navigation guided by remote control. *Nature* 417:37–8.

Tarsy D, Vitek JL, Starr PA, Okun MS (2008) *Deep Brain Stimulation in Neurological and Psychiatric Disorders* Humana Press.

Theogarajan L (2008) A low-power fully implantable 15-channel retinal stimulator chip. *IEEE J Solid-St Circ* 43:2322–2337.

Thurgood B, Warren D, Ledbetter N, Clark G, Harrison R (2009) A wireless integrated circuit for 100-channel charge-balanced neural stimulation. *IEEE T Biomed Circ Syst* 3:405 –414.

Tsividis Y (1999) *Operation and modeling of the MOS transistor, second edition* Oxford University Press, New York, 2nd edition.

Vidal J, Ghovanloo M (2010) Towards a switched-capacitor based stimulator for efficient deep-brain stimulation In *EMBS*, pp. 2927 –2930.

Vu ET, Mazurek ME, Kuo YC (1994) Identification of a forebrain motor programming network for the learned song of zebra finches. *J Neurosci* 14:6924–6934.

Wang CZ, Herbst JA, Keller GB, Hahnloser RH (2008) Rapid interhemispheric switching during vocal production in a songbird. *PLoS Biol* 6:e250.

Wattanapanitch W, Fee M, Sarpeshkar R (2007) An energy-efficient micropower neural recording amplifier. *IEEE T Biomed Circ Syst* 1:136–147.

Wei XF, Grill WM (2009) Impedance characteristics of deep brain stimulation electrodes in vitro and in vivo. *J Neural Eng* 6:046008.

Xiao J, Peterchev A, Zhang J, Sanders S (2004) A 4 μA quiescent-current dual-mode digitally controlled buck converter ic for cellular phone applications. *IEEE J Solid-St Circ* 39:2342 – 2348.

Yu AC, Margoliash D (1996) Temporal hierarchical control of singing in birds. *Science* 273:1871–5.

Zhak SM, Baker MW, Sarpeshkar R (2003) A low-power wide dynamic range envelope detector. *IEEE J Solid-St Circ* 38:1750–1753.

Zoll PM (1952) Resuscitation of the heart in ventricular standstill by external electric stimulation. *New Engl J Med* 247:768–771.