Analysis of Terabit/Second-Class Inter-Chip Parallel Optoelectronic Transceiver

by

Nguyen Hoang Nguyen

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Signature of Author.....
Department of Materials Science and Engineering
August 12, 2010

Certified by.....
Lionel C. Kimerling
Thomas Lord Professor of Materials Science and Engineering
Thesis Supervisor

Accepted by.....
Christopher Schuh
Chair, Departmental Committee on Graduate Students

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ABSTRACT

Electrical copper-based interconnect has been suffering from fundamental physical loss mechanism and its current infrastructure will not be able to meet the increasing demand for data rates due to reaching the limit of the transmission bandwidth-distance product. Optical interconnect has been known as the candidate for taking over the obsolete electrical counterpart owing to the capability of transmitting data at high rates with low loss and the feasibility for parallel integration. Optoelectronic transceiver is one of the essential elements in optical interconnect system. This thesis scrutinizes a complete set of constituent technologies developed for a novel inter-chip parallel optoelectronic (OE) transceiver (known as Terabus transceiver) which is able to communicate data at the speed in the range of Terabit/second.

A novel packaging hierarchy and a creative design for an optical coupling mechanism devised to bring high-level integration and high-speed performance to a final package have been analyzed: Two 4x12 arrays (each < 9 mm^2) of CMOS transmitter and receiver ICs have been flip-chip bonded to a silicon carrier interposer of 1.2-cm^2 size. Other two 4x12 arrays of OE devices (VCSELs and photodiodes) with comparable size are then flip-chip bonded to the corresponding CMOS arrays attached to the silicon carrier, forming the Optochip assembly. The Optochip is in interface with an Optocard by the flip-chip bonding process between the silicon carrier and an organic card patterned with 48 integrated waveguides at density of 16-channel/mm and total length of 30 cm. The 985-nm operating wavelength of the lasers allows a simple optical design with emission and illumination through arrays of relay lenses directly etched into the backside of the OE III-V substrate. A novel design of 45°-tilted and Au-coated mirrors fabricated in 125-μm-pitch acrylate waveguides is to perpendicularly couple the light in and out of the core of these Optocard waveguides. Per-channel performance of up to 20 Gb/s for transmitter and of up to 14 Gb/s for receiver have been realized.

Lastly, the thesis has analyzed the market opportunity of the transceiver by reviewing the market situation, identifying contemporary competing technologies, assessing the market prospect and predicting the cost.

Thesis Supervisor: Lionel C. Kimerling
Title: Thomas Lord Professor of Materials Science and Engineering

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PART I

BACKGROUND OF SILICON MICROPHOTONICS

And

OPTOELECTRONIC TRANSCEIVER FUNDAMENTALS

CHAPTER 1: The coming regime of Silicon microphotonics

1. Why silicon microphotonics?

Electronic communication links are degraded by fundamental physical loss mechanisms including dielectric losses and skin effect losses which are all functions of distance and bandwidth. In addition, near/far end crosstalk and noise aggravate these loss mechanisms. There is the maximum communication rate subjected to losses and noise levels for a given signal strength as stated by Shannon's law. As the demand for ever increasing bandwidth communication proceeds, the communication capability of electronic-based link gets asymptotic to this fundamental limit. Switching to alternative communicating platform is the essential trend. For many industries, photonics platform is the choice to replace electronics platform when the limitation is reached. Figure 1 shows the transition border (the red zone) between these two platforms based up on bandwidth-distance product criteria.

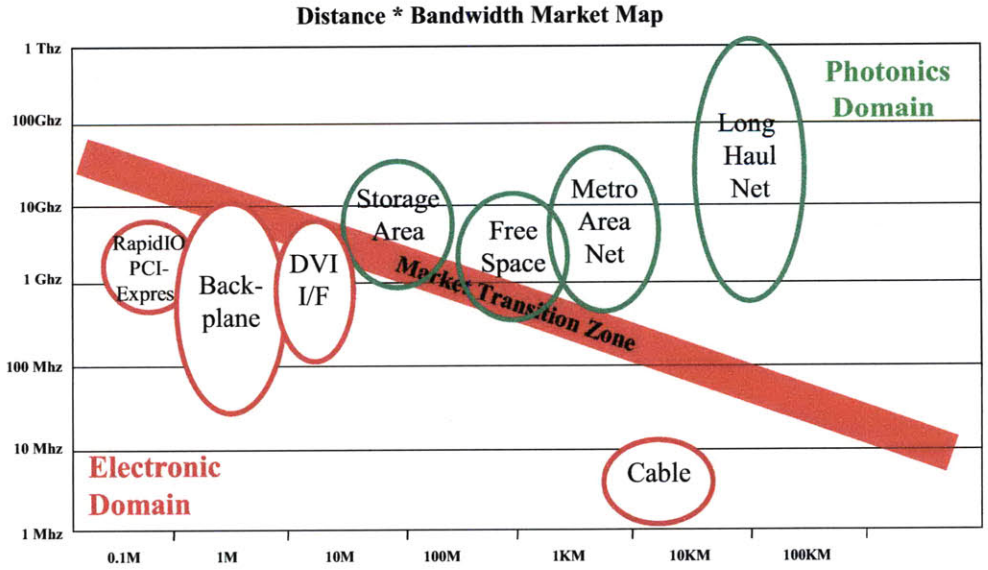

Figure 13: Electronics-photonics domain transition border [1].

As shown clearly, the Long Haul Net has been already in the photonics domain because of the high requirement for transmitting high bandwidth over long distance while conventional Cable is still in the electronics domain due to low requirement for high bandwidth transmission. Each of the above industries is increasing demand for bandwidth throughout the time, ultimately exhausting the practical capabilities of electronic-based solutions.

Challenge for the transition to take place is that: the advent of an optical replacement of suitable cost during this transition zone will enable earlier conversion, that's why the cost of photonic links will likely need to be competitive with the cost of copper-based counterparts. To make use of the economic advantage of silicon, the key to reduce cost will be monolithic integration, just as VLSI electronics. Integrated silicon microphotonics which is fabricated monolithically by CMOS process will achieve a complete set of microphotonics devices using available process in existing CMOS fabs.

The key drivers for silicon microphotonics which are bandwidth cost and bandwidth volume will increase pressure for monolithic photonics integration as well as for low cost and small form factor optical packaging and high-speed interconnect. Key discussed silicon microphotonics technologies which implement optical communication links would be receivers, transmitters, filters, packaging, source and integration strategies. The goal is that sources, detectors, and modulators, as well as passive components such as waveguides and filters are made from silicon or new photonics compatible materials, e.g. Ge, BaTiO3 etc, and acceptable dielectrics and metals.

Figure 2 schematically describes very well elements of silicon microphotonics technology required for a typical optical link.

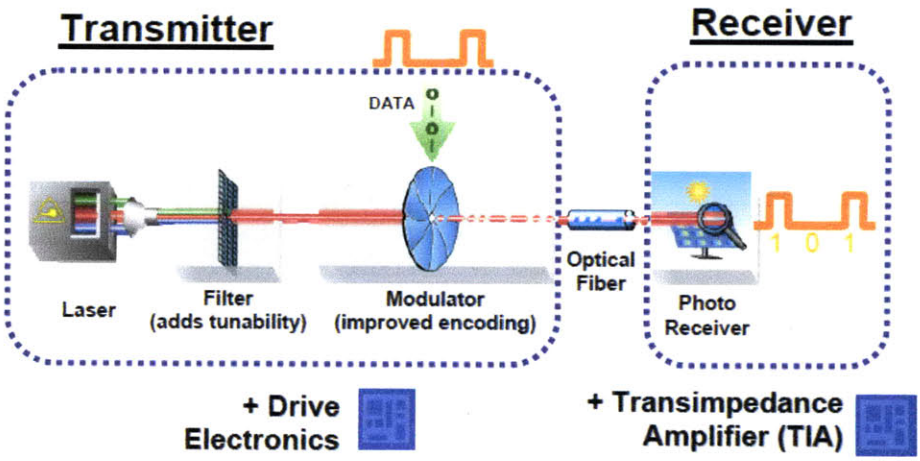

Figure 14: Elements of an optical link [courtesy Intel].

These element technologies are comprised of the followings:

- Integrated Receiver Technology
- Modulator Technology
- Photonic Source Strategy
- Filter Technology
- Packaging and Interconnect Technology

2. Roadmap for Silicon Microphotonics

According to Communications Technology Roadmap (CRT) and MIT Industry Consortium [1], the roadmap for silicon microphotonics is suggested as in Figure 3. There are several prominent characteristics of the roadmap listed as follow, noting that inter-step iterations are expected and essential for technology development:

- Steps in the roadmap illustrate a nature but not necessary linear
- Each block sets the foundation and justification for the subsequent block
- Subsequently blocks may uncover technology that impacts previous blocks

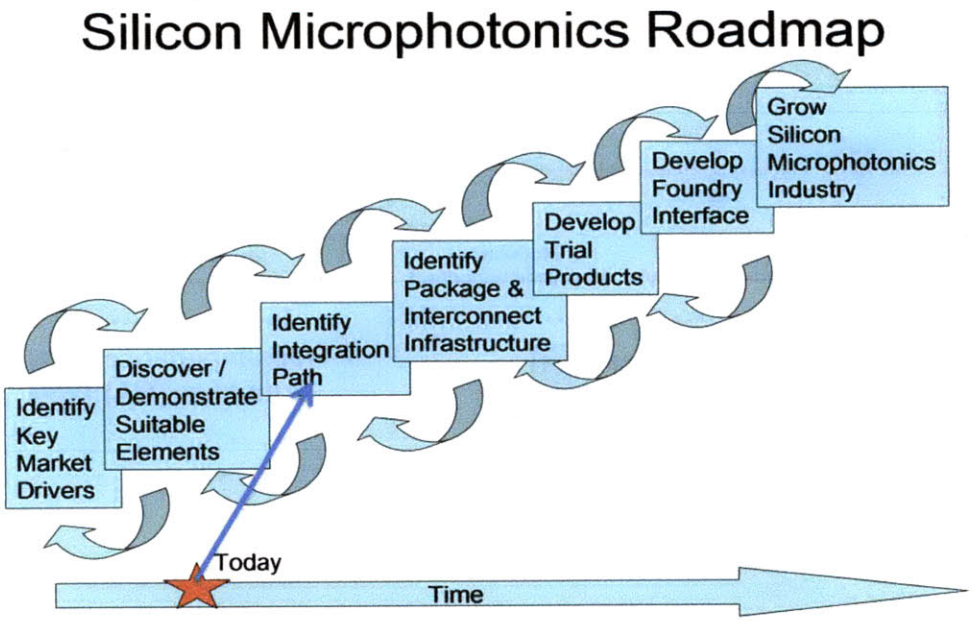

Figure 15: Roadmap for Silicon microphotonics [Courtesy MIT CRT] [1].

The strategy is that different companies will focus on different steps (blocks) in the roadmap, but work together to benefit from the infrastructure of other steps, forming the Microphotonics Industry Consortium.

CHAPTER 2: Optoelectronic Transceiver Fundamentals

1. Overview

The basic function of an optoelectronic transceiver is to receive optical signal which is laser light, convert it into electronic digital signal in terms of binary sequences of 1s & 0s; and in the reverse order, convert binary sequences of 1s & 0s into corresponding optical pulses and transmit them. That's where the name transceiver comes from, reflecting the two-way function of the device which can be described as transmitter and receiver altogether.

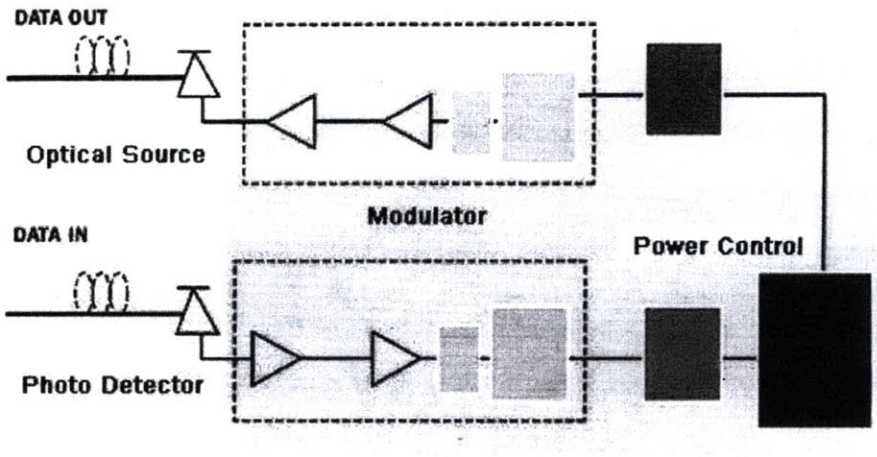

Figure 16: Functional Block Diagram of a typical optoelectronic transceiver.

A typical optoelectronic transceiver consists of 4 major parts: optical laser source, photo detector, electronic modulator and power control unit. Photo detector receives optical variations and converts into voltage and/or current variations whereas, when control signal which is a sequence of binary numbers of 1 & 0 comes in, the modulator dictates the optical laser source to

send out corresponding optical signals. Short-range optoelectronic transceiver functions to receive and transmit optical signal in the range shorter than 1 meter.

2. Parts of Optoelectronic Transceiver

a. Optical Laser Source Technology:

The key function of an optical laser source is to convert electronic signal into optical light. There the following 3 alternatives:

- Light Emitting Diode (LED)
- Edge-Emitting Laser (EEL)
- Vertical Cavity Surface Emitting Laser (VCSEL)

Table 1: Comparison between two common EEL and VCSEL optical laser sources[1].

Specification	EEL	VCSEL
Application	Telecom	Datacom
Active Region Confinement	300*400*0.07	3*3*0.07
Modulation Frequency	20GHz	120GHz
Threshold Current	20mA	0.5mA
Output Power	45mW	0.17mW
Power Efficiency	0.89A/W	11.76A/W

Key consideration for optical source in short range transmission would be modulation frequency and transmission power which are both determined by the size of the active region. With small active layer, the loss should be small, threshold current is reduced and modulation frequency would be larger.

Light Emitting Diode (LED):

LED has a simple structure which contains no confinement layer. Light can come out at any position with a wide range of energy spectrum. As the result, power output for LED is high

[1] *Refer to Reference [5], Table 2.1, page 10.*

and LED is suitable for display and lighting applications. Since the modulation frequency of LED is relatively low, LED is simply not a good candidate for optical source in high-speed transceivers.

Edge-Emitting Laser (EEL):

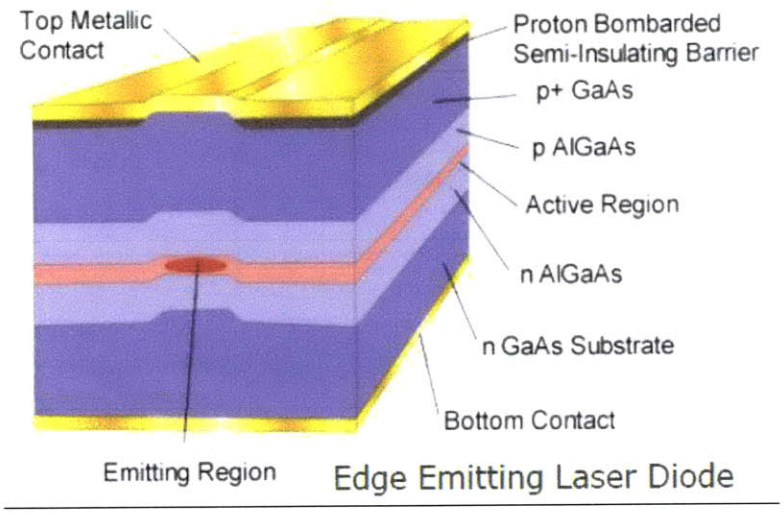

Figure 17: Structure of an edge-emitting laser [2].

In EEL, laser light is emitted laterally from the edge of the structure as shown as the emitting region in Figure 5. The active region is large enough to emit not too weak transmission power (~45mW, as can be seen in Table 1, but still much less than the transmission power of LED, which is ~ 0.1W) while can still achieve relatively high modulation frequency (~20 GHz, as can be seen in Table 1, but still smaller than the modulation frequency observed in VCSEL. With that balancing between emission power and modulation frequency, EEL is now the current technology for telecommunication.

Vertical Cavity Surface Emitting Laser (VCSEL):

In this type of laser, the active layer is confined between two distributed Bragg reflectors (DBRs) which function as laser mirrors. Active area is further reduced by lateral oxidation

confinement, which significantly boosts up the modulation frequency capability (>100GHz) and reduces threshold current of the device down to several μA.

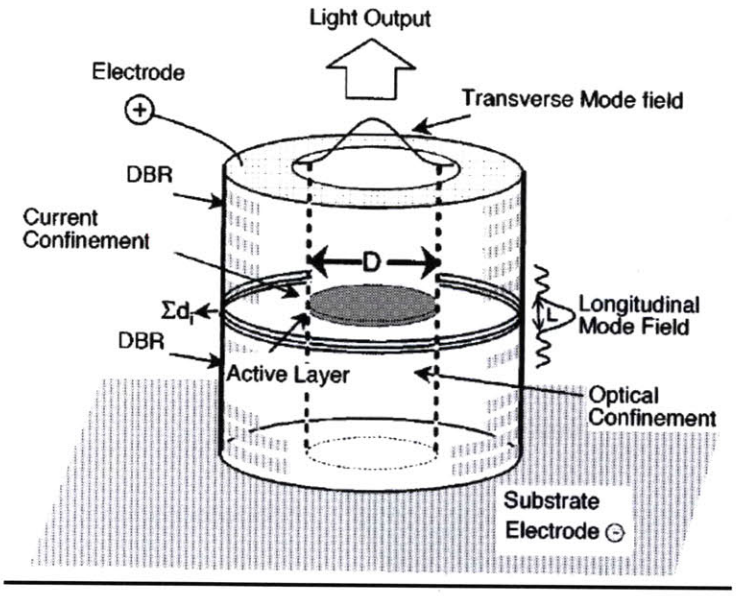

Figure 18: Structure of a vertical cavity surface emitting laser [3].

Having very high modulation frequency, VCSEL has been becoming the right choice for optoelectronic transceiver technology now and in future.

Key Competitive Laser Source Technology:

Two classes of technologies for active optoelectronics (laser sources) are emerging in research labs. Each involves semiconductor particles controllably made on the nanometer length scale: (1) Solution-processed devices using materials such as InAs, PbS, PbSe produce infrared lights and (2) Si-nanocrystal active devices which can be processed by existing CMOS-compatible technologies such as plasma-enhanced chemical vapor deposition (PECVD) to produce photoluminescence and electroluminescence [1].

Key Power Module Technology for Laser Source:

High-speed coherent sources have only been demonstrated through hybridization. In such cases, vertical-cavity surface-emitting laser or edge emitting laser are mounted on Si platform and coupled into appropriate waveguide [1]. Central photonic power source analogous to an electronic power supply may be cost effective, which could feed many ICs without a need for each chip to have its own laser. This benefit should be substantial in multi-link applications but may not be in single optical link. Direct modulation diode lasers (near source) will run at higher energy densities, and likely have lower reliability. Continuous wave lasers (far source) will need to be compatible with on-chip modulation, implying polarization, mode, loss and wavelength control.

Recent Research Breakthrough in Germanium Laser Source:

MIT researchers from the Electronic Materials Research Group (EMAT) led by Professor Lionel C. Kimerling have demonstrated the first laser built from germanium that can produce wavelengths of light for optical communication [4]. It is the first germanium laser to operate at room temperature. Different from other typical materials for lasers, germanium is easy to be integrated into existing processes of silicon chip manufacturing. Since the addition of germanium increase the speed of silicon chips (germanium has carrier mobilities larger than those of silicon), incorporating germanium into the manufacturing process is what almost all chip manufacturers have already done or started to do. This germanium-laser project which is carried out by the group has opened up the new level of monolithic integration for silicon microphotonics.

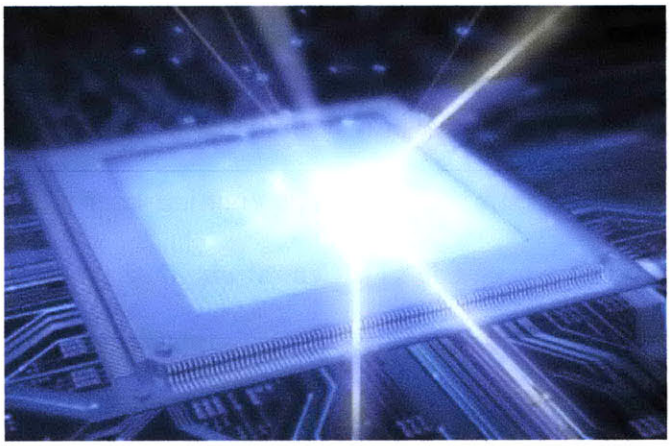

Figure 19: Laser built from germanium for optical communication, courtesy: MIT EMAT group [4].

b. Optical Detector Technology

The key function of photo-detector for optical communication is to convert received optical signals into electrical forms, i.e. either voltage or current variations, for subsequent amplification and signal processing. The P-i-N photo detector consists of 3 layers: intrinsic layer 'i' sandwiched in between the 2 layer semiconductor n-type and p-type to enhance carrier generation by photon stimulation. Incident photons absorbed across the 'i' region would generate electron hole pairs (Figure 8). With voltage bias, these carriers are swept to the p and n regions and get recombined. As the result, the net current exists in the closed circuit. That's fundamentally how optical signal is converted into electrical current by a photo-detector.

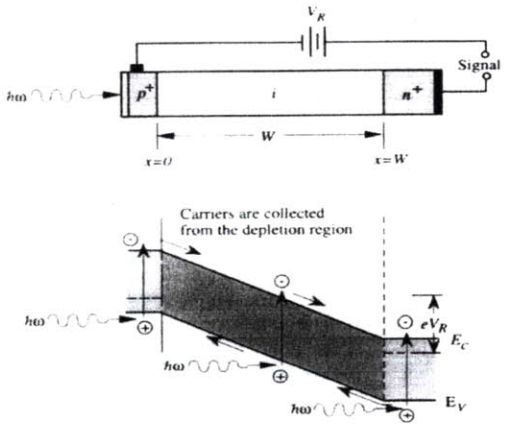

Figure 20: P-I-N photo detector.

Key Technology to Improve Responsiveness of Short-Range Detector by increasing Carrier Mobility:

With Ge on strained Si technique, modulation frequency up to 10GHz has been realized and especially the fabrication is compatible with existing CMOS infrastructure and supply chain. Research is uncovering a variety of way to utilize silicon platforms in receiver (detector) technology while hybridized mounted detectors have already been commercialized. Si itself is a rather poor absorber, i.e. its absorption depth is large, at most popular communication frequencies (λ>1μm). Short germanium absorption depths open the possibility of normal incidence coupled detector diodes, and the responsiveness of Ge extends into longer communication wavelengths especially under strain condition. Higher mobility of Ge allows even faster response.

Key question for silicon receivers is how to interface them to multi-mode fiber for normal incidence diode structures. Addition question for Ge is whether the intrinsic silicon lattice mismatch (4%) can be managed over noise [1].

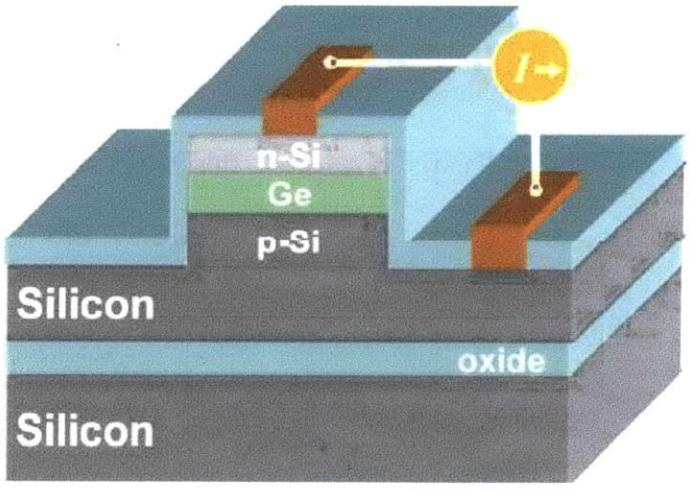

Figure 21: Structure for laterally-coupled germanium diodes [1].

c. Modulator Technology

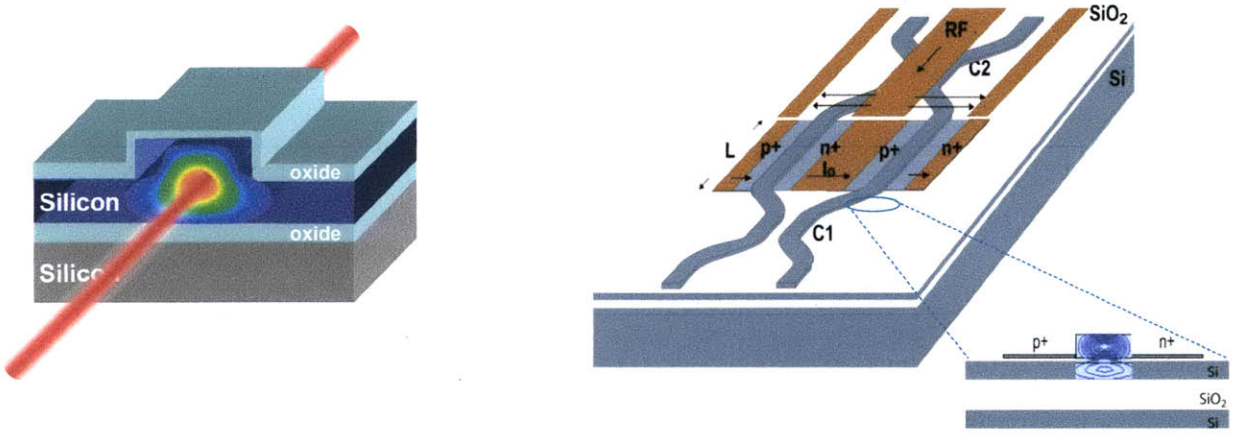

Figure 22: Optoelectronic modulator [courtesy MIT].

In silicon plasma modulator approach [1], silicon waveguide channel is flooded with carriers which alter the channel's refractive index. This variation of refractive index can be utilized in Mach-Zender interferometer structures to create light amplitude modulation. In other approach using electro-optic material such as barium titanate ($BaTiO_3$) for modulators, the materials deposited on a buffer layer of magnesium oxide have shown some compatibility with standard silicon processing techniques. In other modulator research regarding quantum well structures in materials, Si nanocrystals on SiO_2, for example, have shown electroluminescence and electro-absorption. Although still early in research, this is a possible solution for modulators as well as Si laser source.

Key remaining challenge for the current optoelectronic modulator technology is that Si plasma modulation and Si receiver are not likely compatible with each other. Plasma modulator probably needs Ge diode. Electro-optic materials like $BaTiO_3$ are still very much in question to be integrated with standard Si processing.

d. Packaging Technology

It is essential that all components discussed above would be able to be assembled into one highly small compact package. Package for discrete optical source or detector could be either ROSA or TOSA as shown in Figure 11. All of the components are finally put on same substrate and form the product. One of promising alternative technologies is parallel assembly which is ideal for VCSEL since light is emitted vertically [5].

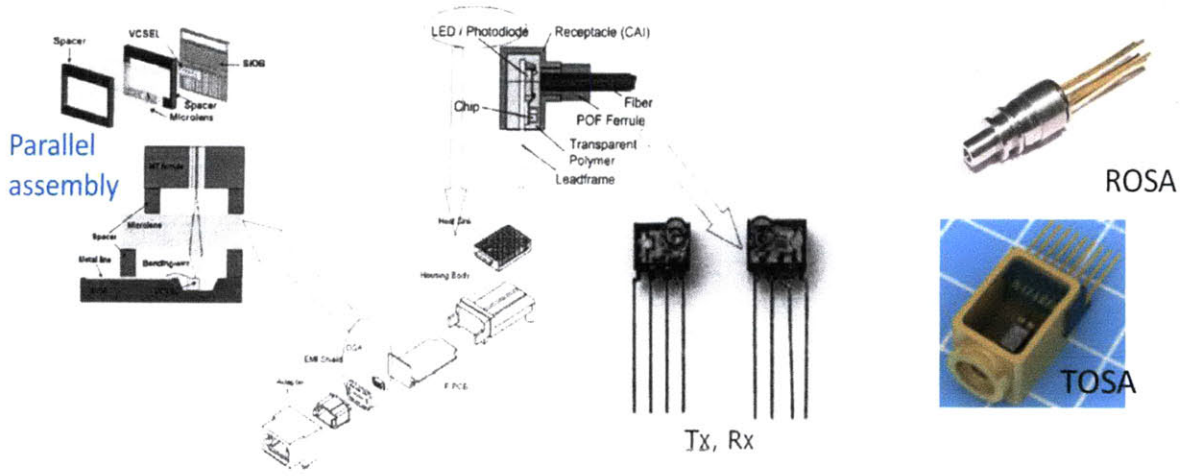

Figure 23: Packaging for optoelectronic transceiver.

e. Monolithic Integration Consideration for Optoelectronic Transceiver

It is the key for silicon microphotonics that devices are built entirely on the Si substrate which can be fabricated using traditional CMOS processing techniques. Monolithic LED has been realized so far. Results of current research on edge-emitting laser (EEL) and vertical cavity surface emitting laser (VCSEL) show that monolithic integration for these optoelectronic devices are highly promising.

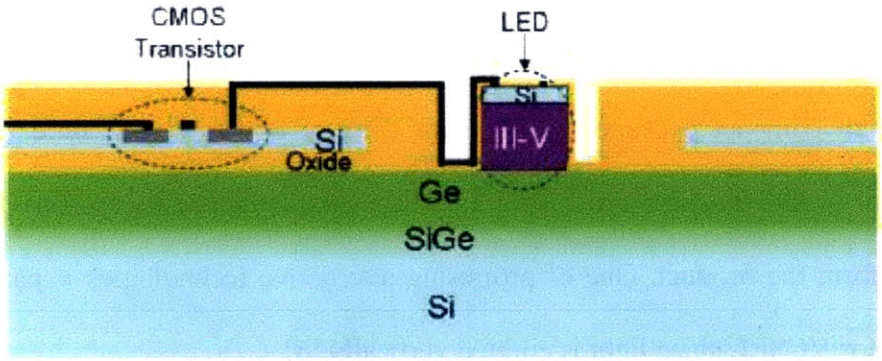

Figure 24: Monolithic LED on Si substrate with CMOS technology [6].

PART II

TERABIT/SECOND-CLASS INTER-CHIP PARALLEL OPTOELECTRONIC TRANSCEIVER

CHAPTER 1: Overview of the Terabus Transceiver

1. Background

In the context of current technology, interconnect bandwidth requirements within high-performance computing systems keep increasing. This common trend is driven strongly by the ever-increasing processor speeds, number of processors per system and wide data bus capacity. Parallel optical interconnect between different blocks of the same circuit board or inter-board through back plane is very promising in terms of data throughput, integration density, power consumption and loss optimization as well as latency. With optical interconnect, the constraint on communication link length is undeniably much more liberated in contrary to electrical (copper) counterpart. Parallel optical interconnects based on multimode fibers with total data rates in the range of 100 Gb/s have been increasingly utilized over the next few years or more for links between racks of servers or between boards over lengths from one meter up to hundreds of meters. The debate now is on when optical interconnect will penetrate further within the board for chip-to-chip communication. The competition between optics and copper-based electrical backplanes for on-board interconnects is comprehensive in terms of speed, power efficiency, form factor and, last but not least, cost especially in the light of the advance in high speed electrical interconnects [7], [8]. It is obvious that there exists a critical bandwidth-length product above which optics is favorable because of power consumption [9] and signal integrity.

The key discussion topic for developers now is which interconnect architectures would significantly benefit from the high bandwidth and high level of density that optical technologies have to offer.

2. Introduction of the Transceiver

As one of excellent optical interconnect architectures, the Terabit/second-class inter-chip parallel optoelectronic transceiver has been developed under the IBM Terabus project. A complete set of technologies [10] has been proposed and developed to support terabit/second inter-chip data transfers over organic cards within high-performance servers, switch routers, and other intensive computing systems. The transceiver architecture (Figure 13) comprises of a chip-like optoelectronic packaging structure (Optochip), assembled directly onto an organic card (Optocard). In order to reduce the size and boost up the speed, integration parallelism is utilized such that the data rate per line is pushed up to 20 Gb/s and the total number of channels in the bus is designed to be 48 (4x12), achieving the overall data transfers in the range of 0.5-1 Tb/s. The 4-by-12 arrays of 985-nm vertical-cavity surface emitting lasers (VCSELs) and photodiodes (PDs) are flip-chip bonded to the corresponding driver and receiver IC arrays which are implemented by 130-nm CMOS technology. These 2 IC arrays are in turn flip-chip assembled onto a 1.2-cm^2 silicon carrier to complete the transceiver Optochip. One thing needs to be clear here is that the latter flip-chip process is carried out first and then followed by the former due to ease of fabrication which will be discussed subsequently in details.

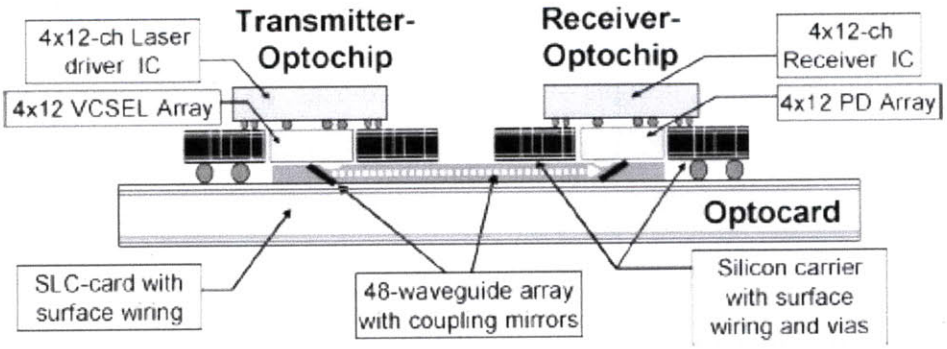

Figure 13: Schematic of Terabit/s package composed of Optocard with waveguides and transceiver Optochips [10].

The silicon carrier has electrical through vias, high speed wiring and the 1.5 mm x 4.2 mm rectangular cavity to house the VCSEL and PD arrays. This 1.2-cm^2-form-factor Optochip module aimed for low-power operation will transmit the data through a 62.5-μm-pitch array comprised of 48 parallel multimode optical waveguides patterned on the Optocard. A novel scheme for optical coupling between the Optochip and Optocard has been developed in which the optoelectronic (OE) arrays, which comprise of VCSELs and PDs, are backside emitting or illuminated through arrays of antireflection-coated micro-lenses etched onto the backside of the OE substrates. Right under the OE devices and inside the waveguides on the Optocard, 45°-tilted mirrors are subtly fabricated to creatively couple the light into and/or out of the array of waveguides (Figure 13).

Single channel has been demonstrated to operate up to 20 Gb/s for transmitter and 14 Gb/s for receiver. The per-channel power dissipation over multimode fiber is observed to be as low as 50 mW for 10-Gb/s single-channel links [10].

The Terabus project has been successful in designing the novel Terabit/s-class OE transceiver with prominent features: high bit rate, high level of channel density, which improved the device form factor, and low power consumption. Subsequently, to compete with purely electrical counterparts, highly reliable and cost-effective prototypes are essential. Therefore, the option criteria for electrical packaging, designs of IC and OE devices, waveguides and optical coupling are recommended as follow [10]:

- Utilization of flip-chip technology to reduce wire-bond parasitics.
- The choice of surface-laminar-circuitry (SLC) as an organic card for the Optocard to make use of high wiring density [11].

- Use of Si carrier interposer for Optochip packaging due to the through vias allow direct solder attachment of the Optochip and the Optocard and dense wiring connected to the ICs on top of the interposer [12].
- Use of CMOS ICs to optimize IC power efficiency and cost.
- Option of operating wavelength of 985 nm to allow simple optical design based upon the III-V GaAs/InP substrate and to permit direct integration of lenses onto the backside of the substrate [13].

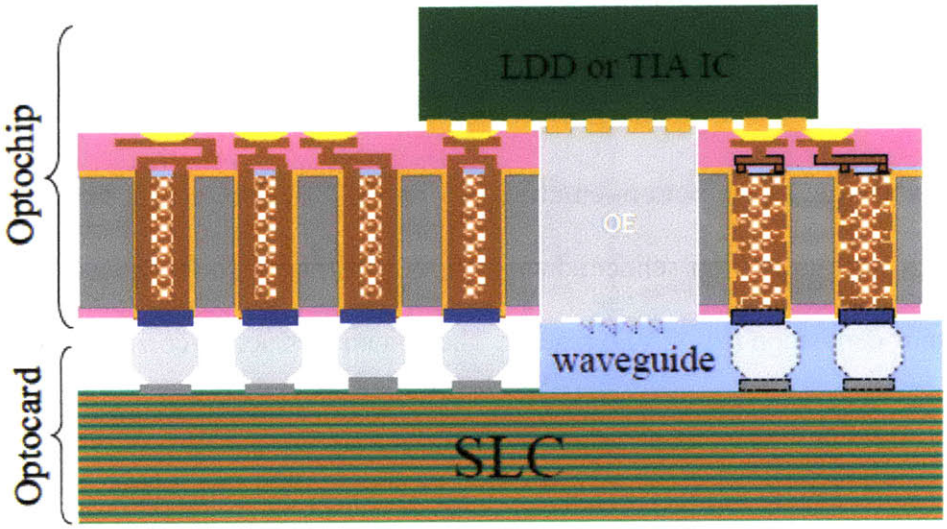

Figure 14: Structure of Terabus/second transceiver [14].

The subsequent sections will analyze the high-speed OE transceiver in details regarding: components and circuits; fabrication, alignment and packaging; as well as optical, electrical characterization, results and evaluation. The structure is as follow:

- 2-D arrays of VCSELs and PDs; CMOS transmitter driver circuits (TX) and receiver circuits (RX).
- Silicon carrier; Optocard; optical coupling and alignment; packaging.
- Results and evaluation: simulations and measurements.

CHAPTER 2: 2-D Arrays of VCSELs and Photodiodes

CMOS Transmitter Driver Circuits and Receiver Circuits

1. Vertical Cavity Surface Emitting Lasers

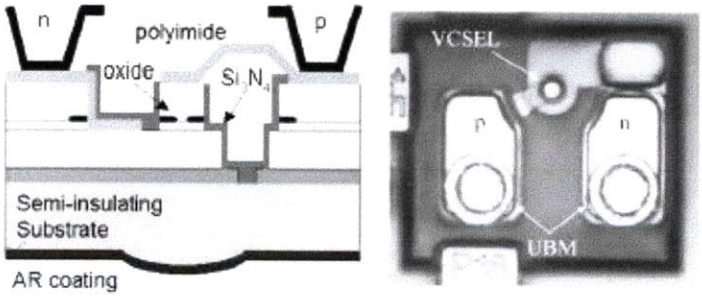

Figure 15: Schematic (left) and photograph (right) of bottom-emitting VCSEL [15].

The schematic of the bottom-emitting 985 nm VCSEL structure is shown in Figure 15. The structures were grown on semiconductor GaAs substrate with low-pressure metal-organic chemical vapor deposition (MOCVD) reactor. The epitaxial structure consists of 27.5 pairs of n-type GaAs/$Al_{0.9}Ga_{0.1}As$ bottom distributed Bragg reflector; 1-λ cavity with multiple quantum well active region and 40 pairs of p-type $Al_{0.1}Ga_{0.9}As/As_{0.95}Ga_{0.05}$ top distributed Bragg reflector [15]. The device have an oxide-confined structure which is optimized for low series resistance, low parasitics and high-speed operation at low current density while minimizing the excess free carrier loss to the device. The multiple quantum well active region contains three strained InGaAs/AlGaAs quantum wells and two thick graded AlGaAs layers to add up to the cavity thickness [15].

The VCSELs with apertures of 4, 6 and 8 μm are fabricated and optimized for 70^{o} – C operation [10]. An array comprised of 4x12 VCSELs is fabricated. The VCSELs with diameter of 4 μm and 6 μm have bandwidths all above 15 GHz and biasing currents of 2mA and 3mA

respectively [15]. All 48 VCSELs are identically modulated and each channel has extinction ratio above 6 dB.

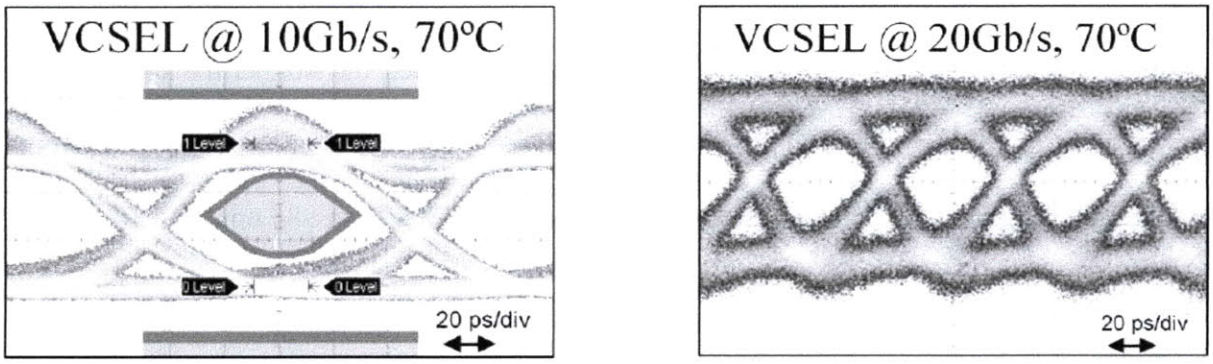

Figure 16: Enlarged eye diagrams of 6-μm VCSELs at 10 and 20 Gb/s (70° C) [15].

Figure 16 illustrates 10 Gb/s and 20 Gb/s eye diagrams of a 6 μm VCSELs operating at 70°C.

2. Photodiodes

Photodiodes with mesa structure are grown on Fe-doped InP substrate and are backside illuminated. The device responsivity is extremely sensitive to optical absorption in the p-InGaAs layer, requiring this layer to be as thin as possible. 4 sizes of 30, 40, 50 and 60 μm are fabricated for the 2-D 4x12-photodiode array. The frequency response is calculated from Fourier transform of impulse response measurements with 2-ps pulses at 985 nm.

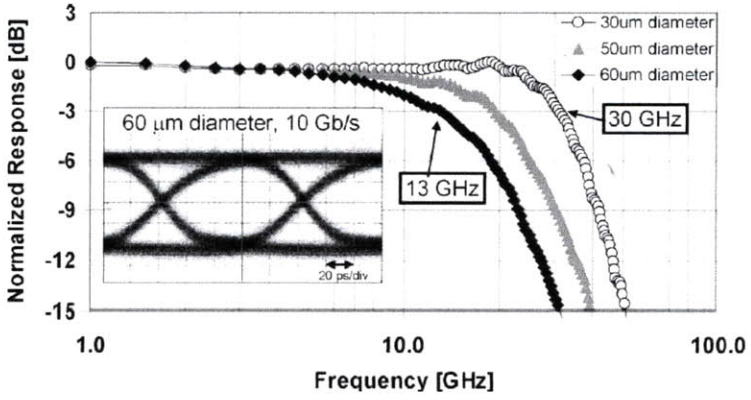

Figure 17: Frequency response of photodiodes with different diameters at 1.5-V reverse bias [10].

Figure 17 shows the inverse relationship between the 3-dB cutoff bandwidth and the diameter of the photodiode, i.e. the smaller the size, the larger the bandwidth, thus the better. At 1.5-V reverse biasing, 60-μm photodiode has 3-dB cutoff bandwidth of 13 GHz while 30-μm photodiode has the one of 30 GHz which is much larger. However, the smaller the size the better tolerance is required; therefore trade-off between bandwidth and tolerance needs to be taken into consideration. The photodiode responsivity is measured as 0.65 A/W at 985 nm [10].

3. CMOS IC Arrays of VCSEL Driver Circuits and Receiver Circuits

The laser diode driver (LDD) (TX) [16] and receiver (RX) [17] IC arrays were fabricated by IBM in standard 130 nm CMOS process. Both of the two chip arrays can be attached to a common silicon carrier and to identical electrical pad layouts of 3.9 mm x 2.3 mm footprint. The fact that Terabus packaging in which OE devices are flip-chip bonded to the corresponding IC circuit arrays has minimized parasitic factors due to direct and short electrical connection feature has facilitated significantly the performance of these IC arrays. Each array contains 48 amplifier elements and uses 2 voltage sources.

a. CMOS VCSEL Driver Circuits:

The LDD array comprised of 48 channels is powered by a 2 voltage sources, one of 1.8 V for the input amplifier circuit and the other of 3.3 V for output stage and bias. Figure 18 shows the structure of each driver circuit which comprises of a differential amplifier, a dc-coupled transconductance output amplifier to supply required modulation current to the VCSEL. The high-output-impedance transconductance amplifier requires less voltage headroom and provides more tolerance to laser series resistance variations. Last but not least, the output stage utilizes a fall time compensation circuit to improve the optical eye symmetry at high data rates.

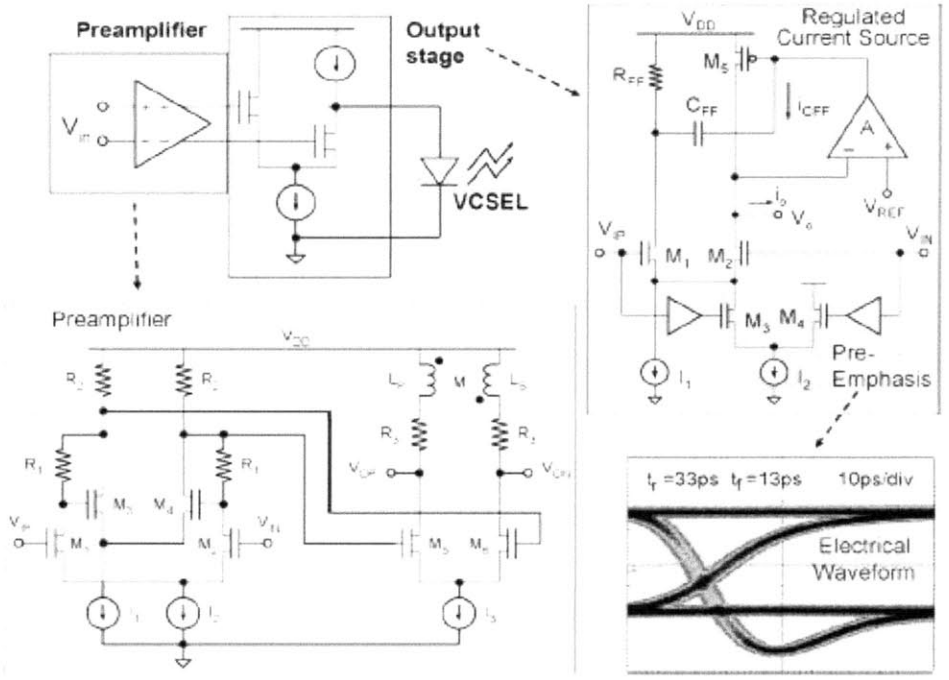

Figure 18: Functional block diagram of a single-channel VCSEL driver IC [16].

Two variations of the basic driver circuit were designed. A low-power design optimized for 10-Gb/s operation is capable of output modulation current swings of 5-6 mA. A high-speed version is capable of achieving data rates up to 20 Gb/s and supplying 11-mA modulation current [16].

b. CMOS Receiver Circuits:

The receiver array comprised of 48 channels is powered by dual 1.8-V supplies for amplifier circuits and a separate 1.5-3-V supply for the photodiode bias. Each receiver channel is structured by a low-noise differential transimpedance amplifier (TIA), a limiting amplifier (LA) and an output buffer as illustrated in Figure 19. TIA and LA circuits are designed to locate at the central region of the chip and fed by a common 1.8-V source. The output buffers, on the other hand, occupy the chip edges and are supplied by a separate 1.8-V source. This designed layout is

purposely to avoid switching noise from large signals at the outputs from interfering with the small signals fed to the inputs of the highly sensitive front-end circuits.

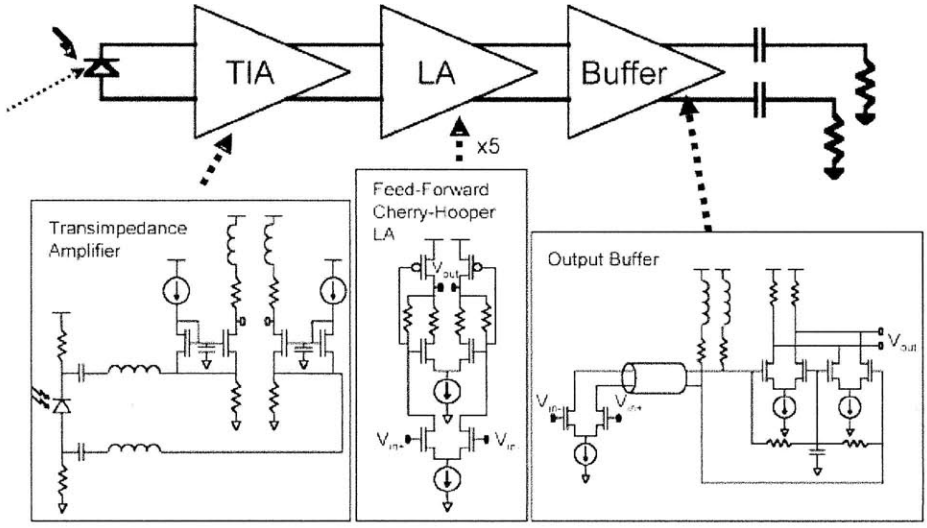

Figure 19: Functional block diagram of a single-channel receiver IC [18].

As indicated in Figure 19, the limiting amplifier (LA) comprises of 5 cascaded differential Cherry-Hopper gain stages with an offset cancellation feedback loop around the final four stages [18]. The gain of the receiver is 80 dB.Ω provided that there is 600-m Vpp differential output signal at the minimum input current of 30 μA.

CHAPTER 3: Silicon Carrier

Optochip Assembly, Optocard

Optical Coupling and Alignment, Packaging

Through vias, high-speed wiring and a through cavity to house the optoelectronic (OE) modules are prominent features of silicon carrier that allow high level of integration density of electrical and optical component on a single substrate to meet small-form-factor requirement for high bandwidth, high performance computing systems. The state-of-the-art set of fabrication, alignment and packaging techniques using eutectic AuSn and SnPb solder systems, integrated-relay-lenses configuration and flip-chip technology has been utilized to realize the transceiver prototype, thank for the maturity of semiconductor processing and packaging industries which has been leveraging high density, high speed parallel optoelectronics, facilitating manufacturability.

1. Silicon Carrier

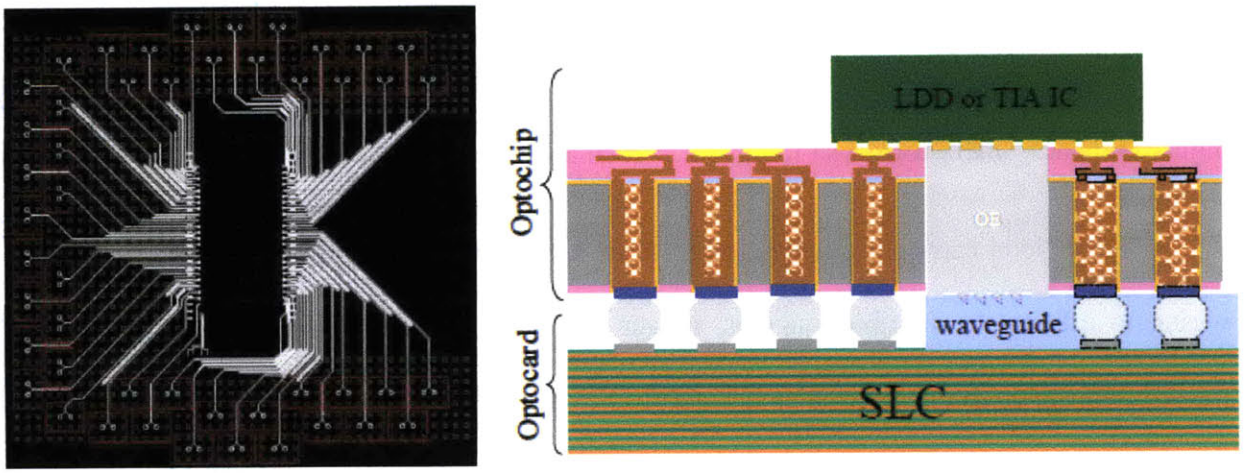

Figure 20: Top view of silicon carrier layout (left); structure of the transceiver (right).

a. Structure and Function:

Silicon carrier dimensioned 1.0 cm x 1.2 cm [10] is the basis for the Optochip packaging structure and assembled directly on top of the Optocard to complete the Terabit/second parallel transceiver. The silicon carrier provides a unique platform with fine pitch, high performance electrical interconnects and ability to integrate heterogeneous components including ICs and OE devices using cutting-edge flip-chip bonding technology [19]. The IC chips are flip-chip attached on top of the silicon carrier using fine-pitch eutectic AuSn solder. Electrical through vias allow transmitting signal and power from the Optocard up to the top surface of the silicon carrier. From that point, signal and power are fed into the ICs through high speed differential microstrip transmission lines patterned on top of the silicon carrier. A through rectangular cavity dimensioned 1.5 mm x 4.2 mm [10] is etched at the center of the silicon carrier to house the OE arrays. Significantly, this architecture effectively improves the optical coupling efficiency by minimizing the optical path length between the OE devices to the optical the waveguides structured on top of the Optocard beneath the silicon carrier, increasing module reliability as well as manufacturability by reducing the height of solder between the Optochip and the Optocard. The OE arrays are flip-chip attached to the IC arrays using eutectic AuSn solder while the silicon carrier is flip-chip attached to the Optocard beneath using eutectic SnPb solder. As the result, the highly compact, small–form-fact module has been achieved.

The silicon carrier is designed with three levels of back-end-of-the-line (BEOL) CMOS wiring to effectively distribute signals, power and ground. High speed differential microstrip transmission lines in charge of signal level (top most wiring) interconnect the IC bond pads on the silicon carrier to through-vias that connect to the Optocard. The top view of the silicon carrier is shown in Figure 20 (left) with the OE cavity cleared at the central region. Differential

microstrip transmission lines and through vias is also shown. The through vias for signal, power and ground are distributed on the three sides of the "C" shape (Figure 20) on the layout, freeing the remaining side to accommodate the Optocard waveguides that couple light between the OE devices.

b. Fabrication and Processing:

This section is to describe the process to fabricate silicon carrier with through vias, fine pitch wiring and through cavity. The robust process for fabricating electrical through vias is critical for the ability to transfer power and signals from top surface of the silicon carrier to the Optocard and vice versa. The fabrication of through-vias comprises of the following stages: via definition, sidewall insulation, via metallization, connection to terminals or surface wiring and through cavity creating and wafer thinning. The through vias are formed before adding fine pitch wiring and through cavity. The fabrication process flow is illustrated in Figure 21.

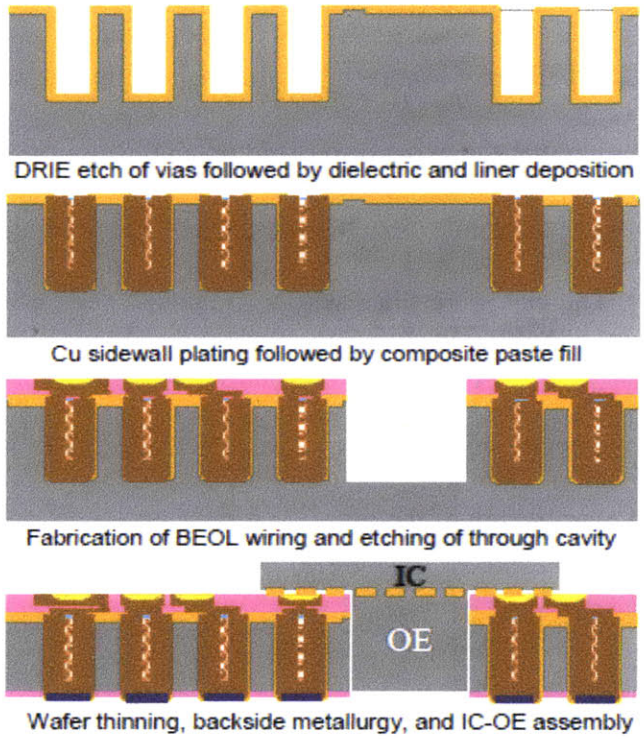

Figure 21: Silicon carrier process flow [14].

Silicon through vias are created using either wet or dry etch process. In this project [14], Bosch-typed deep reactive ion etch (DRIE) with a resist mask were used because of the advantage for alternating deposition and passivation steps to form through vias with smooth straight sidewalls. The vias are dimensioned as 70 μm in diameter with 225-μm pitch and 300 μm in depth, providing an aspect ratio greater than 4:1. After this etching process, the vias were insulated with thermal silicon dioxide (SiO_2) and low pressure chemical vapor deposition (LPCVD) of silicon nitride (Si_3N_4); the purpose is to conformally cover high aspect ratio features which could be done by other alternative methods such as plasma enhanced chemical vapor deposition (PECVD). Subsequently, the via sidewalls were coated with adhesion and diffusion barriers of TaN/Ta and Cu seed using physical vapor deposition (PVD). Coverage of metal coating on via sidewalls was observed to be continuous. Due to the appreciable difference of thermal expansion coefficients between Si-bulk and Cu, which are 3 ppm/°C and 16 ppm/°C respectively, the via sidewalls were then partially electroplated with Cu to accommodate for the thermal expansion of Cu which may occur during thermal cycling in subsequent CMOS process stages. Modeling has shown that the expansion could reach 0.5 μm or more in the case of fully – plated Cu via [14], which potentially results in cracking and fracture of silicon between the densely distributed vias. The vias were filled with a composite paste after excessive Cu had been washed out from the surface using chemical mechanical polishing (CMP). After that, the paste was taken out through sintering process steps to create strong, sealed structure such that BEOL wiring can be patterned over the top of the vias.

The 5-μm thick Cu collars are created around top portions of the deep vias (Figure 22) to provide electrical contact planes between the surface wiring and the through vias.

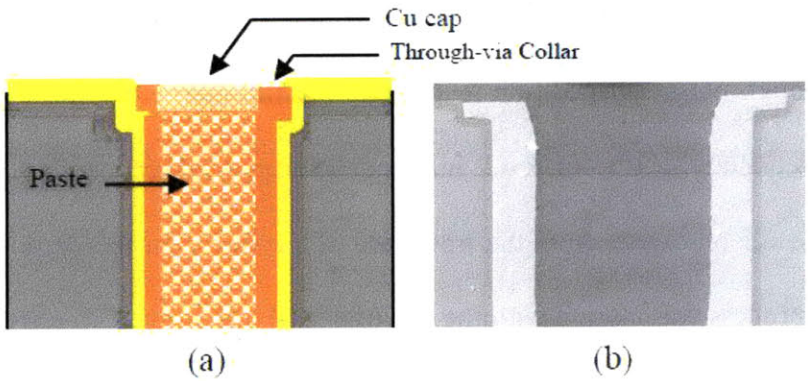

Figure 22: Cu collar for through via:

(a) Schemetic; (b) SEM cross-section of plated through via before paste is filled.

Silicon carrier has inherited the accomplishment of current and previous generations of silicon processing technology to achieve high level of wiring compactness. Figure 23 [14] shows the three levels of BEOL CMOS wiring where two patterned Cu planes (power and ground) extend below the impedance matching signal level and where each signal line is connected to the collar of a through via.

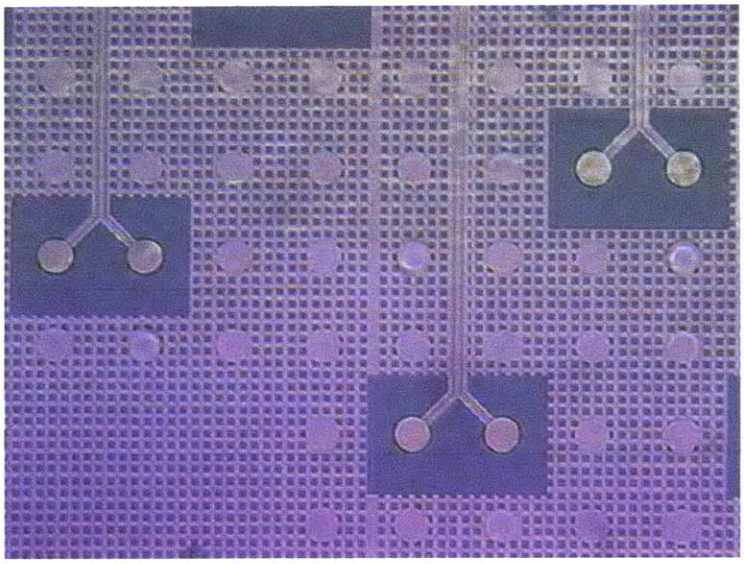

Figure 23: Top view of 3 wiring levels on top of silicon through vias: signal, power and ground [14].

Au bumps with 25 μm in diameter and 3-5 μm in height were created on top of the silicon carrier through plasma deposition to prepare for flip-chip attachment of the ICs to the surface of it. Subsequently, a 1.5 mm x 4.2 mm and 300 μm deep rectangular cavity was etched at the center of the silicon carrier from the front side of the wafer for the purpose of housing the OE module. This process was started with the use of a thick resist mask to pattern the cavity and the dielectric was cleared from the cavity region by the combination of highly selective oxide and nitride reactive ion etching. The cavity was etched up to the desired depth of 300 μm by Bosch-typed deep RIE. Eventually, the wafer was thinned from the backside using wafer grind and polishing process [14] to the desired thickness of 300 μm. Effectively, the previously blind vias and cavity now became the through features with the required thickness. Wet process etching using tetramethylammonium hydroxide (TMAH) was used to expose the through vias from the backside. PECVD oxide was deposited on the backside of the wafer to insulate the backside silicon. Subsequently, CMP was used to selectively remove the oxide out of the bottom surface of only the through vias for electrical connection to the Optocard.

2. Optochip Assembly, Optocard

a. Optochip Assembly:

This assembly process comprises of the following 4 steps which are in sequence:

- Flip-chip bonding of ICs to the silicon carrier
- Flip-chip bonding of the OE arrays to the corresponding IC arrays
- Underfill application
- Flip-chip bonding of the Optochip onto the Optocard.

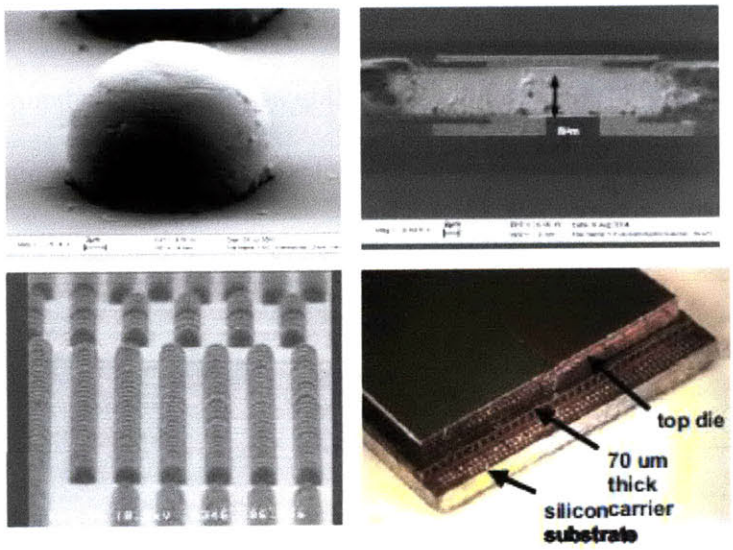

Figure 24: Solder micro bumps and array [20].

This hierarchical assembly procedure was started with flip-chip attachment of the ICs to the silicon carrier using eutectic AuSn (80% Au, 20% Sn) solder, followed by the flip-chip attachment of the OE arrays, which were now already assembled with the silicon carrier, to the corresponding IC arrays using the same soldering metal compound. Finally, the Optochip was attached to the Optocard using eutectic SnPb (63% Sn, 37% Pb) solder. Figure 24 illustrates examples of the solder micro bumps and an array used in flip-chip assembly process. The key point to note for this process is that the melting temperature of eutectic AuSn is 278°C during reflow[2] and greater than 400°C after reflow. This property allowed multiple level of attachment: the ICs were to be attached to the Si carrier first, after reflow the melting temperature of the AuSn solder joint has increased from 278°C to more than 400°C. Subsequently, the OE arrays were attached to the ICs while the ICs were still attached to the silicon carrier owing to the increase of the melting temperature after reflow. Figure 25 (left) describes well this particular sequence.

[2] *A process in which a solder paste is first used temporarily to attach one or several electrical components to contact pads; then the entire assembly is subjected to controlled heat, which melts the solder, permanently connecting the joint. Heating maybe carried out by reflow oven or infrared lamp or by soldering individual joints with a hot pencil.*

The attachment was carried out using flip-chip bonding tool of better than 2-µm alignment accuracy. The bottom view of the Optochip assembly with silicon carrier having under bump metallization (UBM) pads and through cavity together with ICs and OE devices in the cavity is shown in Figure 25 (right). The 4x12 lens array for optical coupling is also clearly seen.

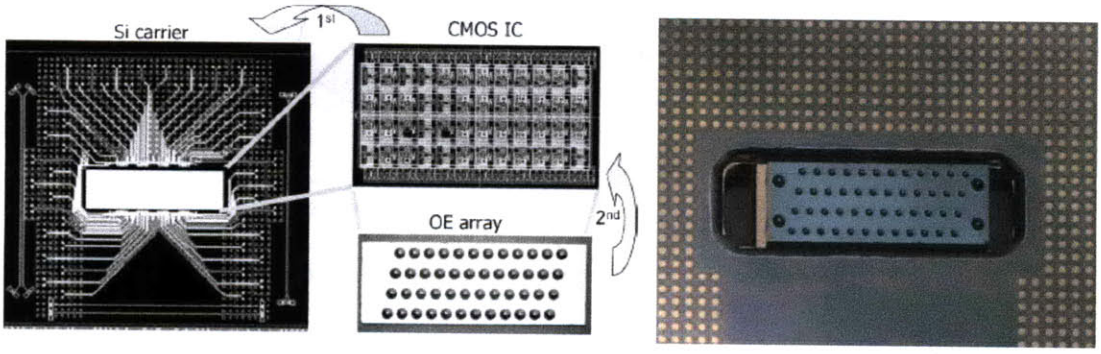

Figure 25: Flip-chip assembly procedure (left). Bottom view of Optochip: OE in cavity and UBM pads (right).

Shear tests were performed on ICs-silicon carrier as well as OE arrays-ICs flip-chip bonds. Average bond strength force of greater than 0.4 kg for the former and of greater than 1 kg for the latter has been observed.

b. Optocard:

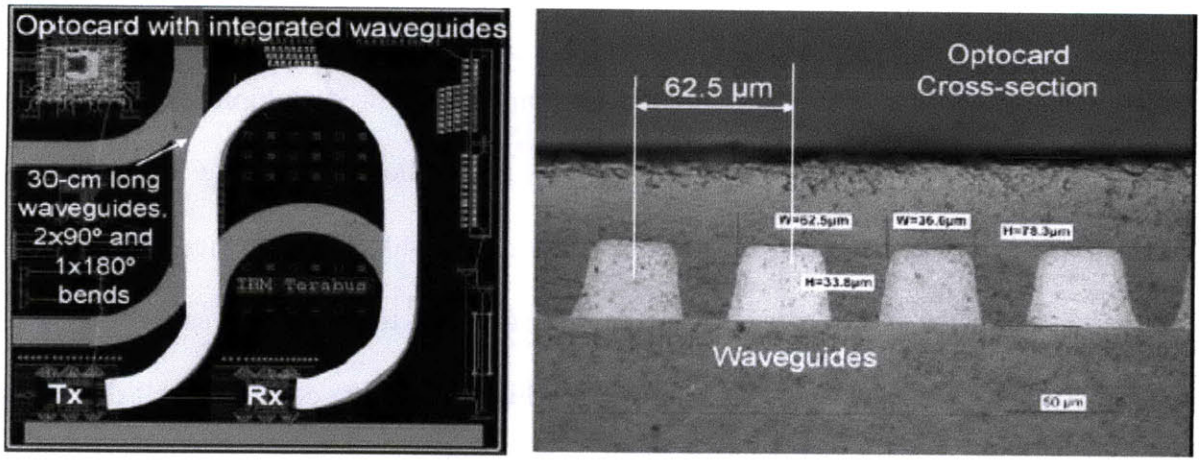

Figure 26: Layout of the Optocard (left) and cross-section with 62.5-µm-pitch integrated waveguides (right) (IBM).

The Optocard is a 15 cm x 15 cm printed circuit board made by surface laminar circuitry (SLC) technology. Figure 26 describes the top-view layout of the Optocard. The SLC has dielectric constant of 3.4 and loss tangent of 0.027. An acrylic layer is deposited on top of the SLC card by doctor blading[3], waveguides are patterned into the layer using photolithography with UV exposure through a contact mask [21]. After that, a solvent will be used to remove the unexposed regions. Lastly, the cladding-core-cladding stack is thermally baked to complete the cure. The Optocard has been patterned with 48 multimode waveguides cross-sectioned of 35 μm x 35 μm on a 62.5-μm pitch. The waveguide link (Figure 26) length is 30 cm, consisting of one 180° and two 90° bends with minimum bend radius of 28.5 mm, which has been proved to be free of bending loss since the required minimum bend radius is 25 mm.

3. Optical Coupling and Alignment, Packaging

a. Optical Couple and Alignment:

i. Optical Coupling Mechanism:

The transceiver has a novel coupling mechanism to guide the light emitted from the VCSELs to the photodiodes. The mechanism consists of the two 4x12 arrays of relay lenses. Each of these arrays is fabricated right on the back surface of the GaAs/InP substrate and exactly aligned to each of the VCSEL and photodiode arrays.

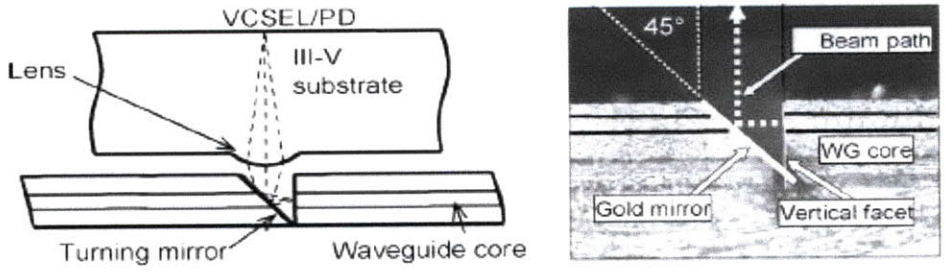

Figure 27: Optical coupling mechanism between OEs and the Optocard waveguides.

[3] *A common tape-casting method in which a ceramic powder slurry, containing an organic solvent such as ethanol and various other additives (e.g., polymer binder), is continuously cast onto a moving carrier... [Encyclopedia Britannica].*

As illustrated in Figure 27, the lens images the laser/photodiode active region onto the waveguide core. The coupling mechanism also includes 45°-tilt mirrors to bend the light perpendicularly from the output of the lasers into the waveguide core and out of the waveguide core into the input of the photodiodes. The mirror surface is coated with a layer of gold to maintain high reflectivity. An optical underfill medium of index 1.5 which is comparable to the waveguide material was used to couple the OE lens surface to the one of the waveguide. According to optical modeling, a lens with radius of curvature of 110-120 μm and conic constant of -2 (hyperbolic) in the GaAs/InP surface is proved to provide efficient coupling to the 35 μm x 35 μm waveguide core.

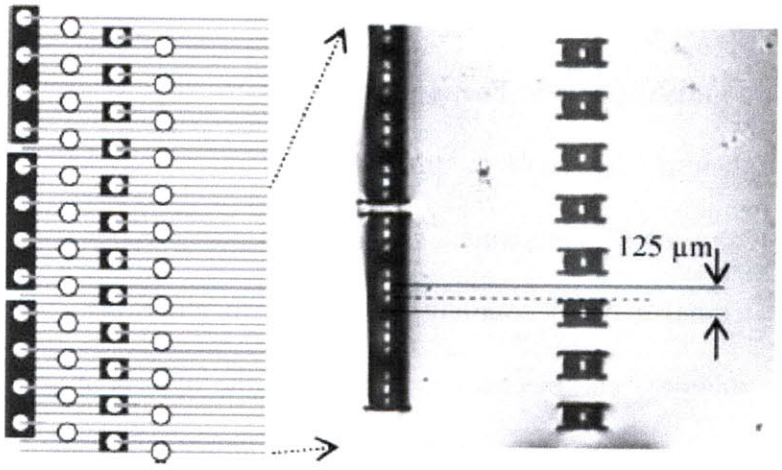

Figure 28: Schematic diagram of mirror fabrication at the end of 48 Optocard waveguides (left). Photograph of fabricated sample illuminated by a white light (right).

Figure 28 (left) shows a schematic diagram of the 48 Optocard waveguides patterned on a pitch of 62.5 μm. The waveguides are arranged by a staggered 4x12 array of OEs. The mirrors in the outermost (left) row are ablated as three long mirrors for manufacturability. Each long mirror couples light between four waveguides and four OE devices in the first row of the Optochip. The smaller mirrors in the third row have the width of approximately 125 μm on a pitch of 250 μm. This layout allows light to be coupled at 125-μm spacing instead of 62.5 μm spacing, which

makes the fabrication much easier. As illustrated in Figure 28 (right), the mirrors are tested with a white light illumination. Some light is leaking through the neighboring channels of the illuminated channel in the large mirror due to the individual mirrors of row three only partially extend over the neighboring waveguides, allowing some light through to the row with large mirror. The laser-ablation process is now under refining to allow fabrication of smaller mirrors at 62.5-μm spacing.

ii. Study for Tolerance of Optical Alignment:

The investigation has been carried out on the sensitivity of the optical coupling efficiency to the mechanical alignment offsets of the relative position of a prototype Optochip to waveguides on prototype Optocard. 980-nm VCSEL and 60-μm-diameter photodiode were used.

By both simulation modeling and measurement, the sensitivity along the optical axis (z-axis) for VCSELs showed optimal coupling at lens-to-waveguide-core separation of 190 μm with large and achievable tolerance of approximate ± 50 μm.

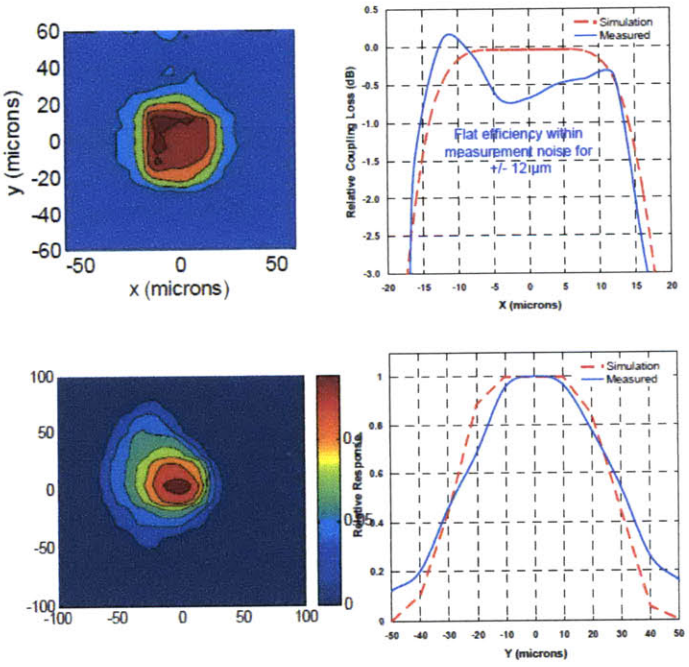

Figure 29: Coupling efficiency of VCSEL (up) and Photodiode (down) to waveguide vs. horizontal offset (x-y) [14].

The dependence on x-y (horizontal) alignment is more critical. Figure 29 (left) shows the contour plots with magnitude in color notation of the coupling efficiency dependence on the horizontal offsets. Figure 29 (right), for VCSEL-waveguide case (up), shows nearly constant coupling efficiency for the offset of ± 12 μm. For photodiode-waveguide case (Figure 29-down), the tolerance of ±10 μm has been realized. As clearly observed, the results obtained from prototype measurement (in blue) and simulation modeling (in dotted red) are in good agreement.

In conclusion, the system mechanical tolerance of budget of ±10 μm has been realized. Therefore, the state-of-the-art flip-chip alignment tools have sufficient accuracy budget (better than ±2 μm) to satisfy the tolerance requirement.

b. Packaging:

i. Optochip-to-Optocard Packaging:

This part is in continuation with section 2: "Optochip Assembly, Optocard" of this chapter.

Before attaching the Optochip to the Optocard, the eutectic solder: SnPb (63% Sn, 37% Pb) is transferred onto the Optocard using injection-molded solder (IMS) technique [22]. Using IMS technique, the solder is deposited in the "C" shape on the Optocard around the waveguide mirror [10]. The IMS process provides the solder columns with approximately 200-μm height which is adequate clearance for Optochip over the 150-μm height of waveguide. Solder height correction is performed during the final attachment in which different temperature between the Optochip and the Optocard are utilized. A shear strength greater than 10 kg is achieved for the flip-chip Optochip-Optocard bonding. In flip-chip bonding, only passive alignment is allowed, as the result, the key constraint here is that the OE chip must be in be visible with the waveguide during the assembly, i.e. features on the OE devices are to directly contact features on the

waveguides. The top-view of the entire Optochip-to-Optocard assembly is shown in Figure 30 (left).

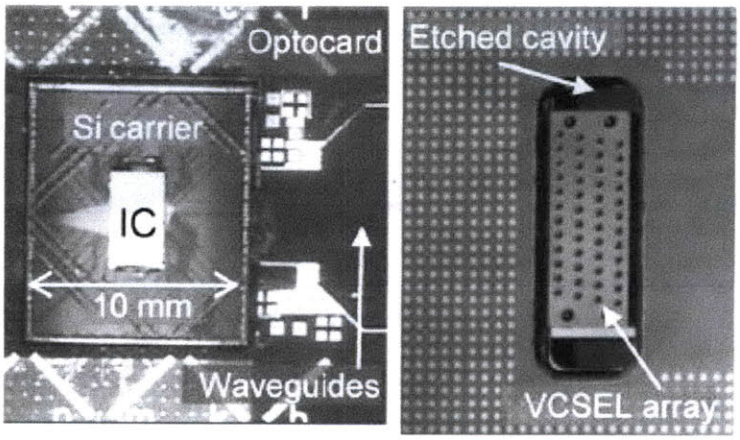

Figure 30: Entire Optochip-on-Optocard assembly (left) and bottom view of silicon carrier (right)

ii. Thermal-Control Consideration for the Package:

Figure 31: 3mm heat pipe in contact with test chip [23].

Due to high level of integration, thermal control is the critical issue for the Terabus package. Especially in high-speed operation, temperature control is essential to ensure satisfactory lifetime of the OE device. The VCSEL threshold current has strong dependence on temperature and so does the photodiode leakage current. There are some critical design requirements. First, the Terabus structure is optimized to operate at 70°C.

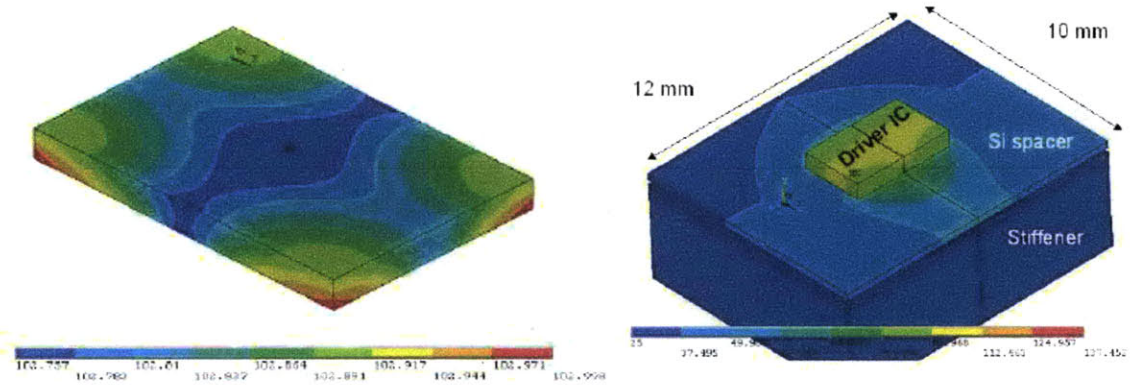

Figure 32 a : Temperature distribution in test chip with no cooling (left) and result for temperature distribution in the entire package (right) [23].

Second, the ICs are operating at low power where 100 mW per channel has been target in the initial phase. Based on the thermal simulations of the entire package (Figure 32a), an additional cooling system has been recommended to cope with a heat flux of up to 60 W/cm^2 [23]. As illustrated in Figure 31, the heat pipe is put in contact with the IC backside for cooling in evaluation phase of the package.

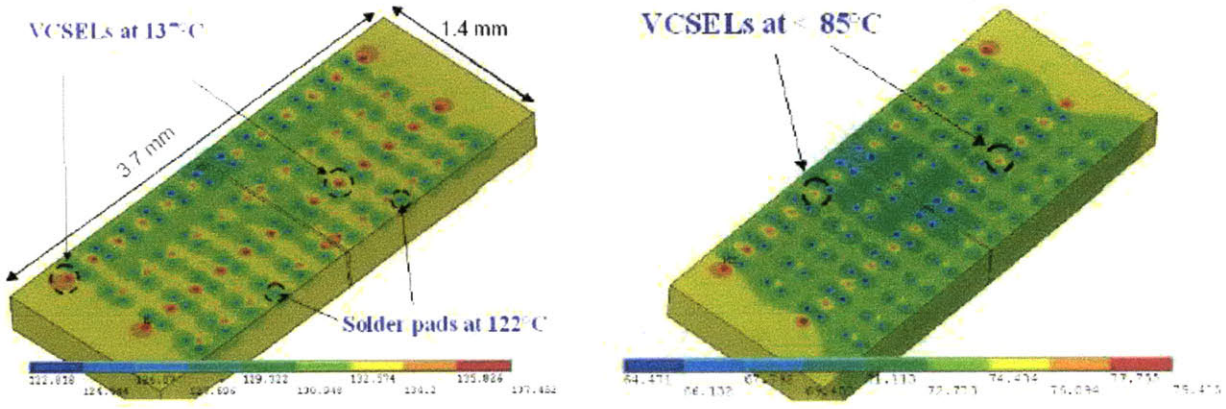

Figure 32 b: Local temperature distribution in the VCSEL chip with no cooling (left) and with heat pipe cooling (right) [23].

Figure 32 b illustrates the effect of the cooling mechanism (the heat pipe) on the thermal map of the VCSEL array. The temperature has significantly reduced throughout the chip with the pipe attached on top.

CHAPTER 4: Results and Evaluation

1. Measurements of Silicon Carrier Electrical Signal Path

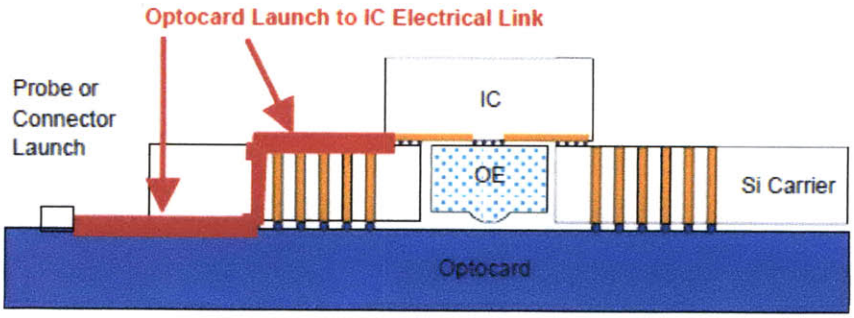

Figure 33: Electrical path (in red) on silicon carrier: strip line on the Optocard and silicon carrier through via, microstrip line [14].

The Silicon carrier electrical path as illustrated in Figure 33 (in red) mainly includes a 7-mm differential microstrip line on silicon carrier, a 0.3-mm differential silicon carrier through via and a 7-mm differential strip line on the Optocard. The link has been characterized up to 20 GHz.

The 7-mm strip line on the Optocard shows about 1.3-dB loss at 20 GHz excitation while the 7-mm microstrip line on silicon carrier shows approximately 3 dB-loss and the through via reveals 0.6-0.9 GHz dB-loss at the same frequency condition. With additional probing loss factors included, measured data shows that the entire link has 5-dB loss at 20 GHz and the 3-dB cutoff was reached at around 10 GHz [14].

a. Measurement of Differential Microstrip Lines on Silicon carrier:

Figure 34 (left) shows the cross section with dimensions of a differential microstrip line on the silicon carrier which will be characterized in time as well as frequency domain using GSSG microprobes. The eye diagram[4] plotted for the 7-mm microstrip line is shown in Figure 34 (right). Since the eye pattern is observed to be "open", the line is qualified for 20-GHz operation.

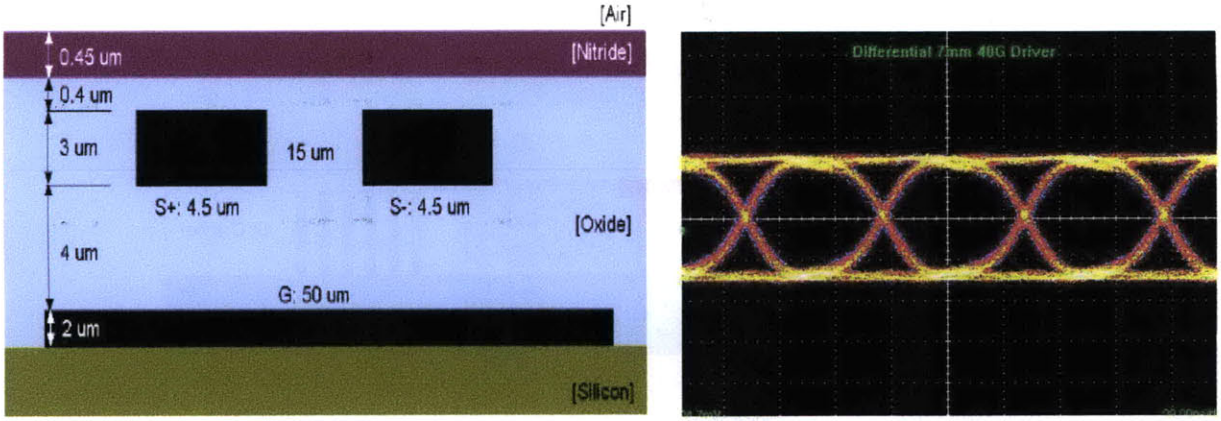

Figure 34: Layer dimensions of differential microstrip transmission lines on the silicon carrier (left) and its eye diagram (right) for 7-mm length at 20 GHz, PRBS 7-1 data pattern [14].

A vector network analyzer is used to characterize the performance of the microstrip line in frequency domain. The calibration was set up using a reference substrate and the short-open-load-through (SOLT) technique. The vector network analyzer will measure the S-parameters of the line to obtain both reflection coefficient (S_{11}) and transmission coefficient (S_{12}). The results obtained were coupled with the effect of probe launches and impedance mismatch between the measured microstrip line and the 100Ω reference impedance of the vector network analyzer. Figure 35 plots out the dependence of the transmission (blue) coefficient and the reflection coefficient (red) of the 7-mm line on various operating frequencies, both are presented in dB.

[4] *In telecommunication, an eye pattern, also known as an eye diagram, is an oscilloscope display in which a digital data signal from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails.*

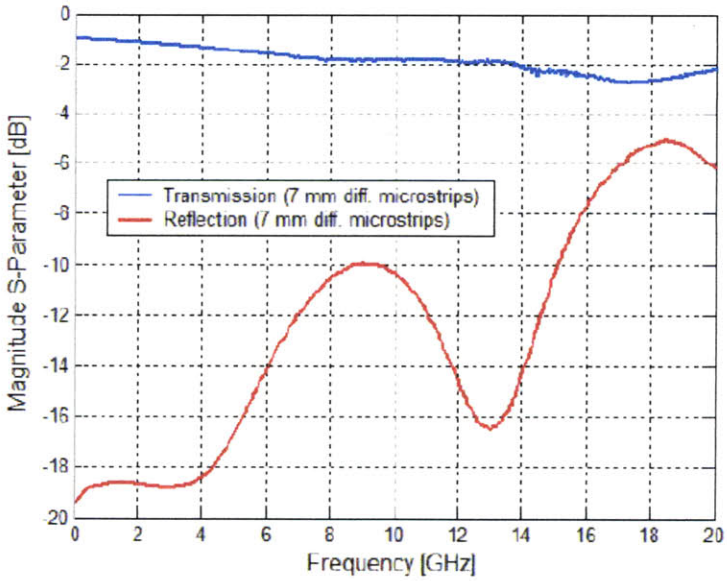

Figure 35: S-Parameters (S_{11} and S_{12}) of the 7-mm silicon carrier microstrip line.

From the plot, the measured insertion loss for the microstrip lines is approximately 2.2 dB at 20 GHz. In addition, from the S-parameters data obtained above, the attenuation of the line can be extrapolated using the T-parameters method proposed in [24] and with the aid of IE3D[5]. Results show that the extrapolated attenuation constant is 4.3 dB/cm at 20 GHz corresponding to 3-dB insertion loss of the line assuming it is ideally matched and the length is 7 mm [14].

b. Measurement of Differential Silicon Carrier Through Via:

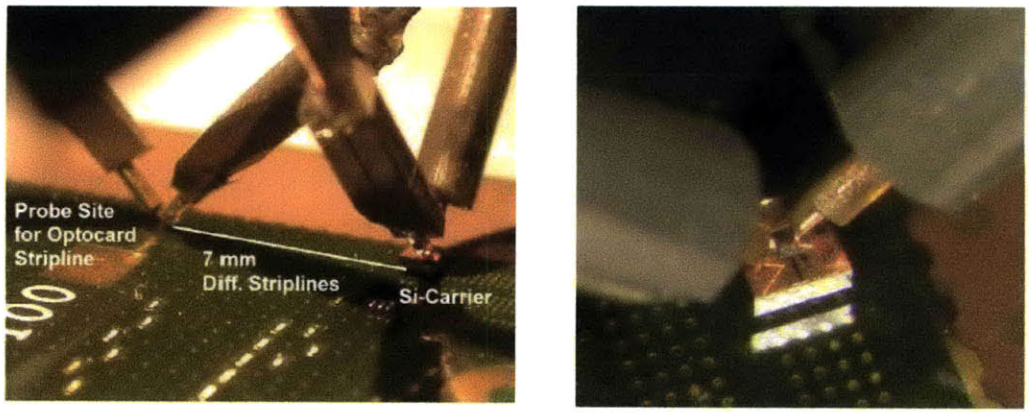

Figure 36: Measurement setup for silicon carrier through via transmission [14].

[5] *An antenna and microwave simulation software developed by Zeland Inc.*

Figure 36 illustrates the measurement setup for probing the transmission of the silicon carrier through-via. The SOLT calibration technique using a reference substrate has been used. The measurement method is as described follow: first, the transmission of the system comprised of the silicon carrier through via and the 7-mm line on the Optocard has been obtained; second, the transmission of the 7-mm reference line on the Optocard has also been obtained. The deference of these two above transmissions indeed represents the upper limit (worst case) of the transmission for the silicon carrier through via since other loss and parasitic factors may be incorporated without using the reference line. The measurement of the two transmissions is plotted out in Figure 37.

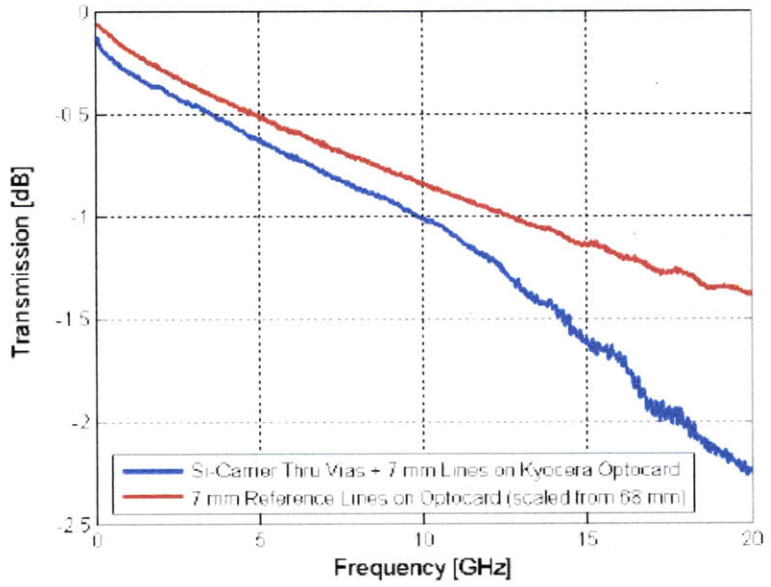

Figure 37: Transmissions of the through via + the 7-mm Optocard line (red) and of the reference Optocard line only (blue).

At operating frequency of 20 GHz, the transmission of the system of through via and line is recorded as –2.25 dB while the transmission of the reference line is approximately -1.4 dB. Therefore, effectively, the transmission of the through via can be deduced approximately as -0.85 dB (since: 2.25 – 1.4 = 0.85). Since this result describes the worst-case scenario, the performance of the silicon carrier through via is expected to be better.

2. Measurement of Optocard Waveguide for Loss and Dispersion

a. Optocard Waveguide Loss Measurements:

To measure the loss of the waveguides on top of the Optocard, a 30-cm multi-bent acrylate waveguides fabricated on a surface-laminar-circuitry (SLC) substrate has been used as a sample. The gold-coated mirrors are fabricated at either ends of the waveguide to couple the laser light at 90° in and out the waveguide [10]. The calibration setup for the mirrors is performed by using a reference 2-cm waveguide system. The 2-D mirror array allows access to 24 waveguides on a125-μm pitch. 980-nm continuous laser light is coupled into a single-mode fiber and imaged into the core of the waveguide. A large-area photo-detector is used to measure the light at the output.

The loss on average of the system is recorded as -4.8 dB, with a best channel loss of -3 dB which is corresponding to an average of 0.16 dB/cm and a loss of 0.1 dB/cm for the best case [10].

b. Optocard Waveguide Dispersion Measurements:

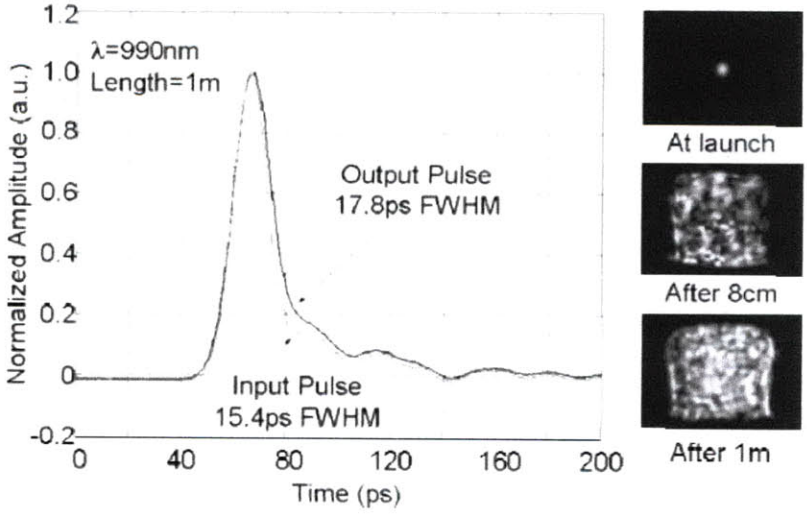

Figure 38: Impulse response measurement of a 1-m multi-mode polymer optical waveguide at input and output (left). Evolution of Images of the single-mode fiber launch into the waveguide due to dispersion (left) [26].

To investigate the modal dispersion of the waveguides, 2-pico-second short pulse is propagated from a Ti:Sapphire laser at 990 nm through waveguides of different lengths [25]. The input and output pulses are measured with a 14-GHz photodiode on a high-speed sample scope. The impulse responses before and after propagation through a 1-m multi-mode waveguide are shown in Figure 38. The pulse broadening evolution is shown at the right of Figure 38, i.e. the initial stop-sized pulse is getting dispersed and broadens as it travels through the waveguide, the longer the length the worse the dispersion.

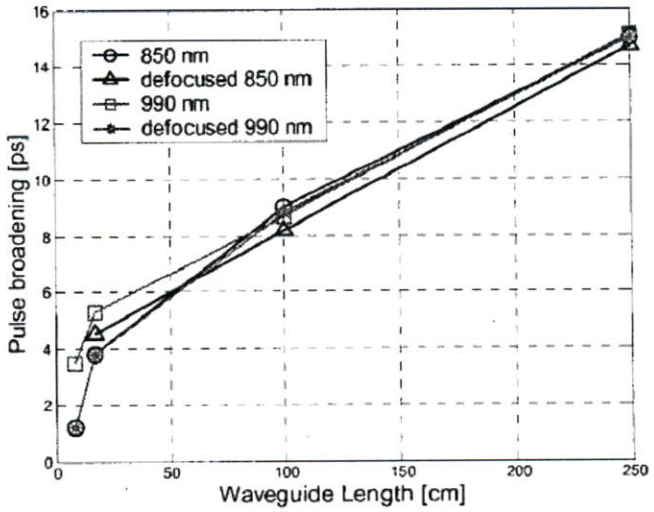

Figure 39: Summary of pulse broadening results for 8, 17, 100 and 255-cm waveguides for both 850 nm and 990 nm [25].

The dependence of pulse broadening on the waveguide lengths for the two wavelengths of 850 nm and 990 nm is illustrated in Figure 39 plots which are produced by deconvoluting the response of the photodiode and the sampling head [25]. The transfer function of different waveguide lengths can be deduced by a fast Fourier transform of the impulse responses [10]. The result shows that for links shorter than 1 m, dispersion will not be appreciable for operation at 40 Gb/s and below. For link 2.5 m long, the 3-dB bandwidth limitation caused by model dispersion decreases to 23 GHz compared to 50 GHz and 39 GHz for the 0.3-m and 1-m long, respectively.

It is useful to note that in organic waveguide, e.g. acrylate, the loss due to factors other than dispersion is significant because of the relatively high intrinsic absorption of this organic medium around 985 nm. Further advance in material technology is necessary for waveguide more than 1m long to perform multi-gigabit/s communication at this wavelength.

3. Optochip Characterization

High-speed testing at the Optochip level is carried out by wire-bonding the Optochips onto a printed circuit card with a cavity in the middle. It is possible to either turns on all 48 channels at the same time or just 6 channels each. The Optochip is characterized by connecting the transmitter and the receiver channels over a 5-m-long 50-μm multi-mode fiber (MMF) link [10]. Photodiode detectors with 30-μm diameter have been used in all experiment since the capability the handle high frequency.

For the Transmitter Optochips, error-free (BER < 10^{-12}) [6] operation at 20 GHz has been measured [16] using a reference receiver. Figure 40 illustrates the corresponding eye diagram.

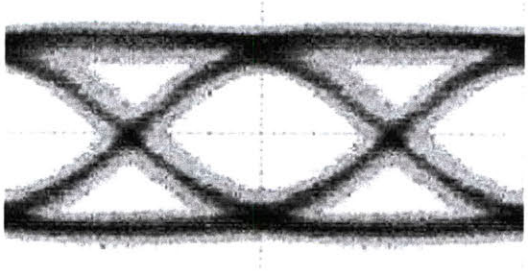

Figure 40: Eye diagram at 20 Gb/s from a Terabus transmitter. The drive circuit included a circuit to compensate for the fall time of the VCSEL emission [26].

[6] *BER (Bit error rate) is the number of received bits that have been altered due to noise, interference and distortion, divided by the total number of transferred bits during a studied time interval.*

The results [26] have shown that these are the fastest directly-modulated VCSEL transmitters with CMOS drivers demonstrated to-date.

For a complete Optochip multi-mode fiber link (from the transmitter Tx Optochip to the receiver Rx Optochip), Figure 41 describes that error free (BER < 10^{-12}) operation has been measured at 14Gb/s with power consumption of 130 mW.

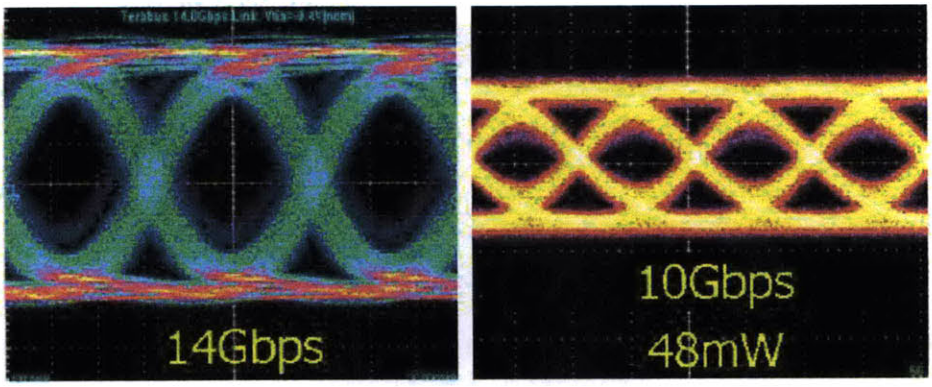

Figure 41: Received eye diagram of a transmitter Optochip to receiver link at 14 Gb/s (left). 10 Gb/s received eye diagram using low power variant circuits and reduced supply voltages [26].

Using variant circuits designed for low power operation and reduced supply voltages, a 48 mW (22mW for transmitter Optochip and 26 mW for receiver Optochip) link was found to be capable of error-free operating at 10 Gb/s.

Crosstalk consideration:

A frequency-domain crosstalk consideration of the transmitter is carried out by modulating one aggressor channel which is in turn excited with data rates of 10, 15, and 20 Gb/s and observing the optical output of adjacent channels with a fiber probe. The optical outputs of the aggressor and the neighboring victim channels are observed with a fast photodiode connected

to an 18 –GHz spectrum analyzer. The single-channel crosstalk below 40 dB with operation frequencies up to 18 GHz has been realized. In high-level integrated parallel receivers, cross channel crosstalk might result in power penalty [10] which can be a consequence of either imperfect optical coupling due to improper alignment between waveguides and the OEs or on-chip crosstalk between electrical signal lines or the substrate itself. Thus, optical coupling and alignment is critical to mitigate the effect of crosstalk. Last but not least, in order to reduce crosstalk, the high-speed on-chip transmission lines are needed to be shielded and each receiver channel is recommended to be decoupled by added capacitors [27].

Power consumption budgeting consideration:

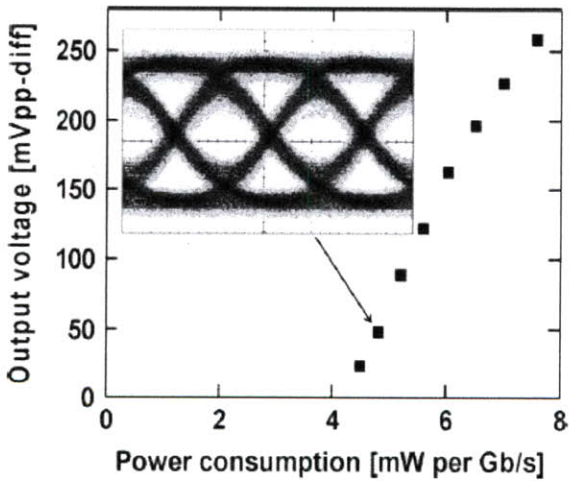

Figure 42: Power consumption per bit rate for a single-channel 10-Gb/s error-free multi-mode fiber link. Inset: received eye of the 48 mW (22 mW for transmitter and 26 mW for receiver) link. [10]

Essentially, the transmitter power consumption depends on a the optical output power of the VCSELs necessary to compensate for the link loss which is obviously higher in transmission over waveguide than over fiber. On the other hand, the receiver power consumption strong depends on the output voltage swing that is required to drive the receiver Optochip as well as the

electrical interface. Consequently, link suffered from higher transmission loss and/or higher required output voltages is to be supplied with larger power. Effectively, to meet low-power operation criteria, loss has to be carefully investigated and minimized. The power budget has to account for coupling and mirror losses, transmission loss due to intrinsic attenuation of the medium material within the waveguide link and also for power penalty for noise and crosstalk at transmitters and receivers.

PART III

MARKET OPPORTUNITY

CHAPTER 1: Market Analysis

1. The Supercomputing Market

The Terabit/second-class inter-chip parallel optoelectronic transceiver has been developed to support high-speed data transmission for supercomputing systems. Processing speeds of fastest computer systems increase exponentially with time and have direct proportionality to the evolution of circuit integration density which is ruled by the widely-known Moore's law. Figure 1 has explained well this fact[7].

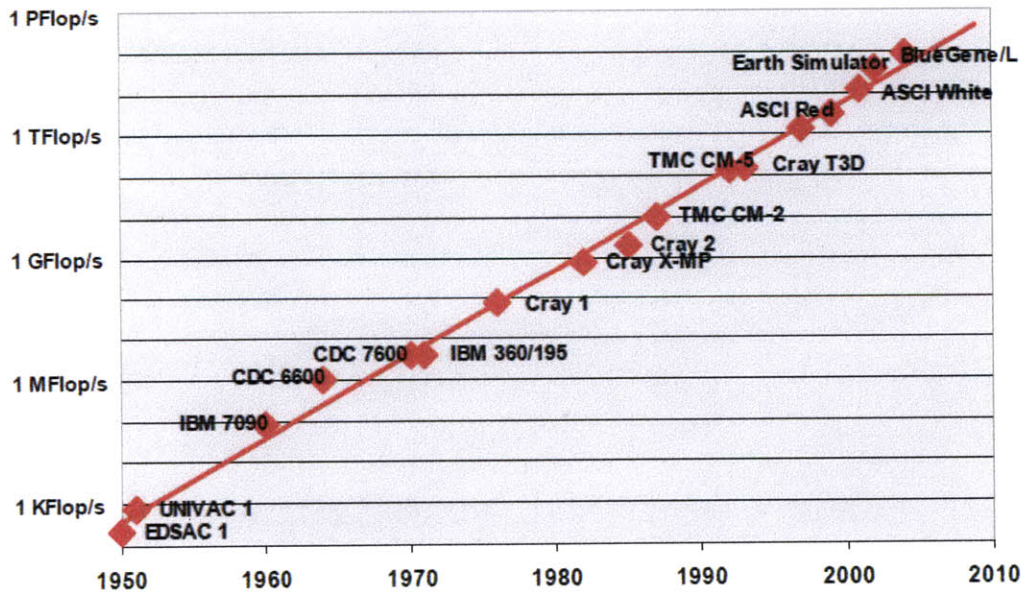

Figure 43: Performance of the fastes computer systems for the last six decades compared to Moore's law [28].

[7] *Flop/s: Floating point operation per second, a performance measurement of a computer system which makes heavily use of floating point calculations, similar to the older measure instructions per second.*

At present, IBM and HP control 80% of the supercomputing market [29]; however, smaller players are trying to gain market share in the near future due to the rising demand towards high-performance computing (HPC) installations in Europe. Figure 44 illustrates the major supercomputing manufacturers and their corresponding active market time intervals [28].

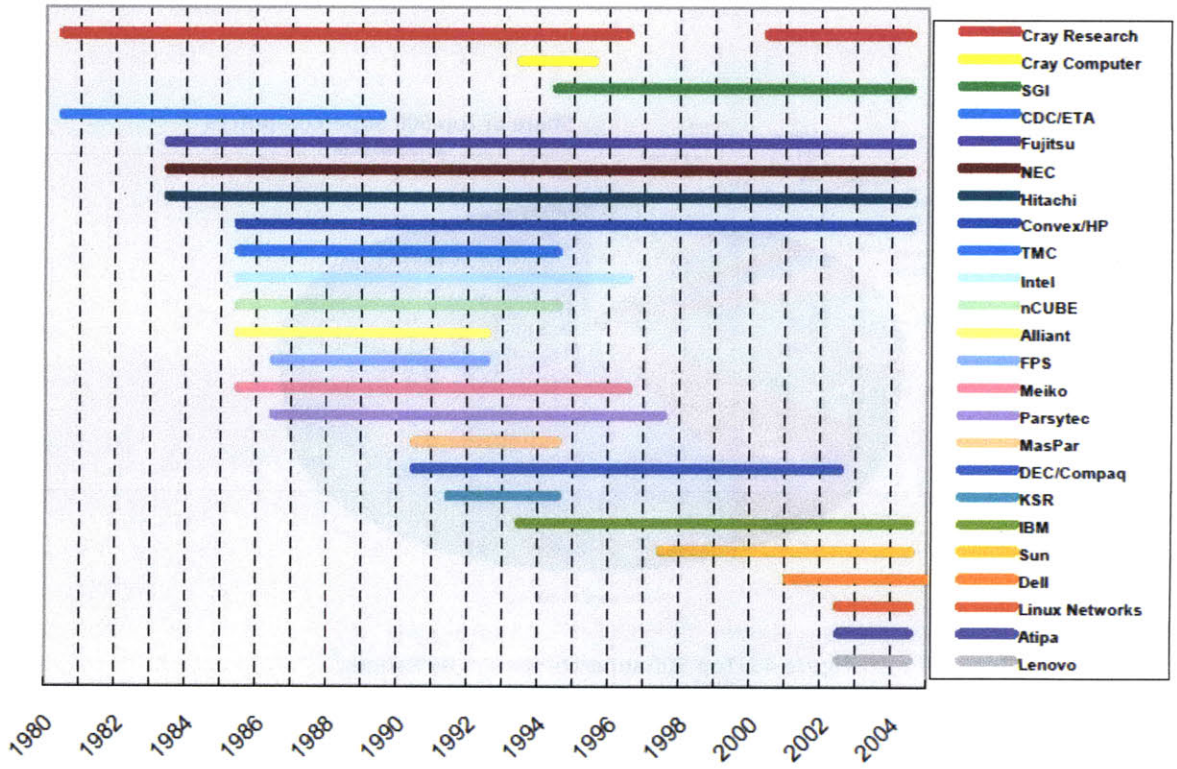

Figure 44: Main active players in high performance computing market throughout time [28].

At the beginning of this year (2010), Fujitsu declared to boost up its supercomputer share from 2.2% now to 10% within the next 5 years. The world market for high performance computers, including machines that cluster standard servers, will expand 10% annually to $14.6 billion.

Previously, IDC (International Data Corporation), a market research and analysis firm specialized in IT, telecommunications and consumer technology, forecasted that in 2008, the global growth for supercomputing storage market would exceed that for servers approximately

11% and that the market for HPC storage would reach about $4.8 billion, compared to $3.8 billion in 2006 [30]. And this predictions turns out to be true and this trend will obviously continue at least for the next few years.

Figure 45 describes the distribution (not production) of world Top 500 supercomputer by nations.

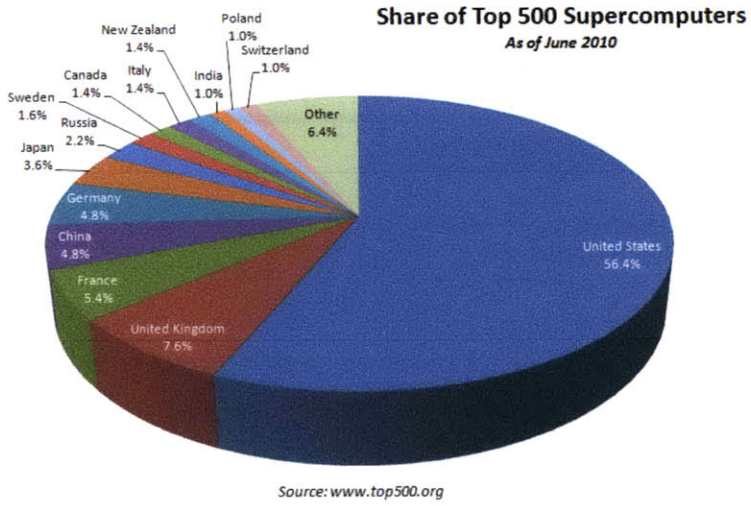

Figure 45: Top 500 supercomputers by nations[8].

The Terabit/second-class inter-chip parallel optoelectronic transceiver aimed at short-range chip-to-chip communication is right now still in improvement phase and we expect the first commercial product soon. Like many other hi-tech devices, it would also experience a process of commercialization from the tough time, probably, until maturity. Even though the increasing growth of the supercomputing market, the market for transceiver for supercomputing has yet to be mature. Usually for a young market to mature, it should undergo take off phase, overshoot phase, cooperation phase and standardization phase as in the case of the local area network (LAN) market [31] for instance.

[8] *Source: http://en.wikipedia.org/wiki/File:Supercomputers_countries_share_pie.PNG.*

2. The need for standardization of inter-chip transceiver market

These above three phases can be summarized as follow. At the beginning, with the high bandwidth-distance product desire and increasing demands for high modulation frequency, many optical interconnect and transceiver suppliers go to participate in the market. The take off phase is marked by the fact that each of these suppliers develop and provide their own products since the market is large and immature, everyone can earn profit without occupying a large market share. When the market mature and saturates, different products using different standards are now becoming incompatible. The bubble explodes in the overshoot phase and the market start to shrinks significantly and the economies of scale could not be achieved for each of the market players. Until this point, there is a need for standardization; big companies cooperate with each other while the small companies are facing difficulties for survival in the market. Let's take the market of transceivers for LAN (the communication range around 1 kilometer) as an example, during those years a lot of work has been carried out to come up with standardizations for transceivers in LAN. As the result, it would be possible to grab some ideas of the current state of the market just by reviewing the standardization process for transceivers.

Table 2: Standardization state for LAN optical connection (2008).

Speed (GB/s)	Avago	Finisar	Emcore	JDSU	Mergeoptics	Total
0.155	149	51	N/A	4	N/A	204
0.622	83	37	N/A	4	N/A	124
1	81	21	2	0	N/A	104
2	24	53	6	4	N/A	87
10	7	18	8	12	30	75
40		1				1

The Table 2 shows the 2008 products of only 5 major suppliers: Avago, Finisa, Emcore, JDSU and Mergeoptics. It's useful to note that, during the early time for optoelectronic transceiver, there are around 200 companies with transceiver products. If each has only five products, then the total number would be appreciable. This mean the product for low speed like 0.155 Gb/s should have a great variety. On the other hand, since the 40 GHz technology has not been mass produced, the number for 40 GHz or higher-speed product shows the real trends for that. However, due to the small number of suppliers in the market, the standardization would be realized soon. For optical transmission in SAN (the communication range around 10-30 meters), big companies have all started to develop the technology and cooperation to establish standardization for active cable[9].

Since it is the common technology trend to develop standardizations which have been occurring for the development of longer-range optical transceivers market, i.e. in LAN and SAN [31], short-range inter-chip optoelectronic transceiver for supercomputing systems also highly requires a standard in order to gain market maturity.

3. Competing Technologies

a. Electrical Copper-based Interconnect Technologies:

Obviously, optoelectronic (OE) transceiver technology for on-board interconnect needs to compete with copper-based electrical back-planes, and significant improvements in terms of speed, power consumption, density, and especially cost have to be achieved for OE transceivers

[9] *A device combined of optical fiber and optoelectronic transceiver [31].*

particularly in the light of the recent progress in high speed electrical interconnects, one of which is the PCI (Peripheral Component Interconnect) express standard.

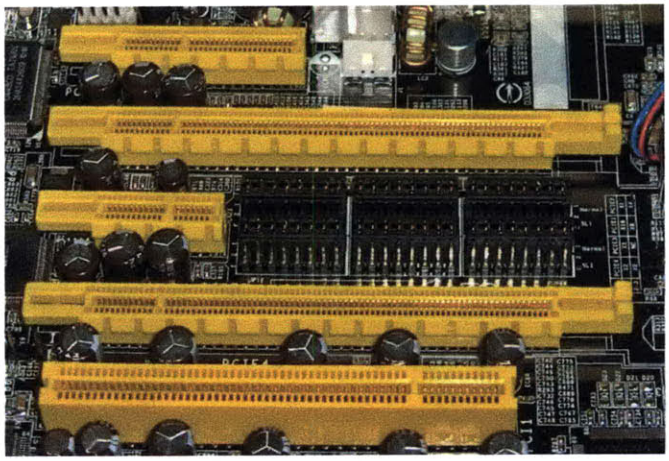

Figure 46: PCI Express slots (from top to bottom: x4 , x16, x1 and x16).

PCI is the standard for interconnect between printed circuit board (PCB) with the peripheral components [32]. The First PCI standard is designed to support a data rate of 250 MB/s in each direction. Generally, 8 lines would be used in parallel to provide a 2 Gb/s speed although 16 lines would be installed together. Throughout the last decade, the PCI bus has served us very well and will continue with the next generation, the PCI express (Figure 46) which has been released in 15th, Jan 2007. This generation doubles the speed of PCI standard. In the blooming demand for high processing speed, the PCI express 3.0, aiming to double the speed of PCI express, is under research and the final specifications which previously were planned by the PIC SIG to be due in 2009 have been delayed until 2011[10].

PCI express is an electronic based standard which is incorporated with transmitter and receiver component for high process speed and can easily reach the limitation of coaxial cable [33]. This builds a large barrier for optical counterpart to penetrate into the market. However,

[10] *Source: http://www.pcisig.com/home*

one may think of a certain way to incorporate the Terabus transceiver technology into the PCI technology to make use of optics in conventional electrical interconnect some day in near future.

b. Optical Interconnect Technologies:

- **The Intel Light Peak:**

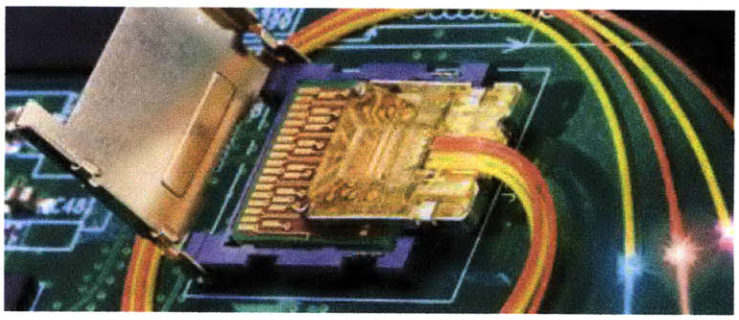

Figure 47: Light Peak technology (Intel)

Light Peak is a new high-speed optical cable technology designed to connect electronic devices to each other [34]. Light Peak delivers high bandwidth starting at 10 Gb/s, a speed at which a Blue-Ray movie can be transferred in less than half a minute. Smaller connectors and longer, thinner, and more flexible cables are made possible by advanced optical technology. Light Peak also allows running multiple protocols simultaneously over a single cable and connecting multiple devices such as peripherals, displays, disk drives, docking station, and more.

Light Peak consists of a controller chip and an optical module which performs the conversion from electricity to light and vice versa, using miniature lasers and photo detectors. Intel is planning to supply the controller chip, and is working with other component manufacturers to deliver all the Light Peak components. Intel expects that in 2010 the components will be ready to ship. Over time, the optical components, which have been designed

to be small, easy to manufacture and affordable, are expected to enjoy the economies of scale that other components have in the computing and consumer electronics industries. Intel is working with the optical component manufacturers to make Light Peak components ready and will work with the industry to determine the best way to make this new technology a standard to accelerate its adoption on a plethora of devices including PCs, handheld devices, workstations, consumer electronic devices and more. Light Peak is complementary to existing I/O technologies, as it enables them to run together on a single cable at higher speeds.

- **The Japan Project - R&D of Elemental Technologies for Future Supercomputers:**

Japan has planned to launch a project to construct a supercomputer with a computing power level of 10 x 10^{15} floating point number operations (PFLOPS)[11] or the Keisoku supercomputer system) by 2010 [35]. In 2005, 2 studies of optical interconnect under this project were initiated to develop elemental technologies for future supercomputing. These studies which both were industry-university collaboration projects continued for three years through 2007.

Application of optical interconnection to the CPU-memory link:

In spite of the ever increasing of CPU processing speed, progress in the data transmission rate between the CPU and memory has been receiving unsymmetrical attention. This would be a potential issue in future generations of computer due to the upper limit of the total computing system caused by CPU-memory transmission rate which has been lagging behind. NEC Corporation and Tokyo Institute of Technology are currently driving special

[11] *P-prefix stands for peta that represent* 10^{15}.

attention on optical interconnection (OI) between the CPU and memory as an alternative solution to speed up the CPU-memory communication rate.

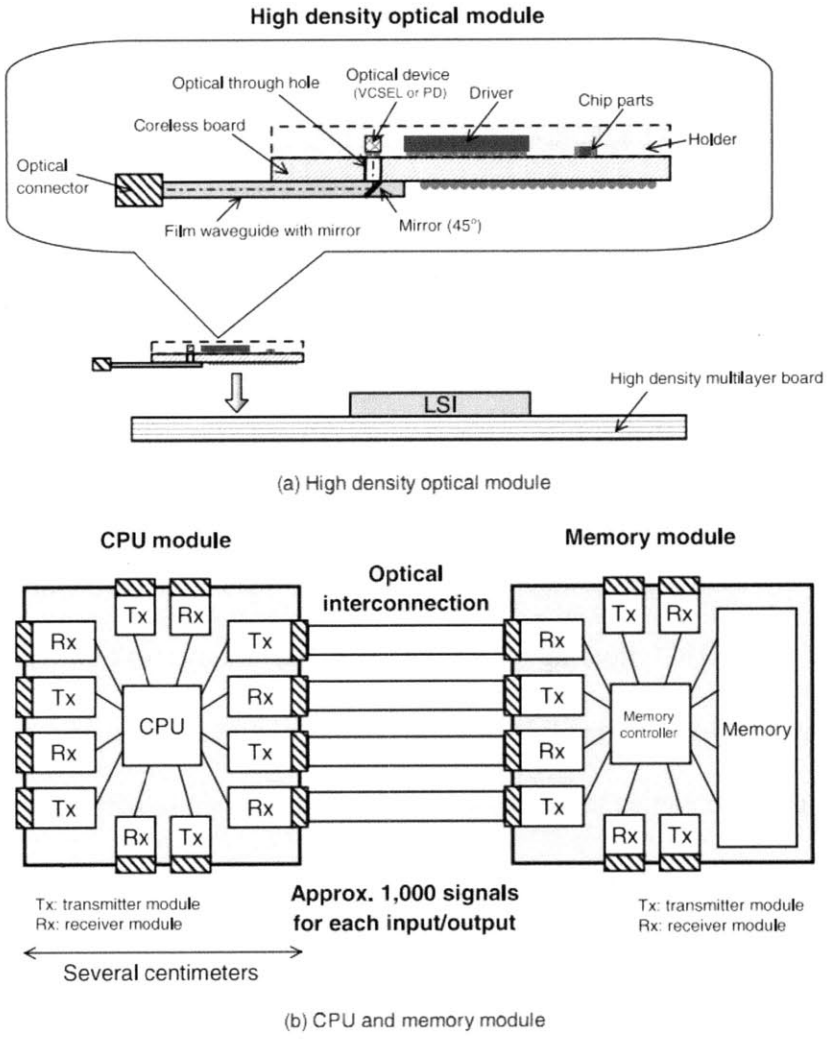

Figure 48: Configuration of CPU-memory optical interconnection [35].

If successful, the project outcome would be the world's first instance of such communication link between CPU and memory. The goal is to achieve the optical signal transmission rate of more than 20 Terabit/s per CPU. NEC predicted that CPU performance would surpass the speed of 100 GFLOPS in 2010. From this perspective, the target rate for CPU-memory transmission is determined to be at least 20 Gb/s, more than a 40 times increase on that

of the Earth Simulator[12]. As the result, the number of CPU signal lines will be halved to approximately one thousand only thanks for the usage of optical links. All in all, Japan said that the system performance target of 20 Terabit/s would be achieved if all of the aforementioned factors are successfully implemented. Figure 48 describes the high density optical module which is claimed by the Japan developers that has the size of a tatami[13] mat, i.e. 1-2 m^2. By taking full advantage of optical links, the module footprint must be reduced to several square centimeters. To realize the sizing goal, the Japanese group planned to do research in a broad range, including the development of a high-density packaging technique for a high-speed optical device (> 20 Gb/s) with the focus on thermal management as in case of the Terabit/second-class inter-chip parallel optoelectronic transceiver, and many other set of relevant technologies.

4. Thoughts on the market prospect of optical interconnect/transceiver

The market opportunity for optical interconnect and optoelectronic transceiver is very broad. The supercomputing market is just one portion of this opportunity pool. For the commercial CPU market segment, it's fairly certain that in the near future optical interconnect will be the integral part of a commercial CPU. Intel is currently the giant in the CPU market for commercial computers. The current computer architecture would experience a revolutionary modification as the result of the future successful incorporation of optical interconnect between inter-chip and even intra-chip links. Consequently, the current competitive landscape of CPUs will be triggered for the potential change of the market share. Mastery in optical interconnect

[12] *the fastest supercomputer in the world from 2002 to 2004 developed by Japan for running global climate models to evaluate the effects of global warming and problems in solid earth geophysics.*
[13] *a traditional type of Japanese flooring.*

technology is the cornerstone to gain a competitive standing in the next generations of CPU, memory and other peripheral devices. Inter-chip and Intra-chip communication requires a high level of technology which, however, can help the developers achieve a strategic and long-standing technical advantage over other competitors in the market.

Robotics is an area where the possibility of explosive growth in the near future is expected. Optical interconnects in general and optoelectronic transceivers in specific are very promising to be key components in the nervous system of these robots, transmitting information calculated in the brain which is nothing but CPU to the corresponding robot muscles and limbs. There would be indeed a significant market for a broad spectrum of applications resulting from this cutting edge technology of optical interconnect.

CHAPTER 2: Production Cost Model

1. The Process-Based Cost Model

Process-based cost model (PBCM) or technical cost model was developed as a method for analyzing the economics of emerging manufacturing processes without the prohibitive economic burdens of trials and errors (Busch 1988) [36], [37]. In the similar logic that today technical models facilitate manufacturing engineers and designers to envision the outcomes of their technical choices before them are carried out in reality. In product development and deployment, PCBM is the powerful tool allowing manufacturers to avoid costly strategic errors and foreseen expenses.

A PBCM has been developed as part of the MIT Communications Technology Roadmapping Project (CTR) specifically for the optoelectronic component industry. The data used in the PBCM has been collected from 20 firms across the optoelectronic supply chain from U.S and U.K and developing East Asia in the duration of 1.5 year from 2003 to early 2005. Although InP is used vastly in the model, the model was supposed to be easily adjusted to accommodate for new design, process and materials for the sake of flexibility in material selection for appropriate optoelectronic devices [37].

The CTR PBCM is a tool which allows the user to forecast and analyze optoelectronics production cost. A detailed description of component processing from front-end component fabrication, assembly and packaging, and subsequent testing steps is necessary to construct the model. From the description and user inputs for specific operating conditions, the model outputs

the predicted requirements for resources including tooling, labor, materials, and energy to satisfy the production target. These requirements then are utilized to calculate the corresponding operation and investment expenses which outcome the production unit cost. In the model, a set of equations have been developed to calculate the cost per good device, the aggregate costs are represented as:

$$C_{Tot} = C_{Material} + C_{Labor} + C_{Energy} + C_{Equipment} + C_{Tooling} + C_{Building} + C_{Overhead}$$

$$C_{El} = {}^{AC_{El}}/_{PV}$$

Where C represents the unit cost per good unit, AC is the annual cost, PV is the good devices per year, and El is the cost element (materials, labor, energy, equipment, tooling, maintenance, and overhead). [38].

52 sub-models each covering a different process have been developed in the first phase of the model. The user picks up from this list of sub-models both the types and order of processes required to produce the desired device. Table 3 and 4 list and classify all the 52 sub-models according to process function.

Table 3: Front-end process modules in a transmitter PBCM [37].

Surface Treatment	Growth/ Deposition	Etch	Lithography	Thermal
Clean	MOCVD	Plasma Etch	HMDS	Cure
Device Labeling	MBE	Asher	Spin-On Resist	Anneal
	PECVD	RIBE	Pre-Bake	
	H-Ion Implant	Wet Etch	Litho (Photo/UV)	
		Spin-Dry	Develop	
		Descum	Post-Bake	
		E-Beam Evap		
		Metal Lift-Off		
		Lapping		

Table 4: Cleaving and back-end process modules in a transmitter PBCM [37].

Backend Assembly	Backend Package	Backend Test
Wafer Cleave	Alignment	Incoming Inspection
Bar Cleave	Bake	Post-Deposition Test
HR Coating	Lidding & Lid Check	Automatic Inspection
AR Coating	Package Clean	Plant Transfer Test Set
Bench Attach	Fiber Attach	Post Wire-Bond Visual
Cooler Assembly	Sleeve Attach	Final Chip on Carrier Visual
Chip Bond		Assembly Visual
Wirebond		Pre-Lid Visual
Burn-In		Post-Ash Visual
Bench Assembly		Chip-On Carrier Test
		Cooler Assembly Test
		Post-Bake Test
		Temperature Cycle
		Final Package Test

The process flow necessary to produce a device is illustrated by process type and order as well as description of the materials, actions, and operating conditions happening at each process step. One could pick one among several pre-defined operational descriptions available and listed for each process, or he/her can specify his/ her own recipe for the model to describe that process step. Table 5 shows these operational descriptions from the 26 inputs in all cases.

Table 5: Process sub-model inputs (required for each process step, e.g., MOCVD) [37].

Process: (e.g., MOCVD)		
Incidental Yield	Direct Labor: Higher Ed.	Operating Time Per Batch
Embedded Yield	Direct Labor: Technician	Setup Time Per Batch
Machine Cost	Direct Labor: Skilled	Maintenance Freq. (/batch)
Capital Dedication (Y/N)	Direct Labor: Unskilled	Maintenance Time
Capital Usage Life	Installation Cost (%)	Tool/Mask Initial Investment
Max. Batch Size	Maintenance Cost (%)	Tool/Mask Add'l Unit Cost
Average Batch Size	Auxiliary Equipment (%)	High-Grade Cleanroom Space
Unplanned Downtime	Energy Consumption (kWh)	Low-Grade Cleanroom Space
		Non-Cleanroom Space

2. Case Study: The Cost Model of the Optoelectronic Transceiver

a. Attributes and Parameters:

The PBCM "ultimately projects the minimum efficiency fabrication line that is capable of producing a defined annual volume of good device and then calculate the cost of installing and operating that line." [38]. There are 3 attributes which are highly important in the case chosen for study:

(1) "The case provides insights on a large range of processes necessary in optoelectronic chip production". Probably, the case of the Terabus has satisfied this attribute since it has utilized a broad spectrum of process and tool used in optoelectronic assembly and fabrication.

(2) "The case focuses on emerging but extant technology for which significant data is available within the industry (i.e., from which to develop models of the relevant processes and against which model results can be calibrated)". Also the Terabus transceiver/interconnect seems to satisfy this attribute well due to this optical interconnect/transceiver is developed by the very novel research technology set which has not been used in mass production.

And (3) "The case addresses a key integration decision being faced by firms". This attribute could be satisfied in the case of the Terabus project since the case utilized key integration strategies like parallelism by device arrays and the state-of-the-art flip-chip bondings to address the design requirement and deal with power loss issue.

The last requirement is not listed as one of the attributes above but rather, the particular required functional specification. "All three scenarios are intended to represent the production of functionally equivalent 10 Gb/s devices with stringent quality specifications". Again, this speed is in the range required for each Tx-Rx link of the Terabus transceiver. (Refer to Chapter II).

In the model, a common set of operational and financial figures has been referenced. Details are listed below in Table 6 and 7.

Table 6: Financial Parameters Used for the Cost Model [37].

Product Life	3	years
Discount Rate	10.0%	
Equipment life (yrs) (default)	10	years
Building Recovery Life (yrs)	25	years
Installation Cost	10%	%fc (default)
Maintenance Cost	15%	%fc (default)
Overhead Burden	30%	%fc (default)
Price of Electricity	$0.080	$/kWh
Labor		
PhD Wage	$40.00	$ / hour
Tech Wage	$25.00	$ / hour
Skilled Wage	$20.00	$ / hour
Unskilled Wage	$15.00	$ / hour
Design Related		
No. of On-Line Designers	1	
Product Designer Salary ($/yr)	$200,000	
Pre-Production Development Investment	$1,500,000	

Table 7: Operational Parameters Used for the Cost Model [37].

Facility Description		
Working Days per Year	240	
Facility Downtimes:		
No shifts	7	hours / day
Worker unpaid breaks	1	hours / day
Worker paid breaks	1.2	hours / day
Unplanned	*Set in process specifications*	
Cost of Building Space		
High Grade Cleanroom	$3.000	$ / m^2
Low Grade Cleanroom	$2.000	$ / m^2
Non-cleanroom	$1.000	$ / m^2
Building Maintenance (% fc)	5.0%	% of fixedcost
Indirect workers/ Direct Worker	0.250	
Indirect workers/Line	1.000	

b. Process Flow for the Terabit/s Inter-chip Parallel Optoelectronic Transceiver:

The processing details of the transceiver components are given in Part II of the thesis. Here are the key points of the process flow:

- *VCSEL* structures are grown on GaAs substrate with low-pressure MOCVD. The epitaxial structure consists of 27.5 pairs of n-type GaAs/$Al_{0.9}Ga_{0.1}As$ bottom distributed Bragg reflector; 1-λ cavity with multiple quantum well active region and 40 pairs of p-type $Al_{0.1}Ga_{0.9}As/As_{0.95}Ga_{0.05}$ top distributed Bragg reflector. The multiple quantum well active region contains 3 strained InGaAs/AlGaAs quantum wells and 2 thick graded AlGaAs layers The apertures are fabricated to be 4, 6 and 8 μm in size. The process for the VCSELs requires: MOVCD, RIE, oxidation system, mask-aligner.

- *Photodiodes* are grown on Fe-doped InP substrate and are backside illuminated. 4 sizes of 30, 40, 50 and 60 μm are fabricated for the 2-D 4x12-photodiode array. The process for the photodiodes requires oxidation, ion implantation, mask aligner, MOCVD.

- *The laser diode driver IC and receiver driver IC* are fabricated in standard 0.13 μm (130 nm) CMOS process. Both of the two chip arrays each with 3.9 mm x 2,3 mm footprint are attached to a common silicon carrier. Each array contains 48 amplifiers and 2 voltage sources.

- In the process of the *silicon carrier*, silicon through vias are created using either wet or dry etch process. Deep reactive ion etch (DRIE) with a resist mask were used. The vias are dimensioned as 70 μm in diameter with 225-μm pitch and 300 μm in depth, providing an aspect ratio greater than 4:1. After this etching process, the vias are insulated with thermal silicon dioxide (SiO_2) and low pressure chemical vapor deposition (LPCVD) of silicon nitride (Si_3N_4). Other alternative methods such as plasma enhanced chemical vapor

deposition (PECVD) are also possible. The via sidewalls are coated with adhesion and diffusion barriers of TaN/Ta and Cu seed using physical vapor deposition (PVD). The vias are filled with a composite paste after excessive Cu has been washed out from the surface using chemical mechanical polishing (CMP). After that, the paste will be taken out through sintering process steps. The 5-μm thick Cu collars are created around top portions of the deep vias. This process requires DRIE, LPCVD, PVD, etc.

- *The Optocard* has been patterned using photolithography with 48 multimode waveguides cross-sectioned of 35 μm x 35 μm on a 62.5-μm pitch. An acrylic layer is deposited on top of the SLC card by doctor blading.

- *Packaging process:* Au bumps with 25 μm in diameter and 3-5 μm in height are created on top of the silicon carrier through plasma deposition to prepare for flip-chip attachment of the ICs to the surface of it. Subsequently, a 1.5 mm x 4.2 mm and 300 μm deep rectangular cavity is etched at the center of the silicon carrier from the front side of the wafer using a thick resist mask to pattern the cavity, which will be etched away by RIE, and the dielectric is cleared from the cavity region by the combination of highly selective oxide and nitride reactive ion etching. The flip-chip attachment of the IC arrays to the silicon carrier and the OE arrays to the IC arrays use eutectic AuSn (80% Au, 20% Sn) solder while Optochip is attached to the Optocard using eutectic SnPb (63% Sn, 37% Pb) solder.

- *Optical coupling mechanism:* 4x12 arrays of Au-coated lenses are fabricated right on the back surface of the GaAs/InP substrate and exactly aligned to each of the VCSEL and photodiode arrays. Each lens is engineered to have radius of curvature of 110-120 μm and conic constant of -2 (hyperbolic), which is proved to provide efficient coupling to the core of a 35 μm x 35 μm waveguide.

The simple process flow illustrating the steps required to fabricate the Terabit/second-class inter-chip optoelectronic transceiver can be visualized as in Figure 49.

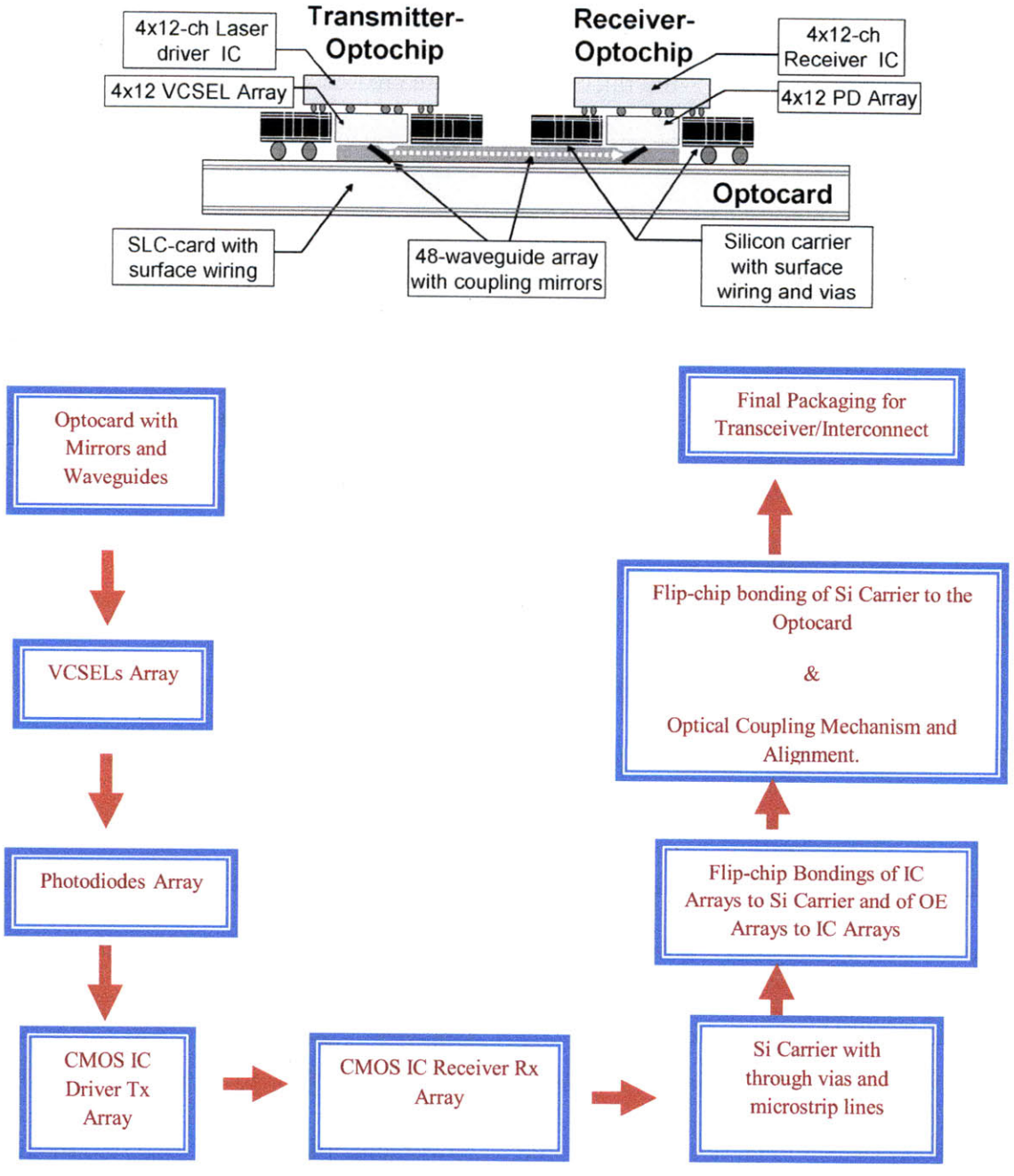

Figure 49: Transceiver fabrication process flow.

c. The Economies of scale

Economies of scale, a critical economic characteristic of any technology during production, describes a manner in which its production unit costs change with respect to the total units produced or production volume. The process-based cost model forecasts this change in production costs with scale by first determining the minimum efficient fabrication line which is capable of meeting a given demand and then inferring the cost of operating that line.

In the report [37] done by Erica and Randolph (MIT), a cost model developed for production of a 1550 nm distributed feedback (DFB) laser and an electro-absorptive modulator on an InP platform has been analyzed and reported. The cost model describes 3 scenarios: (1) a discretely packaged laser and a discretely package modular, (2) a discrete laser and a discrete modulator within a single package, and (3) a laser and a modulator monolithically integrated on a single device. The cost model describing the economies of scale for all the above scenarios is given in Figure 50.

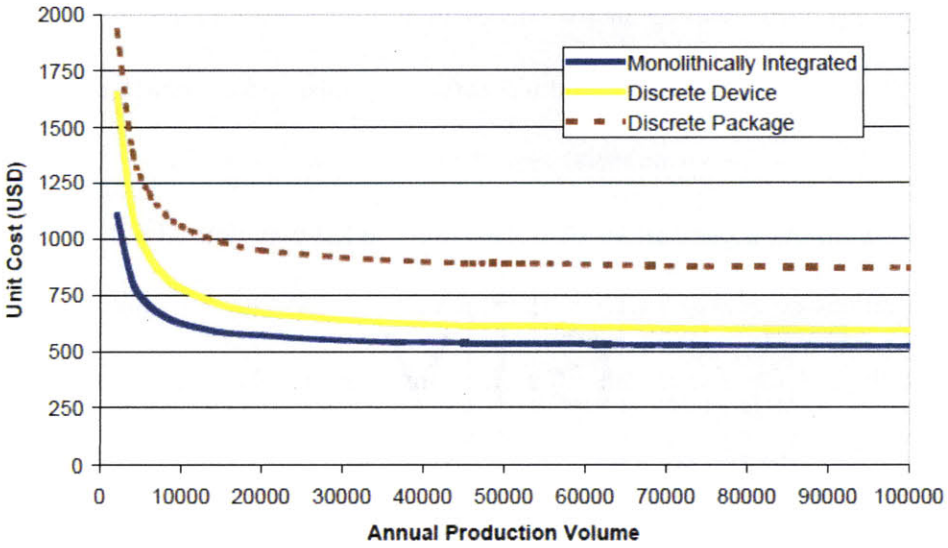

Figure 50: Unit cost vs. annual production volume for the 3 scenarios given in the report [37].

Since all the detail information for processing the Terabus transceiver in every step is nearly impossible to be collected from scratch given the time frame allowed for this thesis to be completed. A simple cost model for the Terabus transceiver may be developed largely based on the result of the study in [37]. Here the second scenarios, a discrete laser and a discrete modulator within a single package, seems to be most relevant to the context of the Terabus structure where the laser, receiver, IC arrays and silicon carrier, Optocard are all discretely packaged together to form a complete compact optoelectronic transceiver/interconnect module. A simple estimation has been carried out to map out the economies of scale of the Terabus transceiver.

Since the Terabus transceiver uses 48 sets of VCSELs, photodiodes and CMOS ICs. The economies of scale of the Terabus can be roughly mapped out in a "quick-and-dirty" manner by scaling the graph of the second scenario by a scalar multiply factor. Taking into account the fact that the Terabus structure is definitely more complex than the system of a laser and a modulator (Terabus transceiver requires silicon carrier with via holes, Optocard with waveguides and coupling mirrors, etc.), the scaling factor should also reflect the number of sets of the devices used (4x12 or 48 sets) and importantly should reflect the cost reduction effect due to packaging in a common module, i.e. lot of material and, therefore, cost will be saved if many devices are integrated inside a common package or platform (think in the way that why the price of the 8-GB thumb drive is not twice as expensive as the price of a 4-GB one, but much cheaper than that instead). Thus, the scaling factor cannot be as simple as 48. The approximate value of 7 is proposed to use since this scaling factor yields the unit price of ~ $4500 at economies of scale, which is the reasonable price for a new high-speed transceiver with respect to an immature market.

As the result, Figure 51 shows the unit cost-production volume relationship for the Terabit/s inter-chip parallel optoelectronic transceiver (Terabus transceiver). Production volumes above 30,000 units per year are critical to reach the economies of scale of around $4,450 per Terabus transceiver produced.

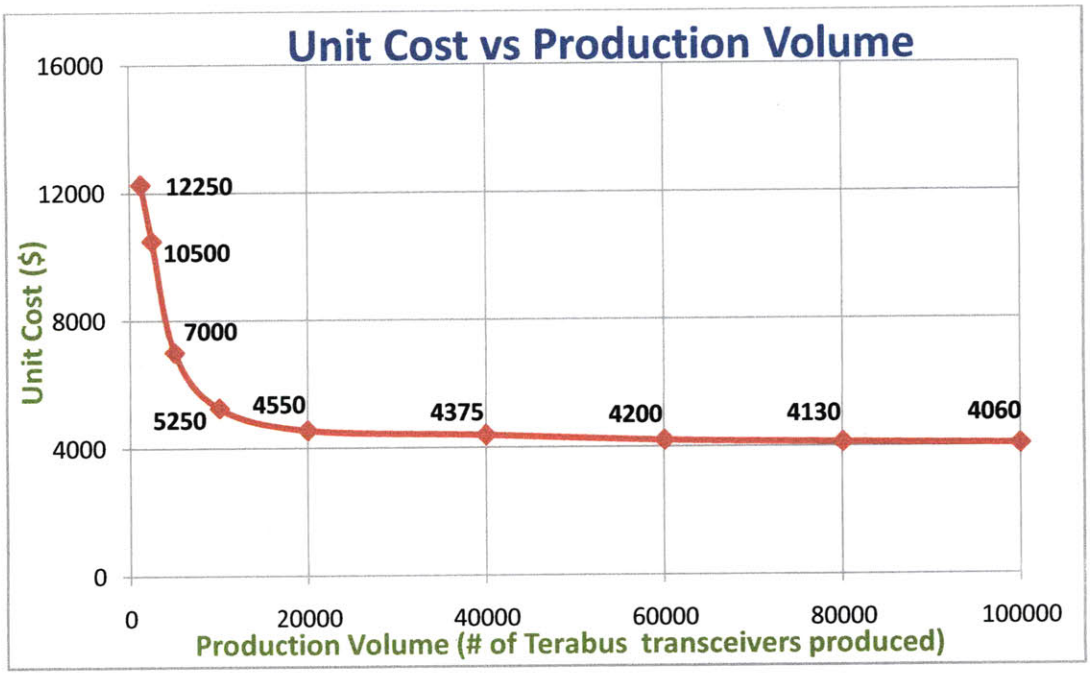

Figure 51: The transceiver cost sensitivity to annual Production Volume.

Given that global market for this powerful transceiver is currently not much larger than 30,000 units annually, it is not surprising that transceiver manufactures will have to cope with heavy cost pressure. Merger and collaboration between companies and across the supply chain are essential to drive down the cost; for instance, increase productions volume by sharing the common platform and resources across products, e.g. running multiple products on a single line.

The top contributors to the overall costs for a general optoelectronic transceiver are, in decreasing order, alignment (i.e., micro-optical alignment of lenses into the package) , assembly-stage testing, isolated die testing after transfer to back-end facility, chip bonding, fiber attachment, bench assembly, visual testing, bench attach, wirebond, and cooler assembly [37].

However, in this Terabus transceiver, the cost for chip-bonding should be placed as the top cost contributor since flip-chip bonding process has been used extensively for assembly the transceiver structure. Here, the data from [37] has been modified to reflect the extensive use of the flip-chip bonding in the Terabus. After modification, flip-chip bonding is adjusted to be the second cost driver in the list of 10. There are ten processes account for 70% of total product cost [37]. Figure 52 describes the breakdown of the unit cost of one Terabus transceiver produced at 30,000-unit annual production volume by top ten cost drivers, assuming that the top 10 covers 70% of the unit cost ($4,450).

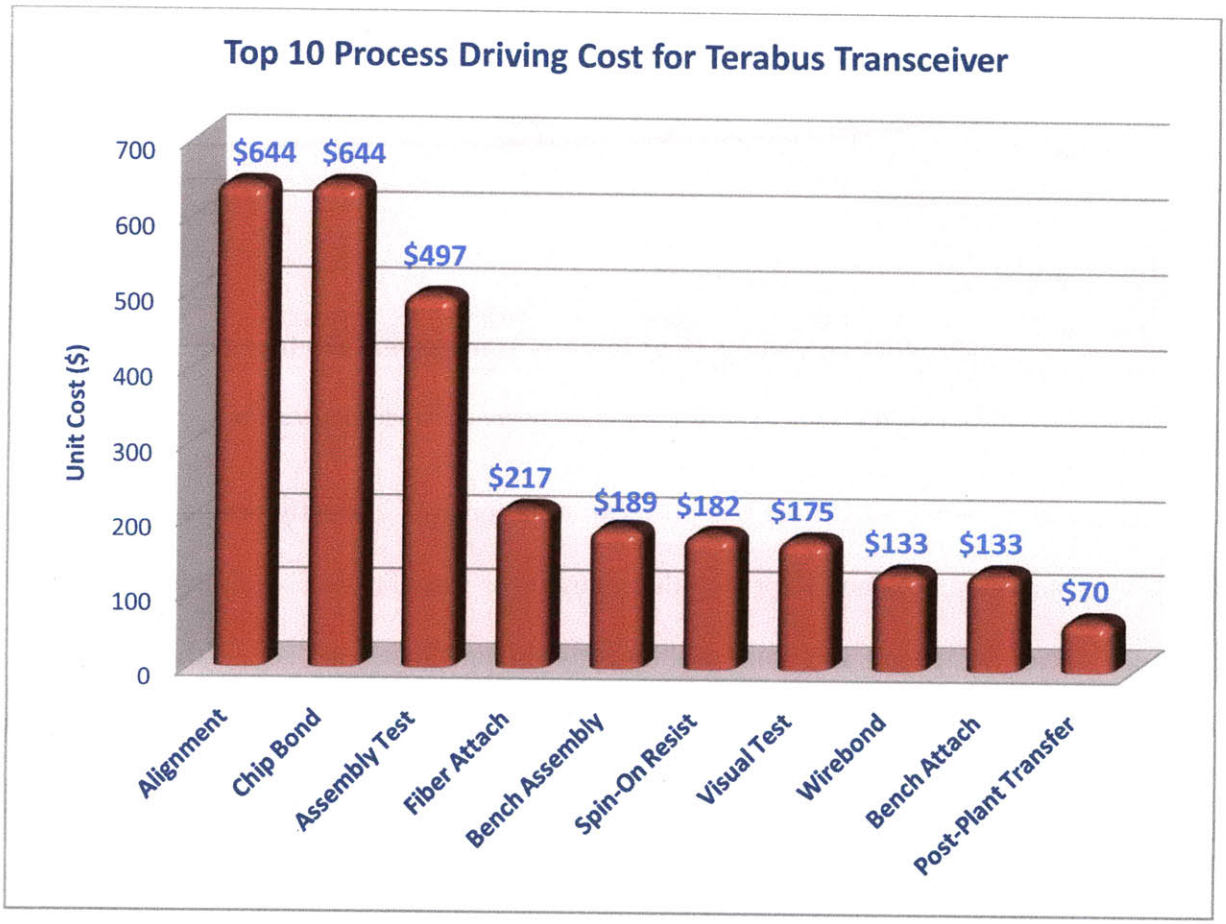

Figure 52: Top 10 process driving cost for the Terabus transceiver at 30,000 units annually.

Efforts focused on eliminating costs within these processes will surely have a significant effect on overall cost. It is very helpful to understand the underlying factors of cost for each of

these processes. Some processes are dominated by equipment costs (e.g., front to back testing, MOCVD), some by material costs (e.g., alignment, chip bond, fiber attach) and others by labor (e.g., assembly and visual test) while some depends on the extent of usage within the processing line, e.g. flip-chip bonding step in the Terabus transceiver processing line.

Rankings of the top ten cost contributors for the fabrication process of the transceiver can be seen in Table 8.

Table 8: Terabus Transceiver Top Ten Cost Drivers

Name of Process Cost Drivers	**Unit Cost Contribution ($)**	**Ranking**
Alignment	644	1
Chip Bond	644	2
Assembly Test	497	3
Fiber Attach	217	4
Bench Assembly	189	5
Spin-On Resist	182	6
Visual Test	175	7
Wirebond	133	8
Bench Attach	133	9
Post-Plant Transfer	70	10

The yield of the entire process can be improved significantly by identifying key steps, i.e. the cost drivers, regarding the number of times these process steps are repeated in the entire process flow and the position in the process flow where these process steps are triggered.

PART IV

CONCLUSION AND RECOMMENDATION FOR FUTURE WORK

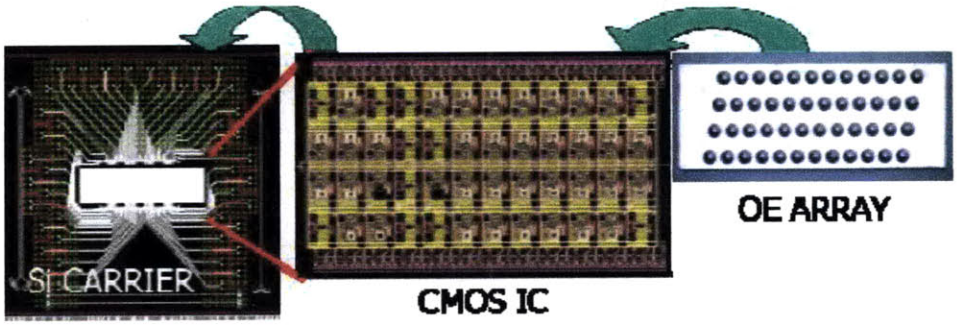

Figure 53: Terabit/s Transceiver Integration hierarchy [26].

As the computational capacity of the integrated circuits increases, higher-bandwidth connections are needed in great demand to transfer data between different processing units. Convention electrical connections will predictably become obsolete due to very high loss level and consequently, much power is required to transport data at ever increasing rates. The prospect of transforming a massive, low cost electronics manufacturing platform for CMOS integrated circuits into photonics regime is currently the interested topic of research and debate.

In this thesis, a complete set of constituent technologies developed for a novel inter-chip parallel optoelectronic (OE) transceiver (Terabus transceiver) which is capable of Terabit/second communication has been scrutinized in depth. A novel packaging hierarchy and a creative design for an optical coupling mechanism devised to bring high-level integration and high-speed performance to a final package have been analyzed: Two 4x12 arrays (each < 9 mm^2) of CMOS transmitter and receiver ICs have been flip-chip bonded to a silicon carrier interposer of 1.2-cm^2 size. Other two 4x12 arrays of OE devices (VCSELs and photodiodes) with comparable size are then flip-chip bonded to the corresponding CMOS arrays attached to the silicon carrier, forming the Optochip assembly. The Optochip is in interface with an Optocard by the flip-chip bonding process between the silicon carrier and an organic card patterned with 48 integrated waveguides at density of 16-channel/mm and total length of 30 cm. The 985-nm operating wavelength of the lasers allows a simple optical design with emission and illumination through arrays of relay lenses directly etched into the backside of the OE III-V substrate. A novel design of 45°-tilted and Au-coated mirrors fabricated in 125-μm-pitch acrylate waveguides is to perpendicularly couple the light in and out of the core of these Optocard waveguides. Per-channel performance of up to 20 Gb/s for transmitter and of up to 14 Gb/s for receiver have been realized, making the overall package transmission capacity of up to range of Terabit/second.

This study is under the Terabus project which is an initial step toward a complete technology for chip-to-chip and/or board-to-board optical buses which would allow a breakthrough in gigabit-data transmission between processors and servers or modules in high-performance computing systems. While the above project architecture is aim for optical interconnect application in general, a novel transceiver with Terabit/second transmission capability as proposed is undeniably one of the other great applications for such set of technologies. Although result obtained to-date is highly promising, significant effort is needed to improve and optimize the performance of the system to achieve the preset desired specifications. Essentially, a marketing strategy and a business plan are necessary for a successful commercial product.

It is almost certain that, in the future, optical interconnects will be the indispensible part of the CPU system. Currently, the CPU market for commercial computers is dominated by some main players. The current computer architecture would experience a revolutionary modification owing to the future successful incorporation of optical interconnects between inter-chip and even intra-chip links. As the result, the current competitive landscape of CPUs will be triggered for the potential change of the market share. The winning players should be ones who would be capable of possessing mastery in optical interconnect and transceiver technology and thus would gain a competitive standing in the next generations of CPU, memory and other peripheral devices. Inter-chip and intra-chip optical links ask for high level of technology which, however, would reward the developers with strategic and sustainable technical advantage over other competitors in the market.

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Appendix

Transceiver Optical Assembly Process Flow

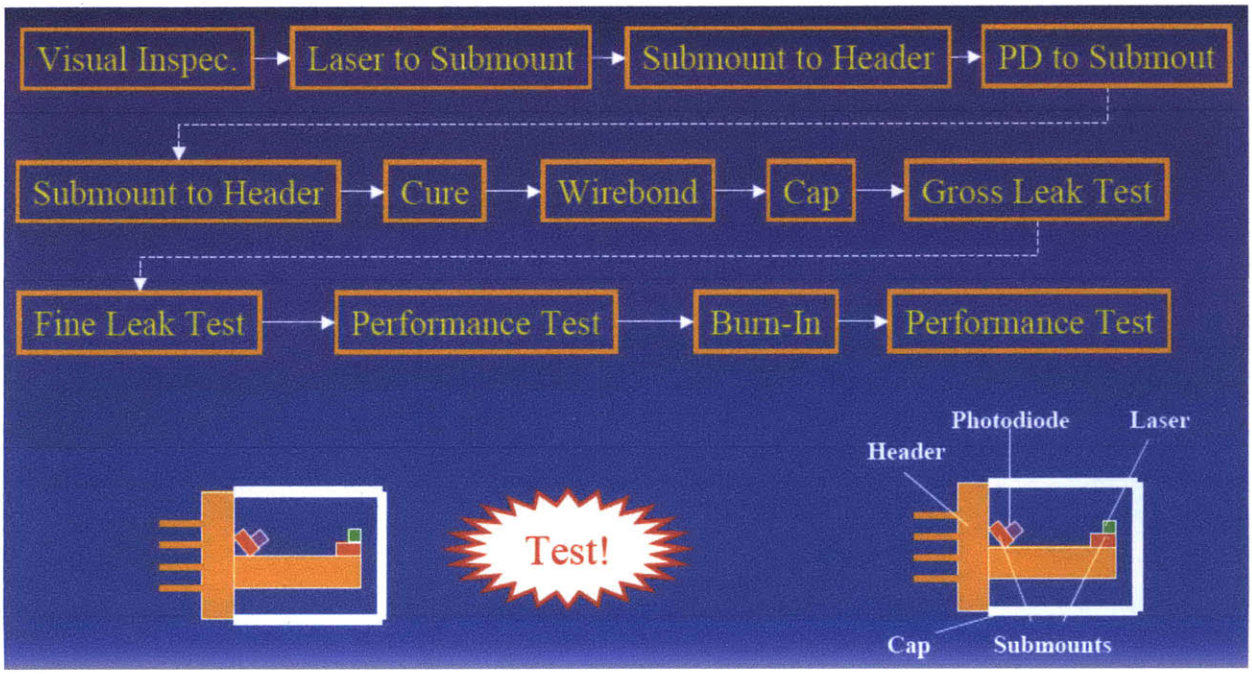

Figure 53: Terabit/s Transceiver Integration hierarchy [26].

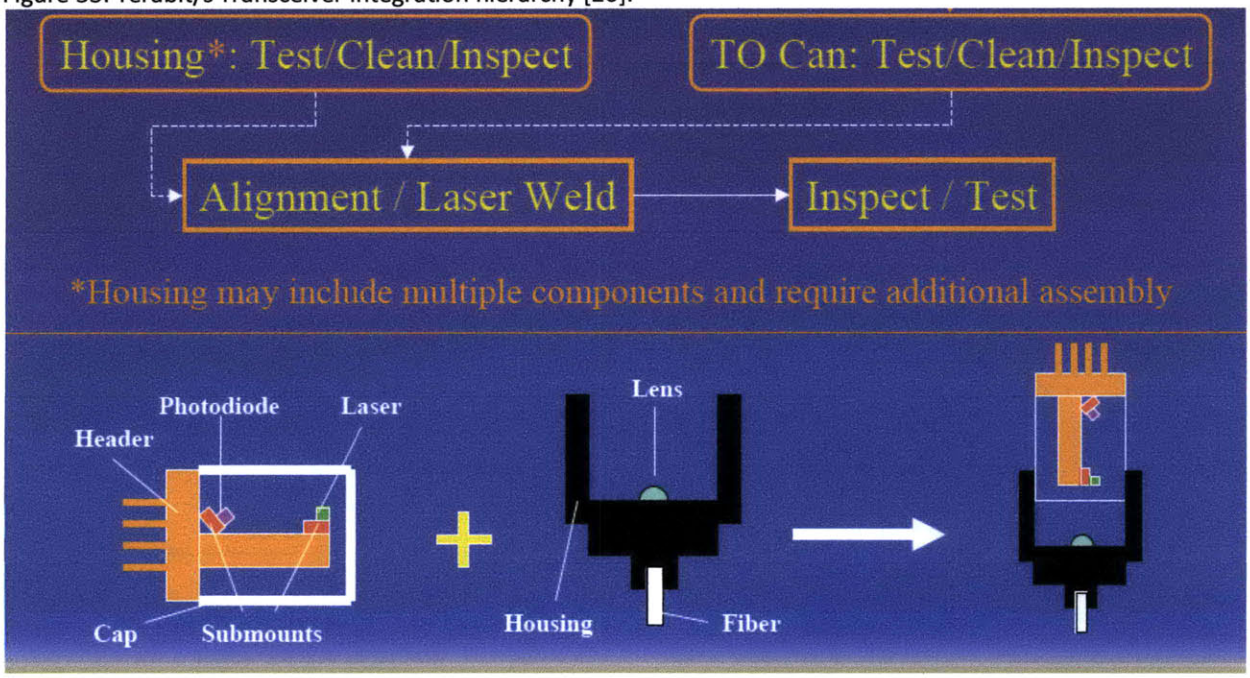

Figure 55: Transceiver Optical Sub-Assembly Process Flow [37].