A PERFORMANCE MEASURE OF PAGE MODE DRAM AS A SECOND LEVEL CACHE IN MICROPROCESSORS

by

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Abstract

An intensive study on three different types of page mode DRAM configurations was conducted to determine the effect of each on a microprocessor. Pure page mode schemes involve holding RAS lines down after an access to main memory in order to cache an entire row. Register-based cache DRAMs utilize a row of registers by the sense amplifiers to create a slightly more flexible cache. Cache DRAMs with embedded SRAMs allow for a fully-functional small SRAM cache to be included inside each DRAM chip. The advantages and disadvantages of each scheme are discussed.

A microprocessor simulator was created to model the performance of each page mode scheme. By incorporating time, this simulator modeled the interaction of microprocessor resources as well the miss rates for the various second level caches. While the performance results are somewhat specific to the particular microprocessor modeled, the second level miss rates will not change as resources are modified. The simulator modeled a floating point unit, integer unit, and a store buffer, as well as a memory system that included first and second level caches, and main memory.

Over two trillion instructions were simulated from the SPEC Benchmarks. A variety of first and second level cache sizes were swept to give comprehensive data on the performance of the page mode configurations. A total of forty-two sweeps were completed across the ten SPEC Benchmarks. Surprisingly, second level miss rates slightly improved as first level cache sizes were increased.

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Dedication

I have enjoyed having the opportunity to work under Pat Bosshart for the duration of this thesis, and his patience, insight, and understanding helped make this all possible. He was truly an inspiring force, both on and off the hockey rink ice.

I would also like to thank Steve Ward for overseeing my thesis from the MIT end, particularly for providing background material and resources when needed.

I am indebted to the members of TI, Integrated Systems Lab for allowing my use of their SPARCstations for background jobs.

I would like also to thank Sun Microsystems, especially Robert Cmelick for the use of the Shadow tracing program.

Finally, I would like to thank my parents for supporting me during my school years. My ambition and drive is a reflection of the encouragement they have given me over the years. I also thank God for giving me the ability to complete this thesis and helping me to keep a proper perspective on the important things in life.

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Chapter 1

Introduction

As microprocessors are clocked at increasingly faster rates, cache performance becomes continually more important. Second level caches have been shown to improve performance, but the cost sometimes prevents designers from including them in a microprocessor. Because memory systems prove to be more of a bottleneck with each new generation of microprocessors, the development of an economical, but effective second level cache becomes more important to the designer.

This thesis explores the performance impact of using various schemes in main memory to create a physically mapped, second level, unified cache. Three categories of page mode schemes are compared. Pure page mode DRAMs can cache rows of data in the sense amps by holding RAS lines down after memory accesses. Register-based cache DRAMs are special purpose DRAMs which allow a very long row to be split up into multiple blocks. Cache DRAM architectures with embedded SRAMs contain a complete SRAM cache on chip with the DRAM. While many such page mode or cache DRAM systems have been proposed, no large scale performance studies have been completed on them. While a successful page mode scheme can save a significant number of cycles, a poor performing system can actually degrade overall performance. A simulator to model microprocessor resources and execution time was created to evaluate the effect of these page mode schemes on both the memory system and the overall microprocessor performance.

The SPEC Benchmark Suite [Dixit 91], release 1, was used for the simulations. While no benchmarks can accurately predict an overall performance for a microprocessor, SPEC seems to be the most comprehensive benchmark suite broadly available today. The

SPEC benchmark suite consists of approximately 45 billion instructions. A series of simulations were completed over different first level cache sizes, second level cache sizes, and second level block sizes. In addition, a performance penalty charge was considered for those page mode schemes that degraded performance on a miss. Result data for this project was compiled by simulating over two trillion instructions.

All graphs for this thesis are included in the appendices. Appendices A and B include information on first level miss rates and clocks per instruction (CPI), respectively. Appendices C and D represent a sweep of second level total cache sizes and second level block sizes while the first level instruction and data caches are held constant. Appendix C shows miss rates for the benchmarks, while Appendix D shows the total performance impact as well as the memory impact of the second level caches on the microprocessor. Appendices E and F represent a second sweep of cache parameters. Two optimal second level block sizes were chosen and the total sizes for both the first and second level cache sizes were increased. Appendix E represents miss rates and Appendix F shows performance impacts. Appendix G includes a partial listing of the raw data collected during the various simulator runs.

The microprocessor resources modeled for this project were from a low-end SPARC processor. While numerous performance indicators are represented in this thesis, one should realize that performance results are somewhat particular to the processor implemented. However, since relatively simple integer and floating point units were implemented, one might expect that if better performing units were used, the impact of the page mode systems would be even greater, since the memory system would be more of a bottleneck to the entire system. The graphs for performance impact could be looked upon as a pessimistic indication of the effect of page mode systems. The graphs for miss rates will be accurate regardless of the performance of the integer and floating point units.

Chapter 2

Simulations

2.1 Shadow

The Shadow [Hsu 89] program from Sun Microsystems was used to gather traces. Shadow is a traceless routine which executes a program while filling up a trace buffer with structures that contain information such as the instruction word, effective address, etc., for each instruction. When the buffer fills up, it calls the simulation program which runs a virtual processor to gather performance results. Once the simulator has executed all the instructions in the trace buffer, it is emptied and the original benchmark program continues while Shadow refills the trace buffer. This scheme allows the simulation of large programs without needing prohibitive amounts of memory. The simulations are all based on programs running on the SPARC architecture.

2.2 Microprocessor Simulator

The simulator created for this project was written in standard C, and modeled all of the major resources of a microprocessor including the integer unit, floating point unit, first and second level caches, store buffer, and main memory. It measured performance by counting clock cycles using an event-driven timing mechanism. Each of these resources contributed to the overall CPI of the system, and the simulator determined how much of the CPI was charged to each resource.

2.2.1 Integer Unit

The integer unit was modeled by updating the time counter an appropriate number of clock cycles for each instruction executed. While most integer instructions took one cycle, store instructions took two cycles, while multiplies and divides took eight and sixteen respectively. Conditional traps took five instructions. All loads including double words were accomplished in one cycle. These clock cycles were also stored in a separate counter which allowed the calculation of an instruction CPI. For an optimal RISC processor, this number should approach one, as should the overall CPI.

2.2.2 Floating Point Unit

The floating point unit was modeled by creating a linked list of floating point structures with a length equal to the length of the floating point queue. Each time a floating point operate instruction was executed, an element was added to the linked list. In the structure, six pieces of information were kept. First, the time was recorded at which the instruction entered the floating point queue. Then three 32 bit register masks were created for the two source registers and the destination register that the instruction used. For these masks, a one in a particular bit number indicated that the corresponding register was used. Next a bit was kept to determine whether the instruction was a floating point compare, which needed to be handled as a special case. Finally, the total amount of time required to complete the instruction was also kept. The floating point queue length could be set to an arbitrary number in the program, but the microprocessor implemented had a queue length of one, so all simulations reflect this length.

When a floating point entry was sent to the queue, the processor was able to continue with other operations provided that some sort of stall was not necessary. These stalls could occur in a number of ways. If the queue were full, and another floating point operation occurred, the processor had to wait for an item to leave the queue. Each time a floating

point load occurred, the source and destination registers of instructions in the queue had to be checked against the source and destination registers of the load to see if a collision occurred. This check could be completed very quickly through a logical AND of the load register masks and the floating point operate register masks. If the destination register of the load matched any of the source or destination registers of pending operations in the queue, then the processor had to wait for the queue to finish the conflicting operation before the load occurred. Similarly, when a floating point store occurred, the destination register of the store had to be compared against the destination registers of each pending instruction in the queue, and a stall would occur on such a collision. A different stall could occur if a floating point branch were executed while there was a pending compare statement in the queue. A floating point branch required the processor to stall until all compares were completed. Finally, a state load or store required the processor to stall until the queue was empty. These processor stall cycles were kept in a separate counter and comprised the floating point CPI. If collisions were avoided, floating point instructions could be executed in parallel with other resources, so no "time" would be charged to the system.

The simulator handled the floating point queue by putting every operation in the queue, and constantly checking for one of the above collisions. If a collision occurred, the completion time of the offending operate instruction was calculated and compared to "current" time. If current time was greater then the completion time, then presumably the floating point instruction had time to complete and no actual collision occurred. If not, current time was updated to equal the completion time of the instruction in order to simulate the stall.

2.2.3 Memory System

The simulator had the ability to model multiple levels of caches, complete with write-back/write-through capability, set associativity, LRU replacement, and variable block size

options. The different page mode schemes were modeled as second level caches. To do this accurately, a few changes were needed. Since the caches were modeled as virtual caches and the page mode schemes created physical caches, the page number bits were scrambled to simulate a random mapping. To simulate this random mapping, the following algorithm was used. First, the bottom twelve bits of the address were changed to zero. These were the offset bits for the page. Then the XOR of the top sixteen bits of the address and the bottom sixteen bits of the address was calculated. The resulting sixteen bits were again split and an XOR was performed on the two sets of eight bits. The resulting eight bits were divided into a top and bottom half for a final XOR. The resulting four bits replaced bits twelve through fifteen of the original address to simulate a random bank and page number for the physical address. Only accesses to the second level, physical DRAM caches received this address.

Additionally, second level block sizes were not allowed to be larger than the 4K byte page size of the operating system. Any larger physical block size would have resulted in two unrelated virtual pages being cached in the same block. The chances of accesses jumping from one virtual page to the other one in the same block would have been extremely small.

The caches were set up as large arrays that contained only the tag since the simulator never needed the actual data. There was no array set up for main memory since all data not found in the caches was assumed to be in main memory. There were a variety of time penalties associated with the different caches. A first level Icache or Dcache miss had a latency charge required to get the first word out. This charge was unavoidable, since the processor had to wait while this occurred. In addition, there was also a possible throughput charge as the Icache or Dcache was busy filling the rest of the block. Once the first word was returned, the processor could begin subsequent operations, but the Icache or Dcache, and the DRAM would be marked busy for the time it took to fill the rest of the block. Any

subsequent request to these resources would have to check the busy counter to see if the block fill was completed. If not, then the processor had to stall. The exception to this case was an Icache collision that resulted from the PC counter being increased by one. The processor avoided the stall for this case. The latency and throughput charges were part of the memory CPI, and consequently the total CPI since the processor could do nothing else during these periods. A second level miss added an additional penalty to the memory system, but was strictly a latency charge since the second level caches were actually specialized main memory DRAM chips. The second level penalties will be discussed more thoroughly when the page mode configurations are discussed.

The store buffer in the microprocessor contained two entries. If a dirty miss occurred, then the block needing to be written back to main memory would be kept in the store buffer. If the store buffer had an entry in it, then the simulator checked each cycle for the DRAM to be marked free to allow the store buffer entry to be written to DRAM. Once the DRAM was free, the store buffer entry was deleted and the DRAM marked busy with the write. If two entries were already in the store buffer and another dirty miss occurred, then the processor stalled to allow one of the entries to be written to main memory. These penalties were included in the memory CPI.

The final component of the CPI came from a load-use stall that occurred in the SPARC Architecture [Sun 89] whenever an instruction tried to use the result of a load that occurred on the previous cycle. The four parts of the CPI give an idea of not only the performance of the microprocessor, but the relative impact an improvement to the memory system might have on the entire system. The graphs in Appendix B show the CPI components for each of the SPEC Benchmarks, as well as the averages for the integer and floating point benchmarks. The first two pages (pp 44-45) show the CPI for a memory system using a simple page mode scheme with 32M bytes of main memory. The memory system accounts for an average of 22 percent of the CPI for the integer benchmarks and 44

percent of the CPI for the floating point benchmarks. The last two pages (pp 46-47) of Appendix B show the CPI breakdown for the largest memory configuration tested, consisting of 32K bytes instruction and data caches, and a 1M bytes second level cache. For this case the memory only accounts for 7 percent of the CPI for the integer benchmarks and 16 percent for the floating point benchmarks.

2.3 Microprocessor Simulator Statistics

The simulator collected a wide variety of miss ratio statistics including miss ratios for reads, writes, data accesses, instruction accesses, and different length data accesses, all for both the first and second levels. Percentages of write backs and read modify writes for the first level caches were also included. A number of performance statistics were also kept, including clocks per instruction (CPI) for each program, broken down by microprocessor resource as discussed earlier. Additionally, DRAM utilization was calculated, as well as percentage of floating point operate instructions.

In order to compare the three page mode schemes, the simulator also returned the number of clock cycles that the page mode systems saved, and gave a percentage performance increase of using a page mode scheme versus a traditional single level caching scheme that uses page mode only for block fills. Finally the simulator returned the number of 2nd level dirty misses that would have occurred if the page mode schemes had somehow been made into write back caches. The total SPECmark performance rating for a benchmark execution was given as well.

For the memory system, the simulator kept two additional sets of statistics. The first set determined the number of cycles the Icache, Dcache, and store buffer caused the microprocessor to stall due to throughput charges. If an Icache request had to wait for an Icache fill from DRAM, then an appropriate counter was increased. Nine such counters were kept to account for each dependency. The second set of statistics tried to determine

patterns that caused the second level to miss. If a second level Dcache access was followed by a second level Dcache miss, then the "d after d" counter was updated. The reasoning behind this was to detect cases for which page mode would most likely fail.

A complete example of one of the simulation files is included in the following two pages.

```
Shadow: version 1.1 (10/Jan/90)
Analyzer: /nfs/ray/u3/shadow/cache5lru: version 3.1 (16/August/90)
Application: fpppp
Hostname: gladstone
Date: Wed Dec 25 05:23:03 1991
Speed: 3 IPS
Status: final


     1448153371 instructions (including annulled)
     1443743811 instructions (excluding annulled)
           34.7 SPECmarks for fpppp


level       size    block   subblk    assoc   write miss

1st I        8 KB    32 B             2-way   write back write allocate
1st D        8 KB    16 B             2-way   write back write allocate
2nd I+D    128 KB     1 KB           direct   write thru write allocate


1st Level:

              #    %instrs  %I+Drefs    %Irefs    %Drefs

      143134607    9.9142%    6.606%                     I+D misses
      115073764    7.9706%    5.311%    7.947%           I   misses
       28060843    1.9437%    1.296%              3.905% D   misses

     2166745975  150.0783%  100.000%                     I+D references
     1448153371  100.3055%   66.836%  100.000%           I   references
      718592604   49.7729%   33.165%           100.000% D   references

      588879185   40.7884%   27.179%            81.949% D   reads
       17710303    1.2267%    0.818%             2.465% D   read misses
      129713419    8.9846%    5.987%            18.052% D   writes
       10350540    0.7170%    0.478%             1.441% D   write misses

       13892891    0.9623%    0.642%             1.934% D   write backs
        3542351    0.2454%    0.164%             0.493% D   read mod writes

           1779    0.0002%    0.001%             0.001% 1 B D reads
             86    0.0001%    0.001%             0.001% 1 B D read misses
           1782    0.0002%    0.001%             0.001% 1 B D writes
             57    0.0001%    0.001%             0.001% 1 B D write misses
            282    0.0001%    0.001%             0.001% 2 B D reads
             33    0.0001%    0.001%             0.001% 2 B D read misses
             71    0.0001%    0.001%             0.001% 2 B D writes
              2    0.0001%    0.001%             0.001% 2 B D write misses
       30170797    2.0898%    1.393%             4.199% 4 B D reads
        1487436    0.1031%    0.069%             0.207% 4 B D read misses
        9149360    0.6338%    0.423%             1.274% 4 B D writes
         514343    0.0357%    0.024%             0.072% 4 B D write misses
      558706327   38.6985%   25.786%            77.751% 8 B D reads
       16222748    1.1237%    0.749%             2.258% 8 B D read misses
      120562206    8.3507%    5.565%            16.778% 8 B D writes
        9836138    0.6813%    0.454%             1.369% 8 B D write misses


2nd Level:

              #    %instrs  %I+Drefs    %Irefs    %Drefs

        2889423    0.2002%    1.841%                     I+D misses
        1278312    0.0886%    0.815%    1.111%           I   misses
        1611111    0.1116%    1.027%              3.841% D   misses
```

```
 157027251   10.8764%  100.000%                          I+D references
 115073764    7.9706%   73.283%  100.000%                I   references
  41953487    2.9059%   26.718%            100.000%      D   references

  17710303    1.2267%   11.279%             42.215%      D   reads
   1056492    0.0732%    0.673%              2.519%      D   read misses
  10350540    0.7170%    6.592%             24.672%      D   writes
    481390    0.0334%    0.307%              1.148%      D   write misses

 374254388  i for i (icache busy)
   7155157  i for d (DRAM busy)
   7369803  i for store (DRAM busy)
  26585091  d for d (dcache busy)
  28876442  d for i (DRAM busy)
   9942228  d for store (DRAM busy)
         0  store for d (DRAM busy)
     83040  store for i (DRAM busy)
         0  store for store (DRAM busy)

4171935848  total ticks of fpu     71.333% of total ticks
 591747328  fpOP instructions      40.988% of total
2010531268  total dram ticks       DRAM busy 34.377%
2365572338  float for float queue  fpu CPI=  1.639
1648494372  memory ticks           mem CPI=  1.142
1579515991  instruction ticks      raw CPI=  1.095
 254989434  load penalties         load CPI= 0.177
5848572135  total ticks            CPI=      4.051

# i  reads  after i      96258012,  # misses       628817            1%
# d  reads  after i      10353389,  # misses       776263            8%
# d  writes after i       6343199,  # misses       397426            7%
# i  reads  after d      10975281,  # misses       328651            3%
# d  reads  after d       3893838,  # misses       182247            5%
# d  writes after d       2151821,  # misses        26715            2%
# st writes after i       2119164,  # misses        73109            4%
# i  reads  after st      7840471,  # misses       320844            5%
# st writes after d      11039903,  # misses          120            1%
# d  reads  after st      3463076,  # misses        97982            3%
# d  writes after st      1855520,  # misses        57249            4%
# st write  after st       733577,  # misses            0            0%

 453736166  # of ticks saved  =  7.76 percent of total

   1239614  # of 2nd level dirty misses
```

2.4 Range of Simulations

Over two trillion instructions were simulated for this project by utilizing twenty SPARCstations with low priority background jobs for a period of about two months. Each run of the SPEC benchmarks, which contained 45 billion instructions, took about two machine weeks on a SPARCstation 2.

Two groups of simulations were run. In the first group, a range of second level block sizes and second level total cache sizes were swept, while the first level caches were held constant at roughly typical values for today's microprocessors. These simulations helped determine optimal block sizes. Total second level cache sizes were kept near values attainable using page mode DRAM in typical memory systems.

There had been some concern that the larger first level cache sizes of future microprocessors could render page mode caches ineffective. Therefore the second group of simulations focused on increasing both the first and second level cache sizes. To reduce simulation time, only two of the best second level block sizes (1K bytes and 512 bytes) were used for these ranges. Additionally, since one run of the Spice Benchmark took as long as the other nine benchmarks combined, some of those runs were eliminated from this sweep. Table 2-I shows a list of all simulations.

Table 2-I: Parameter sweeps of Cache Sizes in Bytes

1st Lvl	2nd Lvl	BlockSize	Sweep
I=8K D=4K	16K - 64K	128 - 4K	First
I=8K D=8K	128K - 1M	512 - 1K	Second
I=16K D=16K	128K - 1M	512 - 1K	
I=32K D=32K	128K - 1M	512 - 1K	

2.5 SPEC Benchmark

The SPEC benchmark is composed of ten individual benchmarks that perform minimal I/O and are designed to be CPU intensive. The programs are large enough to avoid fitting into most first level caches. Four of the programs are integer benchmarks, while six are floating point. The following is a brief description of each of the ten programs [Dixit 91].

001.gcc1.35 - This is a Gnu C compiler, Version 1.35 that measures the time for the compilation of nineteen source files. This program was chosen to test caches, and exhibits a load/store percentage of about 25%. This program is an integer benchmark written in C. 1.2 billion instructions are executed, making it the smallest benchmark.

008.espresso - This is a tool from the University of California at Berkeley that generates and optimizes PLAs. Four input models are run on espresso for this benchmark. The program is relatively small, spending a reasonable amount of time looping. 30% of the instructions are load/store. The benchmark executes a total of 2.9 billion instructions and is an integer benchmark written in C.

013.spice2g6 - Another tool from Berkeley, this is the standard analog circuit simulator widely used in industry. Five copies of a grey code counter are simulated for this benchmark. Although considered a floating-point benchmark, this benchmark only executes about 4% floating point operate instructions, and another 4% floating point load/store. Written in fortran, this program executed by far the most instructions with a total of 22.8 billion.

015.doduc - This is another floating point benchmark that completes a Monte Carlo simulation of the time evolution of a thermohydraulic model for a nuclear reactor's components. Many subroutines are executed, causing the code to jump around quite often. 26% of the instructions are floating point operations while another 24% are floating point

load/store. Most loads are double words. A total of 1.3 billion instructions are run for this benchmark.

020.nasa7 - This benchmark is a collection of seven kernels that test common scientific computations. Written in fortran, this floating point program executes 30% floating point operations, and another 44% floating point load/store instructions. A total of 6.8 billion instructions are executed for this benchmark.

022.li - The third of the integer benchmarks, this is a LISP interpreter written in C. The performance is measured in the time it takes li to solve the Nine Queens problem. A total of 4.9 billion instructions are executed, with about 25% being load/store operations.

023.eqntott - The fourth and last of the integer benchmarks, eqntott translates a logical representation of a Boolean equation into a truth table. About 32% of the instructions are load/store. Although the program will fit in some instruction caches, the data cache is significantly thrashed. This program executes 1.3 billion instructions.

030.matrix300 - This a double-precision floating point intensive benchmark that runs operations on 300 by 300 matrices. 38% of the instructions are floating point load/store and another 25% are floating point operations. 1.44 Megabytes of data accesses can cause significant data cache problems. 1.7 billion instructions are executed for this program.

042.fpppp - This double-precision floating point benchmark measures performance of the two electron integral derivative computation that occurs in a Gaussian series of programs. (I don't know what this means either). 41% of the instructions are floating point operations and another 44% are floating point load/store. A total of 1.4 billion instructions are executed.

047.tomcatv - The sixth floating point benchmark, this benchmark is a mesh generation program. 31% of the instructions are floating point operations and 26% are floating point load/store instructions. A total of 1.6 billion instructions are executed. This program was included because it thrashes the data cache.

When calculating the SPECmark rating for a microprocessor, the time it takes each of the benchmarks to complete on a VAX-11/780 is divided by the completion time on the microprocessor. The geometric mean of these ten ratios is considered the SPECmark rating for the microprocessor. Since each of the benchmarks is given equal consideration in the SPECmak rating, when completing the average floating point and integer graphs for miss rates and performance, the arithmetic mean of the benchmarks is used.

Chapter 3

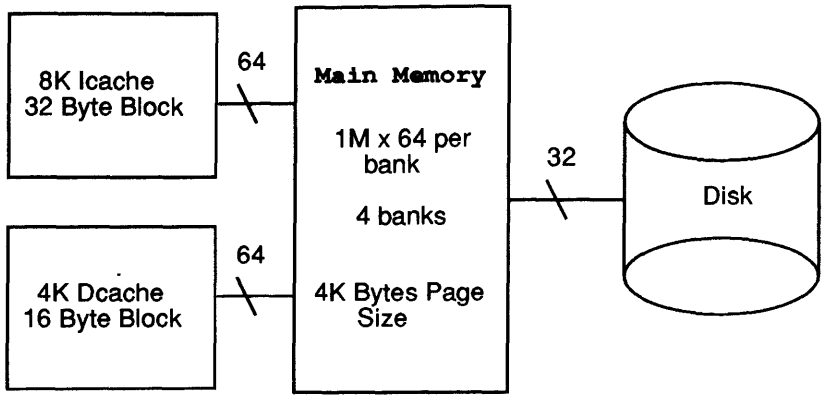
Memory System

The main memory system modeled by the simulator is shown in figure 3-1. The total main memory size was 32M bytes, divided into four independent banks, each configured with 16 1Mx4 bit DRAMs for a bank configuration of 1Mx64 bits. The banks were square with a row consisting of 1Kx64 bits, or 8K Bytes. A normal DRAM access consists of driving the row address and dropping RAS, and then driving the column address and dropping CAS. Immediately after the read is finished, the RAS and CAS lines are precharged high for the next access. For the processor implemented, the DRAMs had an access time of 80ns while the clock period was 15ns. For such a memory system, three ways to design a page mode cache will be presented.

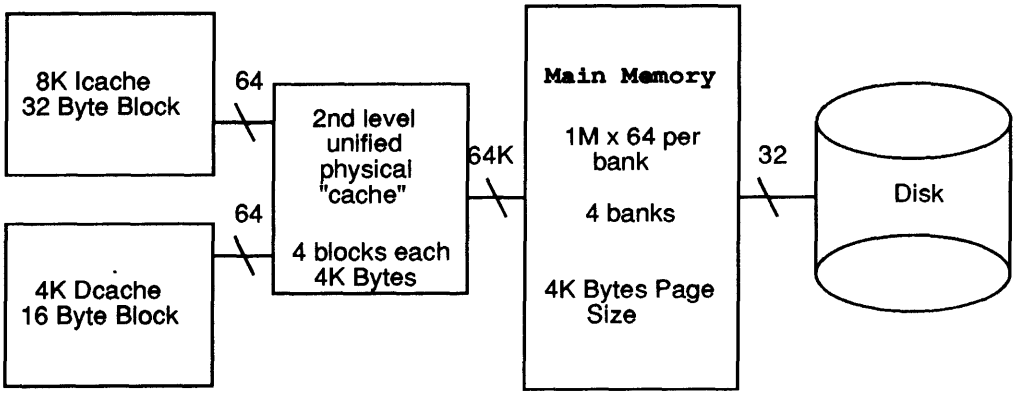
3.1 Pure Page Mode DRAM

Pure page mode DRAMs can cache a row of data in the sense amps by not precharging the RAS lines after an access to main memory. If a subsequent access is in the same row, then only the shorter CAS access need occur. A miss causes the normal RAS access to occur, but must also first precharge the RAS lines. As a result, a miss in a page mode cache is actually slower than a normal DRAM access. This additional time will be referred to as the precharge penalty. If a page mode DRAM cache has too high a miss rate, the added penalty of precharging the RAS lines can decrease overall performance of the memory system.

Pure page mode DRAMs have the limitation of utilizing a small number of very large blocks. The memory configuration discussed earlier consisted of rows 8K bytes long. A four bank main memory allows page mode DRAM to cache only four blocks, each with a size equal to one row. This is illustrated in figure 3-1.



Memory System



Memory System With Page Mode

Figure 3-1: Typical SPARC Memory System

3.1.1 Pure Page Mode Model

Although the memory system modeled created rows that were 8K bytes in length, in practice, half of the 8K byte block size is lost. The virtual page size for the SPARC architecture is 4K bytes. Since the mapping from virtual addresses to physical addresses is essentially random, each 8K byte block in a page mode DRAM caches two distinct and unrelated physical pages. Therefore, the simulator assumed that the extra 4K byte page was useless, and limited the effective block size to a maximum of 4K bytes.

Once the virtual address bits were scrambled, and the page size of the operating

system was taken into account, the page mode systems behaved similarly to a second level cache. A second level cache hit saved the system the RAS access time, which for the processor modeled equaled three clock cycles. For a pure page mode system, a second level miss required not only the three clocks of the RAS access, but cost five additional cycles due to the precharge penalty.

When comparing systems with page mode to a single level caching system, the simulator determined the number of clocks saved by using page mode. For a pure page mode system that included the precharge penalty, the simulator determined exactly how many cycles were lost on a second level miss. While the maximum loss in such a case was five cycles, there were two cases during which a portion of this penalty was not suffered, relative to the single level caching system.

In a single level caching system, whenever a DRAM access is finished, the RAS lines are immediately precharged. However, if an access to a particular DRAM bank was immediately followed by an access to the same bank, the precharge would not be finished in time for the access to complete so the processor would stall. A portion of the precharge penalty assigned to the pure page mode scheme would also be suffered by the single level caching system. The simulator modeled this case when calculating the number of clocks saved by a pure page mode system. Accesses to the same bank were noted, and the time between DRAM requests was calculated. If this time was less than five, then the number of clocks saved by page mode was adjusted accordingly.

The second case was unique to the processor implemented. If the DRAM was busy filling a block, and then another access came for the DRAM, the processor was able to utilize a second bus to look ahead and check for a second level hit if the access was to a different bank. If a miss was detected from the address on the second bus, the bank could begin its precharging process, thereby reducing the precharge penalty suffered. The simulator took this case into account, although it proved to be a fairly rare case.

3.1.2 Trade-offs

The biggest drawback to the pure page mode DRAMs comes from the very large block sizes. As future DRAMs get bigger, rows will get longer and page mode DRAM schemes will merely cache more unrelated physical pages causing even more cached bytes to be wasted. In addition, the total cache size is limited since only one block can be cached per DRAM bank.

A useful side benefit of even this simple page mode scheme comes from the significant power savings of not having to decode the RAS address on a hit. Also, since page mode DRAMs are a commodity item, implementation of this scheme would be relatively simple. However, the precharge penalty can become significant and even degrade overall performance. For the microprocessor implemented, a second level hit saved three clock cycles while a second level miss cost as many as five additional cycles, indicating that a miss rate of more than forty percent in the second level cache would start to cause a degradation of performance.

3.2 Register-Based Cache DRAMs

Special purpose cache DRAMs have been proposed which try and split up the large blocks of page mode DRAMs into smaller, more workable blocks [Arimoto 90], [Asukura 89]. Register-based cache DRAMs solve this problem by placing a row of registers near the sense amps of a conventional DRAM [Goodman 84], [Ward 88], [Ward 90]. These registers can be loaded in blocks of an arbitrary size whenever a RAS access occurs. In addition to allowing smaller block sizes, this scheme also avoids the precharge penalty of page mode DRAMs since the registers now act as the cache and allow the RAS lines to be precharged immediately after the reference.

3.2.1 Register Based Cache DRAM Model

The simulator did not have to worry about special cases when handling register-based cache DRAMs. Since the precharge penalty was eliminated for these second level caches, the number of saved cycles over a single level caching system was three times the number of second level hits. The only modeling difference the simulator took into account was the elimination of this precharge penalty.

3.2.2 Trade-offs

While solving the page mode DRAM problem of huge block sizes, register-based cache DRAMs do not address the issue of total second level cache size. Still one row is typically cached per DRAM bank. Also, since cache DRAMs are not currently commodity parts, their additional cost must be weighed against the benefits gained over pure page mode DRAM.

However, the elimination of the precharge penalty insures that this scheme will never degrade performance. In addition, the power savings can still be significant, since the RAS lines will not have to be dropped on a second level hit.

3.3 Embedded SRAMS

The most extreme form of main memory caching being introduced [Dosaka 92] involves putting a small SRAM memory along with each DRAM chip. This SRAM functions as a complete second level cache and can be designed with an arbitrary total size, block size, and set number. While the design of the previous two page mode schemes leads to a direct-mapped cache, embedded SRAMs have the flexibility of adding multiple sets. This page mode scheme solves both the problem of total cache size for the second level cache, and the problem of block sizes. Like the previous cache DRAM architecture, it also avoids the precharge penalty.

3.3.1 Embedded SRAM Model

There was no modeling difference between this case and the register-based cache DRAMs. The only difference lies in the number of graphs that are applicable to this scheme, since a greater flexibility is attained for DRAMs with embedded SRAMs. As an additional feature, the simulator calculated the number of second level misses that would have occurred if the embedded SRAM had been implemented with a write back scheme. Presumably, this may give a designer some feel for the gain that implementing these embedded SRAMs as write back caches might yield. Once again the number of cycles saved over a single level caching system was simply three times the number of second level hits.

3.3.2 Trade-offs

This system gives maximum flexibility by avoiding all of the penalties the other two systems incurred. There is no precharge penalty, block size limitation, or total cache size limitation. However, these DRAMs are new and very far from becoming common chips. While yielding the most flexibility, they will presumably be the most expensive to implement.

3.4 Simulations

The simulations for this project sweep across many second level block sizes and total sizes. The graphs shown do not differentiate between the three page mode schemes, other than including graphs of second level caches with and without the precharge penalty. However, each page mode scheme merely translates to a second level cache with a different total cache size and block size. When analyzing the memory system of the processor implemented (32MB total), the pure page mode system correlates to 16K bytes for the total cache size, and a block size of 4K bytes. The register-based cache DRAMs correspond to a

32K total cache size (since the entire row can now be used) and any of the different block sizes. Finally DRAMs with embedded SRAMs can correlate to virtually any of the points for different total cache and block sizes. For the pure page mode systems, those graphs that include the precharge penalty should be observed, while the graphs without the penalty should be used for the other two schemes. Graphs with and without the penalty were included for sweeps of all the parameters. By varying the block sizes and the total cache sizes, and deciding whether to include the total precharge penalty, information about all three types of page mode schemes was gathered from the data collected for this project.

Chapter 4

Measurements

Graphs for both miss rates and performance impact are included in the appendices. While the miss ratio statistics gathered are valid for any architecture implementation, the performance impact of the page mode schemes are strictly applicable only to the specific microprocessor implemented. Care must be taken when making generalizations to other systems.

4.1 First Level Cache Results

The miss rates of the first level caches determined the number and frequency of the accesses to the second level page mode caches. Four first level configurations were swept. The first group of simulations kept the first level cache sizes constant with an 8K Icache and a 4K Dcache. The second group of simulations increased these sizes, first increasing the Dcache to 8K bytes, and then increasing both to 16K bytes and then 32K bytes. The block sizes for all configurations were 32 bytes and 16 bytes for the instruction and data caches, respectively. Both caches were two-way set associative and used an LRU replacement scheme. First level miss rates for the different configurations are included in Appendix A. The top graph indicates the total miss rate of each benchmark. The middle graph gives the number of instruction misses divided by instruction references, and the bottom graph works the same way for data references. The columns marked integer and floating point give the arithmetic mean of the miss rates for the appropriate benchmarks.

The total miss rates indicate a miss rate range between one and two percent for the integer benchmarks, and between four and ten for the floating point benchmarks. These miss rates indicate that the benchmarks used were reasonable and that a significant number

of references were reaching the second level. Also, the graphs indicate that more can be gained by increasing the Dcache rather than the Icache. If the benchmarks are assumed to have forty percent load/store operations, then a 1% miss rate drop in the Icache is equivalent to a 2.5% drop in the miss rate of the Dcache. By comparing the benefits of doubling the Icache and the Dcache, it can readily be observed that the Dcache benefits much more, even when taking the above ratio into account. One of the reasons for this is that even with a small Icache, the miss rates are extremely low. For a similarly sized Dcache, the miss rate is a lot higher causing a subsequent doubling to have much more room for improvement.

4.2 First Sweep Miss Rates

The first wave of measurements used constant first level cache sizes of 8K bytes for the instruction cache and 4K bytes for the data cache. Six block sizes were swept, ranging from 128 bytes to 4K bytes, incremented by multiples of two. Additionally, three total cache sizes from 16K bytes to 64K bytes were simulated. A total of eighteen different settings were swept. Appendix C shows a plot of these miss rates. As block sizes are changed, one would expect to see a U-shaped curve of miss rates since very large or very small block sizes should yield higher miss rates [Hennessy 90].

4.2.1 Integer Benchmarks

The graphs for the integer benchmarks in Appendix C show a standard U-shaped curve. The optimal block sizes are 512 bytes and 1K bytes. As the total cache sizes are increased, the curves are shifted down since miss rates improve. The page mode DRAM cache corresponds to a block size of 4K bytes since an entire row of DRAM effectively caches 4K bytes of data. For a four bank main memory scheme (16K Bytes cache total) a page mode DRAM scheme has a miss rate from nine percent for 008.espresso, to about

thirty-two percent for 023.eqntott. The average integer benchmark miss rate is around twenty-two percent for pure page mode DRAM. The break even miss rate for implementing pure page mode DRAM is around forty percent for the processor implemented. The register-based cache DRAMs give the ability to break large blocks into smaller blocks. For a four bank main memory scheme, they can take advantage of an entire row of DRAM giving a total cache size of 32K Bytes. The ability to break large blocks into smaller blocks improves the miss rate between five and ten percent for these benchmarks. The effect is more pronounced on the smaller cache sizes. The ability to increase total cache size yields improvement of about six percent per doubling.

The added flexibility of smaller block sizes and larger total cache sizes of the register-based cache DRAMs and DRAMs with Embedded SRAMs could improve the miss rate by a maximum of about fifteen percent. The optimal case tested is for a DRAM with embedded SRAMs that resulted in a total cache size of 64K and a block size of 1K bytes. The miss rate for such a case is about 8.5%.

4.2.2 Floating Point Benchmarks

The graphs for the floating point benchmarks are much more irregular. While most of the graphs show the standard U-shape, the graphs for 030.matrix300 and 020.nasa7 (p 52)exhibit bizarre behavior. For these two benchmarks, very large and very small block sizes perform the best, causing the extreme block sizes to exhibit the best miss rates. In addition, these two benchmarks change the most when parameters are swept, causing the graph of the average floating point benchmark to be nearly flat.

The configuration for the pure page mode shows an average floating point miss rate of about 37%, just slightly better than the 40% break even point. However, only two of the six floating point benchmarks have a miss rate above 40%. 013.spice2g6 gives a miss rate of 62% while 047.tomcatv gives a miss rate of 45%. Both miss rates go significantly down if the block size is decreased or if the total cache size is increased.

The average floating point miss rate does not change much when block sizes are altered, due primarily to the odd behavior of a couple of the benchmarks. Increasing the total cache size decreases the miss rate by eight percent per doubling. All points on the average floating point graph graph lie under the forty percent mark indicating that any page mode scheme will help, with or without the precharge penalty. The floating point graphs indicate the wide variety of performance that caches can have. Not all benchmarks will behave in an intuitive manner.

4.3 First Sweep Performance

One might expect the performance impact curves to look roughly like the inverse of the cache miss rates curves. The magnitude of the performance gains depend on the implementation of the rest of the system. Performance gains were reduced if an improvement to the memory system caused the processor to be bound by some other resource: for example, an improved memory system performance could make a processor more bound by the floating point execution time. Also, if the CPI of a program is dominated by some resource other than the memory, then no matter how much the memory system is improved, the overall performance will not dramatically increase. The performance graphs are located in Appendix D. For each benchmark, as well as the average integer and floating point benchmarks, four graphs are shown. Performance impact with and without the precharge penalty are considered, as well as the memory impact with and without the precharge penalty. When comparing the impact with and without the RAS precharge penalty, the three lines representing total cache size get bunched together and each line varied over block size gets flattened out when the penalty is eliminated. Since a better performing benchmark with a bigger performance gain must have a better miss rate, the elimination of the RAS precharge penalty will not help it as much as the penalty elimination helps a smaller gain from a poorer performing benchmark. Similarly, the lines

get flattened out over block size, since the poor performing block sizes have more to gain from the elimination of the precharge penalty.

The performance impact is calculated by dividing the number of clocks saved by the page mode scheme by the total number of cycles. The memory impact divides the number of clocks saved by the total number of clocks that contributed to the memory CPI. The memory CPI includes only those clocks charged to the processor for a first level miss. A program that had a zero percent first level miss rate would have a zero memory CPI. The graphs of the memory impact are the same as the graphs for the total impact, with an appropriate scaling factor that models how much of the total CPI is devoted to the memory system. The graphs with the penalty charge assume a pure page mode scheme, while those without the precharge penalty assume either a register-based cache DRAM or a DRAM with embedded SRAMs.

4.3.1 Integer Benchmarks

The overall performance impact for pure page mode DRAM schemes on the integer benchmarks averages to between three and six percent. These graphs include the penalty of the additional RAS precharge time needed on a miss. The ability to change block sizes can gain about one percent while increasing the total cache size from 16K bytes to 64K bytes gains roughly two percent. In general, the first level miss rates are small enough that not much total performance can be gained by improvements to the second level cache. The individual benchmarks do not stray much from the average.

The average integer memory impact for the graphs with the precharge penalty is between fifteen and twenty percent. The ability to change block sizes can give about a seven percent swing, while increasing the total cache size gives an eight percent memory performance increase for each factor of two increase. The ratio of these two graphs show that the memory CPI is roughly one-fifth of the total CPI on average.

By eliminating the precharge penalty and using either register-based DRAMs or DRAMs with embedded SRAMs, the average total performance impact goes up by about two percent, and the memory impact goes up by about ten percent. Changing the block size now only gains a fraction of a percent for the total system, and about four percent for the memory impact. Doubling the cache size gains about five percent on average. Each of the individual integer benchmarks performs similarly. The ratios between the total impact and the memory impact still shows the memory CPI to be about one-fifth of the total CPI.

4.3.2 Floating Point Benchmarks

The performance of the floating point benchmarks is much more erratic. The graph for the average floating point benchmark shows an overall performance gain between two and seven percent and a memory performance gain between five and twenty-five percent when the precharge penalty is included. The ratio between these two numbers indicates that the memory CPI is roughly one-third of the total CPI. Changing the block size gives a small and inconsistent percentage swing while increasing the total cache size shows an overall performance gain of three percent per doubling, and a memory gain of about six percent per doubling. Analyzing any individual benchmark can give wildly different results. 030.matrix300 (p 63) yields negative performance gains for all block sizes other than the maximum, or 4K byte size. Increasing the total cache size does not significantly help the middle block sizes for this benchmark. However, the average of the floating point benchmarks never yields a negative performance for any combination of block size and total cache size.

When the precharge penalty is removed, the difference in performance impact is significant. Since the floating point benchmarks tended to have higher miss rates, the elimination of the precharge penalty impacted these graphs much more than the integer benchmark graphs. The average floating point benchmark without the precharge penalty

yielded overall performance gains between nine and twelve percent and memory improvement between twenty and thirty percent. Changing block sizes still had little and unpredictable affects, while an increase in total cache size gained an additional four percent of both overall and memory performance per doubling. Eliminating the precharge penalty also tended to make all the individual floating point benchmarks behave much closer to the average.

4.4 Second Sweep Miss Rates

The second sweep of simulations increased the first and second level total cache sizes while keeping the second level block sizes constant. Ignoring the 030.matrix300 benchmark, block sizes of 512 Bytes and 1 Kilobyte performed the best and were used for these simulations. Since each new generation of microprocessors will yield higher on-chip first level cache sizes, this group of simulations was aimed at determining whether page mode schemes will be applicable for future processors. First level caches were swept from 8K bytes for both the Icache and the Dcache to 32K bytes. The performance of those first level caches is shown in Appendix A. Second level cache sizes were swept from 128K bytes to 1M bytes by successive powers of two.

Since bigger first level caches would lead to fewer and less frequent second level accesses, one might believe that second level performance would significantly decrease as first level sizes increase. The graphs in Appendix E show that the miss rates actually improve slightly as first level caches get bigger for both the integer and floating point benchmarks. This was a very interesting and somewhat unexpected phenomenon that speaks well for the future of page mode systems. The result is that small second level caches perform better than expected with the larger first level caches. Additionally, as the total size of the second level cache increases, the miss rate continues to drop. For the largest second level cache size tested (1M bytes), the miss rate for all graphs is less than three percent.

4.4.1 Integer Benchmarks

For each of the first level configurations, increasing the total second level cache size significantly reduces the miss rate of the average integer benchmark from five percent (128K total) to about one percent (1M total). Increasing the first level sizes slightly reduces the miss rate for the smaller second level total sizes, while for the larger total cache sizes the miss rate stays constant. For 022.li(p 71), each time the first level cache is doubled, the second level miss rate goes down more than a factor of two. The shape of each of the individual integer benchmark graphs is similar, although the actual values of the miss rates are significantly different. 023.eqntott has a miss rate range from fifteen to five percent, while 008.espresso has a range from one to nearly zero percent.

4.4.2 Floating Point Benchmarks

Once again, the floating point benchmarks exhibit higher average miss rates yielding average values around fifteen percent for the 128K total size to about three percent for the 1M total cache size. Again, the average miss rates slightly decrease as the first level cache sizes are increased. The higher average miss rates for the floating point benchmarks are largely due to 030.matrix300, since the 512 bytes and 1K bytes block sizes were shown to be non-optimal block sizes for this benchmark. Miss rates for this benchmark start at about 45 percent (128K bytes total) but end up around two percent (1M bytes total). For these benchmarks, the second level miss rate of 042.fpppp (p 76) decreases the most as first level cache sizes are doubled.

4.5 Second Sweep Performance

The graphs in Appendix F indicate diminishing yields on the overall performance impact as the first level sizes increase. Since the raw number of accesses to the second level cache is going down, even an improved miss rate will have a lesser impact on the processor because the memory CPI will be a smaller percentage of the total CPI. The graphs in Appendix B indicate how the CPI breakdown changes from the worst case configuration (16K total, 4K blocks) to the largest configuration (1M total, 1K blocks). The memory CPI percentage goes from 22 percent to 7 percent for the integer benchmarks and from 44 percent to 16 percent for the floating point benchmarks. Since the simulator still models the original microprocessor, the simulations for the largest configuration correspond to a processor with relatively weak integer and floating point units, but an extremely powerful memory system. If one assumes that the processor itself will improve as memory systems get larger, then the impact of these page mode schemes would become significantly greater. When comparing the performance with and without the precharge penalty, the difference is almost not noticeable since the miss rates are too small for the precharge elimination to make any significant contribution to performance.

4.5.1 Integer Benchmarks

Since the miss rates were so small for all of the second level total cache sizes, the performance impact remains fairly constant as this parameter is varied. As first level sizes increase, the overall performance gain drops by two percent per doubling. The smallest first level configuration (8K Icache 8K Dcache) yields an almost constant performance gain of six percent over varying second level cache sizes. This decreases to two percent as the first level cache sizes are quadrupled. The memory impact slightly increases as the first level cache sizes are increased. Since the miss rates were getting slightly better with each first level increase, the memory performance impact also gets slightly better. Also, the

increase in total cache size has a more pronounced effect on the memory impact. Memory improvement lies between 33 and 40 percent for the smallest first level size, and increases an additional four percent for the largest first level size. The elimination of the precharge penalty shows little difference since the integer miss rates were so small.

4.5.2 Floating Point Benchmarks

The average floating point benchmark overall performance gain shows a steady increase as second level total cache size is increased, since the miss rate was significantly changing for each doubling. Also, the difference between the lines with the precharge penalty and without are much more significant since the average miss rates were higher for these benchmarks. For the smallest first level sizes, the overall performance gain was between six and twelve percent, going up by roughly two percent for each second level doubling. Each doubling of the first level cache sizes resulted in a halving of this performance gain. The elimination of the precharge penalty gave an additional gain of about two percent for the smallest second level cache size but gave no additional gain for the largest, since the miss rate approached zero.

The memory impact was fairly constant as the first level sizes were increased, indicating a second level miss rate that was largely independent of first level size. With the precharge penalty included, increasing the second level size change the memory impact from 23 percent to about 35 percent. Without the precharge penalty, this change was from 28 to 36 percent.

Chapter 5

Conclusions

A first sweep of cache parameters showed that page mode DRAM could indeed improve the performance of a system. With a constant first level cache size, a sweep of second level block sizes indicated that performance was gained by allowing smaller blocks. In addition, increasing the size of the second level cache continued to increase the performance of the page mode DRAM. Increasing total second level cache size was much more effective than changing the block size.

A second sweep of cache parameters studied the value of page mode schemes for future microprocessors. While two optimal second level block sizes were held constant, the total sizes of the first and second level caches were increased to model the increasing memory system sizes of future processors. The page mode schemes showed improved miss rates for both larger first level cache sizes and larger second level cache sizes. The performance impact on the microprocessor went down as first level cache sizes increased, due to the smaller number of second level cache accesses.

Using pure page mode DRAMs limits both the total cache size and the number of blocks allowed in the second level cache. By not being able to break up rows of DRAM into smaller blocks, 4K bytes were wasted for each cached block. Larger DRAMs would cause even more waste since the rows would get even longer. The total effective cache size could only be increased by adding more banks of main memory DRAM since only 4K bytes per DRAM row can effectively be cached. A four bank main memory system with a total of 32M bytes of memory could be configured with page mode DRAM to create only a 16K bytes second level cache, which is probably too small to be very effective. In addition, as the miss rate got worse, the RAS precharge penalty started to significantly degrade performance.

Register-based cache DRAMs solve the problems of wasted bytes and large blocks. Allowing smaller block sizes helped the miss rates, but not tremendously. Cache DRAMs make effective use of the entire DRAM row, but also could get no bigger than the size of a row multiplied by the number of banks. 32M bytes of main memory translate into 32K bytes of second level cache for a four bank scheme. Simulations showed that this performs reasonably well, but could get even better if the total cache size could somehow be increased. Additionally, register-based cache DRAMS avoid the problem of the RAS precharge penalty, which becomes significant when the second level cache miss rate is marginal.

Cache DRAMs with embedded SRAMs allow arbitrary sizes for both second level blocks and total cache sizes, and eliminate the RAS precharge penalty. Additionally, the designer may consider design issues such as set associativity or write-back caching. This increased flexibility could dramatically increase a memory system's performance since larger second level cache sizes showed increased effectiveness for each doubling. Achieving a large enough total size is the main problem with page mode caches, and only the SRAM-based cache DRAM solves it.

The integer benchmarks showed a very regular second level cache behavior, and second level miss rates were very low. The floating point benchmarks exhibited higher miss rates and responded to parameter changes erratically. For the largest cache sizes, all benchmarks exhibited very small miss rates and significant memory performance improvement.

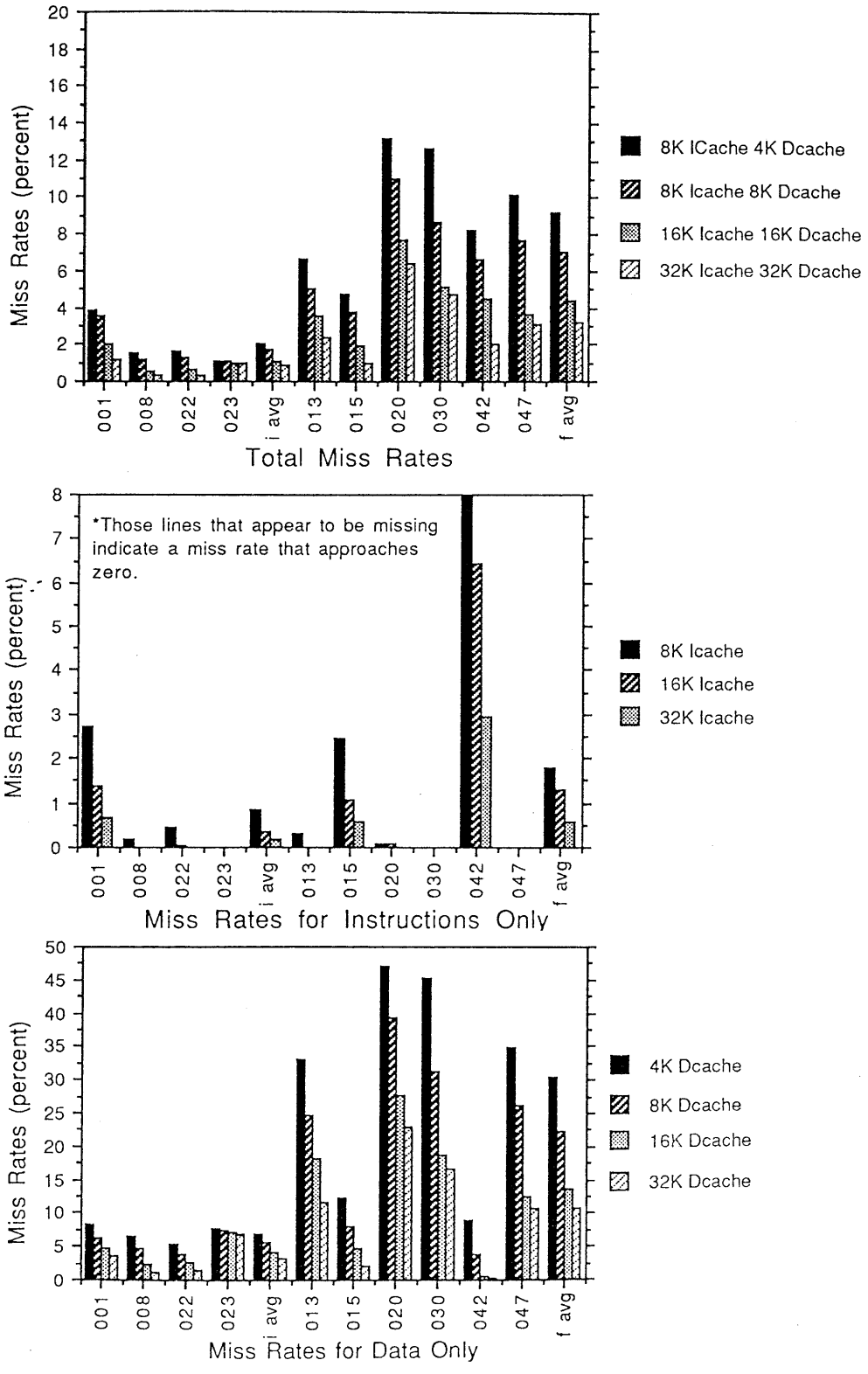
All three schemes improved the performance of a microprocessor. While page mode DRAMs showed the least improvement, they are the most readily available. Register-based cache DRAMS and cache DRAMs with embedded SRAMs were significantly better, but they are not yet commodity parts. Perhaps the most interesting result shown by the simulations was that the second level miss rate did not degrade with increasing first level

cache sizes. Based on this result, the interaction between first and second level cache sizes merits further investigation. Additionally, with the low miss rates shown in the simulations, page mode caches can provide substantial power savings in the memory system.

Appendix A

First Level Miss rates

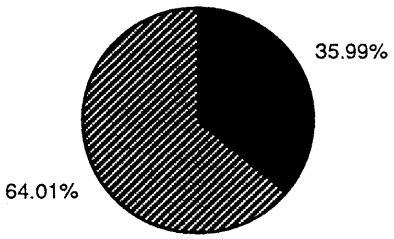
1st Level Miss Rates



Appendix B
CPI breakdown

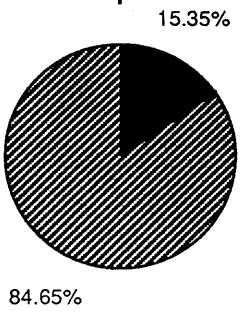
Integer CPI Components for Worst Case Configuration

001.gcc1.35



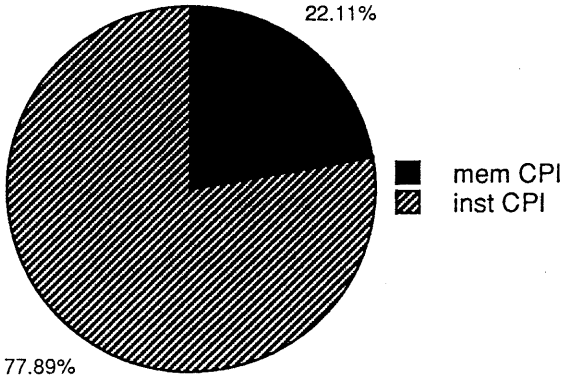
Total CPI = 1.768

008.espresso



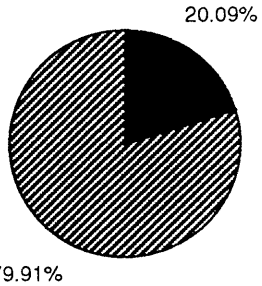
Total CPI = 1.316

Average CPI for Integer Benchmarks



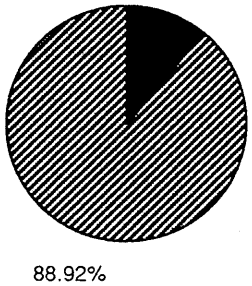
Total CPI = 1.44

022.li



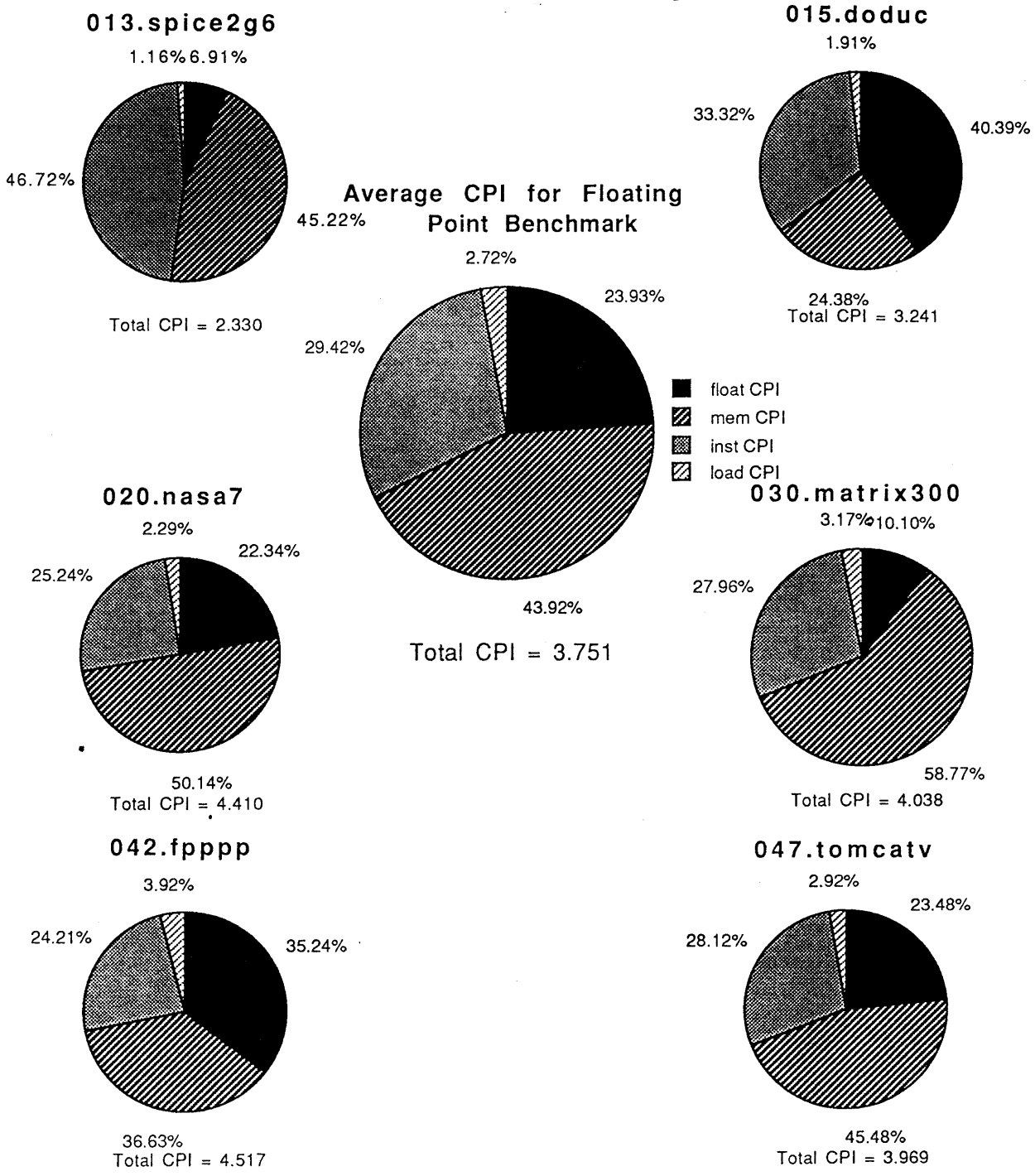
Total CPI = 1.493

023.eqntott



Total CPI = 1.193

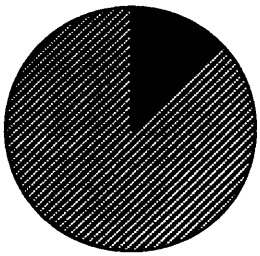
Floating Point CPI Components for Worst Case Configuration



Integer CPI Components for Largest Memory Configuration

001.gcc1.35

13.13%

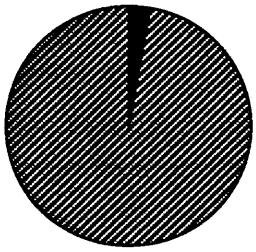


86.87%

Total CPI = 1.303

008.espresso

2.79%

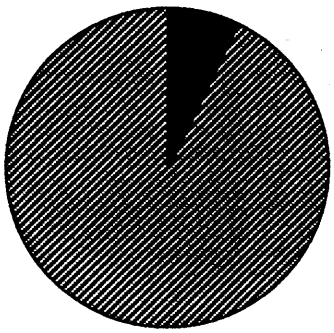


97.21%

Total CPI = 1.146

Average CPI for Integer Benchmarks

7.18%



92.82%

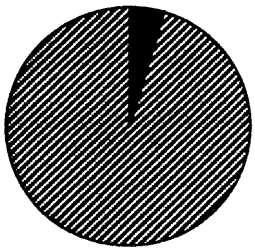
Total CPI = 1.211

mem CPI

inst CPI

022.li

4.48%

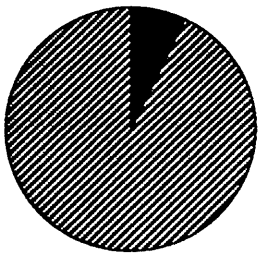


95.52%

Total CPI = 1.249

023.eqntott

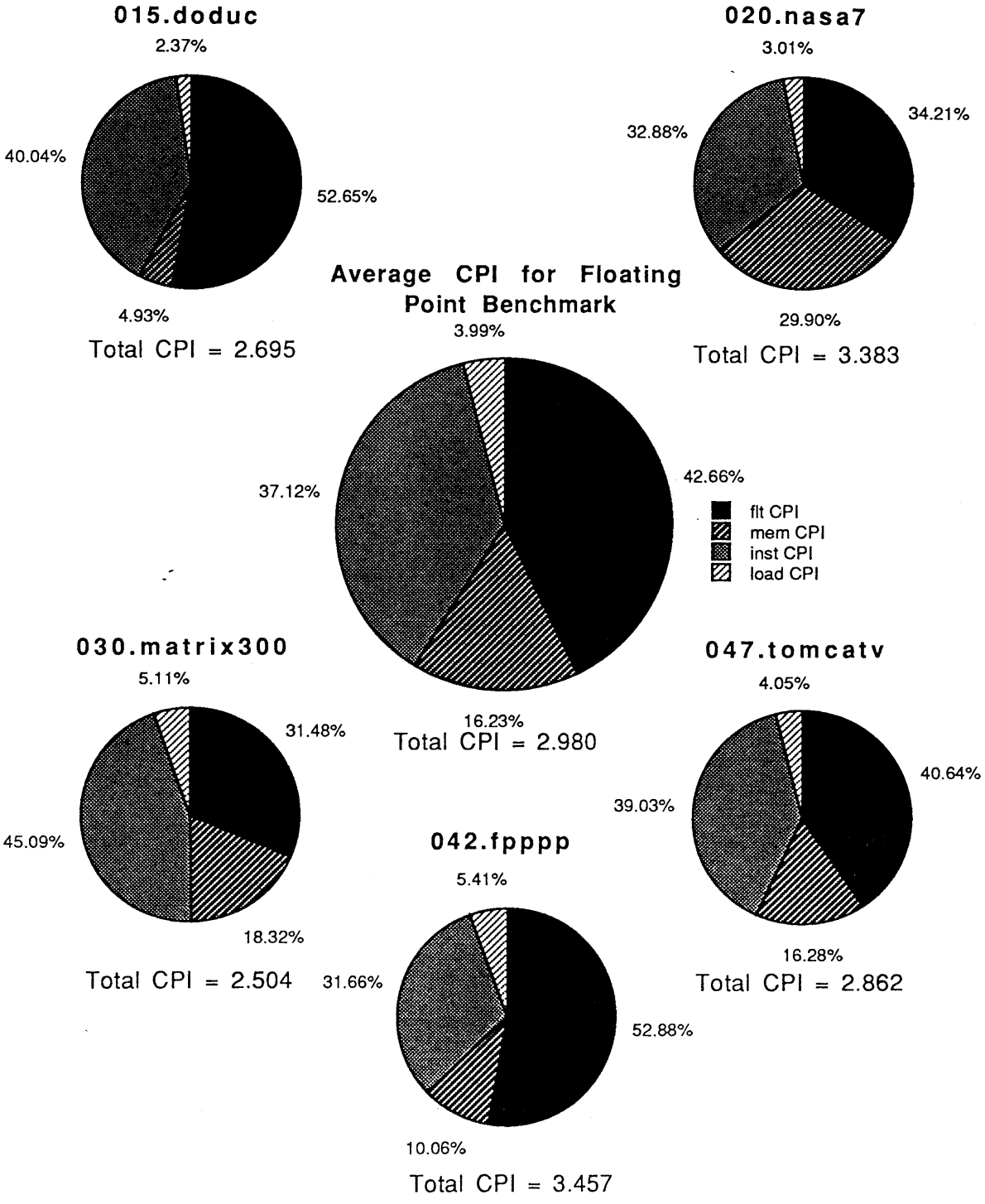
7.01%



92.99%

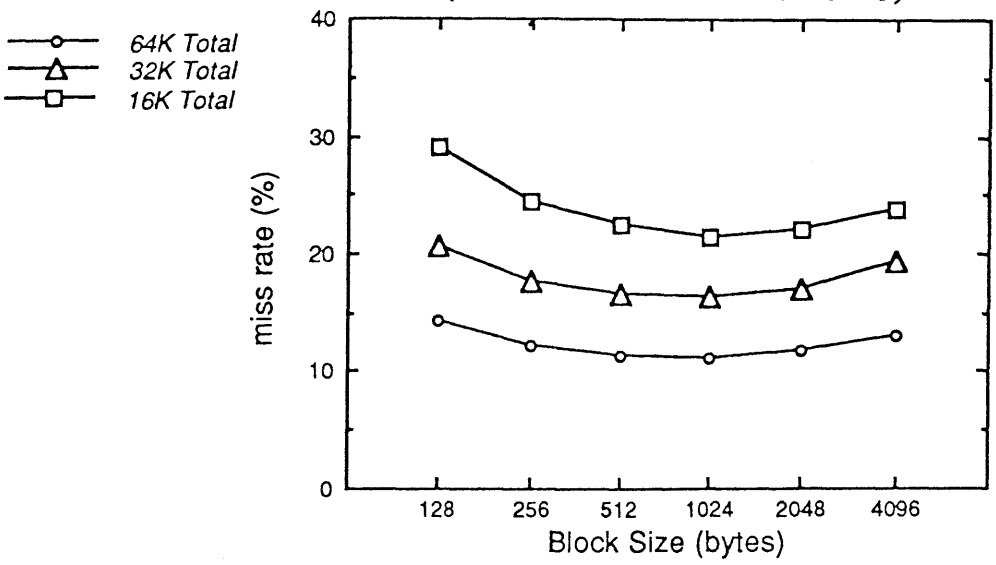
Total CPI = 1.151

Floating Point CPI Components for Largest Memory Configuration

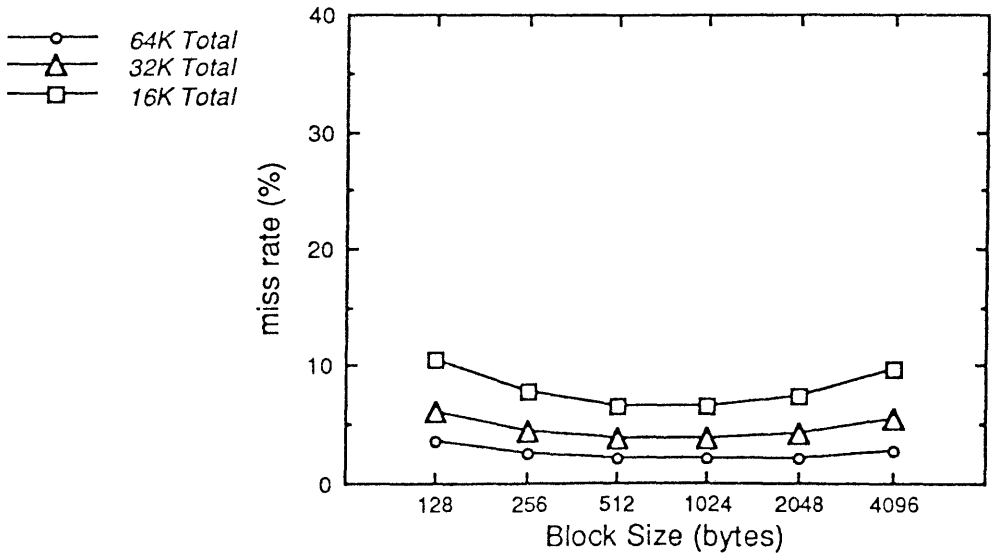


Appendix C
1st Sweep Miss Rates

2nd Level Miss Rates for 001.gcc1.35 (8K Icache 4K Dcache)

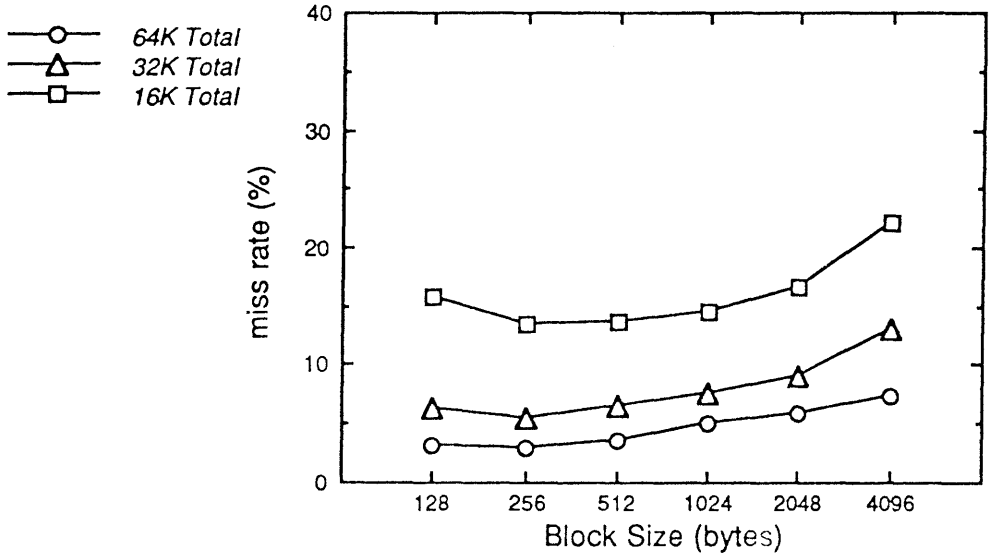


2nd Level Miss Rates for 008.espresso (8K Icache 4K Dcache)

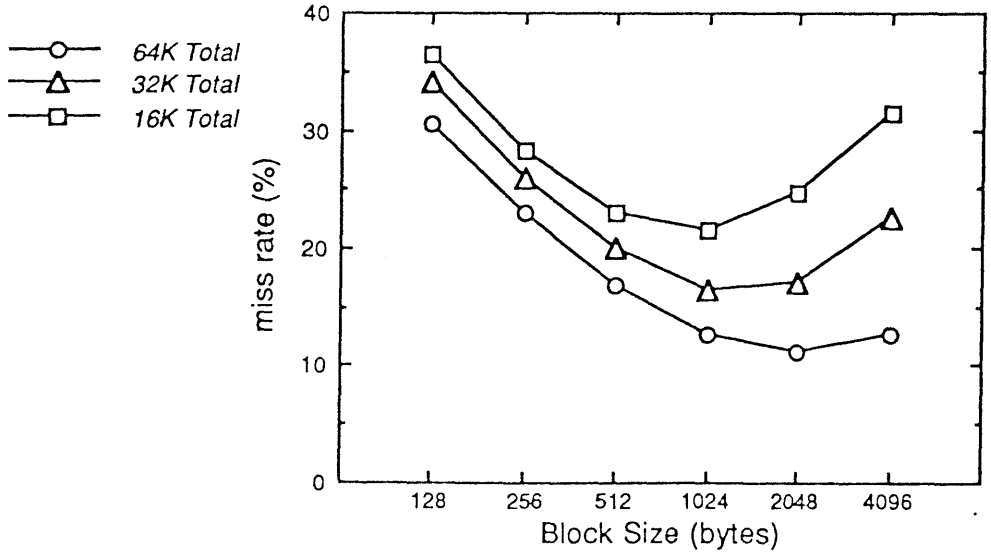


Integer Benchmarks

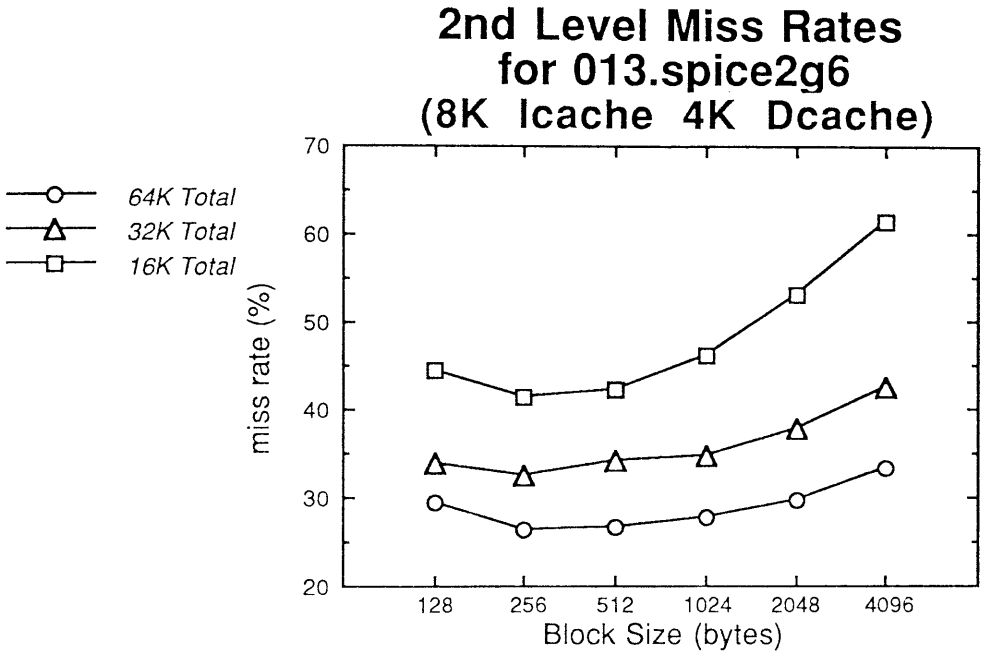
2nd Level Miss Rates for 022.li (8K Icache 4K Dcache)

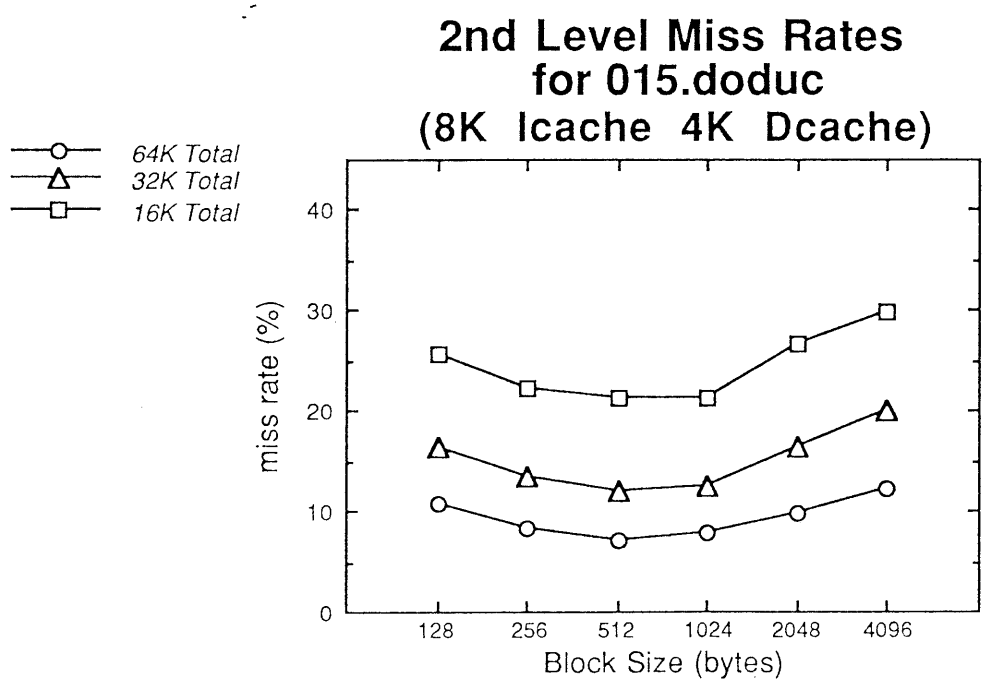


2nd Level Miss Rates for 023.eqntott (8K Icache 4K Dcache)

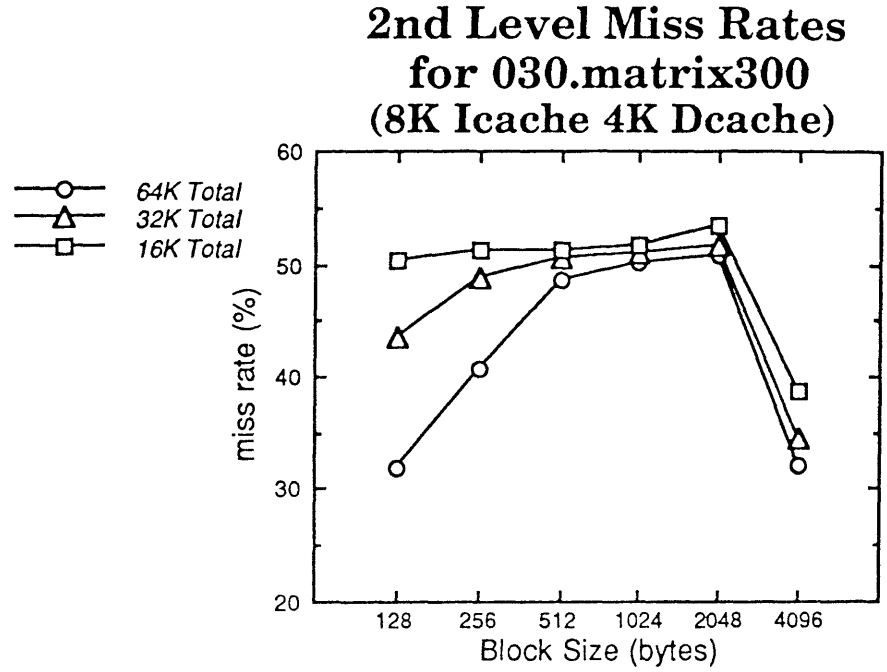


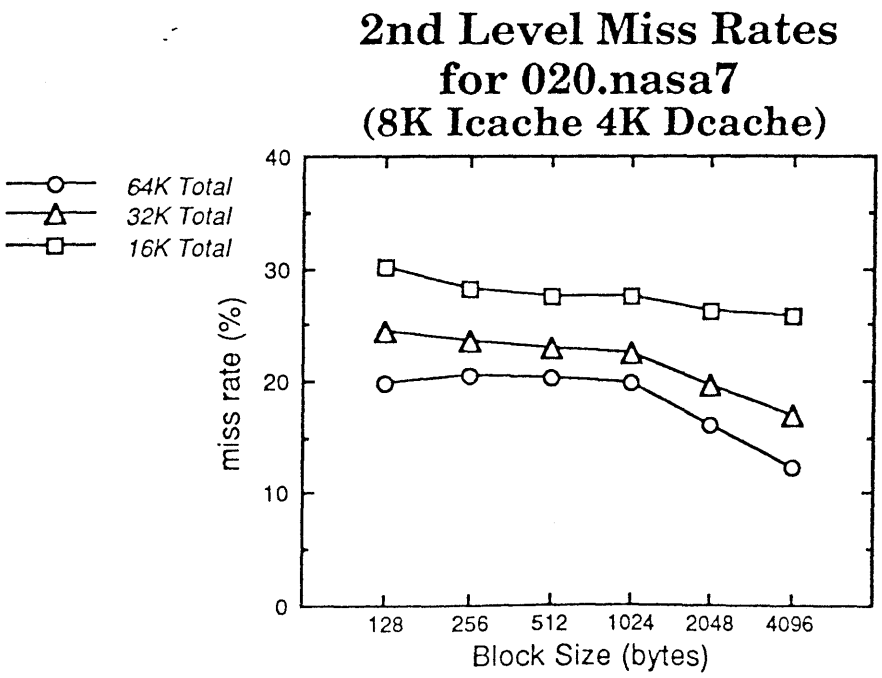
Integer Benchmarks





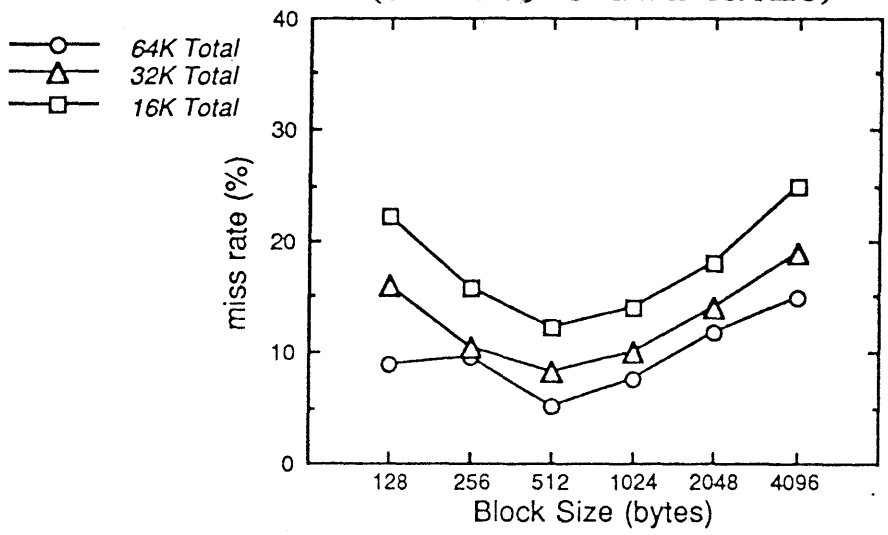
Floating Point Benchmarks



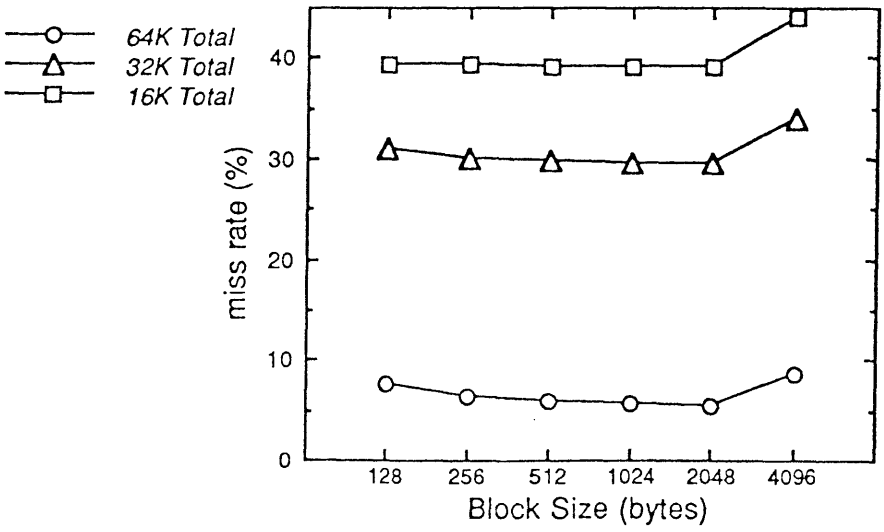


Floating Point Benchmarks

2nd Level Miss Rates for 042.fpppp (8K Icache 4K Dcache)

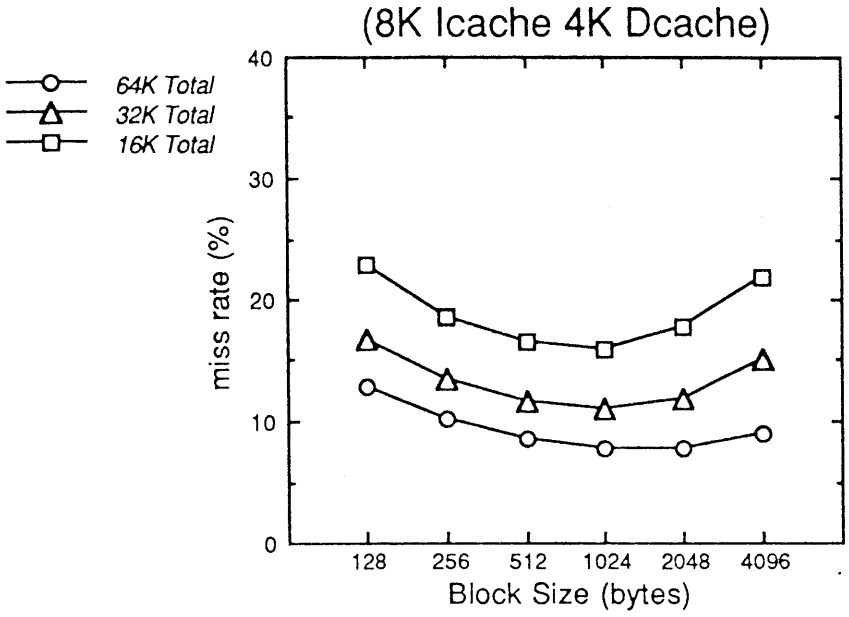


2nd Level Miss Rates for 047.tomcatv (8K Icache 4K Dcache)

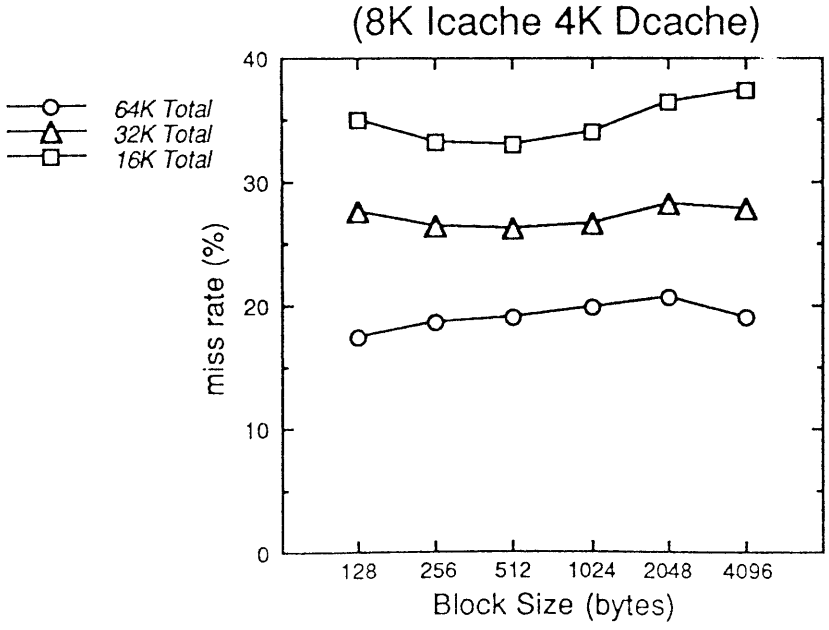


Floating Point Benchmarks

2nd Level Miss Rates for Integer Benchmarks



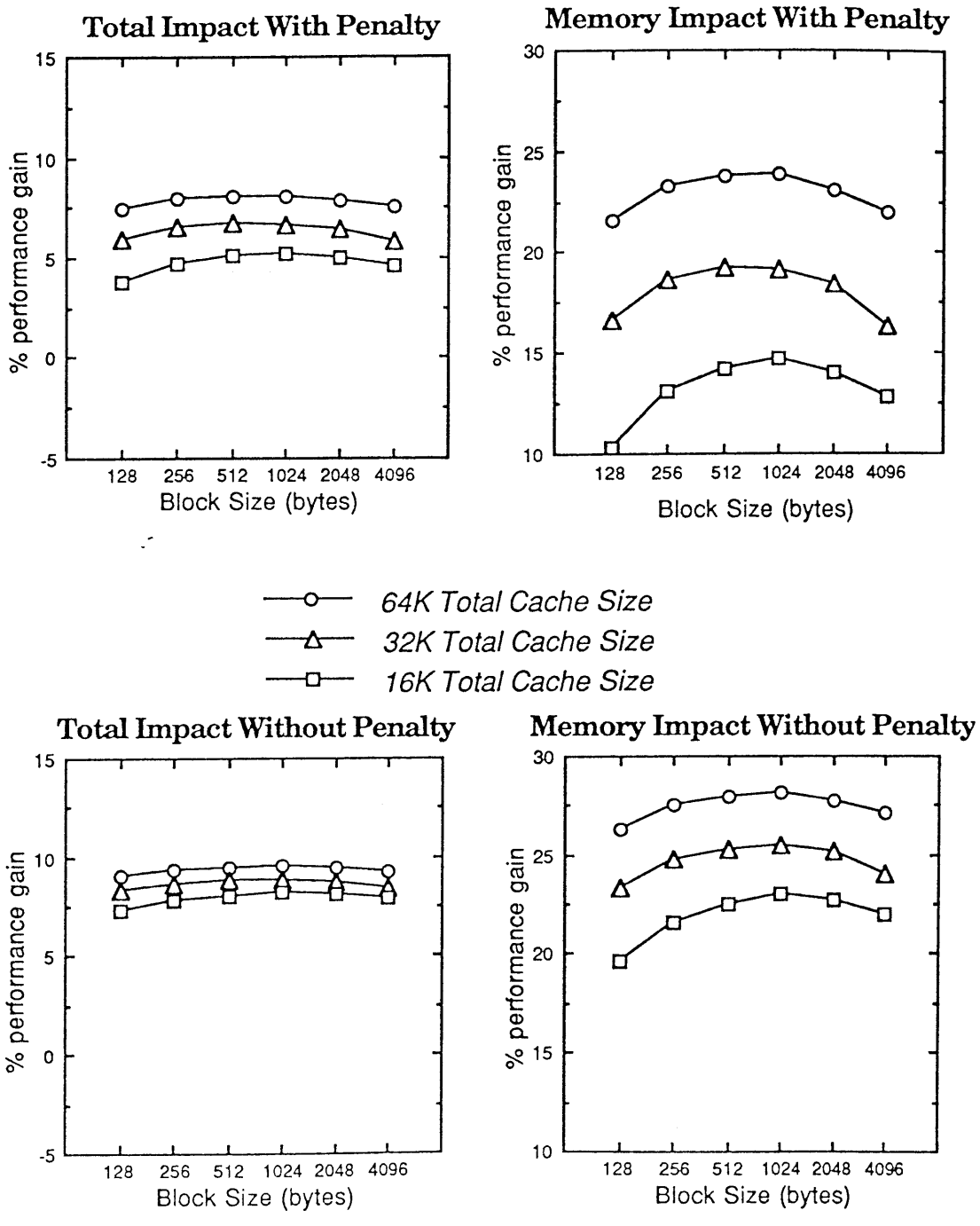
2nd Level Miss Rates for Floating Point Benchmarks



Appendix D
1st Sweep Performance Impact

Performance Impact of 2nd Level for 001.gcc1.35

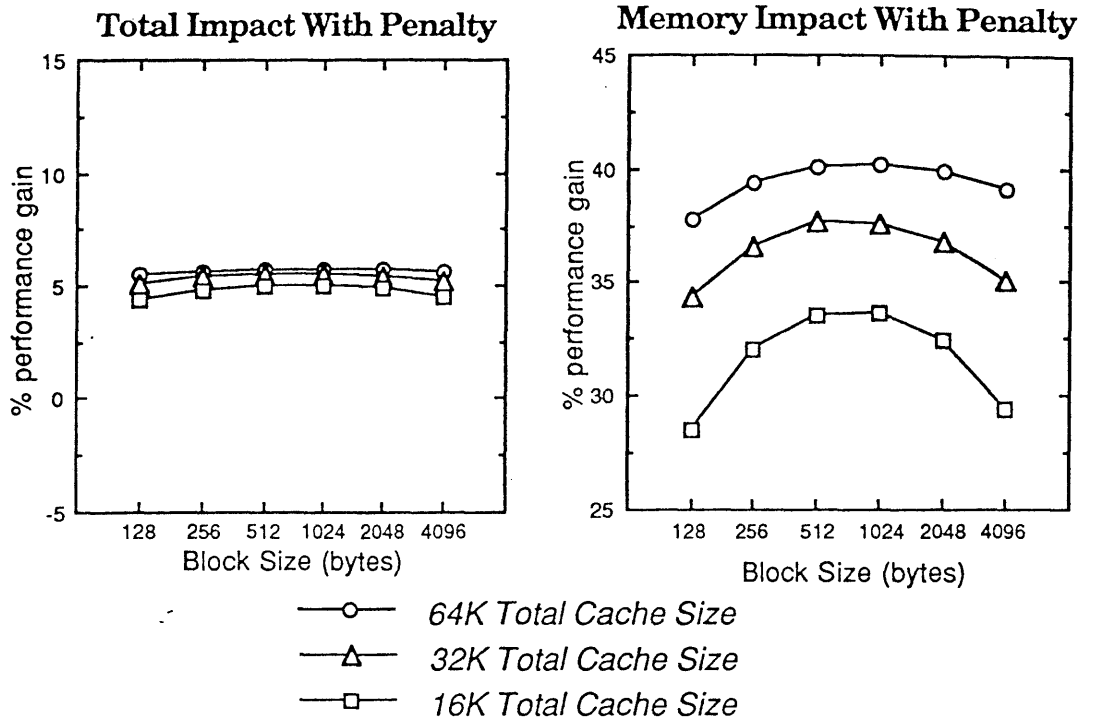
(8K Icache 4K Dcache)

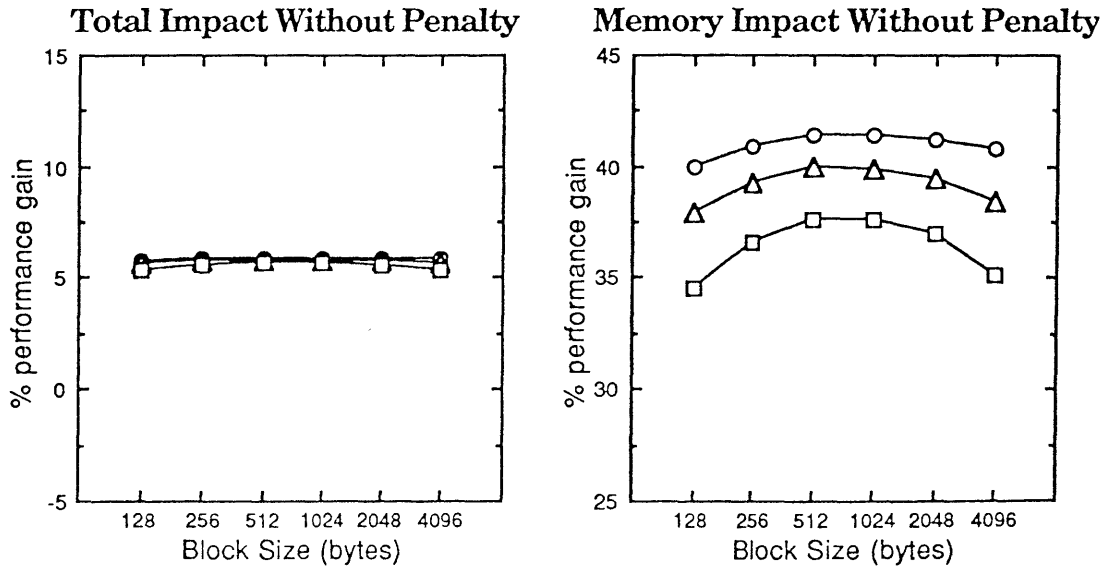


Integer Benchmark

Performance Impact of 2nd Level for 008.espresso

(8K Icache 4K Dcache)

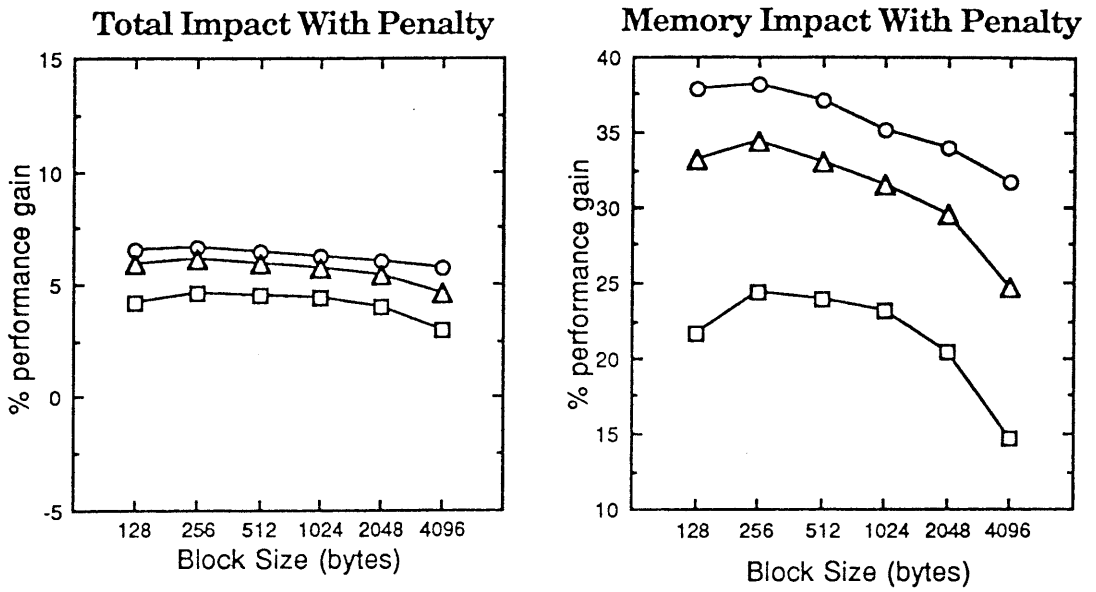




Integer Benchmark

Performance Impact of 2nd Level for 022.li

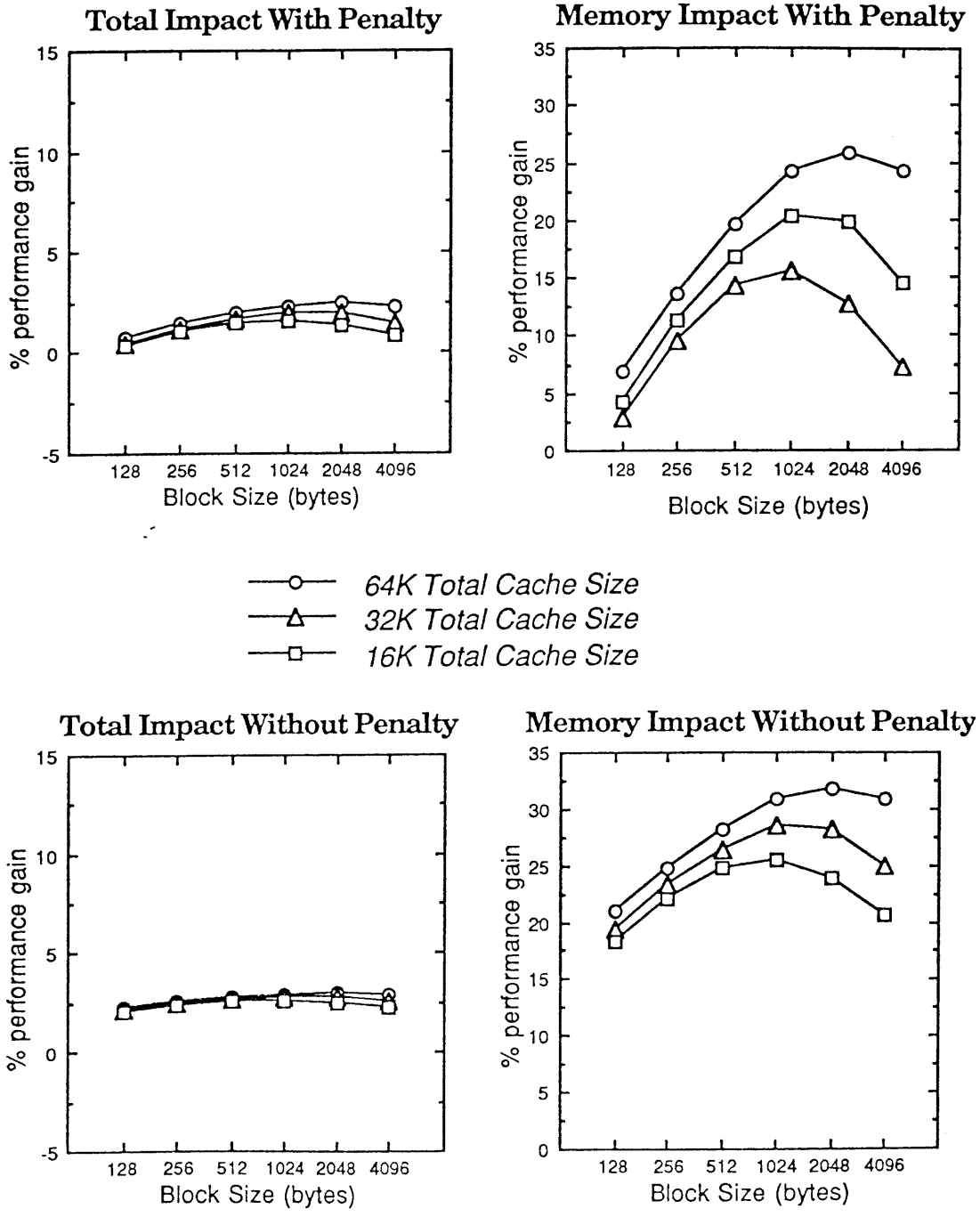
(8K Icache 4K Dcache)



Integer Benchmark

Performance Impact of 2nd Level for 023.eqntott

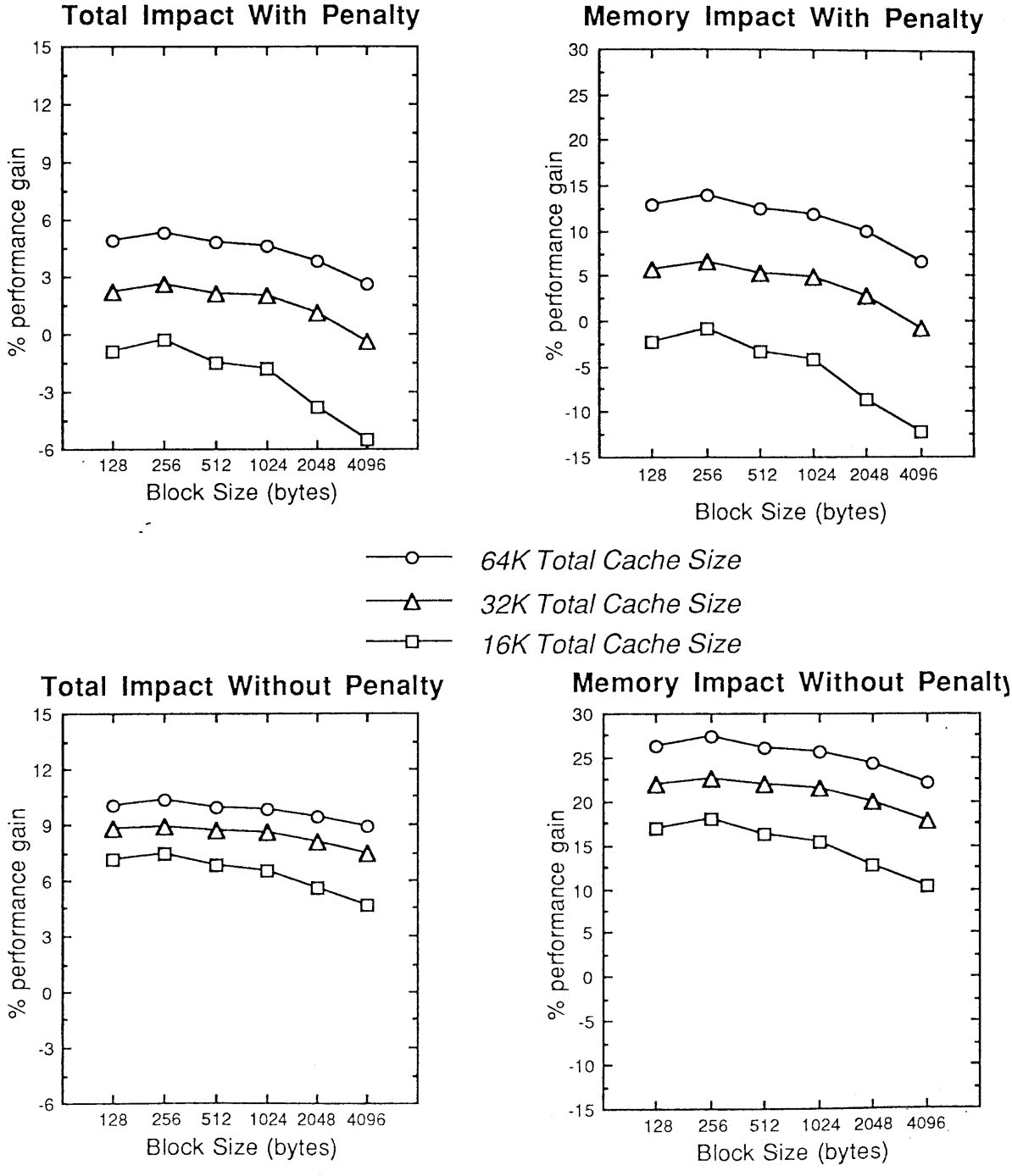
(8K Icache 4K Dcache)



Integer Benchmark

Performance Impact of 2nd Level for 013.spice2g6

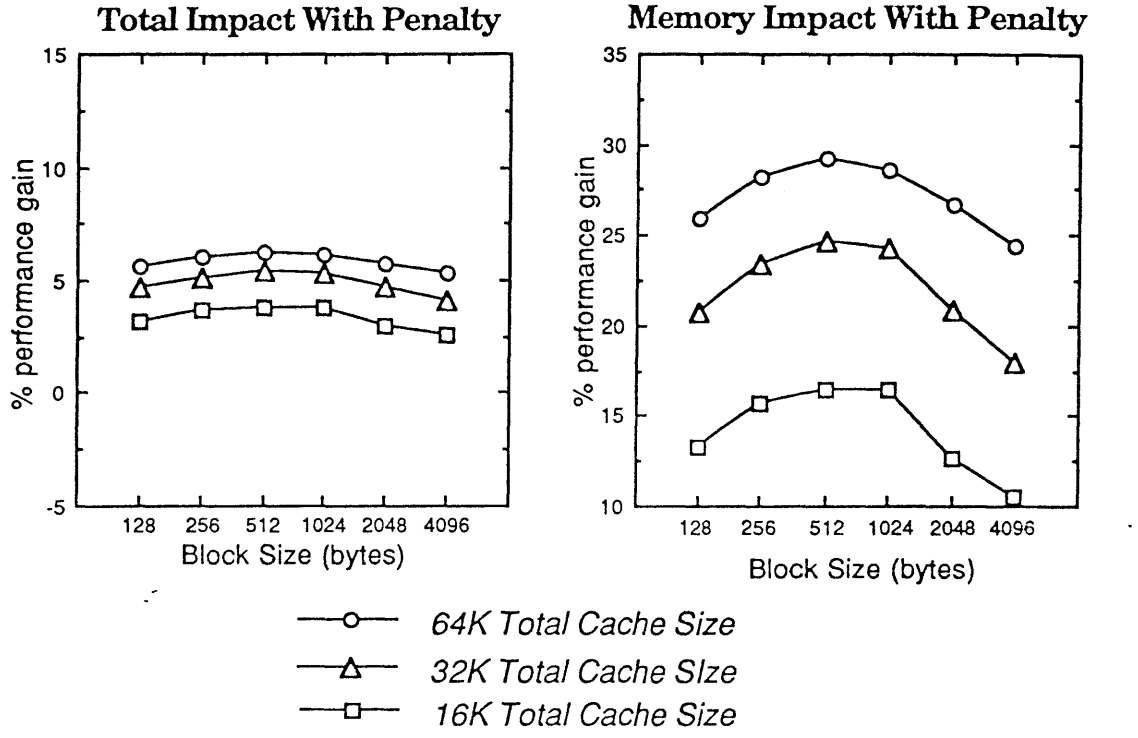
(8K Icache 4K Dcache)

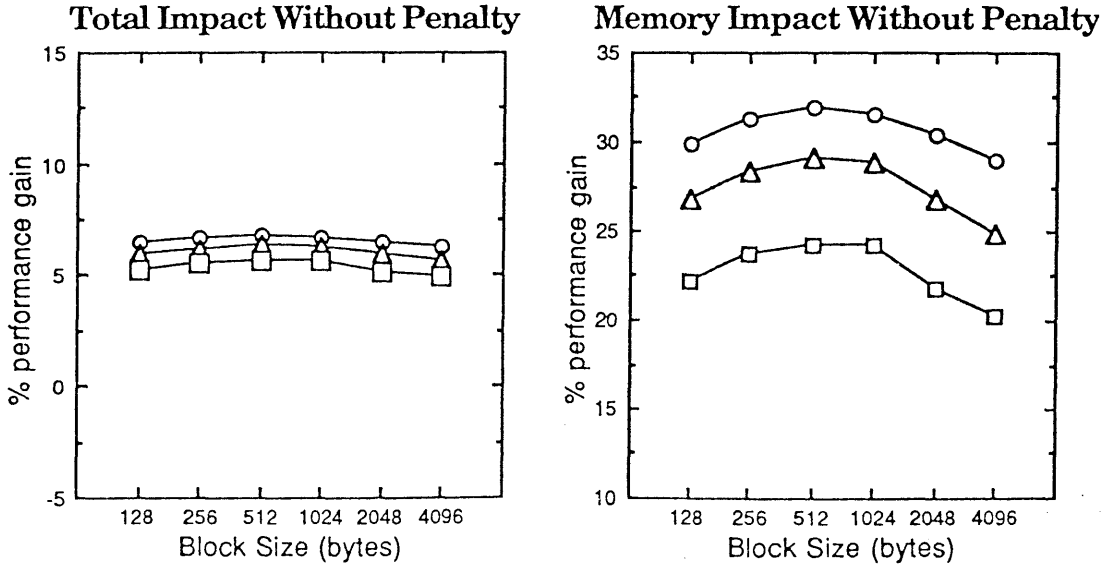


Integer Benchmark

Performance Impact of 2nd Level for 015.doduc

(8K Icache 4K Dcache)

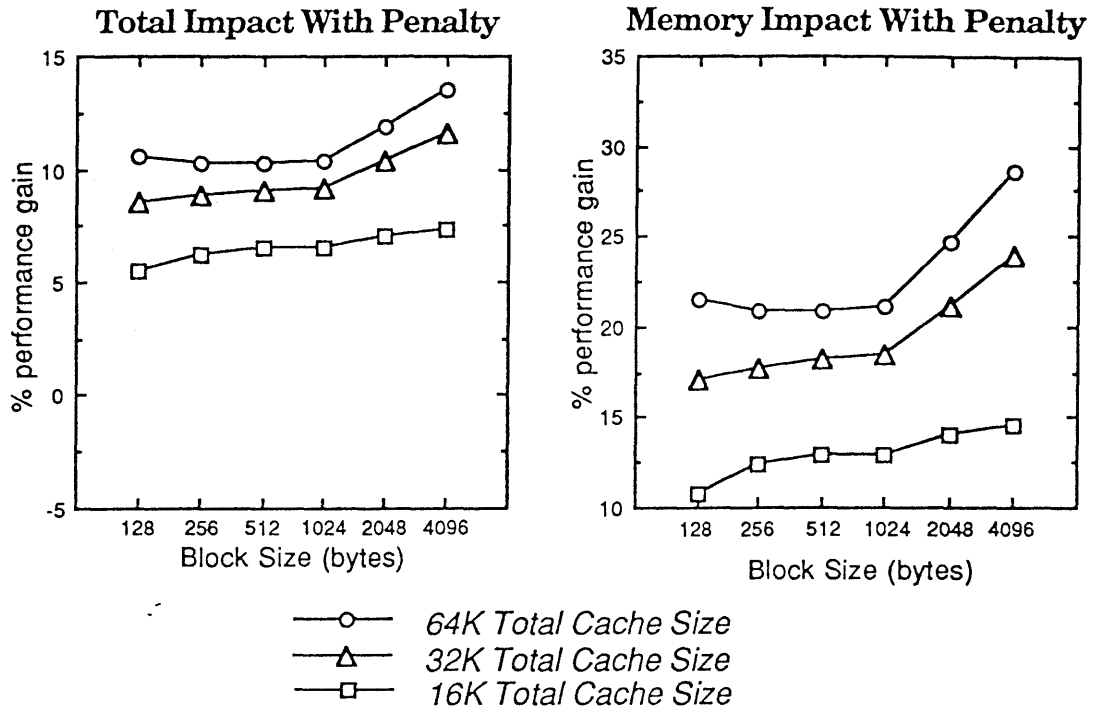


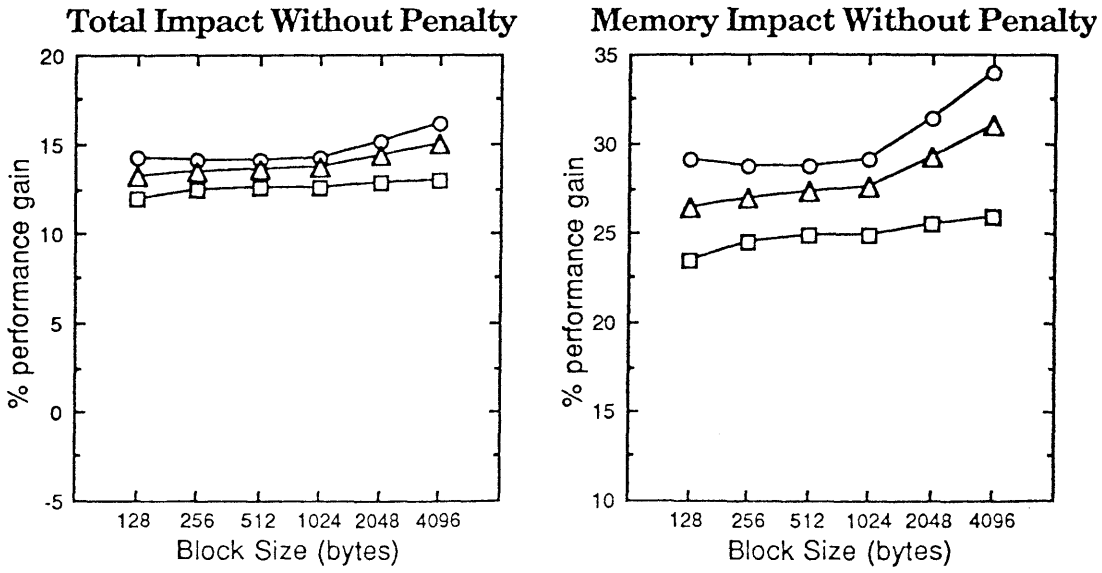


Floating Point Benchmark

Performance Impact of 2nd Level for 020.nasa7

(8K Icache 4K Dcache)

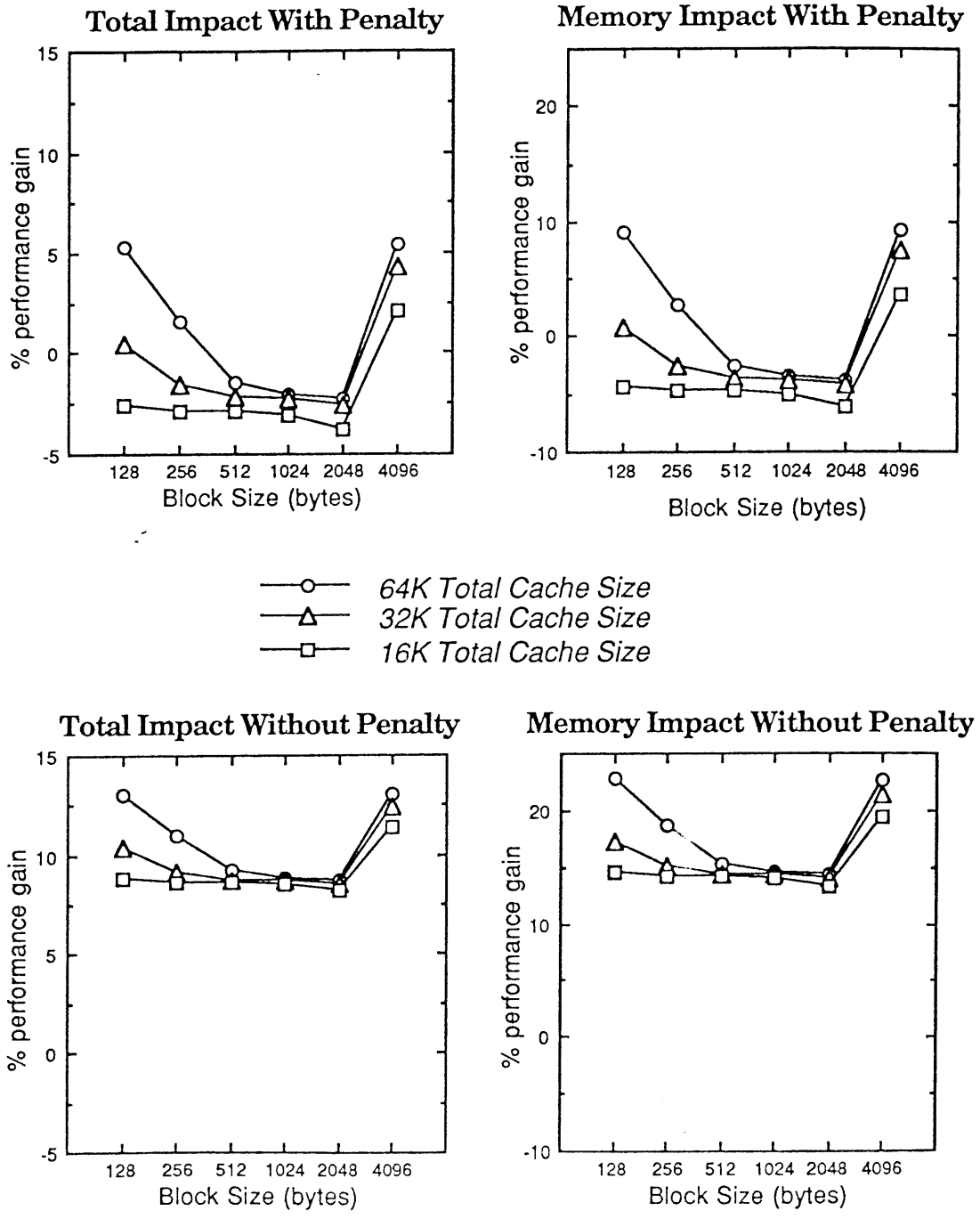




Floating Point Benchmark

Performance Impact of 2nd Level for 030.matrix300

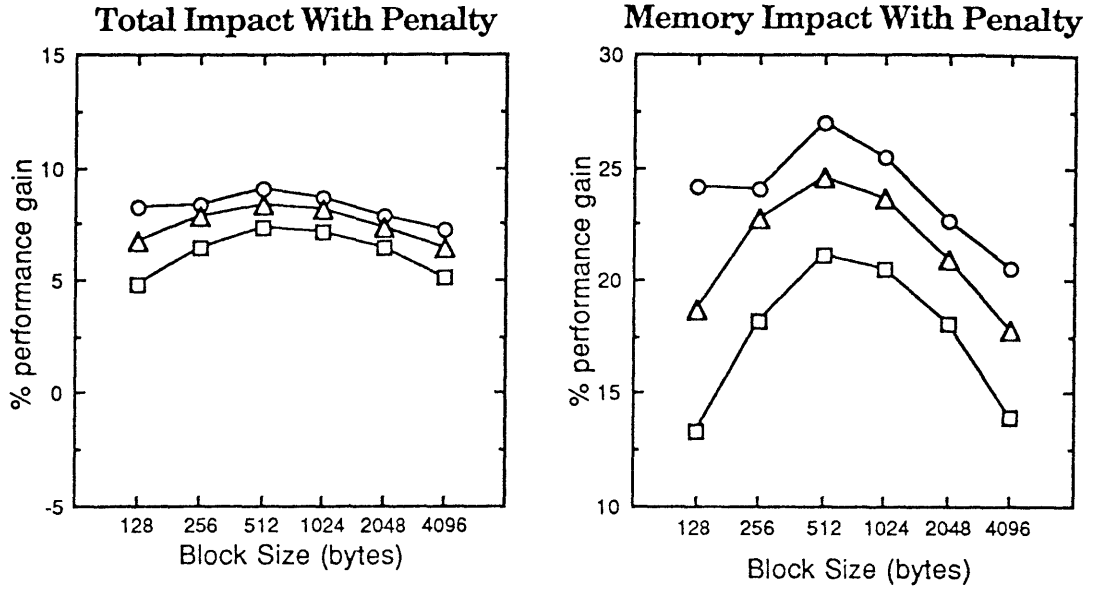
(8K Icache 4K Dcache)

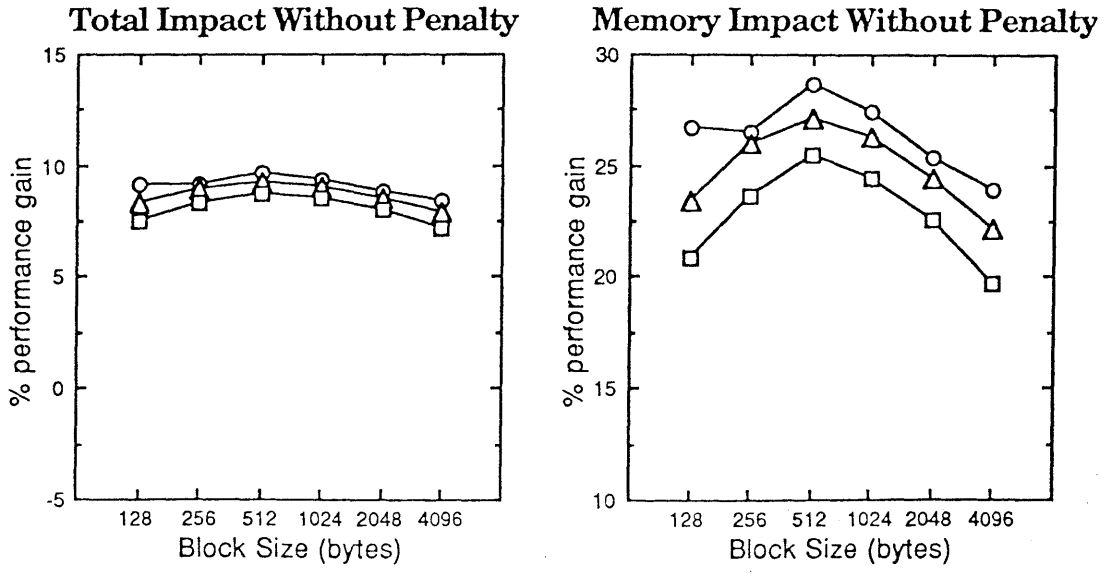


Floating Point Benchmark

Performance Impact of 2nd Level for 042.fpppp

(8K Icache 4K Dcache)

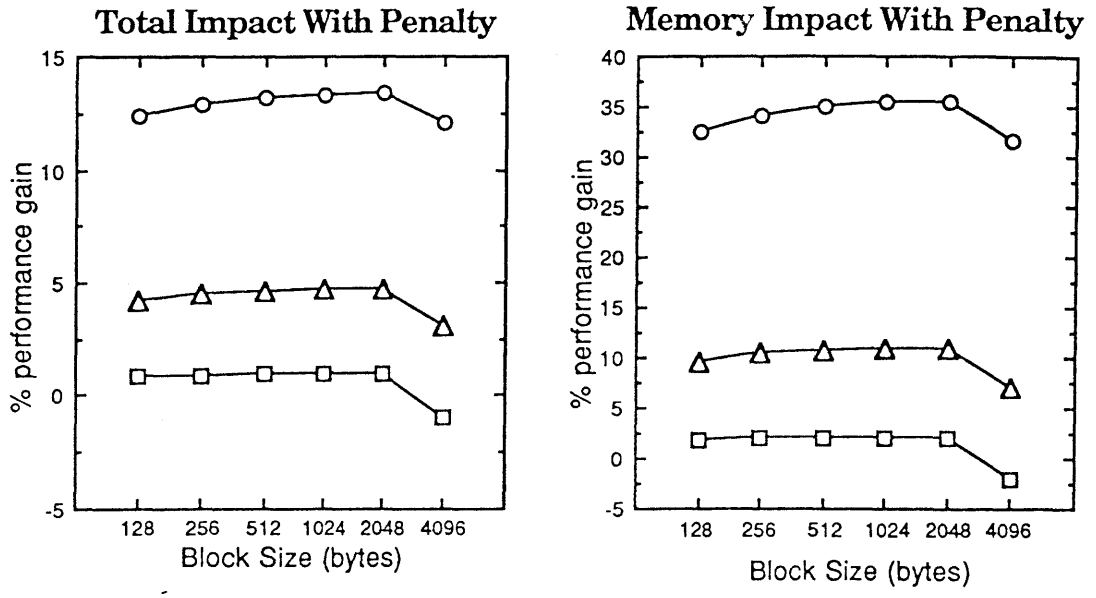


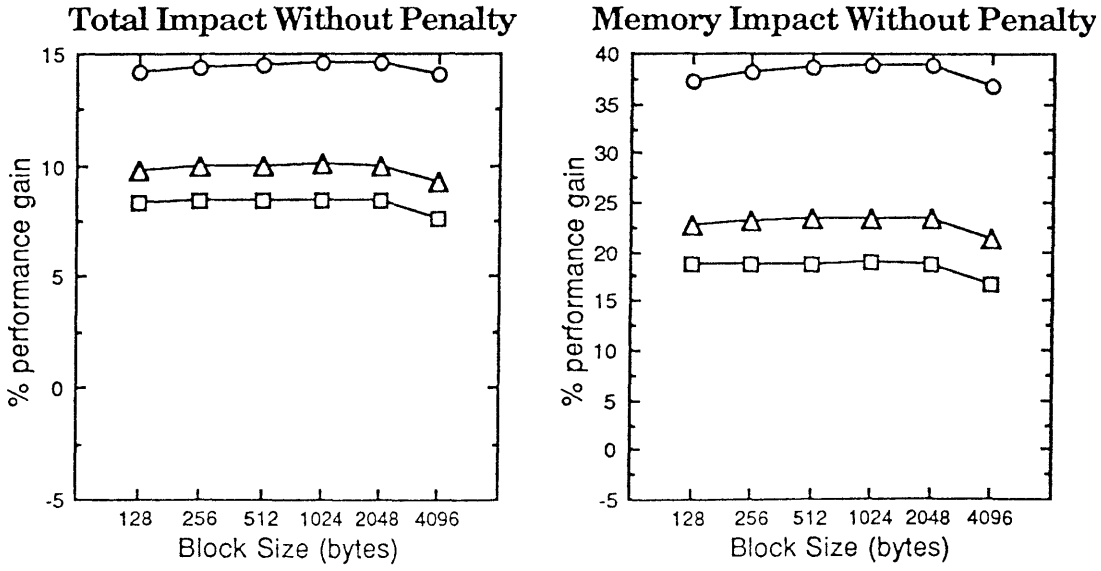


Floating Point Benchmark

Performance Impact of 2nd Level for 047.tomcatv

(8K Icache 4K Dcache)

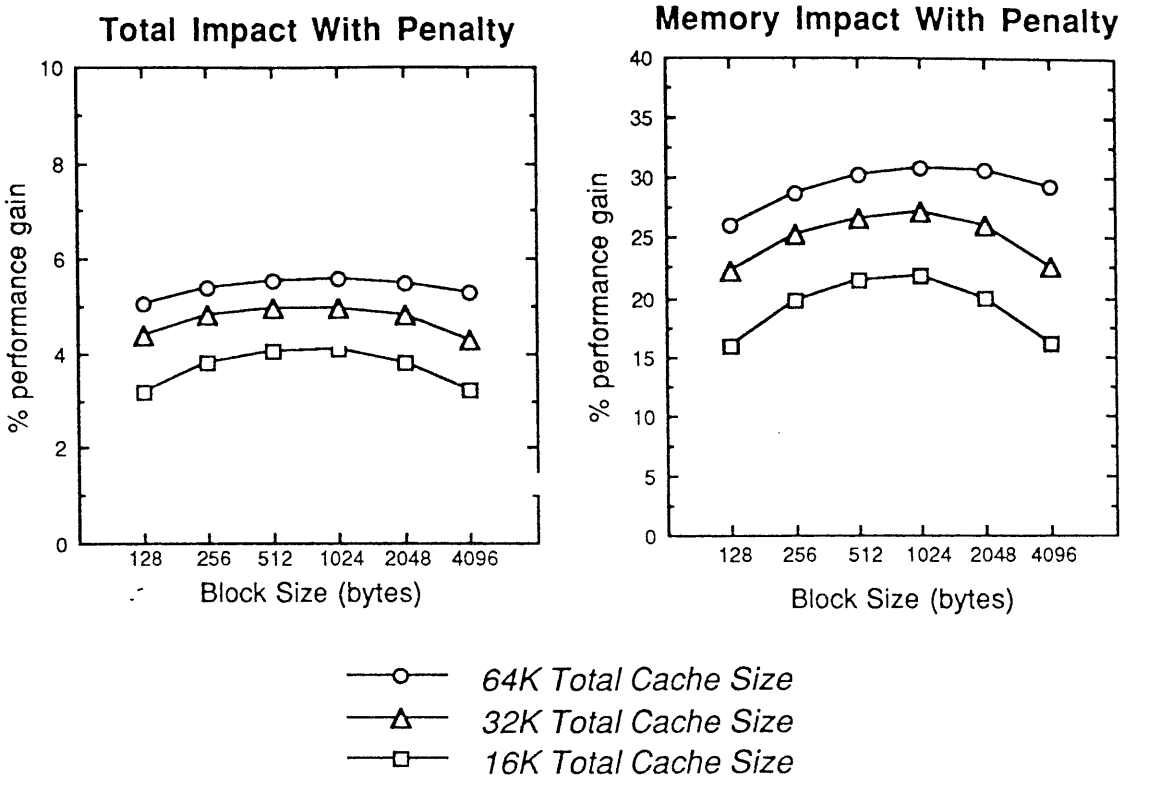


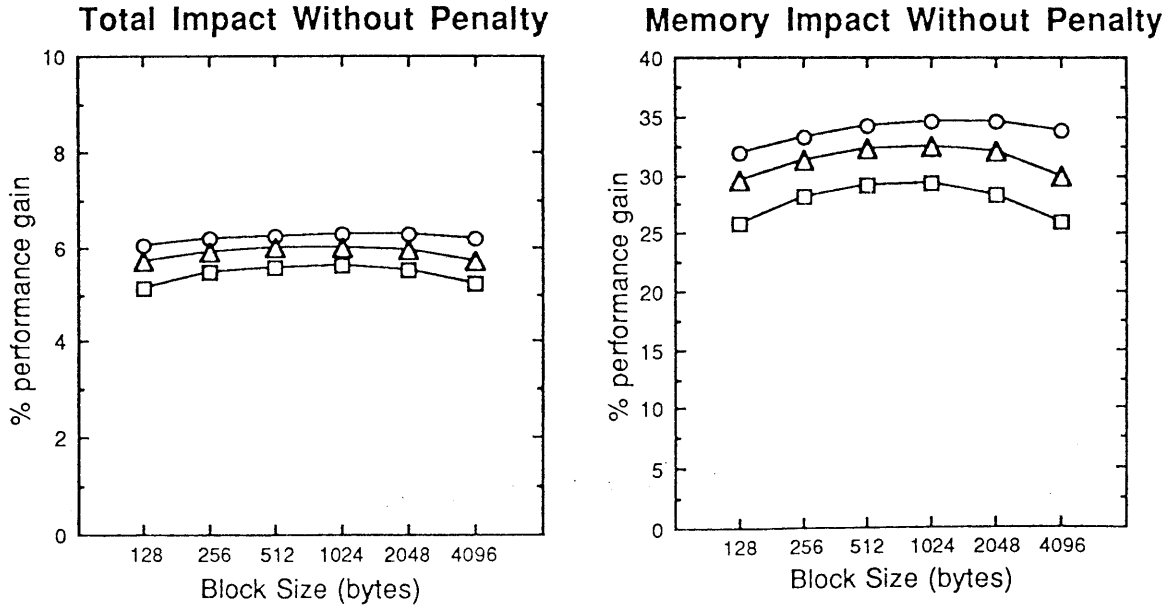


Floating Point Benchmark

Performance Impact of 2nd level for Integer Benchmarks

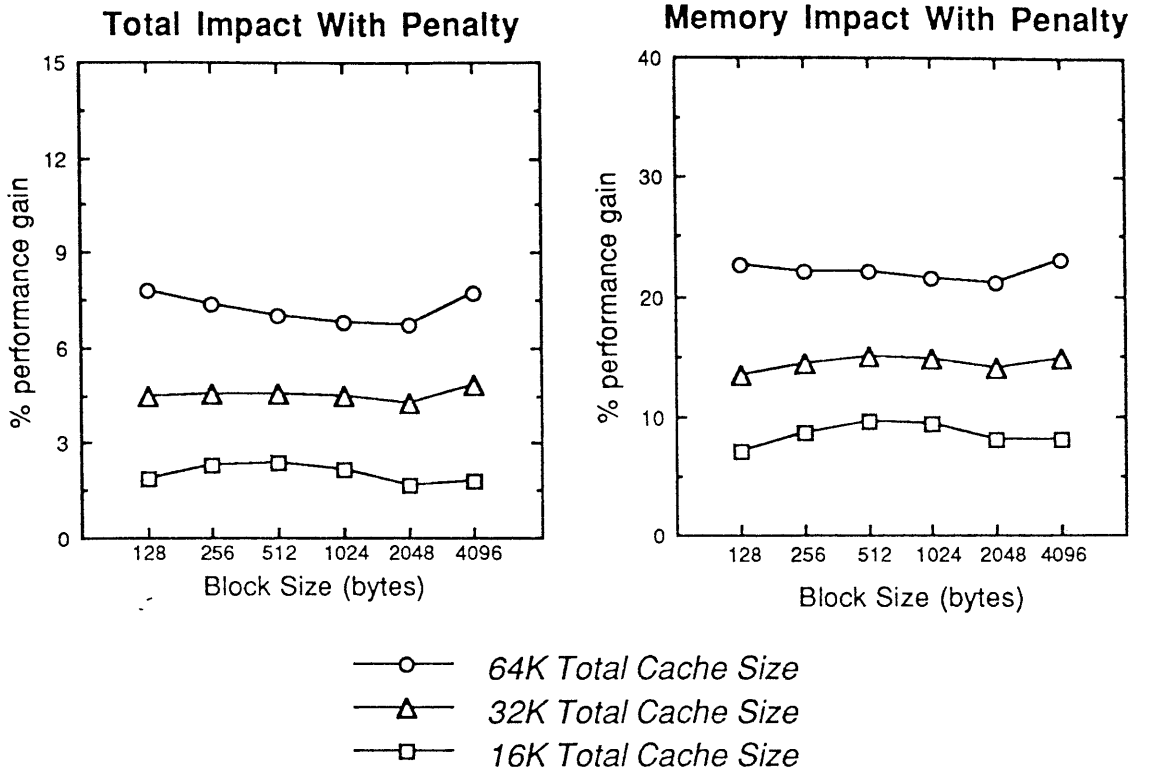
(8K Icache 4K Dcache)

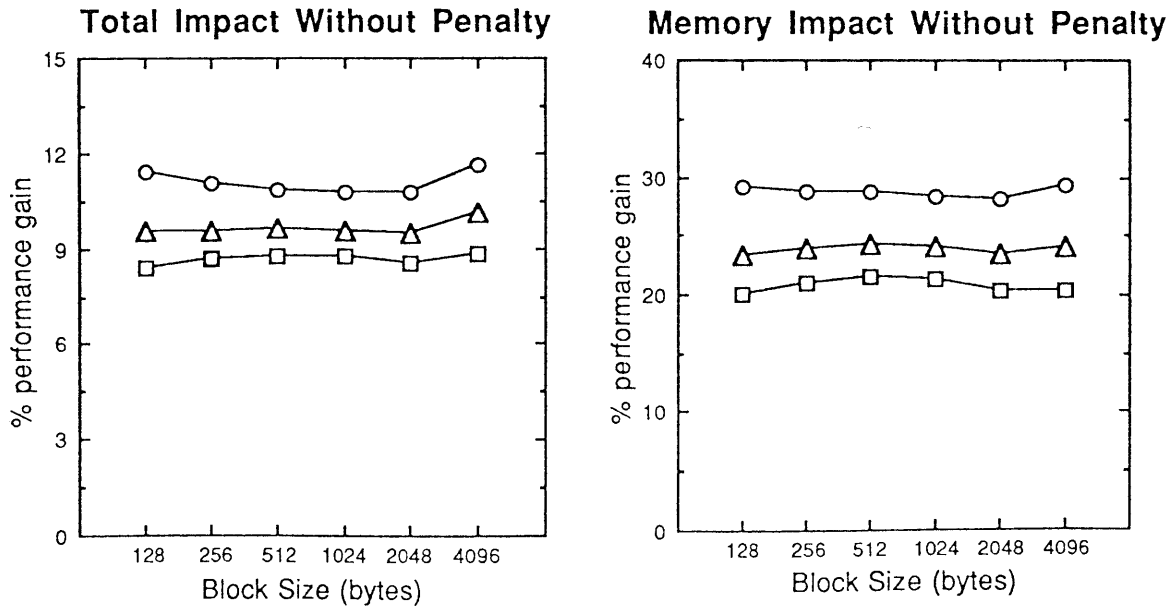




Performance Impact of 2nd level for Floating Point Benchmarks

(8K Icache 4K Dcache)

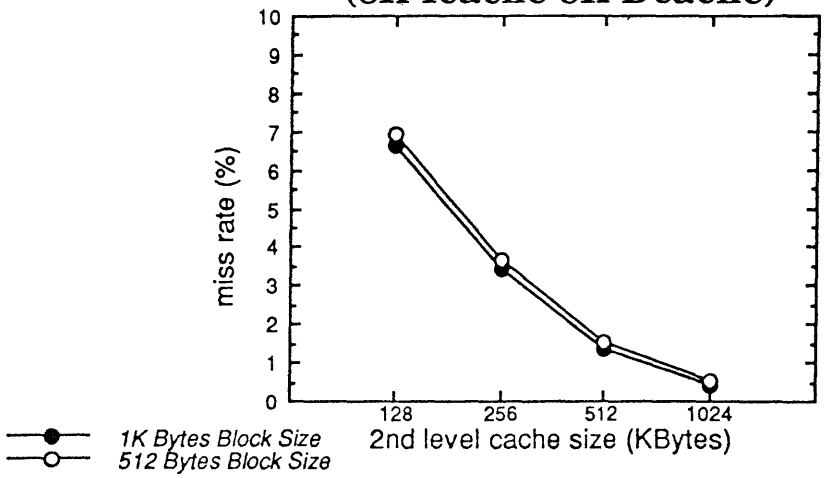




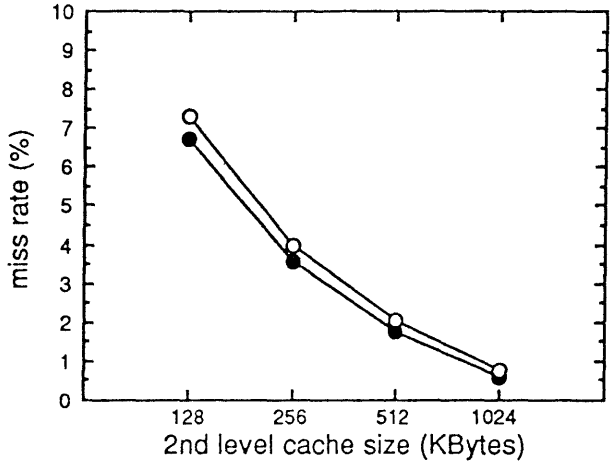
Appendix E
2nd Sweep Miss Rates

2nd Level Miss Rates for 001.gcc1.35

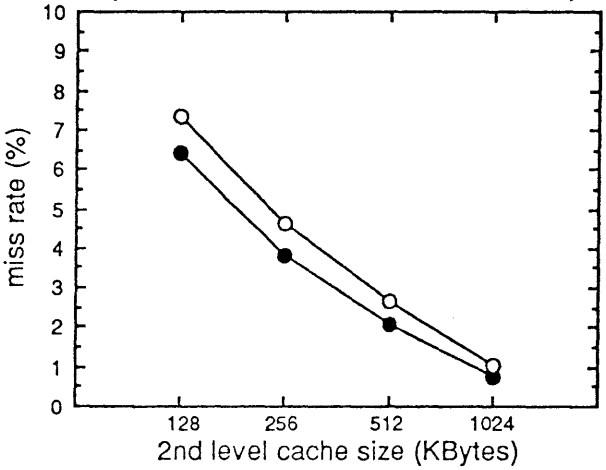
(8K Icache 8K Dcache)



(16K Icache 16K Dcache)

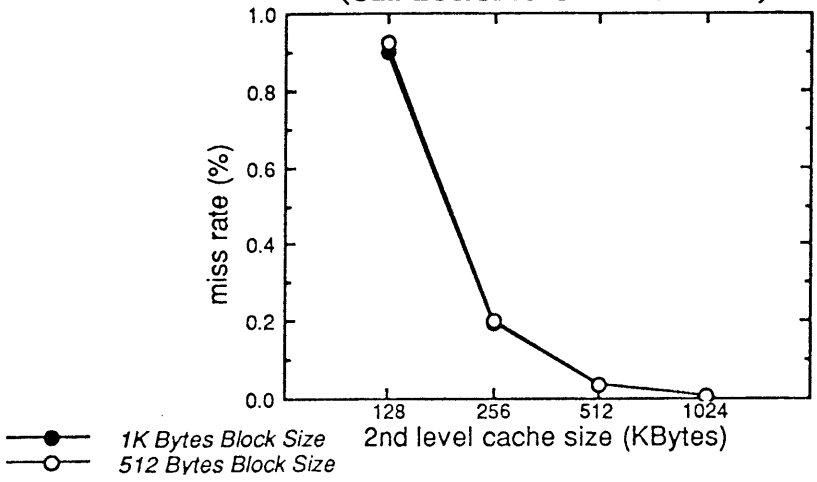


(32K Icache 32K Dcache)

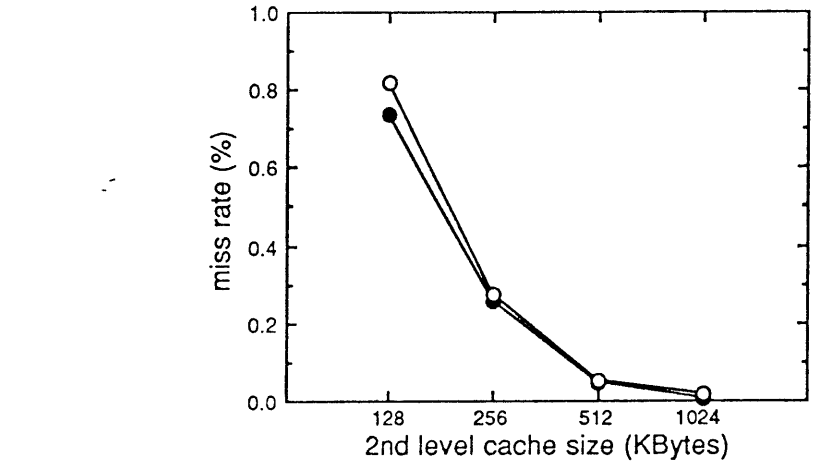


2nd Level Miss Rates for 008.espresso

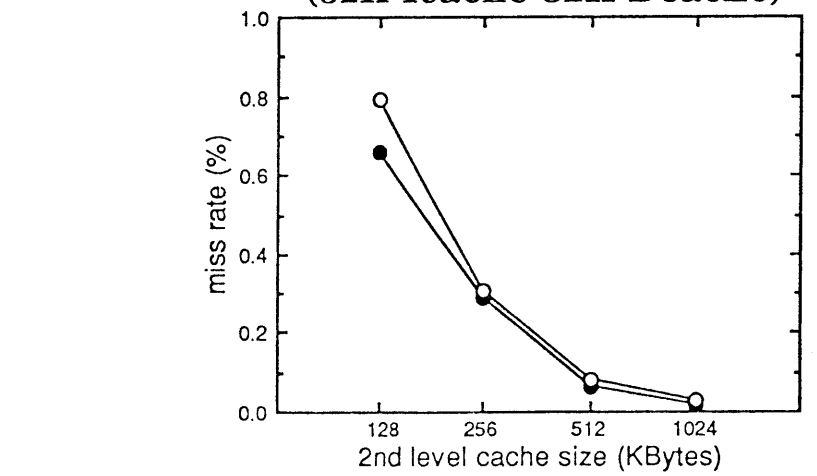
(8K Icache 8K Dcache)



(16K Icache 16K Dcache)

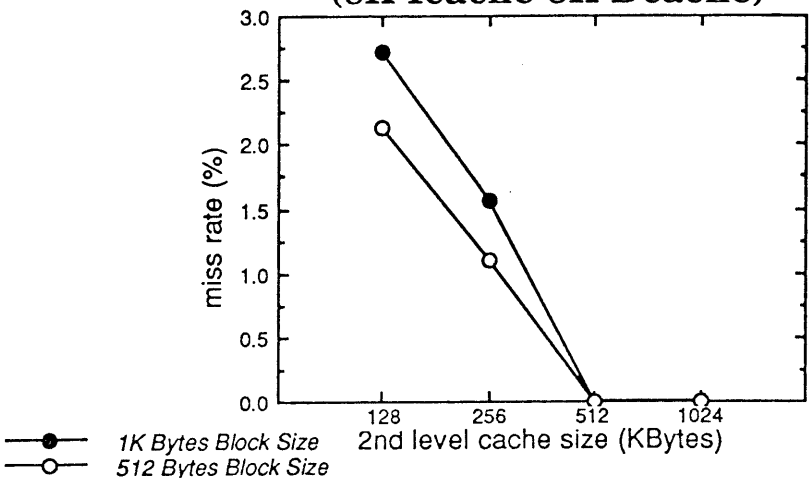


(32K Icache 32K Dcache)

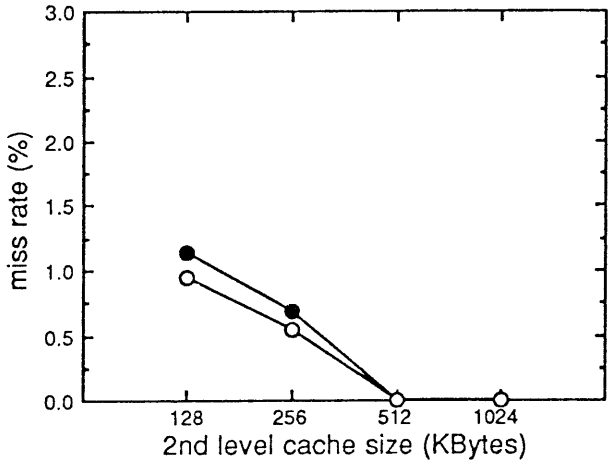


2nd Level Miss Rates for 022.li

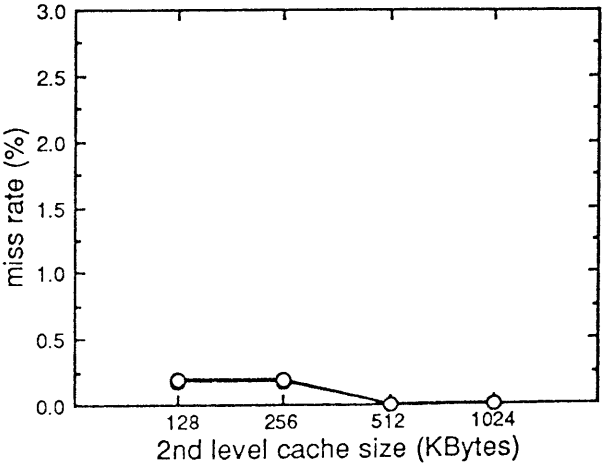
(8K Icache 8K Dcache)



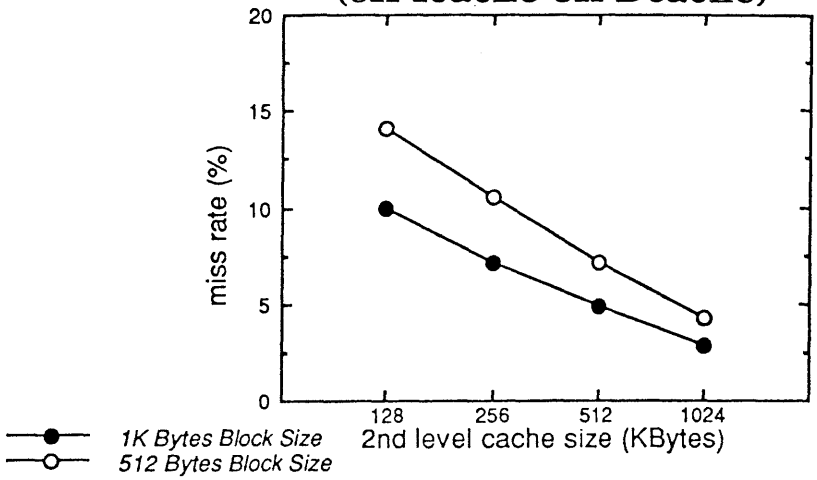
(16K Icache 16K Dcache)



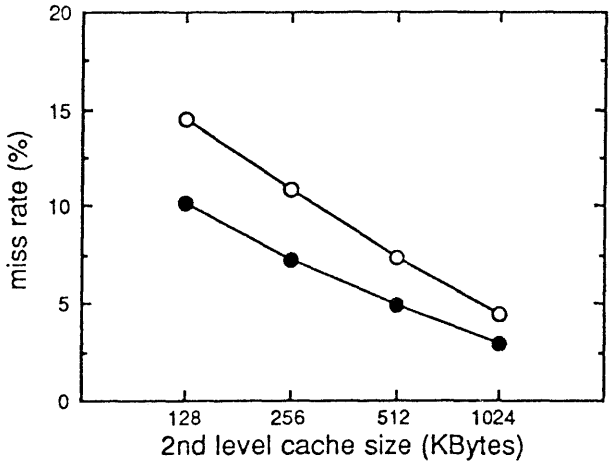
(32K Icache 32K Dcache)



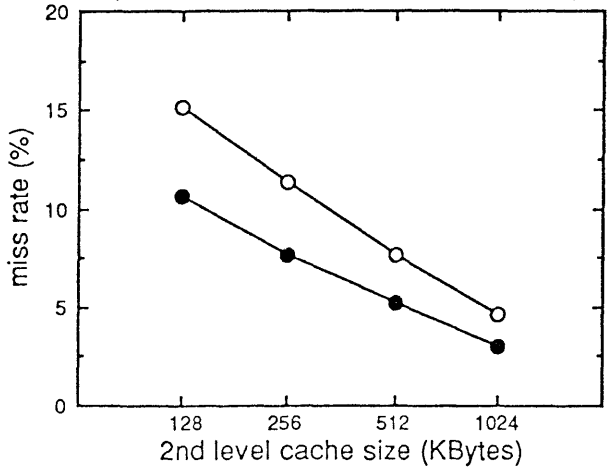
2nd Level Miss Rates for 023.eqntott (8K Icache 8K Dcache)



(16K Icache 16K Dcache)

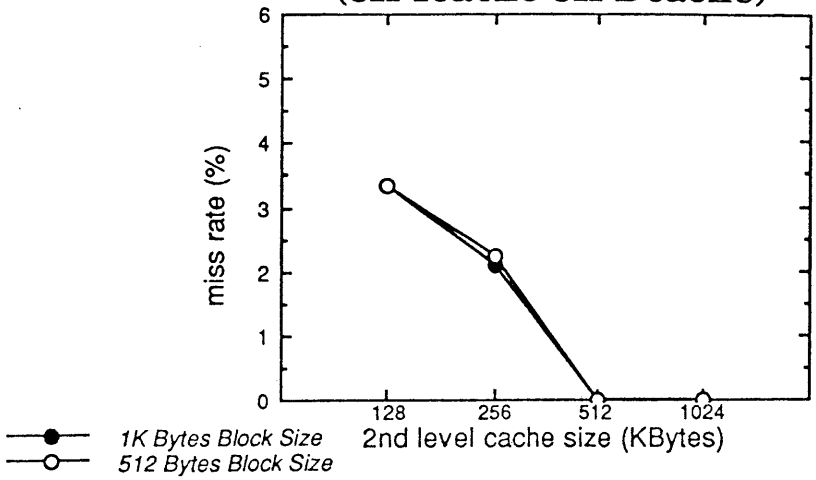


(32K Icache 32K Dcache)

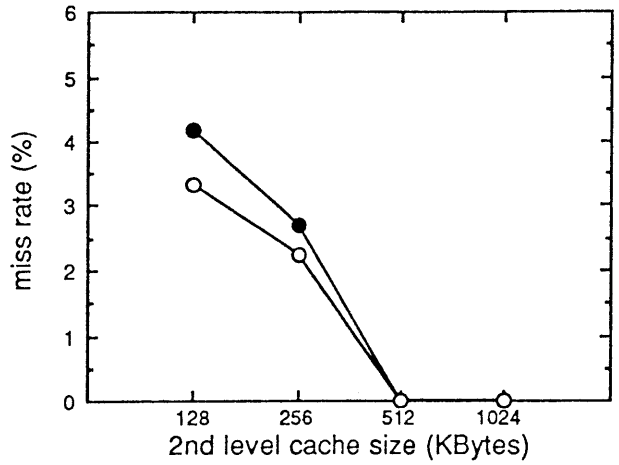


2nd Level Miss Rates for 015.doduc

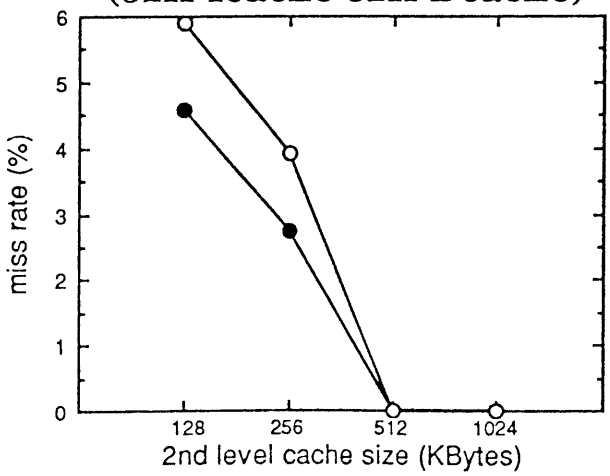
(8K Icache 8K Dcache)



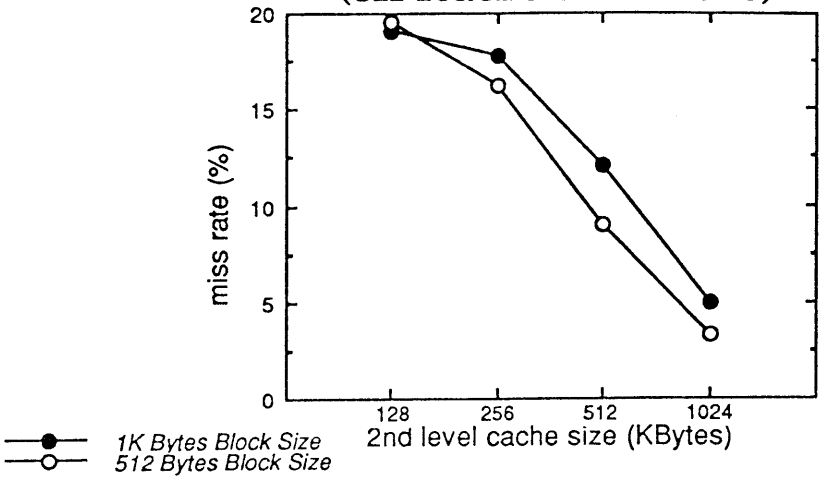
(16K Icache 16K Dcache)



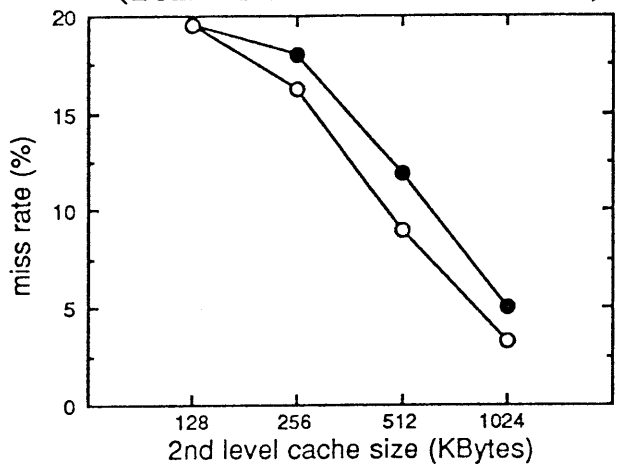
(32K Icache 32K Dcache)



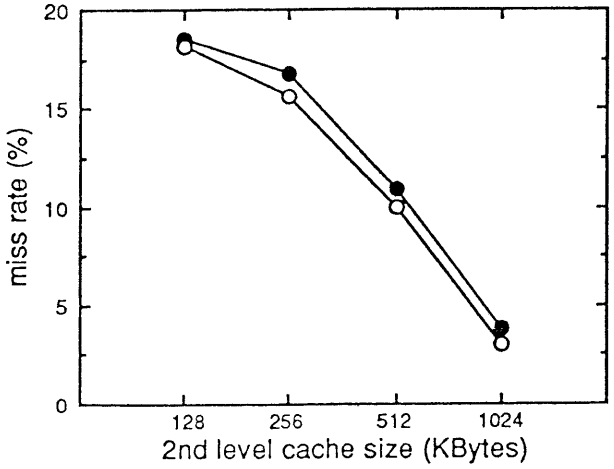
2nd Level Miss Rates for 020.nasa7 (8K Icache 8K Dcache)



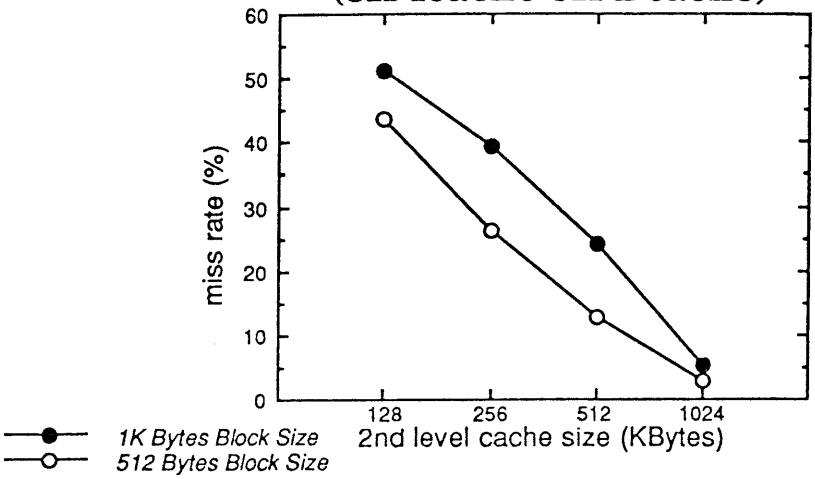
(16K Icache 16K Dcache)



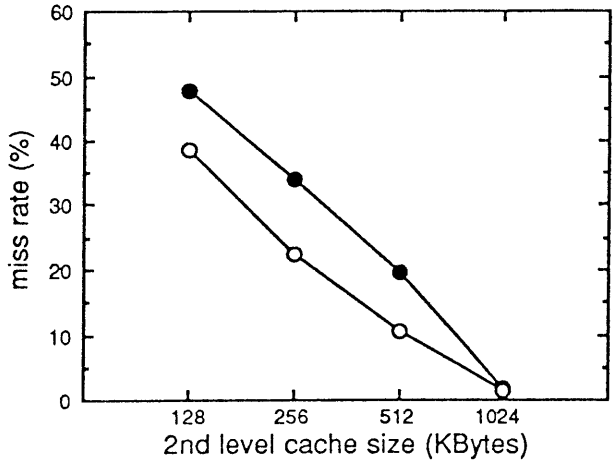
(32K Icache 32K Dcache)



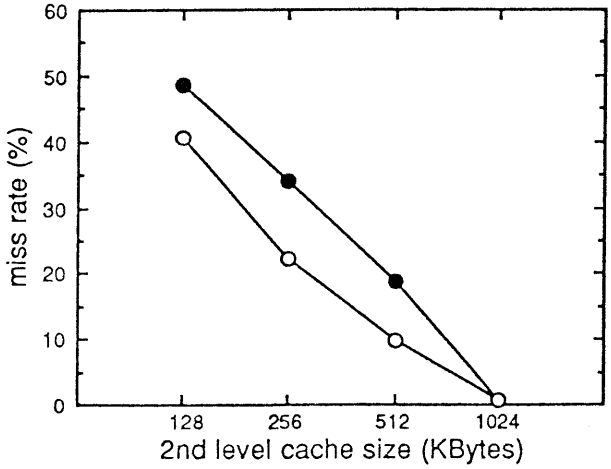
2nd Level Miss Rates for 030.matrix300 (8K Icache 8K Dcache)

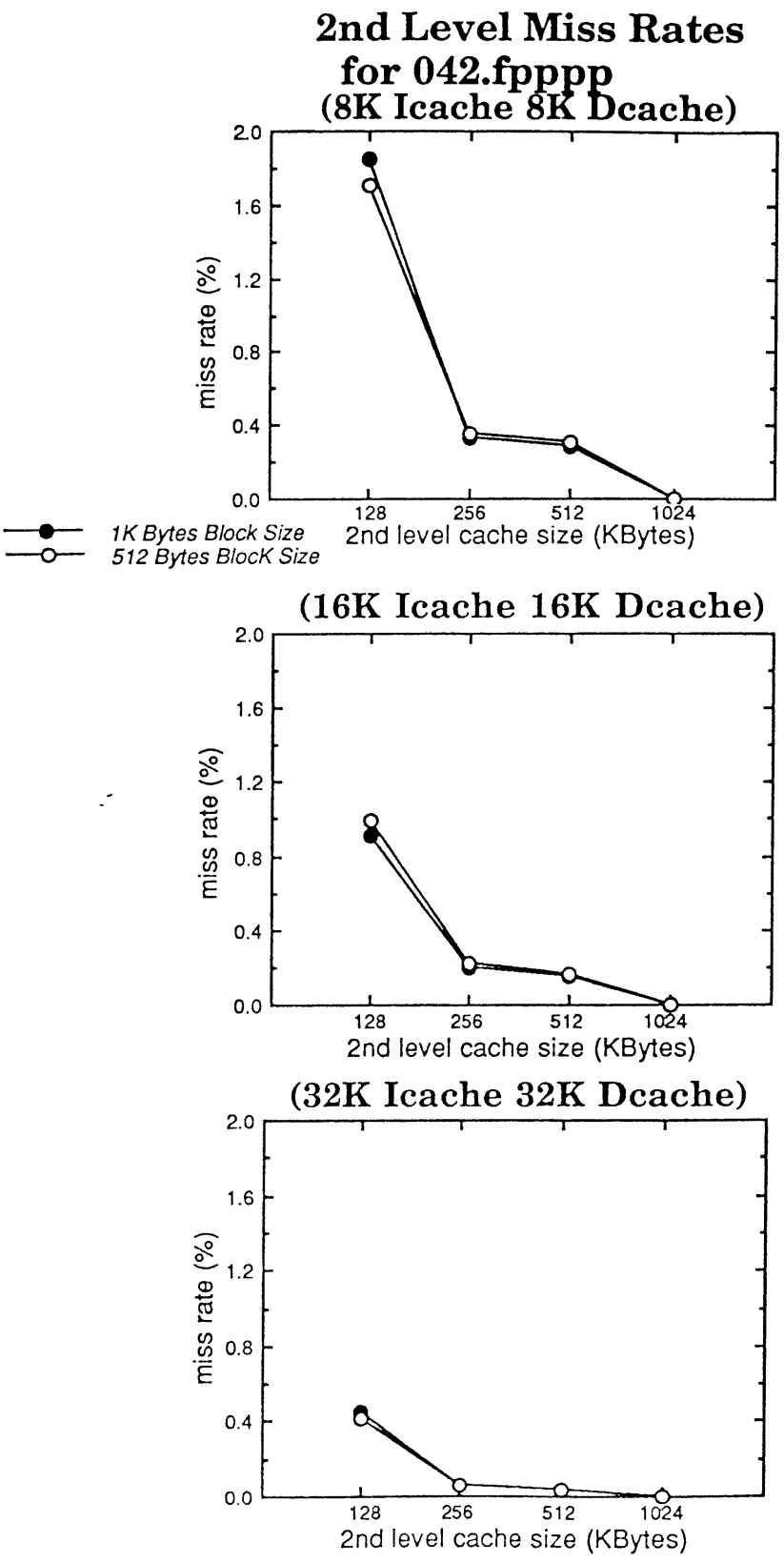


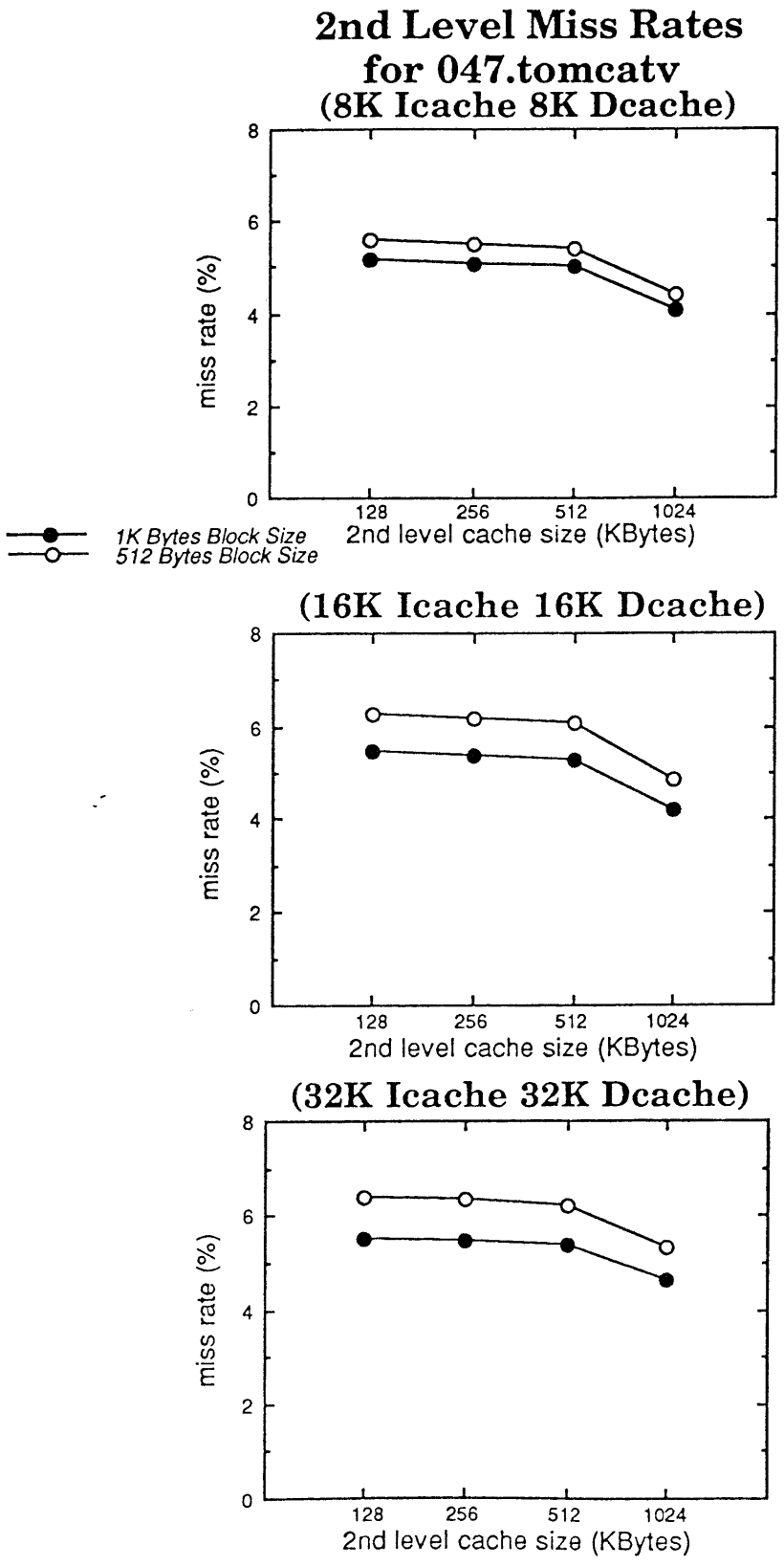
(16K Icache 16K Dcache)



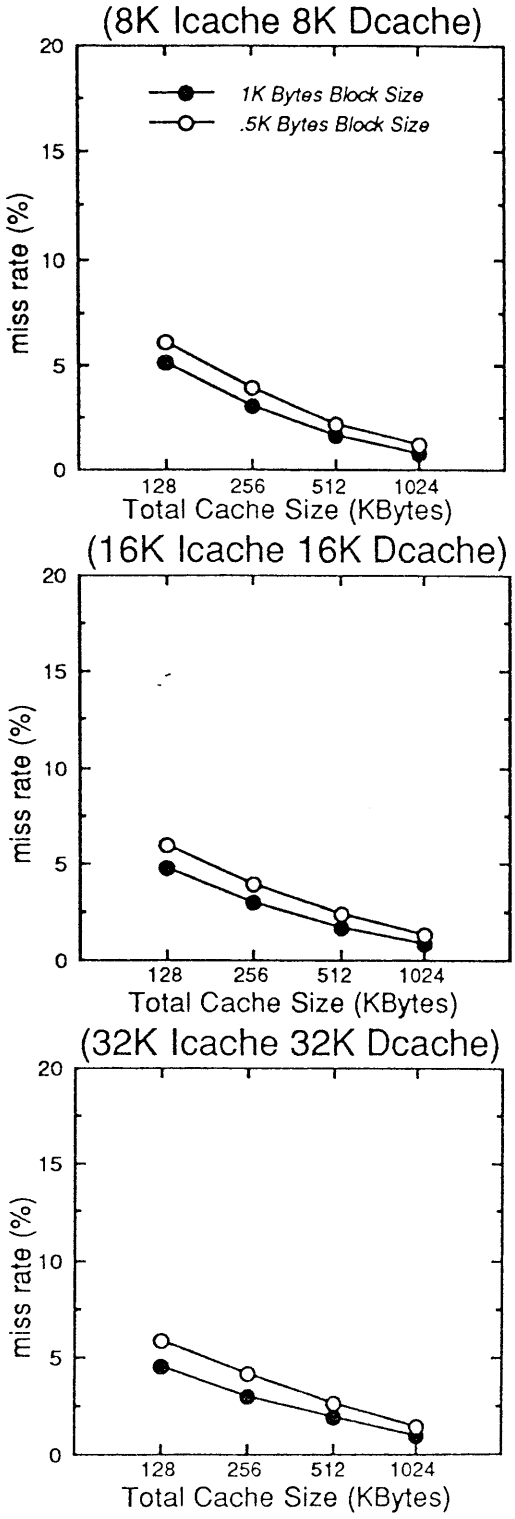
(32K Icache 32K Dcache)



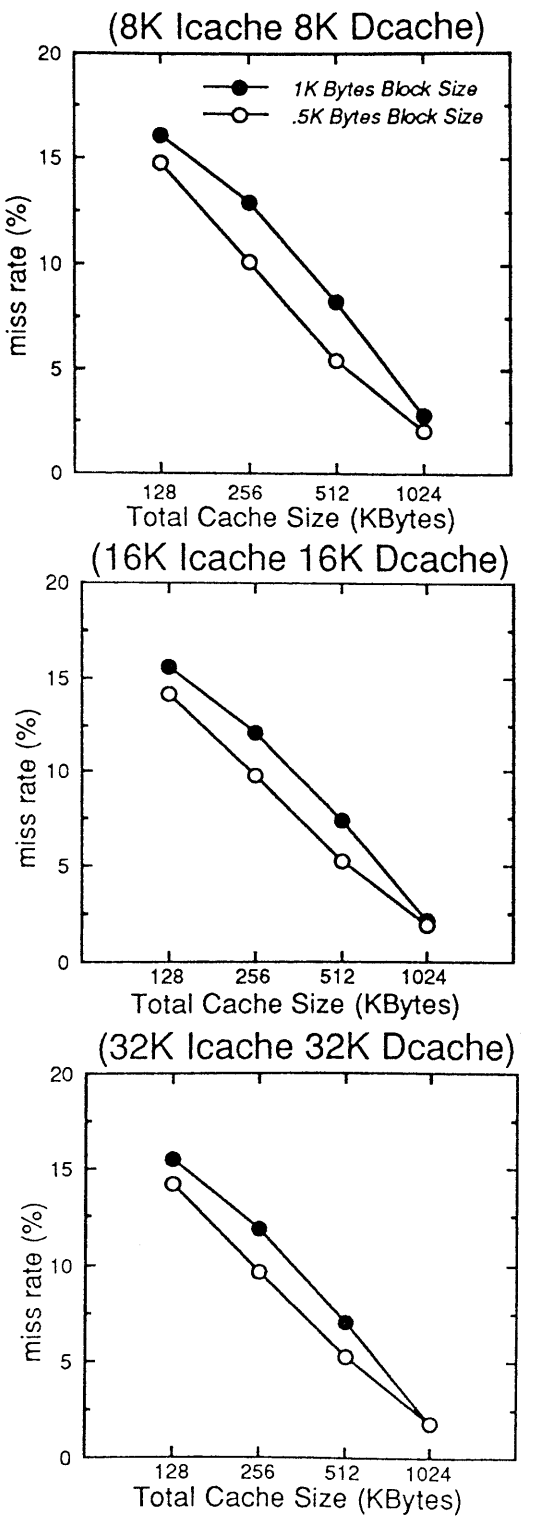

2nd Level Miss Rates
for 042.fpppp
(8K Icache 8K Dcache)
2.0
1.6
1.2
0.8
0.4
0.0
miss rate (%)
128
256
512
1024
2nd level cache size (KBytes)
1K Bytes Block Size
512 Bytes BlocK Size
(16K Icache 16K Dcache)
2.0
1.6
1.2
0.8
0.4
0.0
miss rate (%)
128
256
512
1024
2nd level cache size (KBytes)
(32K Icache 32K Dcache)
2.0
1.6
1.2
0.8
0.4
0.0
miss rate (%)
128
256
512
1024
2nd level cache size (KBytes)


2nd Level Miss Rates
for 047.tomcatv
(8K Icache 8K Dcache)
miss rate (%)
0
2
4
6
8
128
256
512
1024
2nd level cache size (KBytes)
1K Bytes Block Size
512 Bytes Block Size
(16K Icache 16K Dcache)
miss rate (%)
2nd level cache size (KBytes)
(32K Icache 32K Dcache)
miss rate (%)
2nd level cache size (KBytes)

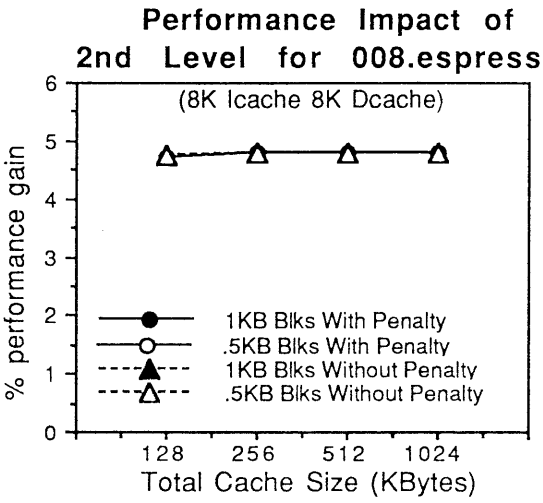
2nd Level Miss Rates for Integer Benchmarks

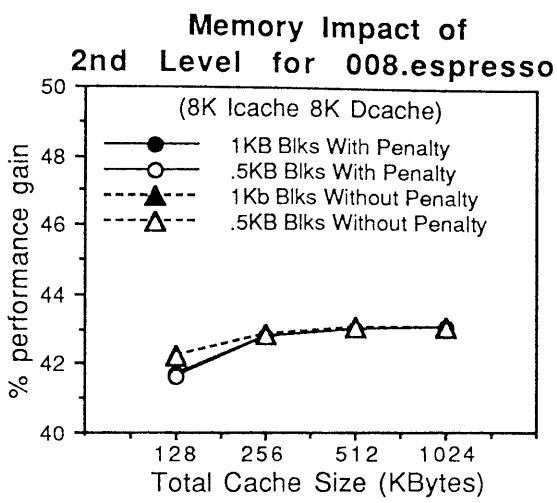


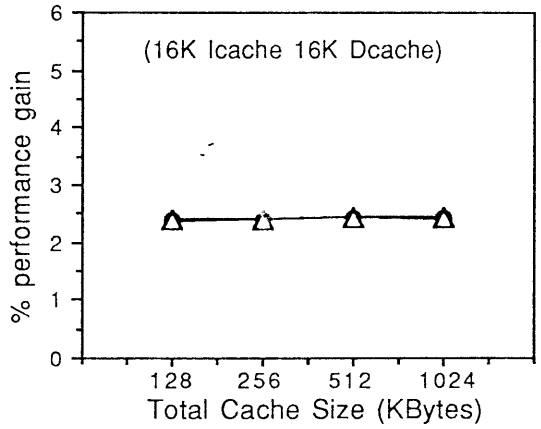
2nd Level Miss Rates for Floating Point Benchmarks

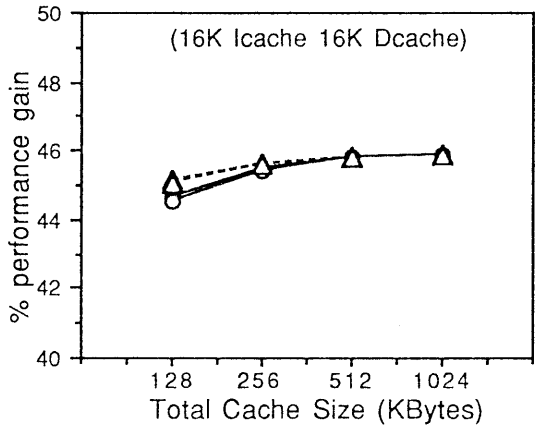


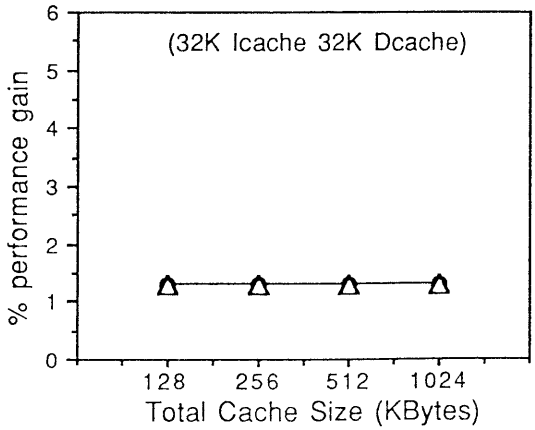
Appendix F
2nd Sweep Performance Impact

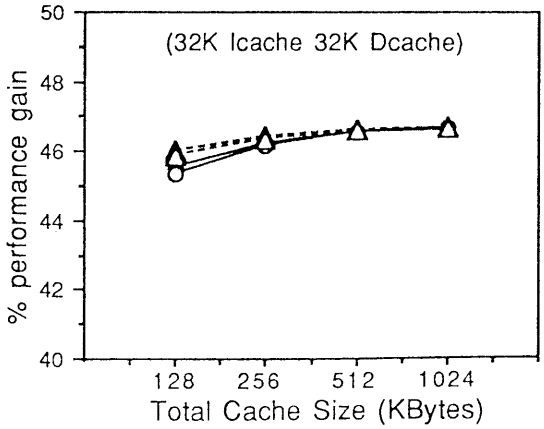

Performance Impact of
2nd Level for 008.espresso
(8K Icache 8K Dcache)
% performance gain
Total Cache Size (KBytes)
128
256
512
1024
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty

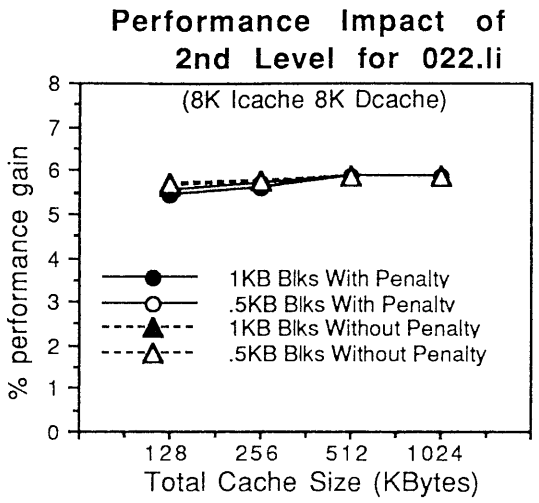

Memory Impact of
2nd Level for 008.espresso
(8K Icache 8K Dcache)
% performance gain
Total Cache Size (KBytes)
1KB Blks With Penalty
.5KB Blks With Penalty
1Kb Blks Without Penalty
.5KB Blks Without Penalty

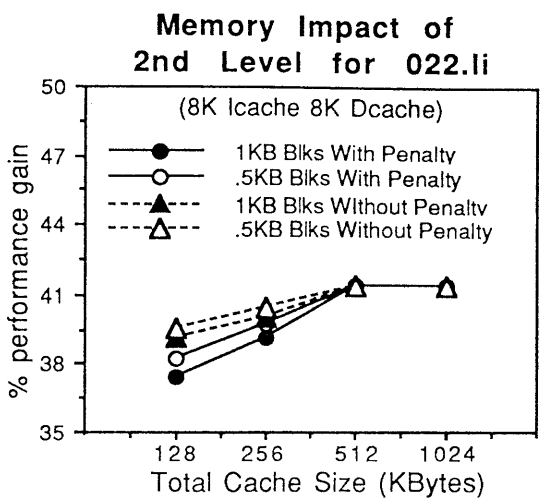

(16K Icache 16K Dcache)
% performance gain
Total Cache Size (KBytes)

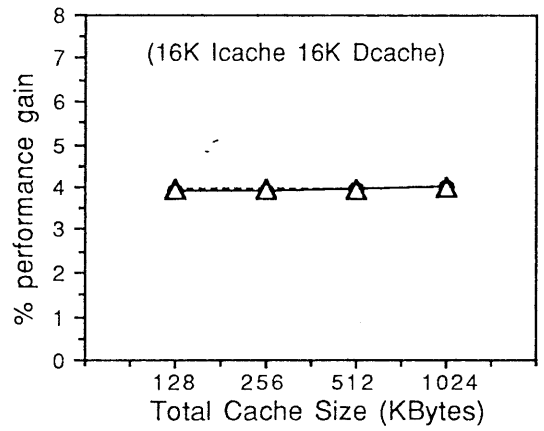

(16K Icache 16K Dcache)
% performance gain
Total Cache Size (KBytes)

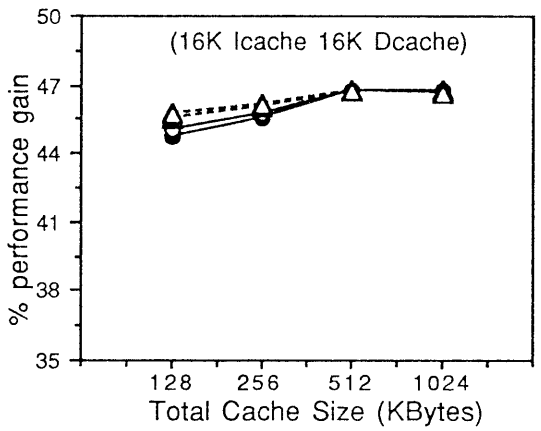

(32K Icache 32K Dcache)
% performance gain
Total Cache Size (KBytes)

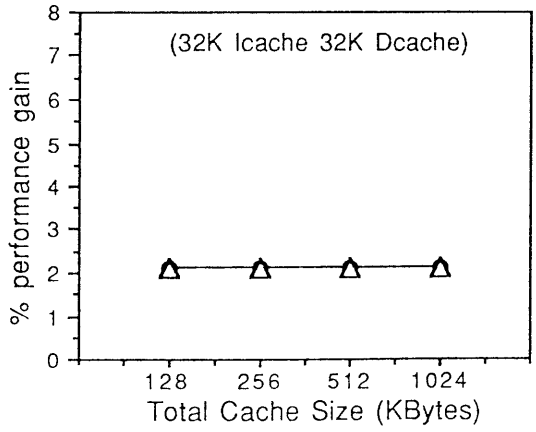

(32K Icache 32K Dcache)
% performance gain
Total Cache Size (KBytes)

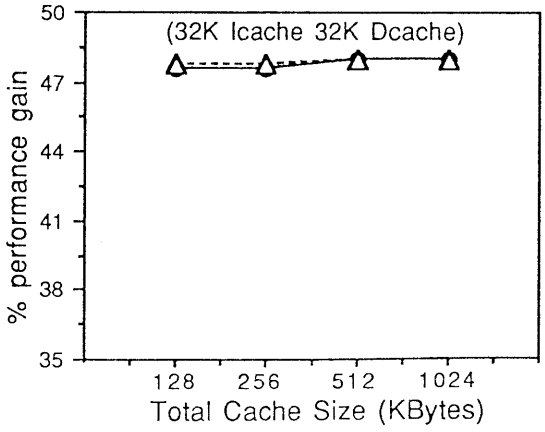

Performance Impact of
2nd Level for 022.li
(8K Icache 8K Dcache)
% performance gain
0
1
2
3
4
5
6
7
8
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

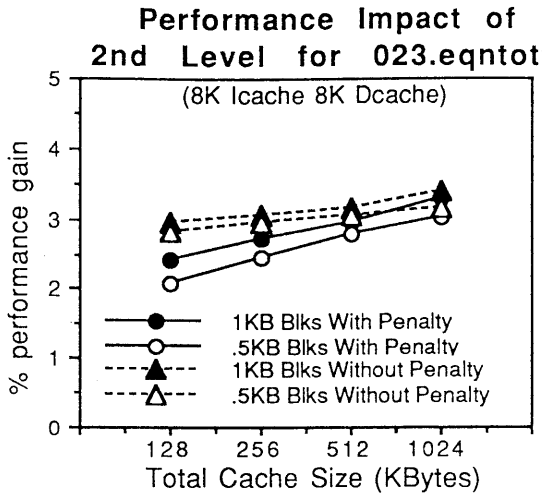

Memory Impact of
2nd Level for 022.li
(8K Icache 8K Dcache)
% performance gain
35
38
41
44
47
50
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

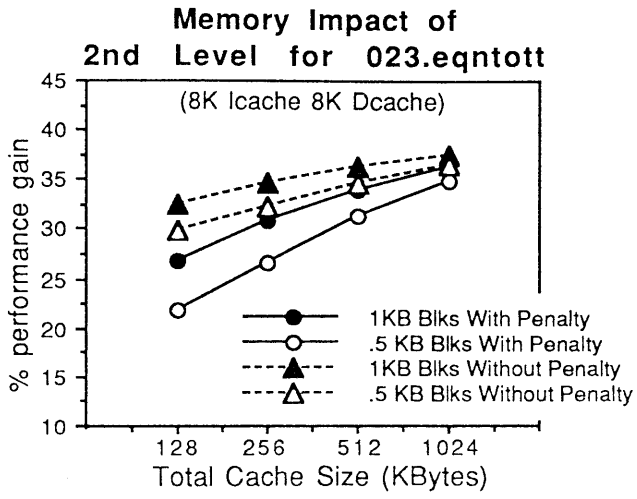

(16K Icache 16K Dcache)
% performance gain
0
1
2
3
4
5
6
7
8
128
256
512
1024
Total Cache Size (KBytes)

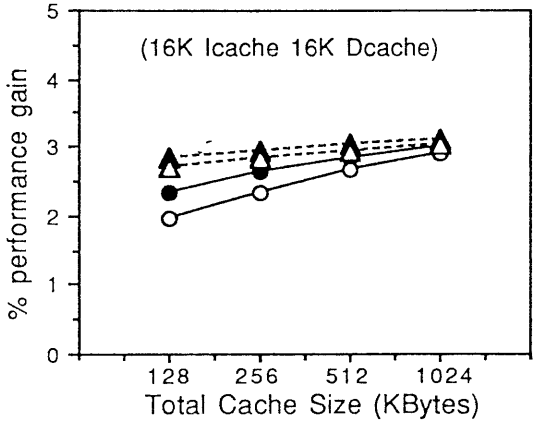

(16K Icache 16K Dcache)
% performance gain
35
38
41
44
47
50
128
256
512
1024
Total Cache Size (KBytes)

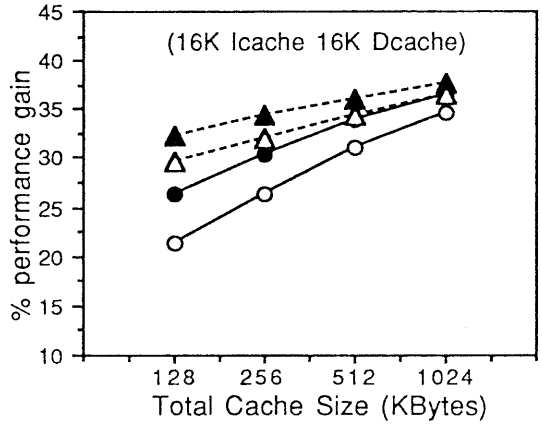

(32K Icache 32K Dcache)
% performance gain
0
1
2
3
4
5
6
7
8
128
256
512
1024
Total Cache Size (KBytes)

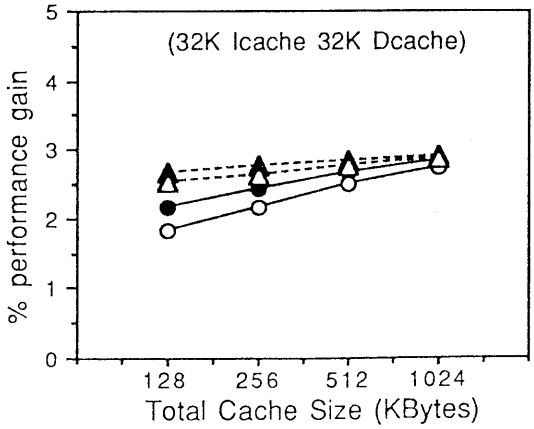

(32K Icache 32K Dcache)
% performance gain
35
38
41
44
47
50
128
256
512
1024
Total Cache Size (KBytes)

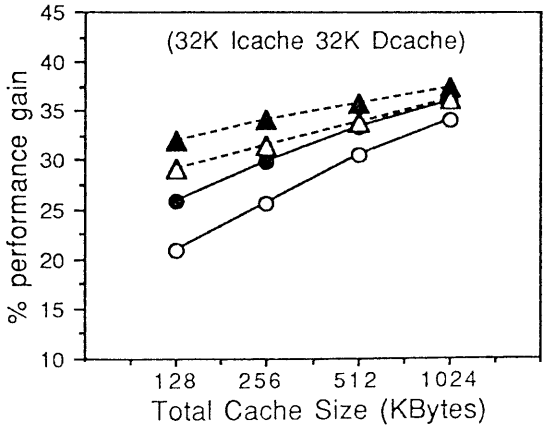

Performance Impact of
2nd Level for 023.eqntott
(8K Icache 8K Dcache)
% performance gain
Total Cache Size (KBytes)
128
256
512
1024
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty

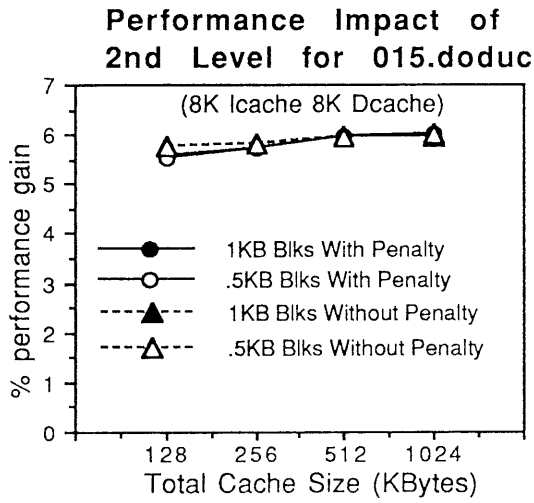

Memory Impact of
2nd Level for 023.eqntott
(8K Icache 8K Dcache)
% performance gain
Total Cache Size (KBytes)
1KB Blks With Penalty
.5 KB Blks With Penalty
1KB Blks Without Penalty
.5 KB Blks Without Penalty

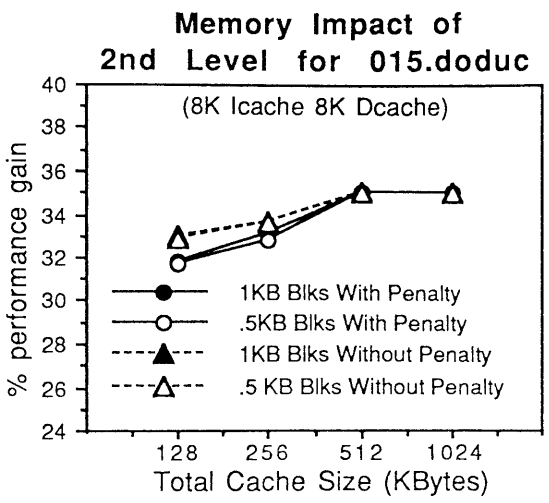

(16K Icache 16K Dcache)
% performance gain
Total Cache Size (KBytes)

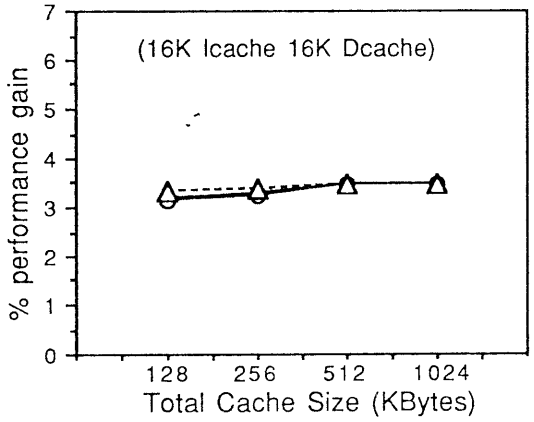

(16K Icache 16K Dcache)
% performance gain
Total Cache Size (KBytes)

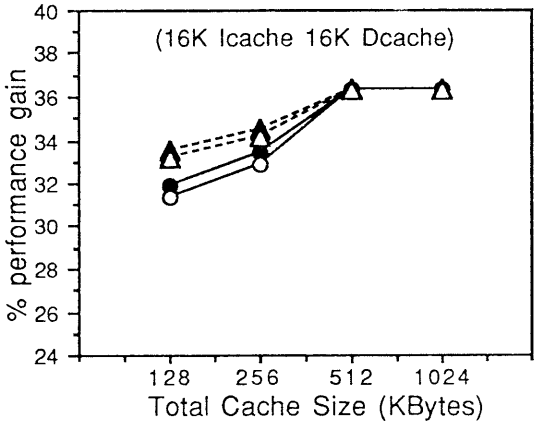

(32K Icache 32K Dcache)
% performance gain
Total Cache Size (KBytes)

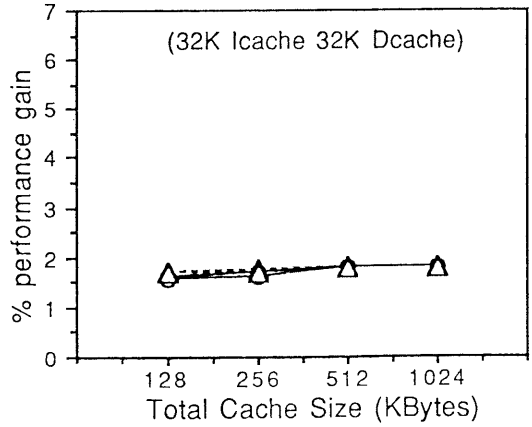

(32K Icache 32K Dcache)
% performance gain
Total Cache Size (KBytes)

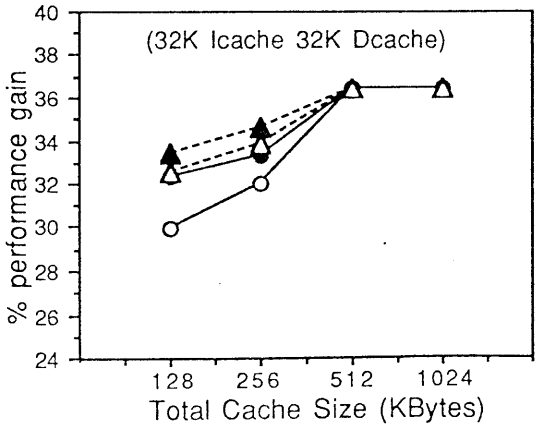

Performance Impact of
2nd Level for 015.doduc
(8K Icache 8K Dcache)
% performance gain
0
1
2
3
4
5
6
7
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

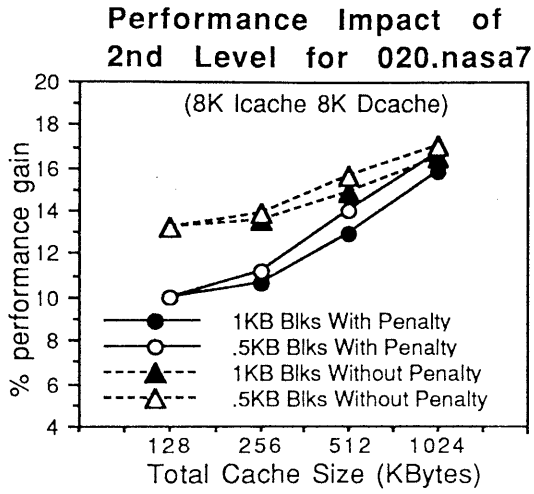

Memory Impact of
2nd Level for 015.doduc
(8K Icache 8K Dcache)
% performance gain
24
26
28
30
32
34
36
38
40
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5 KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

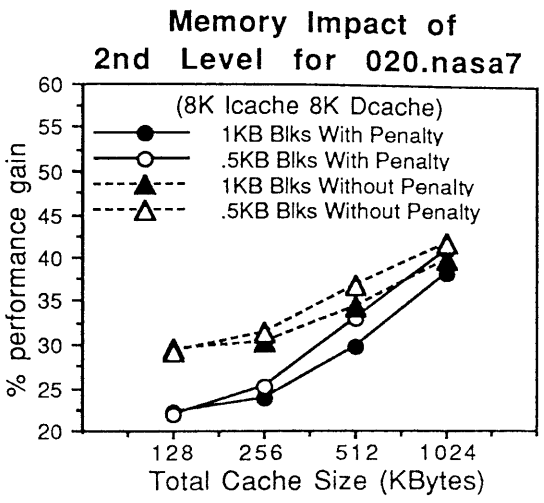

(16K Icache 16K Dcache)
% performance gain
0
1
2
3
4
5
6
7
128
256
512
1024
Total Cache Size (KBytes)

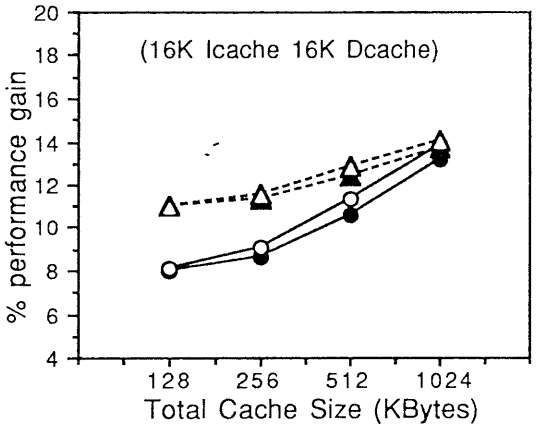

(16K Icache 16K Dcache)
% performance gain
24
26
28
30
32
34
36
38
40
128
256
512
1024
Total Cache Size (KBytes)

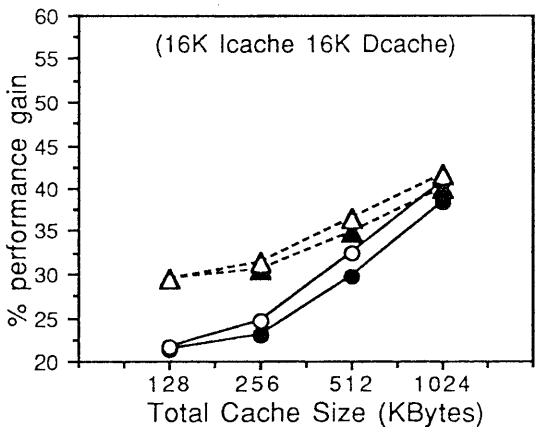

(32K Icache 32K Dcache)
% performance gain
0
1
2
3
4
5
6
7
128
256
512
1024
Total Cache Size (KBytes)

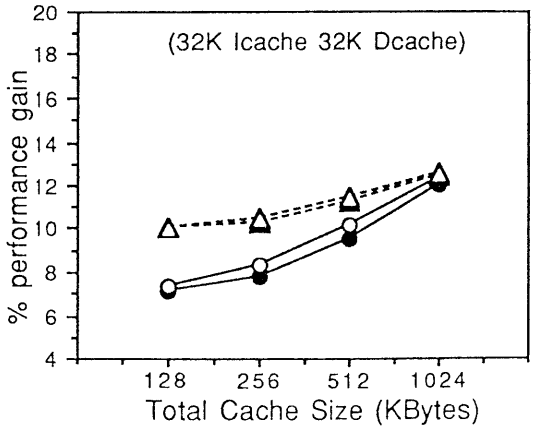

(32K Icache 32K Dcache)
% performance gain
24
26
28
30
32
34
36
38
40
128
256
512
1024
Total Cache Size (KBytes)

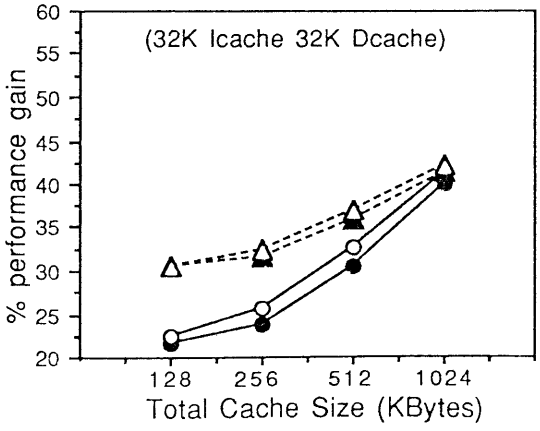

Performance Impact of
2nd Level for 020.nasa7
(8K Icache 8K Dcache)
% performance gain
20
18
16
14
12
10
8
6
4
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

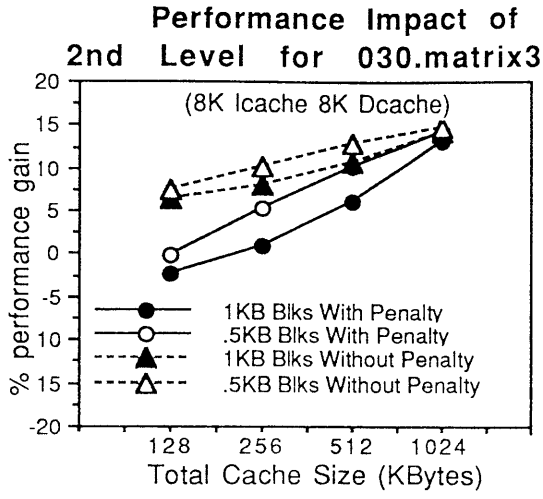

Memory Impact of
2nd Level for 020.nasa7
(8K Icache 8K Dcache)
% performance gain
60
55
50
45
40
35
30
25
20
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

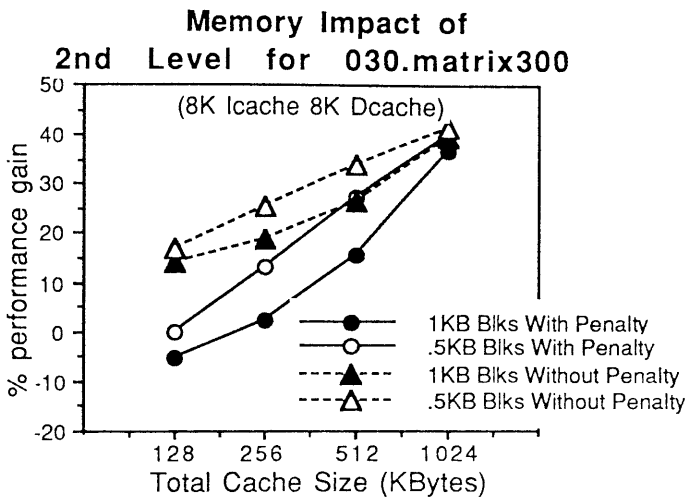

(16K Icache 16K Dcache)
% performance gain
20
18
16
14
12
10
8
6
4
128
256
512
1024
Total Cache Size (KBytes)

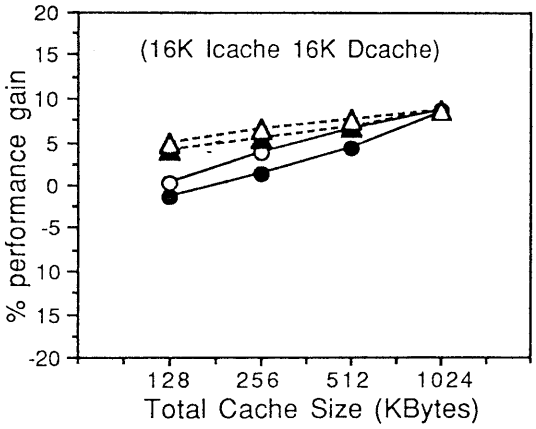

(16K Icache 16K Dcache)
% performance gain
60
55
50
45
40
35
30
25
20
128
256
512
1024
Total Cache Size (KBytes)

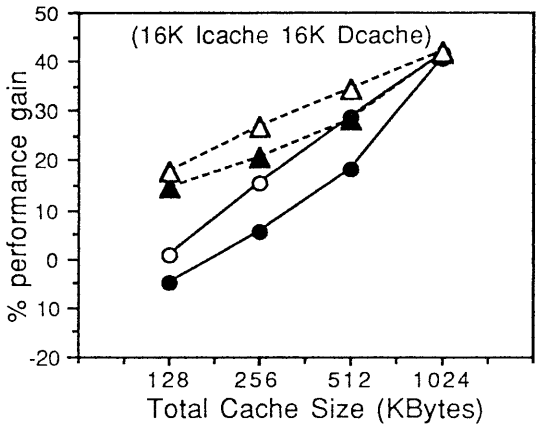

(32K Icache 32K Dcache)
% performance gain
20
18
16
14
12
10
8
6
4
128
256
512
1024
Total Cache Size (KBytes)

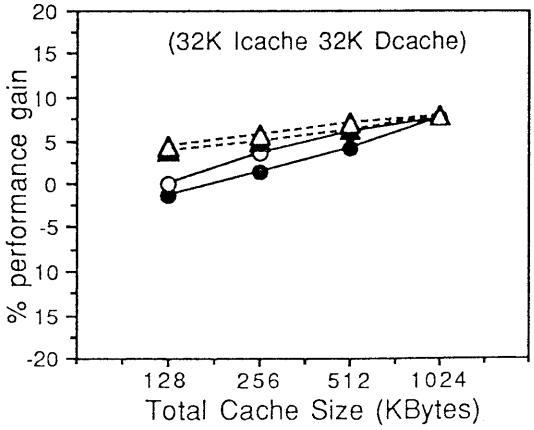

(32K Icache 32K Dcache)
% performance gain
60
55
50
45
40
35
30
25
20
128
256
512
1024
Total Cache Size (KBytes)

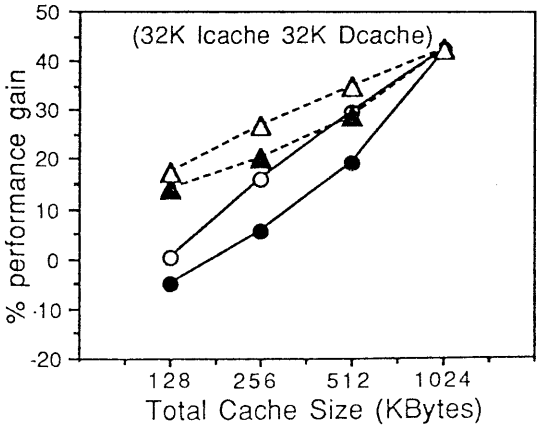

Performance Impact of
2nd Level for 030.matrix300
(8K Icache 8K Dcache)
% performance gain
Total Cache Size (KBytes)
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty

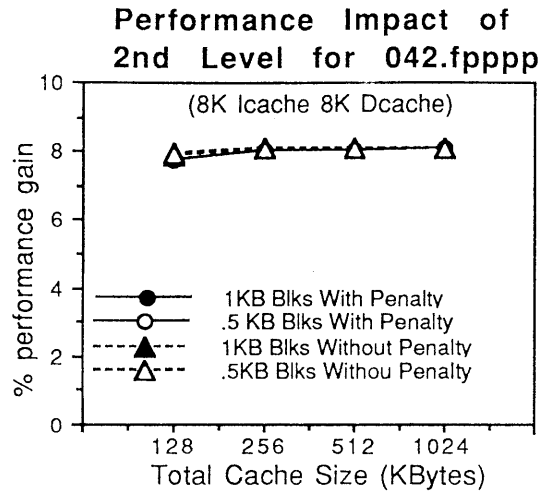

Memory Impact of
2nd Level for 030.matrix300
(8K Icache 8K Dcache)
% performance gain
Total Cache Size (KBytes)
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty

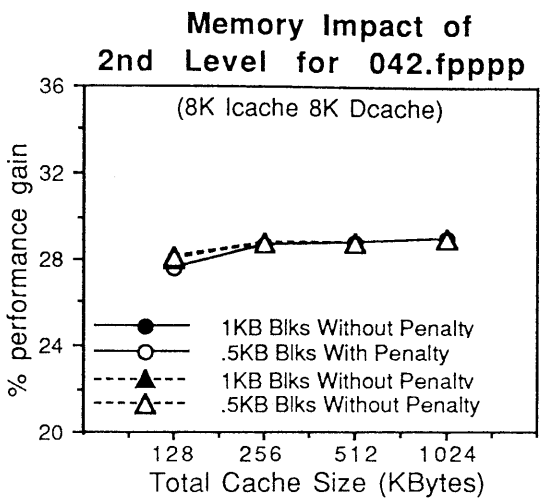

(16K Icache 16K Dcache)
% performance gain
Total Cache Size (KBytes)

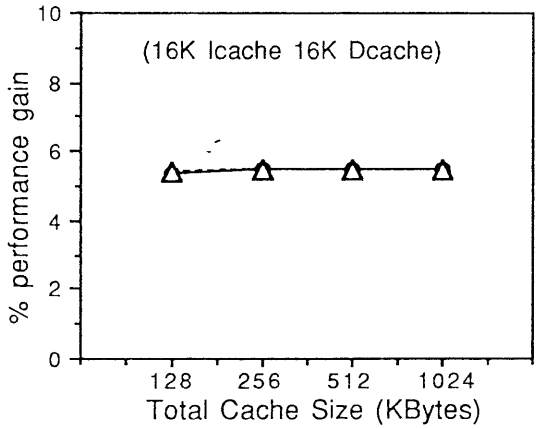

(16K Icache 16K Dcache)
% performance gain
Total Cache Size (KBytes)

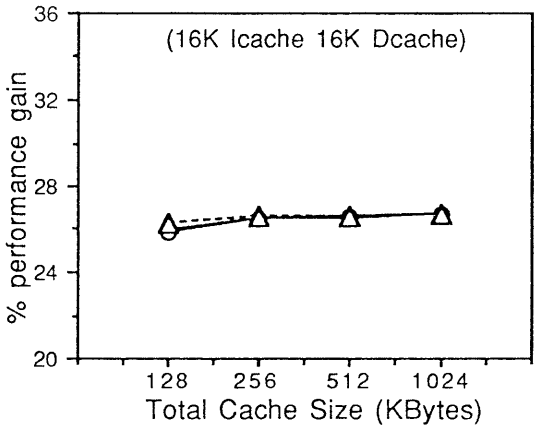

(32K Icache 32K Dcache)
% performance gain
Total Cache Size (KBytes)

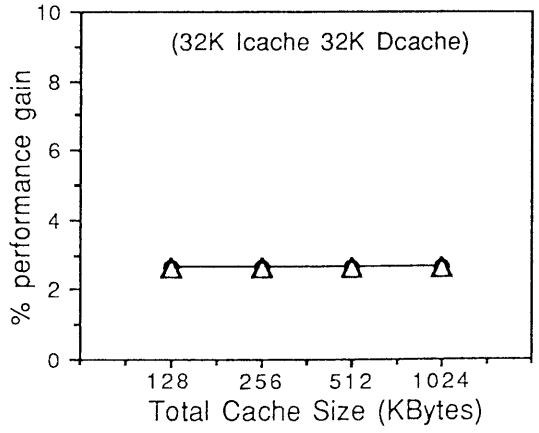

(32K Icache 32K Dcache)
% performance gain
Total Cache Size (KBytes)

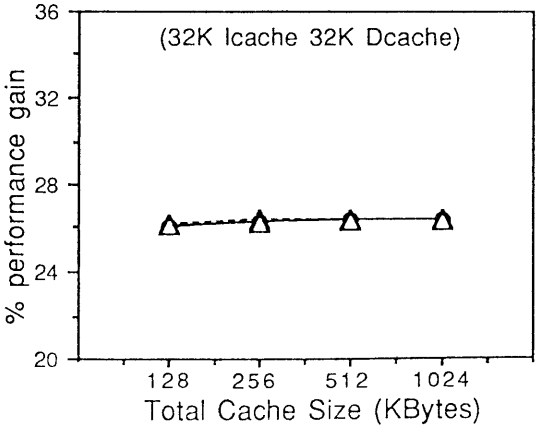

Performance Impact of
2nd Level for 042.fpppp
(8K Icache 8K Dcache)
% performance gain
10
8
6
4
2
0
1KB Blks With Penalty
.5 KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Withou Penalty
128
256
512
1024
Total Cache Size (KBytes)

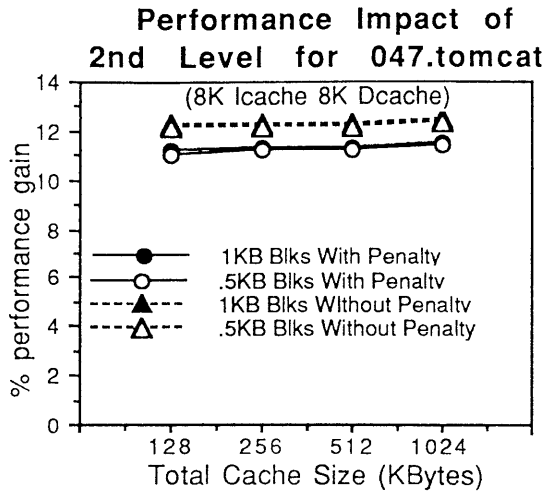

Memory Impact of
2nd Level for 042.fpppp
(8K Icache 8K Dcache)
% performance gain
36
32
28
24
20
1KB Blks Without Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

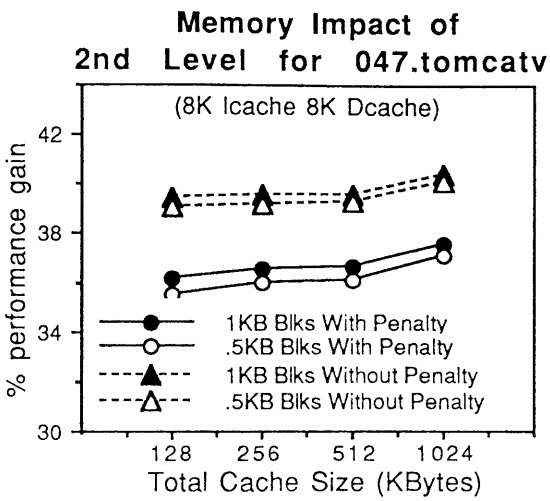

(16K Icache 16K Dcache)
% performance gain
10
8
6
4
2
0
128
256
512
1024
Total Cache Size (KBytes)

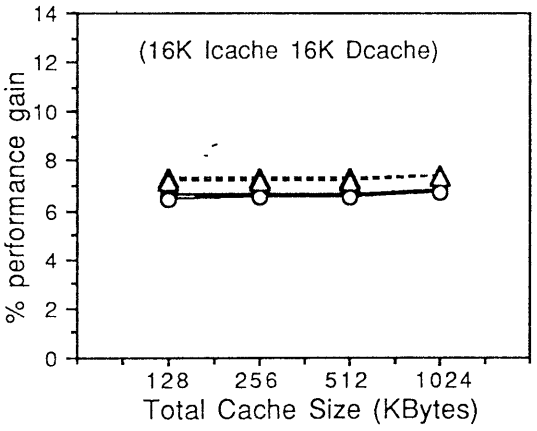

(16K Icache 16K Dcache)
% performance gain
36
32
28
24
20
128
256
512
1024
Total Cache Size (KBytes)

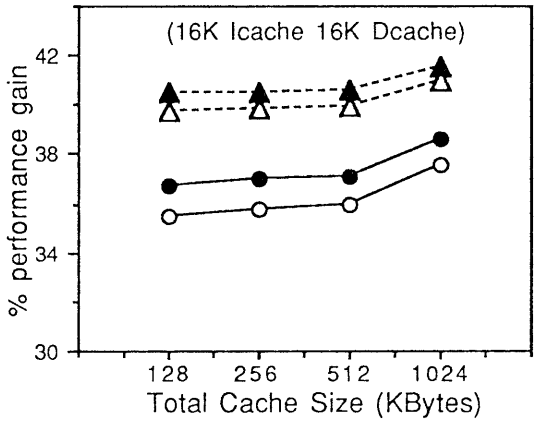

(32K Icache 32K Dcache)
% performance gain
10
8
6
4
2
0
128
256
512
1024
Total Cache Size (KBytes)

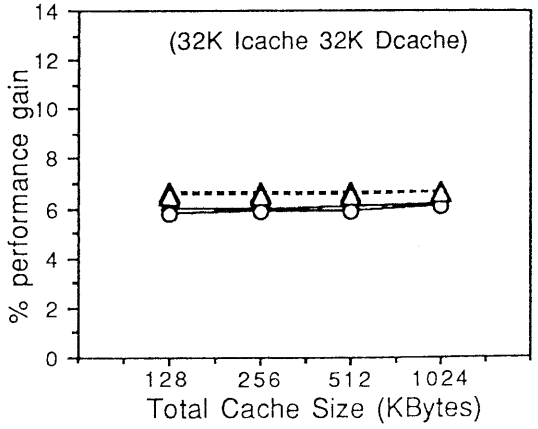

(32K Icache 32K Dcache)
% performance gain
36
32
28
24
20
128
256
512
1024
Total Cache Size (KBytes)

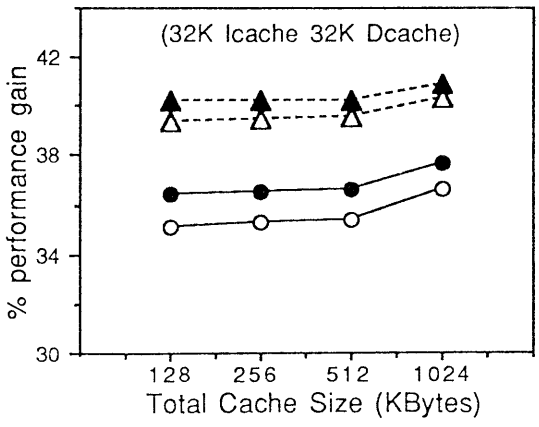

Performance Impact of
2nd Level for 047.tomcatv
(8K Icache 8K Dcache)
% performance gain
0
2
4
6
8
10
12
14
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks WIthout Penaltv
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)


Memory Impact of
2nd Level for 047.tomcatv
(8K Icache 8K Dcache)
% performance gain
30
34
38
42
1KB Blks With Penalty
.5KB Blks With Penalty
1KB Blks Without Penalty
.5KB Blks Without Penalty
128
256
512
1024
Total Cache Size (KBytes)

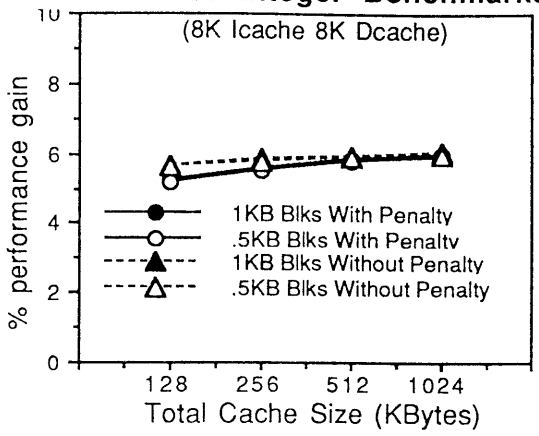

(16K Icache 16K Dcache)
% performance gain
0
2
4
6
8
10
12
14
128
256
512
1024
Total Cache Size (KBytes)

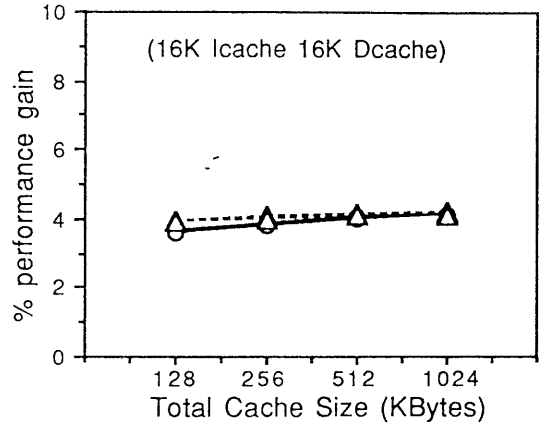

(16K Icache 16K Dcache)
% performance gain
30
34
38
42
128
256
512
1024
Total Cache Size (KBytes)

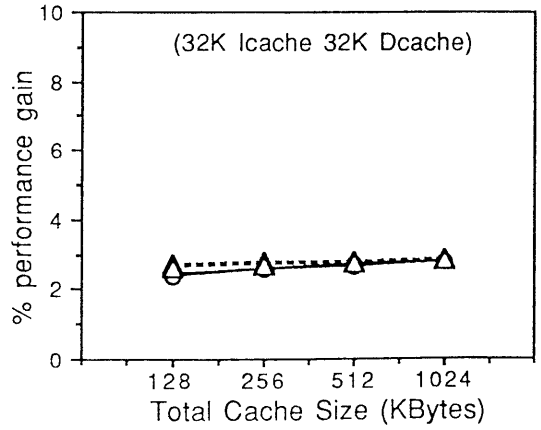

(32K Icache 32K Dcache)
% performance gain
0
2
4
6
8
10
12
14
128
256
512
1024
Total Cache Size (KBytes)


(32K Icache 32K Dcache)
% performance gain
30
34
38
42
128
256
512
1024
Total Cache Size (KBytes)

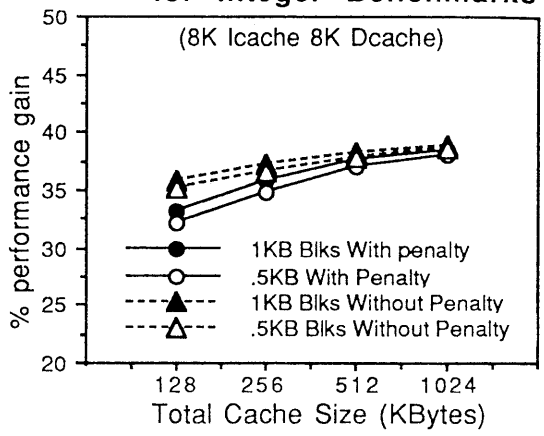
Performance Impact of 2nd Level for Integer Benchmarks

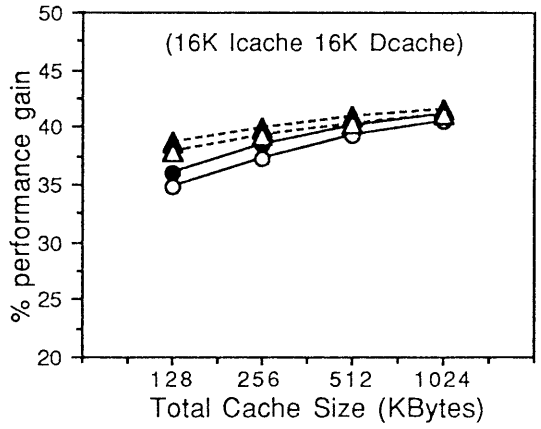


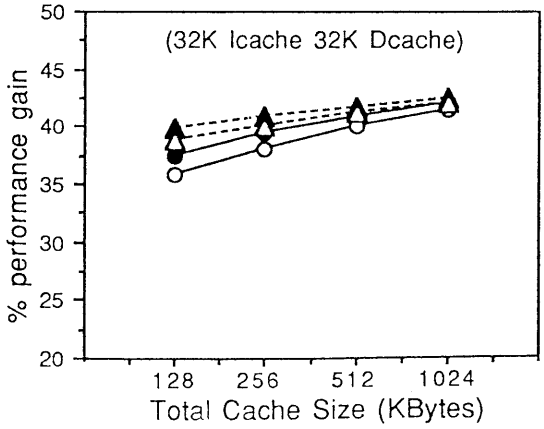




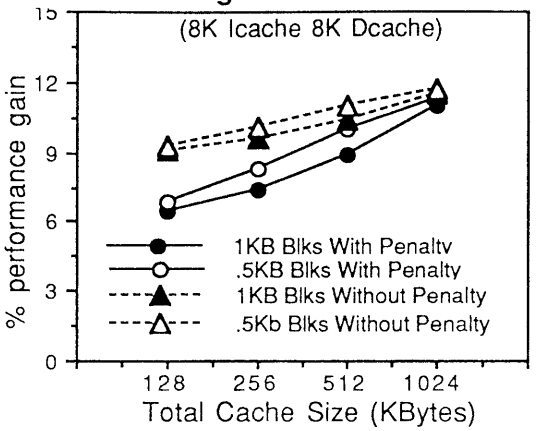
Memory Impact of 2nd Level for Integer Benchmarks

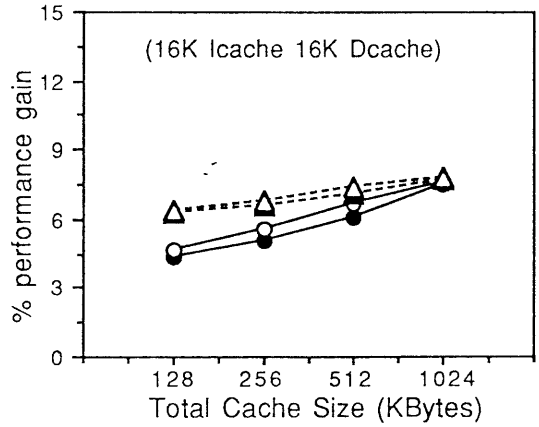


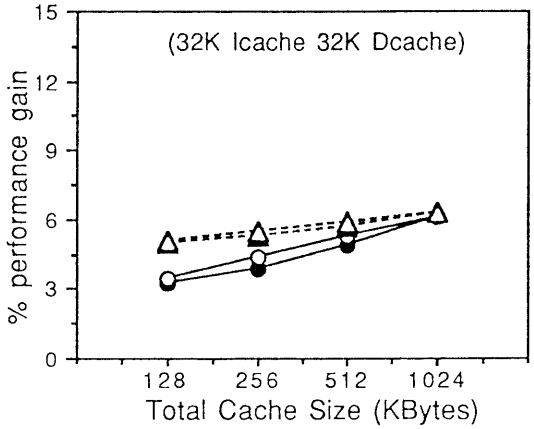




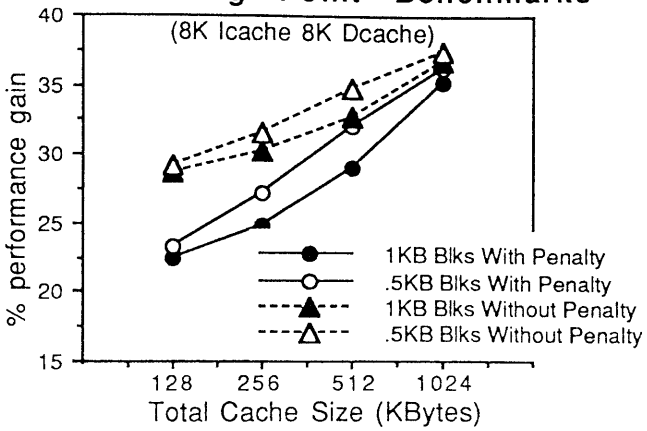
Performance Impact of 2nd Level for Floating Point Benchmarks

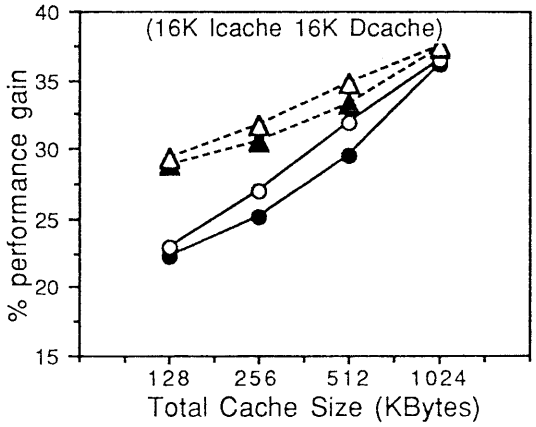


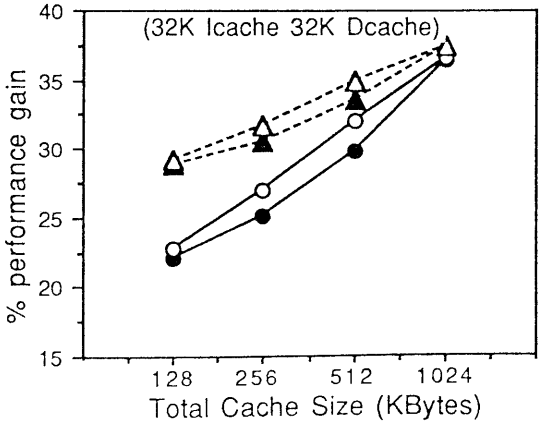




Memory Impact of 2nd Level for Floating Point Benchmarks







Appendix G
Sample Raw Data

```
Application: 001.gcc1.35

     1258984771 instructions (including annulled)
     1217214604 instructions (excluding annulled)
           46.0 SPECmarks for gcc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B             direct   write thru write allocate
1st Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
       61631828    5.0633%   3.893%                      I+D misses
       34597640    2.8424%   2.185%    2.748%            I   misses
       27034188    2.2210%   1.708%               8.340% D   misses

     1583154081  130.0637%  100.000%                     I+D references
     1258984771  103.4316%   79.524%  100.000%           I   references
      324169310   26.6321%   20.476%            100.000% D   references

      225256902   18.5059%   14.228%             69.487% D   reads
       16567802    1.3611%    1.047%              5.111% D   read misses
       98912408    8.1261%    6.248%             30.513% D   writes
       10466386    0.8599%    0.661%              3.229% D   write misses

       12815086    1.0528%    0.809%              3.953% D   write backs
        2348700    0.1930%    0.148%              0.725% D   read mod writes
2nd Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
       16775601    1.3782%   22.534%                      I+D misses
        9229931    0.7583%   12.398%   26.678%            I   misses
        7545670    0.6199%   10.136%             18.936% D   misses

       74446206    6.1161%  100.000%                     I+D references
       34597640    2.8424%   46.473%  100.000%           I   references
       39848566    3.2738%   53.527%            100.000% D   references

       16567802    1.3611%   22.255%              5.111% D   reads
        5951616    0.4890%    7.995%              1.836% D   read misses
       10466386    0.8599%   14.059%              3.229% D   writes
        1565347    0.1286%    2.103%              0.483% D   write misses

      104445009  i for i (icache busy)
        1598365  i for d (DRAM busy)
        1987790  i for store (DRAM busy)
        7580906  d for d (dcache busy)
       10361103  d for i (DRAM busy)
        4076706  d for store (DRAM busy)
              0  store for d (DRAM busy)
          13687  store for i (DRAM busy)
              0  store for store (DRAM busy)

        1419650  total ticks of fpu    0.066% of total ticks
         120384  fpOP instructions     0.010% of total
      964956935  total dram ticks      DRAM busy 44.979%
        1096908  float for float queue fpu CPI=  0.001
      767888963  memory ticks          mem CPI=  0.631
     1376242149  instruction ticks     raw CPI=  1.131
         143779  load penalties        load CPI= 0.000
     2145371799  total ticks           CPI=      1.763

      109294979  # of ticks saved  =  5.09 percent of total

        4637939  # of 2nd level dirty misses
```

```
Application: 008.espresso

     3102930952 instructions (including annulled)
     2930507476 instructions (excluding annulled)
           39.3 SPECmarks for espresso

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B             direct   write thru write allocate
1st Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
      59147806    2.0183%    1.506%                      I+D misses
       5417408    0.1849%    0.138%    0.175%            I   misses
      53730398    1.8335%    1.368%              6.507%  D   misses

    3928686273  134.0616%  100.000%                      I+D references
    3102930952  105.8837%   78.981%  100.000%           I   references
     825755321   28.1779%   21.019%            100.000%  D   references

     681401797   23.2520%   17.344%             82.519%  D   reads
      48718626    1.6625%    1.240%              5.900%  D   read misses
     144353524    4.9259%    3.674%             17.481%  D   writes
       5011772    0.1710%    0.128%              0.607%  D   write misses

      17844947    0.6089%    0.454%              2.161%  D   write backs
      12833175    0.4379%    0.327%              1.554%  D   read mod writes
2nd Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
       5079427    0.1733%    6.597%                      I+D misses
       1343165    0.0458%    1.745%   24.793%            I   misses
       3736262    0.1275%    4.853%              5.220%  D   misses

      76992418    2.6273%  100.000%                      I+D references
       5417408    0.1849%    7.036%  100.000%           I   references
      71575010    2.4424%   92.964%            100.000%  D   references

      48718626    1.6625%   63.277%              5.900%  D   reads
       3174193    0.1083%    4.123%              0.384%  D   read misses
       5011772    0.1710%    6.509%              0.607%  D   writes
        551803    0.0188%    0.717%              0.067%  D   write misses

      16302269  i for i (icache busy)
        210415  i for d (DRAM busy)
        179532  i for store (DRAM busy)
      42600294  d for d (dcache busy)
       1412638  d for i (DRAM busy)
       1226860  d for store (DRAM busy)
             0  store for d (DRAM busy)
          2078  store for i (DRAM busy)
             0  store for store (DRAM busy)

        108223  total ticks of fpu     0.003% of total ticks
          8755  fpOP instructions      0.000% of total
     759210607  total dram ticks       DRAM busy 19.776%
         52955  float for float queue  fpu CPI=  0.000
     573915215  memory ticks           mem CPI=  0.196
    3265169566  instruction ticks      raw CPI=  1.114
          2355  load penalties         load CPI= 0.000
    3839140091  total ticks            CPI=      1.310

     192602952  # of ticks saved  =  5.02 percent of total

       2190891  # of 2nd level dirty misses
```

Application: spice2g6

```
    23810783700 instructions (including annulled)
    22775128234 instructions (excluding annulled)
          31.8 SPECmarks for spice2g6

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
     1958630374    8.5999%    6.638%                      I+D misses
       79734588    0.3501%    0.271%    0.335%            I   misses
     1878895786    8.2498%    6.367%              32.968% D   misses

    29509960940  129.5710%  100.000%                      I+D references
    23810783700  104.5474%   80.688%  100.000%           I   references
     5699177240   25.0237%   19.313%            100.000% D   references

     4792611768   21.0432%   16.241%              84.094% D   reads
     1803511822    7.9188%    6.112%              31.646% D   read misses
      906565472    3.9806%    3.073%              15.907% D   writes
       75383964    0.3310%    0.256%               1.323% D   write misses

      171994488    0.7552%    0.583%               3.018% D   write backs
       96610524    0.4242%    0.328%               1.696% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      981327155    4.3088%   46.059%                      I+D misses
       15014603    0.0660%    0.705%   18.831%           I   misses
      966312552    4.2429%   45.354%              47.117% D   misses

     2130624749    9.3551%  100.000%                      I+D references
       79734588    0.3501%    3.743%  100.000%           I   references
     2050890161    9.0050%   96.258%            100.000% D   references

     1803511822    7.9188%   84.648%              87.939% D   reads
      954494720    4.1910%   44.799%              46.541% D   read misses
       75383964    0.3310%    3.539%               3.676% D   writes
       11727894    0.0515%    0.551%               0.572% D   write misses

      239039751  i for i (icache busy)
        5356032  i for d (DRAM busy)
        6250388  i for store (DRAM busy)
      276030980  d for d (dcache busy)
       52847103  d for i (DRAM busy)
       69788733  d for store (DRAM busy)
              0  store for d (DRAM busy)
           5657  store for i (DRAM busy)
              0  store for store (DRAM busy)

     7841192173  total ticks of fpu    15.574% of total ticks
      962369533  fpOP instructions     4.226% of total
    27278425460  total dram ticks      DRAM busy 54.178%
     3671733514  float for float queue fpu CPI=  0.162
    21296666093  memory ticks          mem CPI=  0.936
    24784595920  instruction ticks     raw CPI=  1.089
      597255631  load penalties        load CPI= 0.027
    50350251158  total ticks           CPI=      2.211

     -736557578  # of ticks saved  = -1.47 percent of total
```

```
Application: doduc

     1316441137 instructions (including annulled)
     1304567925 instructions (excluding annulled)
           29.8 SPECmarks for doduc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       79526491    6.0961%    4.677%                      I+D misses
       32267170    2.4734%    1.898%    2.452%            I   misses
       47259321    3.6227%    2.780%              12.305% D   misses

     1700517998  130.3511%  100.000%                      I+D references
     1316441137  100.9102%   77.415%  100.000%           I   references
      384076861   29.4410%   22.586%             100.000% D   references

      298852886   22.9082%   17.575%              77.811% D   reads
       29072774    2.2286%    1.710%               7.570% D   read misses
       85223975    6.5328%    5.012%              22.190% D   writes
       18186547    1.3941%    1.070%               4.736% D   write misses

       19846441    1.5214%    1.168%               5.168% D   write backs
        1659894    0.1273%    0.098%               0.433% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       21148249    1.6211%   21.282%                      I+D misses
        5399990    0.4140%    5.435%   16.736%            I   misses
       15748259    1.2072%   15.848%              23.468% D   misses

       99372844    7.6173%  100.000%                      I+D references
       32267170    2.4734%   32.471%  100.000%           I   references
       67105674    5.1440%   67.530%             100.000% D   references

       29072774    2.2286%   29.257%              43.324% D   reads
        9870202    0.7566%    9.933%              14.709% D   read misses
       18186547    1.3941%   18.302%              27.102% D   writes
        5796598    0.4444%    5.834%               8.639% D   write misses

       76127944  i for i (icache busy)
        3804530  i for d (DRAM busy)
        5610157  i for store (DRAM busy)
       30762008  d for d (dcache busy)
       28424993  d for i (DRAM busy)
        8792833  d for store (DRAM busy)
              0  store for d (DRAM busy)
          52814  store for i (DRAM busy)
              0  store for store (DRAM busy)

     2752142075  total ticks of fpu     66.010% of total ticks
      338148549  fpOP instructions      26.159% of total
     1209094627  total dram ticks       DRAM busy 29.001%
     1712397711  float for float queue  fpu CPI=  1.313
      967749864  memory ticks           mem CPI=  0.742
     1408495477  instruction ticks      raw CPI=  1.080
       80643507  load penalties         load CPI= 0.062
     4169286559  total ticks            CPI=      3.196

      159611912  # of ticks saved  =  3.83 percent of total
```

```
Application: dnasa7

     6800274187 instructions (including annulled)
     6784406507 instructions (excluding annulled)
           44.4 SPECmarks for nasa7

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
     1237399865   18.2389%   13.140%                      I+D misses
        5979542    0.0882%    0.064%    0.088%            I   misses
     1231420323   18.1508%   13.076%              47.052% D   misses

     9417438191  138.8101%  100.000%                      I+D references
     6800274187  100.2339%   72.210%  100.000%            I   references
     2617164004   38.5762%   27.791%             100.000% D   references

     1879496668   27.7032%   19.958%              71.815% D   reads
     1145483039   16.8841%   12.164%              43.769% D   read misses
      737667336   10.8730%    7.833%              28.186% D   writes
       85937284    1.2667%    0.913%               3.284% D   write misses

      502549919    7.4075%    5.337%              19.203% D   write backs
      416612635    6.1408%    4.424%              15.919% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      477625540    7.0401%   27.451%                      I+D misses
        1026763    0.0152%    0.060%   17.172%            I   misses
      476598777    7.0250%   27.392%              27.486% D   misses

     1739949718   25.6464%  100.000%                      I+D references
        5979542    0.0882%    0.344%  100.000%            I   references
     1733970176   25.5582%   99.657%             100.000% D   references

     1145483039   16.8841%   65.835%              66.062% D   reads
      444026754    6.5449%   25.520%              25.608% D   read misses
       85937284    1.2667%    4.940%               4.957% D   writes
       16957069    0.2500%    0.975%               0.978% D   write misses

       18770062  i for i (icache busy)
          98973  i for d (DRAM busy)
          97368  i for store (DRAM busy)
      875701431  d for d (dcache busy)
         797585  d for i (DRAM busy)
      519574010  d for store (DRAM busy)
              0  store for d (DRAM busy)
          16372  store for i (DRAM busy)
              0  store for store (DRAM busy)

    15079121076  total ticks of fpu     49.978% of total ticks
     2075466939  fpOP instructions      30.592% of total
    19068876884  total dram ticks       DRAM busy 63.202%
     6690330973  float for float queue  fpu CPI=  0.987
    15246144905  memory ticks           mem CPI=  2.248
     7549415866  instruction ticks      raw CPI=  1.113
      685812709  load penalties         load CPI= 0.102
    30171704453  total ticks            CPI=      4.448

     1963375393  # of ticks saved  =  6.51 percent of total
```

```
Application: xlisp li-input.lsp

     4962043458 instructions (including annulled)
     4661592279 instructions (excluding annulled)
           60.4 SPECmarks for li

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      104944241    2.2513%    1.612%                      I+D misses
       22411850    0.4808%    0.345%    0.452%            I   misses
       82532391    1.7705%    1.268%              5.322%  D   misses

     6512926989  139.7147%  100.000%                      I+D references
     4962043458  106.4453%   76.188%  100.000%           I   references
     1550883531   33.2694%   23.813%            100.000%  D   references

     1068396583   22.9192%   16.405%             68.890%  D   reads
       54583526    1.1710%    0.839%              3.520%  D   read misses
      482486948   10.3503%    7.409%             31.111%  D   writes
       27948865    0.5996%    0.430%              1.803%  D   write misses

       54109450    1.1608%    0.831%              3.489%  D   write backs
       26160585    0.5612%    0.402%              1.687%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       21918273    0.4702%   13.781%                      I+D misses
        7903684    0.1696%    4.970%   35.266%            I   misses
       14014589    0.3007%    8.812%             10.257%  D   misses

      159053576    3.4121%  100.000%                      I+D references
       22411850    0.4808%   14.091%  100.000%           I   references
      136641726    2.9313%   85.910%            100.000%  D   references

       54583526    1.1710%   34.318%             39.947%  D   reads
        9720978    0.2086%    6.112%              7.115%  D   read misses
       27948865    0.5996%   17.572%             20.455%  D   writes
        4215102    0.0905%    2.651%              3.085%  D   write misses

       76425863  i for i (icache busy)
         449428  i for d (DRAM busy)
        1946165  i for store (DRAM busy)
       36818503  d for d (dcache busy)
        6510120  d for i (DRAM busy)
        3667293  d for store (DRAM busy)
              0  store for d (DRAM busy)
           5937  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu    0.000% of total ticks
              0  fpOP instructions     0.000% of total
     1713310838  total dram ticks      DRAM busy 24.991%
              0  float for float queue fpu CPI=  0.000
     1294737869  memory ticks          mem CPI=  0.278
     5561136309  instruction ticks     raw CPI=  1.193
              0  load penalties        load CPI= 0.000
     6855874178  total ticks           CPI=      1.471

      310412461  # of ticks saved  =  4.53 percent of total

       11990588  # of 2nd level dirty misses
```

```
Application: eqntott -s -.ioplte int_pri_3.eqn

     1376907962 instructions (including annulled)
     1326073659 instructions (excluding annulled)
           46.8 SPECmarks for eqntott

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       17032852    1.2845%    1.066%                      I+D misses
           7623    0.0006%    0.001%    0.001%            I   misses
       17025229    1.2839%    1.066%              7.689%  D   misses

     1598339434  120.5318%  100.000%                      I+D references
     1376907962  103.8335%   86.147%  100.000%           I   references
      221431472   16.6983%   13.854%            100.000%  D   references

      202396631   15.2629%   12.663%             91.404%  D   reads
       16756051    1.2636%    1.049%              7.568%  D   read misses
       19034841    1.4355%    1.191%              8.597%  D   writes
         269178    0.0203%    0.017%              0.122%  D   write misses

         376005    0.0284%    0.024%              0.170%  D   write backs
         106827    0.0081%    0.007%              0.049%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs

        3983894    0.3005%   22.885%                      I+D misses
           1633    0.0002%    0.010%   21.423%            I   misses
        3982261    0.3004%   22.876%             22.886%  D   misses

       17408782    1.3129%  100.000%                      I+D references
           7623    0.0006%    0.044%  100.000%           I   references
       17401159    1.3123%   99.957%            100.000%  D   references

       16756051    1.2636%   96.251%             96.293%  D   reads
        3956063    0.2984%   22.725%             22.735%  D   read misses
         269178    0.0203%    1.547%              1.547%  D   writes
          25533    0.0020%    0.147%              0.147%  D   write misses

          21310  i for i (icache busy)
            104  i for d (DRAM busy)
            240  i for store (DRAM busy)
       26089775  d for d (dcache busy)
           1111  d for i (DRAM busy)
          35206  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu    0.000% of total ticks
              0  fpOP instructions     0.000% of total
      188367021  total dram ticks      DRAM busy 12.004%
              0  float for float queue fpu CPI=  0.000
      162265552  memory ticks          mem CPI=  0.123
     1403832293  instruction ticks     raw CPI=  1.059
        3149652  load penalties        load CPI= 0.003
     1569247497  total ticks           CPI=      1.184

       23227366  # of ticks saved  =  1.49 percent of total

         108409  # of 2nd level dirty misses
```

```
Application: matrix300

     1695008913 instructions (including annulled)
     1693559295 instructions (excluding annulled)
           42.0 SPECmarks for matrix300

level        size    block   subblk    assoc   write miss
1st I        8 KB     32 B              2-way   write back write allocate
1st D        4 KB     16 B              2-way   write back write allocate
2nd I+D     16 KB    512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      295277276   17.4354%   12.577%                      I+D misses
           1162    0.0001%    0.001%    0.001%            I   misses
      295276114   17.4353%   12.577%              45.235%  D   misses

     2347769860  138.6294%  100.000%                      I+D references
     1695008913  100.0856%   72.197%  100.000%            I   references
      652760947   38.5438%   27.804%             100.000%  D   references

      435650797   25.7240%   18.556%              66.740%  D   reads
      294562295   17.3931%   12.547%              45.126%  D   read misses
      217110150   12.8198%    9.248%              33.261%  D   writes
         713819    0.0422%    0.031%               0.110%  D   write misses

      129972785    7.6746%    5.537%              19.912%  D   write backs
      129258966    7.6324%    5.506%              19.802%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      218055680   12.8756%   51.278%                      I+D misses
            261    0.0001%    0.001%   22.462%            I   misses
      218055419   12.8756%   51.277%              51.278%  D   misses

      425249958   25.1099%  100.000%                      I+D references
           1162    0.0001%    0.001%  100.000%            I   references
      425248796   25.1098%  100.000%             100.000%  D   references

      294562295   17.3931%   69.269%              69.269%  D   reads
      217520276   12.8440%   51.152%              51.152%  D   read misses
         713819    0.0422%    0.168%               0.168%  D   writes
         411264    0.0243%    0.097%               0.097%  D   write misses

           3282  i for i (icache busy)
             77  i for d (DRAM busy)
            234  i for store (DRAM busy)
      188773310  d for d (dcache busy)
            583  d for i (DRAM busy)
      126625890  d for store (DRAM busy)
              0  store for d (DRAM busy)
              8  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3024001625  total ticks of fpu     42.029% of total ticks
      432000323  fpOP instructions      25.509% of total
     5336784370  total dram ticks       DRAM busy 74.172%
      690591267  float for float queue  fpu CPI=  0.408
     4376434394  memory ticks           mem CPI=  2.585
     1912122435  instruction ticks      raw CPI=  1.130
      216000307  load penalties         load CPI= 0.128
     7195148403  total ticks            CPI=      4.249

     -207427041  # of ticks saved  = -2.89 percent of total
```

```
Application: fpppp

     1448153391 instructions (including annulled)
     1443743830 instructions (excluding annulled)
           32.1 SPECmarks for fpppp

level        size     block    subblk     assoc    write miss
1st I        8 KB     32 B               2-way    write back write allocate
1st D        4 KB     16 B               2-way    write back write allocate
2nd I+D     16 KB    512 B              direct    write thru write allocate
1st Level:
               #     %instrs  %I+Drefs     %Irefs     %Drefs
       178506365   12.3642%    8.239%                          I+D misses
       115073763    7.9706%    5.311%     7.947%               I   misses
        63432602    4.3937%    2.928%                 8.828%   D   misses

      2166746002  150.0783%  100.000%                          I+D references
      1448153391  100.3055%   66.836%  100.000%               I   references
       718592611   49.7729%   33.165%             100.000%     D   references

       588879193   40.7884%   27.179%                81.949%   D   reads
        37985931    2.6311%    1.754%                 5.287%   D   read misses
       129713418    8.9846%    5.987%                18.052%   D   writes
        25446671    1.7626%    1.175%                 3.542%   D   write misses

        31101650    2.1543%    1.436%                 4.329%   D   write backs
         5654979    0.3917%    0.261%                 0.787%   D   read mod writes
2nd Level:
               #     %instrs  %I+Drefs     %Irefs     %Drefs
        25646460    1.7764%   12.236%                          I+D misses
        10080063    0.6982%    4.810%     8.760%               I   misses
        15566397    1.0782%    7.427%                16.467%   D   misses

       209607923   14.5184%  100.000%                          I+D references
       115073763    7.9706%   54.900%  100.000%               I   references
        94534160    6.5479%   45.101%             100.000%     D   references

        37985931    2.6311%   18.123%                40.183%   D   reads
        10553883    0.7311%    5.036%                11.165%   D   read misses
        25446671    1.7626%   12.141%                26.918%   D   writes
         4500912    0.3118%    2.148%                 4.762%   D   write misses

       355061973  i for i (icache busy)
        14545473  i for d (DRAM busy)
        13585352  i for store (DRAM busy)
        57173076  d for d (dcache busy)
        55213422  d for i (DRAM busy)
        18792436  d for store (DRAM busy)
               0  store for d (DRAM busy)
          577004  store for i (DRAM busy)
               0  store for store (DRAM busy)

      4171935848  total ticks of fpu     66.006% of total ticks
       591747328  fpOP instructions      41.113% of total
      2645853191  total dram ticks       DRAM busy 41.861%
      2299333552  float for float queue  fpu CPI=  1.593
      2186756869  memory ticks           mem CPI=  1.515
      1579516012  instruction ticks      raw CPI=  1.094
       254989434  load penalties         load CPI= 0.177
      6320595867  total ticks            CPI=      4.378

       462513111  # of ticks saved  =  7.32 percent of total
```

```
Application: tomcatv

     1626566071 instructions (including annulled)
     1626346379 instructions (excluding annulled)
           27.7 SPECmarks for tomcatv

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    16 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      234111935   14.3950%   10.189%                      I+D misses
          42481    0.0027%    0.002%    0.003%            I   misses
      234069454   14.3924%   10.187%              34.873%  D   misses

     2297780457  141.2849%  100.000%                      I+D references
     1626566071  100.0136%   70.789%  100.000%            I   references
      671214386   41.2714%   29.212%             100.000%  D   references

      482161503   29.6470%   20.984%              71.835%  D   reads
      204045768   12.5463%    8.881%              30.400%  D   read misses
      189052883   11.6244%    8.228%              28.166%  D   writes
       30023686    1.8461%    1.307%               4.474%  D   write misses

       59903900    3.6834%    2.608%               8.925%  D   write backs
       29880214    1.8373%    1.301%               4.452%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      115017082    7.0722%   39.120%                      I+D misses
           9920    0.0007%    0.004%   23.352%            I   misses
      115007162    7.0716%   39.116%              39.122%  D   misses

      294015730   18.0783%  100.000%                      I+D references
          42481    0.0027%    0.015%  100.000%            I   references
      293973249   18.0757%   99.986%             100.000%  D   references

      204045768   12.5463%   69.400%              69.410%  D   reads
       89125568    5.4802%   30.314%              30.318%  D   read misses
       30023686    1.8461%   10.212%              10.214%  D   writes
       25835288    1.5886%    8.788%               8.789%  D   write misses

         107292  i for i (icache busy)
           3622  i for d (DRAM busy)
           8661  i for store (DRAM busy)
      204037833  d for d (dcache busy)
          27122  d for i (DRAM busy)
       48672709  d for store (DRAM busy)
              0  store for d (DRAM busy)
           1006  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3297778423  total ticks of fpu    51.692% of total ticks
      500809316  fpOP instructions     30.798% of total
     3473346487  total dram ticks      DRAM busy 54.444%
     1531395750  float for float queue fpu CPI=  0.942
     2844030099  memory ticks          mem CPI=  1.749
     1815652734  instruction ticks     raw CPI=  1.116
      188602852  load penalties        load CPI= 0.116
     6379681435  total ticks           CPI=      3.923

       59248151  # of ticks saved  =  0.93 percent of total
```

```
Application: 001.gcc1.35

     1258987043 instructions (including annulled)
     1217217202 instructions (excluding annulled)
           46.7 SPECmarks for gcc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       61617708    5.0622%    3.892%                      I+D misses
       34597540    2.8423%    2.185%    2.748%            I   misses
       27020168    2.2198%    1.707%              8.335%  D   misses

     1583156354  130.0636%  100.000%                      I+D references
     1258987043  103.4316%   79.524%  100.000%            I   references
      324169311   26.6320%   20.476%            100.000%  D   references

      225256901   18.5059%   14.228%             69.487%  D   reads
       16561090    1.3606%    1.046%              5.109%  D   read misses
       98912410    8.1261%    6.248%             30.513%  D   writes
       10459078    0.8593%    0.661%              3.226%  D   write misses

       12805520    1.0520%    0.809%              3.950%  D   write backs
        2346442    0.1928%    0.148%              0.724%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       12349325    1.0146%   16.594%                      I+D misses
        6619462    0.5438%    8.894%   19.133%            I   misses
        5729863    0.4707%    7.699%             14.388%  D   misses

       74422520    6.1142%  100.000%                      I+D references
       34597540    2.8423%   46.488%  100.000%            I   references
       39824980    3.2718%   53.512%            100.000%  D   references

       16561090    1.3606%   22.253%              5.109%  D   reads
        4569805    0.3754%    6.140%              1.410%  D   read misses
       10459078    0.8593%   14.054%              3.226%  D   writes
        1146262    0.0942%    1.540%              0.354%  D   write misses

      104449139  i for i (icache busy)
        1594755  i for d (DRAM busy)
        1984403  i for store (DRAM busy)
        7571102  d for d (dcache busy)
       10357552  d for i (DRAM busy)
        4078919  d for store (DRAM busy)
              0  store for d (DRAM busy)
          13683  store for i (DRAM busy)
              0  store for store (DRAM busy)

        1419650  total ticks of fpu    0.067% of total ticks
         120384  fpOP instructions     0.010% of total
      932393187  total dram ticks      DRAM busy 44.129%
        1096908  float for float queue fpu CPI=  0.001
      735382560  memory ticks          mem CPI=  0.604
     1376244428  instruction ticks     raw CPI=  1.131
         143779  load penalties        load CPI= 0.000
     2112867675  total ticks           CPI=      1.736

      141228315  # of ticks saved  =  6.68 percent of total

        3631043  # of 2nd level dirty misses
```

```
Application: 008.espresso

     3102930952 instructions (including annulled)
     2930507476 instructions (excluding annulled)
           39.5 SPECmarks for espresso

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       59135836    2.0179%    1.505%                      I+D misses
        5417408    0.1849%    0.138%    0.175%            I   misses
       53718428    1.8331%    1.367%              6.505%  D   misses

     3928686273  134.0616%  100.000%                      I+D references
     3102930952  105.8837%   78.981%  100.000%           I   references
      825755321   28.1779%   21.019%            100.000%  D   references

      681401797   23.2520%   17.344%             82.519%  D   reads
       48714100    1.6623%    1.240%              5.899%  D   read misses
      144353524    4.9259%    3.674%             17.481%  D   writes
        5004328    0.1708%    0.127%              0.606%  D   write misses

       17837452    0.6087%    0.454%              2.160%  D   write backs
       12833124    0.4379%    0.327%              1.554%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2840428    0.0969%    3.690%                      I+D misses
         698701    0.0238%    0.908%   12.897%            I   misses
        2141727    0.0731%    2.782%              2.993%  D   misses

       76972954    2.6266%  100.000%                      I+D references
        5417408    0.1849%    7.038%  100.000%           I   references
       71555546    2.4417%   92.962%            100.000%  D   references

       48714100    1.6623%   63.287%              5.899%  D   reads
        1786855    0.0610%    2.321%              0.216%  D   read misses
        5004328    0.1708%    6.501%              0.606%  D   writes
         353338    0.0121%    0.459%              0.043%  D   write misses

       16304066  i for i (icache busy)
         207738  i for d (DRAM busy)
         177838  i for store (DRAM busy)
       42591663  d for d (dcache busy)
        1410574  d for i (DRAM busy)
        1222983  d for store (DRAM busy)
              0  store for d (DRAM busy)
           1967  store for i (DRAM busy)
              0  store for store (DRAM busy)

         108223  total ticks of fpu    0.003% of total ticks
           8755  fpOP instructions     0.000% of total
      741769983  total dram ticks      DRAM busy 19.409%
          52963  float for float queue fpu CPI=  0.000
      556515726  memory ticks          mem CPI=  0.190
     3265169566  instruction ticks     raw CPI=  1.114
           2355  load penalties        load CPI= 0.000
     3821740610  total ticks           CPI=      1.304

      209650154  # of ticks saved  =  5.49 percent of total

        1342476  # of 2nd level dirty misses
```

```
Application: spice2g6

    23810783700 instructions (including annulled)
    22775128234 instructions (excluding annulled)
           33.1 SPECmarks for spice2g6

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B            direct   write thru write allocate
1st Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
     1957916626    8.5968%   6.635%                      I+D misses
       79734588    0.3501%   0.271%    0.335%            I   misses
     1878182038    8.2467%   6.365%              32.956% D   misses

    29509960940  129.5710%  100.000%                     I+D references
    23810783700  104.5474%   80.688%  100.000%           I   references
     5699177240   25.0237%   19.313%            100.000% D   references

     4792611768   21.0432%   16.241%             84.094% D   reads
     1803111961    7.9171%    6.111%             31.639% D   read misses
      906565472    3.9806%    3.073%             15.907% D   writes
       75070077    0.3297%    0.255%              1.318% D   write misses

      171696762    0.7539%    0.582%              3.013% D   write backs
       96626685    0.4243%    0.328%              1.696% D   read mod writes
2nd Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
      726457848    3.1897%   34.113%                      I+D misses
        8725459    0.0384%    0.410%   10.944%           I   misses
      717732389    3.1514%   33.703%             35.014% D   misses

     2129613277    9.3507%  100.000%                     I+D references
       79734588    0.3501%    3.745%  100.000%           I   references
     2049878689    9.0006%   96.256%            100.000% D   references

     1803111961    7.9171%   84.669%             87.962% D   reads
      710761785    3.1208%   33.376%             34.674% D   read misses
       75070077    0.3297%    3.526%              3.663% D   writes
        6938333    0.0305%    0.326%              0.339% D   write misses

      238566350  i for i (icache busy)
        5363383  i for d (DRAM busy)
        6302776  i for store (DRAM busy)
      275963134  d for d (dcache busy)
       53633583  d for i (DRAM busy)
       70035618  d for store (DRAM busy)
              0  store for d (DRAM busy)
           5457  store for i (DRAM busy)
              0  store for store (DRAM busy)

     7841192173  total ticks of fpu    16.222% of total ticks
      962369533  fpOP instructions     4.226% of total
    25256616926  total dram ticks      DRAM busy 52.251%
     3676856610  float for float queue fpu CPI=  0.162
    19278443632  memory ticks          mem CPI=  0.847
    24784595920  instruction ticks     raw CPI=  1.089
      597255631  load penalties        load CPI= 0.027
    48337151793  total ticks           CPI=      2.123

     1027890272  # of ticks saved  =  2.13 percent of total
```

Application: doduc

```
     1316441095 instructions (including annulled)
     1304567885 instructions (excluding annulled)
           30.3 SPECmarks for doduc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       79201288    6.0711%    4.658%                      I+D misses
       32267170    2.4734%    1.898%    2.452%            I   misses
       46934118    3.5977%    2.760%              12.220% D   misses

     1700517946  130.3511%  100.000%                      I+D references
     1316441095  100.9102%   77.415%  100.000%           I   references
      384076851   29.4410%   22.586%             100.000% D   references

      298852876   22.9082%   17.575%              77.811% D   reads
       28989483    2.2222%    1.705%               7.548% D   read misses
       85223975    6.5328%    5.012%              22.190% D   writes
       17944635    1.3756%    1.056%               4.673% D   write misses

       19416837    1.4884%    1.142%               5.056% D   write backs
        1472202    0.1129%    0.087%               0.384% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       11861036    0.9092%   12.028%                      I+D misses
        3634634    0.2787%    3.686%   11.265%           I   misses
        8226402    0.6306%    8.342%              12.399% D   misses

       98618037    7.5595%  100.000%                      I+D references
       32267170    2.4734%   32.720%  100.000%           I   references
       66350867    5.0861%   67.281%             100.000% D   references

       28989483    2.2222%   29.396%              43.692% D   reads
        5607319    0.4299%    5.686%               8.452% D   read misses
       17944635    1.3756%   18.197%              27.046% D   writes
        2547767    0.1953%    2.584%               3.840% D   write misses

       75242130  i for i (icache busy)
        3946926  i for d (DRAM busy)
        5451468  i for store (DRAM busy)
       30429776  d for d (dcache busy)
       29239514  d for i (DRAM busy)
        7767834  d for store (DRAM busy)
              0  store for d (DRAM busy)
          63848  store for i (DRAM busy)
              0  store for store (DRAM busy)

     2752142075  total ticks of fpu    67.133% of total ticks
      338148549  fpOP instructions     25.921% of total
     1134563107  total dram ticks      DRAM busy 27.676%
     1716396426  float for float queue fpu CPI=  1.316
      894048982  memory ticks          mem CPI=  0.686
     1408495433  instruction ticks     raw CPI=  1.080
       80643507  load penalties        load CPI= 0.062
     4099584348  total ticks           CPI=      3.143

      220044568  # of ticks saved  =  5.37 percent of total
```

```
Application: dnasa7

     6800274207 instructions (including annulled)
     6784406515 instructions (excluding annulled)
           45.2 SPECmarks for nasa7

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B            direct   write thru write allocate
1st Level:
               #    %instrs  %I+Drefs    %Irefs    %Drefs
      1237326330   18.2378%   13.139%                      I+D misses
         5979543    0.0882%    0.064%    0.088%            I   misses
      1231346787   18.1497%   13.076%              47.049%  D   misses

      9417438218  138.8101%  100.000%                      I+D references
      6800274207  100.2339%   72.210%  100.000%            I   references
      2617164011   38.5762%   27.791%             100.000%  D   references

      1879496667   27.7032%   19.958%              71.815%  D   reads
      1145421758   16.8832%   12.163%              43.766%  D   read misses
       737667344   10.8730%    7.833%              28.186%  D   writes
        85925029    1.2666%    0.913%               3.284%  D   write misses

       502511001    7.4069%    5.336%              19.201%  D   write backs
       416585972    6.1404%    4.424%              15.918%  D   read mod writes
2nd Level:
               #    %instrs  %I+Drefs    %Irefs    %Drefs
       396529757    5.8448%   22.792%                      I+D misses
           61620    0.0010%    0.004%    1.031%            I   misses
       396468137    5.8439%   22.788%              22.867%  D   misses

      1739837264   25.6447%  100.000%                      I+D references
         5979543    0.0882%    0.344%  100.000%            I   references
      1733857721   25.5566%   99.657%             100.000%  D   references

      1145421758   16.8832%   65.835%              66.063%  D   reads
       385384256    5.6805%   22.151%              22.227%  D   read misses
        85925029    1.2666%    4.939%               4.956%  D   writes
         7445625    0.1098%    0.428%               0.430%  D   write misses

        18848451  i for i (icache busy)
           63664  i for d (DRAM busy)
           94110  i for store (DRAM busy)
       875610365  d for d (dcache busy)
          680402  d for i (DRAM busy)
       519438606  d for store (DRAM busy)
               0  store for d (DRAM busy)
           16372  store for i (DRAM busy)
               0  store for store (DRAM busy)

     15079121076  total ticks of fpu     50.771% of total ticks
      2075466939  fpOP instructions      30.592% of total
     18592222530  total dram ticks       DRAM busy 62.599%
      6695873694  float for float queue  fpu CPI=  0.987
     14769524079  memory ticks           mem CPI=  2.177
      7549415897  instruction ticks      raw CPI=  1.113
       685812709  load penalties         load CPI= 0.102
     29700626379  total ticks            CPI=      4.378

      2684779125  # of ticks saved  =  9.04 percent of total
```

```
Application: xlisp li-input.lsp

     4962043458 instructions (including annulled)
     4661592279 instructions (excluding annulled)
           61.2 SPECmarks for li

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      104944241    2.2513%    1.612%                      I+D misses
       22411850    0.4808%    0.345%    0.452%            I   misses
       82532391    1.7705%    1.268%              5.322%  D   misses

     6512926989  139.7147%  100.000%                      I+D references
     4962043458  106.4453%   76.188%  100.000%           I   references
     1550883531   33.2694%   23.813%            100.000%  D   references

     1068396583   22.9192%   16.405%             68.890%  D   reads
       54583526    1.1710%    0.839%              3.520%  D   read misses
      482486948   10.3503%    7.409%             31.111%  D   writes
       27948865    0.5996%    0.430%              1.803%  D   write misses

       54109450    1.1608%    0.831%              3.489%  D   write backs
       26160585    0.5612%    0.402%              1.687%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       10302524    0.2211%    6.478%                      I+D misses
        3787412    0.0813%    2.382%   16.900%            I   misses
        6515112    0.1398%    4.097%              4.769%  D   misses

      159053576    3.4121%  100.000%                      I+D references
       22411850    0.4808%   14.091%  100.000%           I   references
      136641726    2.9313%   85.910%            100.000%  D   references

       54583526    1.1710%   34.318%             39.947%  D   reads
        4095045    0.0879%    2.575%              2.997%  D   read misses
       27948865    0.5996%   17.572%             20.455%  D   writes
        2342248    0.0503%    1.473%              1.715%  D   write misses

       76425863  i for i (icache busy)
         449428  i for d (DRAM busy)
        1946165  i for store (DRAM busy)
       36818503  d for d (dcache busy)
        6510120  d for i (DRAM busy)
        3667293  d for store (DRAM busy)
              0  store for d (DRAM busy)
           5937  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu    0.000% of total ticks
              0  fpOP instructions     0.000% of total
     1624125696  total dram ticks      DRAM busy 24.002%
              0  float for float queue fpu CPI=  0.000
     1205552727  memory ticks          mem CPI=  0.259
     5561136309  instruction ticks     raw CPI=  1.193
              0  load penalties        load CPI= 0.000
     6766689036  total ticks           CPI=      1.452

      398601524  # of ticks saved  =  5.90 percent of total

        5595815  # of 2nd level dirty misses
```

```
Application: eqntott -s -.ioplte int_pri_3.eqn

     1376907962 instructions (including annulled)
     1326073659 instructions (excluding annulled)
           46.9 SPECmarks for eqntott

level       size     block    subblk     assoc    write miss
1st I       8 KB     32 B               2-way    write back write allocate
1st D       4 KB     16 B               2-way    write back write allocate
2nd I+D    32 KB    512 B              direct    write thru write allocate
1st Level:
              #     %instrs  %I+Drefs     %Irefs     %Drefs
       17032852     1.2845%    1.066%                        I+D misses
           7623     0.0006%    0.001%     0.001%             I   misses
       17025229     1.2839%    1.066%                 7.689% D   misses

     1598339434   120.5318%  100.000%                        I+D references
     1376907962   103.8335%   86.147%  100.000%             I   references
      221431472    16.6983%   13.854%             100.000% D   references

      202396631   15.2629%   12.663%              91.404% D   reads
       16756051    1.2636%    1.049%               7.568% D   read misses
       19034841    1.4355%    1.191%               8.597% D   writes
         269178    0.0203%    0.017%               0.122% D   write misses

         376005    0.0284%    0.024%               0.170% D   write backs
         106827    0.0081%    0.007%               0.049% D   read mod writes
2nd Level:
              #     %instrs  %I+Drefs     %Irefs     %Drefs
        3475761     0.2622%   19.966%                        I+D misses
            561     0.0001%    0.004%     7.360%             I   misses
        3475200     0.2621%   19.963%              19.972% D   misses

       17408782     1.3129%  100.000%                        I+D references
           7623     0.0006%    0.044%  100.000%             I   references
       17401159     1.3123%   99.957%             100.000% D   references

       16756051     1.2636%   96.251%              96.293% D   reads
        3455795     0.2607%   19.851%              19.860% D   read misses
         269178     0.0203%    1.547%               1.547% D   writes
          19073     0.0015%    0.110%               0.110% D   write misses

          21310  i for i (icache busy)
            104  i for d (DRAM busy)
            240  i for store (DRAM busy)
       26089775  d for d (dcache busy)
           1111  d for i (DRAM busy)
          35206  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu     0.000% of total ticks
              0  fpOP instructions      0.000% of total
      184353811  total dram ticks       DRAM busy 11.779%
              0  float for float queue  fpu CPI=  0.000
      158252342  memory ticks           mem CPI=  0.120
     1403832293  instruction ticks      raw CPI=  1.059
        3149652  load penalties         load CPI= 0.003
     1565234287  total ticks            CPI=      1.181

       26549482  # of ticks saved  =  1.70 percent of total

          89084  # of 2nd level dirty misses
```

```
Application: matrix300

     1695008913 instructions (including annulled)
     1693559295 instructions (excluding annulled)
           42.1 SPECmarks for matrix300

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      295277276   17.4354%   12.577%                      I+D misses
           1162    0.0001%    0.001%    0.001%            I   misses
      295276114   17.4353%   12.577%              45.235%  D   misses

     2347769860  138.6294%  100.000%                      I+D references
     1695008913  100.0856%   72.197%  100.000%            I   references
      652760947   38.5438%   27.804%             100.000%  D   references

      435650797   25.7240%   18.556%              66.740%  D   reads
      294562295   17.3931%   12.547%              45.126%  D   read misses
      217110150   12.8198%    9.248%              33.261%  D   writes
         713819    0.0422%    0.031%               0.110%  D   write misses

      129972785    7.6746%    5.537%              19.912%  D   write backs
      129258966    7.6324%    5.506%              19.802%  D   read mod writes

2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      215330848   12.7147%   50.637%                      I+D misses
            237    0.0001%    0.001%   20.396%            I   misses
      215330611   12.7147%   50.637%              50.637%  D   misses

      425249958   25.1099%  100.000%                      I+D references
           1162    0.0001%    0.001%  100.000%            I   references
      425248796   25.1098%  100.000%             100.000%  D   references

      294562295   17.3931%   69.269%              69.269%  D   reads
      214859561   12.6869%   50.526%              50.526%  D   read misses
         713819    0.0422%    0.168%               0.168%  D   writes
         397765    0.0235%    0.094%               0.094%  D   write misses

           3282  i for i (icache busy)
             77  i for d (DRAM busy)
            234  i for store (DRAM busy)
      188773310  d for d (dcache busy)
            583  d for i (DRAM busy)
      126625890  d for store (DRAM busy)
              0  store for d (DRAM busy)
              8  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3024001625  total ticks of fpu     42.104% of total ticks
      432000323  fpOP instructions      25.509% of total
     5323864992  total dram ticks       DRAM busy 74.126%
      690591267  float for float queue  fpu CPI=  0.408
     4363515016  memory ticks           mem CPI=  2.577
     1912122435  instruction ticks      raw CPI=  1.130
      216000307  load penalties         load CPI= 0.128
     7182229025  total ticks            CPI=      4.241

     -158787020  # of ticks saved  = -2.22 percent of total
```

```
Application: fpppp

     1448153391 instructions (including annulled)
     1443743830 instructions (excluding annulled)
           32.4 SPECmarks for fpppp

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      179674151   12.4451%    8.293%                      I+D misses
      115073763    7.9706%    5.311%    7.947%            I   misses
       64600388    4.4746%    2.982%              8.990%  D   misses

     2166746002  150.0783%  100.000%                      I+D references
     1448153391  100.3055%   66.836%  100.000%           I   references
      718592611   49.7729%   33.165%            100.000%  D   references

      588879193   40.7884%   27.179%             81.949%  D   reads
       39255681    2.7191%    1.812%              5.463%  D   read misses
      129713418    8.9846%    5.987%             18.052%  D   writes
       25344707    1.7555%    1.170%              3.527%  D   write misses

       30961775    2.1446%    1.429%              4.309%  D   write backs
        5617068    0.3891%    0.260%              0.782%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       17286127    1.1974%    8.207%                      I+D misses
        5603971    0.3882%    2.661%    4.870%            I   misses
       11682156    0.8092%    5.547%             12.225%  D   misses

      210635841   14.5896%  100.000%                      I+D references
      115073763    7.9706%   54.632%  100.000%           I   references
       95562078    6.6191%   45.369%            100.000%  D   references

       39255681    2.7191%   18.637%             41.079%  D   reads
        8494393    0.5884%    4.033%              8.889%  D   read misses
       25344707    1.7555%   12.033%             26.522%  D   writes
        3061521    0.2121%    1.454%              3.204%  D   write misses

      355912566  i for i (icache busy)
       14197551  i for d (DRAM busy)
       14882105  i for store (DRAM busy)
       57995645  d for d (dcache busy)
       53501600  d for i (DRAM busy)
       18376129  d for store (DRAM busy)
              0  store for d (DRAM busy)
         683691  store for i (DRAM busy)
              0  store for store (DRAM busy)

     4171935848  total ticks of fpu     66.614% of total ticks
      591747328  fpOP instructions      40.988% of total
     2596762365  total dram ticks       DRAM busy 41.463%
     2293202776  float for float queue  fpu CPI=  1.589
     2135182840  memory ticks           mem CPI=  1.479
     1579516012  instruction ticks      raw CPI=  1.095
      254989434  load penalties         load CPI= 0.177
     6262891062  total ticks            CPI=      4.338

      523933622  # of ticks saved  =  8.37 percent of total
```

```
Application: tomcatv

     1626566072 instructions (including annulled)
     1626346391 instructions (excluding annulled)
           28.5 SPECmarks for tomcatv

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    32 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      234671046   14.4294%   10.213%                      I+D misses
          42480    0.0027%    0.002%    0.003%            I   misses
      234628566   14.4268%   10.212%              34.956%  D   misses

     2297780456  141.2849%  100.000%                      I+D references
     1626566072  100.0136%   70.789%  100.000%            I   references
      671214384   41.2714%   29.212%             100.000%  D   references

      482161509   29.6470%   20.984%              71.835%  D   reads
      204553491   12.5775%    8.903%              30.476%  D   read misses
      189052875   11.6244%    8.228%              28.166%  D   writes
       30075075    1.8493%    1.309%               4.481%  D   write misses

       59878691    3.6818%    2.606%               8.921%  D   write backs
       29803616    1.8326%    1.298%               4.441%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       87332340    5.3699%   29.650%                      I+D misses
           8851    0.0006%    0.004%   20.836%            I   misses
       87323489    5.3694%   29.647%              29.651%  D   misses

      294549629   18.1112%  100.000%                      I+D references
          42480    0.0027%    0.015%  100.000%            I   references
      294507149   18.1086%   99.986%             100.000%  D   references

      204553491   12.5775%   69.447%              69.457%  D   reads
       69958965    4.3017%   23.752%              23.755%  D   read misses
       30075075    1.8493%   10.211%              10.213%  D   writes
       17346638    1.0667%    5.890%               5.891%  D   write misses

         105498  i for i (icache busy)
           3551  i for d (DRAM busy)
           9682  i for store (DRAM busy)
      204620494  d for d (dcache busy)
          30235  d for i (DRAM busy)
       48112327  d for store (DRAM busy)
              0  store for d (DRAM busy)
            600  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3297778423  total ticks of fpu     53.043% of total ticks
      500809316  fpOP instructions      30.794% of total
     3301143846  total dram ticks       DRAM busy 53.097%
     1542710928  float for float queue  fpu CPI=  0.949
     2670249906  memory ticks           mem CPI=  1.642
     1815652725  instruction ticks      raw CPI=  1.117
      188602852  load penalties         load CPI= 0.116
     6217216411  total ticks            CPI=      3.823

      286418493  # of ticks saved  =  4.61 percent of total
```

```
Application: 001.gcc1.35

     1259060745 instructions (including annulled)
     1217290497 instructions (excluding annulled)
           47.4 SPECmarks for gcc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       61392801    5.0434%    3.878%                      I+D misses
       34594333    2.8419%    2.185%    2.748%            I   misses
       26798468    2.2015%    1.693%              8.267%  D   misses

     1583229821  130.0618%  100.000%                      I+D references
     1259060745  103.4314%   79.525%  100.000%           I   references
      324169076   26.6304%   20.475%            100.000%  D   references

      225257129   18.5048%   14.228%             69.488%  D   reads
       16431934    1.3499%    1.038%              5.069%  D   read misses
       98911947    8.1256%    6.247%             30.512%  D   writes
       10366534    0.8516%    0.655%              3.198%  D   write misses

       12738857    1.0465%    0.805%              3.930%  D   write backs
        2372323    0.1949%    0.150%              0.732%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        8463056    0.6952%   11.416%                      I+D misses
        4578982    0.3762%    6.177%   13.236%            I   misses
        3884074    0.3191%    5.239%              9.824%  D   misses

       74130979    6.0898%  100.000%                      I+D references
       34594333    2.8419%   46.666%  100.000%           I   references
       39536646    3.2479%   53.334%            100.000%  D   references

       16431934    1.3499%   22.166%              5.069%  D   reads
        3118746    0.2562%    4.207%              0.962%  D   read misses
       10366534    0.8516%   13.984%              3.198%  D   writes
         752887    0.0618%    1.016%              0.232%  D   write misses

      104497364  i for i (icache busy)
        1591390  i for d (DRAM busy)
        2015226  i for store (DRAM busy)
        7310436  d for d (dcache busy)
       10267932  d for i (DRAM busy)
        4059832  d for store (DRAM busy)
              0  store for d (DRAM busy)
          13876  store for i (DRAM busy)
              0  store for store (DRAM busy)

        1419650  total ticks of fpu    0.068% of total ticks
         120384  fpOP instructions     0.010% of total
      901547269  total dram ticks      DRAM busy 43.288%
        1096964  float for float queue fpu CPI=  0.001
      705127389  memory ticks          mem CPI=  0.579
     1376317463  instruction ticks     raw CPI=  1.131
         143716  load penalties        load CPI= 0.000
     2082685532  total ticks           CPI=      1.711

      167540448  # of ticks saved  =  8.04 percent of total

        2529101  # of 2nd level dirty misses
```

```
Application: 008.espresso

     3102930786 instructions (including annulled)
     2930507314 instructions (excluding annulled)
          39.7 SPECmarks for espresso

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       58868398    2.0088%    1.498%                      I+D misses
        5417375    0.1849%    0.138%    0.175%            I   misses
       53451023    1.8240%    1.361%               6.473% D   misses

     3928686124  134.0616%  100.000%                      I+D references
     3102930786  105.8837%   78.981%  100.000%           I   references
      825755338   28.1779%   21.019%            100.000% D   references

      681401825   23.2520%   17.344%             82.519% D   reads
       48545015    1.6565%    1.236%              5.879% D   read misses
      144353513    4.9259%    3.674%             17.481% D   writes
        4906008    0.1674%    0.125%              0.594% D   write misses

       17705834    0.6042%    0.451%              2.144% D   write backs
       12799826    0.4368%    0.326%              1.550% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        1548092    0.0528%    2.022%                      I+D misses
         513975    0.0175%    0.671%    9.488%            I   misses
        1034117    0.0353%    1.350%               1.453% D   misses

       76573904    2.6130%  100.000%                      I+D references
        5417375    0.1849%    7.075%  100.000%           I   references
       71156529    2.4281%   92.925%            100.000% D   references

       48545015    1.6565%   63.396%              5.879% D   reads
         871713    0.0297%    1.138%              0.106% D   read misses
        4906008    0.1674%    6.407%              0.594% D   writes
         161752    0.0055%    0.211%              0.020% D   write misses

       16308807  i for i (icache busy)
         207248  i for d (DRAM busy)
         177561  i for store (DRAM busy)
       42478588  d for d (dcache busy)
        1402189  d for i (DRAM busy)
        1206249  d for store (DRAM busy)
              0  store for d (DRAM busy)
           1828  store for i (DRAM busy)
              0  store for store (DRAM busy)

         108223  total ticks of fpu    0.003% of total ticks
           8755  fpOP instructions     0.000% of total
      728254412  total dram ticks      DRAM busy 19.118%
          52935  float for float queue fpu CPI=  0.000
      544063045  memory ticks          mem CPI=  0.186
     3265169389  instruction ticks     raw CPI=  1.114
           2355  load penalties        load CPI= 0.000
     3809287724  total ticks           CPI=      1.300

      218274840  # of ticks saved  =  5.73 percent of total

         649461  # of 2nd level dirty misses
```

```
Application: spice2g6

    23810783660 instructions (including annulled)
    22775128206 instructions (excluding annulled)
          33.9 SPECmarks for spice2g6

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
     1958630368    8.5999%    6.638%                      I+D misses
       79734583    0.3501%    0.271%    0.335%            I   misses
     1878895785    8.2498%    6.367%              32.968% D   misses

    29509960888  129.5710%  100.000%                      I+D references
    23810783660  104.5474%   80.688%  100.000%           I   references
     5699177228   25.0237%   19.313%             100.000% D   references

     4792611764   21.0432%   16.241%              84.094% D   reads
     1803511822    7.9188%    6.112%              31.646% D   read misses
      906565464    3.9806%    3.073%              15.907% D   writes
       75383963    0.3310%    0.256%               1.323% D   write misses

      171994487    0.7552%    0.583%               3.018% D   write backs
       96610524    0.4242%    0.328%               1.696% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      568111268    2.4945%   26.665%                      I+D misses
        366076    0.0161%    0.172%    4.592%            I   misses
      564450504    2.4784%   26.493%              27.523% D   misses

     2130624742    9.3551%  100.000%                      I+D references
       79734583    0.3501%    3.743%  100.000%           I   references
     2050890159    9.0050%   96.258%             100.000% D   references

     1803511822    7.9188%   84.648%              87.939% D   reads
      559032796    2.4546%   26.238%              27.259% D   read misses
       75383963    0.3310%    3.539%               3.676% D   writes
        5402190    0.0238%    0.254%               0.264% D   write misses

      239039725  i for i (icache busy)
        5356032  i for d (DRAM busy)
        6250388  i for store (DRAM busy)
      276029959  d for d (dcache busy)
       52847105  d for i (DRAM busy)
       69788214  d for store (DRAM busy)
              0  store for d (DRAM busy)
           5657  store for i (DRAM busy)
              0  store for store (DRAM busy)

     7841192173  total ticks of fpu    16.645% of total ticks
      962369533  fpOP instructions     4.226% of total
    24032444907  total dram ticks      DRAM busy 51.014%
     3677085511  float for float queue fpu CPI=  0.162
    18050684012  memory ticks          mem CPI=  0.793
    24784595868  instruction ticks     raw CPI=  1.089
      597255631  load penalties        load CPI= 0.027
    47109621022  total ticks           CPI=      2.069

     2257854075  # of ticks saved  =  4.80 percent of total
```

```
Application: doduc

     1316441129 instructions (including annulled)
     1304567915 instructions (excluding annulled)
           30.6 SPECmarks for doduc

level       size     block    subblk     assoc    write miss
1st I       8 KB     32 B                2-way    write back write allocate
1st D       4 KB     16 B                2-way    write back write allocate
2nd I+D    64 KB    512 B               direct    write thru write allocate
1st Level:
              #     %instrs  %I+Drefs     %Irefs     %Drefs
       79201289     6.0711%    4.658%                          I+D misses
       32267172     2.4734%    1.898%     2.452%               I   misses
       46934117     3.5977%    2.760%               12.220%   D   misses

     1700517986   130.3511%  100.000%                          I+D references
     1316441129   100.9102%   77.415%   100.000%               I   references
      384076857    29.4410%   22.586%             100.000%   D   references

      298852879    22.9082%   17.575%              77.811%   D   reads
       28989482     2.2222%    1.705%               7.548%   D   read misses
       85223978     6.5328%    5.012%              22.190%   D   writes
       17944635     1.3756%    1.056%               4.673%   D   write misses

       19416837     1.4884%    1.142%               5.056%   D   write backs
        1472202     0.1129%    0.087%               0.384%   D   read mod writes
2nd Level:
              #     %instrs  %I+Drefs     %Irefs     %Drefs
        7020416     0.5382%    7.119%                          I+D misses
        2392534     0.1834%    2.427%     7.415%               I   misses
        4627882     0.3548%    4.693%               6.975%   D   misses

       98618038     7.5595%  100.000%                          I+D references
       32267172     2.4734%   32.720%   100.000%               I   references
       66350866     5.0861%   67.281%             100.000%   D   references

       28989482     2.2222%   29.396%              43.692%   D   reads
        3239378     0.2484%    3.285%               4.883%   D   read misses
       17944635     1.3756%   18.197%              27.046%   D   writes
        1339120     0.1027%    1.358%               2.019%   D   write misses

       75242142  i for i (icache busy)
        3946925  i for d (DRAM busy)
        5451464  i for store (DRAM busy)
       30429774  d for d (dcache busy)
       29239507  d for i (DRAM busy)
        7767834  d for store (DRAM busy)
              0  store for d (DRAM busy)
          63848  store for i (DRAM busy)
              0  store for store (DRAM busy)

     2752142075  total ticks of fpu     67.663% of total ticks
      338148549  fpOP instructions      25.921% of total
     1100530753  total dram ticks       DRAM busy 27.057%
     1718325192  float for float queue  fpu CPI=  1.318
      860016617  memory ticks           mem CPI=  0.660
     1408495471  instruction ticks      raw CPI=  1.080
       80643507  load penalties         load CPI= 0.062
     4067480787  total ticks            CPI=      3.118

      251353780  # of ticks saved  =  6.18 percent of total
```

```
Application: dnasa7

     6800274171 instructions (including annulled)
     6784406481 instructions (excluding annulled)
           45.6 SPECmarks for nasa7

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
     1237498291   18.2404%   13.141%                      I+D misses
        5979544    0.0882%    0.064%    0.088%            I   misses
     1231518747   18.1522%   13.078%              47.056%  D   misses

     9417438173  138.8101%  100.000%                      I+D references
     6800274171  100.2339%   72.210%  100.000%            I   references
     2617164002   38.5762%   27.791%             100.000%  D   references

     1879496657   27.7032%   19.958%              71.815%  D   reads
     1145289417   16.8813%   12.162%              43.761%  D   read misses
      737667345   10.8730%    7.833%              28.186%  D   writes
       86229330    1.2710%    0.916%               3.295%  D   write misses

      502715354    7.4099%    5.339%              19.209%  D   write backs
      416486024    6.1389%    4.423%              15.914%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      351764912    5.1850%   20.214%                      I+D misses
          52817    0.0008%    0.004%    0.884%            I   misses
      351712095    5.1842%   20.211%              20.281%  D   misses

     1740213565   25.6502%  100.000%                      I+D references
        5979544    0.0882%    0.344%  100.000%            I   references
     1734234021   25.5621%   99.657%             100.000%  D   references

     1145289417   16.8813%   65.814%              66.041%  D   reads
      346682676    5.1100%   19.922%              19.991%  D   read misses
       86229330    1.2710%    4.956%               4.973%  D   writes
        4717544    0.0696%    0.272%               0.273%  D   write misses

       18829463  i for i (icache busy)
          97487  i for d (DRAM busy)
          49989  i for store (DRAM busy)
      875864445  d for d (dcache busy)
         709528  d for i (DRAM busy)
      519347490  d for store (DRAM busy)
              0  store for d (DRAM busy)
          16372  store for i (DRAM busy)
              0  store for store (DRAM busy)

    15079121076  total ticks of fpu     51.255% of total ticks
     2075466939  fpOP instructions      30.592% of total
    18312531848  total dram ticks       DRAM busy 62.245%
     6696078395  float for float queue  fpu CPI=  0.987
    14488867295  memory ticks           mem CPI=  2.136
     7549415860  instruction ticks      raw CPI=  1.113
      685812709  load penalties         load CPI= 0.102
    29420174259  total ticks            CPI=      4.337

     3028858443  # of ticks saved  = 10.30 percent of total
```

```
Application: xlisp li-input.lsp

     4962043458 instructions (including annulled)
     4661592279 instructions (excluding annulled)
           61.6 SPECmarks for li

level        size    block   subblk    assoc   write miss
1st I        8 KB    32 B              2-way   write back write allocate
1st D        4 KB    16 B              2-way   write back write allocate
2nd I+D     64 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      104976462    2.2520%    1.612%                      I+D misses
       22411850    0.4808%    0.345%    0.452%            I   misses
       82564612    1.7712%    1.268%               5.324% D   misses

     6512926989  139.7147%  100.000%                      I+D references
     4962043458  106.4453%   76.188%  100.000%           I   references
     1550883531   33.2694%   23.813%            100.000% D   references

     1068396583   22.9192%   16.405%             68.890% D   reads
       54729156    1.1741%    0.841%              3.529% D   read misses
      482486948   10.3503%    7.409%             31.111% D   writes
       27835456    0.5972%    0.428%              1.795% D   write misses

       53707948    1.1522%    0.825%              3.464% D   write backs
       25872492    0.5551%    0.398%              1.669% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        5671969    0.1217%    3.575%                      I+D misses
        2240611    0.0481%    1.412%    9.998%            I   misses
        3431358    0.0737%    2.163%               2.519% D   misses

      158684297    3.4041%  100.000%                      I+D references
       22411850    0.4808%   14.124%  100.000%           I   references
      136272447    2.9234%   85.877%            100.000% D   references

       54729156    1.1741%   34.490%             40.162% D   reads
        1397362    0.0300%    0.881%              1.026% D   read misses
       27835456    0.5972%   17.542%             20.427% D   writes
        1966805    0.0422%    1.240%              1.444% D   write misses

       76547532  i for i (icache busy)
         481828  i for d (DRAM busy)
        1924279  i for store (DRAM busy)
       35944209  d for d (dcache busy)
        6366737  d for i (DRAM busy)
        2824693  d for store (DRAM busy)
              0  store for d (DRAM busy)
           5933  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu    0.000% of total ticks
              0  fpOP instructions     0.000% of total
     1584548062  total dram ticks      DRAM busy 23.557%
              0  float for float queue fpu CPI=  0.000
     1165354832  memory ticks          mem CPI=  0.250
     5561136309  instruction ticks     raw CPI=  1.193
              0  load penalties        load CPI= 0.000
     6726491141  total ticks           CPI=      1.443

      432884982  # of ticks saved  =  6.44 percent of total

        3213768  # of 2nd level dirty misses
```

```
Application: eqntott -s -.ioplte int_pri_3.eqn

     1376907962 instructions (including annulled)
     1326073659 instructions (excluding annulled)
           47.1 SPECmarks for eqntott

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       17032547    1.2845%    1.066%                      I+D misses
           7623    0.0006%    0.001%    0.001%            I   misses
       17024924    1.2839%    1.066%               7.689% D   misses

     1598339434  120.5318%  100.000%                      I+D references
     1376907962  103.8335%   86.147%  100.000%            I   references
      221431472   16.6983%   13.854%             100.000% D   references

      202396631   15.2629%   12.663%              91.404% D   reads
       16755884    1.2636%    1.049%               7.568% D   read misses
       19034841    1.4355%    1.191%               8.597% D   writes
         269040    0.0203%    0.017%               0.122% D   write misses

         375856    0.0284%    0.024%               0.170% D   write backs
         106816    0.0081%    0.007%               0.049% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2949016    0.2224%   16.941%                      I+D misses
             45I   0.0001%    0.003%    5.917%            I   misses
        2948565    0.2224%   16.938%              16.946% D   misses

       17408330    1.3128%  100.000%                      I+D references
           7623    0.0006%    0.044%  100.000%            I   references
       17400707    1.3122%   99.957%             100.000% D   references

       16755884    1.2636%   96.253%              96.295% D   reads
        2934556    0.2213%   16.858%              16.865% D   read misses
         269040    0.0203%    1.546%               1.547% D   writes
          13865    0.0011%    0.080%               0.080% D   write misses

          21320  i for i (icache busy)
            105  i for d (DRAM busy)
            242  i for store (DRAM busy)
       26089682  d for d (dcache busy)
           1099  d for i (DRAM busy)
          35199  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu    0.000% of total ticks
              0  fpOP instructions     0.000% of total
      180174537  total dram ticks      DRAM busy 11.542%
              0  float for float queue fpu CPI=  0.000
      154074325  memory ticks          mem CPI=  0.117
     1403832293  instruction ticks     raw CPI=  1.059
        3149652  load penalties        load CPI= 0.003
     1561056270  total ticks           CPI=      1.178

       30142570  # of ticks saved  =  1.94 percent of total

          71442  # of 2nd level dirty misses
```

```
Application: matrix300

     1695008957 instructions (including annulled)
     1693559338 instructions (excluding annulled)
           42.5 SPECmarks for matrix300

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs

      295281420   17.4356%   12.578%                      I+D misses
           1157    0.0001%    0.001%    0.001%            I   misses
      295280263   17.4355%   12.578%              45.236%  D   misses

     2347769916  138.6294%  100.000%                      I+D references
     1695008957  100.0856%   72.197%  100.000%            I   references
      652760959   38.5438%   27.804%             100.000%  D   references

      435650808   25.7240%   18.556%              66.740%  D   reads
      294566887   17.3934%   12.547%              45.127%  D   read misses
      217110151   12.8198%    9.248%              33.261%  D   writes
         713376    0.0422%    0.031%               0.110%  D   write misses

      129975797    7.6748%    5.537%              19.912%  D   write backs
      129262421    7.6326%    5.506%              19.803%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      206336555   12.1837%   48.521%                      I+D misses
            212    0.0001%    0.001%   18.324%            I   misses
      206336343   12.1836%   48.521%              48.521%  D   misses

      425257117   25.1103%  100.000%                      I+D references
           1157    0.0001%    0.001%  100.000%            I   references
      425255960   25.1102%  100.000%             100.000%  D   references

      294566887   17.3934%   69.268%              69.269%  D   reads
      205949628   12.1608%   48.430%              48.430%  D   read misses
         713376    0.0422%    0.168%               0.168%  D   writes
         360163    0.0213%    0.085%               0.085%  D   write misses

           3235  i for i (icache busy)
             84  i for d (DRAM busy)
            237  i for store (DRAM busy)
      188771206  d for d (dcache busy)
            620  d for i (DRAM busy)
      126529121  d for store (DRAM busy)
              0  store for d (DRAM busy)
              8  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3024001625  total ticks of fpu     42.546% of total ticks
      432000323  fpOP instructions      25.509% of total
     5249434418  total dram ticks       DRAM busy 73.857%
      690538846  float for float queue  fpu CPI=  0.408
     4288964107  memory ticks           mem CPI=  2.533
     1912122482  instruction ticks      raw CPI=  1.130
      216000307  load penalties         load CPI= 0.128
     7107625742  total ticks            CPI=      4.197

     -106793300  # of ticks saved  = -1.51 percent of total
```

```
Application: fpppp

     1448153360 instructions (including annulled)
     1443743814 instructions (excluding annulled)
           32.6 SPECmarks for fpppp

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      179674154   12.4451%    8.293%                      I+D misses
      115073765    7.9706%    5.311%    7.947%            I   misses
       64600389    4.4746%    2.982%              8.990%  D   misses

     2166745959  150.0783%  100.000%                      I+D references
     1448153360  100.3055%   66.836%  100.000%           I   references
      718592599   49.7729%   33.165%            100.000%  D   references

      588879190   40.7884%   27.179%             81.949%  D   reads
       39255681    2.7191%    1.812%              5.463%  D   read misses
      129713409    8.9846%    5.987%             18.052%  D   writes
       25344708    1.7555%    1.170%              3.527%  D   write misses

       30961776    2.1446%    1.429%              4.309%  D   write backs
        5617068    0.3891%    0.260%              0.782%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       10956960    0.7590%    5.202%                      I+D misses
        3214112    0.2227%    1.526%    2.794%            I   misses
        7742848    0.5364%    3.676%              8.103%  D   misses

      210635845   14.5896%  100.000%                      I+D references
      115073765    7.9706%   54.632%  100.000%           I   references
       95562080    6.6191%   45.369%            100.000%  D   references

       39255681    2.7191%   18.637%             41.079%  D   reads
        5173254    0.3584%    2.457%              5.414%  D   read misses
       25344708    1.7555%   12.033%             26.522%  D   writes
        2524993    0.1749%    1.199%              2.643%  D   write misses

      355912566  i for i (icache busy)
       14197551  i for d (DRAM busy)
       14882108  i for store (DRAM busy)
       57995642  d for d (dcache busy)
       53501597  d for i (DRAM busy)
       18376130  d for store (DRAM busy)
              0  store for d (DRAM busy)
         683691  store for i (DRAM busy)
              0  store for store (DRAM busy)

     4171935848  total ticks of fpu     67.088% of total ticks
      591747328  fpOP instructions      40.988% of total
     2551524329  total dram ticks       DRAM busy 41.031%
     2294211460  float for float queue  fpu CPI=  1.590
     2089944784  memory ticks           mem CPI=  1.448
     1579515967  instruction ticks      raw CPI=  1.095
      254989434  load penalties         load CPI= 0.177
     6218661645  total ticks            CPI=      4.308

      564036822  # of ticks saved  =  9.08 percent of total
```

Application: tomcatv

```
     1626566032 instructions (including annulled)
     1626346353 instructions (excluding annulled)
           30.9 SPECmarks for tomcatv

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       4 KB    16 B              2-way   write back write allocate
2nd I+D    64 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      234111934   14.3950%   10.189%                      I+D misses
          42480    0.0027%    0.002%    0.003%            I   misses
      234069454   14.3924%   10.187%              34.873%  D   misses

     2297780406  141.2849%  100.000%                      I+D references
     1626566032  100.0136%   70.789%  100.000%            I   references
      671214374   41.2714%   29.212%             100.000%  D   references

      482161499   29.6470%   20.984%              71.835%  D   reads
      204045768   12.5463%    8.881%              30.400%  D   read misses
      189052875   11.6244%    8.228%              28.166%  D   writes
       30023686    1.8461%    1.307%               4.474%  D   write misses

       59903900    3.6834%    2.608%               8.925%  D   write backs
       29880214    1.8373%    1.301%               4.452%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       17302079    1.0639%    5.885%                      I+D misses
           7370    0.0005%    0.003%   17.350%            I   misses
       17294709    1.0635%    5.883%               5.884%  D   misses

      294015729   18.0783%  100.000%                      I+D references
          42480    0.0027%    0.015%  100.000%            I   references
      293973249   18.0757%   99.986%             100.000%  D   references

      204045768   12.5463%   69.400%              69.410%  D   reads
       10647870    0.6548%    3.622%               3.623%  D   read misses
       30023686    1.8461%   10.212%              10.214%  D   writes
        6632673    0.4079%    2.256%               2.257%  D   write misses

         107292  i for i (icache busy)
           3622  i for d (DRAM busy)
           8661  i for store (DRAM busy)
      204037833  d for d (dcache busy)
          27117  d for i (DRAM busy)
       48672709  d for store (DRAM busy)
              0  store for d (DRAM busy)
           1006  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3297778423  total ticks of fpu    57.703% of total ticks
      500809316  fpOP instructions     30.794% of total
     2778167673  total dram ticks      DRAM busy 48.611%
     1562001301  float for float queue fpu CPI=  0.961
     2148851286  memory ticks          mem CPI=  1.322
     1815652683  instruction ticks     raw CPI=  1.117
      188602852  load penalties        load CPI= 0.116
     5715108122  total ticks           CPI=      3.515

      752050090  # of ticks saved  = 13.16 percent of total
```

```
Application: 001.gcc1.35

     1258997667 instructions (including annulled)
     1217227427 instructions (excluding annulled)
           49.4 SPECmarks for gcc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       55118803    4.5282%    3.482%                      I+D misses
       34598255    2.8424%    2.185%    2.748%            I   misses
       20520548    1.6858%    1.296%              6.330%  D   misses

     1583166971  130.0634%  100.000%                      I+D references
     1258997667  103.4316%   79.524%  100.000%           I   references
      324169304   26.6318%   20.476%            100.000%  D   references

      225256896   18.5057%   14.228%             69.487%  D   reads
       11451859    0.9408%    0.723%              3.533%  D   read misses
       98912408    8.1260%    6.248%             30.513%  D   writes
        9068689    0.7450%    0.573%              2.798%  D   write misses

       10856284    0.8919%    0.686%              3.349%  D   write backs
        1787595    0.1469%    0.113%              0.551%  D   read mod writes

2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        4550041    0.3738%    6.897%                      I+D misses
        2548580    0.2094%    3.863%    7.366%            I   misses
        2001461    0.1644%    3.034%              6.379%  D   misses

       65973660    5.4200%  100.000%                      I+D references
       34598255    2.8424%   52.443%  100.000%           I   references
       31375405    2.5776%   47.557%            100.000%  D   references

       11451859    0.9408%   17.358%              3.533%  D   reads
        1494335    0.1228%    2.265%              0.461%  D   read misses
        9068689    0.7450%   13.746%              2.798%  D   writes
         504430    0.0414%    0.765%              0.156%  D   write misses

      107240884  i for i (icache busy)
        1028779  i for d (DRAM busy)
        1486486  i for store (DRAM busy)
        5097161  d for d (dcache busy)
        6548968  d for i (DRAM busy)
        3328892  d for store (DRAM busy)
              0  store for d (DRAM busy)
           8906  store for i (DRAM busy)
              0  store for store (DRAM busy)

        1419650  total ticks of fpu    0.071% of total ticks
         120384  fpOP instructions     0.010% of total
      800037675  total dram ticks      DRAM busy 39.991%
        1096692  float for float queue fpu CPI=  0.001
      623062006  memory ticks          mem CPI=  0.512
     1376255042  instruction ticks     raw CPI=  1.131
         143491  load penalties        load CPI= 0.000
     2000557231  total ticks           CPI=      1.644

      168858627  # of ticks saved  =  8.44 percent of total

        1442927  # of 2nd level dirty misses
```

```
Application: 008.espresso

     3102930952 instructions (including annulled)
     2930507476 instructions (excluding annulled)
           41.0 SPECmarks for espresso

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate

1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       44467253    1.5174%    1.132%                      I+D misses
        5417408    0.1849%    0.138%    0.175%            I   misses
       39049845    1.3325%    0.994%              4.729%  D   misses

     3928686273  134.0616%  100.000%                      I+D references
     3102930952  105.8837%   78.981%  100.000%           I   references
      825755321   28.1779%   21.019%            100.000%  D   references

      681401797   23.2520%   17.344%             82.519%  D   reads
       35842942    1.2231%    0.912%              4.341%  D   read misses
      144353524    4.9259%    3.674%             17.481%  D   writes
        3206903    0.1094%    0.082%              0.388%  D   write misses

       14547660    0.4964%    0.370%              1.762%  D   write backs
       11340757    0.3870%    0.289%              1.373%  D   read mod writes

2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
         544274    0.0186%    0.922%                      I+D misses
         332979    0.0114%    0.564%    6.146%            I   misses
         211295    0.0072%    0.358%              0.394%  D   misses

       59014234    2.0138%  100.000%                      I+D references
        5417408    0.1849%    9.180%  100.000%           I   references
       53596826    1.8289%   90.820%            100.000%  D   references

       35842942    1.2231%   60.736%              4.341%  D   reads
         175458    0.0060%    0.297%              0.021%  D   read misses
        3206903    0.1094%    5.434%              0.388%  D   writes
          35750    0.0012%    0.061%              0.004%  D   write misses

       16676474  i for i (icache busy)
         128406  i for d (DRAM busy)
         111445  i for store (DRAM busy)
       27850150  d for d (dcache busy)
         910154  d for i (DRAM busy)
         764898  d for store (DRAM busy)
              0  store for d (DRAM busy)
            358  store for i (DRAM busy)
              0  store for store (DRAM busy)

         108223  total ticks of fpu    0.003% of total ticks
           8755  fpOP instructions     0.000% of total
      562414373  total dram ticks      DRAM busy 15.280%
          52805  float for float queue fpu CPI=  0.000
      415561332  memory ticks          mem CPI=  0.142
     3265169566  instruction ticks     raw CPI=  1.114
           2355  load penalties        load CPI= 0.000
     3680786058  total ticks           CPI=      1.256

      173009550  # of ticks saved  =  4.70 percent of total

         145604  # of 2nd level dirty misses
```

Application: spice26

```
    23810783680 instructions (including annulled)
    22775128214 instructions (excluding annulled)
           38.0 SPECmarks for spice2g6

level       size    block   subblk    assoc   write miss
1st I    1st I       8 KB    32 B     2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate

1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
     1482298083    6.5084%    5.023%                      I+D misses
       79734784    0.3501%    0.270%    0.335%            I   misses
     1402563299    6.1583%    4.753%              24.610% D   misses

    29509960877  129.5710%  100.000%                      I+D references
    23810783651  104.5473%   80.687%  100.000%           I   references
     5699177226   25.0237%   19.313%             100.000% D   references

     4792611764   21.0432%   16.241%              84.093% D   reads
     1341752460    5.8913%    4.547%              23.543% D   read misses
      906565462    3.9805%    3.072%              15.907% D   writes
       60810839    0.2670%    0.206%               1.067% D   write misses

      148434719    0.6517%    0.503%               2.604% D   write backs
       87624093    0.3847%    0.297%               1.537% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs

      321453964    1.4114%   19.712%                      I+D misses
        1283814    0.0056%    0.079%    1.610%            I   misses
      320170150    1.4058%   19.634%              20.643% D   misses

     1630732521    7.1601%  100.000%                      I+D references
       79734784    0.3501%    4.890%  100.000%           I   references
     1550997737    6.8101%   95.110%             100.000% D   references

     1341752460    5.8913%   82.279%              23.543% D   reads
      316423004    1.3893%   19.404%               5.552% D   read misses
       60810839    0.2670%    3.729%               1.067% D   writes
        3742281    0.0164%    0.229%               0.066% D   write misses

      242703899  i for i (icache busy)
        2048073  i for d (DRAM busy)
        5980742  i for store (DRAM busy)
      217843410  d for d (dcache busy)
       47899058  d for i (DRAM busy)
       49658327  d for store (DRAM busy)
              0  store for d (DRAM busy)
            104  store for i (DRAM busy)
              0  store for store (DRAM busy)

     7841192173  total ticks of fpu    18.603% of total ticks
      962369533  fpOP instructions     4.226% of total
    17599089357  total dram ticks      DRAM busy 41.754%
     3734015262  float for float queue fpu CPI=  0.164
    13033821055  memory ticks          mem CPI=  0.572
    24784595856  instruction ticks     raw CPI=  1.088
      597255614  load penalties        load CPI= 0.026
    42149687787  total ticks           CPI=      1.851

     2575181654  # of ticks saved  =  6.11 percent of total

       45855343  # of 2nd level dirty misses
```

```
Application: doduc

     1316441149 instructions (including annulled)
     1304567934 instructions (excluding annulled)
           31.7 SPECmarks for doduc

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate

1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       63145612    4.8404%    3.714%                      I+D misses
       32267169    2.4734%    1.898%    2.452%            I   misses
       30878443    2.3670%    1.816%              8.040%  D   misses

     1700518013  130.3511%  100.000%                      I+D references
     1316441149  100.9102%   77.415%  100.000%           I   references
      384076864   29.4410%   22.586%            100.000%  D   references

      298852887   22.9082%   17.575%             77.811%  D   reads
       17053863    1.3073%    1.003%              4.441%  D   read misses
       85223977    6.5328%    5.012%             22.190%  D   writes
       13824580    1.0598%    0.813%              3.600%  D   write misses

       14681059    1.1254%    0.864%              3.823%  D   write backs
         856479    0.0657%    0.051%              0.223%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2601828    0.1995%    3.344%                      I+D misses
        1071083    0.0822%    1.377%    3.320%            I   misses
        1530745    0.1174%    1.967%              3.360%  D   misses

       77826477    5.9657%  100.000%                      I+D references
       32267169    2.4734%   41.461%  100.000%           I   references
       45559308    3.4923%   58.540%            100.000%  D   references

       17053863    1.3073%   21.913%             37.433%  D   reads
        1009839    0.0775%    1.298%              2.217%  D   read misses
       13824580    1.0598%   17.764%             30.345%  D   writes
         493822    0.0379%    0.635%              1.084%  D   write misses

       81481445  i for i (icache busy)
        2887850  i for d (DRAM busy)
        4001369  i for store (DRAM busy)
       20205646  d for d (dcache busy)
       21285943  d for i (DRAM busy)
        5879124  d for store (DRAM busy)
              0  store for d (DRAM busy)
          52435  store for i (DRAM busy)
              0  store for store (DRAM busy)

     2752142075  total ticks of fpu    70.130% of total ticks
      338148549  fpOP instructions     25.921% of total
      880851845  total dram ticks      DRAM busy 22.446%
     1748875208  float for float queue fpu CPI=  1.341
      686364719  memory ticks          mem CPI=  0.527
     1408495492  instruction ticks     raw CPI=  1.080
       80643507  load penalties        load CPI= 0.062
     3924378926  total ticks           CPI=      3.009

      217381130  # of ticks saved  =  5.54 percent of total

        1216417  # of 2nd level dirty misses
```

```
Application: dnasa7

     6800274227 instructions (including annulled)
     6784406530 instructions (excluding annulled)
           48.1 SPECmarks for nasa7

level        size     block    subblk     assoc    write miss
1st I        8 KB     32 B               2-way    write back write allocate
1st D        8 KB     16 B               2-way    write back write allocate
2nd I+D    128 KB    512 B             direct    write thru write allocate
1st Level:
               #     %instrs  %I+Drefs     %Irefs     %Drefs
      1033205318    15.2292%   10.972%                        I+D misses
         5979543     0.0882%    0.064%    0.088%              I   misses
      1027225775    15.1410%   10.908%               39.250%  D   misses

      9417438243   138.8101%  100.000%                        I+D references
      6800274227   100.2339%   72.210%  100.000%              I   references
      2617164016    38.5762%   27.791%             100.000%  D   references

      1879496668    27.7032%   19.958%               71.815%  D   reads
       942267014    13.8888%   10.006%               36.004%  D   read misses
       737667348    10.8730%    7.833%               28.186%  D   writes
        84958761     1.2523%    0.903%                3.247%  D   write misses

       491061675     7.2381%    5.215%               18.764%  D   write backs
       406102914     5.9859%    4.313%               15.517%  D   read mod writes
2nd Level:
               #     %instrs  %I+Drefs     %Irefs     %Drefs
       296935371     4.3768%   19.481%                        I+D misses
            4923     0.0001%    0.001%    0.083%              I   misses
       296930448     4.3767%   19.481%               19.557%  D   misses

      1524266894    22.4673%  100.000%                        I+D references
         5979543     0.0882%    0.393%  100.000%              I   references
      1518287351    22.3791%   99.608%             100.000%  D   references

       942267014    13.8888%   61.818%               62.062%  D   reads
       294019897     4.3338%   19.290%               19.366%  D   read misses
        84958761     1.2523%    5.574%                5.596%  D   writes
         2789790     0.0412%    0.184%                0.184%  D   write misses

        19182542  i for i (icache busy)
           28717  i for d (DRAM busy)
           34031  i for store (DRAM busy)
       738811944  d for d (dcache busy)
          265671  d for i (DRAM busy)
       428613755  d for store (DRAM busy)
               0  store for d (DRAM busy)
              45  store for i (DRAM busy)
               0  store for store (DRAM busy)

     15079121076  total ticks of fpu    54.118% of total ticks
      2075466939  fpOP instructions     30.592% of total
     15991934353  total dram ticks      DRAM busy 57.394%
      7040252699  float for float queue fpu CPI=  1.038
     12588131747  memory ticks          mem CPI=  1.856
      7549415923  instruction ticks     raw CPI=  1.113
       685812709  load penalties        load CPI= 0.102
     27863613078  total ticks           CPI=      4.108

      2768768231  # of ticks saved  =  9.94 percent of total

       177082961  # of 2nd level dirty misses
```

```
Application: xlisp li-input.lsp

     4962043458 instructions (including annulled)
     4661592279 instructions (excluding annulled)
           63.7 SPECmarks for li

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       80635512    1.7298%    1.239%                      I+D misses
       22411850    0.4808%    0.345%    0.452%            I   misses
       58223662    1.2491%    0.894%              3.755%  D   misses

     6512926989  139.7147%  100.000%                      I+D references
     4962043458  106.4453%   76.188%  100.000%           I   references
     1550883531   33.2694%   23.813%            100.000%  D   references

     1068396583   22.9192%   16.405%             68.890%  D   reads
       37515443    0.8048%    0.577%              2.419%  D   read misses
      482486948   10.3503%    7.409%             31.111%  D   writes
       20708219    0.4443%    0.318%              1.336%  D   write misses

       45510094    0.9763%    0.699%              2.935%  D   write backs
       24801875    0.5321%    0.381%              1.600%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2680302    0.0575%    2.125%                      I+D misses
        1376322    0.0296%    1.092%    6.142%            I   misses
        1303980    0.0280%    1.034%              1.258%  D   misses

      126145307    2.7061%  100.000%                      I+D references
       22411850    0.4808%   17.767%  100.000%           I   references
      103733457    2.2253%   82.234%            100.000%  D   references

       37515443    0.8048%   29.740%             36.166%  D   reads
         488104    0.0105%    0.387%              0.471%  D   read misses
       20708219    0.4443%   16.417%             19.963%  D   writes
         815876    0.0176%    0.647%              0.787%  D   write misses

       78581420  i for i (icache busy)
         206679  i for d (DRAM busy)
         984865  i for store (DRAM busy)
       26850476  d for d (dcache busy)
        3503117  d for i (DRAM busy)
        2284609  d for store (DRAM busy)
              0  store for d (DRAM busy)
           6001  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu     0.000% of total ticks
              0  fpOP instructions      0.000% of total
     1268444806  total dram ticks       DRAM busy 19.526%
              0  float for float queue  fpu CPI=  0.000
      935190502  memory ticks           mem CPI=  0.201
     5561136309  instruction ticks      raw CPI=  1.193
              0  load penalties         load CPI= 0.000
     6496326811  total ticks            CPI=      1.394

      357768849  # of ticks saved  =  5.51 percent of total

        1257483  # of 2nd level dirty misses
```

```
Application: eqntott -s -.ioplte int_pri_3.eqn

     1376907962 instructions (including annulled)
     1326073659 instructions (excluding annulled)
           47.3 SPECmarks for eqntott
level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       16564949    1.2492%    1.037%                      I+D misses
           7623    0.0006%    0.001%    0.001%            I   misses
       16557326    1.2486%    1.036%               7.478% D   misses

     1598339434  120.5318%  100.000%                      I+D references
     1376907962  103.8335%   86.147%  100.000%           I   references
      221431472   16.6983%   13.854%            100.000% D   references

      202396631   15.2629%   12.663%             91.404% D   reads
       16298941    1.2292%    1.020%              7.361% D   read misses
       19034841    1.4355%    1.191%              8.597% D   writes
         258385    0.0195%    0.017%              0.117% D   write misses

         360626    0.0272%    0.023%              0.163% D   write backs
         102241    0.0078%    0.007%              0.047% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2393109    0.1805%   14.140%                      I+D misses
            380    0.0001%    0.003%    4.985%            I   misses
        2392729    0.1805%   14.137%            14.144% D   misses

       16925406    1.2764%  100.000%                      I+D references
           7623    0.0006%    0.046%  100.000%           I   references
       16917783    1.2758%   99.955%            100.000% D   references

       16298941    1.2292%   96.299%             96.343% D   reads
        2383333    0.1798%   14.082%             14.088% D   read misses
         258385    0.0195%    1.527%              1.528% D   writes
           9343    0.0008%    0.056%              0.056% D   write misses

          21504  i for i (icache busy)
             87  i for d (DRAM busy)
            165  i for store (DRAM busy)
       25540390  d for d (dcache busy)
            856  d for i (DRAM busy)
          28803  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu     0.000% of total ticks
              0  fpOP instructions      0.000% of total
      171448125  total dram ticks       DRAM busy 11.039%
              0  float for float queue  fpu CPI=  0.000
      146240843  memory ticks           mem CPI=  0.111
     1403832293  instruction ticks      raw CPI=  1.059
        3149652  load penalties         load CPI= 0.003
     1553222788  total ticks            CPI=      1.172

       32017425  # of ticks saved  =  2.07 percent of total

          49863  # of 2nd level dirty misses
```

```
Application: matrix300

     1695008871 instructions (including annulled)
     1693559255 instructions (excluding annulled)
           52.8 SPECmarks for matrix300

level        size    block   subblk    assoc    write miss
1st I        8 KB    32 B              2-way    write back write allocate
1st D        8 KB    16 B              2-way    write back write allocate
2nd I+D    128 KB   512 B             direct    write thru write allocate
1st Level:
               #    %instrs  %I+Drefs    %Irefs    %Drefs
       204608877   12.0816%    8.716%                      I+D misses
            1162    0.0001%    0.001%    0.001%            I   misses
       204607715   12.0816%    8.715%              31.345%  D   misses

      2347769808  138.6294%  100.000%                      I+D references
      1695008871  100.0856%   72.197%  100.000%           I   references
       652760937   38.5438%   27.804%             100.000%  D   references

       435650787   25.7240%   18.556%              66.740%  D   reads
       204026212   12.0472%    8.691%              31.256%  D   read misses
       217110150   12.8198%    9.248%              33.261%  D   writes
          581503    0.0344%    0.025%               0.090%  D   write misses

        46540513    2.7481%    1.983%               7.130%  D   write backs
        45959010    2.7138%    1.958%               7.041%  D   read mod writes
2nd Level:
               #    %instrs  %I+Drefs    %Irefs    %Drefs
       109324465    6.4554%   43.530%                      I+D misses
             198    0.0001%    0.001%   17.040%           I   misses
       109324267    6.4553%   43.530%              43.530%  D   misses

       251149061   14.8297%  100.000%                      I+D references
            1162    0.0001%    0.001%  100.000%           I   references
       251147899   14.8296%  100.000%             100.000%  D   references

       204026212   12.0472%   81.238%              81.238%  D   reads
       109120924    6.4433%   43.449%              43.449%  D   read misses
          581503    0.0344%    0.232%               0.232%  D   writes
          203011    0.0120%    0.081%               0.081%  D   write misses

            3278  i for i (icache busy)
              79  i for d (DRAM busy)
             228  i for store (DRAM busy)
       165323297  d for d (dcache busy)
             594  d for i (DRAM busy)
        39247512  d for store (DRAM busy)
               0  store for d (DRAM busy)
               8  store for i (DRAM busy)
               0  store for store (DRAM busy)

      3024001625  total ticks of fpu    52.916% of total ticks
       432000323  fpOP instructions     25.509% of total
      3076330086  total dram ticks      DRAM busy 53.832%
      1059206625  float for float queue fpu CPI=  0.626
      2527454413  memory ticks          mem CPI=  1.493
      1912122391  instruction ticks     raw CPI=  1.130
       216000307  load penalties        load CPI= 0.128
      5714783736  total ticks           CPI=      3.375

        -6606058  # of ticks saved  = -0.12 percent of total

        33773923  # of 2nd level dirty misses
```

```
Application: fpppp

     1448153349 instructions (including annulled)
     1443743790 instructions (excluding annulled)
           34.7 SPECmarks for fpppp

level       size    block   subblk    assoc   write miss
1st I        8 KB    32 B              2-way   write back write allocate
1st D        8 KB    16 B              2-way   write back write allocate
2nd I+D    128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      143134606    9.9142%    6.606%                      I+D misses
      115073763    7.9706%    5.311%    7.947%            I   misses
       28060843    1.9437%    1.296%              3.905%  D   misses

     2166745950  150.0783%  100.000%                      I+D references
     1448153349  100.3055%   66.836%  100.000%           I   references
      718592601   49.7729%   33.165%            100.000%  D   references

      588879183   40.7884%   27.179%             81.949%  D   reads
       17710303    1.2267%    0.818%              2.465%  D   read misses
      129713418    8.9846%    5.987%             18.052%  D   writes
       10350540    0.7170%    0.478%              1.441%  D   write misses

       13892891    0.9623%    0.642%              1.934%  D   write backs
        3542351    0.2454%    0.164%              0.493%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2673134    0.1852%    1.703%                      I+D misses
        1225368    0.0849%    0.781%    1.065%            I   misses
        1447766    0.1003%    0.922%              3.451%  D   misses

      157027250   10.8764%  100.000%                      I+D references
      115073763    7.9706%   73.283%  100.000%           I   references
       41953487    2.9059%   26.718%            100.000%  D   references

       17710303    1.2267%   11.279%             42.215%  D   reads
         947336    0.0657%    0.604%              2.259%  D   read misses
       10350540    0.7170%    6.592%             24.672%  D   writes
         498470    0.0346%    0.318%              1.189%  D   write misses

      374254394  i for i (icache busy)
        7155157  i for d (DRAM busy)
        7369803  i for store (DRAM busy)
       26585093  d for d (dcache busy)
       28876443  d for i (DRAM busy)
        9941892  d for store (DRAM busy)
              0  store for d (DRAM busy)
          83040  store for i (DRAM busy)
              0  store for store (DRAM busy)

     4171935848  total ticks of fpu     71.352% of total ticks
      591747328  fpOP instructions      40.988% of total
     2008969988  total dram ticks       DRAM busy 34.360%
     2365550486  float for float queue  fpu CPI=  1.639
     1646932771  memory ticks           mem CPI=  1.141
     1579515968  instruction ticks      raw CPI=  1.095
      254989434  load penalties         load CPI= 0.177
     5846988659  total ticks            CPI=      4.050

      454009051  # of ticks saved  =  7.77 percent of total

        1121184  # of 2nd level dirty misses
```

```
Application: tomcatv

     1626566091 instructions (including annulled)
     1626346394 instructions (excluding annulled)
           33.2 SPECmarks for tomcatv

level       size    block   subblk    assoc   write miss
1st I       8 KB    32 B              2-way   write back write allocate
1st D       8 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      175741703   10.8060%    7.649%                      I+D misses
          42479    0.0027%    0.002%    0.003%            I   misses
      175699224   10.8034%    7.647%              26.177% D   misses

     2297780482  141.2849%  100.000%                      I+D references
     1626566091  100.0136%   70.789%  100.000%           I   references
      671214391   41.2714%   29.212%             100.000% D   references

      482161504   29.6470%   20.984%              71.835% D   reads
      146013109    8.9780%    6.355%              21.754% D   read misses
      189052887   11.6244%    8.228%              28.166% D   writes
       29686115    1.8254%    1.292%               4.423% D   write misses

       53009079    3.2594%    2.307%               7.898% D   write backs
       23322964    1.4341%    1.016%               3.475% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       12762288    0.7848%    5.580%                      I+D misses
           6236    0.0004%    0.003%   14.681%            I   misses
       12756052    0.7844%    5.577%               5.578% D   misses

      228750570   14.0654%  100.000%                      I+D references
          42479    0.0027%    0.019%  100.000%           I   references
      228708091   14.0627%   99.982%             100.000% D   references

      146013109    8.9780%   63.831%              63.843% D   reads
        7347310    0.4518%    3.212%               3.213% D   read misses
       29686115    1.8254%   12.978%              12.980% D   writes
        5403112    0.3323%    2.363%               2.363% D   write misses

         108345  i for i (icache busy)
           3521  i for d (DRAM busy)
           5248  i for store (DRAM busy)
      155742912  d for d (dcache busy)
          26342  d for i (DRAM busy)
       27978912  d for store (DRAM busy)
              0  store for d (DRAM busy)
            398  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3297778423  total ticks of fpu    61.924% of total ticks
      500809316  fpOP instructions     30.794% of total
     2159129815  total dram ticks      DRAM busy 40.543%
     1664695752  float for float queue fpu CPI=  1.024
     1656616346  memory ticks          mem CPI=  1.019
     1815652760  instruction ticks     raw CPI=  1.117
      188602852  load penalties        load CPI= 0.116
     5325567710  total ticks           CPI=      3.275

      588287056  # of ticks saved  = 11.05 percent of total

       11066031  # of 2nd level dirty misses
```

```
Application: 001.gcc1.35

     1259003629 instructions (including annulled)
     1217233775 instructions (excluding annulled)
           56.6 SPECmarks for gcc

level        size     block    subblk     assoc    write miss
1st I       16 KB     32 B                2-way    write back write allocate
1st D       16 KB     16 B                2-way    write back write allocate
2nd I+D    128 KB    512 B               direct    write thru write allocate
1st Level:
               #     %instrs  %I+Drefs     %Irefs     %Drefs
        32474667     2.6679%    2.051%                        I+D misses
        17231963     1.4157%    1.088%     1.369%             I   misses
        15242704     1.2522%    0.963%                4.702%  D   misses

      1583172929   130.0632%  100.000%                        I+D references
      1259003629   103.4315%   79.524%  100.000%             I   references
       324169300    26.6316%   20.476%             100.000%  D   references

       225256896    18.5056%   14.228%                69.487%  D   reads
         7797169     0.6406%    0.493%                 2.405%  D   read misses
        98912404     8.1260%    6.248%                30.513%  D   writes
         7445535     0.6117%    0.470%                 2.297%  D   write misses

         8724629     0.7168%    0.551%                 2.691%  D   write backs
         1279094     0.1051%    0.081%                 0.395%  D   read mod writes
2nd Level:
               #     %instrs  %I+Drefs     %Irefs     %Drefs
         3017670     0.2479%    7.325%                        I+D misses
         1724012     0.1416%    4.185%    10.005%             I   misses
         1293658     0.1063%    3.140%                 5.399%  D   misses

        41194644     3.3843%  100.000%                        I+D references
        17231963     1.4157%   41.831%  100.000%             I   references
        23962681     1.9686%   58.169%             100.000%  D   references

         7797169     0.6406%   18.928%                 2.405%  D   reads
          941356     0.0773%    2.285%                 0.290%  D   read misses
         7445535     0.6117%   18.074%                 2.297%  D   writes
          350849     0.0288%    0.852%                 0.108%  D   write misses

        53782728  i for i (icache busy)
          364879  i for d (DRAM busy)
          689440  i for store (DRAM busy)
         3544711  d for d (dcache busy)
         2500225  d for i (DRAM busy)
         2551321  d for store (DRAM busy)
               0  store for d (DRAM busy)
            2915  store for i (DRAM busy)
               0  store for store (DRAM busy)

         1419650  total ticks of fpu    0.081% of total ticks
          120384  fpOP instructions     0.010% of total
       479295539  total dram ticks      DRAM busy 27.468%
         1096690  float for float queue fpu CPI=  0.001
       367451937  memory ticks          mem CPI=  0.302
      1376261004  instruction ticks     raw CPI=  1.131
          143792  load penalties        load CPI= 0.000
      1744953423  total ticks           CPI=      1.434

       103738742  # of ticks saved  =  5.95 percent of total

          980513  # of 2nd level dirty misses
```

```
Application: 008.espresso

     3102930952 instructions (including annulled)
     2930507476 instructions (excluding annulled)
           43.8 SPECmarks for espresso

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       20240025    0.6907%    0.515%                      I+D misses
         626119    0.0214%    0.016%    0.020%            I   misses
       19613906    0.6693%    0.499%              2.375%  D   misses

     3928686273  134.0616%  100.000%                      I+D references
     3102930952  105.8837%   78.981%  100.000%           I   references
      825755321   28.1779%   21.019%            100.000%  D   references

      681401797   23.2520%   17.344%             82.519%  D   reads
       17929892    0.6118%    0.456%              2.171%  D   read misses
      144353524    4.9259%    3.674%             17.481%  D   writes
        1684014    0.0575%    0.043%              0.204%  D   write misses

        7569884    0.2583%    0.193%              0.917%  D   write backs
        5885870    0.2008%    0.150%              0.713%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
         227082    0.0077%    0.817%                      I+D misses
          72196    0.0025%    0.260%   11.531%            I   misses
         154886    0.0053%    0.557%              0.570%  D   misses

       27807452    0.9489%  100.000%                      I+D references
         626119    0.0214%    2.252%  100.000%           I   references
       27181333    0.9275%   97.748%            100.000%  D   references

       17929892    0.6118%   64.479%              2.171%  D   reads
         127122    0.0043%    0.457%              0.015%  D   read misses
        1684014    0.0575%    6.056%              0.204%  D   writes
          27711    0.0009%    0.100%              0.003%  D   write misses

        2027508  i for i (icache busy)
          14116  i for d (DRAM busy)
          28771  i for store (DRAM busy)
       11146728  d for d (dcache busy)
         118634  d for i (DRAM busy)
         427890  d for store (DRAM busy)
              0  store for d (DRAM busy)
            198  store for i (DRAM busy)
              0  store for store (DRAM busy)

         108223  total ticks of fpu     0.003% of total ticks
           8755  fpOP instructions      0.000% of total
      255163555  total dram ticks       DRAM busy 7.399%
          55519  float for float queue  fpu CPI=  0.000
      183626687  memory ticks           mem CPI=  0.063
     3265169566  instruction ticks      raw CPI=  1.114
           2355  load penalties         load CPI= 0.000
     3448854127  total ticks            CPI=      1.177

       81747824  # of ticks saved  =  2.37 percent of total

         115309  # of 2nd level dirty misses
```

```
Application: spice2g6

    23810783596 instructions (including annulled)
    22775128146 instructions (excluding annulled)
           41.6 SPECmarks for spice2g6

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
     1037068529    4.5536%    3.515%                      I+D misses
         906625    0.0040%    0.004%    0.004%            I   misses
     1036161904    4.5496%    3.512%              18.181% D   misses

    29509960809  129.5710%  100.000%                      I+D references
    23810783596  104.5474%   80.688%  100.000%           I   references
     5699177213   25.0237%   19.313%             100.000% D   references

     4792611749   21.0432%   16.241%              84.094% D   reads
      982175117    4.3125%    3.329%              17.234% D   read misses
      906565464    3.9806%    3.073%              15.907% D   writes
       53986787    0.2371%    0.183%               0.948% D   write misses

      134152850    0.5891%    0.455%               2.354% D   write backs
       80166063    0.3520%    0.272%               1.407% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      237803942    1.0442%   20.304%                      I+D misses
         199490    0.0009%    0.018%   22.004%           I   misses
      237604452    1.0433%   20.287%              20.303% D   misses

     1171220711    5.1426%  100.000%                      I+D references
         906625    0.0040%    0.078%  100.000%           I   references
     1170314086    5.1386%   99.923%             100.000% D   references

      982175117    4.3125%   83.860%              83.925% D   reads
      234772464    1.0309%   20.046%              20.061% D   read misses
       53986787    0.2371%    4.610%               4.614% D   writes
        2829370    0.0125%    0.242%               0.242% D   write misses

        2424017  i for i (icache busy)
          92527  i for d (DRAM busy)
          89316  i for store (DRAM busy)
      191737771  d for d (dcache busy)
         590907  d for i (DRAM busy)
       41393972  d for store (DRAM busy)
              0  store for d (DRAM busy)
             38  store for i (DRAM busy)
              0  store for store (DRAM busy)

     7841192173  total ticks of fpu    20.420% of total ticks
      962369533  fpOP instructions     4.226% of total
    12407019526  total dram ticks      DRAM busy 32.310%
     3881753380  float for float queue fpu CPI=  0.171
     9126966066  memory ticks          mem CPI=  0.401
    24784595801  instruction ticks     raw CPI=  1.089
      607586548  load penalties        load CPI= 0.027
    38400901795  total ticks           CPI=      1.687

     1779160233  # of ticks saved  =  4.64 percent of total

       37576704  # of 2nd level dirty misses
```

```
Application: doduc

     1316441149 instructions (including annulled)
     1304567934 instructions (excluding annulled)
           33.9 SPECmarks for doduc

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       32407547    2.4842%    1.906%                      I+D misses
       14313771    1.0973%    0.842%    1.088%            I   misses
       18093776    1.3870%    1.065%               4.711% D   misses

     1700518013  130.3511%  100.000%                      I+D references
     1316441149  100.9102%   77.415%  100.000%           I   references
      384076864   29.4410%   22.586%            100.000% D   references

      298852887   22.9082%   17.575%             77.811% D   reads
        8972653    0.6878%    0.528%              2.337% D   read misses
       85223977    6.5328%    5.012%             22.190% D   writes
        9121123    0.6992%    0.537%              2.375% D   write misses

       10169438    0.7796%    0.599%              2.648% D   write backs
        1048315    0.0804%    0.062%              0.273% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2046323    0.1569%    4.807%                      I+D misses
         896441    0.0688%    2.106%    6.263%            I   misses
        1149882    0.0882%    2.701%               4.069% D   misses

       42576495    3.2637%  100.000%                      I+D references
       14313771    1.0973%   33.619%  100.000%           I   references
       28262724    2.1665%   66.382%            100.000% D   references

        8972653    0.6878%   21.075%             31.748% D   reads
         733707    0.0563%    1.724%              2.597% D   read misses
        9121123    0.6992%   21.423%             32.273% D   writes
         395084    0.0303%    0.928%              1.398% D   write misses

       37421717  i for i (icache busy)
        1296173  i for d (DRAM busy)
        2247356  i for store (DRAM busy)
       12536873  d for d (dcache busy)
       10031793  d for i (DRAM busy)
        4396462  d for store (DRAM busy)
              0  store for d (DRAM busy)
          55534  store for i (DRAM busy)
              0  store for store (DRAM busy)

     2752142075  total ticks of fpu    74.972% of total ticks
      338148549  fpOP instructions     25.921% of total
      469563079  total dram ticks      DRAM busy 12.792%
     1813775378  float for float queue fpu CPI=  1.391
      366878189  memory ticks          mem CPI=  0.282
     1408495492  instruction ticks     raw CPI=  1.080
       81790283  load penalties        load CPI= 0.063
     3670939342  total ticks           CPI=      2.814

      114858769  # of ticks saved  =  3.13 percent of total

         996036  # of 2nd level dirty misses
```

```
Application: dnasa7

     6800274227 instructions (including annulled)
     6784406530 instructions (excluding annulled)
          52.9 SPECmarks for nasa7

level       size    block   subblk    assoc    write miss
1st I      16 KB    32 B              2-way    write back write allocate
1st D      16 KB    16 B              2-way    write back write allocate
2nd I+D   128 KB   512 B             direct    write thru write allocate
1st Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
      727709708   10.7263%    7.728%                      I+D misses
        5978143    0.0882%    0.064%    0.088%            I   misses
      721731565   10.6381%    7.664%              27.577% D   misses

     9417438243  138.8101%  100.000%                      I+D references
     6800274227  100.2339%   72.210%  100.000%           I   references
     2617164016   38.5762%   27.791%             100.000% D   references

     1879496668   27.7032%   19.958%              71.815% D   reads
      666429339    9.8230%    7.077%              25.464% D   read misses
      737667348   10.8730%    7.833%              28.186% D   writes
       55302226    0.8152%    0.588%               2.114% D   write misses

      432854903    6.3802%    4.597%              16.540% D   write backs
      377552677    5.5651%    4.010%              14.427% D   read mod writes
2nd Level:
             #    %instrs  %I+Drefs    %Irefs    %Drefs
      227792060    3.3576%   19.628%                      I+D misses
           4820    0.0001%    0.001%    0.081%            I   misses
      227787240    3.3576%   19.628%              19.729% D   misses

     1160564487   17.1064%  100.000%                      I+D references
        5978143    0.0882%    0.516%  100.000%           I   references
     1154586344   17.0183%   99.485%             100.000% D   references

      666429339    9.8230%   57.423%              57.721% D   reads
      225620747    3.3256%   19.441%              19.542% D   read misses
       55302226    0.8152%    4.766%               4.790% D   writes
        2037350    0.0301%    0.176%               0.177% D   write misses

       19247418  i for i (icache busy)
          28114  i for d (DRAM busy)
          11643  i for store (DRAM busy)
      495178784  d for d (dcache busy)
         178286  d for i (DRAM busy)
      319799671  d for store (DRAM busy)
              0  store for d (DRAM busy)
            136  store for i (DRAM busy)
              0  store for store (DRAM busy)

    15079121076  total ticks of fpu     59.545% of total ticks
     2075466939  fpOP instructions      30.592% of total
    12174603603  total dram ticks       DRAM busy 48.076%
     7579511915  float for float queue  fpu CPI=  1.118
     9509419765  memory ticks           mem CPI=  1.402
     7549415923  instruction ticks      raw CPI=  1.113
      685812766  load penalties         load CPI= 0.102
    25324160369  total ticks            CPI=      3.733

     2045613180  # of ticks saved  =  8.08 percent of total

      148905641  # of 2nd level dirty misses
```

```
Application: xlisp li-input.lsp

     4962043458 instructions (including annulled)
     4661592279 instructions (excluding annulled)
           68.0 SPECmarks for li

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       43672563    0.9369%    0.671%                      I+D misses
        2581210    0.0554%    0.040%    0.053%            I   misses
       41091353    0.8815%    0.631%              2.650%  D   misses

     6512926989  139.7147%  100.000%                      I+D references
     4962043458  106.4453%   76.188%  100.000%           I   references
     1550883531   33.2694%   23.813%            100.000%  D   references

     1068396583   22.9192%   16.405%             68.890%  D   reads
       25987194    0.5575%    0.400%              1.676%  D   read misses
      482486948   10.3503%    7.409%             31.111%  D   writes
       15104159    0.3241%    0.232%              0.974%  D   write misses

       37316750    0.8006%    0.573%              2.407%  D   write backs
       22212591    0.4766%    0.342%              1.433%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
         764014    0.0164%    0.944%                      I+D misses
         419883    0.0091%    0.519%   16.267%            I   misses
         344131    0.0074%    0.425%              0.439%  D   misses

        80988485    1.7374%  100.000%                      I+D references
         2581210    0.0554%    3.188%  100.000%           I   references
        78407275    1.6820%   96.813%            100.000%  D   references

        25987194    0.5575%   32.088%             33.144%  D   reads
          156149    0.0034%    0.193%              0.200%  D   read misses
        15104159    0.3241%   18.650%             19.264%  D   writes
          187982    0.0041%    0.233%              0.240%  D   write misses

         7481885  i for i (icache busy)
            2366  i for d (DRAM busy)
           57098  i for store (DRAM busy)
        19873047  d for d (dcache busy)
          418196  d for i (DRAM busy)
         1110070  d for store (DRAM busy)
               0  store for d (DRAM busy)
               0  store for i (DRAM busy)
               0  store for store (DRAM busy)

               0  total ticks of fpu    0.000% of total ticks
               0  fpOP instructions     0.000% of total
       747868380  total dram ticks      DRAM busy 12.286%
               0  float for float queue fpu CPI=  0.000
       526101957  memory ticks          mem CPI=  0.113
      5561136309  instruction ticks     raw CPI=  1.193
               0  load penalties        load CPI= 0.000
      6087238266  total ticks           CPI=      1.306

       236888912  # of ticks saved  =  3.90 percent of total

          349179  # of 2nd level dirty misses
```

```
Application: eqntott -s -.ioplte int_pri_3.eqn

     1376907962 instructions (including annulled)
     1326073659 instructions (excluding annulled)
           47.4 SPECmarks for eqntott

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       15978750    1.2050%    1.000%                      I+D misses
           1803    0.0002%    0.001%    0.001%            I   misses
       15976947    1.2049%    1.000%              7.216%  D   misses

     1598339434  120.5318%  100.000%                      I+D references
     1376907962  103.8335%   86.147%  100.000%           I   references
      221431472   16.6983%   13.854%            100.000%  D   references

      202396631   15.2629%   12.663%             91.404%  D   reads
       15739936    1.1870%    0.985%              7.109%  D   read misses
       19034841    1.4355%    1.191%              8.597%  D   writes
         237011    0.0179%    0.015%              0.108%  D   write misses

         334338    0.0253%    0.021%              0.151%  D   write backs
          97327    0.0074%    0.007%              0.044%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2369545    0.1787%   14.526%                      I+D misses
            120    0.0001%    0.001%    6.656%            I   misses
        2369425    0.1787%   14.525%             14.527%  D   misses

       16312747    1.2302%  100.000%                      I+D references
           1803    0.0002%    0.012%  100.000%           I   references
       16310944    1.2301%   99.989%            100.000%  D   references

       15739936    1.1870%   96.489%             96.500%  D   reads
        2360576    0.1781%   14.471%             14.473%  D   read misses
         237011    0.0179%    1.453%              1.454%  D   writes
           8811    0.0007%    0.055%              0.055%  D   write misses

           4974  i for i (icache busy)
             43  i for d (DRAM busy)
             49  i for store (DRAM busy)
       24798161  d for d (dcache busy)
            332  d for i (DRAM busy)
          23091  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu     0.000% of total ticks
              0  fpOP instructions      0.000% of total
      165733298  total dram ticks       DRAM busy 10.703%
              0  float for float queue fpu CPI=  0.000
      141616298  memory ticks          mem CPI=  0.107
     1403832293  instruction ticks     raw CPI=  1.059
        3149659  load penalties        load CPI= 0.003
     1548598250  total ticks           CPI=      1.168

       30351541  # of ticks saved  =  1.96 percent of total

          45813  # of 2nd level dirty misses
```

```
Application: matrix300

     1695008934 instructions (including annulled)
     1693559315 instructions (excluding annulled)
           64.2 SPECmarks for matrix300

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      121491883    7.1738%    5.175%                      I+D misses
           1001    0.0001%    0.001%    0.001%            I   misses
      121490882    7.1738%    5.175%              18.612% D   misses

     2347769886  138.6294%  100.000%                      I+D references
     1695008934  100.0856%   72.197%  100.000%           I   references
      652760952   38.5438%   27.804%             100.000% D   references

      435650802   25.7240%   18.556%              66.740% D   reads
      120936999    7.1410%    5.152%              18.527% D   read misses
      217110150   12.8198%    9.248%              33.261% D   writes
         553883    0.0328%    0.024%               0.085% D   write misses

        5129131    0.3029%    0.219%               0.786% D   write backs
        4575248    0.2702%    0.195%               0.701% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       50318109    2.9712%   39.740%                      I+D misses
            190    0.0001%    0.001%   18.982%           I   misses
       50317919    2.9712%   39.740%              39.740% D   misses

      126620181    7.4766%  100.000%                      I+D references
           1001    0.0001%    0.001%  100.000%           I   references
      126619180    7.4766%  100.000%             100.000% D   references

      120936999    7.1410%   95.512%              95.513% D   reads
       50111438    2.9590%   39.577%              39.577% D   read misses
         553883    0.0328%    0.438%               0.438% D   writes
         206200    0.0122%    0.163%               0.163% D   write misses

           2801  i for i (icache busy)
             71  i for d (DRAM busy)
            166  i for store (DRAM busy)
      116382561  d for d (dcache busy)
            547  d for i (DRAM busy)
        2032968  d for store (DRAM busy)
              0  store for d (DRAM busy)
              8  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3024001625  total ticks of fpu     64.270% of total ticks
      432000323  fpOP instructions      25.509% of total
     1540125892  total dram ticks       DRAM busy 32.733%
     1298358757  float for float queue  fpu CPI=  0.767
     1278681468  memory ticks           mem CPI=  0.756
     1912122457  instruction ticks      raw CPI=  1.130
      216000307  load penalties         load CPI= 0.128
     4705162989  total ticks            CPI=      2.779

        9960652  # of ticks saved  =  0.22 percent of total

        3998486  # of 2nd level dirty misses
```

```
Application: fpppp

     1448153349 instructions (including annulled)
     1443743790 instructions (excluding annulled)
           37.5 SPECmarks for fpppp

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       97260892    6.7368%    4.489%                      I+D misses
       93425965    6.4711%    4.312%    6.452%            I   misses
        3834927    0.2657%    0.177%              0.534%  D   misses

     2166745950  150.0783%  100.000%                      I+D references
     1448153349  100.3055%   66.836%  100.000%           I   references
      718592601   49.7729%   33.165%            100.000%  D   references

      588879183   40.7884%   27.179%             81.949%  D   reads
        2919439    0.2023%    0.135%              0.407%  D   read misses
      129713418    8.9846%    5.987%             18.052%  D   writes
         915488    0.0635%    0.043%              0.128%  D   write misses

        1073532    0.0744%    0.050%              0.150%  D   write backs
         158044    0.0110%    0.008%              0.022%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
         972788    0.0674%    0.990%                      I+D misses
         488702    0.0339%    0.497%    0.524%            I   misses
         484086    0.0336%    0.493%              9.864%  D   misses

       98333953    6.8111%  100.000%                      I+D references
       93425965    6.4711%   95.009%  100.000%           I   references
        4907988    0.3400%    4.992%            100.000%  D   references

        2919439    0.2023%    2.969%             59.484%  D   reads
         358203    0.0249%    0.365%              7.299%  D   read misses
         915488    0.0635%    0.931%             18.654%  D   writes
         125882    0.0088%    0.129%              2.565%  D   write misses

      322894180  i for i (icache busy)
         477846  i for d (DRAM busy)
         387563  i for store (DRAM busy)
        2461773  d for d (dcache busy)
        2722345  d for i (DRAM busy)
         432150  d for store (DRAM busy)
              0  store for d (DRAM busy)
             23  store for i (DRAM busy)
              0  store for store (DRAM busy)

     4171935848  total ticks of fpu     77.127% of total ticks
      591747328  fpOP instructions      40.988% of total
     1359569696  total dram ticks       DRAM busy 25.135%
     2458039485  float for float queue  fpu CPI=  1.703
     1113665822  memory ticks           mem CPI=  0.772
     1579515968  instruction ticks      raw CPI=  1.095
      257966785  load penalties         load CPI= 0.179
     5409188060  total ticks            CPI=      3.747

      288156908  # of ticks saved  =  5.33 percent of total

         360336  # of 2nd level dirty misses
```

```
Application: tomcatv

     1626566113 instructions (including annulled)
     1626346426 instructions (excluding annulled)
           37.7 SPECmarks for tomcatv

level       size    block   subblk    assoc   write miss
1st I      16 KB    32 B              2-way   write back write allocate
1st D      16 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       83516279    5.1353%    3.635%                      I+D misses
          19062    0.0012%    0.001%    0.002%            I   misses
       83497217    5.1341%    3.634%              12.440%  D   misses

     2297780507  141.2849%  100.000%                      I+D references
     1626566113  100.0136%   70.789%  100.000%           I   references
      671214394   41.2714%   29.212%             100.000%  D   references

      482161515   29.6470%   20.984%              71.835%  D   reads
       66811736    4.1081%    2.908%               9.954%  D   read misses
      189052879   11.6244%    8.228%              28.166%  D   writes
       16685481    1.0260%    0.727%               2.486%  D   write misses

       36455368    2.2416%    1.587%               5.432%  D   write backs
       19769887    1.2157%    0.861%               2.946%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        7534657    0.4633%    6.281%                      I+D misses
           3825    0.0003%    0.004%   20.067%            I   misses
        7530832    0.4631%    6.278%               6.279%  D   misses

      119971189    7.3768%  100.000%                      I+D references
          19062    0.0012%    0.016%  100.000%           I   references
      119952127    7.3756%   99.985%             100.000%  D   references

       66811736    4.1081%   55.690%              55.699%  D   reads
        4531668    0.2787%    3.778%               3.778%  D   read misses
       16685481    1.0260%   13.908%              13.911%  D   writes
        2995861    0.1843%    2.498%               2.498%  D   write misses

          46614  i for i (icache busy)
           1160  i for d (DRAM busy)
           1267  i for store (DRAM busy)
       60699100  d for d (dcache busy)
          16122  d for i (DRAM busy)
        8140441  d for store (DRAM busy)
              0  store for d (DRAM busy)
              6  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3297778423  total ticks of fpu     70.341% of total ticks
      500809316  fpOP instructions      30.794% of total
     1139005755  total dram ticks       DRAM busy 24.295%
     1836097354  float for float queue  fpu CPI=  1.129
      847939712  memory ticks           mem CPI=  0.522
     1815652773  instruction ticks      raw CPI=  1.117
      188603050  load penalties         load CPI= 0.116
     4688292889  total ticks            CPI=      2.883

      301313158  # of ticks saved  =  6.43 percent of total

        6197797  # of 2nd level dirty misses
```

```
Application: 001.gcc1.35

     1258990785 instructions (including annulled)
     1217220271 instructions (excluding annulled)
           61.8 SPECmarks for gcc

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       19332820    1.5883%    1.221%                      I+D misses
        8242653    0.6772%    0.521%    0.655%            I   misses
       11090167    0.9111%    0.701%              3.421%  D   misses

     1583160061  130.0636%  100.000%                      I+D references
     1258990785  103.4316%   79.524%  100.000%            I   references
      324169276   26.6319%   20.476%            100.000%  D   references

      225256882   18.5058%   14.228%             69.487%  D   reads
        5051281    0.4150%    0.319%              1.558%  D   read misses
       98912394    8.1261%    6.248%             30.513%  D   writes
        6038886    0.4961%    0.381%              1.863%  D   write misses

        6965851    0.5723%    0.440%              2.149%  D   write backs
         926965    0.0762%    0.059%              0.286%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        1927711    0.1584%    7.335%                      I+D misses
        1046688    0.0860%    3.982%   12.698%            I   misses
         881023    0.0724%    3.352%              4.884%  D   misses

       26282535    2.1592%  100.000%                      I+D references
        8242653    0.6772%   31.362%  100.000%            I   references
       18039882    1.4821%   68.638%            100.000%  D   references

        5051281    0.4150%   19.219%              1.558%  D   reads
         599722    0.0493%    2.282%              0.185%  D   read misses
        6038886    0.4961%   22.977%              1.863%  D   writes
         280503    0.0230%    1.067%              0.087%  D   write misses

       26279390  i for i (icache busy)
         150361  i for d (DRAM busy)
         329374  i for store (DRAM busy)
        2320333  d for d (dcache busy)
        1013628  d for i (DRAM busy)
        2230364  d for store (DRAM busy)
              0  store for d (DRAM busy)
           2034  store for i (DRAM busy)
              0  store for store (DRAM busy)

        1419650  total ticks of fpu    0.089% of total ticks
         120384  fpOP instructions     0.010% of total
      292322908  total dram ticks      DRAM busy 18.287%
        1097308  float for float queue fpu CPI=  0.001
      221072828  memory ticks          mem CPI=  0.182
     1376248132  instruction ticks     raw CPI=  1.131
         144678  load penalties        load CPI= 0.000
     1598562946  total ticks           CPI=      1.313

       66060946  # of ticks saved  =  4.13 percent of total

         723922  # of 2nd level dirty misses
```

```
Application: 008.espresso

     3102930952 instructions (including annulled)
     2930507476 instructions (excluding annulled)
           45.0 SPECmarks for espresso

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       10540288    0.3597%    0.268%                      I+D misses
         155944    0.0053%    0.004%    0.005%            I   misses
       10384344    0.3544%    0.264%              1.258%  D   misses

     3928686273  134.0616%  100.000%                      I+D references
     3102930952  105.8837%   78.981%  100.000%           I   references
      825755321   28.1779%   21.019%            100.000%  D   references

      681401797   23.2520%   17.344%             82.519%  D   reads
        9515064    0.3247%    0.242%              1.152%  D   read misses
      144353524    4.9259%    3.674%             17.481%  D   writes
         869280    0.0297%    0.022%              0.105%  D   write misses

        4160680    0.1420%    0.106%              0.504%  D   write backs
        3291400    0.1123%    0.084%              0.399%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
         116083    0.0040%    0.790%                      I+D misses
           7085    0.0002%    0.048%    4.543%            I   misses
         108998    0.0037%    0.742%              0.750%  D   misses

       14695390    0.5015%  100.000%                      I+D references
         155944    0.0053%    1.061%  100.000%           I   references
       14539446    0.4961%   98.939%            100.000%  D   references

        9515064    0.3247%   64.749%              1.152%  D   reads
          88863    0.0030%    0.605%              0.011%  D   read misses
         869280    0.0297%    5.915%              0.105%  D   writes
          20107    0.0007%    0.137%              0.002%  D   write misses

         461836  i for i (icache busy)
           2256  i for d (DRAM busy)
           4000  i for store (DRAM busy)
        5281418  d for d (dcache busy)
          14214  d for i (DRAM busy)
         180379  d for store (DRAM busy)
              0  store for d (DRAM busy)
             39  store for i (DRAM busy)
              0  store for store (DRAM busy)

         108223  total ticks of fpu    0.003% of total ticks
           8755  fpOP instructions     0.000% of total
      133941649  total dram ticks      DRAM busy 3.986%
          55715  float for float queue fpu CPI=  0.000
       95331789  memory ticks          mem CPI=  0.033
     3265169566  instruction ticks     raw CPI=  1.114
           2355  load penalties        load CPI= 0.000
     3360559425  total ticks           CPI=      1.147

       43236030  # of ticks saved  =  1.29 percent of total

          83043  # of 2nd level dirty misses
```

```
Application: doduc

     1316441191 instructions (including annulled)
     1304567974 instructions (excluding annulled)
           35.3 SPECmarks for doduc

level       size     block    subblk     assoc    write miss
1st I      32 KB     32 B                2-way    write back write allocate
1st D      32 KB     16 B                2-way    write back write allocate
2nd I+D   128 KB    512 B               direct    write thru write allocate
1st Level:
              #     %instrs  %I+Drefs     %Irefs     %Drefs
       15581304     1.1944%    0.917%                          I+D misses
        7420765     0.5689%    0.437%     0.564%               I   misses
        8160539     0.6256%    0.480%                2.125%   D   misses

     1700518065   130.3511%  100.000%                          I+D references
     1316441191   100.9102%   77.415%   100.000%               I   references
      384076874    29.4410%   22.586%             100.000%     D   references

      298852897    22.9082%   17.575%                77.811%   D   reads
        3486056     0.2673%    0.205%                 0.908%   D   read misses
       85223977     6.5328%    5.012%                22.190%   D   writes
        4674483     0.3584%    0.275%                 1.218%   D   write misses

        5425912     0.4160%    0.320%                 1.413%   D   write backs
         751429     0.0576%    0.045%                 0.196%   D   read mod writes
2nd Level:
              #     %instrs  %I+Drefs     %Irefs     %Drefs
        1238271     0.0950%    5.895%                          I+D misses
         593753     0.0456%    2.827%     8.002%               I   misses
         644518     0.0495%    3.069%                4.745%   D   misses

       21005898     1.6102%  100.000%                          I+D references
        7420765     0.5689%   35.328%   100.000%               I   references
       13585133     1.0414%   64.673%             100.000%     D   references

        3486056     0.2673%   16.596%                25.661%   D   reads
         337804     0.0259%    1.609%                 2.487%   D   read misses
        4674483     0.3584%   22.254%                34.409%   D   writes
         306712     0.0236%    1.461%                 2.258%   D   write misses

       20400719  i for i (icache busy)
         383132  i for d (DRAM busy)
         892918  i for store (DRAM busy)
        5894224  d for d (dcache busy)
        2870226  d for i (DRAM busy)
        1618511  d for store (DRAM busy)
              0  store for d (DRAM busy)
             36  store for i (DRAM busy)
              0  store for store (DRAM busy)

     2752142075  total ticks of fpu     78.093% of total ticks
      338148549  fpOP instructions      25.921% of total
      235309303  total dram ticks       DRAM busy 6.677%
     1851398189  float for float queue  fpu CPI=  1.420
      182089080  memory ticks           mem CPI=  0.140
     1408495536  instruction ticks      raw CPI=  1.080
       82236280  load penalties         load CPI= 0.064
     3524219085  total ticks            CPI=      2.702

       54540015  # of ticks saved  =  1.55 percent of total

         620997  # of 2nd level dirty misses
```

```
Application: dnasa7

     6800274207 instructions (including annulled)
     6784406522 instructions (excluding annulled)
           55.9 SPECmarks for nasa7

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      599946973    8.8431%    6.371%                      I+D misses
           7633    0.0002%    0.001%    0.001%            I   misses
      599939340    8.8430%    6.371%              22.924% D   misses

     9417438216  138.8101%  100.000%                      I+D references
     6800274207  100.2339%   72.210%  100.000%           I   references
     2617164009   38.5762%   27.791%            100.000% D   references

     1879496669   27.7032%   19.958%              71.815% D   reads
      553085669    8.1524%    5.873%              21.134% D   read misses
      737667340   10.8730%    7.833%              28.186% D   writes
       46853671    0.6907%    0.498%               1.791% D   write misses

      384510045    5.6676%    4.083%              14.692% D   write backs
      337656374    4.9770%    3.586%              12.902% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      179008425    2.6386%   18.184%                      I+D misses
            660    0.0001%    0.001%    8.647%            I   misses
      179007765    2.6386%   18.184%              18.184% D   misses

      984456869   14.5106%  100.000%                      I+D references
           7633    0.0002%    0.001%  100.000%           I   references
      984449236   14.5105%  100.000%            100.000% D   references

      553085669    8.1524%   56.182%              56.183% D   reads
      177490200    2.6162%   18.030%              18.030% D   read misses
       46853671    0.6907%    4.760%               4.760% D   writes
        1458040    0.0215%    0.149%               0.149% D   write misses

          30174  i for i (icache busy)
            246  i for d (DRAM busy)
            334  i for store (DRAM busy)
      382721725  d for d (dcache busy)
           2182  d for i (DRAM busy)
      275156852  d for store (DRAM busy)
              0  store for d (DRAM busy)
             47  store for i (DRAM busy)
              0  store for store (DRAM busy)

    15079121076  total ticks of fpu     62.909% of total ticks
     2075466939  fpOP instructions      30.592% of total
    10177190256  total dram ticks       DRAM busy 42.459%
     7852949694  float for float queue  fpu CPI=  1.158
     7881708310  memory ticks           mem CPI=  1.162
     7549415892  instruction ticks      raw CPI=  1.113
      685931116  load penalties         load CPI= 0.102
    23970005012  total ticks            CPI=      3.534

     1763570219  # of ticks saved  =  7.36 percent of total

      128368864  # of 2nd level dirty misses
```

```
Application: xlisp li-input.lsp

     4962043458 instructions (including annulled)
     4661592279 instructions (excluding annulled)
           71.2 SPECmarks for li

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       21130402    0.4533%    0.325%                      I+D misses
         140530    0.0031%    0.003%    0.003%            I   misses
       20989872    0.4503%    0.323%              1.354%  D   misses

     6512926989  139.7147%  100.000%                      I+D references
     4962043458  106.4453%   76.188%  100.000%           I   references
     1550883531   33.2694%   23.813%            100.000%  D   references

     1068396583   22.9192%   16.405%             68.890%  D   reads
       13453668    0.2887%    0.207%              0.868%  D   read misses
      482486948   10.3503%    7.409%             31.111%  D   writes
        7536204    0.1617%    0.116%              0.486%  D   write misses

       19949249    0.4280%    0.307%              1.287%  D   write backs
       12413045    0.2663%    0.191%              0.801%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
          79042    0.0017%    0.193%                      I+D misses
          32048    0.0007%    0.079%   22.806%            I   misses
          46994    0.0011%    0.115%              0.115%  D   misses

       41077761    0.8812%  100.000%                      I+D references
         140530    0.0031%    0.343%  100.000%           I   references
       40937231    0.8782%   99.658%            100.000%  D   references

       13453668    0.2887%   32.752%             32.865%  D   reads
          21480    0.0005%    0.053%              0.053%  D   read misses
        7536204    0.1617%   18.347%             18.410%  D   writes
          25514    0.0006%    0.063%              0.063%  D   write misses

         412327  i for i (icache busy)
            753  i for d (DRAM busy)
          34652  i for store (DRAM busy)
        9314990  d for d (dcache busy)
         104898  d for i (DRAM busy)
         501208  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu     0.000% of total ticks
              0  fpOP instructions      0.000% of total
      371034611  total dram ticks       DRAM busy 6.377%
              0  float for float queue  fpu CPI=  0.000
      257748566  memory ticks           mem CPI=  0.056
     5561136309  instruction ticks      raw CPI=  1.193
              0  load penalties         load CPI= 0.000
     5818884875  total ticks            CPI=      1.249

      122606217  # of ticks saved  =  2.11 percent of total

          54265  # of 2nd level dirty misses
```

```
Application: eqntott -s -.ioplte int_pri_3.eqn

     1376907962 instructions (including annulled)
     1326073659 instructions (excluding annulled)
           47.7 SPECmarks for eqntott

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       15019316    1.1327%    0.940%                      I+D misses
           1781    0.0002%    0.001%    0.001%            I   misses
       15017535    1.1325%    0.940%               6.783% D   misses

     1598339434  120.5318%  100.000%                      I+D references
     1376907962  103.8335%   86.147%  100.000%           I   references
      221431472   16.6983%   13.854%            100.000% D   references

      202396631   15.2629%   12.663%             91.404% D   reads
       14804203    1.1164%    0.927%              6.686% D   read misses
       19034841    1.4355%    1.191%              8.597% D   writes
         213332    0.0161%    0.014%              0.097% D   write misses

         303674    0.0230%    0.019%              0.138% D   write backs
          90342    0.0069%    0.006%              0.041% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        2312739    0.1745%   15.094%                      I+D misses
            110    0.0001%    0.001%    6.177%            I   misses
        2312629    0.1744%   15.093%            15.095% D   misses

       15322573    1.1555%  100.000%                      I+D references
           1781    0.0002%    0.012%  100.000%           I   references
       15320792    1.1554%   99.989%            100.000% D   references

       14804203    1.1164%   96.617%             96.629% D   reads
        2304276    0.1738%   15.039%             15.041% D   read misses
         213332    0.0161%    1.393%              1.393% D   writes
           8330    0.0007%    0.055%              0.055% D   write misses

           4933  i for i (icache busy)
             41  i for d (DRAM busy)
             41  i for store (DRAM busy)
       23488560  d for d (dcache busy)
            288  d for i (DRAM busy)
          21137  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

              0  total ticks of fpu    0.000% of total ticks
              0  fpOP instructions     0.000% of total
      156374179  total dram ticks      DRAM busy 10.149%
              0  float for float queue fpu CPI=  0.000
      133916117  memory ticks          mem CPI=  0.101
     1403832293  instruction ticks     raw CPI=  1.059
        3149659  load penalties        load CPI= 0.003
     1540898069  total ticks           CPI=      1.163

       27812596  # of ticks saved  =  1.81 percent of total

          40748  # of 2nd level dirty misses
```

```
Application: matrix300

     1695008872 instructions (including annulled)
     1693559267 instructions (excluding annulled)
           65.8 SPECmarks for matrix300

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
      109475916    6.4643%    4.663%                      I+D misses
            901    0.0001%    0.001%    0.001%            I   misses
      109475015    6.4642%    4.663%              16.772% D   misses

     2347769807  138.6294%  100.000%                      I+D references
     1695008872  100.0856%   72.197%  100.000%           I   references
      652760935   38.5438%   27.804%             100.000% D   references

      435650793   25.7240%   18.556%              66.740% D   reads
      108923279    6.4317%    4.640%              16.687% D   read misses
      217110142   12.8198%    9.248%              33.261% D   writes
         551736    0.0326%    0.024%               0.085% D   write misses

         727624    0.0430%    0.031%               0.112% D   write backs
         175888    0.0104%    0.008%               0.027% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       44533706    2.6296%   40.412%                      I+D misses
            178    0.0001%    0.001%   19.756%           I   misses
       44533528    2.6296%   40.411%              40.412% D   misses

      110201684    6.5072%  100.000%                      I+D references
            901    0.0001%    0.001%  100.000%           I   references
      110200783    6.5071%  100.000%             100.000% D   references

      108923279    6.4317%   98.840%              98.841% D   reads
       44308551    2.6163%   40.207%              40.208% D   read misses
         551736    0.0326%    0.501%               0.501% D   writes
         224695    0.0133%    0.204%               0.204% D   write misses

           2558  i for i (icache busy)
             57  i for d (DRAM busy)
            151  i for store (DRAM busy)
      108265276  d for d (dcache busy)
            468  d for i (DRAM busy)
         484558  d for store (DRAM busy)
              0  store for d (DRAM busy)
              8  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3024001625  total ticks of fpu     65.891% of total ticks
      432000323  fpOP instructions      25.509% of total
     1347899454  total dram ticks       DRAM busy 29.370%
     1335284565  float for float queue  fpu CPI=  0.789
     1126044775  memory ticks           mem CPI=  0.665
     1912122382  instruction ticks      raw CPI=  1.130
      216000307  load penalties         load CPI= 0.128
     4589452029  total ticks            CPI=      2.710

        4918397  # of ticks saved  =  0.11 percent of total

         515755  # of 2nd level dirty misses
```

```
Application: fpppp

     1448153371 instructions (including annulled)
     1443743822 instructions (excluding annulled)
           40.6 SPECmarks for fpppp

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B            direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       43879504    3.0393%    2.026%                      I+D misses
       42420691    2.9383%    1.958%    2.930%            I   misses
        1458813    0.1011%    0.068%               0.204% D   misses

     2166745975  150.0783%  100.000%                      I+D references
     1448153371  100.3055%   66.836%  100.000%           I   references
      718592604   49.7729%   33.165%            100.000% D   references

      588879194   40.7884%   27.179%              81.949% D   reads
        1297145    0.0899%    0.060%               0.181% D   read misses
      129713410    8.9846%    5.987%              18.052% D   writes
         161668    0.0112%    0.008%               0.023% D   write misses

         214853    0.0149%    0.010%               0.030% D   write backs
          53185    0.0037%    0.003%               0.008% D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
         182541    0.0127%    0.414%                      I+D misses
          92135    0.0064%    0.209%    0.218%            I   misses
          90406    0.0063%    0.206%               5.404% D   misses

        44093717    3.0542%  100.000%                      I+D references
        42420691    2.9383%   96.206%  100.000%           I   references
         1673026    0.1159%    3.795%            100.000% D   references

         1297145    0.0899%    2.942%              77.533% D   reads
           69902    0.0049%    0.159%               4.179% D   read misses
          161668    0.0112%    0.367%               9.664% D   writes
           20503    0.0015%    0.047%               1.226% D   write misses

       150864382  i for i (icache busy)
          102942  i for d (DRAM busy)
           17398  i for store (DRAM busy)
          756568  d for d (dcache busy)
          768621  d for i (DRAM busy)
          112530  d for store (DRAM busy)
               0  store for d (DRAM busy)
              21  store for i (DRAM busy)
               0  store for store (DRAM busy)

      4171935848  total ticks of fpu    83.577% of total ticks
       591747328  fpOP instructions     40.988% of total
       610364412  total dram ticks      DRAM busy 12.228%
      2639741701  float for float queue fpu CPI=  1.829
       503443650  memory ticks          mem CPI=  0.349
      1579515981  instruction ticks     raw CPI=  1.095
       269068181  load penalties        load CPI= 0.187
      4991769513  total ticks           CPI=      3.458

       131045996  # of ticks saved  =  2.63 percent of total

           40112  # of 2nd level dirty misses
```

```
Application: tomcatv

     1626566133 instructions (including annulled)
     1626346434 instructions (excluding annulled)
           37.9 SPECmarks for tomcatv

level       size    block   subblk    assoc   write miss
1st I      32 KB    32 B              2-way   write back write allocate
1st D      32 KB    16 B              2-way   write back write allocate
2nd I+D   128 KB   512 B             direct   write thru write allocate
1st Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
       72351944    4.4488%    3.149%                      I+D misses
           3664    0.0003%    0.001%    0.001%            I   misses
       72348280    4.4486%    3.149%             10.779%  D   misses

     2297780534  141.2849%  100.000%                      I+D references
     1626566133  100.0136%   70.789%  100.000%           I   references
      671214401   41.2714%   29.212%            100.000%  D   references

      482161514   29.6470%   20.984%             71.835%  D   reads
       55894116    3.4368%    2.433%              8.328%  D   read misses
      189052887   11.6244%    8.228%             28.166%  D   writes
       16454164    1.0118%    0.717%              2.452%  D   write misses

       36029545    2.2154%    1.569%              5.368%  D   write backs
       19575381    1.2037%    0.852%              2.917%  D   read mod writes
2nd Level:
              #    %instrs  %I+Drefs    %Irefs    %Drefs
        6939399    0.4267%    6.403%                      I+D misses
            633    0.0001%    0.001%   17.277%            I   misses
        6938766    0.4267%    6.403%              6.403%  D   misses

      108380584    6.6641%  100.000%                      I+D references
           3664    0.0003%    0.004%  100.000%           I   references
      108376920    6.6639%   99.997%            100.000%  D   references

       55894116    3.4368%   51.573%             51.574%  D   reads
        4180239    0.2571%    3.857%              3.858%  D   read misses
       16454164    1.0118%   15.182%             15.183%  D   writes
        2757225    0.1696%    2.545%              2.545%  D   write misses

           8887  i for i (icache busy)
            160  i for d (DRAM busy)
            316  i for store (DRAM busy)
       59243856  d for d (dcache busy)
           1521  d for i (DRAM busy)
        8304580  d for store (DRAM busy)
              0  store for d (DRAM busy)
              0  store for i (DRAM busy)
              0  store for store (DRAM busy)

     3297778423  total ticks of fpu    70.670% of total ticks
      500809316  fpOP instructions     30.794% of total
     1029981245  total dram ticks      DRAM busy 22.072%
     1889862004  float for float queue fpu CPI=  1.163
      772387821  memory ticks          mem CPI=  0.475
     1815652804  instruction ticks     raw CPI=  1.117
      188603248  load penalties        load CPI= 0.116
     4666505877  total ticks           CPI=      2.870

      270875449  # of ticks saved  =  5.81 percent of total

        3804931  # of 2nd level dirty misses
```

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