European Coordination for Accelerator Research and Development

PUBLICATION

Development and Tests of PWM Amplifier for Driving the Piezoelectric Elements

Matiulko, J (Technical University of Lodz) *et al*

04 February 2010

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project EuCARD, grant agreement no. 227579.

This work is part of EuCARD Work Package **10: SC RF technology for higher intensity proton accelerators and higher energy electron linacs**.

The electronic version of this EuCARD Publication is available via the EuCARD web site <http://cern.ch/eucard> or on the CERN Document Server at the following URL : <http://cdsweb.cern.ch/record/1237828>

Development and Tests of PWM Amplifier for Driving the Piezoelectric Elements

Jacek Matiulko, Tomasz Poźniak, Konrad Przygoda
Department of Microelectronics and Computer Science
Technical University of Lodz
Lodz, Poland
{jmatiulko, pozniak, kprzygod}@dmcs.pl

Mariusz Grecki
Group of Maschine Strahlkontrollen
Deutsches Elektronen-Synchrotron
Hamburg, Germany
mariusz.grecki@desy.de

Abstract—**The paper describes the design and research work carried out to prepare the prototype of pulse amplifier. The work was aimed to describe main operational parameters of PWM amplifiers enabling using them to control the piezoelectric actuators used for active compensation of Lorentz force detuning of superconducting cavities.**

Index Terms—**PWM amplifier, piezoelectric elements**

I. Introduction

Superconducting (SC) resonant cavities are the integral part of accelerator modules in linear accelerators. The 9-cell 1.3 GHz cavities can be operated with high operating gradients of order of tens of MV/m. They are susceptible to small changes of dimension caused by Lorentz forces and mechanical vibrations. The piezoelectric based fast tuners, driven by power amplifiers, are dedicated for compensation purpose. Current piezo driving circuits are based on linear amplifiers. Main disadvantages of linear amplifiers are low efficiency and significantly high power loses. The PWM are becoming more and more popular among amplifiers. They are characterized by 90-95% efficiency arising from the fact that transistors in output circuit amplifier are impulse working. Therefore the power they lose is minimal. The principal of operation of such amplifier is based on PWM pulse width modulation. The clock signal (saw-form, triangular, cosine curve) is modulated by input signal. This operation creates rectangular pulse train on the output of the modulator. The frequency of this signal is that same like clock frequency. Pulse width modulation depends on the voltage of input signal. The modulated pulses are intensified by power level then demodulated by low-pass filters which have a significant slope of characteristic. The paper presents the first development and tests of PWM power amplifier circuit used for driving the piezoelectric elements. The main goal for the tests was to investigate AC and DC characteristics of such amplifiers to achieve the stable operation with capacitive load driven by specific compensation pulse shapes. The undertaken tests proved the possibilities of replacing the linear amplifiers currently used for driving the piezo electric fast frequency tuners.

II. Hardware Owerview

The work on PWM amplifiers has been started with building a system from discreet elements (Fig.1). This system was used to carry out the basic research and analysis which allowed understanding the characteristics of such amplifiers. As can be seen on the figure the size of discreet elements amplifier depends on the size of power transistor, radiator on which they are being attached and also on the size of filter that was used in output stage and also series of integrated circuits, which were used to build amplifier's blocks.

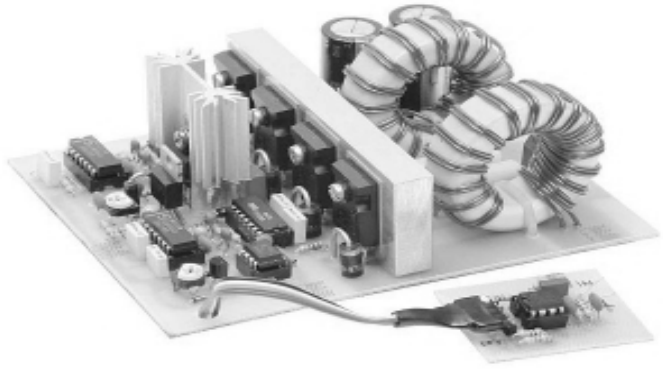

Figure 1. The PWM amplifier's system built with discreet elements, [1]

Eventually it was decided to use in further research integrated circuit of PWM amplifier make Apex, symbol SA60 [2]. Block diagram is shown in Fig. 2.

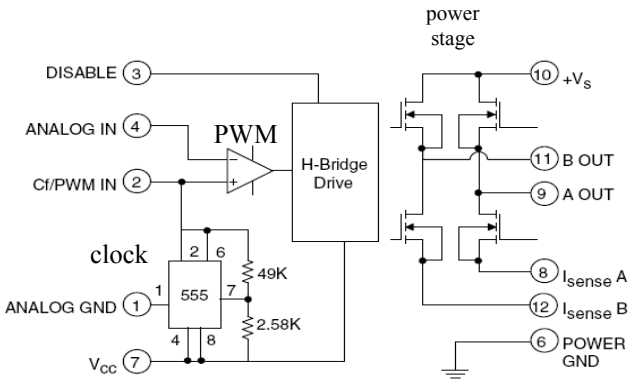

Figure 2. The block diagram of integrated circuit SA60, [2]

Main blocks of this system consists of internal clock based on 555 timer device, PWM comparator enabling configuration of the modulator, block of power transistors drivers and a power stage in full bridge configuration. The amplifier is powered by two types of voltage. Input stage is powered by Vcc voltage,

during start up and tests voltage of 15V was used. Power stage is powered by Vs voltage, which value can reach up to 80V and amplification of the amplifier depends on the value of this voltage. First tests were supposed to describe transient characteristics of SA60 amplifier, its relation between the load voltage and the voltage given at the input of the amplifier. This input is also an input of the PWM modulator which is a comparator that compares this voltage with triangle-form signal of 555 clock. Characteristic of 555 system is that triangle-form signal is between 1/3 Vcc and 2/3 Vcc. In order to compare input signal and generated clock signal it is necessary to consider that the input signal must be between desired voltage levels. The idea is presented in Fig. 3.

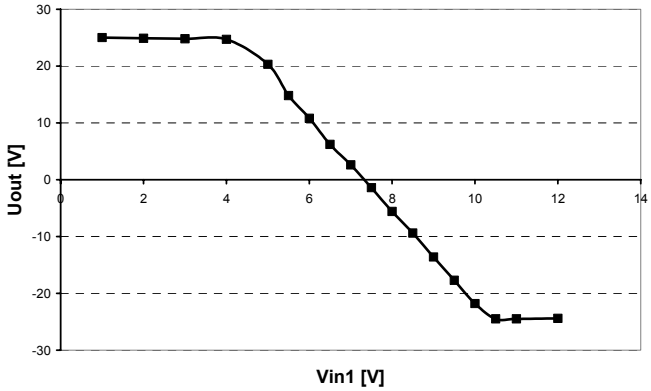

Figure 3. The characteristic of PWM amplifier Vout = f (Vin1), SA60

Therefore, it is necessary to use preamplifier circuit which is going to change amplifying signal to 1/2 of Vcc voltage. A preamplifier stage is shown in Fig. 4. The system sums input signal with constant voltage from the potentiometer. After summing, the amplified signal is inverted. The main goal of the potentiometer is to achieve null offset at the output of the amplifier.

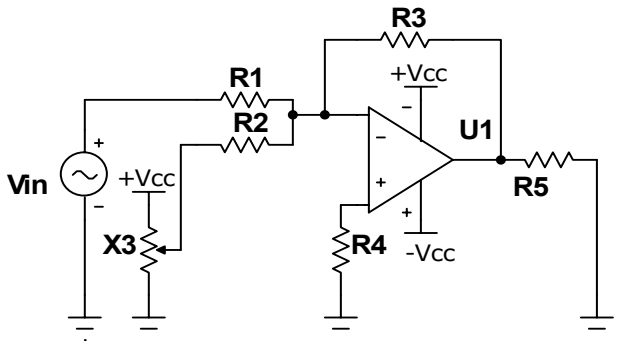

Figure 4. The electrical circuit of the preamplifier stage

Moreover, the figure 3 describes the fact that amplitude of the signal put on the power amplifier should not exceed 2.5 V because over this value the signal undergoes deformation. Fig. 5 shows how preamplifier works. The picture is showing signal amplification, inversion of phase and shift to level of 1/2 of Vcc power supply.

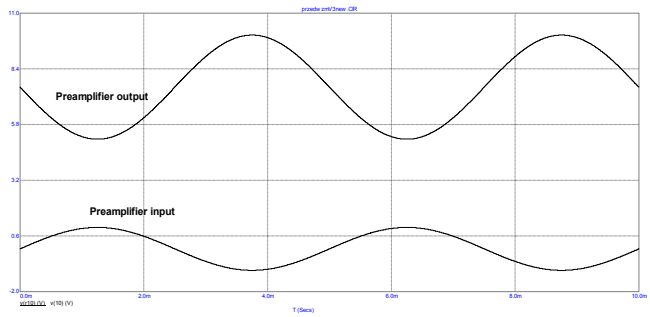

Figure 5. The work of preamplifier: down course Vin1 voltage and upper course Vout voltage upwards

A design of an output filter system was next step of our work. It is a system of low-pass filter which is responsible for demodulation of output function of power stage. The course of power stage output and filtered course achieved by using LC filter and also a spectrum of output voltage where harmonic connected with modulating frequency occurs, as well as harmonic connected with clock frequency and high harmonic frequency switching together with side bands are shown in Fig. 6. The role of the filter is to damp effectively switching frequency but the modulating frequency signal together with its harmonics should not be damped.

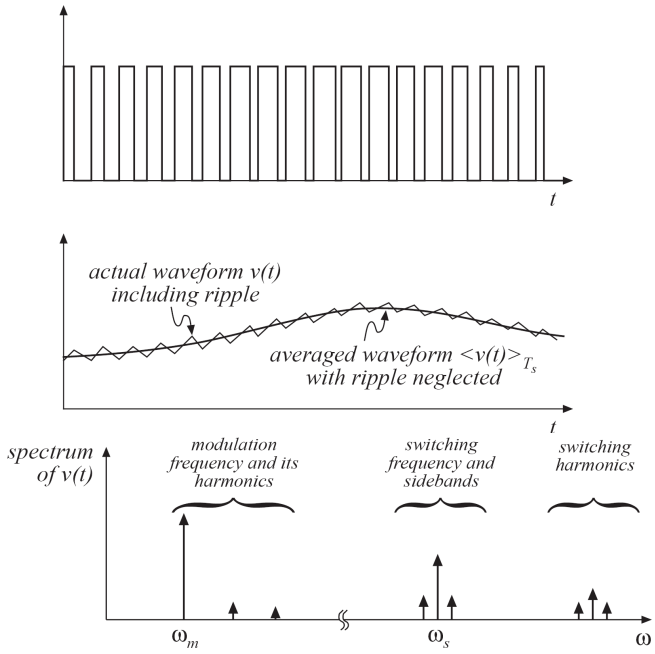

Figure 6. The output voltage spectrum with sinusoidal modulation of duty cycle [3]

The switching frequency of the system can be easily regulated using external capacitor connected between ground and - Cf/PWM in - input [2]. The desired capacitance of 98 pF computed from the following formula:

$$C_f\,(pF) = \left(\frac{1.44\times10^7}{f_{sw}}\right) - 50 \qquad (1)$$

allows setup of the switching frequency of the PWM amplifier to 100 kHz.

The dedicated tools were used to design the proper output filter stage [4]. Two main conditions should be considered by designer for proper operation of the output stage. First of all, the cut off frequency of the filter should be smaller of order of magnitude than the switching frequency of PWM amplifier. On the other hand, the high capacitance (around 5 μF) of the piezoelectric elements, typically used with fast frequency tuners, should be at least of the order of magnitude bigger than the designed filter capacitors. The output filter circuit is presented in Fig. 7.

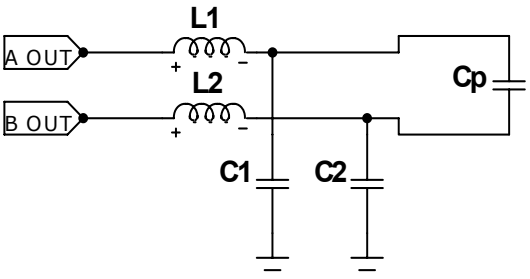

Figure 7. The Analog low-pass filter on the output of PWM amplifier

III. The Experimental Results

The prototype digital control system was used for driving PWM amplifier. It consists of Simcon DSP [5] and 32-channel DAC/PZS prototype boards connected each other using optical link. The Simcon DSP board is based on Virtex II Pro FPGA device which communicates with industrial SPARC CPU using VME bus. The 32-channel DAC/PZS board is based on Spartan II FPGA and it communicates with outside world using gigalink transceiver. The block diagram of the system is depicted in Fig. 8.

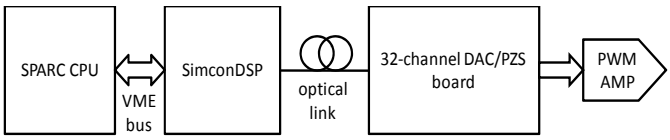

Figure 8. The block diagram of digital control system with PWM amplifier.

The Simcon DSP board is controlled using Mexsol-based VME communication library. The dedicated communication protocol was designed and developed to allow the setup of each DAC output of 32-channel DAC/PZS board using optical transmission. The simple Matlab script was written to setup the chosen DAC output with proper pulse shape, amplitude, frequency or time advance to external synchronization signal. The maximum operating sampling frequency of DAC device ported to 32-channel DAC/PZS board is 400 kHz. The sampling frequency for 32 channels corresponds to 12.5 kHz per channel. The desired output signal frequency is between 200 Hz and 300 Hz. It gives around 64 samples per single period of generated signal. The output circuits of 32-channel DAC device are buffered with 2nd pole analog low-pass active filter with cut off frequency of order of 1 kHz. The analog filters allow smoothing the DAC output signals to avoid the current spikes when driving the capacitive load of order of a few μF. The experimental setup was installed in laboratory conditions. The SimconDSP board was installed in VME crate while the 32-channel DAC/PZS board was assembled inside Eurocrate with integrated power supply unit. The SPARC CPU computer was accessible using Ethernet interface thru ssh (secure shell) communication protocol.

The amplifying system that was used during the tests is shown in Fig 9.

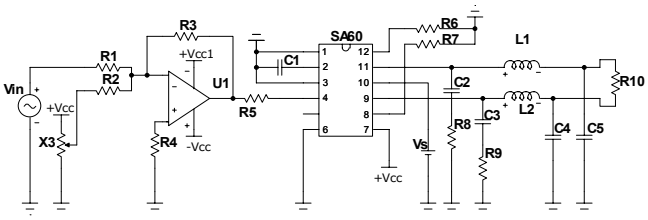

Figure 9. Complete system of PWM amplifier which was used for simulation and for measurements

During the tests the high power stage driver with signal conditioning circuit were supplied with 15 V. The power amplifier stage was supplied with 30 V. The frequency characteristics of the PWM amplifier were determined by simulation on the SA60 amplifier model supported by Apex and next proofed with real measurements with the same conditions. The results are depicted in Fig. 10.

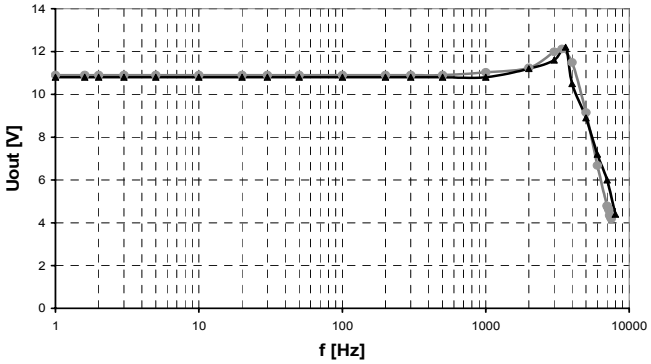

Figure 10. Frequency characteristics of PWM amplifier acquired for AC analysis, in simulation – grey curve with circles, in measurements – black curve with triangles

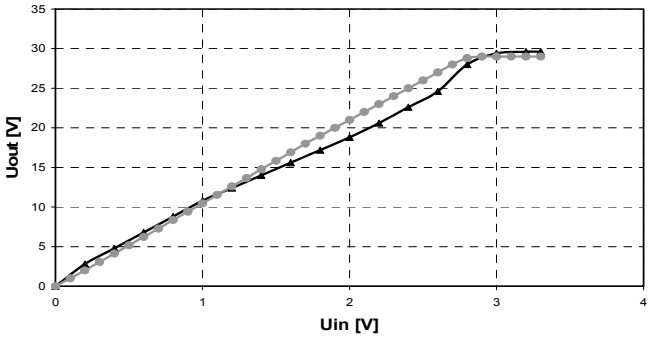

Figure 11. The characteristics PWM amplifier Vout = f (Vin) determined for middle part of frequency characteristic: in simulation – grey curve with circles, in measurements – black curve with triangles

As one can noticed, the PWM amplifier bandwidth is in range of 7 kHz. It is a satisfactory value in order to detuning compensation pulse frequency in range of 200 Hz.

The characteristics, shown in Fig. 11, compare the output signal amplitude versus the input signal amplitude for both the simulation and real measurements. The input signal frequency was set to range of order of 200 Hz. It is clearly visible, that for the higher input voltage levels, below the saturation of the both characteristics, the simulation and real measurements are slightly different. Therefore it is reasonable to add the feedback loop to the power amplifier circuit. It will improve the linearity of the DC characteristics.

The objective of the following tests was to present the influence of power stage supply voltage on the amplifier output voltage. The tests were carried out for the input signal frequency of 200 Hz, situated in the middle of bandwidth. The linear dependence of output signal amplitude versus power supply unit setup has been confirmed by simulation and during the laboratory tests (see Fig. 12).

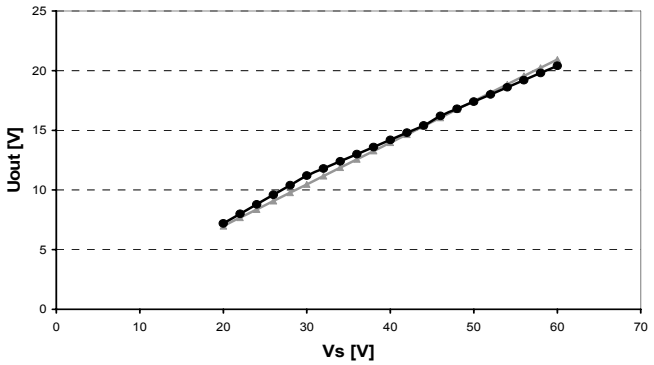

Figure 12. Characteristics of influence of the power stage supply of PWM amplifier on output voltage: in simulation – grey curve with circles, in measurements – black curve with triangles

IV. Summary

The experimental results have shown the proper operation of the PWM amplifier with prototype piezo control system (as the reference source of the compensation pulse shape) as well as the stable operation with both the resistance and capacitance loads. Moreover, the most crucial operational parameter of PWM amplifier such gain was deeply investigated. It was directly proofed that the power amplifier gain linearly depends on both the input signal amplitude as well as the setup of power supply unit. The carried out tests proofed the possibilities to use the PWM amplifier to control the piezoelectric actuators for the Lorentz force detuning compensation.

In order to reach a final conclusion thermal tests and compatibility tests should be carried out. It is also necessary to determine power losses during the work under certain circumstances in accelerator and comparing the results with the results achieved for linear amplifiers [6], [7].

Acknowledgement

The research leading to these results has received funding from the European Commission under the EuCARD FP7 Research Infrastructures grant agreement no. 227579. The author is a scholarship holder of project entitled "Innovative education ..." supported by European Social Fund.".

References

[1] "Elektronika dla wszystkich", ISSN 1425-1698, 06.2008.

[2] Apex H-Bridge Motor Driver/Amplifiers SA60 user guide, 8/2008, SA60U Rev K, Cirrus Logic inc, http://www.cirrus.com/en/pubs/proDatasheet/SA60U_K.pdf.

[3] R. W. Erickson, D. Maksimović: "Fundamentals of Power Electronics". Kluver Academic Publishers; ISBN: 0792372700; 2nd edition (February 2001).

[4] http://www.cirrus.com/en/pubs/software/PowerDesign_rev15-PWM.zip.

[5] W. Giergusiewicz, W. Jalmuzna, K. Pozniak, N. Ignashin, M. Grecki, D. Makowski, T. Jezynki, K. Perkuszewski, K. Czuba, S. Simrock, and R. Romaniuk, "Low latency control board for LLRF system – Simcon 3.1, Photonics Applications in Industry and Research IV, August 2005.

[6] K. Przygoda, M. Grecki, T. Poźniak, "Control System for Compensation of Lorentz Force Detuning for Superconducting Cavities, "14th Int. Conf. MIXDES 2008, Tech. Univ. Łódź, Poland, 2007.

[7] T. Pozniak, K. Przygoda, "8-channels Piezo Driver – Power Amplifier for Correction of SC Cavities Deformations in Linear Accelerators," Internal reports of DMCS no.7, Tech. Univ. of Lodz, Poland, 2007.