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Evaluation of an ATCA Based LLRF System at FLASH

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Abstract—**Future RF Control systems will require simultaneous data acquisition of up to 100 fast ADC channels at sampling rates of around 100 MHz and real time signal processing within a few hundred nanoseconds. At the same time the standardization of Low-Level RF systems are common objectives for all laboratories for cost reduction, performance optimization and machine reliability. Also desirable are modularity and scalability of the design as well as compatibility with accelerator instrumentation needs including the control system. All these requirements can be fulfilled with the new telecommunication standard ATCA when adopted to the domain of instrumentation. We describe the architecture and design of an ATCA based LLRF system for the European XFEL. Initial results of the demonstration of such a system at the FLASH user facility will be presented. Presented are the results of operating essential components of a prototype during the machine studies in January and March 2009.**

Index Terms—**Accelerator, Control, Feedback, Advanced TCA**

I. Conceptual Design of LLRF Based on the ATCA Standard

The LLRF system for each rf station at the European XFEL must support acquisition of more than 100 ADC channels and data processing of all these channels on a time scale of several hundred nanoseconds to set the actuator for the klystron drive signal for cavity field control. Fast piezotuners are used to compensate the Lorentz force detuning during the pulse. The architecture of the RF system for the European XFEL is shown in Figure 1.

Overall of the order of 100 applications will be implemented to ensure good field control, easy operation and high availability. The time scale for these applications range from some 100 nanoseconds over microseconds to milliseconds and seconds. The signal processing architecture with the communication links must be designed to support the required applications. The main requirements for the electronics standard are:

- Modularity,
- Scalability,

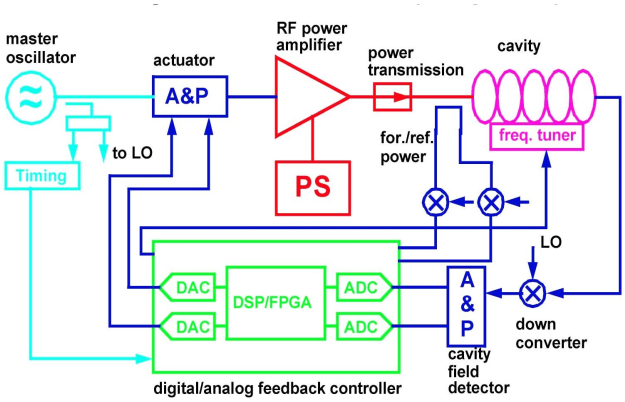

Figure 1. LLRF System Architecture

- Availability of COTS components,
- Long term support,
- Low latency, high bandwidth communication links,
- Support signal processing in a distributed heterogeneous system of processors (FPGA, DSP, CPU),
- Compatibility with accelerator control system hardware and software.

The ATCA solution is composed of several ATCA carrier boards which can hold up to 3 AMC modules with different functionality. The carrier board includes a large FPGA (Virtex V) for low latency signal processing, and a DSP (TigerSHarc) for floating point operations. The following ADC modules types will be required:

- 8 channel ADC,
- 8 channel DAC,
- Vector-modulator with 2 DACs,
- Timing receiver with clock synthesizer,
- 8 channel piezodriver,
- Signal processor card with FPGA and or DSP,
- 8 channel optical GbE.

The downconverters are be mounted as mezzanine cards on a rear transition module (RTM). This board is designed with only few active components to improve the MTBF. All signals are connected from the rear of the shelf.

II. Goals of the Demonstration

The demonstration of the ATCA based LLRF system at FLASH is performed in three phases:

1. Demonstration of the RF control for 1 accelerator section using a commercial carrier blade, a commercial AMC ADC board and a in-house build AMC Vector-modulator.
2. Demonstration of cavity field measurements of 8 cavities with the ATCA carrier board, AMC ADC card and RTM module with downconverters
3. Control of 24 cavities with the complete system consisting of several ATCA carrier boards with AMC modules and downconverters on RTM modules.

The various technical aspects that are verified during the demonstrations are listed in Table 1.

TABLE I. Aspects of Demonstration

Objective	Comment
Analog IO	Demonstrate that noise added to the signal from the input to rear transition module through Zone 3 and carrier board to the AMC module is not degraded
Communication links	Demonstrate that the scheme of low latency links, PCIe and GbE is functional.
Operation in the accelerator environment	Demonstrate that the ATCA based LLRF is functional in the noisy accelerator environment.
Rear transition module	Demonstrate the concept of rear transition modules with downconverters.
Timing distribution	Demonstrate that the timing distribution system is functional.
Timing jitter	Demonstrate that the measured timing jitter is adequate for LLRF control.
IPMI	Demonstrate the IPMI implementation.

The last phase of the demonstration with control of 24 cavities will be performed in September 2009 just before the long shutdown for the FLASH upgrade.

III. Hardware Architecture

A. Demonstration with Commercial Carrier

The set-up of the hardware for the demonstration with the commercial carrier boards is shown in Figure 2.

The hardware used in the first experiment consists of an ATCA CPU Blade Adlink 6900, 8 channel fast ADC card (TAMC900 from Tews), Vector-Modulator (VM) card with DACs (in-house design), and downconverters on the rear transition module. The block diagram of hardware is presented in figure 2. All required signals: external source for RF reference, clock and timing signals are supplied from FLASH accelerator facility. The probe signals from cavities and the Local Oscillator (LO) signal with frequency f_{LO}=1.354 GHz are connected to downconverters.

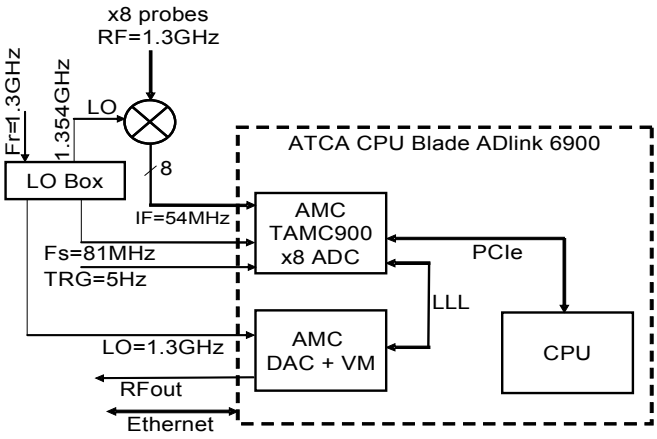

Figure 2. Hardware block diagram for the first demonstration

The output signal with an intermediate frequency of f_{IF}=54 MHz is connected to data acquisition ADC-AMC module (TAMC 900). Probe signals are sampled at a clock frequency f_S=81 MHz during the RF pulse. The sampled data are sent from ADC AMC card to the VM AMC card via low latency links (LLL) with a maximum latency of 120 ns. The LLRF controller is implemented in the Xilinx FPGA V5 on the TAMC900 module. The processed output signal is converted into analogue I and Q components and send to the input of the vector modular which drives the preamplifier of the klystron. Communication between the hardware componentes is accomplished via PCIe interface and Gigabit Ethernet.

During the demonstration at FLASH the LLRF system (shown in figure 3) has been connected to the 8 cavities in cryomodule 4. The measured rf field stability has been comparable to the stability achieved by the existing VME based systems.

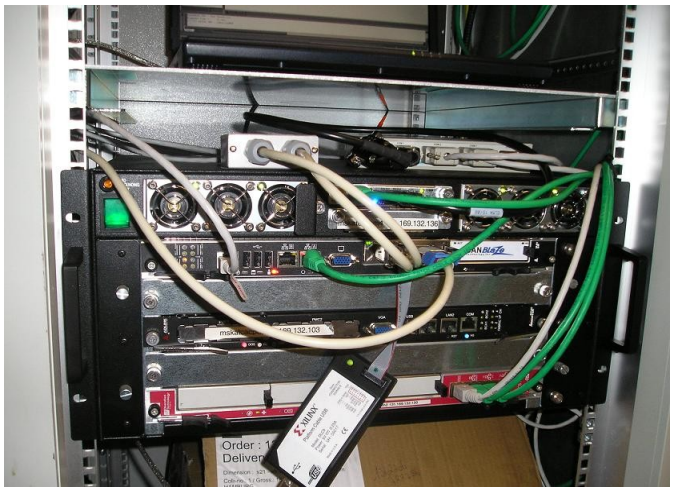

Figure 3. Set-up used for the first demonstration

B. Demonstration with LLRF CARRIER and RTM

The hardware used during the second experiment consists mainly of in-house designed subsystems. Block diagram with the hardware used during second experiment is presented in figure 4. The ATCA carrier board with three AMC bays and customised analogue signals in Zone 3 was designed at DESY. The other components used in the previous experiment are connected or mounted directly on the carrier board. The custom designed eight channel downconverter are installed on the RTM board. LO and probe signals are connected directly to the RTM. The DAQ module is installed in AMC bay on the ATCA carrier board. All required signals are provided by the carrier: 8 analogue signals from downconverters, LLL to VM and main FPGA. The VM module is installed in the second AMC bay. Low latency connection is required for transmission of real-time data from DAQ to VM. The main LLRF controller is implemented in the FPGA present on the VM module.

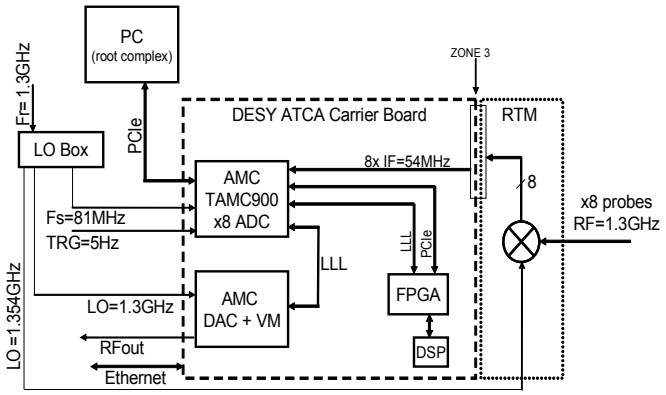

Figure 4. Hardware block diagram for the second demonstration

The carrier board contains PCIe switch that is connected to external PC computer. The computer operates as a Root Complex device required by PCIe interface. The configuration parameters of the LLRF controller can be send via Gigabit Ethernet to the PC computer and forwarded to the destination device via PCIe connection.

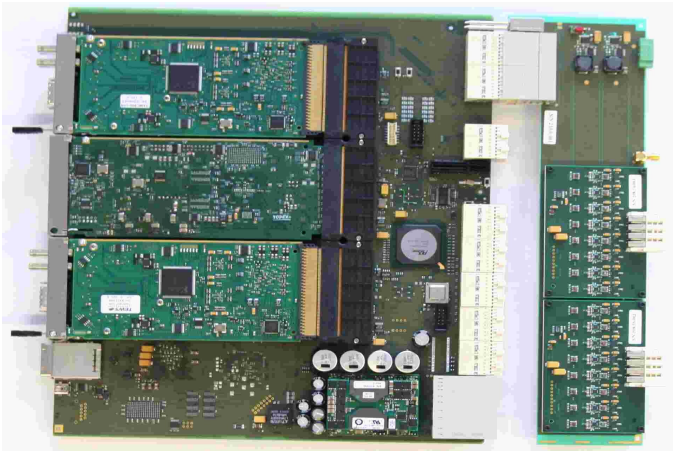

Figure 5. ATCA LLRF system consisting of ATCA carrier, AMCs and RTM module with downconverters.

IV. Software Architecture

The software architecture used in tests is presented in figure 6. The software used for both tests is similar. All presented components were used in the first test with commercial carrier. The grey components were not used in second test with LLRF carrier.

The software consists of VHDL and C/C++ components. The VHDL components were implemented in FPGA of AMC cards. The DAQ component collects data from ADCs and makes it available through Internal Interface to control software. In parallel the data from ADCs is sent to LLRF controller. The control signal is sent through LLL to DACs & VM Control component which drives the klystron. The Timing Component receives timing signals from the FLASH system and synchronizes operation of the LLRF controller as well as sends interrupts through PCIe to the DOOCS server. When the DOOCS server receives interrupts, which indicates end of the RF pulse, it reads data from DAQ system and visualizes it on DOOCS Panels.

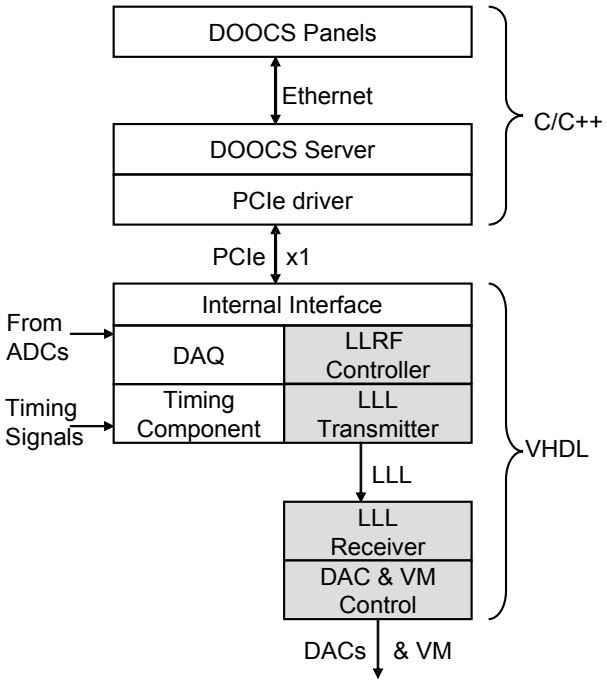

Figure 6. Architecture of software used in tests

Many of the software components such as LLRF controller, DAQ, Timing or DOOCS server were adapted from existing LLRF system running in VME system at FLASH. Some of the components specific for the platform such as PCIe driver, LLL transceiver were developed from scratch.

V. System Performance

The noise levels measured in the set-up in figure 5 without rf input signals has been 200μV (rms). The result of a measurement of a cavity probe signal is shown in figure 7. The IF frequency of 54 MHz has been sampled with a 81 MHz clock. The resulting phase jitter of about 0.25 deg. rms at the full measurement bandwidth of 200 MHz will be reduced to

about 0.02 deg. rms at the closed loop bandwidth of about 20 kHz.

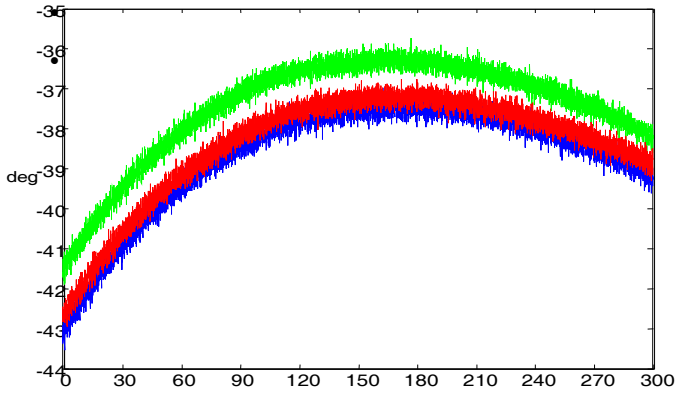

Figure 7. Phase jitter measured during 300 ms of the flat-top and shown for 3 consecutive pulse

VI. Acknowledgment

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VII. Summary

The initial experience with the new ATCA standard applied for instrumentation and control purposes has been very positive. The demonstration at FLASH has proven that the ATCA standard can be used for instrumentation purposes where many channels of small signal levels must be processed with low noise of and low latencies of a few hundred nanoseconds.

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