FPGA-based Bit-Error-Rate Tester for SEU-hardened Optical Links

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Abstract

The next generation of optical links for future High-Energy Physics experiments will require components qualified for use in radiation-hard environments. To cope with radiation induced single-event upsets, the physical layer protocol will include Forward Error Correction (FEC). Bit-Error-Rate (BER) testing is a widely used method to characterize digital transmission systems. In order to measure the BER with and without the proposed FEC, simultaneously on several devices, a multi-channel BER tester has been developed. This paper describes the architecture of the tester, its implementation in a Xilinx Virtex-5 FPGA device and discusses the experimental results.

I. Introduction

High-speed optical links offer many advantages, which make them an attractive choice for today's communication systems. In order to reach the multi-gigabit domain, these systems have to fulfill many stringent requirements (e.g. low jitter, low noise etc.), which is a very challenging task for both component manufacturers and system designers. In addition, using these links in future High-Energy Physics (HEP) experiments at CERN's upgraded Large Hadron Collider (super LHC or SLHC), requires special care to be taken during component selection, testing and verification. The selected components will be required to operate at 5 Gbit/s and beyond (up to 10 Gbit/s), with low power dissipation in high-radiation-level environment [1].

To address these challenges, a radiation hard optical link is being developed by CERN and collaborating institutes. The work is shared between two sub-projects: the GigaBit Transceiver (GBT) project [2] is responsible for the design of radiation-hard ASICs and the implementation of the custom physical layer protocol in FPGA devices [3]; while the Versatile Link (VL) project [4] covers the system architectures and the required link components. The proposed system architecture is shown in Figure 1.

II. Component testing

In order to qualify components for the next generation of radiation hard optical links, their performance must be evaluated in the laboratory and in a radiation environment. Laboratory evaluation based on eye diagram measurements has been implemented by our group [5] [1]. It proposes a method for a visual comparison of the different modules that provides a good insight into the performance of the transceivers. However, eye diagram measurements cannot easily be used for Single-Event Upset (SEU) tests where rarely occurring events must be captured.

A. Bit-error-rate testing

The bit error rate (BER) is an important characteristic of a digital communication system. During a BER test, a known bit sequence is transmitted through the system. At the output the received bits are compared with the expected ones. The BER can be calculated using the following simple equation.

$$BER = \frac{number\ of\ bit\ errors}{total\ number\ of\ bits} \quad (1)$$

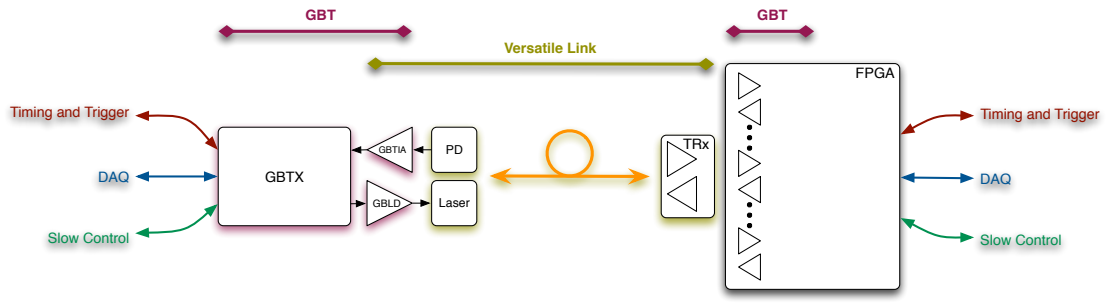

Figure 1: Radiation hard optical link architecture

Although this equation is very simple, the exact BER can be achieved only if the denominator approaches infinity. Since it is not possible to meet this requirement in real life, the BER is usually measured within the so-called confidence interval (CI). The width of the CI is defined by the confidence level (CL). Assuming that the errors will occur in the system due to random noise, we can calculate the time (T) required to reach the target BER using the following equation [6] [7],

$$T = -\frac{ln(1-CL)}{BER * R} + \frac{ln(\sum_{k=0}^{N} \frac{(n*BER)^k}{k!})}{BER * R} \quad (2)$$

where R is the line rate, n is the total number bits transmitted, and N is the number of errors that occurred during the transmission. This equation represents a trade-off between test time and confidence level. When N = 0 (i.e. error free transmission), the solution of Equation 2 is trivial. The result is shown in Figure 2.

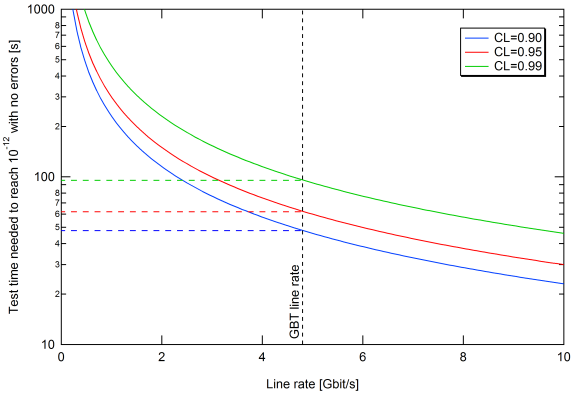

Figure 2: Time required to reach 10^{-12} BER vs. line rate

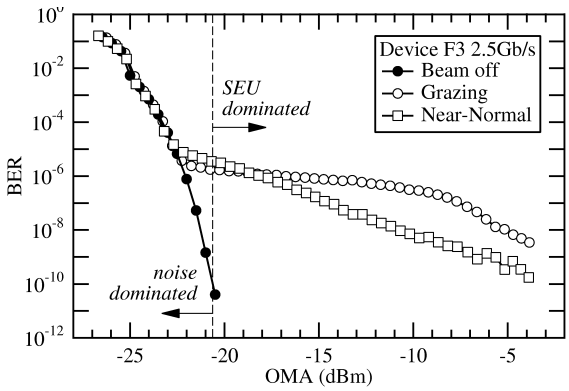

Figure 3: Illustration of the effect of SEUs on a photodiode

The test time can be reduced by stressing the system [8]. The idea of the accelerated BER testing is based on the the assumption that the errors in the system are caused by Gaussian noise. By reducing the signal level while keeping the noise constant, the signal to noise ratio (SNR) is also reduced which in turn will increase the error rate leading to a shorter test. In the presence of radiation, however, there is a region where the error rate is dominated by the SEUs (see Figure 3) [9].

B. Custom BERT

Measuring several transceiver components in a radiation environment sequentially is not practical. A multi-channel BERT can greatly improve the overall run time and simplify the procedure. In addition, by implementing the custom physical layer protocol proposed by the GBT project, the custom BERT will be able to show the performance of the applied FEC during SEU tests. Finally, the addition of an error logging facility will help us to better understand the error propagation mechanisms in the overall system.

III. Implementation

The BERT is implemented on an ML523 Transceiver Characterization Platform from Xilinx (see Figure 4) [10]. The board features a Virtex-5 FPGA (XC5VFX100T) that supports up to 16 high-speed transceivers each operating at up to 6.5 Gbit/s speed. In addition, the board contains 128 MB DDR2 memory connected to the FPGA device. The transceivers as well as the clock resources are accessible through high-quality SMA connectors. For low-speed communication with the board, there is a standard serial port (RS232) available on the board. Device programming and debugging can be done using the JTAG interface. The firmware running on the platform and the software controlling the operation are detailed in the next sections.

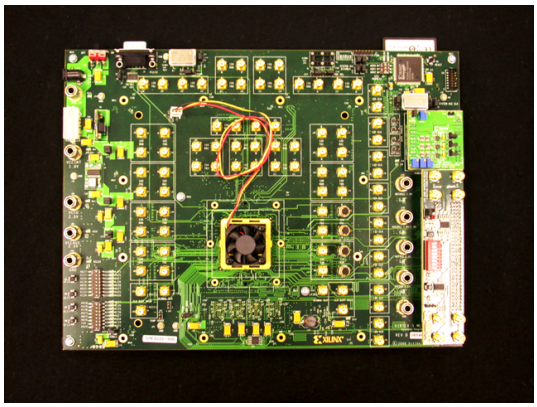

Figure 4: ML523 transceiver characterization platform from Xilinx

A. Firmware

The firmware design is based on the System-on-Chip (SoC) concept. The architecture is shown in Figure 5. The system is built around one of the two embedded processor blocks available in the Virtex-5 FPGA. The processor block contains a PowerPC 440 processor, crossbar and its interfaces. The crossbar can be connected to both master and slave peripherals in the system using Processor Local Bus (PLB) interfaces. In this design we use two PLBs to improve overall system performance.

Certain peripherals can also be provided with access to external memory via the crossbar. The communication between the control software and the processor is established using the standard UART peripheral, while the BERT specific functions are included in the BERT core. This latter is detailed in the following paragraph.

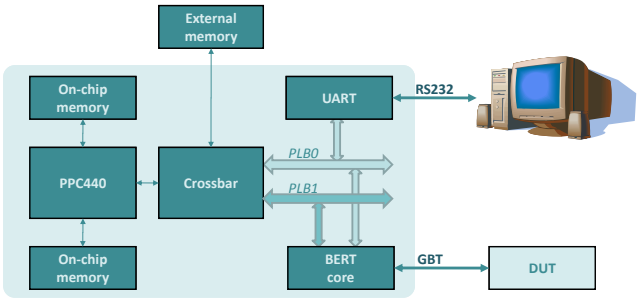

Figure 5: Firmware architecture

The BERT core is a custom peripheral with slave and master PLB interfaces and the high-speed serial terminals. The slave interface gives access to several control and status registers. The master interface is used to transfer messages to the external memory that need to be recorded during the measurement. The high-speed ports are connected to the external device under test. Inside the module, there are two separate data paths (see Figure 6). The transmitter path contains a Generator which produces simple test patterns. The data are encoded to GBT-compatible frames by the GBT Encoder. These frames include the FEC bits which allow the receiver to correct the errors that eventually occur during the transmission. For debugging purposes, errors can be injected into the transmitted data path at a programmable rate. The frames are converted to a high-speed serial stream by the multi-gigabit transceiver (MGT). Upon reception, the MGT receiver converts the serial bit stream into words which in turn are processed by the GBT Decoder. The decoder corrects the errors using the redundancy field encoded in each frame.

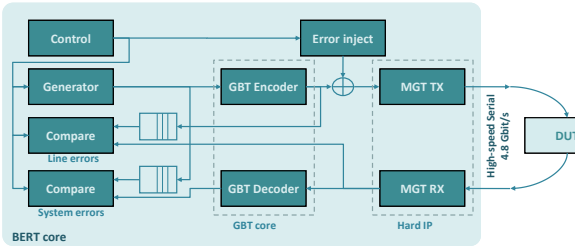

Figure 6: The firmware architecture of the BERT core

Besides the main data paths, the BERT core contains two feedback paths from the transmitter to the receiver carrying data from the pattern generator and from the GBT Encoder. To compensate for the latency that occurs during the transmission, these paths are routed through delay lines which are adjusted dynamically. In the receiver, the data from the generator and from the encoder are compared with received data available before and after the GBT decoder respectively. The differences are accumulated by counters and the values are used to calculate the line and system error rates. Using these two values, the performance of the FEC can be measured.

B. *Software*

The proper functioning of the BERT is ensured by a piece of software running on the embedded processor and a Labview script which is executed on the host computer. The firmware is responsible for the communication between the firmware and the PC, while the latter controls the measurement and provides a graphical interface (GUI) for the user.

The embedded process is a simple command interpreter. The commands, in the form of strings, are sent from the Labview script and received by the UART. The results are sent back through the serial port following the execution of the commands. The interpreter supports register read and write, as well as more complex sequences like the initialization. It can be easily extended or modified in case new functions are needed.

The Labview script is organized in two nested loops (see Figure 7). The outer loop controls the instruments (e.g. the optical attenuator) and initializes the tester. Following initialization, the script verifies the link status of the selected channels and masks inactive channels. The inner loop reads the counters of the active channels and checks whether the stop criteria are met. The values are recorded before the outer loop is restarted. The measurement is finished when a preset target BER is reached on all the active channels.

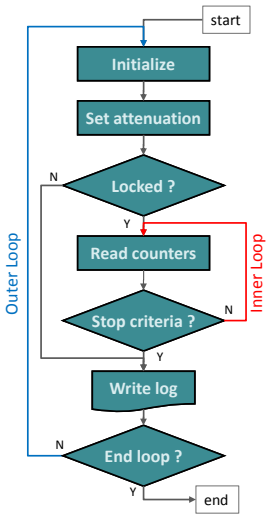

Figure 7: Measurement flow

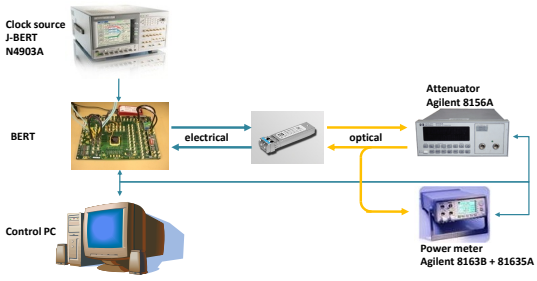

Figure 8: Lab test setup

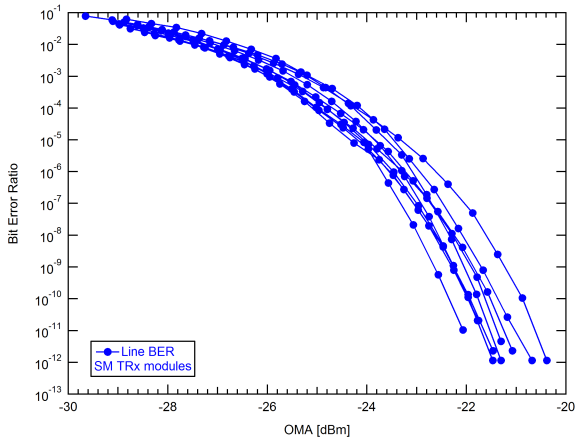

Figure 9: Test results of the single-mode modules

IV. Measurements

A. Test setup

The measurements in the lab are carried out with the setup described hereafter. The reference clock is generated by a high-precision clock source. The electrical interface of the optical transceiver is connected to one of the available high-speed channels on the BERT. The optical output from the transceiver is fed through an attenuator followed by a splitter. One splitter branch is used to close the optical loop while the other is connected to the optical power meter for monitoring purposes. The test instruments, as well as the BERT are controlled by a Labview script executed on a host PC (see Figure 8).

B. Results

Several single-mode (SM) and multi-mode (MM) transceiver modules were tested in the laboratory using the BERT. In some cases the package shielding was partially removed from the module by the manufacturer in order to reduce the mass sufficiently to allow the modules to be used inside a detector. The modules tested are summarized in Table 1.

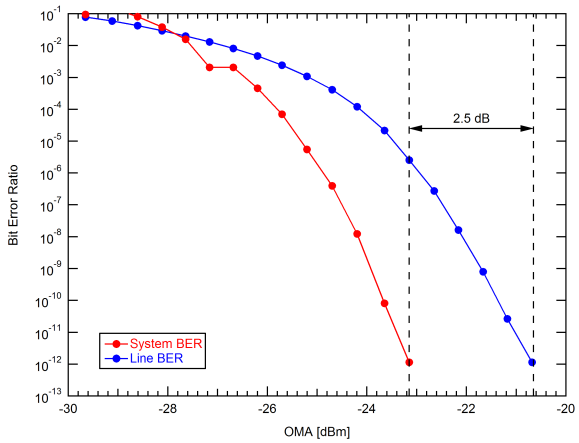

Figure 10: System and line BER

Table 1: Summary table of the tested optical transceivers

Type	Laser	Package
Single-mode	VCSEL	closed
Single-mode	DFB	closed
Single-mode	DFB	open
Multi-mode	VCSEL	closed
Multi-mode	VCSEL	open

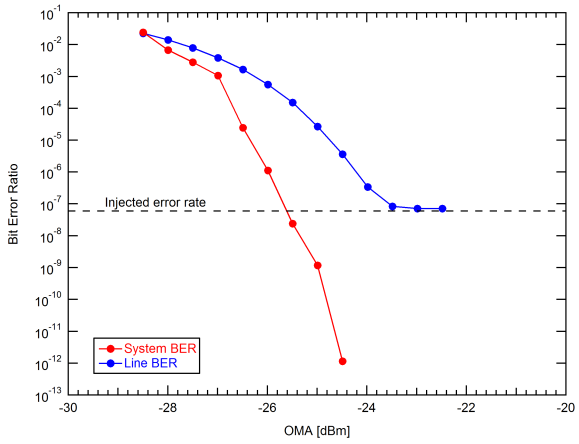

Figure 11: System and line BER, with errors injected

A scan of the line BER was carried out on all the devices, in order to compare their performance. The BER curves measured on the SM modules are shown in Figure 9. The results show no large differences between the transceivers, which is a promising preliminary information about the impact of the reduced shielding before the detailed EMI tests will take place.

The coding gain can be defined as the difference between transmit power required to send and receive error-free data without FEC and the transmit power required when the FEC is used. The coding gain is usually expressed in decibels (dB). In order to measure the coding gain of the FEC used in the GBT protocol, we can use line and system BER values recorded during the tests. The two curves in Figure 10 show an example. According to these results, the FEC implemented in the GBT protocol represents approximately 2.5 dB coding gain.

To demonstrate the error correcting capability of the physical layer protocol, one more measurement was done. During this test, the BERT was configured to inject burst of errors in the encoded data as explained earlier in Section A. The result (Figure 11) shows that the line error rate is limited as expected. However, since the burst length does not exceed the correction capability of the decoder, the errors are fixed in the receiver and the system BER will continue to fall as the optical power is increased.

V. Conclusion

Optical transceiver components will be tested to verify their compliance with the requirements of next generation radiation hard optical links in High-Energy Physics experiments. In order to quantify the effects of radiation, the components will be irradiated and the impact of the SEU on the BER will be investigated.

A multi-channel BER tester supporting the measurement of several components simultaneously has been developed. The BER tester operates at multiple data rates up to a maximum of 6.5 Gbit/s.

The described BER tester was fully verified in the laboratory. It was used to measure the performance of commercial transceivers and to study the impact of different packaging solutions on the BER. In addition, by calculating the BER both before and after the error correction, the tool allowed us to evaluate the performance of FEC implemented in the GBT protocol.

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