Low power discriminator for ATLAS pixel chip

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Abstract

The design of the front-end (FE) pixel electronics requires low power, low noise and low threshold dispersion. In this work, we propose a new architecture for the discriminator circuit. It is based on the principle of dynamic biasing and developed for the FE chip of the ATLAS pixel upgrade. This paper presents two discriminator structures where the bias current depends on the presence of a signal at the input of the discriminator. Since the activity in the FE chip is very low, the power consumption is largely reduced allowing the material reduction in the B-layer.

I. INTRODUCTION

A pixel FE chip is under development in a 130 nm CMOS technology for the B-layer replacement. The chip contains 26,880 pixels arranged in 80 columns and 336 rows. The pixel size is set to 50 µm × 250 µm.

The present pixel design uses a continuous biased discriminator where the bias current is defined to reach the required speed by minimizing the time delay. This allows assigning the hits to their corresponding bunch numbers with high probability.

In the analog pixel architecture, the discriminator power consumption can reach 20% of the total pixel power budget. Since the average counting rate for one pixel is low, it is possible to greatly reduce the power consumption of the pixel if the discriminator is biased only when a hit is present. This paper proposes an efficient way to design very low power discriminators for pixel detectors.

Two different architectures based on the dynamic biasing principle are proposed. In the first one, an input differential stage controls the bias of the main comparator stage. The input voltage signal is converted to a current signal used to bias the second stage after applying a multiplicative factor. The second architecture uses two stages. An auxiliary comparator with a lower threshold value powers up selectively the main comparator stage.

A prototype test chip has been designed as an array of 322 pixels and the different discriminator architectures are implemented in this design.

In the section II, the pixel structure is described and the main specifications are given. In the section III, the different proposed discriminator architectures are described as well as the present one. The section IV is dedicated to the experimental results and the comparison between the different architectures in terms of propagation delay as well as power consumption, noise and dispersion performances.

II. THE PIXEL STRUCTURE AND SPECIFICATIONS

The analog pixel readout chain foreseen for the FEI4 chip is shown in Figure 1. The pixel contains a fast charge preamplifier, a second stage amplifier, a discriminator and a logic bloc to transfer the hit information to the chip periphery. It is optimized for low noise, low power and fast rise time. The output signal of the second stage is coupled to a discriminator for comparison with a global threshold. Threshold tuning is allowed by dedicated local DACs. Calibration of the analog pixel electronics is performed by a local charge injection circuitry.

Table 1 : Main specifications of the FEI4 pixel

Pixel size	50 × 250	µm^2
Maximum charge	100,000	electron
Normal pixel input capacitance range	300-500	fF
Single channel ENC sigma (400fF)	300	electron
Total analog supply current @400fF	10	µA/pixel
Average hit rate	200	MHz/cm^2
Total digital supply current @ 100KHz	10	µA/pixel
Tuned threshold dispersion (max)	100	electron

The important specifications of the FEI4 are summarized in the Table 1. We can see the low value of the average hit rate meaning that each pixel receives in average one hit every 1600 bunch crossing.

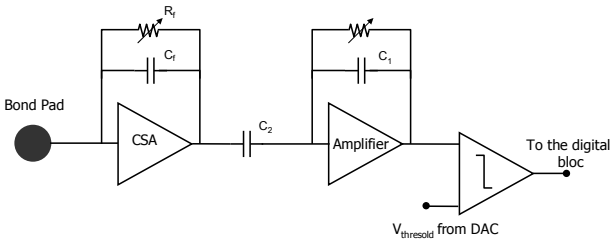

Figure 1 : Architecture of the analog pixel readout

III. THE NEW DISCRIMINATOR ARCHITECTURES

A. The current structure of the discriminator (Version 1)

In the current design shown in Figure 2, the comparator is using the two stages usual architecture.

In the Front end pixel, the comparator output is driving a low capacitance composed mainly by the input capacitance of the driven logic gate added to the interconnection capacitance. Since this load capacitance has a low value, the propagation delay is limited by the bandwidth of the amplifier and not by the slew rate. In this case the transfer function poles have to be as large as possible in order to minimise the propagation delay. Secondly, specifications in term of sensitivity for this stage require a high DC gain. Thus, we need a design with a high gain-bandwidth product.

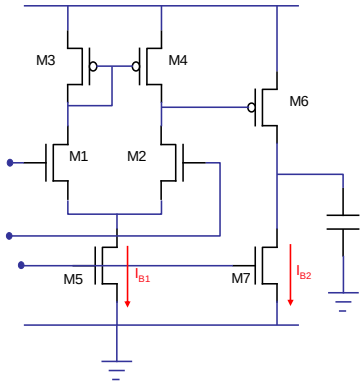

Figure 2 : The current structure of the comparator

Since the gain-bandwidth is proportional to the transconductance g_m of the input transistors, the bias current I_{B1} has to be set at a relatively high value. In order to assign the hits to their corresponding bunch numbers the time walk has to be maintained below 20 ns. A bias current around 4 µA to 5 µA is needed to meet this specification. This represents nearly 20% of the total pixel consumption.

B. Discriminator with dynamic biasing based on current mirror (Version 2)

In this structure, the input differential stage composed by M11-M12 controls the bias current of the main comparator stage composed by M1-M2. The idea is to use the current flowing into an arm of the first differential pair and apply it with a multiplication factor K to the second stage as an additional bias current.

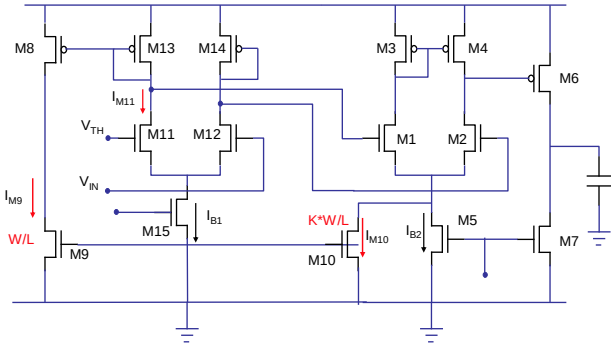

Figure 3 : Dynamic biasing based on current mirror

If the input signal is far from the threshold V_{TH}, The totality of the bias current I_{B1} flows in the arm composed by the transistor M12. No current is flowing in the transistor M11 and there is no additional current to the bias current I_{B2} for the main comparator supply (Figure 4).

When the level of the input signal approaches the threshold, one fraction of I_{B1} is flowing in the transistor M11 and it is copied with applying a factor K. This current is added to the bias current I_{B2}. Everything happens as if the input voltage signal is converted to a current signal used to bias the main comparator stage with applying a multiplicative factor.

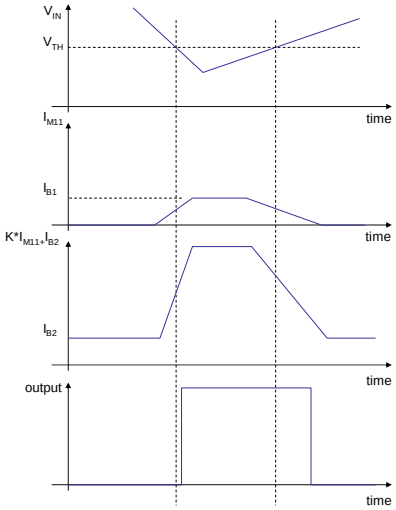

Figure 4 Waveforms timing in the comparator

In order to reach similar performances as in the version 1, the DC bias currents I_{B1} and I_{B2} are set to 350 nA each, setting the total consumption for this discriminator to the very low level of 700 nA.

The critical point for this structure is how to speed up the current mirror response. This is required to enable high current switching in the second stage when the input signal is crossing the threshold voltage.

The only way to reduce the propagation time in the current mirror is to reduce the gate capacitance of the transistors M13, M8 and M9. This can be done easily by reducing the size of

those transistors. However this has an impact on the threshold dispersion of the pixel.

C. *Discriminator with dynamic biasing using variable resistance (Version 3)*

This architecture also uses two stages. The auxiliary comparator composed by M11-M12 corresponding to the first stage powers up selectively the main comparator stage. This is achieved by applying a lower threshold value V_{THL} to the auxiliary stage while the true value of threshold V_{THT} is applied to the main stage composed by M1-M2.

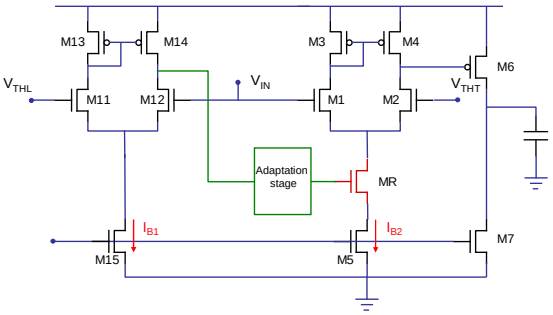

Figure 5 : Dynamic biasing using variable resistance

When the amplitude of the input signal V_{IN} coming from the amplifier is low and doesn't reach the threshold V_{THL}, the totality of the current I_{B1} flows through M12 and M14. The output of this stage is low and the transistor MR is off. There is no current in the main stage. When the input signal V_{IN} reaches V_{THL}, the output of the first stage increases and drives the transistor MR from region of high resistance to a region with low resistance allowing the current I_{B2} to flow in the differential pair of the second stage.

Since the current at the second stage can be potentially set to a high value, the speed of this comparator is well improved.

In order to optimize the switching performances of this design the threshold V_{THL} has to be near the true threshold. Thus, the first stage requires a low propagation delay but the required DC current is lower than that required by a two stage comparator. In order to keep the same performances as in the version 1, simulations show that the auxiliary stage bias current I_{B1} has to be set around 1 µA.

In this prototype, the threshold V_{THL} is generated with different sizes for M11 and M12. In the final design, V_{THL} can be generated by the same DAC generating the threshold V_{THT}.

IV. Experimental Results

A. *Test chip design*

A prototype test chip has been designed as an array of 322 pixels. Different discriminator architectures were implemented in this design. All discriminators are associated to the similar front end. The chip was designed and implemented in a 130 nm CMOS technology. It is based on the previous prototype chip designed by the pixel collaboration [1].

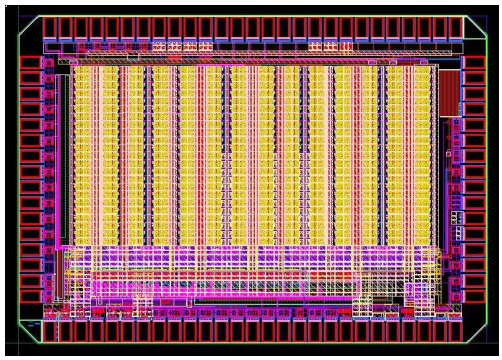

Figure 6 : Test chip layout

Figure 6 shows the layout of the chip. The die size is 3 mm × 2 mm. It is arranged in 14 columns and 23 rows of pixels with a size of 50 µm × 250 µm each. The 3 versions were implemented in this chip. For each version of the discriminator, 3 to 4 columns of pixels were dedicated.

B. *Time delay*

In order to measure the resolution in time of the front end chain, we measured the propagation delay from the edge of the injected charge to the discriminator output. The level of charge is adjusted by an external calibrated voltage pulse flowing to the local charge injection circuit of each pixel. It is obvious that the total delay is not attributed only to the discriminator stage but depends also on the behaviour of the preamplifier and the amplifier stages when the injected charge varies. In this prototype, each comparator version is associated to exactly the same pixel design. Thus, the propagation delay differences between the studied structures are attributed only to the discriminator.

Figure 7 shows the propagation delay of the whole analog pixel chain when the threshold is set to 4500 e- and the charge over the threshold varies from 0 to 8000 e-.

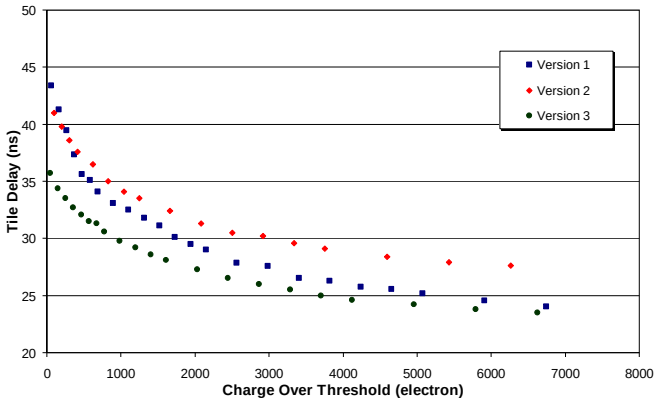

Figure 7 : Time Delay for a charge threshold = 4500 e

The version 3 shows better switching performances than the other versions and the time walk is estimated to 12 ns. In this design, during the switching phase, the current varies from 0 to 30 µA. This high current level allows reaching better time delay but can be a source of crosstalk which can be propagated to the sensitive areas through the power supply lines. Measurements will be done in order to check if there is any influence on the neighbouring charge amplifiers during this switching phase.

In the version 2, the switching current is limited to 8 µA. The time walk doesn't exceed 15 ns with a DC bias current of only 700 nA.

C. Noise and threshold dispersion

Measurements show that the structure of the comparator doesn't have any influence on the noise. The typical value of the measured Input Noise Equivalent Charge is around 90 e- when there is no input capacitance and no leakage current.

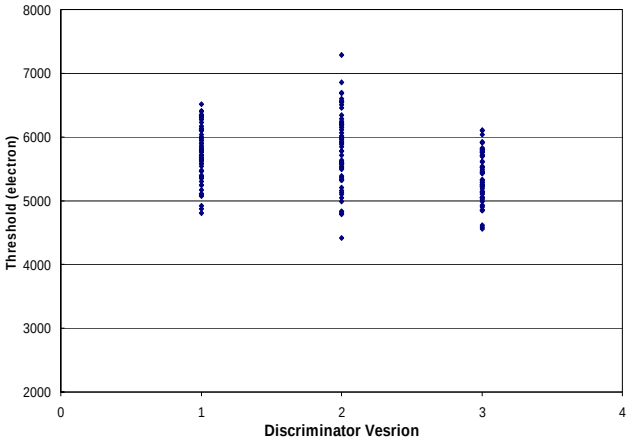

Figure 8 Threshold dispersion

However, the version 2 of the discriminator introduces more dispersion in the pixel as shown in Figure 8. In fact the area of he input transistor is set as low as possible in order to increase the speed of the current mirror. However, this threshold dispersion can be contained and all the pixels can be tuned after threshold adjustment.

Table 2 Performances comparison

	Current consumption	Current spike*	Time walk
Version 1 (Reference design)	5.3 µA	5.1 µA	20 ns
Version 2 (Current-Mirror)	0.7 µA	8 µA	15 ns
Version 3 (Variable resistance)	1.2 µA	30 µA	12 ns

* Estimated from simulations

Performances are summarized in Table 2. The version 2 of the discriminator based on the current mirror technique is a good design candidate to be implemented in the final design.

V. CONCLUSION

A very low power consumption discriminator suitable for pixel chips where the average hit rate is low has been described in this paper. The architecture is based on the dynamic biasing principle.

A prototype chip containing almost 300 pixels has been designed in order to test the different proposed architectures. We showed that the new structures can reach a faster time response, very low power consumption than the present design while at the same time ensuring no degradation of the other important performances of the front end pixel.

Using such a design in the FEI4 chip can save 20% of the total power consumption compared to the present design.

VI. ACKNOWLEDGEMENTS

We would like to thank R. Fei for the test and K. Arnaud for the test board design.

VII. REFERENCES

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