Wafer Screening of ABCN-25 readout ASIC

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Abstract

The ABCN-25 chip was fabricated in 2008 in the IBM 0.25 micron CMOS process. One wafer was immediately diced to make chips available for evaluation with test PCBs and hybrids, programmes which are reported separately to this conference. A second wafer was later diced untested to ensure continuity of supply. Early indications based on the first diced wafer suggested a percentage yield of more than 95%, however the community decided to screen the remaining wafers such that faulty die could be excluded from the module construction programme. This paper documents the test hardware, software and procedures used to perform the screening. An overview of results is also given.

I. Introduction

The ATLAS Binary Chip-Next (ABCN-25) readout ASIC is designed to support the R&D programme towards silicon detector modules for the ATLAS Tracker Upgrade. The chip implements pipelined binary readout for 128 silicon short strip detector channels.

Fabricated in 0.25 micron IBM CMOS technology during late 2008, the first wafer was diced immediately. Initial tests of wire-bonded chips revealed the design to be fully functional with a very high yield [1], [2]. However, as each detector module will use 40 chips, it remains important that any faulty chips are identified on-wafer such that they can be excluded from the build process.

II. Hardware and Software

The wafers were probed at the Rutherford Appleton Laboratory using a Cascade Microtech model S300 probe station. The machine, which has a 12" chuck, can easily accommodate the 8" ABCN-25 wafers. The custom cantilever epoxy probe card shown in figure 1, made by Rucker and Kolls, Milpitas, CA, has 122 probes. In place of the usual edge connector, 0.1" header pins are used to provide connectivity, a deliberate choice to give added clearance above the wafer surface during probing. The card has also been shortened to minimize the trace lengths and all LVDS pairs are terminated with 100 ohm resistors at the probe ring. Figure 2 shows the probe card aligned with an ABCN-25 die, probes in contact.

Commercial off the shelf (COTS) hardware from National Instruments (NI) is used to read out each ASIC. Fast test vectors are generated by the NI PCI-6562 400 Mb/s Digital Waveform Generator/Analyzer, which has 16 LVDS channels, and slow test vectors are generated by the NI PCI-6509 Low-Cost 96-channel TTL Digital I/O card.

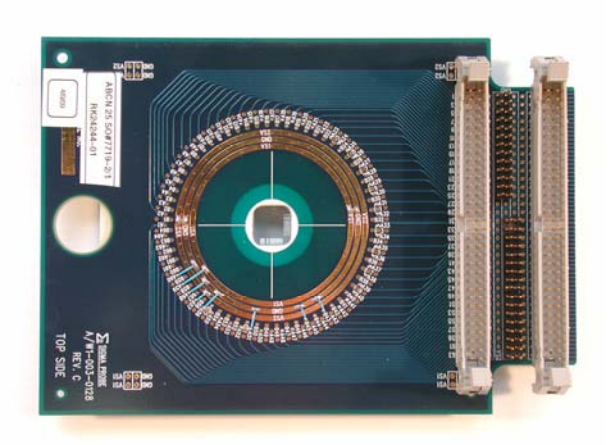

Figure 1: ABCN-25 Probe Card

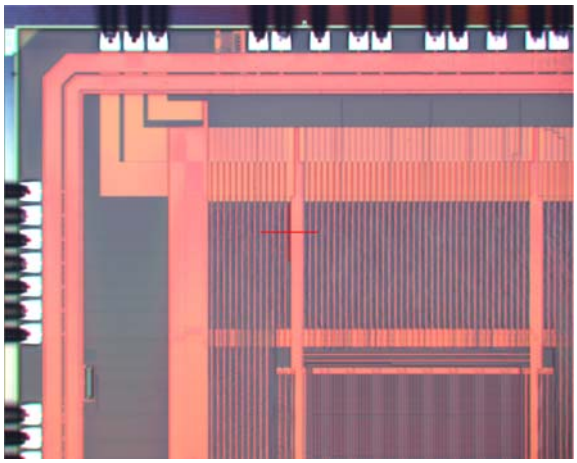

Figure 2: Probes in contact with ABCN-25 die

The single bonded chip PCB shown in figure 3 (left) was used extensively during firmware development and system commissioning. The custom driver board shown in figure 3 (right) performs level translation and implements a number of operational modes in which different combinations of ABCN-25 IO lines are mapped to fast and slow IO channels. The multiplexing is achieved by means of a Xilinx Spartan 3E FPGA with firmware written in VHDL. Analogue switches are provided to enable the chip's built-in custom power blocks to be exercised and to route the chip's analogue monitor pads to an Agilent 34401A digital multimeter. A second digital multimeter is used to monitor the analogue voltage generated by the ABCN-25's internal regulator, and a Thurlby-Thandar

programmable power supply is used to provide constant voltage or constant current sources to the device under test.

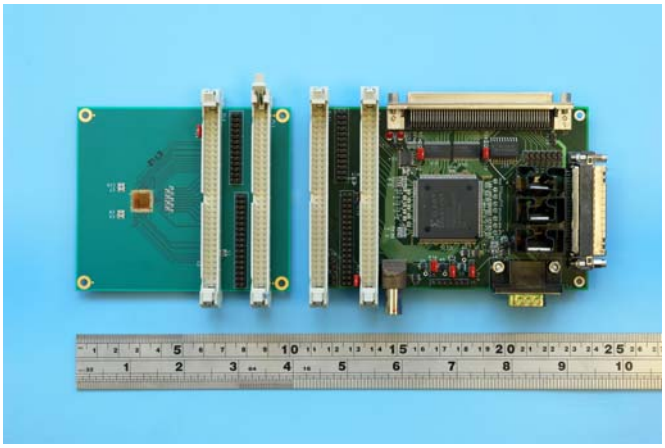

Figure 3: ABCN-25 Bonded Chip and Custom Driver PCBs

The software used to control the system is a development of the SCTDAQ package used during early tests of the ABCN-25 chip. Written in C++, using ROOT for data analysis, this package originally used custom VME readout modules but has been successfully adapted to use COTS hardware from NI.

III. Test Methodology

The test sequence comprises three parts: digital/power tests, DAC characterisation and analogue characterisation.

A. Digital/Power tests

Four test vector blocks engineered to test the complete digital functionality of the chip were supplied by the ASIC design team as Value Change Dump (.vcd) files. Each block was converted into a pair of Hierarchical Waveform Storage (.hws) files using National Instruments' Digital Waveform Editor utility as shown in figure 4: one file representing the waveform input to the chip, shown at the top, and a second file describing the expected output, shown at the bottom.

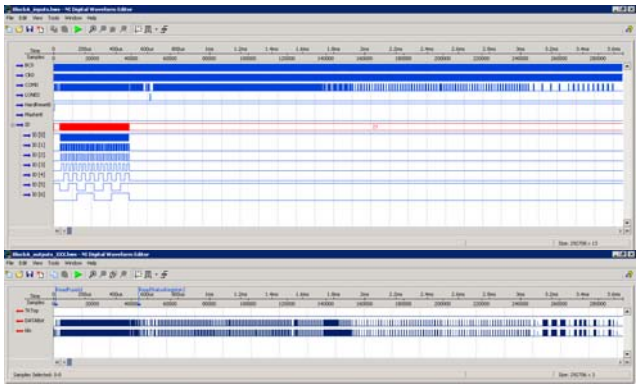

Figure 4: Vector Block A: Inputs and Expected outputs

Bearing in mind that ABCN-25 has built-in shunt regulator functionality to be used as part of a serially powered system [3], each test is performed under different powering conditions such that the basic functionality of each of the shunt blocks may be demonstrated. For a chip to be considered good, it must return no errors for any vector block. In addition, for tests executed with serial powering shunts active, the full source current must be drawn at the expected voltage.

B. DAC characterisation

The ABCN-25 design includes an on-chip multiplexer which enables each of a number of internal analogue signals to be routed to an external voltmeter. These nodes include the output of each of the chip's Digital to Analogue Converters (DACs). During the wafer probing, a digital voltmeter is used to record 8 points to characterise each DAC, and a single measurement for each static node available through the multiplexer. Additional measurements are made of the bandgap reference made available at the vbgtest pin and of the analogue voltage derived from the digital supply by the chip's built in regulator. Chips having DACs with anomalous single point measurements or DAC step sizes are considered as rejects.

C. Analogue characterisation

Each ABCN-25 readout channel has a 5-bit threshold DAC, used to compensate for offset variations across the chip. In addition the step size of these DACs , known as the trim range, may be set to one of 8 possible levels. All wafer probing data is recorded using trim range 4. With all trim DACs set to zero, threshold scans are made for charges of 1.5fC, 2.0fC and 2.5fC, injected using the ABCN-25's internal calibration circuitry. A fourth threshold scan is then made for an injected charge of 2.0fC, but this time the trim DACs are set to 31. This data may be analysed to calculate the gain, offset and noise of each channel and to estimate the number of channels which may be trimmed using the selected trim range. For a chip to be considered as good, it must have no more than one bad (dead, stuck or untrimmable) channel.

IV. Operational Experience

The probe card had been stored for some months before probing began. In order to make low resistance contacts it was necessary to clean the needles by scrubbing them a few times against an alumina ceramic sheet. Once reproducible results had been demonstrated using individual cut die, probing of the four remaining wafers began.

The software was originally written to retest die which failed any of the digital vector blocks, having first dropped and raised the chuck to relocate the probe needles, and to abort the test sequence if the die still failed. As we gained experience with the system, this was modified such that the sequence would only abort if three consecutive die failed both automated test attempts. In this manner a typical wafer of 456 complete ASICs would run to completion overnight, leaving a small number of die to be investigated in the morning. In all cases, the DAC and analogue characterisations were skipped for die which failed the digital tests. The test sequence takes approximately 2 minutes per die, dominated by the DAC characterisation (60%), but for such a small number of wafers this was not considered to be an issue.

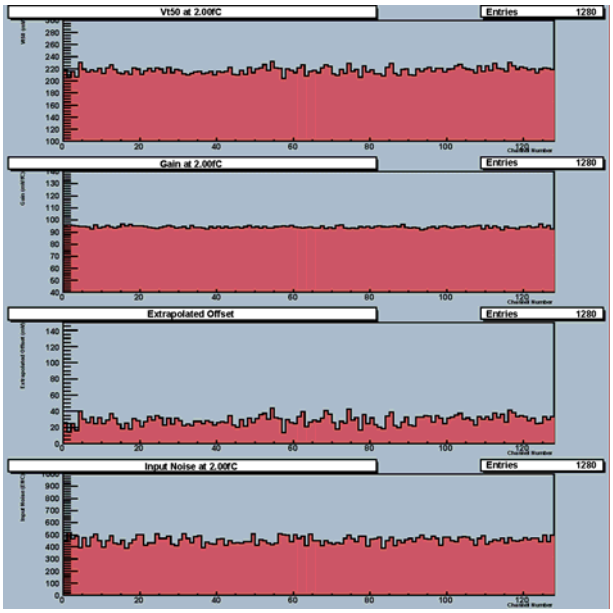

Figure 5: Typical Three Point Gain Result.

A typical three point gain result for a probed chip is shown in figure 5. The top graph illustrates good threshold uniformity across the chip, the second plot shows the gain to be 95mV/fC and the bottom one shows the calculated input noise to be of order 450 ENC. The gain is approximately 10% lower than that of a bonded chip and the calculated noise is hence around 10% higher. The results are still of sufficient quality to screen wafers for anomalous die.

Figure 6 shows gain for all die of a single wafer and figure 7 shows the step size of one of ABCN-25's threshold DACs, also as a function of die number. Both plots show data from wafer A6GBD0X and feature the same two obvious outliers, having zero gain in one plot and a step size of half the normal value in the other. Hence the gain could not be determined due to a failure of the threshold DAC. Indeed all major DAC anomalies, both threshold and bias parameters, were found on die which would in any case have been rejected due to their limited analogue functionality. For production screening this could be an important observation, as the threshold scans complete much more quickly than the DAC characterisations.

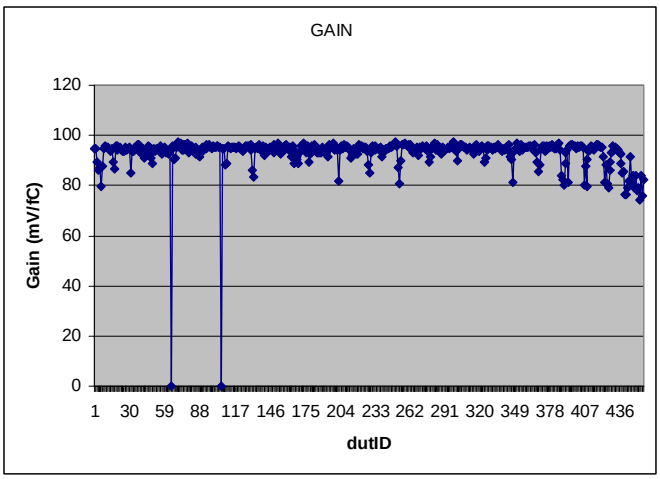

Figure 6: Gain vs Die Number, wafer A6GBD0X

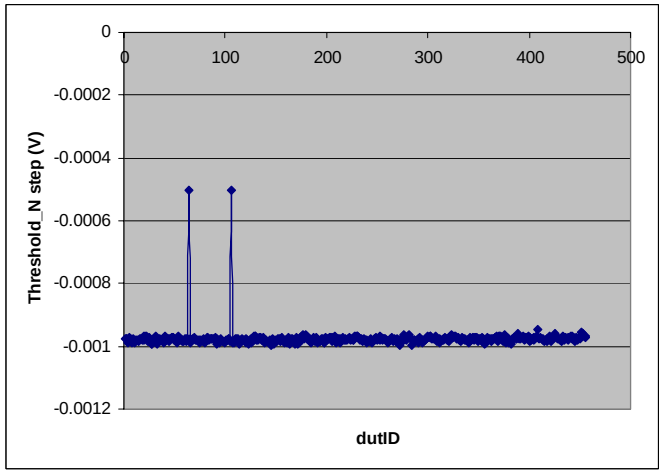

Figure 7: Threshold DAC step size, wafer A6GBD0X

V. Results

Result maps of the four probed wafers are shown overleaf in figures 8 to 11, summarised below in table 1. The pattern displayed by wafer AJGBMX is perhaps the most interesting, having a cluster of digital failures near the wafer notch (top) and a cluster of analogue failures near the wafer serial number (bottom). The orientation of the die is such that the digital portion is nearest the wafer edge near the notch, and the analogue portion is nearest the wafer edge near the serial number. So this pattern is consistent with a processing defect affecting circuit blocks at large radii.

Wafer	Digital Rejects	Analogue Rejects	Good Die	Total Yield
A6GBD0X	10	4	442	96.9%
AJGBDMX	18	12	426	93.4%
ARGBCYX	15	1	440	96.5%
AWGBDAX	12	15	429	94.1%
Overall	55	32	1737	**95.2%**

Table 1: Yield Summary

VI. Conclusion

Four ABCN-25 wafers were successfully probed. The overall yield before dicing was found to be 95.2%. Commercial hardware from National Instruments provided an appropriate platform to readout each chip.

VII. Outlook

It is planned to order further ABCN-25 wafers in the near future, to provide continued support to the ATLAS strip tracker upgrade programme. These wafers will also be screened at RAL. Looking further ahead, most elements of the present system may also be used to test future generations of ATLAS strip tracker readout chips made in 0.13 micron technology.

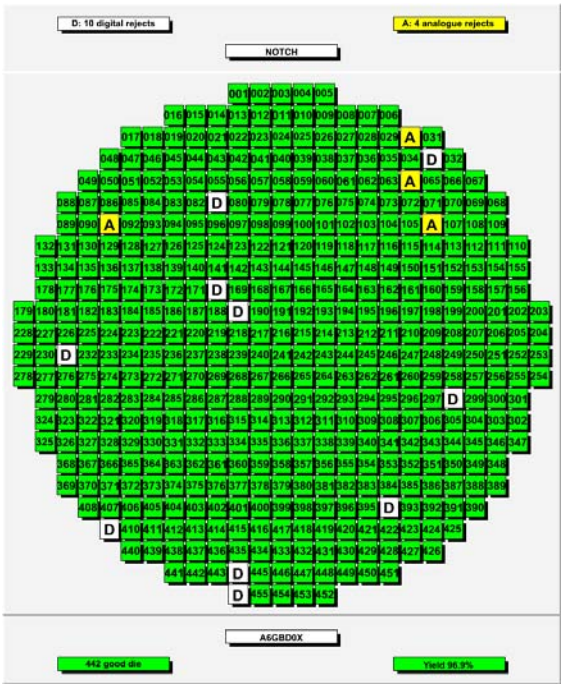

Figure 8: Wafer A6GBD0X test map

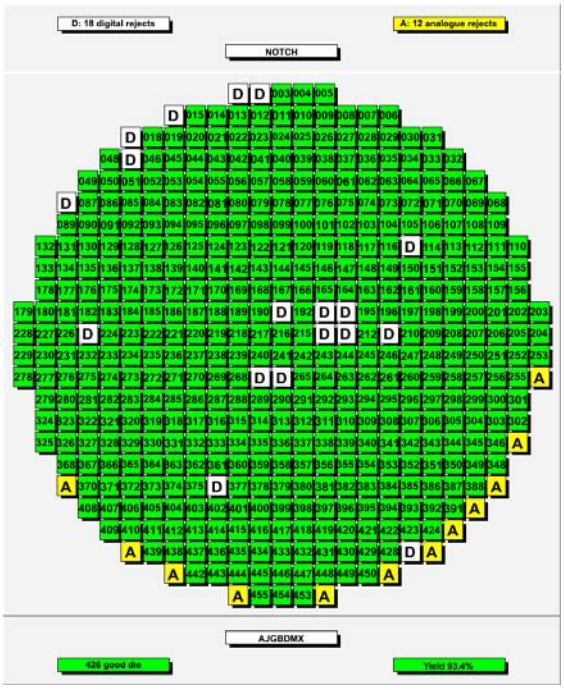

Figure 9: Wafer AJGBDMX test map

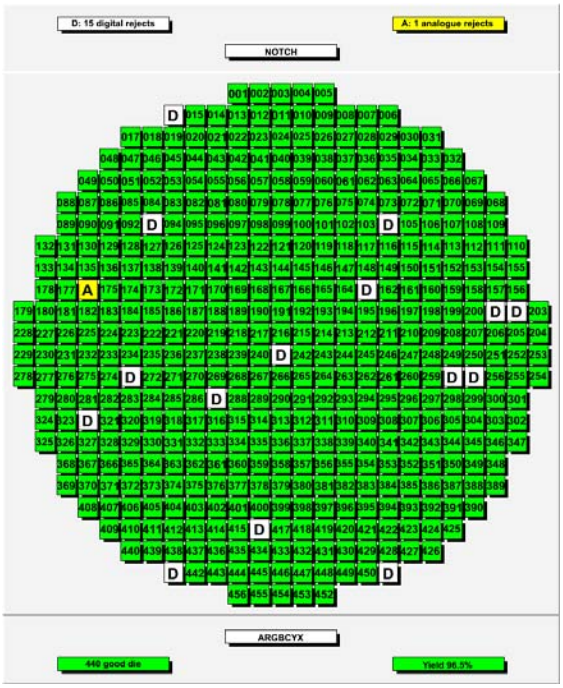

Figure 10: Wafer ARGBCYX test map

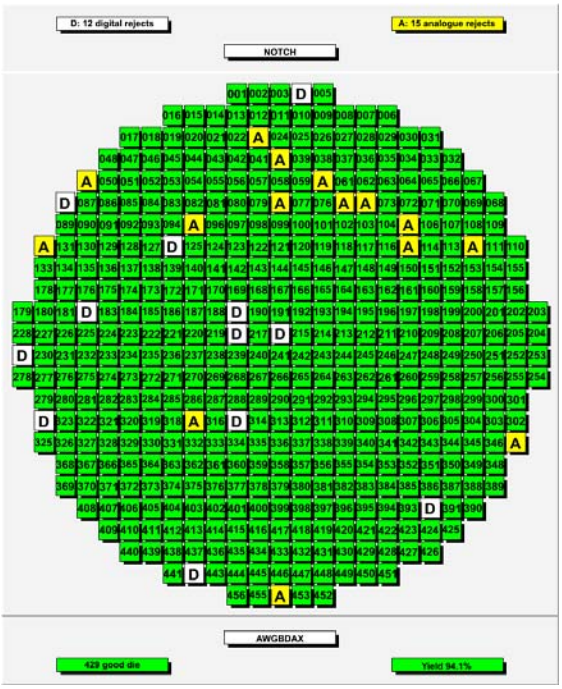

Figure 11: Wafer AWGBDAX test map

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VIII. REFERENCES

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[2] "Prototype flex hybrid and module designs for the ATLAS Inner Detector Upgrade utilising the ABCN-25 readout chip and Hammamatsu large area Silicon sensors", A. Greenall, proceedings of this conference.

[3] "Performance and Comparison of Custon Serial Powering Regulators and Architectures for SLHC Silicon Trackers", T. Tic et al, proceedings of this conference.

IX. ACKNOWLEDGEMENTS

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