Hardware studies for the upgrade of the ATLAS Central Trigger Processor

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Abstract

The ATLAS Central Trigger Processor (CTP) is the final stage of the first level trigger system which reduces the collision rate of 40 MHz to a level-1 event rate of 75 kHz. The CTP makes the Level-1 trigger decision based on multiplicity values of various transverse-momentum thresholds as well as energy information received from the calorimeter and muon trigger sub-systems using programmable selection criteria.

In order to improve the rejection rate for the first phase of the luminosity upgrade of the LHC to $3 \cdot 10^{34}$ cm^{-2} s^{-1} planned for 2015, one of the options being studied consists of adding a topological trigger processor, using Region-Of-Interest information from the calorimeter and potentially also the muon trigger. This will require an upgrade of the CTP in order to accommodate the additional trigger inputs. The current CTP system consists of a 9U VME64x crate with 11 custom designed modules where the functionality is largely implemented in FPGAs. The constraint for the upgrade study presented here was to reuse the existing hardware as much as possible. This is achieved by operating the backplane at twice the design frequency and required developing new FPGA firmware for several of the CTP modules.

We present the design of the newly developed firmware for the input, monitoring and core modules of the CTP as well as results from initial tests of the upgraded system.

I. Introduction

The ATLAS experiment at the Large Hadron Collider (LHC) at CERN uses a three-level trigger system. The Level-1 trigger [1] is a synchronous system operating at the bunch crossing (BC) frequency of 40.08 MHz of the LHC. It uses information on clusters and global energy in the calorimeters and on tracks found in the dedicated muon trigger detectors to reduce the event rate to 75 kHz. Figure 1 shows an overview of the ATLAS Level-1 trigger system. The Muon to Central Trigger Processor Interface (MUCTPI) [2] combines the data from the trigger sectors of the two dedicated muon trigger detectors in the barrel and end-cap regions and calculates muon candidate multiplicity values. The Central Trigger Processor (CTP) [3] uses the muon multiplicities from the MUCTPI together with electron/photon, tau/hadron and jet multiplicities, as well as event energy information received from the calorimeter trigger processors to make the final Level-1 trigger decision (L1A) based on a list of programmable selection criteria (trigger menu). Trigger inputs from various other sources, such as luminosity detectors, minimum bias scintillators and beam pick-ups can also be taken into account. The CTP receives timing signals from the LHC and distributes them, along with the L1A, through the trigger, timing and control (TTC) network to the sub-detector back-end and front-end electronics. It also sends Region-of-Interest (RoI) data to the Level-2 trigger system (LVL2) and trigger summary information to the data acquisition system (DAQ). In addition the CTP provides integrated and bunch-by-bunch scaler data for monitoring of the trigger, detector and beam conditions. For a full overview see [4].

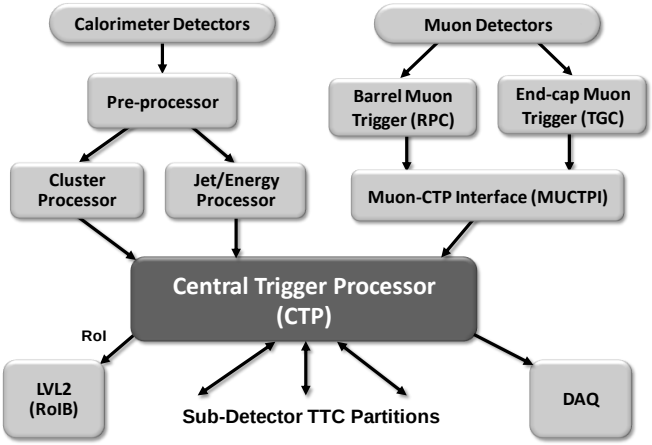

Figure 1: Overview of the ATLAS Level-1 Trigger

II. CTP Architecture

The CTP system consists of a single 9U VME64x chassis with three dedicated backplanes and 11 custom designed modules of 6 different types. Figure 2 below shows the architecture of the CTP.

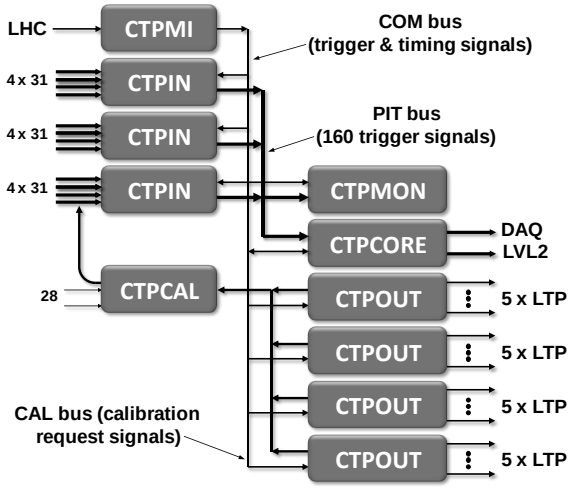

Figure 2: Architecture of the CTP

The machine interface module (CTPMI) receives the timing signals from the LHC and distributes them over the COM backplane to the other modules. Each of the 3 input modules (CTPIN) receives up to 124 trigger input signals, synchronizes and aligns them and sends selected trigger signals over the PIT bus backplane to the monitoring and core modules. The monitoring module (CTPMON) performs bunch-by-bunch monitoring of the PIT bus signals. The core module (CTPCORE) generates the Level-1 accept signal (L1A) according to programmable selection criteria and sends trigger summary information to the Level-2 trigger and DAQ systems through optical link interfaces (S-LINK). The four output modules (CTPOUT) distribute the trigger and timing signals through up to 20 cables to the sub-detector TTC partitions and receive calibration requests from the sub-detectors. The calibration module (CTPCAL) time-multiplexes the calibration request signals from the CAL backplane and performs level conversion of front-panel NIM input trigger signals.

Figure 5 shows a picture of the CTP crate installed in the ATLAS underground counting room. From left to right are the CTPMI, three CTPINs, the CTPMON, the CTPCORE, four CTPOUTs, and the CTPCAL modules. Currently 9 of the 12 CTPIN input connectors are used, however not all of the signals on the trigger cables are allocated. Another two complete CTP systems are available in the laboratory as spares as well as for firmware and software development.

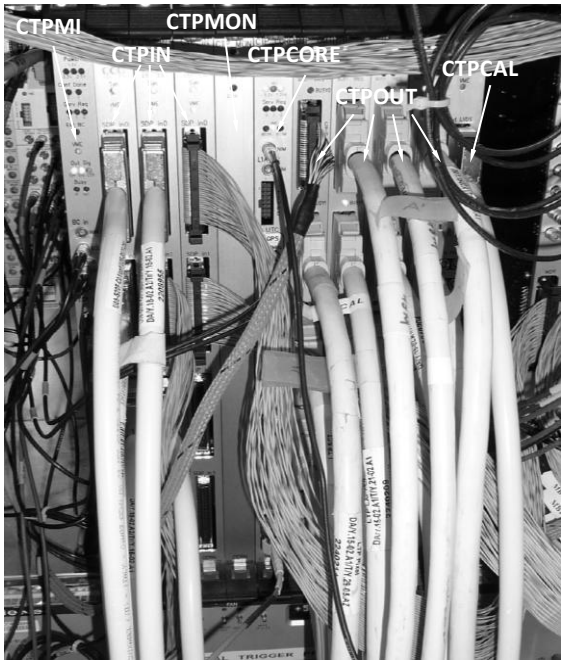

Figure 3: The CTP installed in the ATLAS counting room

III. CTP Trigger Path

Figure 4 below shows the trigger path of the CTP. Each of the three CTPIN modules receives, synchronises and aligns the trigger signals from four input cables with 31 signals each. Reconfigurable switch matrices then select which of the aligned trigger inputs to drive onto the 160 PIT bus lines.

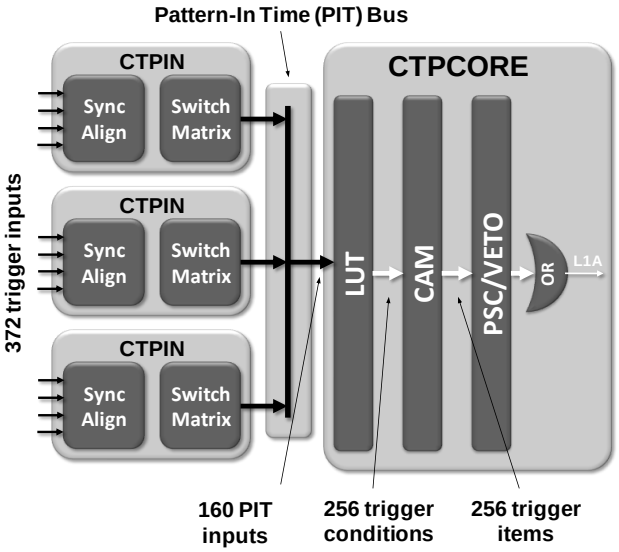

Figure 4: CTP trigger path

The CTPCORE module receives the 160 selected trigger signals from the PIT bus. Look-up tables (LUT) at the input generate 256 trigger conditions from the 160 PIT signals and additional internal triggers. A ternary contents-addressable memory (CAM) then calculates 256 trigger items as logical combinations of these trigger conditions. Those trigger items are pre-scaled and gated with a programmable mask, preventive dead-time and the busy signal from the experiment's readout. The logical OR of all items then forms the final L1A signal which is fanned out to the sub-detectors. Dead-time is generated in the CTPCORE to prevent the front-end buffers in the experiment from overflowing. The memory files for the LUT and CAM of the CTPORE and the configuration files for the switch matrices of the CTPINs are automatically generated from the Level-1 trigger menu by software and are loaded when the CTP is configured. The design of the CTP has been optimized for low latency; it takes only 4 bunch crossings (BC) from the trigger signals being received at the CTPIN to the L1A signal being sent from the CTPOUT modules to the experiments TTC partitions.

There are a total of up to 372 trigger inputs for the full CTP system however the number of trigger signals usable in the L1A formation is limited to 160 by the number of PIT bus lines. In order to accommodate additional trigger input signals we have therefore doubled the PIT bus transfer rate by operating it at 80 MHz using double-data rate (DDR) signalling. This results in an effective PIT bus width of 320 bits. This modification also required significant changes to the FPGA firmware of the CTPIN, CTPMON and CTPCORE modules.

The PIT backplane is a short multi-drop bus which connects the switch matrix outputs of the 3 CTPIN modules to the inputs of the CTPCORE and CTPMON modules. It spans 5 VME slots and uses SSTL2 signal levels with a combined series/parallel termination scheme. Although the PIT bus was originally only designed to operate at 40 MHz, the DDR operation has been shown to work reliably.

IV. The CTP Input Module

The CTPIN has four identical channels, which receive 31 LVDS trigger input signals at 40 MHz each. Figure 5 below shows a picture of the CTPIN module.

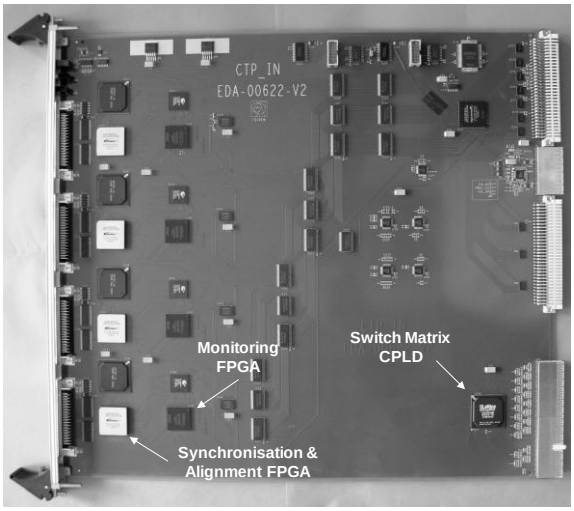

Figure 5: Picture of the CTPIN module

After level conversion, an FPGA synchronizes the trigger inputs to the internal clock, aligns them with respect to each other using programmable length pipelines and optionally checks their parity. The synchronized trigger inputs can be stored in a diagnostic memory for debugging and monitoring purposes. The memory can also be used to inject data into the channel. This functionality is implemented in an Altera Stratix FPGA (EP1S20).

A second FPGA (Altera Cyclone EP1C20) is used to monitor the trigger inputs with counters that integrate over all bunches in a LHC turn. Each channel also features a TDC (CERN HPTDC ASIC) to measure the phase of every trigger input signal. Finally a configurable switching matrix implemented in a CPLD (Lattice ispXPLD) is used to select and route the aligned trigger inputs to the PIT bus. The internal clock of the CTPIN module can be adjusted using a programmable delay line (CERN DELAY25 ASIC). Figure 6 below shows a simplified block diagram of the module.

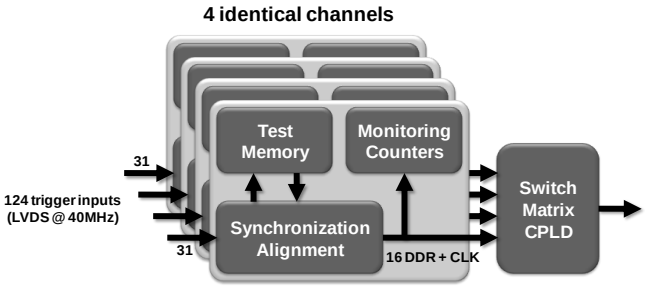

Figure 6: CTPIN architecture

The modified firmware of the synchronization and alignment FPGA features DDR output registers which drive the 31 trigger signals onto 16 DDR lines. Since the monitoring FPGA connects to the same lines, DDR input registers were added there. In addition a 90° phase shifted clock is sent to the monitoring FPGA in order to correctly latch the DDR signals. The 16 DDR output signals of each channel are sent to the switch matrix CPLD which selects and routes up to 64 signals from the CTPIN onto the 160 PIT bus lines.

V. The CTP Core Module

The LUT/CAM FPGA (Xilinx XC2VP50) receives the PIT bus signals on the CTPCORE and implements the LUT and CAM for the trigger formation. DDR input registers were added at the input, the clock for latching the PIT signals can be adjusted using a programmable delay line (CERN DELAY25 ASIC). Figure 7 below shows a picture of the CTPCORE module.

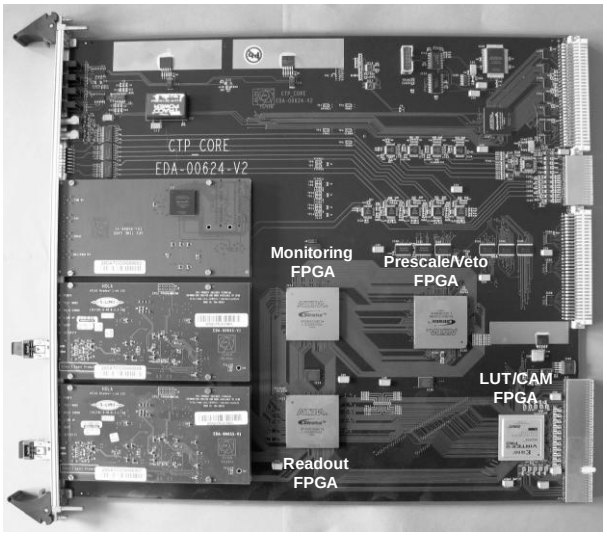

Figure 7: Picture of the CTPCORE module

Since there are now twice as many trigger inputs, the structure of the LUT and CAM also needed to be adapted. Figure 8 below shows a block diagram of the new LUT/CAM FPGA.

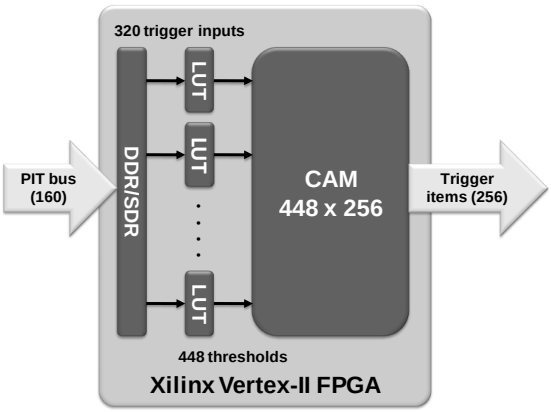

Figure 8: CTPCORE LUT/CAM FPGA

An array of 28 12-input LUTs generates 448 trigger conditions from the 320 trigger inputs. This includes the internally generated triggers, namely two random triggers, two pre-scaled clocks and eight triggers for programmable groups of bunch crossings. The width of the ternary CAM was also increased from 256 originally to 448 to accommodate all the

trigger conditions. However the number of trigger items was kept at 256, because of limited FPGA resources and PCB connections.

The trigger inputs on the CTPCORE are also sent to another FPGA which implements monitoring counters and writes them into FIFO buffers for DAQ/LVL2 readout and monitoring. This functionality is implemented in an Altera Stratix FPGA (EP1S60). Since there are not enough PCB connections for the 320 trigger signals, DDR signaling was also used to transmit these signals to the monitoring/readout FPGA. In addition the number of PIT monitoring counters was doubled (324) and the readout formatting unit was adapted to accommodate the additional PIT bus data words required in the readout/monitoring event format.

VI. The CTP Monitoring Module

The CTPMON module decodes the 160 PIT bus signals and selects trigger inputs that are to be monitored. It then builds a histogram with 3564 entries for each of the 160 decoded PIT signals, in order to monitor them on a bunch-by-bunch basis. This functionality requires a large number of on-chip memory blocks and is implemented in 4 large Altera Stratix FPGAs (EP1S80).

The firmware of the PIT bus interface FPGA was modified to include DDR input registers, but unfortunately the memory resources of the histogramming FPGAs were not sufficient to increase the number of signals being monitored. Therefore we decided to implement a simple selection mechanism in the PIT bus interface FPGA which allows selecting 160 of the 320 trigger inputs for monitoring.

VII. Test Results

After an extensive verification phase using simulation and static timing analysis, the modified FPGA firmware was loaded onto one of the reference CTP systems and tested. Slightly adapted versions of the system test programs from the software framework developed for diagnostics and operation of the CTP [5] were used for this purpose. These test programs allow sending arbitrary data patterns from the test memories on the CTPIN modules and checking the various monitoring buffers and counters on the CTPIN, CTPMON and CTPCORE modules against the calculated values. In order to determine the timing margins we also measured the timing window where the PIT bus data could be safely latched on the CTPCORE and CTPMON modules. This was done by scanning the programmable clock delays available on the CTPIN and CTPCORE modules and checking the correct operation using the test programs mentioned above. The concept is illustrated in Figure 9 below.

The valid data window for latching the PIT bus signals at the CTPMON input was measured to be 65% (8 ns) of the clock half-period (12.5 ns) and 70% (9 ns) at the CTPCORE input. Timing variations between the three CTPIN modules were small, on the order of 1 ns. The trigger latency has increased to 7 BC, due to the DDR input and output registers that had were added in the FPGAs.

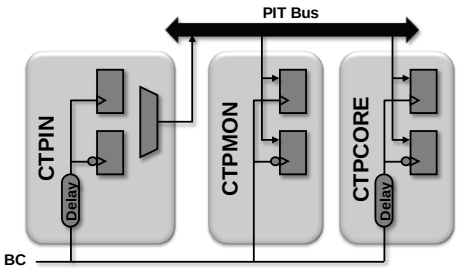

Figure 9: PIT bus timing scan

VIII. Summary

We have presented an upgrade of the ATLAS CTP which increases the number of useable trigger inputs from 160 currently to 320 by operating the PIT bus backplane at 80 MHz using DDR signaling. This was feasible because the PIT bus backplane was carefully designed, and the FPGAs on the CTPIN and CTPCORE modules are relatively recent and have sufficient spare resources.

The basic functionality of the CTP has been maintained, there are however some limitations:

- The CTPMON can only monitor 160 of the 320 PIT signals due to limited FPGA memory resources.
- The mapping of the trigger input signals to the LUT inputs on the CTPCORE using the switch matrices on the CTPIN modules is somewhat less flexible since trigger inputs need to be allocated in pairs.
- The latency has increased from 4 to 7 BC, although it may be possible to reduce this to 6 BC.

The CTP upgrade presented here could even be of interest before the first phase of the LHC luminosity upgrade, since already now all 160 PIT bus signals are allocated, so there is no headroom for potential additional trigger inputs.

IX. References

[1] The ATLAS Collaboration, "*The ATLAS Experiment at the CERN Large Hadron Collider*", JINST 3 (2008) S08003.

[2] S. Haas et al., "*The ATLAS Level-1 Muon to Central Trigger Processor Interface*", Topical Workshop on Electronics for Particle Physics, CERN-2007-007, November 2007.

[3] R. Spiwoks et al., "*The ATLAS Level-1 Central Trigger Processor (CTP)*", 11th Workshop on Electronics for LHC and Future Experiments, CERN/LHCC/2005/038 265, November 2005.

[4] S. Ask et al., "*The ATLAS Central Level-1 Trigger Logic and TTC System*", JINST 3 (2008) P08002.

[5] R. Spiwoks et al., "*Framework for Testing and Operation of the ATLAS Level-1 MUCTPI and CTP*", these proceedings.