A Self Triggered Amplifier/Digitizer Chip for CBM

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Abstract

The development of front-end electronics for the planned CBM experiment at FAIR/GSI is in full progress. For charge readout of the various sub-detectors a new self-triggered amplification and digitization chip is being designed and tested.

The mixed signal readout chip will have 32-64 channels each containing a low-power/low-noise preamplifier/shaper front-end, an 8-9 bit ADC and a digital post-processing based on a FIR/IIR-filter. The ADC has a pipeline architecture that uses a novel current-mode storage cell as a basic building block.

The current prototype provides 26 different parametrized preamplifier/shaper/discriminator channels, 8 pipeline ADCs, a readout shift register matrix and a synthesized redundant signed binary (RSD) decoder.

I. Introduction

The fixed target Compressed Baryonic Matter (CBM) experiment is one of several heavy-ion experiments being built within the planned accelerator expansion FAIR (Facility for Antiproton and Ion Research) at Gesellschaft für Schwerionenforschung (GSI) in Darmstadt, Germany [1]. A superconducting synchrotron double ring accelerator (STS100/300) with 1.100 m circumference will be the heart of FAIR whereas the existing GSI accelerators UNILAC and SIS18 will serve as an injector. The two synchrotron rings will produce pulsed beams of up to 2.7 GeV/u for U^{28+}, 29 GeV for protons (SIS100) and 34 GeV/u for U^{92+} (SIS300) [8]. In the photo-montage below (fig. 1), the SIS double ring structure is shown in the upper right corner, the already existing GSI facilities are on the left (white-gray structures).

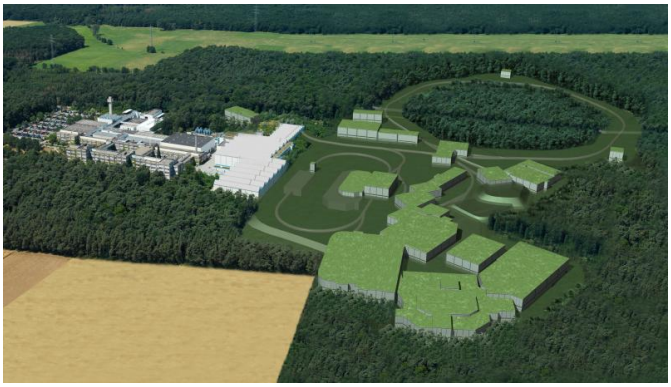

Figure 1: Photo-montage of the facility expansion FAIR at GSI [1]

The physical goal of the CBM experiment is to investigate highly compressed nuclear matter produced in direct nucleus-nucleus collisions. More precisely, one aims to explore the “deconfinement” phase transition in the QCD phase diagram from hadronic matter to quark-gluon matter that takes place at temperatures of about 170 MeV [2]. The first experiments at FAIR are scheduled to start in 2014, the complete facility is expected to be finished in 2016.

The CBM detector concept comprises of several different sub-detector types that must be able to deliver precise tracking and timing measurements and to allow for reliable particle identification. Among other sub-detectors, a Silicon Tracking System (STS) built of silicon strip-sensors will be used as main tracking device and a Transition Radiation Detector (TRD) will separate electrons from pions and also track charged particles. Since from simulations one expects nucleus-nucleus interaction rates of about 10 MHz with each event producing up to 1000 charged particles [9], the demands on the different sub-detectors, the front-end electronics and the data acquisition (DAQ) in terms of data-rates and radiation-tolerance are high.

For both, STS and TRD, high-rate, low-power and low-noise readout ASICs are needed. Since the Poisson distributed collisions between the nuclei are not correlated to a global trigger signal, the readout ASICs for both detectors as well as the complete DAQ must be self-triggered. Besides other groups that pursue different approaches (e.g. a low-power, moderate resolution, time-over-threshold front-end design from AGH [3]), we have joined the CBM collaboration and started a new front-end readout chip development in 2006.

In this paper we will describe the current status of our work on the front-end readout electronics and especially the results we have as yet achieved with our last prototype. Moreover we sketch our concept for the first complete readout ASIC, that will integrate on one die 32-64 channels each performing the analog amplification, shaping and digitization as well as some digital filtering, hit detection and data reduction. We intend to submit the new readout chip in the end of 2010.

II. Prototype Architecture

A. Design Overview

Our current prototype chip is sized 3.2 x 1.5 mm² and has been fabricated in the UMC 0.18 µm 1P6M technology. One die carries 26 charge sensitive amplifier channels, 8 pipeline

ADCs, a shift register matrix of 5.3 kbit, two synthesized control/decoder blocks and different test and calibration circuits. 12 current DACs with 7 bit resolution allow for internal bias generation.

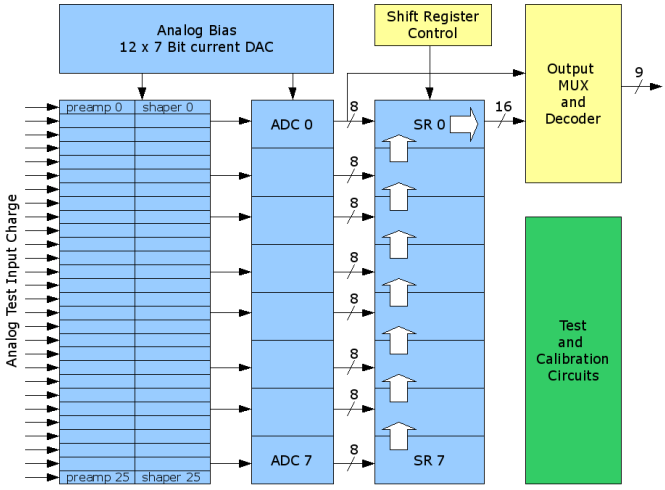

Figure 2: Block-diagram of latest prototype

As sketched in fig. 2, the 8 ADCs are connected to 8 different amplifier channels. The readout concept is to continuously run the ADCs which as well continuously write their digital output results into the corresponding subsequent shift register sub-blocks. During conversion phase, all ADC sample values older than 42 sample steps are thereby discarded, since the length of the shift registers is limited to 42 bits.

If an internal or external trigger signal occurs, all 8 shift register sub-blocks are connected in series (white arrows in fig. 2) and the whole data is shifted to the output decoder logic where it is further processed (redundant binary to "normal" binary decoder [6]) and afterward passed to the outer world. Since this oscilloscope-like methodology causes long dead-times, it will of course not be feasible for the final readout chip, but in the current prototype it significantly decreases the digital logic area, the number of necessary output pins and the overall data-rates.

The shift register matrix is build using two dynamic 3T D-RAM cells per register bit. For calculating the total amount of 5.3 kbit, one must consider that each ADC produces 2 x 8 bit (time-multiplexed) per sampling step: 8 ADCs x (16 bit / sample * ADC) x 42 samples (shift register length).

B. Layout

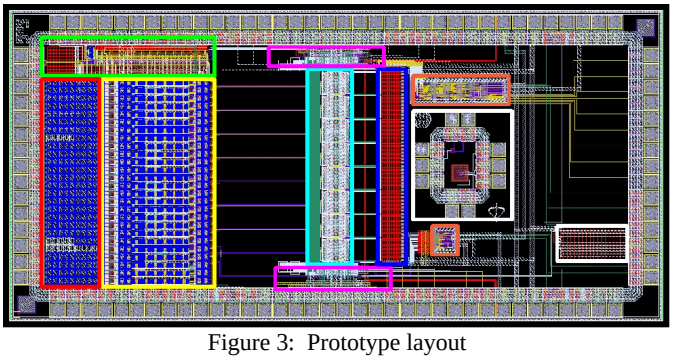

Figure 3: Prototype layout

Figure 3 shows the complete chip layout. The die has a total of 110 pads sitting on a 80 µm pitch. The 26 preamplifier/shaper channels are marked yellow. In the red box are the metal-metal capacitors that are connected to the amplifier inputs as a replacement for a "real" external detector capacitance. The bias circuitry of the amplifier channels including the 12 DACs is highlighted green. Framed in light blue are the 8 pipeline ADCs. Its bias structures and some hand-made control logic is marked pink. The blue box surrounds the 5.3 kbit shift register matrix. Both synthesized blocks are orange-colored, the upper one provides the output control and decoder logic while the lower one switches the shift register matrix and the ADCs. The different test structures are bordered white.

C. Amplifier/Shaper Channels

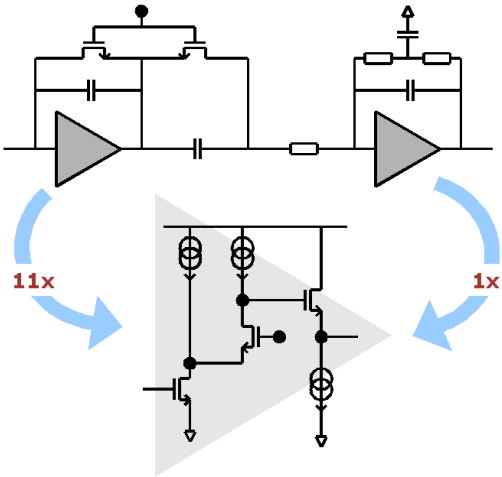

Figure 4: Simplified preamplifier/shaper schematic

As sketched above (fig. 4), each amplifier channel basically consists of a single-ended preamplifier with NMOS input and a pole-zero cancellation feedback, a 2nd order T-feedback shaper (82 ns shaping-time) and a comparator (not shown) with LVDS output. The preamplifiers of the different channels were realized with varied design parameters to figure out what the lowest possible noise values are and how they can be achieved. In particular, due to the high impact of the input NMOS on the overall noise characteristics of the whole preamplifier, 3 different types of input NMOS were used within the different channels: normal (NMOS with triwell, minimal gate length), no-triwell (NMOS without triwell, minimal gate length) and long (NMOS with triwell, non-minimal gate length).

For both, preamplifier and shaper, a unified amplifier cell was used several times. By choosing a certain number of amplifier cells for the preamplifier during design phase, one can easily optimize the tradeoff between power consumption and amplifier noise for a given detector capacitance. In the final chip the total number of amplifier cells will be configurable/switchable to be able to individually adjust the power and noise characteristics of the preamplifier to the actual detector capacitance.

Furthermore a special injection cell was included in every channel that provides 3 different ways for injecting test

charges. The whole channel block was layed out by hand and covers about 40 x 540 µm².

D. Pipeline ADC

The current-mode pipeline ADCs have 8 pipeline stages and therefore generate 9 bit per conversion step at a maximum speed of 24 MSamples/s. Each ADC produces a raw data stream of 400 Mbit/s that is fed into the storage matrix and decoded afterward. The ADC realizes the popular 1.5 bit algorithmic conversion technique which adds some redundancies into the output data for the benefit of relaxing the accuracy requirements of the comparator but for the costs of an additional redundant binary to binary decoder [7].

The probably most challenging building block of an algorithmic ADC in general is the multiplication unit. In our design a novel current storage cell, as it is sketched below (fig. 5), was used to perform a multiplication by two. This is actually done by copying the input current twice into two different copy cells and by connecting both cells together afterward to finally produce the doubled input current.

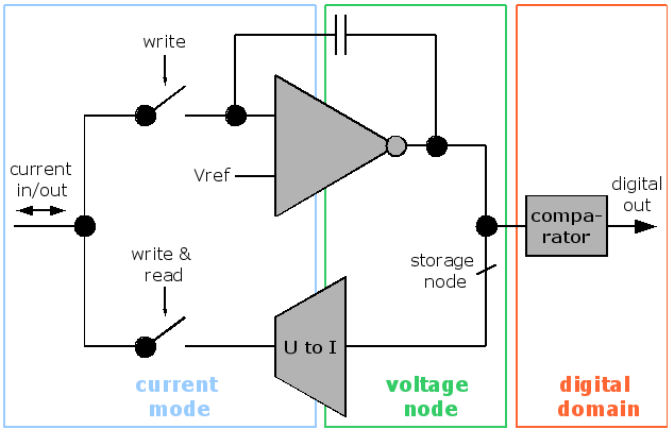

Figure 5: Novel current copy cell

The basic principle of the current copy cell (cp. again fig. 5) is to integrate the input current onto the feedback capacitance (upper part of the loop) while concurrently reconverting the output voltage of the integrator back to a current (lower part of the loop) as long as the input current and the reconverted current are unequal. If at any time both currents exactly cancel each other, an equilibrium is reached and the primary input current can easily be stored just by opening both write switches (fig. 5). To read out the stored current again only the (lower) read switch must be closed.

The offset correction also required during each algorithmic conversion is done by enabling or disabling some additional current sources that are directly integrated into the current copy cell.

III. Test Setup

The prototype chip was directly bonded to a PCB that also carries the bias circuitry, some LVDS buffers, level shifters and different connectors. The PCB itself is mounted on a Xilinx Spartan FPGA board that provides all necessary infrastructure for FPGA programming and data exchange via USB with a PC. An impression of the test setup is shown below (fig. 6).

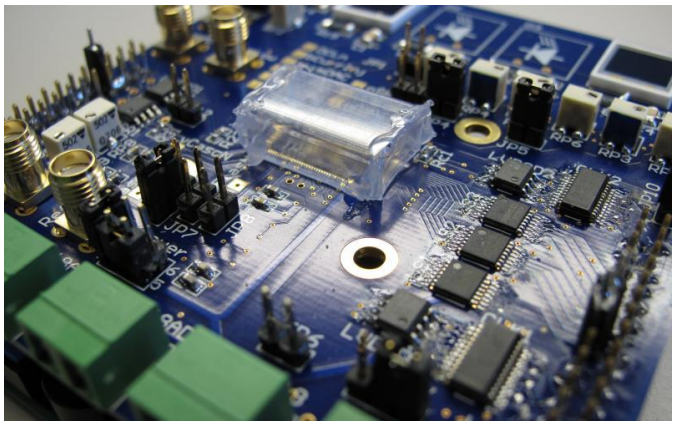
Figure 6: Test setup: The die is directly bonded to the PCB

IV. Prototype Results

A. Measurements of Amplifiers/Shapers

Well-known test charges can easily be injected into the amplifier inputs by using a calibrated internal injection capacitance. The pulse shapes of both the preamplifier and the shaper outputs can be studied qualitatively with a monitor bus, for precise noise values the discriminators within the channels are used to perform s-curve scans.

What is not shown here, the overall pulse shapes and the general amplifier/shaper behavior matches nearly perfectly the simulation (output pulse peaking-time about 95 ns) and therefore satisfies our expectations, whereas unfortunately the measured noise does not, as the following overview (fig. 7) shows.

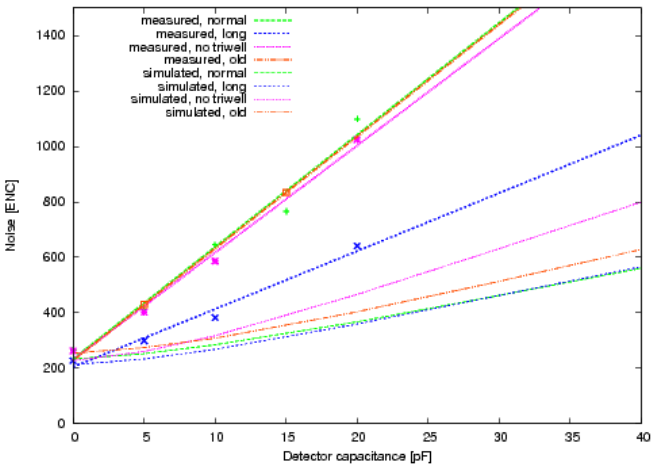

Figure 7: Preamplifier noise vs. detector capacitance

To obtain these results many noise measurements have been performed. In particular, the equivalent noise charge (ENC) had to be extracted from measured s-curves of the different channels (different input NMOS types) while connecting different capacitive loads.

From the graphic it is apparent, that although the noise offset (at 0 pF detector capacitance) is for all simulations and

measurements at about 200 e ENC, the measured slopes of the different channel versions differ significantly from both simulation and each other.

The most important result here is that hardly any variation of the input NMOS type did have a significant impact on the measured noise, whereas using a longer input NMOS with a non-minimal gate length caused a dramatic decrease of the noise slope by a factor of about 2. Even through many different theories were made and many different sophisticated simulations including extracted post-placement simulations were performed, neither the difference of the noise values between the long and the normal channels nor the absolute deviation of all noise values from simulation could really be understood yet. Further investigations are ongoing.

Nevertheless the long channel has a measured noise of about 800 e ENC for a 30 pF detector capacitance while consuming only 3.6 mW and therewith already satisfies the project requirements.

B. Measurement of Pipeline ADC

We have measured many ADC transfer characteristics with DC inputs at a conversion speed of 24 MSamples/s and a corresponding clock frequency of 200 MHz, an exemplary result is shown below (fig. 8).

Besides demonstrating the proper operation of the ADCs itself, the successful measurements of the characteristic ADC curve also implicitly proves the proper operation of all involved readout components (shift register matrix, control blocks, redundant signed binary decoder, etc.).

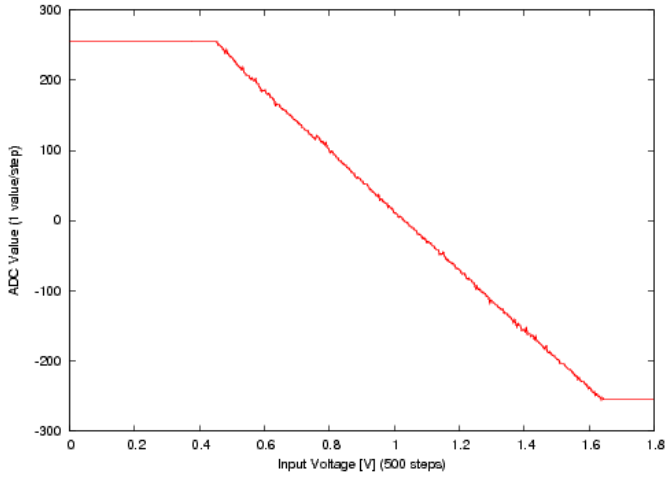

Figure 8: ADC transfer characteristic at 24 MSamples/s

Based on the evaluation of the differential non-linearity (DNL), the best measurements of the 9 bit design so far give an effective resolution of 7-8 bit, what has actually approximately been predicted by simulation. Thereby the ADC only consumes 4.5 mW at a conversion speed of 24 MSamples/s and covers just about 130 x 120 µm² chip area.

C. System: Amplifier/Shaper + ADC

Since, as described above, some shaper outputs can be connected to ADC inputs, shaper pulses can directly be digitized on-chip. For the following plot (fig. 9) 1000 hits have been recorded in this way.

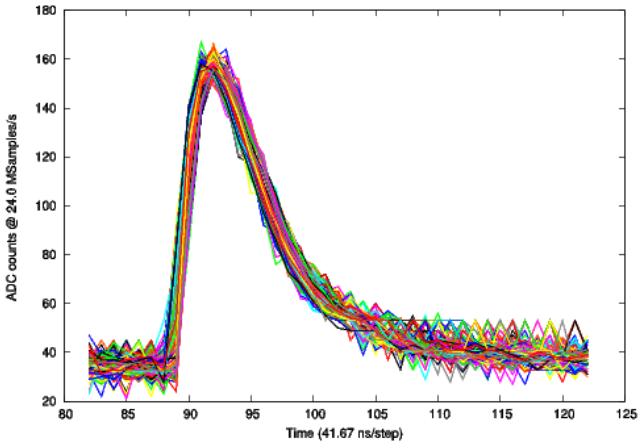

Figure 9: Overlay of 1000 shaper output pulses digitized with on-chip ADC at 24Msamples/s

Since the measured shaper noise (at 5 pF input load) is smaller than one last significant bit (LSB) of the ADC, the observable disturbance here is only caused by ADC noise.

In general, by increasing the overall front-end gain, one could easily scale the shaper noise levels to the same scale as the ADC noise levels, at least as long as the needed dynamic range is not limiting. This will of course be considered in the final readout chip design.

From a theoretical point of view, the impulse response of the 2nd order shaper should be of the type (x/T^2) * exp(-x/T) and indeed fitting the digitized data in this way gave very good agreement.

D. Summary Table

The following table summarizes the most important characteristics of the prototype ASIC.

Chip Technology	UMC 0.18 µm, 1P6M, MiMCaps
Chip Area	1.5 x 3.2 mm²
Channel / ADC Area	40 x 540 / 130 x 120 µm²
Number of Channels / ADCs	26 / 8
Power per Channel / ADC	3.8 / 4.5 mW
Shaper Noise (ENC)	200 e + 20 e / pF
Shaper Peaking-Time	95 ns
ADC Resolution	7-8 bit effective
ADC Speed	24 MSamples / s

V. Outlook: Complete v1.0 ASIC

A. Design Concept

The next milestone is to build the complete version 1.0 chip, that will have 32 mixed signal channels each consisting of an amplifier, an ADC and a post-processing including for example an IIR/FIR-filter, a digital hit detector and a simple

data compression unit. Moreover a 1-2 GBit LVDS transmitter cell and simple protocol encoder are intended. A very first draft of the conceptual block diagram is shown below (fig. 10).

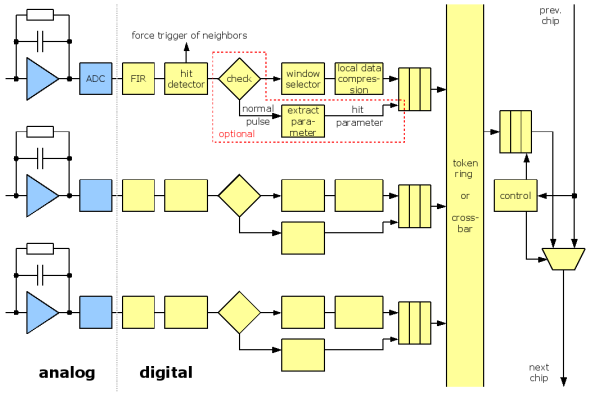

Figure 10: Preliminary block diagram of the first complete chip

Furthermore, a hit parameter extraction unit that evaluates information as for example the hit amplitude is currently in discussion.

At present a token ring network seems to be the most simple and evenhanded solution to connect the channel outputs with the digital processing and transmission unit.

To save transmission bandwidth it is intended to connect several chips with lower load (due to a lower event rate) to enable them to share one LVDS transmitter via a simple serial round-robin protocol.

B. Radiation Tolerance

Calculations estimate the whole readout electronics to be exposed to radiation doses between 1 krad (time of flight detector) and 20 Mrad (first STS layer) [4] what in general demands for special circuit techniques feasible to increase the radiation-tolerance of both digital and analog chip parts. In our case, extensive investigations from GSI have shown the UMC 0.18 µm technology to be per se sufficiently radiation-tolerant up to a certain limit while showing very good annealing characteristics [5]. For this reason, the usage of special radiation hardening techniques is yet not intended.

C. Preliminary Floor-plan

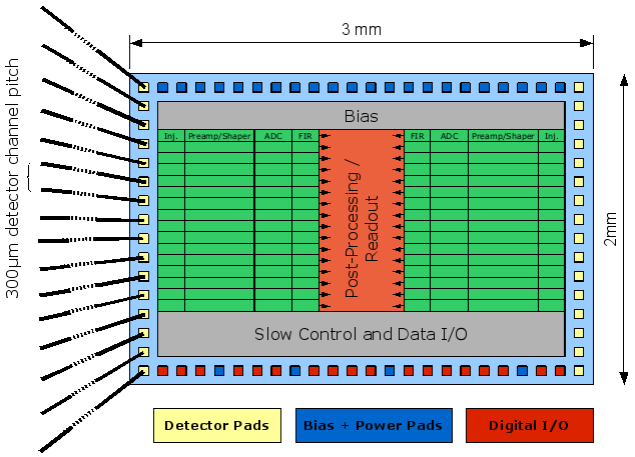

Figure 11: Preliminary floor-plan

A preliminary floor-plan concept is shown in the graphic above (fig. 11). The about 3 x 2 mm² sized die will have a separated bias circuitry, two symmetric 16-channel blocks, a centered digital processing area and a digital slow-control and I/O unit. The 32 detector channels will be wire-bonded to both the left and the right side to relax the overall pitch proportions.

VI. Conclusions

With the successful measurement of the low-noise and low-power analog preamplifier/shaper circuits on the one hand and the small low-power 7-8 bit ADCs on the other hand, we have conceptually finished the whole analog front-end and therefore reached an important milestone, even if several refinements certainly still have to be scheduled.

Moreover, as we have shown, we already have an overall design concept how the first complete readout chip should be realized and due to the effective cooperation with the different detector and physics groups, the final specification will soon be completed.

The submission of the complete readout ASIC is scheduled to the end of 2010.

VII. Acknowledgment

This work has been conducted using tools from Cadence Design System. We appreciate the support and the opportunities we got from our participation in the Cadence Academic Network.

VIII. References

[1] The Facility for Anitproton and Ion Research (FAIR) project website: http://www.gsi.de/fair

[2] The Compressed Baryonic Matter (CBM) experiment website: http://www.gsi.de/fair/experiments/cbm

[3] K. Kasiński, P. Gryboś, R. Szczygieł “TOTO1 ASIC – First Results”, 14th CBM CM Split, Croatia, October 2009

[4] W.F.J. Müller “Radiation Doses in CBM - A first estimate and an assessment of consequences”, 11th CBM CM at GSI, Germany, February 2008

[5] S. Löchner “Radiation studies on the UMC 180 nm CMOS process”, CBM Progress Report 2008

[6] S.M. Yen, C.S. Laih, C.H. Chen, and J.Y. Lee “An Efficient Redundant Binary Number to Binary Number Converter”, IEEE Journal of Solid State Circuits, Vol. 27, No. 1, pp. 109-112, Jan 1992.

[7] J.S. Wang, C.L. Wey, “A 12-bit 100-ns/bit 1.9-mW CMOS Switched-Current Cyclic A/D Converter”, IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 5, May 1999, pp: 507

[8] H.H. Gutbrod at al, FAIR Baseline Technical Report 2006, Executive Summary, ISBN 3-9811298-0-6

[9] V. Friese, W.F.J. Müller, P. Senger “The CBM experiment at FAIR”, CBM Progress Report 2008